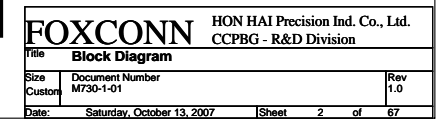


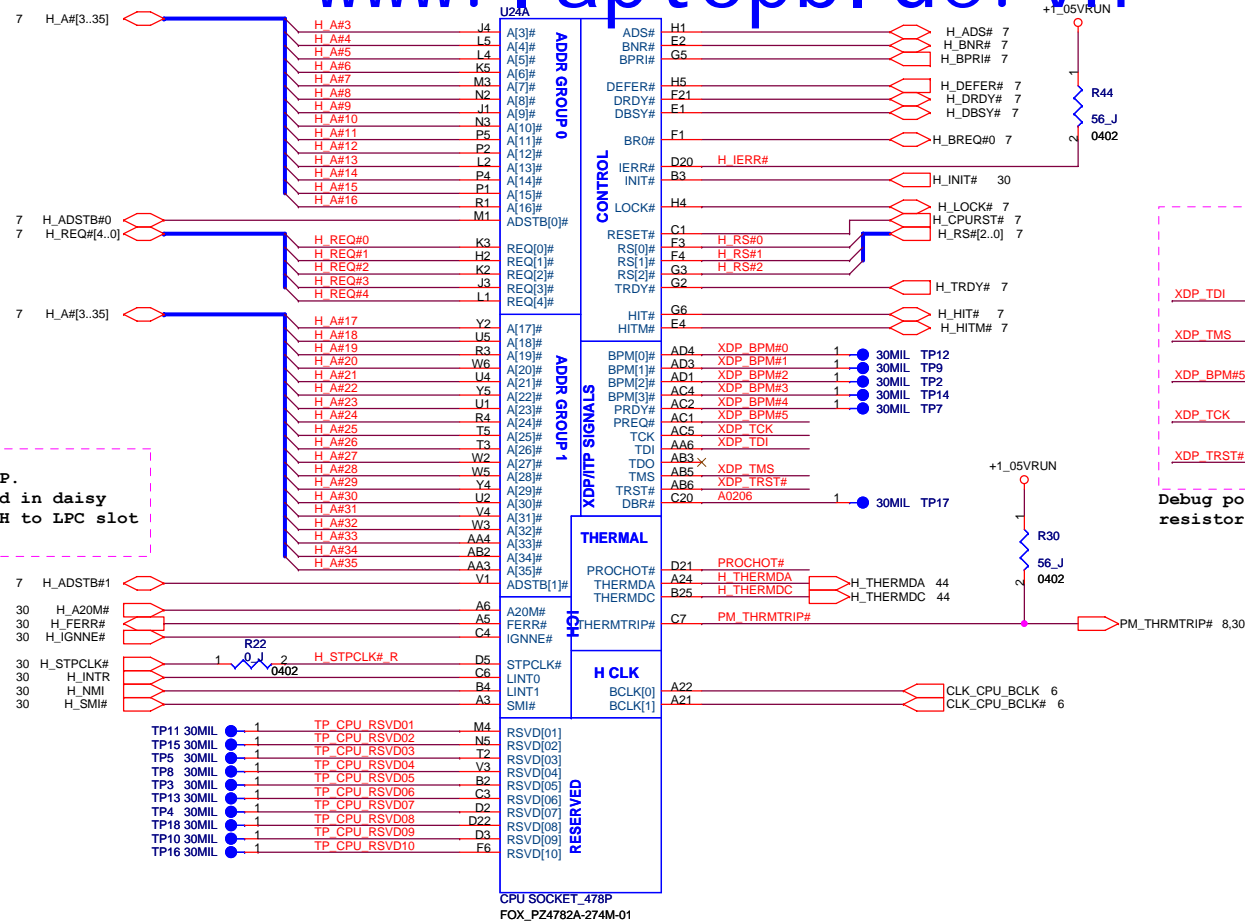
Schematics Page Index (Title / Revision / Change Date)								
Page	Title of Schematics Page	Rev.	Date	Page	Title of Schematics Page	Rev.	Date	
01	Index page	1.0	07'10/19	36	Flash ROM/XBUS	1.0	07'10/19	
02	Block Diagram	1.0	07'10/19	37	Mini-PCIE Card	1.0	07'10/19	
03	Merom(HOST BUS) 1/3	1.0	07'10/19	38	FeliCa/MDC	1.0	07'10/19	
04	Merom(HOST BUS) 2/3	1.0	07'10/19	39	EXPRESS	1.0	07'10/19	
05	Merom(Power/Gnd) 3/3	1.0	07'10/19	40	AUDIO(CODEC/POWER) 1/4	1.0	07'10/19	
06	CLOCK GEN	1.0	07'10/19	41	AUDIO( AMP/HP/SPK) 2/4	1.0	07'10/19	
07	Crestline (HOST) 1/7	1.0	07'10/19	42	AUDIO( EXTMIC) 3/4	1.0	07'10/19	
08	Crestline (DMI) 2/7	1.0	07'10/19	43	AUDIO(MUTE) 4/4	1.0	07'10/19	
09	Crestline (GRAPHIC) 3/7	1.0	07'10/19	44	FAN/Thermal-Sensor	1.0	07'10/19	
10	Crestline (DDRII) 4/7	1.0	07'10/19	45	PCI (PCI BUS) 1/3	1.0	07'10/19	
11	Crestline (POWER,VCC) 5/7	1.0	07'10/19	46	PCI (i.LINK) 2/3	1.0	07'10/19	
12	Crestline (VCC CORE) 6/7	1.0	07'10/19	47	PCI (SD/MS-DUO) 3/3	1.0	07'10/19	
13	Crestline (VSS) 7/7	1.0	07'10/19	48	USB2.0	1.0	07'10/19	
14	DDRII(SO-DIMM_0) 1/3	1.0	07'10/19	49	LAN (88E8039)	1.0	07'10/19	
15	DDRII(SO-DIMM_1) 2/3	1.0	07'10/19	50	LAN Transformer	1.0	07'10/19	
16	DDRII(Termination) 3/3	1.0	07'10/19	51	Touch/Lid/LED	1.0	07'10/19	
17	VGA(PCI-E)	1.0	07'10/19	52	Power Bottom & USB Board	1.0	07'10/19	
18	VGA(STRAP)	1.0	07'10/19	53	Power Design Diagram	1.0	07'10/19	
19	VGA(GDDR)	1.0	07'10/19	54	DCIN&Charger	1.0	07'10/19	
20	VGA(MULTIUSE)	1.0	07'10/19	55	SYS Power (+3_3V/+5V)	1.0	07'10/19	
21	VGA(LVDS/VDAC )	1.0	07'10/19	56	SYS Power(+1_5V/+1_05V)	1.0	07'10/19	
22	VRAM(GDDR)	1.0	07'10/19	57	DDR2 Power(+1_8V/+0_9V)	1.0	07'10/19	
23	VGA(POWER) 1/3	1.0	07'10/19	58	CPU Power_VHCORE	1.0	07'10/19	
24	VGA(POWER) 2/3	1.0	07'10/19	59	VGA Power(+1_2V/+1_2V)	1.0	07'10/19	
25	VGA(POWER) 3/3	1.0	07'10/19	60	Others power plane	1.0	07'10/19	
26	VRAM(BYPASS)	1.0	07'10/19	61	OVP protection	1.0	07'10/19	
27	CRT	1.0	07'10/19	62	HOLE	1.0	07'10/19	
28	LVDS	1.0	07'10/19	63	History ( 1 )	1.0	07'10/19	
29	ICH8-M( PCI/USB ) 1/5	1.0	07'10/19	64	History ( 2 )	1.0	07'10/19	
30	ICH8-M( LPC,IDE,SATA )2/5	1.0	07'10/19	65	History ( 3 )	1.0	07'10/19	
31	ICH8-M( GPIO) 3/5	1.0	07'10/19	66	History ( 4 )	1.0	07'10/19	
32	ICH8-M( POWER) 4/5	1.0	07'10/19	67	History ( 5 )	1.0	07'10/19	
33	ICH8-M( GND) 5/5	1.0	07'10/19	68				
34	SATA HDD/CD-ROM	1.0	07'10/19	69				
35	EC+KBC(3910)	1.0	07'10/19	70				

M730 Main Board		M/B P/N:	1P-0079100-8010 (FUBAI) 1P-0079500-8010 (HANSTAR) 1P-0079G00-8010 (TRIPOD)
		P/B P/N:	1P-1079100-8010 (FUBAI) 1P-1079500-8010 (HANSTAR) 1P-1079G00-8010 (TRIPOD)
		U/B P/N:	1P-1079101-8010 (FUBAI) 1P-1079501-8010 (HANSTAR) 1P-1079G01-8010 (TRIPOD)

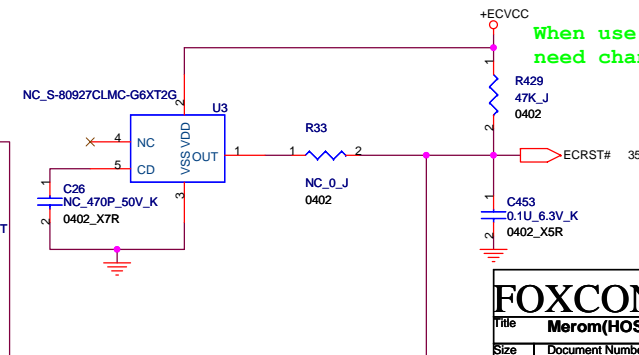
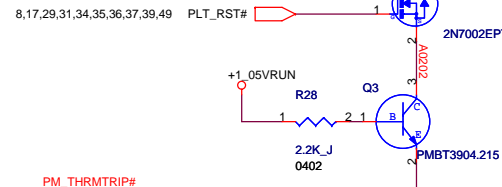
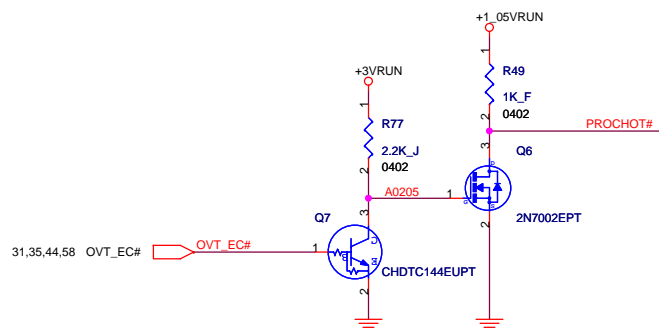
P. Leader	Check by	Design by

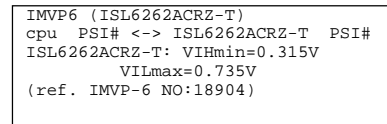
<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title Index Page		
Size A3	Document Number M730-1-01	Rev 1.0
Date: Saturday, October 13, 2007 Sheet 1 of 67		

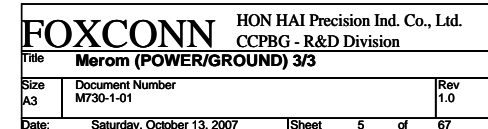


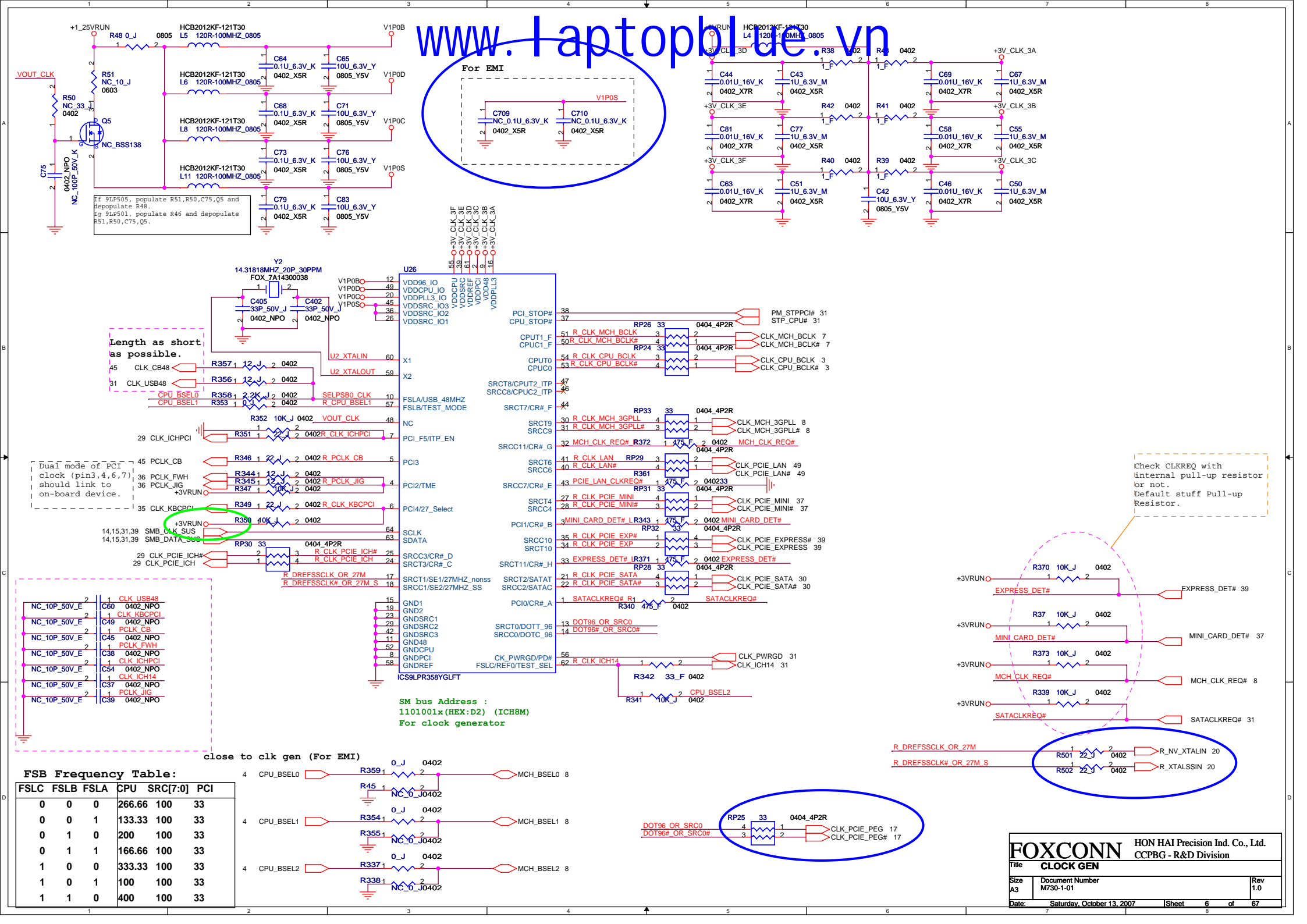


ICH8M's GPIO12: VIL---> -0.5V ~ 0.8V  
VIH---> 2.0V ~ 3.3+0.5V  
MEROM's PROCHOT#: VIL---> -0.1V ~ 0.3\*VCCP  
VIH---> 0.7\*VCCP ~ VCCP+0.1

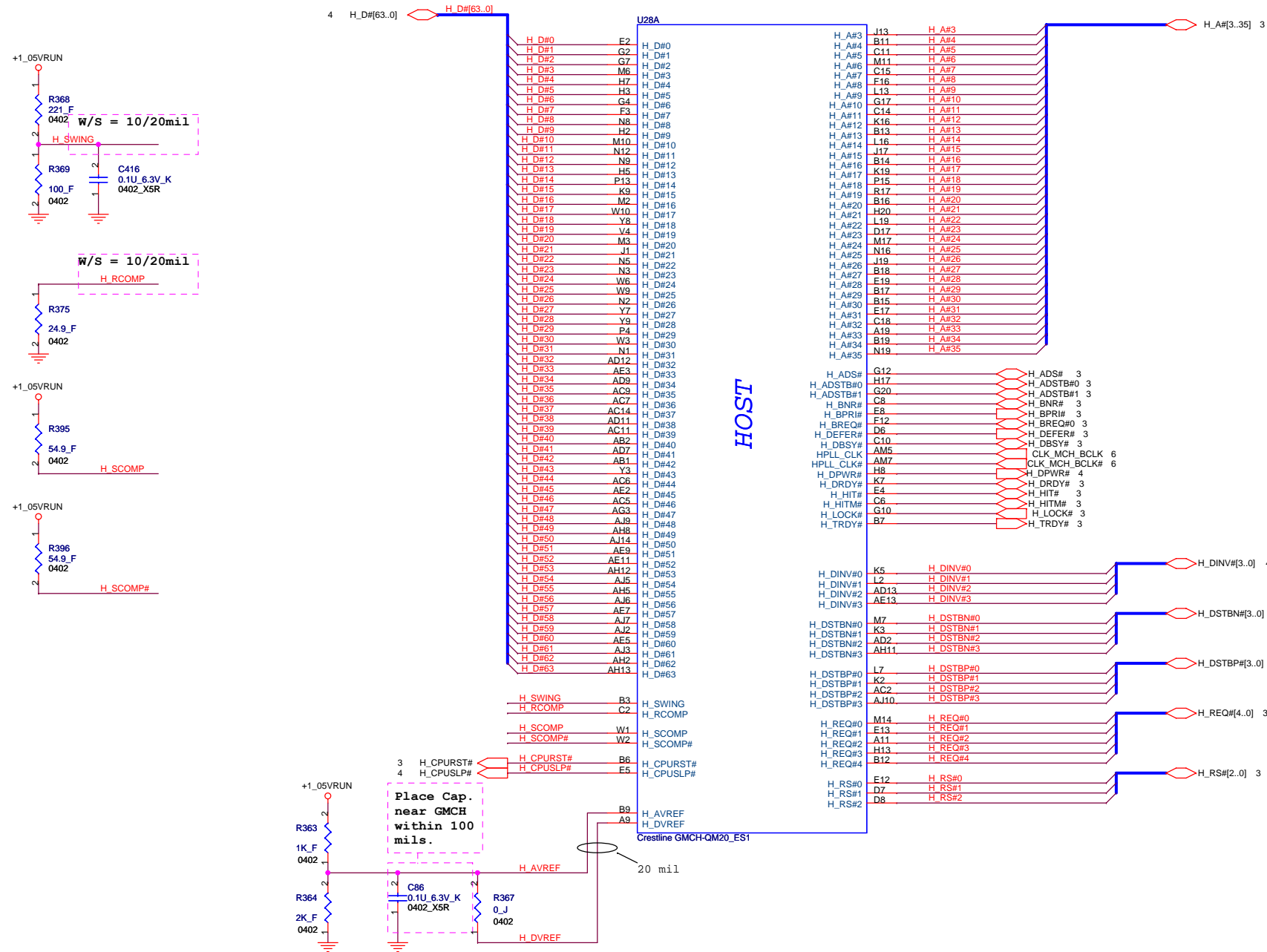


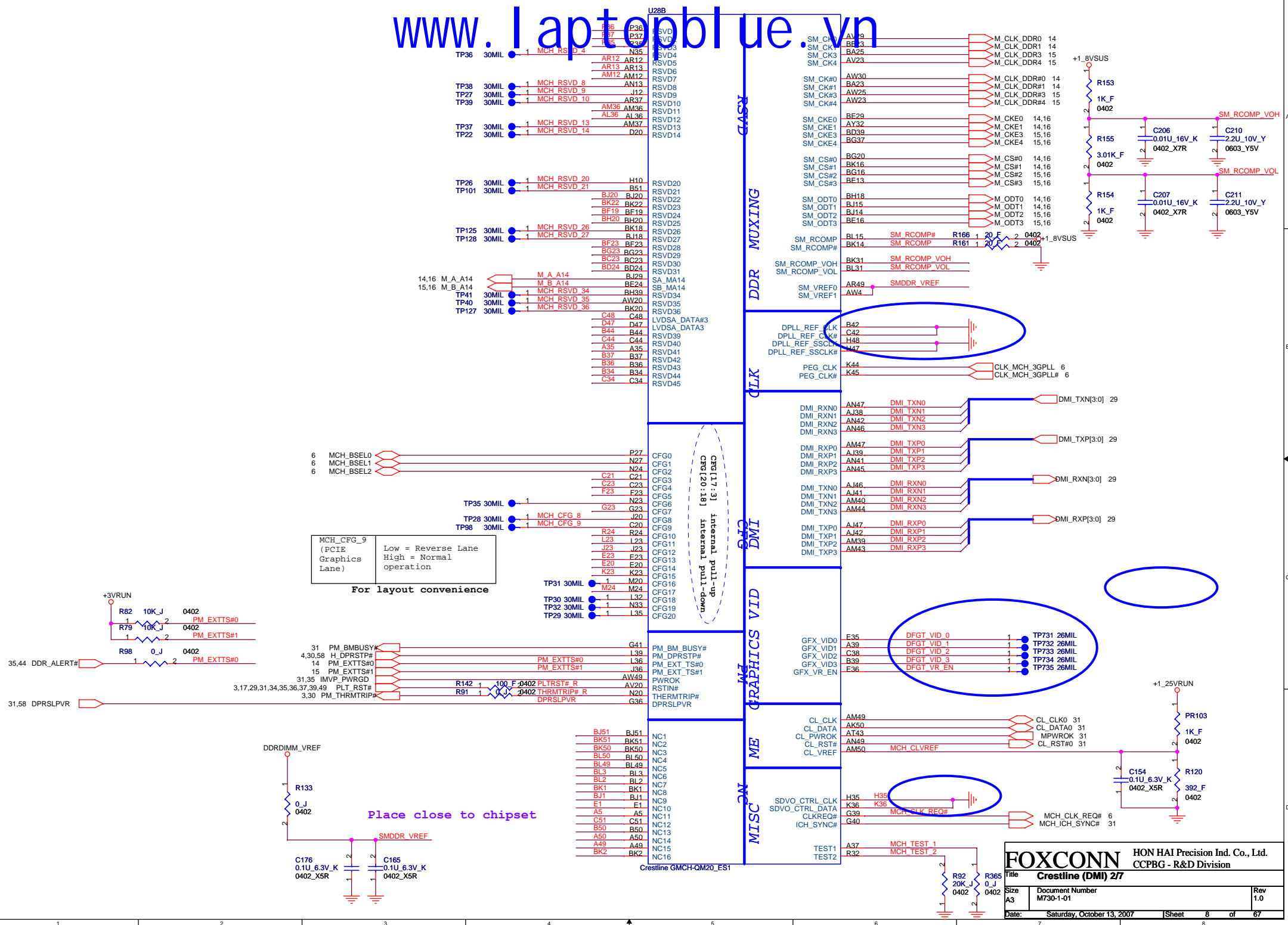




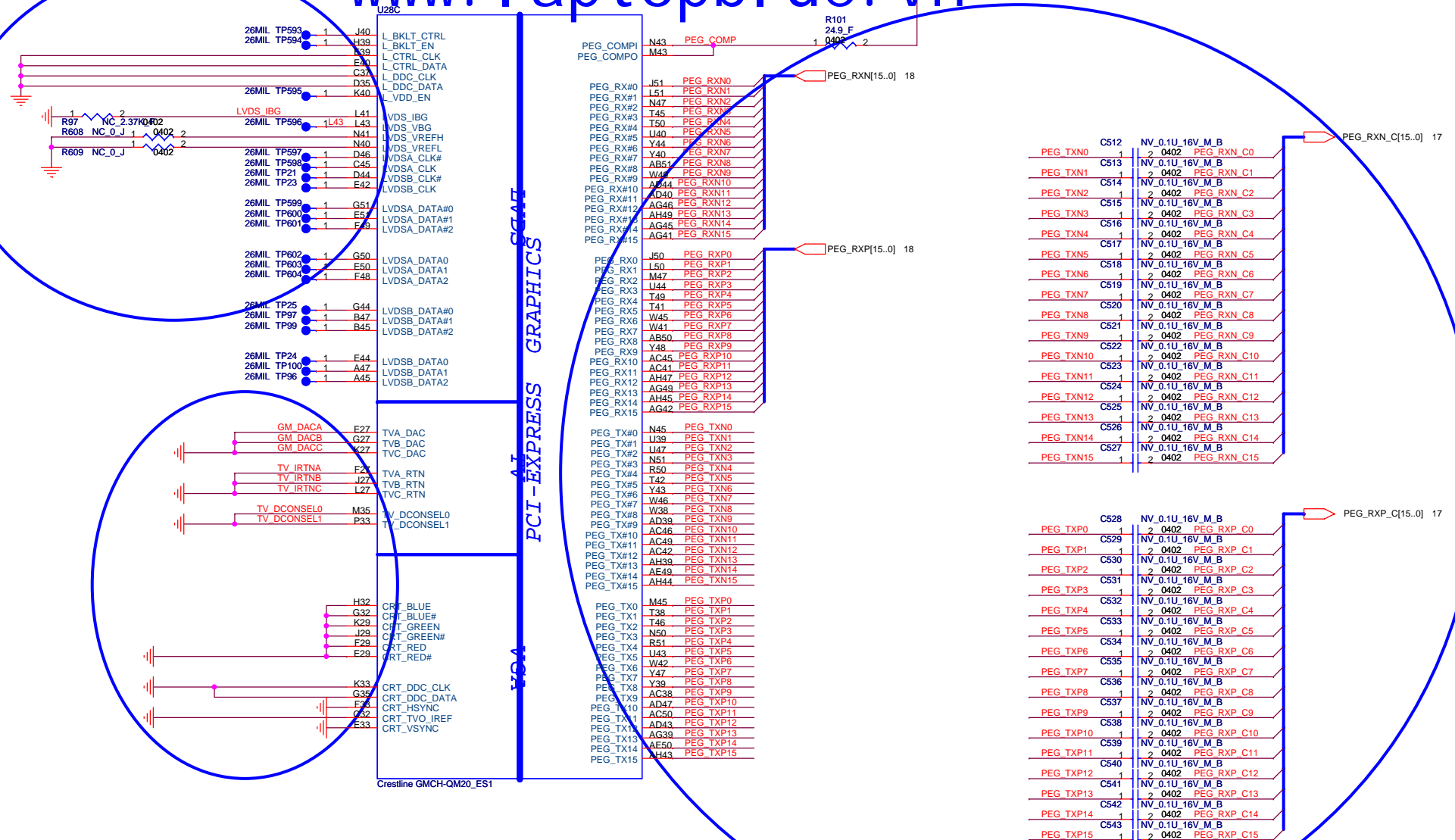


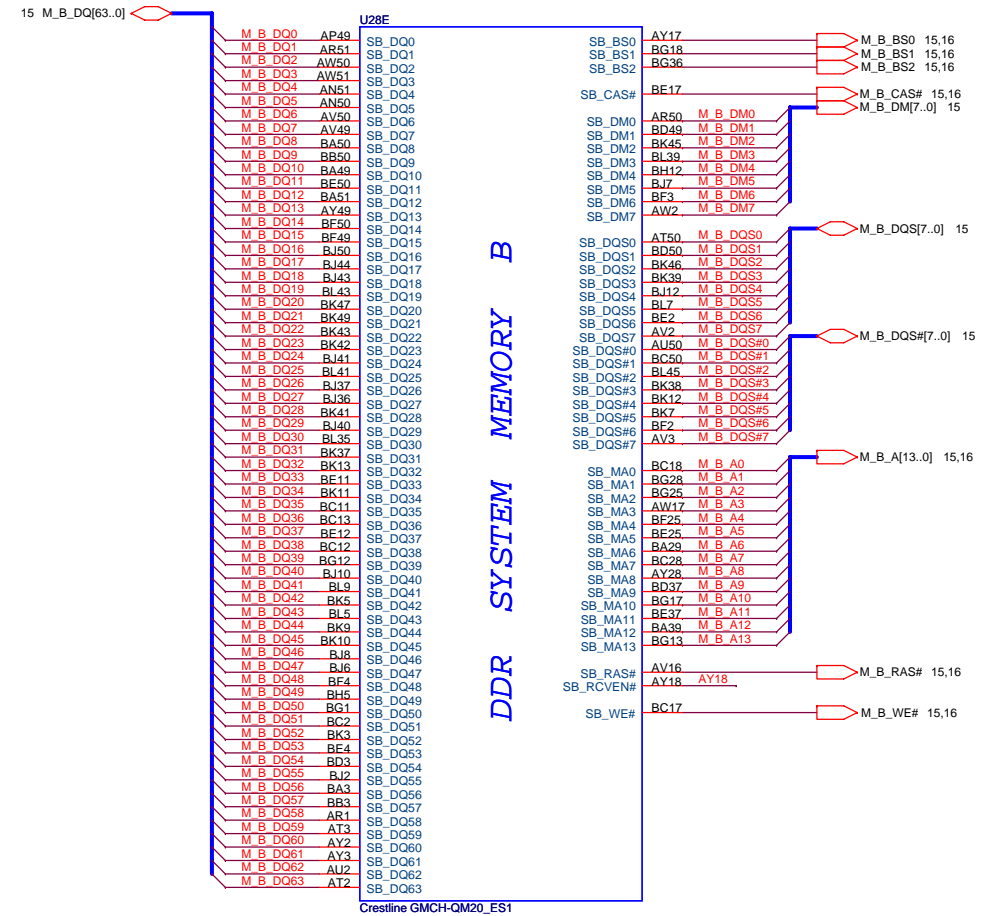
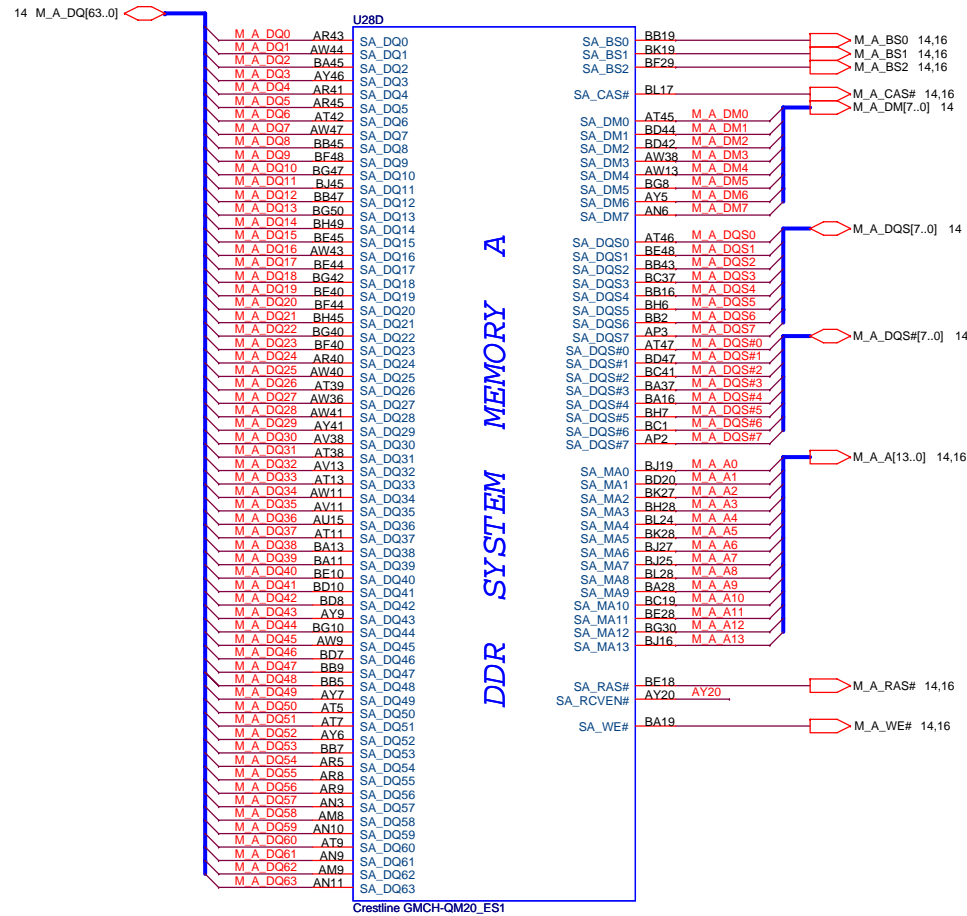




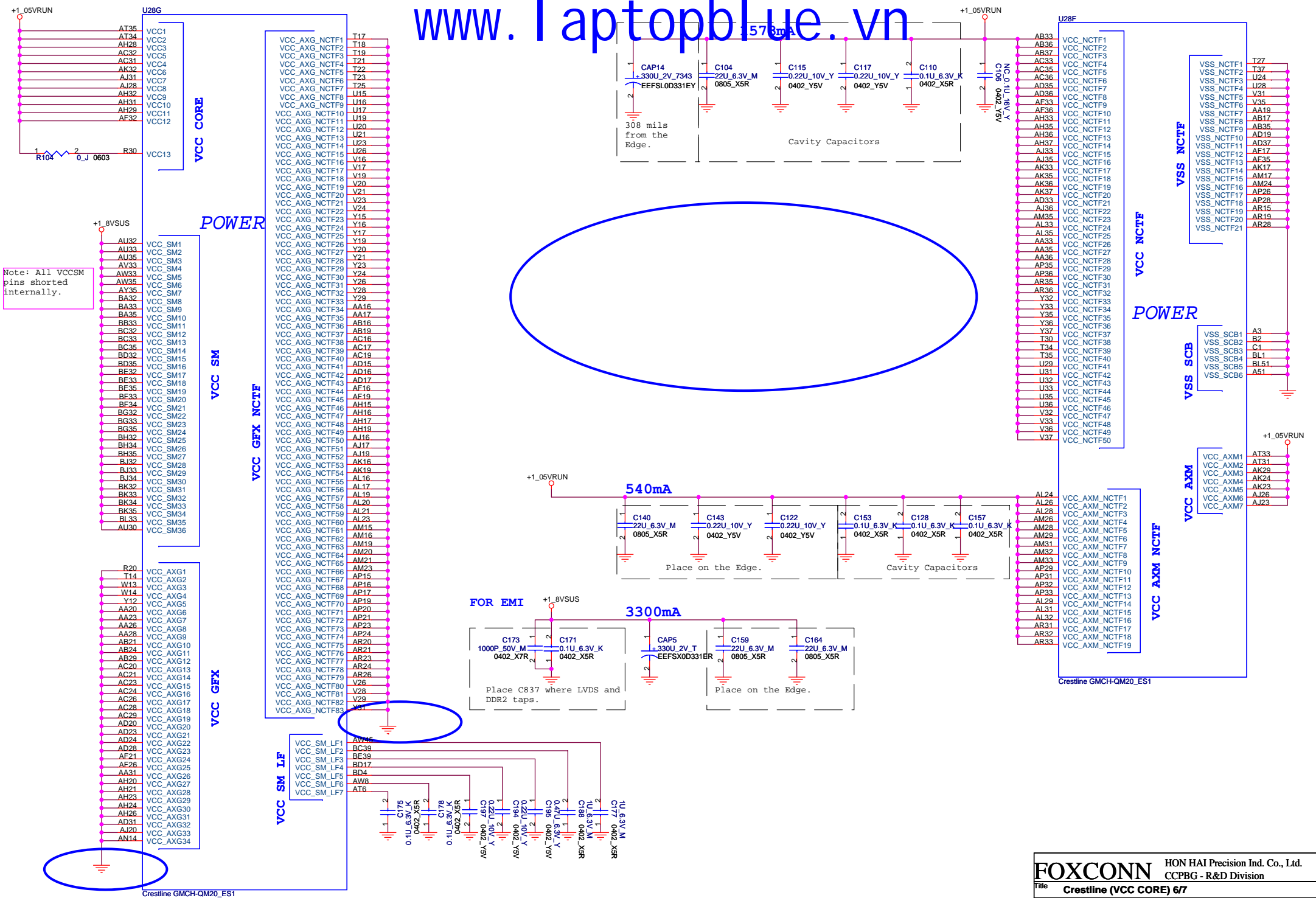








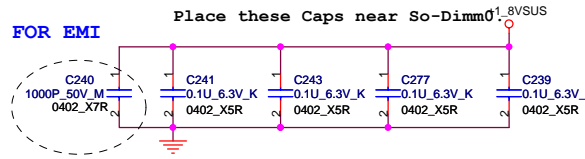
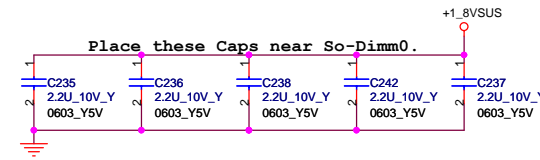
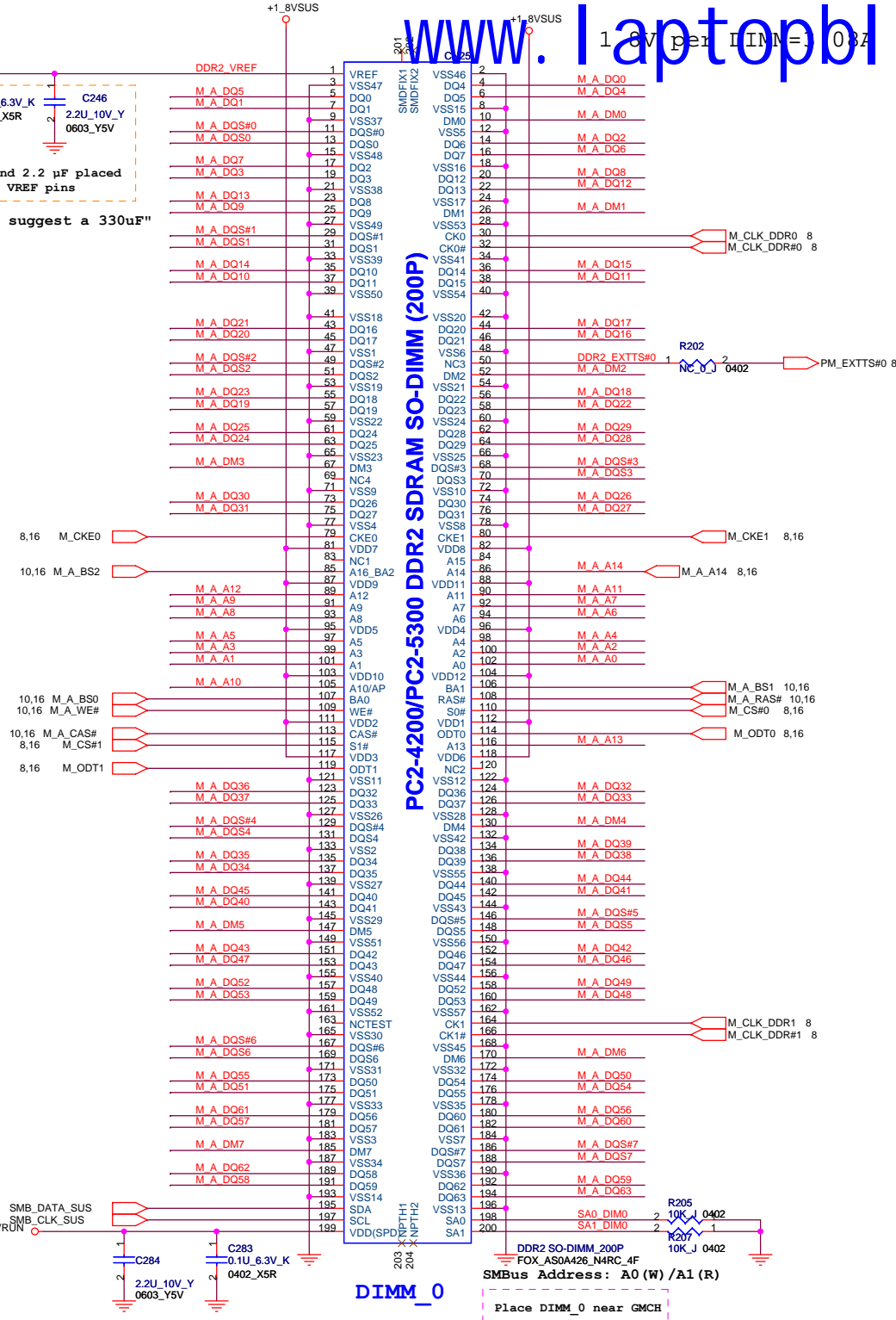
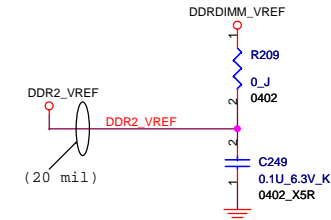
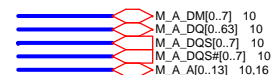






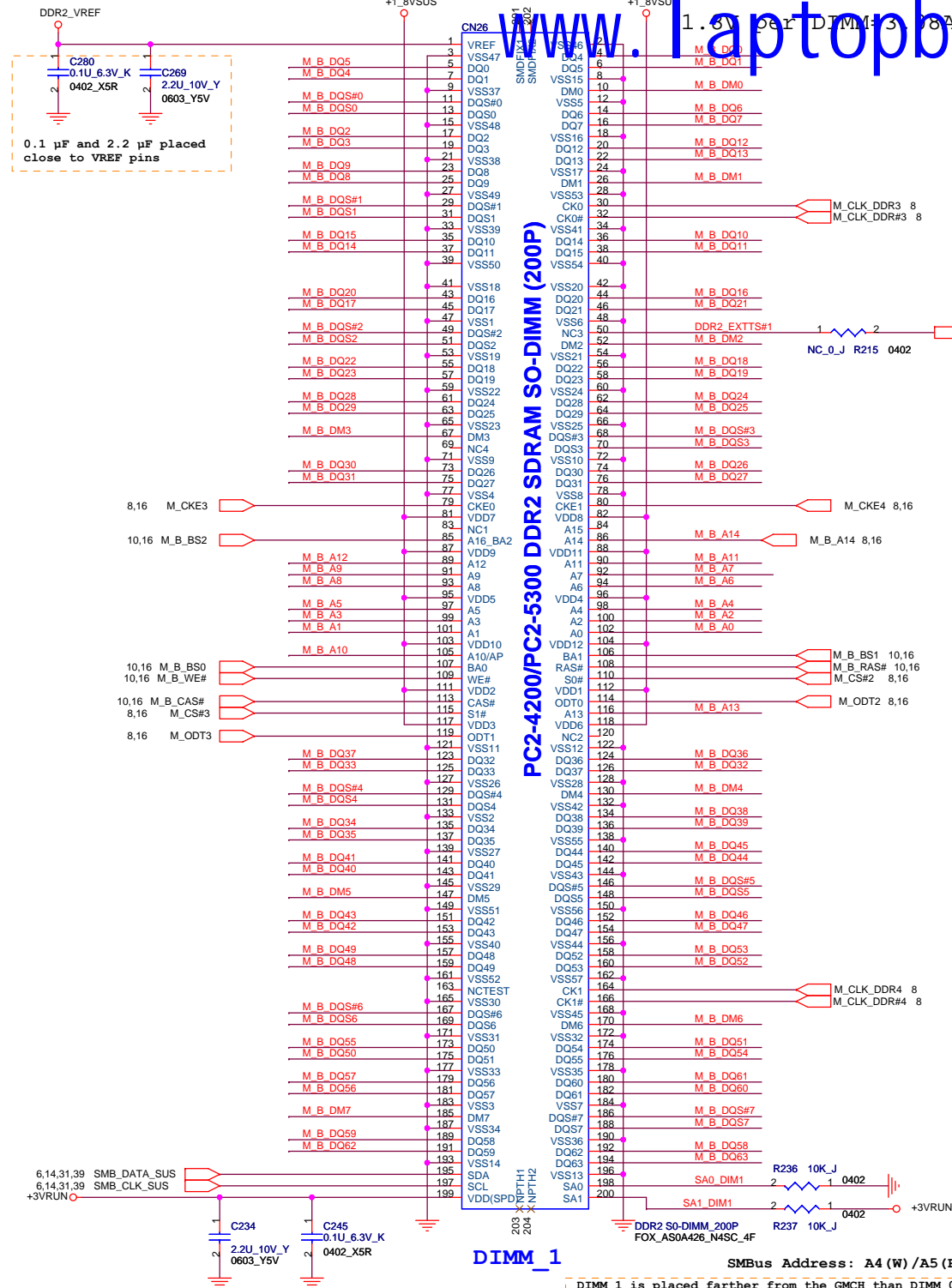
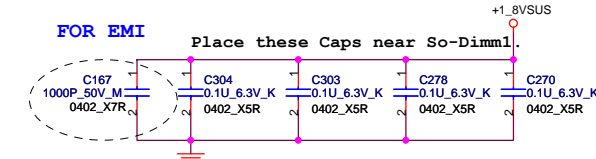
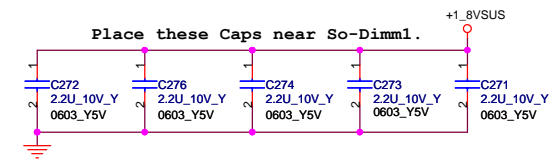
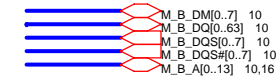
"Intel check list suggest a 330uF"

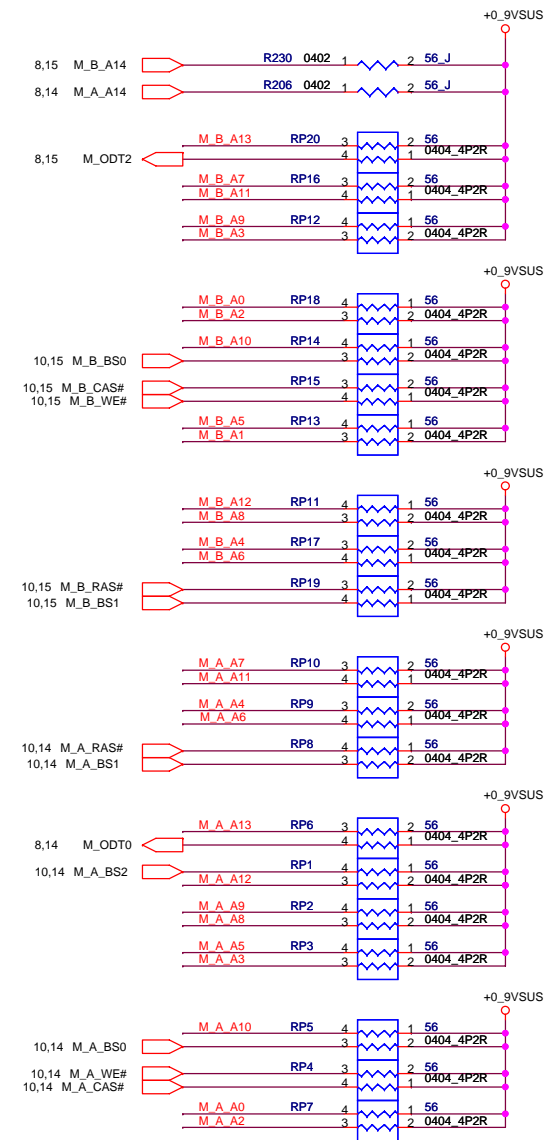
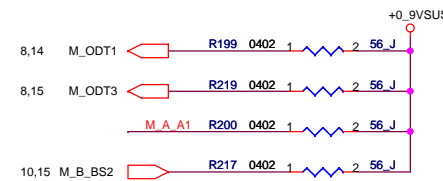
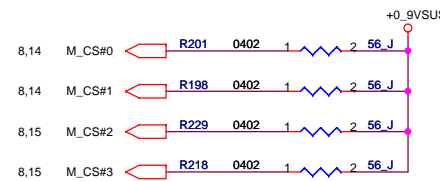
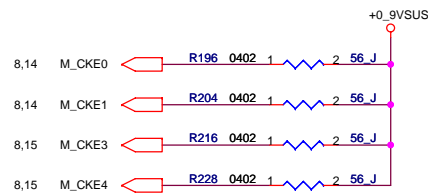
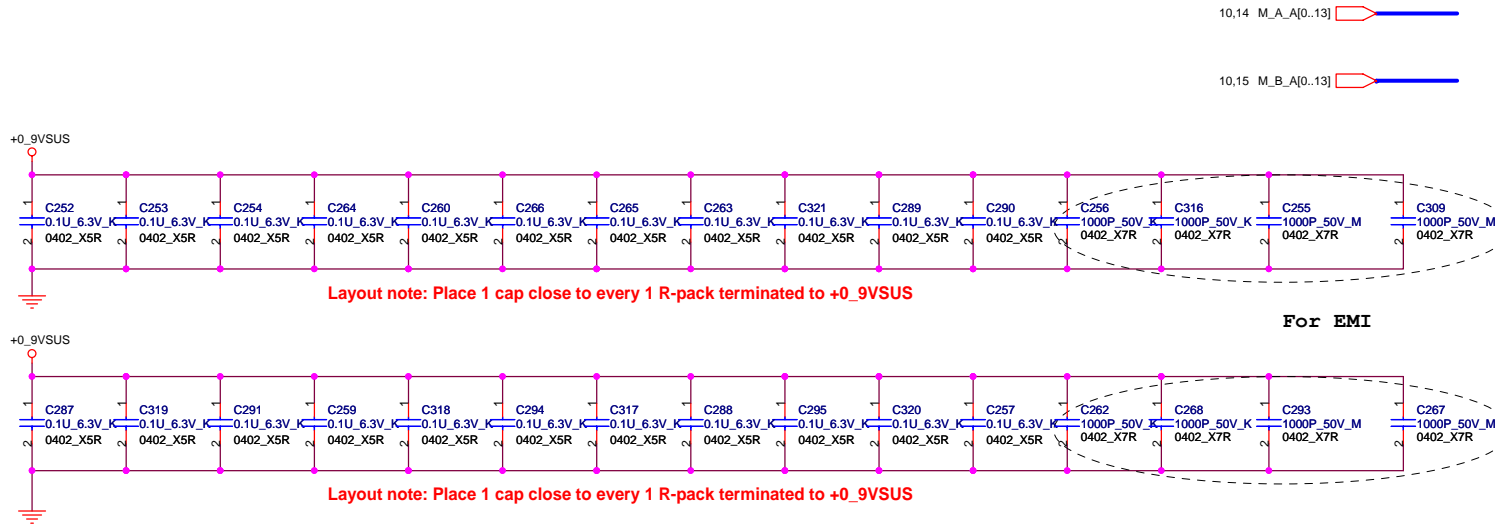
0.1 uF and 2.2 uF placed close to VREF pins

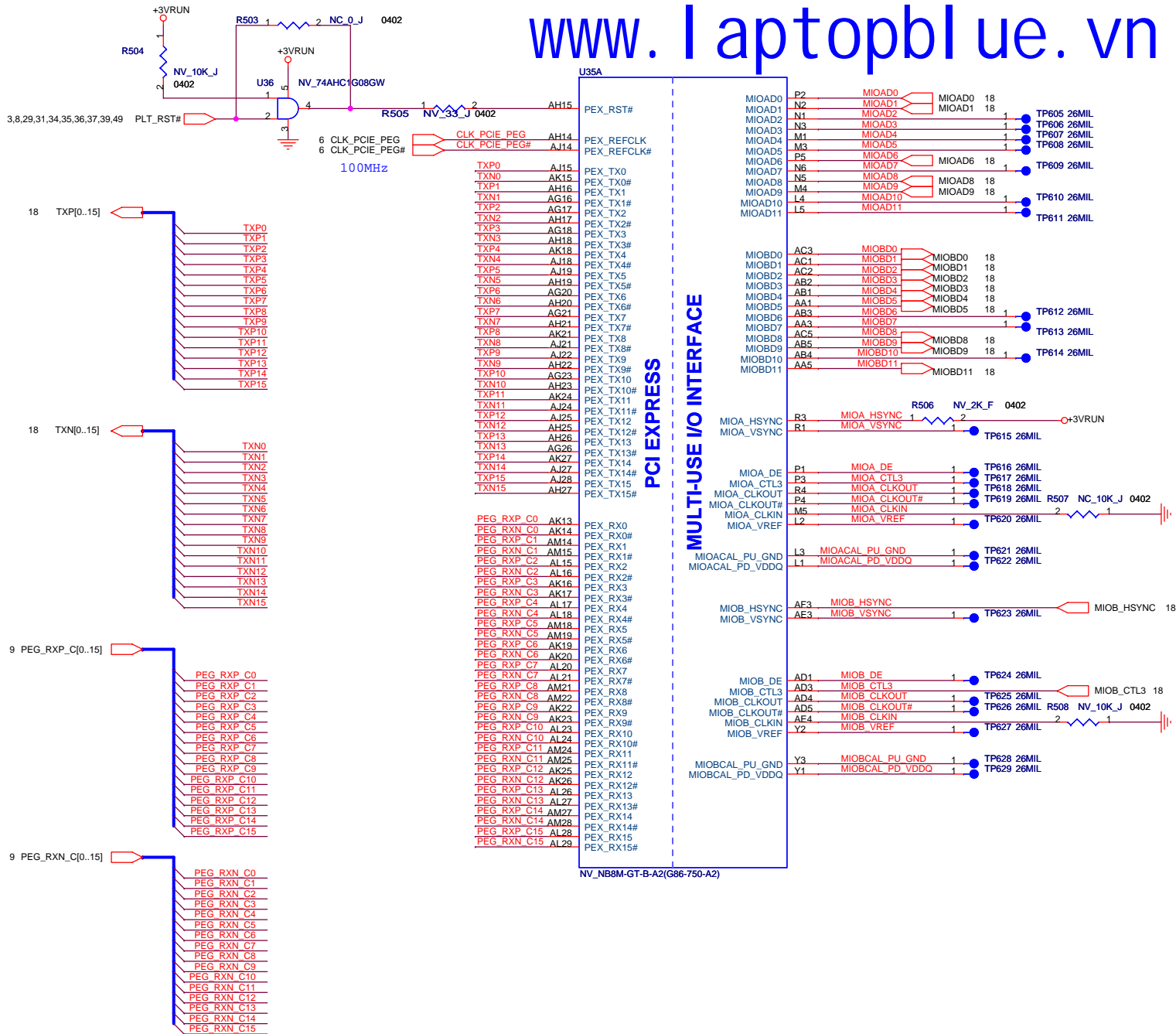




PC2-4200/PC2-5300 DDR2 SDRAM SO-DIMM (200P)

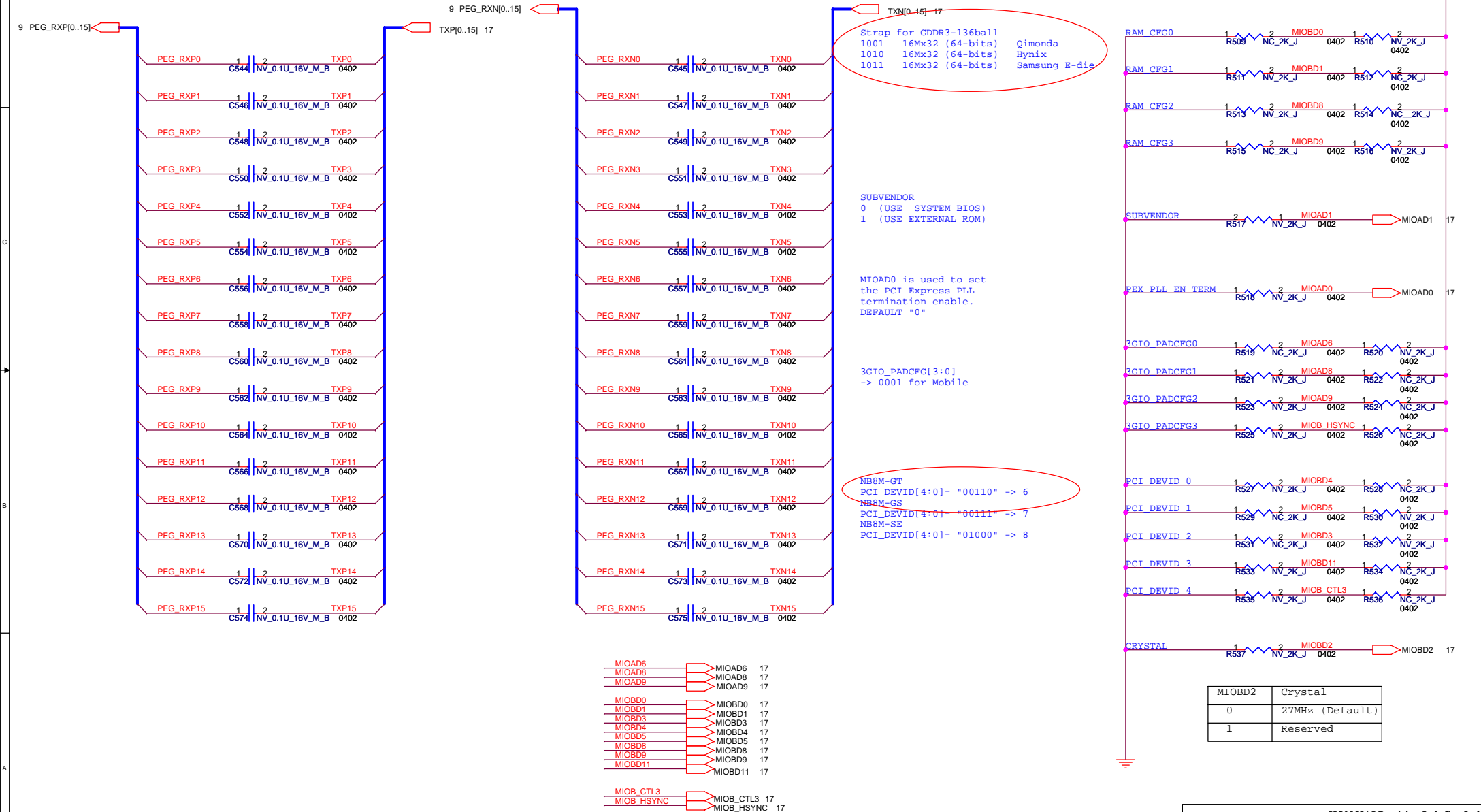


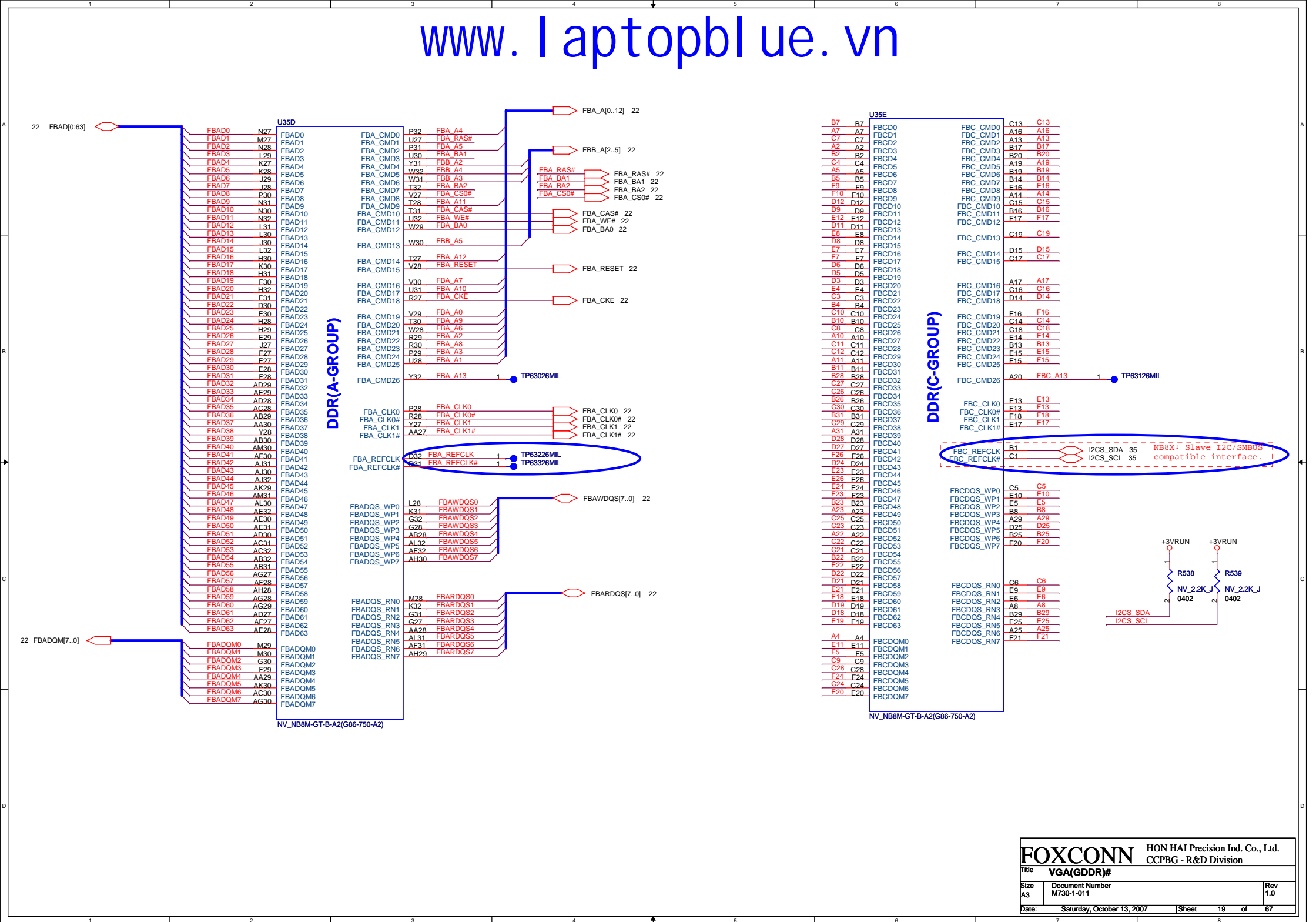




SKU	Qimonda	Finion	HYNIX	Samsung
Vendor PN	W111NE2121BF	W111NE2121BF	W111NE2121BF	K4J52324QE-BC14
M.H PN	13-HYB18H5-3003	13-HY5RS12-3001	13-HY5RS12-3001	13-K4J5232-3001
Configuration	NB8M-GT with 2pcs (16Mx32) GDDR3			
LOCATION	Stuff R511,R510	Stuff R512,R509	Stuff R512,R510	No Stuff R511,R509

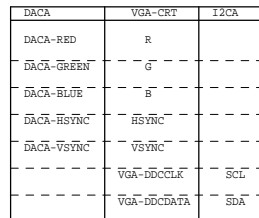
FAE: TV Mode Strap no use, remove.  
(MIOAD7, MIOAD10, MIOBD6)

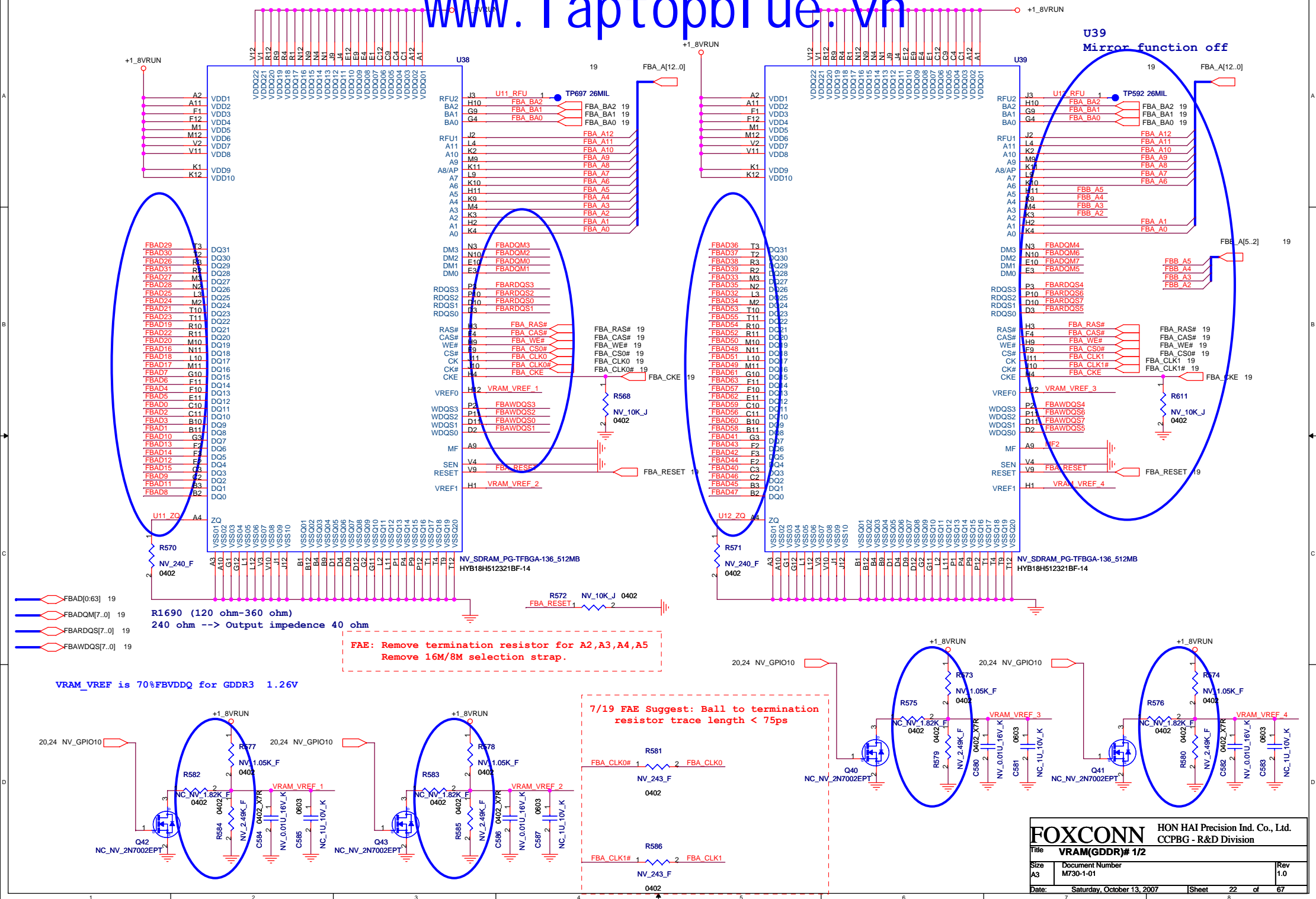


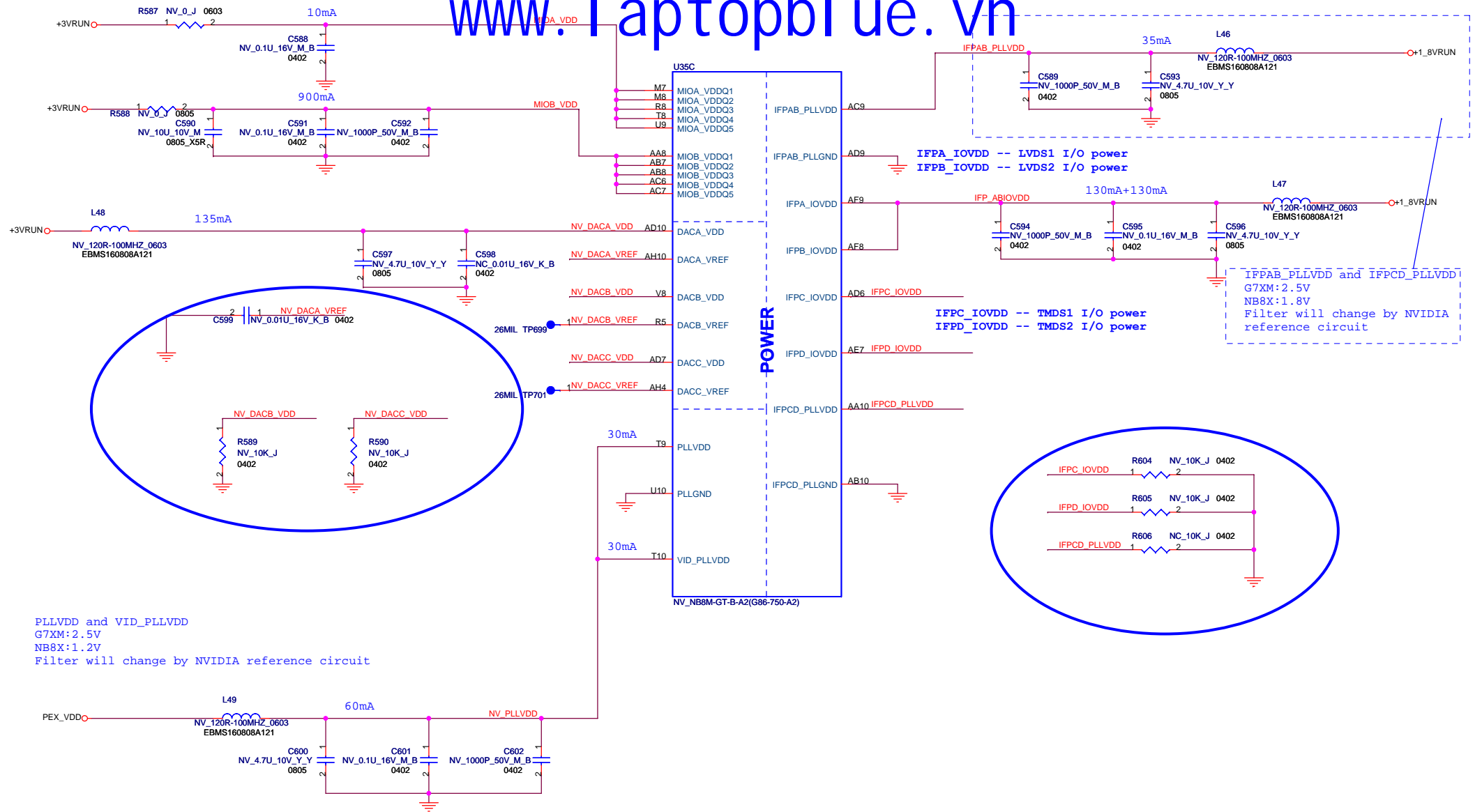


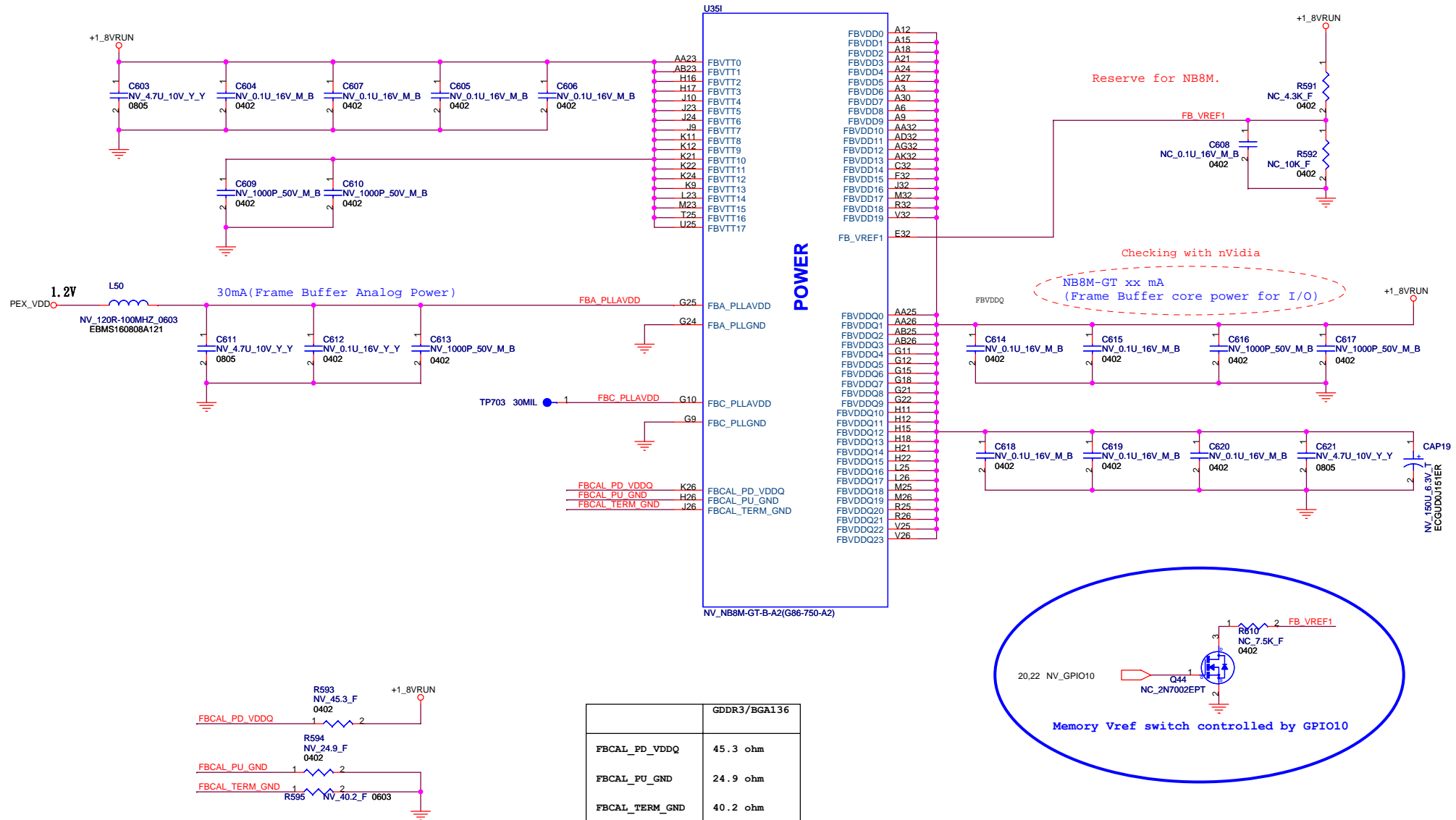


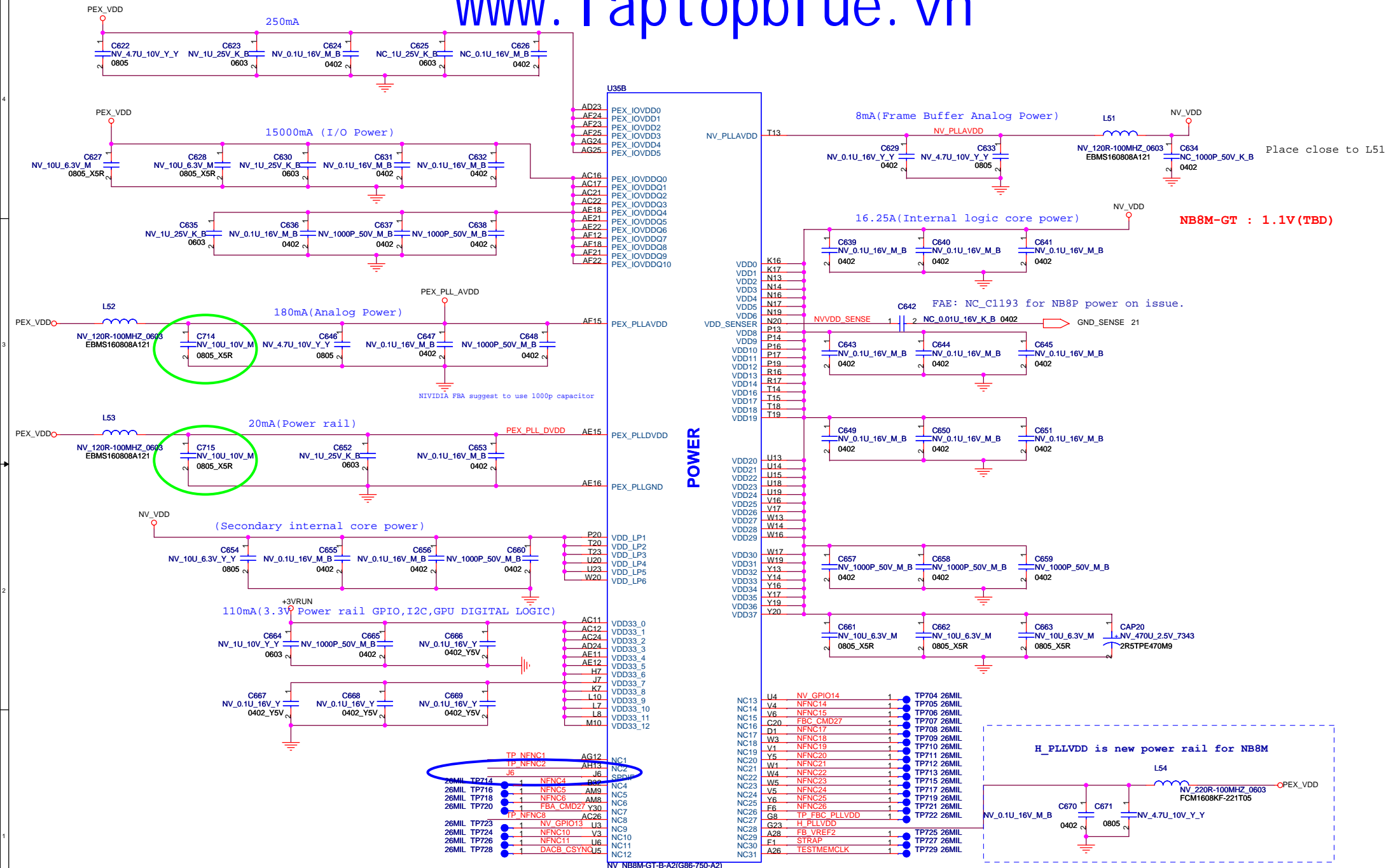






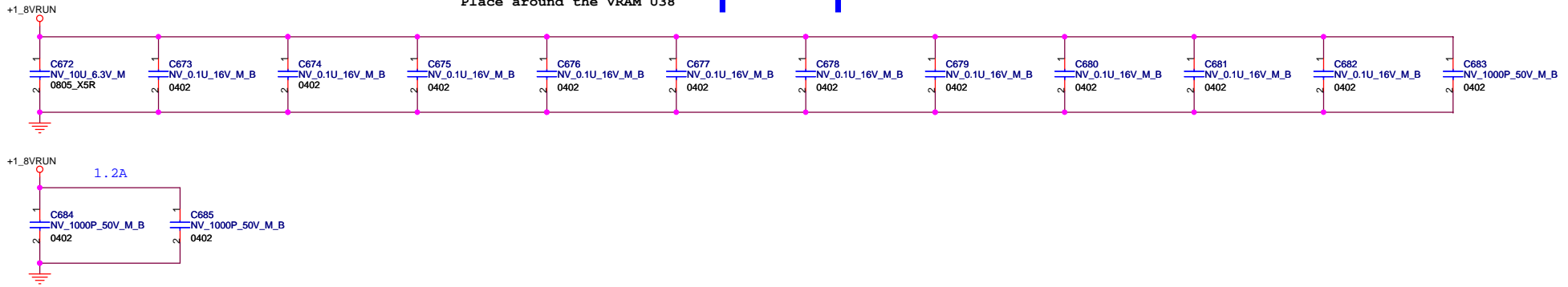




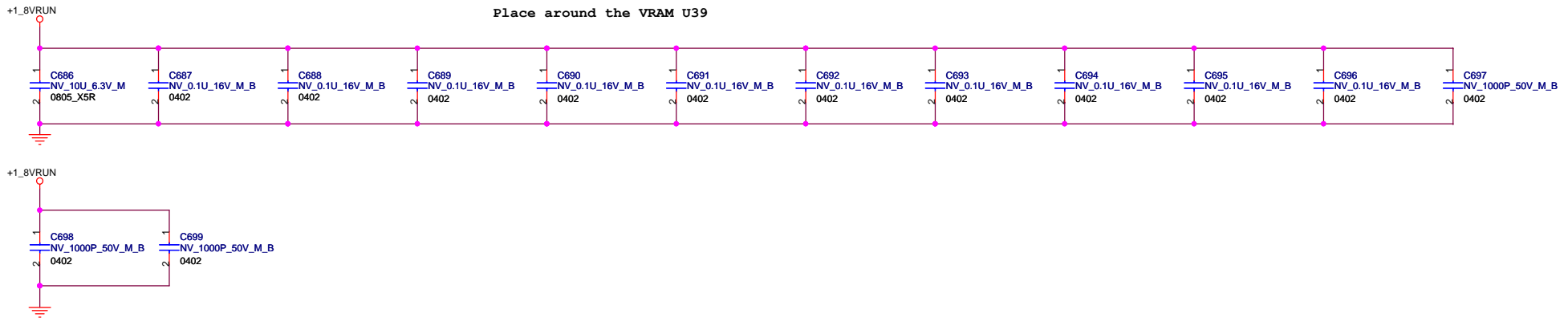


NB8X update  
 -FBC\_CMD27: FBC\_CMD27: Additional memory address bit to support dual rank 8 bank memory configuration.  
 -DACB\_CSINC: Composite sync for SCART support  
 -NV\_GPIO14: Additional GPIO

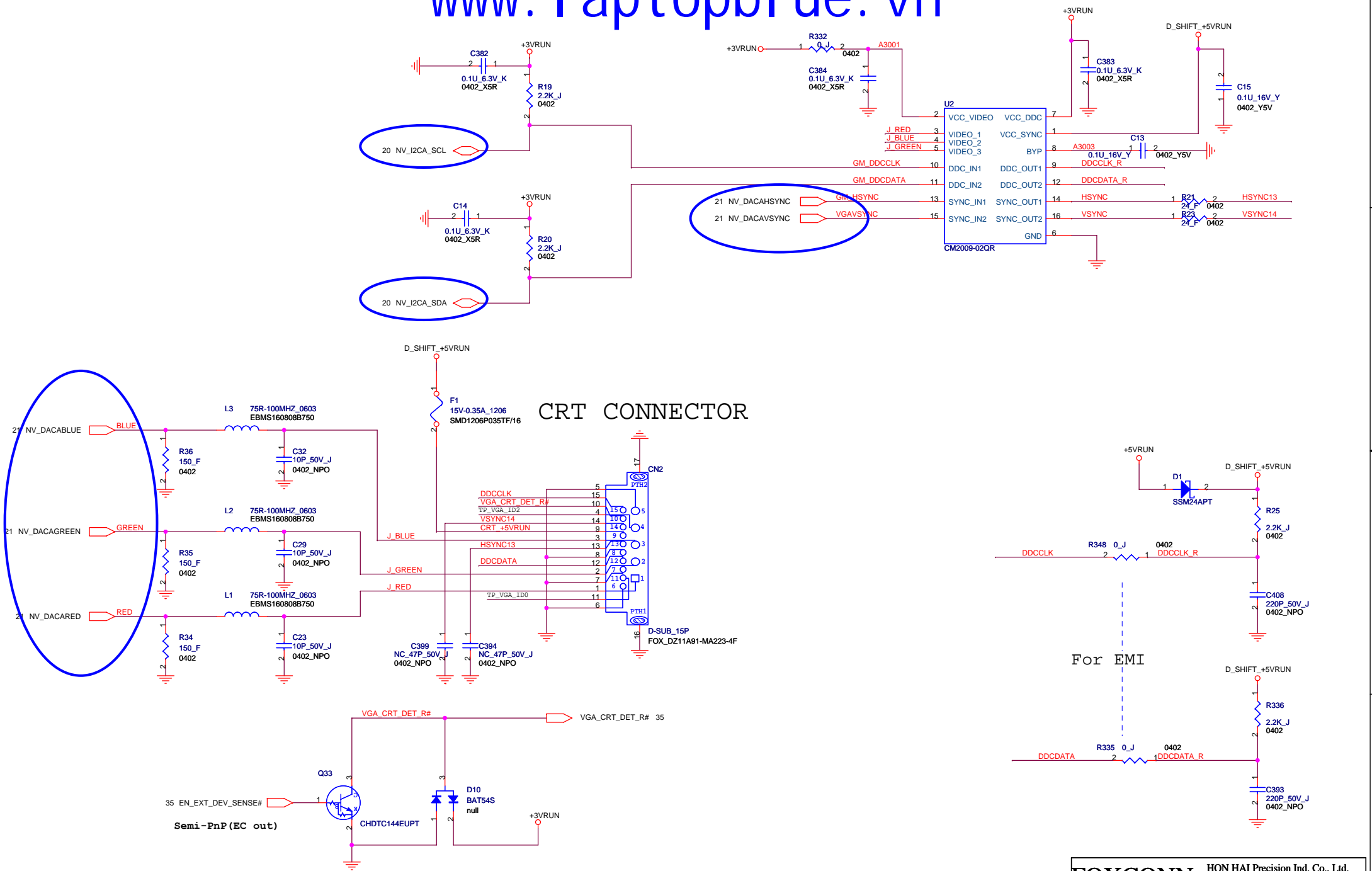
Place around the VRAM U38



Place around the VRAM U39

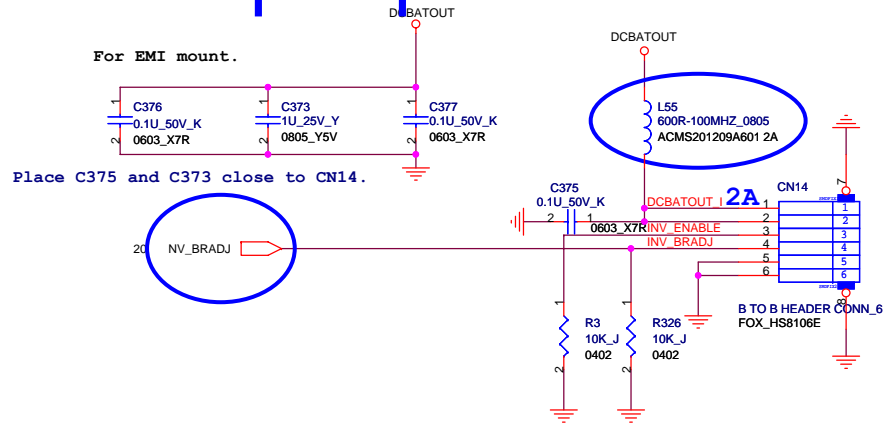
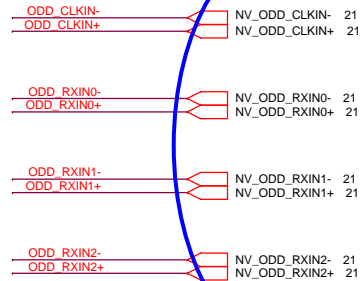




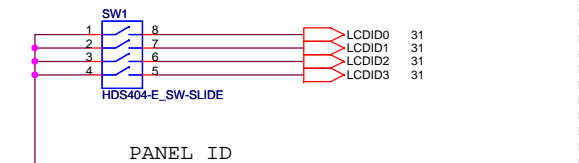
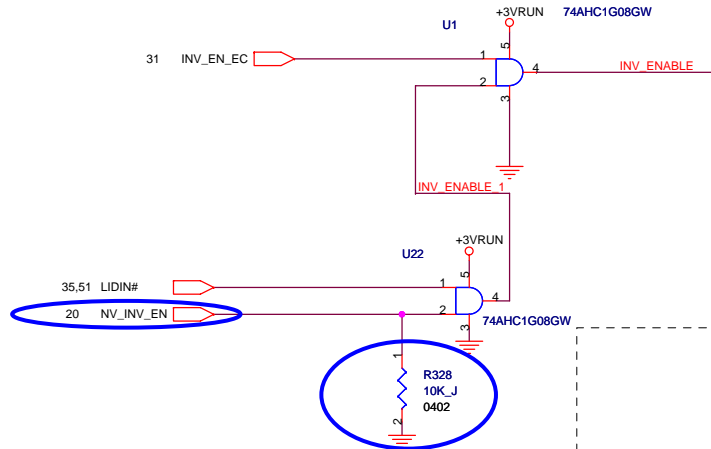
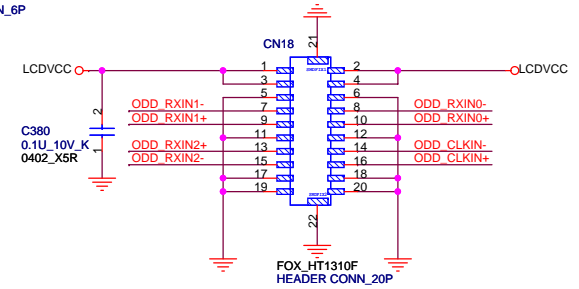


# LVDS

www.laptopblue.vn



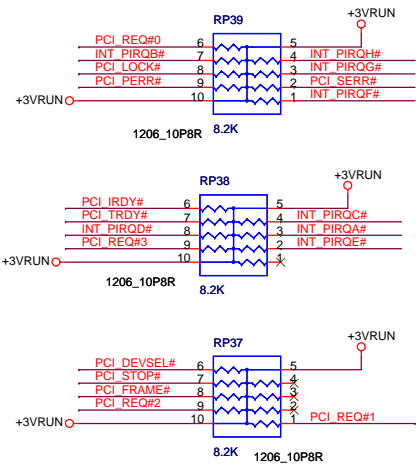
## INVERTER CONN.



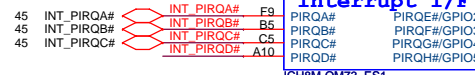
**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
CCPBG - R&D Division

Title			Rev
LVDS			1.0
Size A3	Document Number M730-1-01		
Date:	Saturday, October 13, 2007	Sheet	28 of 67

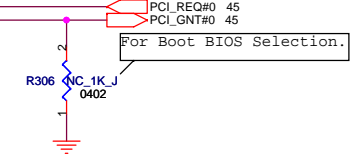
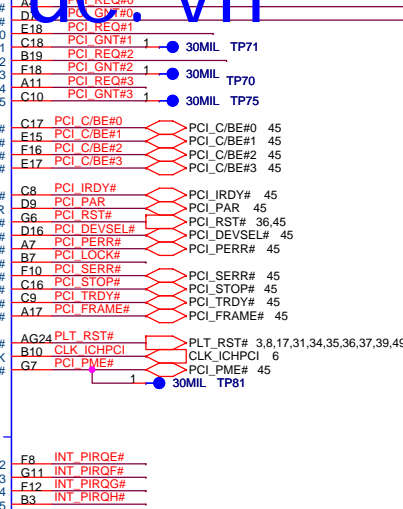
The R597 will consume about 0.054 Watt ( $3.3 \times 3.3 / 200 = 0.054W$ ). We changed resistor to 0603 size (1/8 Watt)



PCI Pullups

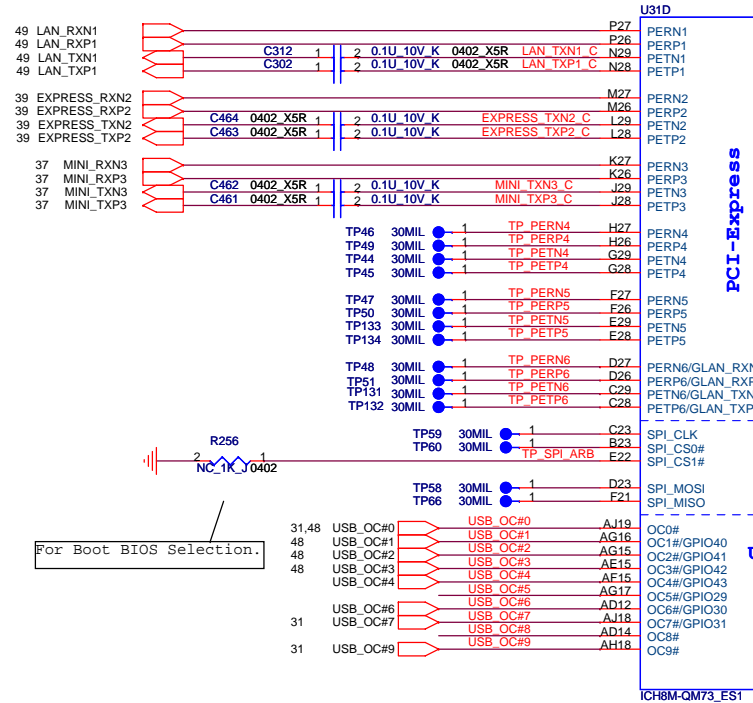


ICH8M-QM73\_ES1

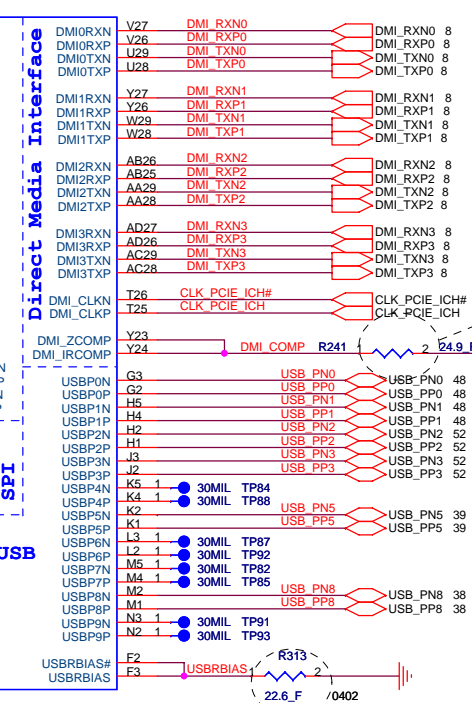


Strap for Boot-BIOS

	QNT0#	SPI_CS1#
EP(Default)	H1	H1
PCI	H1	LOW
SPI	LOW	H1

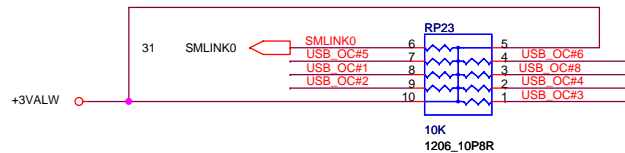


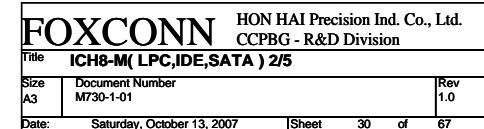
ICH8M-QM73\_ES1

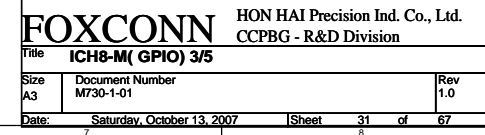


Place within 500 mils of ICH

Place within 500 mils of ICH and don't routing next to high speed signals





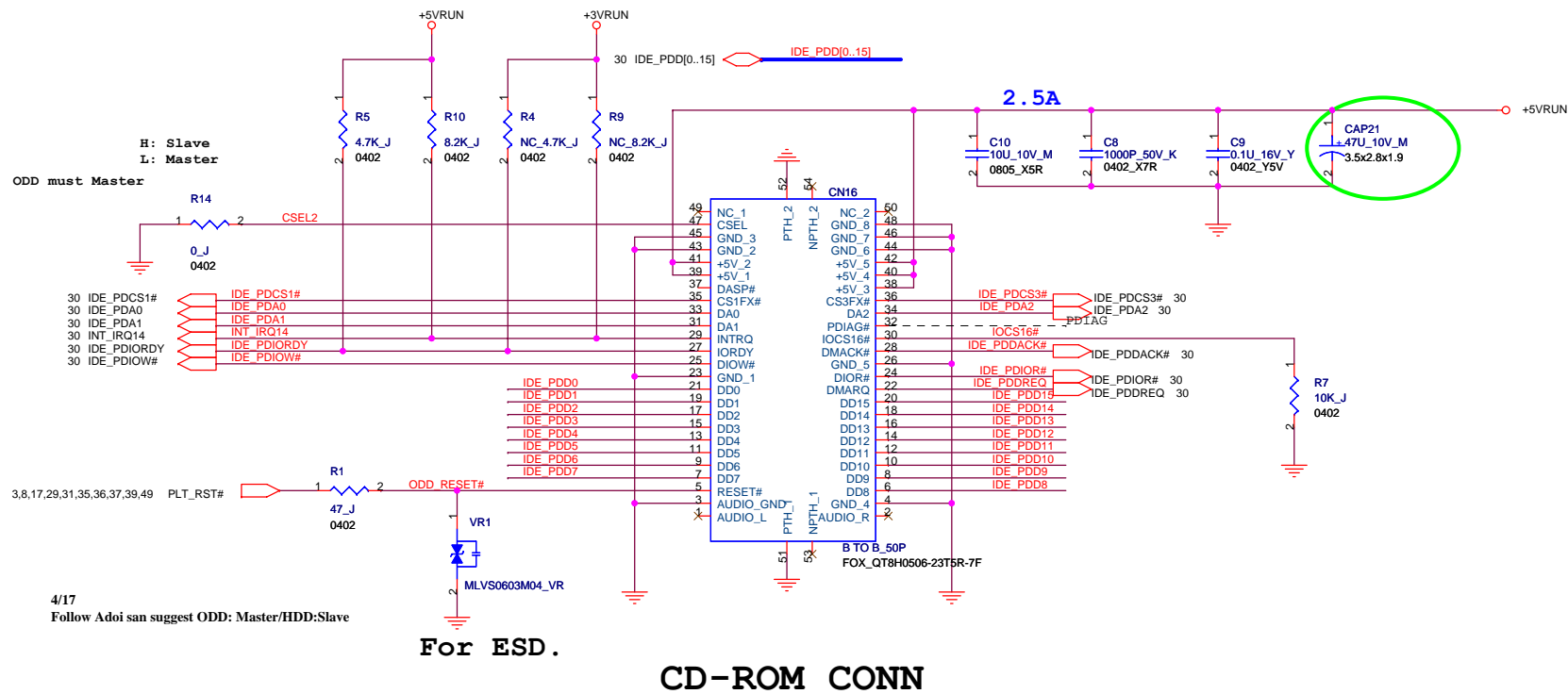
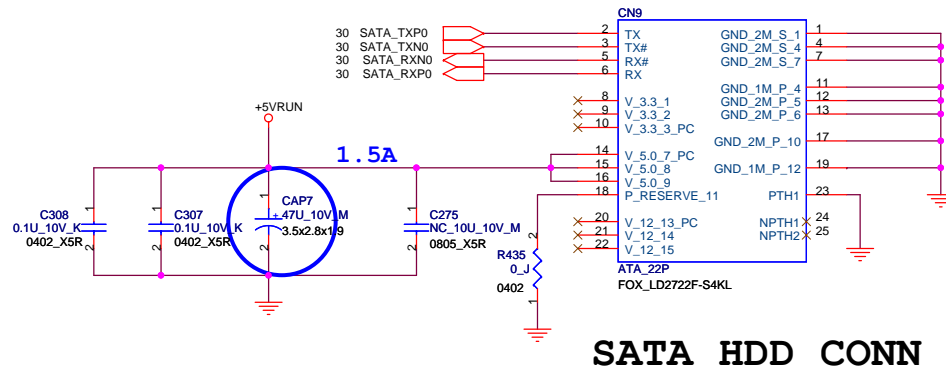


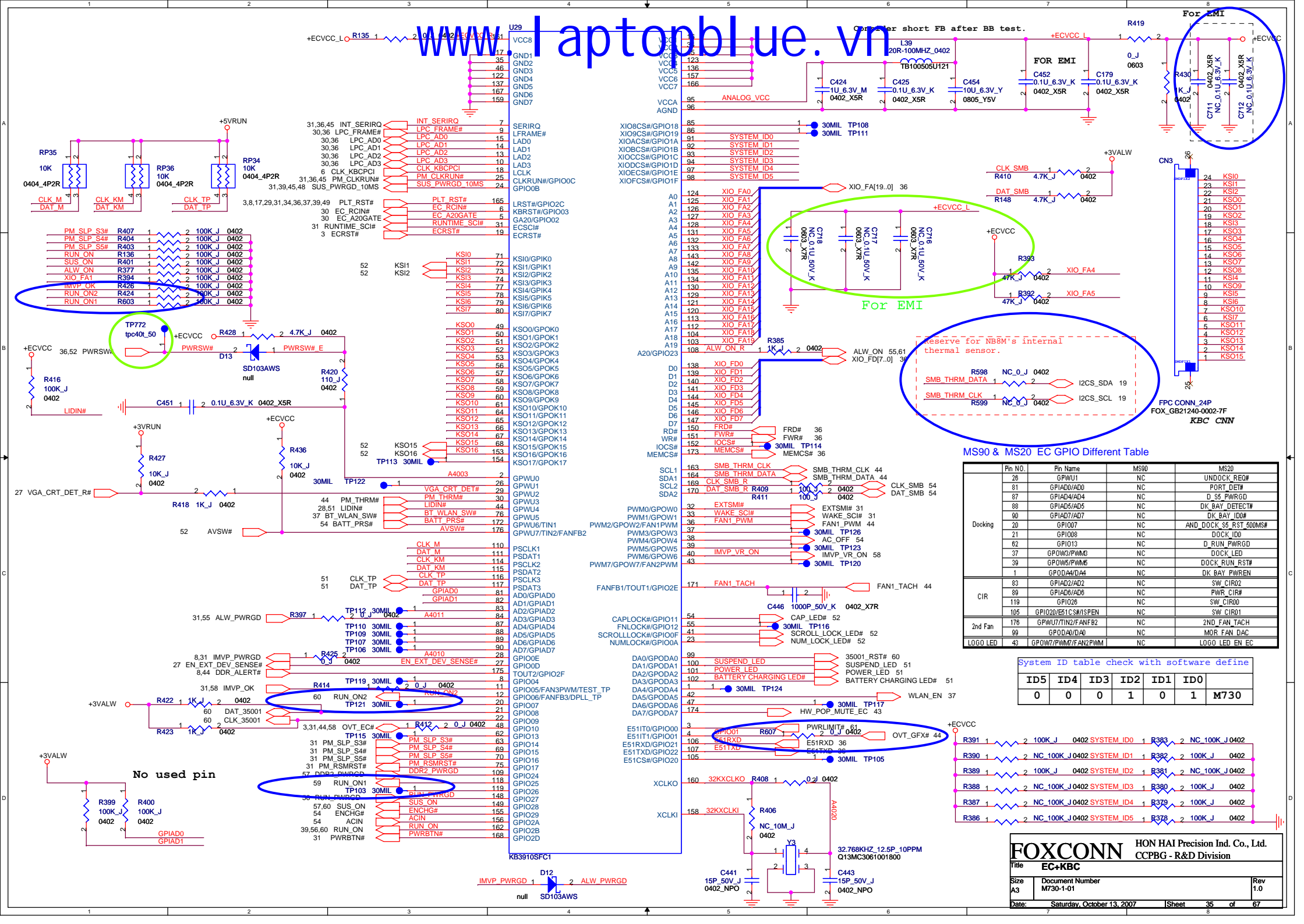


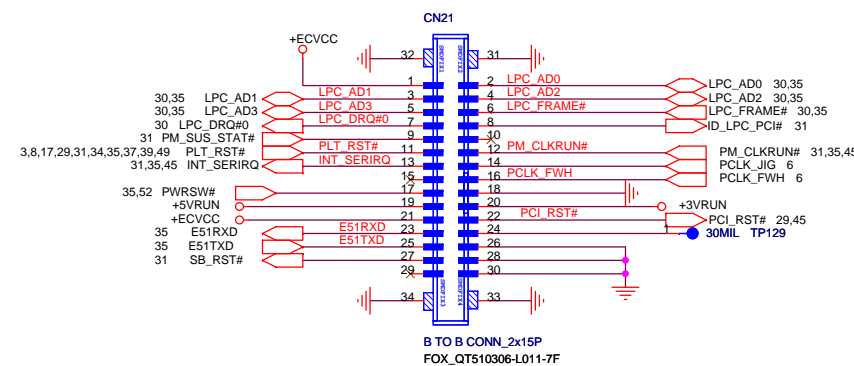
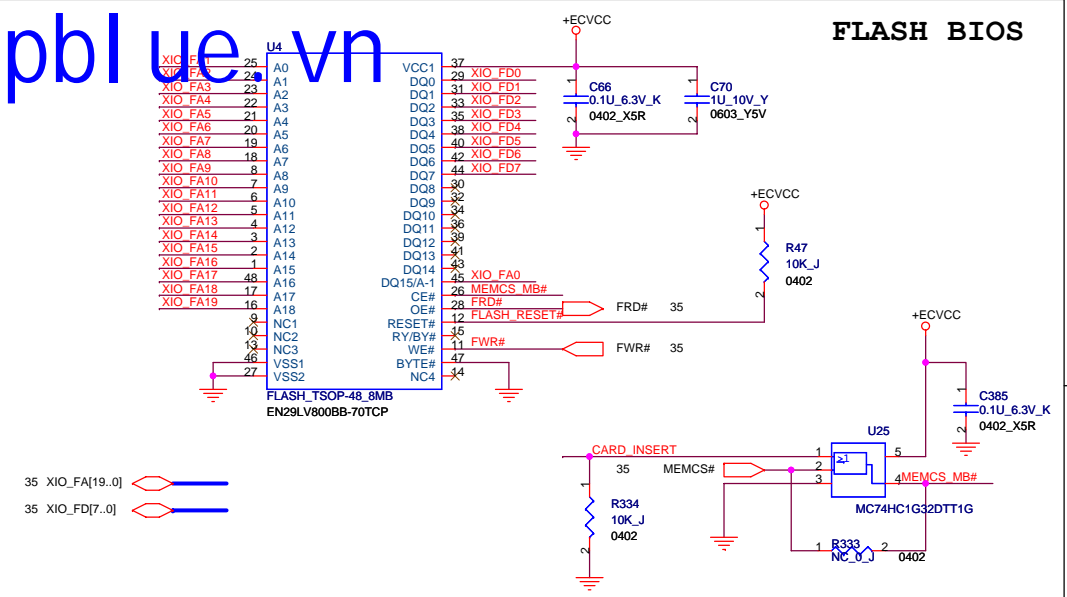


REF			
A23	VSS001	VSS099	Z
A5	VSS002	VSS100	Z
AA2	VSS003	VSS101	L13
AA7	VSS004	VSS102	L15
A25	VSS005	VSS103	L26
AB1	VSS006	VSS104	L27
AB24	VSS007	VSS105	L4
AC11	VSS008	VSS106	L5
AC14	VSS007	VSS107	M12
AC25	VSS010	VSS108	M13
AC26	VSS011	VSS109	M14
AC27	VSS012	VSS110	M15
AD1	VSS013	VSS111	M16
AD28	VSS014	VSS112	M17
AD29	VSS013	VSS113	M23
AD29	VSS016	VSS114	M28
AD3	VSS017	VSS115	M29
AD4	VSS018	VSS116	M3
AD6	VSS019	VSS117	N1
AE1	VSS020	VSS118	N11
AE12	VSS021	VSS119	N12
AE2	VSS022	VSS120	N13
AE22	VSS023	VSS121	N14
AD1	VSS024	VSS122	N15
AE5	VSS025	VSS123	N16
AE6	VSS026	VSS124	N17
AE9	VSS027	VSS125	N26
AE10	VSS028	VSS126	N27
AE14	VSS029	VSS127	N27
AE16	VSS030	VSS128	N4
AE18	VSS031	VSS129	N6
AE3	VSS032	VSS130	P12
AF4	VSS033	VSS131	P13
AG6	VSS034	VSS132	P14
AG6	VSS035	VSS133	P15
AH10	VSS036	VSS134	P16
AH13	VSS037	VSS135	P17
AH6	VSS038	VSS136	P21
AH19	VSS039	VSS137	P28
AH2	VSS040	VSS138	P29
AE28	VSS041	VSS139	R1
AH22	VSS042	VSS140	R11
AH24	VSS043	VSS141	R12
AH26	VSS044	VSS142	R13
AH3	VSS045	VSS143	R14
AH4	VSS046	VSS144	R15
AH5	VSS047	VSS145	R16
AJ5	VSS048	VSS146	R17
B11	VSS049	VSS147	R18
B14	VSS050	VSS148	R28
B1	VSS051	VSS149	R4
B2	VSS052	VSS150	T12
B20	VSS053	VSS151	T13
B22	VSS054	VSS152	T14
BB	VSS055	VSS153	T15
C24	VSS056	VSS154	T16
C27	VSS057	VSS155	T17
C27	VSS058	VSS156	T2
C6	VSS059	VSS157	U12
D12	VSS060	VSS158	U13
D15	VSS061	VSS159	U14
D18	VSS062	VSS160	U15
D2	VSS063	VSS161	U17
D4	VSS064	VSS162	U17
E21	VSS065	VSS163	U26
E24	VSS066	VSS164	U27
F4	VSS067	VSS165	U2
F9	VSS068	VSS166	U3
E23	VSS069	VSS167	U5
F28	VSS070	VSS168	V15
F29	VSS071	VSS169	V28
G7	VSS072	VSS170	V29
F1	VSS073	VSS171	W2
G1	VSS074	VSS172	W26
E2	VSS075	VSS173	W27
G13	VSS076	VSS174	Y28
G19	VSS077	VSS175	Y29
G23	VSS078	VSS176	Y4
G25	VSS077	VSS177	Y4
G25	VSS080	VSS178	AB4
G26	VSS081	VSS179	AB23
G27	VSS082	VSS180	AB5
H2	VSS083	VSS181	AB6
H28	VSS084	VSS182	U4
H3	VSS085	VSS183	W24
H3	VSS086	VSS184	
H6	VSS087		
J25	VSS088	VSS_NCTF01	A1
J26	VSS089	VSS_NCTF02	A2
J27	VSS090	VSS_NCTF03	A28
J5	VSS091	VSS_NCTF04	AH1
J4	VSS092	VSS_NCTF05	AH29
J5	VSS093	VSS_NCTF06	AJ1
K23	VSS094	VSS_NCTF07	AJ2
K28	VSS095	VSS_NCTF08	AJ28
K2	VSS096	VSS_NCTF09	AJ29
K3	VSS097	VSS_NCTF10	B1
K6	VSS098	VSS_NCTF11	B29
		VSS_NCTF12	

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title <b>ICH8-M( GND) 5/5</b>			
Size A3	Document Number M730-1-01	Rev 1.0	
Date:	Saturday, October 13, 2007	Sheet	33 of 67

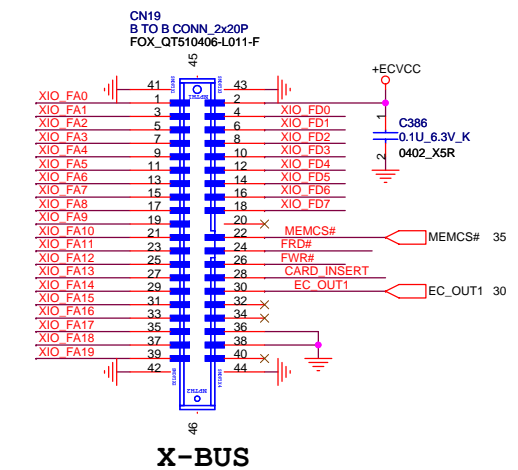




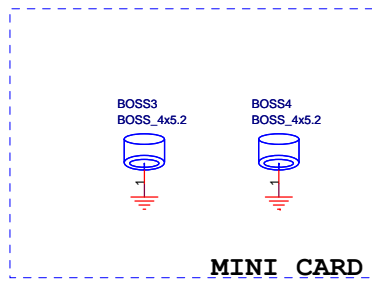


JIG-120

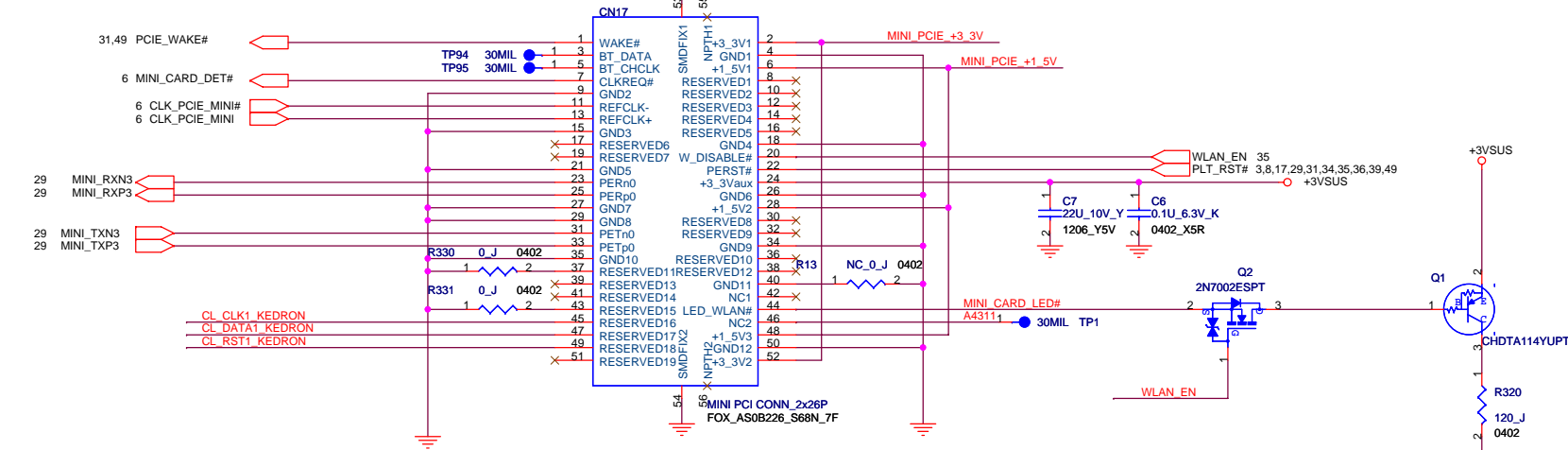
Pin 18 of JIG-120 is useless in debug board, so we let pin 18 NC.



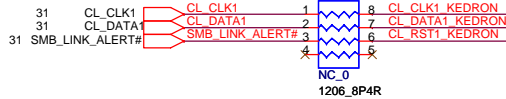
X-BUS



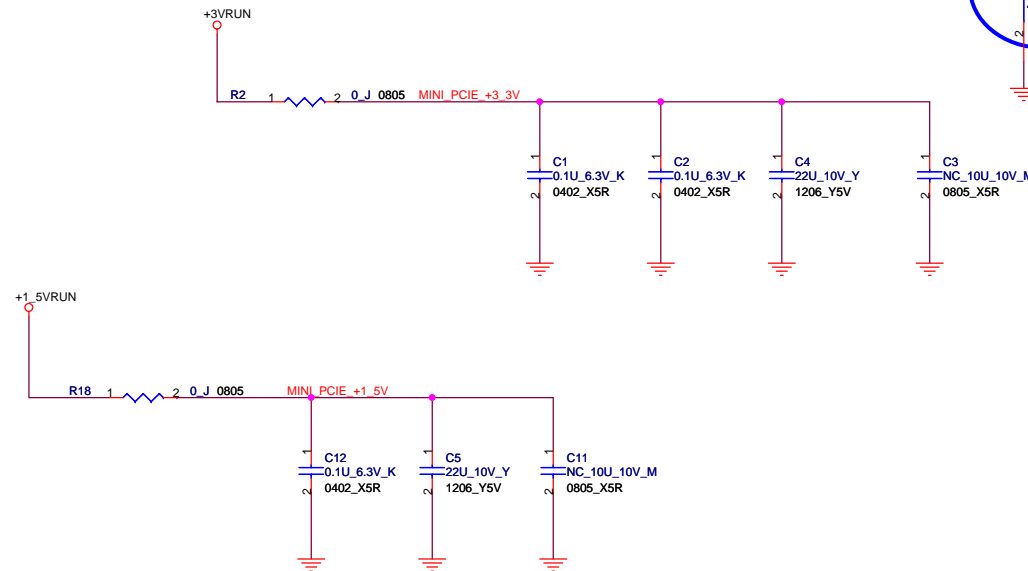
SW2 PIN8,9 : NPTH



## Mini Card. WLAN

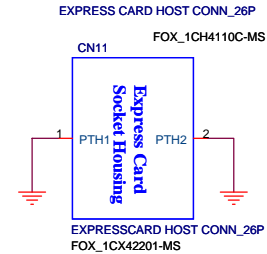
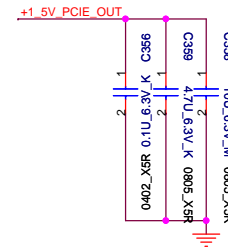
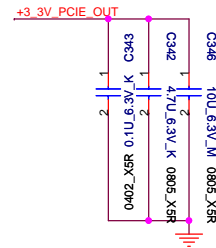
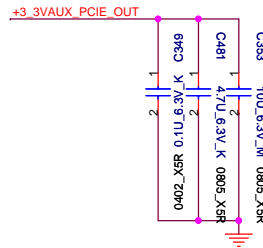
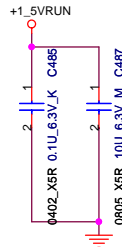
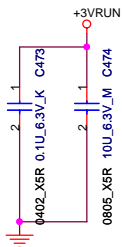
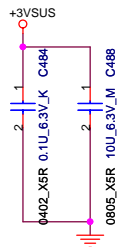
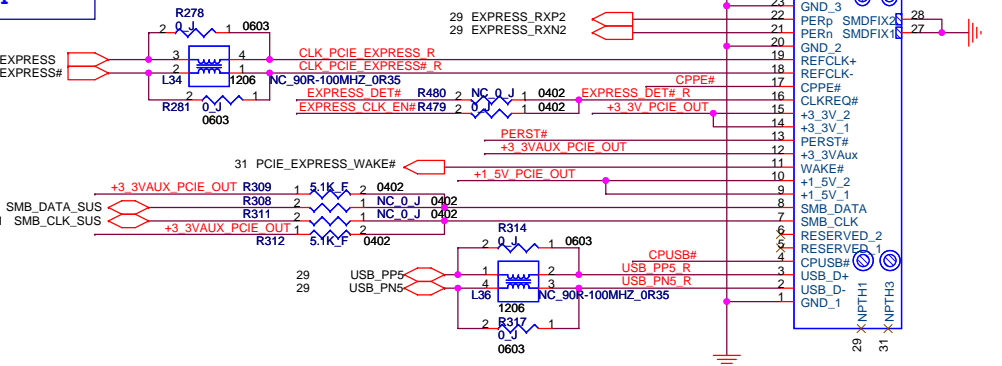
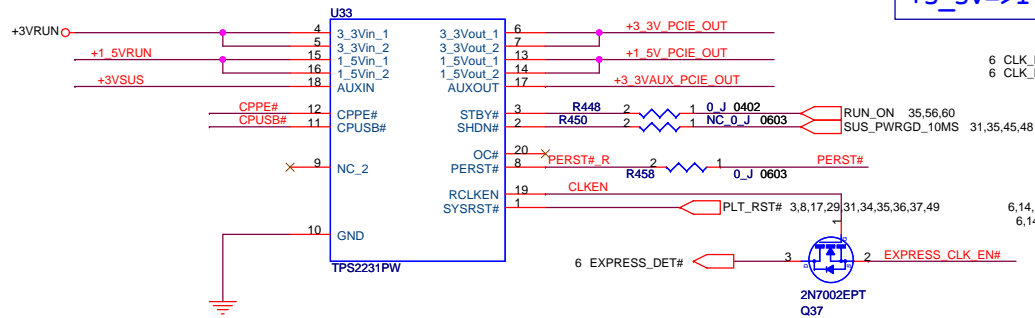


+1.5V=>0.5A  
+3.3VAux=>0.33A  
+3.3V=>1A



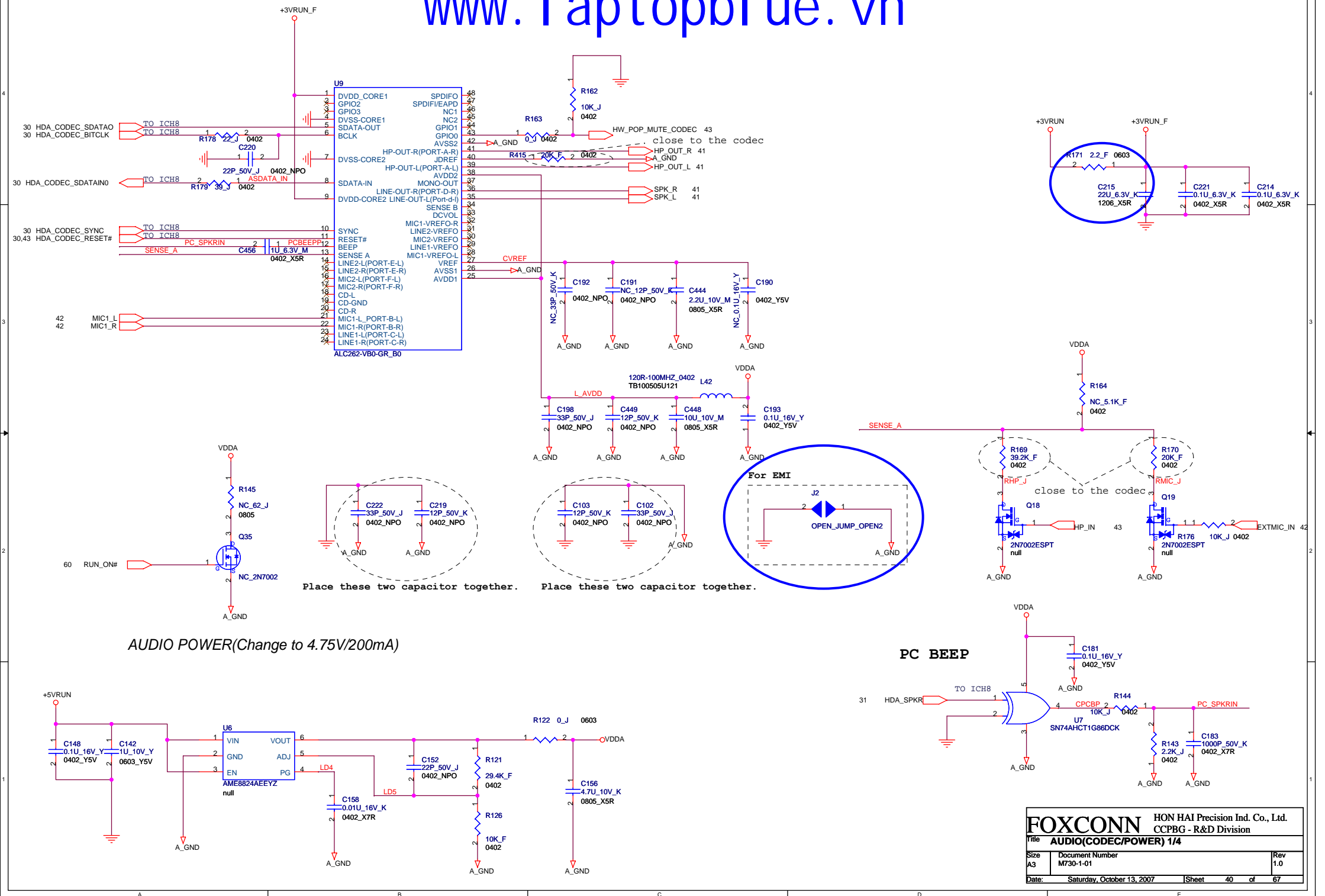


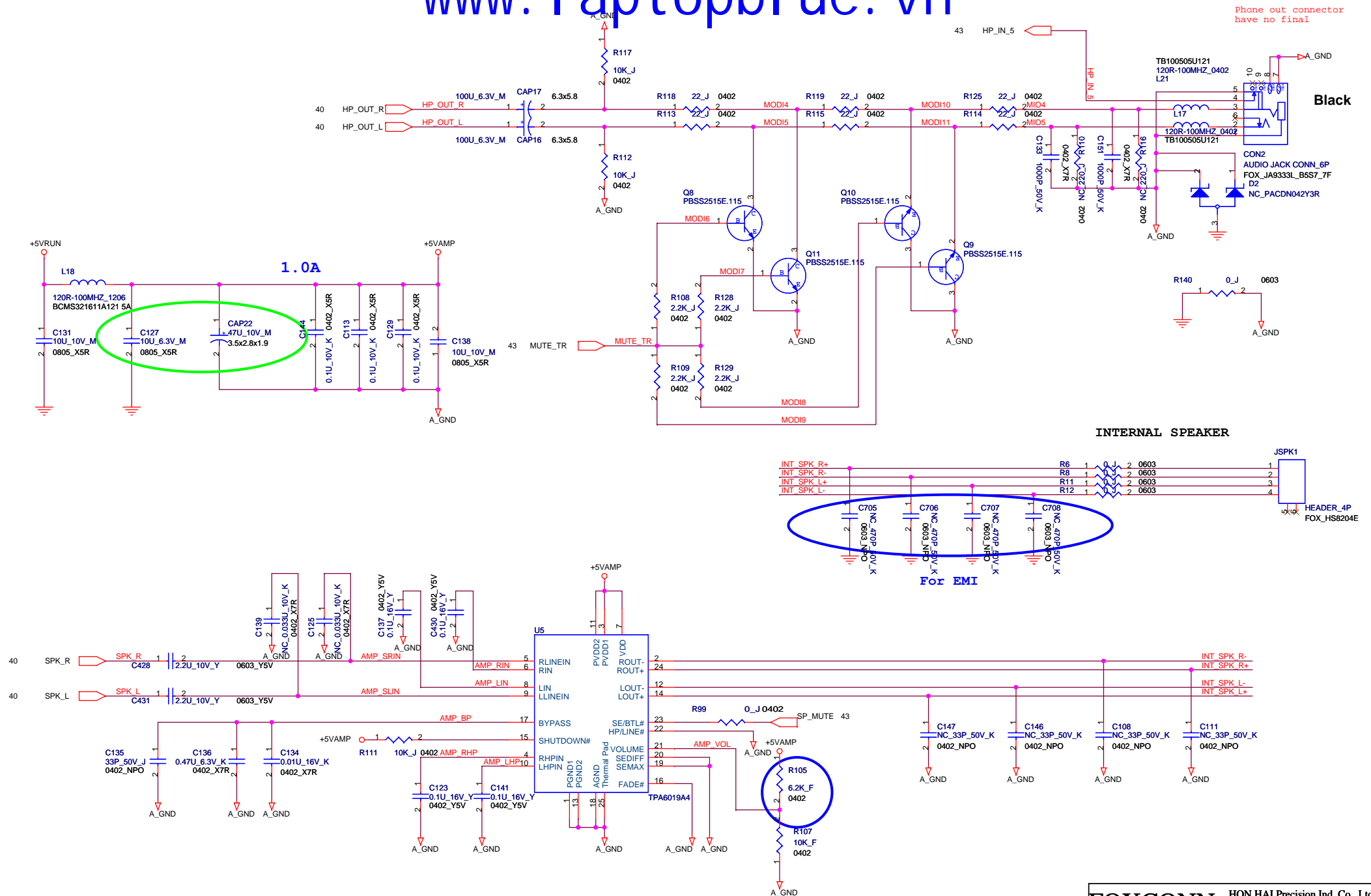
+1\_5V=>0.65A  
+3\_3VAux=>0.275A  
+3\_3V=>1.3A

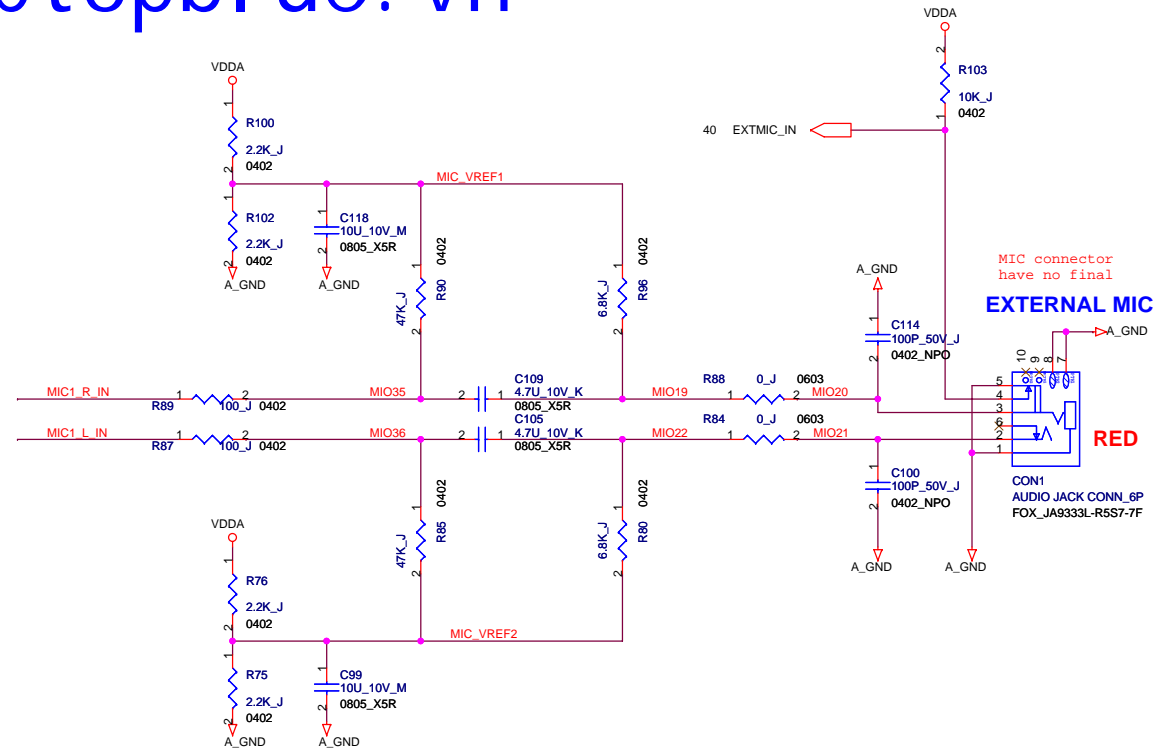
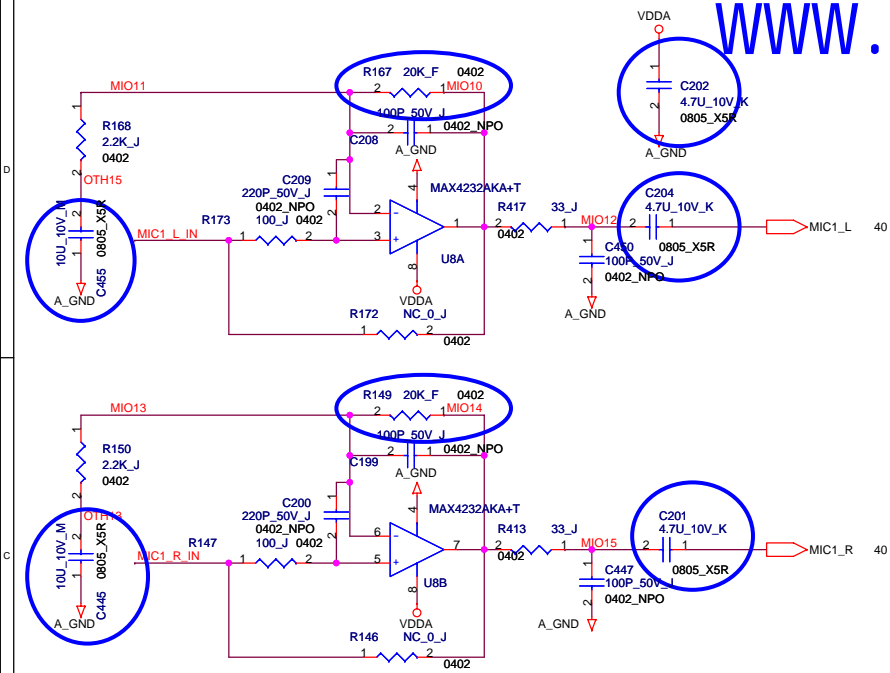


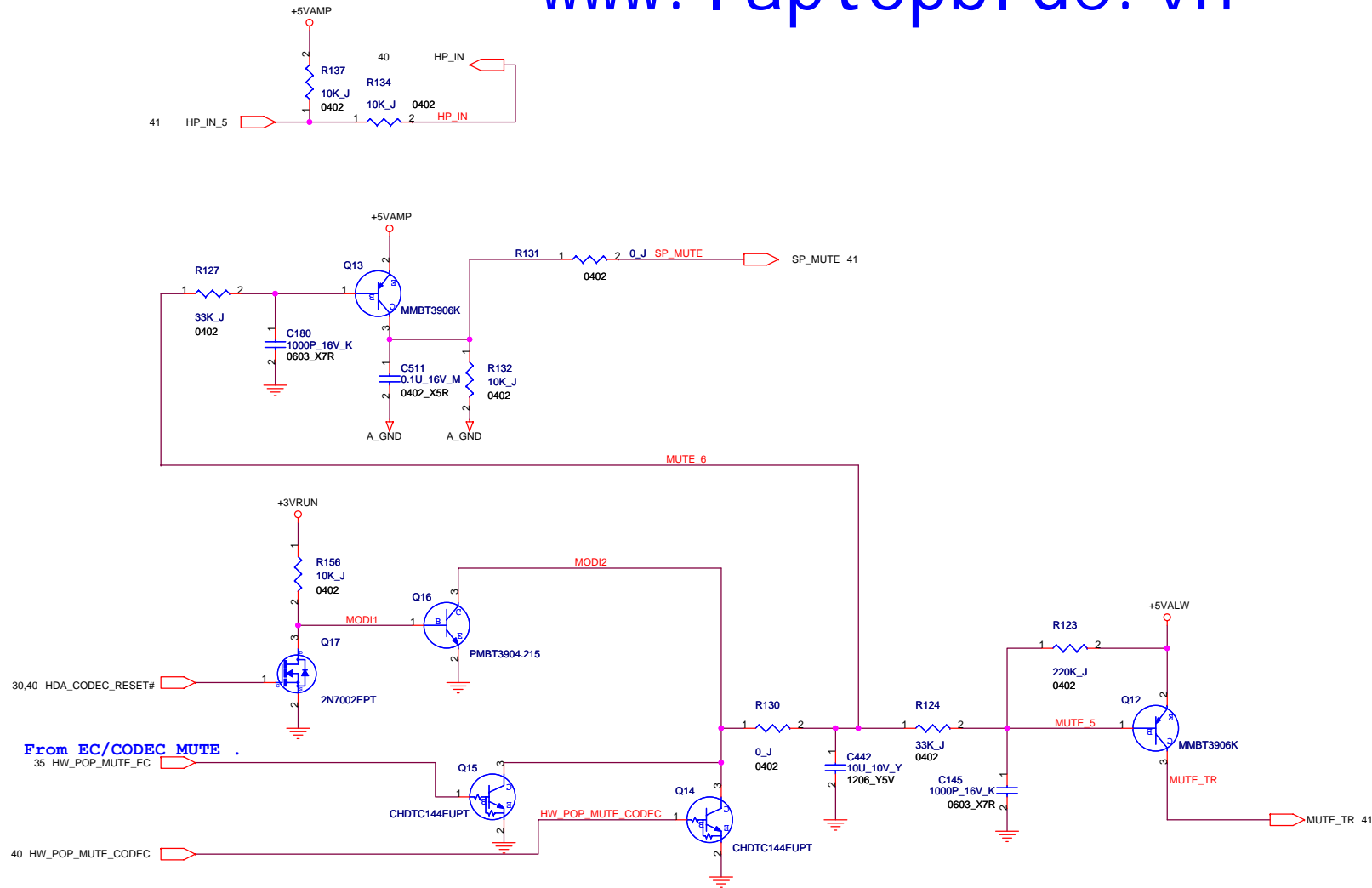
Express Card Housing

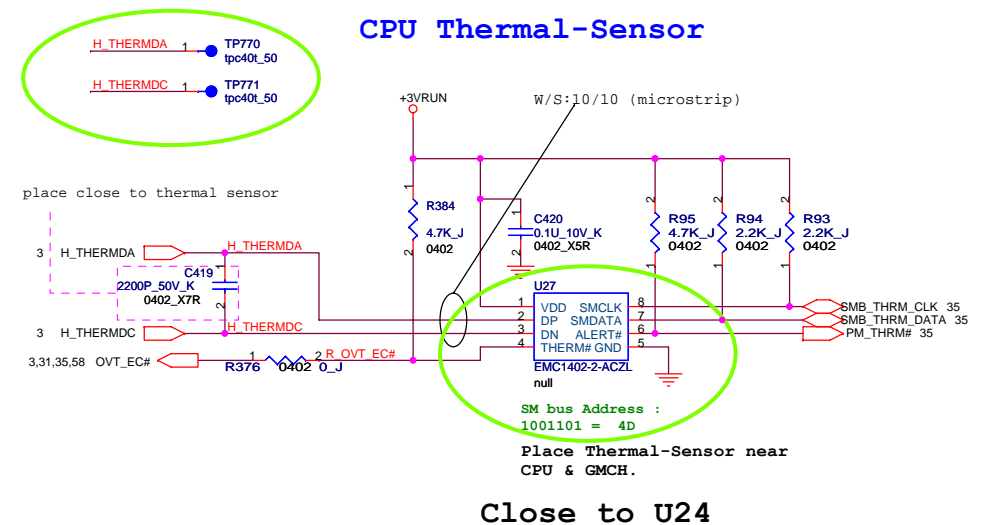
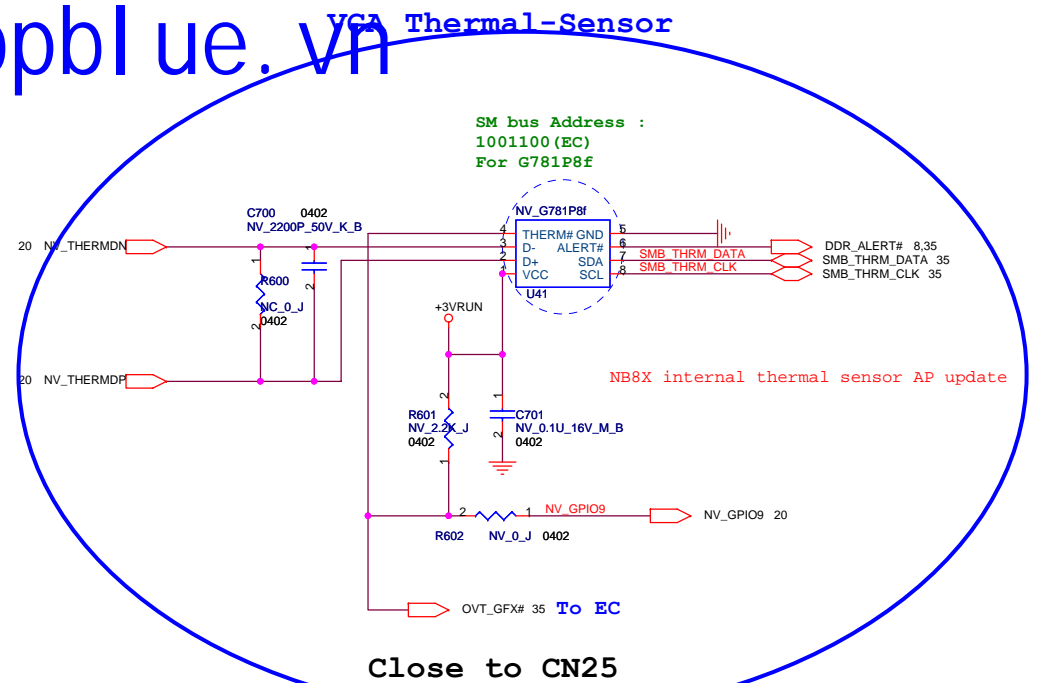
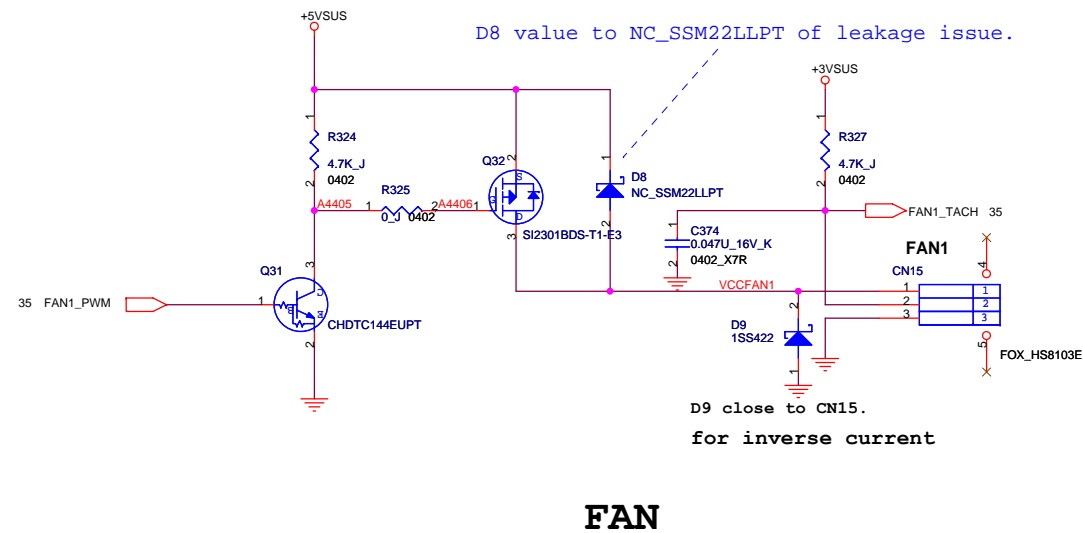


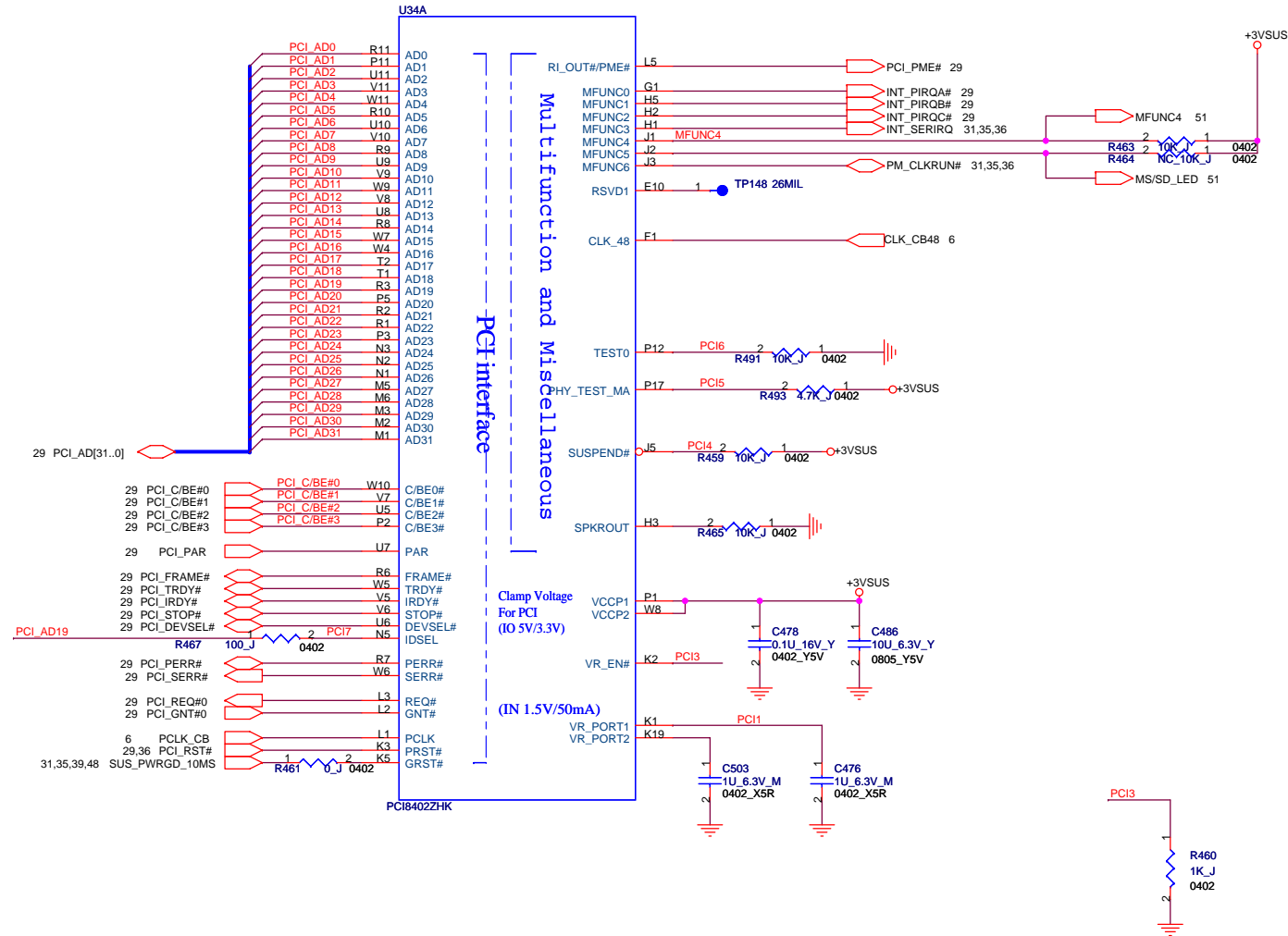






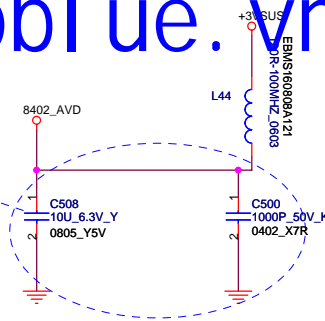




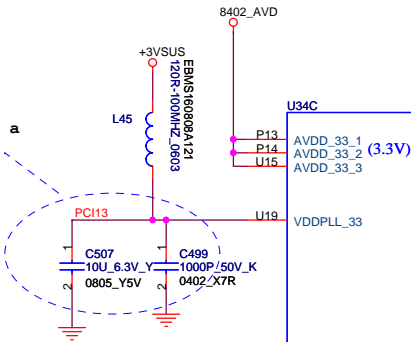




This array must be placed close to AVDD (Pin P13, P14, U15). They must be tied to a low-impedance GND.



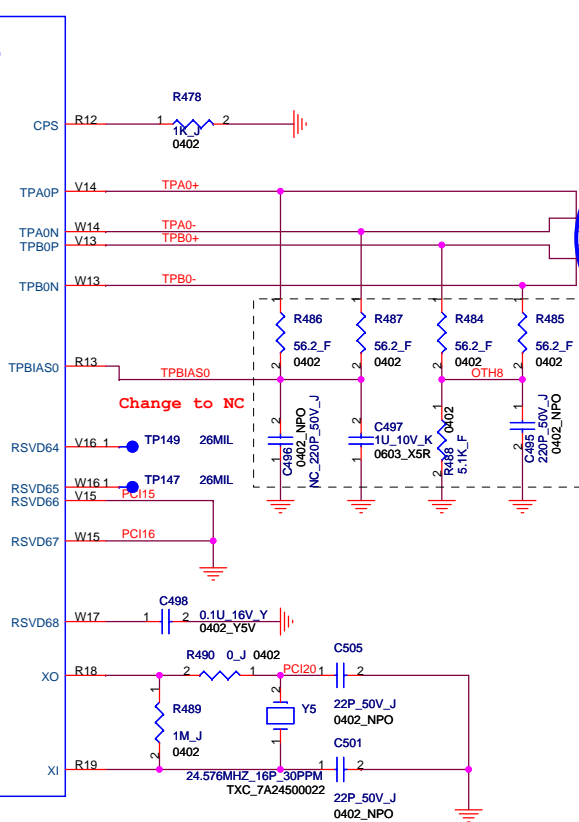
This array must be placed close to VDPLL (Pin U19)  
They must be tied to a low-impedance GND.



This capacitor should be placed between Pin P15 and Pin R17 .

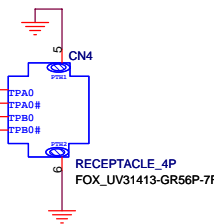
This capacitor must be placed to IC pin

VSSPLL must be tied to a low-impedance GND.



Place near PCI8402.

**iLink CONN.**



## Card BUS / 16-Bit PC Card Interface

### Clamp Voltage For PC CARD (IO 5V/3.3V)

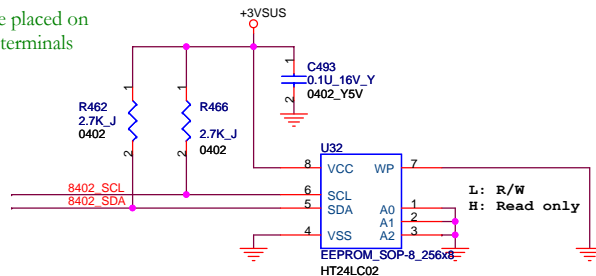
**Serial / Parallel  
PC Card Power Switch**

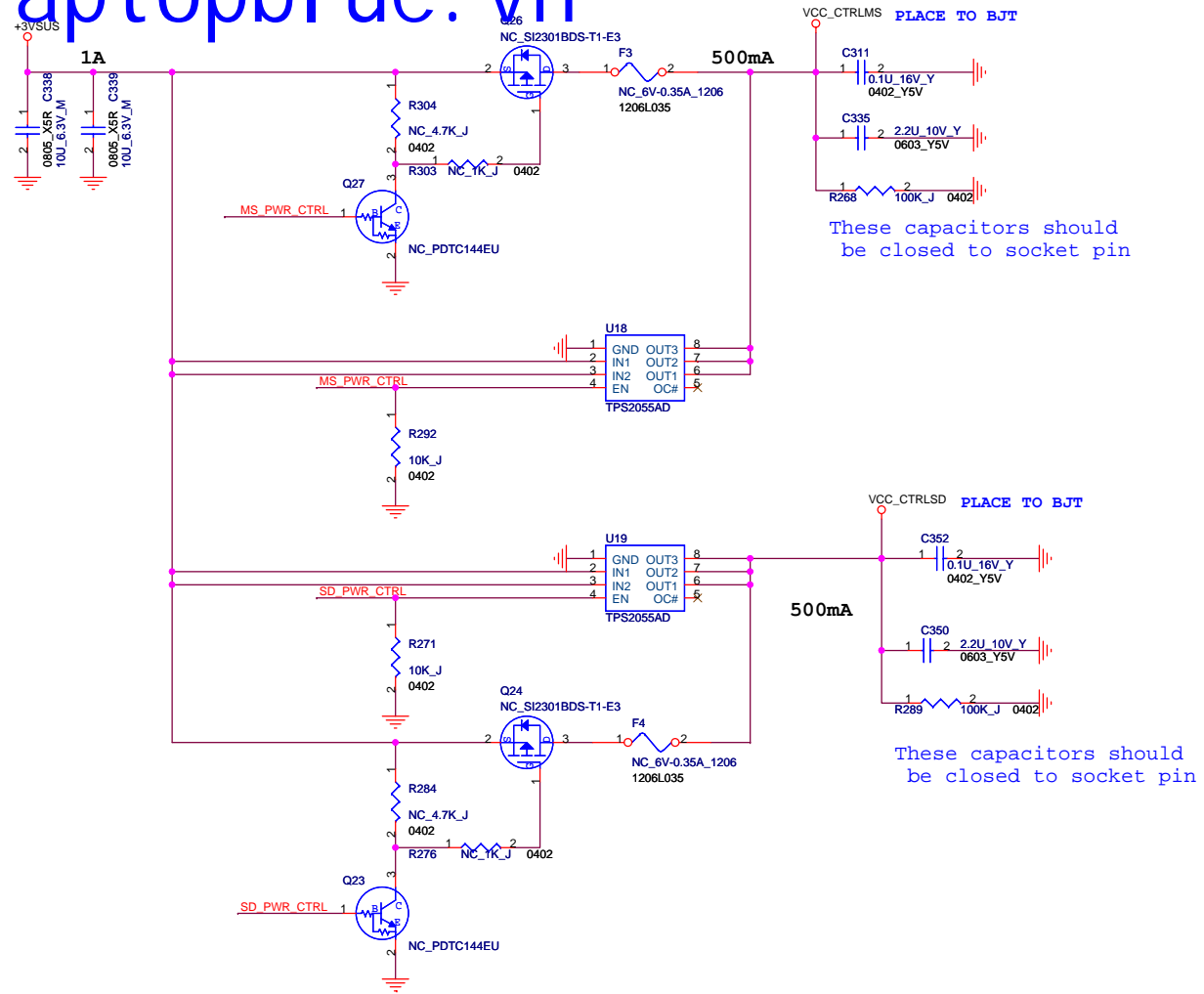
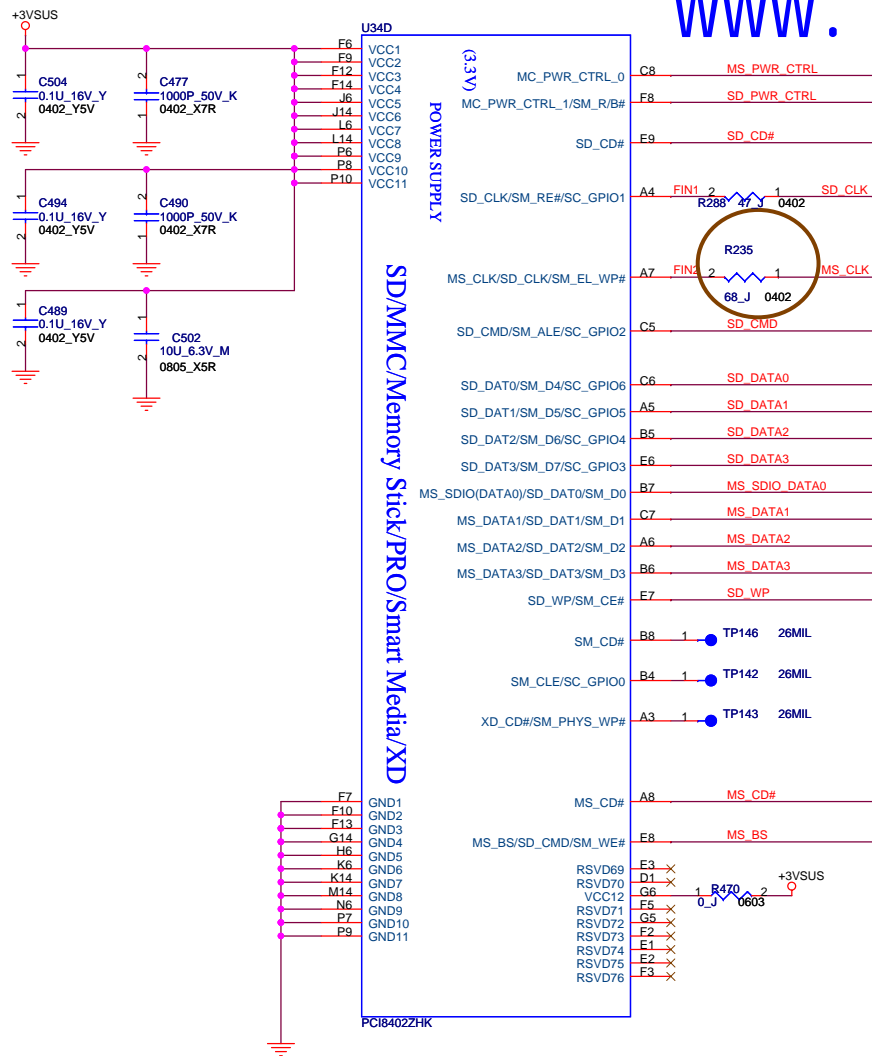
DATA/VD2/VPPD1  
LATCH/VD3/VPPD0  
CLOCK/VD1/VCCD0#  
RSVD/VD0/VCCD1#

PCI8402ZHK



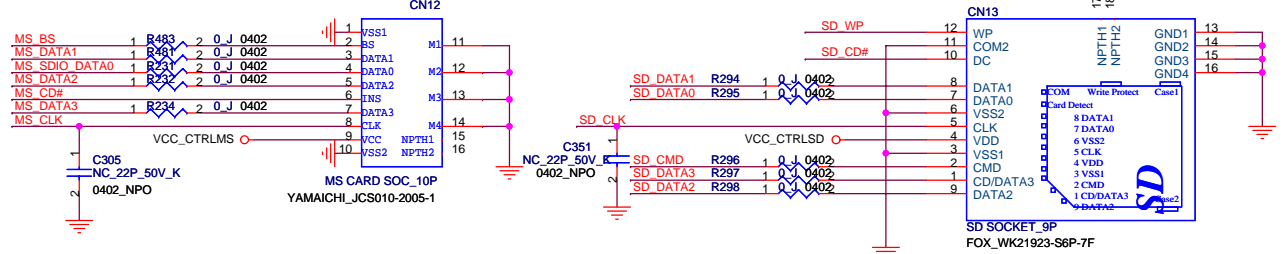
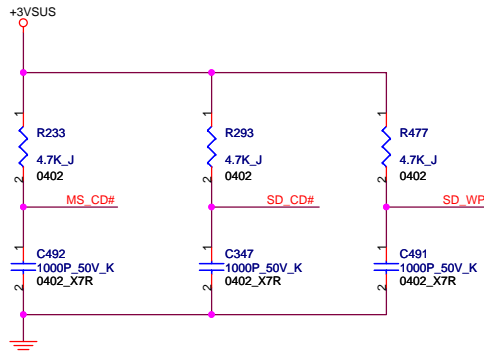
Resistors should be placed on the SCL and SDA terminals



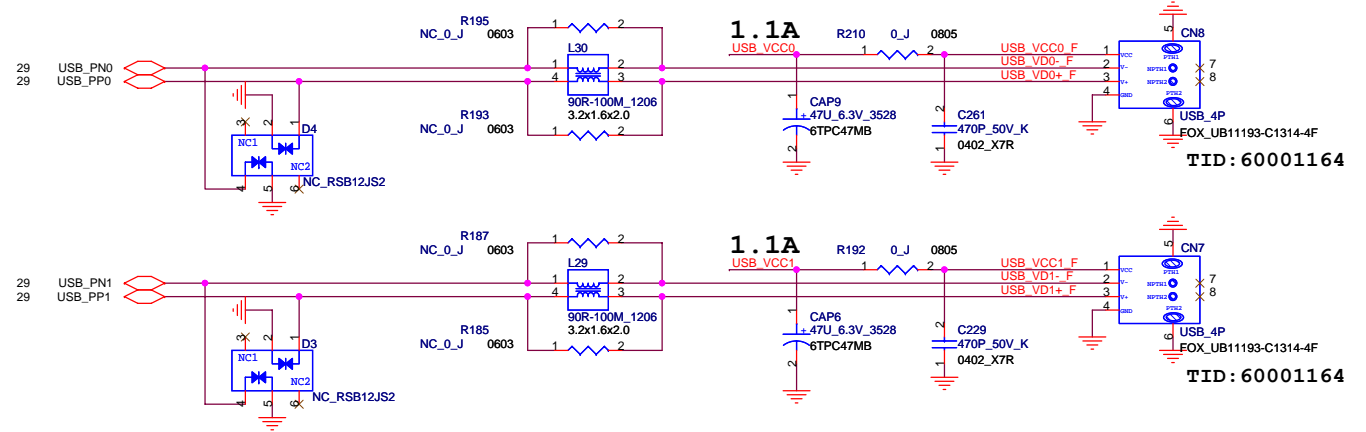
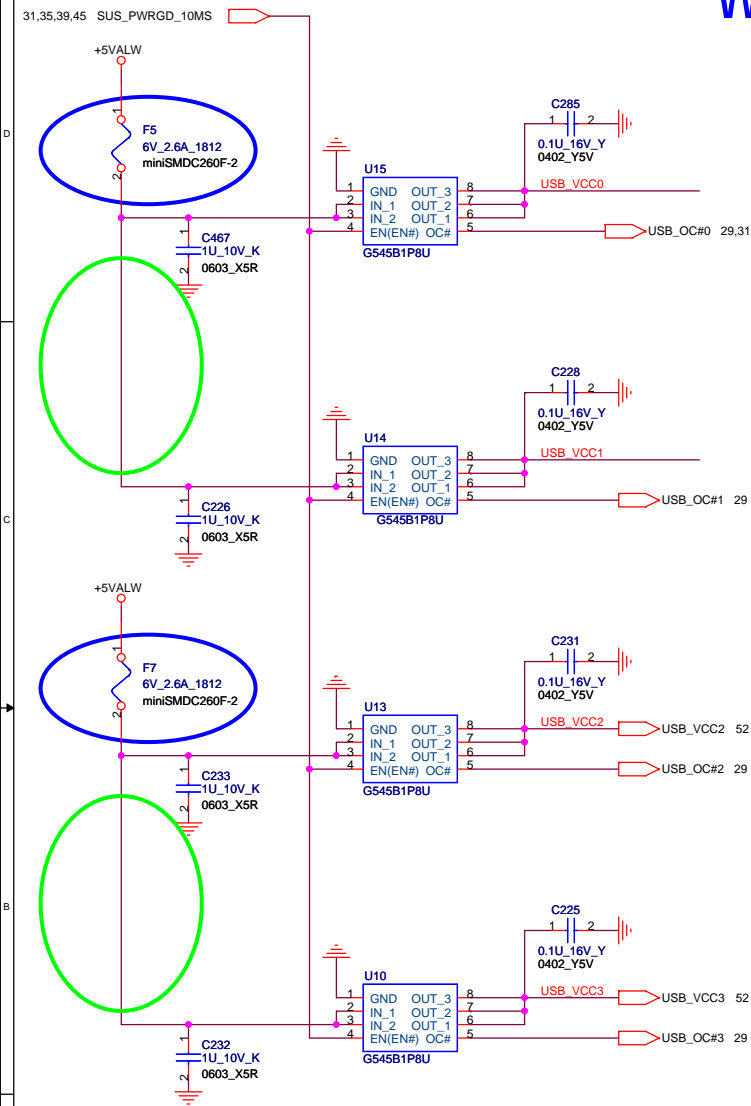


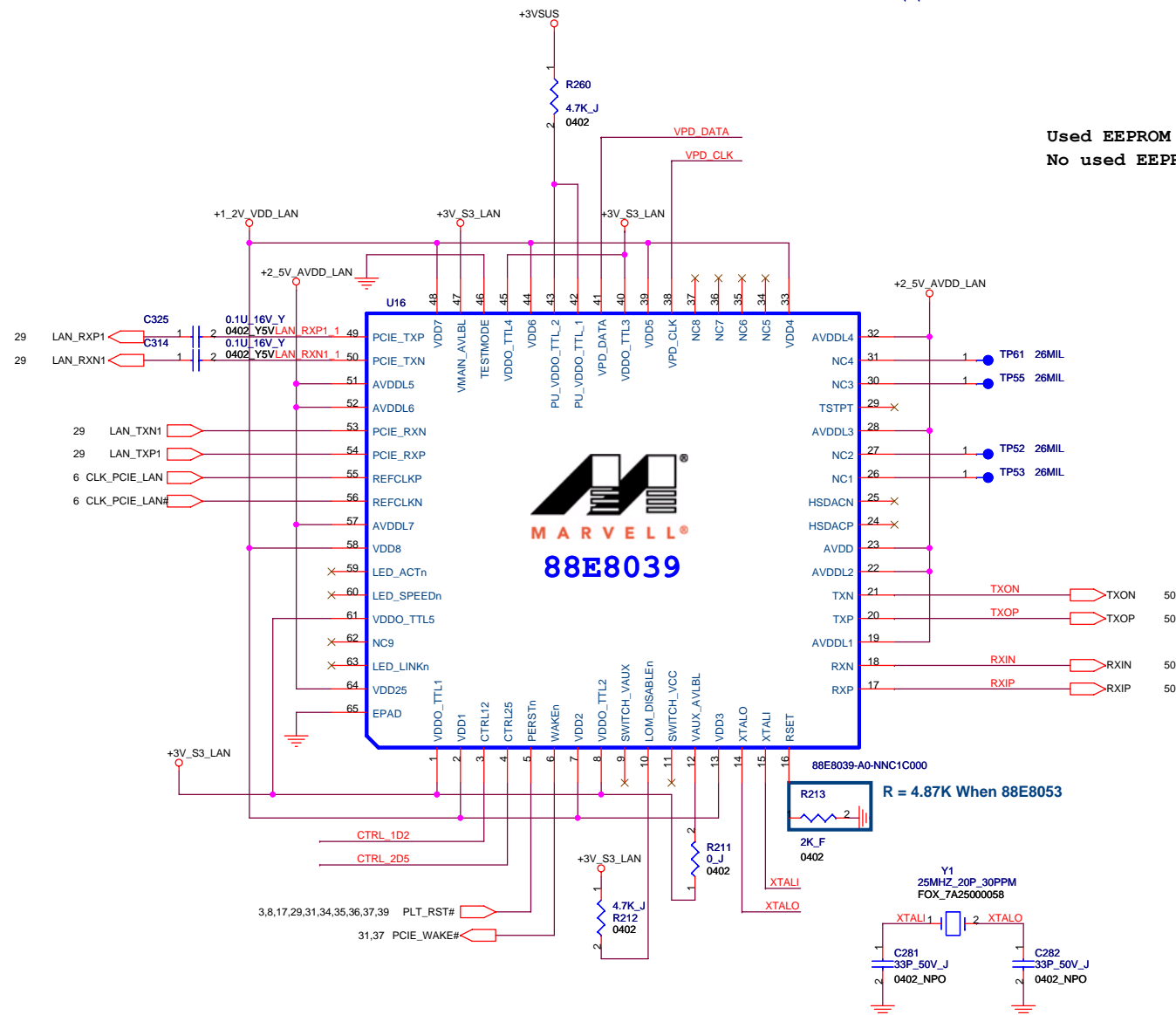
MS STD/DUO CONN.

SD CONN.

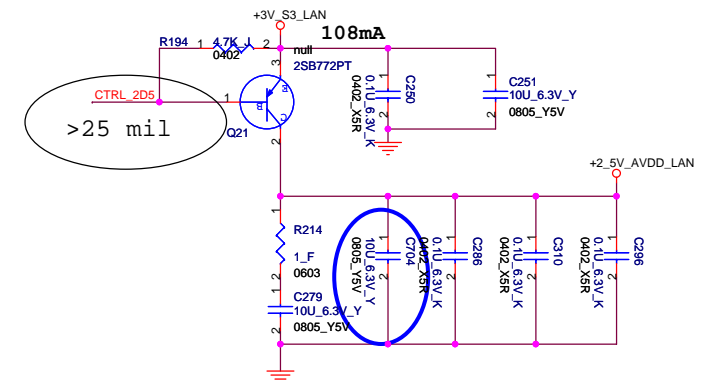
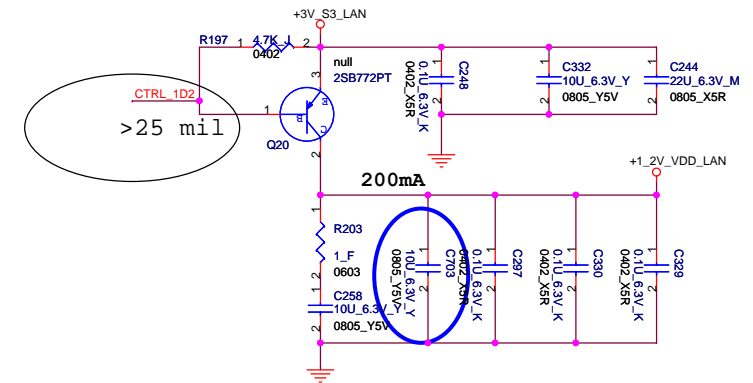
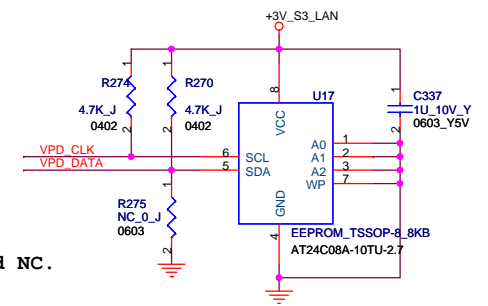


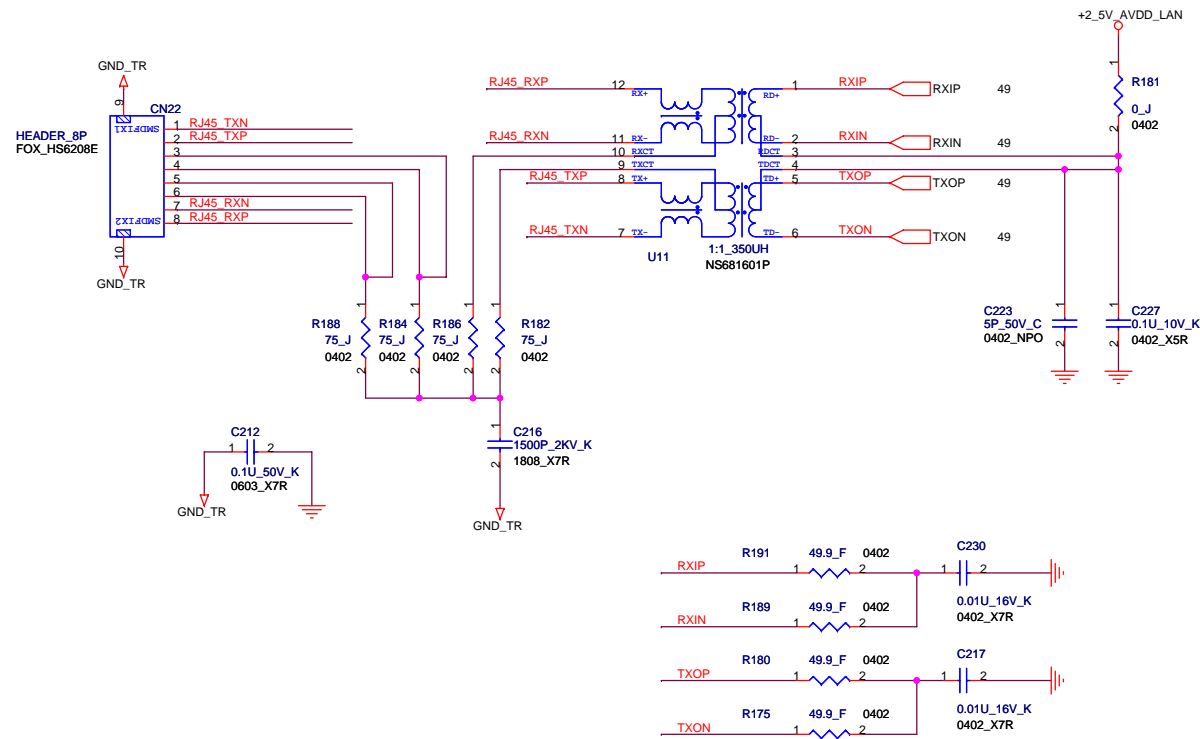
USB CONN.



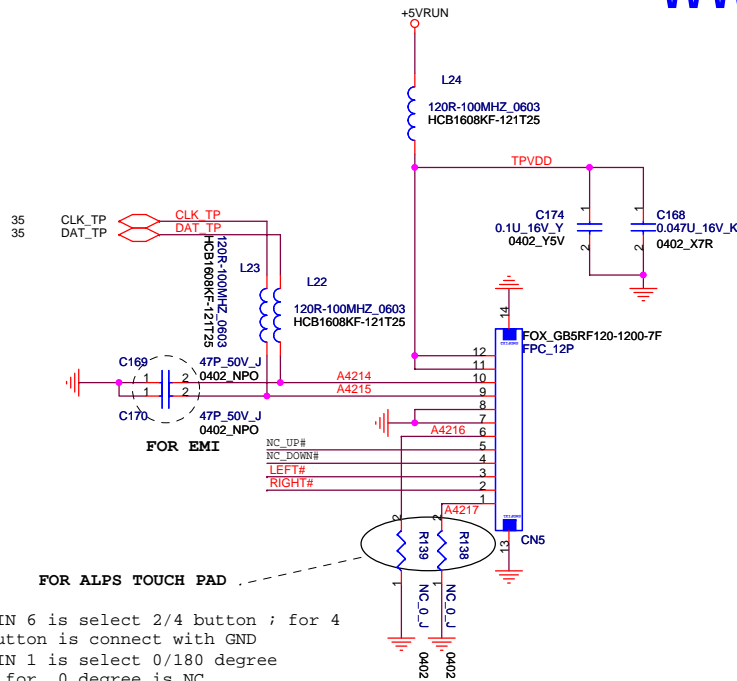


Used EEPROM R275 need NC.  
No used EEPROM R270/U17/C337 need NC.

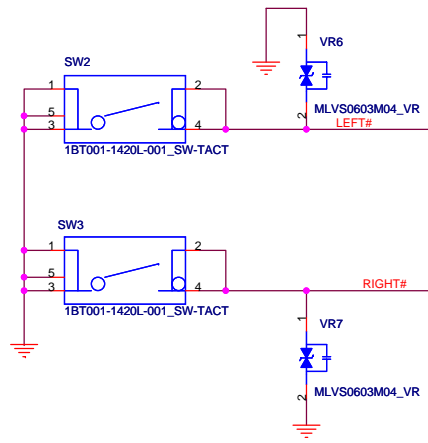




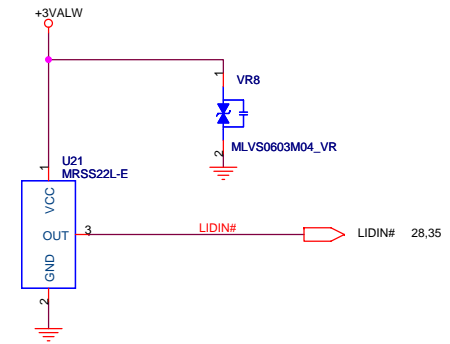
## Touch Pad CONN.



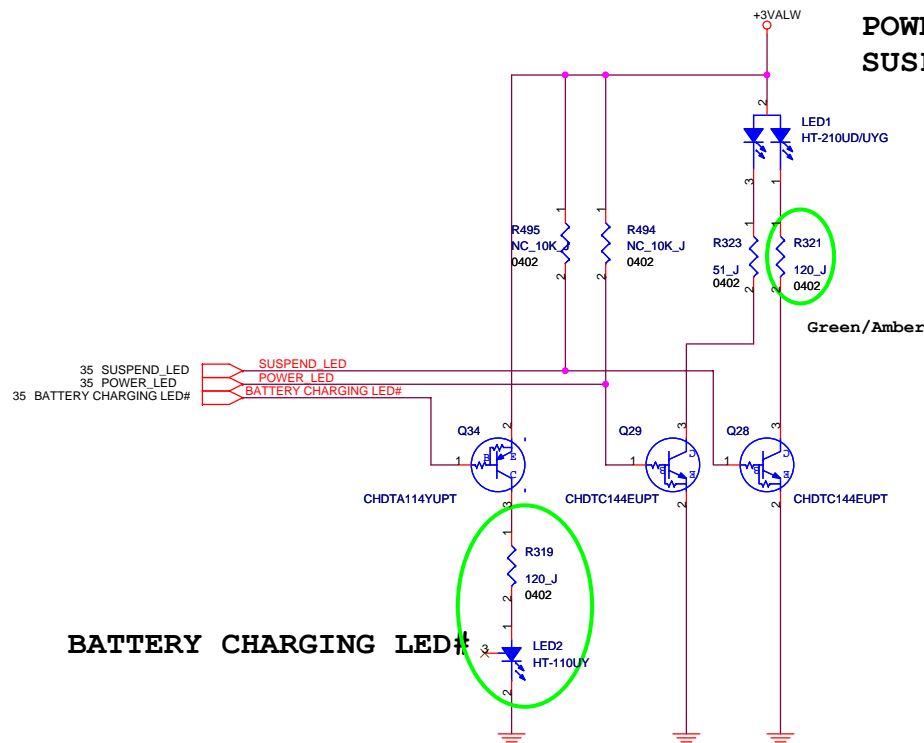
## TP\_Right Button



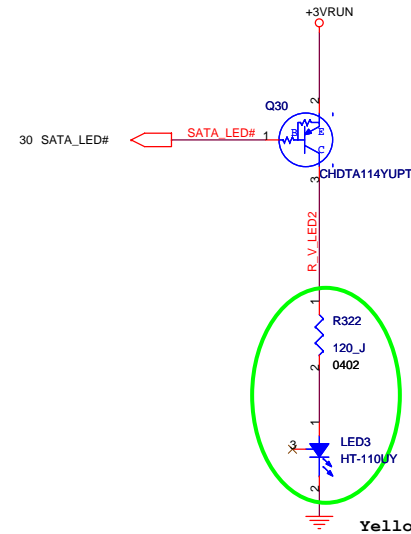
## LID Switch



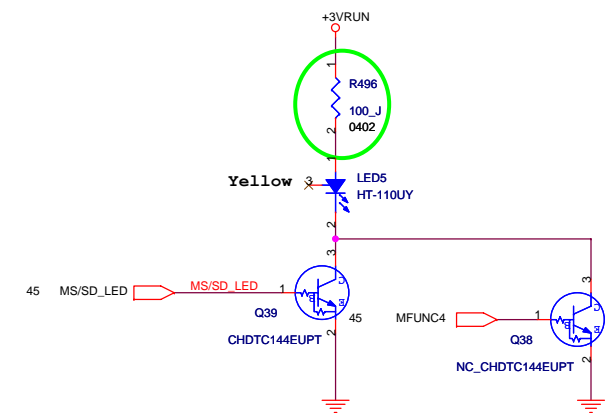
## POWER\_LED SUSPEND\_LED



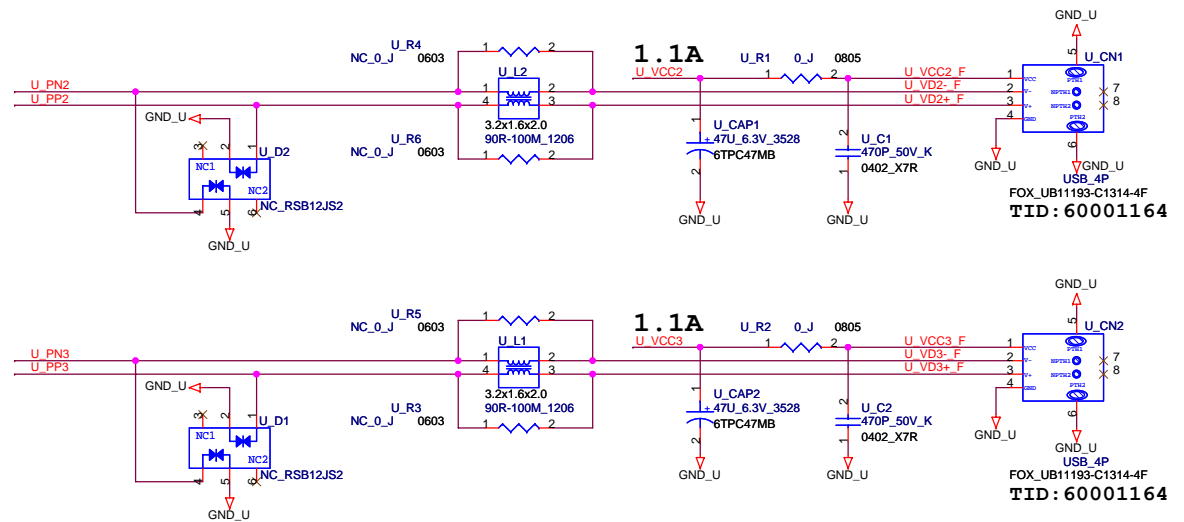
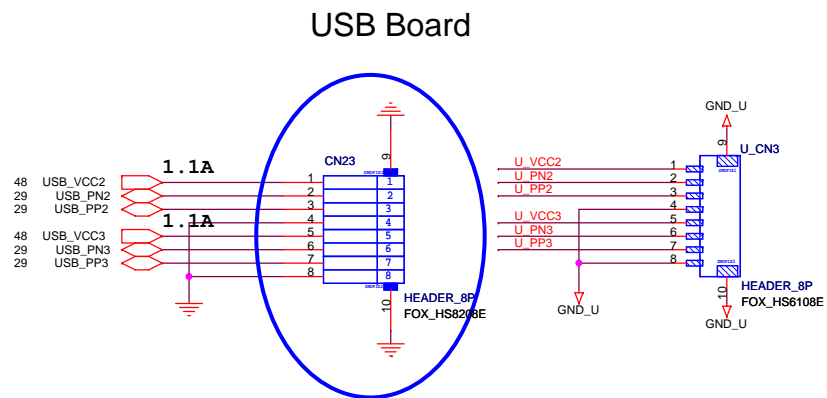
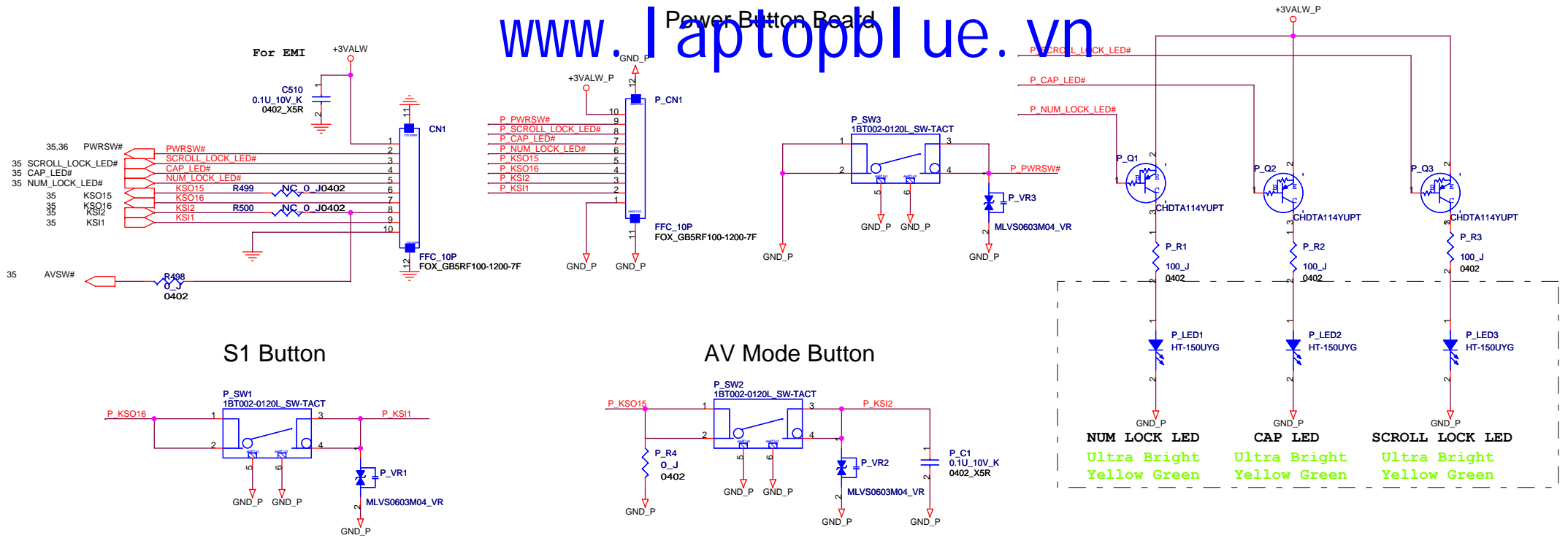
## SATA\_LED#

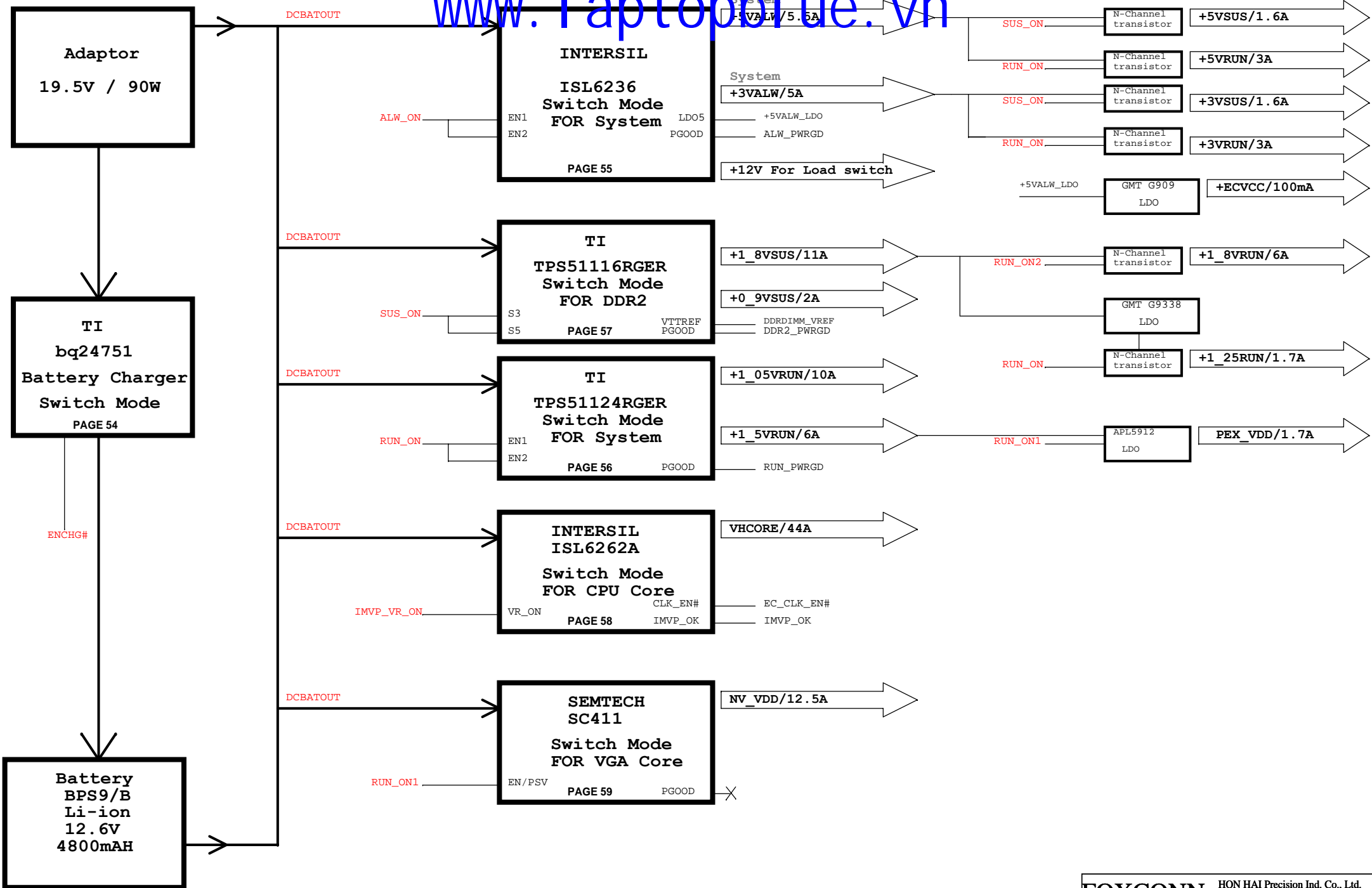


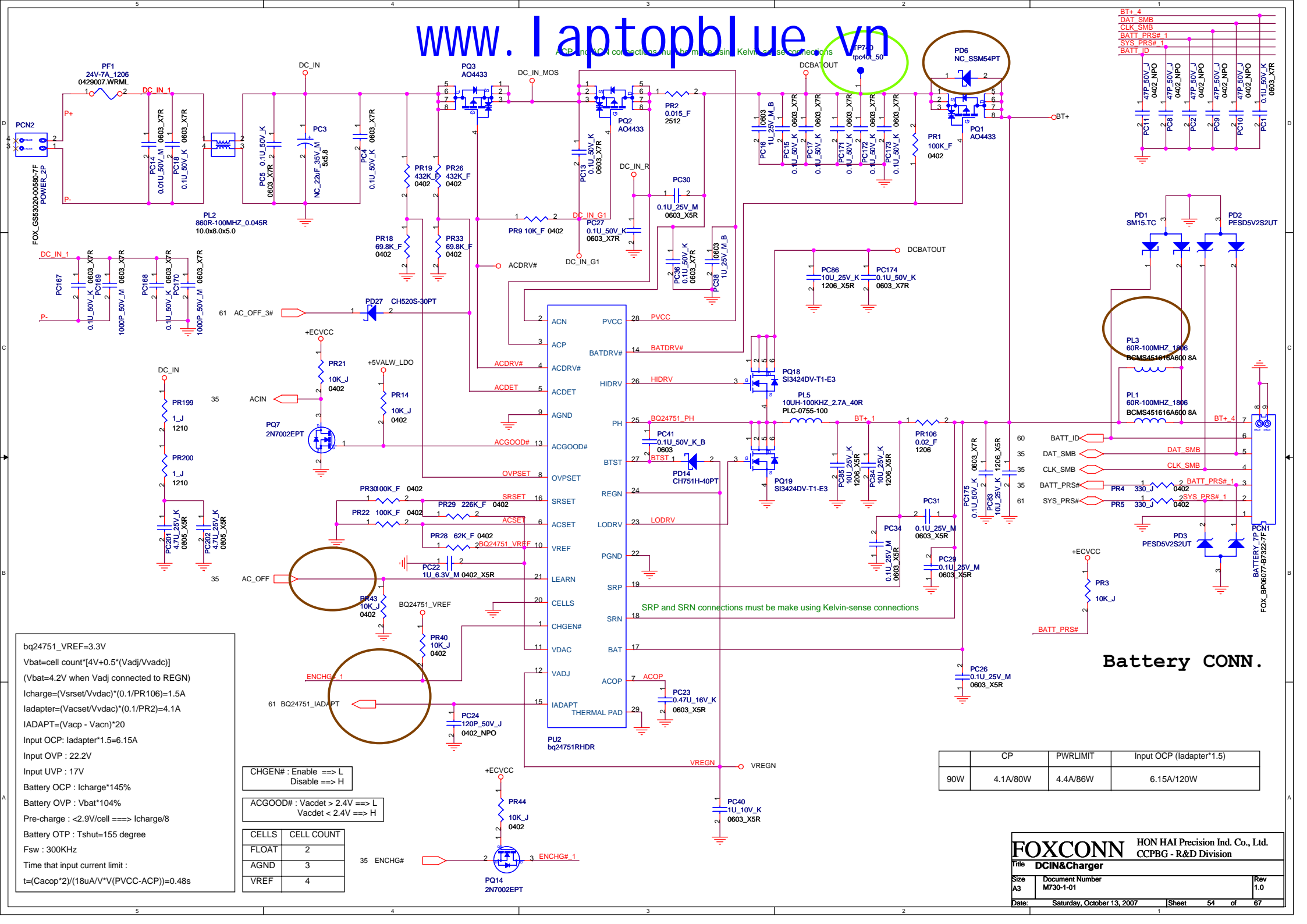
## MS/SD LED







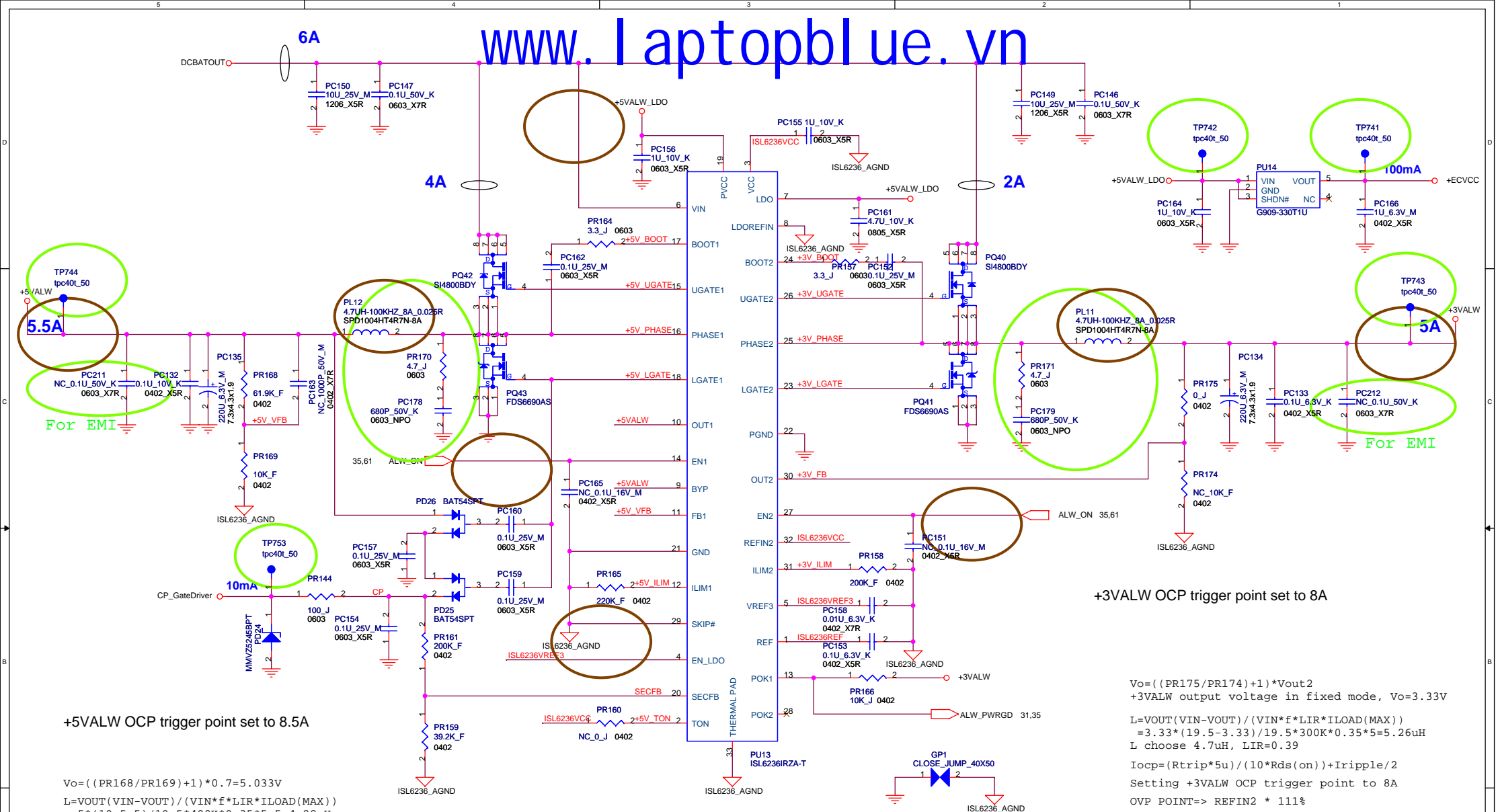




bq24751\_VREF=3.3V  
 $V_{bat} = \text{cell count} \times [4V + 0.5 \times (V_{adj} / V_{vdc})]$   
 $(V_{bat} = 4.2V \text{ when } V_{adj} \text{ connected to } REGN)$   
 $I_{charge} = (V_{srset} / V_{vdc}) \times (0.1 / PR106) = 1.5A$   
 $I_{adapter} = (V_{acset} / V_{vdc}) \times (0.1 / PR2) = 4.1A$   
 $I_{ADAPT} = (V_{acp} - V_{vacn}) \times 20$   
 Input OCP:  $I_{adapter} \times 1.5 = 6.15A$   
 Input OVP: 22.2V  
 Input UVP: 17V  
 Battery OCP:  $I_{charge} \times 145\%$   
 Battery OVP:  $V_{bat} \times 104\%$   
 Pre-charge:  $< 2.9V / \text{cell} \implies I_{charge} / 8$   
 Battery OTP:  $T_{shut} = 155 \text{ degree}$   
 $F_{sw} = 300KHz$   
 Time that input current limit:  
 $t = (C_{acop} \times 2) / (18uA \times V \times (V_{VCC} - ACP)) = 0.48s$

CHGEN# : Enable ==> L Disable ==> H	
ACGOOD# : Vacdet > 2.4V ==> L Vacdet < 2.4V ==> H	
CELLS	CELL COUNT
FLOAT	2
AGND	3
VREF	4

	CP	PWRLIMIT	Input OCP (Iadapter*1.5)
90W	4.1A/80W	4.4A/86W	6.15A/120W



+5VALW OCP trigger point set to 8.5A

Vo=((PR168/PR169)+1)\*0.7=5.033V

$$L = \frac{VOUT(VIN-VOUT)}{(VIN*f*LIR*ILOAD(MAX))} = \frac{5*(19.5-5)}{19.5*400K*0.35*5.5} = 4.82\mu H$$

L choose 4.7uH, LIR=0.36

$$Iocp = \frac{Rtrip*5u}{(10*Rds(on)) + Iripple/2}$$

Setting +5VALW OCP trigger point to 8.5A

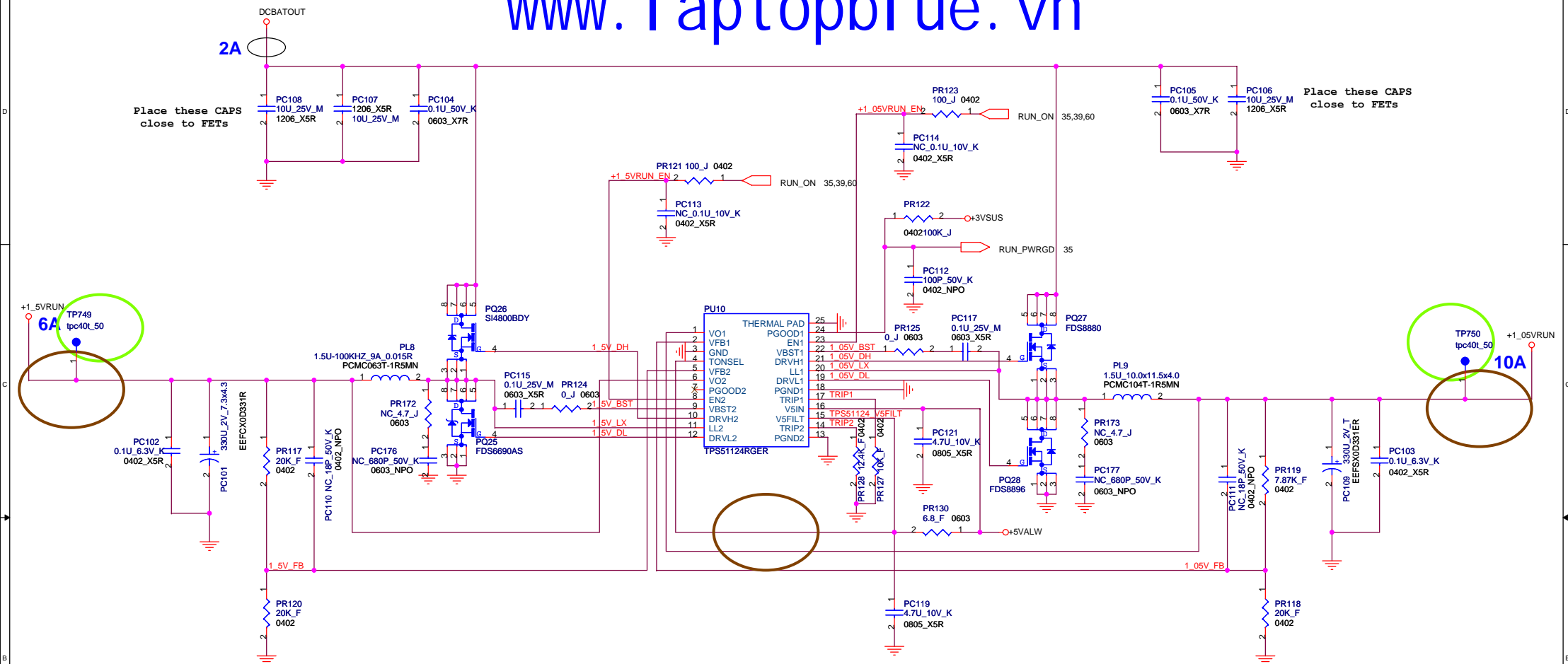
OVP POINT=> VFB \* 111%

UVP POINT=> VFB \* 70%

Switching Frequency = 400KHz

TON	Operating Frequency (+5VALW/+3VALW)
VCC	200KHz/300KHz
REF(OPEN)	400KHz/300KHz
GND	400KHz/500KHz

SKIP#	Operating Mode
GND	Pulse-Skipping
REF	Ultrasonic-Skip
VCC	PWM



Setting +1\_5VRUN OCP trigger point to 10.6A

$V_o = ((PR117/PR120)+1) \cdot 0.758 = 1.516V$   
 $L = VOUT(VIN - VOUT) / (VIN \cdot f \cdot LIR \cdot ILOAD(MAX))$   
 $= 1.5 \cdot (19.5 - 1.5) / 19.5 \cdot 420K \cdot 0.35 \cdot 6 = 1.57uH$   
 L choose 1.5uH, LIR=0.366  
 $I_{ocp} = (R_{trip} \cdot 10u) / R_{ds(on)} + I_{ripple} / 2$   
 Setting +1\_5VRUN OCP trigger point to 10.6A  
 OVP POINT=> VFB \* 115%  
 UVP POINT=> VFB \* 70%  
 Switching Frequency = 420KHz

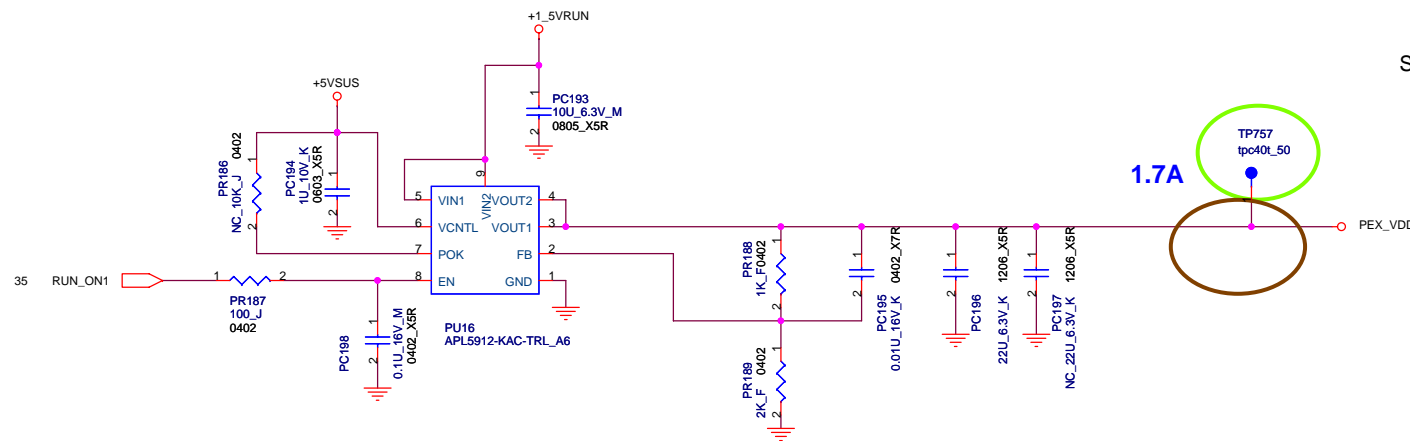
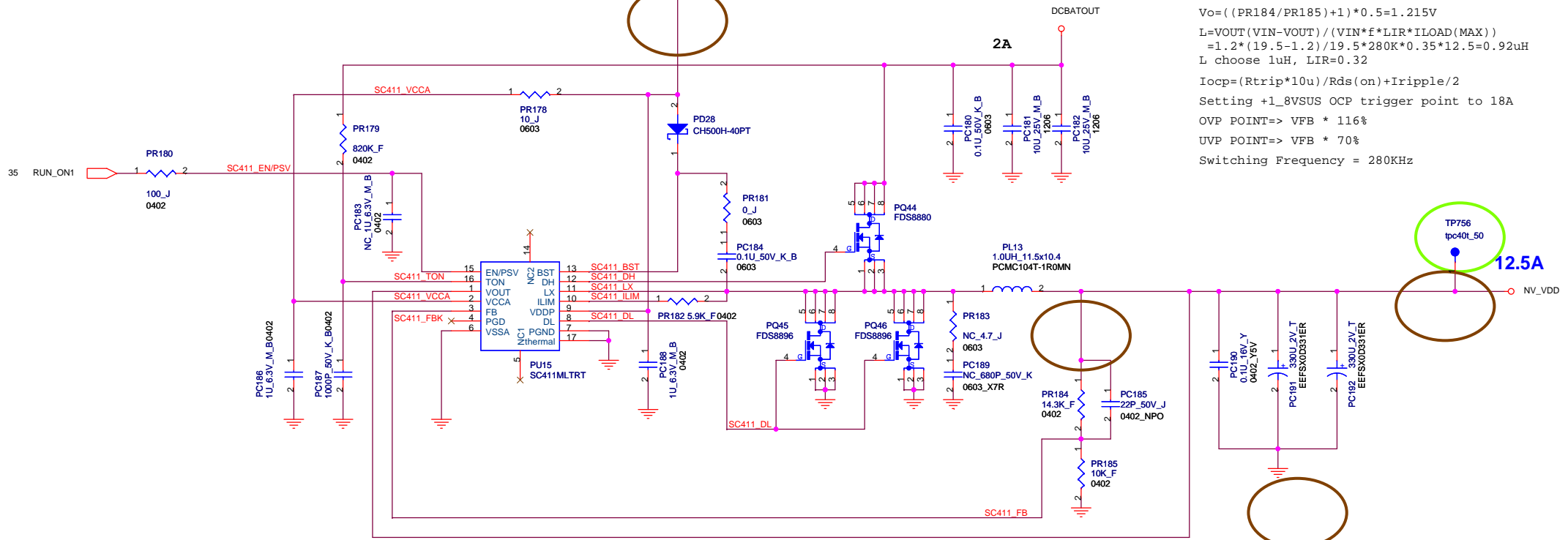
Setting +1\_05VRUN OCP trigger point to 14.6A

$V_o = ((PR119/PR118)+1) \cdot 0.758 = 1.056V$   
 $L = VOUT(VIN - VOUT) / (VIN \cdot f \cdot LIR \cdot ILOAD(MAX))$   
 $= 1.05 \cdot (19.5 - 1.05) / 19.5 \cdot 360K \cdot 0.35 \cdot 10 = 0.79uH$   
 L choose 1.5uH, LIR=0.18  
 $I_{ocp} = (R_{trip} \cdot 10u) / R_{ds(on)} + I_{ripple} / 2$   
 Setting +1\_05VRUN OCP trigger point to 14.6A  
 OVP POINT=> VFB \* 115%  
 UVP POINT=> VFB \* 70%  
 Switching Frequency = 360KHz

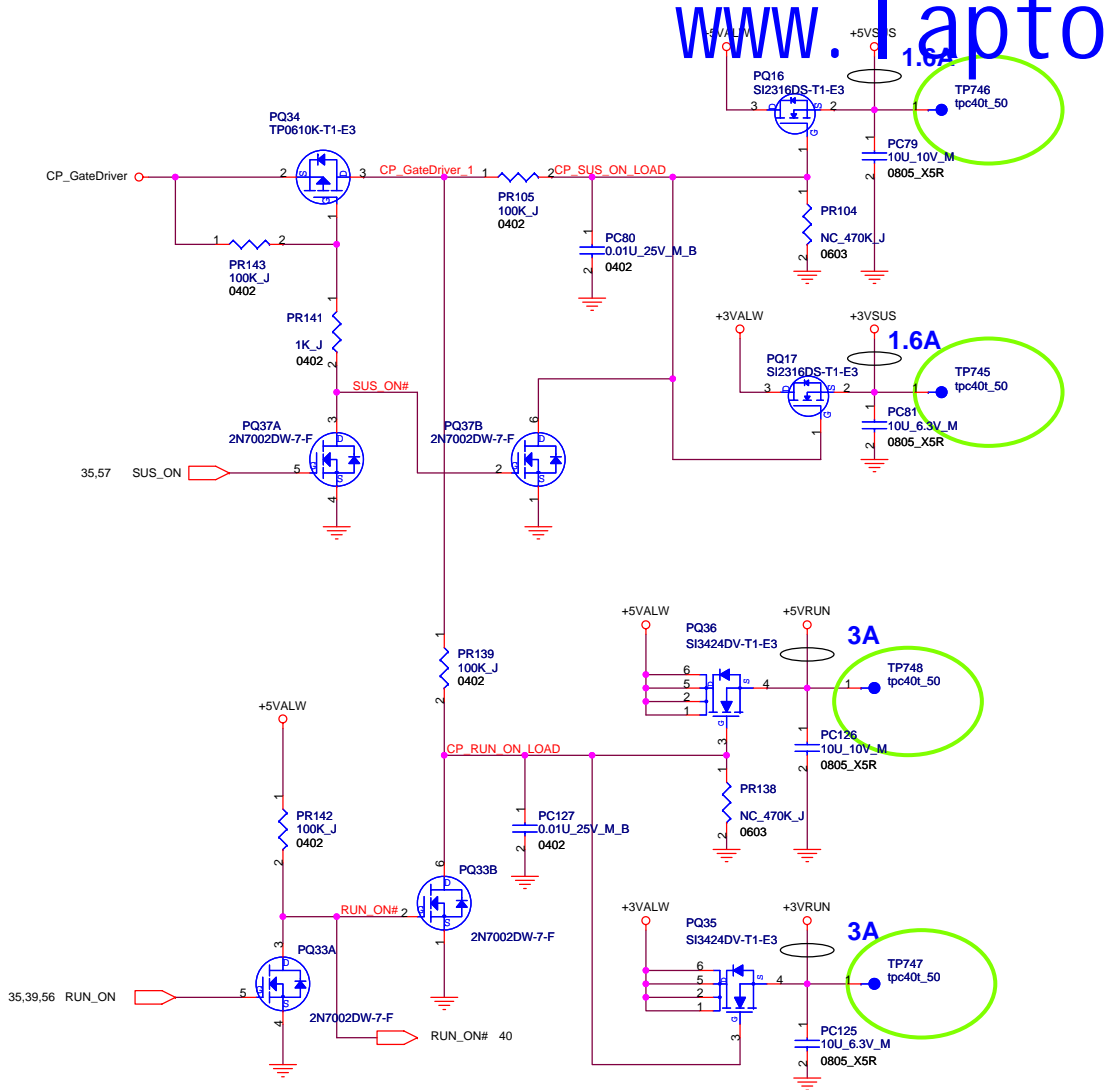




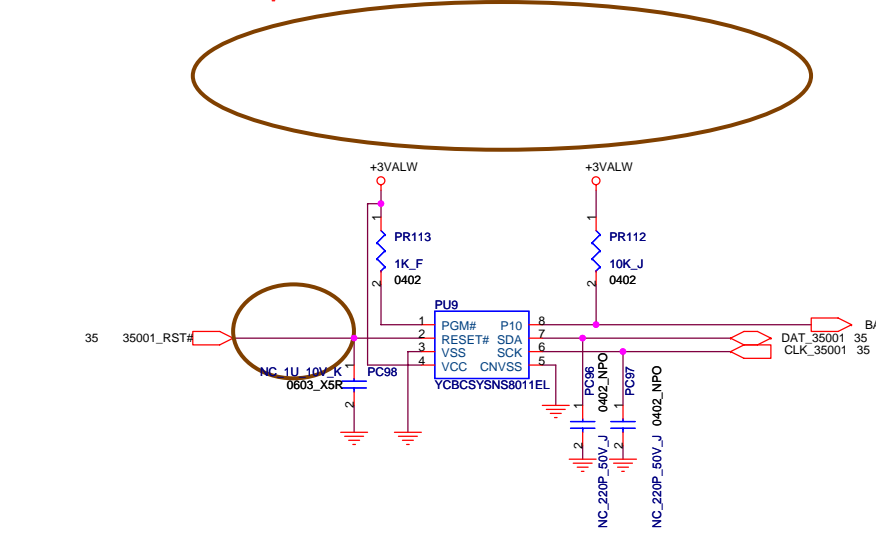
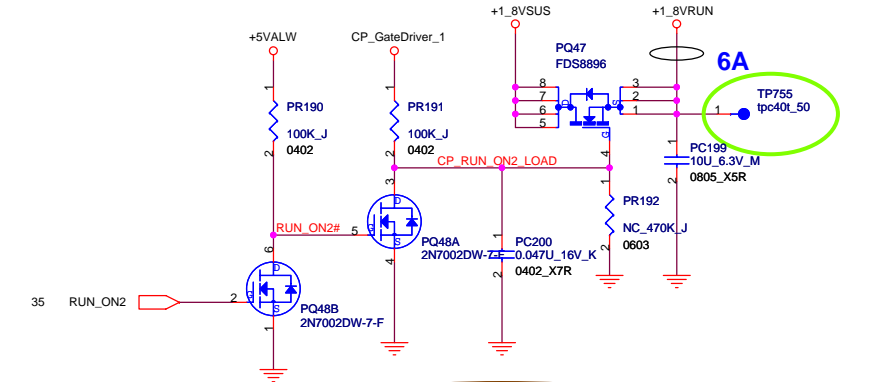
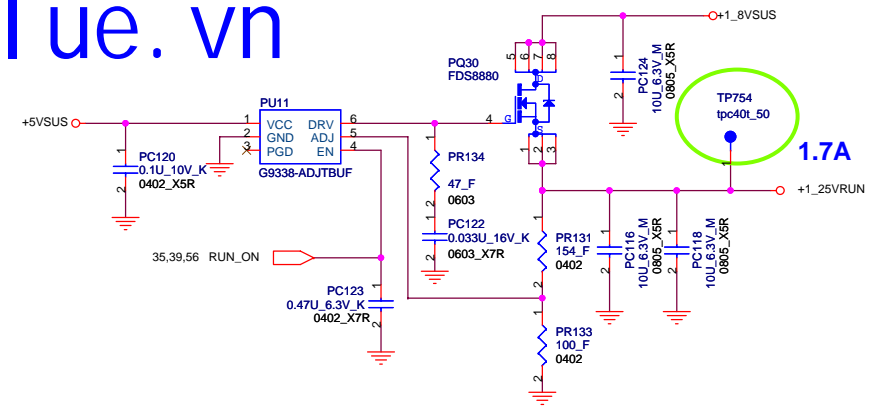
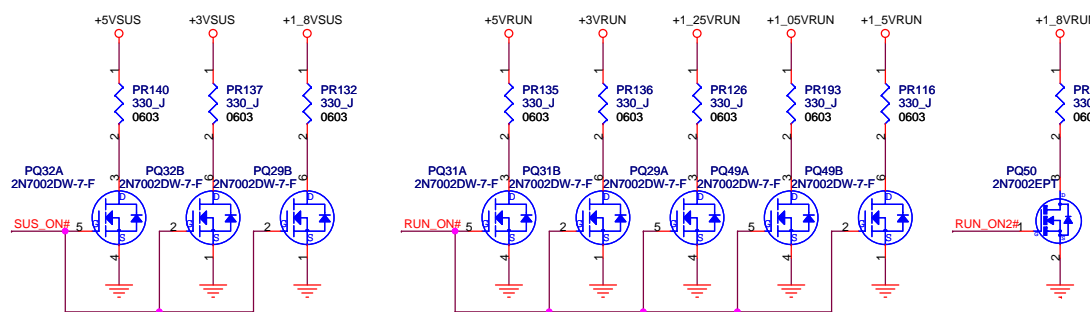


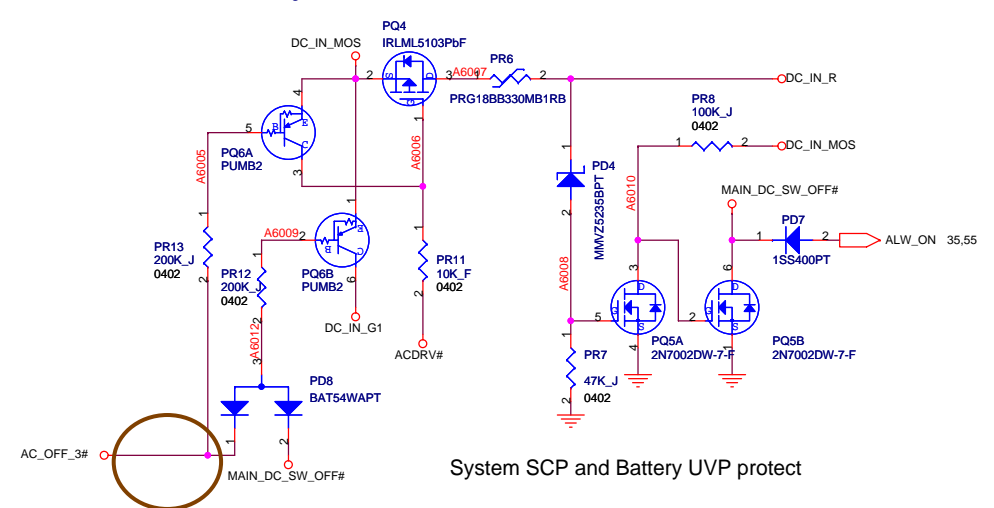
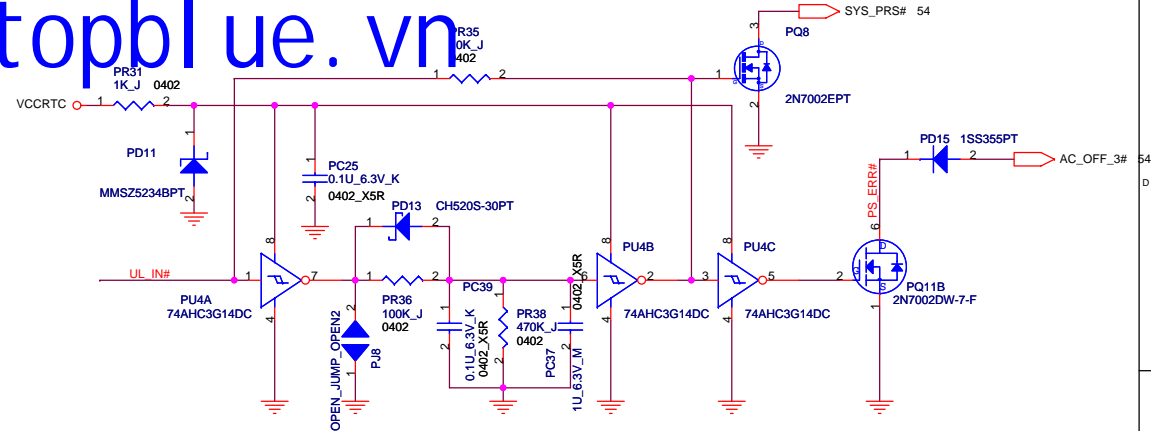
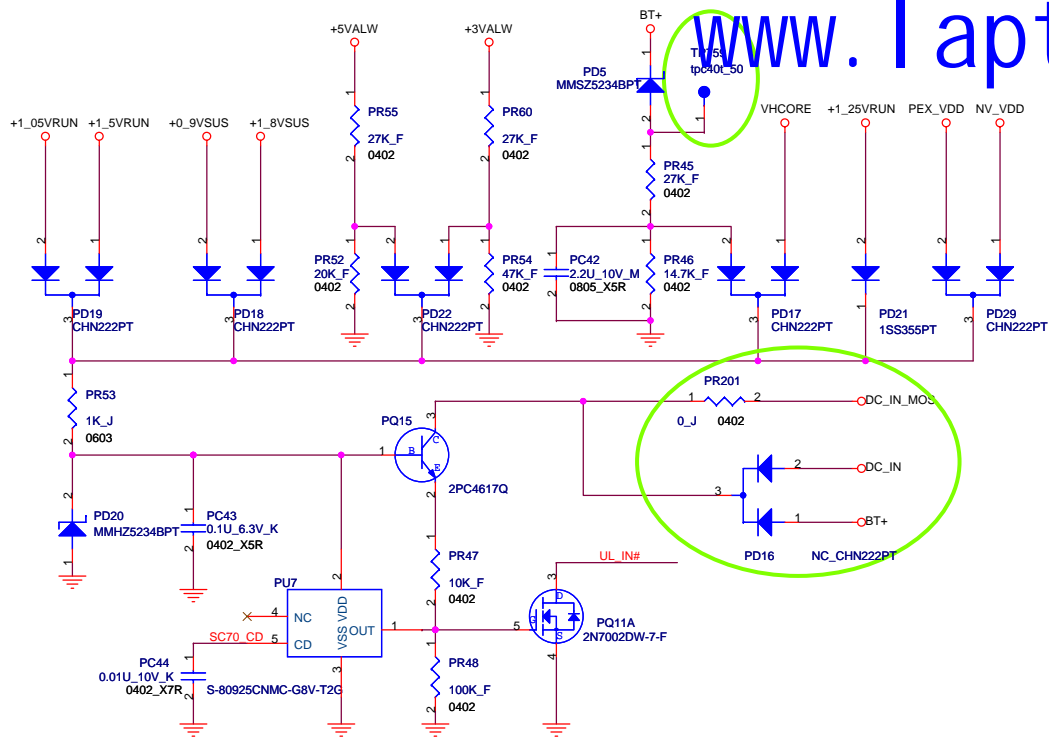


Setting +1\_8VSUS OCP trigger point to 16A

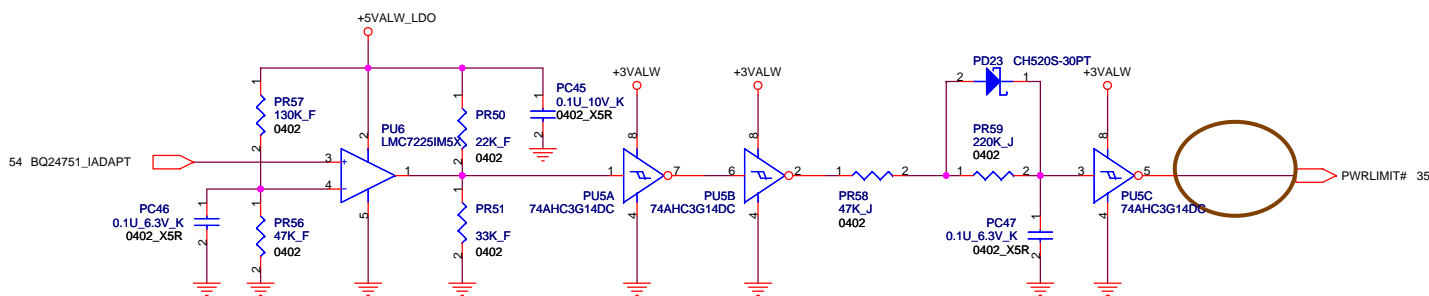


Discharge circuit for power-off

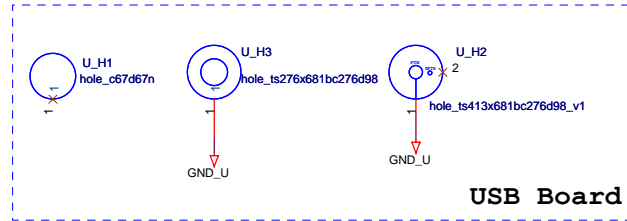
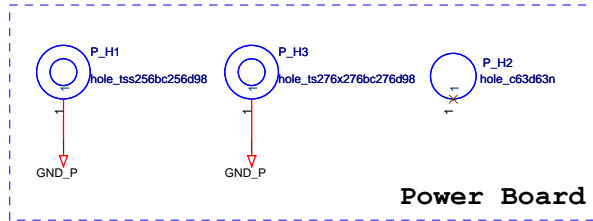
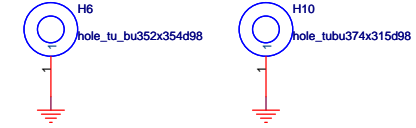
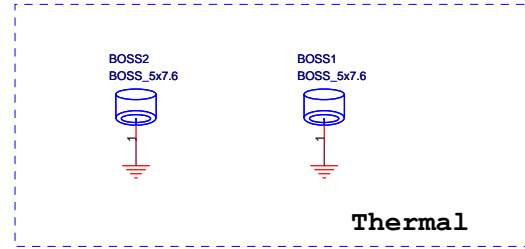
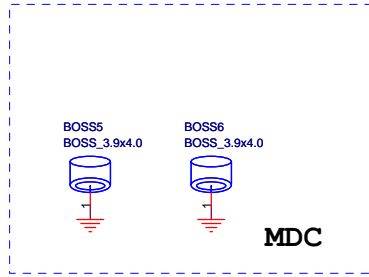
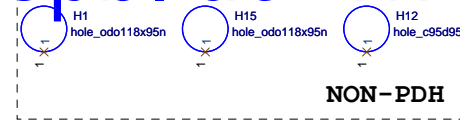
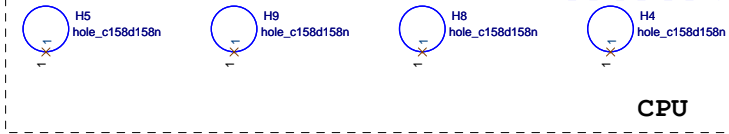




System SCP and Battery UVP protect



Setting PWRLIMIT# trigger point to 4.4A



## M730 EVT

### (2007/05/29)

Base on M720\_SCHEMATIC\_0528\_1700.

### (2007/05/30)

P.35 Add R607 for OVT\_GFX#

P.23 Add R604,R605 and R606 for IFPC/D power

### (2007/05/31)

P.40 Change R171 to 22ohm,C215 to 22uf.

P.42 Change C201,C202,C204 to X5R.

P.44 Delete U12,R183,R190 and C224 for remove memory thermal sensor solution.

P.9 Delete R366,R69,R74 and R81.

P.11 Delete Internal graphics power.

P.12 Delete Internal graphics power.

P.54 Change PR2 from 0.02\_F 2512 to 0.015\_F 2512 for 90W adapter application.

P.60 Change PQ47 from SI4800BDY to FDS8896

P.28 Add C702

### (2007/06/04)

P.54 Change PR28 from 44.2K\_F to 62K\_F for setting constant power trigger point to 4.1A

P.57 Change PR147 from 6.8K\_F to 10K\_F for setting +1\_8VSUS OCP trigger point to 16A

P.59 Change PR184 from 14K\_F to 14.3K\_F for setting NV\_VDD to 1.215V

P.59 Change PR182 from 6.8K\_F to 5.9K\_F for setting NV\_VDD OCP to 18A

P.59 Add PR197, PR198 0\_J for NV\_VDD feedback remote sense.

P.61 Change PR56 from 53.6K\_F to 47K\_F for setting PWRLIMIT trigger point to 4.4A.

### (2007/06/05)

P.54 Change PQ18 and PQ19 from SI4800BDY to SI3424DV for layout space.

P.54 Change PC24 from 120pF 10% to 120pF 5% for purchase difficult.

P.60 Change PQ35 and PQ36 from SI4800BDY to SI3424DV for layout space.

### (2007/06/08)

P.62 Add BOSS7 and BOSS8 for thermal request

### (2007/06/14)

P.9 Change R97 to NC

P.9 Add R608/R609 and NC for LVDS\_VREFH and LVDS\_VREFL

P.8 Add TP731,TP732,TP733,TP734,TP735 for GFX\_VID[3:0] and GFX\_VR\_EN

### (2007/06/22)

P.19 Net I2CS\_SDA & I2CS\_SCL exchange with TP632 & TP633

P.22 Q40,Q41,Q42,Q43,R575,R576,R582 and R583 change from NC to mount for Nvidia save power function

P.24 Add and NC Q44,R610 for Nvidia save power function reserve

P.34 CAP7 change from 1C-41S0476-M000 to 1C-41R0476-M200 for layout convenient

P.62 Delete BOSS7,BOOS8 for ME request

### (2007/06/23)

P.62 H14 change to 1X-HOLE000-0474 for ME request

P.62 H17 change to 1X-HOLE000-0473 for ME request

### (2007/06/25)

P.62 Update H14 screw hole pad.

P.34 Change CAP7 to mount, and C275 to no mount for M720 HDD noise issue.

P.38 Update FeliCa pin define for M720 A'SSY issue.

P.49 Add C703,C704 for M720 LAN noise issue.

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### (2007/06/28)

P.57 Delete PR15 0ohm for application note.

P.58 Change PC57 from 170pF 10% to 270pF 5% for purchase difficult.

P.58 Add TP736, TP737, TP738 and TP739 test pin for application note.

P.56 PL8 change from 1L-DSPD100-4H02 to 1T-00001U5-0000 for layout convenient.

### (2007/06/29)

P.22 Delete R569 and add R611 for mirror function off.

P.22 Modify address and command signals of U39 for mirror function off.

### (2007/07/02)

P.22 R577,R578,R573,R574 change from 4.3k to 1.05k for nVidia's suggestion.

P.22 R582,R583,R575,R576 change from 4.02k to 1.82k for nVidia's suggestion.

P.22 R584,R585,R579,R580 change from 10k to 2.49k for nVidia's suggestion.

P.28 Add R612 and NC R596,U40 for GPIO3 of GPU is active high which is nVidia's suggestion.

### (2007/07/03)

P.37 Change LED4 to HT-110YG for M720 LED issue.

P.51 Change R321,R323 to 51ohm,LED2,LED3 to HT-110Y for M720 LED issue.

P.48 Change F5~F8 to 2.6A poly-switch for M720 USB loading and noise issue.

P.52 Change CN23 to HS-8208E for M720 USB loading and noise issue.

### (2007/07/05)

P.11 L28 change to 1uH/220mA for M720 component spec. issue.

P.08 Delete C509 for layout convenient.

P.46 Change L27 to SINKA OD6560T-E900T for purchase difficult.

P.28 NC R612 and mount R596,U40 for GPIO3 of GPU is set active low which is the same as MS90.

P.22 Swap data signals of VRAM for layout convenient.

### (2007/07/06)

P.54 Change PC3 from mount to dummy for M720 application note.

P.54 Change PC38 from 4.7uF\_25V 0805 to 1uF\_25V 0603 for M720 application note.

P.54 Remove PR176 10\_J for M720 application note.

P.54 Add PR199, PR200 1\_J 1206 and PC201, PC202 4.7uF\_25V 0805 for M720 DC\_IN RC snubber circuit.

P.38 L25 change from BK1608LL121-T to TB160808B121 for purchase difficult.

P.54 PL1,PL3 change from BLM41PG600SN1L to BCMS451616A600-8A for purchase difficult.

P.05 CAP3 change from EEFSLOD331EY to 2R5TPE330M9 for purchase difficult.

P.12 CAP14 change from EEFSLOD331EY to 2R5TPE330M9 for purchase difficult.

### (2007/07/09)

P.54 Change PR199, PR200 form 1206 to 1210 for M720 power rating safety.

P.05 CAP3 change back to EEFSLOD331EY for purchase difficult.

P.12 CAP14 change back to EEFSLOD331EY for purchase difficult.

### (2007/07/10)

P.11 L28 change to EBLS2012-1R0M 0.25A for M720 component spec. issue.

### (2007/07/11)

P.28 Add L55 for M720 EMI issue.

P.41 Delete VR2~VR5 and add C705~C708(NC) for M720 EMI issue.

FOXCONN			HON HAI Precision Ind. Co., Ltd.	
Title History (1)			CCPBG - R&D Division	
Size	Document Number		Rev	
A3	M730-1-01		1.0	
Date:	Saturday, October 13, 2007		Sheet	63 of 67

**(2007/07/12)**

P.54 Add PJ9 for application.  
P.55 PR170,PR171,PC178,PC179 change to NC for application.  
P.59 PR183,PC189 change to NC for application.  
P.22 Change Q40~Q43 and R575,R576,R582,R583 to NC for customer request.  
P.06 Add C709,C710 and reserve for EMI application.  
P.57 Add PC203~PC210 and reserve for EMI application.  
P.35 Add C711,C712 and reserve for EMI application.  
P.38 Add C713 and reserve for EMI application.

**(2007/07/13)**

P.40 Add J2 for EMI application.

**(2007/07/16)**

P.42 Change C455,C445 to 10uF,R167,R149 to 20 Kohm for M720 MIC. THD+N issue.  
P.35 Change R382 to mount and R390 to NC for system ID modification.  
P.54 PR199,PR200 change to 1/3 W for PUR issue.

**(2007/07/17)**

P.37 Change LED4 to HT-110UYG for M720 MOR request.

**(2007/07/20)**

P.41 Change R105 to 6.2Kohm for M720 audio issue.

**M730 DVT****(2007/07/27)**

P.48 Delete F6,F8 for MOR's request.  
P.61 Change PD16 from mount to NC, add PR201 0ohm for application.  
P.06 Modify R350 pin1 connection from GND to +3VRUN for GPU select 27MHz issue.

**(2007/08/13)**

P.51 Change LED2,LED3 from HT-110Y to HT-110UY  
Change R319,R322 from 47ohm to 120ohm and R321 from 51ohm to 120ohm  
Change R496 from 47ohm to 100ohm for M720 LED brightness request from MOR

**(2007/08/14)**

Add test pin TP740~TP772 for power test jig.

**(2007/08/17)**

P.34 Add CAP21 for +5VRUN noise issue of ODD  
P.41 Add CAP22 for +5VAMP noise issue of CODEC  
C127 change from no mount to mount for +5VAMP noise issue of CODEC  
P.25 Add C714/C715 for PEX\_PLL\_AVDD/PEX\_PLL\_DVDD noise issue

**(2007/08/23)**

P.38 NC R152,R151,F2,L25,C185,C186,CN6 for no Felica SKU  
P.44 U27 change from GMT G781-1P8f to SMSC EMC1402-2-ACZL for Penryn CPU concern

**(2007/08/25)**

P.62 H3 change to 1X-HOLE000-0519 for ME's request

**(2007/08/28)**

P.55 PL11,PL12 change from SPD1004HT4R7N-8A to PCMC063T-4R7MN  
for ME interference issue.  
P.55 PR170,PR171,PC178,PC179 change from NC to mount for EMI issue.  
P.57 PR145 change from 3.3ohm to 4.7ohm and PC131 change from 1000P to 680P  
for EMI issue.

**(2007/08/28)**

P.38 Add and reserve C716,C717,C718 0603 cap for EMI solution.  
P.56 Add and reserve PC211,PC212 0603 cap for EMI solution.  
P.57 Add and reserve PC213 0603 cap for EMI solution.  
P.58 Add and reserve PC214~PC218 0603 cap for EMI solution.

**M730 PVT****(2007/09/27)**

P.54 Delete PJ9 for application.  
P.54 Change PD6 from mount to NC for UL\_Lock issue.  
P.54 Delete PR25, PR41, PR42 for application.  
P.55 PL11,PL12 change from PCMC063T-4R7MN to SPD1004HT4R7N-8A  
for MOR request.  
P.55 Delete PJ4, PJ5 for application.  
P.55 Delete PR155, PR156, PR162, PR163, PR167 for application.  
P.56 Delete PJ1, PJ2 for application.  
P.56 Delete PR129 for application.  
P.57 Delete PJ3 for application.  
P.58 Delete PR70, PR71, PR84, PR86, PR90, PR93, PR94, PR96, PR97, PR99,  
PR102 for application.  
P.59 Delete PJ6, PJ7 for application.  
P.59 Delete PR177, PR197, PR198 for application.  
P.60 Delete PR110, PR111, PR114 for application.  
P.61 Delete PR20, PR49 for application.

**(2007/10/17)**

P.25 Add netname "J6" for U35 Pin J6 for application.

**(2007/10/19)**

P.47 Change R235 from 47ohm to 68ohm for MS Card Media-C  
MS\_CLK undershoot issue

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title <b>History ( 2 )</b>			
Size A3	Document Number M730-1-01		Rev 1.0
Date:	Friday, October 19, 2007	Sheet 64 of	67



www.laptopblue.vn

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title <b>History ( 3 )</b>			
Size A3	Document Number M730-1-01		Rev 1.0
Date:	Saturday, October 13, 2007	Sheet 65 of	67

www.laptopblue.vn

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title <b>History (4)</b>			
Size A3	Document Number M730-1-01		Rev 1.0
Date:	Saturday, October 13, 2007	Sheet 66 of 67	

www.laptopblue.vn

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title <b>History ( 5 )</b>			
Size A3	Document Number M730-1-01		Rev 1.0
Date:	Saturday, October 13, 2007	Sheet 67 of	67