

# Schematics Page Index (Title / Revision / Change Date)

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Project Code & Schematics Subject: M850 Main Board\_8L

PCB P/N: 1P-0094J00-8011(IRIS)  
1P-0094500-8011(HANNSTAR)

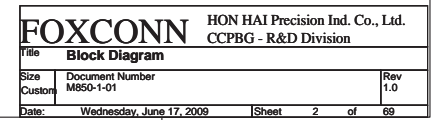
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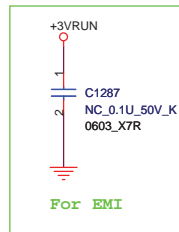
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FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	Index Page	
Size	Document Number	Rev
Custom	M850-1-01	1.0
Date:	Wednesday, April 08, 2009	Sheet 1 of 69

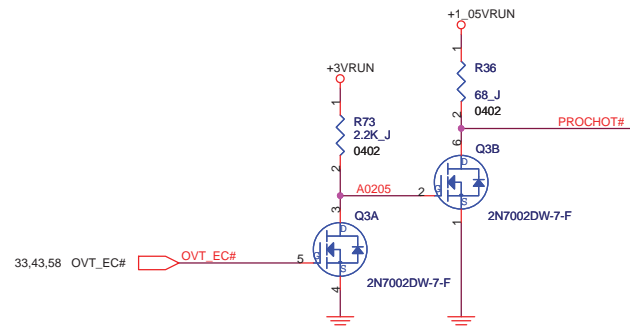
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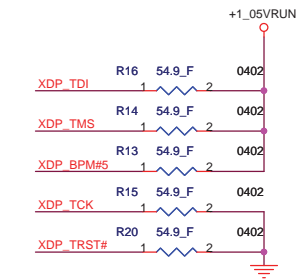
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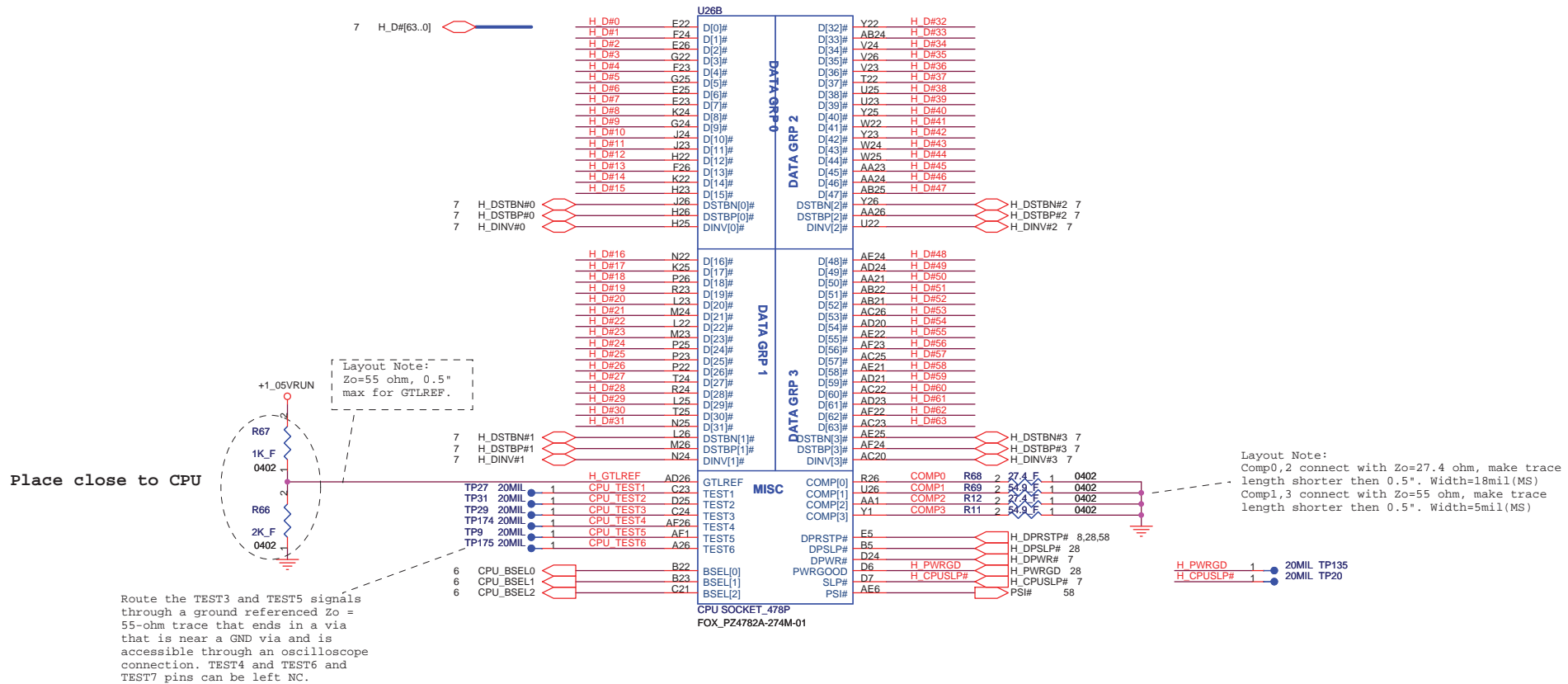


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H\_CPURST# 1 20MIL TP2

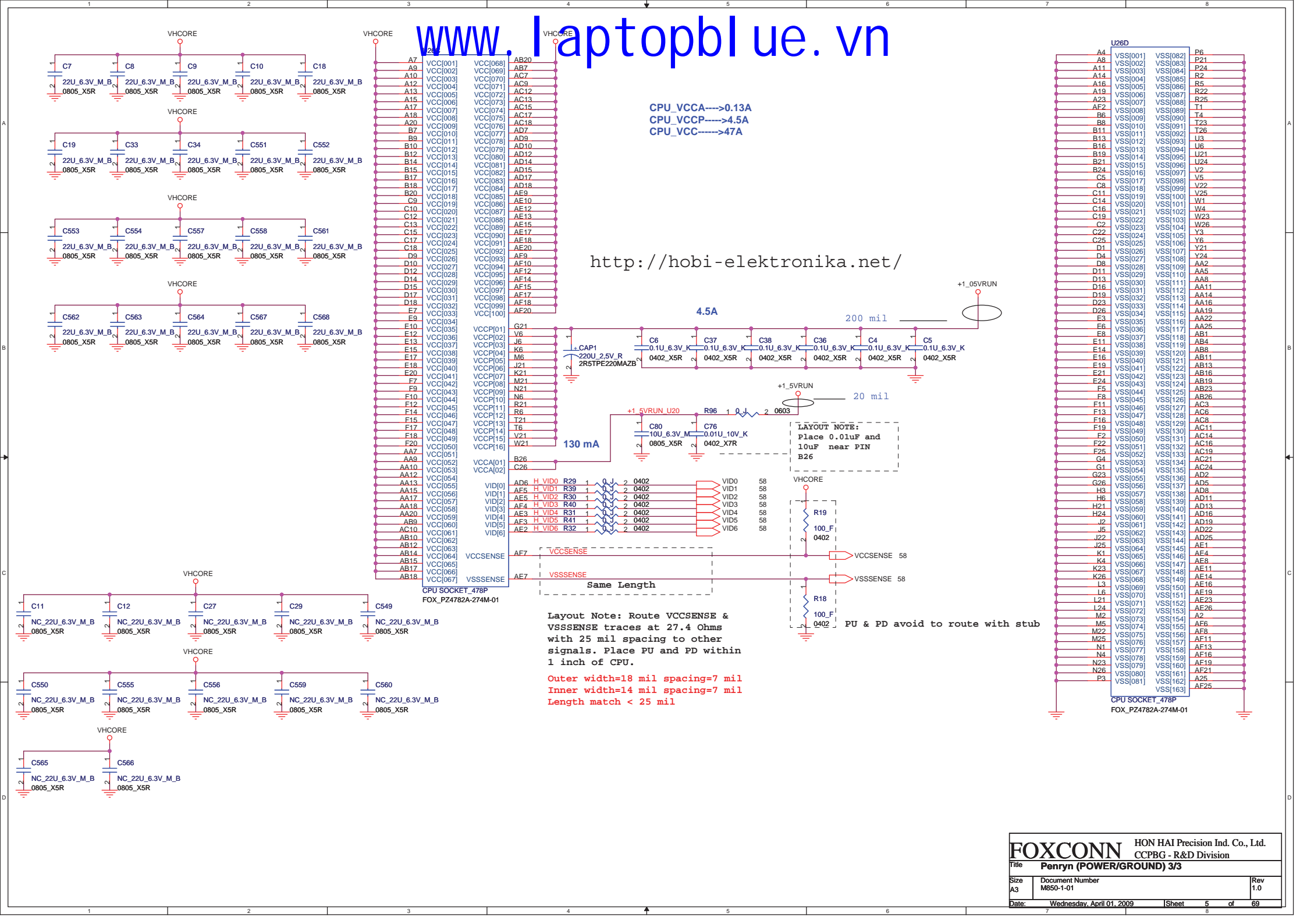


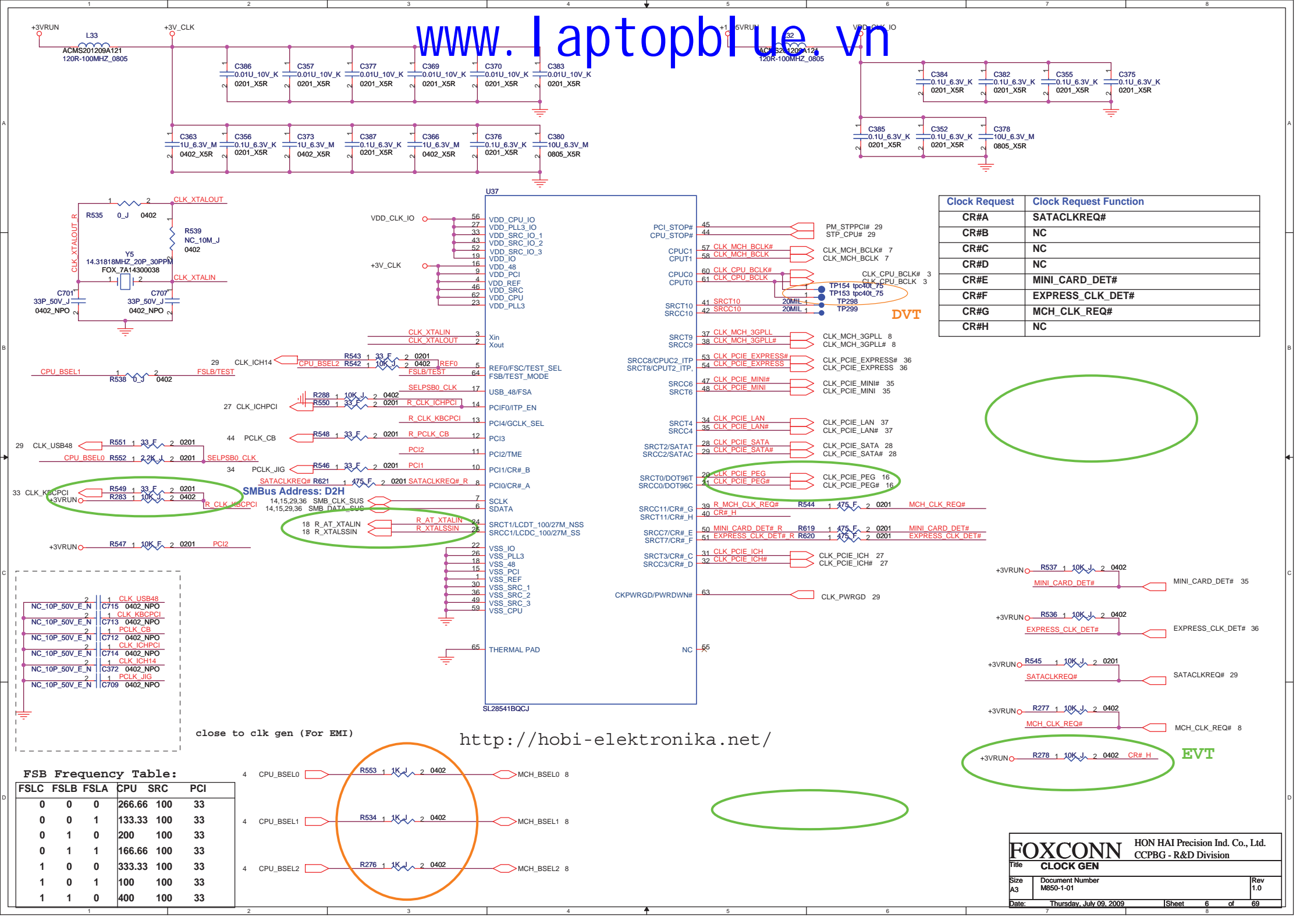
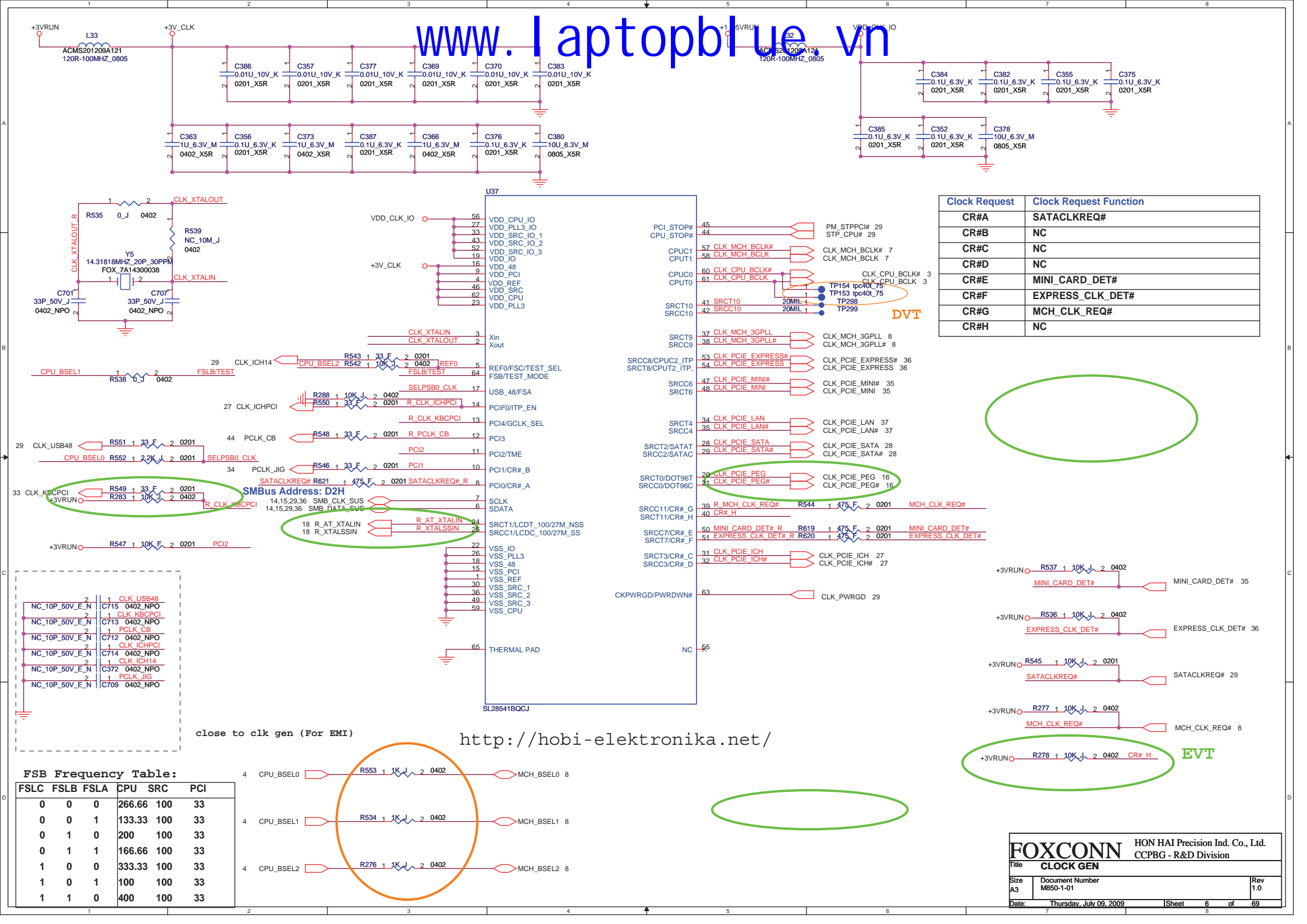


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CPU\_VCCA---->0.13A  
CPU\_VCCP---->4.5A  
CPU\_VCC---->47A

<http://hobi-elektronika.net/>



[illegible]

www.laptopblue.vn

http://hobi-elektronika.net/

close to clk gen (For EMI)

FSB Frequency Table:

FSLC	FSLB	FSLA	CPU	SRC	PCI
0	0	0	266.66	100	33
0	0	1	133.33	100	33
0	1	0	200	100	33
0	1	1	166.66	100	33
1	0	0	333.33	100	33
1	0	1	100	100	33
1	1	0	400	100	33

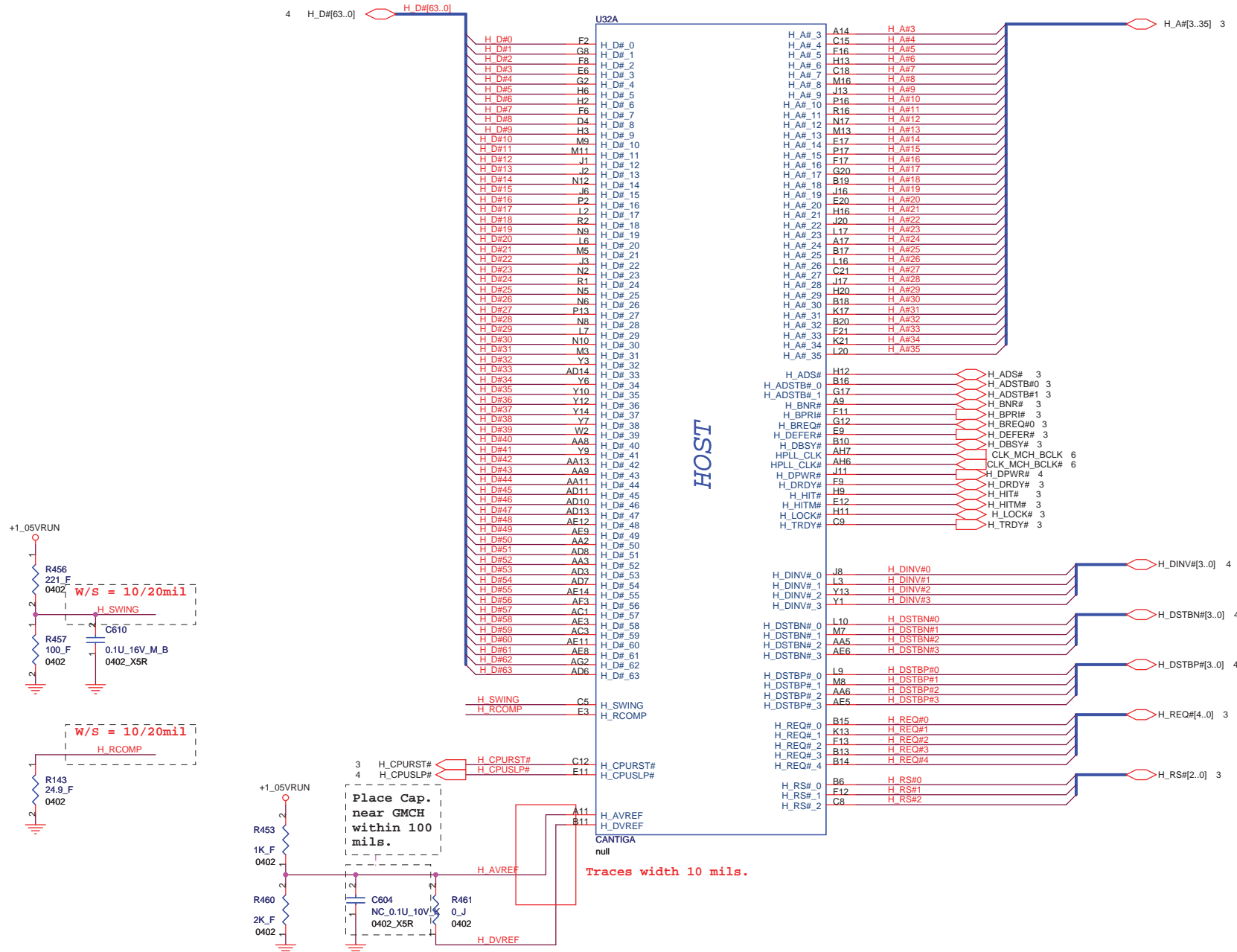
FOXCONN HON HAI Precision Ind. Co., Ltd.  
CCPBG - R&D Division

Title: CLOCK GEN

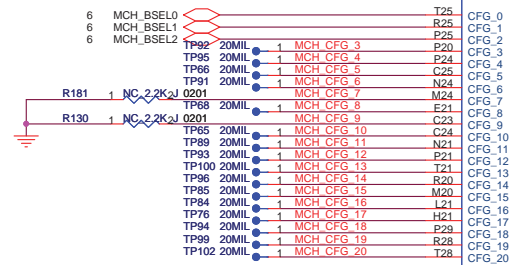
Size: A3 Document Number: M950-1-01 Rev: 1.0

Date: Thursday, July 09, 2009 Sheet: 6 of 69





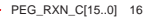
MCH_CFG_0-2 FSB Frequency	000 = FSB1066 ; 010 = FSB800; 011 = FSB667 ; Others = Reserved
MCH_CFG_3-4	Reserved
MCH_CFG_5 DMI X2 Select	Low = DMI X2 High = DMI X4 (Default)
MCH_CFG_6 ITPM Host Interface	Low =The ITPM Host Interface is enabled2 High = The ITPM Host Interface is disabled (default)
MCH_CFG_7 Intel Management Engine Crypto Strap	Low = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel Management Engine Crypto TLS cipher suite with confidentiality (default)
MCH_CFG_8	Reserved
MCH_CFG_9 PCIe Graphics Lane	Low = Reverse Lane High = Normal operation (default)
MCH_CFG_10 PCIe Loopback enable	Low = Enabled3 High = Disabled (default)
MCH_CFG_11	Reserved
MCH_CFG_12 ALLZ	Low = ALLZ mode enabled3 High = Disabled (default)
MCH_CFG_13 XOR	Low = XOR mode enabled3 High = Disabled (default)
MCH_CFG_14-15	Reserved
MCH_CFG_16 FSB Dynamic ODT	Low = Dynamic ODT disabled High = Dynamic ODT enabled (default)
MCH_CFG_17-18	Reserved
MCH_CFG_19 DMI Lane Reversal	Low = Normal operation (Default): Lane Numbered in Order High = Reverse Lanes DMI x4 mode [(G)MCH->ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [(G)MCH ->ICH]: (3->0, 2->1)
MCH_CFG_20 Digital Display Port (SDVO/ DP/iHDMI) Concurrent with PCIe	Low = Only digital display port (SDVO/DP/iHDMI) or PCIe is operational (default). High = Digital display port (SDVO/DP/iHDMI) and PCIe are operating simultaneously via the PEG port



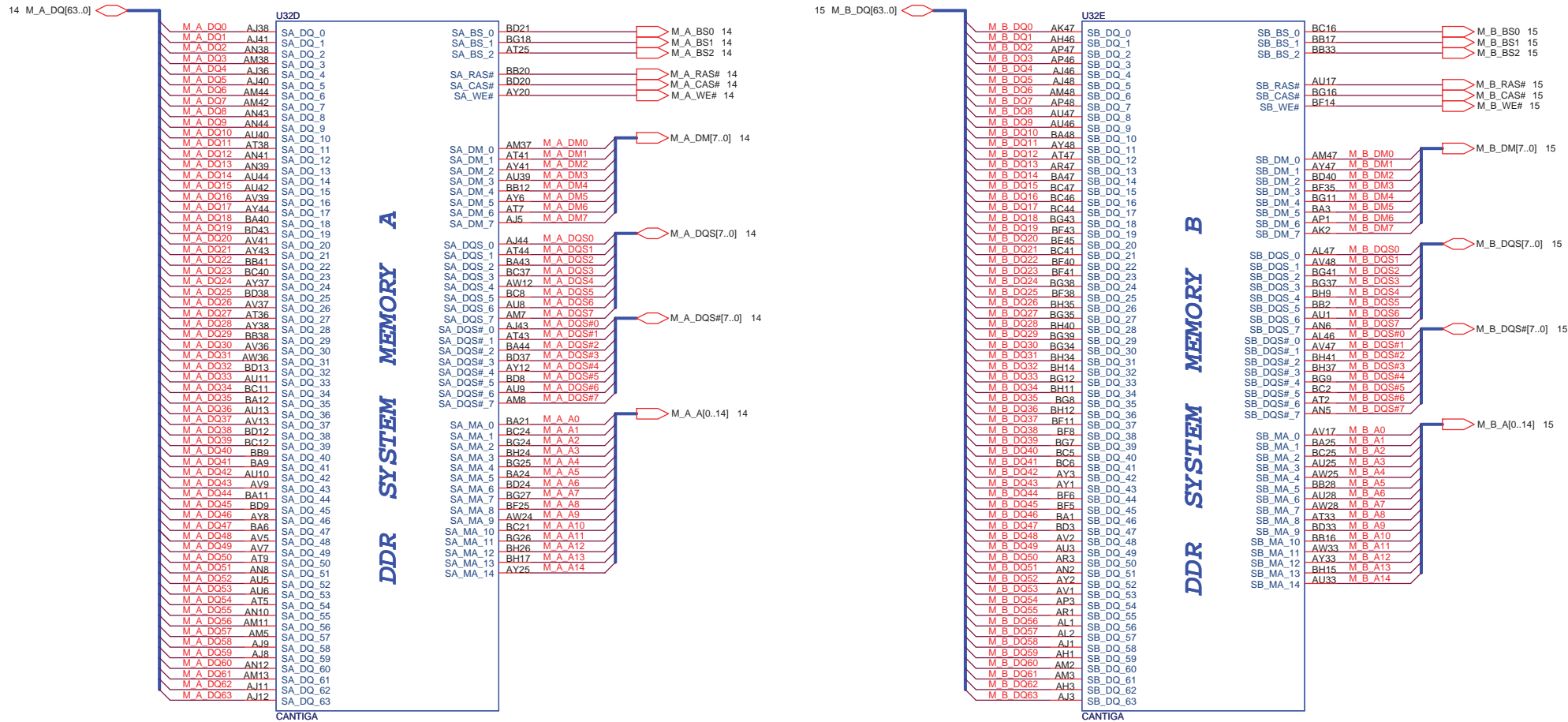


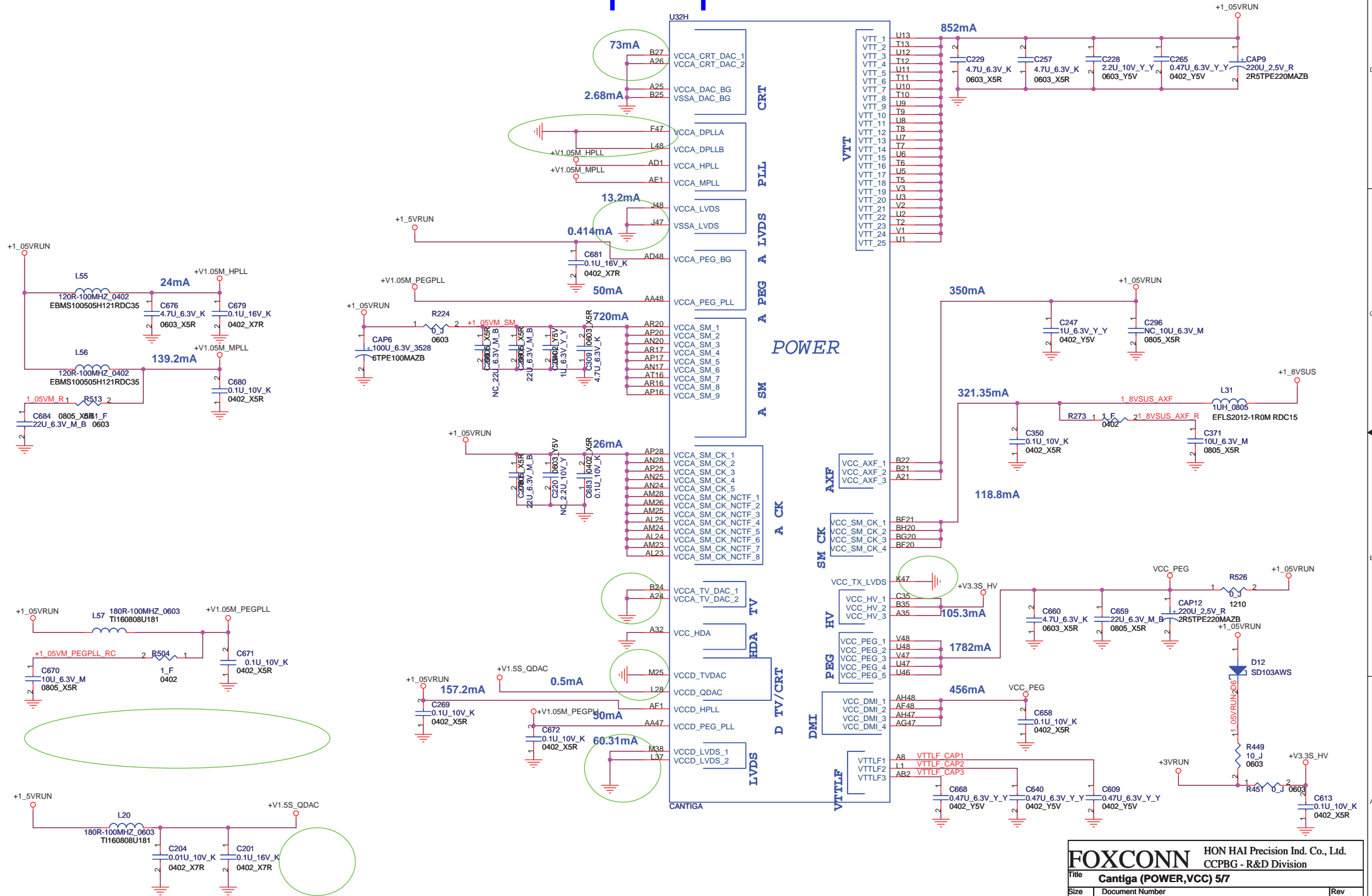


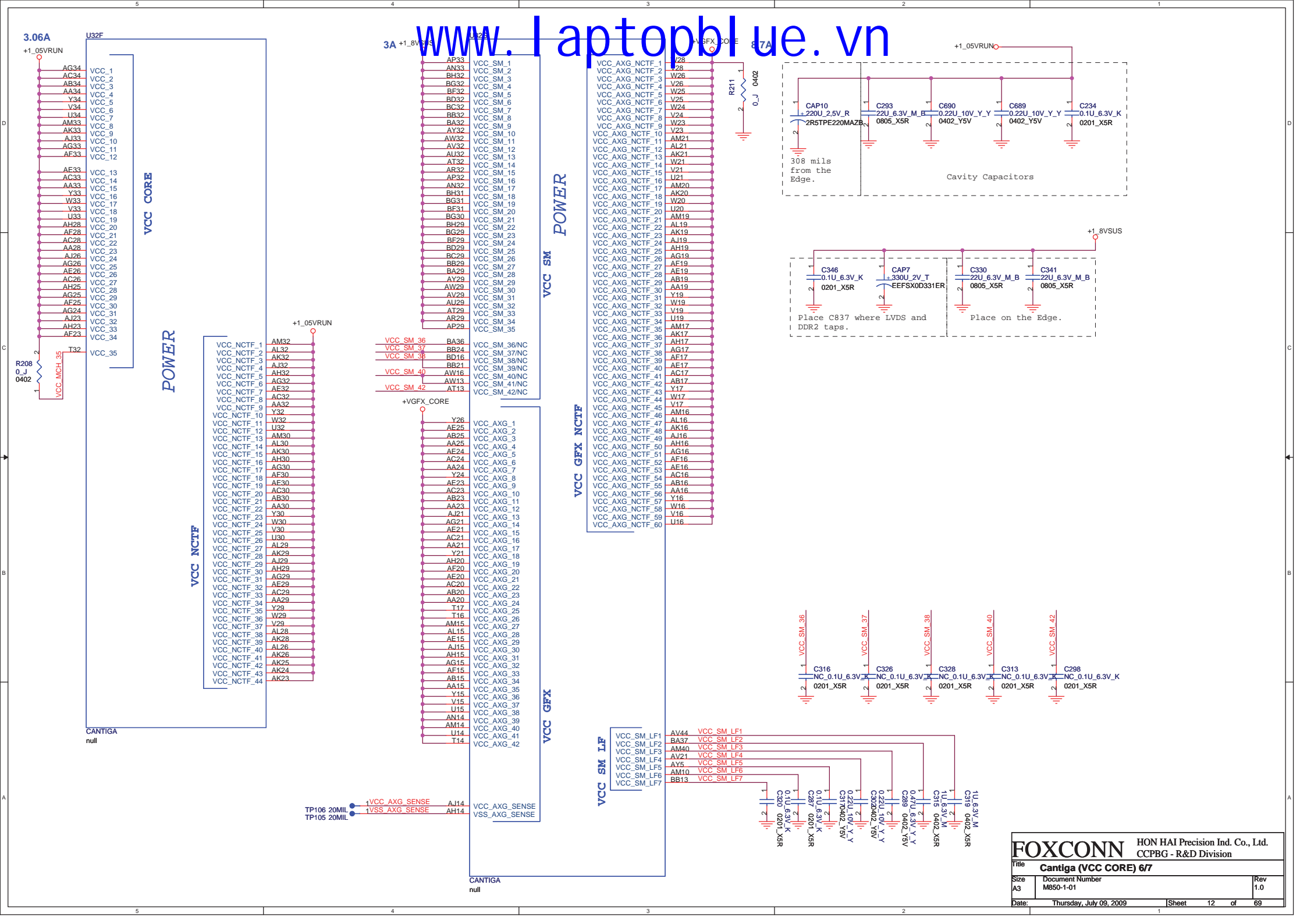
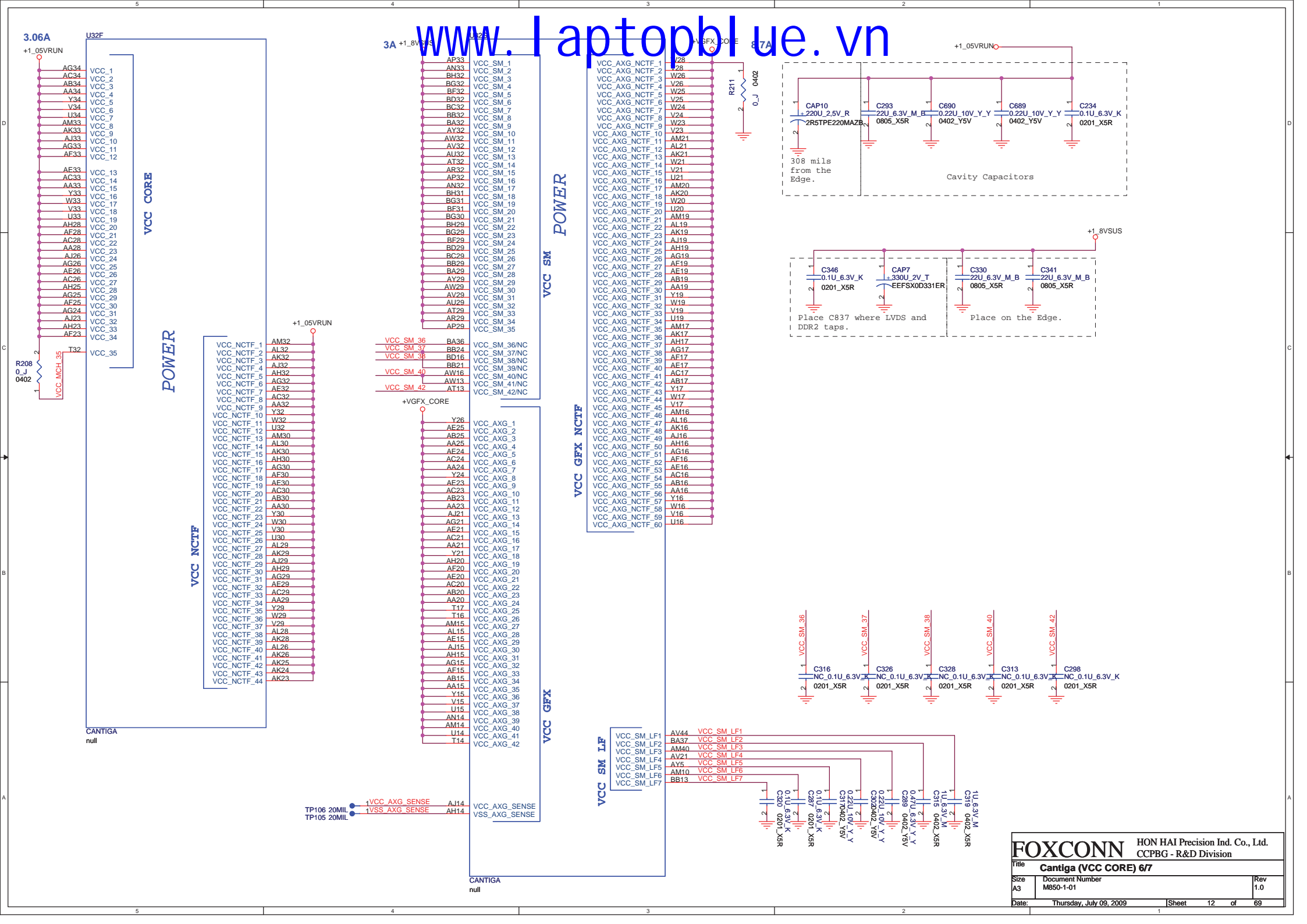
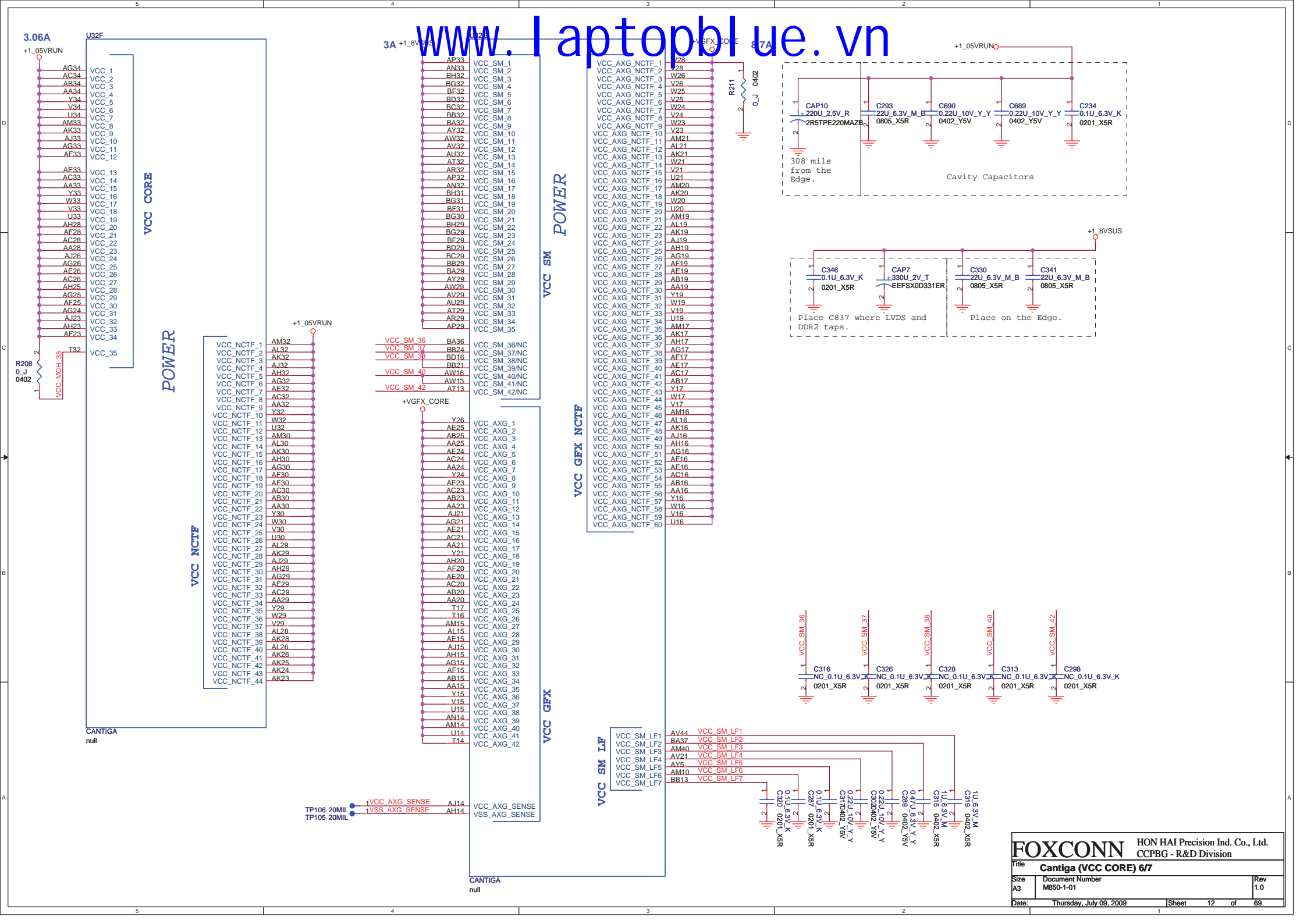
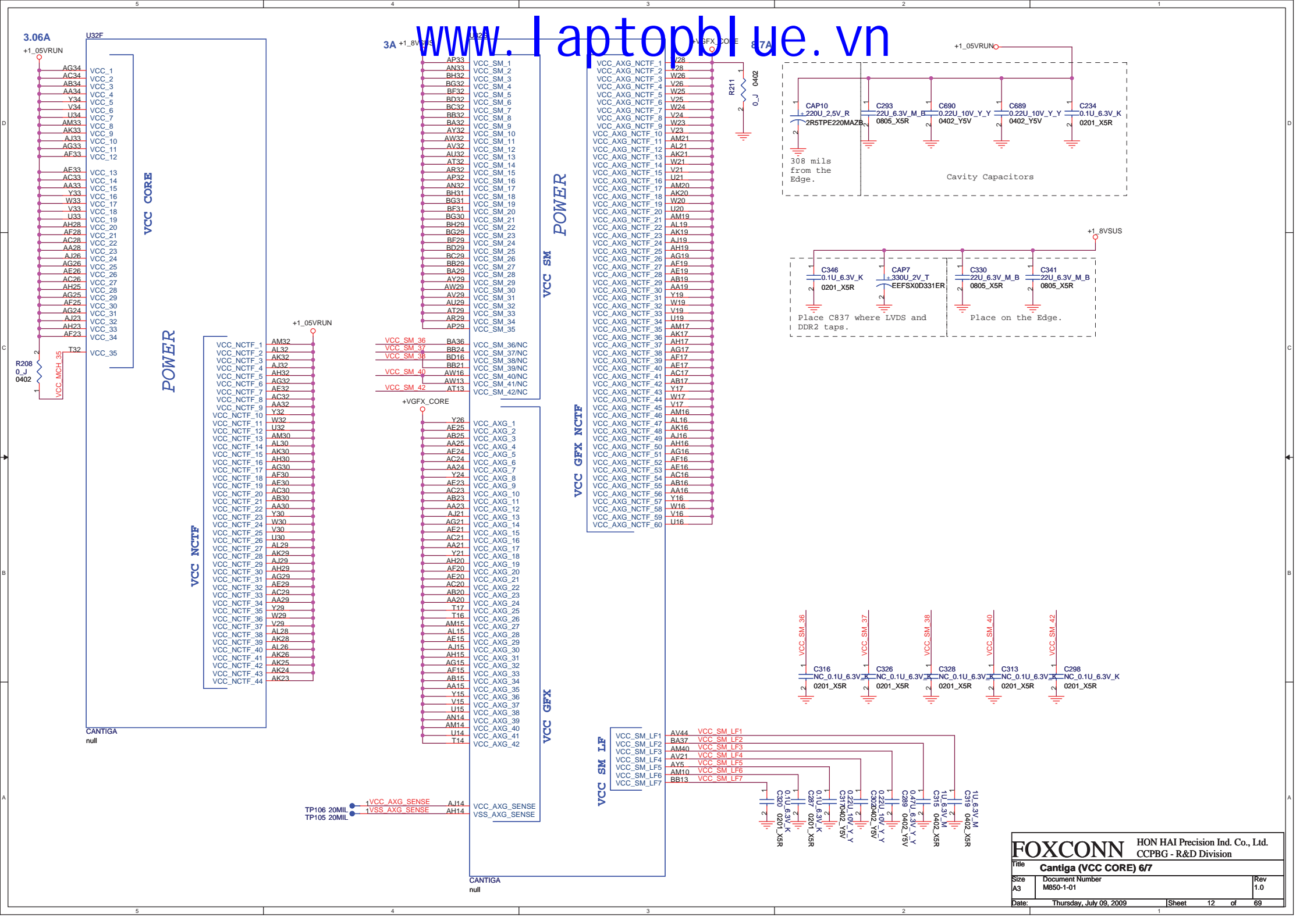
## GRAPHICS

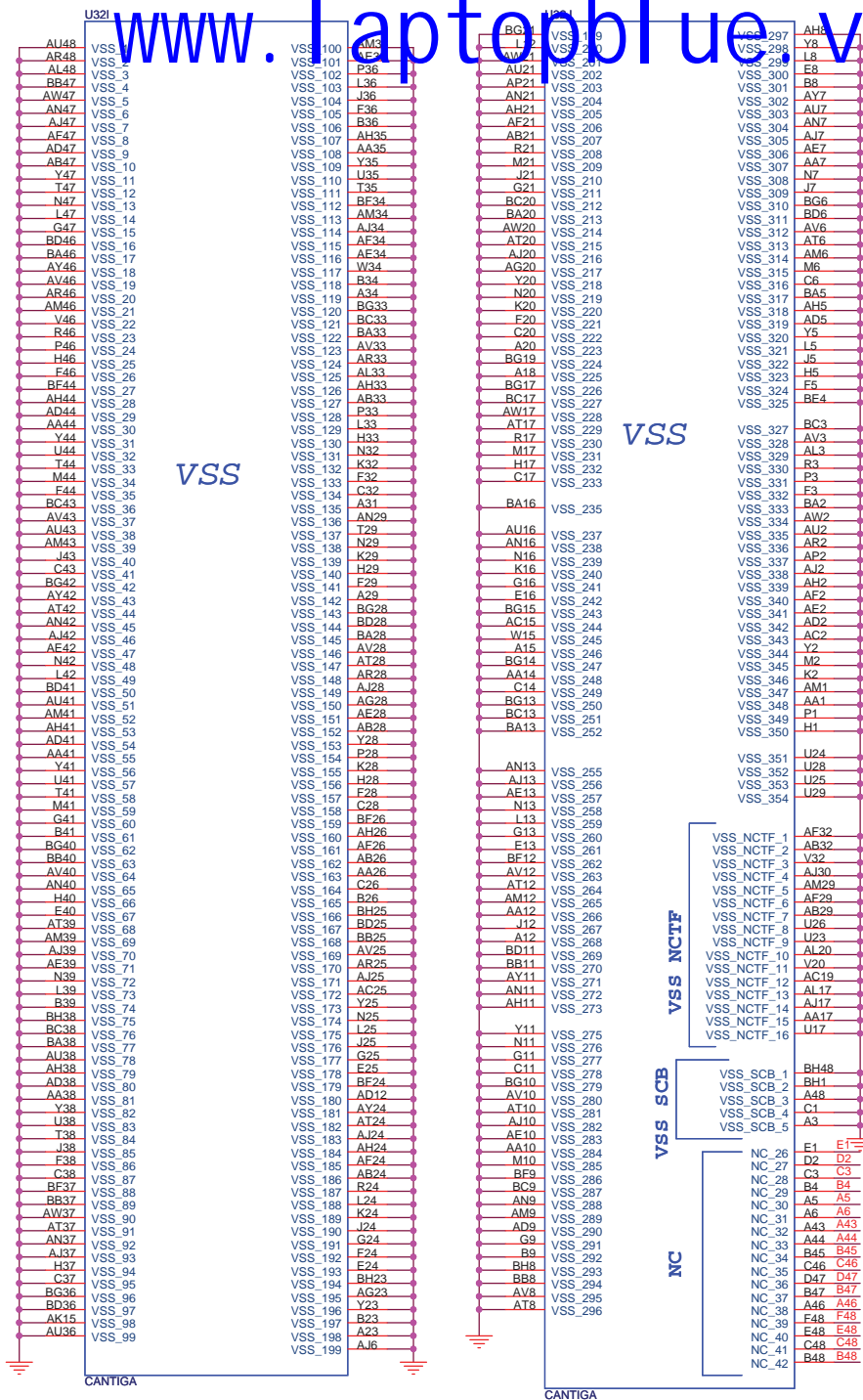
PCI-EXF  
ΔI.

```
PEG_RXP_C[15..0] 16
```

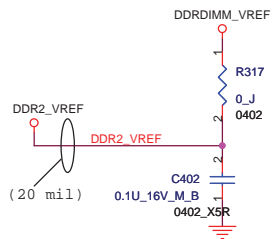
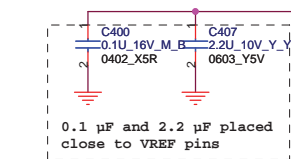












M\_CKE0

M\_A\_BS2

M\_A\_BS0

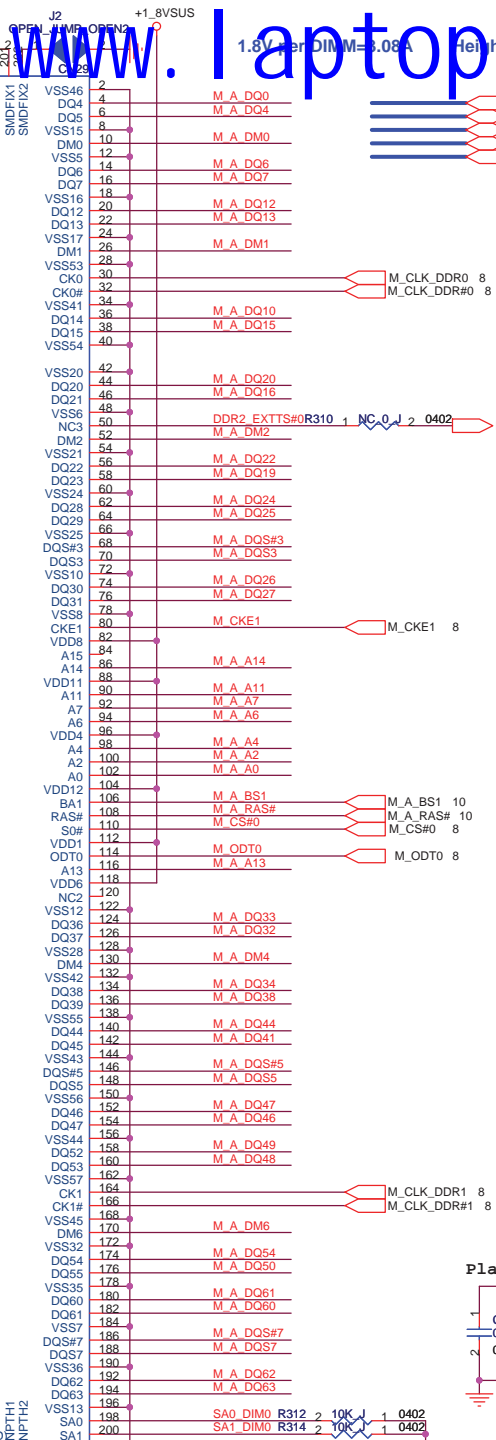
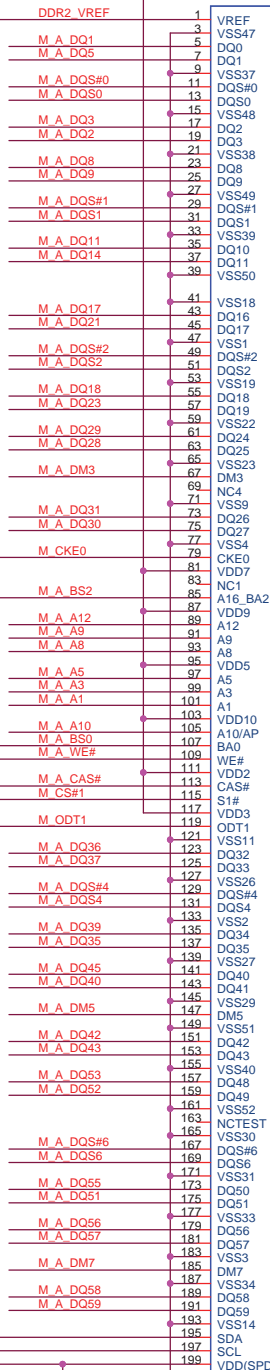
M\_A\_WE#

M\_A\_CAS#

M\_CS#1

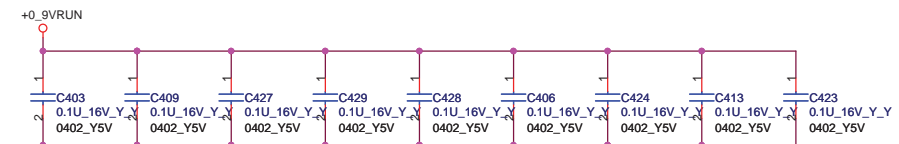
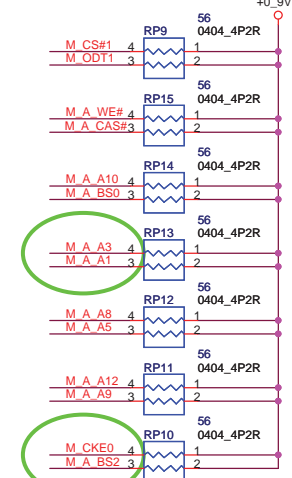
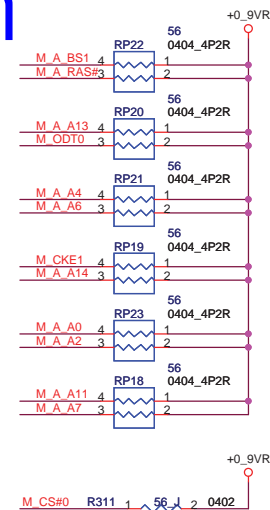
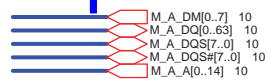
M\_ODT1

6,15,29,36 SMB\_DATA\_SUS  
6,15,29,36 SMB\_CLK\_SUS  
+3VRUN

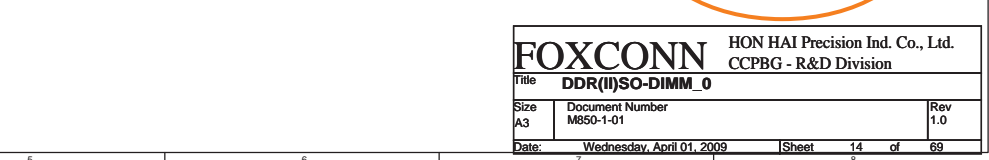
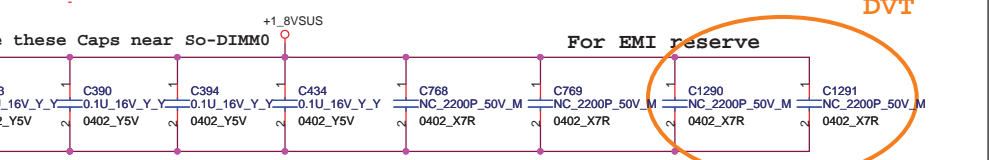
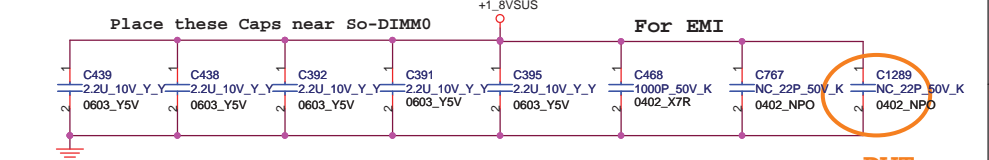
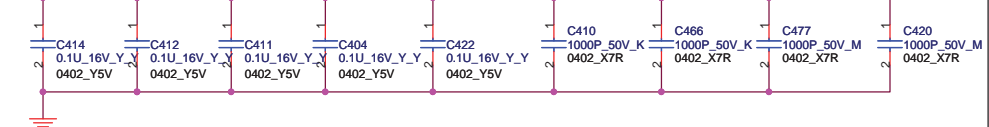


SMBus Address: A0H(W)/A1H(R)

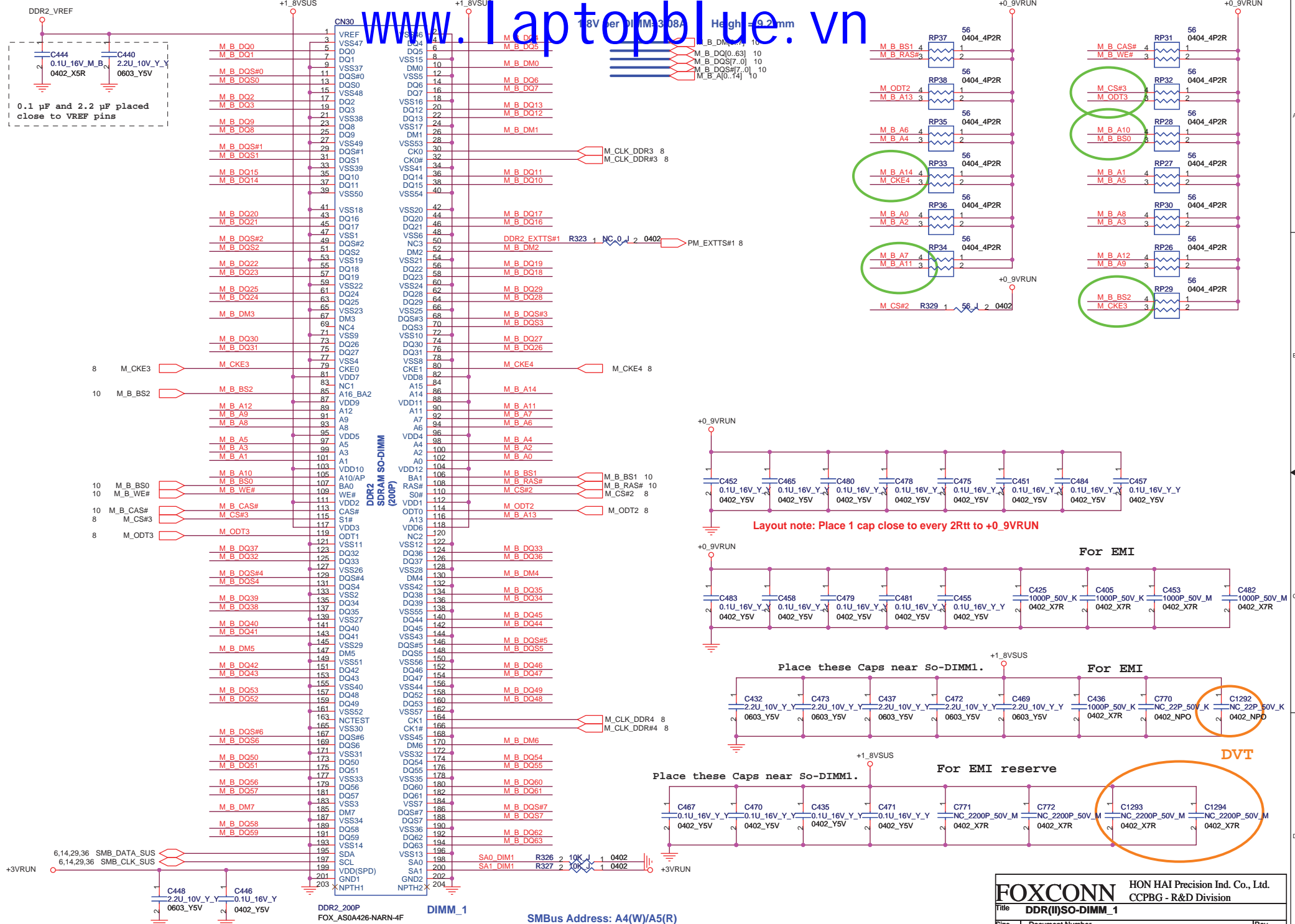
Place DIMM\_0 near GMCH

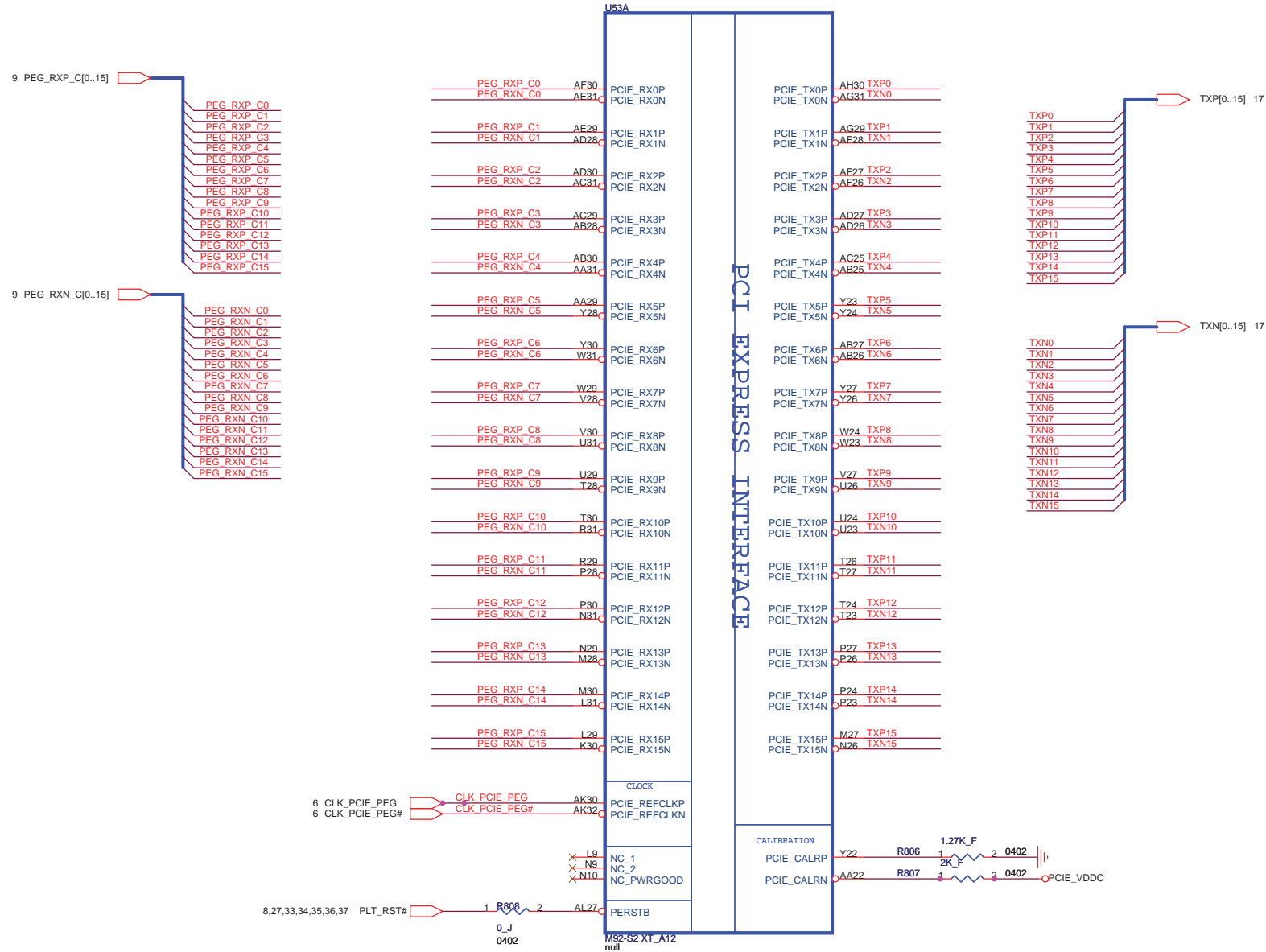


Layout note: Place 1 cap close to every 2 Rtt to +0.9VRUN  
<http://hobi-elektronika.net/> For EMI

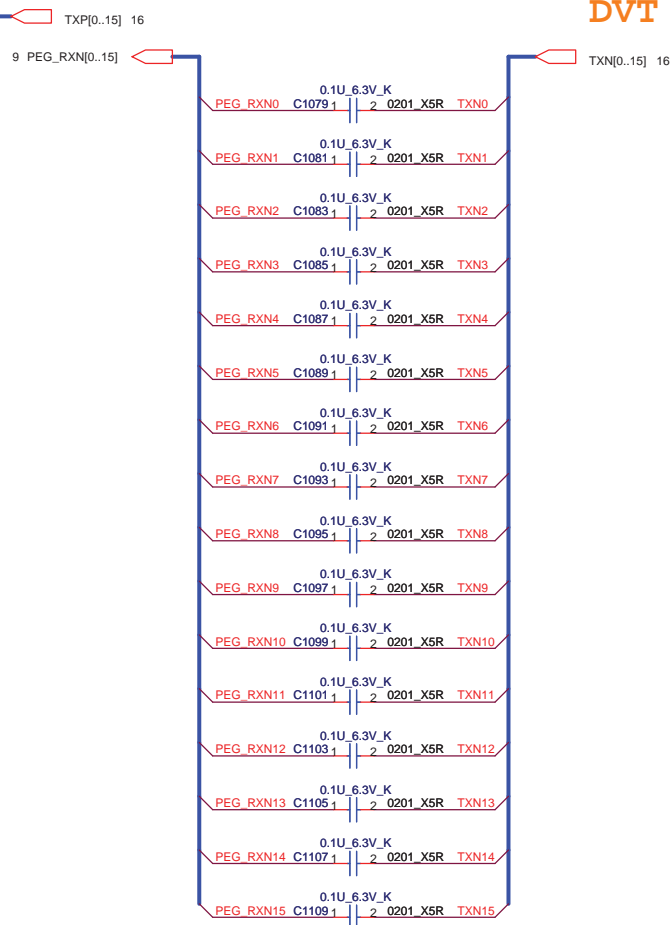
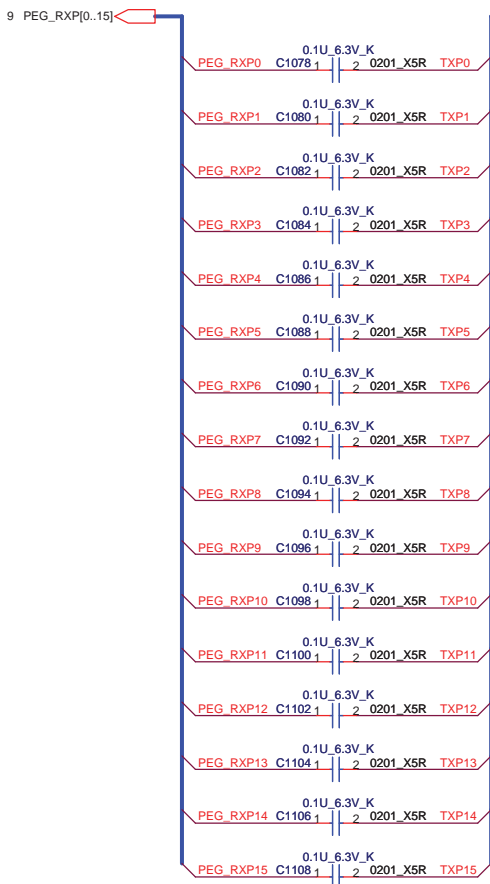








	Mount	NC		Mount	NC		Mount	NC
Hynix-256MB H5RS1H23MFR-11C	R812,R809	R910,R911, R811,R810	Samsung-256MB K4J10324QD-HC12	R812,R810	R910,R911, R811,R809	Samsung-512MB K4J10324QD-HC12	R910 R812,R810	R911 R811,R809
Hynix-512MB H5RS1H23MFR-11C	R910 R812,R809	R911 R811,R810	Qimonda-256MB HYB18H1G321A2F-10	R811,R810	R910,R911, R812,R809	Qimonda-512MB HYB18H1G321A2F-10	R910 R811,R810	R911 R812,R809



## DVT

## DVT

Strap for GDDR3-136ball  
ATL\_DVPDATA[1:0:21:20]

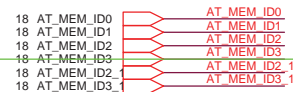
0001 32Mx32 Qimonda-256MB  
0010 32Mx32 Hynix-256MB  
0011 32Mx32 Samsung-256MB  
0101 32Mx32 Qimonda-512MB  
0110 32Mx32 Hynix-512MB  
0111 32Mx32 Samsung-512MB

If no ROM attached, GPIO[13:12:11] ;  
CONFIG(2:0)  
controls the memory aperture size.  
64MB 010  
128MB 000  
256MB 001  
512MB 001

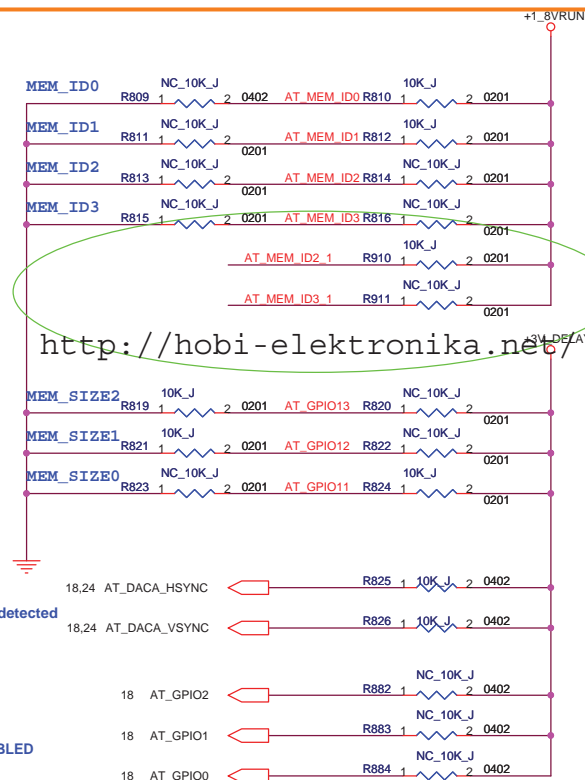
HSYNC , VSYNC  
AUD[1] , AUD[0]

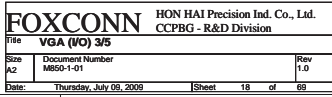
0,0 No audio function  
0,1 Audio for DisplayPort and HDMI if dongle is detected  
1,0 Audio for DisplayPort only  
1,1 Audio for both DisplayPort and HDMI

GPIO 0 : PCIE FULL TX OUTPUT SWING  
GPIO 1 : PCIE TRANSMITTER DE-EMPHASIS ENABLED  
GPIO 2 : PCIE GEN2 ENABLED

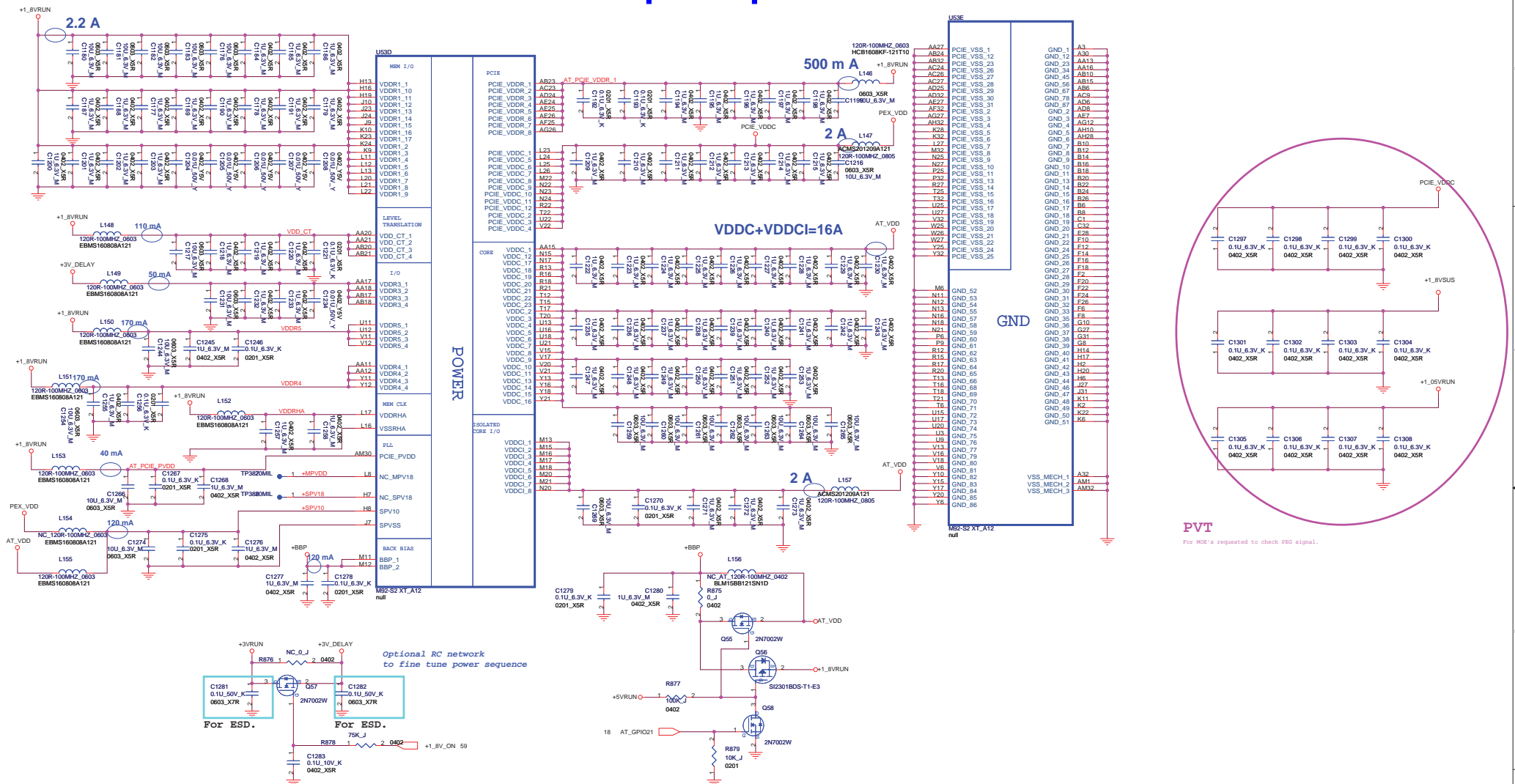


For AMD verification

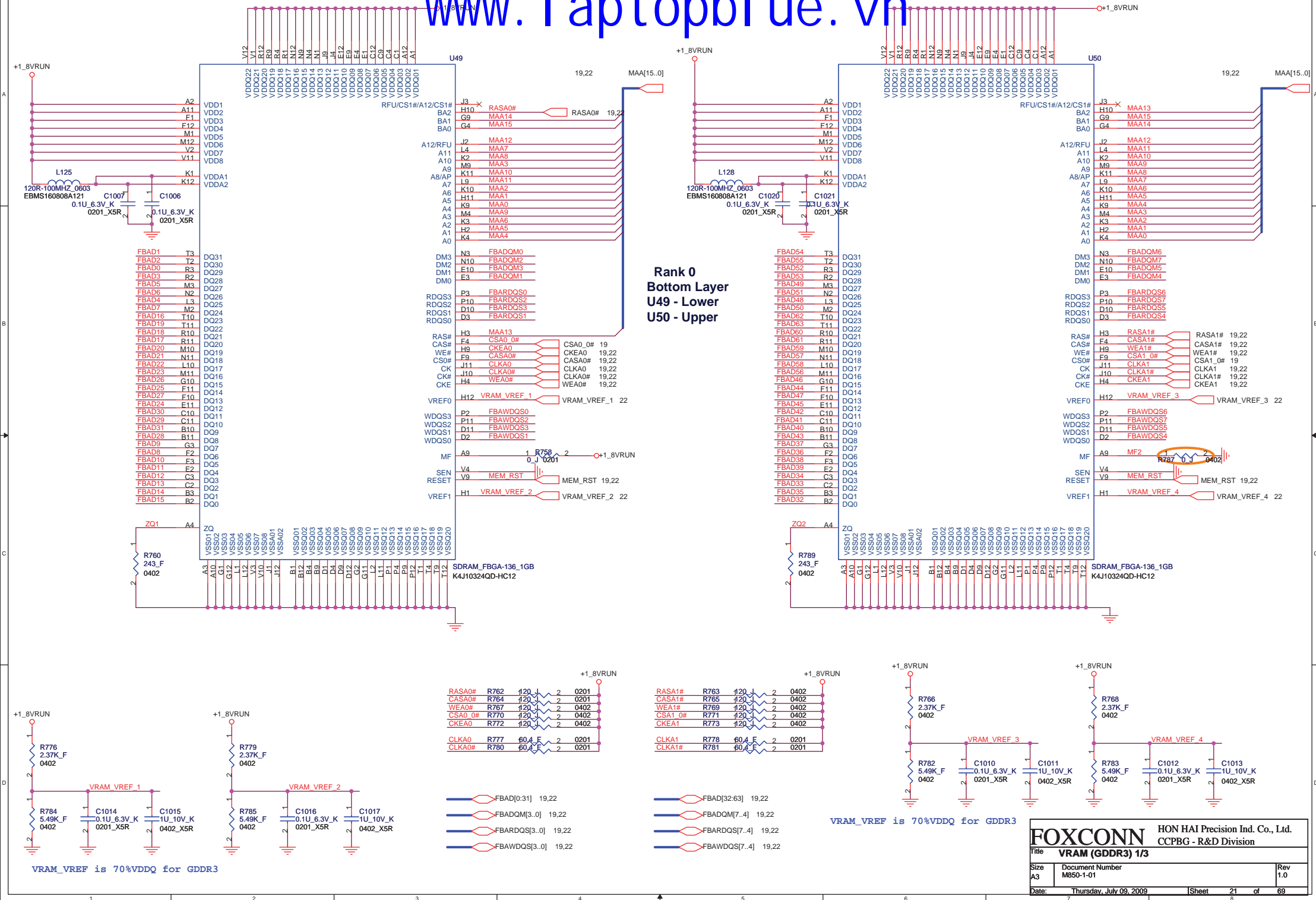








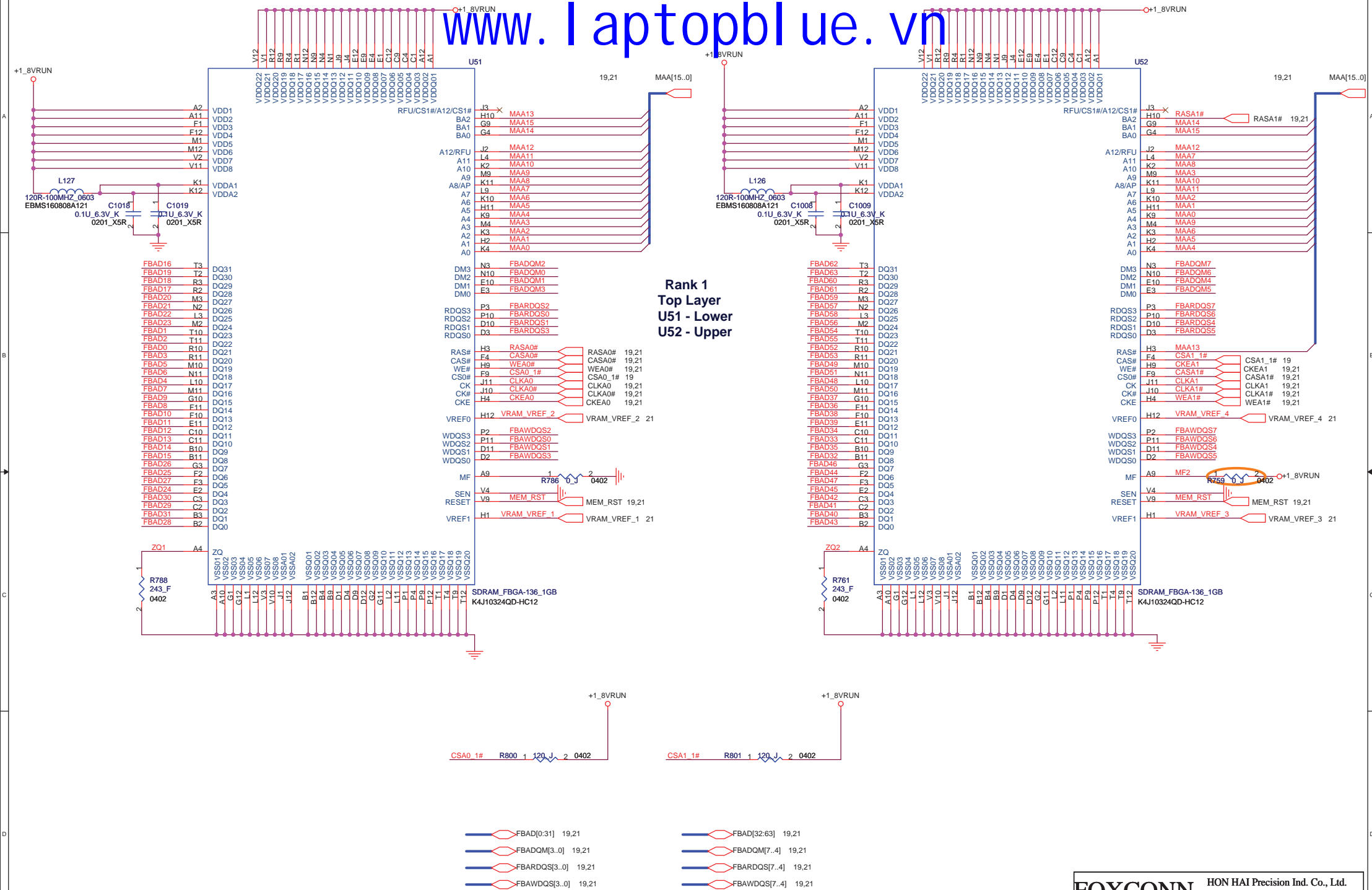


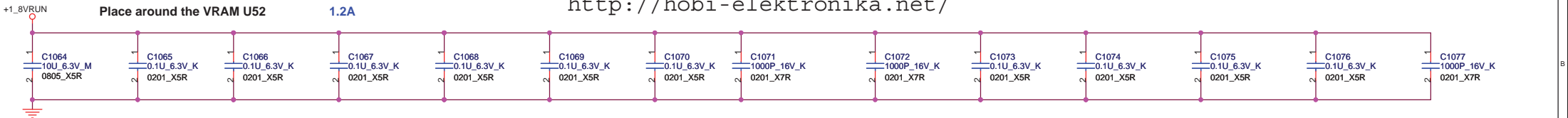
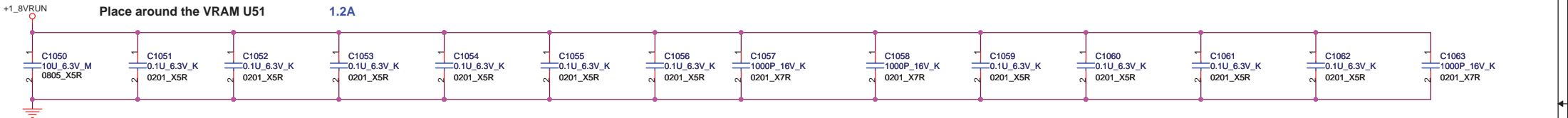
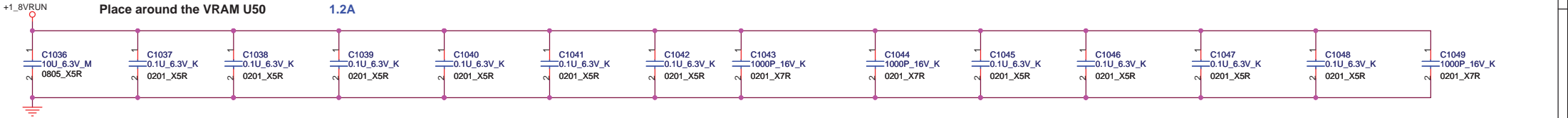
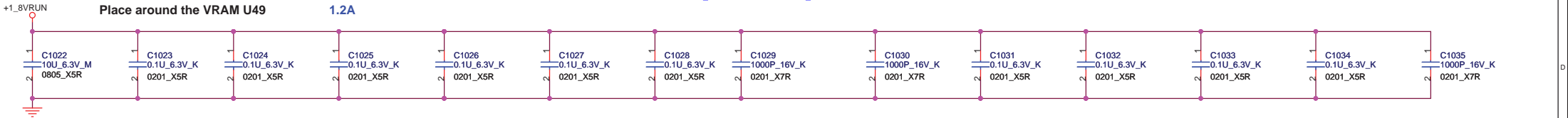


U51

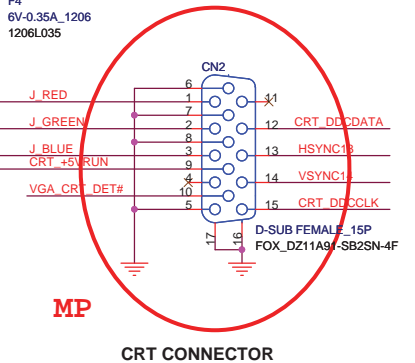
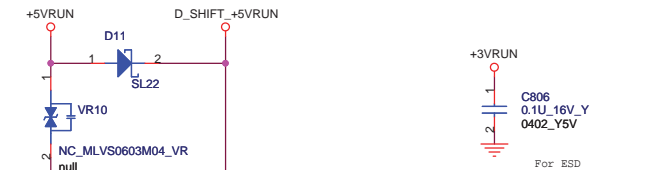
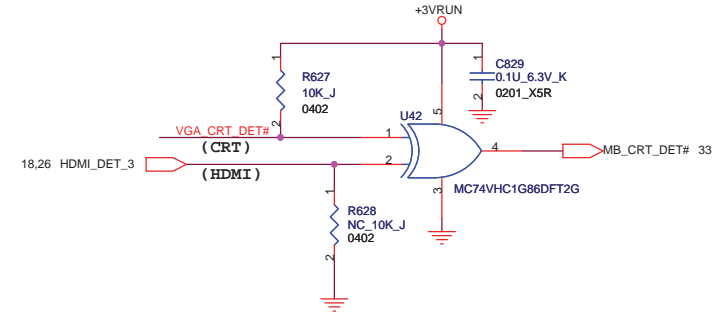
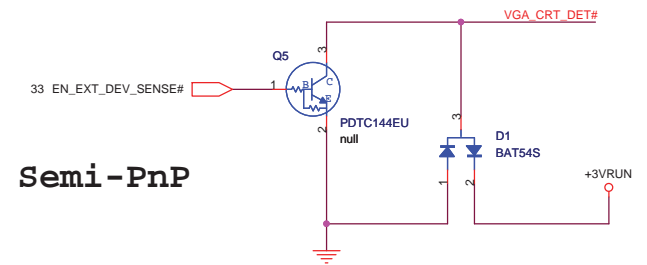
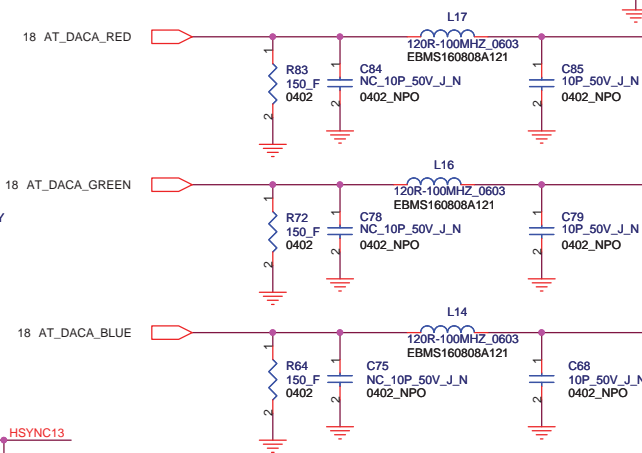
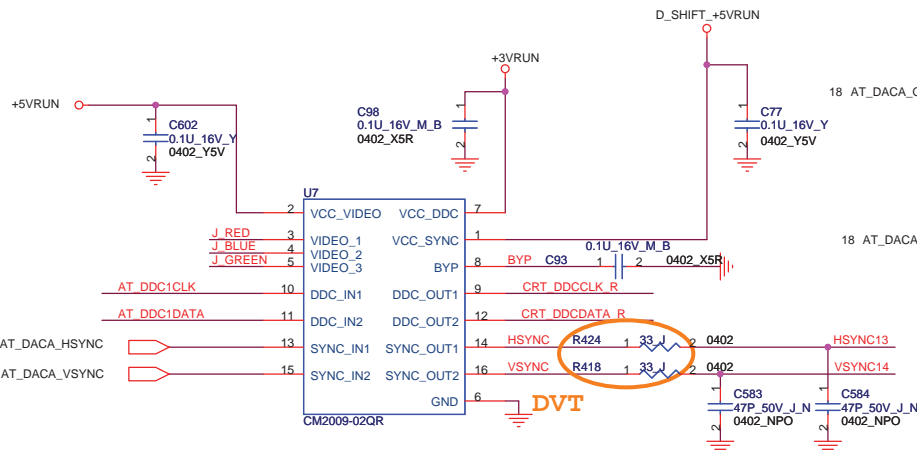
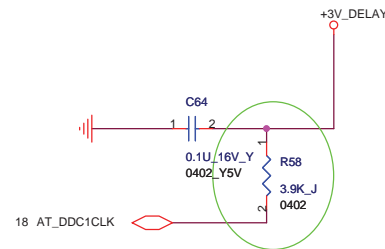
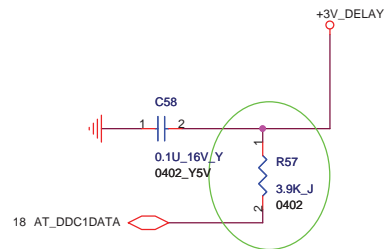
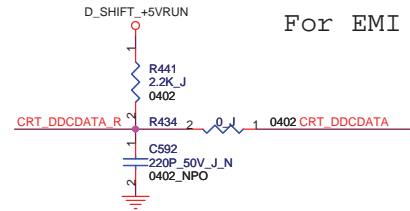
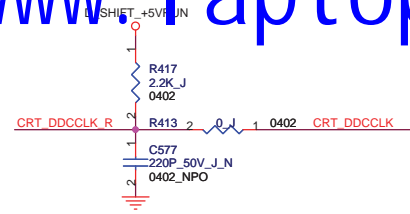
19,21 MAA[15..0]

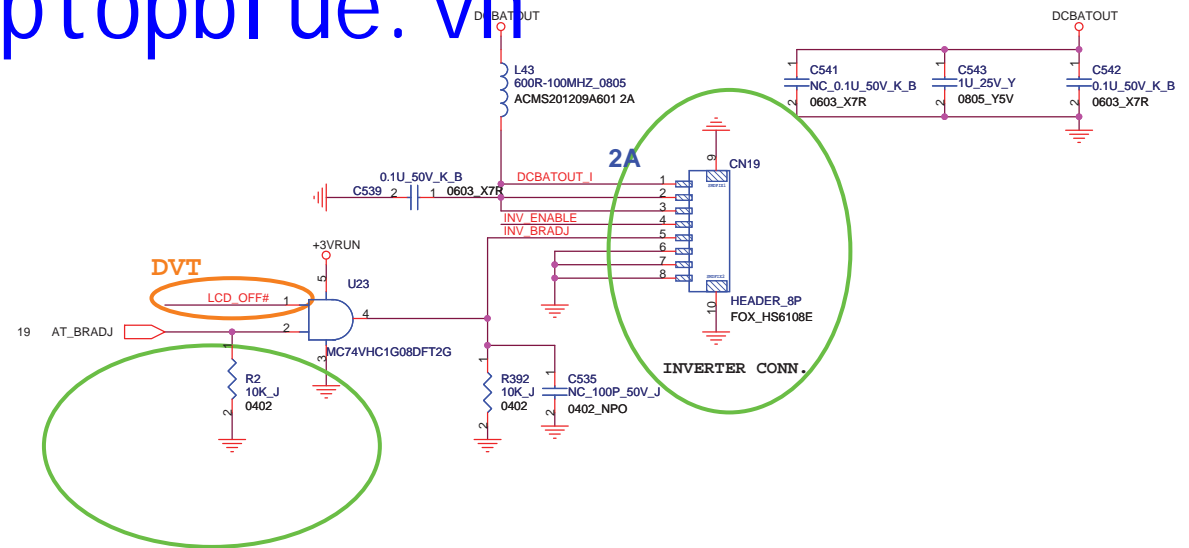
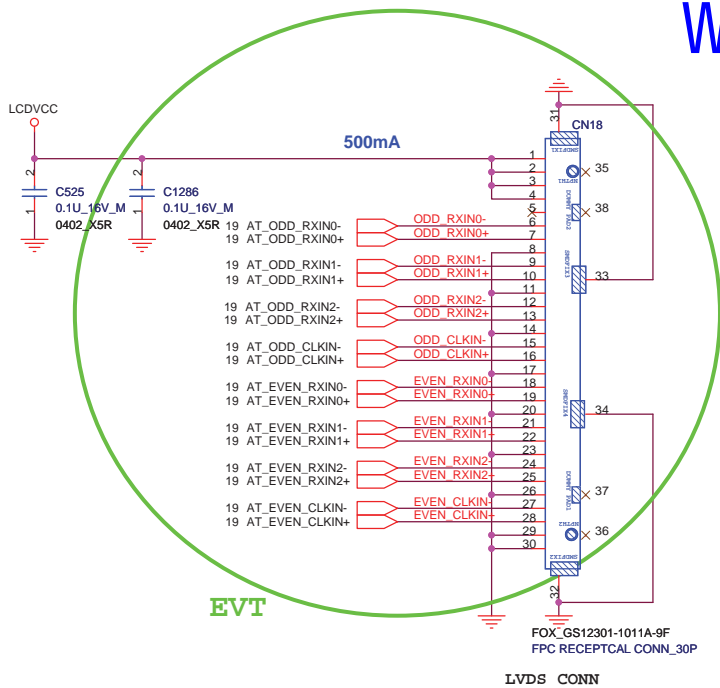
222 V V R  
221 V V R  
220 V V R



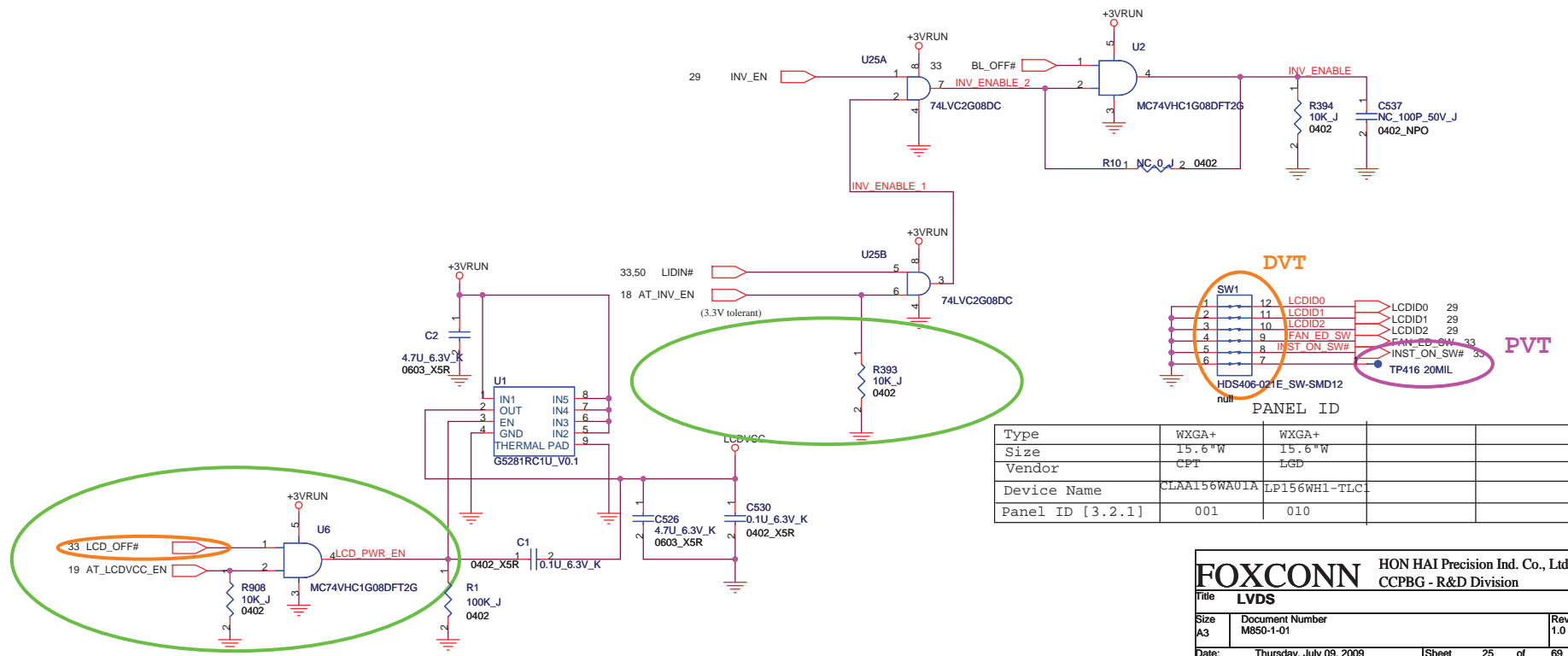


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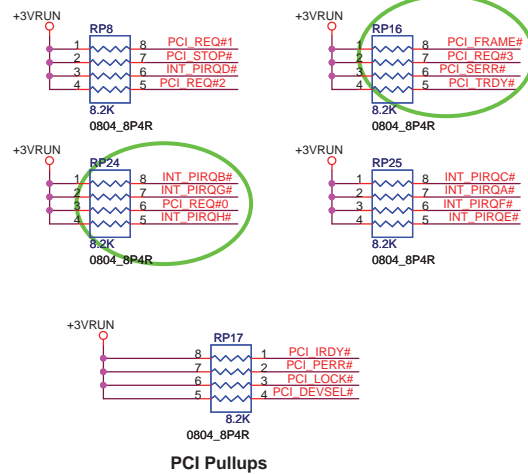


<http://hobi-elektronika.net/>

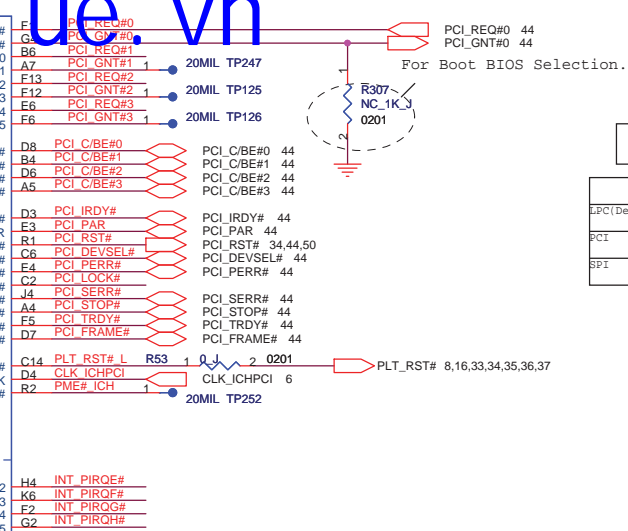
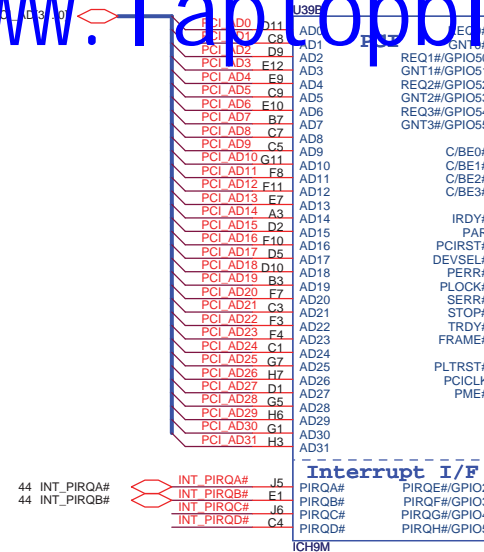








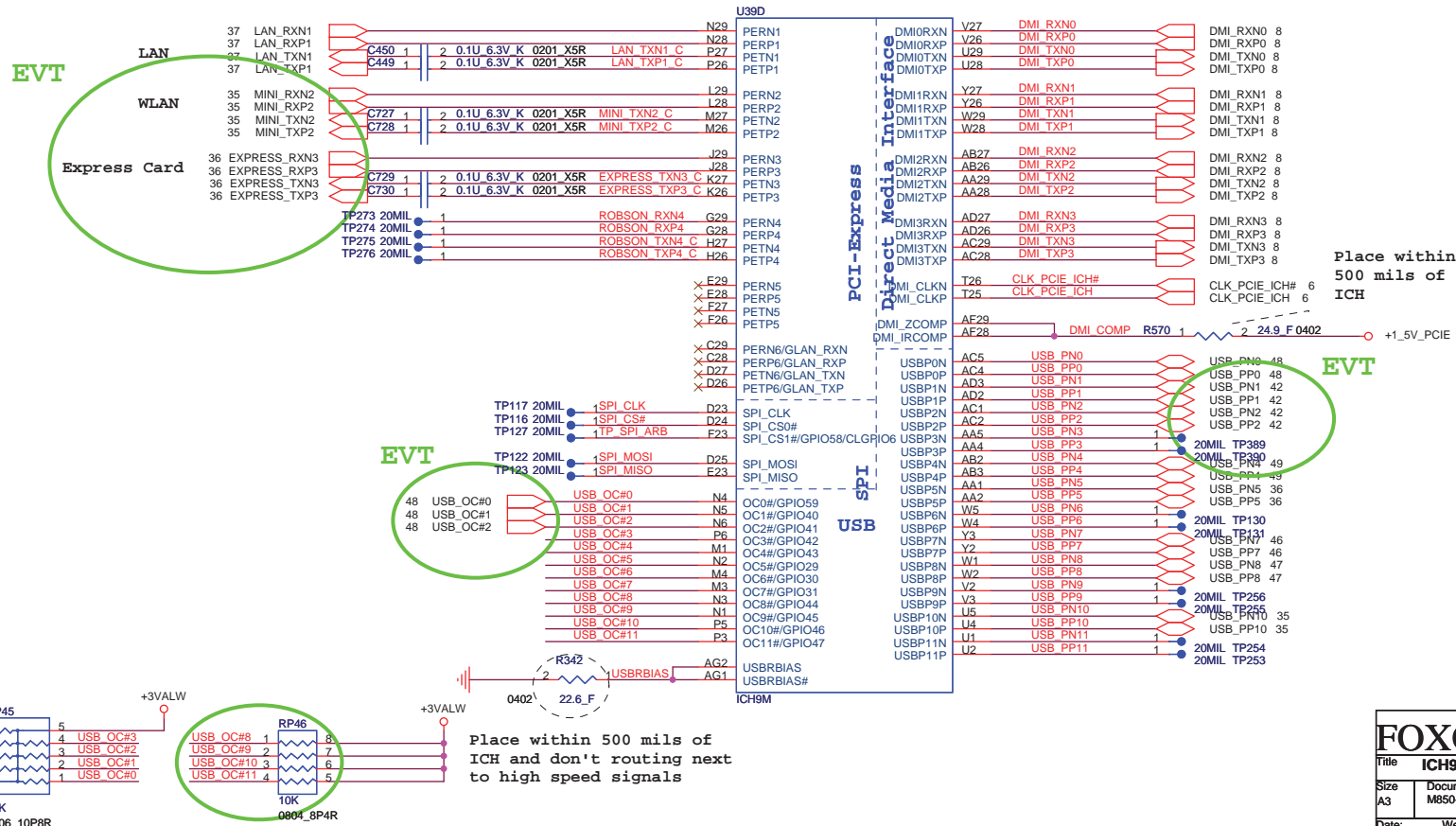
## PCI Pullups



Strap for  
Boot-BIOS

	GNT0#	SPI_CS1#
LPC(Default)	Hi	Hi
PCI	Hi	LOW
SPI	LOW	Hi

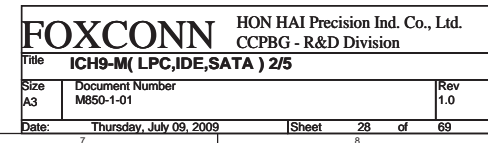
<http://hobi-elektronika.net/>



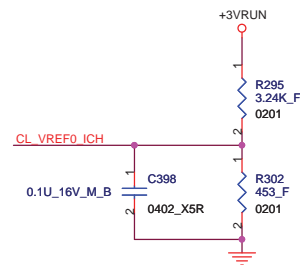
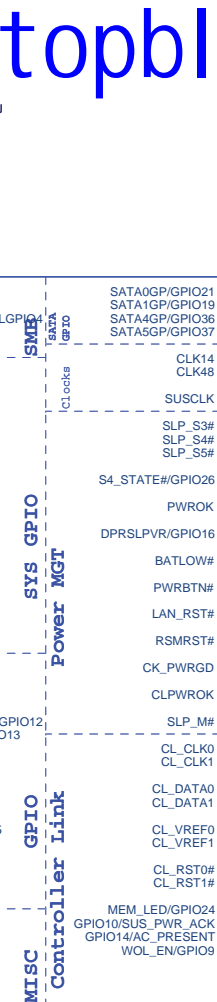
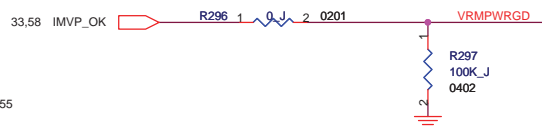
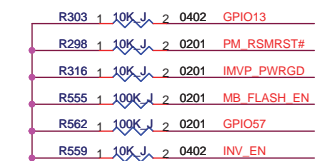
USB PORT	Function
PORT-0	Ext. Port
PORT-1	Ext. Port
PORT-2	Ext. Port
PORT-3	
PORT-4	Bluetooth
PORT-5	EXPRESS CARD
PORT-6	
PORT-7	Camera
PORT-8	Felica
PORT-9	
PORT-10	Wi-MAX
PORT-11	

**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
CCPBG - R&D Division

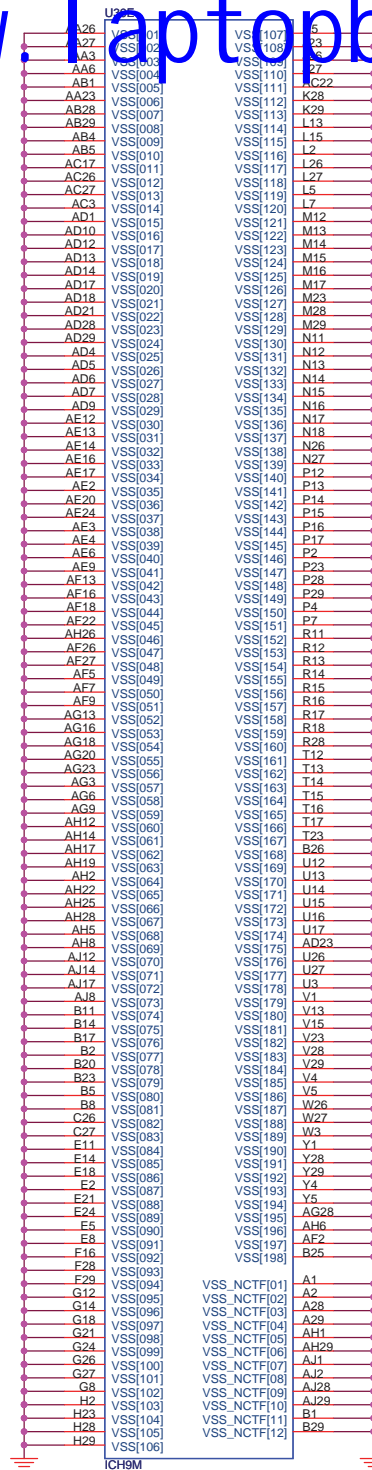
Title				ICH9-M( PCI/DMI/USB/PCIE ) 1/5			
Size		Document Number				Rev	
A3		M850-1-01				1.0	
Date:		Wednesday, April 01, 2009		Sheet		27 of 69	



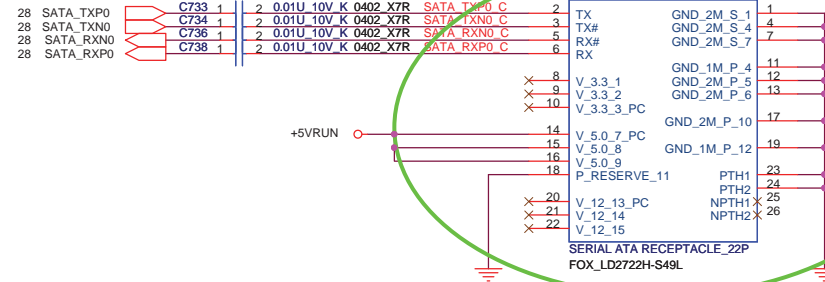
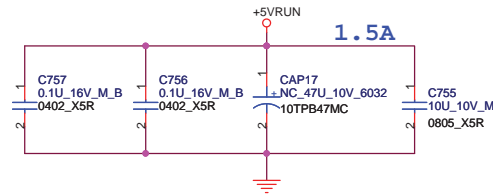
Low=Default  
High=No-reboot





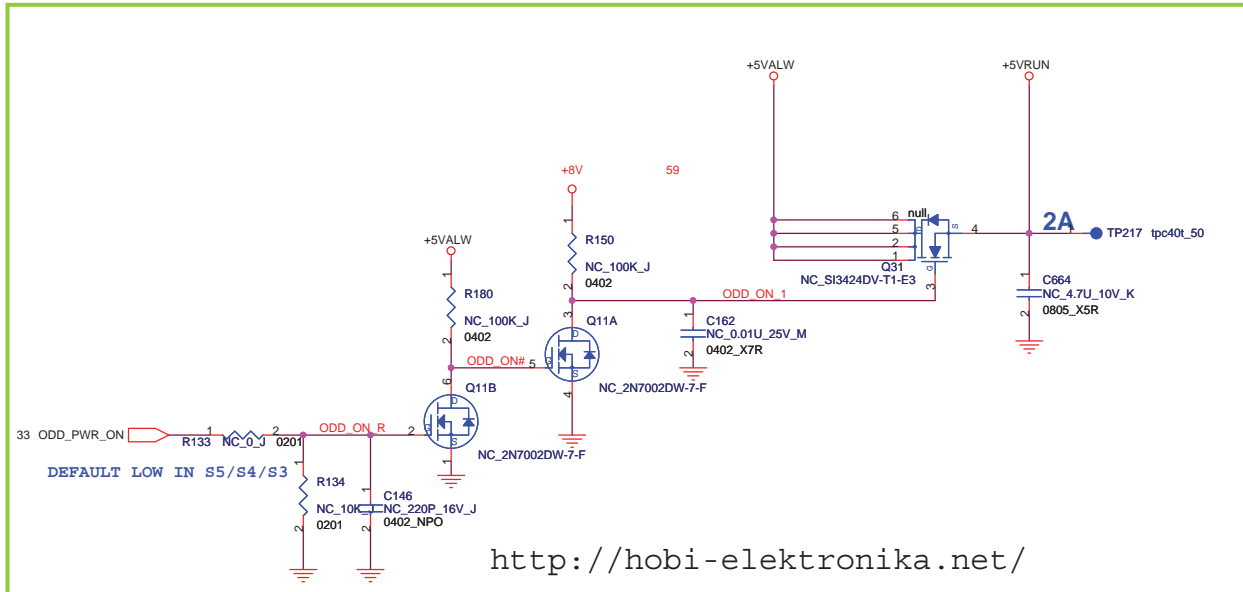
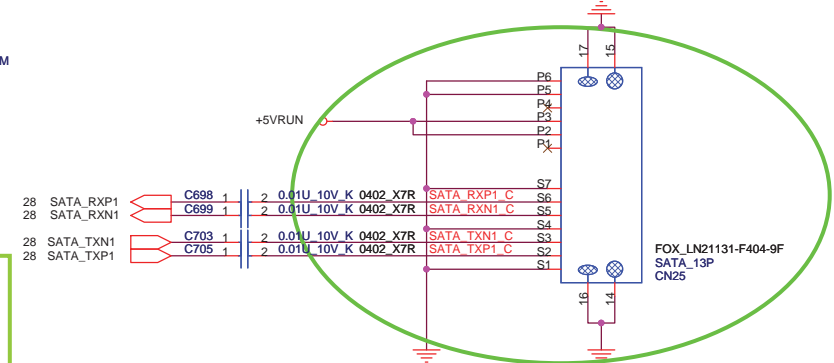
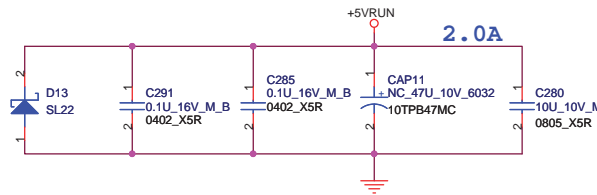


## SATA HDD CONN



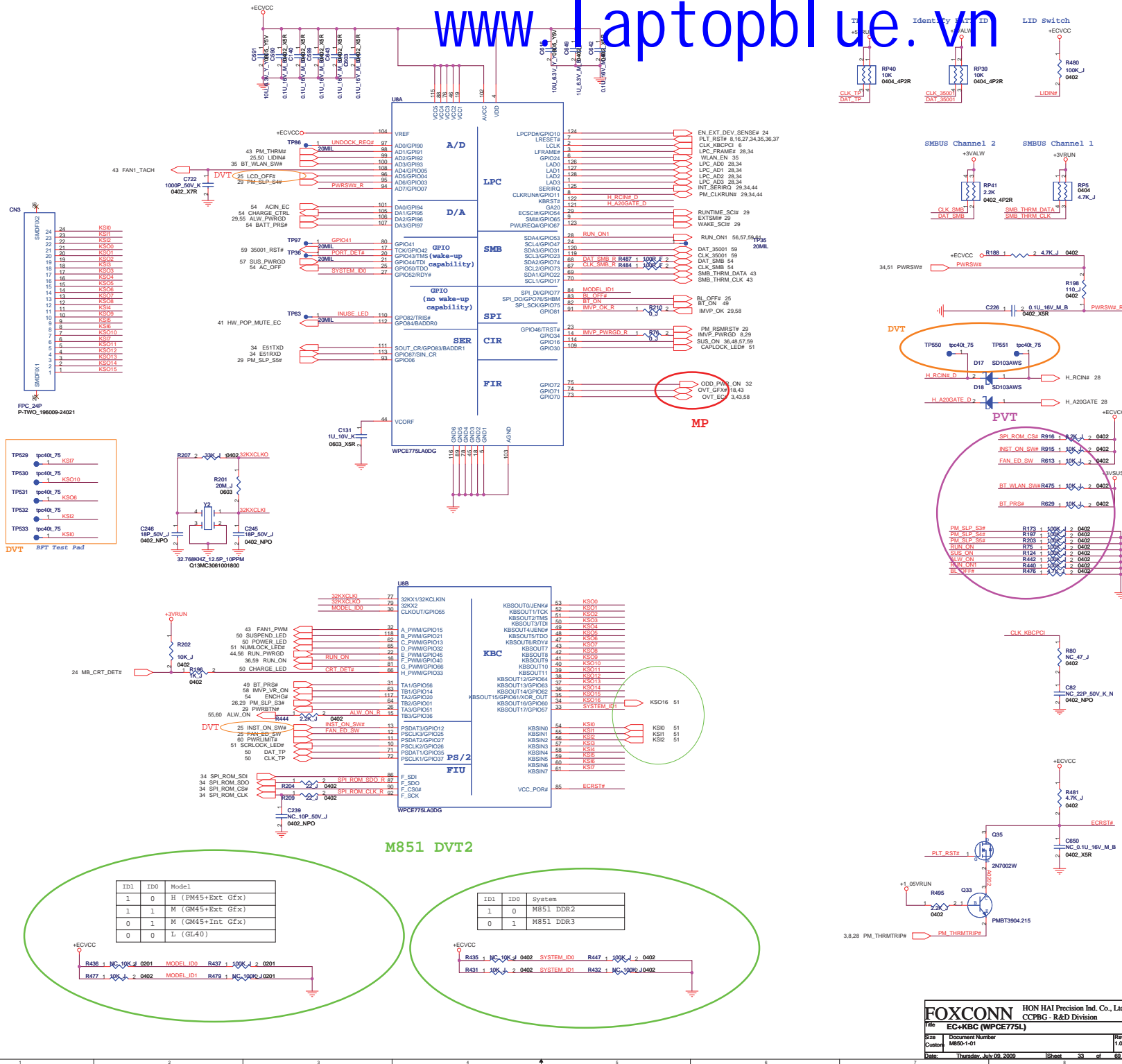
EVT

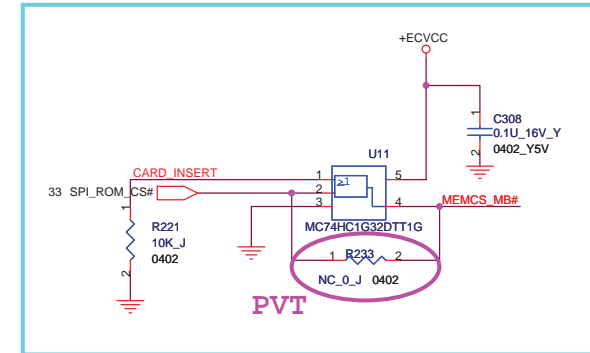
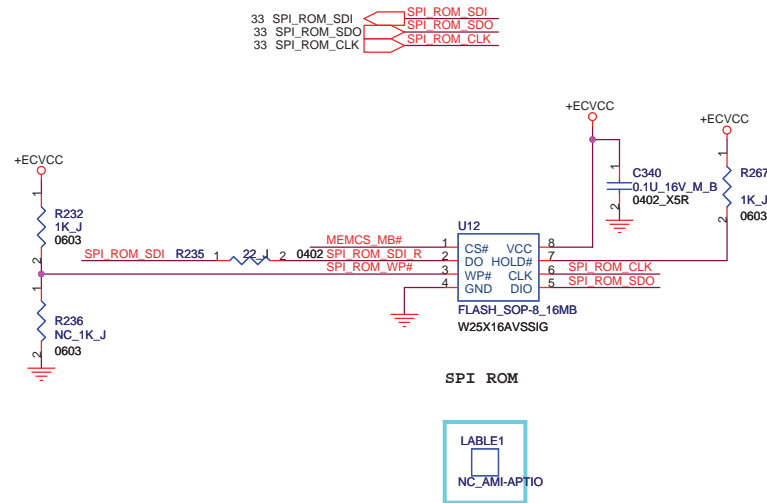
## SATA ODD CONN



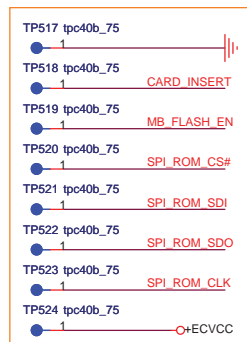
<http://hobi-elektronika.net/>



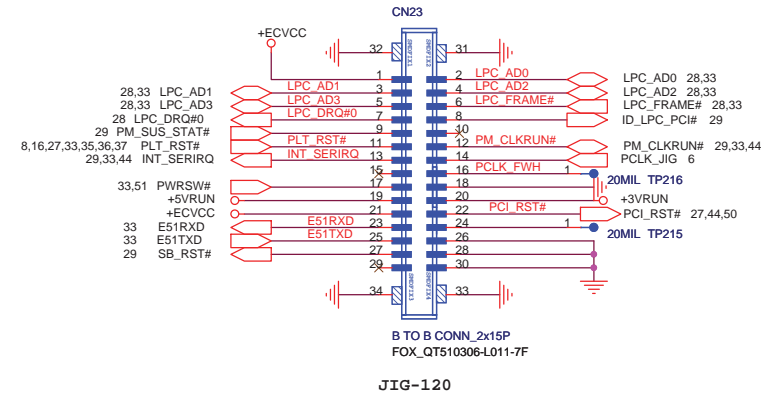
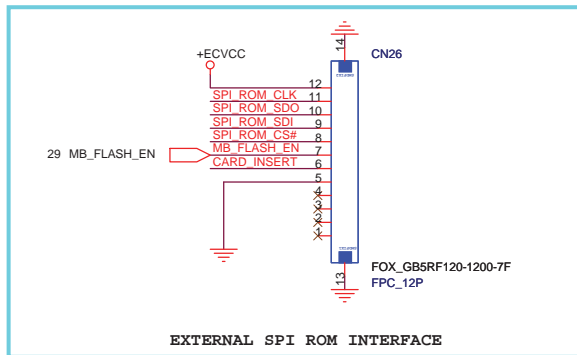




<http://hobi-elektronika.net/>



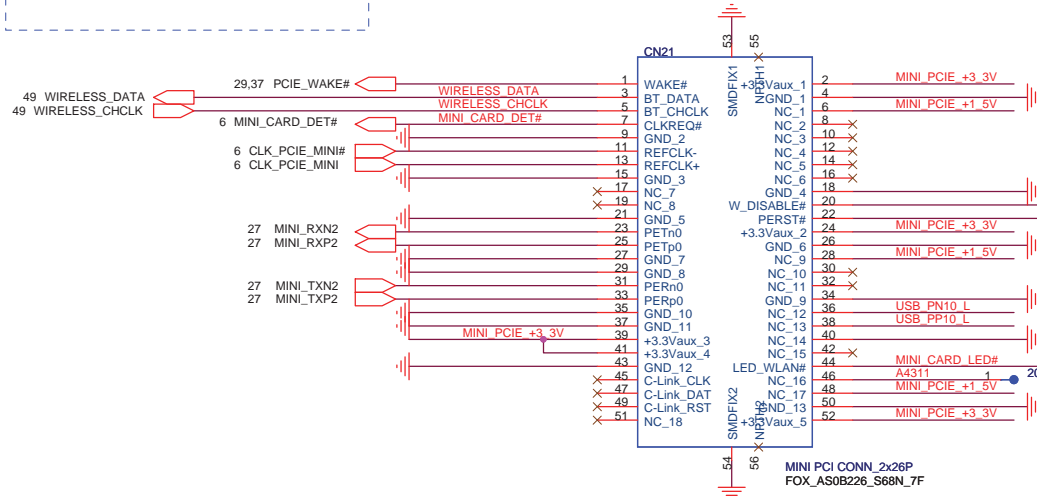
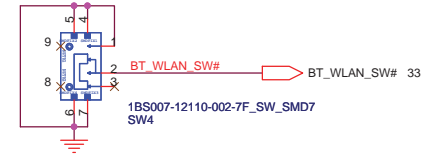
DVT BFT Test Pad



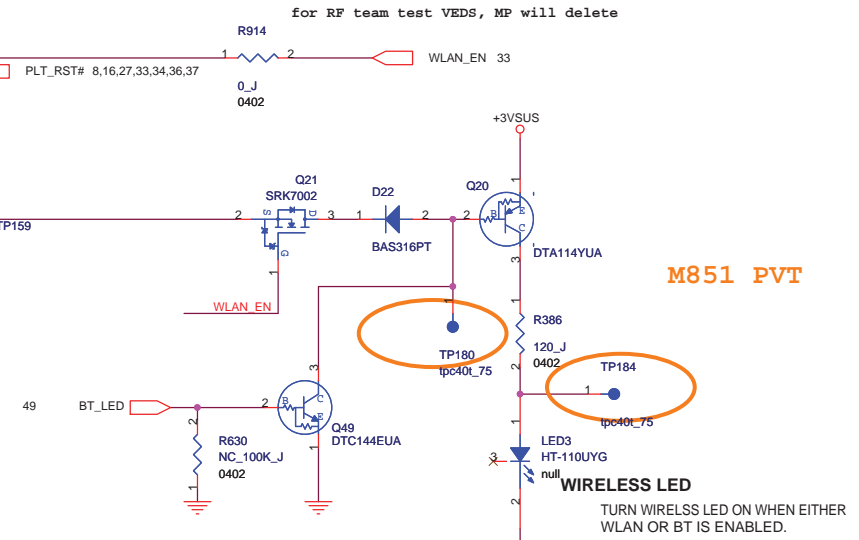


Half Mini Card

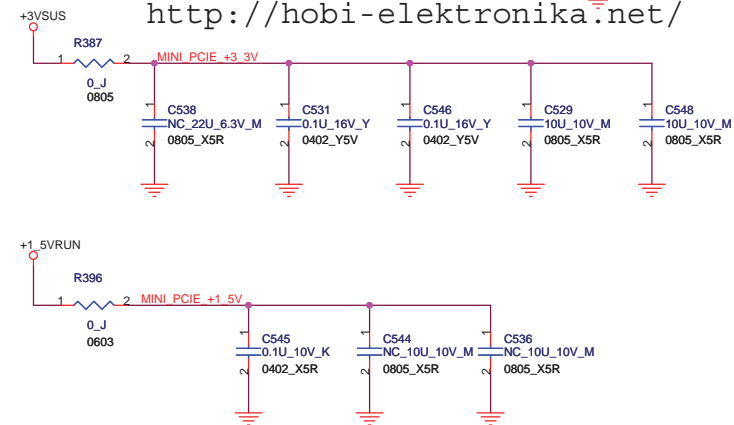
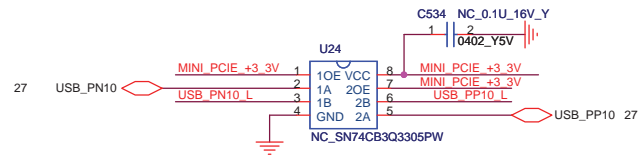
+1\_5V=>0.5A Peak/0.375A Normal  
+3\_3VAux=>2.75A Peak/1.1A Normal



Half Mini Card  
WLAN



<http://hobi-elektronika.net/>



Pin2,4 & Pin12,14  
Pin3,5 & Pin11,13  
short for test GMT577

EV7

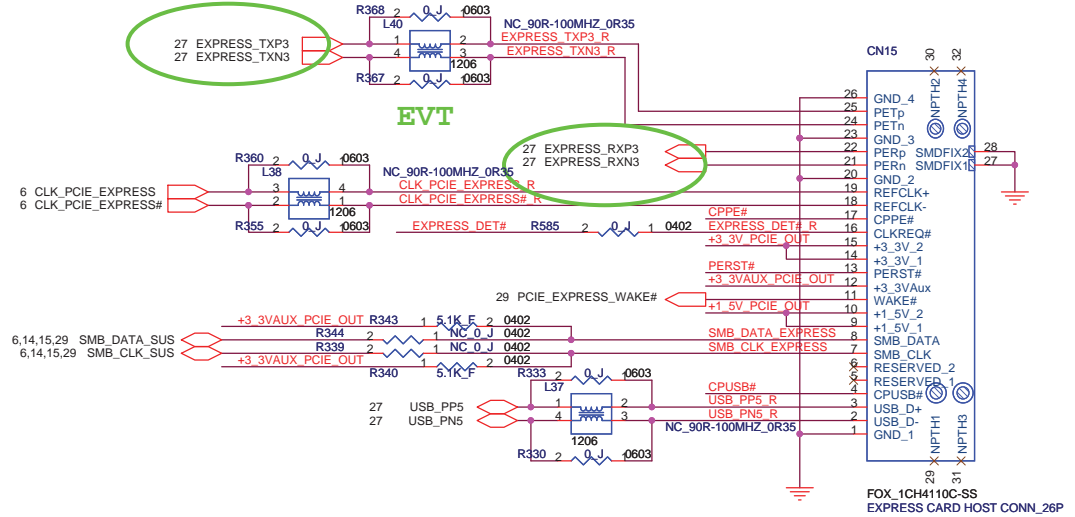
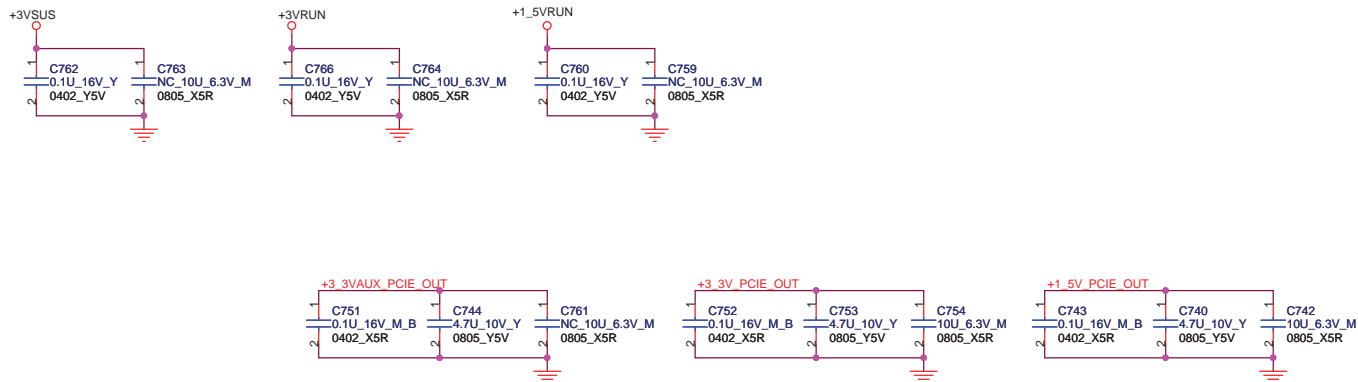
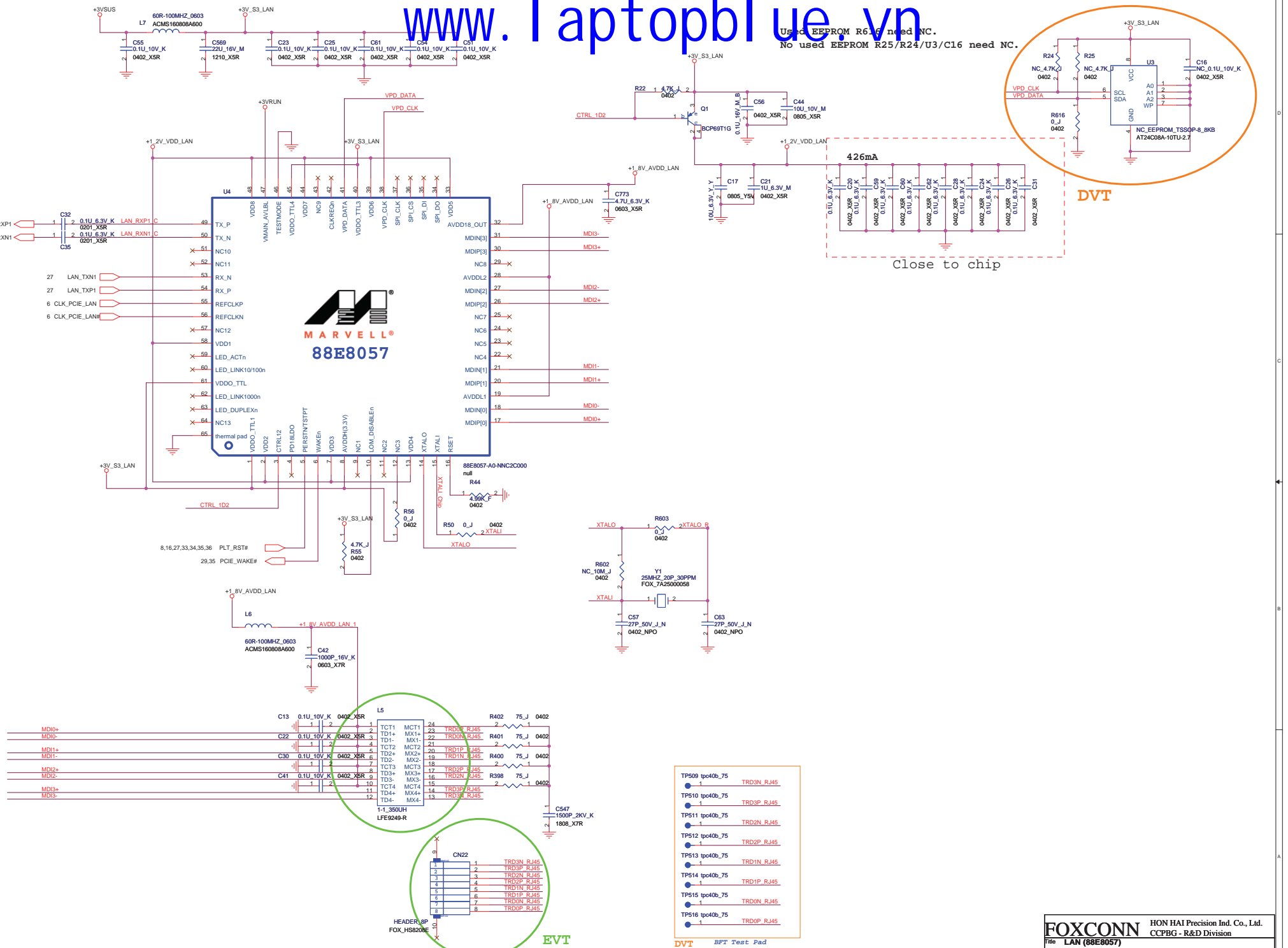
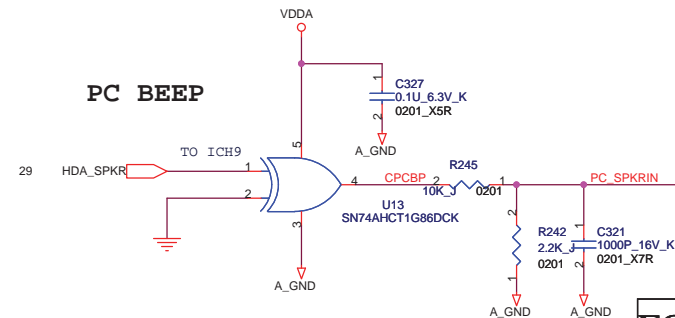
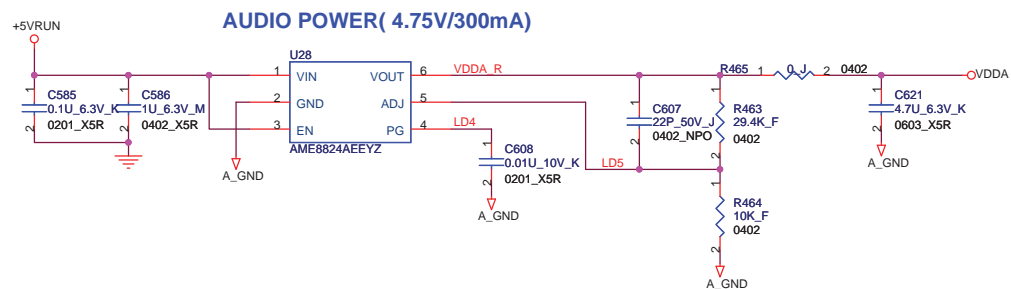
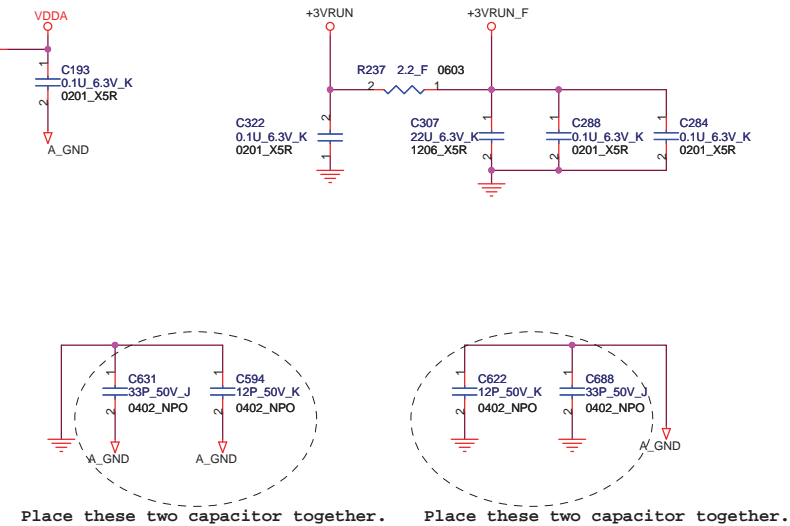


Diagram of Express Card Socket Housing. The housing is labeled "Express Card Socket Housing" and "EXPRESSCARD\_26P FOX\_1CX42201-SM". It shows two pins, PTH1 and PTH2, connected to ground symbols.

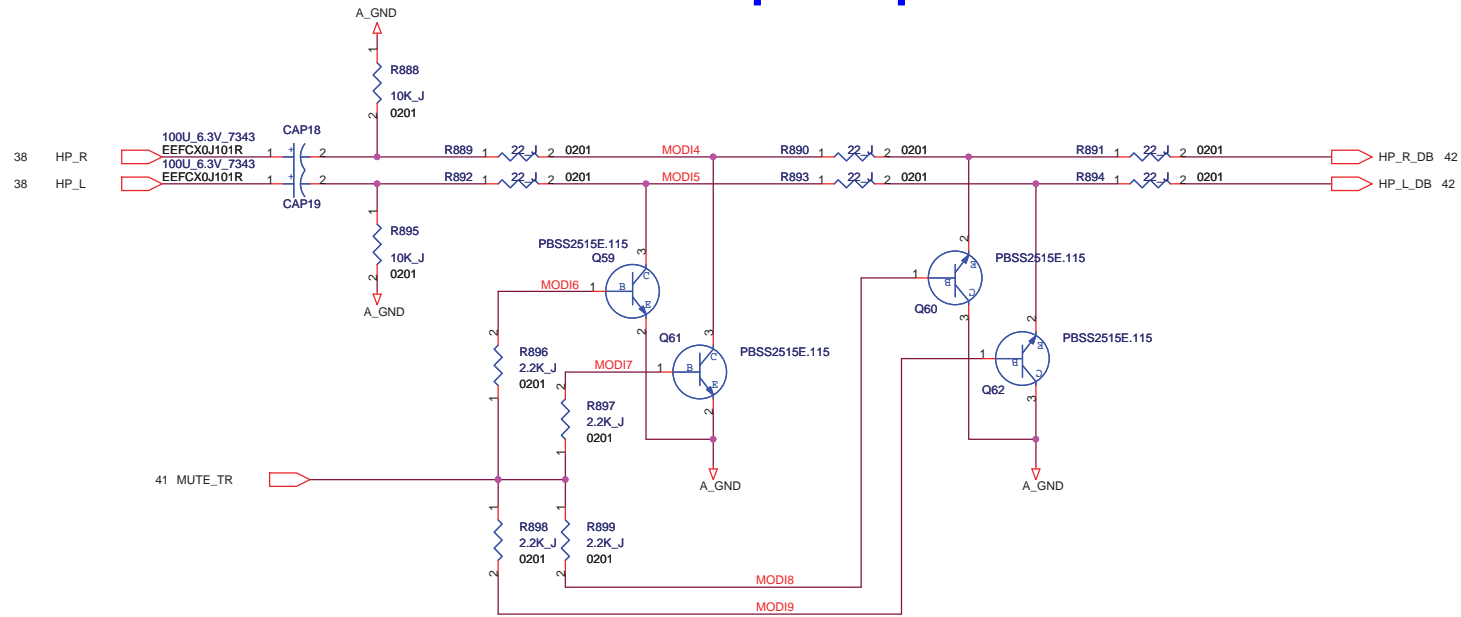


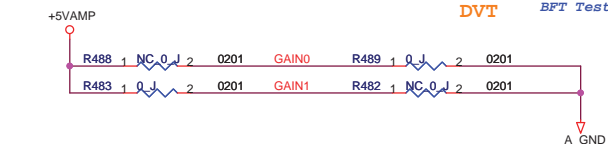
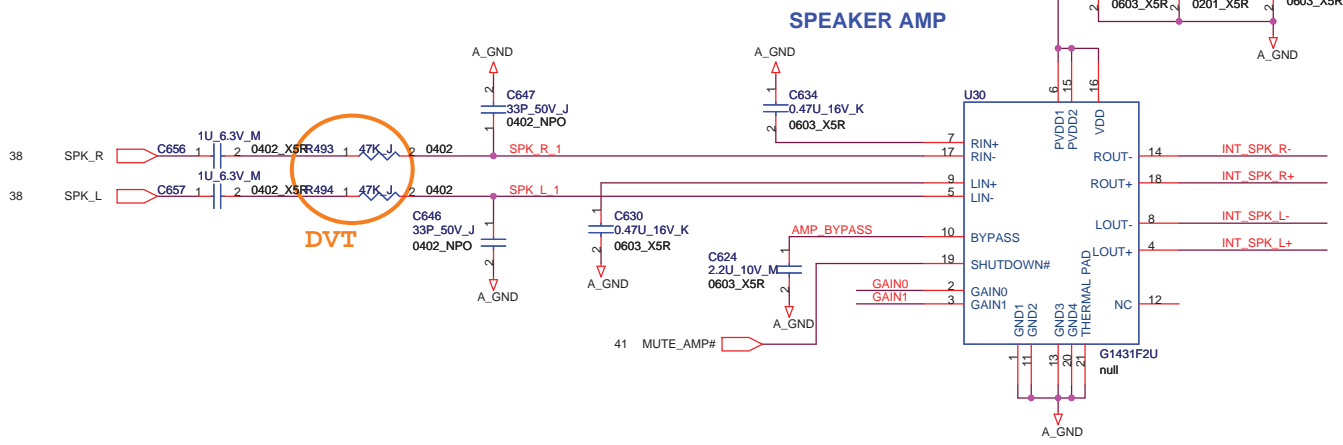
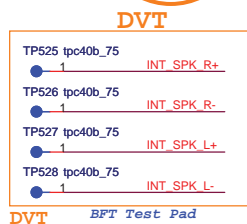
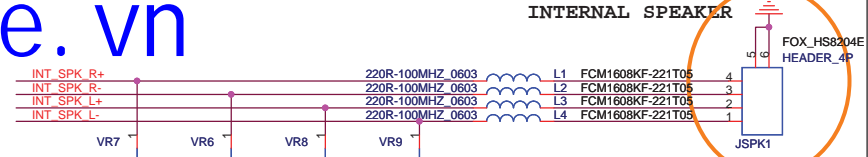
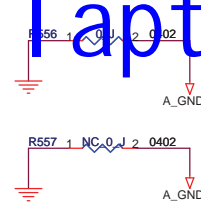
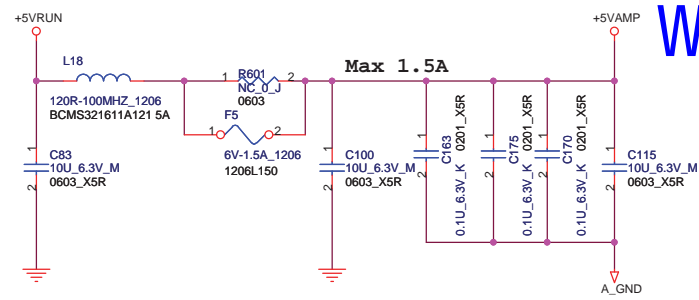
Used EEPROM R616 need NC.  
No used EEPROM R25/R24/U3/C16 need NC.



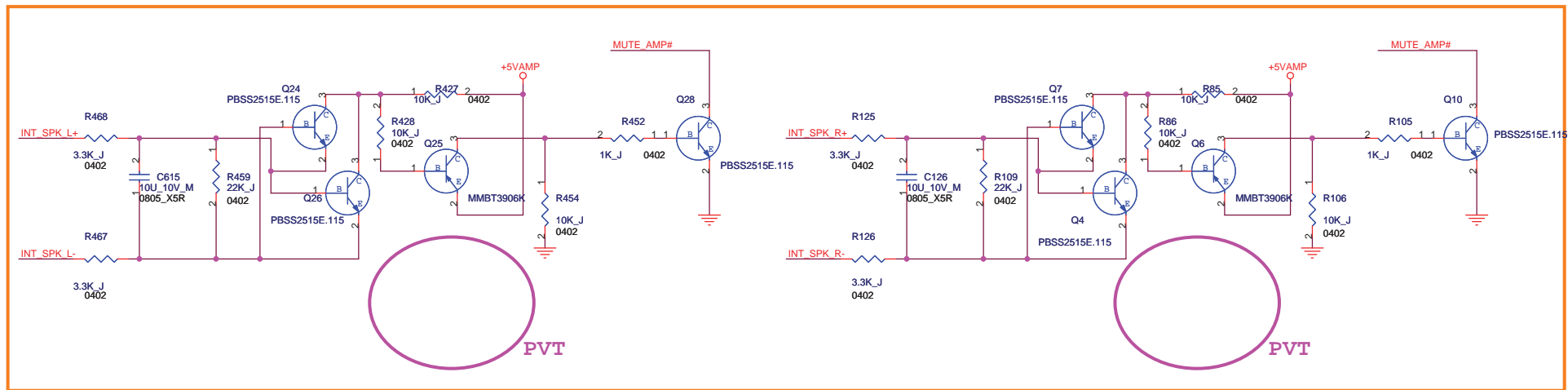




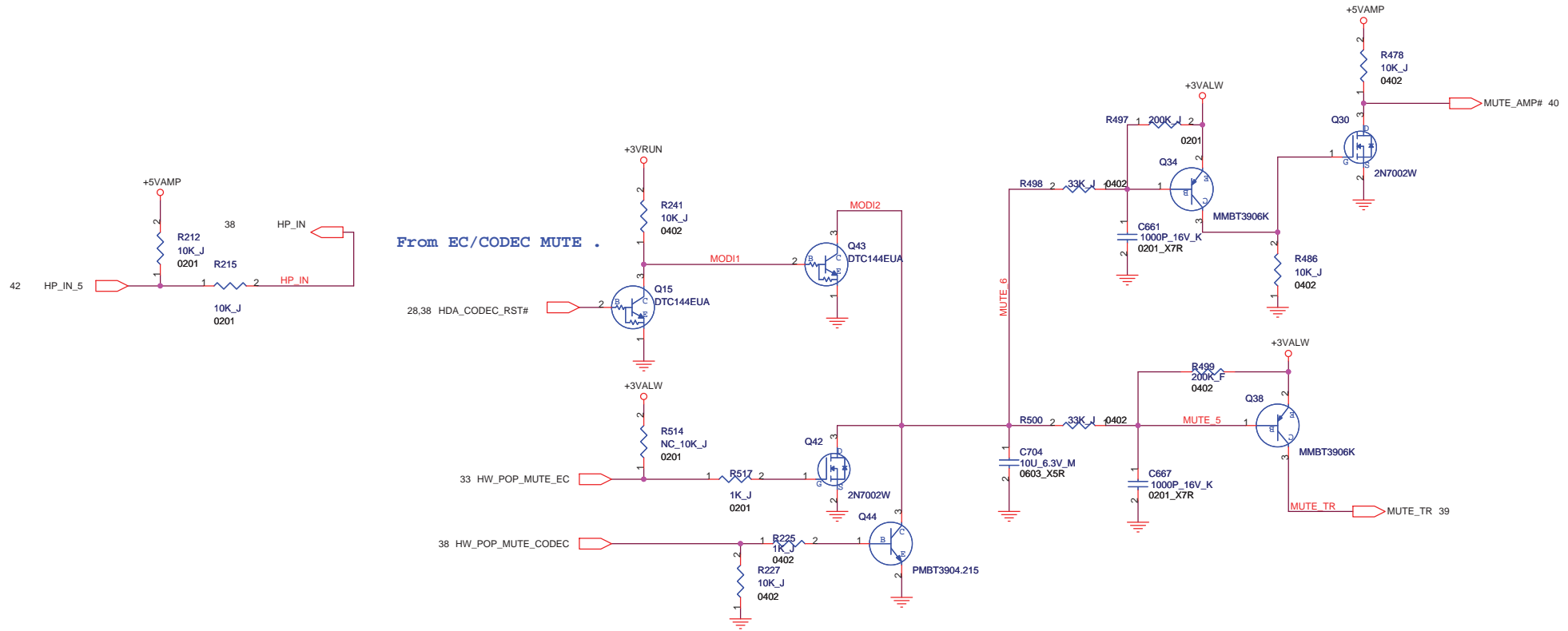


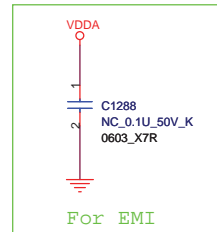
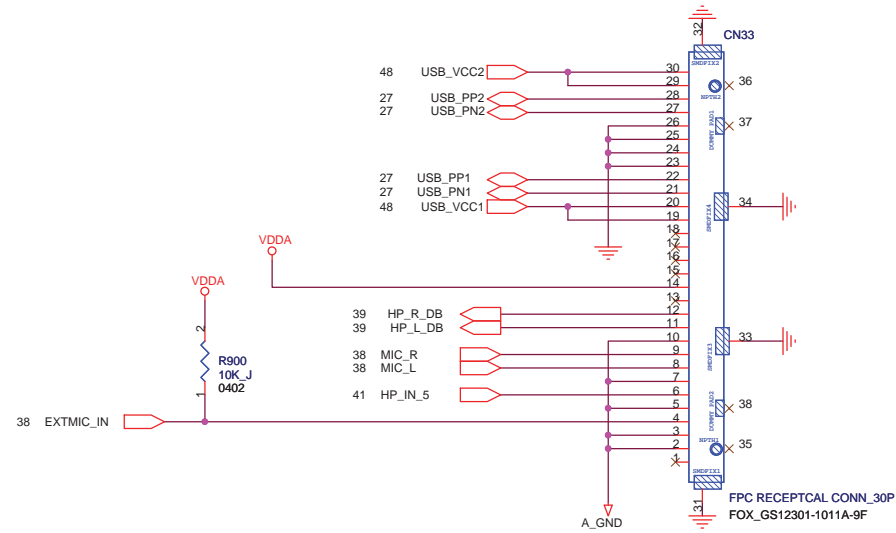


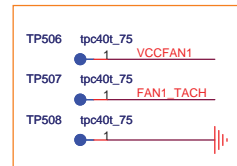
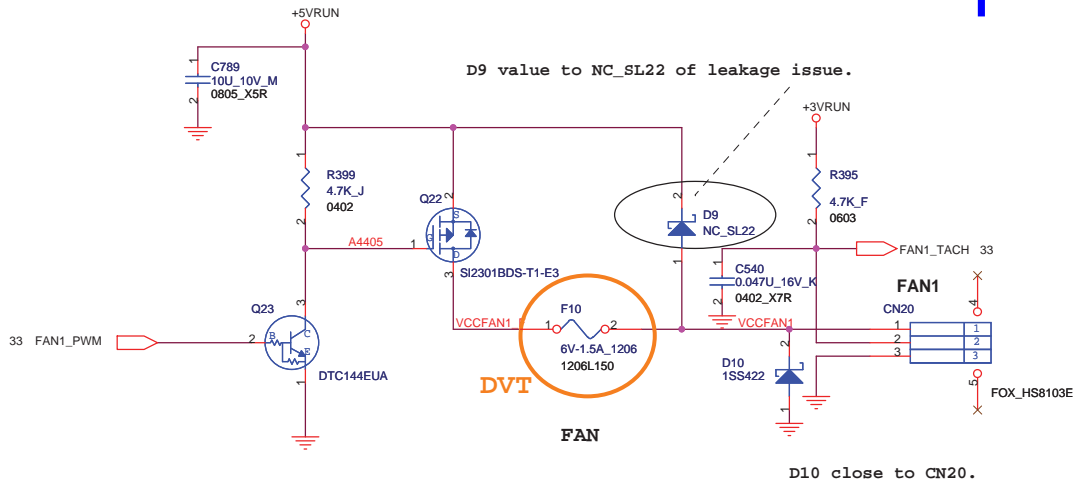
	GAIN0	GAIN1
6 dB	0	0
10 dB	0	1
15.6 dB	1	0
21.6 dB	1	1



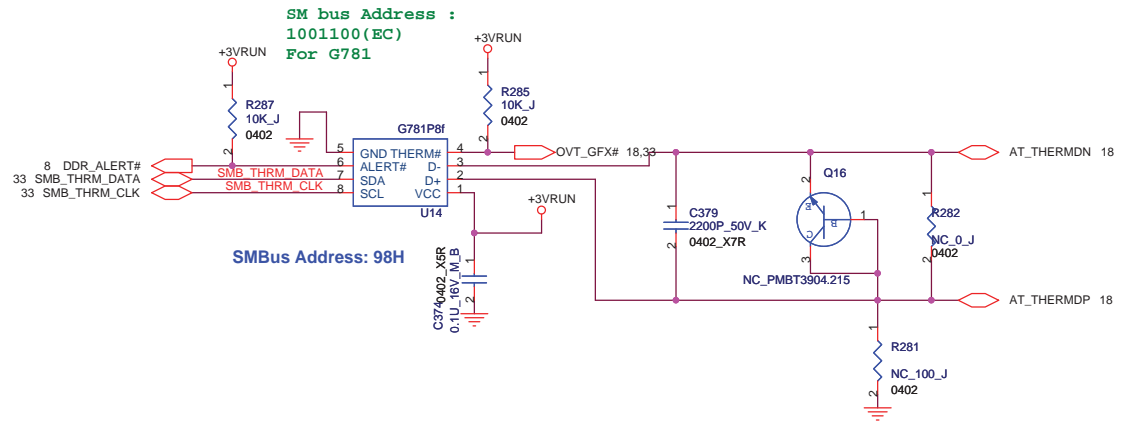
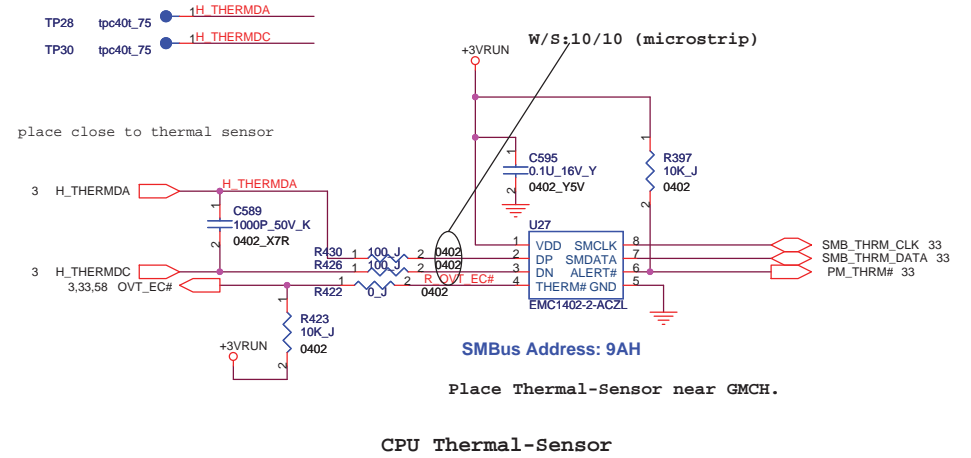
For Mor request, add the speaker cable short protection circuit

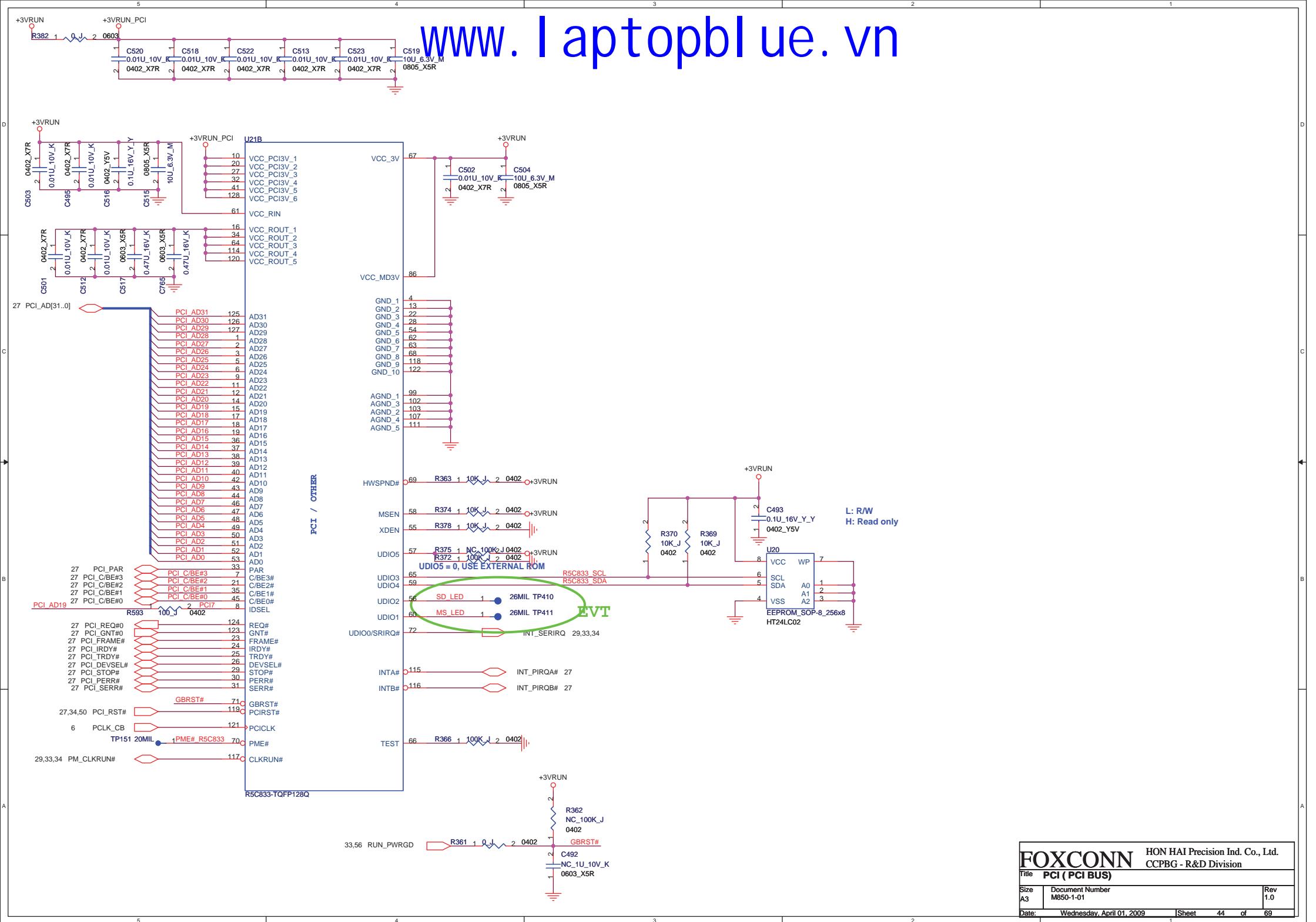






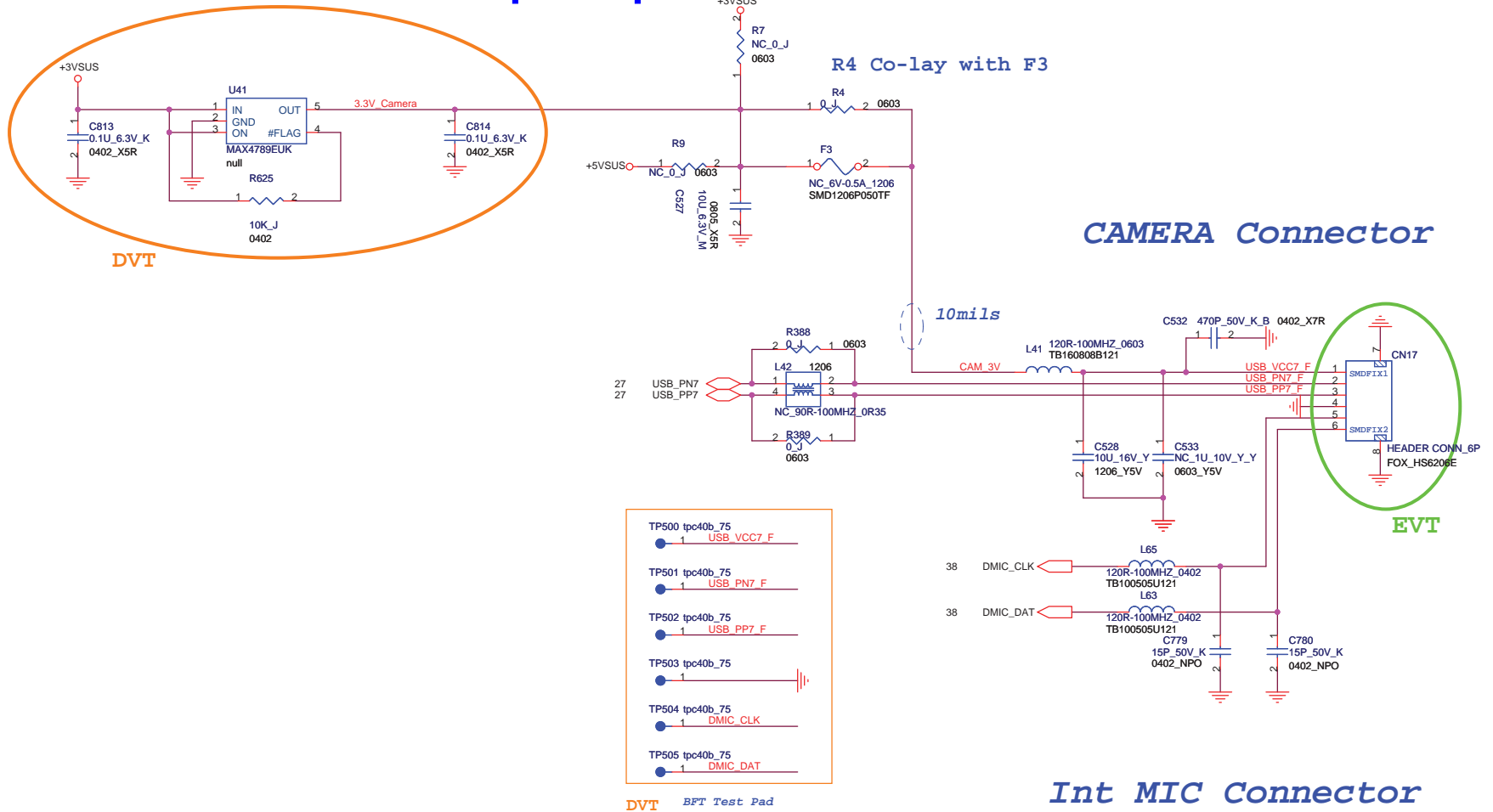
DVT BFT Test Pad

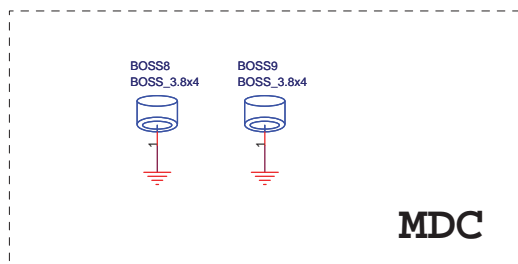
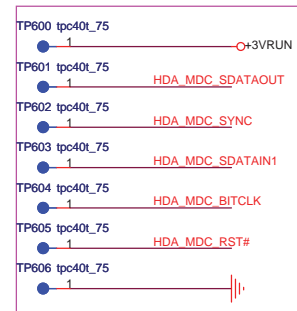
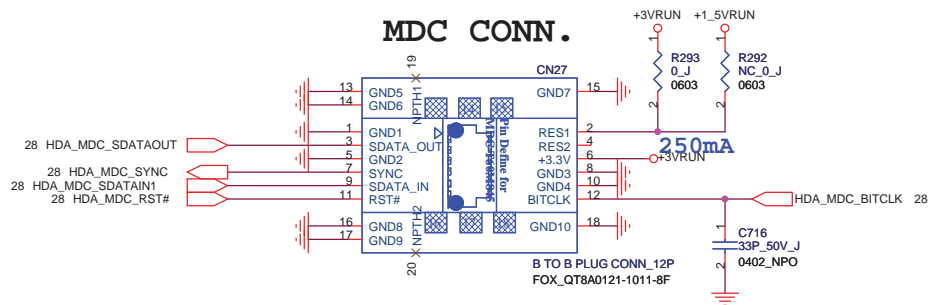
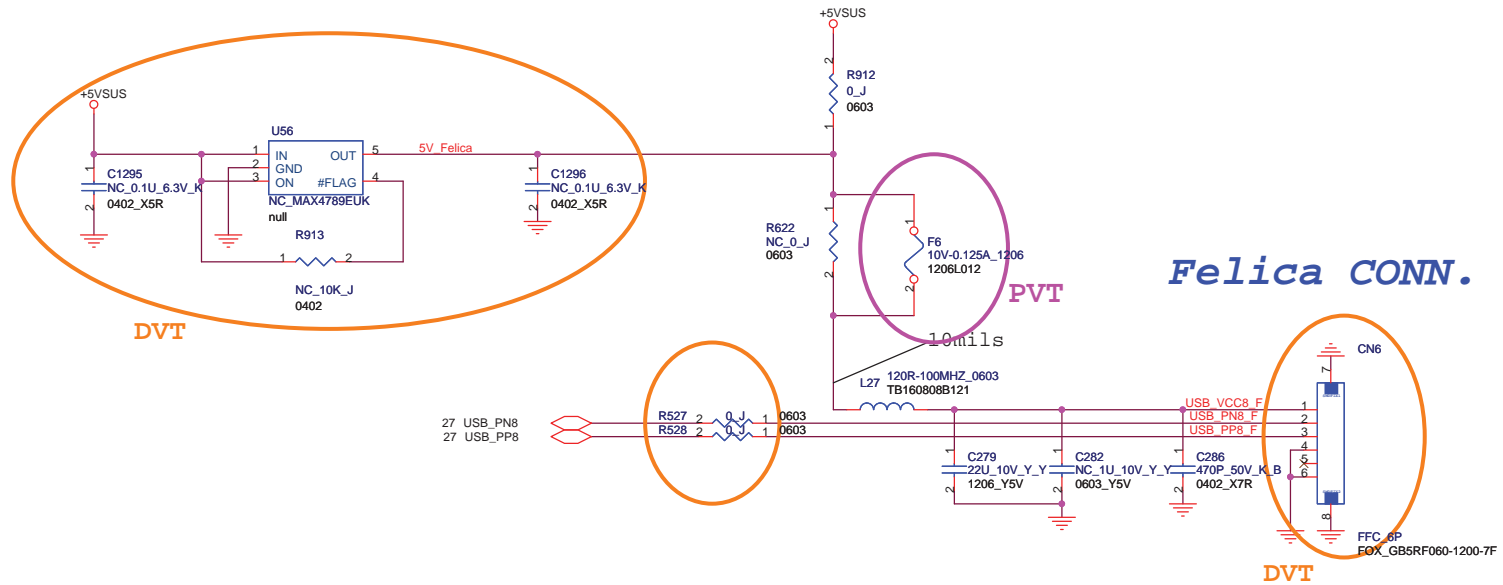








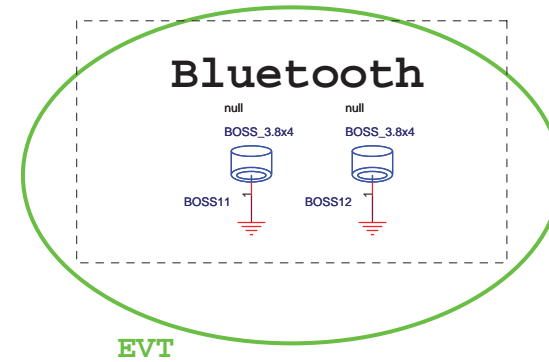
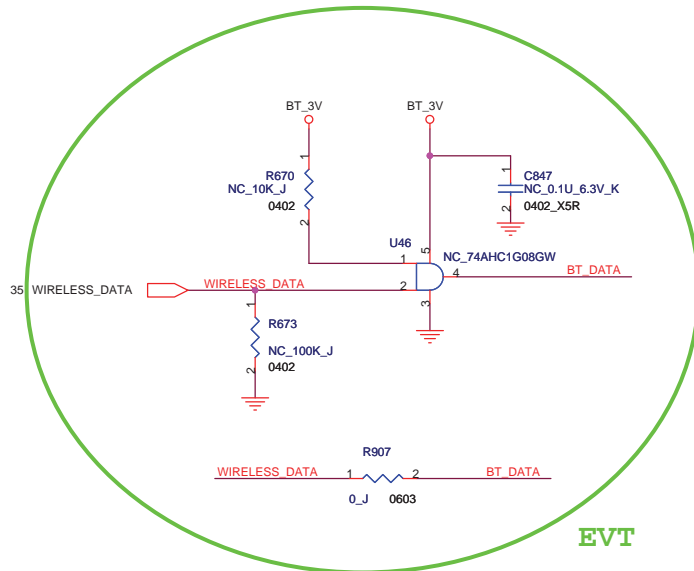
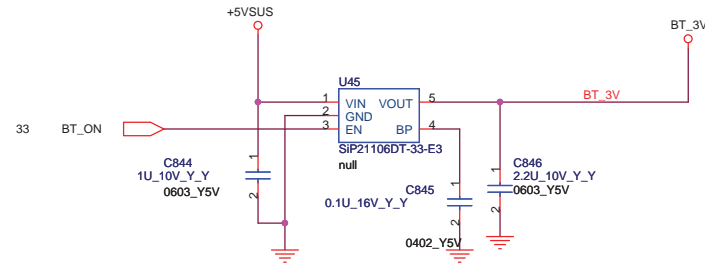
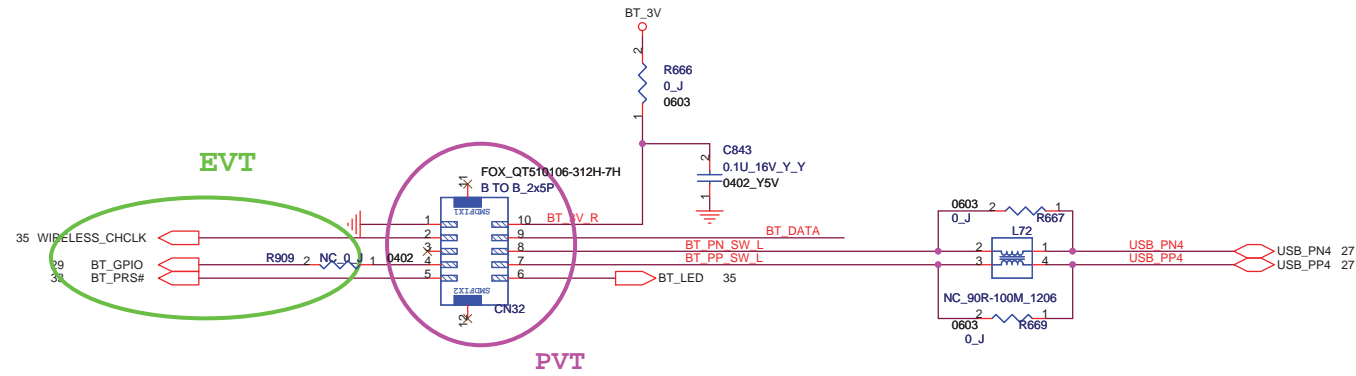


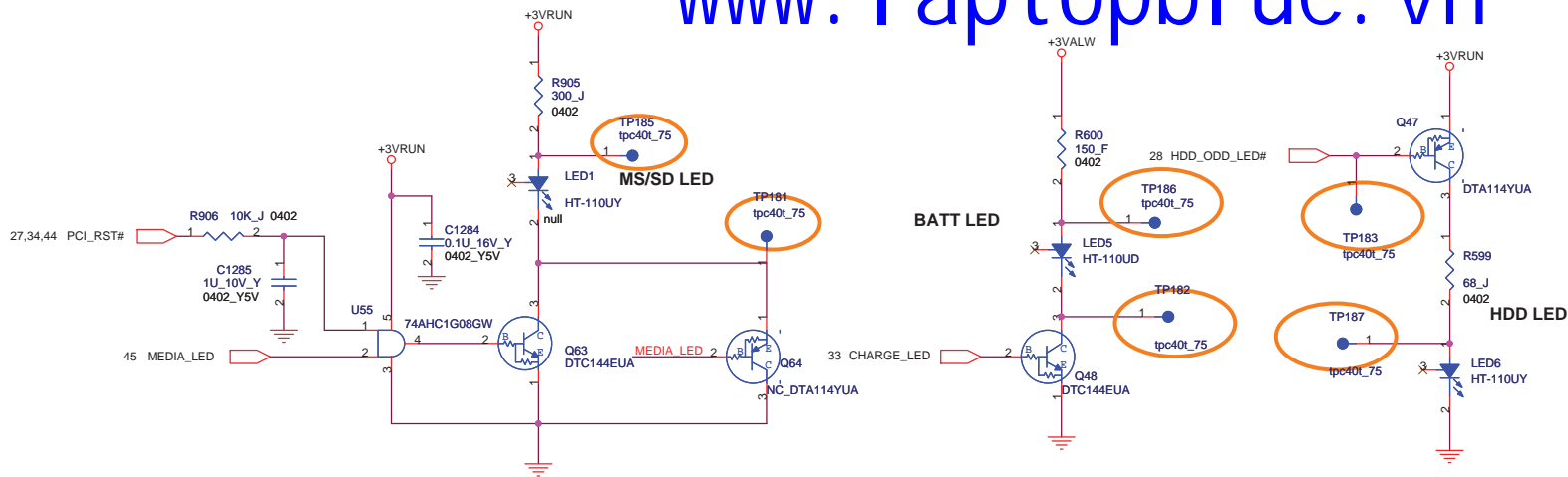




# www.laptopblue.vn

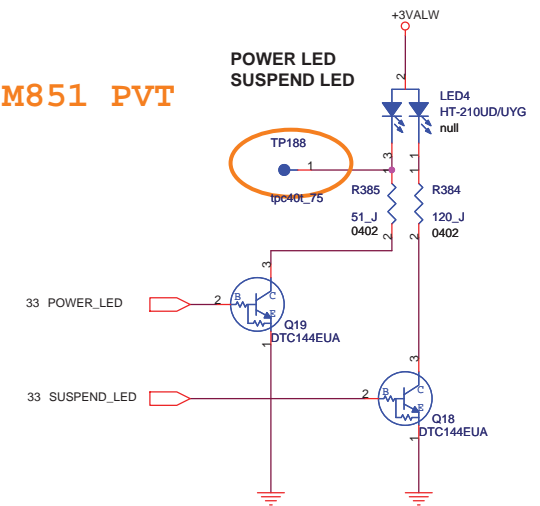
## Bluetooth connector





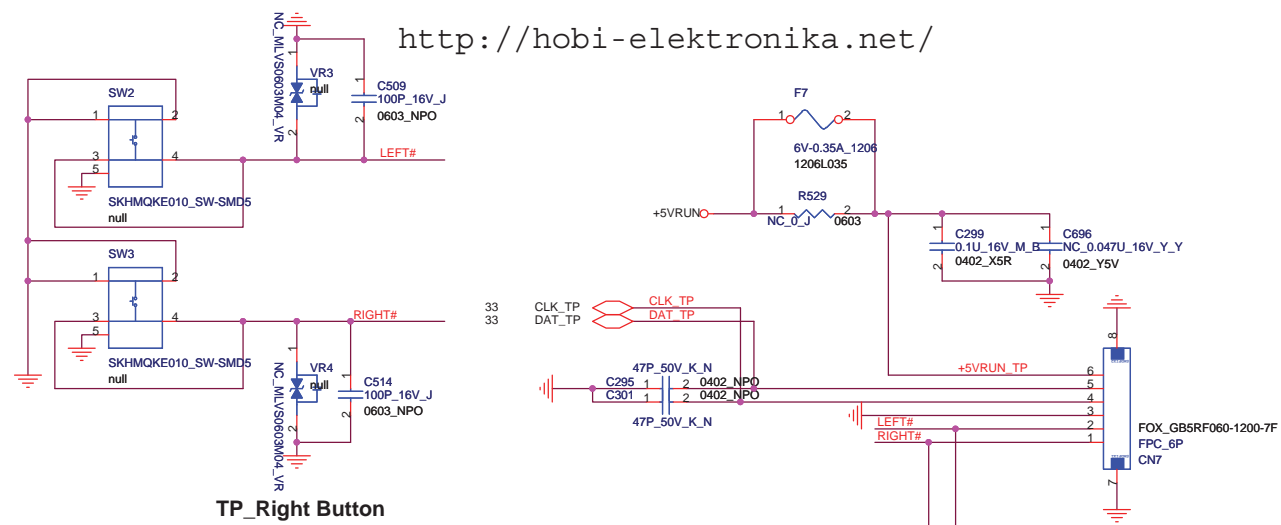
M851 PVT

POWER LED  
SUSPEND LED



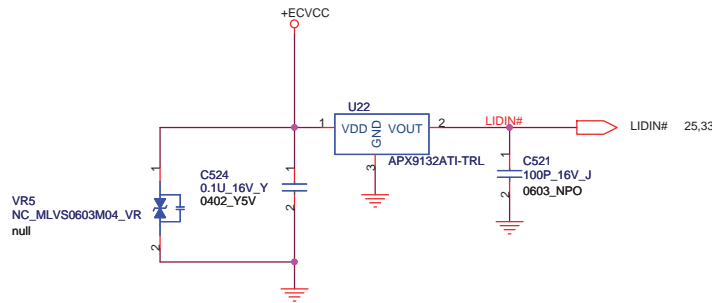
TP\_LEFT Button

<http://hobi-elektronika.net/>

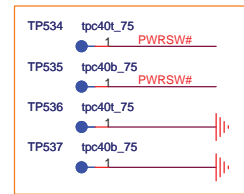
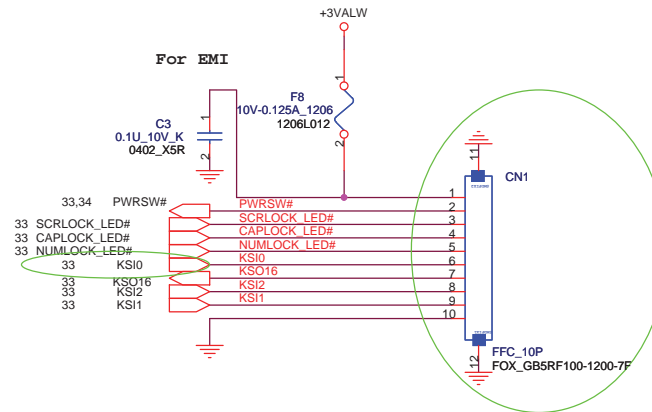


TP\_Right Button

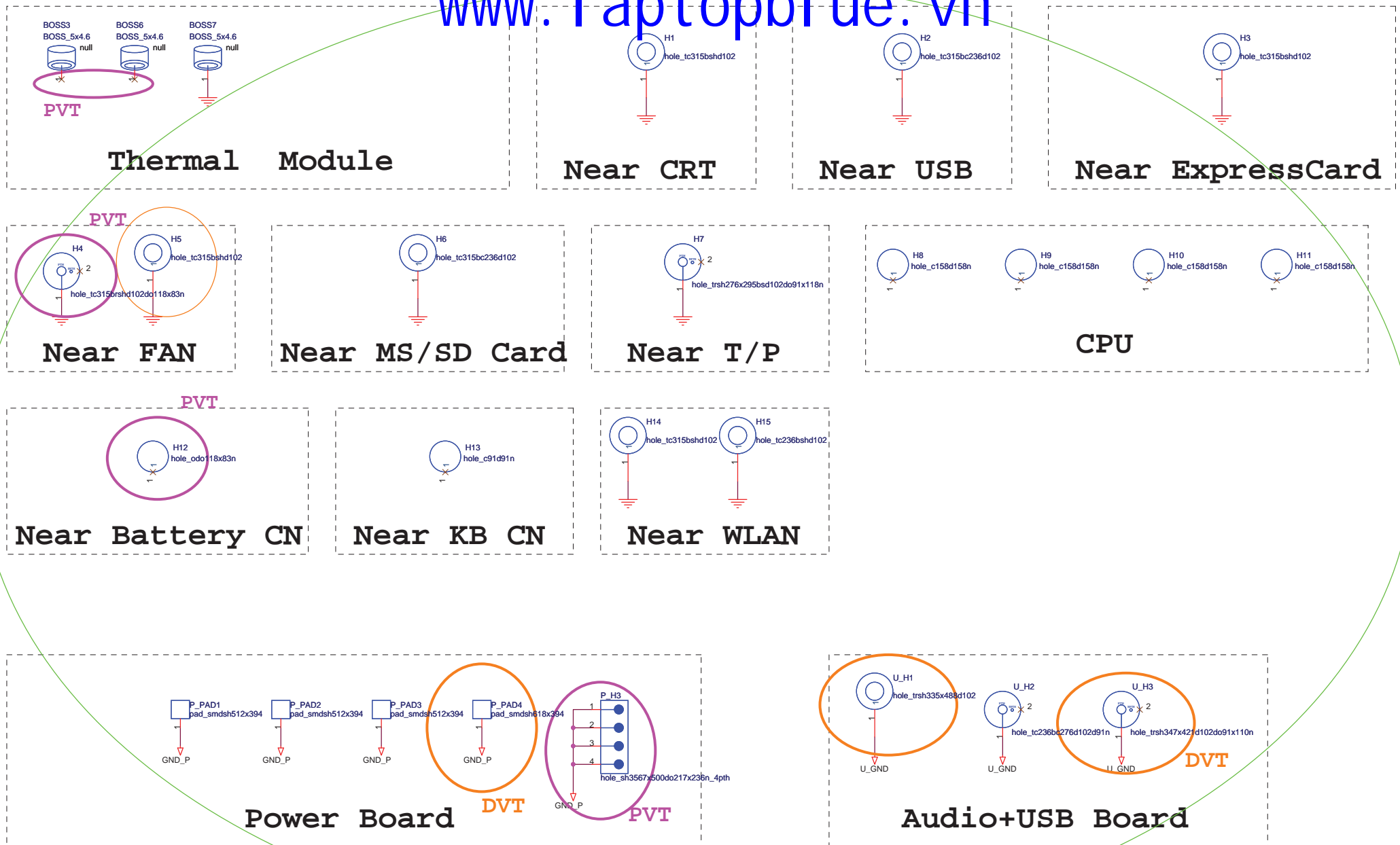
LID Switch

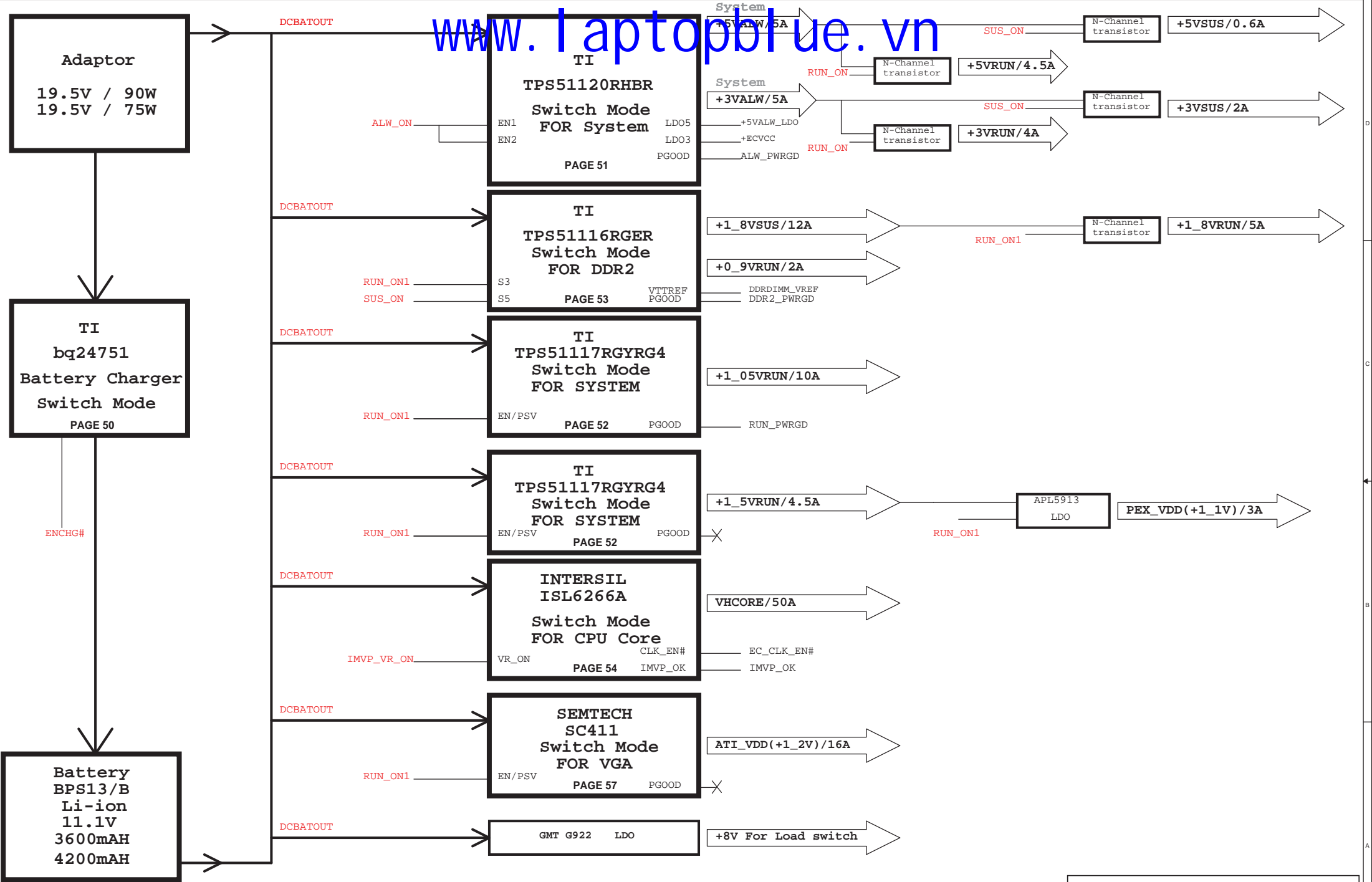


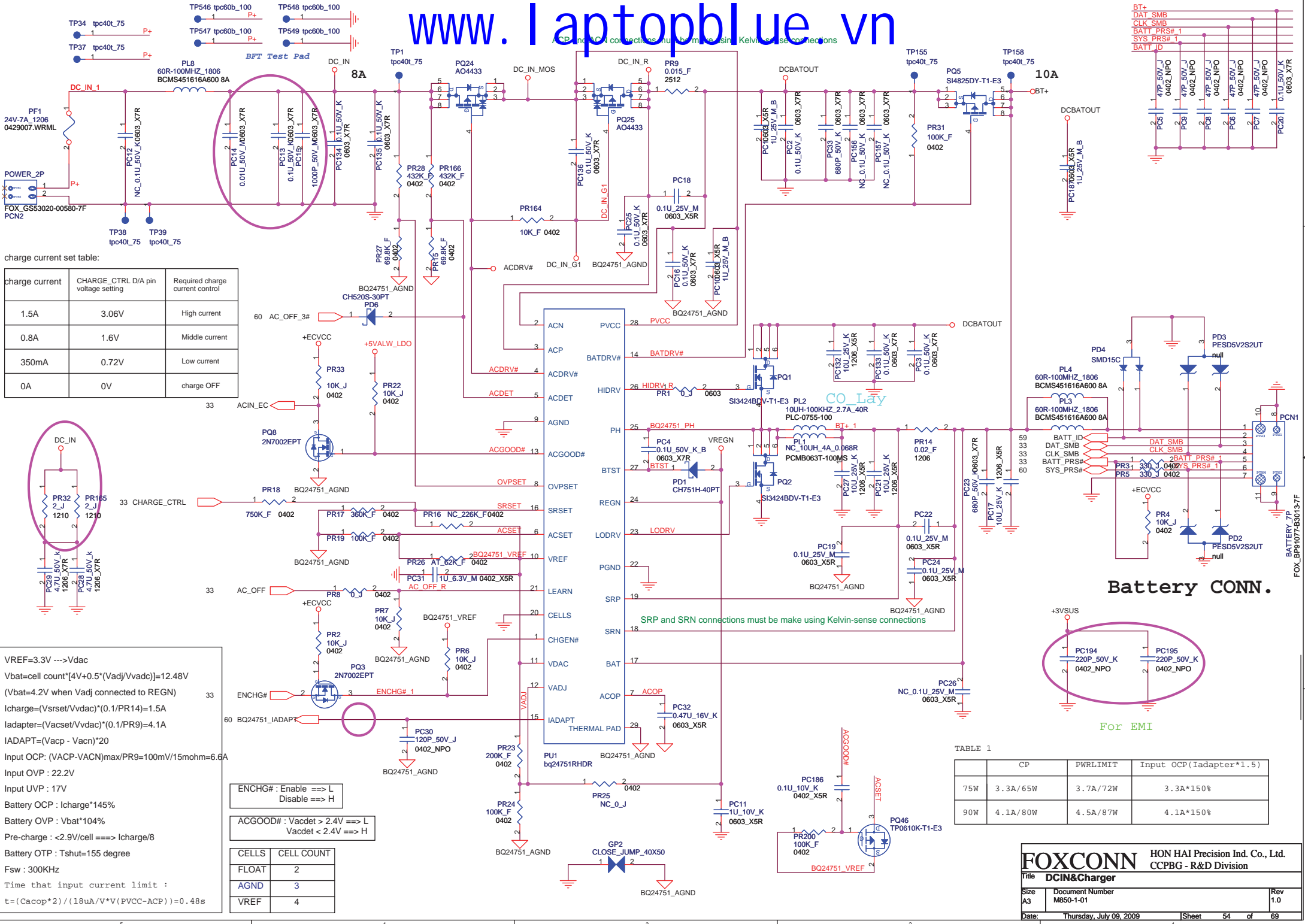




DVT BFT Test Pad

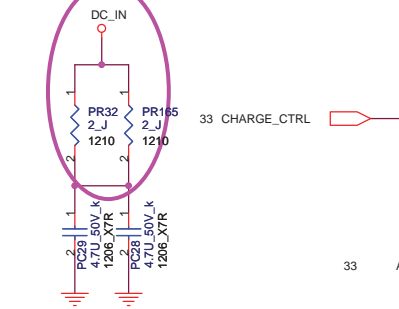






charge current set table:

charge current	CHARGE_CTRL D/A pin voltage setting	Required charge current control
1.5A	3.06V	High current
0.8A	1.6V	Middle current
350mA	0.72V	Low current
0A	0V	charge OFF

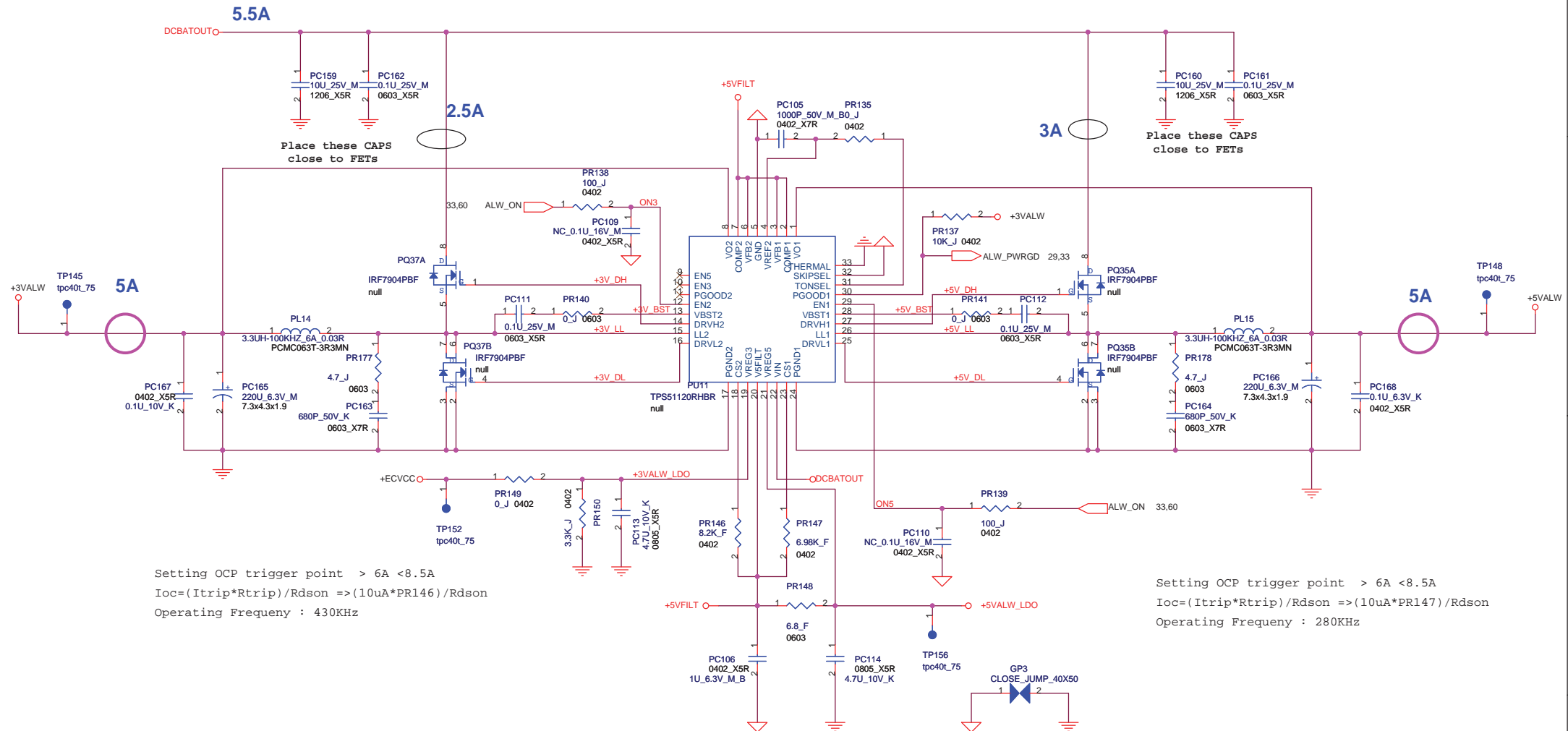


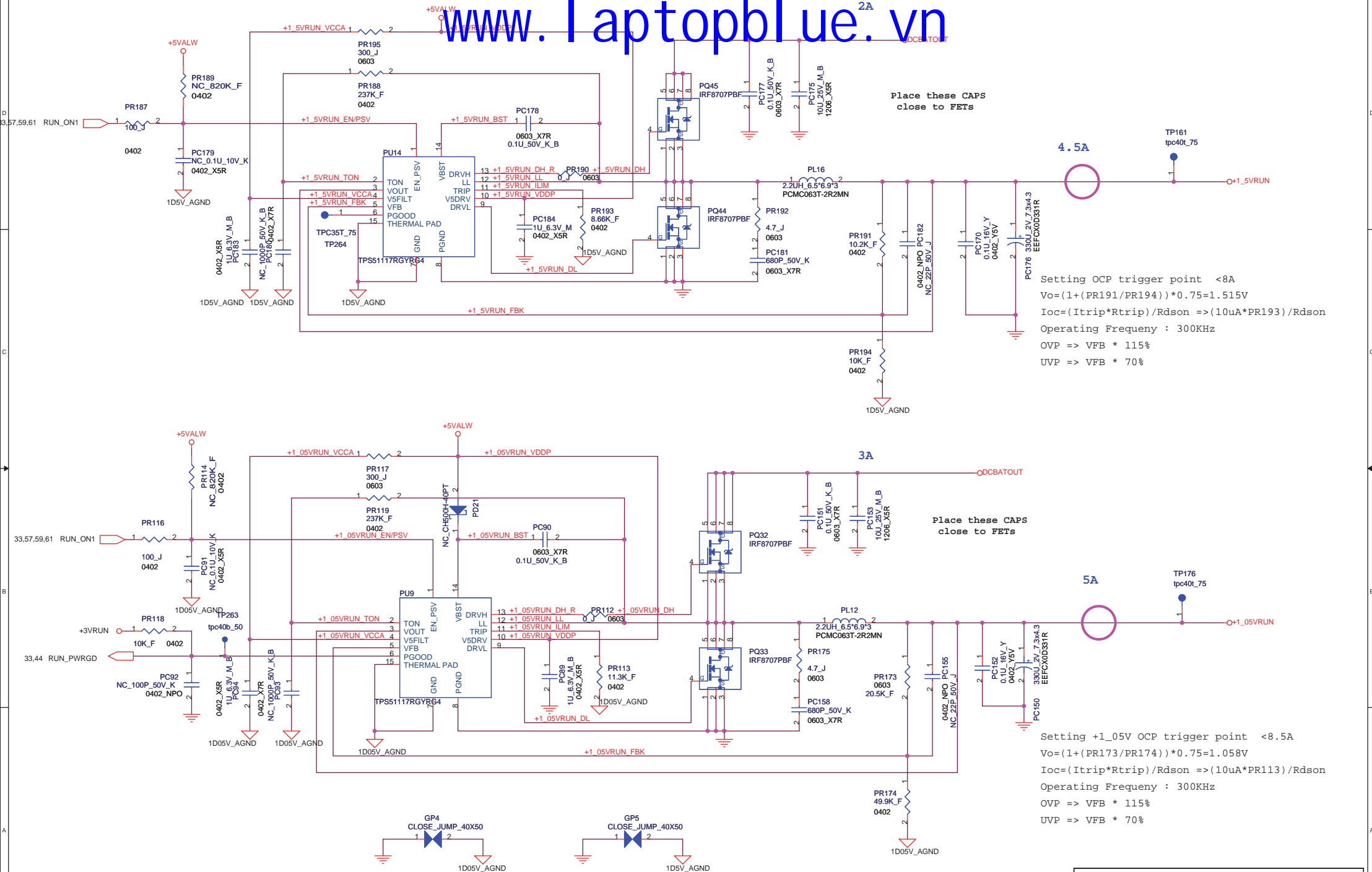
VREF=3.3V --->Vdac  
Vbat=cell count\*[4V+0.5\*(Vadj/Vvdc)]=12.48V  
(Vbat=4.2V when Vadj connected to REGN)  
Icharge=(Vsrset/Vvdc)\*(0.1/PR14)=1.5A  
Iadapter=(Vacset/Vvdc)\*(0.1/PR9)=4.1A  
IADAPT=(Vacp - Vacn)\*20  
Input OCP: (VACP-VACN)max/PR9=100mV/15mohm=6.6A  
Input OVP: 22.2V  
Input UVP: 17V  
Battery OCP: Icharge\*145%  
Battery OVP: Vbat\*104%  
Pre-charge: <2.9V/cell ==> Icharge/8  
Battery OTP: Tshut=155 degree  
Fsw: 300KHz  
Time that input current limit: t=(Cacop\*2)/(18uA/V\*V(PVCC-ACP))=0.48s

ENCHG#: Enable ==> L Disable ==> H	
ACGOOD#: Vacdet > 2.4V ==> L Vacdet < 2.4V ==> H	
CELLS	CELL COUNT
FLOAT	2
AGND	3
VREF	4

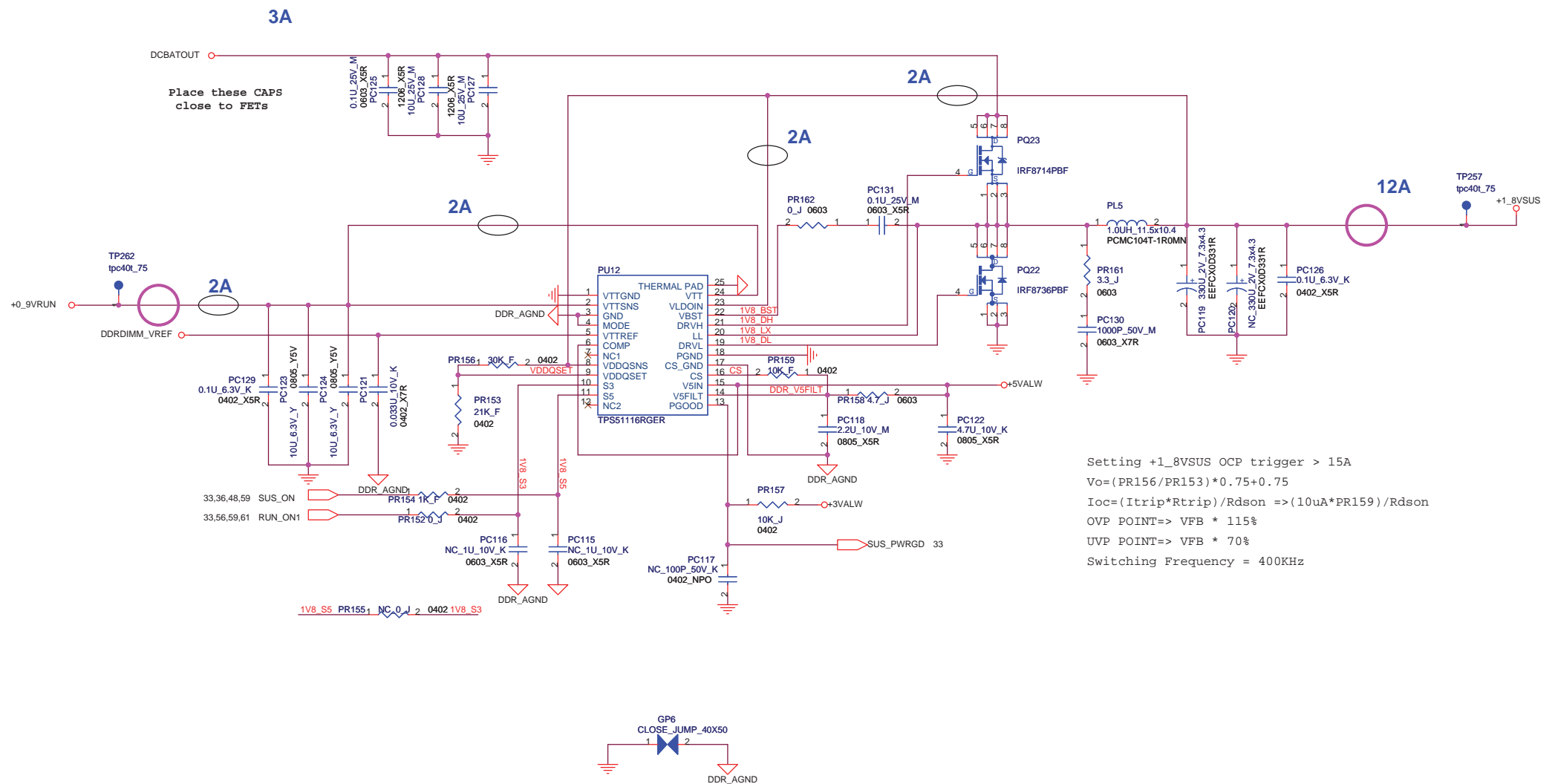
TABLE 1

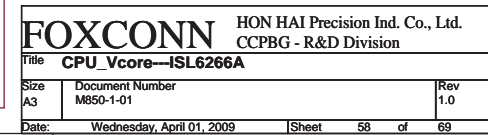
	CP	PWRLIMIT	Input OCP(Iadapter*1.5)
75W	3.3A/65W	3.7A/72W	3.3A*150%
90W	4.1A/80W	4.5A/87W	4.1A*150%

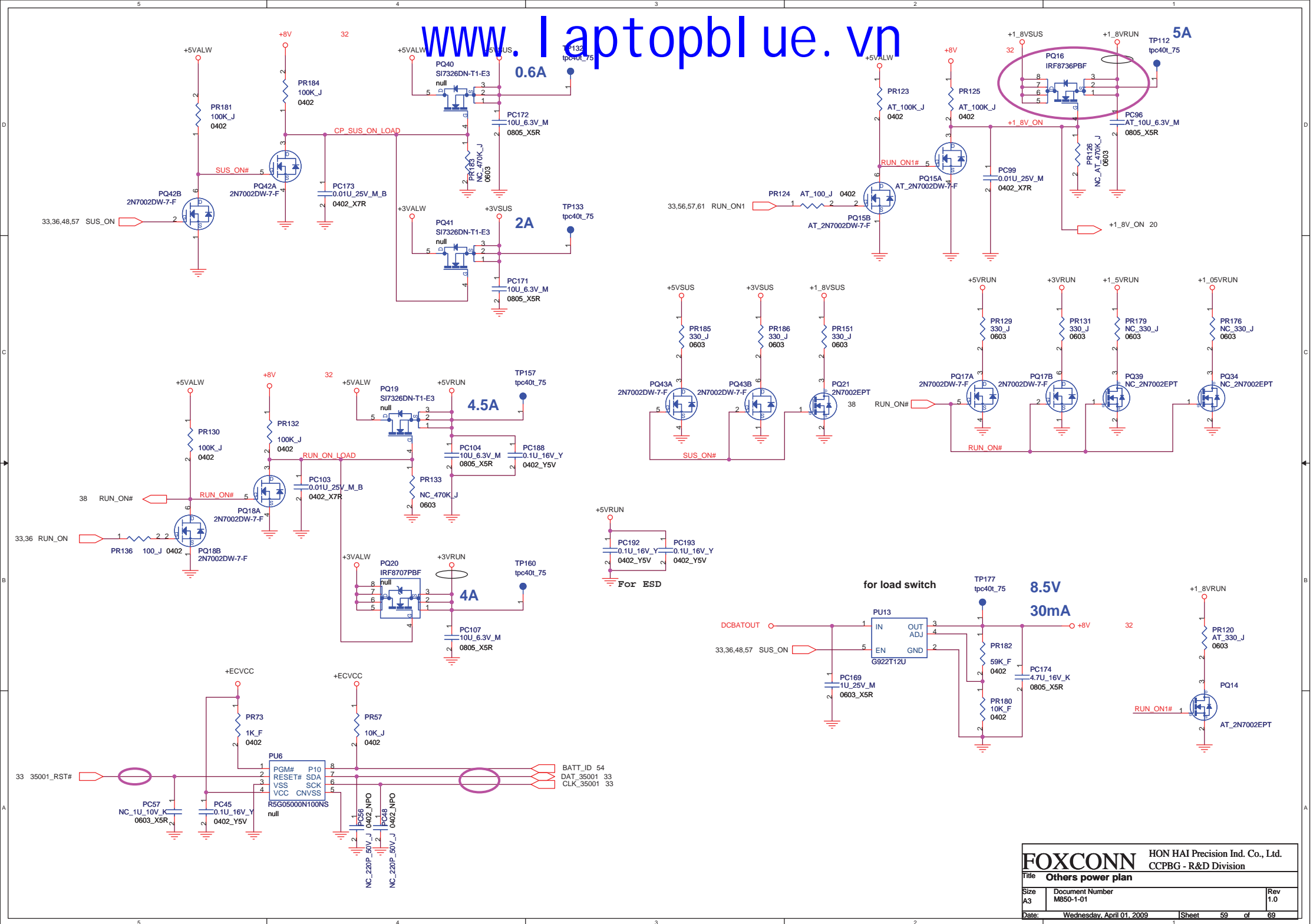


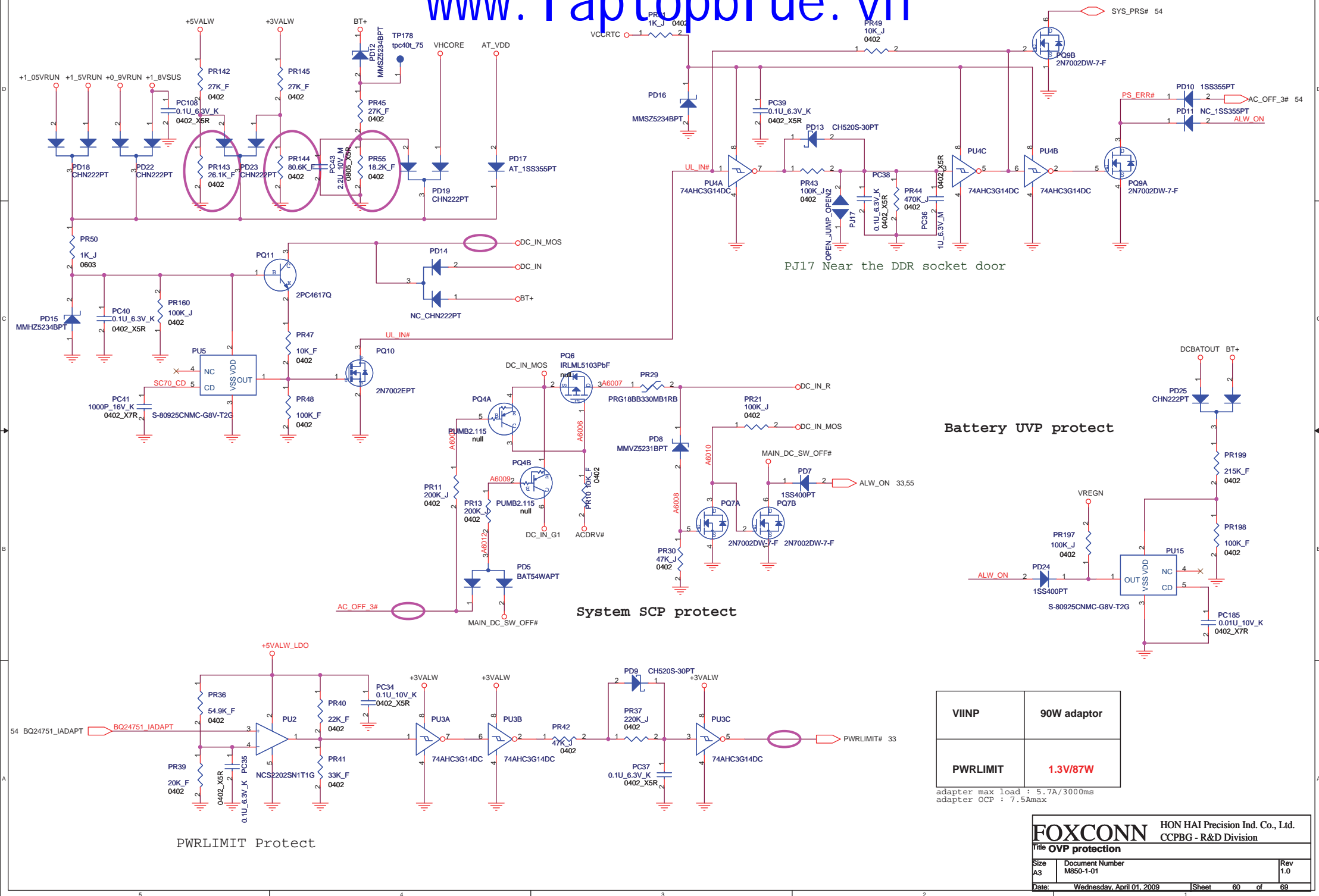








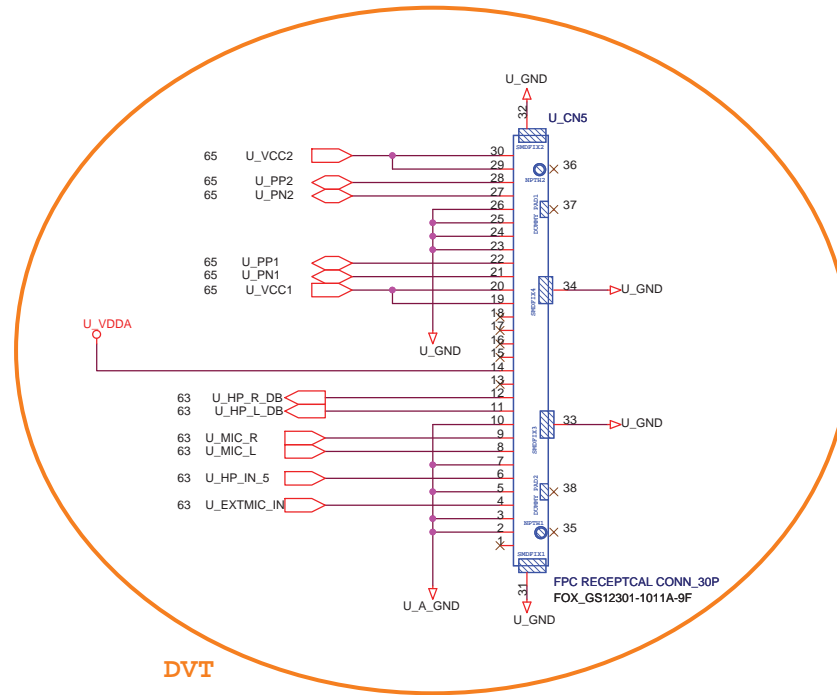


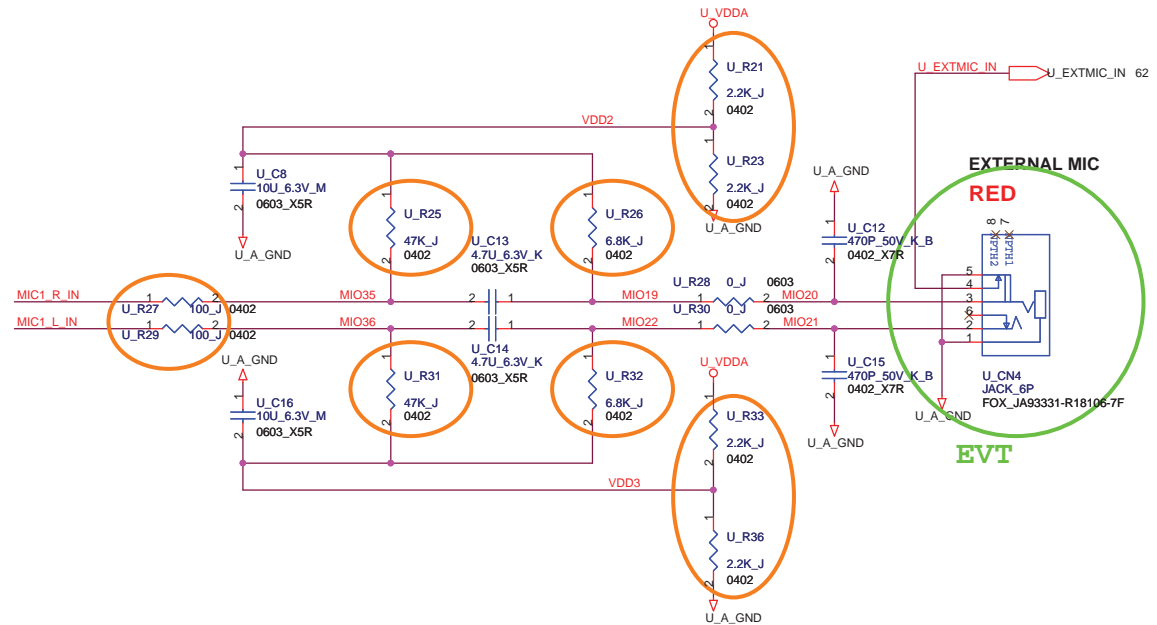
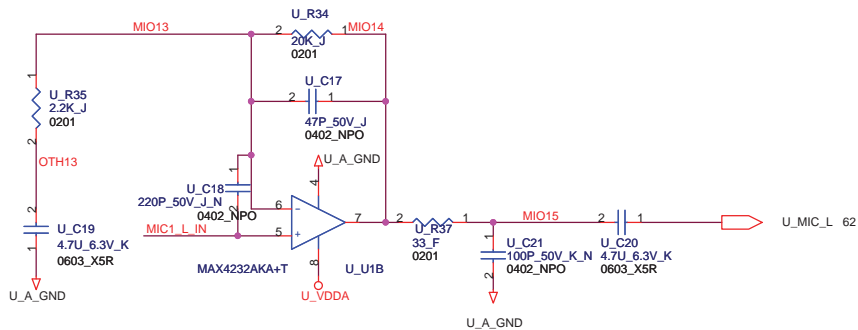
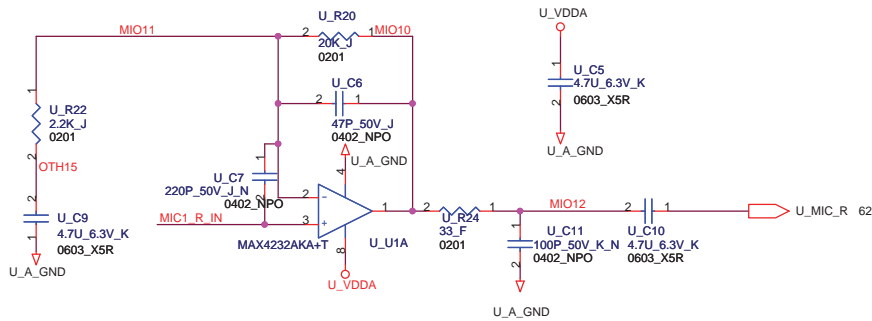
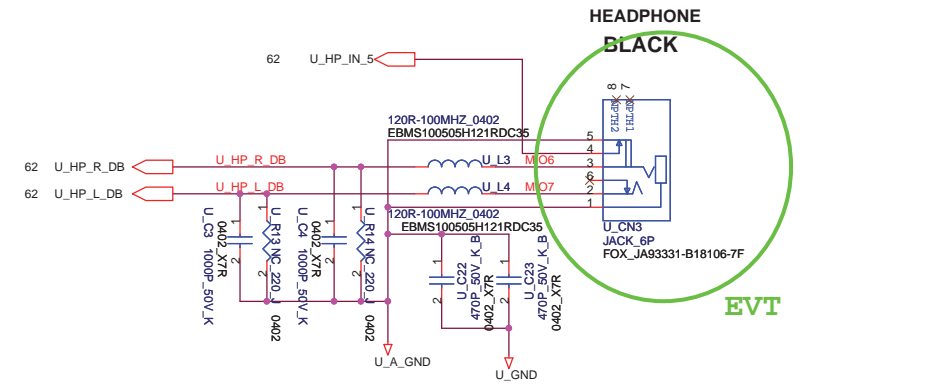


## M92-S2 XT Setting Table

PWRCNTL_0	PWRCNTL_1	GPU Voltage
0	0	0.95V
1	0	1.2V

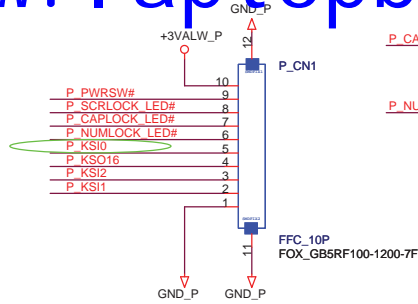
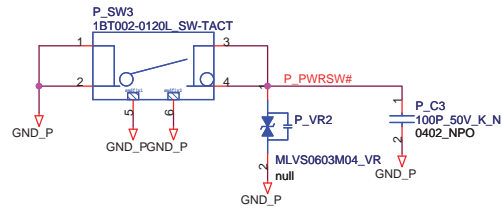
Power Control	GPIO
PWRCNTL_0	GPIO15
PWRCNTL_1	GPIO20







POWER BUTTON



P\_CAPLOCK\_LED#

P\_NUMLOCK\_LED#

EVT

+3VALW\_P

+3VALW\_P

+3VALW\_P

P\_Q1

P\_Q2

P\_Q3

DTA114YUA

DTA114YUA

DTA114YUA

P\_R1

P\_R2

P\_R3

120\_J

120\_J

120\_J

0402

0402

0402

P\_LED1

P\_LED2

P\_LED3

HT-110UYG

HT-110UYG

HT-110UYG

null

null

null

GND\_P

GND\_P

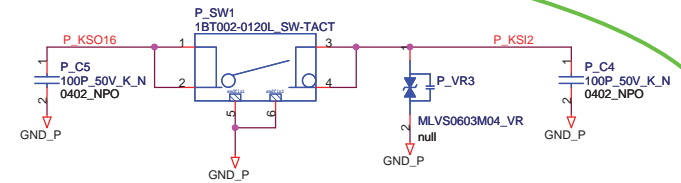
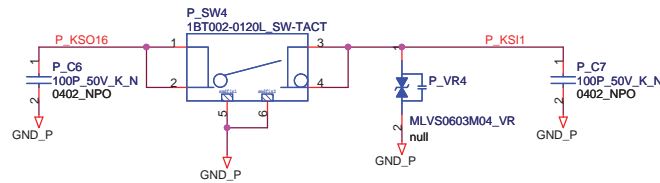
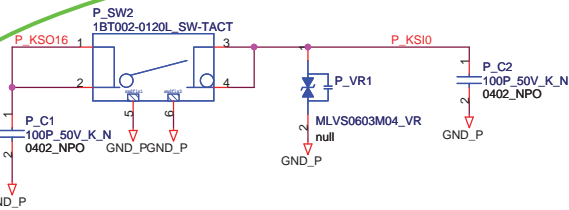
GND\_P

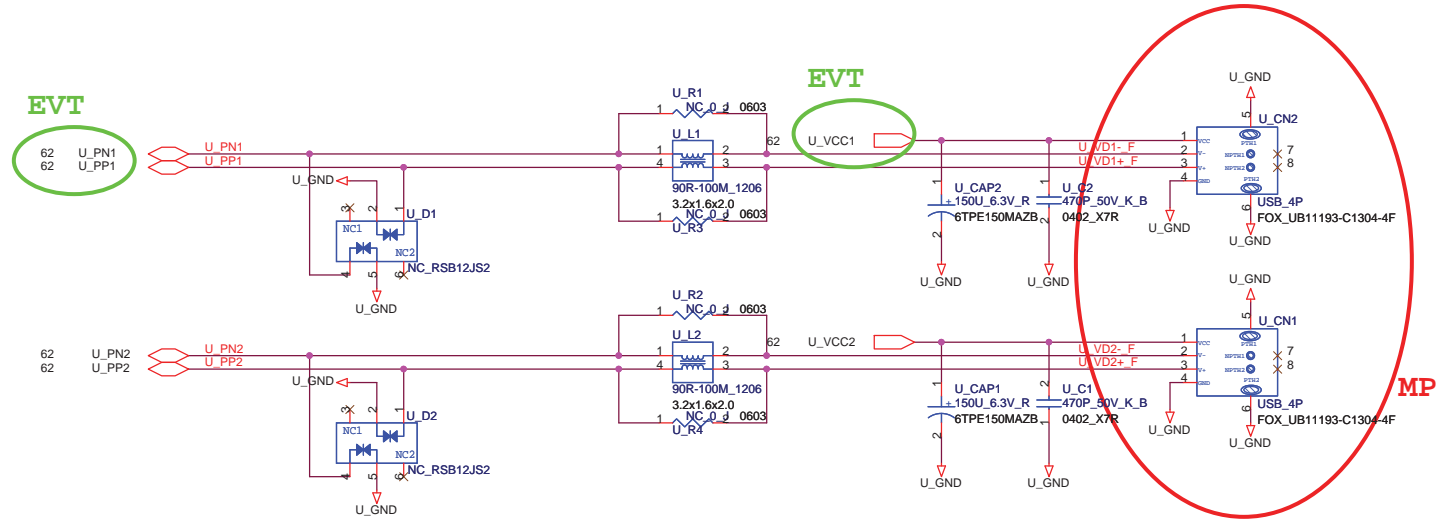
Instant ON

Mute

Display OFF

EVT





## M850 EVT

### (2008/08/29)

P.45 Change CN16 from WK21923-S6P-7F to WK21923-R6S-7F for ME request.  
P.32 Change CN25 from LN27131-A403-4F to LN21131-F404-9F for ME request.  
P.32 Change CN13 from LD2722F-SR6L to LD2722H-S49L for ME request.  
P.25 Change CN18 from HT1310F to GS12201-1011-9F for ME request.  
P.46 Change CN17 from HS6106E to HS6206E for ME request.  
P.37 Change CN22 from HS6108E to HS8208E for ME request.  
P.33 Change CN3 from GB21240-0002-7F to 196009-24021 for ME request.  
P.49 Change CN32 from QT510106-111H-7F to QT510106-311H-7F for ME request.  
P.35 Change SW4 from 1BS007-12120-002-7F to 1BS007-12110-002-7F for ME request.  
P.39 Change U\_CN4 from JA9333L-R5S7-7F to JA93331-R18106-7F for ME request.  
P.39 Change U\_CN3 from JA9333L-B5S7-7F to JA93331-B18106-7F for ME request.  
P.51 Change U\_CN1 and U\_CN2 from UB11193-C1314-4F to UB11193-C1308-4F for ME request.  
P.52 Add BOSS11 and BOSS12 for ME request.

### (2008/08/29)

P.45 Change CN11 form UV31413-GR56P-7F to UV31413-WZ03P-7F for ME request.  
P.24 Change CN2 from DZ11A91-MA2SY-4F to DZ11A91-SB281-4F for ME request.  
P.26 Change CN31 from QJ5119L-NT03-4F to QJ5119L-NK03-4F for ME request.  
P.48 Change CN9 from UB11193-C1314-4F to UB1112C-CA501-7F for ME request.

### (2008/09/01)

P.55 Change PR146 from 6.98K\_F to 8.2K\_F for OCP setting.  
P.55 Change PR147 from 6.19K\_F to 6.98K\_F for OCP setting.  
P.56 Change PR193 from 5.49K\_F to 8.66K\_F for OCP setting.  
P.56 Change PR113 from 8.66K\_F to 11.3K\_F for OCP setting.  
P.61 Change PR87 from 6.8K\_F to 8.2K\_F for OCP setting.  
P.61 Change PR99 from 8.2K\_F to 6.98K\_F for AT\_VDD voltage setting to 1.2V.

### (2008/09/02)

P.25 Change CN18 from GS12201-1011-9F to GS12301-1011A-9F for support Dual-LVDS.  
P.25 Add RP51,RP52,RP53 and RP54 for support Dual-LVDS.

### (2008/09/19)

P.35 Delete R611&R612 for MOR's requested  
P.35 Add D22 for MOR's requested  
P.27,42,48,51 Change external USB port from USBP3N/USBP3P to USBP1N/USBP1P for MOR's requested  
P.27,35,36 Change PCIE port from Express Card #2, WLAN #3 to WLAN #2, Express Card #3 for MOR's requested  
P.54 Change PCN1 from BP91077-B2013-7F to BP91077-B3013-7F for ME's requested  
P.37 Change U4 from 88E8055 to 88E8057 for MOR's requested  
P.49 Delete R668,674,672,671 for MOR's requested  
P.35 Change C538,C544,C536 to NC for MOR's requested

### (2008/09/22)

P.45 Change CN11 from UV31413-WZ03P-7F to UV31413-RU81P-7F for ME's requested

### (2008/09/24)

P.48 Change CN9 from UB1112C-CA501-7F to UB1112C-CA207-7F for ME's requested

### (2008/09/26)

P.65 [Power board DB button] Add P\_SW4,P\_C6,P\_C7,P\_VR4 for add mute button  
P.25 [Inverter CONN] Change CN19 from HS6106E to HS6108E for support LED backlight function  
P.25 [Panel ID Switch] Change SW1 from HDS404-E to FHDS-04-T-V-T/R for shortage issue

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### (2008/10/02)

P.16 [Express Card] Add R901 R902,R903,R904 for test GMT577 ExpressCard power switch

P.37 [GLAN]Change L5 from NS682403P to LFE9249-R for PUR's suggestion  
P.26 [HDMI] Change CN31 from QJ5119L-NK03-4F to QJ5119L-NT03-4F for ME's ID concern

P.52 [Thermal Module Nut] Change BOSS3,BOSS6,BOSS7 form F50M20-501130BS to EMI\_F50M20\_351130BS for ME's concern

P.21,22 [VRAM] Change U49,U50,U51,U52 from K4J10324QD-HC14 to K4J10324QD-HC12 for support 800MHz

P.50 [TouchPad] Change CN7 from GB5RF120-1200-7F to GB5RF060-1200-7F for change to 6-pin solution

P.60 [OVP protection]Delete PR35 CA\_69.8K\_F for 8L version unnecessary resister.

P.50 [MS/SD LED] Combine MS/SD LED for MOR's requested

P.65 [Caps/Num/Scroll lock LED] Change from HT-150YG to HT-110UYG for ME's ID concern

P.14 [DDR2] Swap RP13,RP10 pin assignment for layout convenient

P.15 [DDR2] Swap RP33,RP34,RP32,RP28,RP29 pin assignment for layout convenient

P.25 [LVDS] Change L98 from EBMS160808A121(400mA) to HCB1608KF-121T10(1A) for Panel max current is 500mA

### (2008/10/06)

P.27 [ICH9] Swap RP46,RP24,RP16 pin assignment for layout convenient  
P.50 [TP] Reserved 12pin TP solution in EVT

### (2008/10/07)

P.49 [BT]NC U46,R673,R670,C847 and add R907 for BT module has internal protection schematics for BT\_DATA pin.

P.35 [WLAN]Change Q49 from FET to transistor for a little cost down.

P.54 [DCIN&Charger]Delete PR34 for 8L version unnecessary resister.

P.52 [HOLE]Update HOLE for ME's requested.

P.11 [Cantiga] Delete R121,R151 for 8L version unnecessary resister.

### (2008/10/08)

P.11 [Cantiga]Delete C202,C225 for VCCD\_TVDAC can be connected to GND form Intel DG mention.

P.18 [VGA]REFCLK jumper R849.2pin should be connected to R848.1pin side not R848.2pin side. In case if you use REFCLK, It's voltage should be deviced also.

P.18 [VGA]Delete R840,R841,R843 and connect R2B,G2B,B2B to GND directly.

P.24 [CRT]Change DDC 3V pull-up R57,R58 from 2.2k to 3.9k to meet E-DDC spec.

P.25 [LVDS]Add R908 for AT\_LCDVCC\_EN need 10k pull-down as AMD Check list 8-1 mention.

P.26 [HDMI]Delete R649 for HDMI DDC need back drive protection so cannot use R649.

P.26 [HDMI]Delete D21 and R652 for if using diode, HDMI\_+5VRUN voltage cannot meet spec. And HDMI\_+5VRUN need back drive protection.

P.25 [LVDS]Change R393 from 10k to 100k to meet desing guide.

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(2008/10/09)

- P.21 [VRAM]Change R770,R771 from 82.5ohm to 120ohm for AMD suggestion
- P.33,51,64 [Button]Delte KSO15 and add KSI0 control signal for SW request
- P.49 [BT]Add R909(NC) for new BT module reserved
- P.11 [Cantiga>Delete R116 for useless
- P.33 [EC]Change R477,R437 to mount and R479,R436 to NC for H model ID change to "10"
- P.25 [LVDS]Change back R393 from 100k to 10k to meet AMD check list 8-8.

(2008/10/10)

- P.62 [Audio+USB CONN]Swap pin assignment for cable routing smooth.
- P.03 [Penryn]Add C1287(NC) for EMI verification.
- P.33 [EC]Add R910~R933 for EMI verification.
- P.51 [Power Board CONN]Add C1288~C1295(NC) for EMI verification.
- P.17 [VGA>Delete R817,R818 for GPIO9 is VGA\_DIS strap.

(2008/10/11)

- P.52 [HOLE]Update all holes for ME's requested

(2008/10/13)

- P.33 [EC>Delete R910~R933 for layout space not enough
- P.51 [Power Board CONN>Delete C1288~C1295 for layout space not enough.
- P.48 [USB]Change CN9 from UB1112C-CA207-7F to UB11123-CA301-7F for ME's concerned.
- P.54 [DCIN&Charger]Add PC194,PC195(NC) for EMI verification

(2008/10/14)

- P.52 [HOLE>Delete H16,H17,H18 for ME's requested.
- P.17 [VGA]Add R910,R911 for AMD confirm pin DVPPDATA\_22 and DVPPDATA\_23 function
- P.29 [ICH9>Delete R301 for needless
- P.48 [USB]Change CN9 from UB11123-CA301-7F to UB111M3-CA4S4-7F for ME's requested

(2008/10/15)

- P.16 [VGA]Change R849 from 0ohm to 100ohm and Net for R861.1&R860.1 changed to R\_AT\_XTALIN for MOR's comment
- P.42 [Audio]Add C1288(NC) for EMI verification

(2008/10/16)

- P.50 [T/P]Reverse CONN for ME's requested

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(2008/11/13)

- P.40 [Audio]Reverse JSPK1 pin definiens for ME's cable routing concern
- P.62 [Audio+USB DB]Reverse U\_CN5 pin definiens for ME's cable routing concern
- P.47 [Felica]Reverse CN6 pin definiens for ME's cable routing concern
- P.50 [T/P]Reverse CN7 pin definiens for ME's cable routing concern
- P.18 [VGA]Connect U53.T11&R11 to GND for ATI updated
- P.17 [VGA]Change R815,R814 to NC and R910 to mount for ATI DVPPDATA[23,22] failure issue

(2008/11/15)

- P.50 [T/P>Delete CN34,R530,R531 for cancel 12pin T/P solution

(2008/11/17)

- P.26 [HDMI]Change CN31 from QJ5119L-NT03-4F to QJ1119L-NT03-4F(Dip type) for CONN issue

(2008/11/19)

- P.16 [HDMI]Swap RP47 and RP49 for layout convenient
- P.52 [HOLE]Change U\_H3 size for ME's requested
- P.52 [HOLE>Delete P\_PAD5 and add P\_H3 for ME's requested
- P.52 [HOLE]Change P\_PAD4 size for ME's requested
- P.52 [HOLE>Delete P\_H1 and P\_H2 for ME's requested

(2008/11/24)

- P.55 [SYS Power (+3\_3V/+5V)] Add test point TP152, TP156
- P.56 [SYS Power(+1\_5V/+1\_05V))] Add test point TP161, TP176
- P.58 [CPU\_Vcore---ISL6266A] Add test point TP179
- P.59 [Others power plane] Add test point TP132, TP133, TP157, TP160, TP177
- P.60 [OVP protection] Add test point TP178

(2008/12/01)

- P.54 [DCIN&Charger] Add test point TP34, TP37, TP38, TP39
- P.54 [DCIN&Charger] Change PQ5 from AO4433 to SI4825DY-T1-E3 for EMI Issue
- P.58 [CPU\_Vcore---ISL6266A] Add PJ11 for power test

(2008/12/02)

- P.62 Change U\_CN5 pin33 and Pin34 to connect U\_GND
- P.06 [Clock Gen] Change test point type of TP153,TP154 for L6 requested
- P.63 [Audio]Change U\_R21,U\_R23,U\_R33,U\_R36,U\_R27,U\_R29,U\_R25,U\_R26,U\_R31 and U\_R32 from 0201 to 0402 for L6 requested
- P.33 [EC,LVDS] Add LED\_OFF#(GPIO04) signal to U6.1 and U23.1 for Display Off issue.
- P.25 [LVDS] Change SW1 from 8pin to 12pin for add Instant ON function

(2008/12/04)

- P.50 [T/P Buttom] Change SW2 and SW3 from 1BT001-1420L-001(160g) to 1BT001-1410L-001(100g) for ME's requested
- P.26 [HDMI] Swap RP47 and RP49 for layout convenience

(2008/12/05)

- P.52 [HOLE] Change U\_H3 from 1X-HOLE000-0935 to 1X-HOLE000-0959 for ME's requested
- P.52 [HOLE] Change U\_H1 from 1X-HOLE000-0905 to 1X-HOLE000-0958 for ME's requested
- P.52 [HOLE] Change P\_H3 from 1X-HOLE000-0936 to 1X-HOLE000-0960 for ME's requested

(2008/12/10)

- P.33,34,37,40,43,46,51,54 [Test Pad] Add TP500~TP549 for BFT test pad
- P.54 [DCIN] Delete PL6 for safety concern
- P.37 [GLAN]NC R24,R25,U3,C16 and mount R616 for using M8057 internal EEPROM.
- P.17 [VGA]Update VRAM strp for add Hynix VRAM
- P.33 [EC]Add TP550,TP551 for detect D17 reverse from L6's suggestion
- P.48 [USB]Add TP552~TP554 for detect USB power switch leakage from L6's suggestion

(2008/12/12)

- P.59 [Other power plane]Change PQ40,PQ41 from SI2316DS-T1-E3 to SI7326DN-T1-E3 for overload test issue.
- P.26 [HDMI]Change R647 and R646 to 3.9k ohm for meet E-DDC spec.
- P.49 [BT]Change CN32 from QT510106-311H-7F to QT510106-312H-7F for ME's requested.

## M850 DVT

(2008/12/15)

- P.54 [DCIN&Charger] Change PC194, PC195 from NC\_0.1U\_50V\_K 0603 to 220P\_50V\_K 0603 for EMI request
- P.61 [VGA Power] Change PR99 from 6.98K\_F 0402 to 11K\_F 0402 for AMD M92 Power-Play function
- P.61 [VGA Power] Change PR110 from NC\_49.9K\_F 0402 to 19.6K\_F 0402 for AMD M92 Power-Play function
- P.61 [VGA Power] Change PQ12 from NC to mount for AMD M92 Power-Play function
- P.61 [VGA Power] Change PC85 from NC to mount for AMD M92 Power-Play function
- P.61 [VGA Power] Change PR103 from 0\_J 0402 to 1K\_J 0402 for AMD M92 Power-Play function

(2008/12/18)

- P.54 [DCIN&Charger] Change PC28, PC29 from 4.7U\_25V\_K 0805 to 4.7U\_50V\_K 1206 for reducing DC\_IN inrush voltage.
- P.54 [DCIN&Charger] Parallel PR32 and PR165 for reducing DC\_IN inrush voltage.
- P.54 [DCIN&Charger] Change PL1 from SPD8D43PT100M to PCMB063T-100MS for 2nd source implement.
- P.50 [LED] Change R385 from 33ohm to 51ohm for LED brightness issue

(2008/12/19)

- P.60 [OVP Protection] Add PR160 100K\_J 0402 for MOR request.
- P.46 [CAM]Change U41 to MAX4789EUK and delete C815,C816,R626 for VEDS current limit requested.
- P.43 [FAN]Add F10 for prevent FAN sorot issue of MOR requested
- P.24 [CRT]Change R418 and R424 from 22ohm to 33ohm for improve VEDS AGRB issue.
- P.24 [CRT]Change CN2 from DZ11A91-SB281-4F to DZ11A91-SB2SN-4F for ME's requested.

(2008/12/20)

- P14,15 [DDR2]Add C1289,C1290,C1291,C1292,C1293,C1294 (NC) for EMI concern and MOR requested
- P.50 [TP]Change F7 from 0.5A to 0.35A for MOR's requested
- P.47 [Felica]Change F6 from 0.5A to 0.35A for MOR's requested
- P.47 [Felica]Add U56,C1295,C1296,R913 (NC) and R912 for reserve power switch for MOR's requested
- P.40 [Audio]Change R493,R494 from 1k to 47k for Pi-Pi noise issue

(2008/12/22)

- P.35 [Half Mini Card]Add R914 for RF team test VEDS,MP will delete it.
- P.54 [DCIN&Charger]Change TP546~TP549 from 40mil to 60mil for BFT side requested.
- P.23,33 [EC]Change signal name "LED\_OFF#" to "LCD\_OFF#" for MOR's suggestion.
- P.60 [OVP]Change PC41 from 0.01uF to 1nF for Power\_Abnormal\_Conditions issue.
- P.47 [Felica>Delete L60 for needless and SMT requested
- P.48 [USB>Delete L61 for needless and SMT requested

(2008/12/23)

- P.37 [Marvell GLAN>Delete TP538~TP545 for layout space concern
- P.45 [PCI]Change C496 from 27p to 22p for improve crytal accuracy
- P.29 [ICH9]Change footprint of D8 for SMT requested
- P.30 [ICH9]Change footprint of D14 for SMT requested

(2008/12/24)

- P.52 [HOLE]Change H5 from 1X-HOLE000-0925 to 1X-HOLE000-0913 for ME's requested

## M850 DVT

(2008/12/26)

- P.33 [EC] Add R915 for updating Instand On function.

(2009/02/09)

- P.50 [T/P]Update the connection of SW2 and SW3 to correct T/P function
- P.35 [WLAN]Update the connection of WLAN Switch to meet ME's requested

(2009/02/10)

- P.54 [DCIN&Charger] Change PR32, PR165 from 1\_J 1210 to 2\_J 1210 for reducing DC\_IN inrush voltage.
- P.54 [DCIN&Charger] Change PC194, PC195 from 220P\_50V\_K 0603\_NPO to 220P\_50V\_K 0402\_NPO for PUR convenient.
- P.54 [DCIN&Charger] Delete PR12 for unnecessary.
- P.55 [SYS Power(+3\_3V/+5V)] Delete PJ1, PJ2 for unnecessary.
- P.56 [SYS Power(+1\_5V/+1\_05V)] Delete PJ3, PJ4 for unnecessary.
- P.57 [DDR2 Power(+1\_8V/+0\_9V)] Delete PJ5, PJ8 for unnecessary.
- P.58 [CPU\_Vcore---ISL6266A] Delete PR20, PR38, PR46, PR65, PJ11 for unnecessary.
- P.58 [CPU\_Vcore---ISL6266A] Change PC145 from MATSUSHITA, EEEFK1E101XP to CHEMI-CON, EMVE250ADA101MF80G for MOR request.
- P.59 [Others power plane] Delete PR72, PR77, PR89 for unnecessary.
- P.60 [OVP protection] Delete PR97, PR105, PR108 for unnecessary.
- P.61 [VGA Power(ATI VDD)] Delete PJ7, PJ9, PJ10 for unnecessary.

(2009/02/13)

- P.29 [ICH9]Change R573 from mount to NC because BT\_GPIO is not used for M850.
- P.25 [LVDS]Change signal name "INST\_ON\_SW" to "INST\_ON\_SW#" because it's low active.
- P.33 [EC]Change signal name "INST\_ON\_SW" to "INST\_ON\_SW#" because it's low active.

(2009/02/19)

- P.50 [LED]Change R600 from 120ohm to 150ohm to satisfy brightness requested.
- P.47 [Felica]Change F6 from 0.35A to 0.25A for felica module heated concern.
- P.33 [EC]Add R916 for SPI ROM datasheet updated.
- P.52 [HOLE]Change H4 from 1X-HOLE000-0926 to 1X-HOLE000-1052 for ME's requested.
- P.52 [HOLE]Change H12 from 1X-HOLE000-0915 to 1X-HOLE000-1051 for ME's requested.
- P.65 [USB]Change U\_CN1 and U\_CN2 form UB11193-C1308-4F to UB111S3-C1GS6-4H for ME's requested.

(2009/02/20)

- P.59 [Others power plane] Change PQ16 from IRF8714PBF to IRF8736PBF for +1\_8VRUN voltage drop issue.
- P.60 [OVP protection] Change PR55 from 14.7K\_F 0402 to 18.2K\_F 0402 for BT+ OVP setting.
- P.60 [OVP protection] Change PR143 from 20K\_F 0402 to 26.1K\_F 0402 for +5VALW OVP setting.
- P.60 [OVP protection] Change PR144 from 47K\_F 0402 to 80.6K\_F 0402 for +3VALW OVP setting.
- P.24 [CRT] Change CN2 from DZ11A91-SB2SN-4F to DZ11A91-SA2SN-4H for ME's requested.
- P.47 [Felica]Change F6 from 0.25A to 0.125A for felica module heated concern.

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(2009/02/23)

- P.50 [TP]Change SW2 and SW3 from 19-1BT0011-1003 to 19-SKHM0KE-1000 for ME's requested.
- P.54 [DCIN]Move PC13,PC14,PC15 to the another side of PL8 for improving EMC.
- P.52 [HOLE]Change BOSS3,BOSS6 from connect to GND to NC for improving EMC.
- P.49 [BT]Change CN32 from QT510106-312H-7F to QT510106-312H-7H for ME's requested.
- P.45 [ILINK]Change CN11 from UV31413-RU81P-7F to UV31413-RU82P-7H for ME's requested.
- P.20 [VGA]Add C1297~C1308 for MOR's requested to check PEG signal.

(2009/02/24)

- P.48 [USB]Change CN9 from UB111M3-CA4S4-7F to UB111M3-CAGS4-7H for MOR's requested.

(2009/02/25)

- P.52 [HOLE]Change P\_H3 from 1X-HOLE000-0960 to 1X-HOLE000-1054 for EMC's requested.
- P.33 [EC]Change R915,R613,R475,R629,R435,R431(10K) from 0201 to 0402 for SMT's requested.
- P.33 [EC]Change R173,R197,R203,R75,R124,R442,R440,R447,R432(100K) from 0201 to 0402 for SMT's requested.
- P.33 [EC]Change R476(4.7K) from 0201 to 0402 for SMT's requested.
- P.34 [Flash ROM]Change R233(0) from 0201 to 0402 for SMT's requested.

(2009/02/25b)

- P.47 [Modem]Add TP600~TP606 for BFT test requested.

(2009/02/26)

- P.48 [USB]Change C810 from Y5V to X5R for MOR VEDS requested.
- P.40 [Audio>Delete Q27,R450,R614,Q8,R98,R615 for unnecessary to improve BFT test point.

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(2009/04/01)

- P.33 [EC]Signal symbol "OVT\_GFX#" change to two-way type for avoiding confusion from SW's suggestion.

(2009/04/08)

- P.24 [CRT]Change CN2 from FOX\_DZ11A91-SA2SN-4H to FOX\_DZ11A91-SB2SN-4F (same as DVT used) for CONN discoloration issue.
- P.48 [USB2.0]Change CN9 from FOX\_UB111M3-CAGS4-7H to FOX\_UB111M3-CA4S4-7F (same as DVT used) for CONN discoloration issue.
- P.65 [USB DB]Change U\_CN1 and U\_CN2 from FOX\_UB111S3-C1GS6-4H to FOX\_UB11193-C1304-4F for CONN discoloration issue.

(2009/04/09)

- P.45 [ILINK]Change CN11 from UV31413-RU82P-7H to UV31413-WU82P-7F for CONN discoloration issue.

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(2009/07/08)

- P.35 [Half Mini Card]Add TP180,TP184 for LED test in L6.
- P.50 [LED&T/P&LID]Add TP181,TP182,TP183 TP185,TP186,TP187,TP188 for LED test in L6.

(2009/07/09)

- P.06 [Half Mini Card]Change R542,R276,R283,R288,R553,R277,R278,R536,R537,R538, R534 from 0201 to 0402 for SMT's request.
- P.08 [Cantiga (DMI) ]Change R286,R231,R193,R195 from 0201 to 0402 for SMT's request.
- P.12 [Cantiga (VCC CORE)]Change R208 from 0201 to 0402 for SMT's request.
- P.17 [VGA (Strap)]Change R809,R825,R826 from 0201 to 0402 for SMT's request.
- P.18 [VGA (I/O)]Change R830,R831,R828 from 0201 to 0402 for SMT's request.
- P.21 [VRAM (GDDR3)]Change R787,R763,R769,R765,R773,R771,RR772,R767,R770 from 0201 to 0402 for SMT's request.
- P.22 [VRAM (GDDR3)]Change R801,R786,R800 from 0201 to 0402 for SMT's request.
- P.28 [ICH9-M (LPC,IDE,SATA)]Change R101 from 0201 to 0402 for SMT's request.
- P.29 [ICH9-M (GPIO)]Change R541,R540,R567, R322,R575,R300,R297,R303 from 0201 to 0402 for SMT's request.
- P.33 [EC+KBC (WPCE775L)]Change R444,R477 from 0201 to 0402 for SMT's request.
- P.38 [Audio (CODEC & POWER)]Change R230,R217 from 0201 to 0402 for SMT's request.
- P.39 [Audio (HP)]Change R893,R894 from 0201 to 0402 for SMT's request.
- P.41 [Audio (MUTE)]Change R241,R499,R227,R225,R486,R498,R500,R478 from 0201 to 0402 for SMT's request.

(2009/07/13)

- P.39 [Audio (HP)]Change R893,R894 to 0201 again for avoiding side effect.