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P. Leader	Check by	Design by

Project Code & Schematics Subject: MS21 MP Main Board

(TYPE 2)

PCB P/N: 1P-0068100-8011 (FUBAI)
1P-0068500-8011 (Hannstar)FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

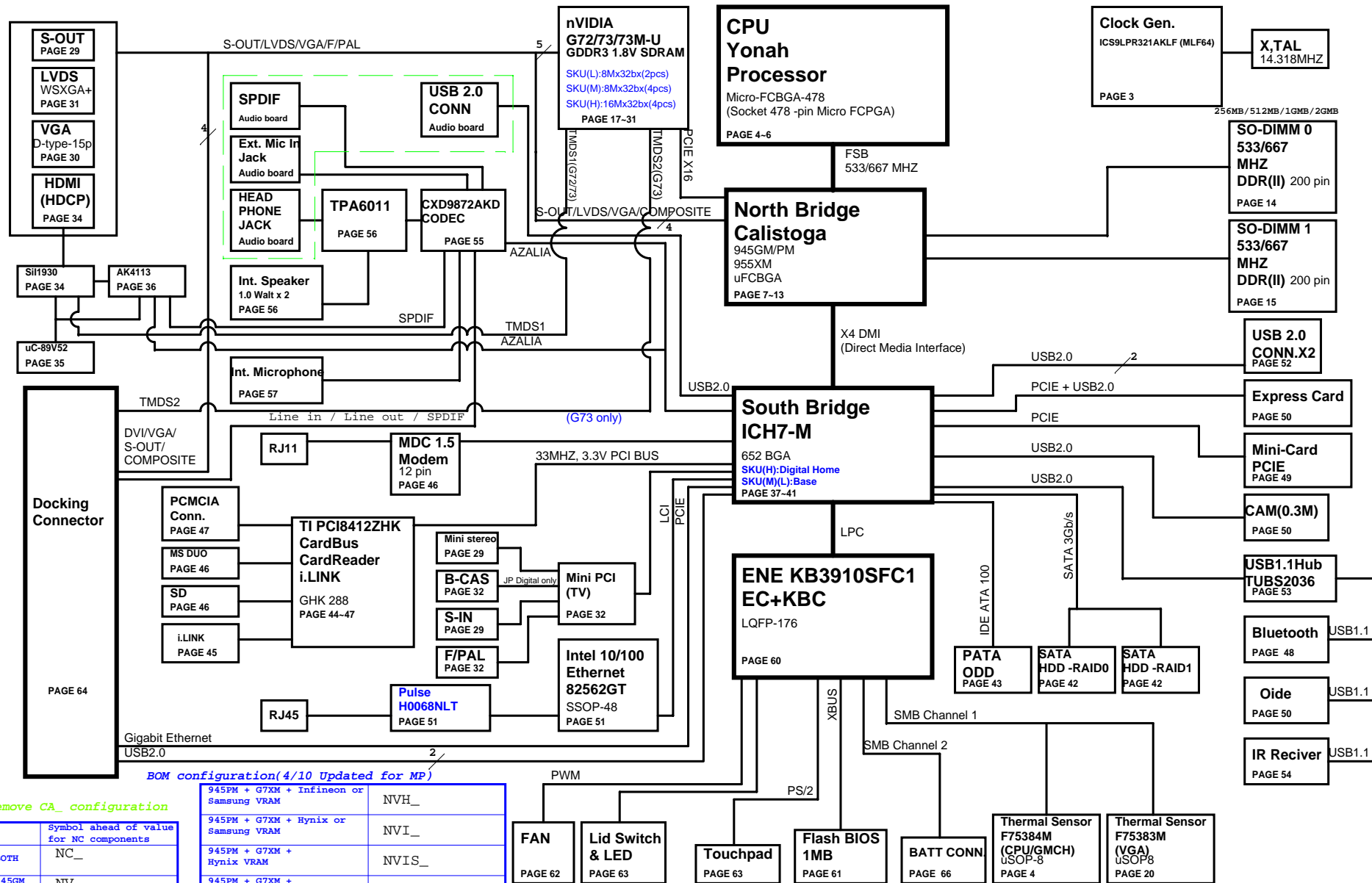
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Size A3	Document Number (MS21-1-01) MainBoard (MBX-164) TYPE2	Rev 1.1
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MS21(CALISTOGA FM+Gfx Block Diagram)

Red texts:
New modified

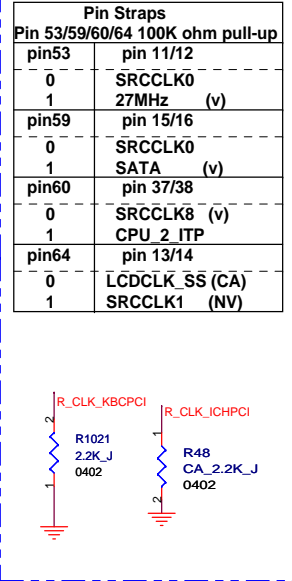


BOM configuration(4/10 Updated for MP)

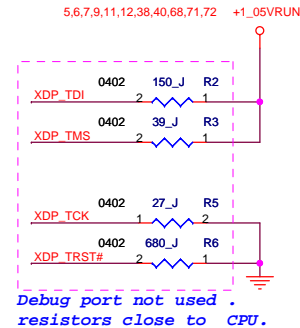
Remove CA configuration

Symbol ahead of value for NC components	
BOTH	NC_
945GM	NV_
945PM + G72M	NV73_
945PM + G73M	NV72_
945PM + G72M or G73M-U	NV73Only_

945PM + G7XM + Infineon or Samsung VRAM	NVH_
945PM + G7XM + Hynix or Samsung VRAM	NVI_
945PM + G7XM + Hynix VRAM	NVIS_
945PM + G7XM + Infineon VRAM	NVHS_
945PM + G72M or G73M	NV16M_, NV73U_
945PM + G73M-U	NV8M_, NV7273_
*JP Digital TV Tuner SKU & No Tuner SKU not stick	JDTVNC_



FSLB	FSLA	CPU	SRC[7:0]	PCI
0	0	100	100	33
0	1	133	100	33
1	0	200	100	33
1	1	166	100	33

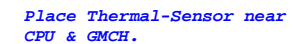


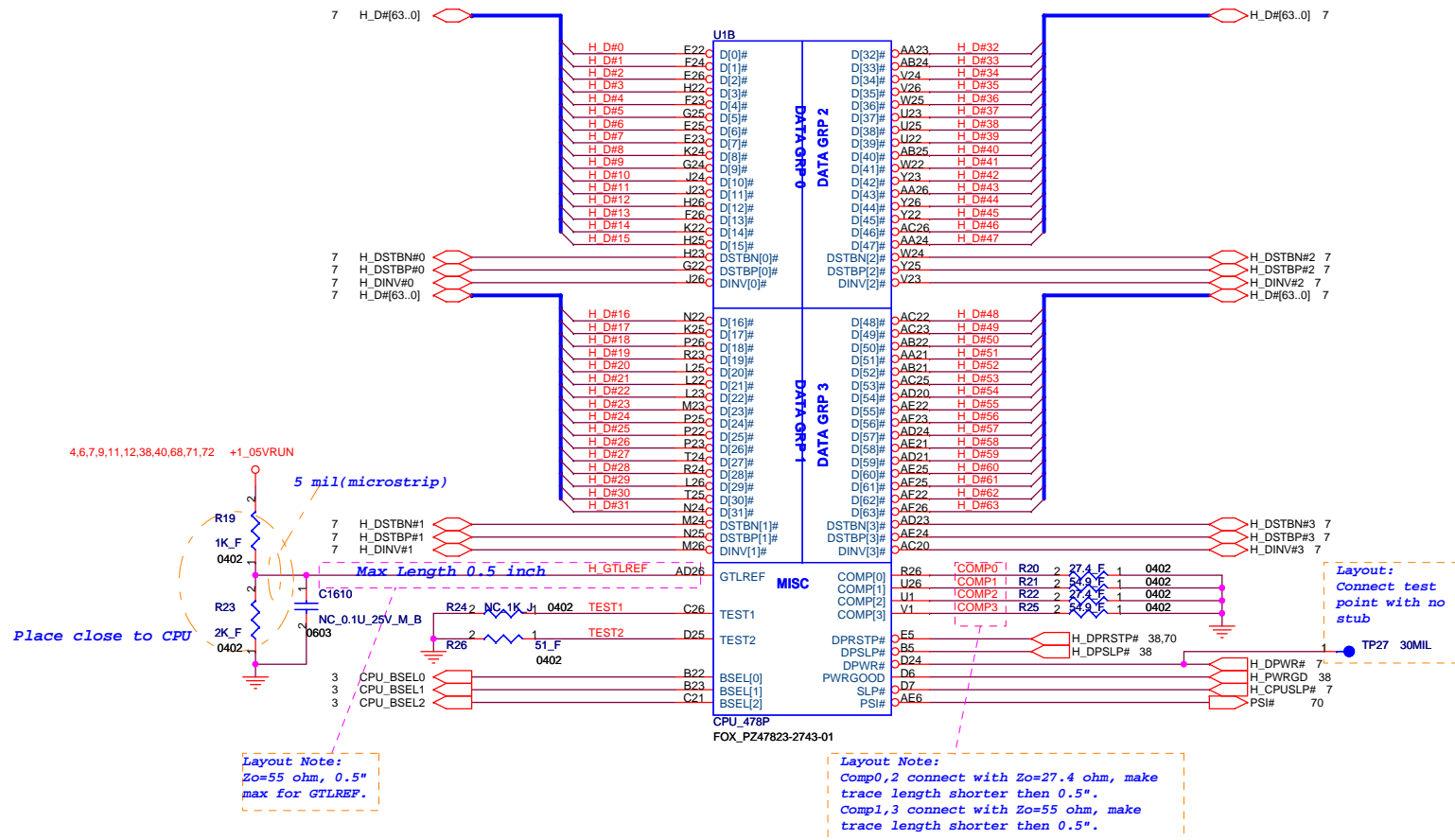
A#[32-39], APM#[0-1]:
Leave escape routing
on for future
functionality

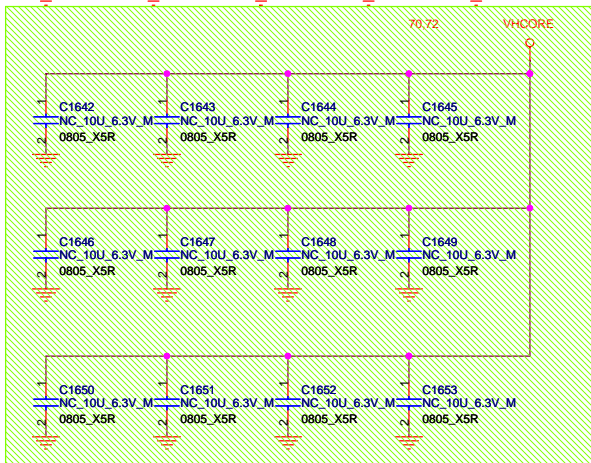
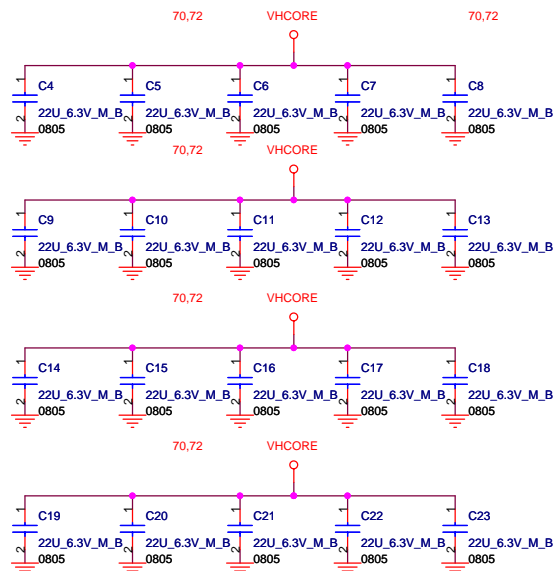
```

ICH7M's GPIO12:  VIL---> -0.5V ~ 0.8V
                  VIH--->  2.0V ~ 3.3+0.5V
YONAH's PROCHOT#: VIL---> -0.1V ~ 0.3*VCCP
                  VIH--->  0.7*VCCP ~ VCCP+0.1

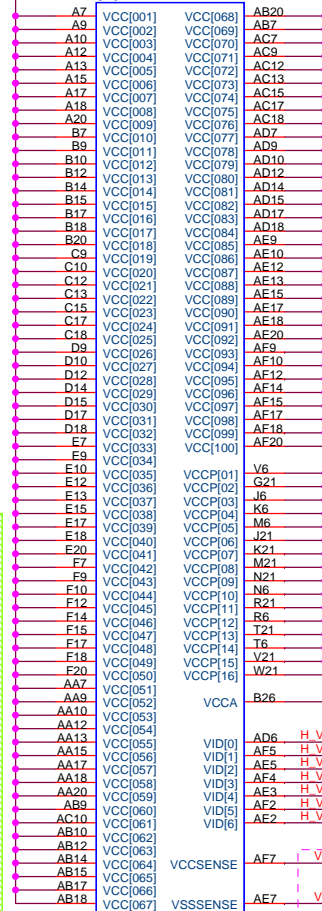
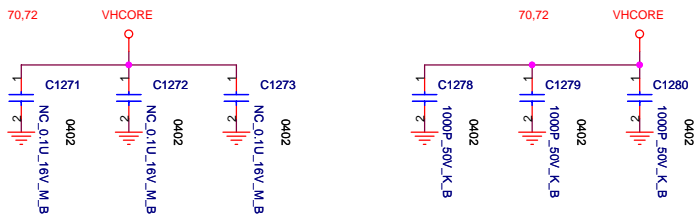
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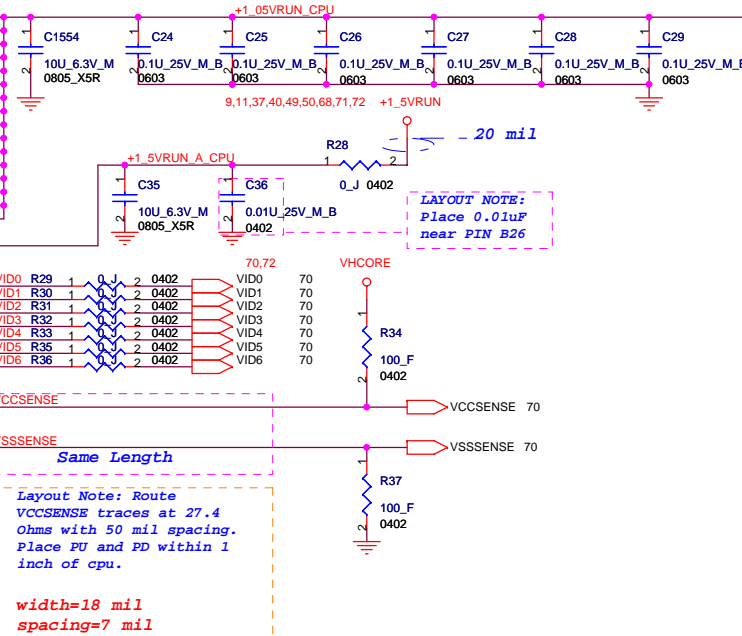




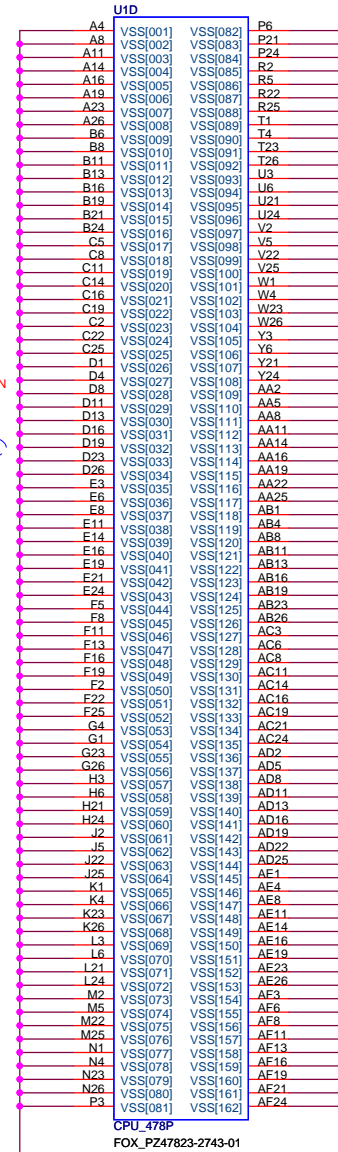
Backup 10uF capacitors for 22uF shortage.

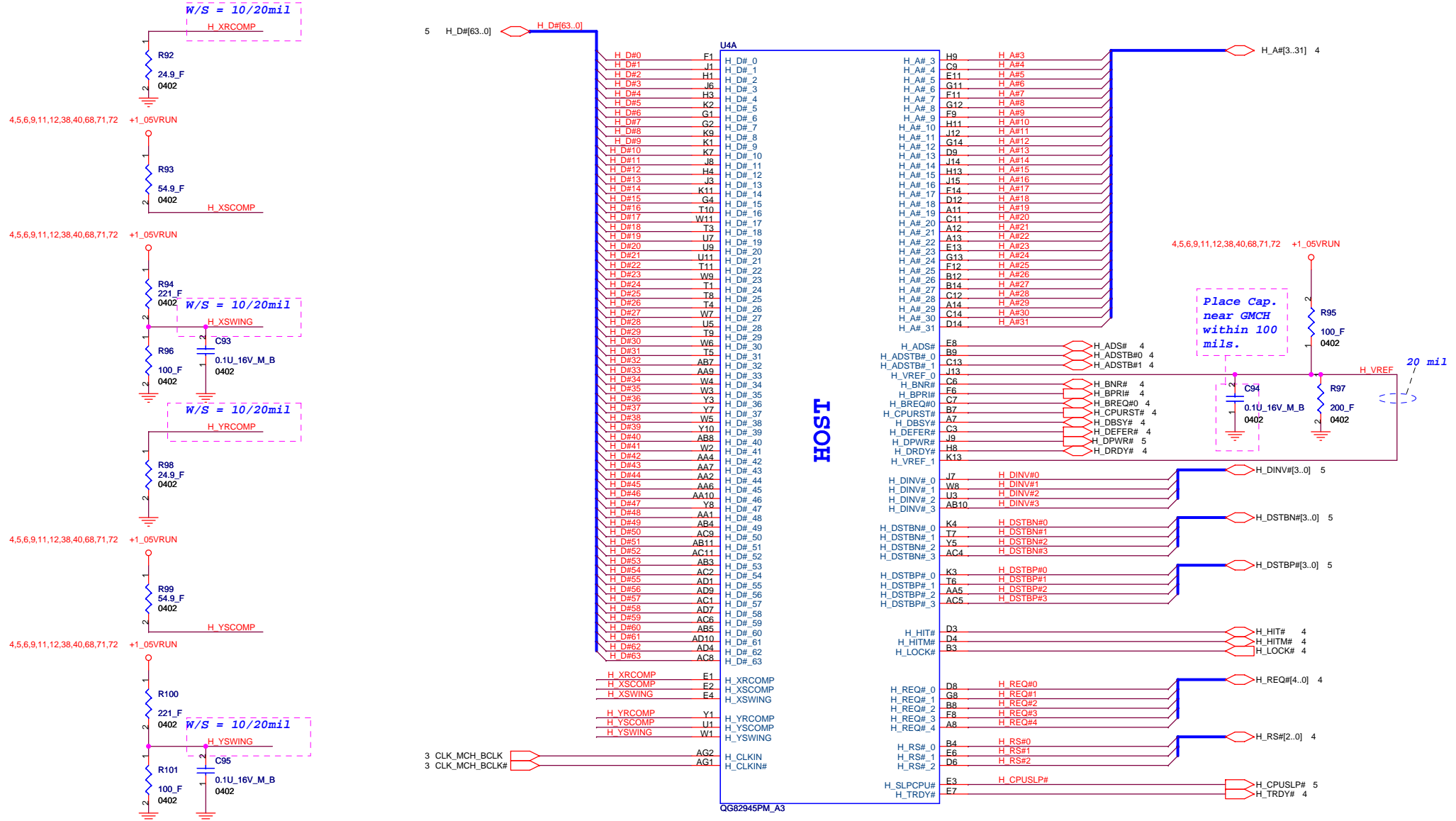


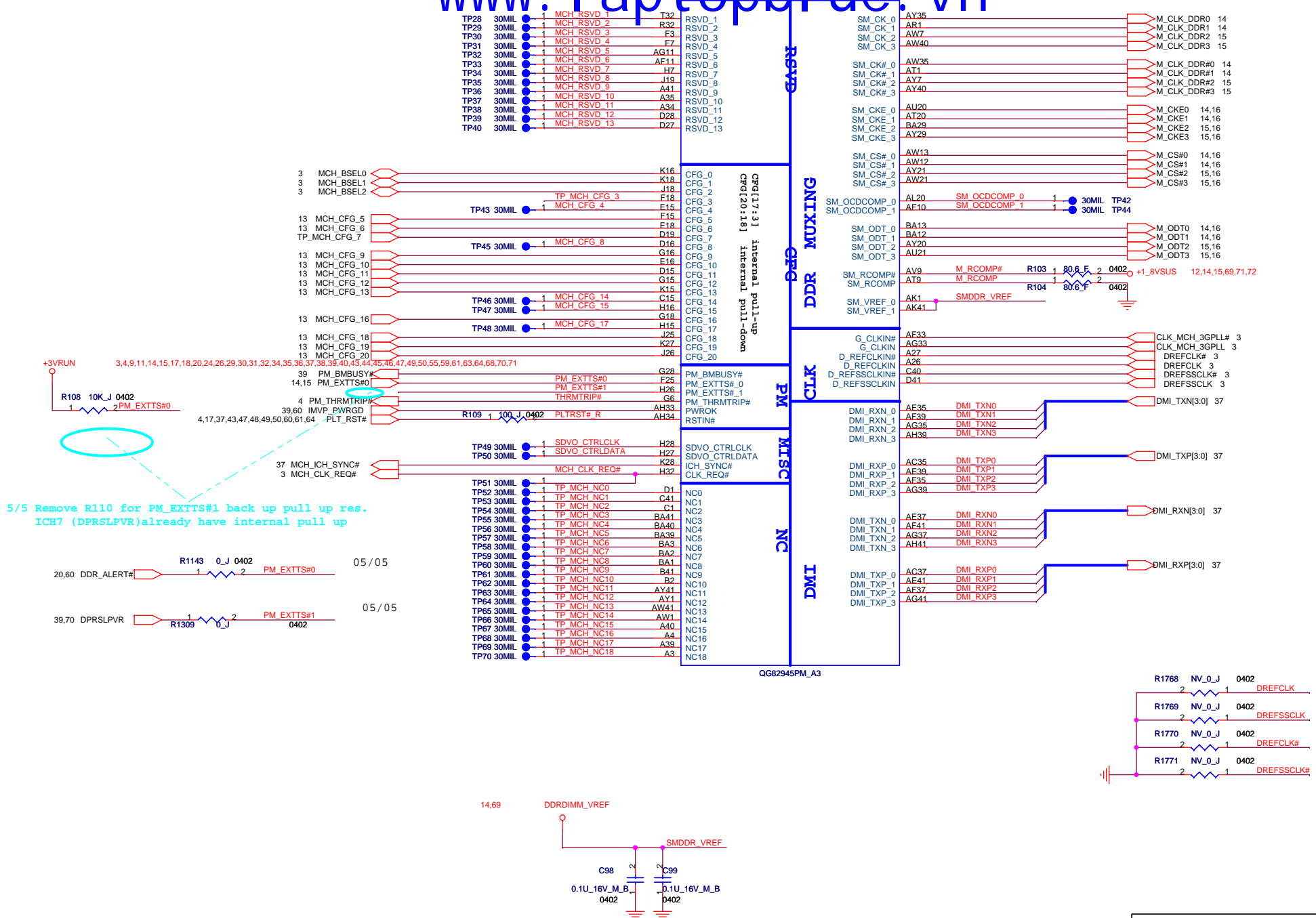
CPU_VCCA----->120mA
CPU_VCCP----->2.5A
CPU_VCC----->44A

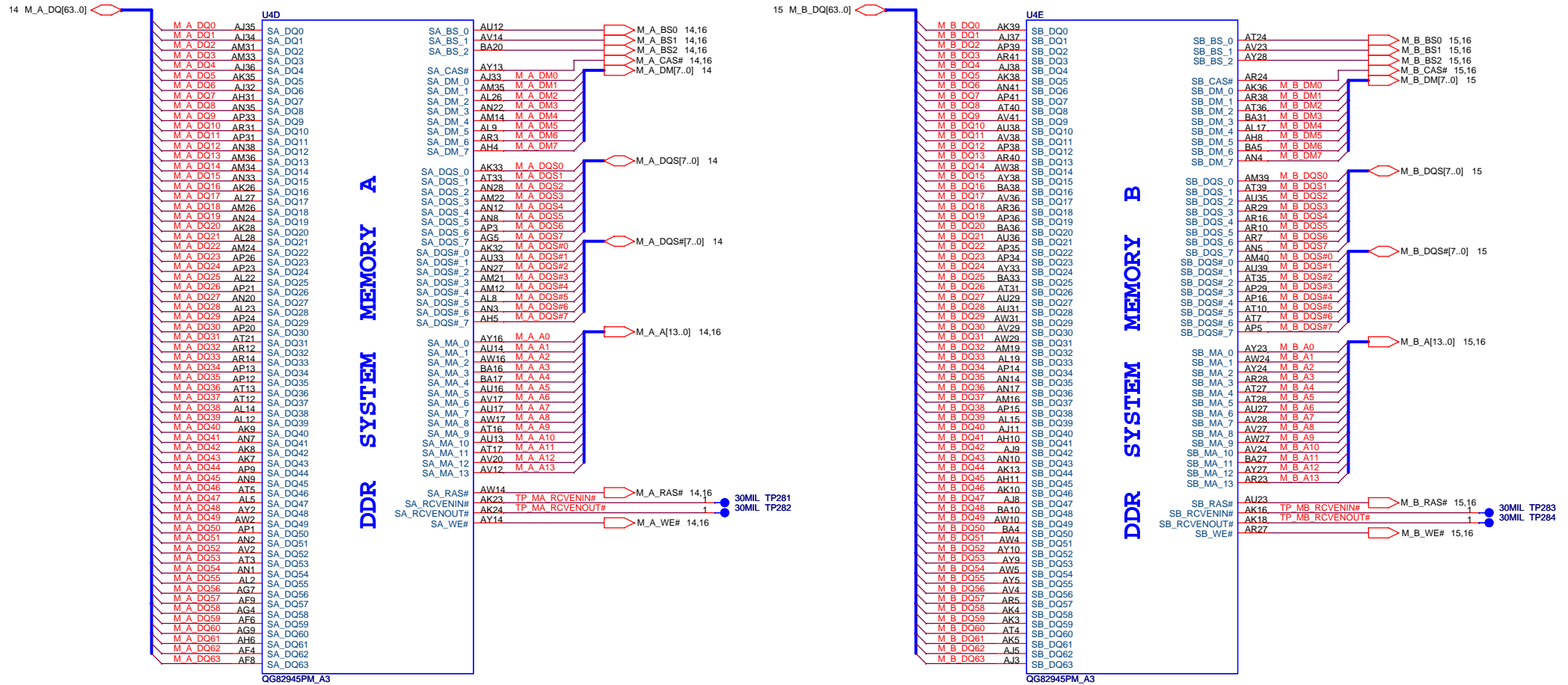


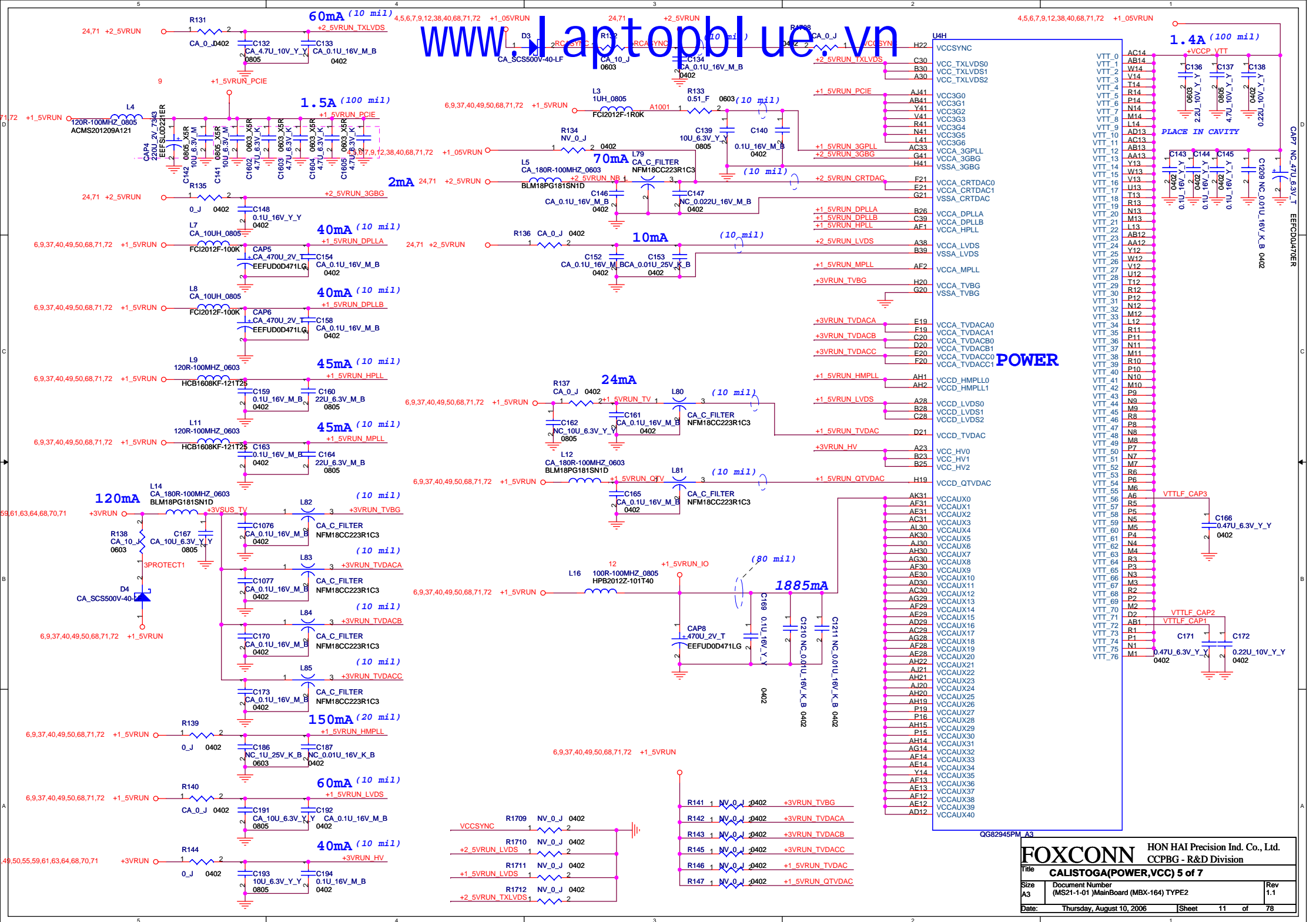
Layout Note: Route VCCSENSE traces at 27.4 Ohms with 50 mil spacing. Place PU and PD within 1 inch of cpu.
width=18 mil
spacing=7 mil

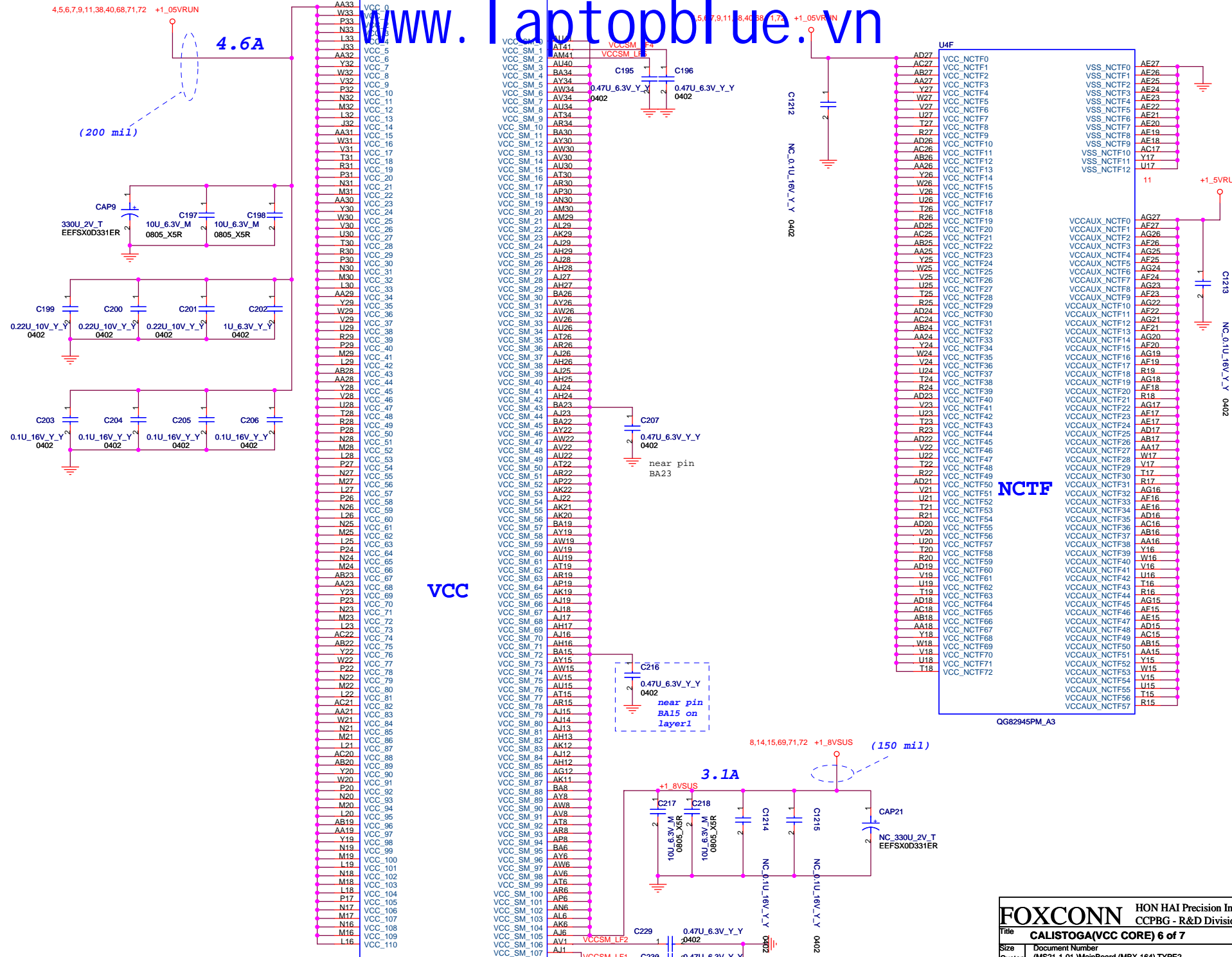












8 MCH_CFG_5 ◀ 1 ● 30MIL TP554

MCH_CFG_5	Low = DMIX2 High = DMIX4
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8 MCH_CFG_6 ◀ 1 ● 30MIL TP556

MCH_CFG_6	Low = Moby Dick High = Calistoga DDR2 select (default high)
-----------	-------------------------------------------------------------------

8 TP_MCH_CFG_7 ◀ TP_MCH_CFG_7

MCH_CFG_7 (CPU Strap)	Low = RSVD High = Mobile Yonah processor
--------------------------	------------------------------------------------

8 MCH_CFG_9 ◀ 1 ● 30MIL TP559

MCH_CFG_9 (PCIe Graphics Lane)	Low = Reverse Lane High = Normal operation For layout convenience
-----------------------------------	-------------------------------------------------------------------------

8 MCH_CFG_10 ◀ 1 ● 30MIL TP560

MCH_CFG_10 (HOST PLL VCC SELECT)	Low = RESERVED High = MOBILITY
-------------------------------------	-----------------------------------

8 MCH_CFG_11 ◀ 1 ● 30MIL TP562

MCH_CFG_11 (PSB 4x CLK ENABLE)	Low = Calistoga High = Reserved
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8 MCH_CFG_12 ◀ 1 ● 30MIL TP562

8 MCH_CFG_13 ◀ 1 ● 30MIL TP563

MCH_CFG_13:12 (XOR/ALLZ)	00=Partial Clock Gating Disable 01=XOR Mode Enable 10=All-Z Mode Enable 11=Normal Operation(Default)
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8 MCH_CFG_16 ◀ 1 ● 30MIL TP564

MCH_CFG_16 (FSB Dynamic ODT)	Low = Dynamic ODT Disabled High = Dynamic ODT Enable
---------------------------------	---------------------------------------------------------

MCH_CFG_18 (VCC_CORE Select)	Low = 1.05V(default) High = 1.5V
---------------------------------	-------------------------------------

8 MCH_CFG_18 ◀ 1 ● 30MIL TP555

MCH_CFG_19 (DMI LANE REVERSAL)	Low = Normal(default) High = LANES REVERSED
-----------------------------------	------------------------------------------------

8 MCH_CFG_19 ◀ 1 ● 30MIL TP558

MCH_CFG_20 (PCIe Backward Interoperability mode)	Low = Only SDVO or PCIE x1 is operational (defaults)) High = SDVO and PCIE x1 are operating simultaneously via the PEG port
-----------------------------------------------------	--------------------------------------------------------------------------------------------------------------------------------

8 MCH_CFG_20 ◀ 1 ● 30MIL TP561

Layout Noe:
Location of all MCH_CFG strap resistors needs to be close to trace to minimize stub

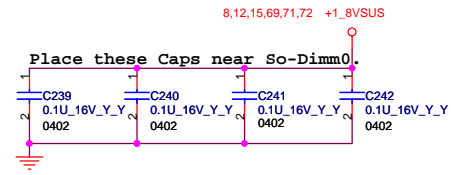
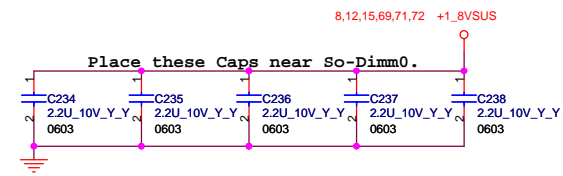
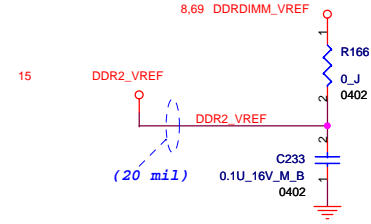
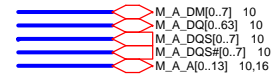
AC23	VSS_7	AK34	VSS_97
AA41	VSS_1	AG34	VSS_98
W41	VSS_2	AF34	VSS_99
T41	VSS_3	AE34	VSS_100
P41	VSS_4	AC34	VSS_101
M41	VSS_5	C34	VSS_102
J41	VSS_6	AW33	VSS_103
F41	VSS_7	AV33	VSS_104
AV40	VSS_8	AR33	VSS_105
AP40	VSS_9	C23	VSS_106
AK40	VSS_10	AE33	VSS_107
AN40	VSS_11	AB33	VSS_108
Y40	VSS_12	Y33	VSS_109
AG40	VSS_13	V33	VSS_110
AE40	VSS_14	T33	VSS_111
B40	VSS_15	R33	VSS_112
AV39	VSS_16	M33	VSS_113
AR39	VSS_17	H33	VSS_114
AN39	VSS_18	G33	VSS_115
AC39	VSS_19	F33	VSS_116
AA39	VSS_20	D33	VSS_117
Y39	VSS_21	B33	VSS_118
W39	VSS_22	AH32	VSS_119
V39	VSS_23	AG32	VSS_120
T39	VSS_24	AF32	VSS_121
R39	VSS_25	Y21	VSS_122
P39	VSS_26	AE32	VSS_123
N39	VSS_27	P21	VSS_124
M39	VSS_28	K21	VSS_125
L39	VSS_29	J21	VSS_126
J39	VSS_30	H21	VSS_127
H39	VSS_31	C21	VSS_128
G39	VSS_32	AW20	VSS_129
F39	VSS_33	AR20	VSS_130
D39	VSS_34	AN20	VSS_131
C39	VSS_35	AJ20	VSS_132
AT38	VSS_36	AK20	VSS_133
AM38	VSS_37	Y11	VSS_134
AH38	VSS_38	AT29	VSS_135
AG38	VSS_39	AN29	VSS_136
AF38	VSS_40	AB29	VSS_137
AE38	VSS_41	T29	VSS_138
AC38	VSS_42	N29	VSS_139
C38	VSS_43	K29	VSS_140
AK37	VSS_44	G29	VSS_141
AH37	VSS_45	D18	VSS_142
AB37	VSS_46	E29	VSS_143
AA37	VSS_47	C29	VSS_144
Y37	VSS_48	B29	VSS_145
W37	VSS_49	A29	VSS_146
V37	VSS_50	BA28	VSS_147
T37	VSS_51	AM17	VSS_148
R37	VSS_52	AL17	VSS_149
P37	VSS_53	AP28	VSS_150
N37	VSS_54	AM28	VSS_151
M37	VSS_55	AD28	VSS_152
L37	VSS_56	AC28	VSS_153
J37	VSS_57	F16	VSS_154
H37	VSS_58	J28	VSS_155
G37	VSS_59	C16	VSS_156
F37	VSS_60	E28	VSS_157
D37	VSS_61	AP27	VSS_158
C37	VSS_62	AM27	VSS_159
AT36	VSS_63	AK27	VSS_160
AM36	VSS_64	L15	VSS_161
AH36	VSS_65	F27	VSS_162
AG36	VSS_66	B15	VSS_163
AF36	VSS_67	C27	VSS_164
AE36	VSS_68	M26	VSS_165
AC36	VSS_69	K26	VSS_166
C36	VSS_70	AA14	VSS_167
AK35	VSS_71	D26	VSS_168
AH35	VSS_72	AK25	VSS_169
AG35	VSS_73	H14	VSS_170
AF35	VSS_74	P25	VSS_171
AE35	VSS_75	K25	VSS_172
AC35	VSS_76	H25	VSS_173
C35	VSS_77	E25	VSS_174
AT34	VSS_78	AN13	VSS_175
AM34	VSS_79	A25	VSS_176
AH34	VSS_80	BA24	VSS_177
AG34	VSS_81	AG13	VSS_178
AF34	VSS_82	P13	VSS_179
AE34	VSS_83	AL24	
AC34	VSS_84	AW23	
C34	VSS_85		
AK33	VSS_86		
AH33	VSS_87		
AG33	VSS_88		
AF33	VSS_89		
AE33	VSS_90		
AC33	VSS_91		
C33	VSS_92		
AK32	VSS_93		
AH32	VSS_94		
AG32	VSS_95		
AF32	VSS_96		

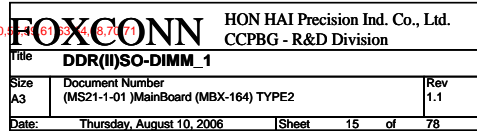
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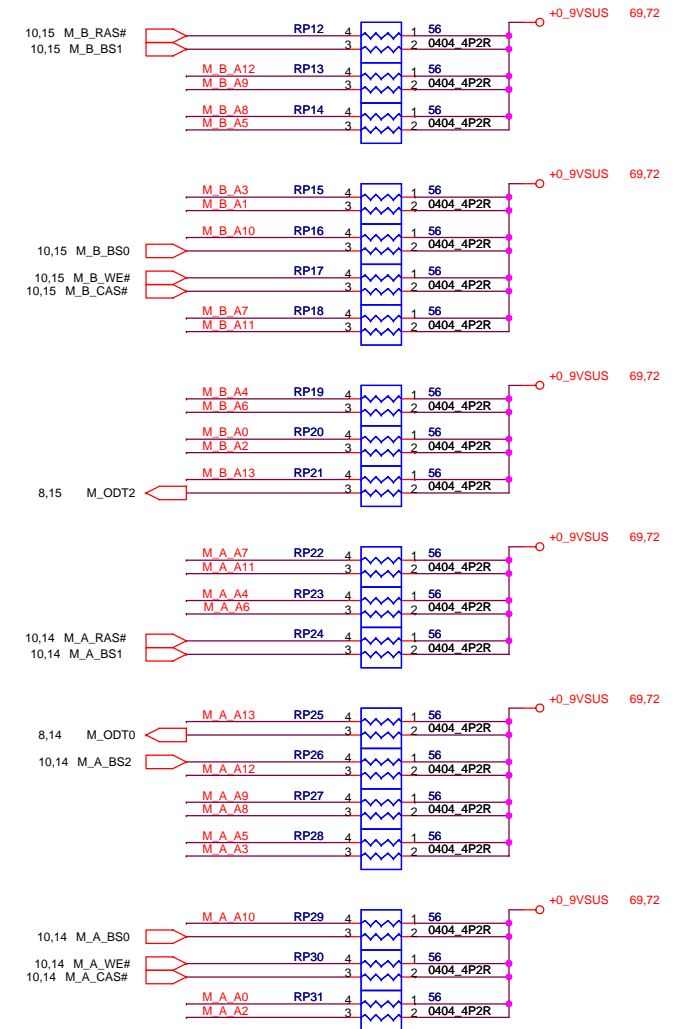
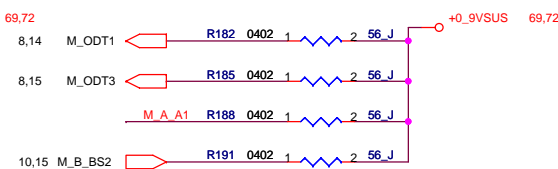
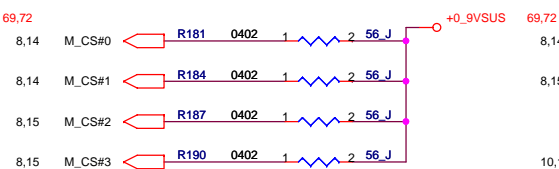
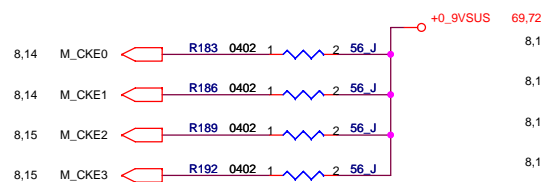
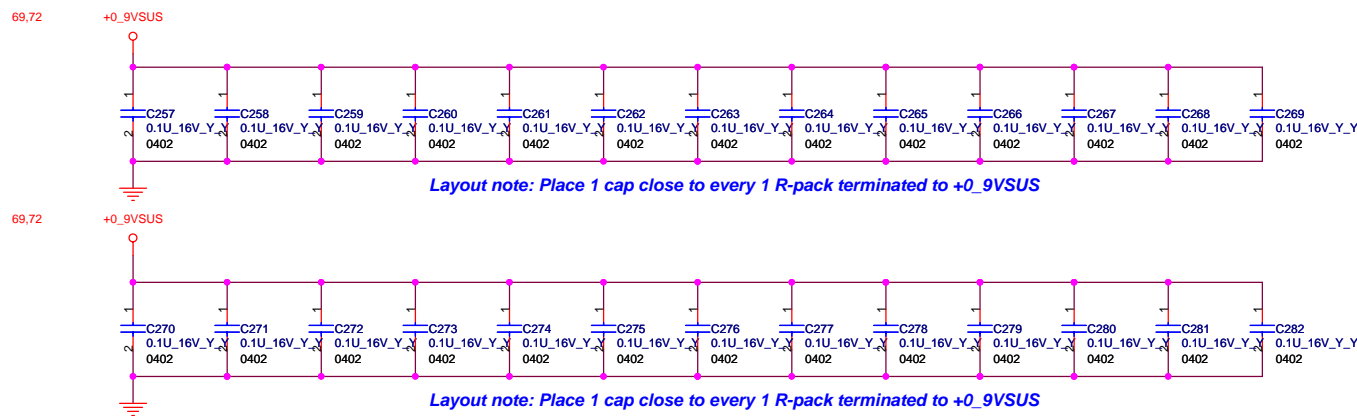
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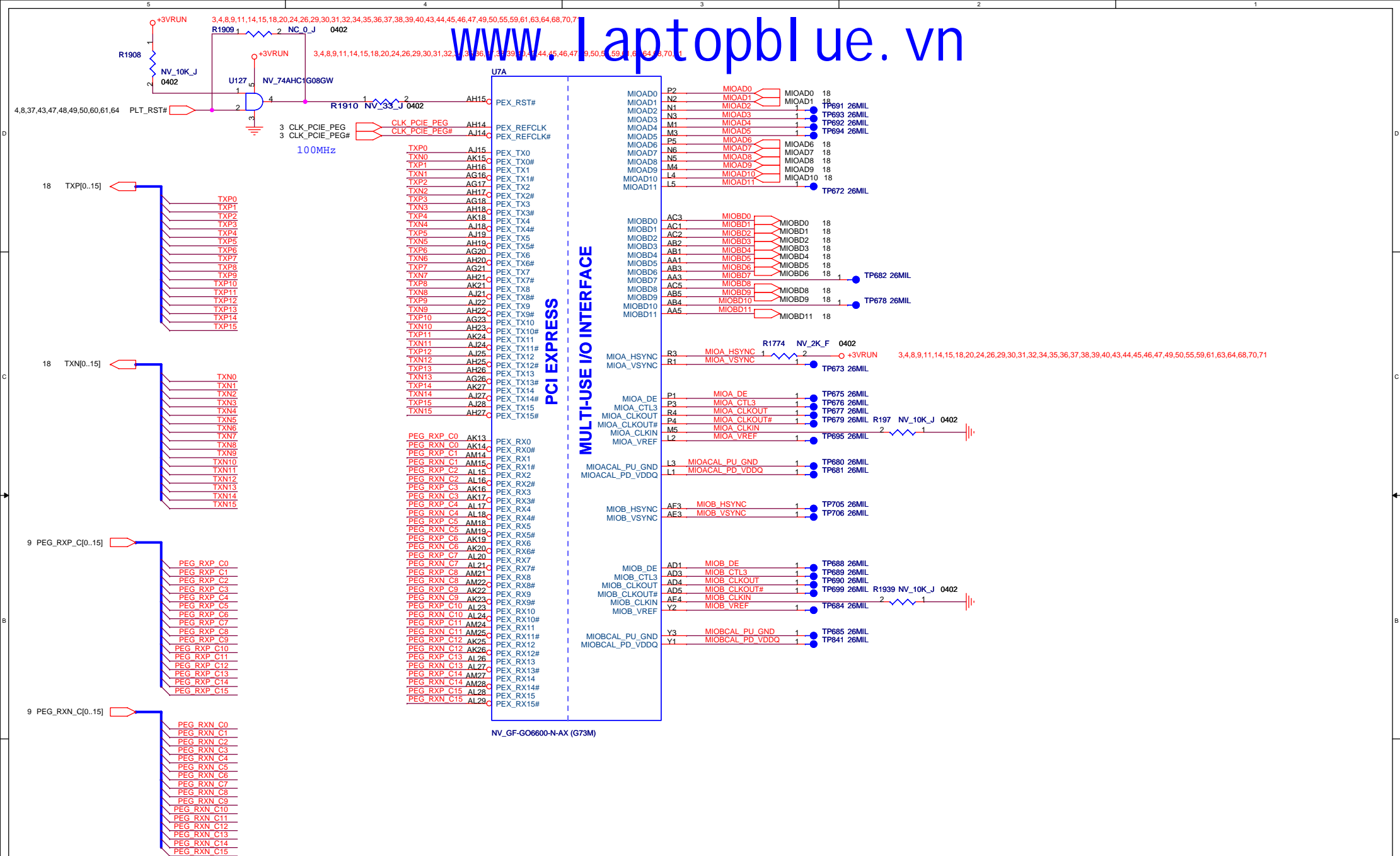
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AN23	VSS_181	D11	VSS_274
AM23	VSS_182	B11	VSS_275
AH23	VSS_183	AV10	VSS_276
AG23	VSS_184	AP10	VSS_277
W23	VSS_185	AL10	VSS_278
K23	VSS_186	AJ10	VSS_279
J23	VSS_187	AG10	VSS_280
F23	VSS_188	AC10	VSS_281
C23	VSS_189	W10	VSS_282
AA22	VSS_190	U10	VSS_283
Y22	VSS_191	BA9	VSS_284
G22	VSS_192	AW9	VSS_285
D22	VSS_193	AR9	VSS_286
E22	VSS_194	AH9	VSS_287
D22	VSS_195	AB9	VSS_288
A22	VSS_196	Y9	VSS_289
RA21	VSS_197	R9	VSS_290
AR21	VSS_198	G9	VSS_291
AN21	VSS_199	E9	VSS_292
AL21	VSS_200	A9	VSS_293
AB21	VSS_201	AG8	VSS_294
Y21	VSS_202	AD8	VSS_295
P21	VSS_203	AA8	VSS_296
K21	VSS_204	UR	VSS_297
J21	VSS_205	K8	VSS_298
H21	VSS_206	C8	VSS_299
C21	VSS_207	BA7	VSS_300
AW20	VSS_208	AV7	VSS_301
AR20	VSS_209	AP7	VSS_302
AN20	VSS_210	AL7	VSS_303
AJ20	VSS_211	AJ7	VSS_304
K20	VSS_212	AH7	VSS_305
B20	VSS_213	AF7	VSS_306
A20	VSS_214	AC7	VSS_307
AN19	VSS_215	R7	VSS_308
AC19	VSS_216	G7	VSS_309
W19	VSS_217	D7	VSS_310
K19	VSS_218	AG6	VSS_311
G19	VSS_219	AD6	VSS_312
C19	VSS_220	AB6	VSS_313
AH18	VSS_221	Y6	VSS_314
K29	VSS_222	U6	VSS_315
H18	VSS_223	N6	VSS_316
D18	VSS_224	K6	VSS_317
A18	VSS_225	B6	VSS_318
AY17	VSS_226	AV5	VSS_319
AR17	VSS_227	AD5	VSS_320
AP17	VSS_228	AE5	VSS_321
AY14	VSS_229	AF5	VSS_322
AK17	VSS_230	AR4	VSS_323
AV16	VSS_231	AP4	VSS_324
AN16	VSS_232	AL4	VSS_325
AL16	VSS_233	AL4	VSS_326
J16	VSS_234	Y4	VSS_327
F16	VSS_235	Y4	VSS_328
C16	VSS_236	U4	VSS_329
AN15	VSS_237	J4	VSS_330
AM15	VSS_238	F4	VSS_331
AK15	VSS_239	C4	VSS_332
N15	VSS_240	AY3	VSS_333
L15	VSS_241	AW3	VSS_334
G15	VSS_242	AV3	VSS_335
A15	VSS_243	AL3	VSS_336
BA14	VSS_244	AH3	VSS_337
AT14	VSS_245	AG3	VSS_338
M26	VSS_246	AF3	VSS_339
K26	VSS_247	AD3	VSS_340
F26	VSS_248	AC3	VSS_341
D26	VSS_249	AA3	VSS_342
AK25	VSS_250	G3	VSS_343
H14	VSS_251	AT2	VSS_344
P25	VSS_252	AR2	VSS_345
K25	VSS_253	AP2	VSS_346
H25	VSS_254	AK2	VSS_347
E25	VSS_255	AJ2	VSS_348
AN13	VSS_256	AD2	VSS_349
A25	VSS_257	AB2	VSS_350
BA24	VSS_258	Y2	VSS_351
AG13	VSS_259	Y2	VSS_352
P13	VSS_260	T2	VSS_353
AL24	VSS_261	N2	VSS_354
AW23	VSS_262	J2	VSS_355
	VSS_263	H2	VSS_356
	VSS_264	F2	VSS_357
	VSS_265	C2	VSS_358
	VSS_266	AL1	VSS_359
	VSS_267		VSS_360
	VSS_268		
	VSS_269		
	VSS_270		
	VSS_271		
	VSS_272		

QG82945PM_A3









TV MODE(NV43M/G7X)		
NTSC (01)		
MIOAD10	MIOAD7	TVMODE
0	0	SECAM
0	1	NTSC
1	0	PAL
1	1	CRT

Strap for GDDR3-136ball
 0001 16Mx32Infineon
 0010 16Mx32Hynix
 0011 16Mx32Samsung

0101 8Mx32Infineon
 0110 8Mx32Hynix
 0111 8Mx32Samsung

SUBVENDOR
 0 (USE SYSTEM BIOS)
 1 (USE EXTERNAL ROM)

MIOAD0 is used to set
 the PCI Express PLL
 termination enable.
 DEFAULT "0"

3GIO_PADCFG[2:0]
 001 for NV43/NV44
 010 for G7X/NV42

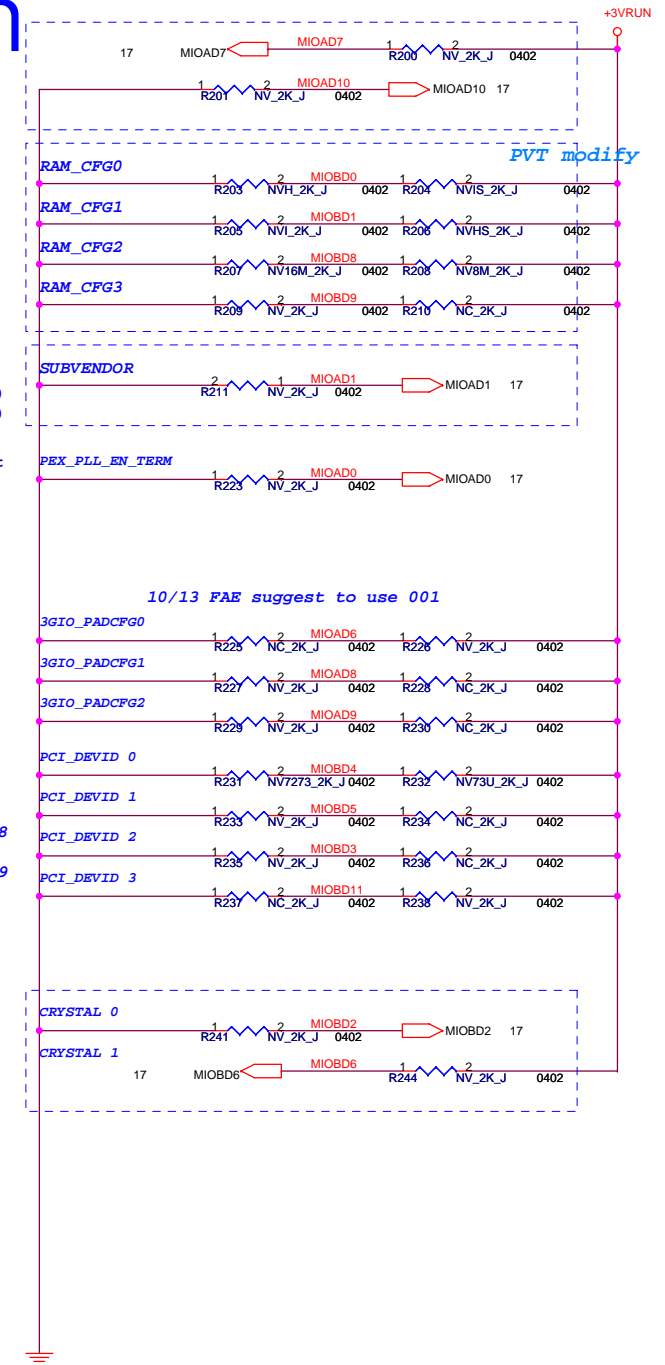
G72M/G73M/NV43M
 PCI_DEVID[3:0]="1000"->8
 G73M-U
 PCI_DEVID[3:0]="1001"->9

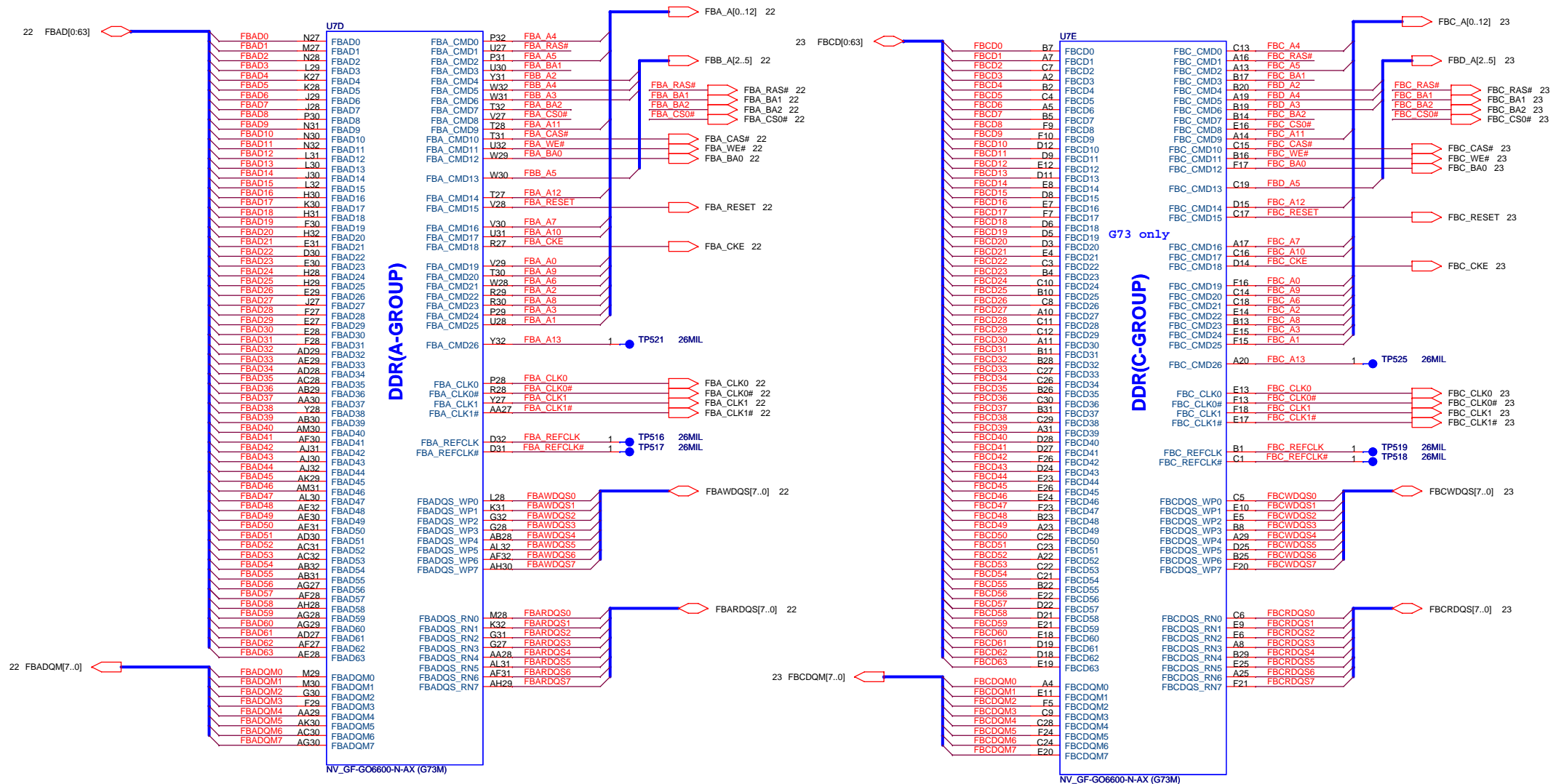
CRYSTAL(NV43M/G7X)
 10 (27M Hz)

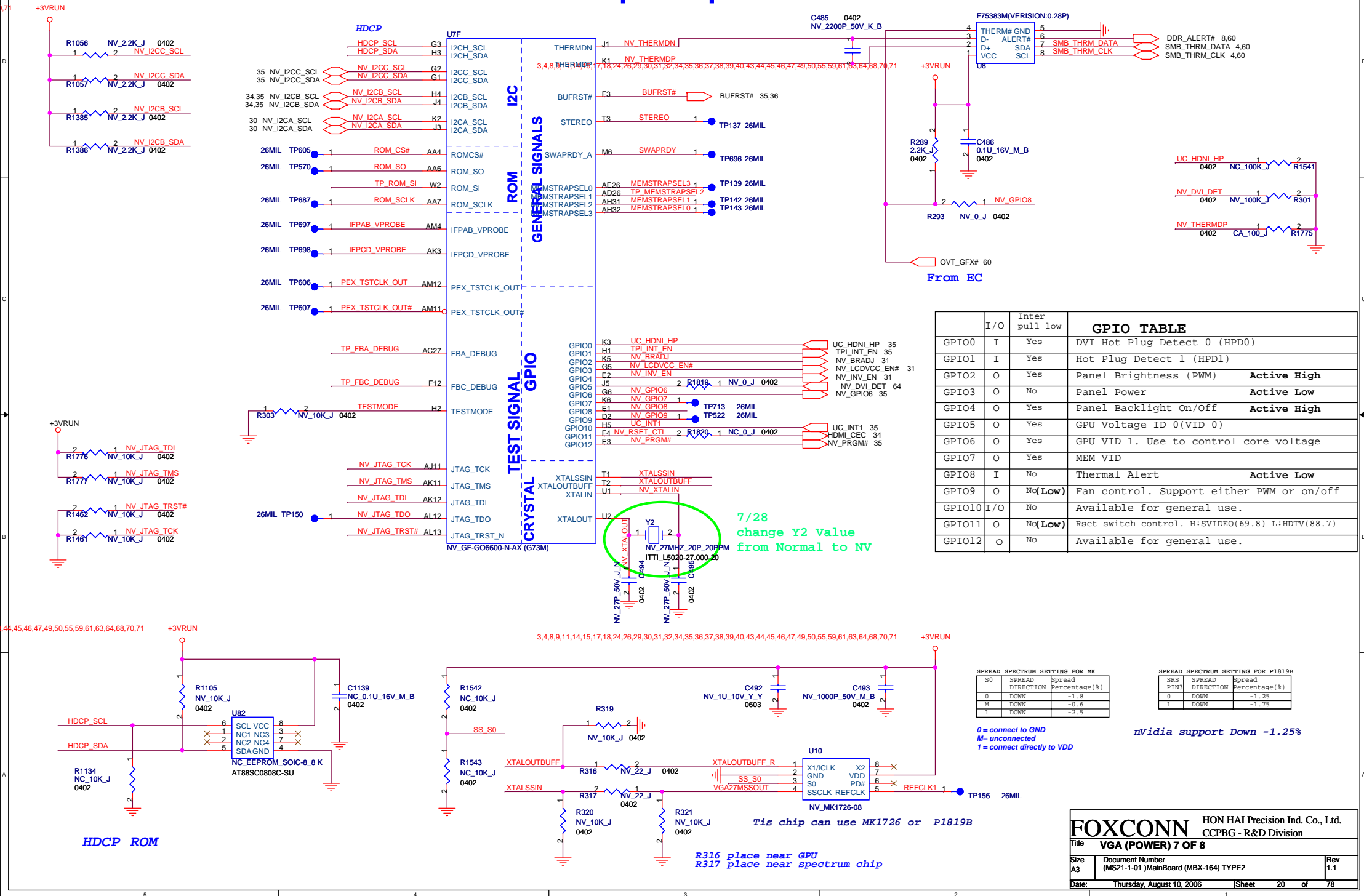
MIOBD6	MIOBD2	Crystal
1	0	27MHz
0	1	14.318MHz
0	0	13.5MHz
1	1	Reserved

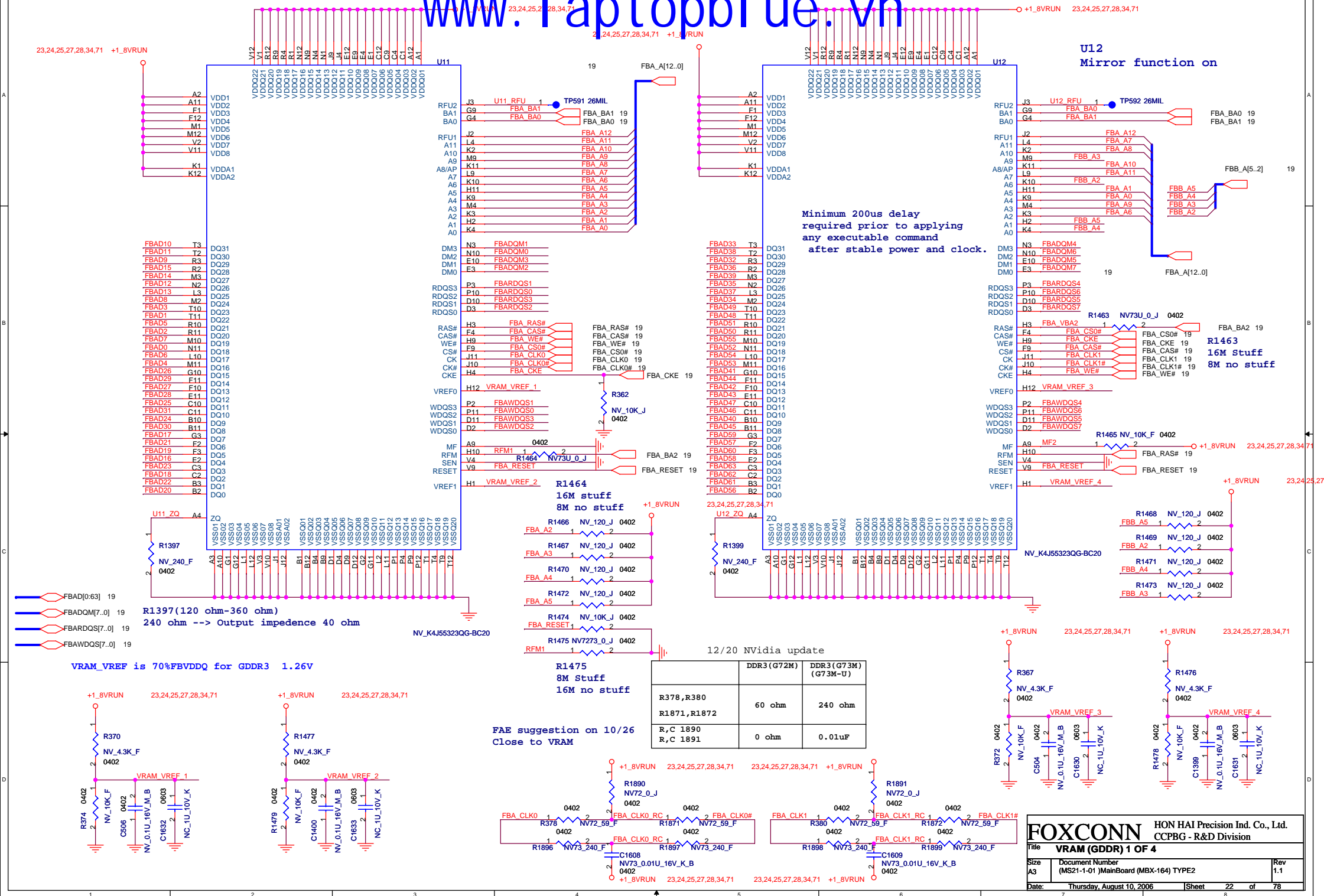
ROM_TYPE(NV43M/G7X) NC
 MIOBD10,MIOBD_HSYNC

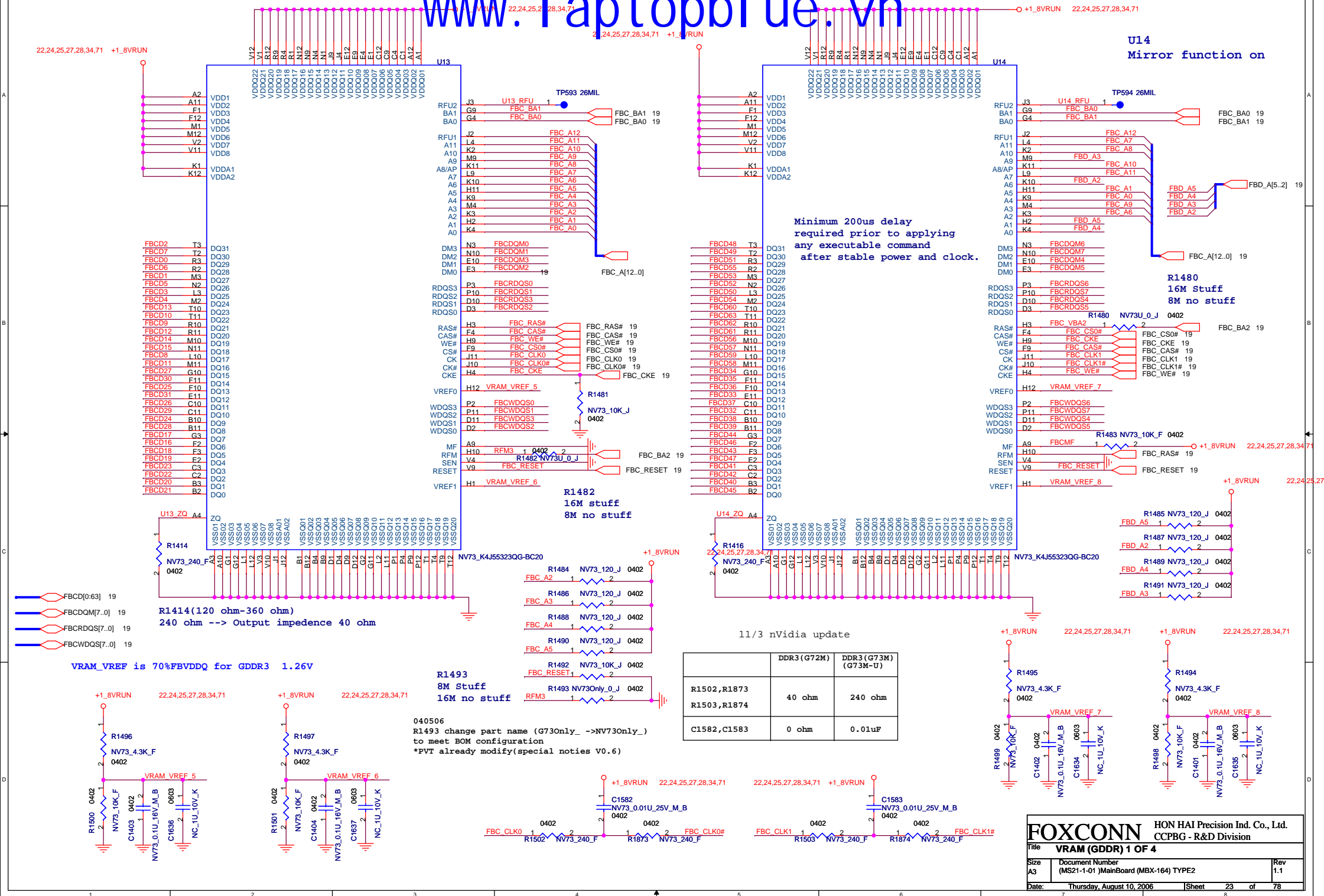
00 PARALLEL
 01 SERIAL_AT25F
 10 SERIAL_SST45VF
 11 LPC

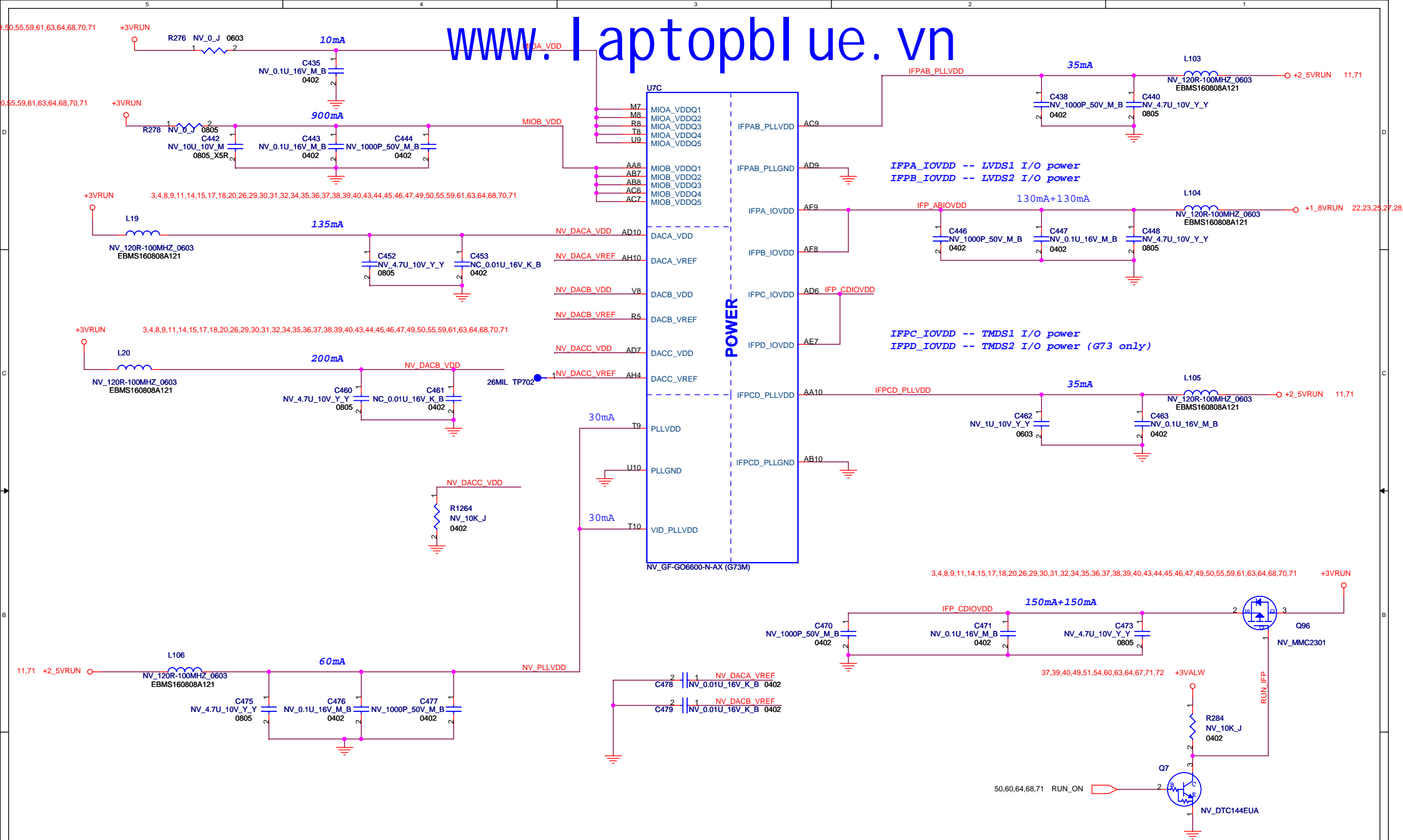




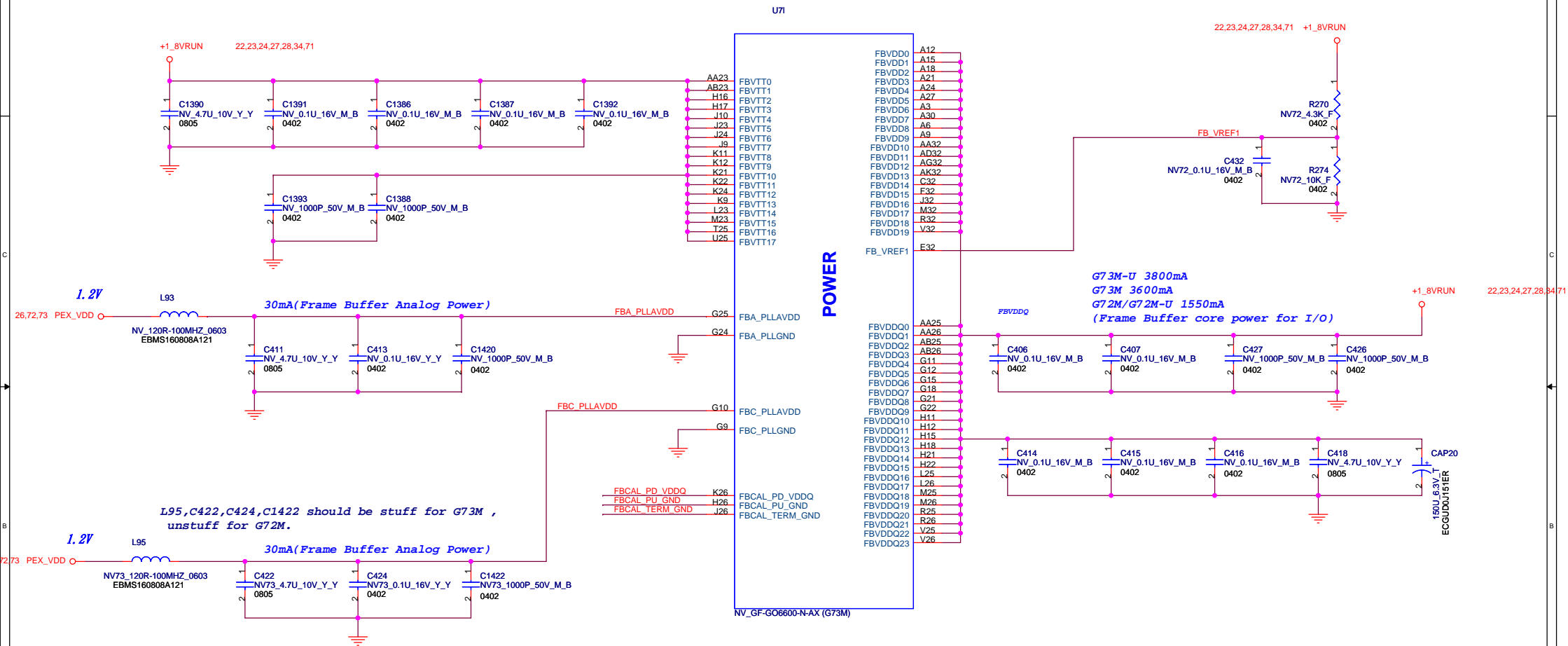








For GDDR3 FBVTT require decoupling capacitor,FBVDD don't require them.



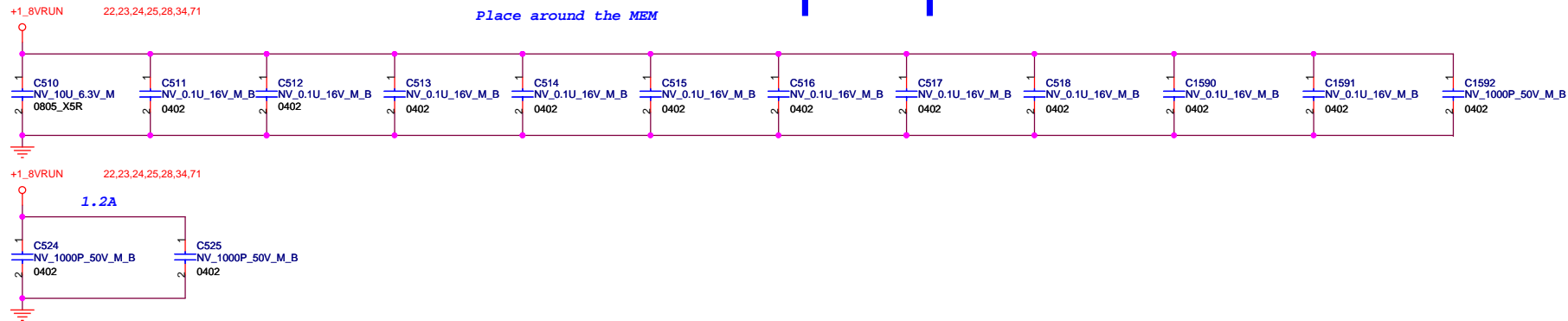
	DDR1	DDR3(G72M)	DDR3(G73M)
FBCAL_PD_VDDQ	40 ohm	60 ohm	50 ohm
FBCAL_PU_GND	30 ohm	40 ohm	40 ohm
FBCAL_TERM_GND	NC	40 ohm	40 ohm



R1544 NV72_10K_J 0402

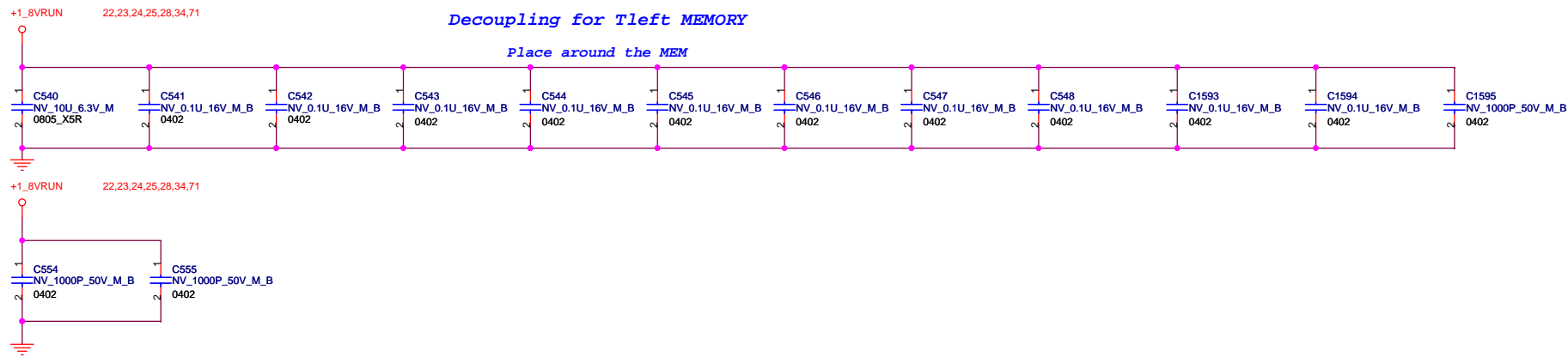
Decoupling for Tright MEMORY

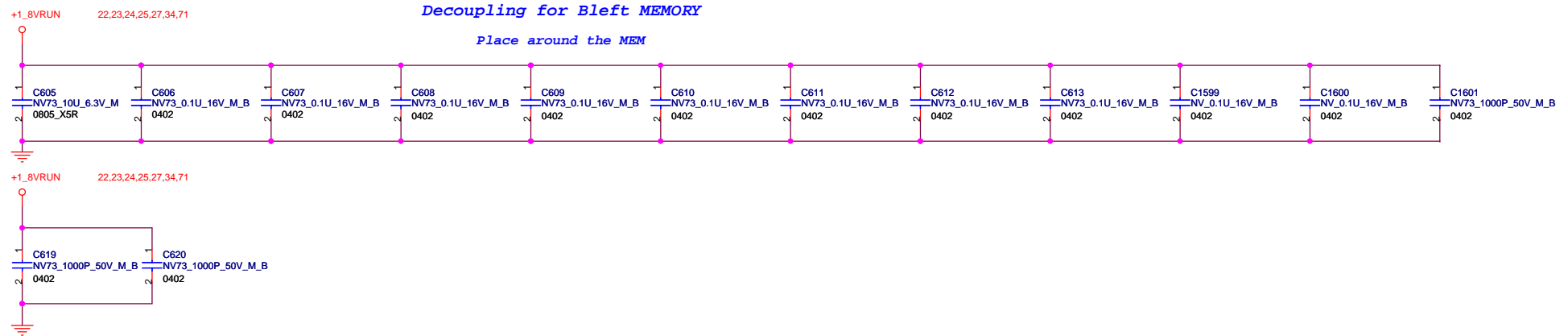
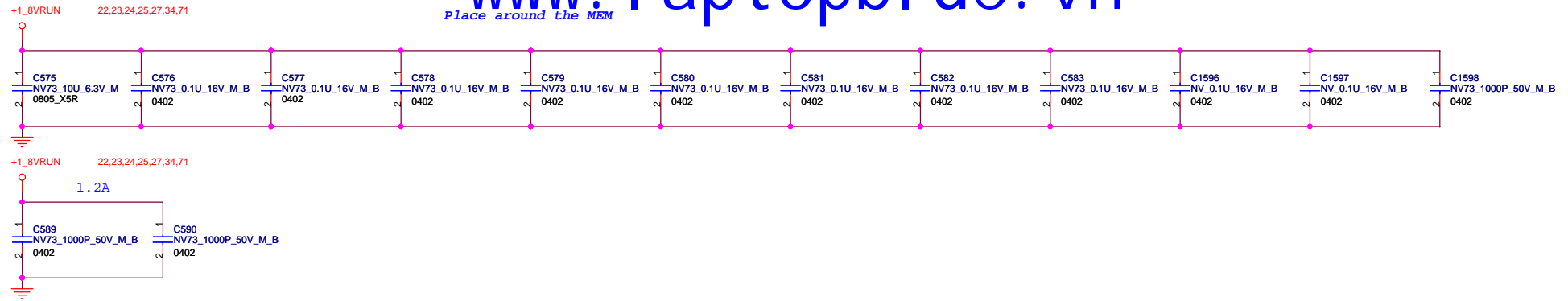
Place around the MEM



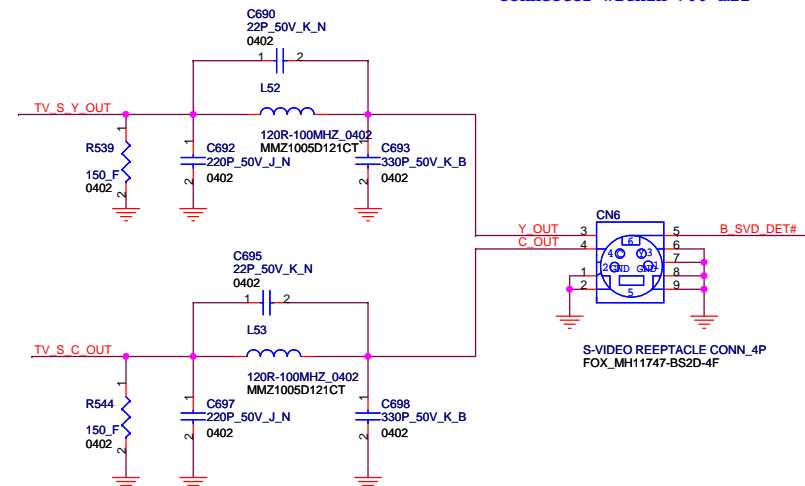
Decoupling for Tleft MEMORY

Place around the MEM



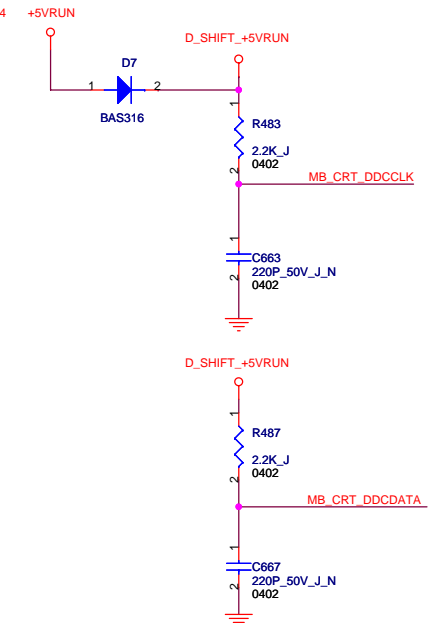
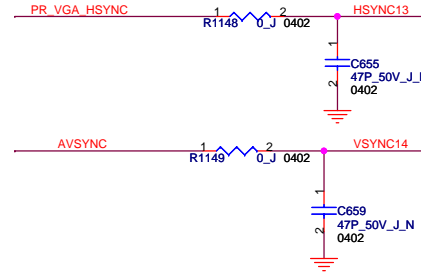


30,34,35,38,40,42,43,47,55,56,57,61,63,70,71,73,74 +5VRUN



*When DOCKED# L, MB SCAN OFF,
When DOCKED# H, MB SCAN ON.*

Semi-PnP(EC IN)



LVDS

Group1

Group2

www.laptopblu.com

2006/6/2

```
(do inverter (do (circut (ft sch)
the inverter circuit is the same with MS20 MP)
Detail change list
Delete PR426&PR427 and change
C604-1, C1557-1, C1558-1, CN49pin1, pin2
net name INVERTER VCC to net DCBATOUT.
```

Place C640 and C1558 close to CN49.

66,67,68,69,70,71,72,73 DCBATOUT

3,4,8,9,11,14,15,17,18,20,24,26,29,30,32,34,35,36,37,38,39,40,43,44,45,46,47,49,50,55,59,61,63,64,68,70,71

U106,U15,U16 can use ON (MC74VHC1G08DFT2G)
H.H. PN:14-MC74VHC-1G04

INVERTER CONNECTOR

LVDS CONNECTOR

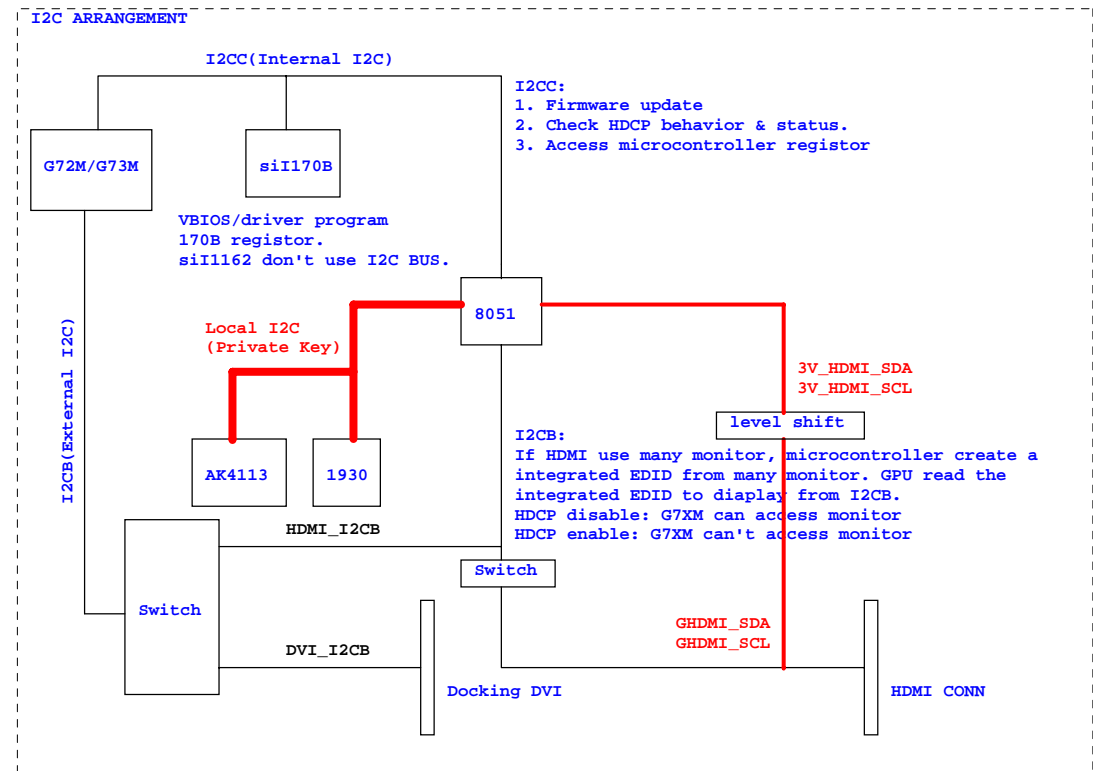
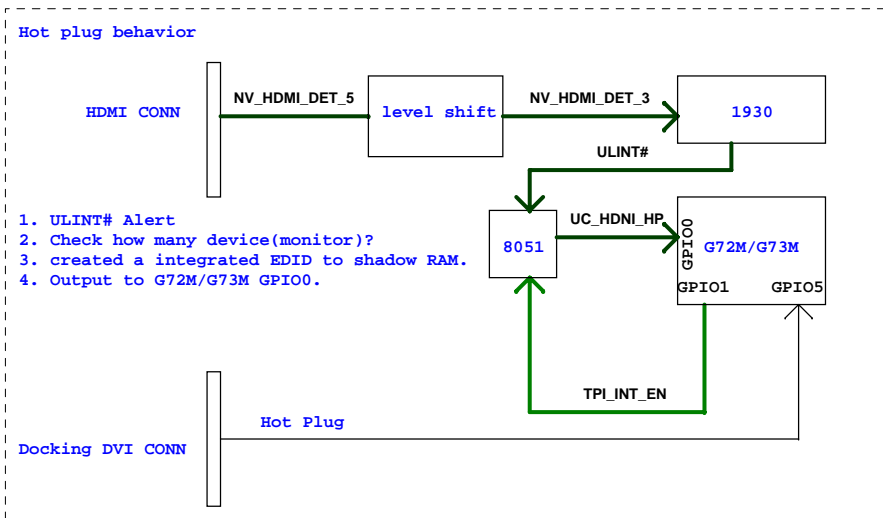
PANEL ID

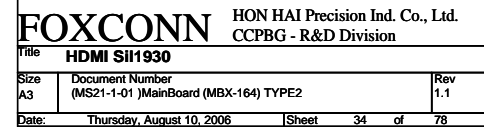
```
FAN_SEL:
H: Foxconn FAN
L: MOR cooling unit
```

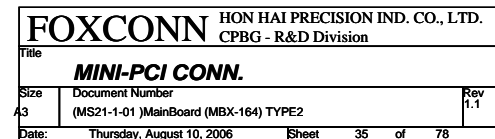
Type	WXGA+	WXGA+	WUXGA
Size	17" wide	17" wide	17" wide
Vender	LG-PHILIPS	LG-PHILIPS	SHARP
Device Name	LP171WP7-TLAL	LP171WX2-A4K3	LQ170M1LA04
Panel ID Check[3..0]	2 Lamps	1 Lamps	2 Lamps
	0001	0010	0100

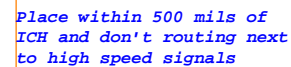
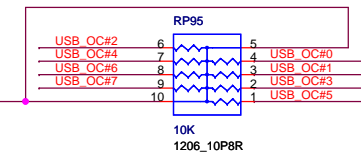
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title LVDS			
Size A3	Document Number (MS21-1-01) MainBoard (MBX-164) TYPE2		Rev 1.1
Date:	Thursday, August 10, 2006	Sheet	31 of 78

Hot plug behavior & I2C ARRANGEMENT block diagram





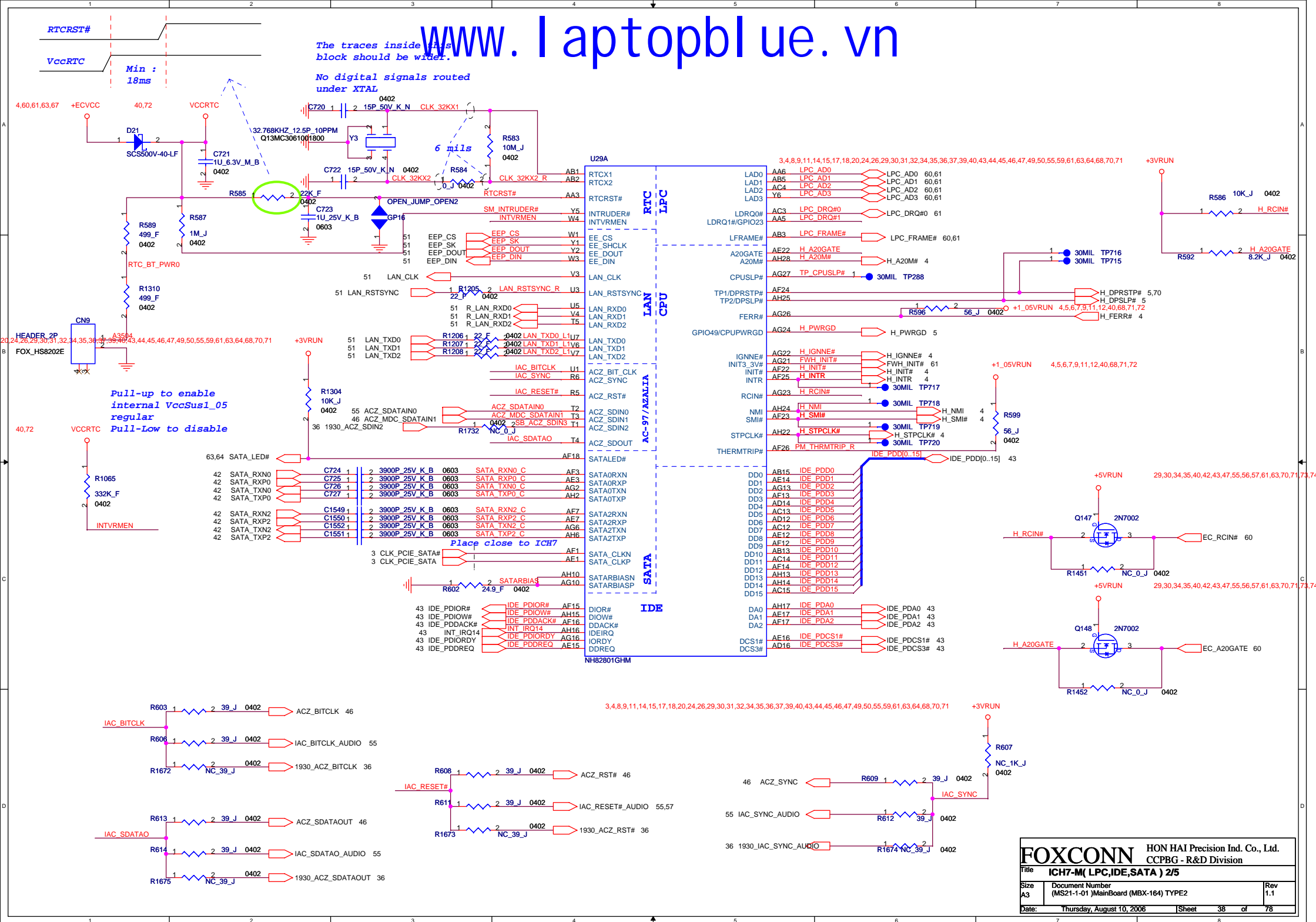


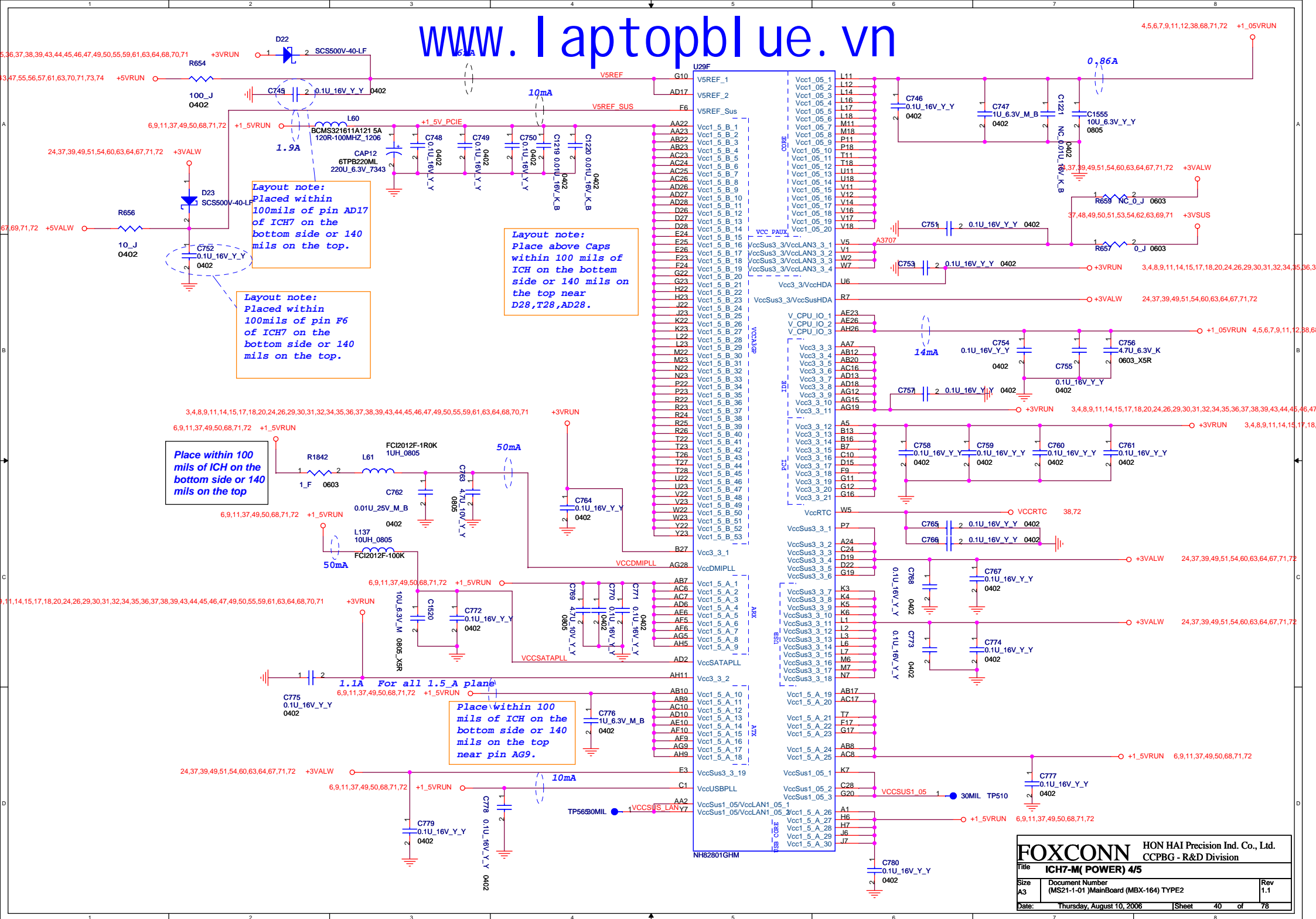


	GNT5#	GNT4#
LPC(Default)	Hi	Hi
PCI	Hi	LOW

Place within
500 mils of
ICH

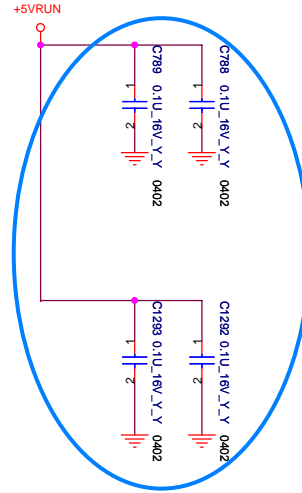
www.laptopblue.vn





5/6
 For power droup cause 0.16V voltage loss Issue
 (1)F7,F8,F19,F20 no stuff
 (2)Co-layout normal open gap GP17~GP18 with fuse
 5/27 Delete SATA HDD Fuse backup circuit
 (1)Remove F7,F8,F19,F20 Pad
 (2)Remove GP17~GP18 open gap

29,30,34,35,38,40,43,47,55,56,57,61,63,70,71,73,74

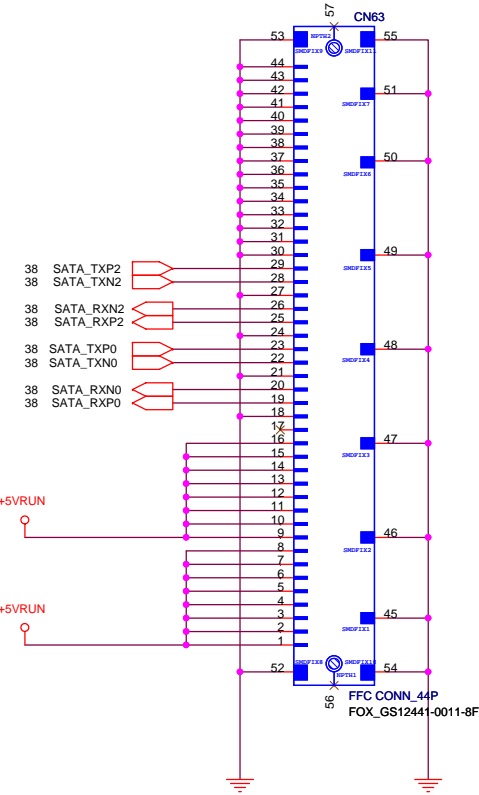


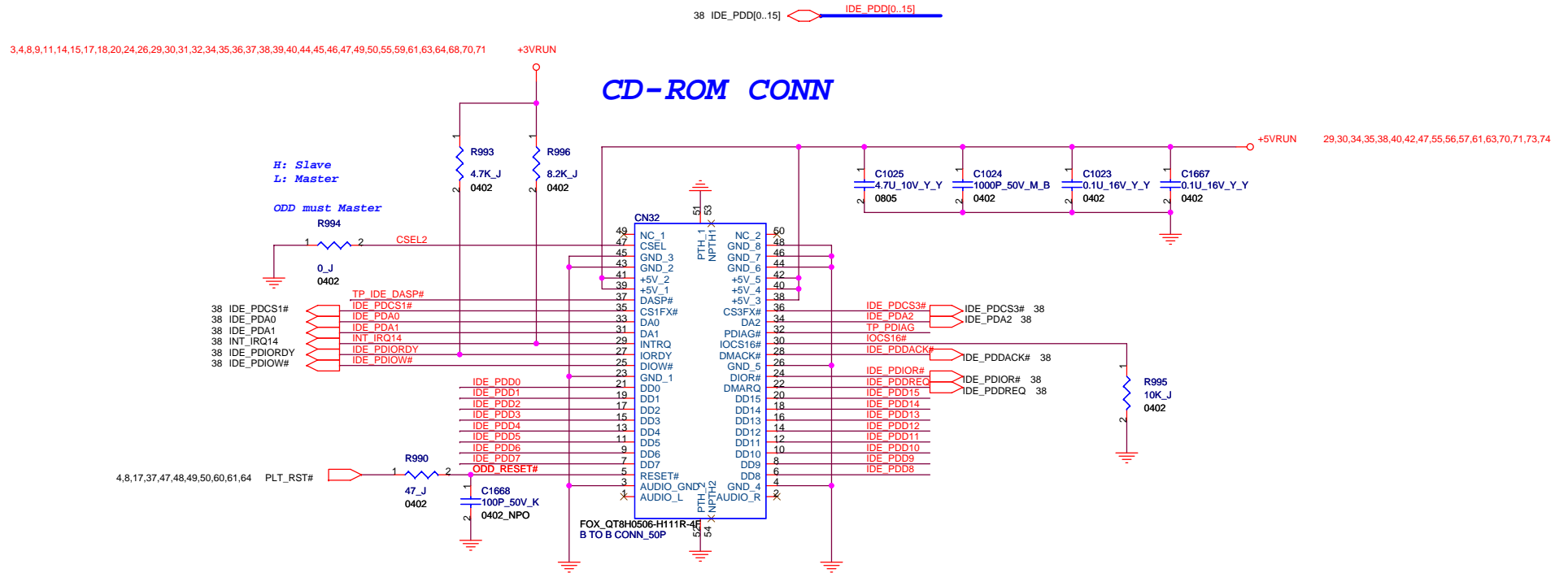
29,30,34,35,38,40,43,47,55,56,57,61,63,70,71,73,74

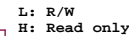
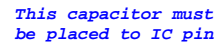
+5VRUN

29,30,34,35,38,40,43,47,55,56,57,61,63,70,71,73,74

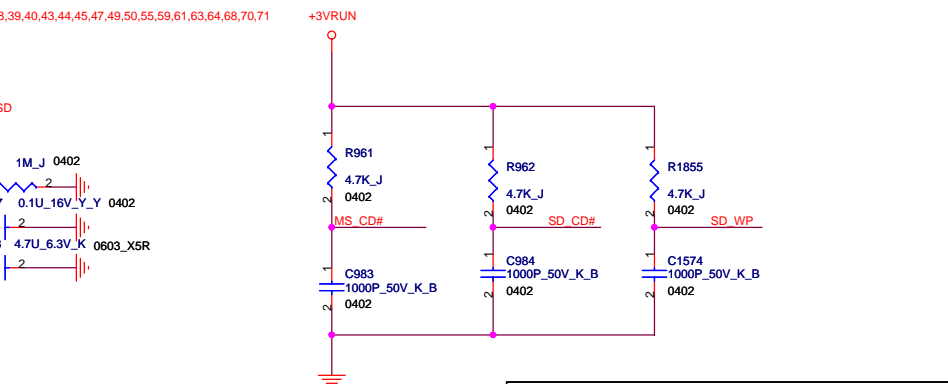
+5VRUN

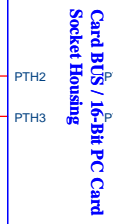


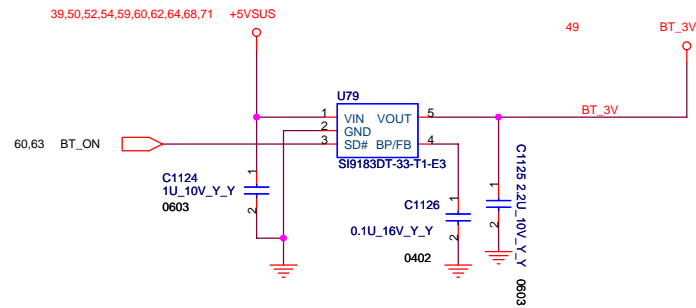




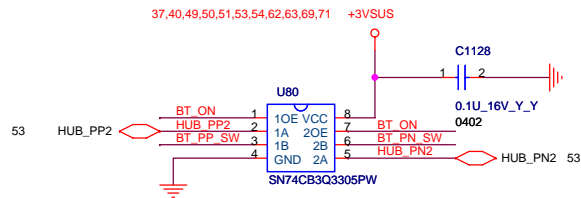
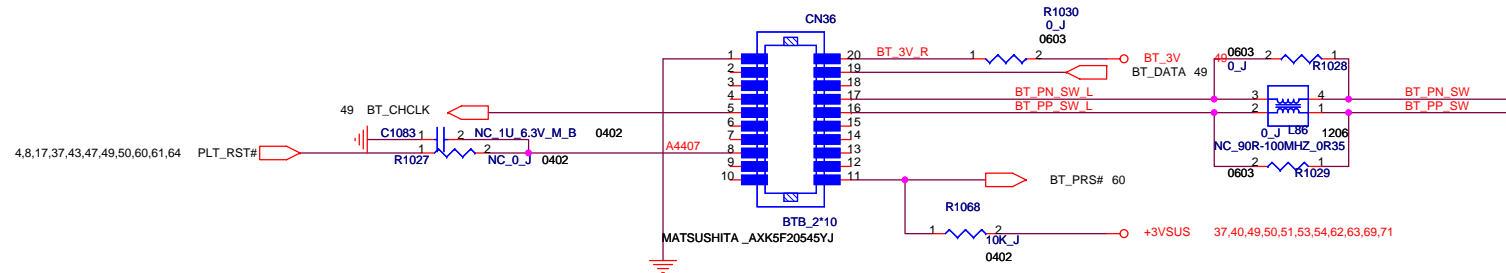
SD/CONN.







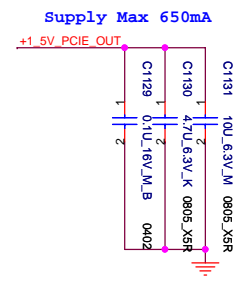
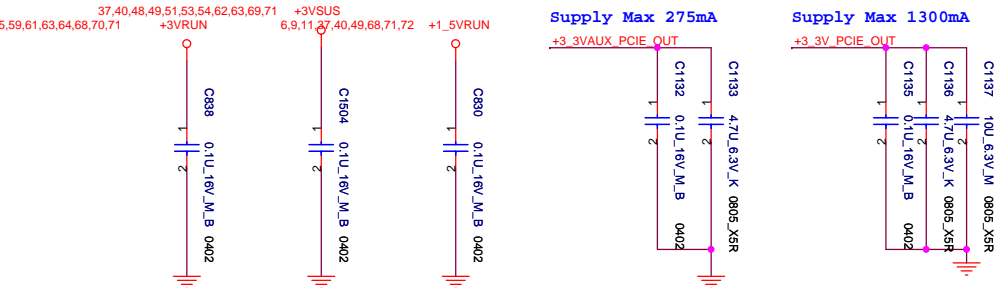
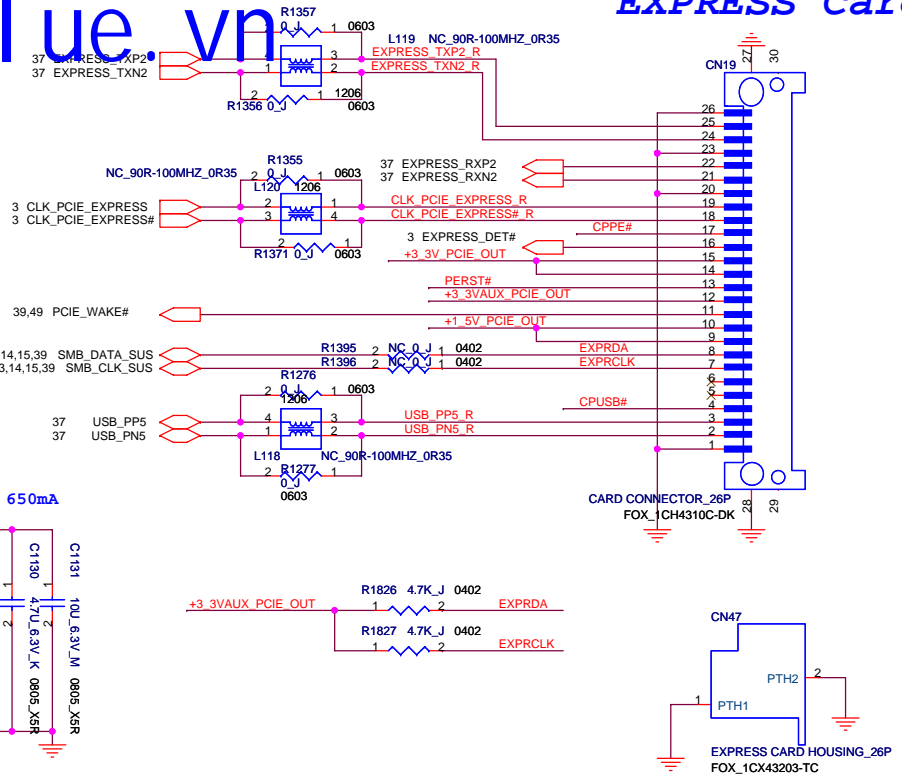
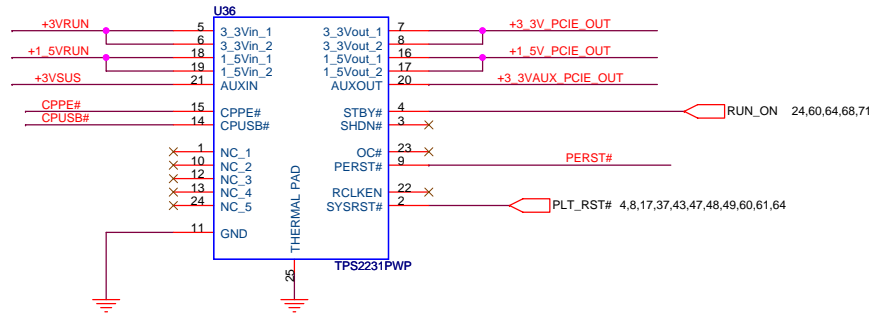
Bluetooth connector



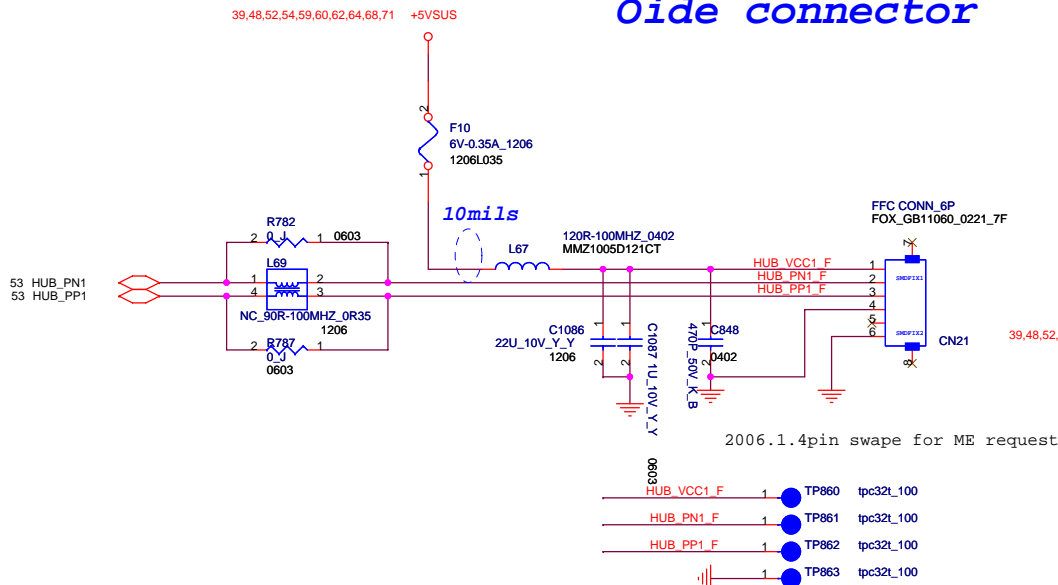
VOLTAGE INPUTS ⁽¹⁾			LOGIC INPUTS			VOLTAGE OUTPUTS ⁽²⁾			MODE ⁽³⁾
AUXIN	3.3VIN	1.5VIN	SHDN	STBY	CP ⁽⁴⁾	AUXOUT	3.3VOUT	1.5VOUT	Card Inserted
Off	x	x	x	x	x	Off	Off	Off	Card Inserted
On	x	x	0	x	x	GND	GND	GND	Standby
On	x	x	1	x	1	GND	GND	GND	Card Inserted
On	On	On	1	0	0	On	Off	Off	Standby
On	On	On	1	1	0	On	On	On	Card Inserted

www.laptopbl ue. vn

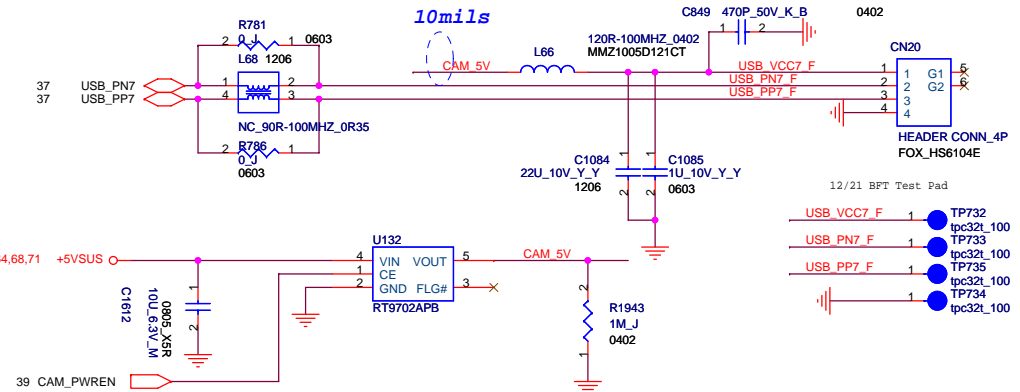
EXPRESS Card



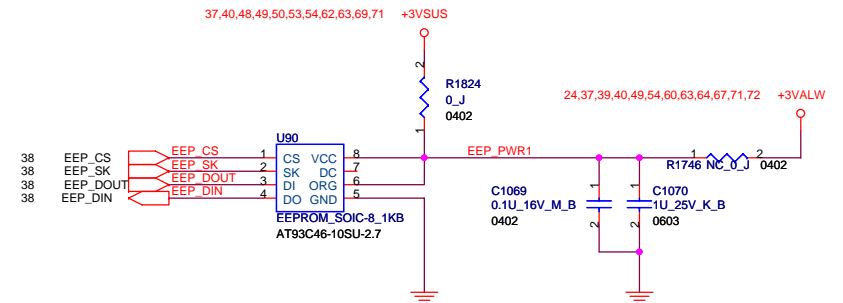
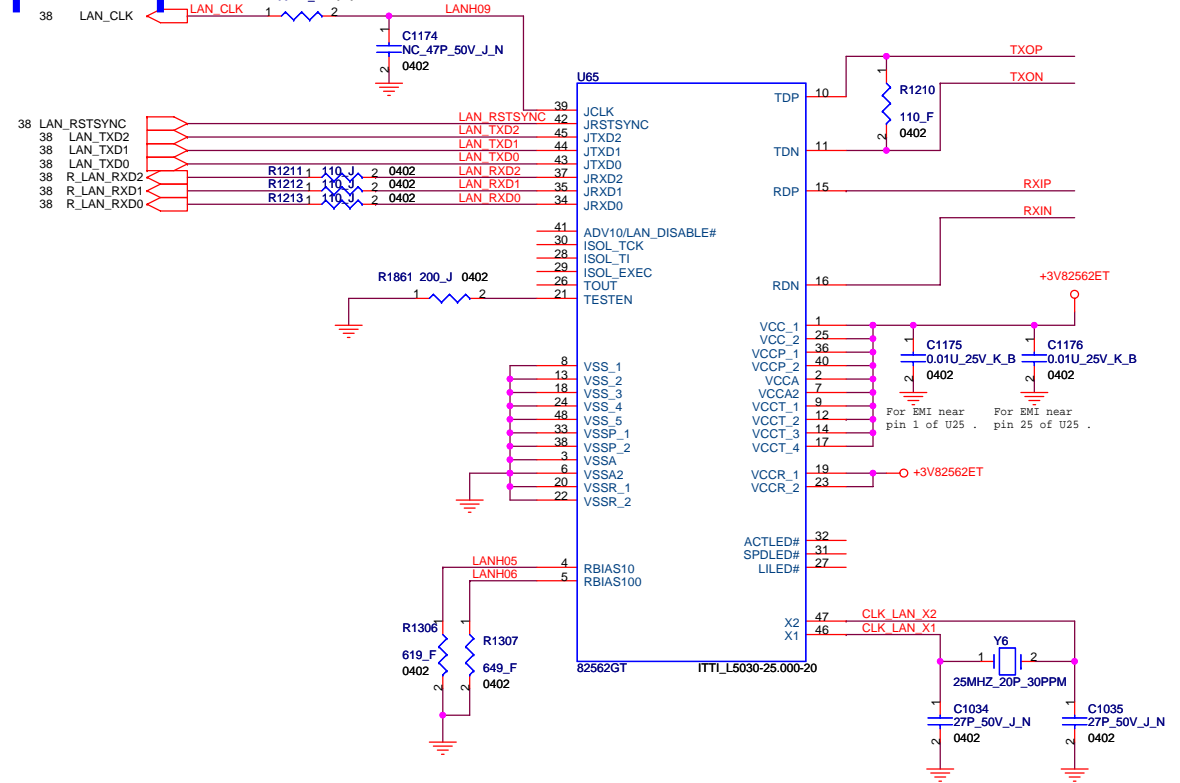
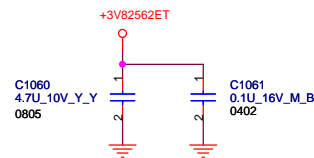
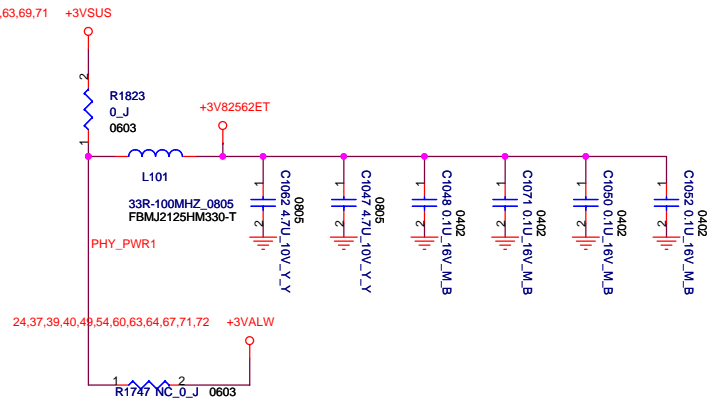
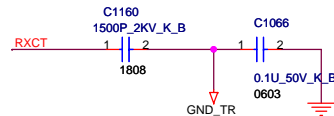
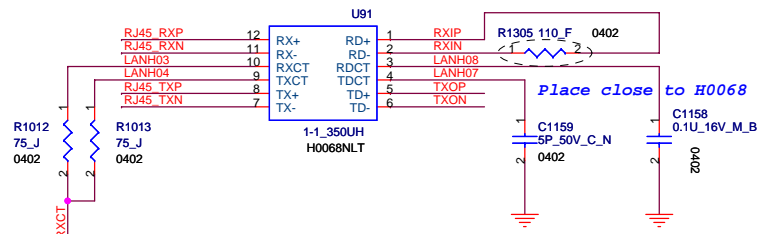
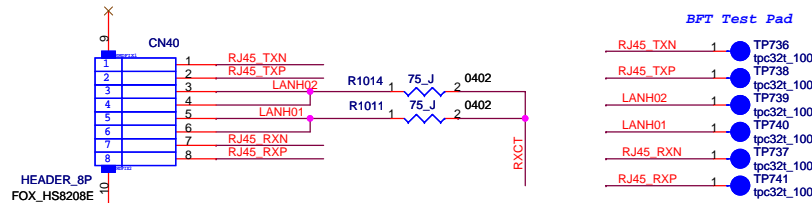
Oide connector



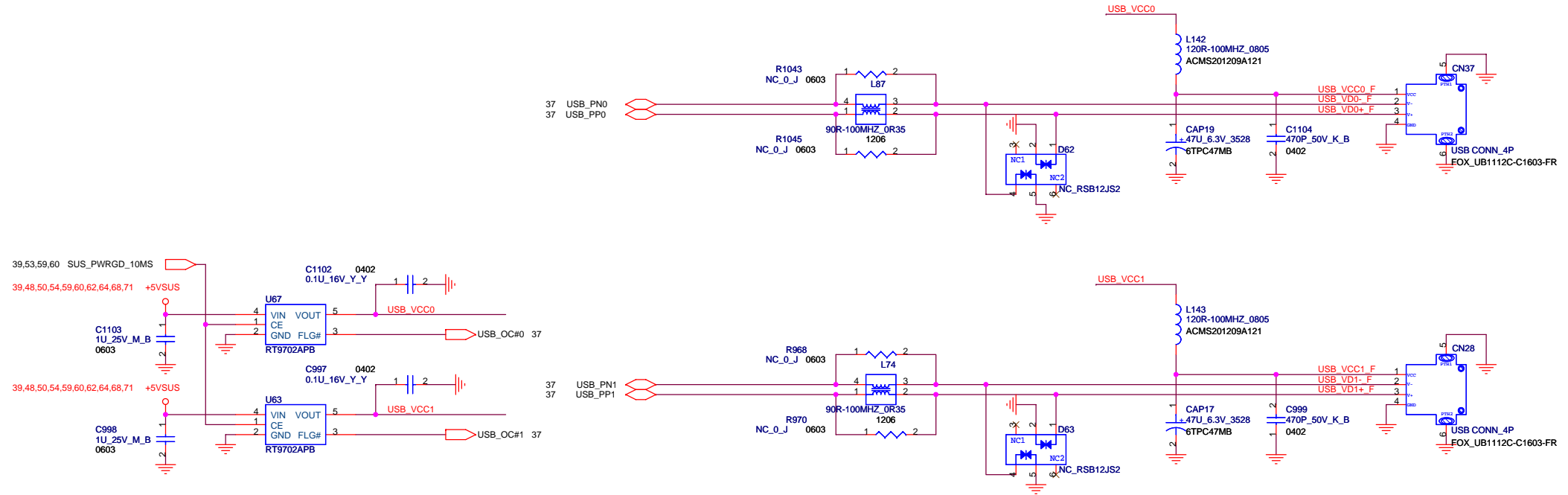
CAMERA connector



LAN connector

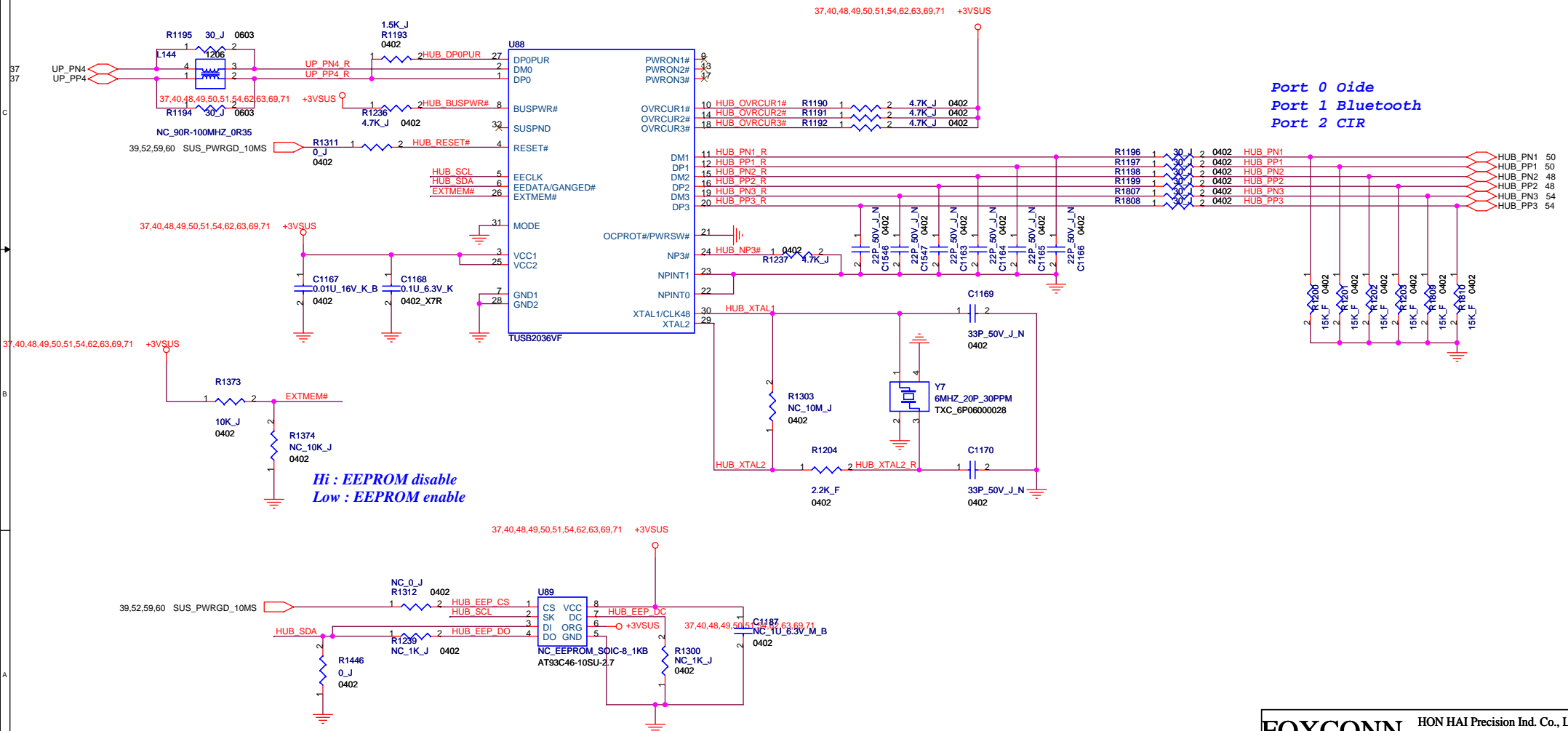


USB connector #2

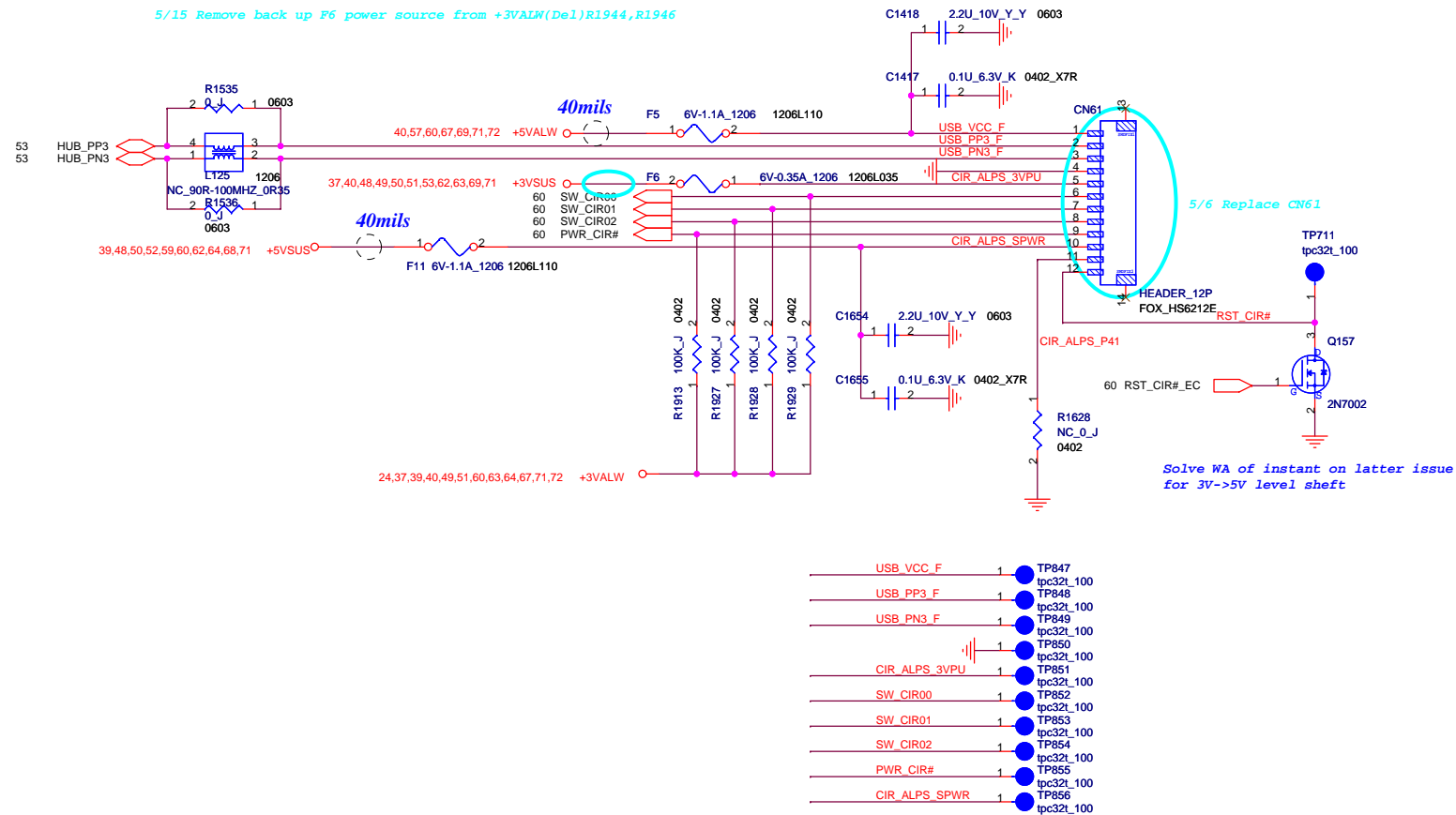


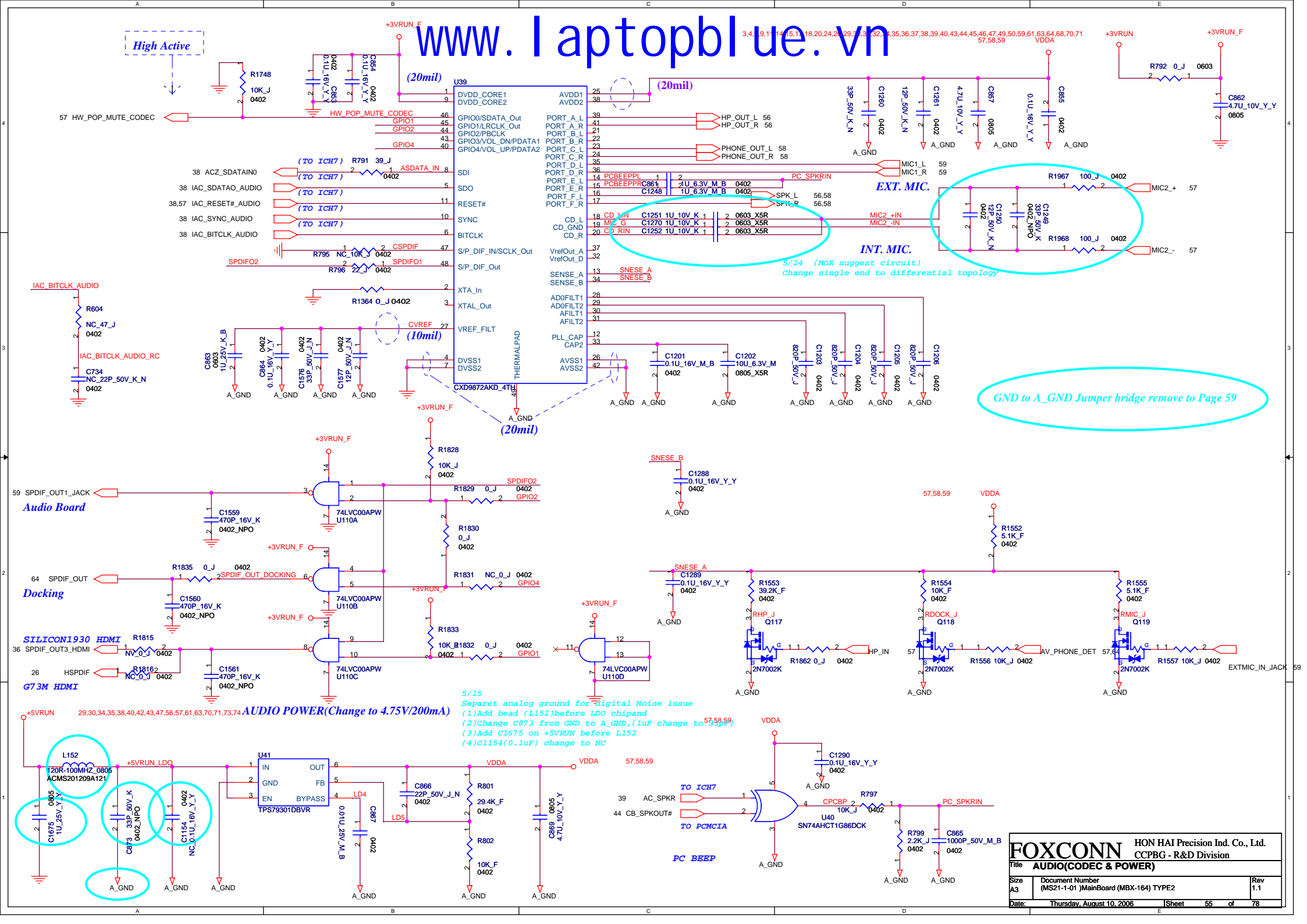
Application design in datasheet 27 ohm;
but 30ohm is also in range of USB Spec.

USB 1.1 HUB

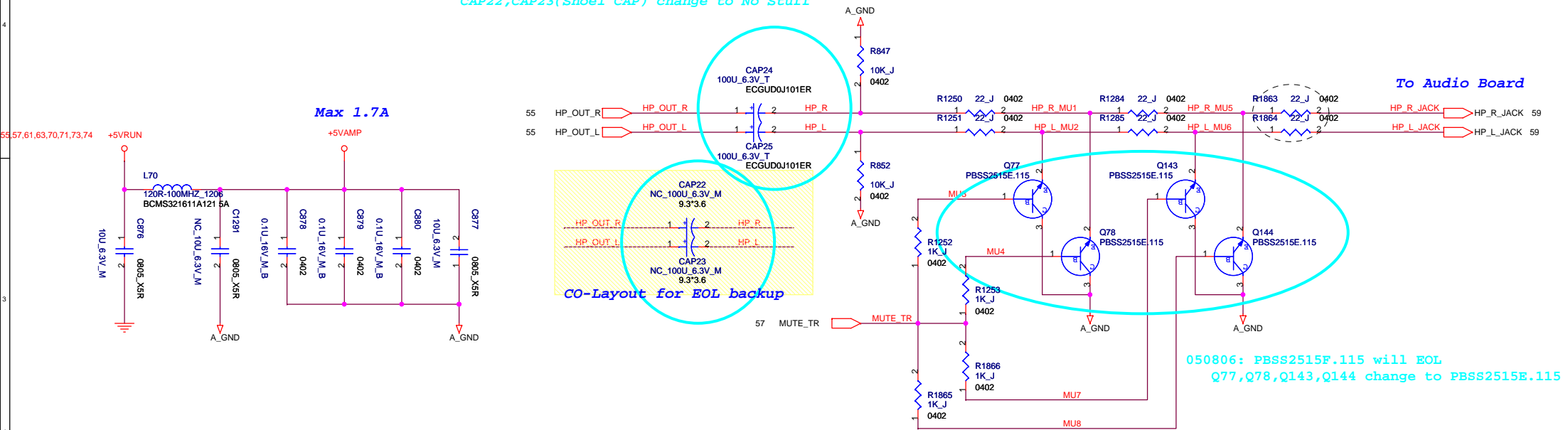


IR Rreceiver connector





```
050806: Shoei CAP will EOL
CAP24,CAP25(SP CAP) change to Stuff
CAP22,CAP23(Shoei CAP) change to No Stuff
```

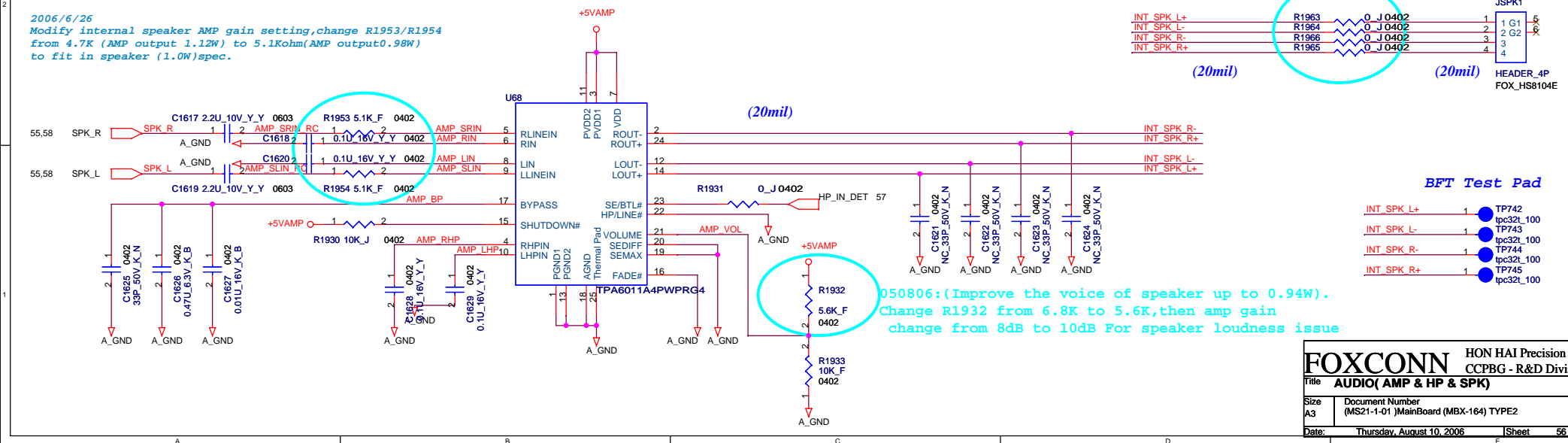


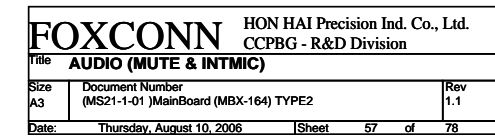
INTERNAL SPEAKER

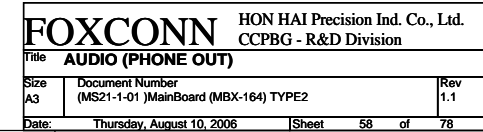
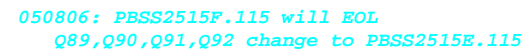
050806:(Improve the voice of speaker up to 0.94W).
Add damping Resistors R1953 on AMP_SRIN,R1954 on AMP_SLIN
then speaker amp output won't be distorted.
For speaker loudness issue.

2006/6/26
Modify internal speaker AMP gain setting,change R1953/R1954
from 4.7K (AMP output 1.12W) to 5.1Kohm(AMP output0.98W)
to fit in speaker (1.0W)spec.

050806:(Improve the voice of speaker up to 0.94W).
EMI team confirm whether
it is ok to use 0ohm resistor replacing bead



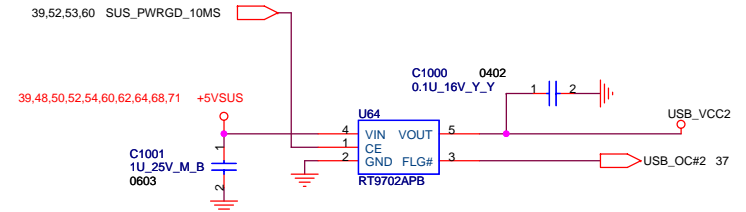
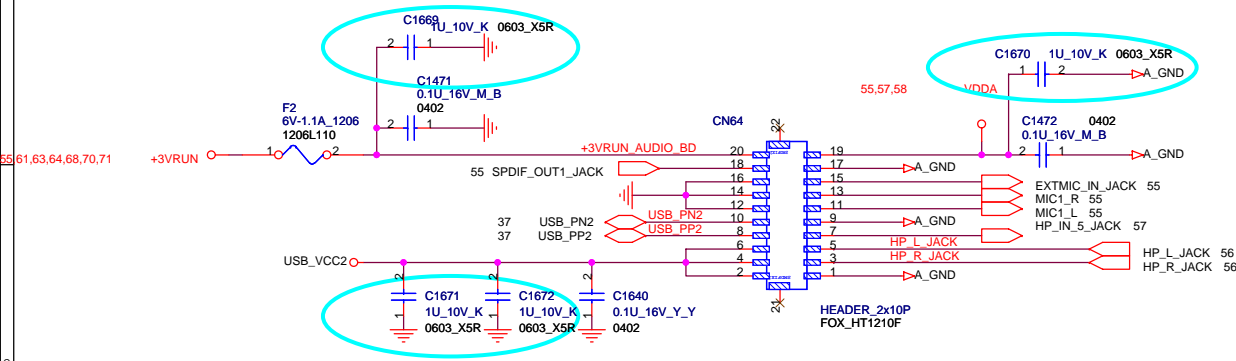




Audio Board connector

050806: (To improve SNR issue)

Add 1uF capacitors close CN64 :C1671,C1672 on USB_VCC2,
C1669 on +3VRUN_AUDIO_BD, and C1670 on VDDA .



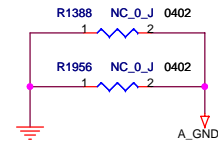
5/6

Separate analog ground for digital Noise issue:

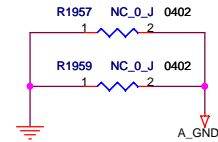
- (1) Remove GP3 (Close Jumper) not bridge between GND and A_GND
- (2) Backup two jumper resistors for bridge between GND and A_GND
(C1388, C1966 on Screw hole H3, C1957, C1959 on screw hole H5)
- (3) Isolate screw hole H4, add 100pF capacitors C1673, C1674 for EMI, Zener diode D100 for ESD
- (4) Add jumper resistor for Return patch R1955 close L70 (+5VAMP) & R1958 close U41 (+5VRUN) & R1960 close codec.

Backup two jumper resistors for bridge between GND and A_GND

Close screw hole H3

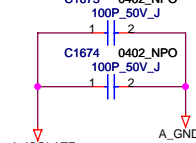


Close screw hole H5

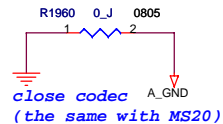
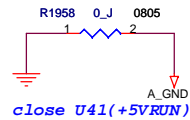
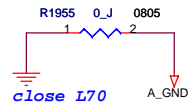


Isolate screw hole H4, and add EMI/ESD solution

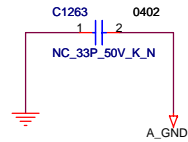
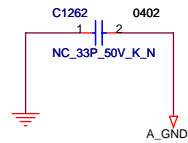
EMI



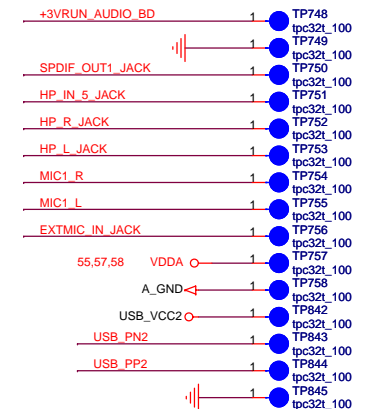
Add jumper resistor for Return patch

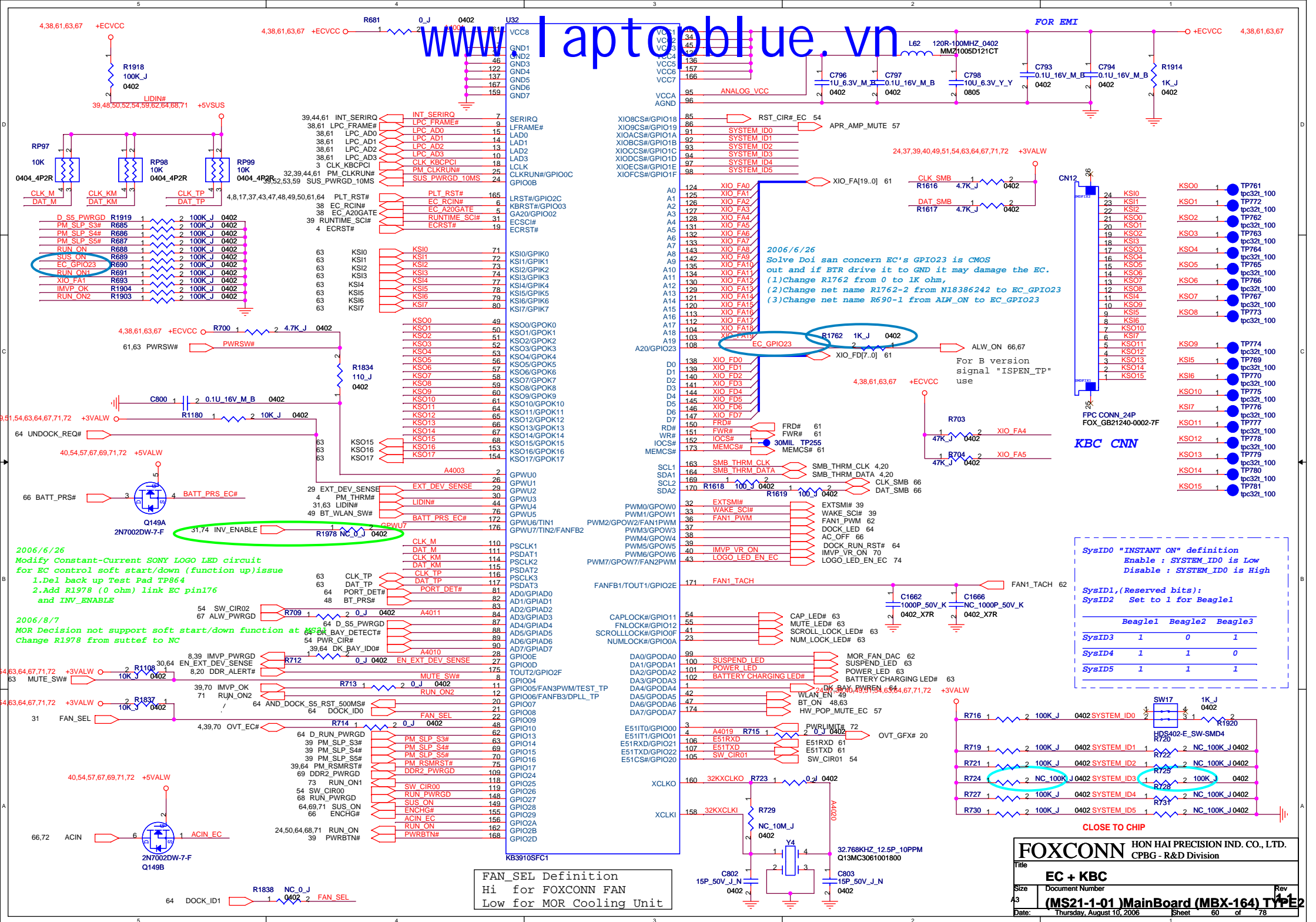


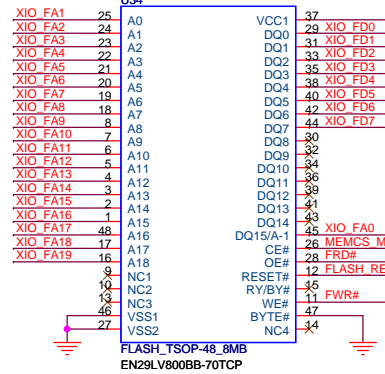
Original EMI back up solution to continue with MS20 (bridge between GND and A_GND)



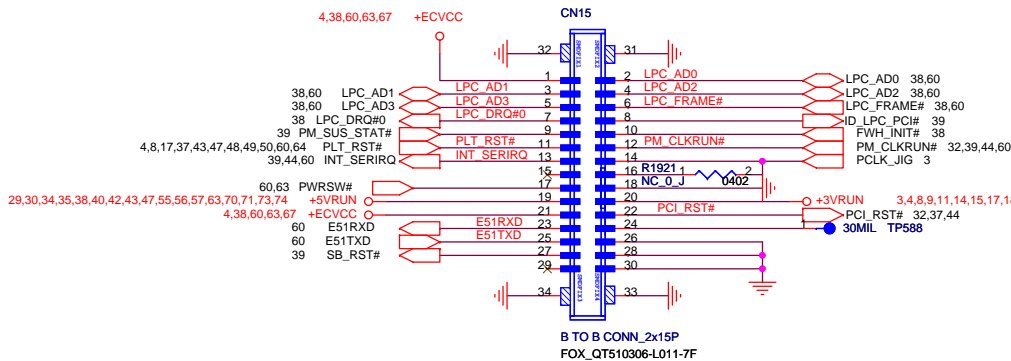
BFT Test Pad



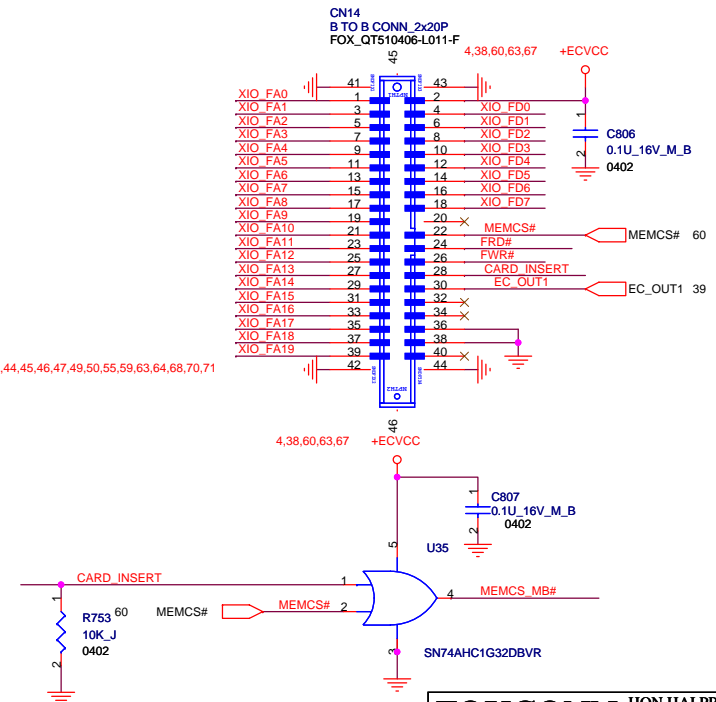


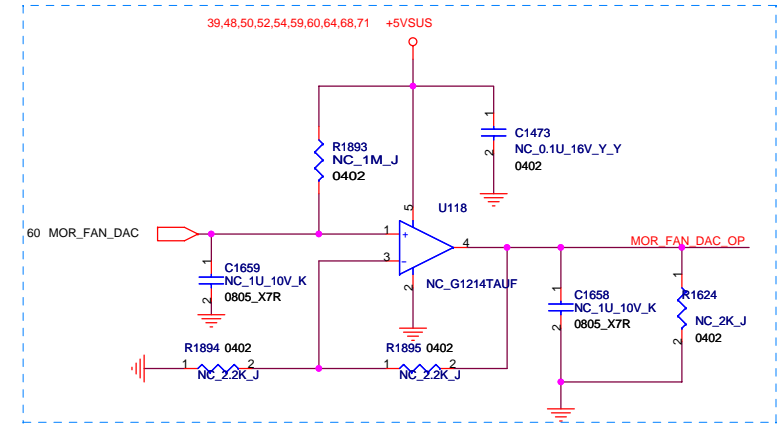
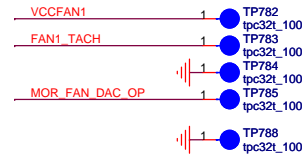
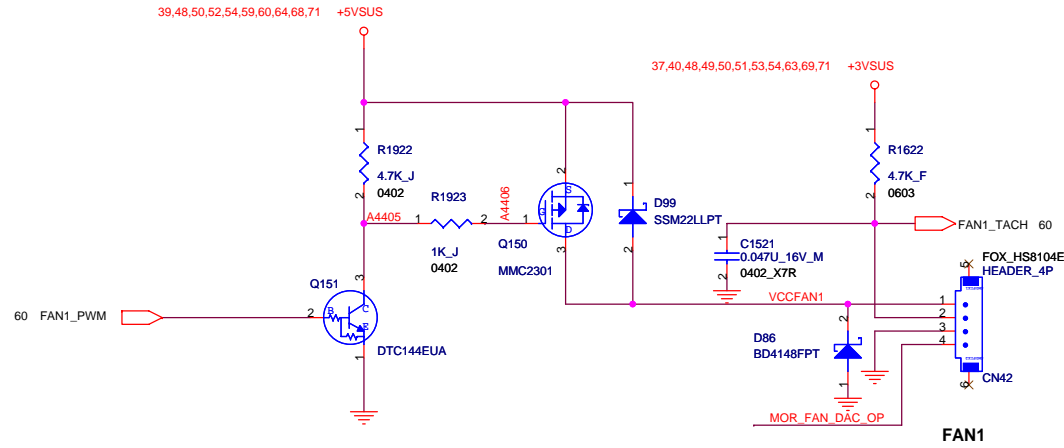


JIG-120

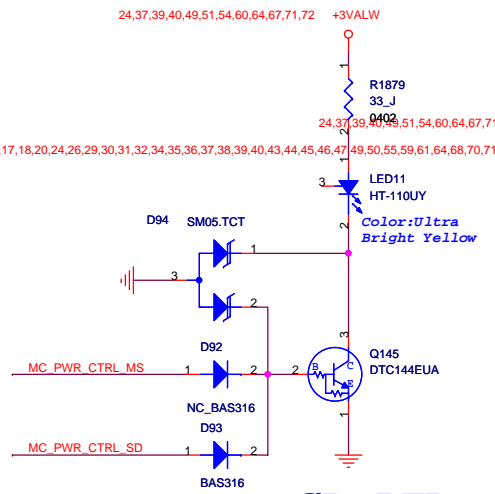


X-BUS

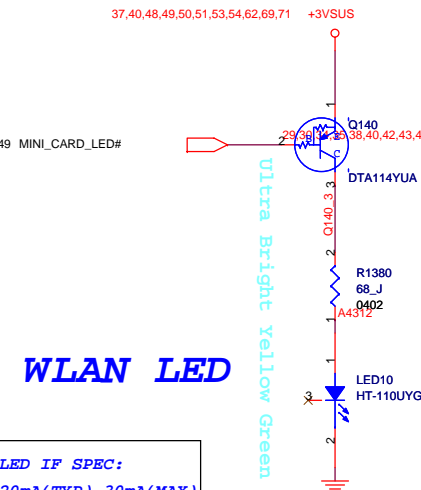
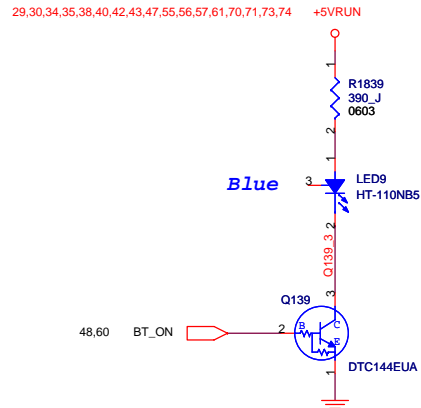




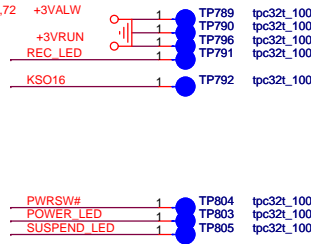
6/28 MOR fan circuit modify to backup
(NC)U118
(NC)R1893
(NC)R1894
(NC)R1895
(NC)R1624
(NC)C1473



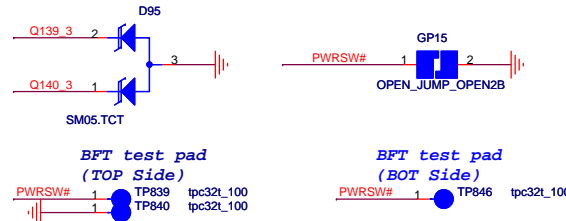
SD LED BLUETOOTH LED



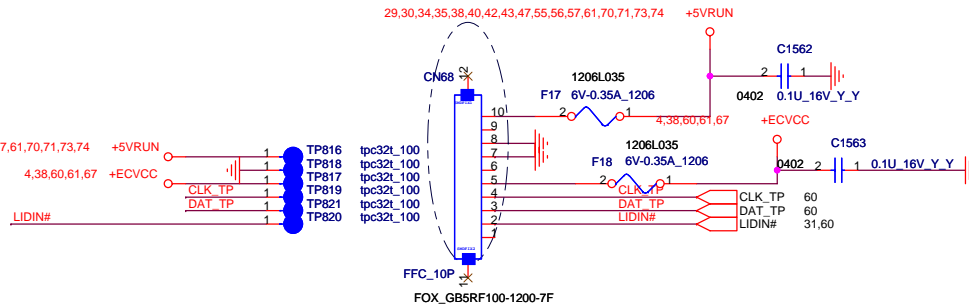
LED IF SPEC:
20mA(TYP), 30mA(MAX)



To Power Button Board Connector

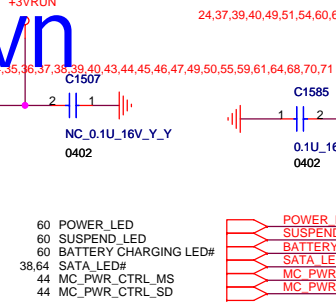


CN68 Change from MOLEX to FOXCONN By kain 0517

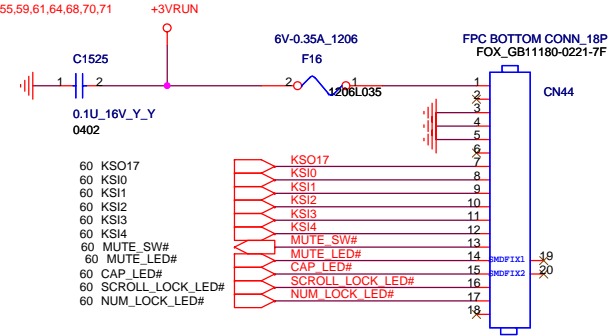
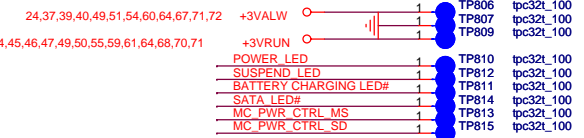


To Touch Pad Board Connector

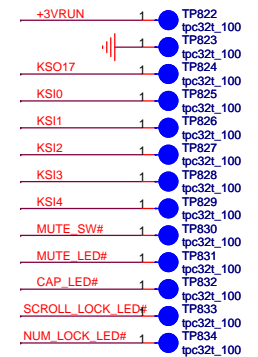
062606: Move Logo Led Circuit module to page 74.

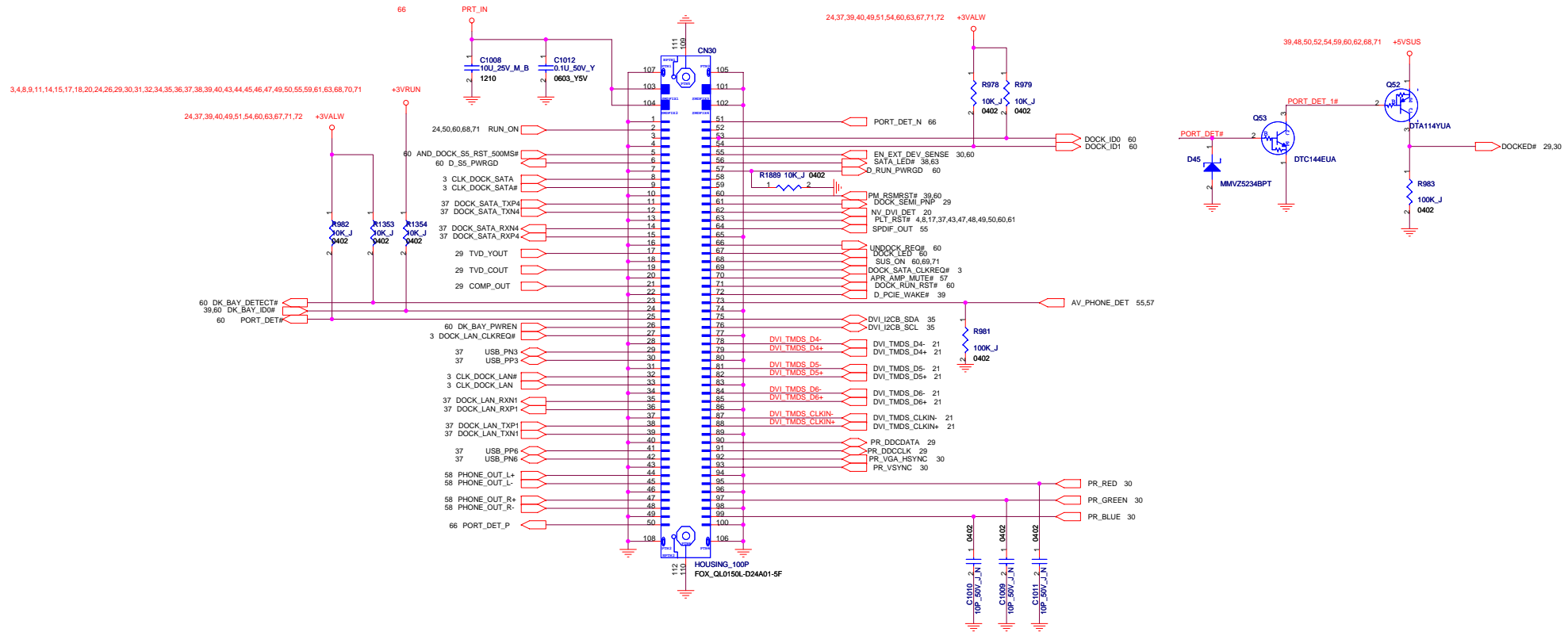


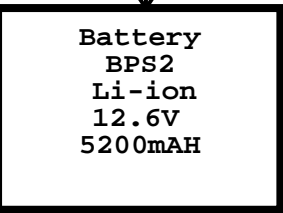
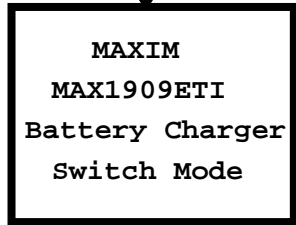
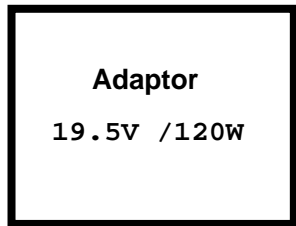
To LED Board Connector



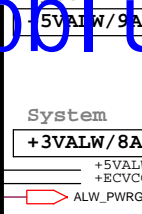
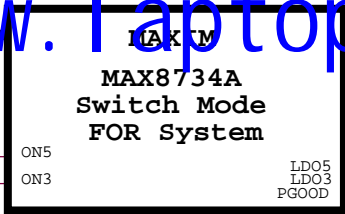
To AV Function Board Connector



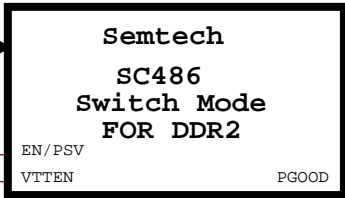
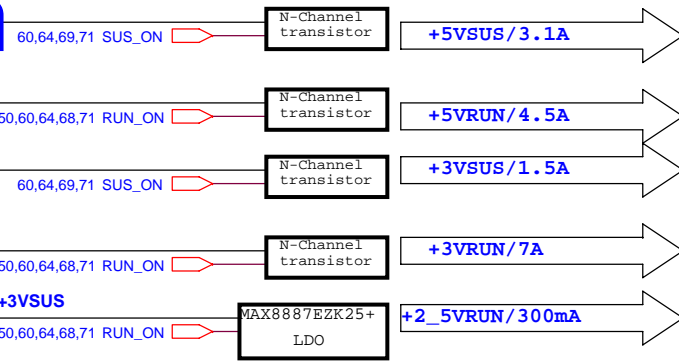
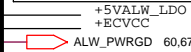




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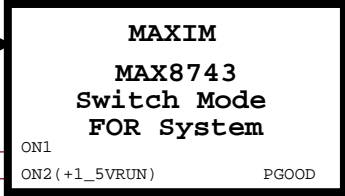
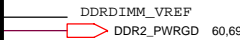


System



+1_8VSUS/15.5A

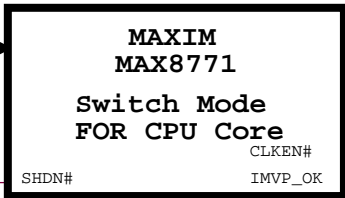
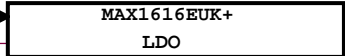
+0_9VSUS/2A



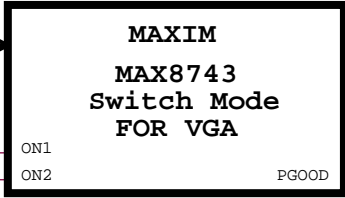
+1_05VRUN/9.5A

+1_5VRUN/7A

+8V For Load switch

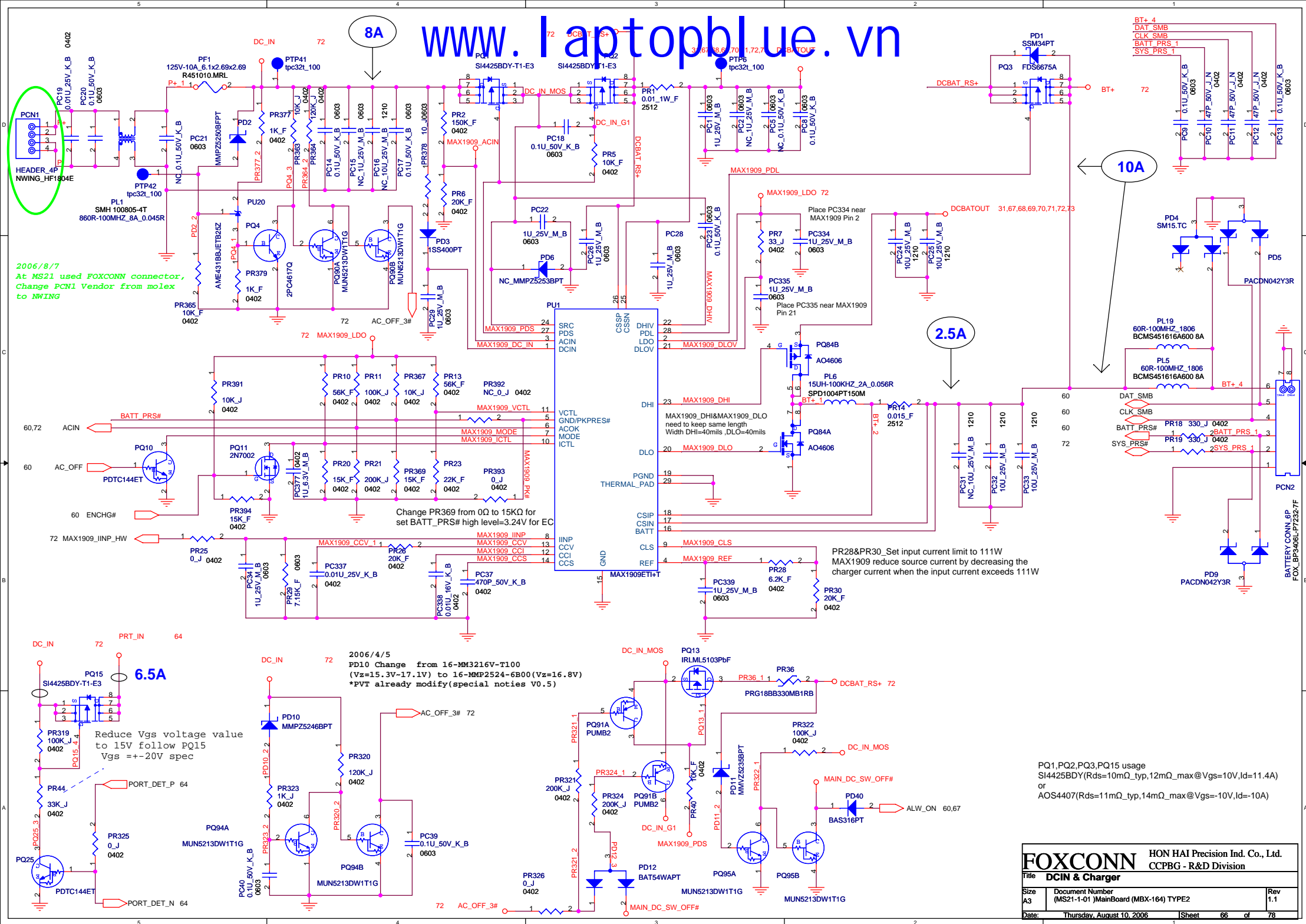


VHORE/44A



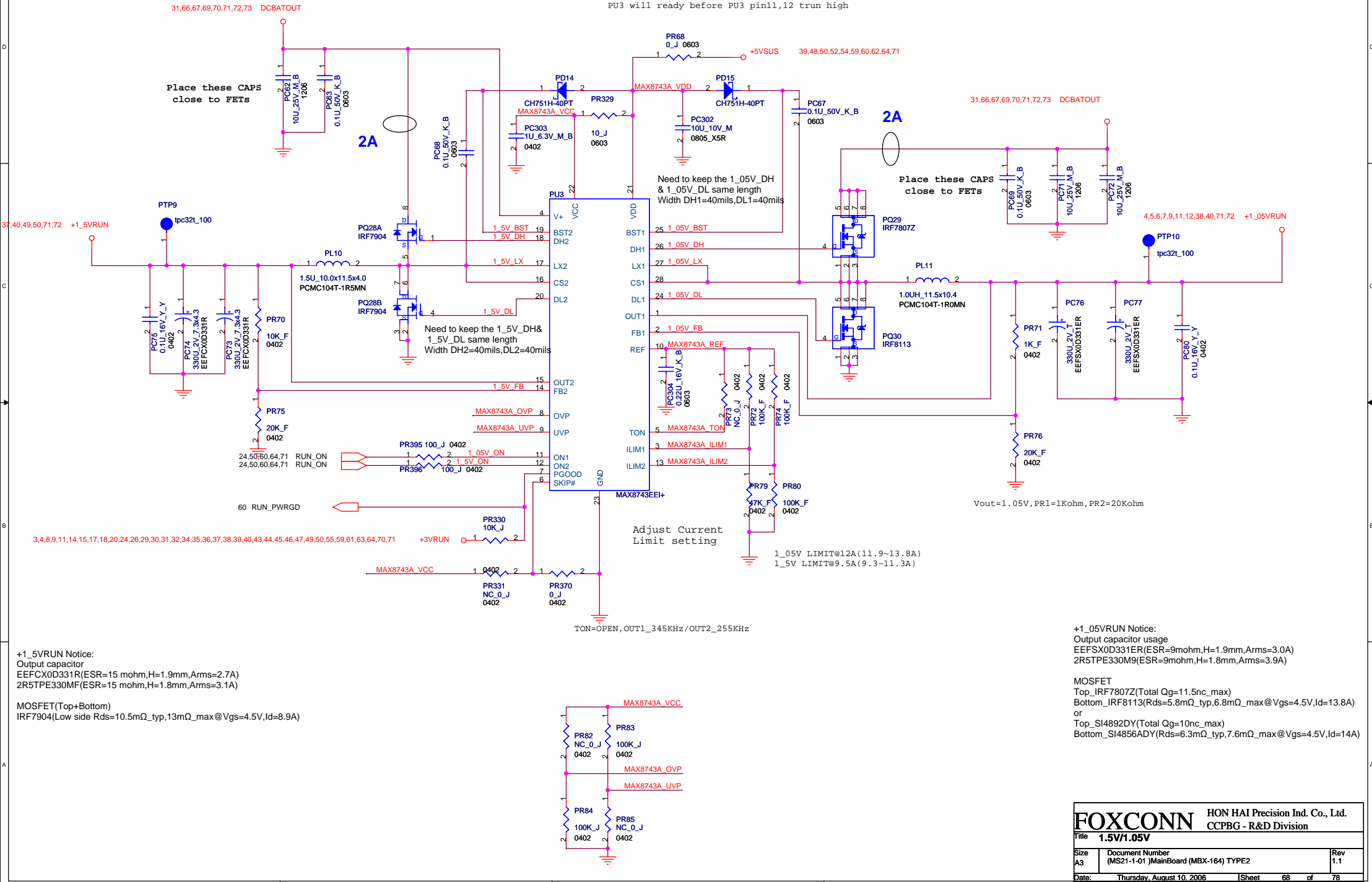
PEX_VDD(1.2V)/2A

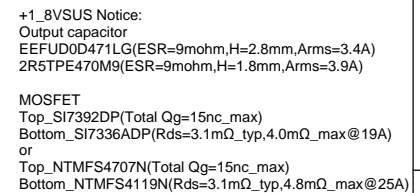
NV_VDD(1.025V)/16.5A



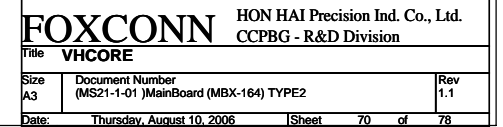
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title DCIN & Charger			
Size A3	Document Number (MS21-1-01) MainBoard (MBX-164) TYPE2		Rev 1.1
Date:	Thursday, August 10, 2006	Sheet	66 of 78

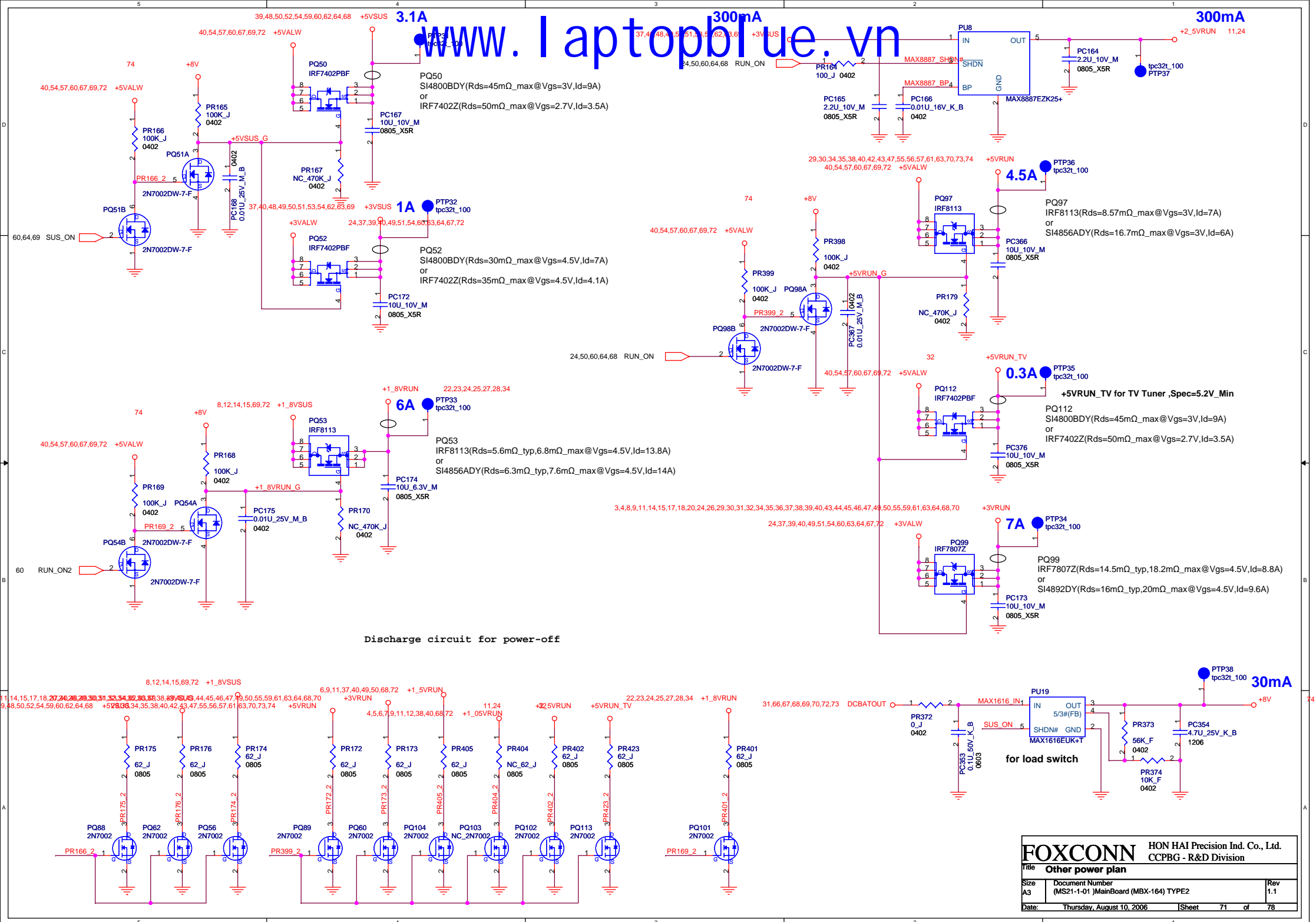
Use +5VSUS for PU3 pin21 to ensure
PU3 will ready before PU3 pin11,12 trun high

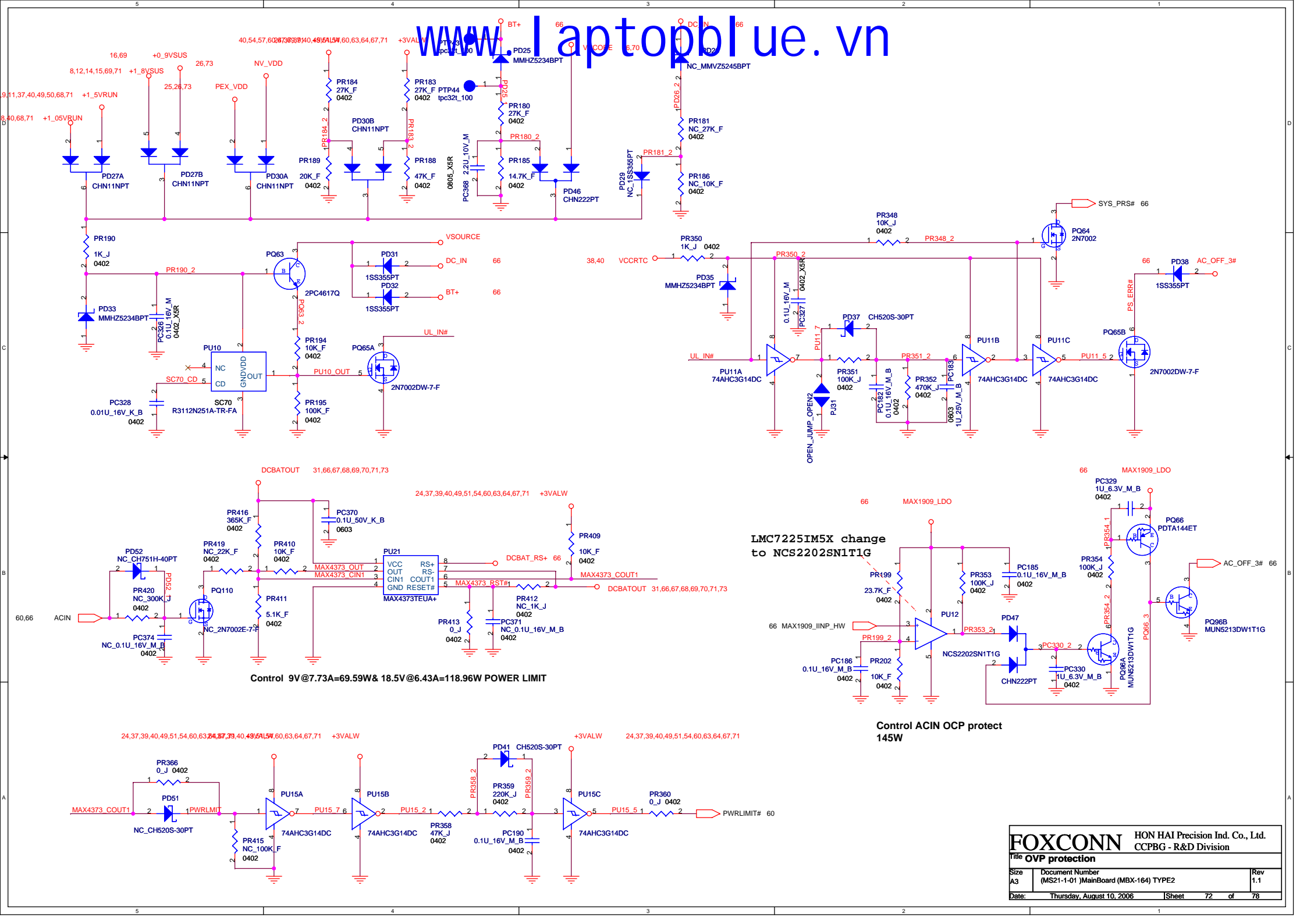




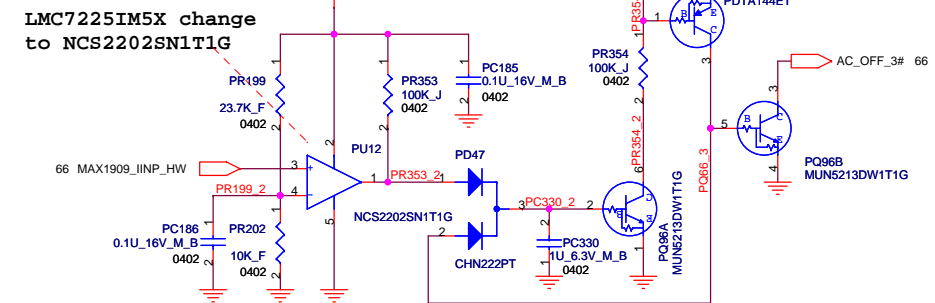
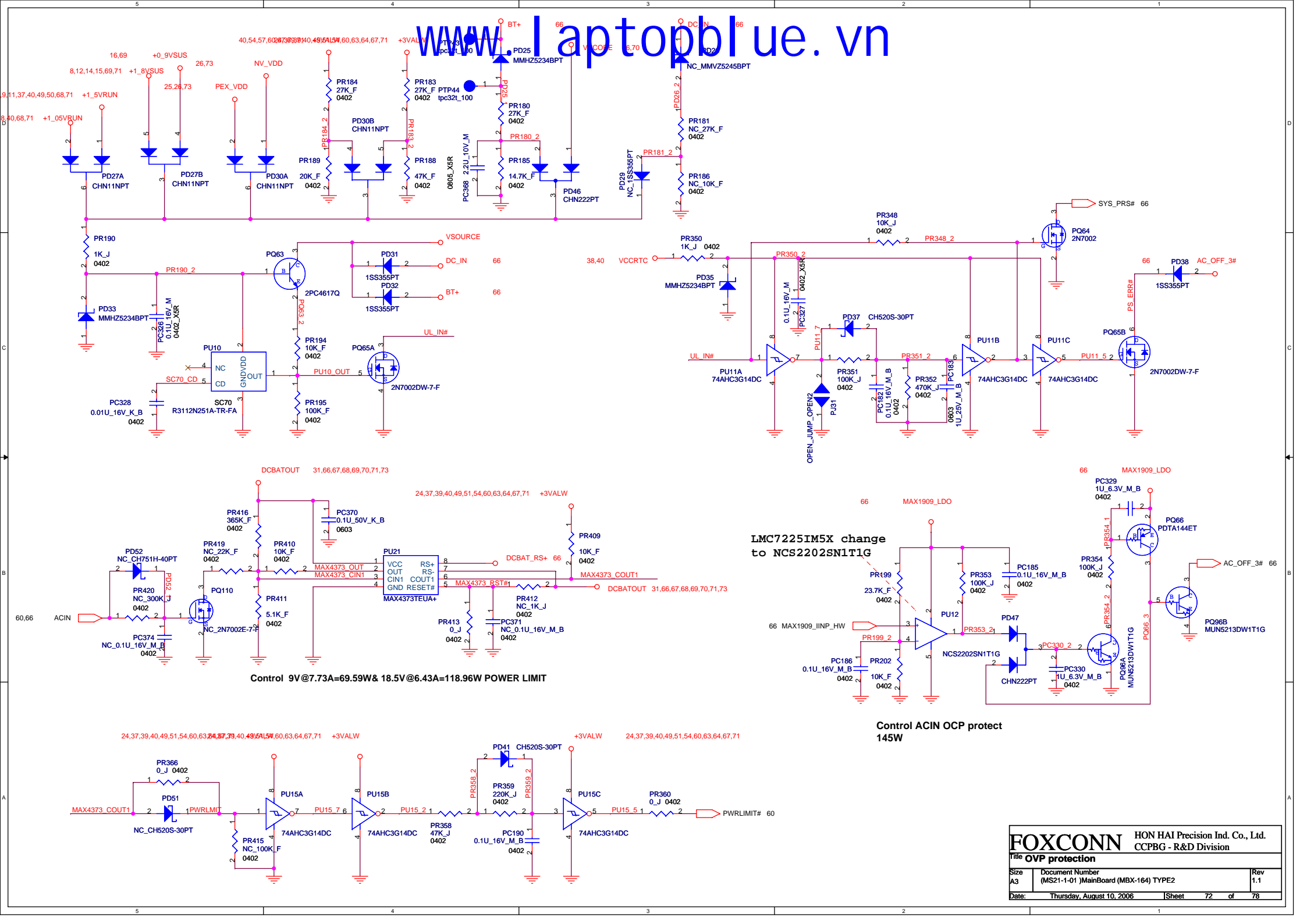
1_8V LIMIT@20A(19.2~24A)







LMC7225IM5X change
to NCS2202SN1T1G

Control ACIN OCP protect
145W

2006/6/26

Modify Constant-Current SONY LOGO LED circuit

for U138 cost issue

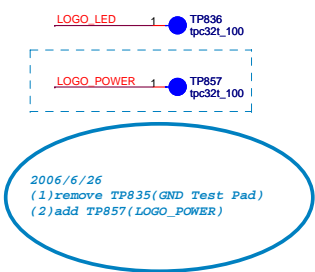
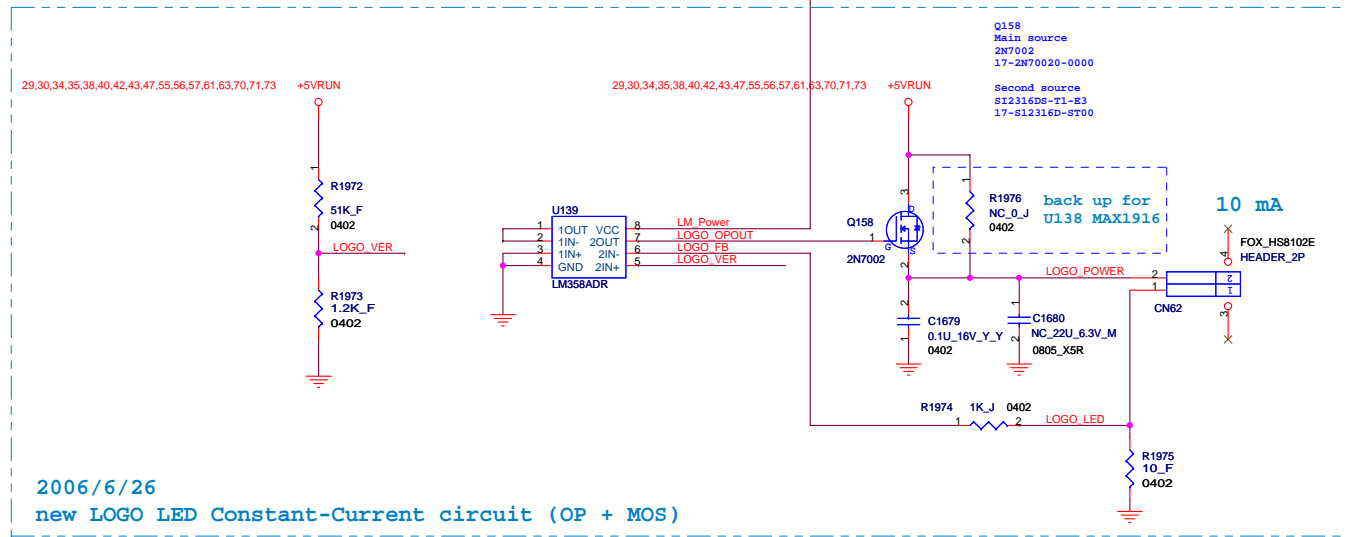
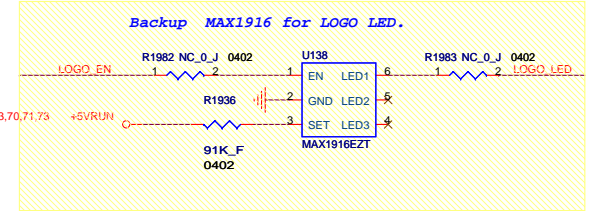
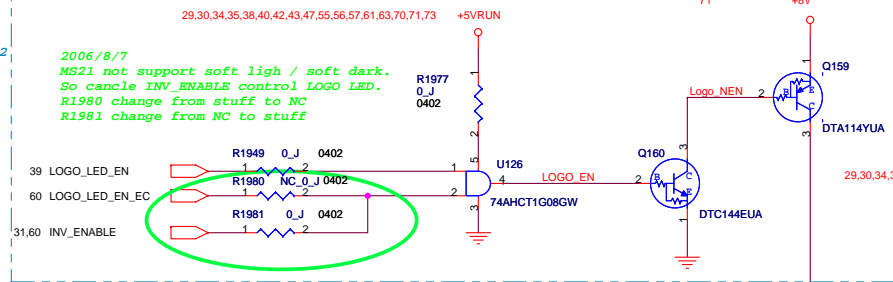
- 1.Back up:U138(MAX1916EZT),R1936 (91K ohm,0402),R1982(0R,NC),R1983(0R,NC)
 - 2.Remove back up solution U139(GMT,G5920TB1UF),C1660(0.1u)
 - 3.Add new Constant-Current circuit (OP + MOS)
- 51K ohm: R1972 ,
1.2K ohm: R1973 ,
1k ohm:R1974 ,
10 ohm: R1975
(NC)0 ohm: R1976(for back up U138 MAX1916)
0.1uF,16V: C1679
(NC)22uF,6.3V: C1680
OP LM358 ADR : U139
N-MOS 2N7002: Q158
N-MOS DTA114YUA:Q159
P-MOS DTC144EUA:Q160

for EC control soft start/down (function up)issue

- 1.Del R1948(back up LOGO_LED_EN_EC to U126 pin1)
- 2.Serial (Back up) R1981 between INV_ENABLE to U126 pin2
- 3.Move net LOGO_LED_EN_EC from R1948 pin1 to R1980 pin1
- 4.Add R1977 between +5VRUN to U126 pin5(VCC)
- 5.Add R1980 between Logo_led_en_ec to U126 pin2

2006/6/26

EC & SB control soft start/down



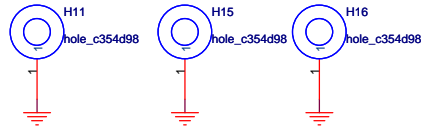
2006/6/26

(Del inverter boost circuit , after change ,the inverter circuit is the same with MS20 MP)
Detail location

10U_25V_M*9pcs(PC380,PC381,PC382,PC383,PC384,PC385,PC386,PC389,PC390),
0.01U_25V_K*1pcs(PC387),1U_25V_M*1pcs(PC388),0.22U_16V_M*1pcs(PC391),
220P_50V_K*1pcs(PC392),SKS30-04AT-G*1pcs(PD53),8UH-100KHZ_2.5A_0.07R*1pcs(PL22),
2N7002*2pcs(PQ9114,PQ116),FDS6680A*1pcs(PQ117),120K_F*1pcs(PR432),
0.03_F*1pcs(PR434)95.3K_F*1pcs(PR435),10K_F*1pcs(PR436),MAX668EUB+T*1pcs(PU22),

HOLE

Type 1



Type 2

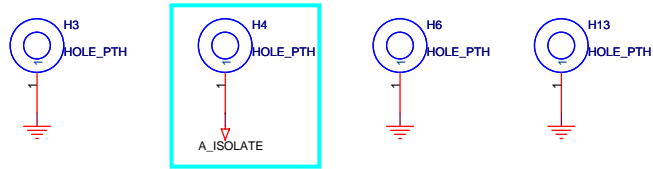
2005/10/24
Remove Screw Hole H2 P/N 1X-HOLE000-0108
because the Hole overlay with CN32 and layout will
modify component screw shipe

Type 3

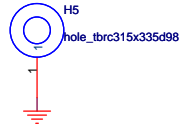
2005/10/24
Remove Screw Hole H1 P/N 1X-HOLE000-0110
because the Hole overlay with CN32 and layout will
modify component screw shipe

2006/5/6
Separet analog ground for digital Noise issue:
Isolate screw hole H4 Change H4 net name from
A_GND to A_ISOLATE

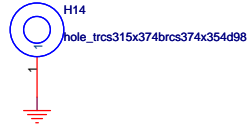
Type 4



Type 5



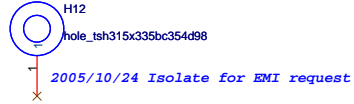
Type 6



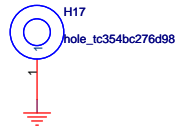
Type 7



Type 8



Type 9



Type CPU



BOSS1
BOSS_3.9x4.0

BOSS2
BOSS_3.9x4.0

BOSS(H=3.1)
MDC
(TOP side)

BOSS3
BOSS_3.9x5.0

BOSS(H=2.8)
Blue Tooth
(BOP side)

BOSS4
BOSS_3.9x5.0

BOSS5
BOSS_3.9x5.0

BOSS(H=2.8)
TV Tuner
(BOP side)

Type NPTH Guide (spherical)HOLD



Type NPTH Guide (oval-shaped)HOLD



MS20 MP to MS21 DVT Change History

(2006/5/23)

- (川) 01.(Page08) Remove R110 for PM_EXTTS#1 back up pull up res.ICH7 (DPRSLPVR)already have internal pull up
- (川) 02.(Page14) Remove backup DIMM thermal senser Change R168 from stuff to NC(basis on MS20 MP ECR)
- (川) 03.(Page15) Remove backup DIMM thermal senser Change R1627 from stuff to NC(basis on MS20 MP ECR)
- (蘭) 04.(Page34) US Silicon Image ATC test HDMI DDC capacitance fail(>50pF)change U128 no stuff Basis on MS20 MP ECR
add back up res.(R1962)no stuff for U128 VCC
- (才) 05.(Page39) Delete U30,R1183,R649 (backup circuit)
- (賣) 06.(Page42) For power droup cause 0.16V voltage loss Issue(1)F7,F8,F19,F20 no stuff(2)Co-layout GP17-GP20 with fuse
- (業) 07.(Page55) Separet analog ground for digital Noise issue
(1)Add bead (L152)before LDO chipand
(2)Change C873 from GND to A_GND
(3)Add C1675 on +5VRUN before L152
- (業) 08.(Page56) Shoei CAP will EOL. CAP24,CAP25(SP CAP) change to Stuff: CAP22,CAP23(Shoei CAP) change to No Stuff
- (業) 09.(Page56) PBSS2515F.115 will EOL ,Q77,Q78,Q143,Q144 change to PBSS2515E.115
- (業) 10.(Page56) Improve the voice of speaker up to 0.94W
(1)Add damping Resistors R1953 on SRIN,R1954 on AMP_SLIN then speaker amp output won't be distorted.
(2)Change R1932 from 6.8K to 5.6K, then amp gain change from 8dB to 10dB.
- (業) 11.(Page57) PBSS2515F.115 will EOL Q89,Q90,Q91,Q92 change to PBSS2515E.115
- (業) 12.(Page59) Improve SNR issue,Add 1uF capacitors close CN64 :C1671,C1672 on USB_VCC2,C1669 on +3VRUN_AUDIO_BD, and C1670 on VDDA .
- (業) 13.(Page59) Separet analog ground for digital Noise issue:
(1)Remove GP3 (Close Jumper)not bridge between GND and A_GND
(2)Backup two jumper resistors for bridge between GND and A_GND
(C1388,C1966 on Screw hole H3,C1957,C1959 on screw hole H5)
(3)Isolate screw hole H4,add 100pF capacitors C1673,C1674 for EMI,Zener diode D100 for ESD
(4)Add jumper resistor for Return patch R1955 close L70(+5VAMP) & R1958 close U41(+5VRUN),& R1960 close codec
- (才) 14.(Page39) Remove back up circuit LVDS GPIO on U29 pinU2(1)Add Test Pad TP890 on GPIO34(2)Del Q126
- (賣) 15.(Page54) Remove back up F6 power source from +3VALW (Del)R1944,R1946
- (青) 16.(Page67) Reserve PC64(10U_25V_M_B 1206) for 1210 size shortage. Change PR57 from 0805 size to 0603 size for 0603 size rated current is also enough.
- (青) 17.(Page70) Add PC375 (0.1uF) to avoid IMVP_OK signal 700mV pulse when power on. Change PC107/PC108 from 2.2U_16V_M to 2.2U_10V_M for 2.2U_16V_M shortage.
- (青) 18.(Page71) Change PC164/PC165 from 2.2U_16V_M to 2.2U_10V_M for 2.2U_16V_M shortage.
- (青) 19.(Page71) Change PC368 from 2.2U_16V_M to 2.2U_10V_M for 2.2U_16V_M shortage. Change PU12 from LMC7225IM5X to NCS2202SN1T1G for LMC7225IM5X shortage.
- (才) 20.(Page60) Modify system ID setting. R725 from stuff change to NC,R726 from NC change to stuff
- (蘭) 21.(Page32) CN66,CN67 Change from MOLEX(IN-0010000-MWG0) to FOXCONN(IN-0010000-F0T0)
- (賣) 22.(Page63) CN68 Change from MOLEX(IN-0010000-MWG0) to FOXCONN(IN-0010000-F0T0)
- (業) 23.(Page57) Add C1676 (4.7 uF/bupass cap) close A_U99 pin8
- (業) 24.(Page58) Add C1677,C1678 (4.7 uF/bupass cap) close A_U101,U102 pin8
- (青) 25.(Page74) Add Inverter Boost Circuit

(2006/5/24)

- (業) 1.(Page55) According to MOR suggest Change Int MIC topology from single end to differential
(1) C1251 change from 33pF 0402 to 1uF 0603
(2) C1252 change from 12pF 0402 to 1uF 0603
(3) C1270 change from 0.1F 0402 to 1uF 0603
(4) Add R1967, R1968 100 ohm 0402
- 2.(Page57) According to MOR suggest Change Int MIC topology from single end to differential
(1) C1231 change from 4.7uF 0805 to 220pF 0402
(2) C1232 change from 1uF 0805 to 4.7uF 0805
(3) C1233 change from 4.7uF 0805 to NC_33pF 0402
(4) C1234 change from 100pF 0402 to NC_33pF 0402
(5) C1237 change from 100pF 0402 to 33pF 0402
(6) R1318 change from 10Kohm 0402 to 5.1Kohm 0402
(7) R1319 change from 1Kohm 0402 to 4.7Kohm 0402
(8) R1320 change from 33ohm 0402 to 100ohm 0402
(9) R1321 change from NC_0ohm 0402 to 4.7Kohm 0402
(10) R1325 change from 47Kohm 0402 to 4.7Kohm 0402
(11) R1326 change from 7.5Kohm 0402 to 2.2Kohm 0402
(12) R1327 change from 100ohm 0402 to 1Kohm 0402
(13) Add R1970, R1971 100 ohm 0402
(14) Add R1969 4.7 Kohm 0402
(15) R1236 change from 4.7u to 1u

(2006/5/26)

- (業) (1) C1230 change from 2200pF to 4700 pF by MOR request

MS21 DVT to MS21 PVT Change History

(2006/6/25)

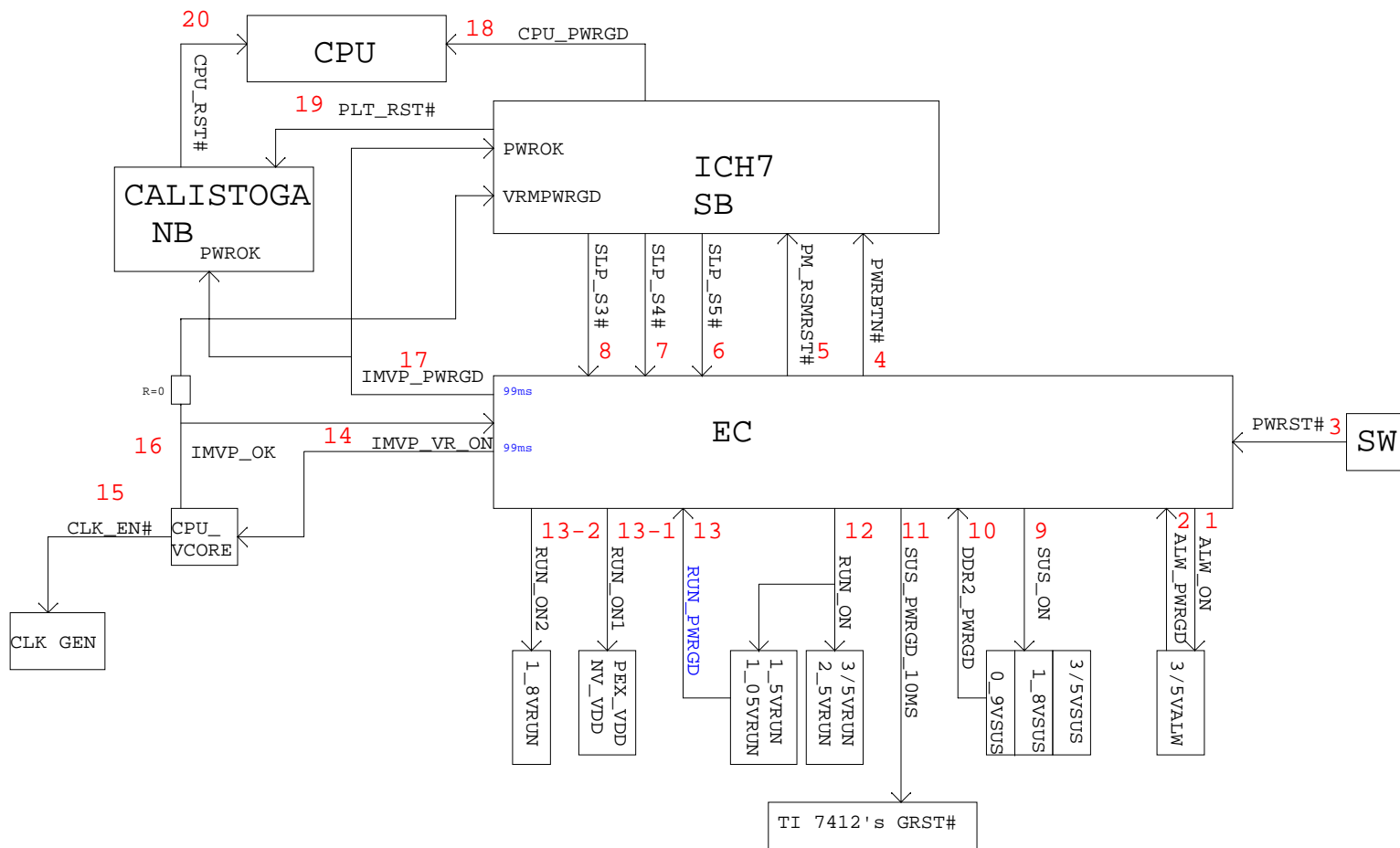
- (才) 01.(Page60) Solve Doi san concern EC's GPIO23 is CMOS out and if BTR drive it to GND it may damage the EC.
(1)Change R1762 from 0 to 1K ohm,
(2)Change net name R1762-2 from N18386242 to EC_GPIO23
(3)Change net name R690-1 from ALW_ON to EC_GPIO23
- (蘭) 02.(Page31) Del inverter boost circuit , after change ,the inverter circuit is the same with MS20 MP
(1)Delete PR426&PR427
(2)change C604-1,C1557-1,C1558-1,CN49 pin1,pin2 net name INVERTER_VCC to net DCBATOUT.
- (賣) 03.(Page74) Del inverter boost circuit , after change ,the inverter circuit is the same with MS20 MP
Delete 10U_25V_M*1pcs(PC380,PC381,PC382,PC383,PC384,PC385,PC386,PC389,PC390),
0.01U_25V_K*1pcs (PC387),1U_25V_M*1pcs(PC388),0.22U_16V_M*1pcs(PC391),
220P_50V_K*1pcs(PC392),SKS30-04AT-G*1pcs(PD53),8UH-100KH2_2.5A_0.07R*1pcs(PL22),
2N7002*2pcs(PQ114,PQ116),FDS6680A*1pcs(PQ117),120K_F*1pcs(PR432),
0.03_F*1pcs(PR434)95.3K_F*1pcs(PR435),10K_F*1pcs(PR436),MAX668EUB+T*1pcs(PU22),
100K_u*1pcs (PR428) 100K_u*1pcs (PR429)
- (青) 04.(Page67)Change PR53&PR55 from 100_J to 0_J by Mor side suggestions
Original PR53&PR55(100ohm) is used as current limit.But now we have added series 1K ohm,
(Page 60, change R1762 from 0 ohm to 1K ohm) So we need not 100ohm resistor for curret limit
- (業) 05.(Page56) Modify internal speaker AMP gain setting,change R1953/R1954 from 4.7K (AMP output 1.12W) to 5.1Kohm(AMP output0.98W) to fit in speaker (1.0W)spec.
- (業) 06.(Page57) Modify internal MIC AMP gain setting,change R1318 from 5.1K to 5.9K ohm, To lead TYPE2 board gain (differential type MIC)the same with TYPE1 board single end MIC) (Gain=9.2)
- (才) 07.(Page60) Modify Constant-Current SONY LOGO LED circuit for EC control soft start/down (function up)issue
(1).Del back up Test Pad TP864
(2).Add R1978 (0 ohm) link EC pin176 and INV_ENABLE
- (賣) 08.(Page74) Modify Constant-Current SONY LOGO LED circuit
A.for U138 cost issue
1.Back up:U138(MAXI1916EZT),R1936 (91K ohm,0402),R1982(0R,NC),R1983(0R,NC)
2.Remove back up solution U139(GMT,G5920TBIUF),C1660(0.1u)
3.Add new Constant-Current differential circuit (OP + MOS)
51K ohm: R1972 ,
1.2K ohm: R1973 ,
1k ohm:R1974
10 ohm: R1975
(NC)0 ohm: R1976(for back up U138 MAXI1916)
0.1uF,16V: C1679
(NC)22uF,6.3V: C1680
OP L4358 ADR : U139
N-MOS 2N7002: Q158
N-MOS DTAL14YUA:Q159
P-MOS DTCL144EUA:Q160

B.for EC control soft start/down (function up)issue
1.Del R1948(back up LOGO_LED_EN_EC to U126 pin1)
2.Serial (Back up) R1981 between INV_ENABLE to U126 pin2
3.Move net LOGO_LED_EN_EC from R1948 pin1 to R1980 pin1
4.Add R1977 between +5VRUN to U126 pin5(VCC)
5.Add R1980 between Logo_led_en_ec to U126 pin2
- (賣) 09.(Page 42) Delete SATA HDD Fuse backup circuit
(1)Remove F7,F8,F19,F20 Pad
(2)Remove GP17-GP18 open gap
- (才) 10. (Page 62) MOR fan circuit modify to backup
(NC)U118 (NC)R1893
(NC)R1624 (NC)C1473
(NC)R1894 (NC)R1895

MS21 PVT to MS21 MP Change History

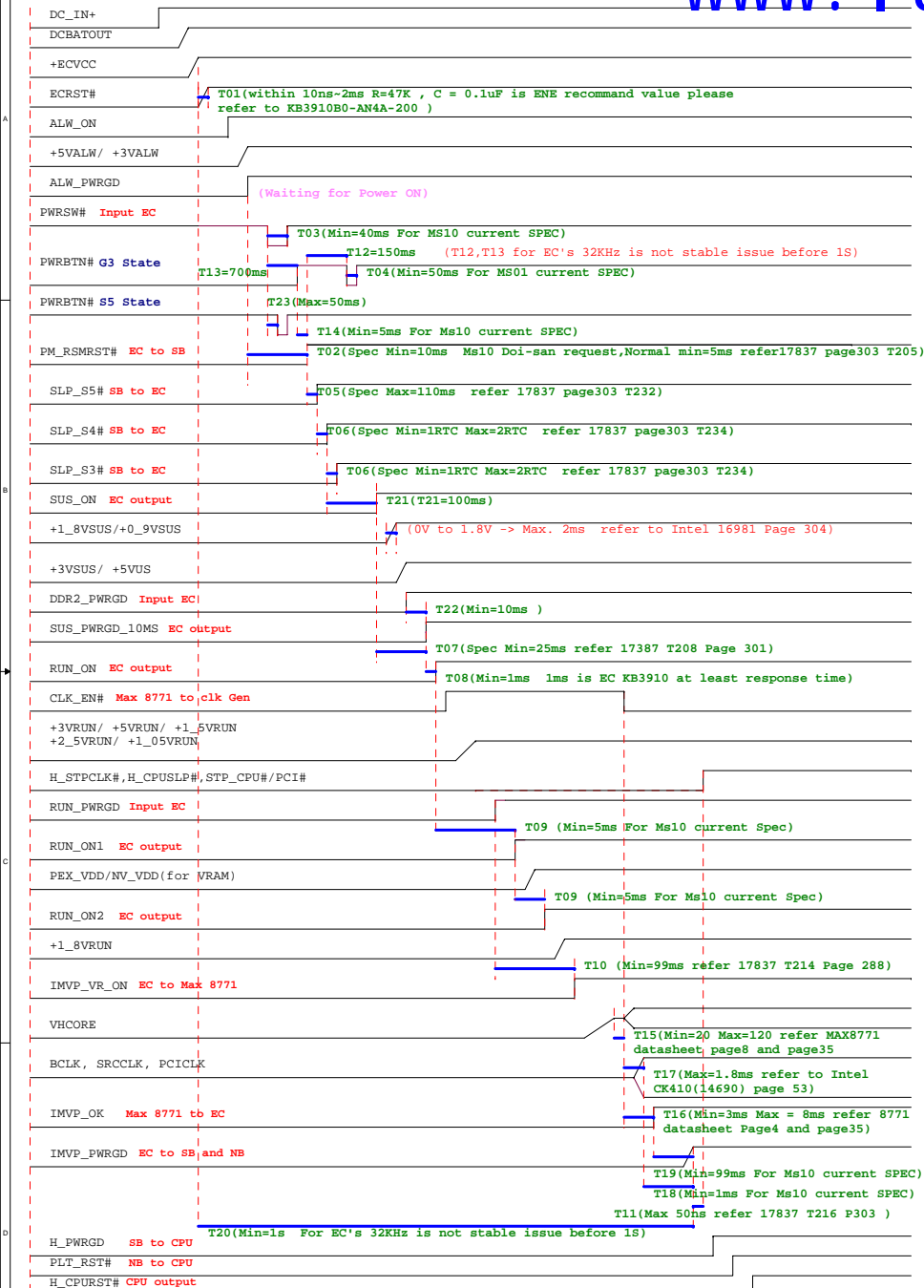
- (賣) 01.(Page74) MS21 not support soft ligh / soft dark. So cancle INV_ENABLE control LOGO LED.
R1980 change from stuff to NC
R1981 change from NC to stuff
- (才) 02.(Page60) MS21 not support soft ligh / soft dark. So cancle INV_ENABLE control LOGO LED.
R1978 Change from stuff to NC
- (業) 03.(Page57) Change C1676 from stuff to NC for MOR suggestion Cost down request.
- (青) 04.(Page66) At MS21 PCN1 used FOXCONN connector, Change PCN1 Vendor from molex to NWING
- (良) 05.(Page29) Change D60,D61,D81 Value from NV to Normal
- (良) 06.(Page20) Change Y2 Value from Normal to NV

MS21 Power On Sequence Block Diagram

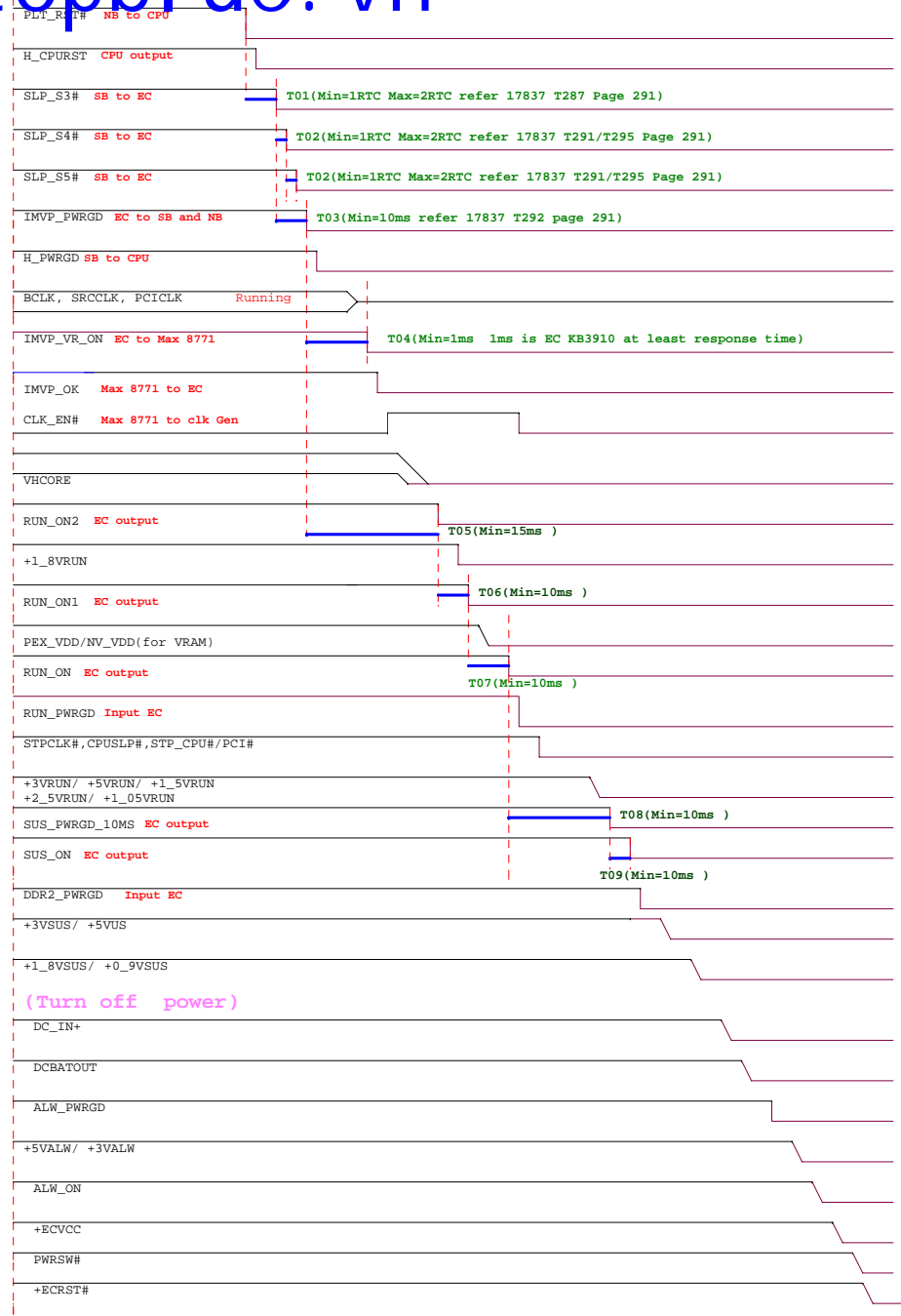


Power On/Off Sequence Specification

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T01	T02	T03	T04	T05	T06	T07	T08	T09	T10	T11	
within 10ns-2ms	Min. 10ms	Min. 40ms	Min. 50ms	Max. 110ms	1 - 2 RTCLK	Min. 25ms	Min. 1ms	Min. 10ms	Min. 99ms	Max. 50ms	
T12	T13	T14	T15	T16	T17	T18	T19	T20	T21	T22	T23
Min. 150ms	Min. 700ms	Min. 5ms	Min: 20us Max: 120us	Min: 3ms Max: 8ms	1.8ms	Max. 1ms	Min. 99ms	Min. 1s	100ms	Min. 10ms	Max. 50ms



T01	T02	T03	T04	T05	T06	T07	T08	T09
1 - 2 RTCLK	1 - 2 RTCLK	Min. 10ms	Min. 1ms	Min. 15ms	Min. 10ms	Min. 10ms	Min. 10ms	Min. 10ms