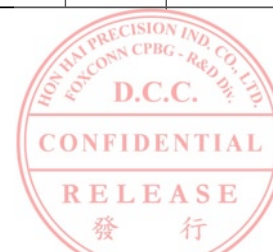


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12	VGA(nVIDIA NV44M) 2/5	0.2	050523	37	VRAM 2.5V/1.25V	0.2	050523
13	VGA(nVIDIA NV44M) 3/5	0.2	050523	38	STEP-UP	0.2	050523
14	VGA(nVIDIA NV44M) 4/5	0.2	050523	39	other power plan	0.2	050523
15	VGA(nVIDIA NV44M) 5/5	0.2	050523	40	OVP protection	0.2	050523
16	NV44M(DDR F_A B_1)	0.2	050523	41	History(1)	0.2	050523
17	DDR(II)SO-DIMM	0.2	050523	42	History(2)	0.2	050523
18	DDR(II)Termination	0.2	050523	43	Revision History	0.2	050523
19	ICH6-M( CPU,PCI,IDE )	0.2	050523				
20	ICH6-M( USB,HUB,LPC )	0.2	050523				
21	ICH6-M( POWER&GND )	0.2	050523				
22	IDE (HDD&CD_ROM)	0.2	050523				
23	USB2.0/OIDE/FAN/DOCKING	0.2	050523				
24	PCI7420B(PCMCIA)	0.2	050523				
25	PCI7420B(iLink,MS)/MDC	0.2	050523				



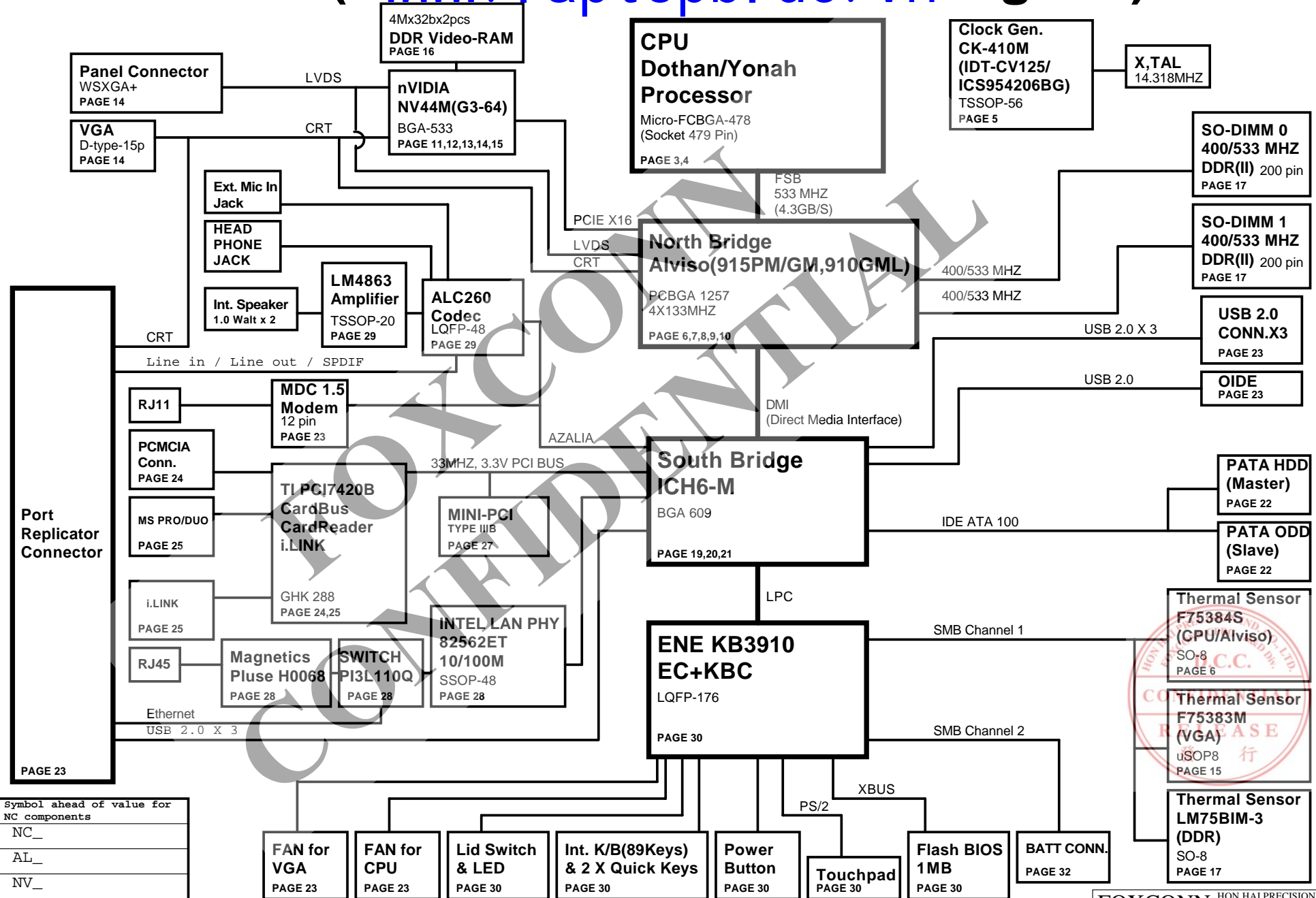
P. Leader	Appr. by	Check by	Design by
			Alex

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Title MS03 DVT_M/B			
Size	Document Number MS03-1-01	Rev 0.2	
Date:	Monday, May 23, 2005	Sheet	1 of 43

Project Code & Schematics Subject:	MS03 M/B-FUBAI	PCB P/N:	1P-0055100-80SB
Project Code & Schematics Subject:	MS03 M/B-HANNSTAR	PCB P/N:	1P-0055500-80SB
Project Code & Schematics Subject:	MS03 M/B-NAN YA	PCB P/N:	1P-0055200-80SB

# MS03(915PM/GM+Gfx Block Diagram)

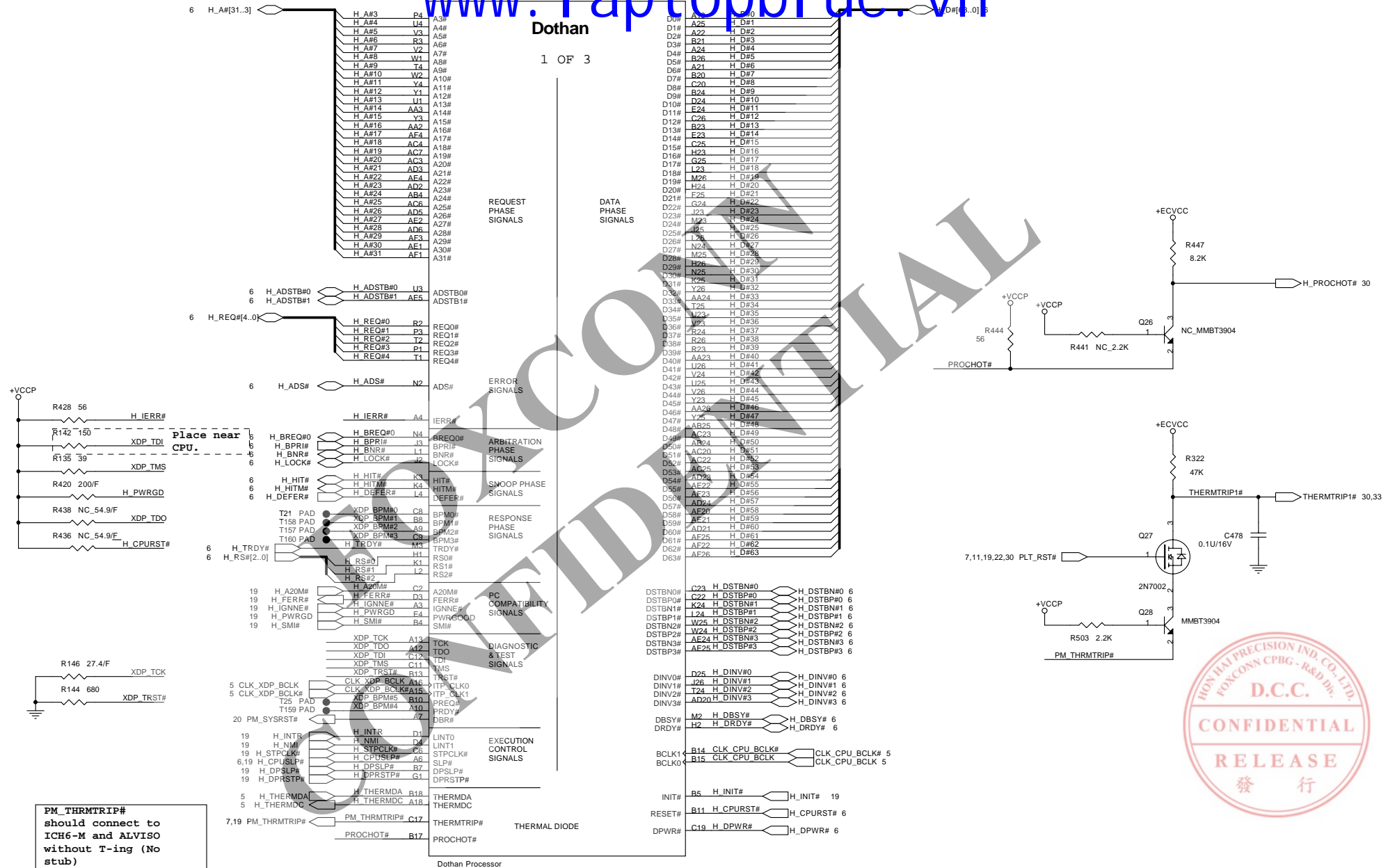
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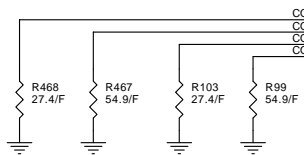


BOM configuration

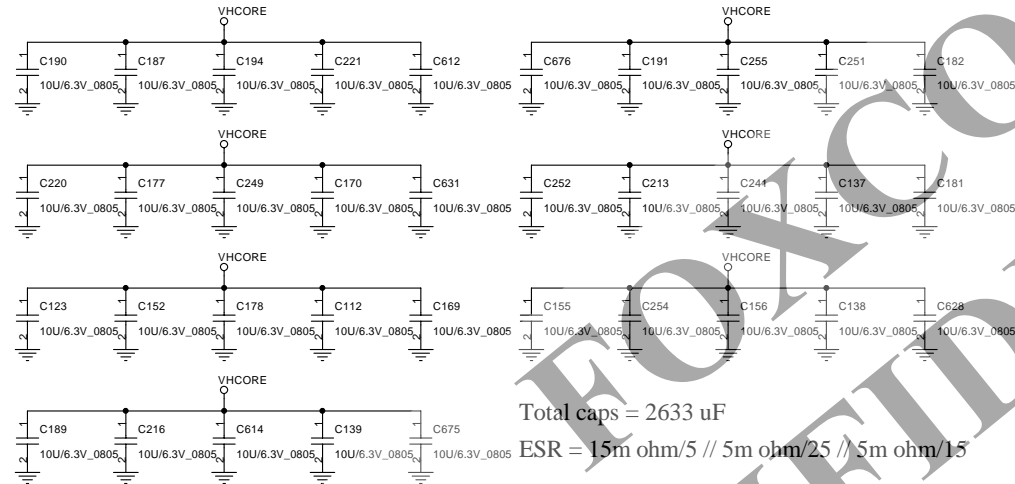
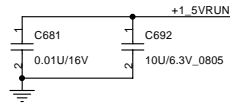
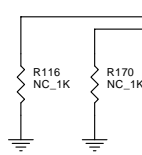
Dothan

1 OF 3

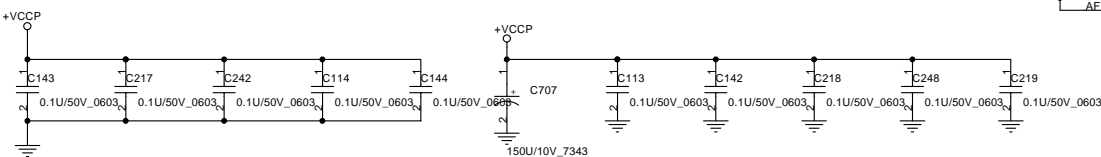




Place pulldown resistors  
within 0.5" of COMP pins



Total caps = 2633 uF  
ESR = 15m ohm/5 // 5m ohm/25 // 5m ohm/15



COMP0	P26
COMP1	P26
COMP2	AB2
COMP3	AB1

H_GTLREF	AD26
TEST1	C5
TEST2	F23

T155PAD	TP_CPU_NC1	B2
T11 PAD	TP_NC_2	C3
T153PAD	TP_NC_3	AF7
T152PAD	TP_NC_4	AC1
T169 PAD	TP_NC_5	F26

T167 PAD	TP_VCCA3	AC26
T3 PAD	TP_VCCA2	AB1
T154 PAD	TP_VCCA1	F26

+1.5VRUN

VHCORE

D6 VCC00

D8 VCC01

D18 VCC02

D22 VCC03

E5 VCC04

E7 VCC05

E9 VCC06

E17 VCC07

E19 VCC08

E21 VCC09

F6 VCC10

F8 VCC11

F18 VCC12

F20 VCC13

F22 VCC14

G1 VCC15

G2 VCC16

H6 VCC17

H22 VCC18

J5 VCC19

K21 VCC20

K22 VCC21

U5 VCC22

V6 VCC23

W21 VCC24

W5 VCC25

W21 VCC26

W21 VCC27

Y2 VCC28

AA5 VCC29

AA7 VCC30

AA9 VCC31

AA11 VCC32

AA13 VCC33

AA15 VCC34

AA17 VCC35

AA19 VCC36

AA21 VCC37

AB6 VCC38

AB8 VCC39

AB10 VCC40

AB12 VCC41

AB14 VCC42

AB16 VCC43

AB18 VCC44

AB20 VCC45

AB22 VCC46

AC9 VCC47

AC11 VCC48

AC13 VCC49

AC15 VCC50

AC17 VCC51

AD8 VCC52

AD10 VCC53

AD12 VCC54

AD14 VCC55

AD16 VCC56

AD18 VCC57

AE9 VCC58

AE11 VCC59

AE13 VCC60

AE15 VCC61

AE17 VCC62

AE19 VCC63

AF8 VCC64

AF10 VCC65

AF12 VCC66

AF14 VCC67

AF16 VCC68

AF18 VCC69

AF18 VCC70

AF18 VCC71

Dothan  
2 OF 3

POWER,  
GROUND,  
RESERVED  
SIGNALS

VHCORE

D6 VCC00

D8 VCC01

D18 VCC02

D22 VCC03

E5 VCC04

E7 VCC05

E9 VCC06

E17 VCC07

E19 VCC08

E21 VCC09

F6 VCC10

F8 VCC11

F18 VCC12

F20 VCC13

F22 VCC14

G1 VCC15

G2 VCC16

H6 VCC17

H22 VCC18

J5 VCC19

K21 VCC20

K22 VCC21

U5 VCC22

V6 VCC23

W21 VCC24

W5 VCC25

W21 VCC26

W21 VCC27

Y2 VCC28

AA5 VCC29

AA7 VCC30

AA9 VCC31

AA11 VCC32

AA13 VCC33

AA15 VCC34

AA17 VCC35

AA19 VCC36

AA21 VCC37

AB6 VCC38

AB8 VCC39

AB10 VCC40

AB12 VCC41

AB14 VCC42

AB16 VCC43

AB18 VCC44

AB20 VCC45

AB22 VCC46

AC9 VCC47

AC11 VCC48

AC13 VCC49

AC15 VCC50

AC17 VCC51

AD8 VCC52

AD10 VCC53

AD12 VCC54

AD14 VCC55

AD16 VCC56

AD18 VCC57

AE9 VCC58

AE11 VCC59

AE13 VCC60

AE15 VCC61

AE17 VCC62

AE19 VCC63

AF8 VCC64

AF10 VCC65

AF12 VCC66

AF14 VCC67

AF16 VCC68

AF18 VCC69

AF18 VCC70

AF18 VCC71

Dothan Processor

VSS00	A2
VSS01	A5
VSS02	A8
VSS03	A11
VSS04	A14
VSS05	A17
VSS06	A20
VSS07	A23
VSS08	A26
VSS09	B3
VSS10	B6
VSS11	B9
VSS12	B12
VSS13	B15
VSS14	B18
VSS15	B21
VSS16	B24
VSS17	B27
VSS18	C1
VSS19	C4
VSS20	C7
VSS21	C10
VSS22	C13
VSS23	C16
VSS24	C19
VSS25	C22
VSS26	C25
VSS27	C28
VSS28	D1
VSS29	D4
VSS30	D7
VSS31	D10
VSS32	D13
VSS33	D16
VSS34	D19
VSS35	D22
VSS36	D25
VSS37	D28
VSS38	E3
VSS39	E6
VSS40	E9
VSS41	E12
VSS42	E15
VSS43	E18
VSS44	E21
VSS45	E24
VSS46	E27
VSS47	E30
VSS48	E33
VSS49	E36
VSS50	E39
VSS51	F1
VSS52	F4
VSS53	F7
VSS54	F10
VSS55	F13
VSS56	F16
VSS57	F19
VSS58	F22
VSS59	F25
VSS60	F28
VSS61	G2
VSS62	G5
VSS63	G8
VSS64	G11
VSS65	G14
VSS66	G17
VSS67	G20
VSS68	G23
VSS69	G26
VSS70	H3
VSS71	H6
VSS72	H9
VSS73	H12
VSS74	H15
VSS75	H18
VSS76	H21
VSS77	H24
VSS78	H27
VSS79	H30
VSS80	I1
VSS81	I4
VSS82	I7
VSS83	I10
VSS84	I13
VSS85	I16
VSS86	I19
VSS87	I22
VSS88	I25
VSS89	J1
VSS90	J4
VSS91	J7
VSS92	J10
VSS93	J13
VSS94	J16
VSS95	J19
VSS96	J22
VSS97	J25
VSS98	K1
VSS99	K4

H_VID0	H_VID0R88	0	E2
H_VID1	H_VID1R87	0	E3
H_VID2	H_VID2R86	0	E4
H_VID3	H_VID3R85	0	E5
H_VID4	H_VID4R84	0	E6
H_VID5	H_VID5R83	0	E7

Same Length

R633 NC\_54.9/F

R634 NC\_54.9/F

5.7 CPU\_BSEL0

5.7 CPU\_BSEL1

R440 0

PSI#

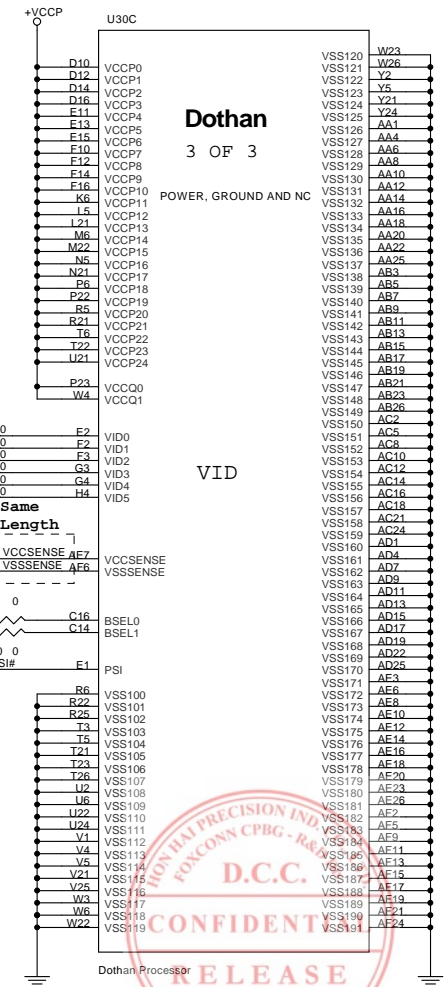
35

PSI#

E1

PSI

R6

 R22 | VSS100 || R22 | VSS101 |
R22	VSS102
R22	VSS103
R22	VSS104
R22	VSS105
R22	VSS106
R22	VSS107
R22	VSS108
R22	VSS109
R22	VSS110
R22	VSS111
R22	VSS112
R22	VSS113
R22	VSS114
R22	VSS115
R22	VSS116
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R22	VSS185
R22	VSS186
R22	VSS187
R22	VSS188
R22	VSS189
R22	VSS190
R22	VSS191


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MS03 DVT\_M/B

Document Number

MS03-1-01

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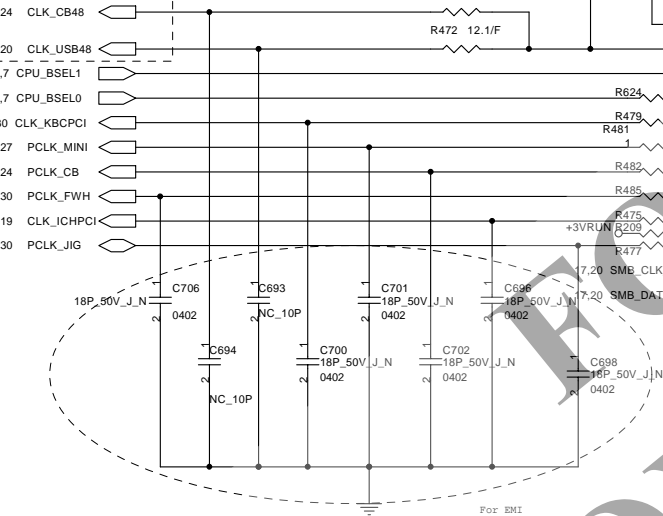
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Rev 0.2

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

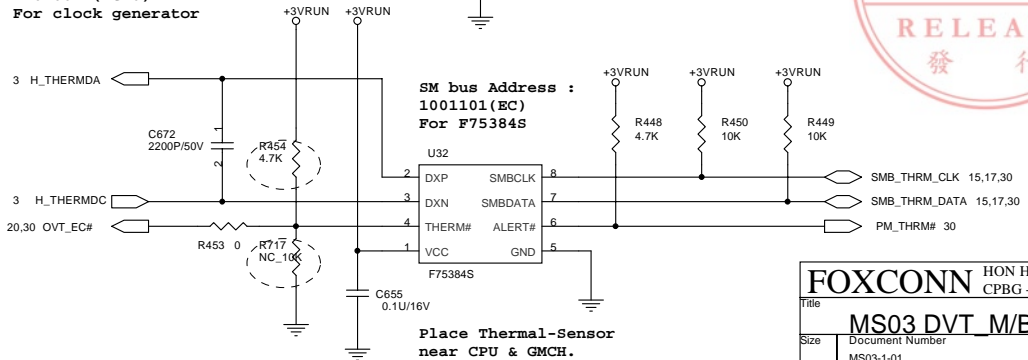
Placed within  
500mils of Y1

Length as short  
as possible.



CONFIDENTIAL

IDTCV125 / ICS954206BG  
SM bus Address :  
1101001 (ICH6)  
For clock generator



SM bus Address :  
1001101 (EC)  
For F75384S

Place Thermal-Sensor  
near CPU & GMCH.

CLK\_XDP\_BCLK# R460 NC 49.9/F  
CLK\_XDP\_BCLK# R458 NC 49.9/F  
CLK\_MCH\_BCLK# R465 49.9/F  
CLK\_MCH\_BCLK# R463 49.9/F  
CLK\_CPU\_BCLK# R471 49.9/F  
CLK\_CPU\_BCLK# R469 49.9/F  
CLK\_MCH\_3GPLL R457 49.9/F  
CLK\_MCH\_3GPLL# R455 49.9/F

CLK\_PCIE\_ICH# R459 49.9/F  
CLK\_PCIE\_ICH# R456 49.9/F

Alviso Chip  
HOST

CPU

CLK\_PCIE\_PEG# R462 NV 49.9/F  
CLK\_PCIE\_PEG# R461 NV 49.9/F  
DREFCLK# R470 AL 49.9/F  
DREFSSCLK# R466 NV 0  
DREFSSCLK# R185 AL 49.9/F  
DREFSSCLK# R183 NV 0  
DREFCLK# R631 AL 49.9/F  
DREFSSCLK# R632 AL 49.9/F

Alviso Chip

For NV44M & Alviso option  
R\_CLK\_KBCPCI R626 NC 10K  
R\_PCLK\_MINI R627 NC 10K

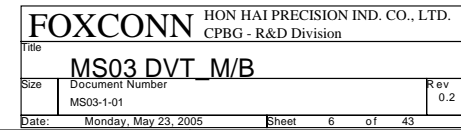
ICH6  
DMI

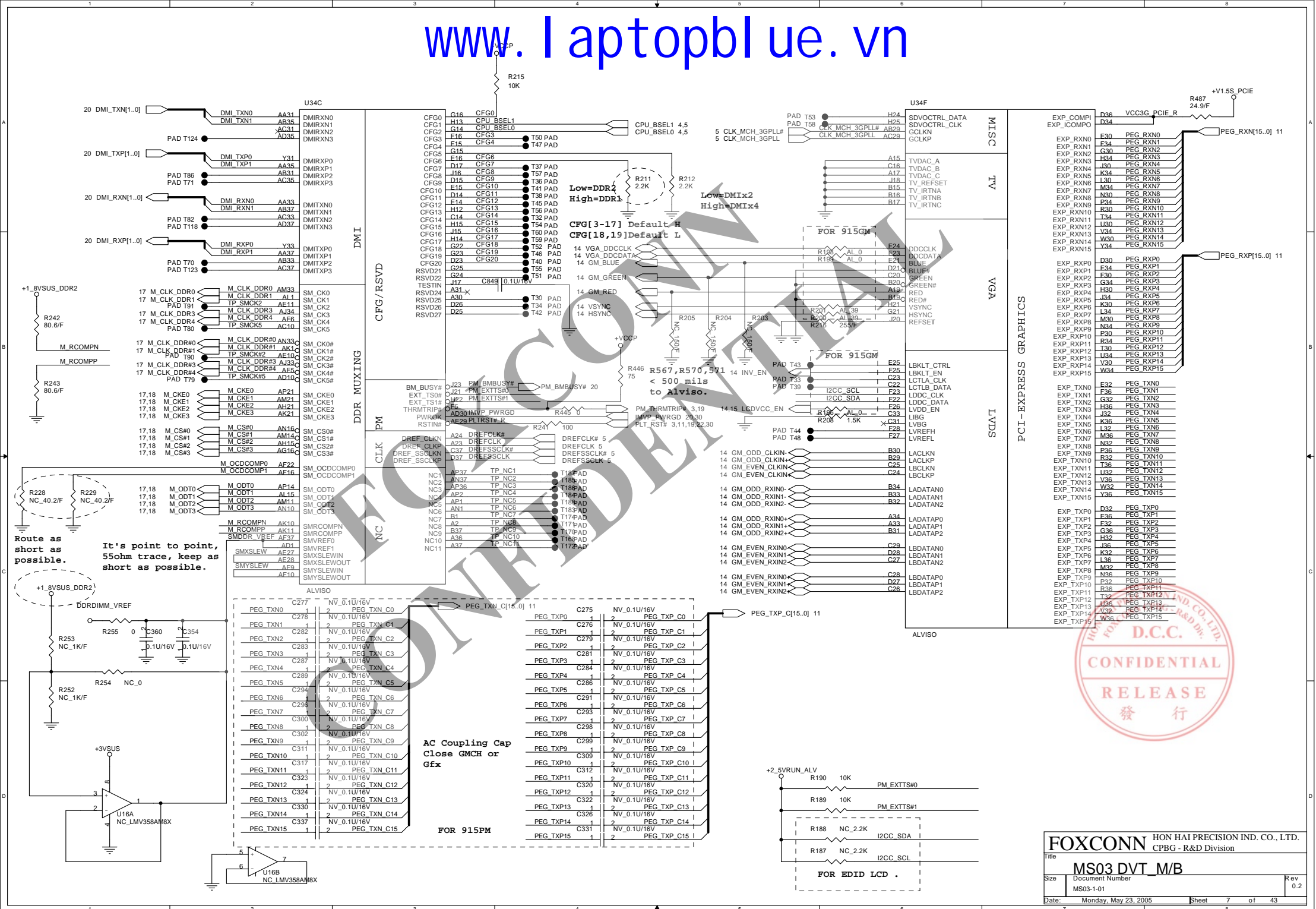
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NV44M

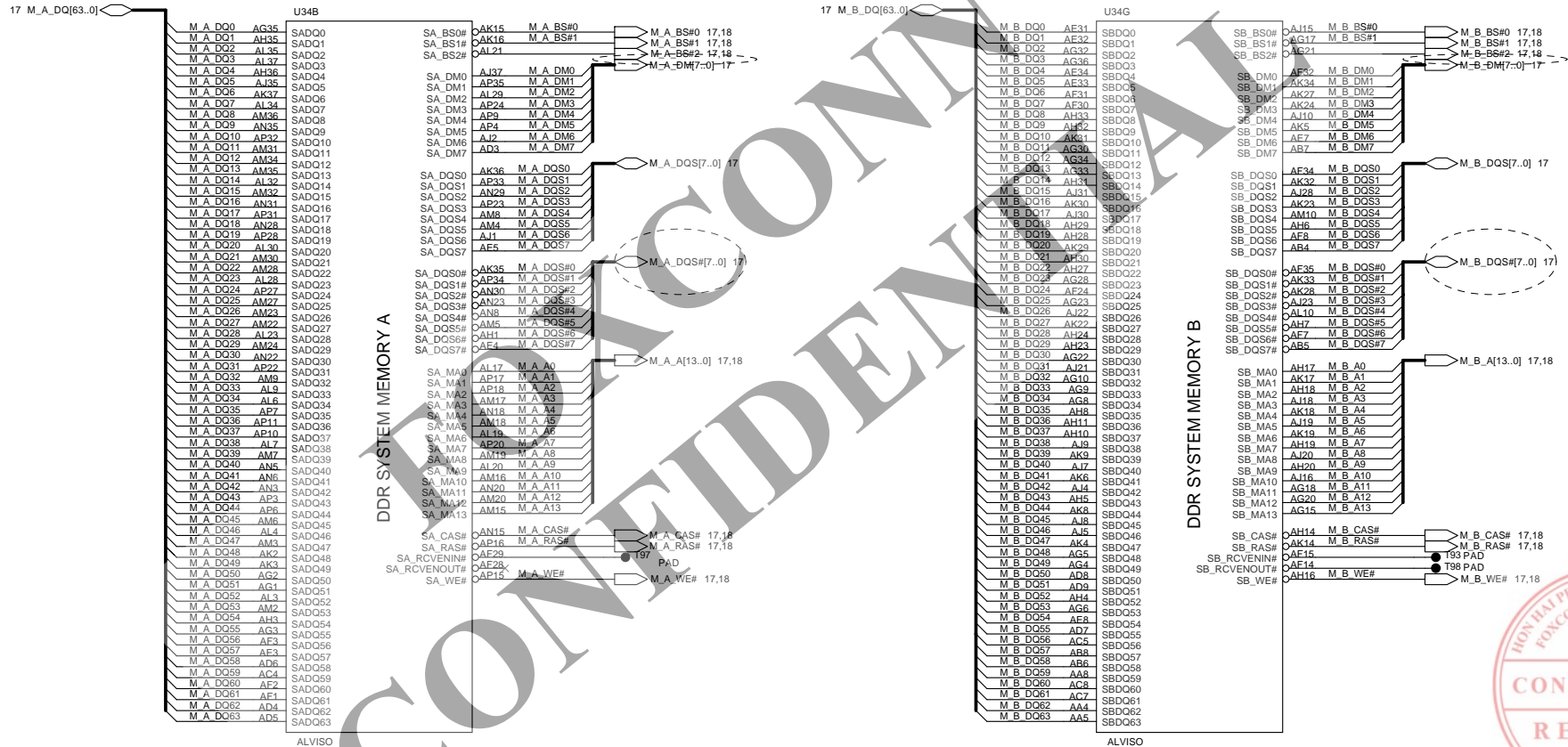
ALVISO SSCK



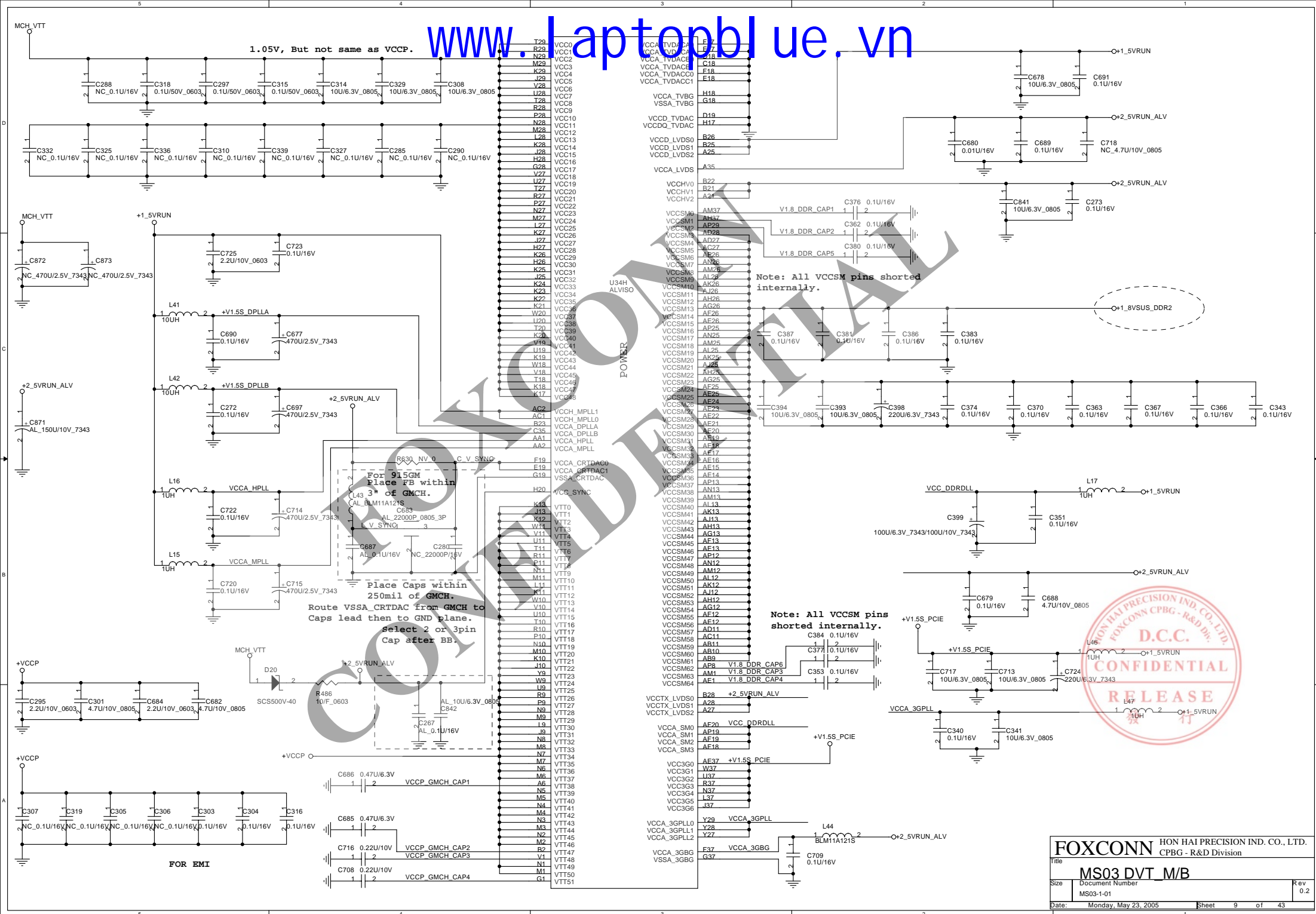




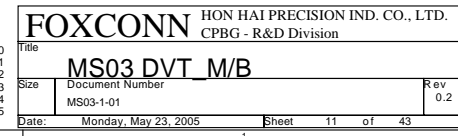




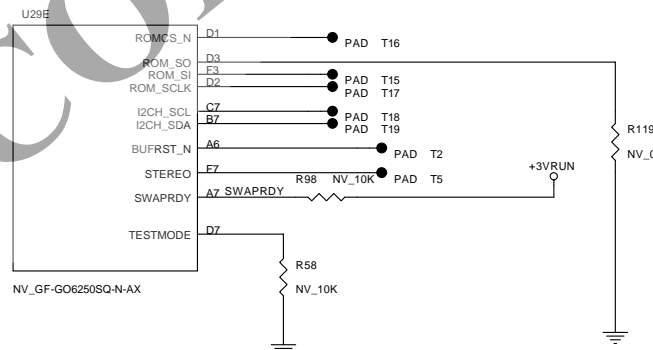
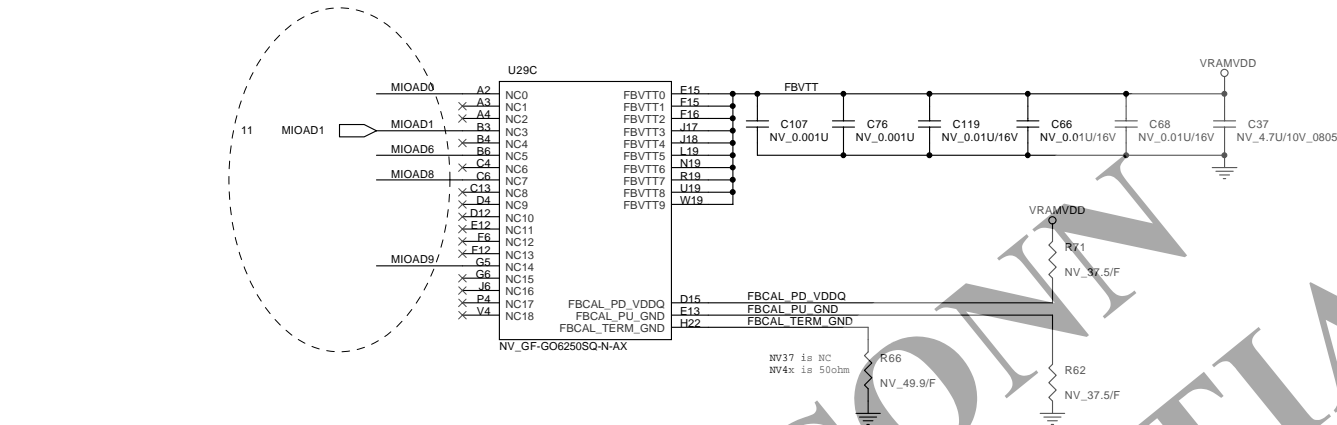








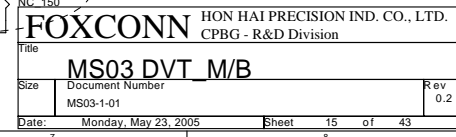


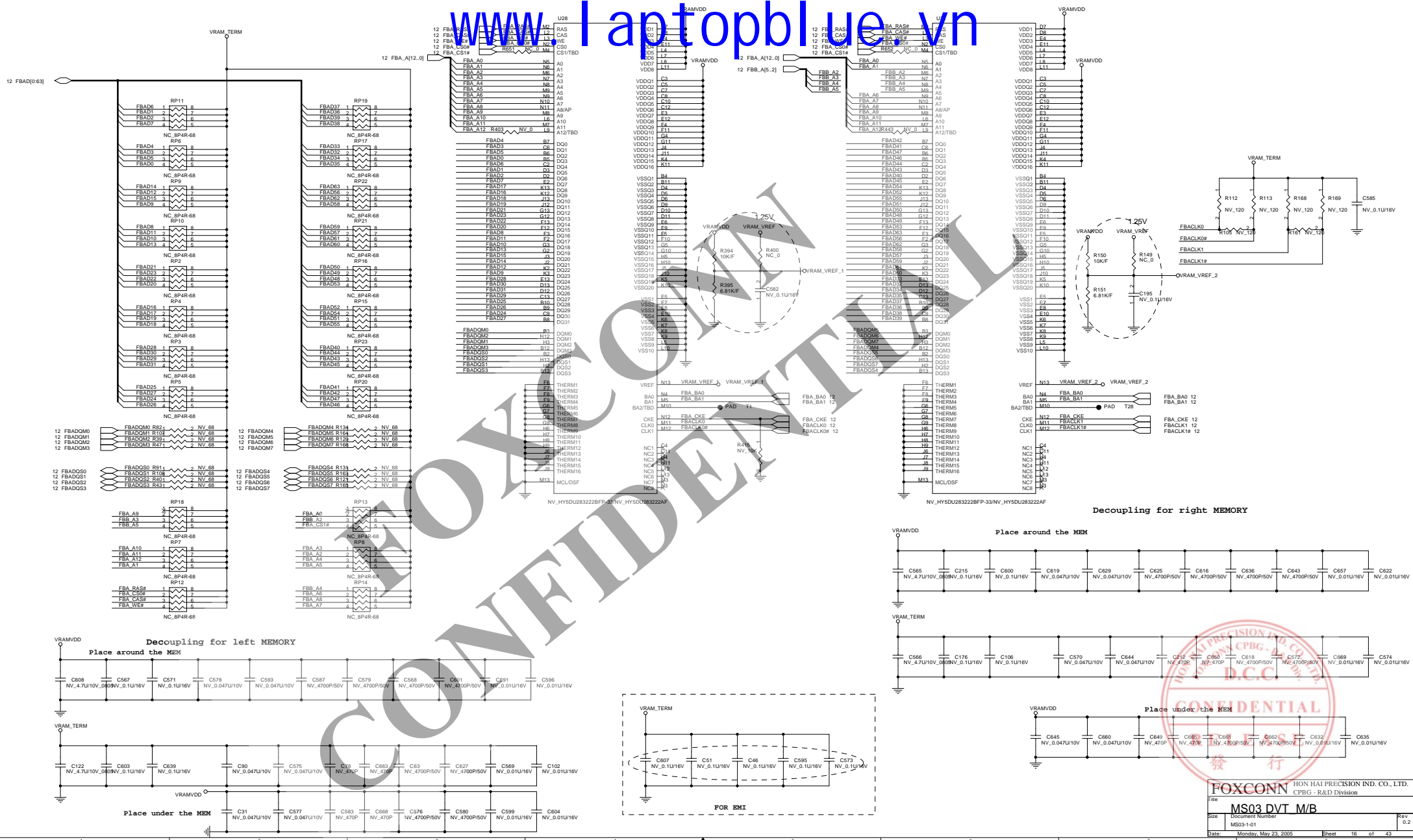


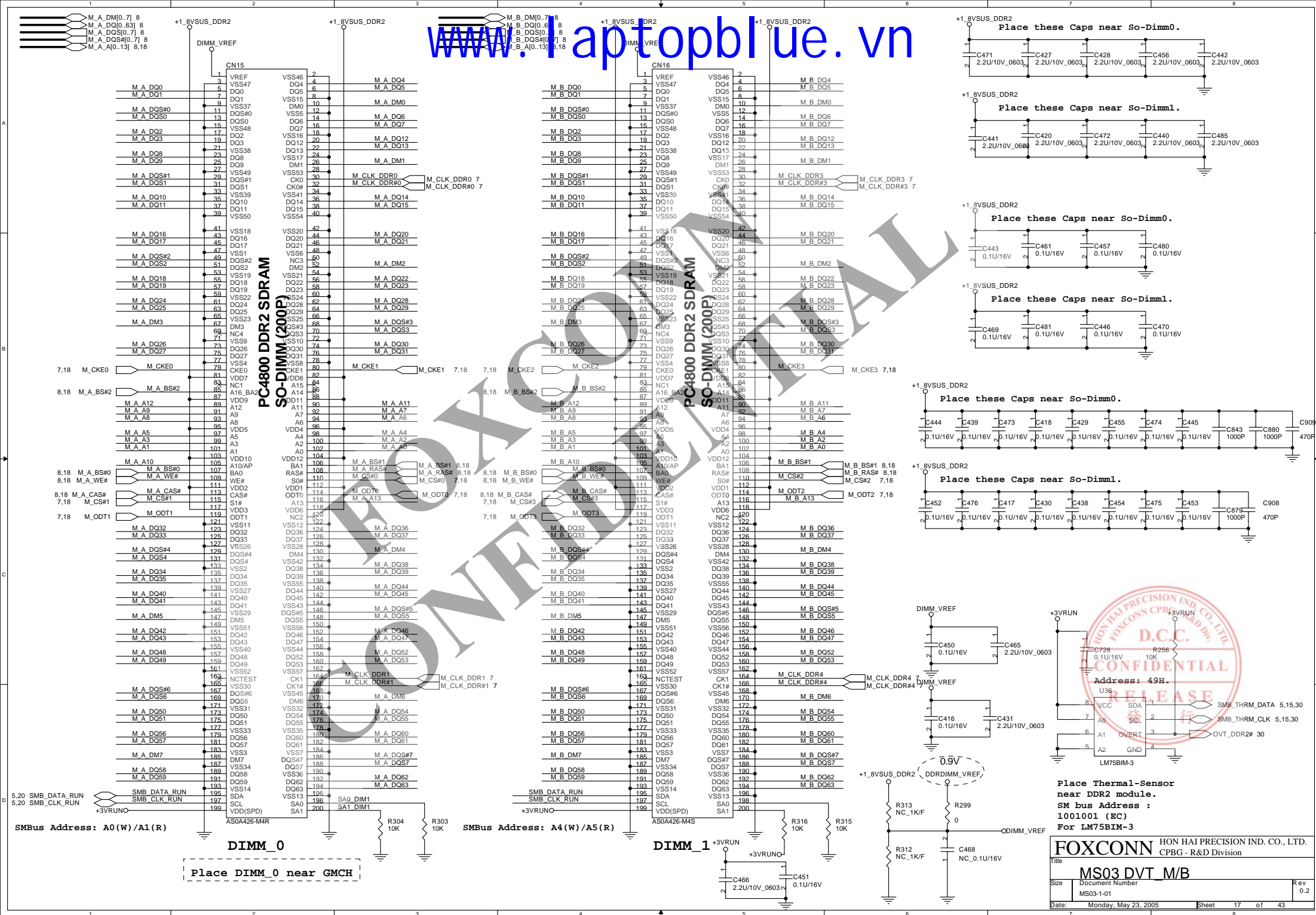




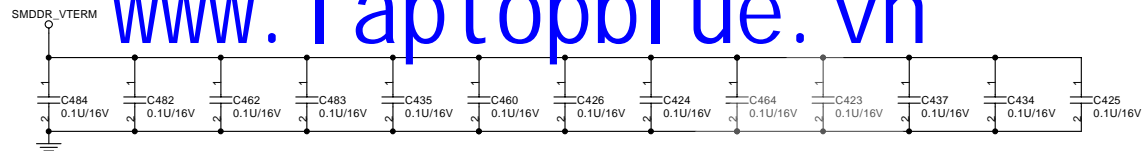
Date: Monday, May 23, 2005 Sheet 14 of 43



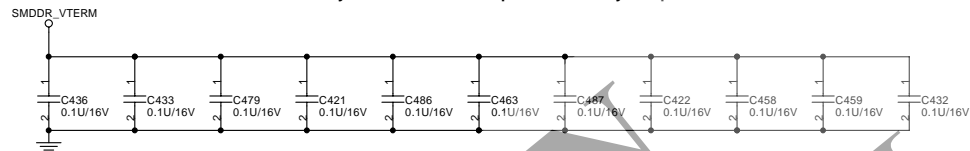




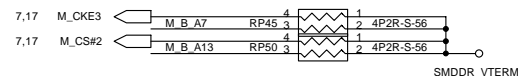
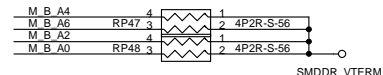
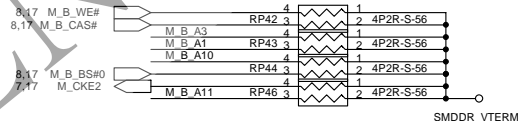
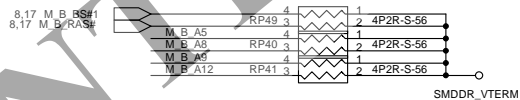
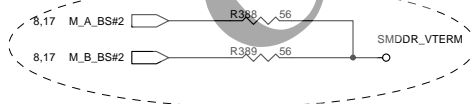
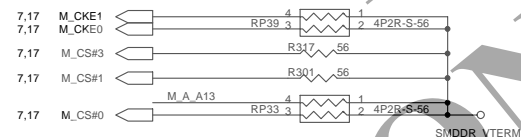
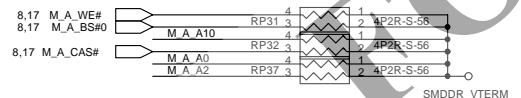
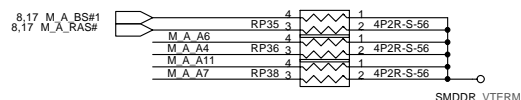
M\_A\_A[0..13] 8,17  
M\_B\_A[0..13] 8,17



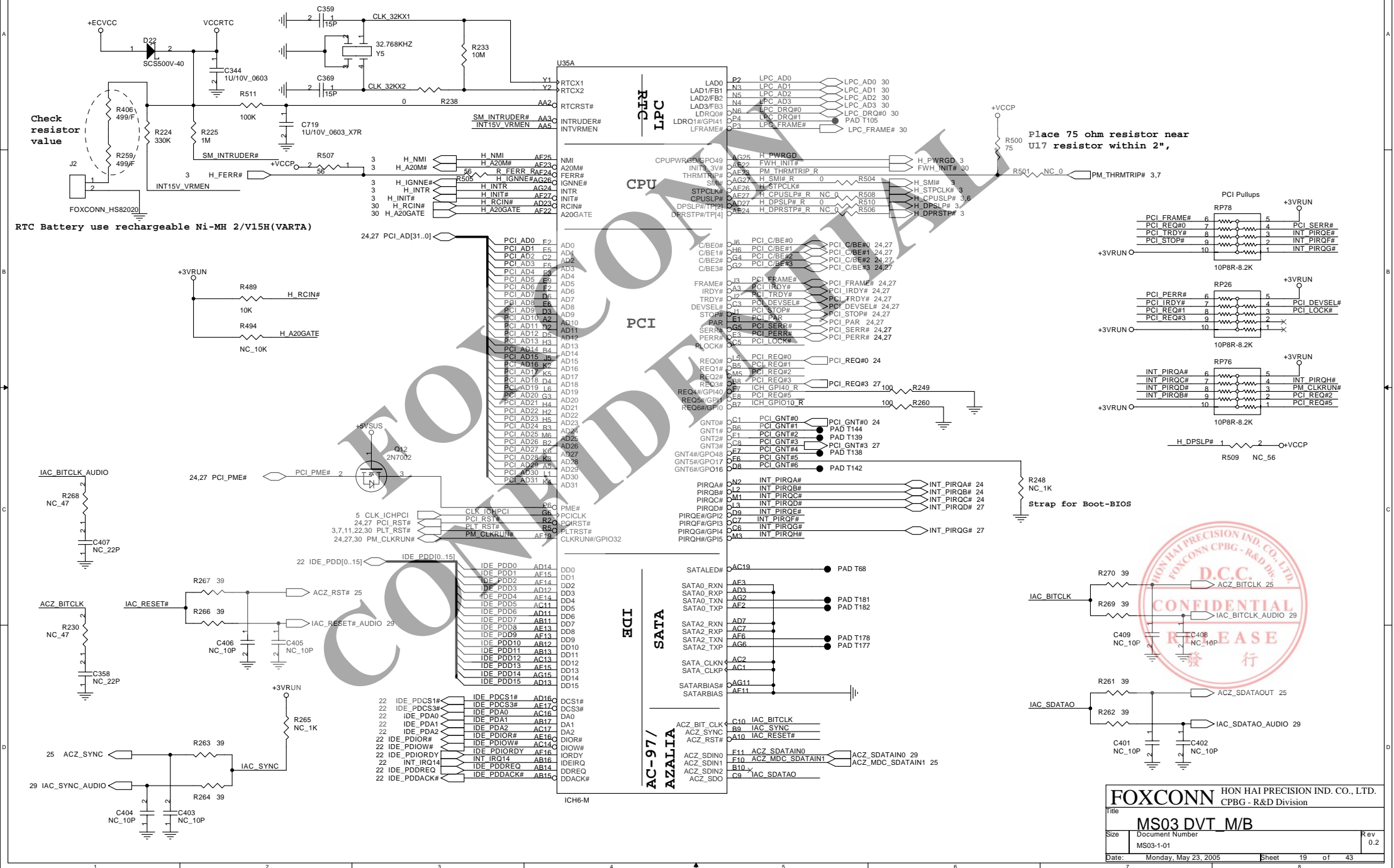
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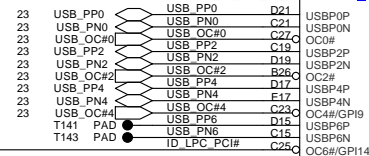
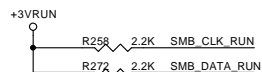


Layout note: Place 1 cap close to every 1 R-pack terminated to SMDDR\_VTERM.









# USB

# DMI

# PCI-EXPRESS

# SM&SMI

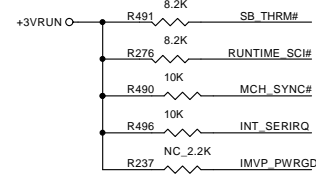
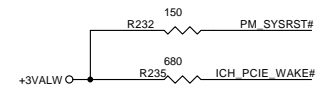
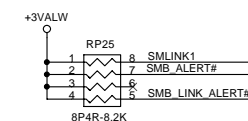
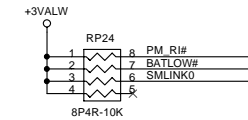
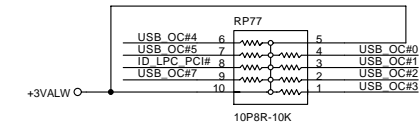
# PM

# MISC&GPIO

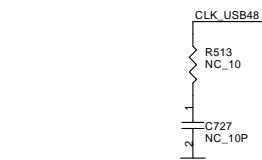
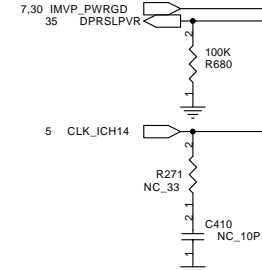
# LAN

# RESERVED

# ICH6-M

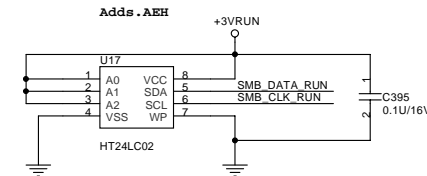


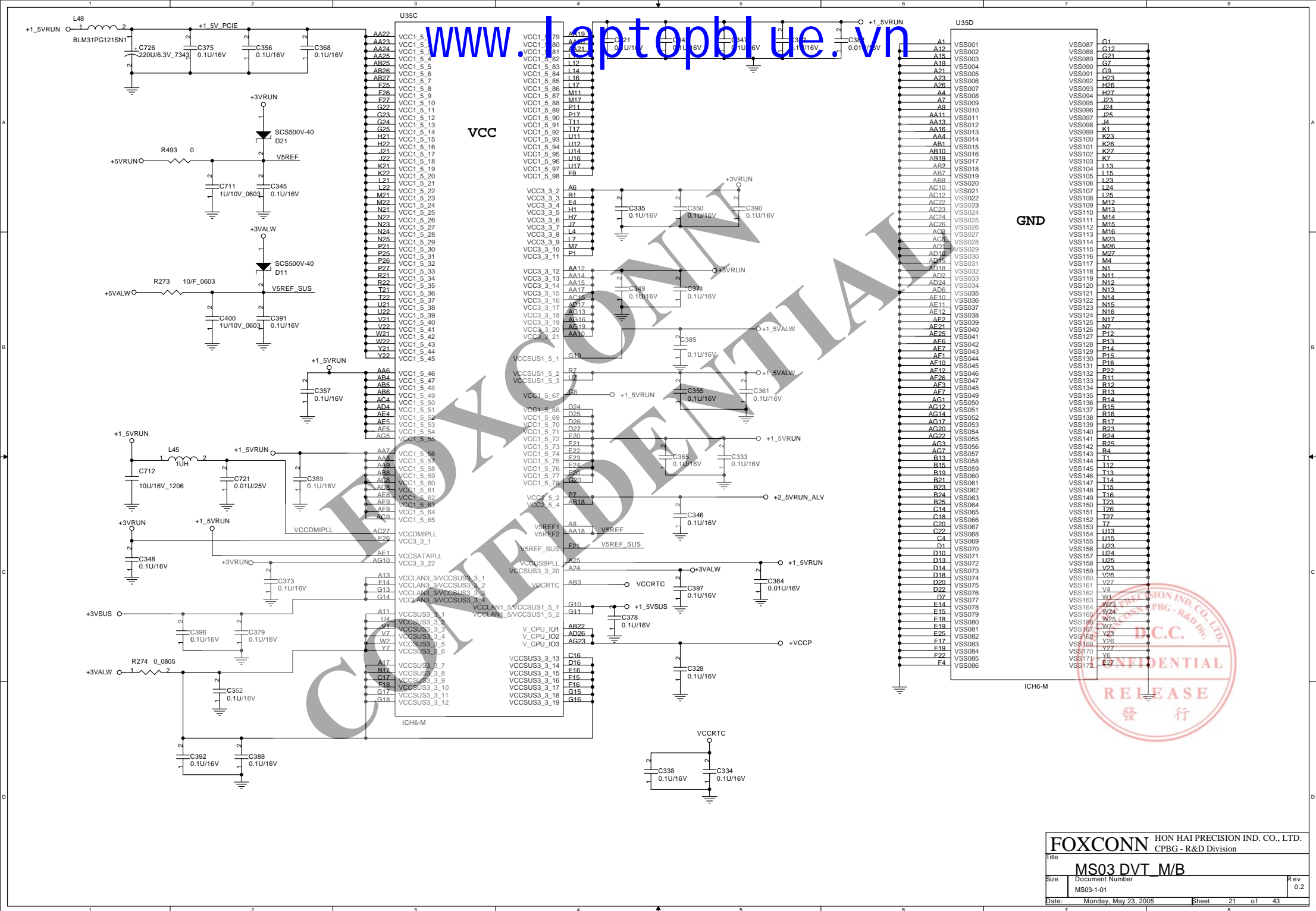
30 ID\_LPC\_PCI#  
80 Port I/F:  
H: LCP bus  
L: PCI bus

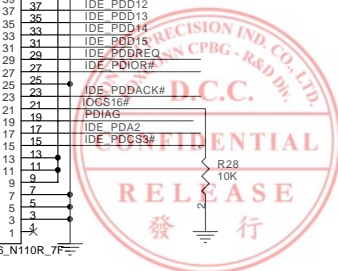
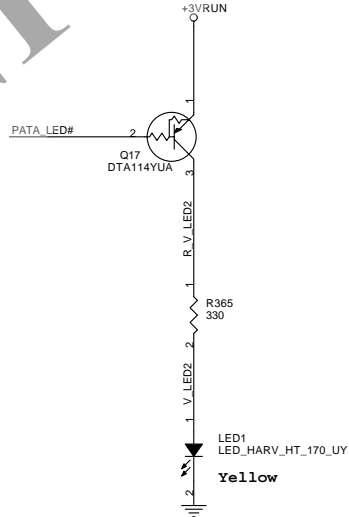
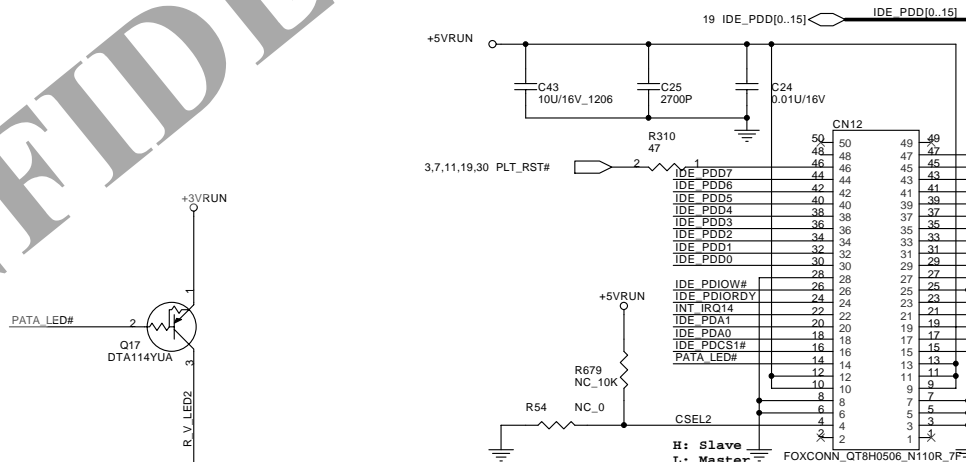
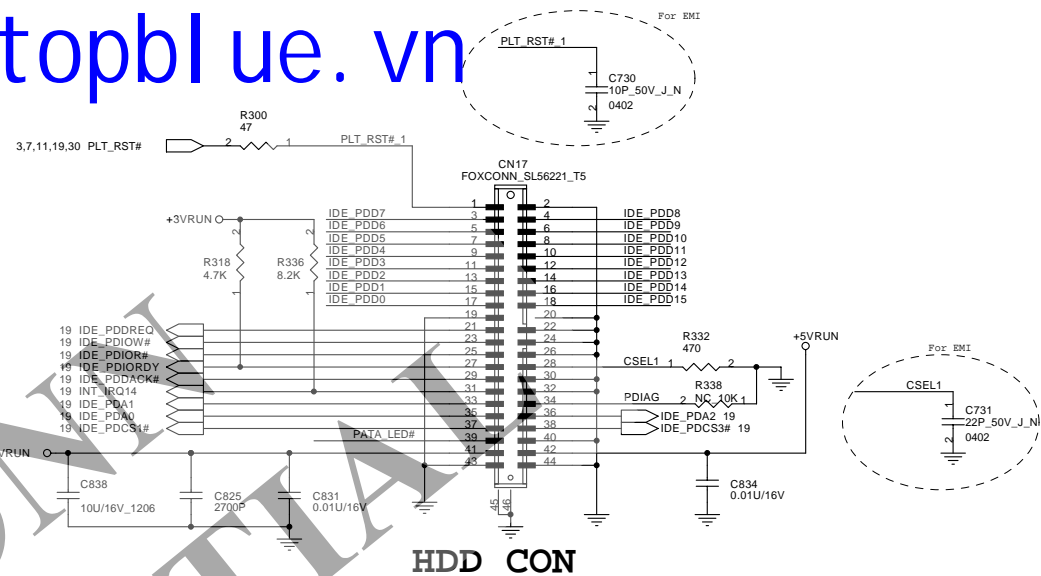


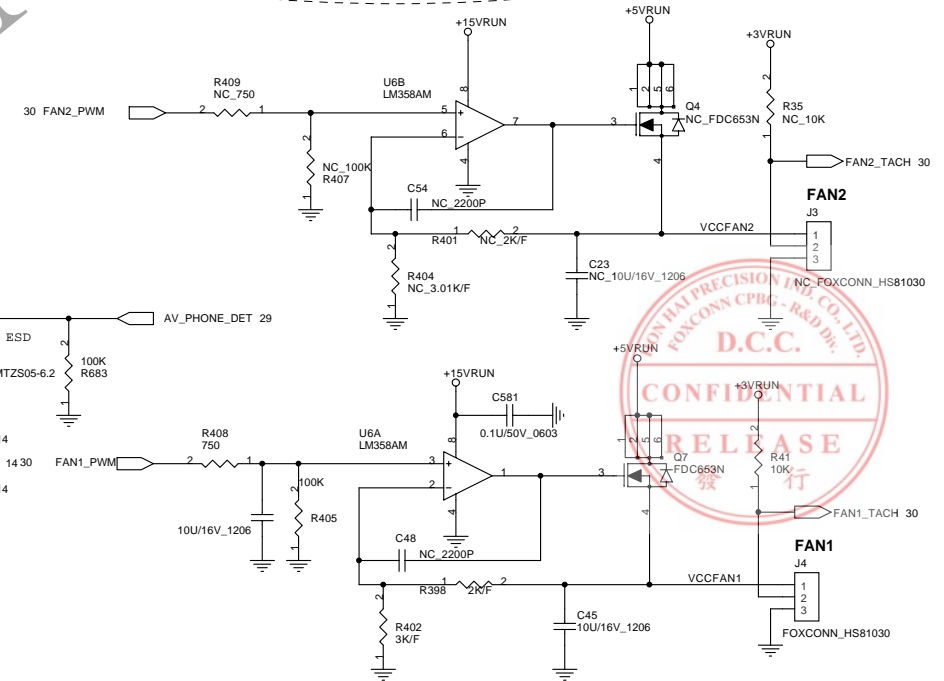
Strap for No-reboot  
R251 1K/F  
AC SPKR

Adds .AEH









**FAN**

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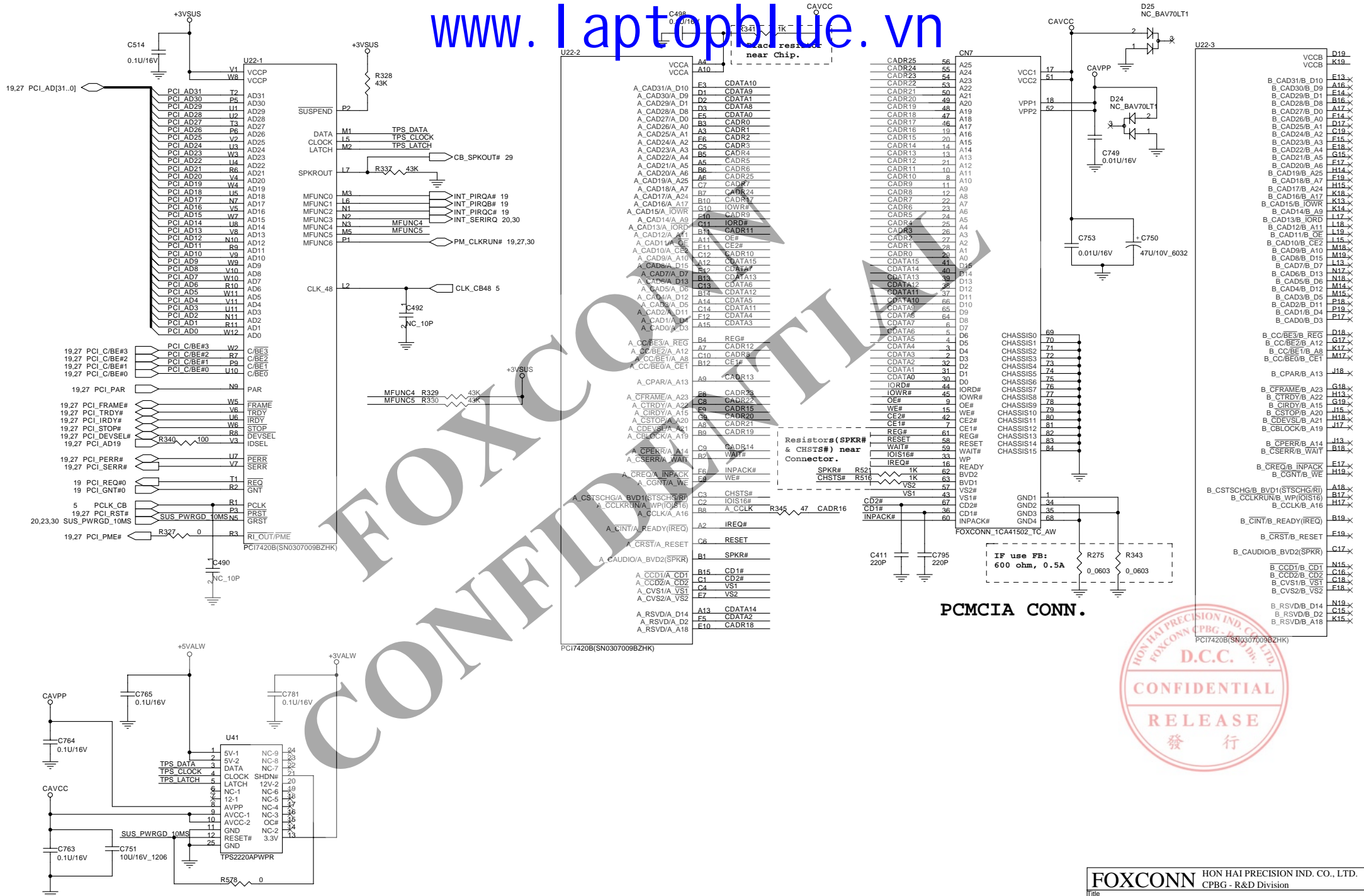
MS03 DVT M/B

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PCMCIA CONN.

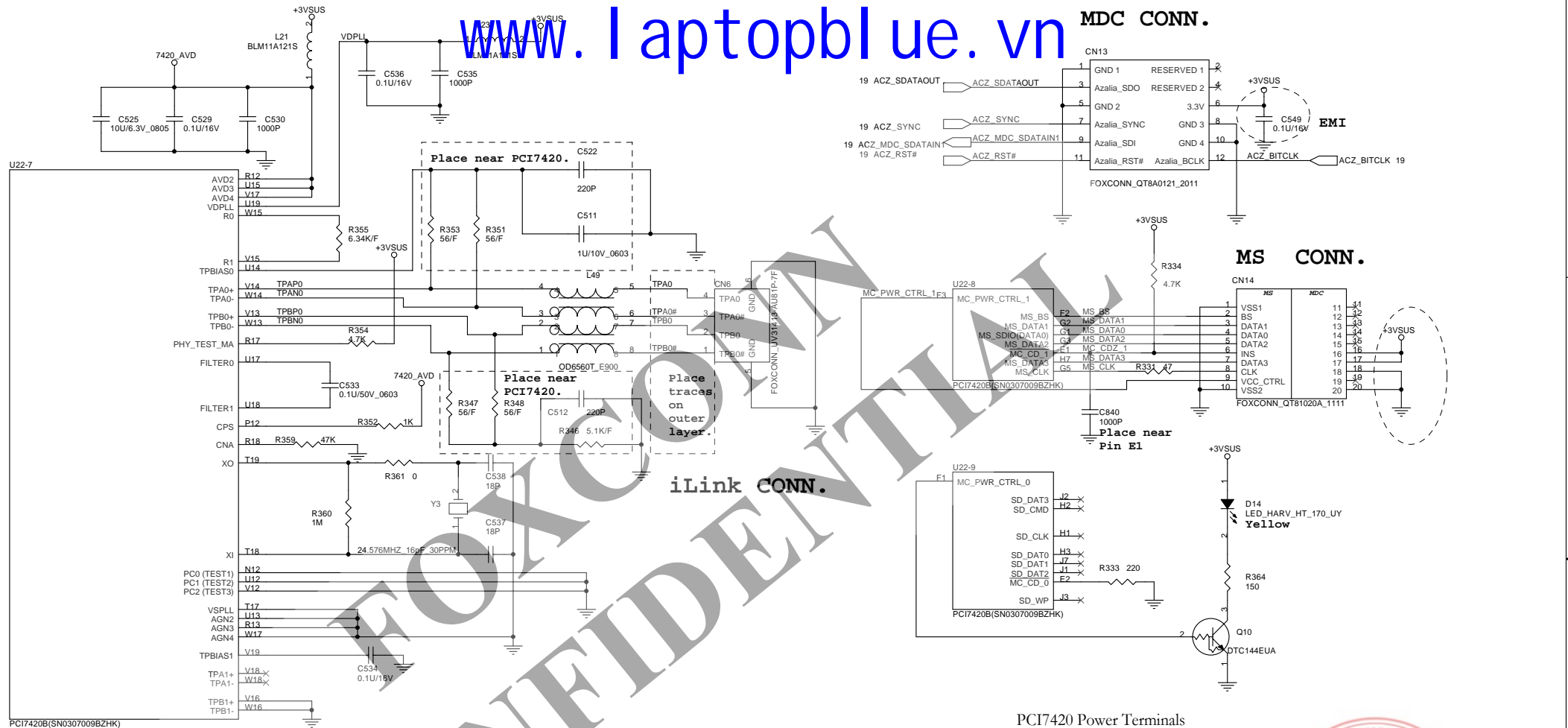
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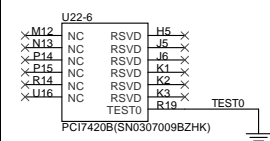
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7	8

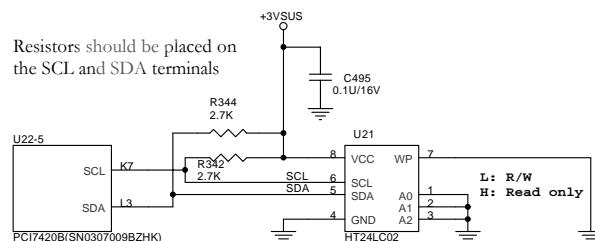
MDC CONN.



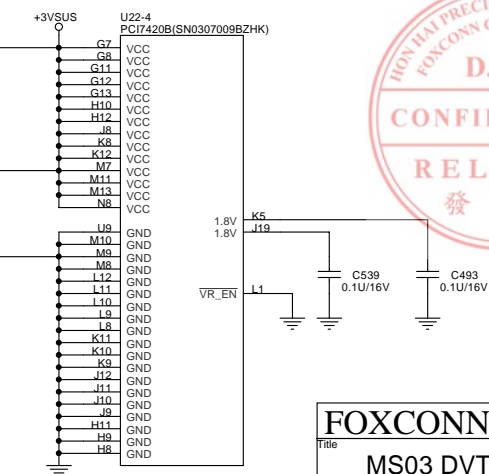
## PCI7420 UNUSED TERMINALS



Resistors should be placed on the SCL and SDA terminals



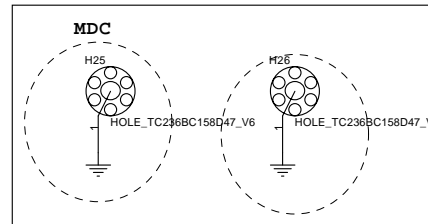
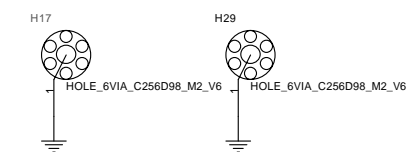
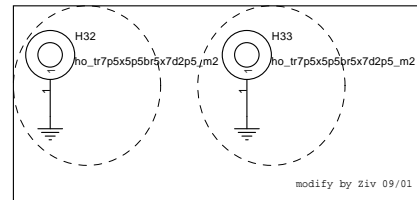
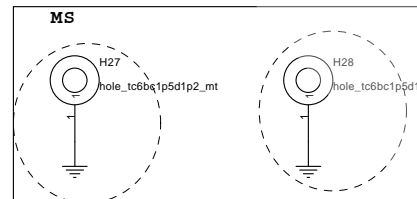
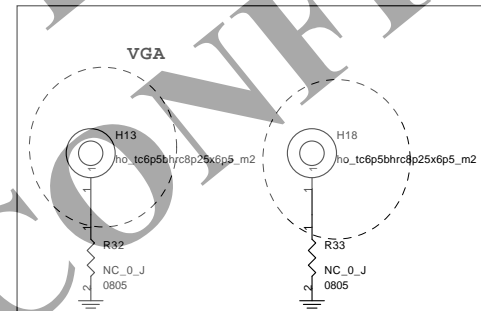
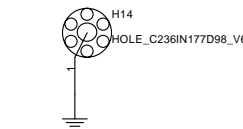
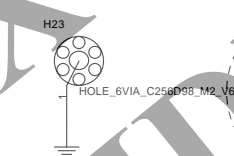
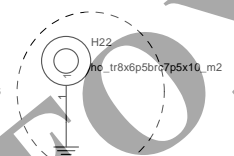
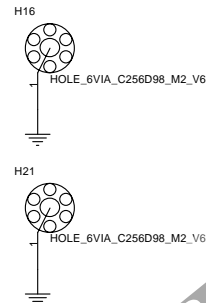
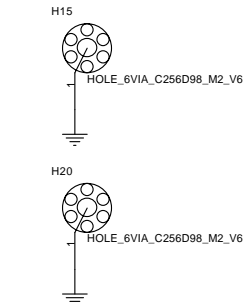
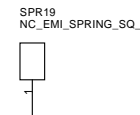
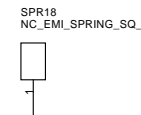
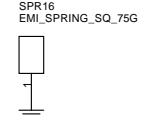
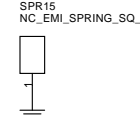
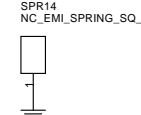
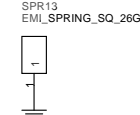
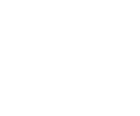
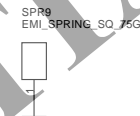
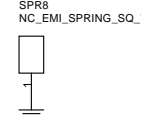
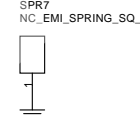
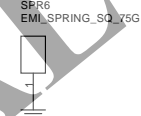
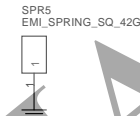
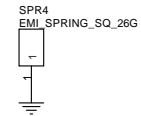
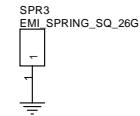
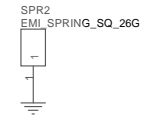
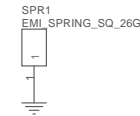
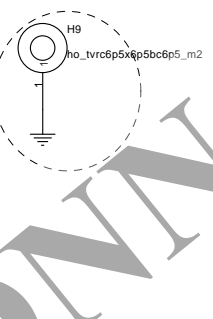
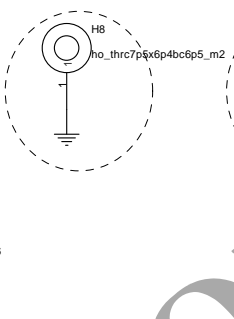
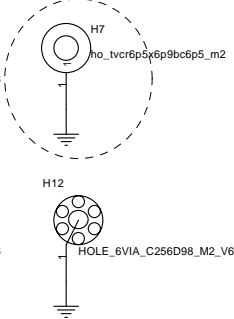
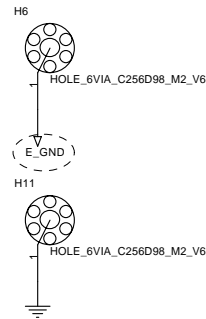
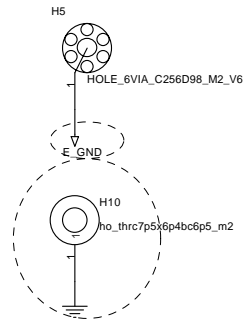
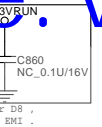
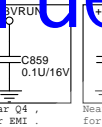
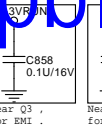
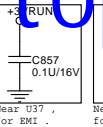
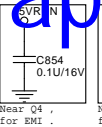
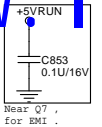
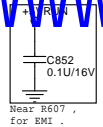
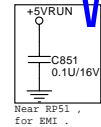
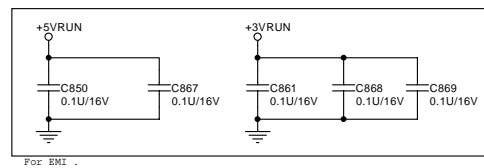
## PCI7420 Power Terminals

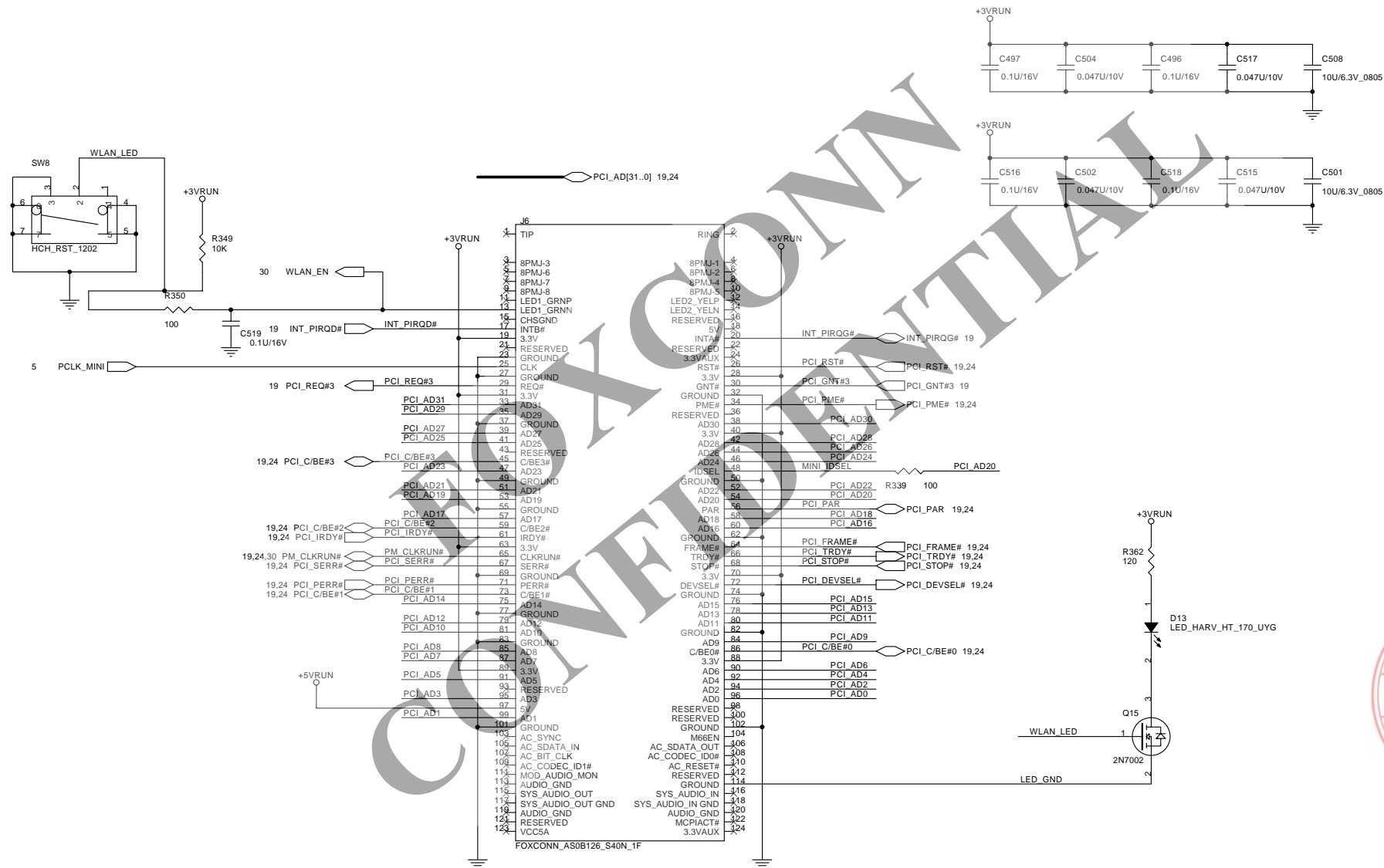


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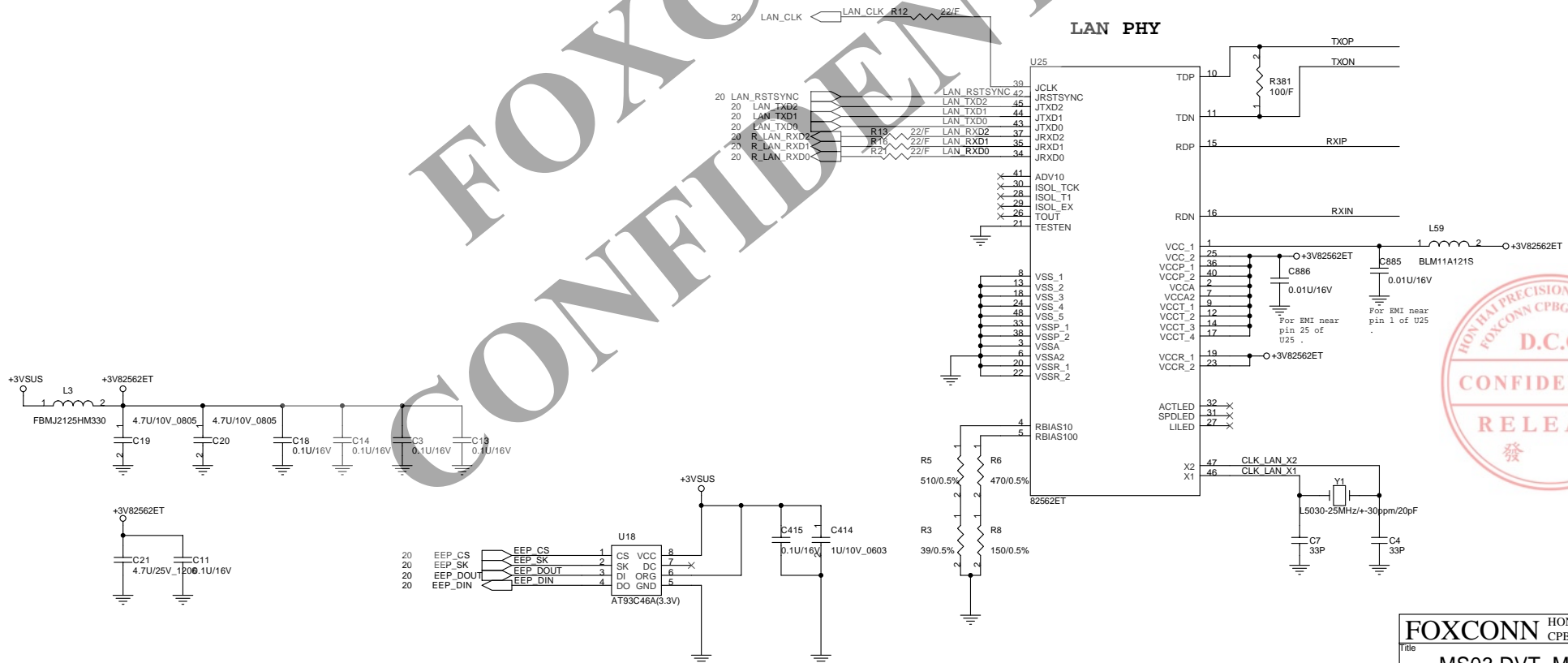
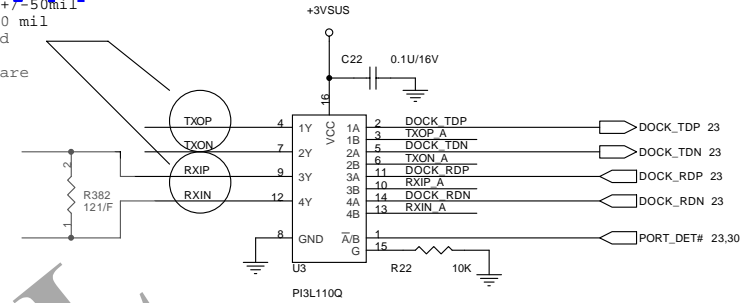
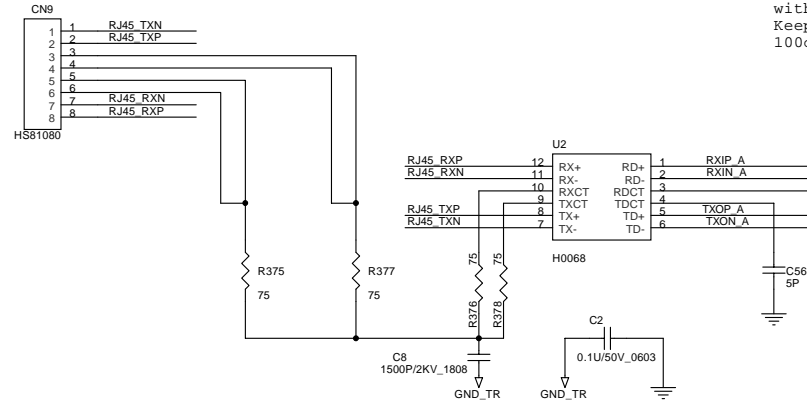
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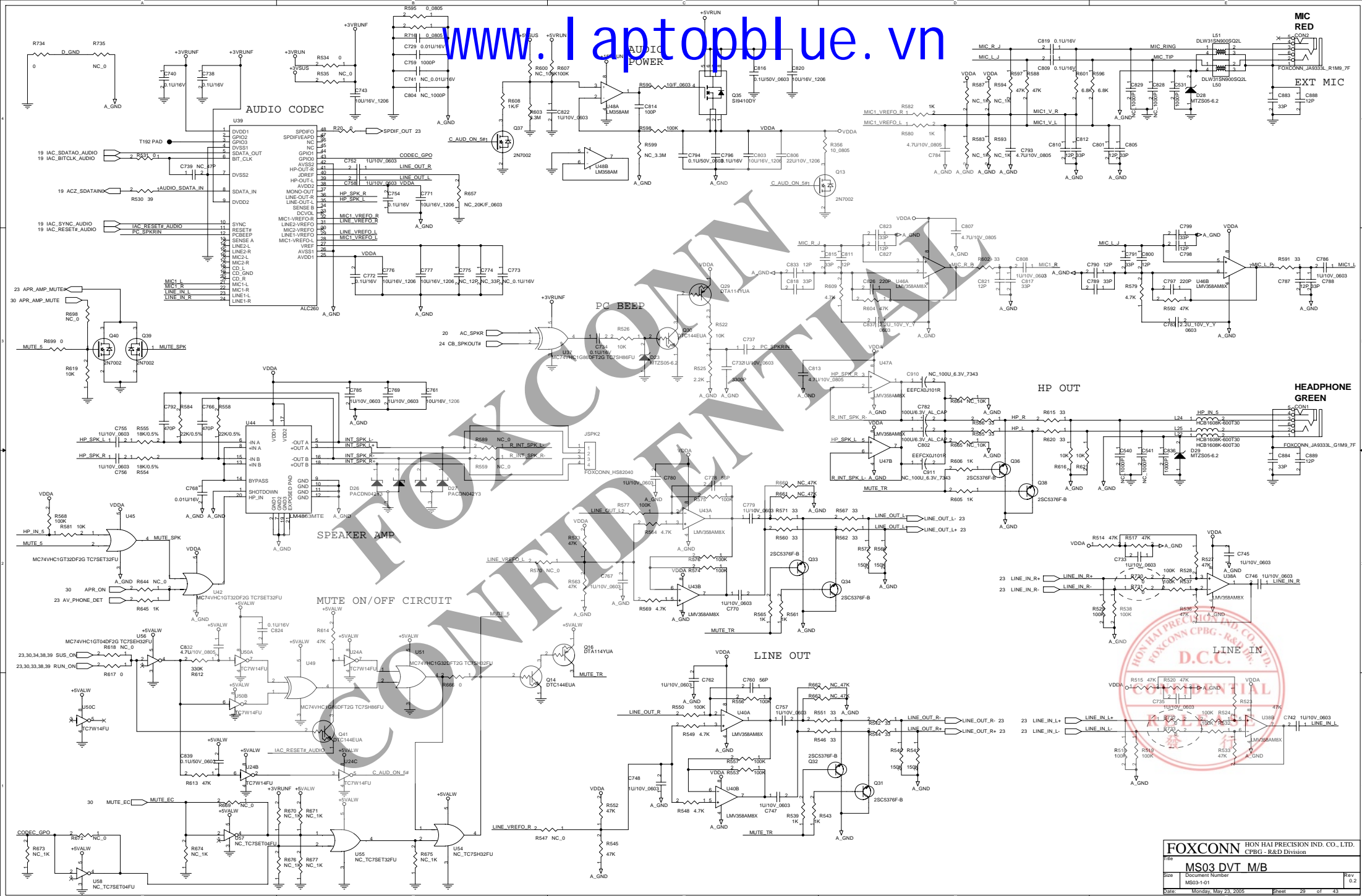


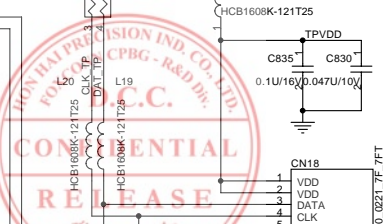


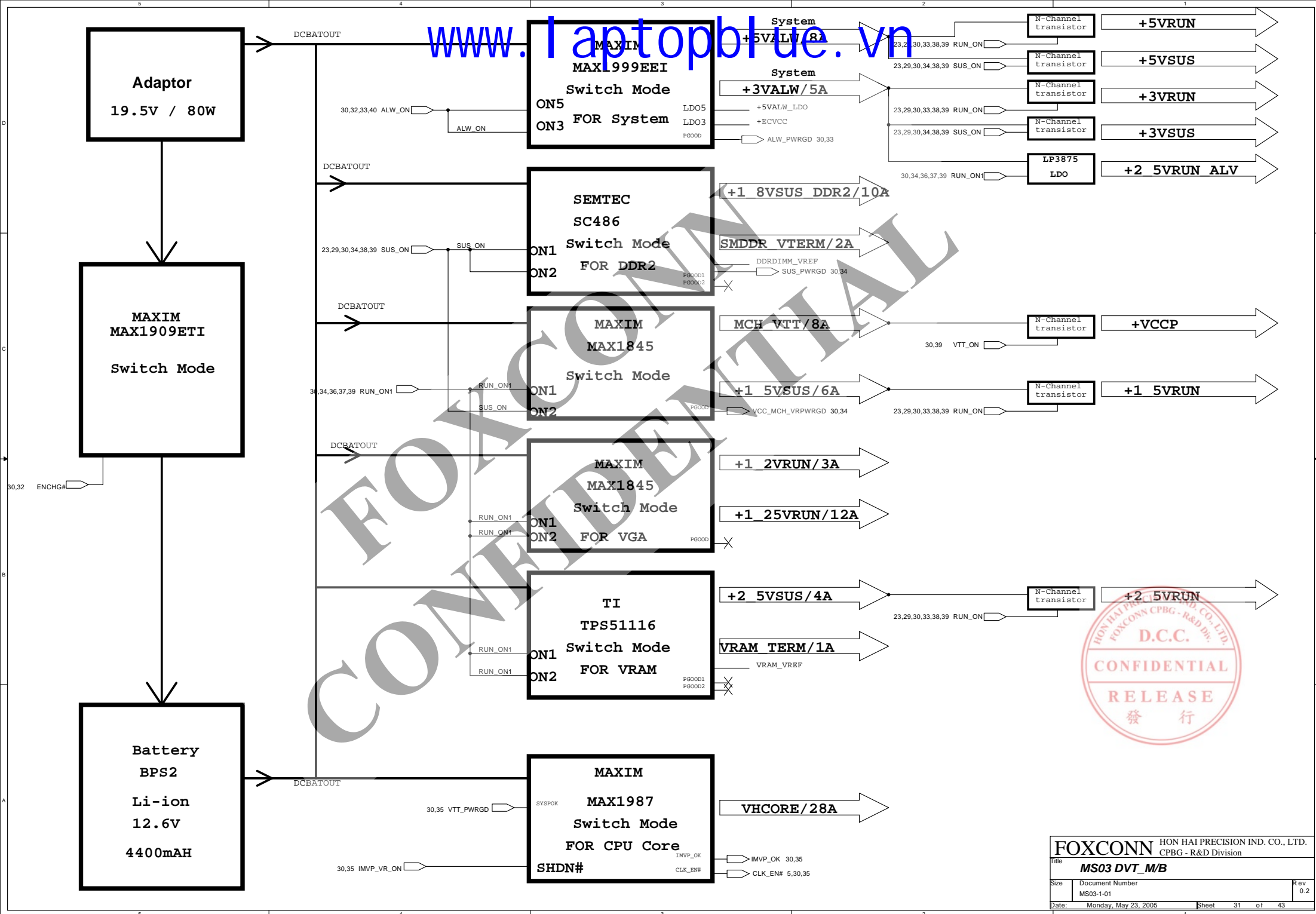
Match trace length  
 LAYOUT NOTES:  
 Match total length of chip side Rx and Tx pair traces +/-50mil  
 Match length of cable side Rx and Tx pair traces +/- 50 mil  
 Total line TX+ to TX- and RX- and RX+ should be matched  
 within 50 mils.  
 Keep 50mil space between pairs and other traces.Pairs are  
 100ohm differential,





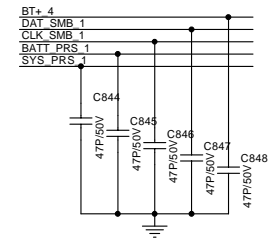




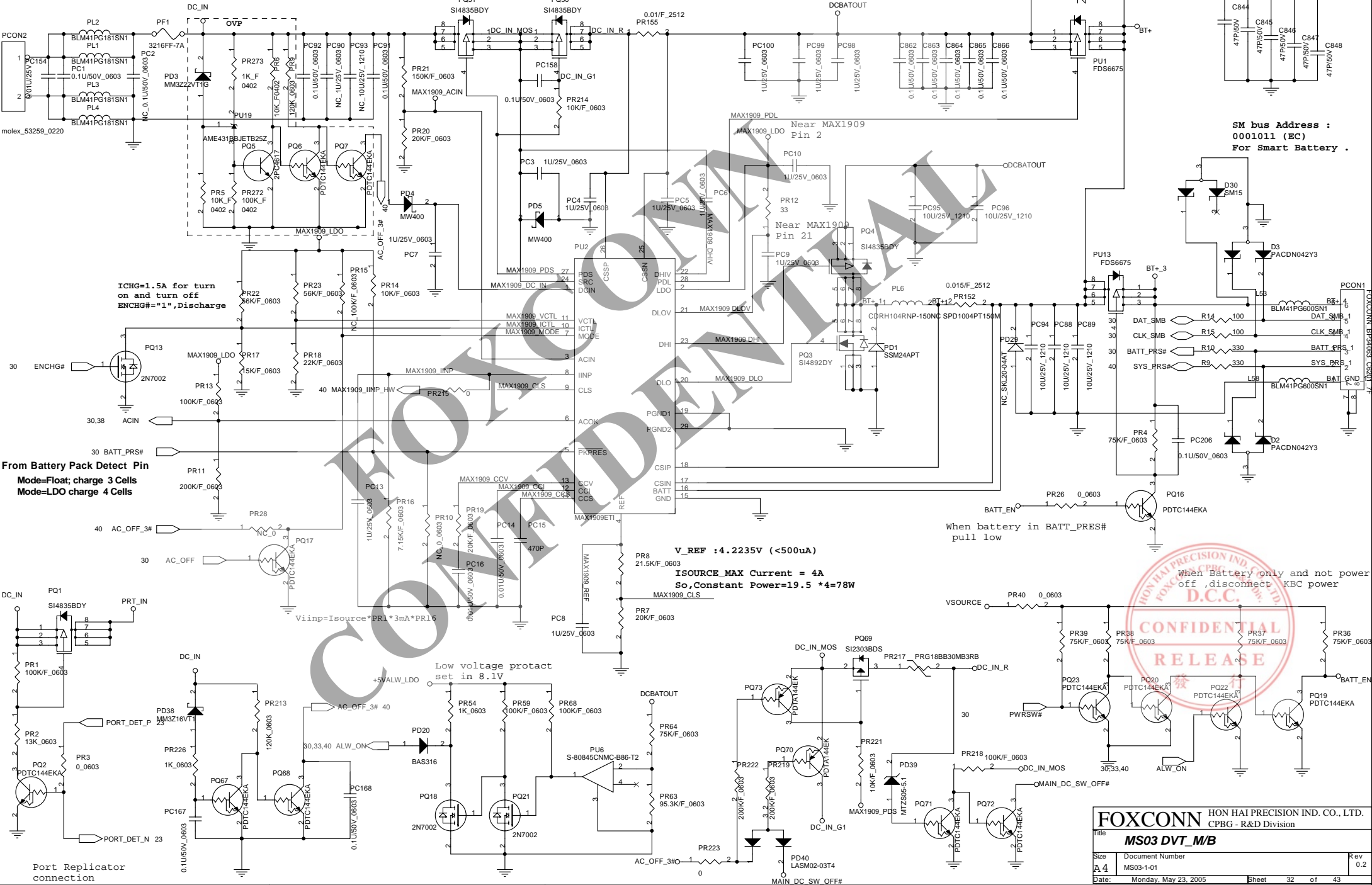


DC\_IN from port replicator

AC IN Threshold 2.089V Max  
AC\_IN > 2.089V --> AC DETECT



SM bus Address :  
0001011 (EC)  
For Smart Battery .



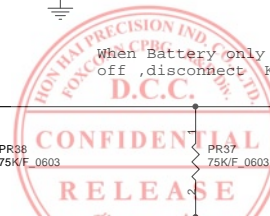
ICHG=1.5A for turn on and turn off  
ENCHG#="1", Discharge

From Battery Pack Detect Pin  
Mode=Float; charge 3 Cells  
Mode=LDO charge 4 Cells

V\_REF : 4.2235V (<500uA)  
ISOURCE\_MAX Current = 4A  
So, Constant Power=19.5 \*4=78W

When battery in BATT\_PRES# pull low

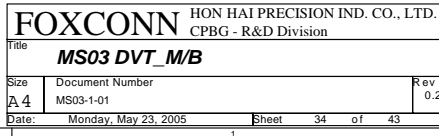
When Battery only and not power off, disconnect KBC power

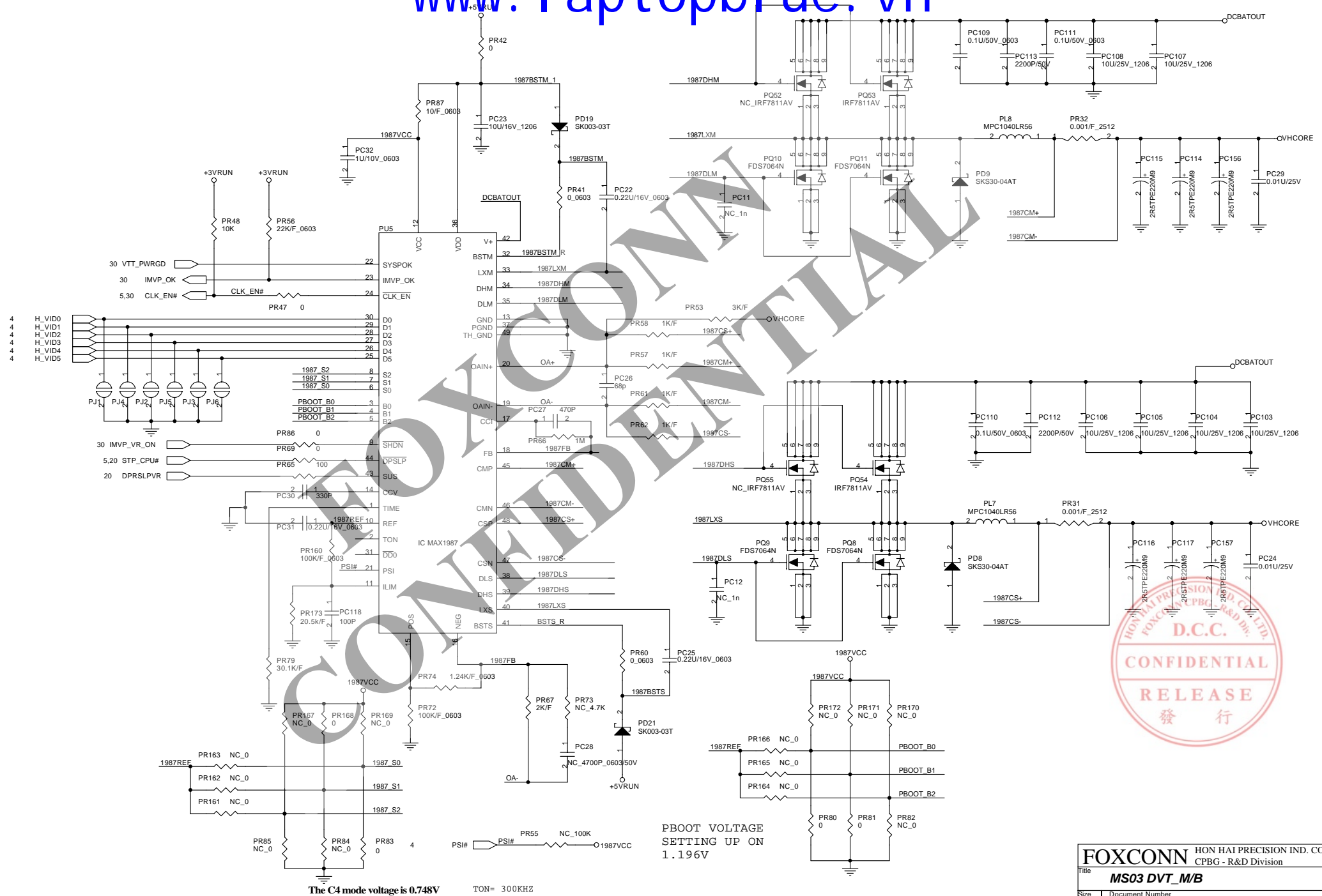


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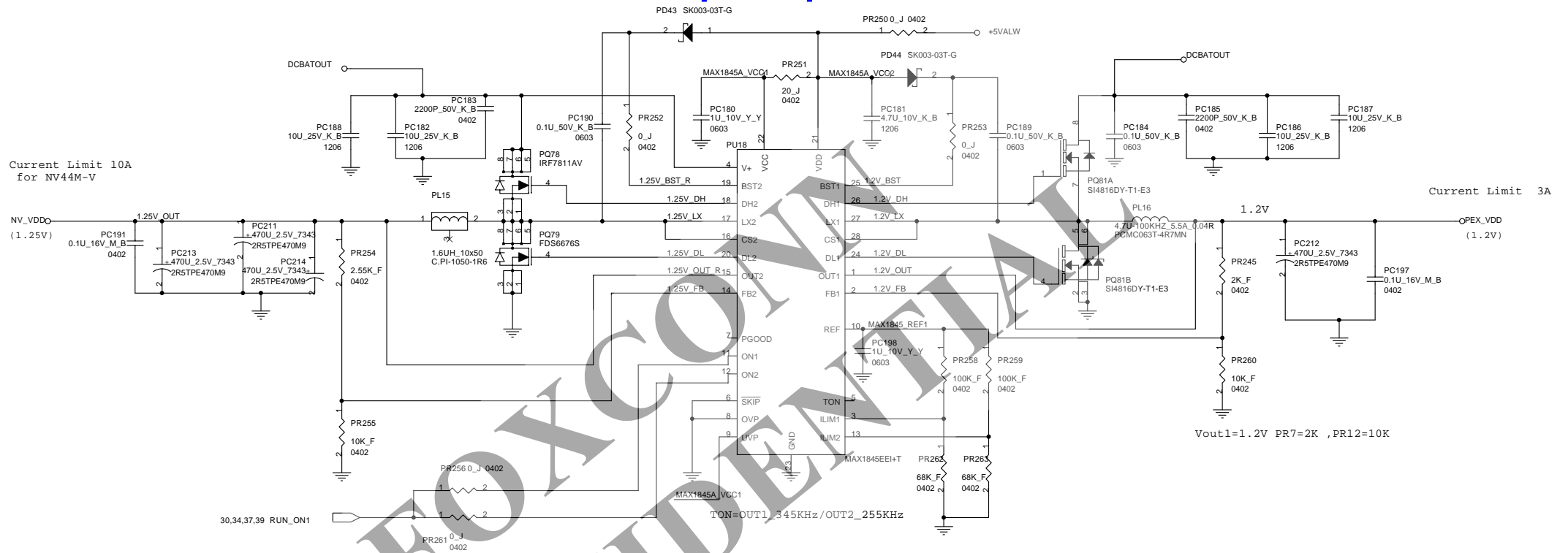




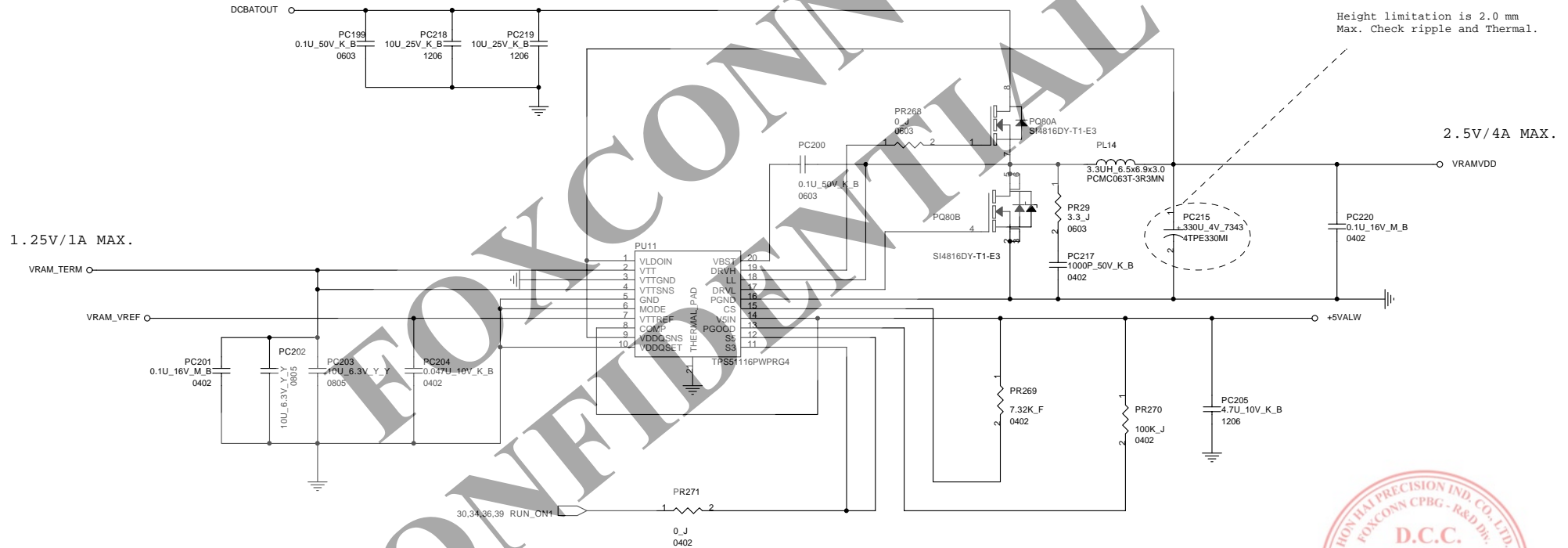


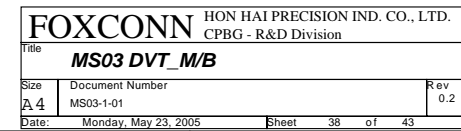
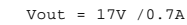


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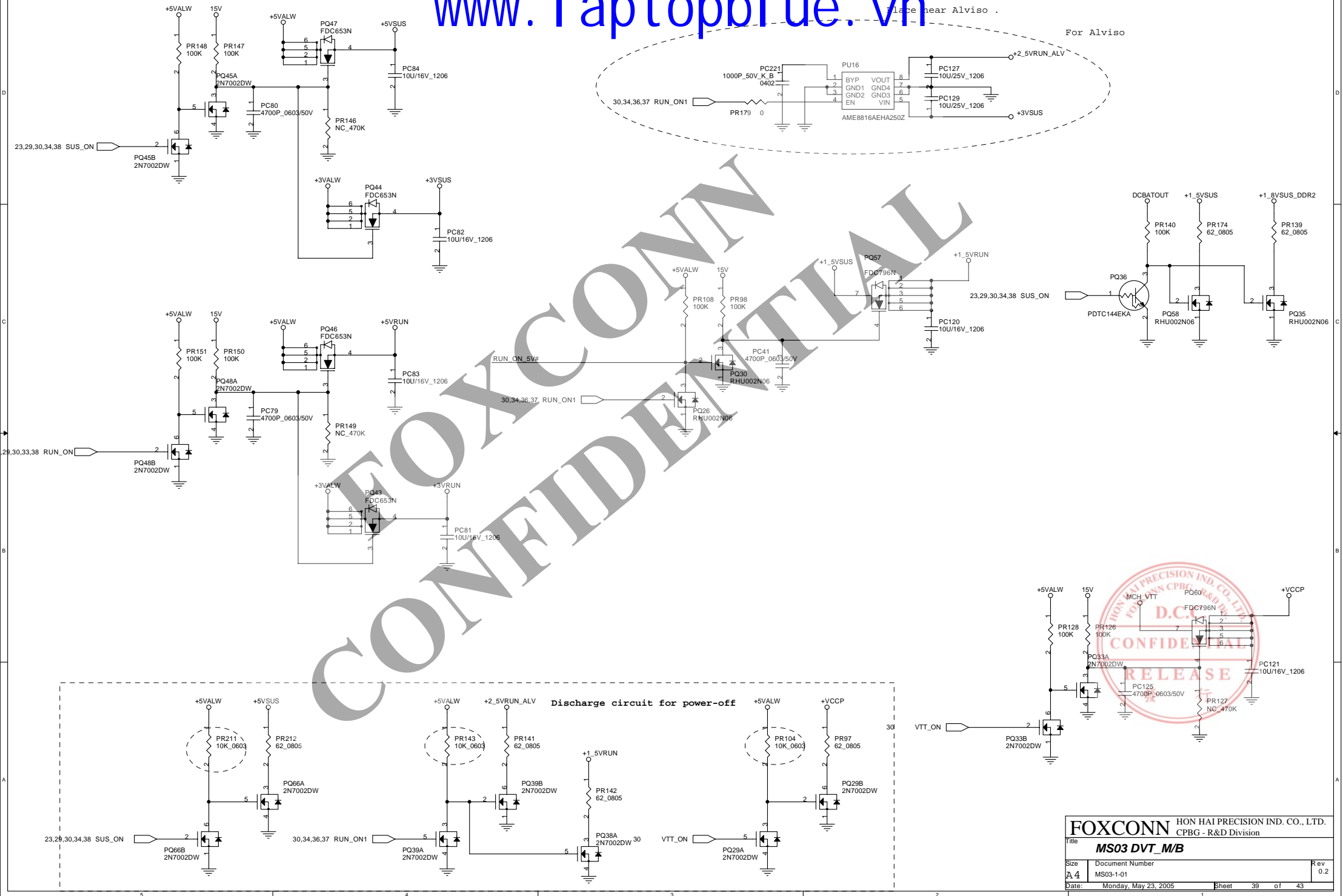


Power daughter board for VGA

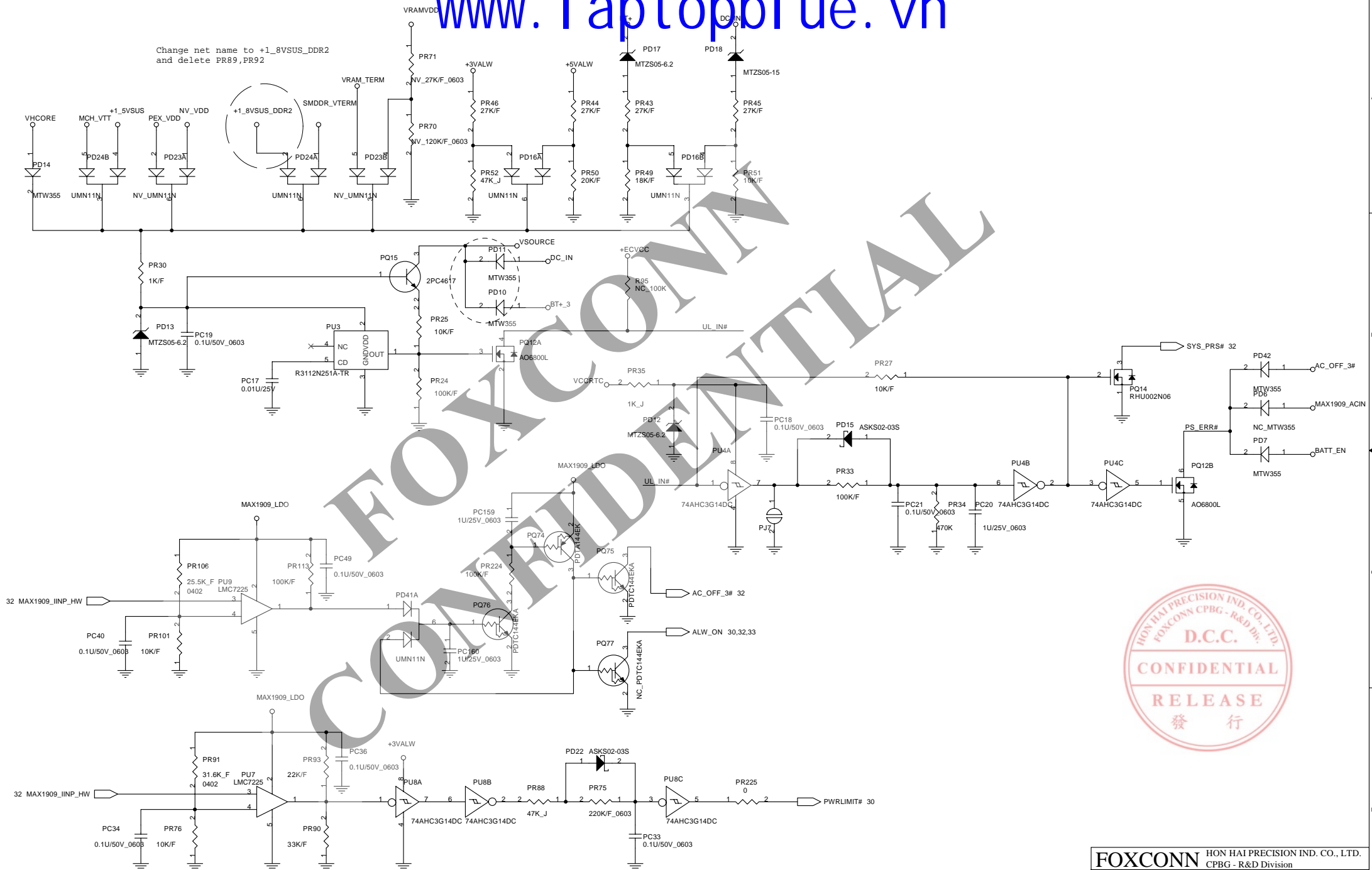








Change net name to +1\_8VSUS\_DDR2  
and delete PR89,PR92





HISTORY  
(2005/05/18)

P29: Change C783, C837 from 1U/10V\_0603 to 2.2U\_10V\_Y\_Y.  
P26: Change H27, H28 from ho\_tclp5bc6d1p2\_m2(ho\_tclp5bc6d1p2\_mb) to hole\_tc6bc1p5d1p2\_mt(ho\_tc6bc1p5d1p2\_mt).  
P40: Change PR91 from 31.6K to 25.5K, change PR109 from 49.9K to 31.6K.  
P29: Delete R611, R622, R628, R629, R647, R648, R649, R650, JSPK1.  
P29: Add C910, C911 NC\_100U\_6.3V\_7343.

(2005/05/19)

P29: Add R734,R735 for anti-digital noise interference.

(2005/05/20)

P30: Change R311, R314 from 10K to 4.7K\_J.  
P29: Change R735 from mount to NC.  
P05: Change R481 from 56ohm to 47ohm.  
P05: Change R478 from 56ohm to 47ohm.

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