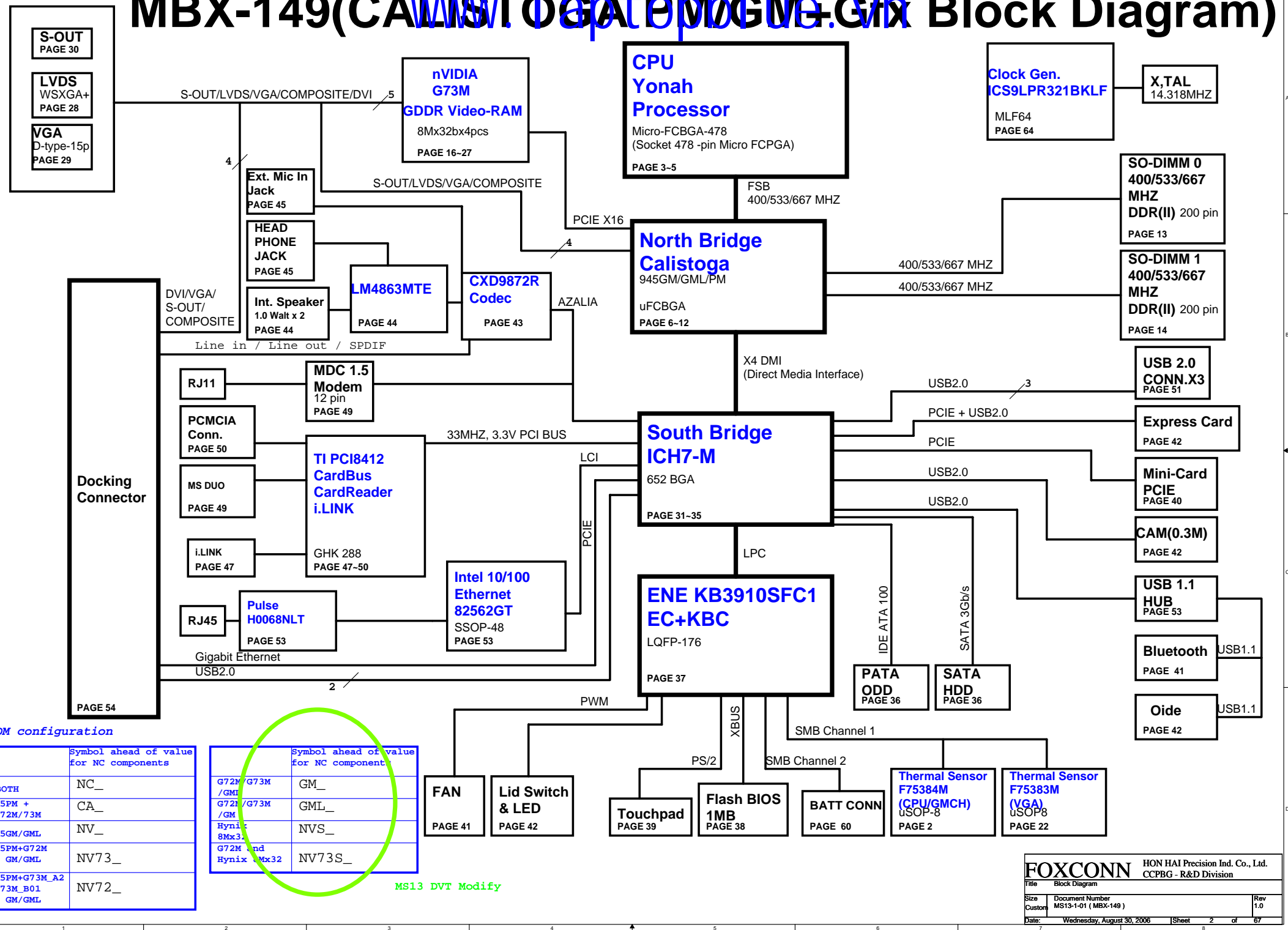


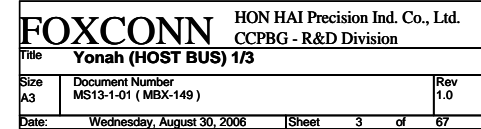
www.laptopblue.vn

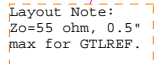
D11

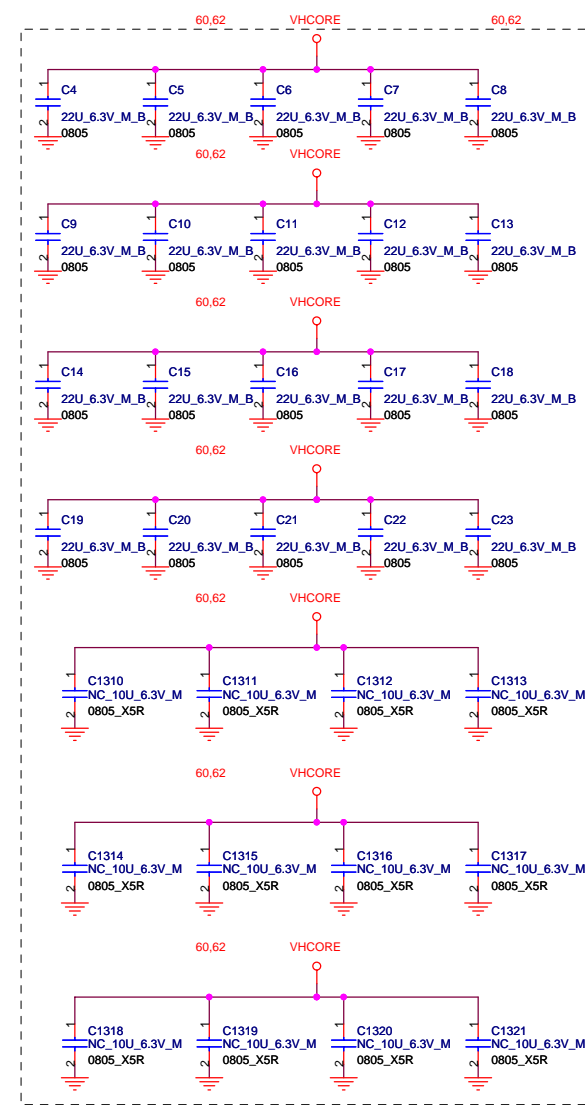
<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title      Index Page			
Size A3	Document Number MS13-1-01 (MBX-149)	Rev 1.0	
Date:	Wednesday, August 30, 2006	Sheet	1 of 67

# MBX-149(CALISTO)GAPEM/GM-Gix Block Diagram

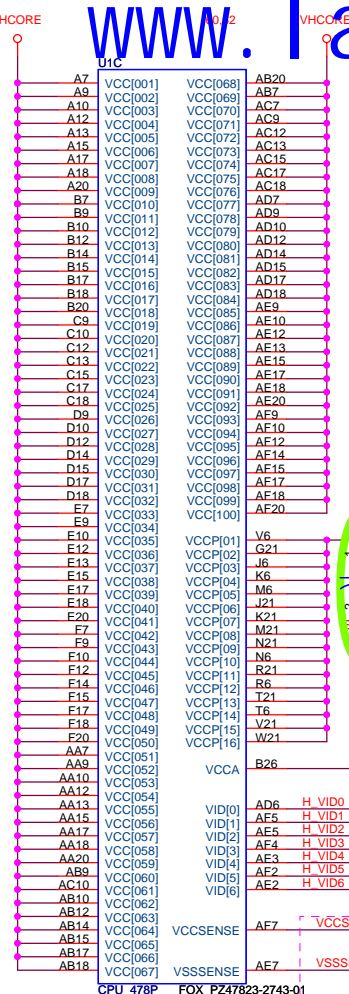






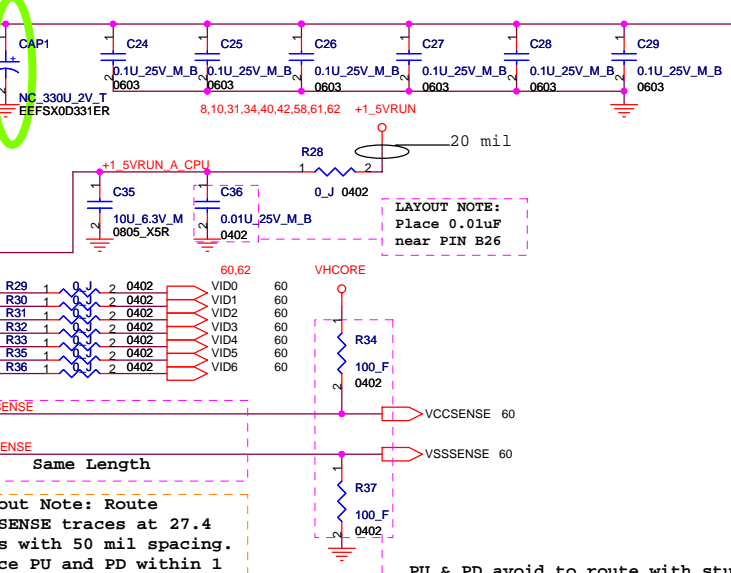


10uF \*32 instead of 22uF\*20 for 22uF 6.3V\_0805 shortage



CPU\_VCCA---->120mA  
CPU\_VCCP----->2.5A  
CPU\_VCC----->44A

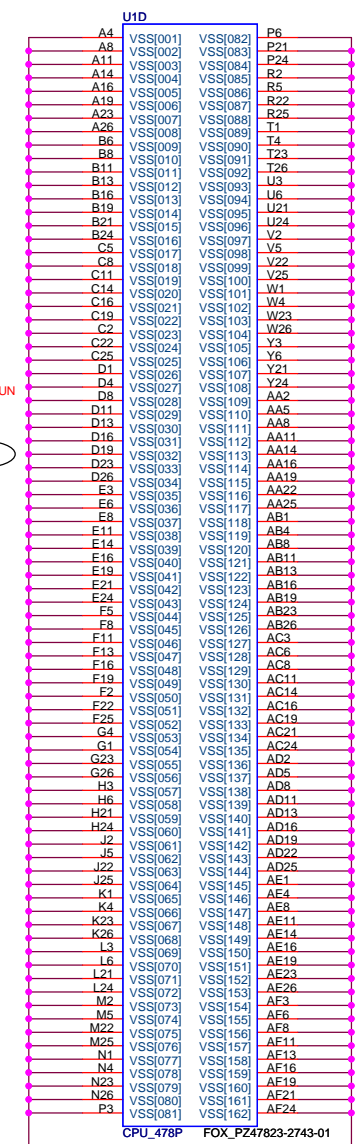
MS13 DVT Modify

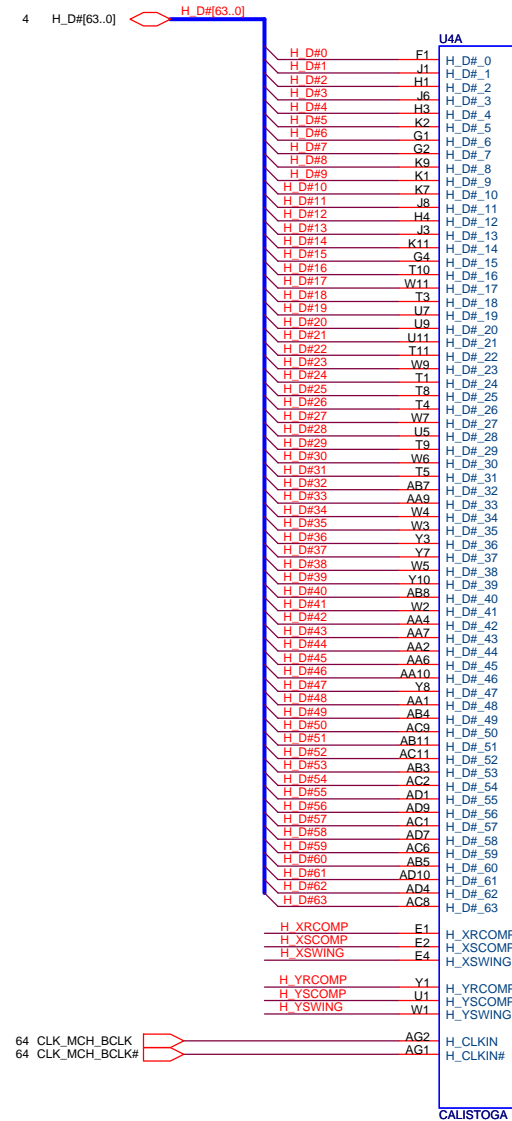
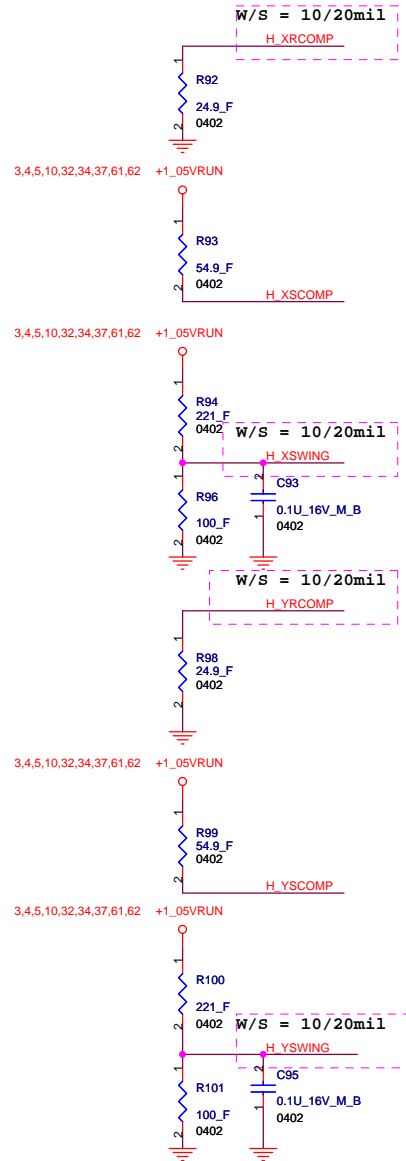


Layout Note: Route VCCSENSE traces at 27.4 Ohms with 50 mil spacing. Place PU and PD within 1 inch of cpu.  
width=18 mil  
spacing=7 mil

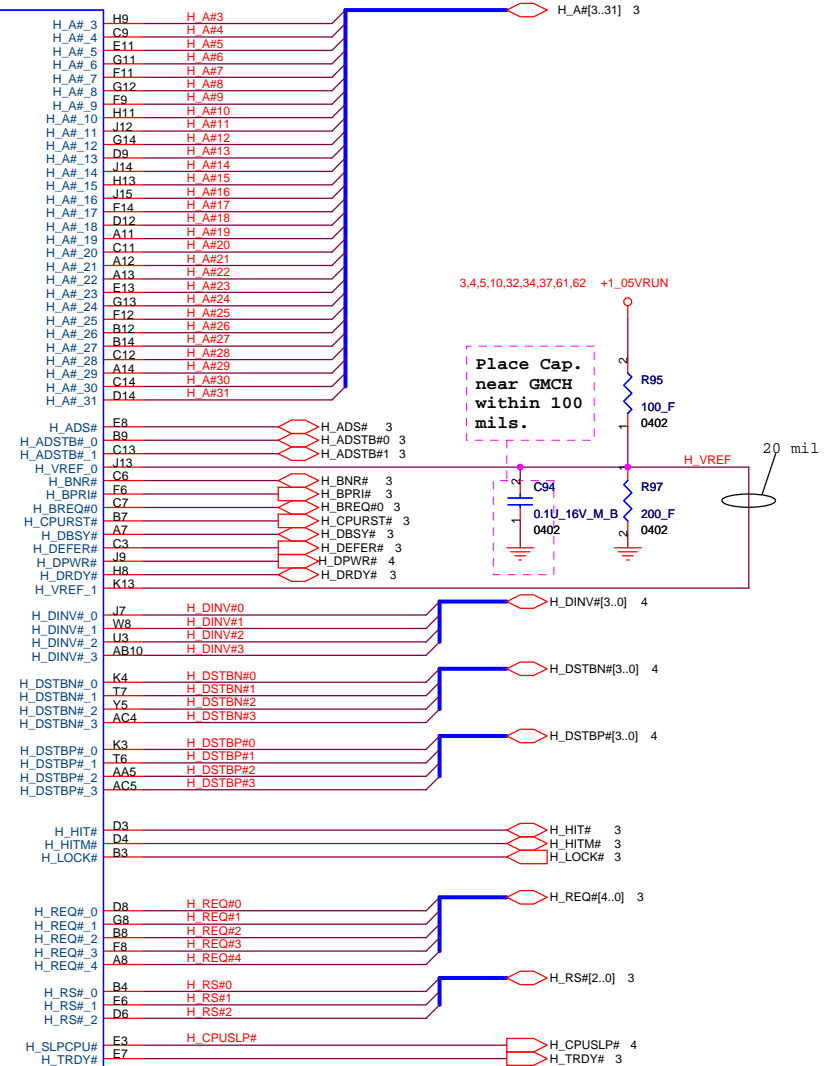
LAYOUT NOTE:  
Place 0.01uF near PIN B26

PU & PD avoid to route with stub



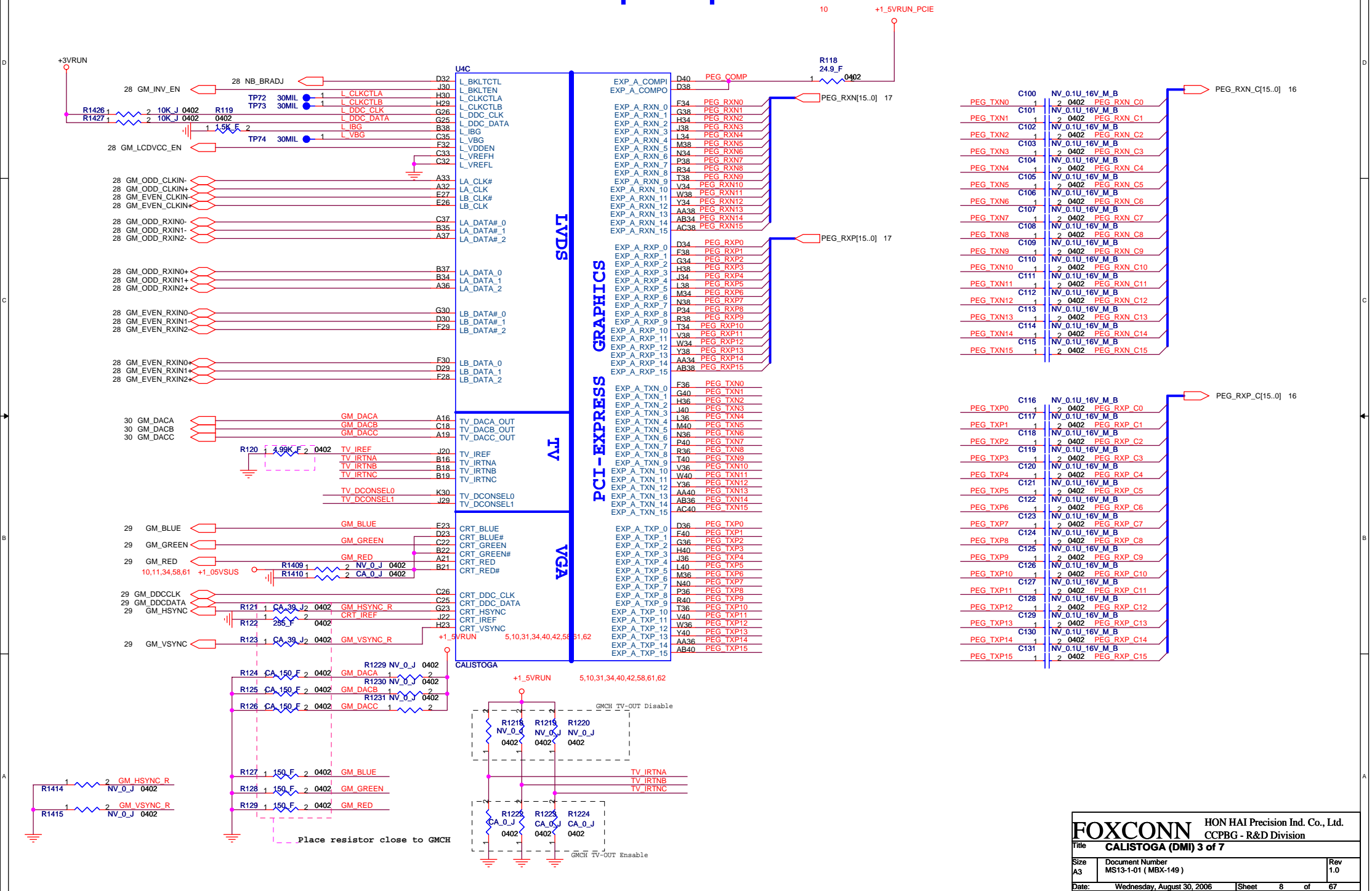


HOST

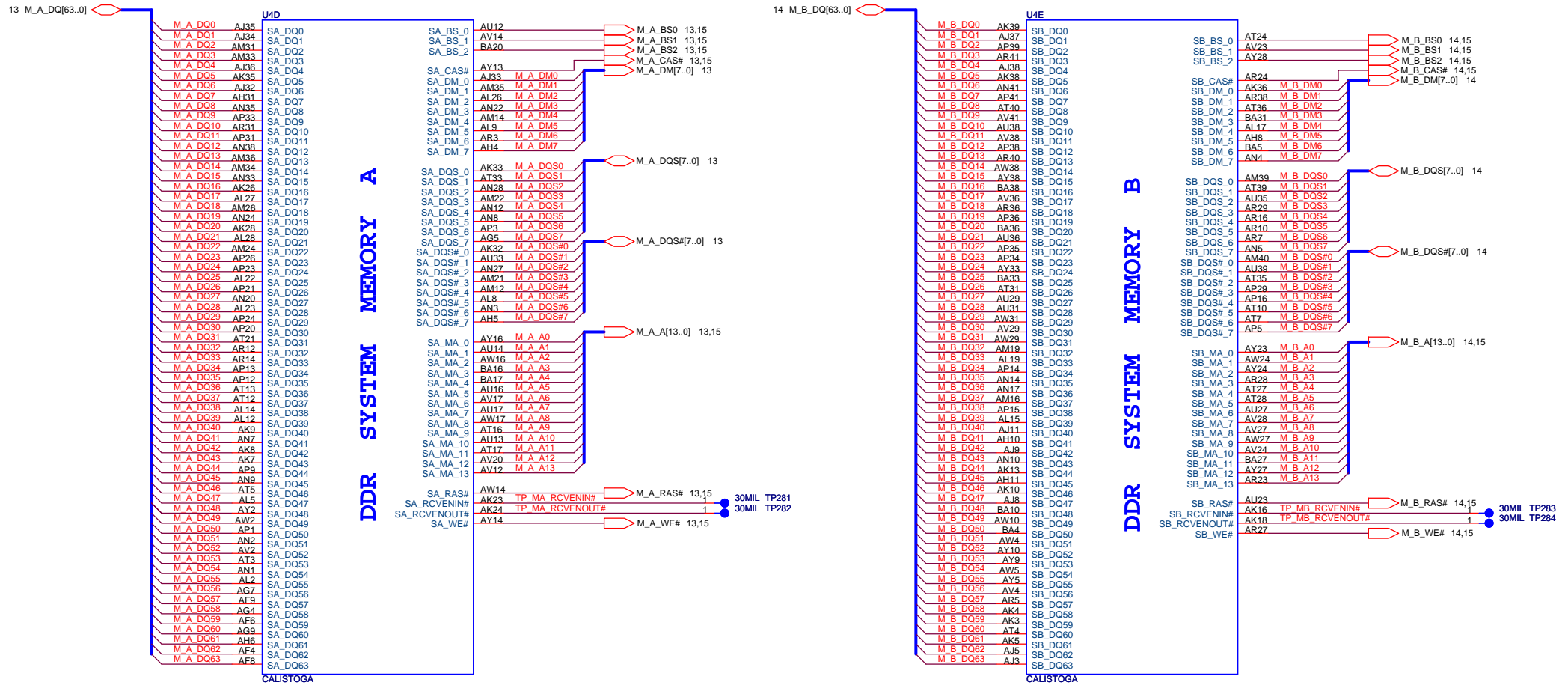


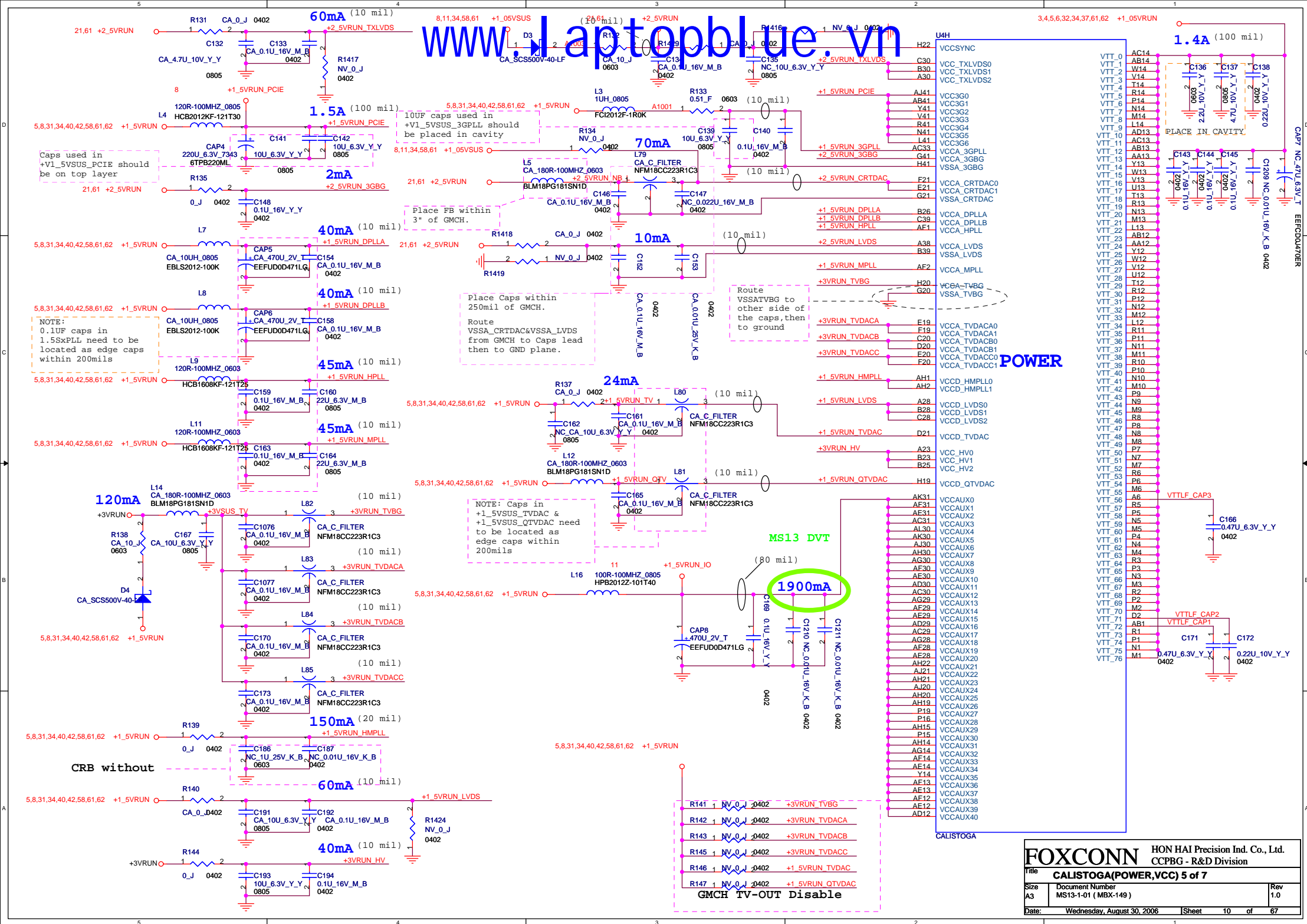




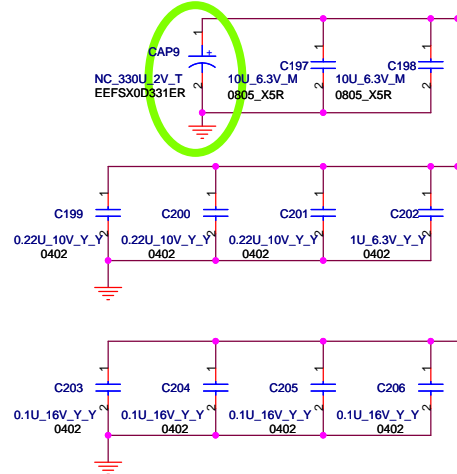








MS13 DVT Modify

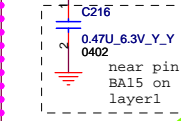
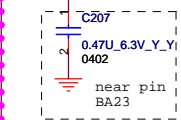


AA33 VCC\_0  
W33 VCC\_1  
P33 VCC\_2  
N33 VCC\_3  
L33 VCC\_4  
J33 VCC\_5  
AA32 VCC\_6  
Y32 VCC\_7  
W32 VCC\_8  
Y32 VCC\_9  
N32 VCC\_10  
M32 VCC\_11  
L32 VCC\_12  
J32 VCC\_13  
AA31 VCC\_14  
W31 VCC\_15  
P31 VCC\_16  
N31 VCC\_17  
M31 VCC\_18  
Y31 VCC\_19  
W30 VCC\_20  
P30 VCC\_21  
N30 VCC\_22  
M30 VCC\_23  
L30 VCC\_24  
AA29 VCC\_25  
W29 VCC\_26  
Y29 VCC\_27  
N29 VCC\_28  
M29 VCC\_29  
L29 VCC\_30  
AA28 VCC\_31  
W28 VCC\_32  
Y28 VCC\_33  
N28 VCC\_34  
M28 VCC\_35  
L28 VCC\_36  
AA27 VCC\_37  
W27 VCC\_38  
Y27 VCC\_39  
N27 VCC\_40  
M27 VCC\_41  
L27 VCC\_42  
AA26 VCC\_43  
W26 VCC\_44  
Y26 VCC\_45  
N26 VCC\_46  
M26 VCC\_47  
L26 VCC\_48  
AA25 VCC\_49  
W25 VCC\_50  
Y25 VCC\_51  
N25 VCC\_52  
M25 VCC\_53  
L25 VCC\_54  
AA24 VCC\_55  
W24 VCC\_56  
Y24 VCC\_57  
N24 VCC\_58  
M24 VCC\_59  
L24 VCC\_60  
AA23 VCC\_61  
W23 VCC\_62  
Y23 VCC\_63  
N23 VCC\_64  
M23 VCC\_65  
L23 VCC\_66  
AA22 VCC\_67  
W22 VCC\_68  
Y22 VCC\_69  
N22 VCC\_70  
M22 VCC\_71  
L22 VCC\_72  
AA21 VCC\_73  
W21 VCC\_74  
Y21 VCC\_75  
N21 VCC\_76  
M21 VCC\_77  
L21 VCC\_78  
AA20 VCC\_79  
W20 VCC\_80  
Y20 VCC\_81  
N20 VCC\_82  
M20 VCC\_83  
L20 VCC\_84  
AA19 VCC\_85  
W19 VCC\_86  
Y19 VCC\_87  
N19 VCC\_88  
M19 VCC\_89  
L19 VCC\_90  
AA18 VCC\_91  
W18 VCC\_92  
Y18 VCC\_93  
N18 VCC\_94  
M18 VCC\_95  
L18 VCC\_96  
AA17 VCC\_97  
W17 VCC\_98  
Y17 VCC\_99  
N17 VCC\_100  
M17 VCC\_101  
L17 VCC\_102  
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W16 VCC\_104  
Y16 VCC\_105  
N16 VCC\_106  
M16 VCC\_107  
L16 VCC\_108

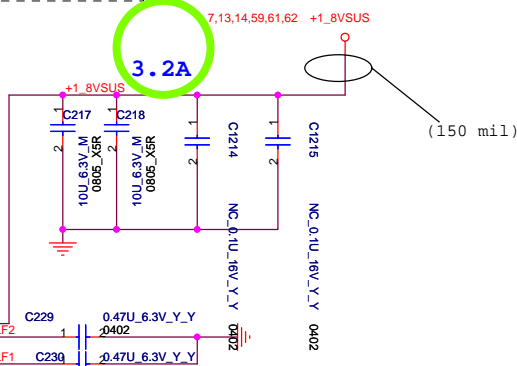
VCC

VCC\_SM\_1 U41  
VCC\_SM\_2 AM41  
VCC\_SM\_3 AU40  
VCC\_SM\_4 AX34  
VCC\_SM\_5 AW34  
VCC\_SM\_6 AV34  
VCC\_SM\_7 AU34  
VCC\_SM\_8 AT34  
VCC\_SM\_9 BA30  
VCC\_SM\_10 AY30  
VCC\_SM\_11 AW30  
VCC\_SM\_12 AV30  
VCC\_SM\_13 AU30  
VCC\_SM\_14 AT30  
VCC\_SM\_15 AR30  
VCC\_SM\_16 AP30  
VCC\_SM\_17 AN30  
VCC\_SM\_18 AM29  
VCC\_SM\_19 AL29  
VCC\_SM\_20 AK29  
VCC\_SM\_21 AJ29  
VCC\_SM\_22 AH29  
VCC\_SM\_23 AI28  
VCC\_SM\_24 AJ28  
VCC\_SM\_25 AK28  
VCC\_SM\_26 AL28  
VCC\_SM\_27 AH28  
VCC\_SM\_28 AI27  
VCC\_SM\_29 AJ27  
VCC\_SM\_30 AK27  
VCC\_SM\_31 AL27  
VCC\_SM\_32 AV26  
VCC\_SM\_33 AU26  
VCC\_SM\_34 AT26  
VCC\_SM\_35 AR26  
VCC\_SM\_36 AP26  
VCC\_SM\_37 AN26  
VCC\_SM\_38 AJ25  
VCC\_SM\_39 AK25  
VCC\_SM\_40 AI25  
VCC\_SM\_41 AJ24  
VCC\_SM\_42 AK24  
VCC\_SM\_43 AI23  
VCC\_SM\_44 BA22  
VCC\_SM\_45 AY22  
VCC\_SM\_46 AX22  
VCC\_SM\_47 AV22  
VCC\_SM\_48 AU22  
VCC\_SM\_49 AT22  
VCC\_SM\_50 AR22  
VCC\_SM\_51 AP22  
VCC\_SM\_52 AK22  
VCC\_SM\_53 AJ22  
VCC\_SM\_54 AI21  
VCC\_SM\_55 BA20  
VCC\_SM\_56 AY19  
VCC\_SM\_57 AX19  
VCC\_SM\_58 AV19  
VCC\_SM\_59 AU19  
VCC\_SM\_60 AT19  
VCC\_SM\_61 AR19  
VCC\_SM\_62 AP19  
VCC\_SM\_63 AK19  
VCC\_SM\_64 AJ19  
VCC\_SM\_65 AI18  
VCC\_SM\_66 AH17  
VCC\_SM\_67 AJ17  
VCC\_SM\_68 AI16  
VCC\_SM\_69 BA15  
VCC\_SM\_70 AY15  
VCC\_SM\_71 AX15  
VCC\_SM\_72 AV15  
VCC\_SM\_73 AU15  
VCC\_SM\_74 AT15  
VCC\_SM\_75 AR15  
VCC\_SM\_76 AP15  
VCC\_SM\_77 AK15  
VCC\_SM\_78 AJ15  
VCC\_SM\_79 AI14  
VCC\_SM\_80 AH13  
VCC\_SM\_81 AJ13  
VCC\_SM\_82 AI12  
VCC\_SM\_83 AH12  
VCC\_SM\_84 AG12  
VCC\_SM\_85 AK11  
VCC\_SM\_86 AJ11  
VCC\_SM\_87 AI10  
VCC\_SM\_88 AH9  
VCC\_SM\_89 AJ8  
VCC\_SM\_90 AI8  
VCC\_SM\_91 AH7  
VCC\_SM\_92 AJ6  
VCC\_SM\_93 AI6  
VCC\_SM\_94 AH5  
VCC\_SM\_95 AJ4  
VCC\_SM\_96 AI4  
VCC\_SM\_97 AH3  
VCC\_SM\_98 AJ2  
VCC\_SM\_99 AI2  
VCC\_SM\_100 AH1  
VCC\_SM\_101 AJ0  
VCC\_SM\_102 AI0  
VCC\_SM\_103 AH0  
VCC\_SM\_104 AJ0  
VCC\_SM\_105 AI0  
VCC\_SM\_106 AH0  
VCC\_SM\_107 AJ0

Note: All VCCSM pins shorted internally.



MS13 DVT



NCTF

CALISTOGA

7 MCH\_CFG\_5 1 30MIL TP554

MCH\_CFG\_5  
Low = DMIX2  
High = DMIX4

7 MCH\_CFG\_6 1 30MIL TP556

MCH\_CFG\_6  
Low = Moby Dick  
High = Calistoga  
DDR2 select (default high)

7 MCH\_CFG\_7 1 30MIL TP557

MCH\_CFG\_7  
(CPU Strap)  
Low = RSVD  
High = Mobile Yonah processor

7 MCH\_CFG\_9 1 30MIL TP559

MCH\_CFG\_9  
(PCIe Graphics Lane)  
Low = Reverse Lane  
High = Normal operation

For layout convenience

7 MCH\_CFG\_10 1 30MIL TP560

MCH\_CFG\_10  
(HOST PLL VCC SELECT)  
Low = RESERVED  
High = MOBILITY

7 MCH\_CFG\_11 1 30MIL TP561

MCH\_CFG\_11  
(PSB 4x CLK ENABLE)  
Low = Calistoga  
High = Reserved

7 MCH\_CFG\_12 1 30MIL TP562

7 MCH\_CFG\_13 1 30MIL TP563

MCH\_CFG\_13:12  
(XOR/ALLZ)  
00=Partial Clock Gating Disable  
01=XOR Mode Enable  
10=All-Z Mode Enable  
11=Normal Operation(Default)

7 MCH\_CFG\_16 1 30MIL TP564

MCH\_CFG\_16  
(FSB Dynamic ODT)  
Low = Dynamic ODT Disabled  
High = Dynamic ODT Enable

MCH\_CFG\_18  
(VCC\_CORE Select)  
Low = 1.05V(default)  
High = 1.5V

7 MCH\_CFG\_18 1 30MIL TP555

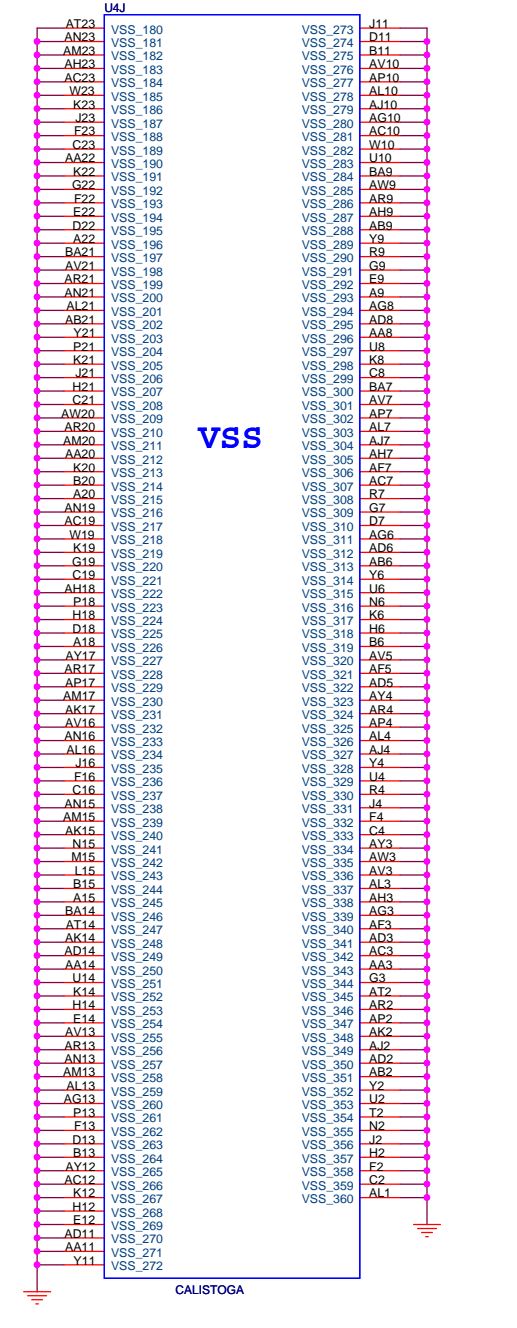
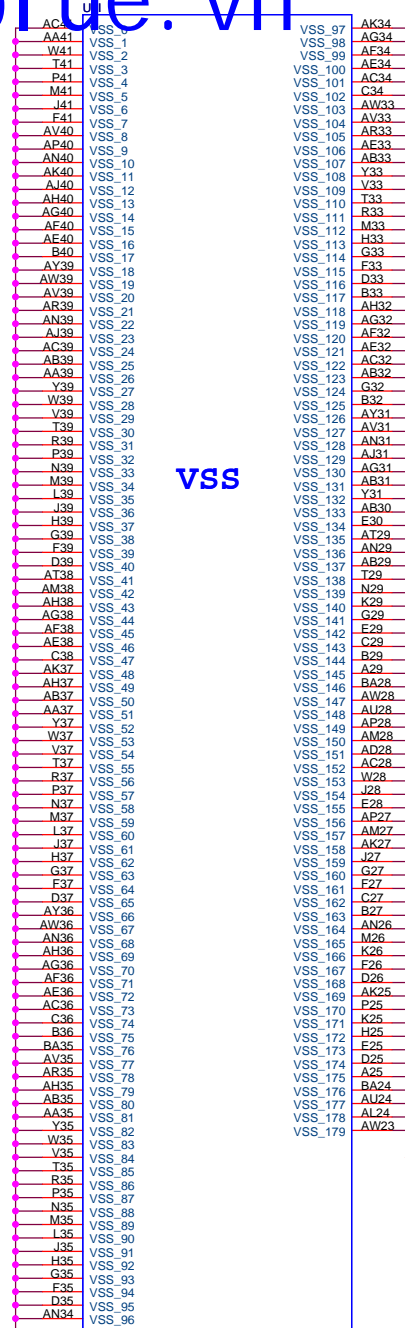
MCH\_CFG\_19  
(DMI LANE REVERSAL)  
Low = Normal(default)  
High = LANES REVERSED

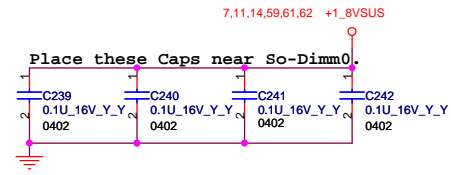
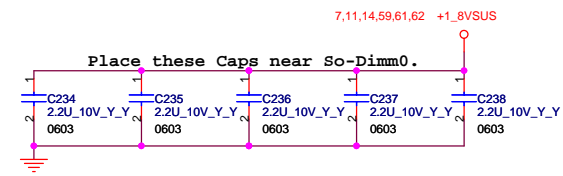
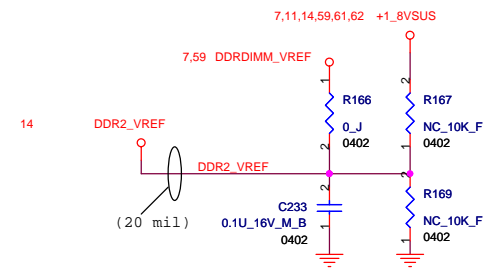
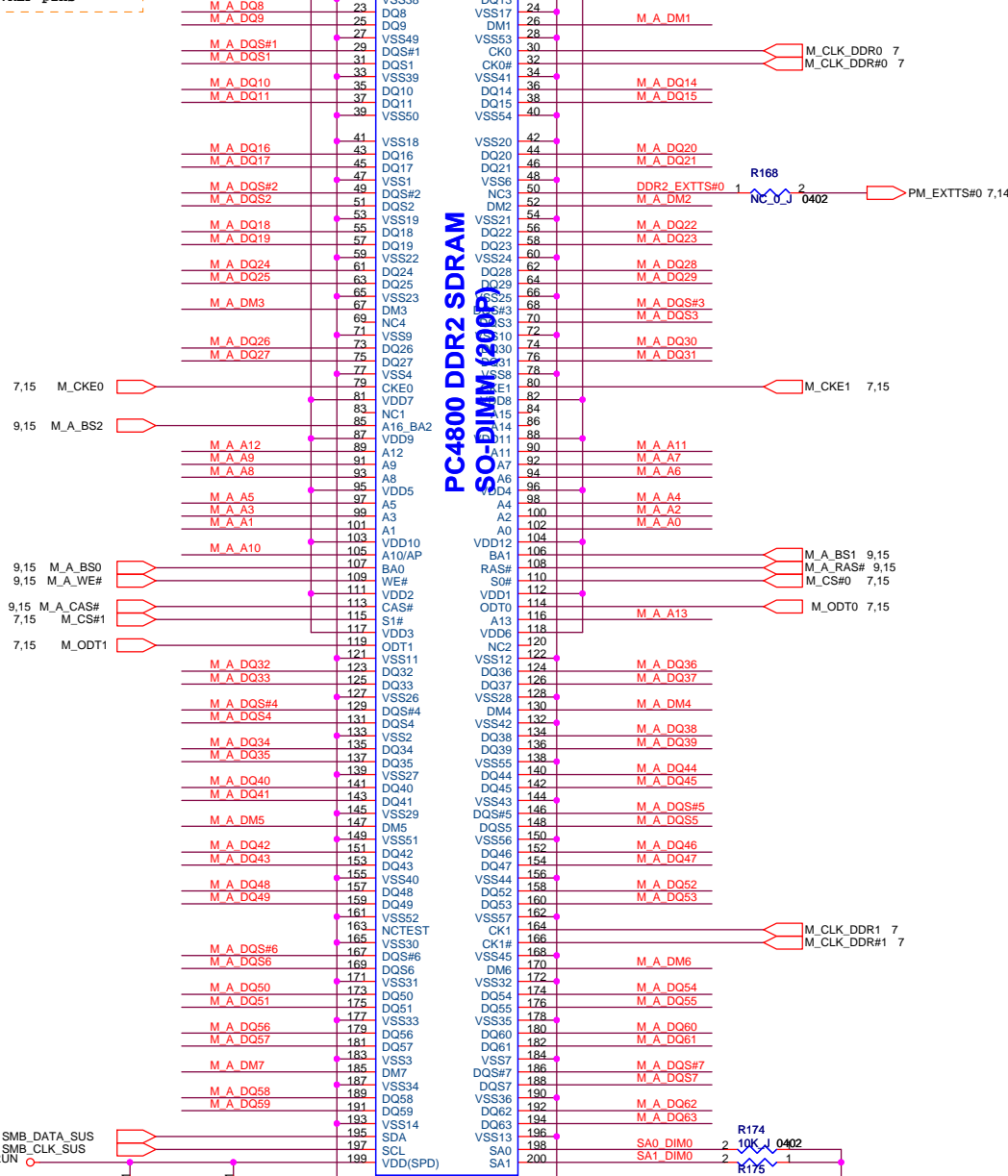
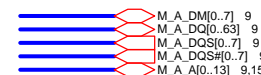
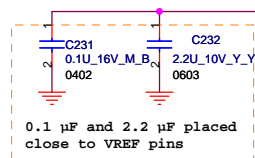
7 MCH\_CFG\_19 1 30MIL TP558

MCH\_CFG\_20  
(PCIe Backward Interoperability mode)  
Low = Only SDVO or PCIE x1 is operational (defaults)  
High = SDVO and PCIE x1 are operating simultaneously via the PEG port

7 MCH\_CFG\_20 1 30MIL TP561

Layout Noe:  
Location of all MCH\_CFG strap resistors needs to be close to trace to minimize stub

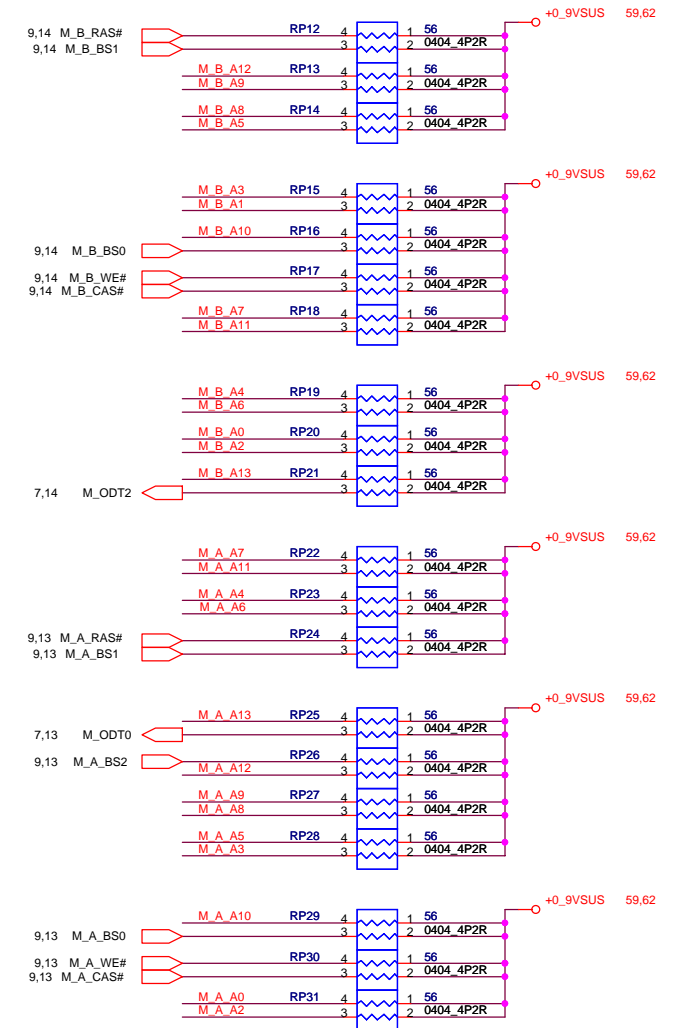
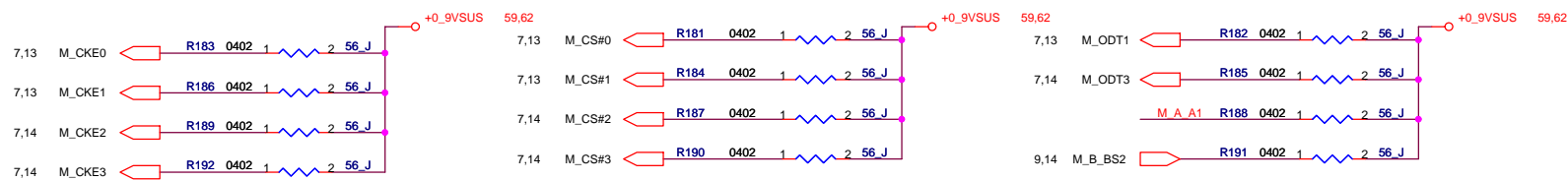
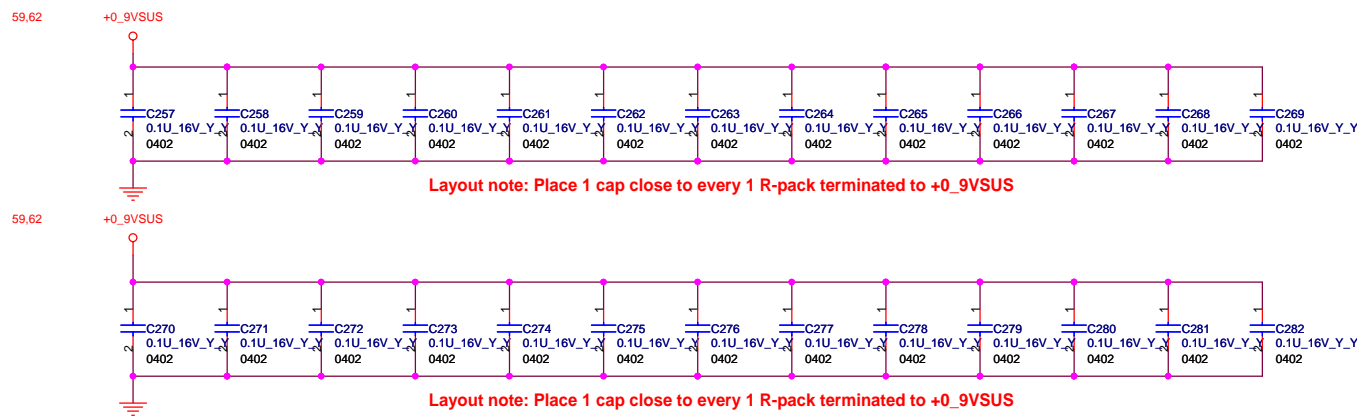


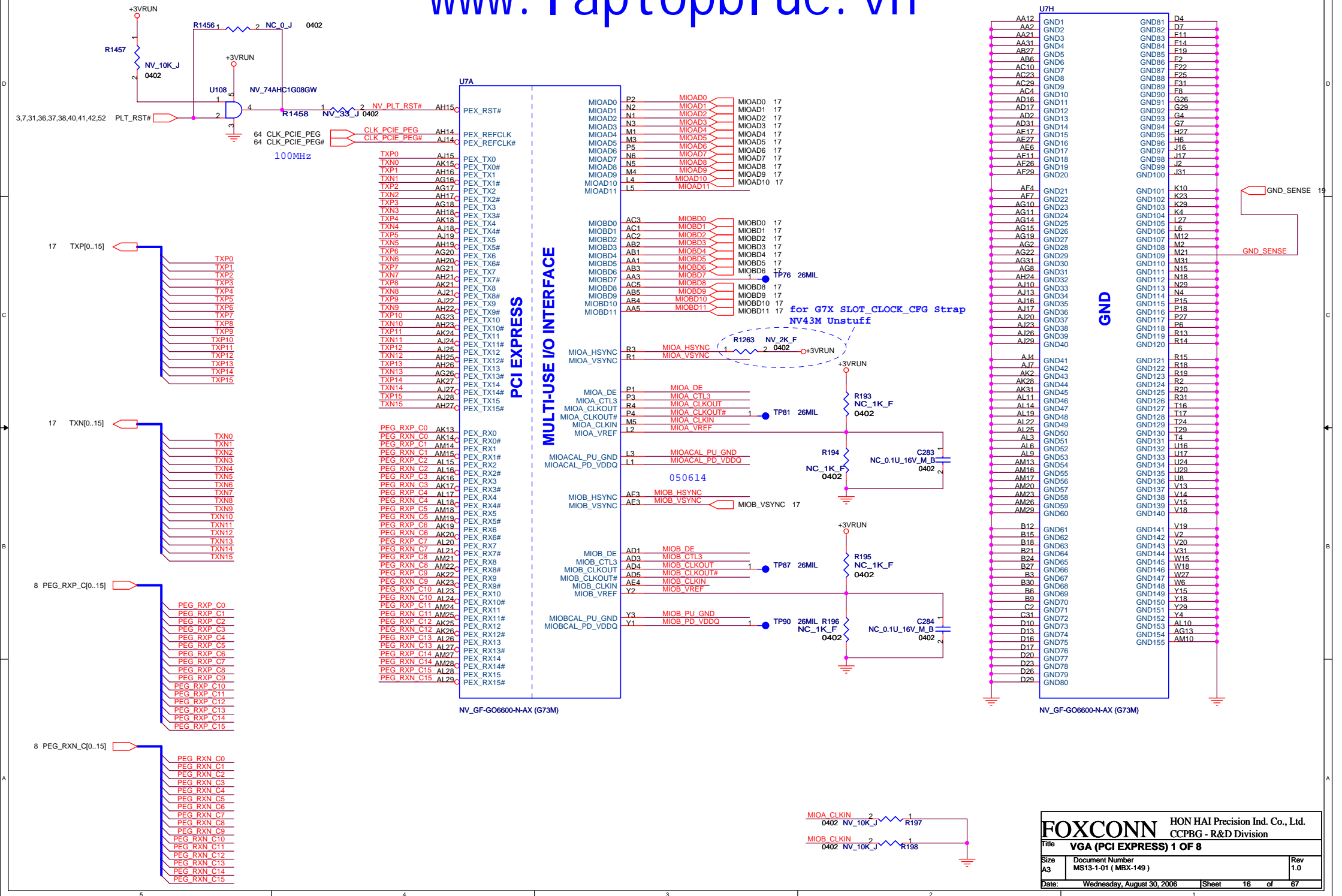




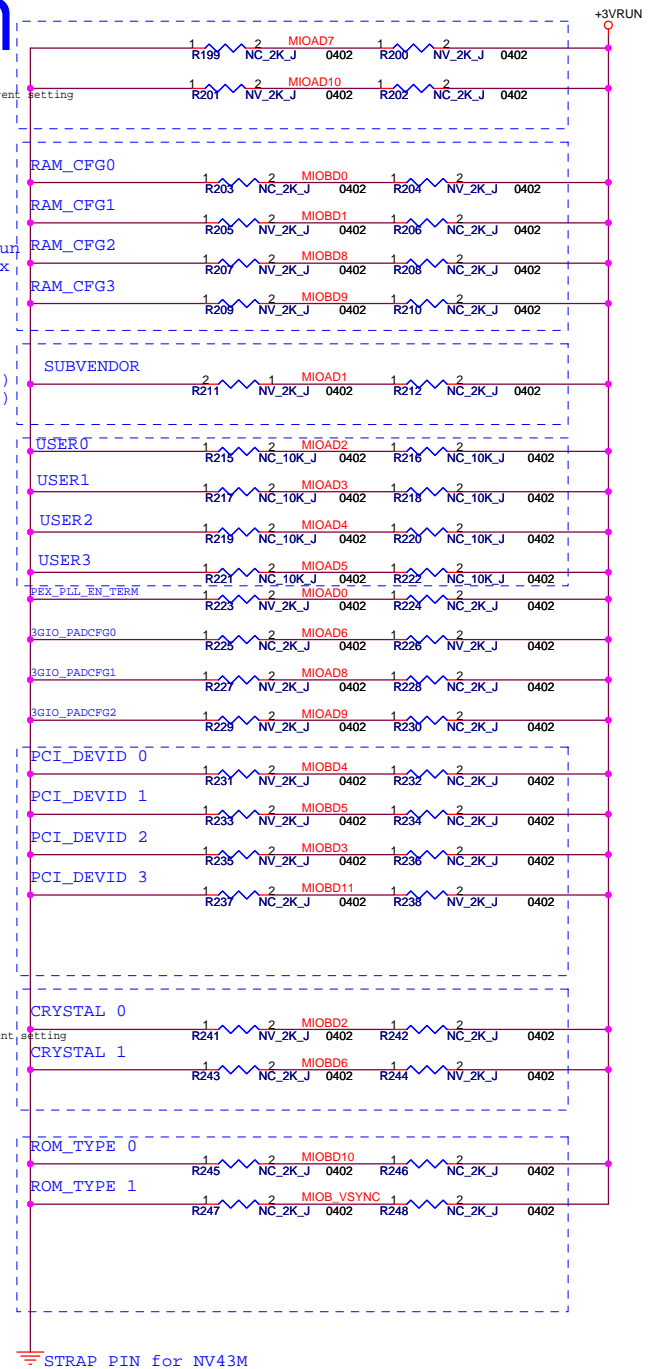
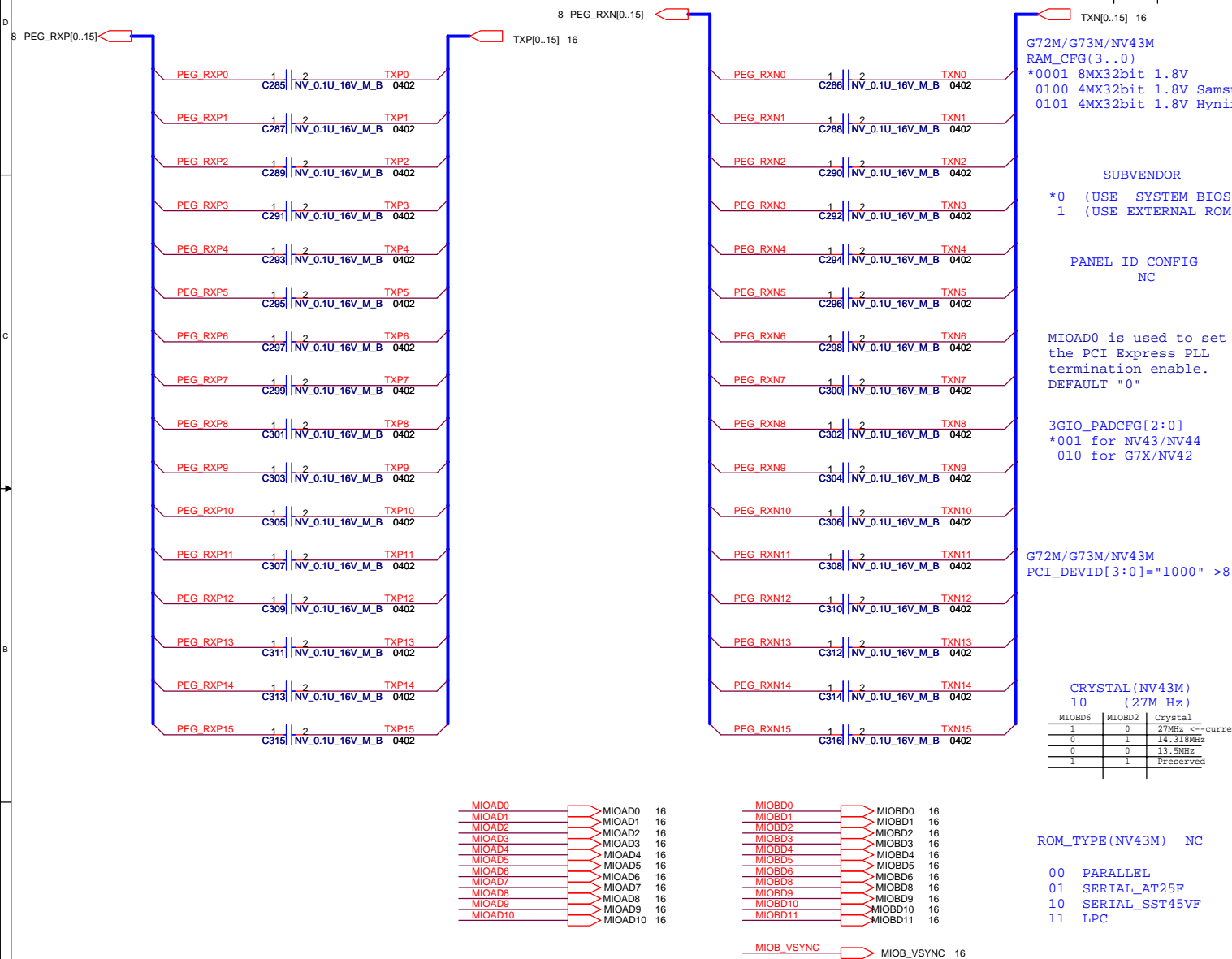


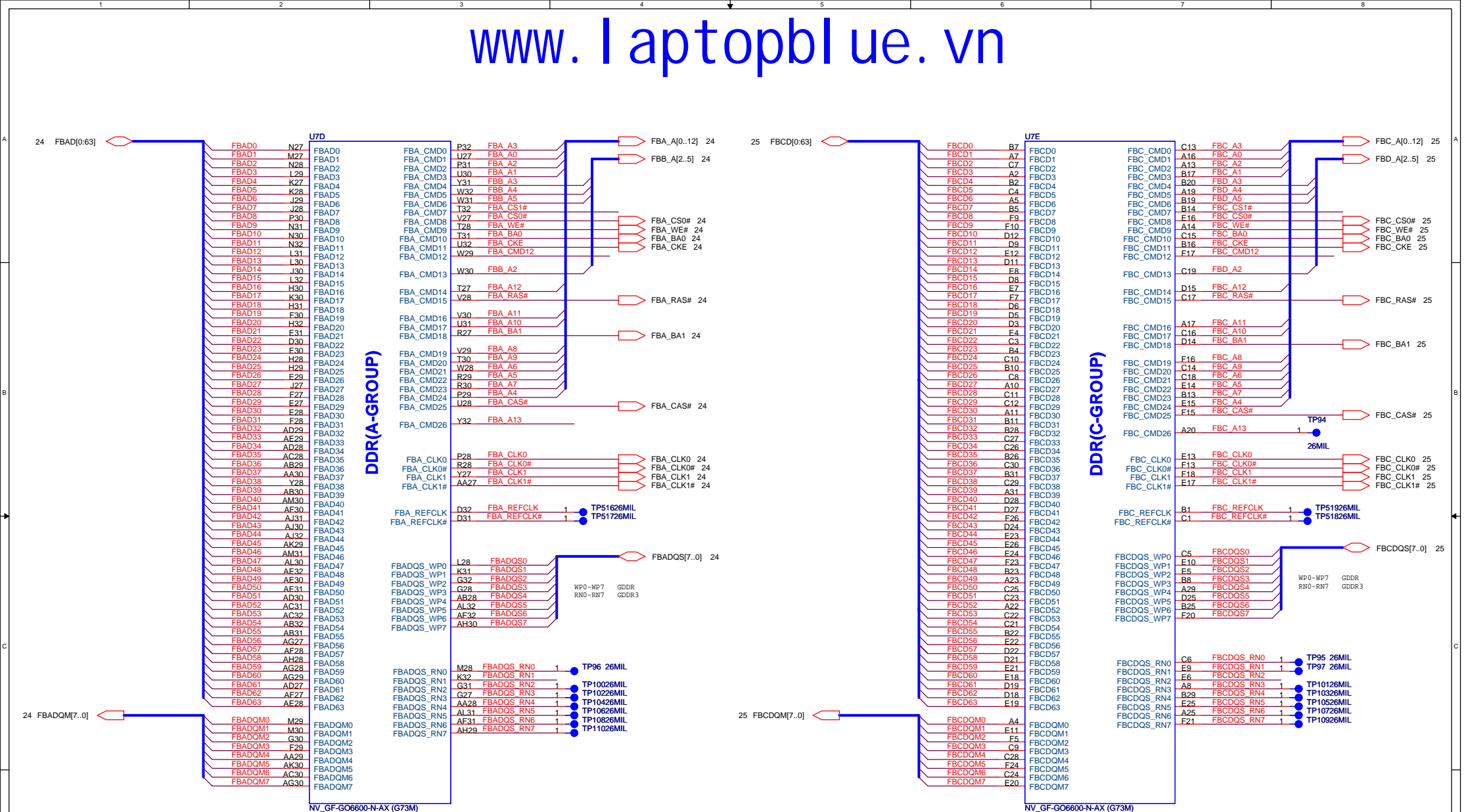


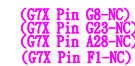




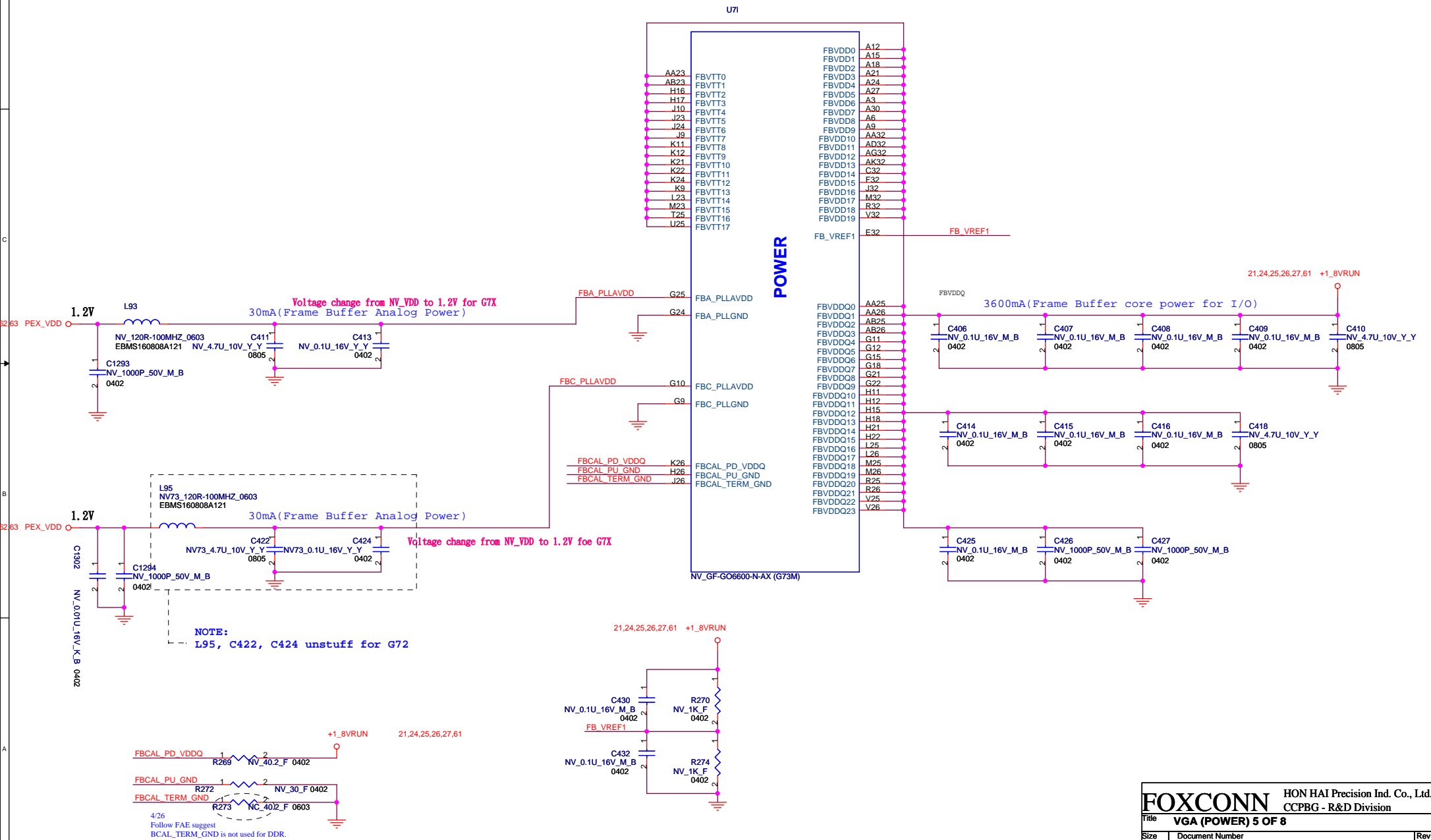
TV MODE(NV43M)			
NTSC (01)			
MIOAD10	MIOAD7	SECAM	
0	0	SECAM	
0	1	NTSC <---current setting	
1	0	PAL	
1	1	CRT	



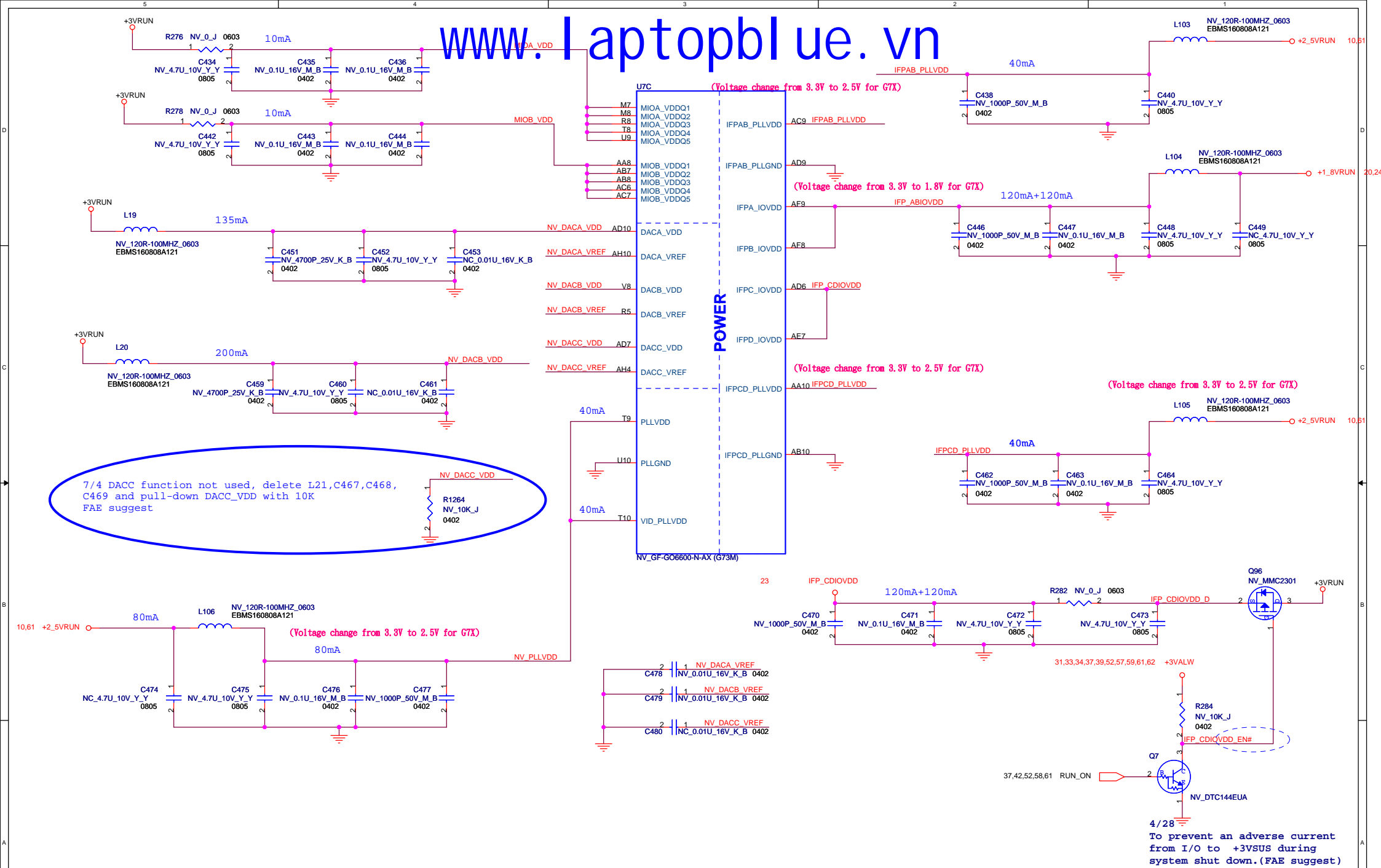


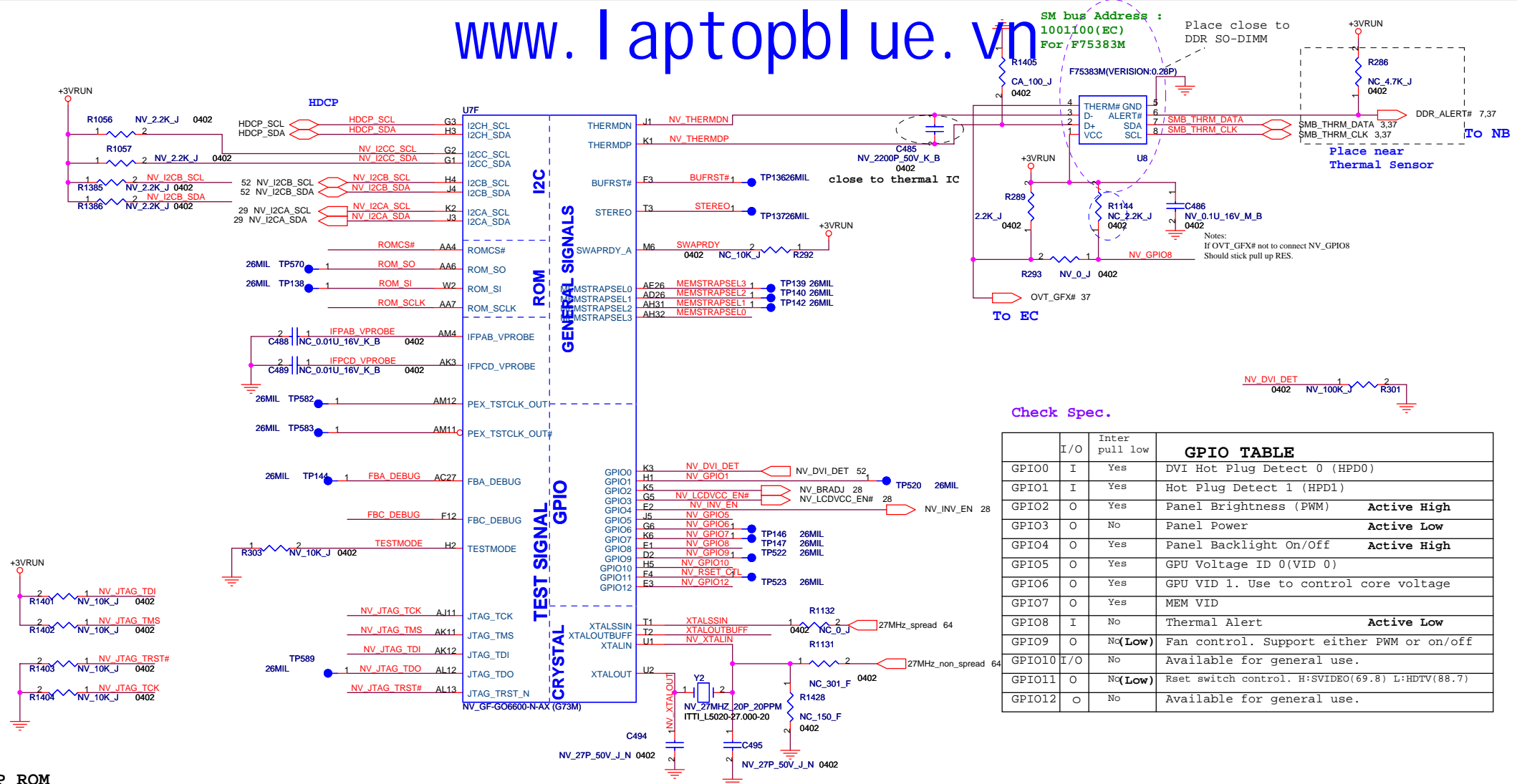


<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title <b>VGA (GDDR/2C/ROM) 4 OF 8</b>			
Size A3	Document Number MS13-1-01 (MBX-149)	Rev 1.0	
Date:	Wednesday, August 30, 2006	Sheet	19 of 67



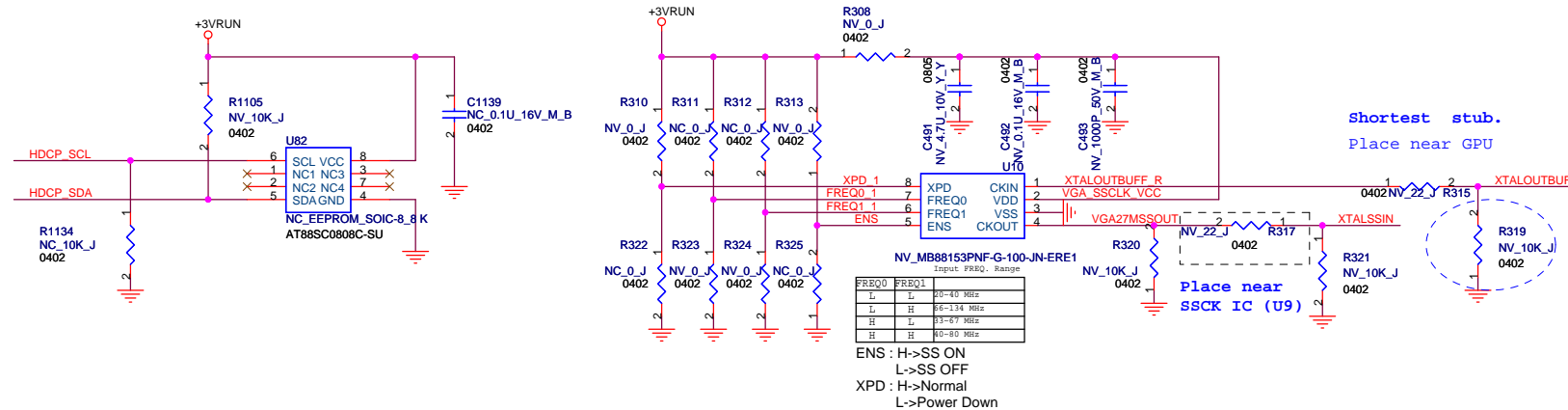


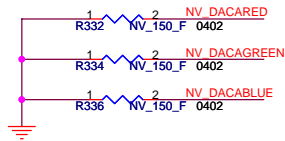




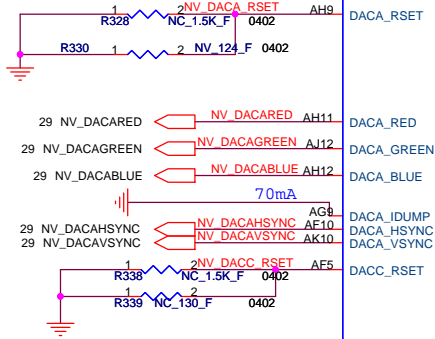
	I/O	Inter pull low	GPIO TABLE
GPIO0	I	Yes	DVI Hot Plug Detect 0 (HPD0)
GPIO1	I	Yes	Hot Plug Detect 1 (HPD1)
GPIO2	O	Yes	Panel Brightness (PWM) <b>Active High</b>
GPIO3	O	No	Panel Power <b>Active Low</b>
GPIO4	O	Yes	Panel Backlight On/Off <b>Active High</b>
GPIO5	O	Yes	GPU Voltage ID 0 (VID 0)
GPIO6	O	Yes	GPU VID 1. Use to control core voltage
GPIO7	O	Yes	MEM VID
GPIO8	I	No	Thermal Alert <b>Active Low</b>
GPIO9	O	No (Low)	Fan control. Support either PWM or on/off
GPIO10	I/O	No	Available for general use.
GPIO11	O	No (Low)	Rset switch control. H:SVIDEO(69.8) L:HDTV(88.7)
GPIO12	O	No	Available for general use.

## HDCP ROM



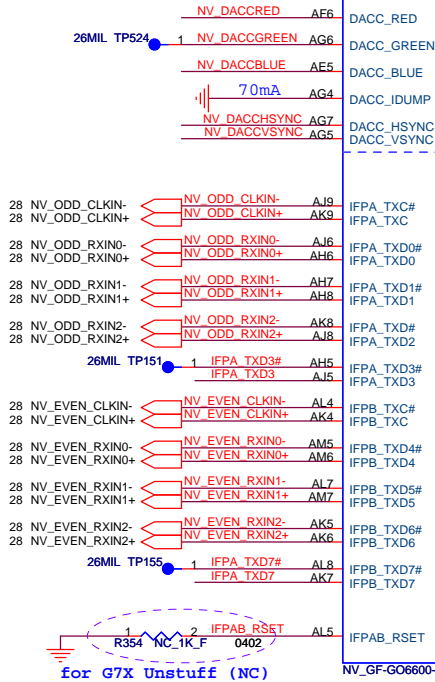


CLOSE TO GPU

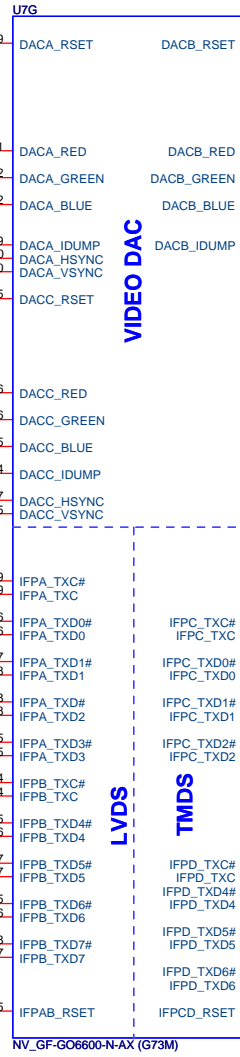


CLOSE TO GPU

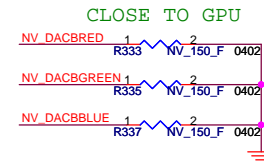
DACA	VGA-CRT			I2CA
DACA-RED	R			
DACA-GREEN	G			
DACA-BLUE	B			
DACA-HSYNC	HSYNC			
DACA-VSYNC	VSYNC			
	VGA-DDCLK			SCL
	VGA-DDCDA			SDA
DACB	S-VIDEO	COMPOSITE	D-CONNECTOR	I2CC
DACB-RED	C		PR	
DACB-GREEN	Y		Y	
DACB-BLUE		COMPOSITE		
			LINE1	SCL
			LINE2	SDA
			LINE3	
DACC	DVI-I			I2CB
DACC-RED	R			
DACC-GREEN	G			
DACC-BLUE	B			
DACC-HSYNC	HSYNC			
DACC-VSYNC	VSYNC			
	DVI-DDCLK			SCL
	DVI-DDCDA			SDA



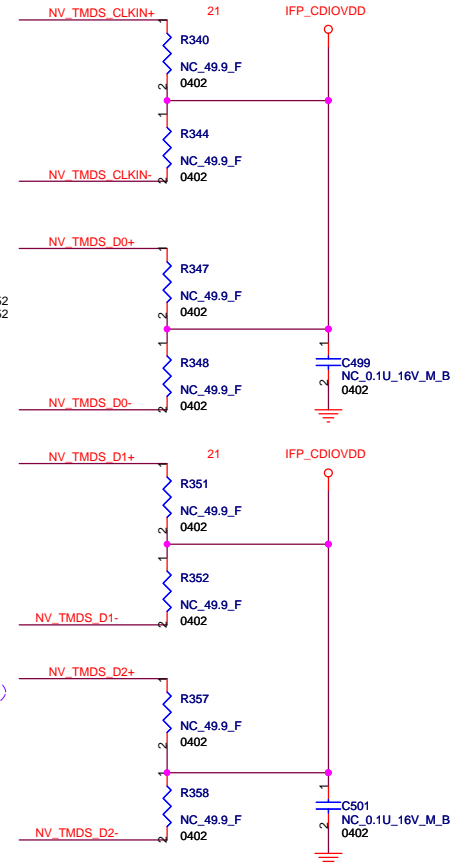
for G7X Unstuff (NC)

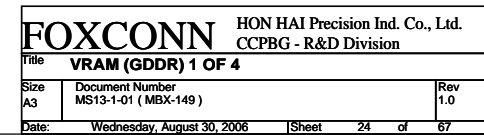


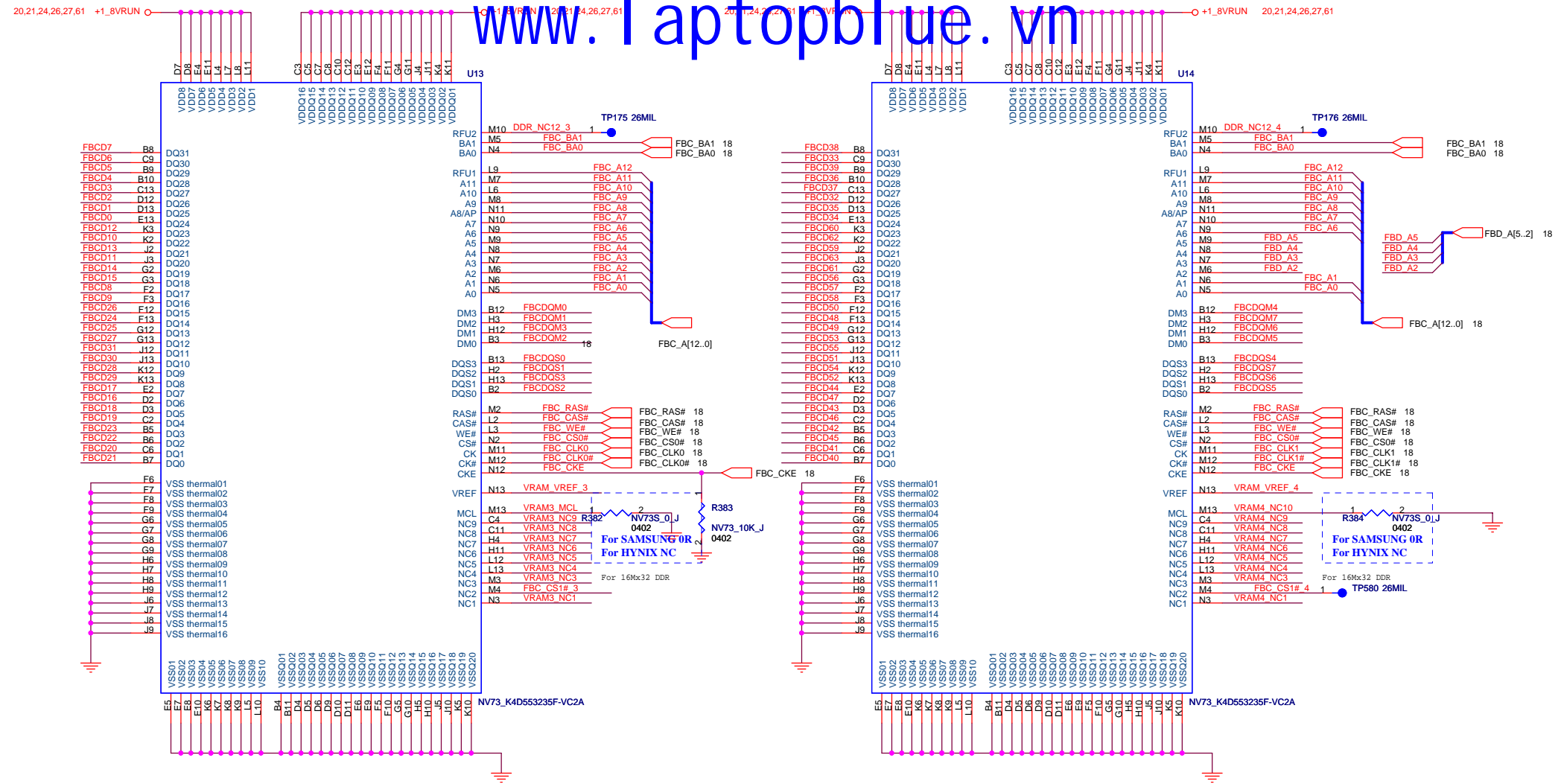
for G7X Unstuff (NC)



CLOSE TO GPU







Three circuit diagrams illustrating the VRAM\_VREF pin connections for different GPU models (G7X and NV43M).

**Left Diagram (G7X):** Shows the connection of the VRAM\_VREF pin to the VRAM\_VREF pin of the GPU. The circuit includes a power supply (+1.8VRUN), a resistor (R389), a capacitor (C507), and a variable capacitor (NV73\_01U\_16V\_M\_B). The VRAM\_VREF pin is connected to the VRAM\_VREF pin of the GPU.

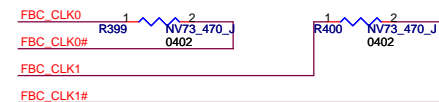
**Middle Diagram (NV43M):** Shows the connection of the VRAM\_VREF pin to the VRAM\_VREF pin of the GPU. The circuit includes a power supply (+1.8VRUN), a resistor (R391), a capacitor (C507), and a variable capacitor (NV73\_01U\_16V\_M\_B). The VRAM\_VREF pin is connected to the VRAM\_VREF pin of the GPU.

**Right Diagram (G7X):** Shows the connection of the VRAM\_VREF pin to the VRAM\_VREF pin of the GPU. The circuit includes a power supply (+1.8VRUN), a resistor (R390), a capacitor (C508), and a variable capacitor (NV73\_01U\_16V\_M\_B). The VRAM\_VREF pin is connected to the VRAM\_VREF pin of the GPU.

**Table of Pin Connections (Right Diagram):**

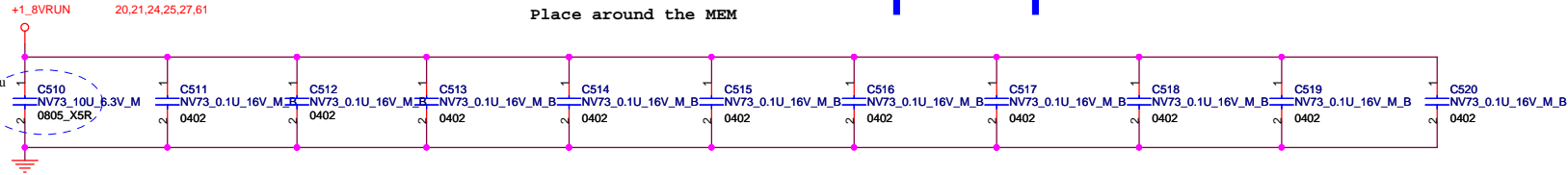
Pin	Value	Pin	Value
VRAM4_NC7	1	TP184	26MIL
VRAM4_NC6	1	TP186	26MIL
VRAM4_NC5	1	TP188	26MIL
VRAM4_NC4	1	TP189	26MIL
VRAM4_NC3	1	TP191	26MIL
VRAM4_NC1	1	TP192	26MIL

If use G72M, please unstuff U13, U14 and their related circuit

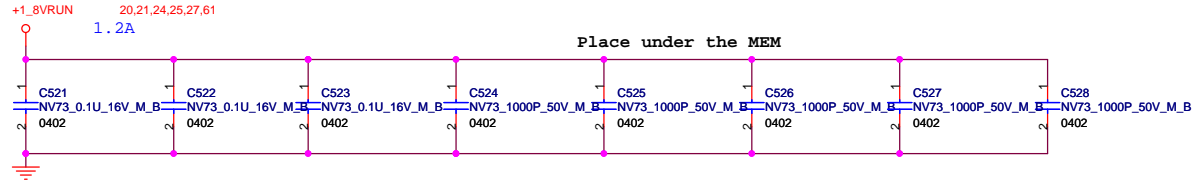


Decoupling for right MEMORY

Place around the MEM

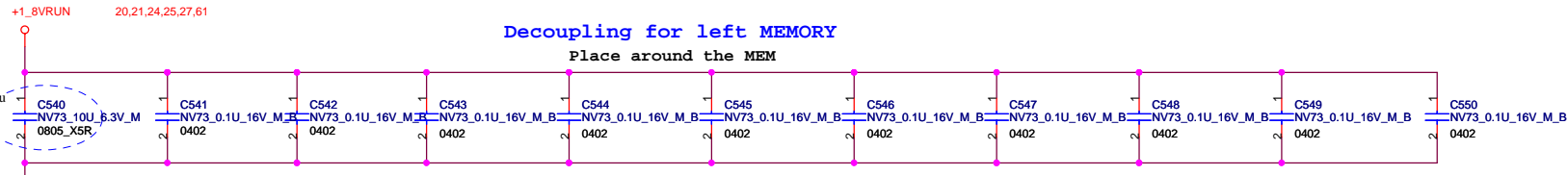


Place under the MEM

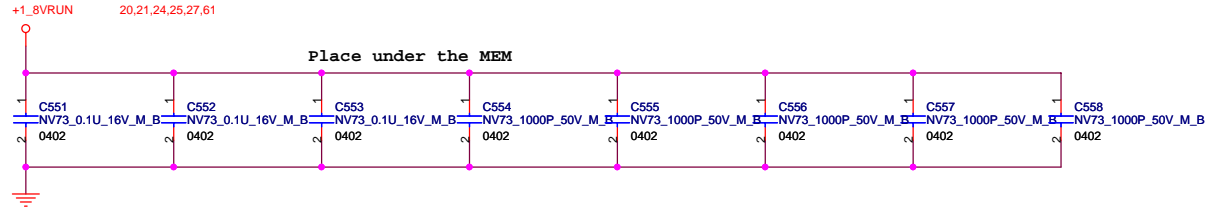


Decoupling for left MEMORY

Place around the MEM

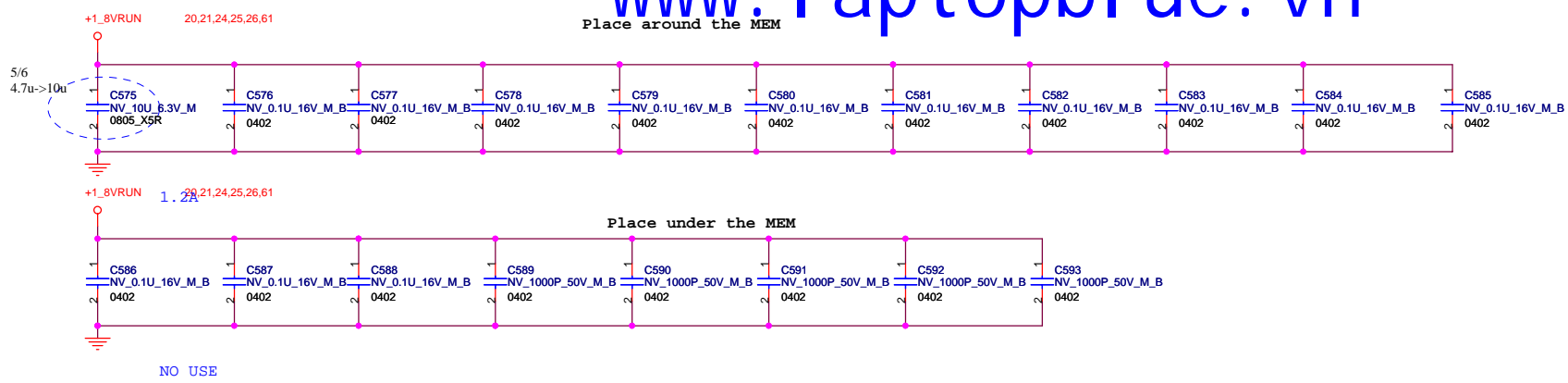


Place under the MEM

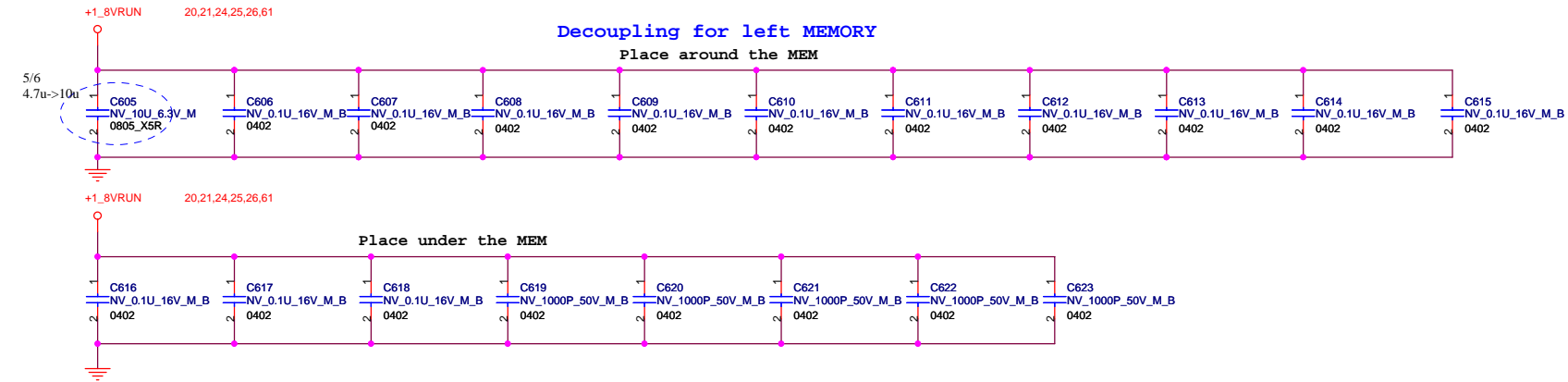




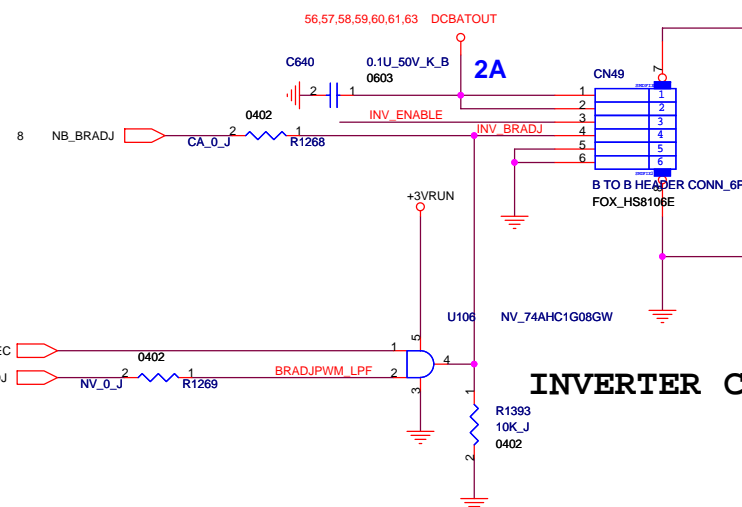
Decoupling for right MEMORY  
Place around the MEM



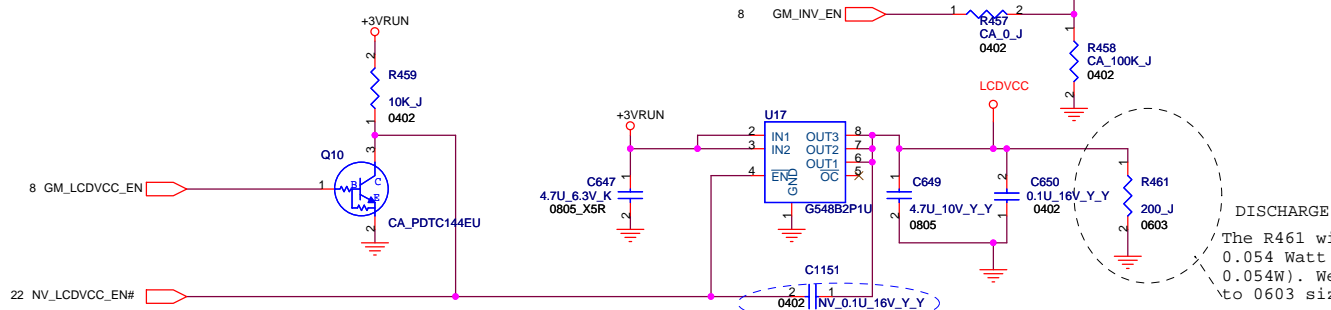
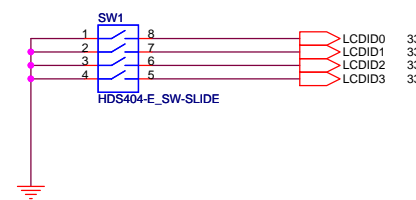
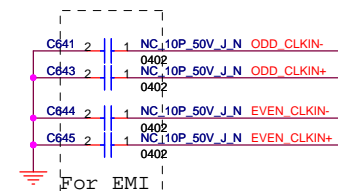
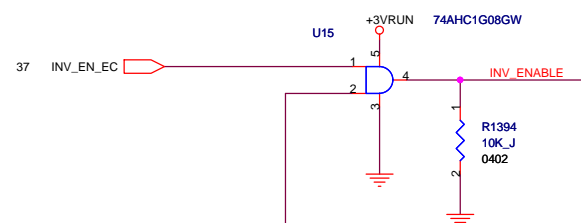
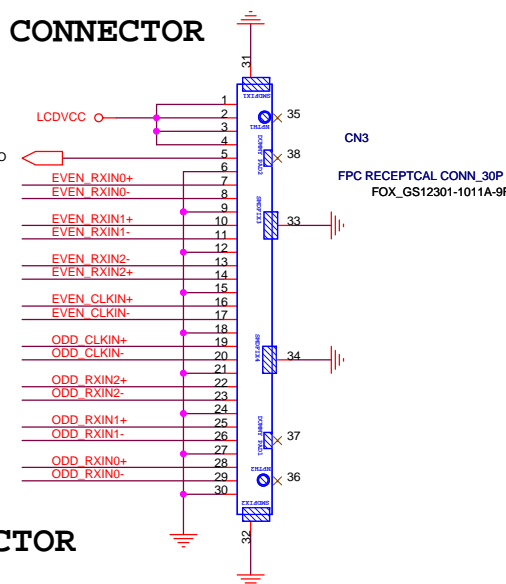
Decoupling for left MEMORY  
Place around the MEM



## LVDS CONNECTOR



## INVERTER CONNECTOR



Type	WXGA	WXGA-HC	WSXGA+
Size	15.4" wide	15.4" wide	15.4" wide
Vendor	Hitachi	Hitachi	Hitachi
Device Name	TX39D81VC1AAA	TX39D80VC1GAA	TX39D90VC1GAA
Panel ID Cheek[3..0]	1000	1000	1100

DISCHARGE

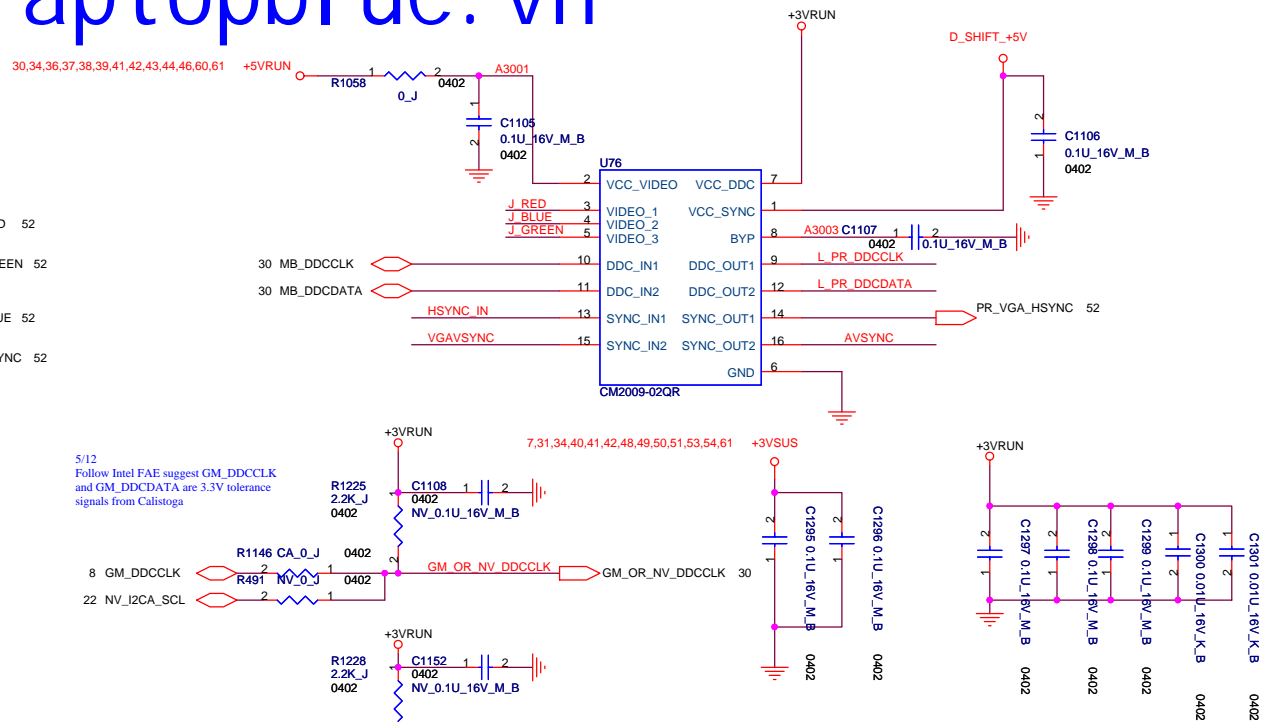
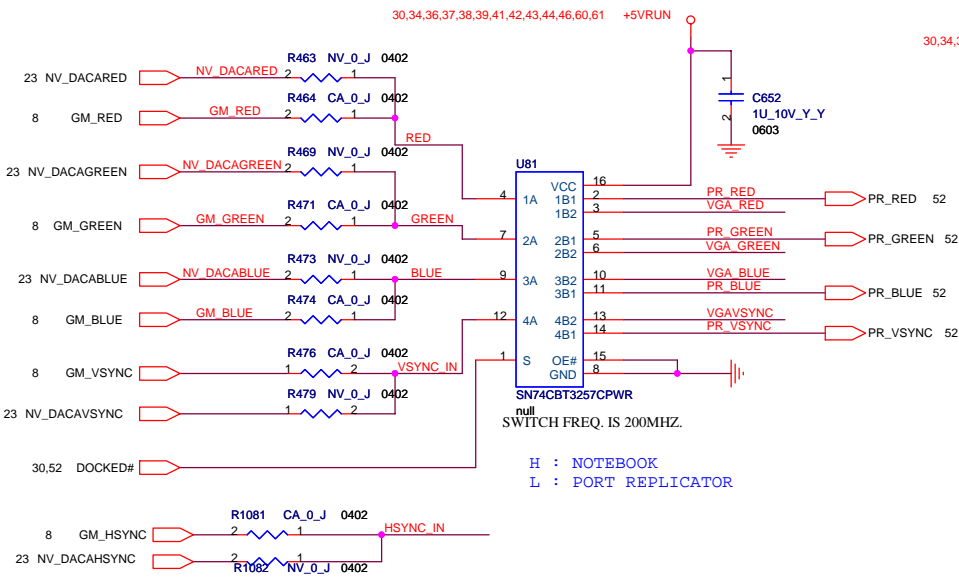
The R461 will consume about 0.054 Watt ( $3.3 \times 3.3 / 200 = 0.054W$ ). We changed resistor to 0603 size (1/8 Watt)

**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
CCPBG - R&D Division

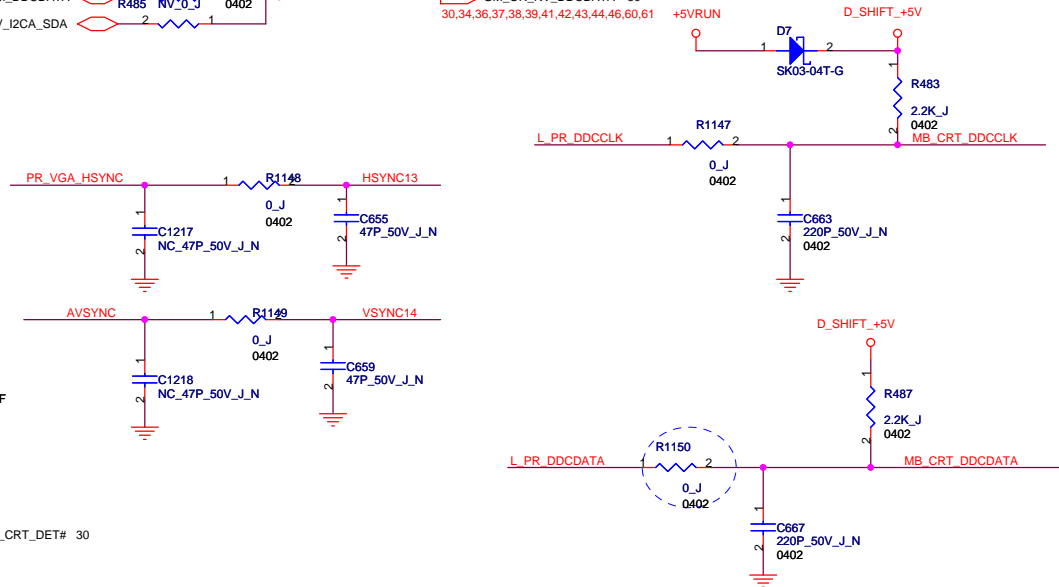
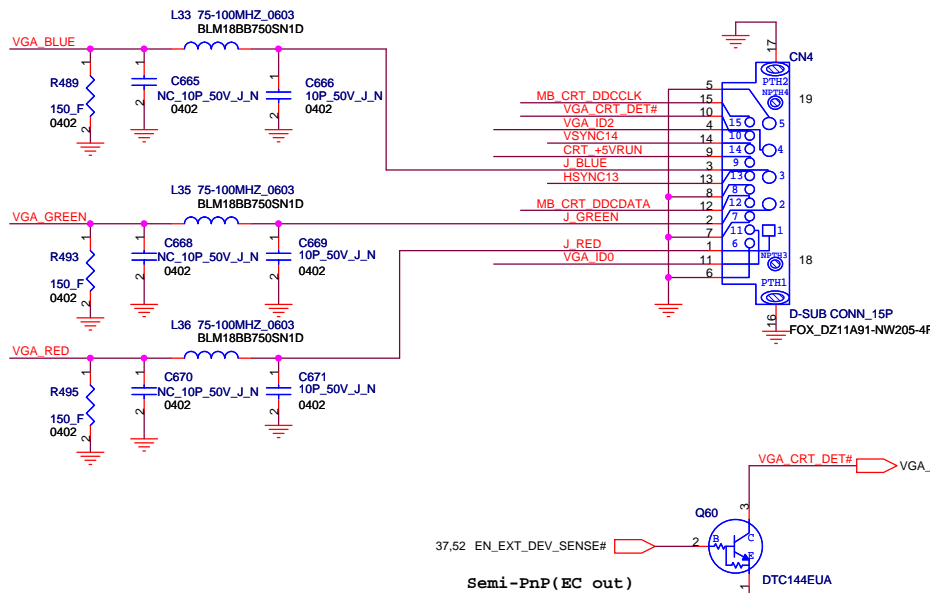
Title			LVDS		
Size	Document Number				Rev
A3	MS13-1-01 ( MBX-149 )				1.0
Date:	Wednesday, August 30, 2006		Sheet	28	of 67

# CRT ANALOG SWITCH

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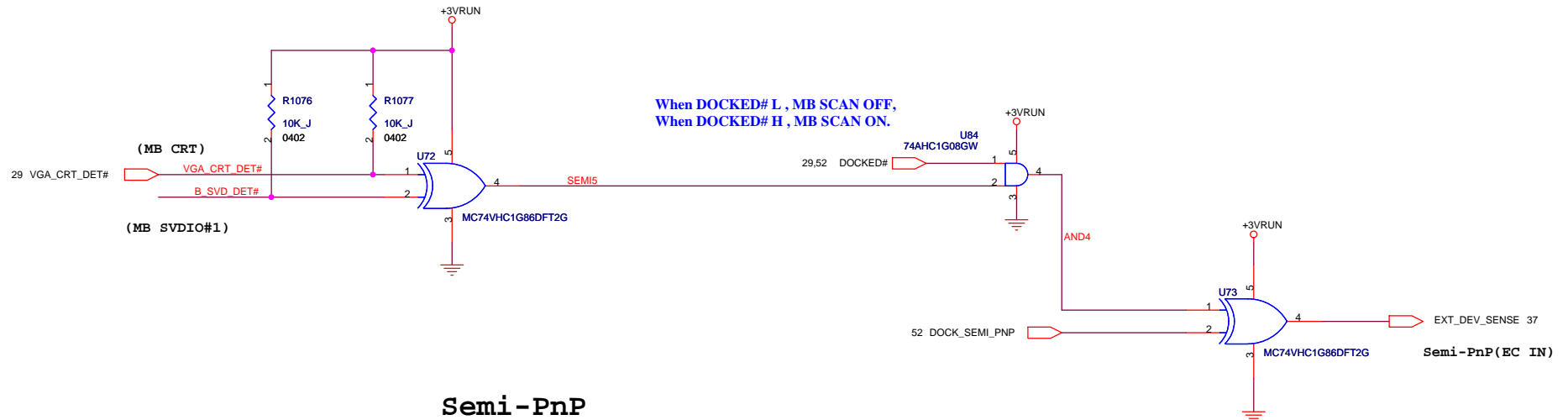
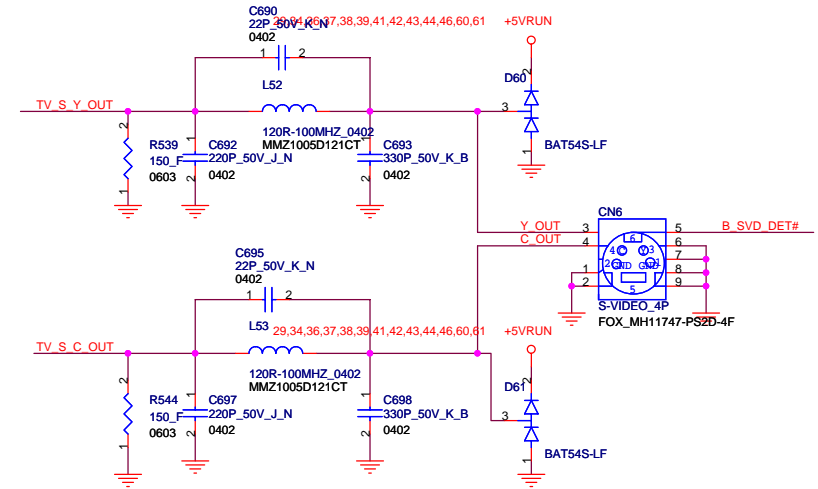
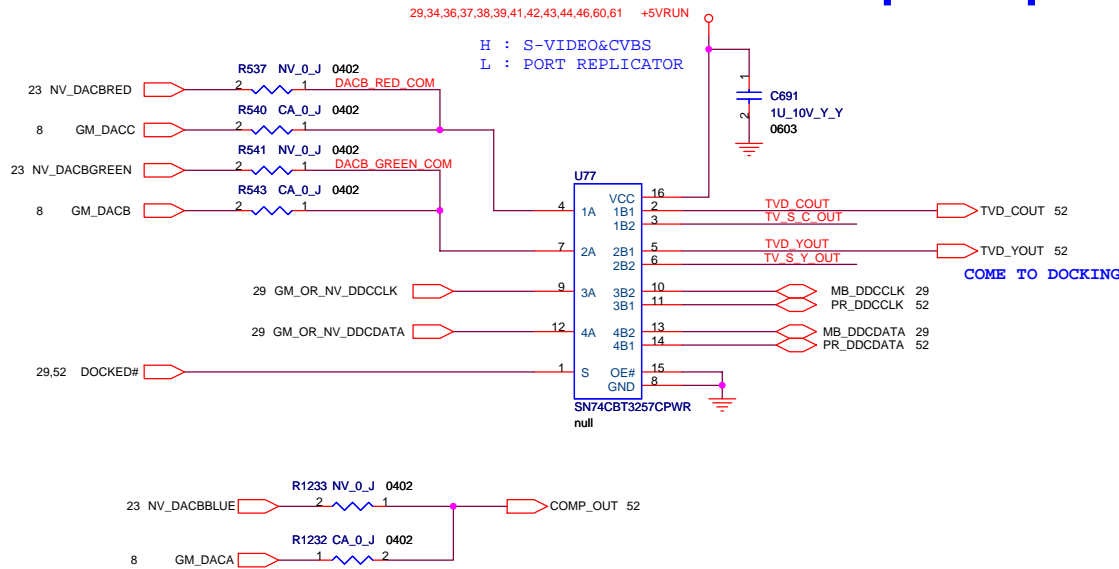


# CRT CONNECTOR

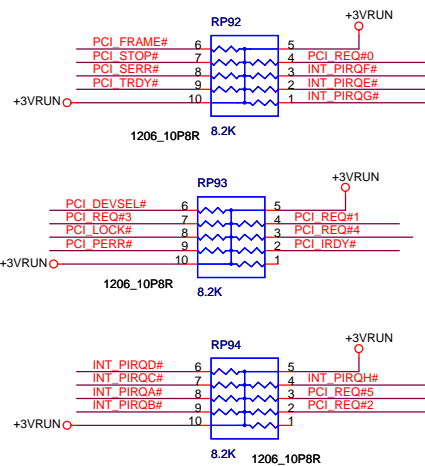


<b>FOXCONN</b>		<b>HON HAI Precision Ind. Co., Ltd.</b>	
		<b>CCPBG - R&amp;D Division</b>	
<b>Title CRT</b>			
<b>Size</b> A3	<b>Document Number</b> MS13-1-01 ( MBX-149 )	<b>Rev</b> 1.0	
<b>Date:</b> Wednesday, August 30, 2006		<b>Sheet</b> 29	<b>of</b> 67

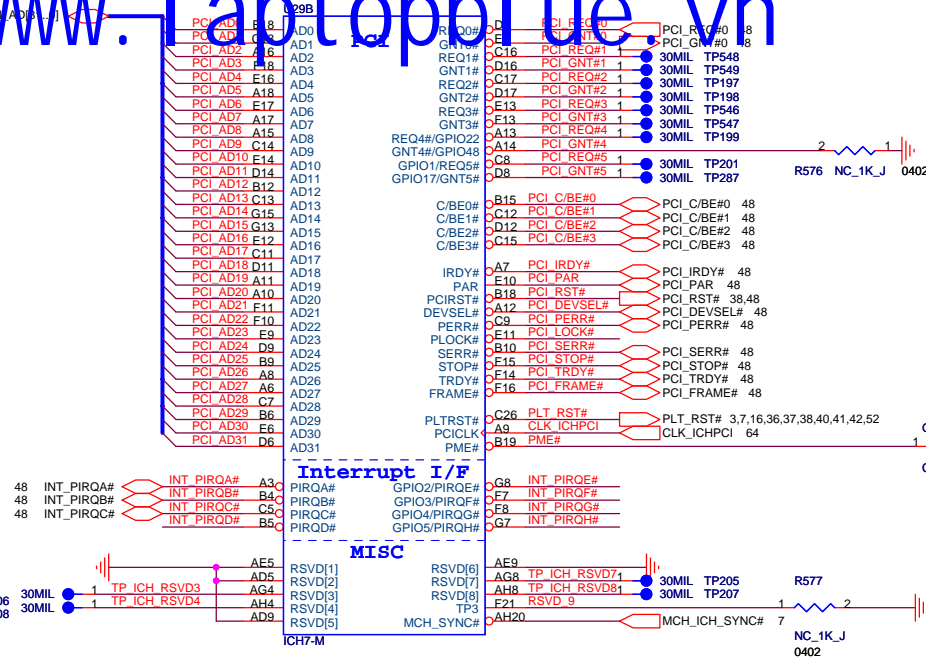
These compoent close to S-Video connector within 700 mil



Semi-PnP

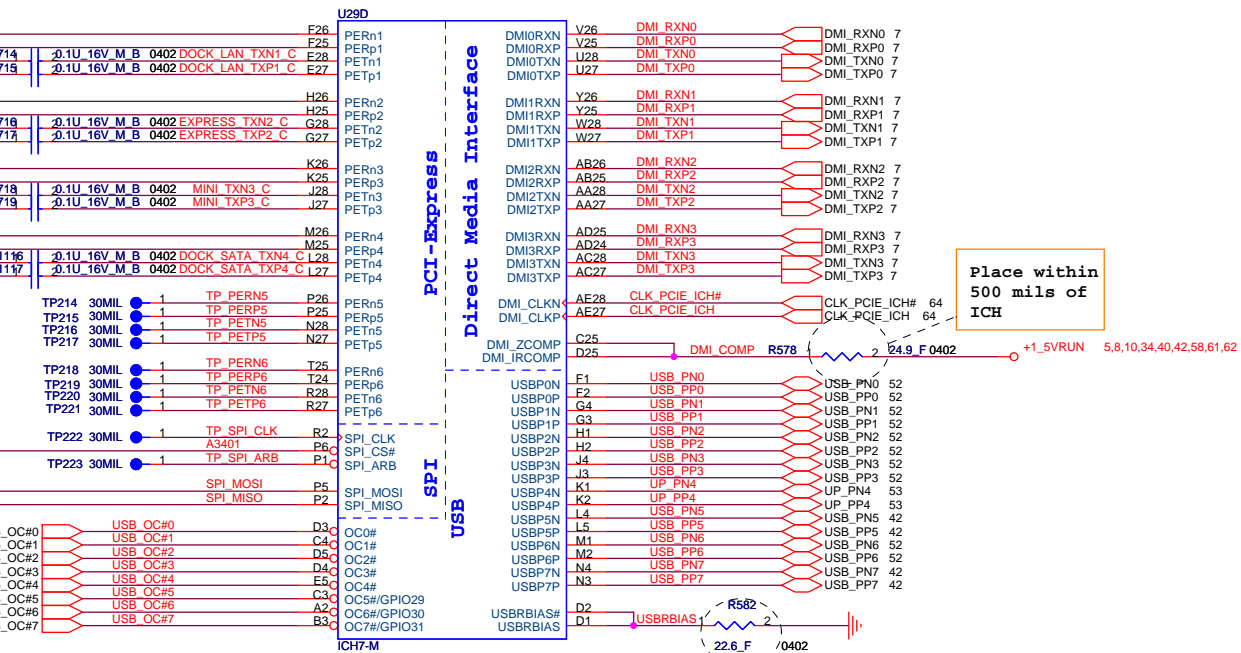


## PCI Pullups



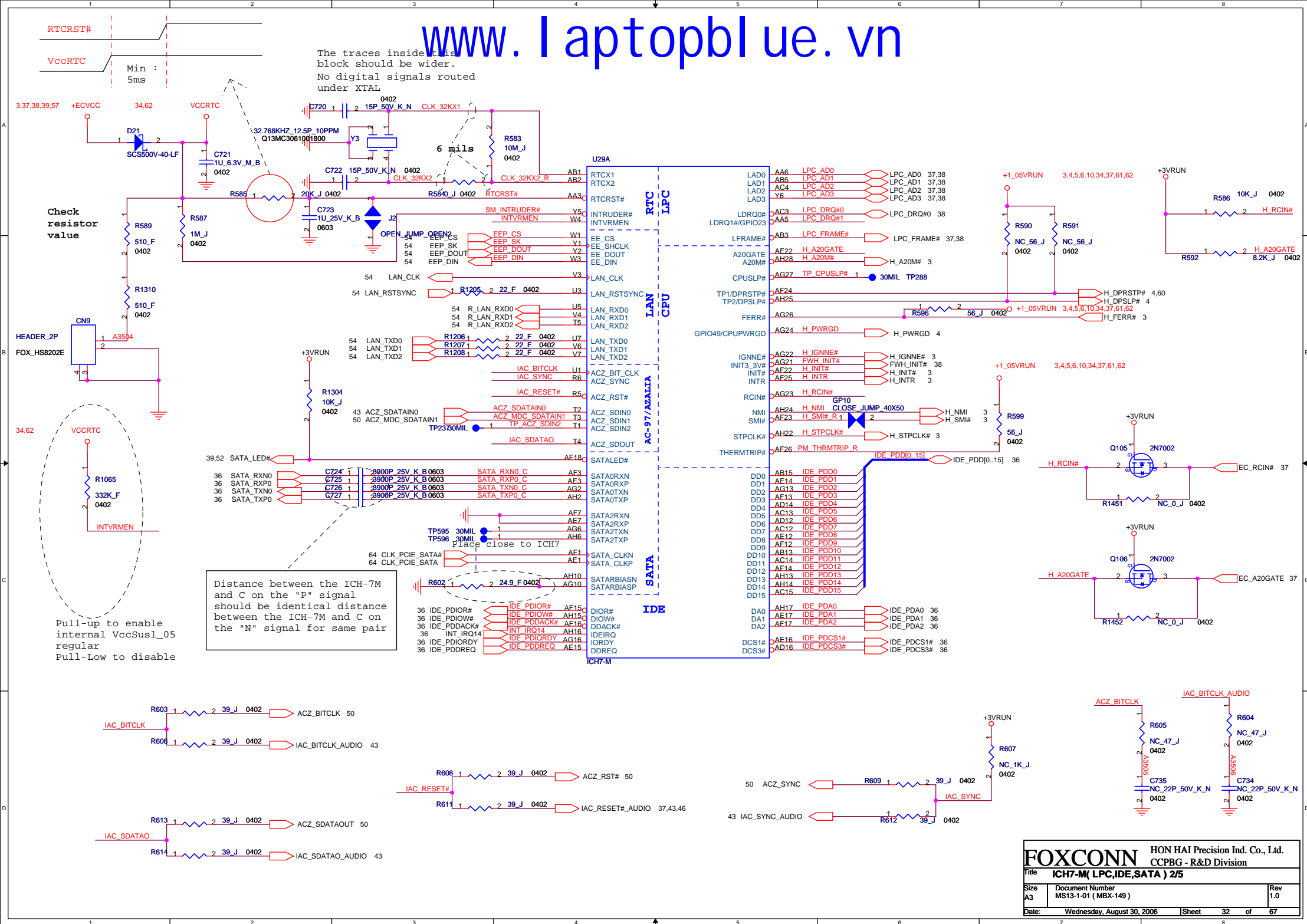
Strap for  
Boot-BIOS

	GNT5#	GNT4#
LPC(Default)	Hi	Hi
PCI	Hi	LOW



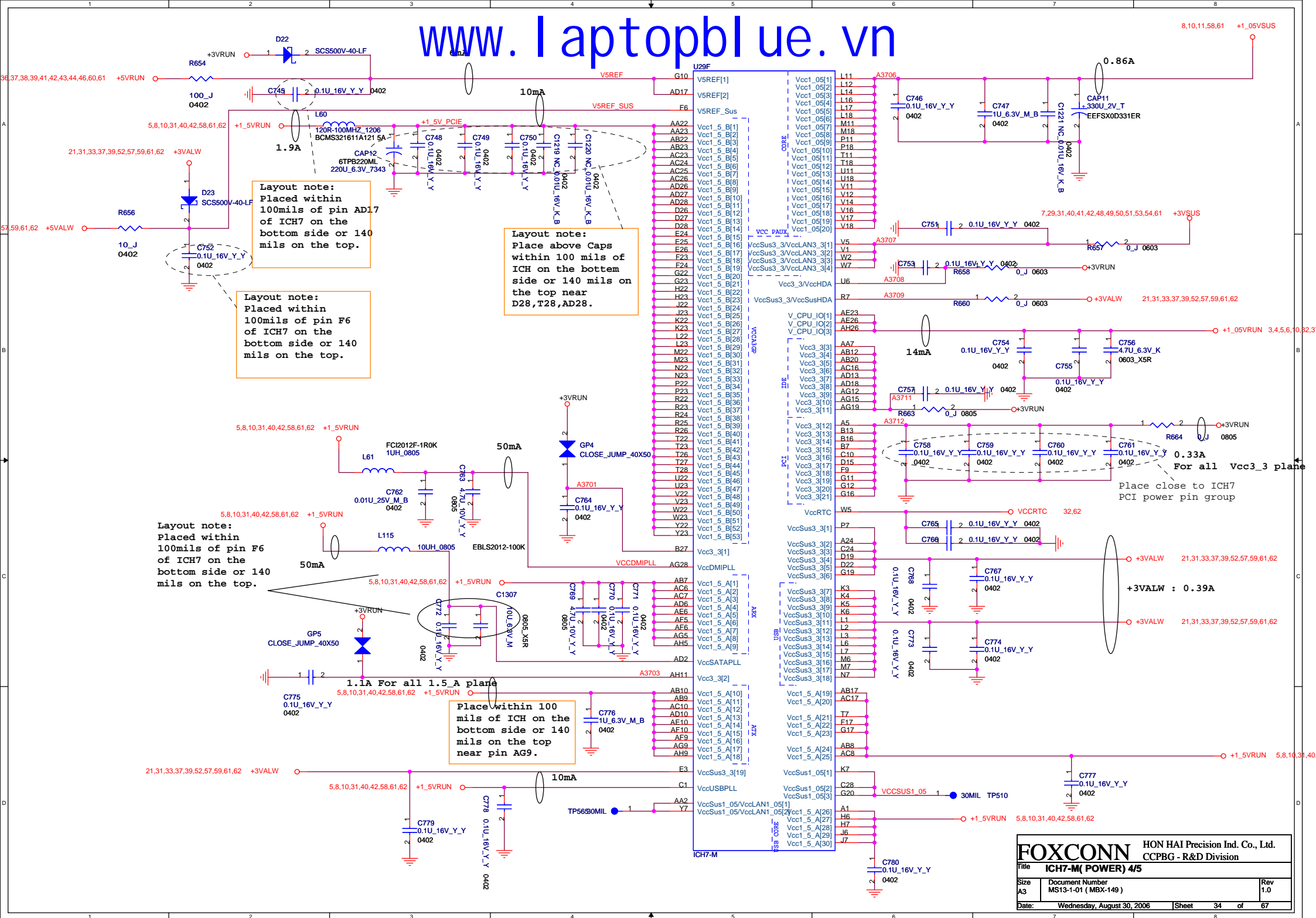
Place within  
500 mils of  
ICH

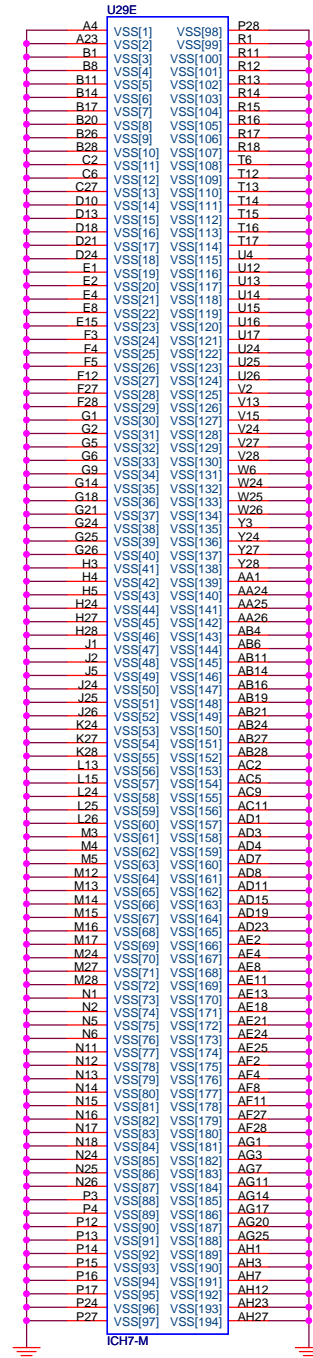
Place within 500 mils of  
ICH and don't routing next  
to high speed signals

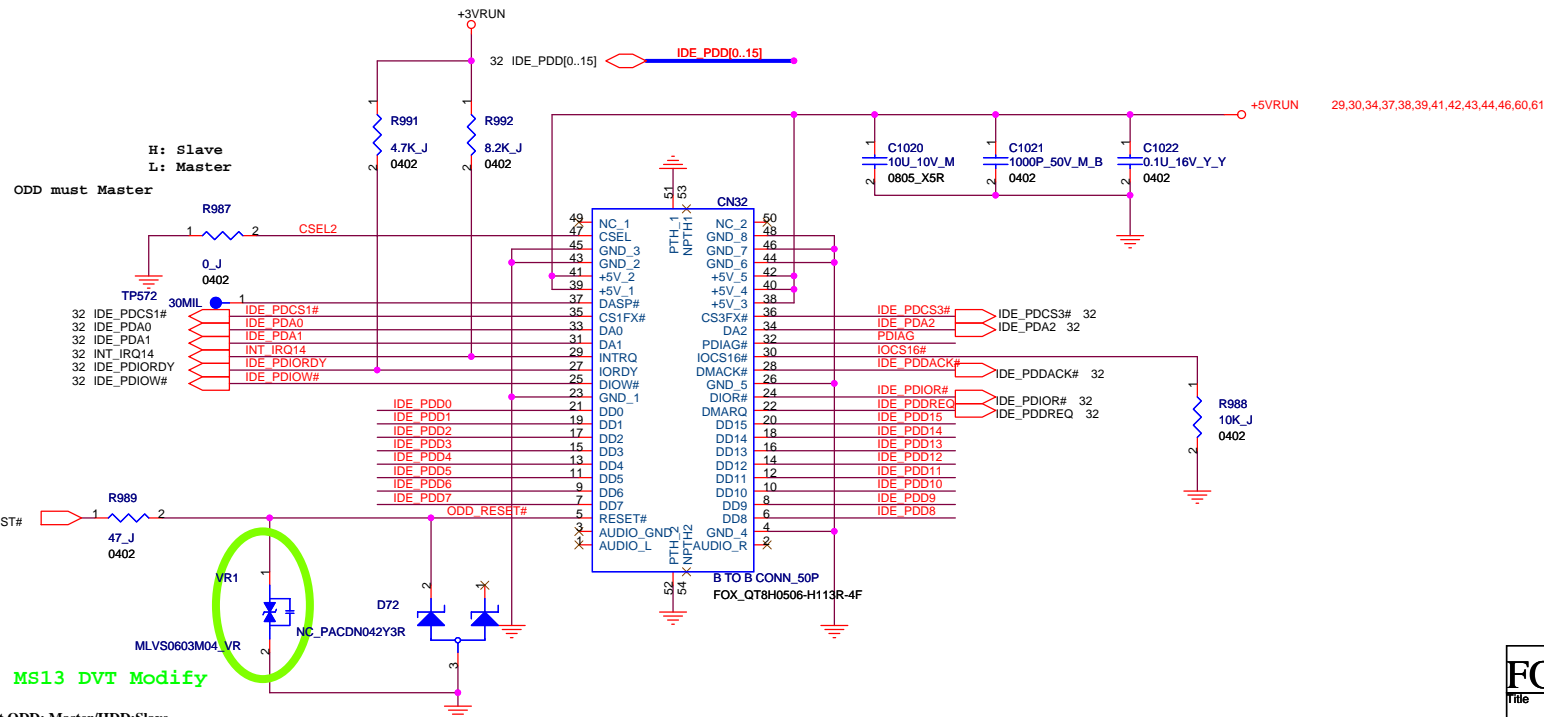
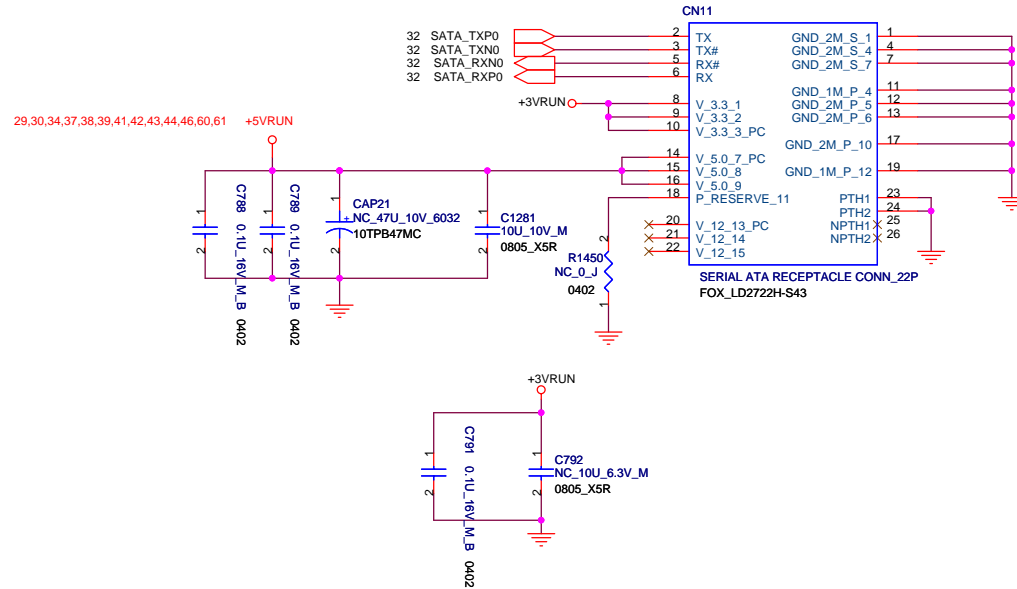


[illegible][illegible]

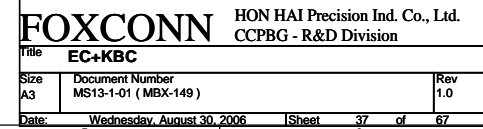


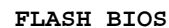






## CD-ROM CONN





41

43

3.32,37,39,57 +ECVCC

2

C806

0.1uF\_16V\_M\_B

2

0402

1

2

4

6

8

10

12

14

16

18

20

22

24

26

28

30

32

34

36

38

40

42

44

SIO FA0

SIO FA1

SIO FA2

SIO FA3

SIO FA4

SIO FA5

SIO FA6

SIO FA7

SIO FA8

SIO FA9

SIO FA10

SIO FA11

SIO FA12

SIO FA13

SIO FA14

SIO FA15

SIO FA16

SIO FA17

SIO FA18

SIO FA19

SIO FD0

SIO FD1

SIO FD2

SIO FD3

SIO FD4

SIO FD5

SIO FD6

SIO FD7

MEMCS#

FRD#

FWR#

CARD\_INSERT

EC\_OUT1

MEMCS# 37,39

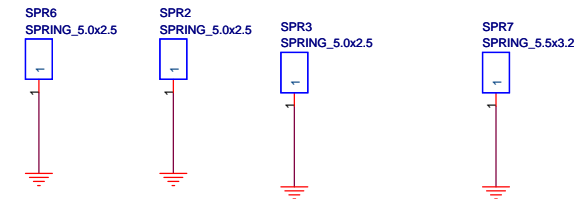
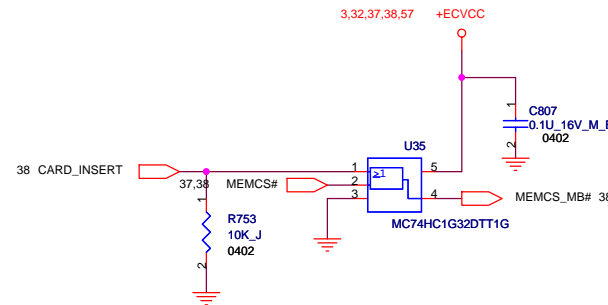
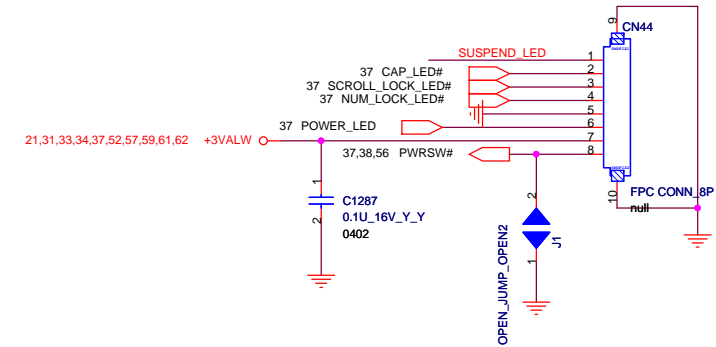
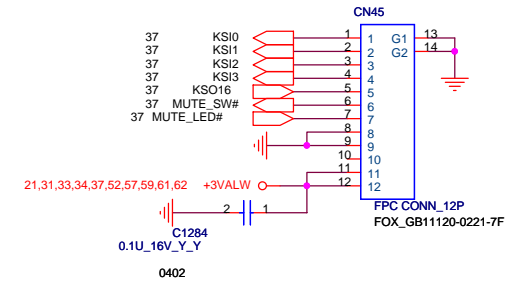
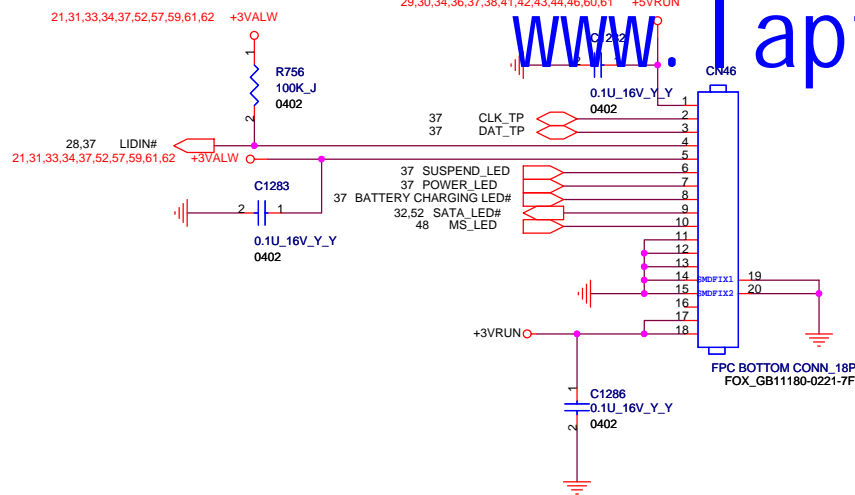
CARD\_INSERT 39

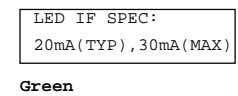
EC\_OUT1 37

CN14

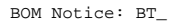
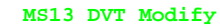
B TO B CONN\_2x20P

FOX\_QT510406-L011-F



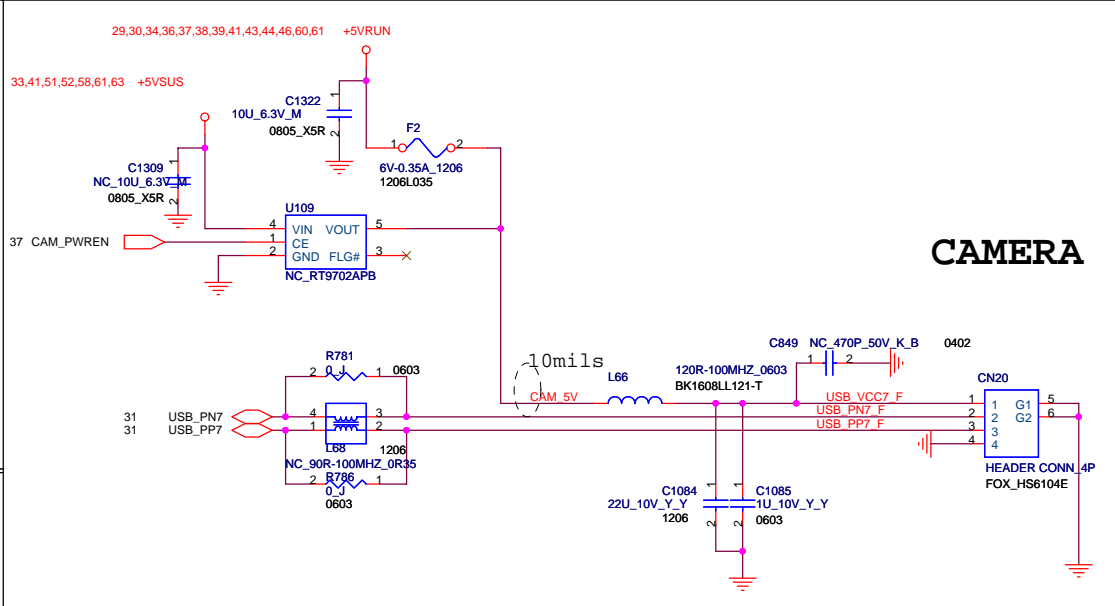
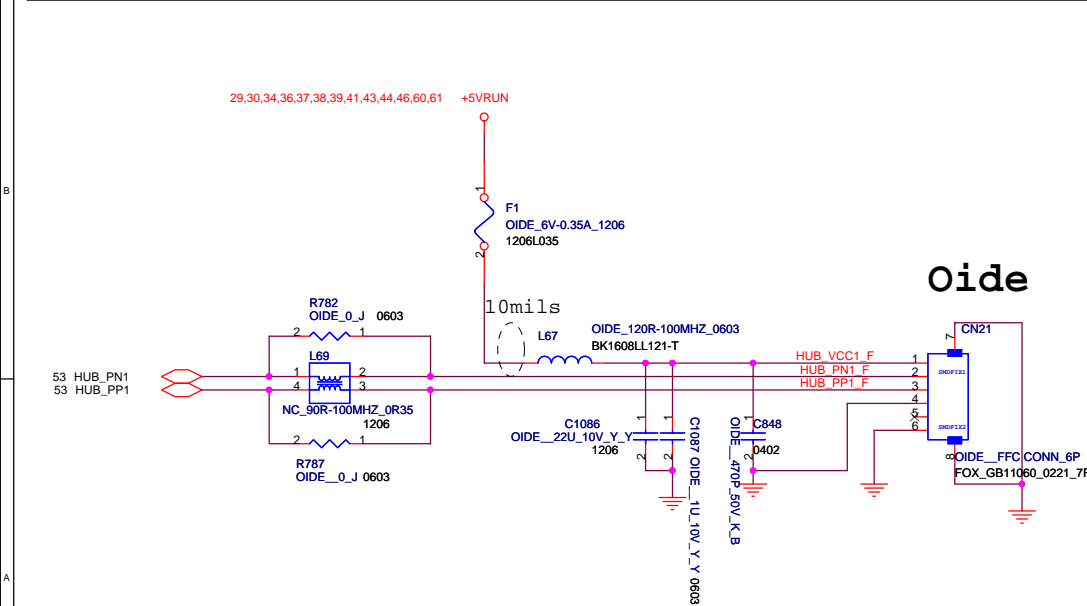
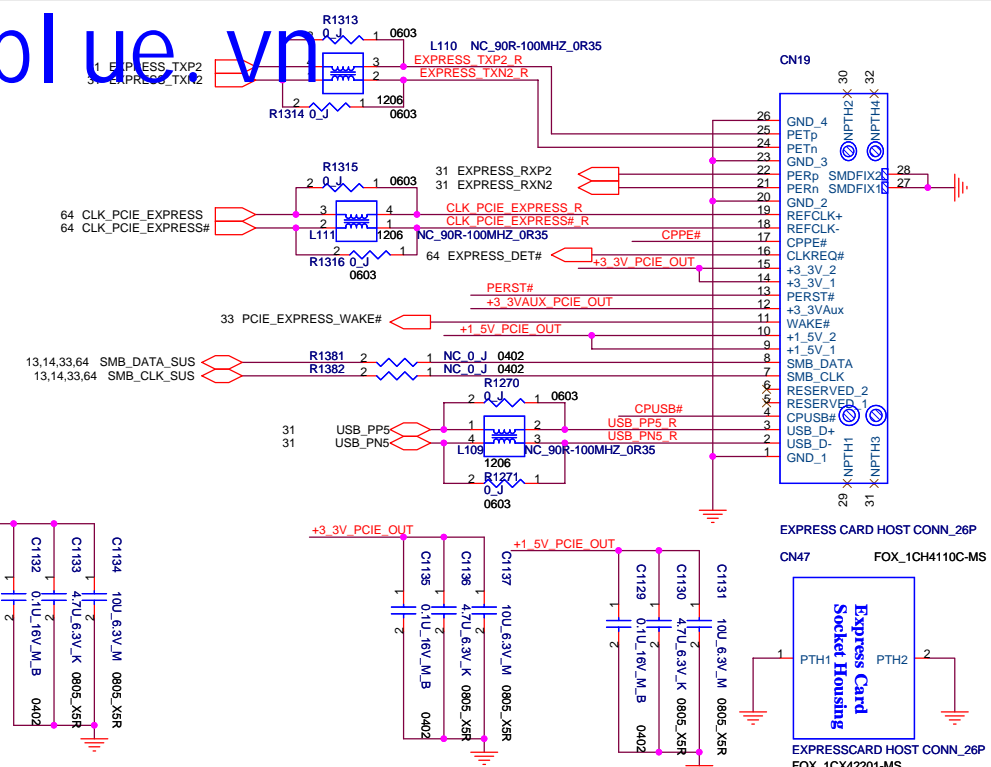
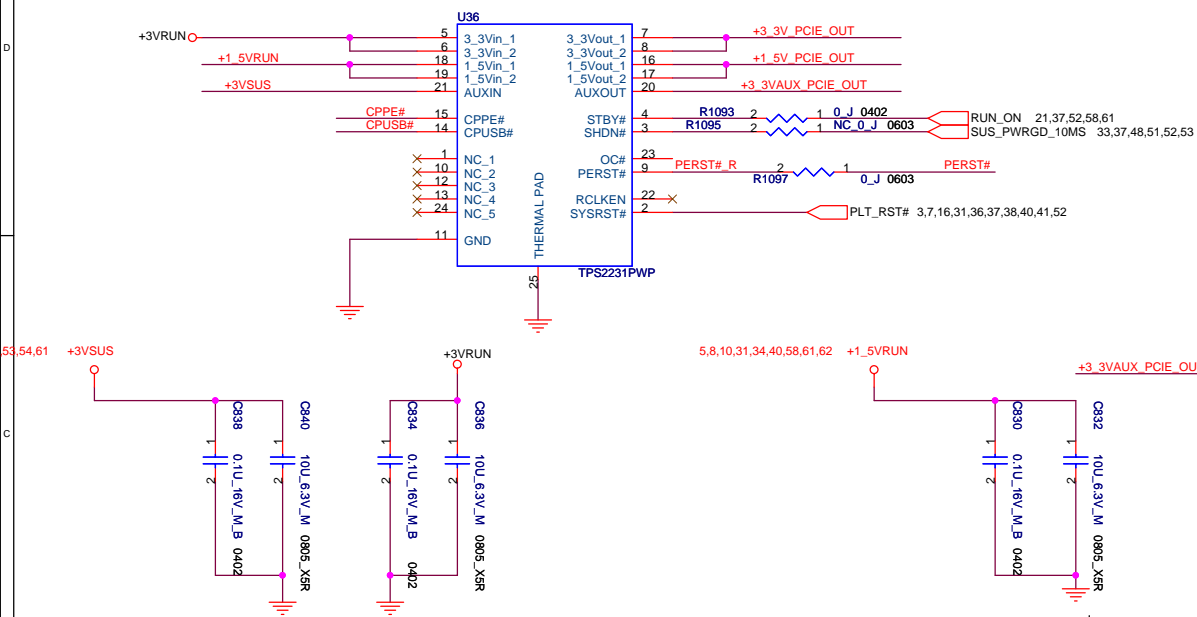






W/ BT SKU	Q93,LEDE9,R1377,U79,C1124,C1125,C1126,C1128,U80,R1068,R1028,R1029,R1030,CN36	stuff
W/O BT SKU	Q93,LEDE9,R1377,U79,C1124,C1125,C1126,C1128,U80,R1068,R1028,R1029,R1030,CN36	no stuff

W/O BT SKU	Q93,LEDE9,R1377,U79,C1124,C1125,C1126, C1128,U80,R1068,R1028,R1029,R1030,CN36	no stuff
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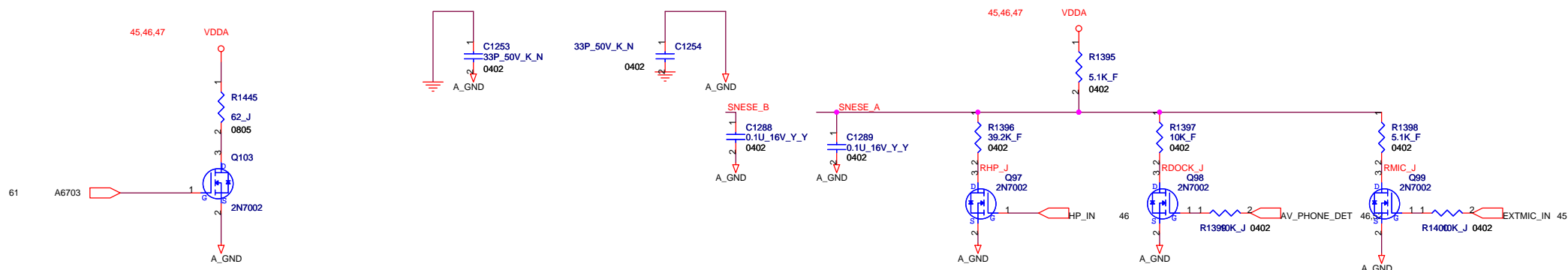
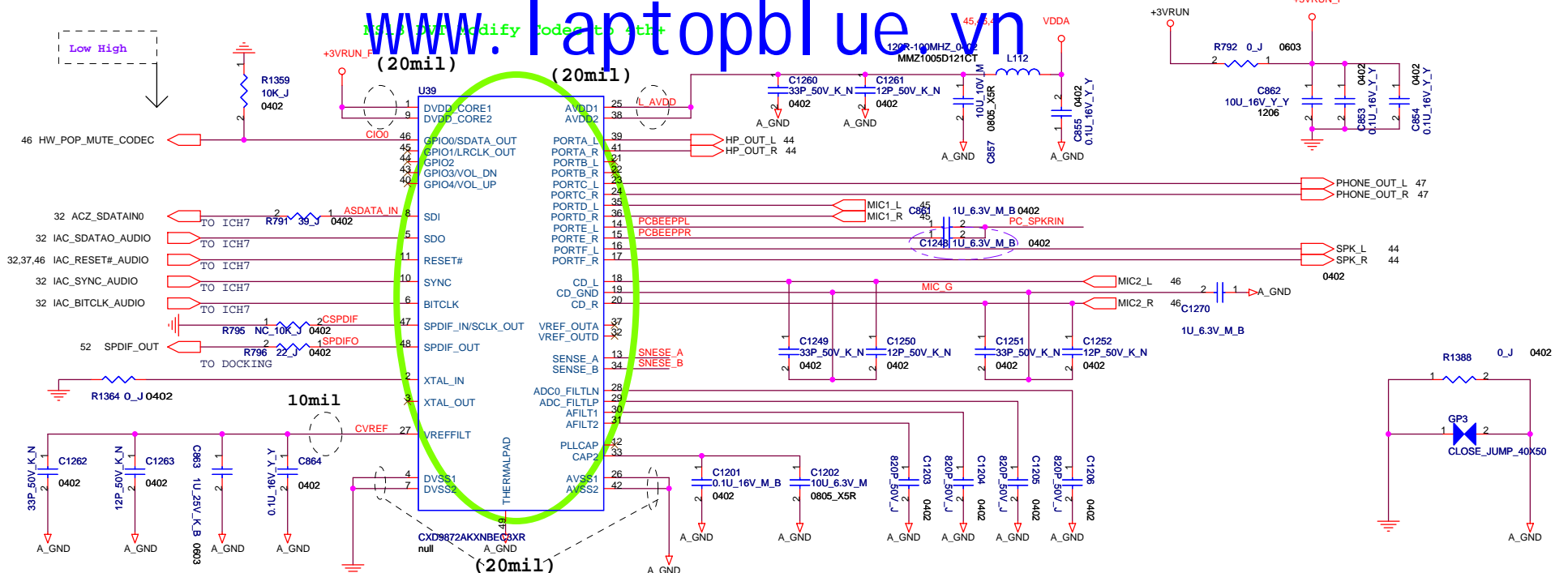


BOM Notice: OIDE\_

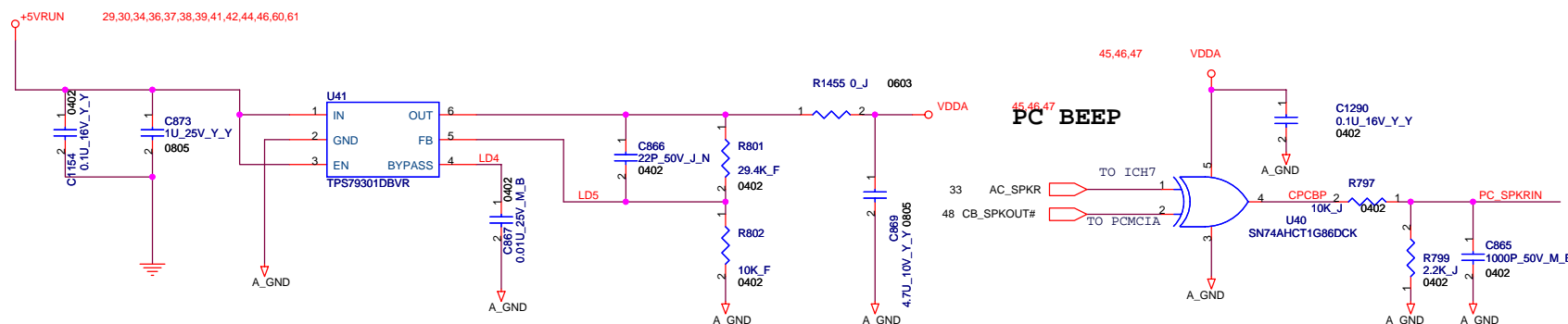
W/ Oide SKU	R782,R787,L67,C1086,C1087,C848,CN21	stuff
W/O Oide SKU	R782,R787,L67,C1086,C1087,C848,CN21	no stuff

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
Title <b>EXPRESS/CAM/OIDE</b>		CCPBG - R&D Division	
Size A3	Document Number MS13-1-01 ( MBX-149 )	Rev 1.0	
Date: Wednesday, August 30, 2006	Sheet 42	of 67	

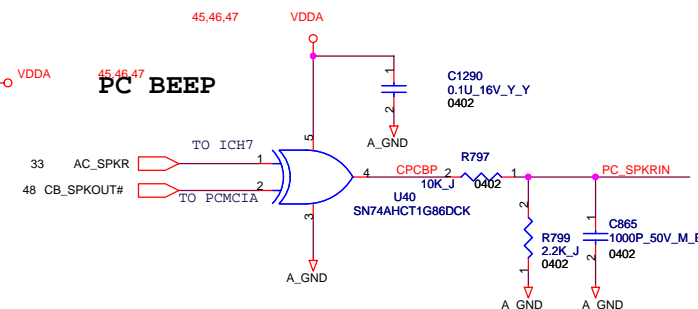
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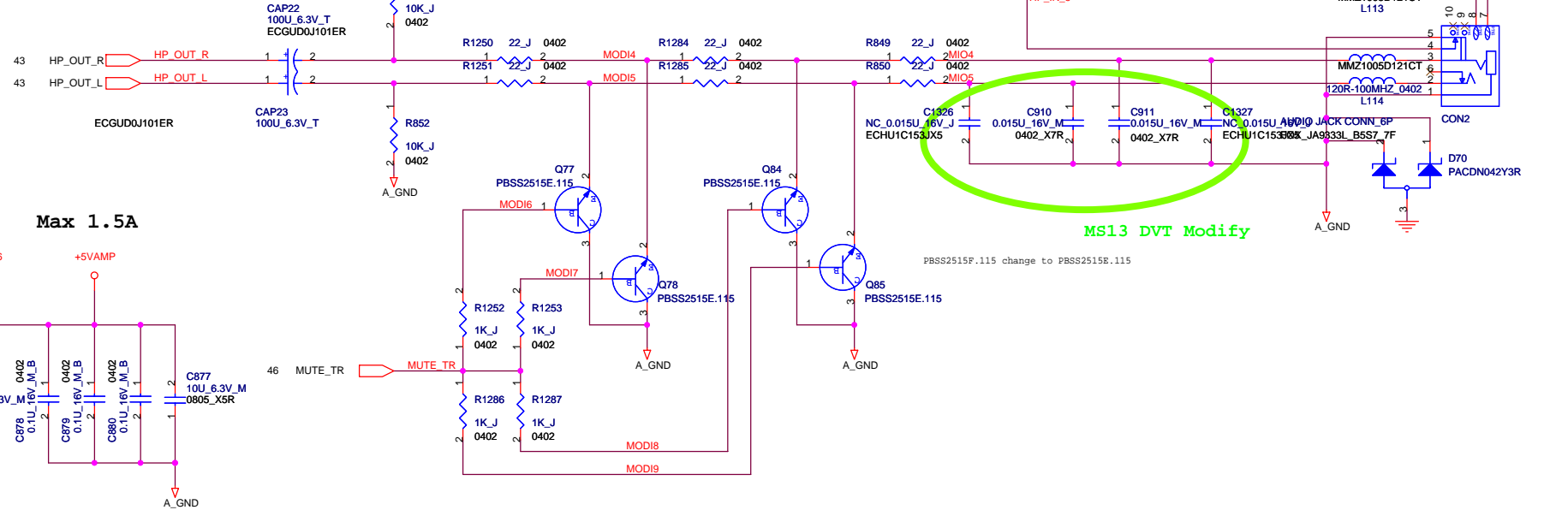
AUDIO POWER(Change to 4.75V/200mA)



<sup>45,46,47</sup>  
PC BEEP



SE0J101-3B\_100uF change  
to ECGUD0J101ER\_100uF

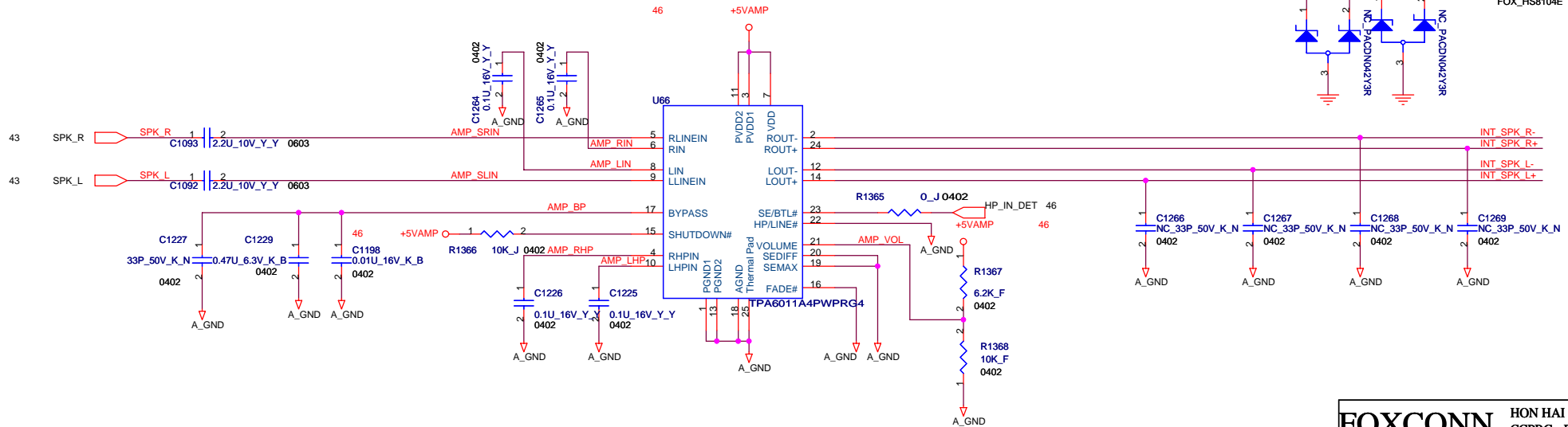
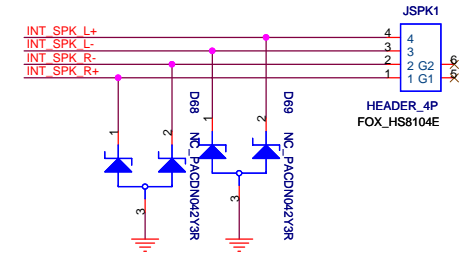


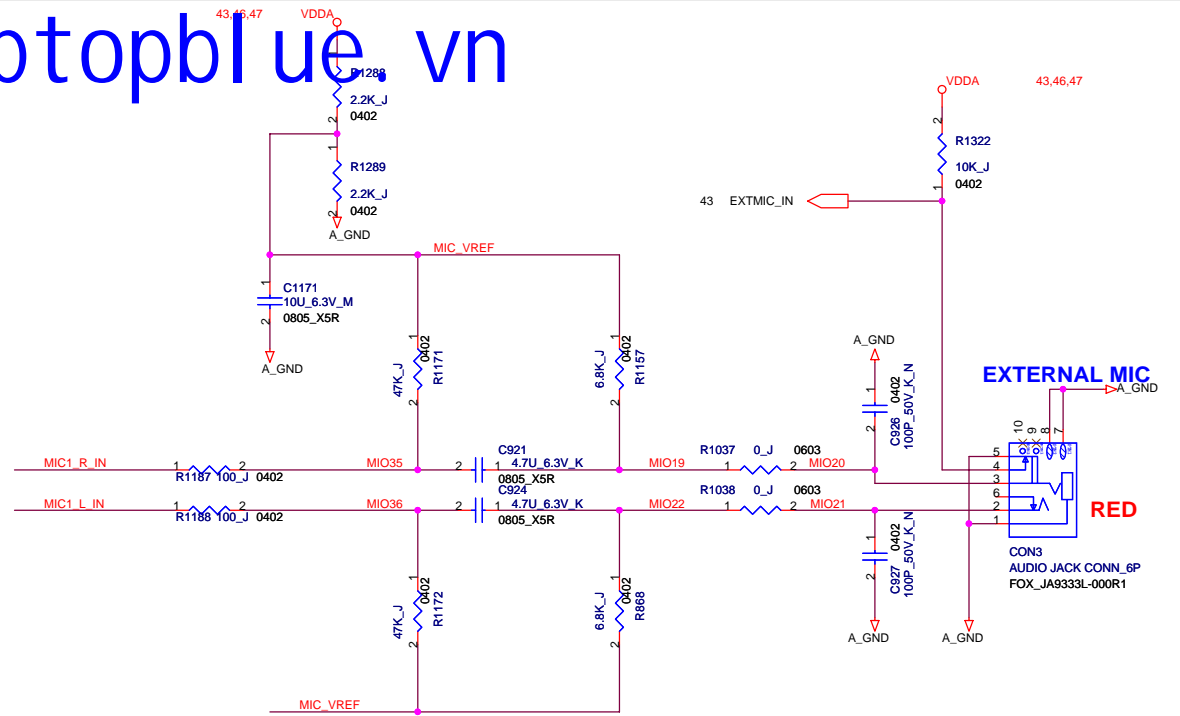
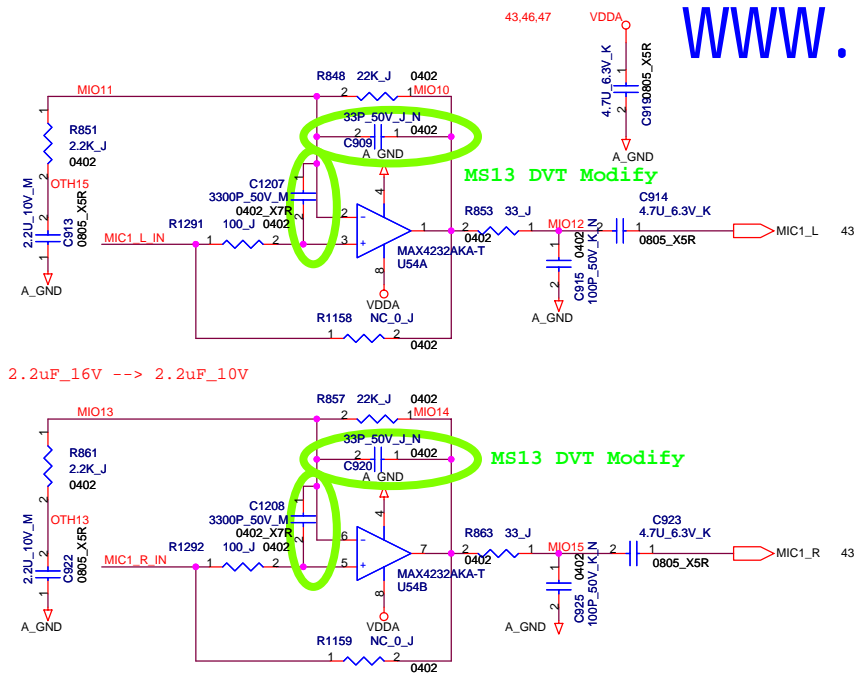
Max 1.5A

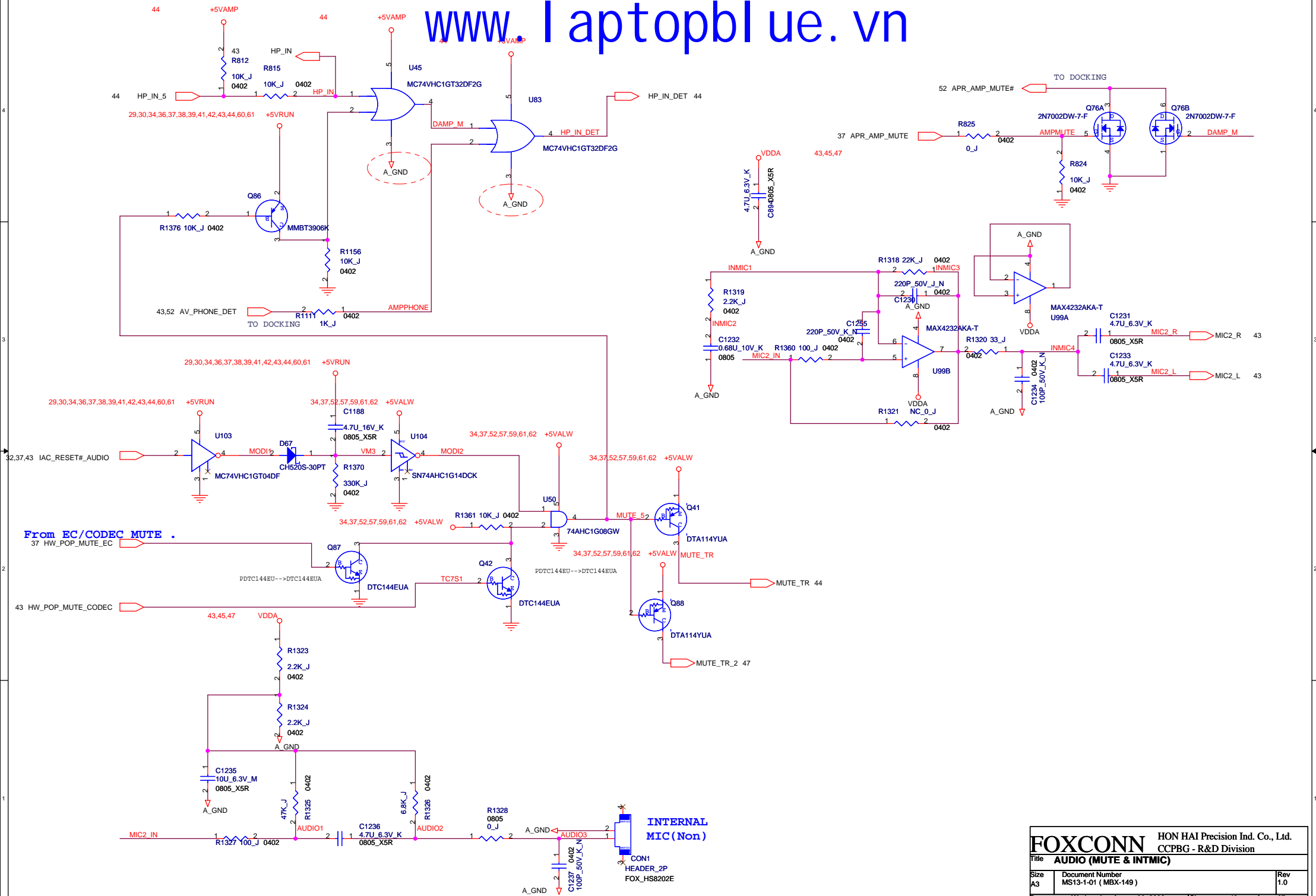
MS13 DVT Modify

PBSS2515F.115 change to PBSS2515E.115

# INTERNAL SPEAKER

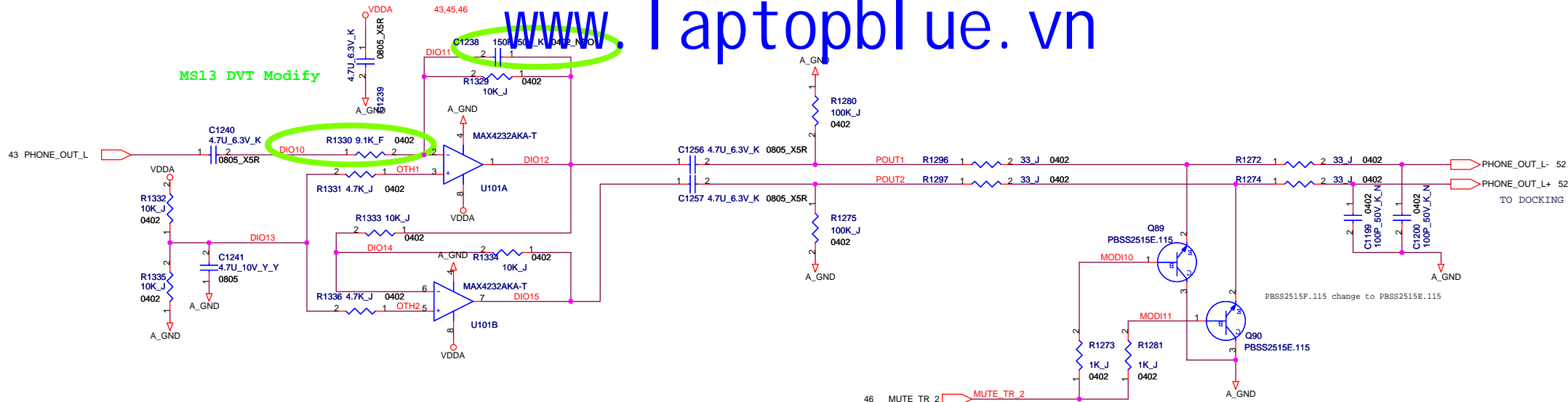




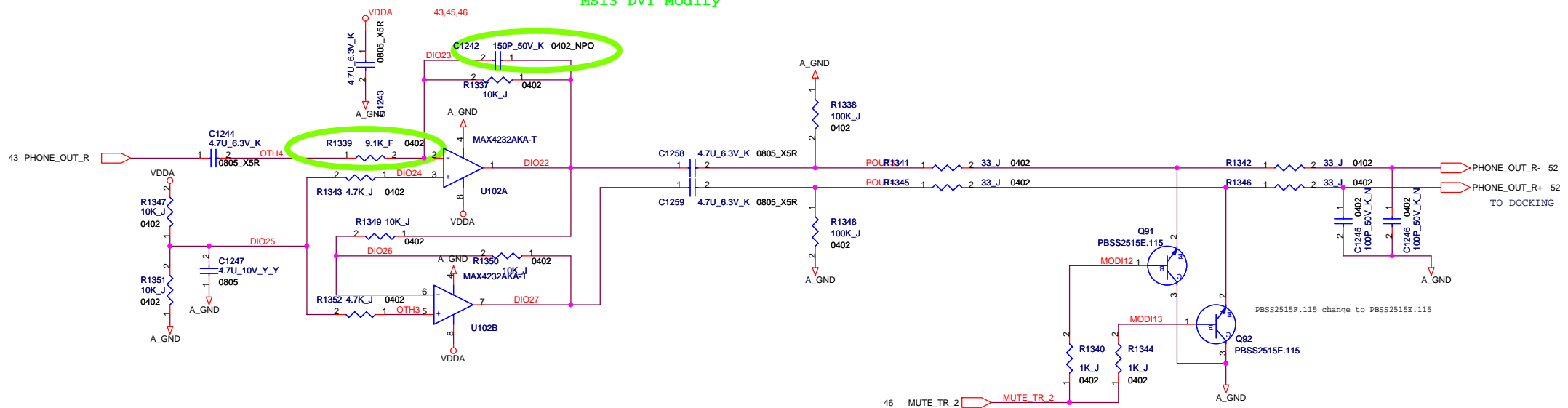




MS13 DVT Modify



MS13 DVT Modify





This array must be placed close to VDPLL(Pin U19)  
They must be tied to a low-impedance GND.

This array must be placed close to AVDD(Pin P13,P14,U15)  
They must be tied to a low-impedance GND.

This capacitor should be placed between Pin P15 and Pin R17 .

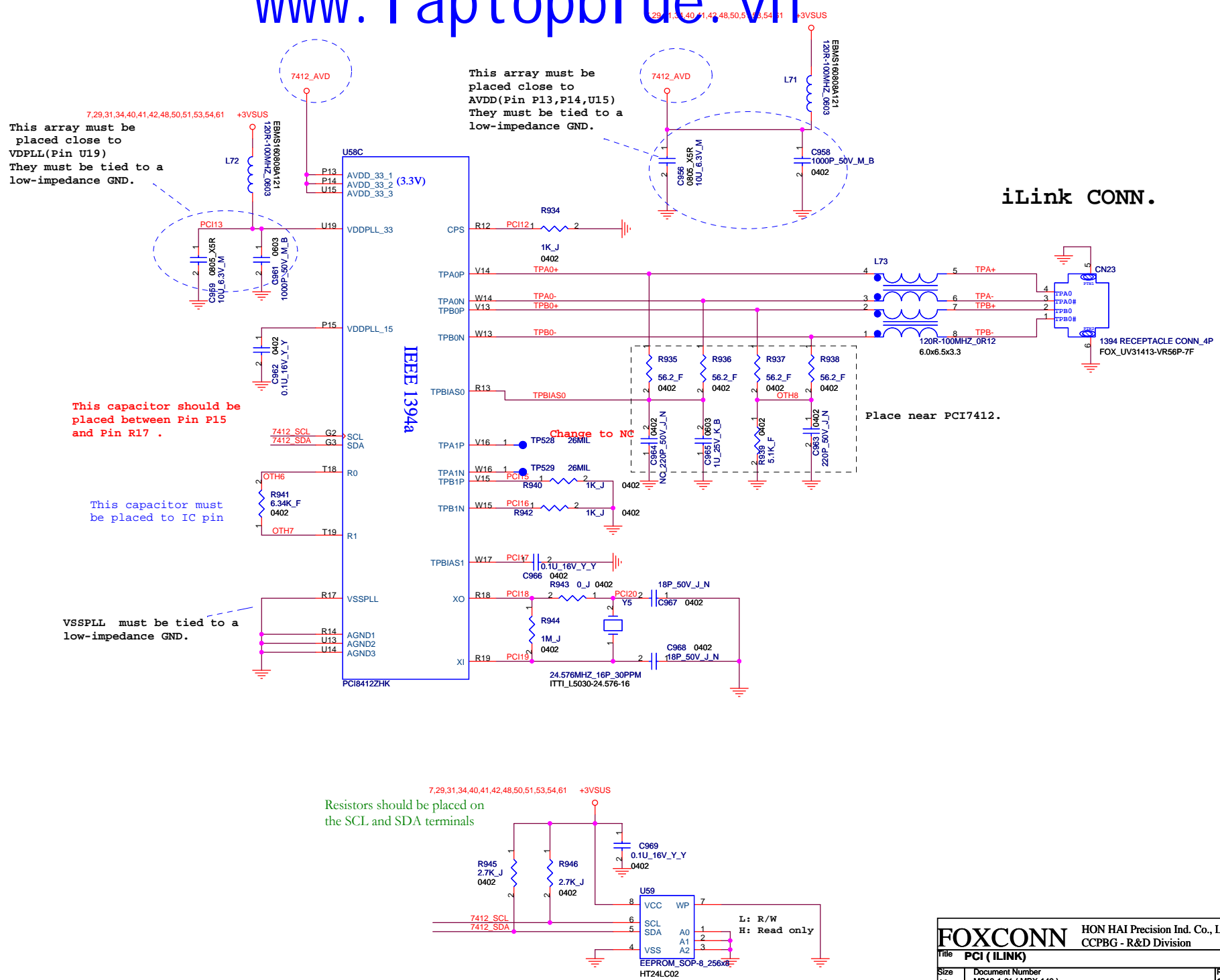
This capacitor must be placed to IC pin

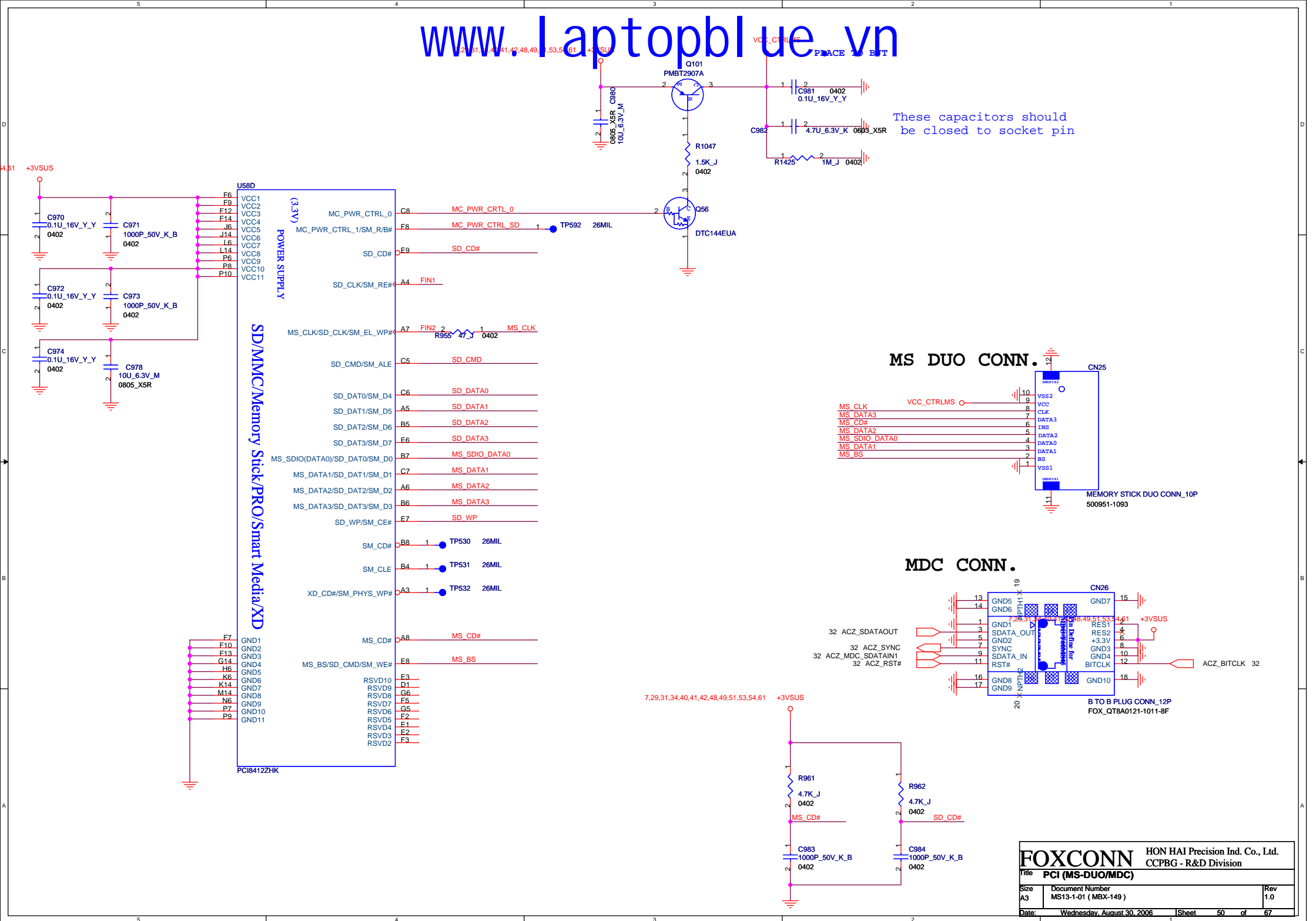
VSSPLL must be tied to a low-impedance GND.

iLink CONN.

Place near PCI7412.

Resistors should be placed on the SCL and SDA terminals





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PCMCIA CONN.

Card BUS / 16-Bit PC Card Interface

Serial / Parallel PC Card Power Switch

Card BUS / 16-Bit PC Card Socket

PCMCIA CONN. 2x34

FOX\_WZ21131-G2

TPS2220BPWPR

FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division

Title: PCI (PCMCIA)

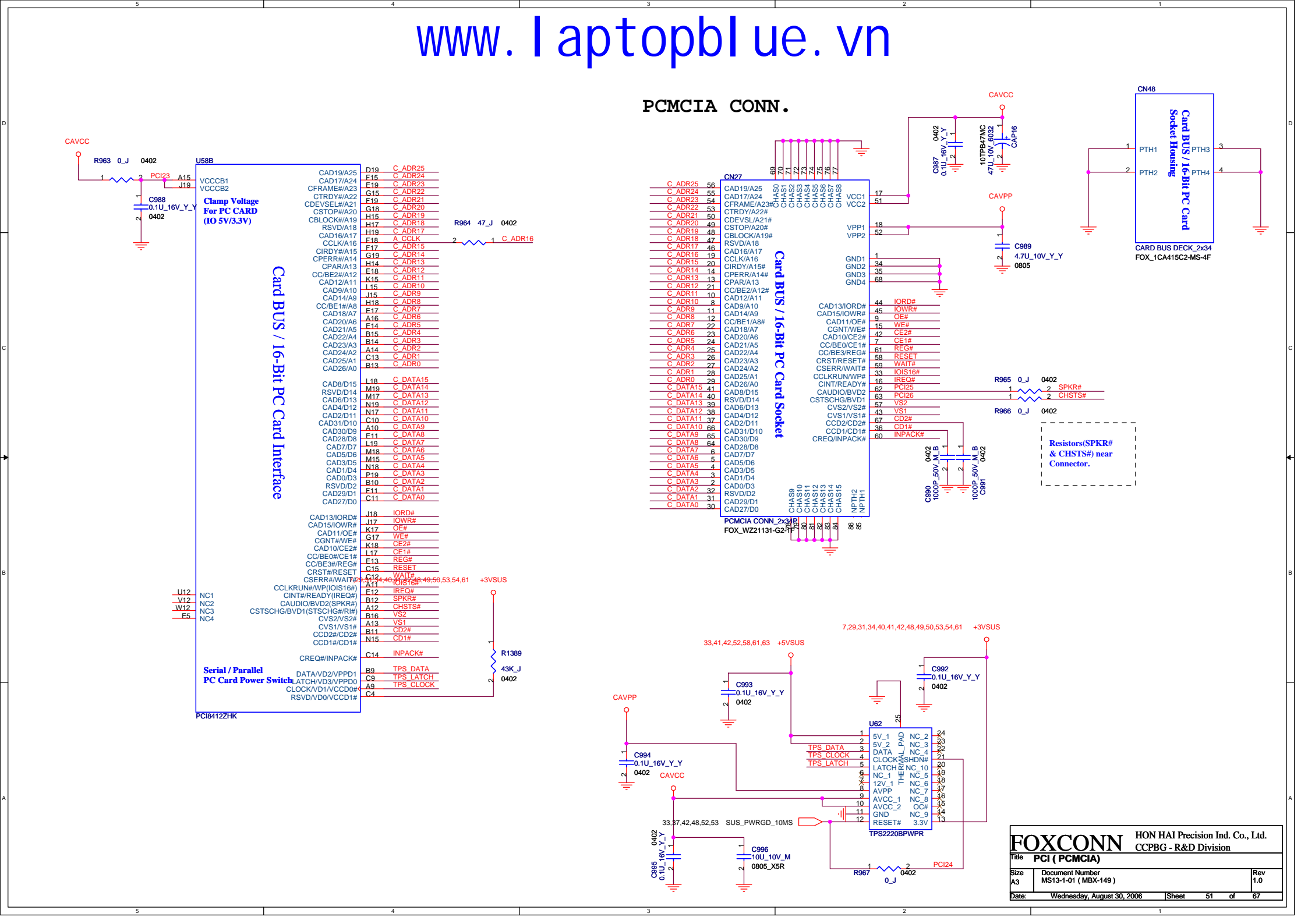
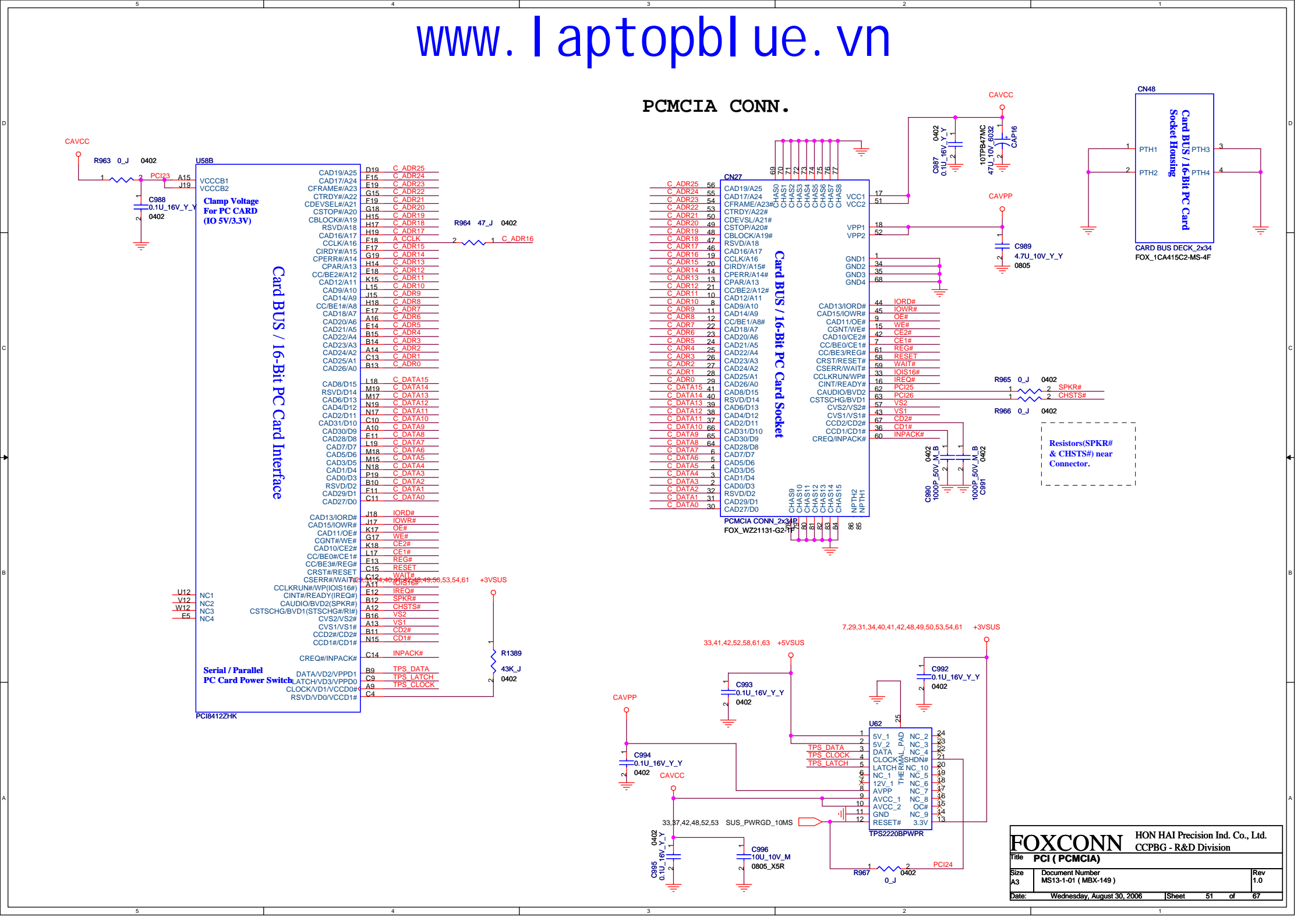
Size: A3

Document Number: MS13-1-01 (MBX-149)

Date: Wednesday, August 30, 2006

Sheet: 51 of 67

Rev: 1.0



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PCMCIA CONN.

Card BUS / 16-Bit PC Card Interface

Serial / Parallel PC Card Power Switch

Card BUS / 16-Bit PC Card Socket

PCMCIA CONN. 2x34

FOX\_WZ21131-G2

TPS2220BPWPR

FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division

Title: PCI (PCMCIA)

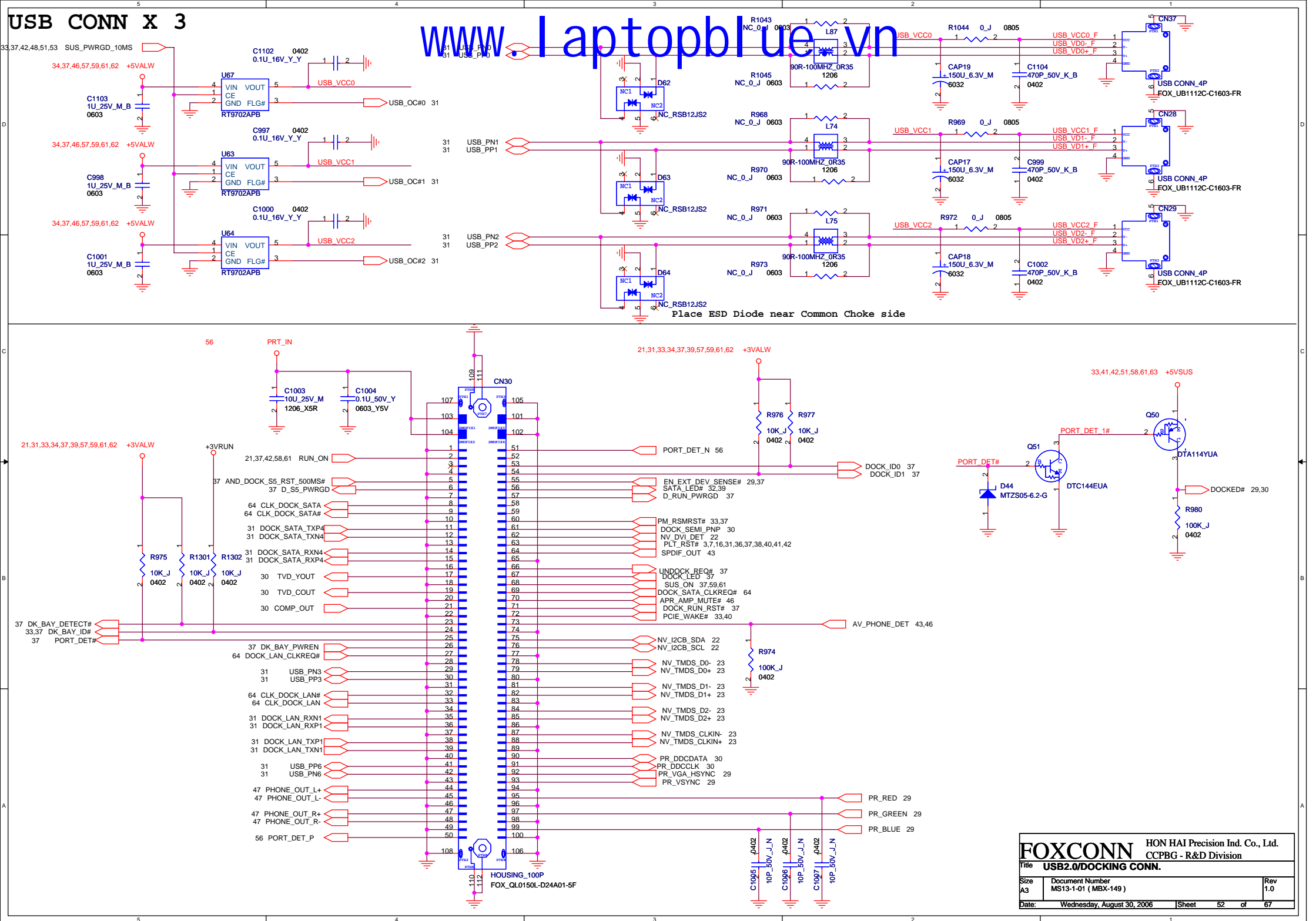
Size: A3

Document Number: MS13-1-01 (MBX-149)

Date: Wednesday, August 30, 2006

Sheet: 51 of 67

Rev: 1.0





BOM notice:

	R1241	R1244	R1247	R1248	R1459	R1460
BT + OIDE SKU	NC	NC	NC	NC	NC	NC
BT SKU	0 ohm	0 ohm	0 ohm	0 ohm	NC	NC
OIDE SKU	0 ohm	0 ohm	NC	NC	0 ohm	0 ohm

BOM notice:

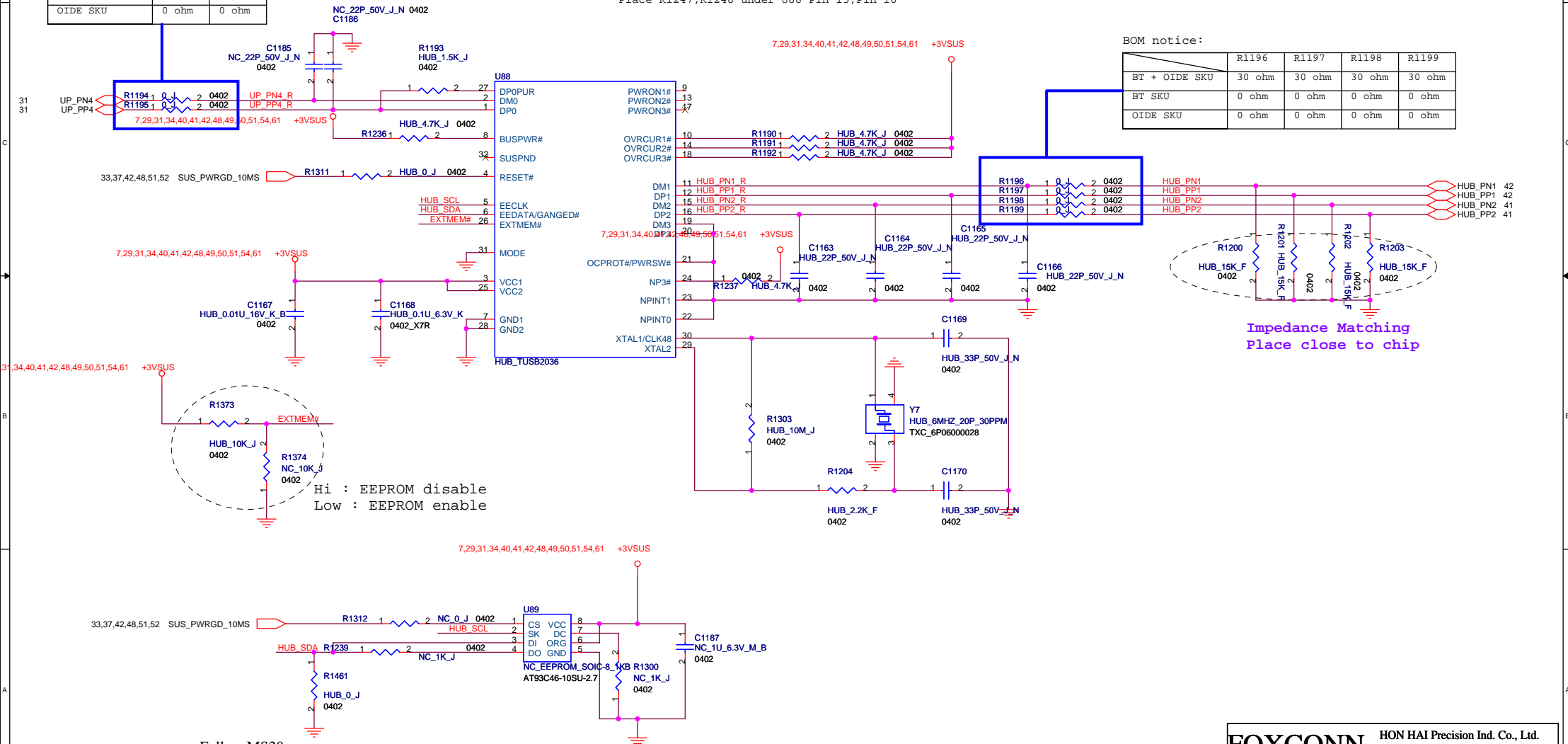
	R1194	R1195
BT + OIDE SKU	30 ohm	30 ohm
BT SKU	0 ohm	0 ohm
OIDE SKU	0 ohm	0 ohm

Layout note:

Place R1243, R1244 under U88 Pin1, Pin2  
Place R1459, R1460 under U88 Pin 11, Pin 12  
Place R1247, R1248 under U88 Pin 15, Pin 16

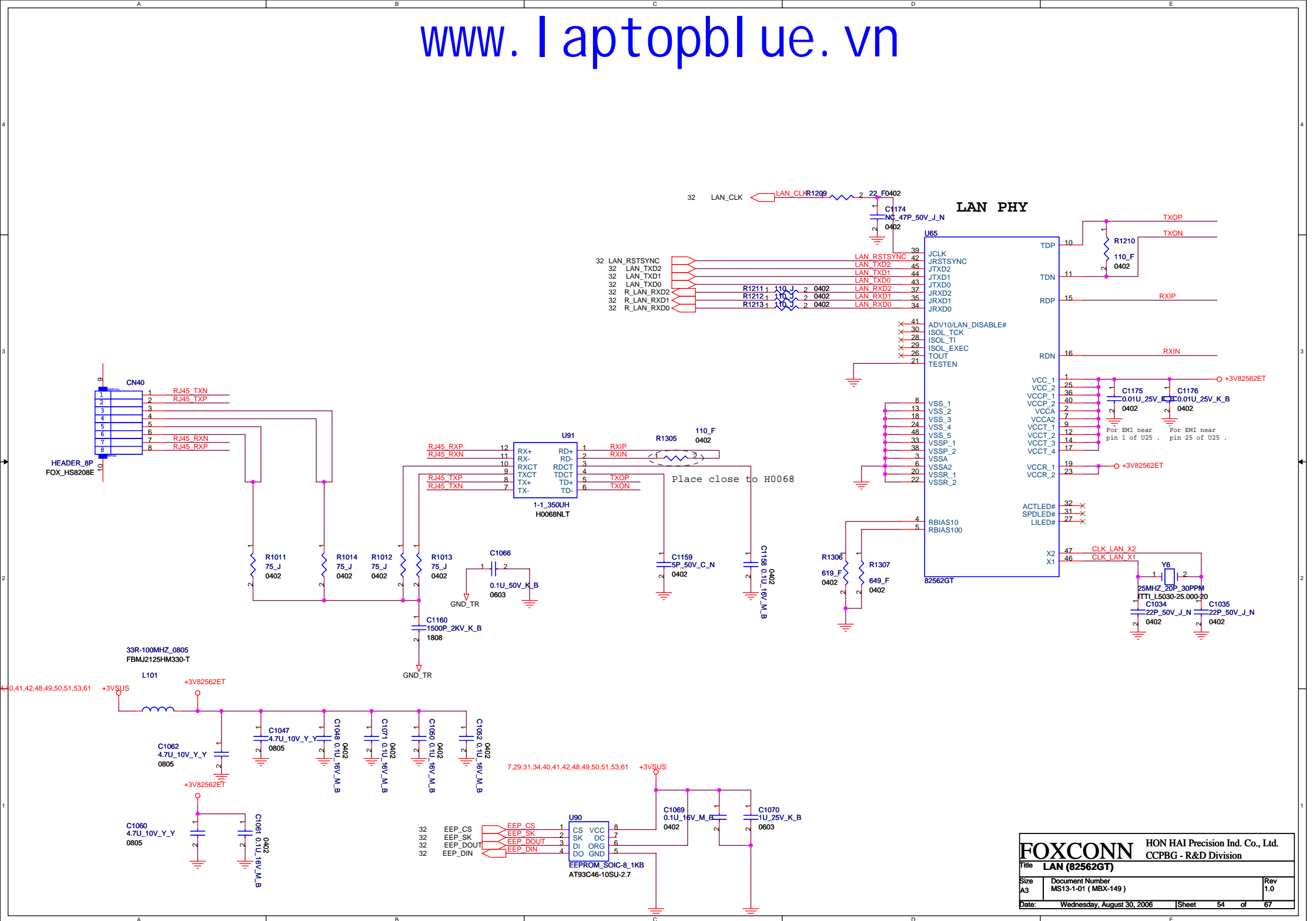
BOM notice:

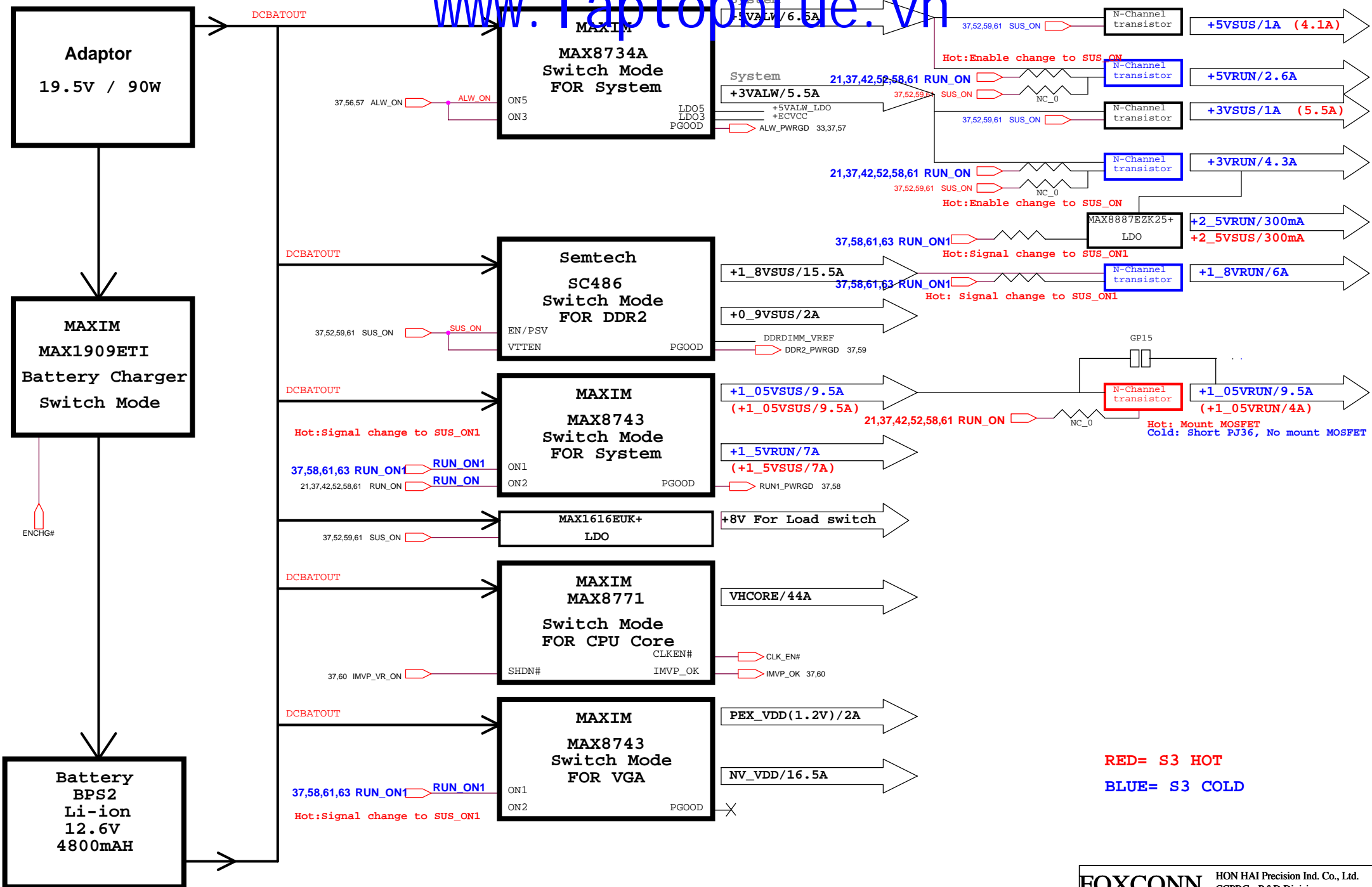
	R1196	R1197	R1198	R1199
BT + OIDE SKU	30 ohm	30 ohm	30 ohm	30 ohm
BT SKU	0 ohm	0 ohm	0 ohm	0 ohm
OIDE SKU	0 ohm	0 ohm	0 ohm	0 ohm

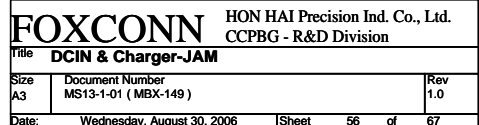


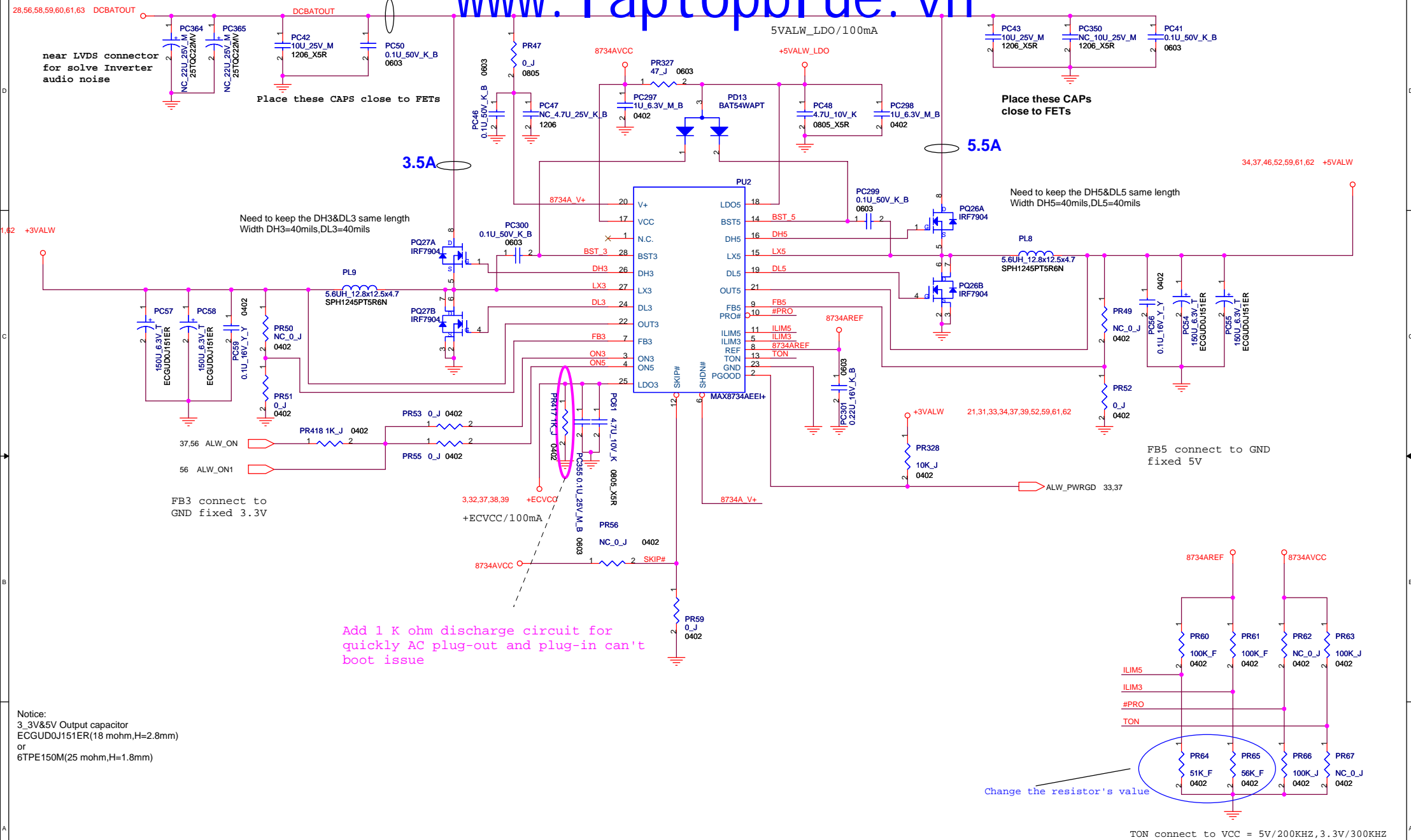
Follow MS20:

Add R1461 0 ohm to GND when EEPROM not in use  
to make sure GANGED# is not left floating  
When EEPROM is used, R1461 is NC









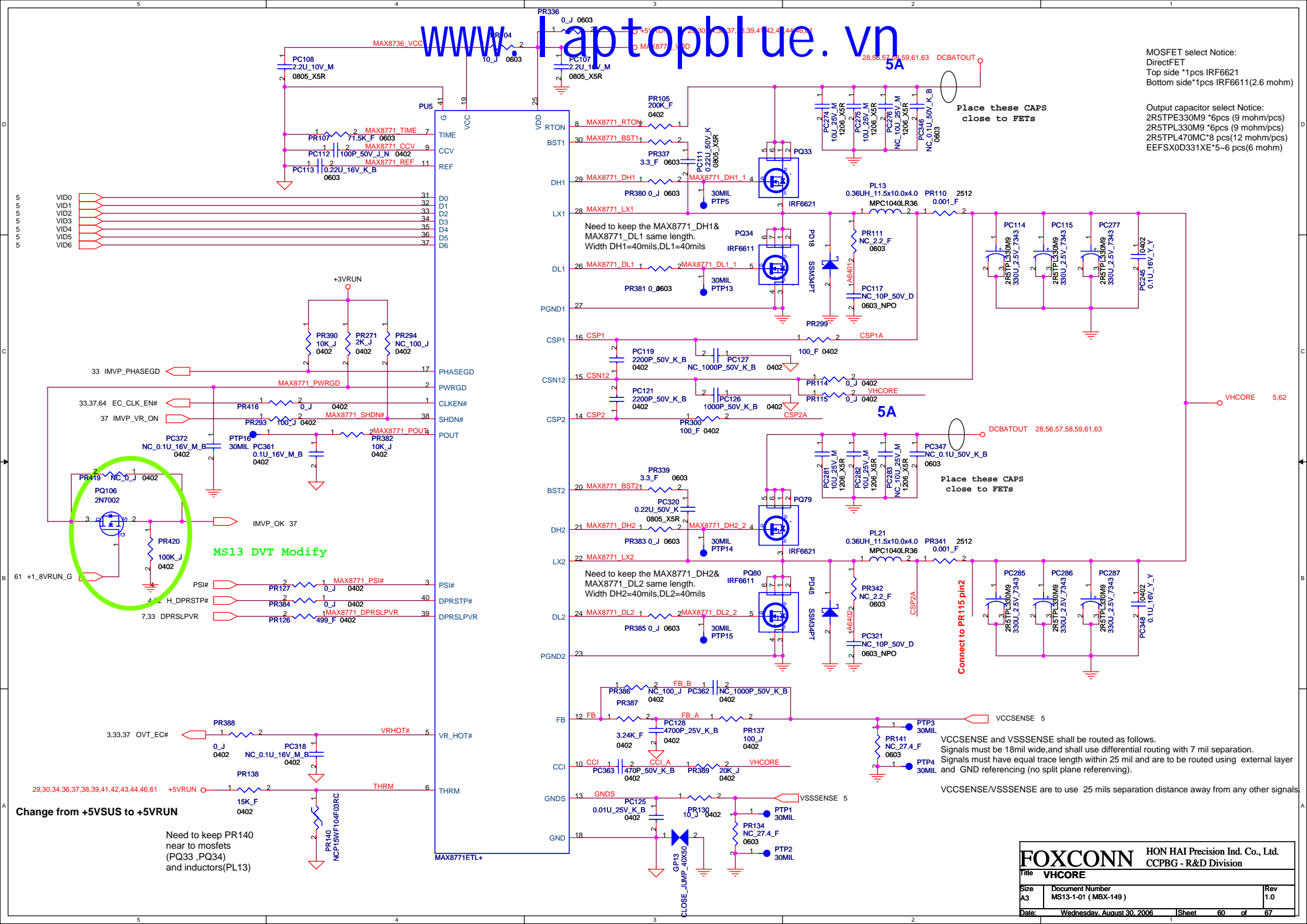
Notice:  
 3\_3V&5V Output capacitor  
 ECGUD0J151ER(18 mohm,H=2.8mm)  
 or  
 6TPE150M(25 mohm,H=1.8mm)







MOSFET select Notice:  
DirectFET  
Top side \*1pcs IRF6621  
Bottom side\*1pcs IRF6611(2.6 mohm)  
  
Output capacitor select Notice:  
2R5TPE330M9 \*6pcs (9 mohm/pcs)  
2R5TPL330M9 \*6pcs (9 mohm/pcs)  
2R5TPL470MC\*8 pcs(12 mohm/pcs)  
EEFSX0D331XE\*5-6 pcs(6 mohm)



Place these CAPS  
close to FETs

Need to keep the MAX8771\_DH1&  
MAX8771\_DL1 same length.  
Width DH1=40mils,DL1=40mils

Need to keep the MAX8771\_DH2&  
MAX8771\_DL2 same length.  
Width DH2=40mils,DL2=40mils

Place these CAPS  
close to FETs

Connect to PR115 pin2

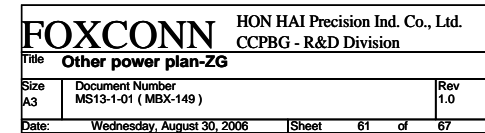
VCCSENSE and VSSSENSE shall be routed as follows.  
Signals must be 18mil wide, and shall use differential routing with 7 mil separation.  
Signals must have equal trace length within 25 mil and are to be routed using external layer  
and GND referencing (no split plane referreving).

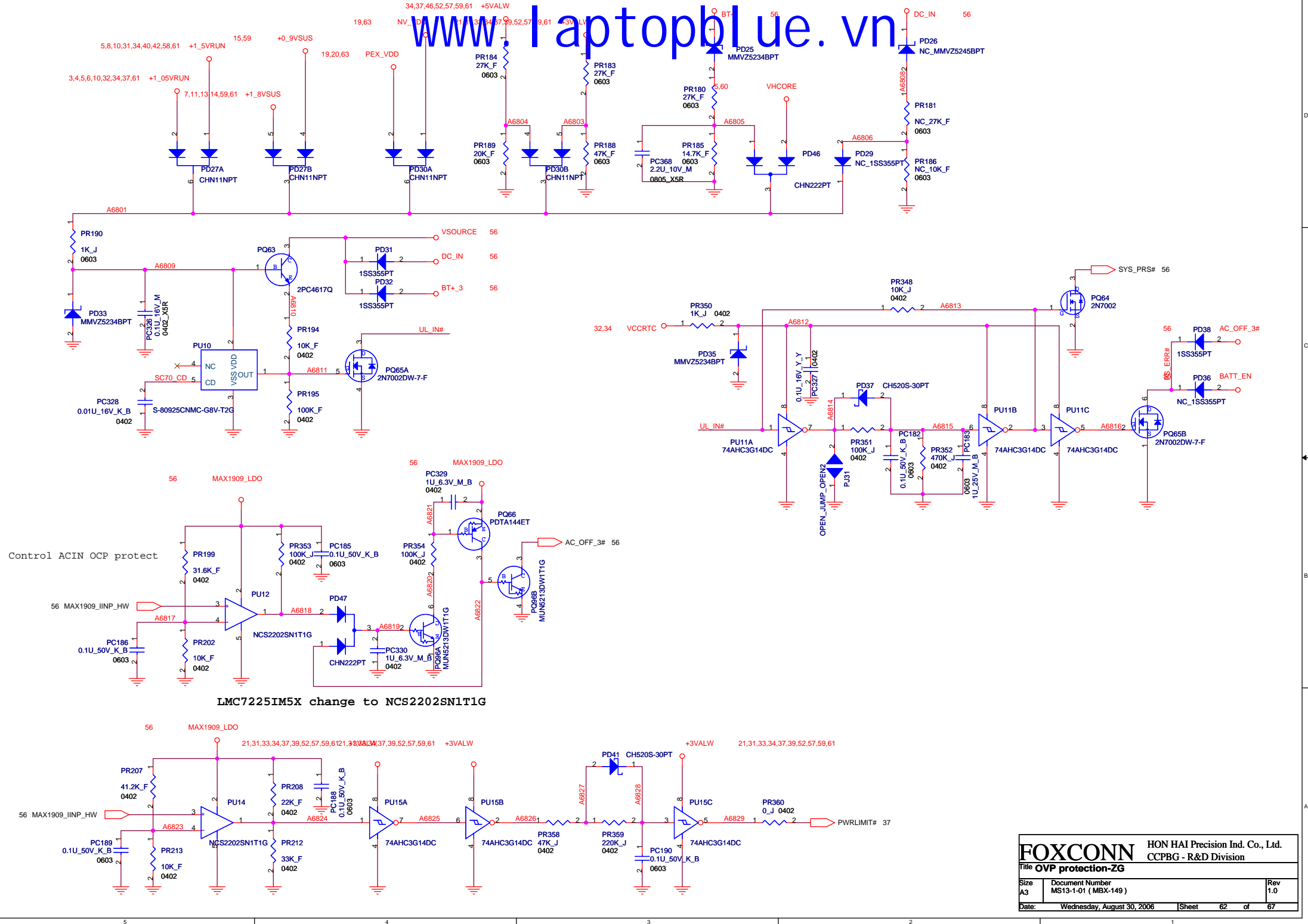
VCCSENSE/VSSSENSE are to use 25 mils separation distance away from any other signals.

MS13 DVT Modify

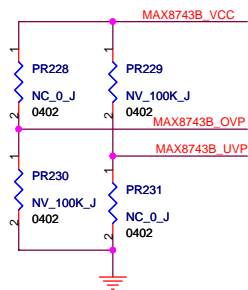
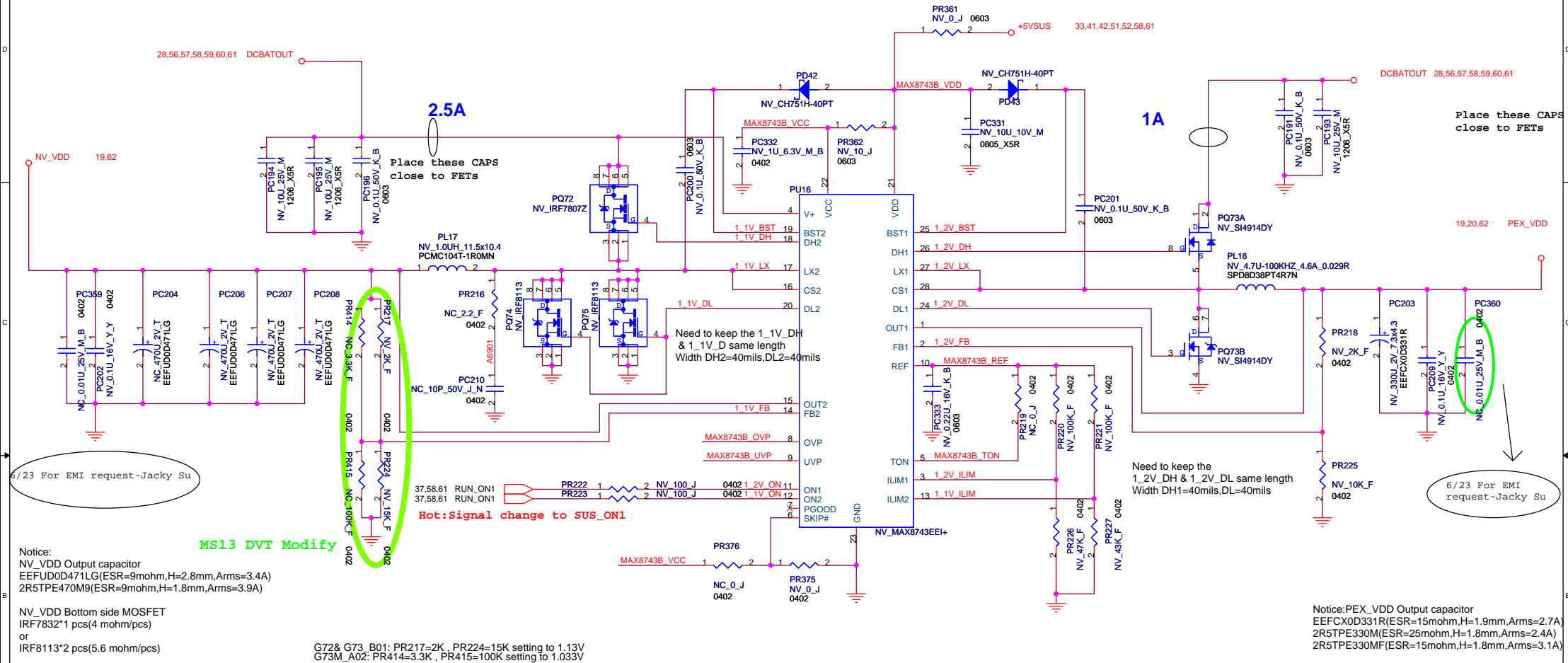
Change from +5VSUS to +5VRUN

Need to keep PR140  
near to mosfets  
(PQ33, PQ34)  
and inductors(PL13)



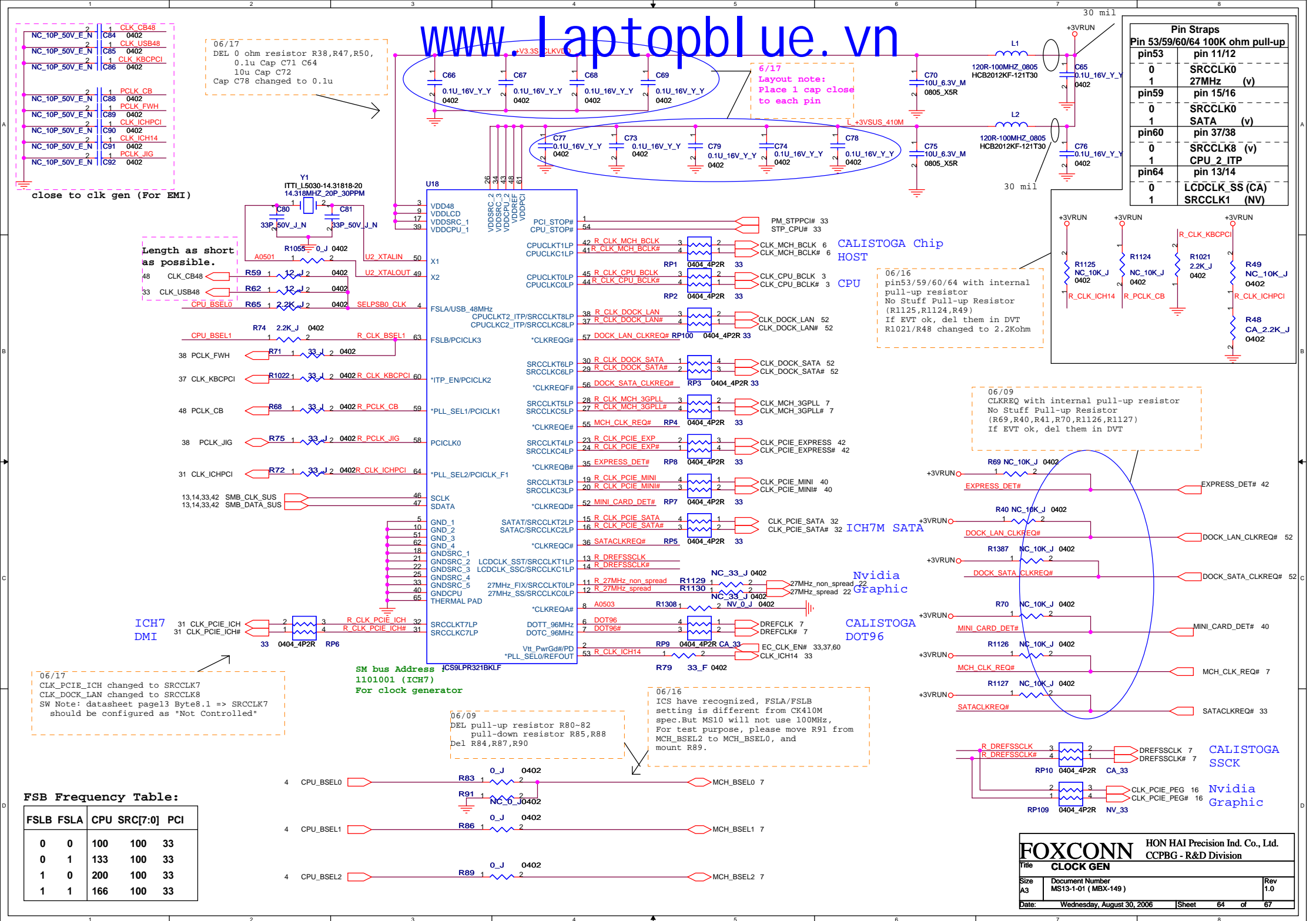


### 5/16 Change +5VRUN to +5VSUS



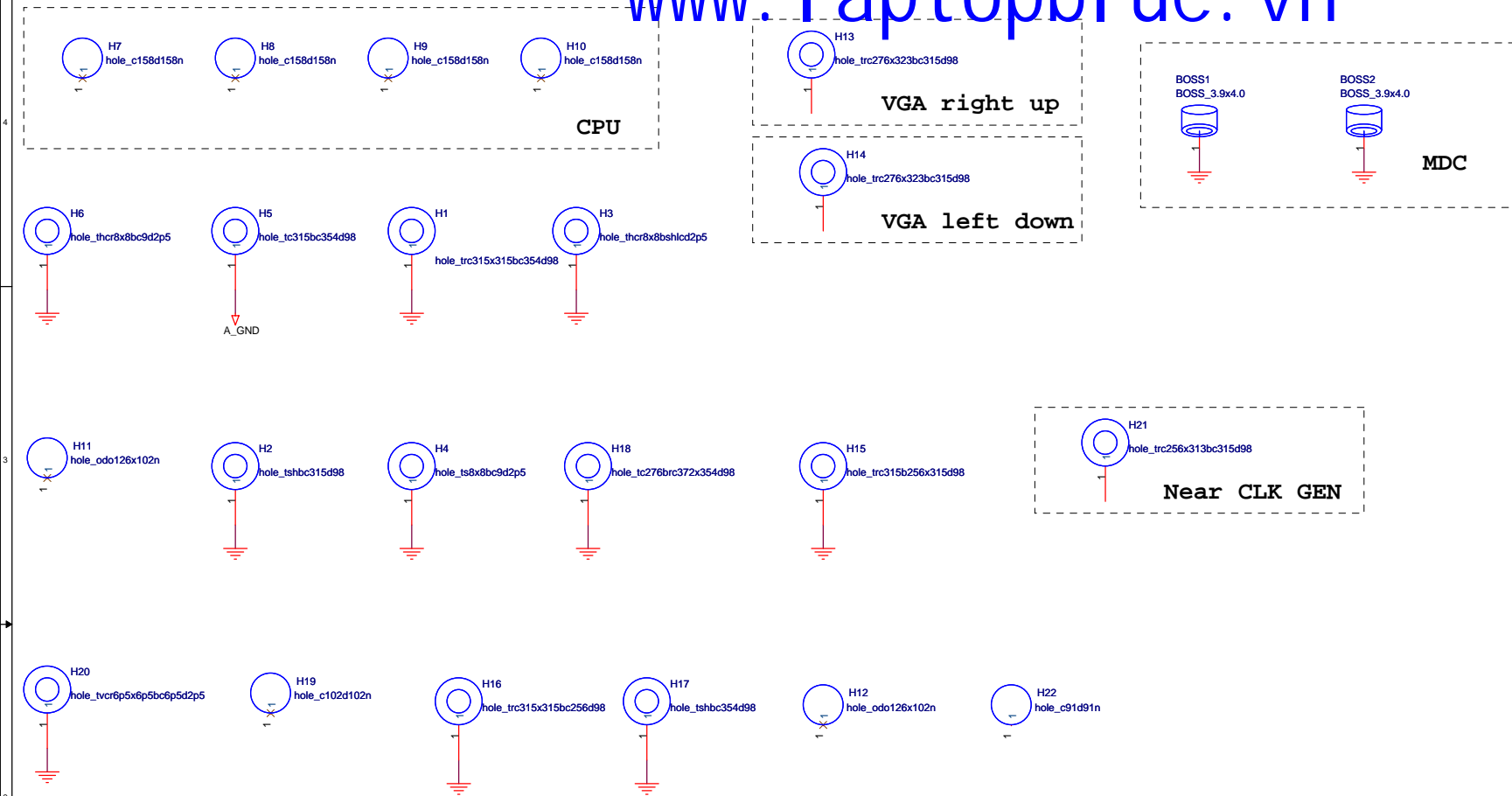
NV\_VDD=Vfb \* (1+R1/R2)  
Vfb=1V  
R1=PR217 or PR414  
R2=PR224 or PR415

<b>FOXCONN</b>		<b>HON HAI Precision Ind. Co., Ltd.</b>	
		<b>CCPBG - R&amp;D Division</b>	
<b>Title      +1_2VRUN+1_1VRUN-LYH</b>			
<b>Size</b>	<b>Document Number</b>	<b>Rev</b>	
<b>A3</b>	<b>MS13-1-01 (MBX-149)</b>	<b>1.0</b>	
<b>Date:</b>	<b>Wednesday, August 30, 2006</b>	<b>Sheet</b>	<b>63 of 67</b>



### FSB Frequency Table:

FSLB	FSLA	CPU	SRC[7:0]	PCI
0	0	100	100	33
0	1	133	100	33
1	0	200	100	33
1	1	166	100	33





HISTORY

(2006/08/16 Initail REV 1.0 )

- P.02 Because MS13 only use G73B01 version, since we delete head value of NV7273B01\_ and NV73A02\_.
- P.63 Change head value as below: PR217(NV7273B01\_2K\_F-->NV\_2K\_F) PR224(NV7273B01\_15K\_F-->NV\_15K\_F)  
PR414(NV73A02\_3.3K\_F-->NC\_3.3K\_F) PR415(NV73A02\_100K\_F-->NC\_100K\_F)
- P.45 Change C909,C920 from 220P\_50V\_J\_N to 100P\_50V\_K\_N. The change will make Frequency Response pass VISTA requirement.
- P.43 Change U39 from CXD9872KXXNBEB2XR to CXD9872AKDNBEC3XR(4th+).
- P.56 Change PR377 from 1K\_F to 15K\_F to avoid resistor damage when OVP occur.
- P.60 Add PQ106, PR420 to prevent glitch occur on the IMVP\_OK signal.
- P.41 Change fan control circuit as same as MS20.
- P.03 Reserve U110,R1467,C1324 for RTC stop issue.
- P.37 Add Q110 for RTC stop issue.
- P.37 Reserve D74 for RTC stop issue.
- P.44 Change C910, C911 from 0.033uF to 0.015uF and modify the size from 1206 to 0402 for co-layout. And we also add C1326,C1327 to keep 1206 size.
- P.47 Change R1330, R1339 from 10K to 9.1K and Change C1238, C1242 from 270pf to 150pf then the phone out D/A will pass.
- P.37 Add Q109, Q110 to prevent ACIN, BATT\_PR# and ENCHG# is faster than ECVCC.

(2006/08/18)

- P.33 Change R633 from 100\_J to 1K\_J and add D75 for PM\_RSMRST# falling timing fail issue.
- P.56 Change PR369 from NC\_0\_J to 15K\_J to make BATT\_PR# signal high level from 5V to 3.3V.
- P.10 Correct +1\_5VRUN maximum current description from 1885mA to 1900mA.
- P.11 Correct +1\_05VSUS maximum current description from 4.6A to 3.5A.
- P.11 Correct +1\_8VSUS maximum current description from 3.1A to 3.2A.

(2006/08/22)

- P.33 Correct D75 from NC\_CA\_SCS500V-40-LF to SCS500V-40-LF.
- P.41 Correct C1308 from NC\_0.01U\_25V\_K\_B to 0.047U\_16V\_M.

(2006/08/23)

- P.45 Change C909,C920 from 100pF to 33pF and change C1207, C1208 from 220pF to 3300pF.  
The Magnitude Response of Microphone(A-D) will be pass.
- P.37 Correct D74 from NC\_CA\_SCS500V-40-LF to NC\_SCS500V-40-LF.

(2006/08/24)

- P.43 Change U39 from CXD9872AKDNBEC3XR(4th+ with dolby) to CXD9872AKXNBEC3XR(4th+ without dolby).
- P.05 Change Cap1 from 330U\_2V\_T to NC\_330U\_2V\_T.
- P.11 Change Cap9 from 330U\_2V\_T to NC\_330U\_2V\_T.

(2006/08/28)

- P.36 Add VR1 for PACDN042Y3R shortage issue.

(2006/08/29)

- P.37 For system ID change, since change R724 from 100K\_J to NC\_100K\_J and change R725 from NC\_100K\_J to 100K\_J.

(2006/08/30)

- P.36 Change VR1 from NC\_MS06A05T1V1\_VR to MLVS0603M04\_VR. And change D72 from PACDN042Y3R to NC\_PACDN042Y3R.
- P.37 Add R1470 for MS13 DVT combine list.

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