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12	CPU Decoupling & VID	M87_MLB	57	DC-In & Battery Connectors	(MASTER)	(MASTER)
13	eXtended Debug Port (XDP)	T9_NOME	58	Power FETs	M87_MLB	08/28/2007
14	NB CPU Interface	T9_NOME	59	IMVP6 CPU VCore Regulator	MASTER	MASTER
15	NB PEG / Video Interfaces	T9_NOME	60	5V / 3.3V Power Supply	MASTER	08/28/2007
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22	NB Graphics Decoupling	M87_MLB	67	NV G84M PCI-E	M87_MLB	08/28/2007
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	27	SB Decoupling	MASTER	MASTER	72	NV G84M GPIO/MIO/Misc	M87_MLB	08/28/2007
	28	SB Misc	M87_MLB	08/28/2007	73	GPU Straps	M87_MLB	08/28/2007
	29	Clock (CK505)	T9_NOME	01/25/2007	74	NV G84M Video Interfaces	M87_MLB	08/28/2007
	30	Clock Termination	M87_MLB	08/28/2007	75	GPU (G84M) Core Supply	M87_MLB	09/26/2007
	31	DDR2 SO-DIMM Connector A	M87_MLB	08/28/2007	76	LVDS Display Connector	MASTER	MASTER
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	34	Left I/O Board Connector	(MASTER)	(MASTER)	79	1.8V FB Power Supply	MASTER	MASTER
	35	Ethernet (Yukon)	T9_NOME	01/25/2007	80	DVI Display Connector	MASTER	MASTER
	36	Yukon Power Control	T9_NOME	03/19/2007	81	Project Specific Connectors	(MASTER)	(MASTER)
	37	Ethernet Connector	M87_MLB	08/28/2007	82	LCD Backlight Support	M87_LIO	12/06/2007
	38	FireWire Link (TSB83AA22)	M87_MLB	08/28/2007	83	CPU/FSB Constraints	T9_NOME	01/25/2007
	39	FireWire PHY (TSB83AA22)	M87_MLB	08/28/2007	84	NB Constraints	T9_NOME	01/25/2007
	40	FireWire Port Power	M87_MLB	08/28/2007	85	Memory Constraints	T9_NOME	01/25/2007
	41	FireWire Ports	M87_MLB	08/28/2007	86	SB Constraints (1 of 2)	T9_NOME	01/25/2007
	42		MASTER	MASTER	87			
	43				88			
	44				89			
	45				90			

42	PATA Connector	MASTER	MASTER	87	SB Constraints (2 of 2)	T9_NAME	01/25/2007
43	External USB Connector	MASTER	MASTER	88	Clock & SMC Constraints	M87_MLB	08/28/2007
44	Left Clutch Barrel Interconnect	M87_MLB	08/28/2007	89	FireWire Constraints	T9_NAME	01/25/2007
45	SMC	M87_MLB					

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Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7431	1	SCHEM,MLB,MBP17	SCH	CRITICAL	
820-2262	1	PCBF,MLB,MBP17	PCB	CRITICAL	

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THIRD ANGLE PROJECTION

ENG APPD	/	MFG APPD	/
QA APPD	/	DESIGNER	/
RELEASE	/	SCALE	NONE
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TITLE
SCHEM,MLB,MBP17

DRAWING NUMBER
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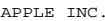
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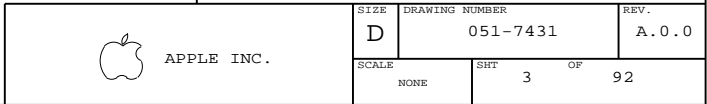
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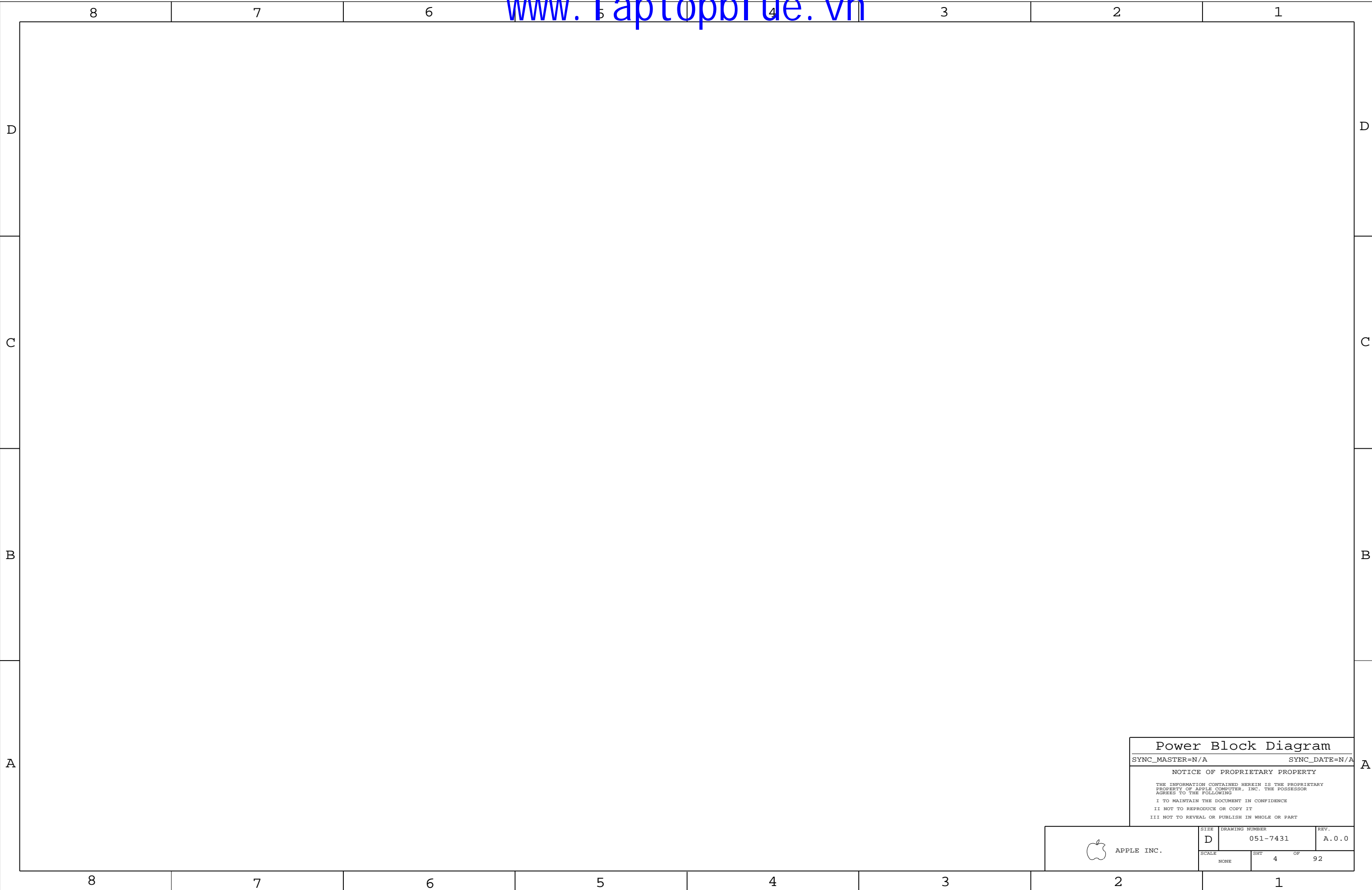
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Power Block Diagram			
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 APPLE INC.	SIZE D	DRAWING NUMBER 051-7431	REV. A.0.0
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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9092	PCBA, 2.6GHZ, 512VRAM-HY, M88	M88_COMMON, CPU_2_6GHZ, FB_512_HYNIX, EEE_Z3K
630-9093	PCBA, 2.6GHZ, 512VRAM-SAM, M88	M88_COMMON, CPU_2_6GHZ, FB_512_SAMSUNG, EEE_Z3L
630-9225	PCBA, 2.5GHZ, 512VRAM-HY, M88	M88_COMMON, CPU_2_5GHZ, FB_512_HYNIX, EEE_ZVW
630-9228	PCBA, 2.5GHZ, 512VRAM-SAM, M88	M88_COMMON, CPU_2_5GHZ, FB_512_SAMSUNG, EEE_ZVX

BOM Groups

BOM GROUP	BOM OPTIONS
M88_COMMON	COMMON, ALTERNATE, M88_COMMON1, M88_COMMON2, M88_DEBUG, M88_PROGPARTS
M88_COMMON1	BKLT_5V_PWR, ISL9504B, ONEWIRE_PU, GPUVID_1P23V
M88_COMMON2	PIV8S3_1V8, SMS_MOT_DIS, YUKON_ULTRA, VGA_TERM_CONN
M88_DEBUG	SMC_DEBUG_NO, XDP, LPCPLUS
M88_PROGPARTS	BOOTROM_PROG, SMC_PROG

BOM GROUP	BOM OPTIONS
FB_256_SAMSUNG	VRAM4, VRAM_16M, VRAM_SAMSUNG, VRAM_256_SAMSUNG
FB_256_HYNIX	VRAM4, VRAM_16M, VRAM_HYNIX, VRAM_256_HYNIX
FB_512_SAMSUNG	VRAM8, VRAM_16M, VRAM_SAMSUNG, VRAM_512_SAMSUNG
FB_512_HYNIX	VRAM8, VRAM_16M, VRAM_HYNIX, VRAM_512_HYNIX

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:Z3K]	CRITICAL	EEE_Z3K
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:Z3L]	CRITICAL	EEE_Z3L
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:ZVW]	CRITICAL	EEE_ZVW
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:ZVX]	CRITICAL	EEE_ZVX

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Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3559	1	IC, PDC, SR, PRQ, 2.6G, 35W, 800FSB, 6M, BGA	U1000	CRITICAL	CPU_2_6GHZ
337S3560	1	IC, PDC, SR, PRQ, 2.5G, 35W, 800FSB, 6M, BGA	U1000	CRITICAL	CPU_2_5GHZ
338S0509	1	IC, GPU, NV, G84M, BGA	U8000	CRITICAL	
338S0432	1	IC, NB, CRESTLINE, GM, CO, PRQ, ROHS-SPECIAL, 965PM	U1400	CRITICAL	
338S0434	1	IC, SB, ICH8M, B1, PRQ, BGA	U2300	CRITICAL	
353S1651	1	IC, ISL9504B, 2PH IMVP6 REG, PMON, QFN48	U7100	CRITICAL	ISL9504B
359S0130	1	IC, SLG2AP101, 1W PWR CLK GEN, CK505, QFN68	U2900	CRITICAL	
338S0386	1	IC, 88B8058, GIGABIT ENET XCVR, 64P QFN	U3700	CRITICAL	

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B

338S0274	1	IC, SMC, HS8/2116	U4900	CRITICAL	SMC_BLANK
341S2194	1	IC, SMC, DEVELOPMENT, M88	U4900	CRITICAL	SMC_PROG
335S0384	1	IC, 16MBIT 8-PIN SPI SERIAL FLASH, SOIC8	U6100	CRITICAL	BOOTROM_BLANK
341S2192	1	IC, EFI ROM, DEVELOPMENT, M87	U6100	CRITICAL	BOOTROM_PROG

333S0423	4	IC, SGRAM, GDDR3, 16MX32, 800MHZ, 136 FBGA	U8400, U8450, U8500, U8550	CRITICAL	VRAM_256_SAMSUNG
333S0423	8	IC, SGRAM, GDDR3, 16MX32, 800MHZ, 136 FBGA	U8400, U8450, U8450, U8450, U8450, U8450, U8450, U8450	CRITICAL	VRAM_512_SAMSUNG
333S0424	4	IC, SGRAM, GDDR3, 16MX32, 900MHZ, 136 FBGA	U8400, U8450, U8500, U8550	CRITICAL	VRAM_256_HYNIX
333S0424	8	IC, SGRAM, GDDR3, 16MX32, 900MHZ, 136 FBGA	U8400, U8450, U8450, U8450, U8450, U8450, U8450, U8450	CRITICAL	VRAM_512_HYNIX

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
157S0011	157S0030		ALL	BAR alt to TCM/BitTech magnetism
138S0603	138S0602		ALL	Barata alt to Memory 256M memoryless comp
353S1681	353S1294		ALL	SI alternate to M6100A1
376S0543	376S0466		ALL	SW alternate to Siliconix SI4401
152S0683	152S0276		ALL	Mag layers alternate to Data/Video
104S0024	104S0017		ALL	Resistor alt alternate to Optima
128S0083	128S0165		ALL	alternate to Helipex from Sanyo 100uF 16 volt
128S0113	128S0160		ALL	alternate to Helipex from Sanyo 220uF 16 volt
128S0115	128S0150		ALL	alternate to Helipex from Sanyo 100uF 16v
128S0122	128S0157		ALL	alternate to Helipex from Sanyo 220uF 16 volt
128S0057	128S0147		ALL	alternate to Helipex from Sanyo 100uF 16v
128S0056	128S0175		ALL	alternate to Helipex from Sanyo 100uF 16 volt
376S0448	376S0445		ALL	ALTERNATE for PDM206

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BOM Configuration

SYNC_MASTER=N/A SYNC_DATE=N/A

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SIZE
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051-7431

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D	<div>Proto:</div> <div>See earlier schematics for info about releases 0.0.1 - 4.0.0</div> <div>EVT:</div> <div>5.0.0:</div> <div>08/03/07 -- Page 5: Removed Q4690 BOM table entry. BOM table is on CSA pg. 46</div> <div>6.0.0 & 5.1.0:</div> <div>08/10/07 -- Synced to M87 MLB label 4.3.0</div> <div>08/10/07 -- Page 3: Revised power block diagram.</div> <div>08/10/07 -- Page 10-12: Updated U1000 CPU part number to reflect latest Penryn pin-out.</div> <div>08/10/07 -- Page 37: T3900,T3901 magnetics changed to 157S0053.</div> <div>08/10/07 -- Page 65: Changed L7810 3.425V G3 Hot inductor to 152S0301. R7070 changed from 100K to 10K.</div> <div>6.1.0:</div> <div>08/14/07 -- Synced to M87 MLB label 5.1.0</div> <div>08/14/07 -- Page 49: Changed Q5322 to SOT23 part same as M87.</div> <div>08/14/07 -- Page 75: Changed GPU VID pull up/downs to 2.2K ohms.</div> <div>6.2.0:</div> <div>08/16/07 -- Removed Rev B Silego clock chip as alternate.</div> <div>08/16/07 -- Page 51: Temp Sensors: Changed U5500 and U5570 to EMC1043-1 APN 353S1947.</div> <div>7.0.0:</div> <div>08/17/07 -- Page 48: Changed SMBus SMC "A" pull ups R5270 and R5271 to 3.3K to improve rise time on SCL..</div> <div>7.1.0:</div> <div>08/22/07 -- Page. 9,34: Added GPIOs to support iPhone headset. ICH8 GPIO 22 IPHS_SW_BIAS_EN_L routes to JJ3400.63</div> <div>08/22/07 -- Page. 9,34: Removed R3410 and R3411. ICH8 GPIO 2 IPHS_SW_INT routes to JJ3400.65</div> <div>08/22/07 -- Synced M87 MLB label 6.2.0</div> <div>08/22/07 -- Page 51: Temp sensors: Added R5501,R5502,R5571,R5572 pull ups on U5500 and U5570.</div> <div>08/22/07 -- Page 61: R7455 changed to 7.5K to change max load current margin on PPIV05.</div> <div>08/22/07 -- Page 90: Changed frame buffer net physical type to GDDR3_50SE.</div> <div>08/22/07 -- Synced M87 LIO label 1.5.0</div> <div>08/22/07 -- Page 66: U7901 voltage follower changed from OPA333 to OPA705.</div> <div>08/22/07 -- Page 82: Changed L9891,L9893,L9894 to 155S0220</div> <div>7.2.0:</div> <div>08/23/07 -- Page 5: Changed CPU parts to ES2, B1 for EVT</div> <div>08/23/07 -- Page 9: IPHS_SW_BIAS_EN_L now connected to SB_SLOAD (GPIO 38).</div> <div>08/23/07 -- Synced M87 MLB label 6.5.0</div> <div>08/23/07 -- Page 50: Current Sensors: Changed U5410 and U5440 to MAX4245 Changed R5413 and R5443 to 0.005 ohm resistors.</div> <div>08/23/07 -- Page 91: Added diff pair properties to new current sensor pairs.</div> <div>08/23/07 -- Synced M87 LIO label 1.7.0</div> <div>08/23/07 -- Page 66: Changed U7901 to MAX4245. Changed F7902 to 740S0055.</div> <div>08/23/07 -- Page 82: Add BOMOPTION OMIT to RX9892.</div> <div>8.0.0:</div> <div>08/24/07 -- Page 25: Added NO STUFF to R2552 (was pull up on SB GPIO38 which is now used on IPHS).</div> <div>08/24/07 -- Page 59: CPU Vcore supply changes per characterizationChanged L7100 and L7101 to 152S0624. Changed C7134 to 0.01uF 132S0042.</div> <div>8.1.0:</div> <div>08/24/07 -- Synced M87 MLB label 8.2.0</div> <div>Page 5,75: Changed BOM option to GPUVID_1P23V</div> <div>Page 73: Changed R5491 and R5493 to 6.81K to allow full resolution of GPUVCORE current sense</div> <div>Page 50: Adding C5411,C5412,C5441,C5442 feedback caps for current sense op amps</div> <div>Page 66: Changed R7920 to halogen free 107S0110.</div> <div>8.2.0:</div> <div>08/29/07 -- Synced m87_mlb CSA pgs. Major release label name : m87_mlb_051-7413.8.2.0</div> <div>08/29/07 -- Changed net physical and net spacing to CRT_50S on these signals NB_CLK100M_DPLSS_P/N NB_CLK96M_DOT_P/N</div> <div>8.3.0:</div> <div>08/29/07 -- Changed the following filters to 155S0371 for supply issues: pg. 43 L4600 pg. 44 FL4735 pg. 76 L9010,L9011</div> <div>08/29/07 -- pg. 80 L9460,L9464,L9468,L9476,L9480,L9484</div> <div>8.4.0:</div> <div>08/30/07 -- Changed the orientation on these filters to match layout: pg. 43 L4600 pg. 76 L9010,L9011</div> <div>9.0.0:</div> <div>08/30/07 -- RFA 529050 EVT Release of Schematic BOM and PCBF</div> <div>9.1.0: BOM Changes only</div> <div>09/04/07 -- Page 5: Added alternate sources for these parts:</div> <div>09/04/07 -- 152S0683 is the Mag layers alternate for Dale/Vishay inductors.</div>											
	C	<div>09/04/07 -- 128S0164 is the Kemet alternate to Sanyo caps</div> <div>09/04/07 -- 104S0023 is the Panasonic alternate to Cyntec resistors</div> <div>09/04/07 -- Page 50: Changed R5425 and R5435 to 104S0023.</div> <div>10.0.0:</div> <div>09/06/07 -- HF capacitor substitution, with halogen parts as alternates. pg. 5 Alternates BOM table updates.</div> <div>11.0.0:</div> <div>09/11/07 -- Page 57: Removed NO STUFF from DZ6960 (377S0044), ESD diode on BATT_POS per Chris.</div> <div>09/11/07 -- Page 5: Removed alternate to 128S0164 Kemet 220uF tantalum cap at C7540 and C7541.</div> <div>09/11/07 -- Added BOM variants and EEE codes for 2.5GHz:</div> <div>09/11/07 -- 630-9225: ZVW PCBA,2.5GHZ,512VRAM-HY,M88</div> <div>09/11/07 -- 630-9228: ZVX PCBA,2.5GHZ,512VRAM-SAM,M88</div> <div>09/11/07 -- Page 62: Removed OMIT property and BOM option table to make C7540 and C7541 only 128S0073.</div> <div>09/11/07 -- Page 82: LCD Backlight Added OMIT properties and BOM option table to change these beads to 155S0220: L9891,L9893,L9894</div>										
B		<div>DVT:</div> <div>11.1.0:</div> <div>09/12/07 --Page 66: Swapped U7901 pins 1 and 3 signals (positive and negative inputs).</div> <div>11.2.0:</div> <div>09/26/07 -- Synced M*& MLB label 10.2.0</div> <div>09/26/07 -- Page 50 & 75: GPUVCORE: Current sense to use IMVP6 IMON + Non-inverting Opamp removed R8992,C8992</div> <div>09/26/07 -- Page 65: Changed C7860 to 0.0047uF (radar://5468257</div> <div>12.0.0:</div> <div>09/28/07 -- Removed BOM tables and OMIT BOM options from HF capacitor substitution, with halogen parts as alternates.</div> <div>09/28/07 -- Synced M87 MLB label 10.3.0</div> <div>09/28/07 -- Page 50: updating GPUVcore current sense resistor values for gain of 4.83</div> <div>12.0.0:</div> <div>10/01/07 -- Synced M87 LIO label 9.0.0 Added R9810</div> <div>10/01/07 -- Synced M87 LIO label 7.0.0</div> <div>10/01/07 -- <rdar://problem/5493576> M87/M88 MLB/LED: LED driver current mirror can not be disabled + power sequencing issue</div> <div><rdar://problem/5510696> TASK: M87 LIO changes to support LED board</div> <div>10/01/07 -- Page 5: Added 376S0448 as alternate for 376S0445.</div> <div>13.0.0:</div> <div>10/05/07 -- Page 5: Removed HDCP ROM. Removed U8770, R8770,R871, C8770.</div> <div>10/05/07 -- Page 75: GPU Vcore supply: Changed L8920 from 152S0525 to 152S0697.Dale 0.9uH 27A inductor has smaller pad size than Vishay IHLP4040.</div> <div>13.1.0:</div> <div>10/09/07 -- Synced m87_MLB label Change 72968 Page 5: Changed Module parts for new Penryn APNs.</div> <div>10/09/07 -- Page 93: <rdar://problem/5525486> M87/88 1V8 FB DC converter transient response improve/BOM change</div> <div>10/09/07 -- R9308 change to 40.2k, 0402, 1%; C9308 change to 680pF, 0402, 10V, 10% C9307 change to 68pF, 0402, 10V, 10%</div>										
	A											
	8	7	6	5	4	3	2	1				

Functional Test Points

Fan Connectors

FUNC_TEST		
TP50	TRUE	PP5V_S0
TP51	TRUE	FAN_LT_PWM
TP52	TRUE	FAN_LT_TACH
TP53	TRUE	FAN_RT_PWM
TP54	TRUE	FAN_RT_TACH

LPC+ Debug Connector

FUNC_TEST		
TP55	TRUE	PP3V42_G3H
TP56	TRUE	PP5V_S0
TP57	TRUE	LPC_AD<0>
TP58	TRUE	LPC_AD<1>
TP59	TRUE	LPC_FRAME_L
TP60	TRUE	PM_CLKRUN_L
TP61	TRUE	PCI_FW_GNT_L
TP62	TRUE	SMC_TMS
TP63	TRUE	DEBUG_RESET_L
TP64	TRUE	SMC_TRST_L
TP65	TRUE	SMC_TDO
TP66	TRUE	SMC_MD1
TP67	TRUE	SMC_TX_L
TP68	TRUE	FWH_INIT_L
TP69	TRUE	PCI_CLK33M_LPCPLUS
TP70	TRUE	LPC_AD<2>
TP71	TRUE	LPC_AD<3>
TP72	TRUE	INT_SERIRQ
TP73	TRUE	PM_SUS_STAT_L
TP74	TRUE	SMC_TDI
TP75	TRUE	SMC_TCK
TP76	TRUE	SMC_RESET_L
TP77	TRUE	SMC_NMI
TP78	TRUE	SMC_RX_L
TP79	TRUE	LINDACARD_GPIO

Left ALS

FUNC_TEST		
TP80	TRUE	ALS_GAIN
TP81	TRUE	LTAIS_OUT
TP82	TRUE	GND

Thermal Diode Connectors

FUNC_TEST		
TP83	TRUE	HSTHMSNS_D_P
TP84	TRUE	HSTHMSNS_D_N
TP85	TRUE	RSFSTHMSNS_D_P
TP86	TRUE	RSFSTHMSNS_D_N
TP87	TRUE	CPUTHMSNS_D2_P
TP88	TRUE	CPUTHMSNS_D2_N

System Validation TPs

FUNC_TEST		
TP89	TRUE	CPU_PWRGD
TP90	TRUE	CPU_DPSLP_L
TP91	TRUE	PM_DPRSLEPVR
TP92	TRUE	CPU_DPSLP_L
TP93	TRUE	PM_LAN_ENABLE
TP94	TRUE	PCI_RST_L
TP95	TRUE	PM_RSMRST_L
TP96	TRUE	PM_SB_PWROK
TP97	TRUE	SB_RTC_RST_L
TP98	TRUE	PM_STPCPU_L
TP99	TRUE	PM_STPPCI_L
TP100	TRUE	VR_PWRGD_CLKEN
TP101	TRUE	VR_PWRGOOD_DELAY
TP102	TRUE	FSB_CPURST_L
TP103	TRUE	FSB_CPUSLP_L
TP104	TRUE	FSB_DPWR_L
TP105	TRUE	NB_SB_SYNC_L
TP106	TRUE	PM_BMBUSY_L

Battery Digital Connector

FUNC_TEST		
TP107	TRUE	SMC_BS_ALERT_L
TP108	TRUE	SMBUS_SMC_BSA_SCL
TP109	TRUE	SMBUS_SMC_BSA_SDA
TP110	TRUE	BATT_POS
TP111	TRUE	GND

Left I/O Power Connector

FUNC_TEST		
TP112	TRUE	PP18V5_DCIN
TP113	TRUE	PPBUS_G3H
TP114	TRUE	GND

Request for at least 10 GND test points

NOTE: 10 additional GND test points are called out separately in these notes.

RTC Battery Connector

FUNC_TEST		
TP115	TRUE	PPVBATT_G3_RTC
TP116	TRUE	GND

Current Sense Calibration

FUNC_TEST		
TP117	TRUE	ISENSE_CAL_EN
TP118	TRUE	PP5V_S0
TP119	TRUE	PPVCORE_S0_CPU
TP120	TRUE	PPVCORE_GPU
TP121	TRUE	GND

2 TPs per

6 TPs, 2 with each of above TP pairs

Left Clutch Barrel Connector

FUNC_TEST		
TP122	TRUE	PP5V_S3_CAMERA_F
TP123	TRUE	USB_CAMERA_F_N
TP124	TRUE	USB_CAMERA_F_P

Other Func Test Points

FUNC_TEST		
TP125	TRUE	PM_SYSRST_L
TP126	TRUE	SMC_ONOFF_L

ICT Test Points

CPU FSB NO_TESTS

MAKE BASE	NO_TEST	
TP127	TRUE	FSB_A_L<31...3>
TP128	TRUE	FSB_ADS_L
TP129	TRUE	FSB_ADSTB_L<1...0>
TP130	TRUE	FSB_BNR_L
TP131	TRUE	FSB_BREQ0_L
TP132	TRUE	FSB_D_L<63...0>
TP133	TRUE	FSB_DBSY_L
TP134	TRUE	FSB_DINV_L<3...0>
TP135	TRUE	FSB_DEDY_L
TP136	TRUE	FSB_DSTB_L_N<3...0>
TP137	TRUE	FSB_DSTB_L_P<3...0>
TP138	TRUE	FSB_HIT_L
TP139	TRUE	FSB_HITM_L
TP140	TRUE	FSB_LOCK_L
TP141	TRUE	FSB_REO_L<4...0>
TP142	TRUE	NC_CPU_RSVD5

NB NO_TESTS

MAKE BASE	NO_TEST	
TP143	TRUE	NC_NB_NC<1...16>
TP144	TRUE	NC_NB_RSVD<26...27>
TP145	TRUE	NC_NB_RSVD<24>

Backlight Connector

FUNC_TEST		
TP146	TRUE	BKLT_PWR
TP147	TRUE	BKLT_GND
TP148	TRUE	BKLT_P5V_EN
TP149	TRUE	BKLT_PWM
TP150	TRUE	GND

IR & Sleep LED Connector

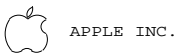
FUNC_TEST		
TP151	TRUE	PP5V_S3
TP152	TRUE	USB_IR_N
TP153	TRUE	USB_IR_P
TP154	TRUE	SYS_LED_ANODE
TP155	TRUE	GND

Functional / ICT Test

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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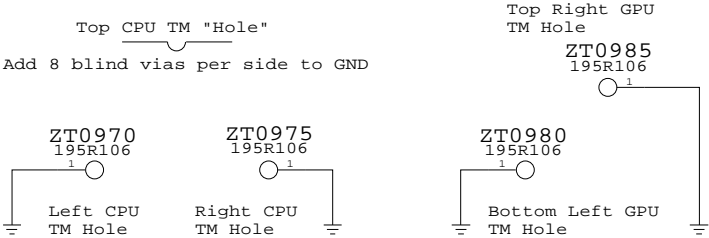
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D	051-7431	A.0.0
SCALE	SHT	OF
NONE	7	92

86 24 9	TP_USB_EXTDN MAKE_BASE=TRUE	==	TP_USB_EXTDN MAKE_BASE=TRUE	9 24 86
86 24 9	TP_USB_EXTDP MAKE_BASE=TRUE	==	TP_USB_EXTDP MAKE_BASE=TRUE	9 24 86
28 25 9 7	PM_SB_PWROK MAKE_BASE=TRUE	==	PM_SB_PWROK	7 9 25 28
59 28 16 9 7	VR_PWRGOOD_DELAY MAKE_BASE=TRUE	==	VR_PWRGOOD_DELAY	7 9 16 28 59
88 67 30 29 9	PEG_CLK100M_GPU_P MAKE_BASE=TRUE	==	PEG_CLK100M_GPU_P	9 29 30 67 88
88 67 30 29 9	PEG_CLK100M_GPU_N MAKE_BASE=TRUE	==	PEG_CLK100M_GPU_N	9 29 30 67 88
55 45 9	SMC_SMS_INT MAKE_BASE=TRUE	==	SMC_SMS_INT	9 45 55
23 9	TP_EXTGPU_PWR_EN MAKE_BASE=TRUE	==	TP_EXTGPU_PWR_EN	9 23
34 25 9	IPHS_SW_BIAS_EN_L MAKE_BASE=TRUE	==	IPHS_SW_BIAS_EN_L	9 25 34
34 24 9	IPHS_SW_INT MAKE_BASE=TRUE	==	IPHS_SW_INT	9 24 34
66 46 45 9	SMC_ENRGYSTR_LDO_EN MAKE_BASE=TRUE	==	SMC_ENRGYSTR_LDO_EN	9 45 46 66
31 9	TP_MEM_A_A<15> MAKE_BASE=TRUE	==	TP_MEM_A_A<15>	9 31
32 9	TP_MEM_B_A<15> MAKE_BASE=TRUE	==	TP_MEM_B_A<15>	9 32
82 28 24 9 7	PLT_RST_L	==	PLT_RST_L	7 9 24 28 82
82 73 72 9	GPU_BL_PWM	==	GPU_BL_PWM	9 72 73 82
82 73 72 9	GPU_BKLT_EN	==	GPU_BKLT_EN	9 72 73 82

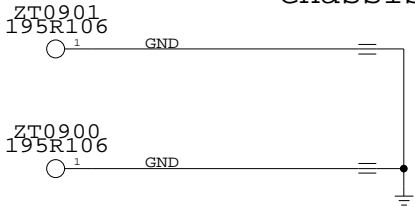
Thermal Module Holes

All holes are plated through holes with two exceptions:

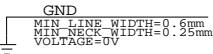
- GND_CHASSIS_RIGHT_FAN_NOTCH (to the left of small well on lower board edge near USB)
- GND_CHASSIS_BATTCONN_HOLE (to the left of DIMM cutout near board edge)



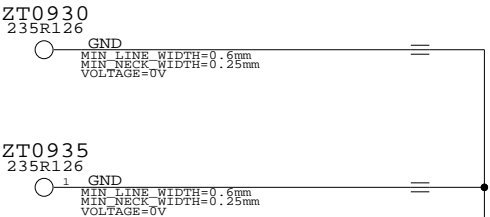
Chassis GNDS



Digital Ground



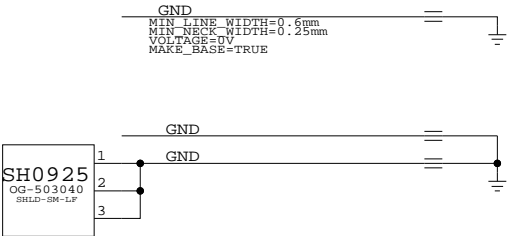
RAM door (Torx) holes



Frame holes



Chassis connection to be made at the mounting hole east of the LVDS connector

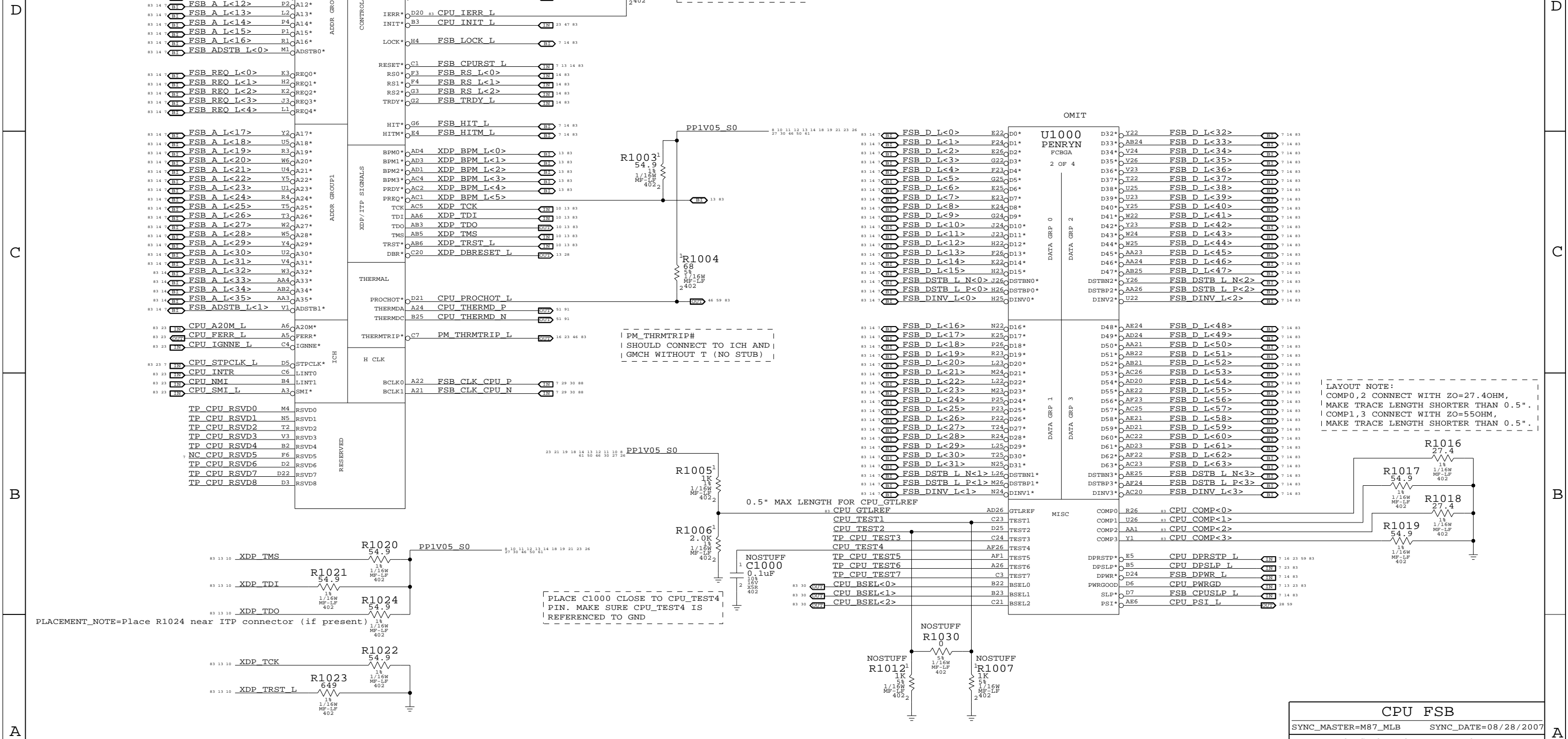


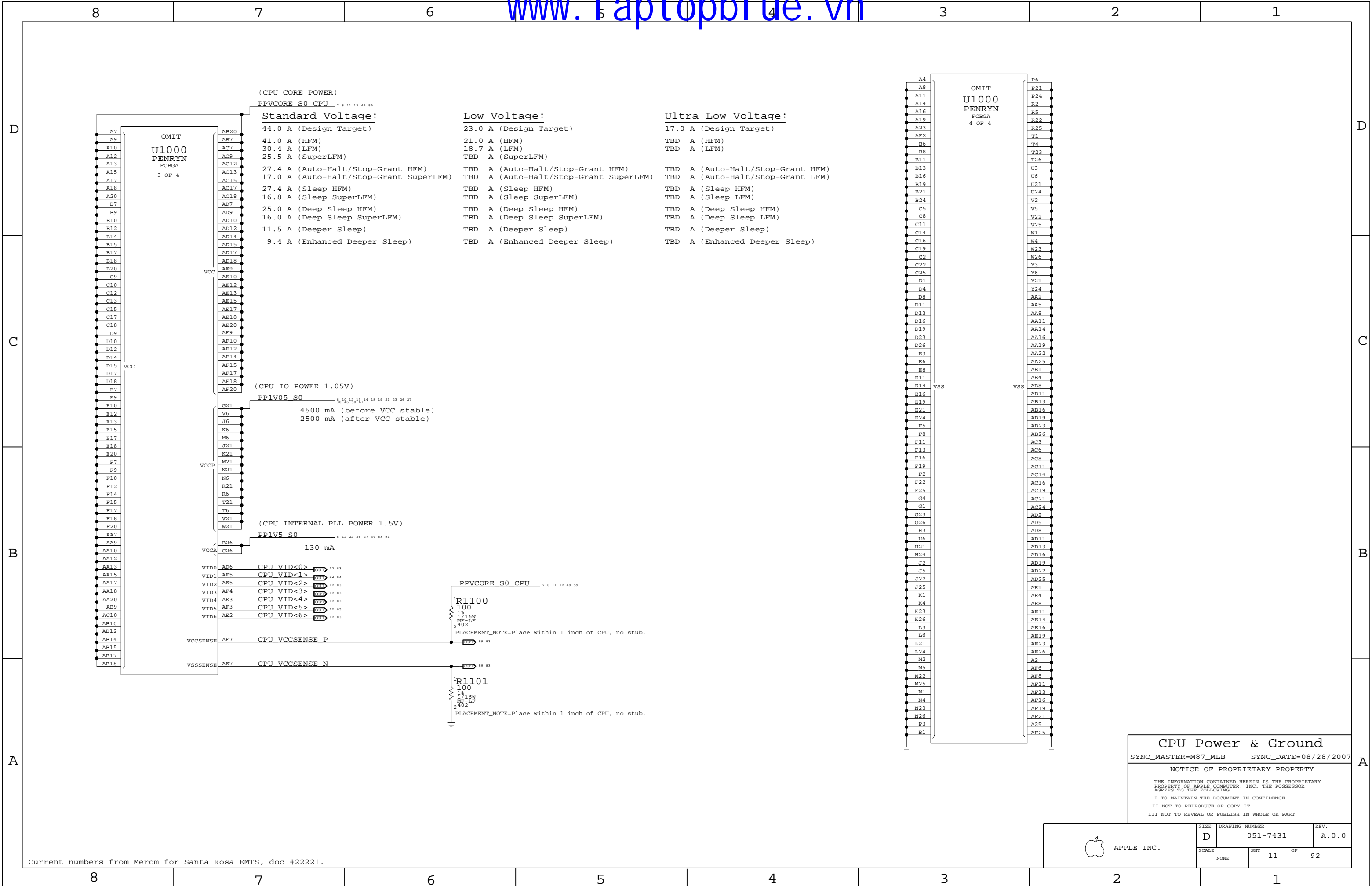
Signal Aliases

SYNC_MASTER=MASTER		SYNC_DATE=MASTER	
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SIZE D	DRAWING NUMBER 051-7431	REV. A.0.0
SCALE NONE	SHT 9	OF 92





CPU Power & Ground

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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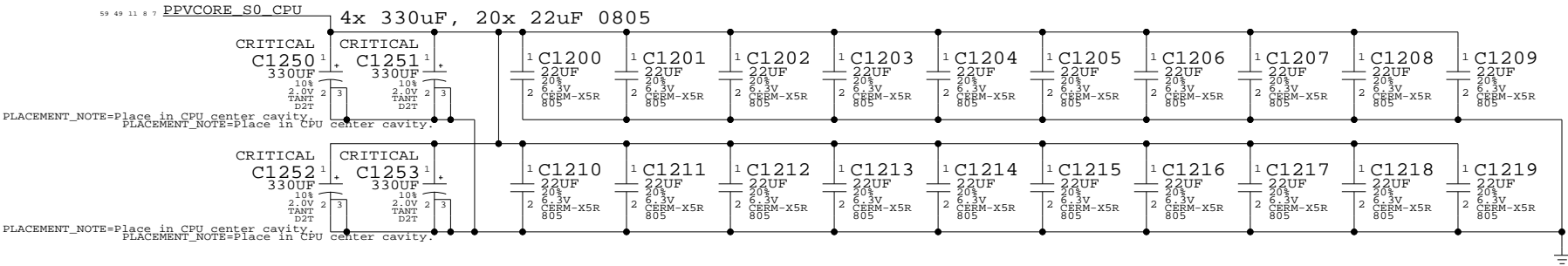
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SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE	SHT 11 OF 92	
NONE		

CPU VCORE HF AND BULK DECOUPLING

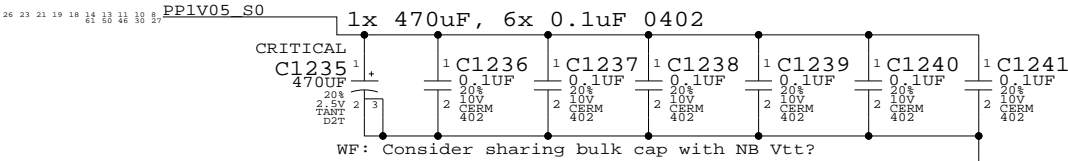


CPU VCORE VID CONNECTIONS

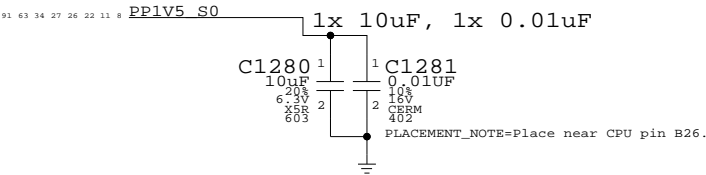
83 11 CPU_VID<0..6> == IMVP6_VID<0..6> 7 59 83

MAKE_BASE=TRUE

VCCP (CPU I/O) DECOUPLING



VCCA (CPU AVdd) DECOUPLING



CPU Decoupling & VID

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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SIZE

D

DRAWING NUMBER

051-7431

REV.

A.0.0

SCALE

NONE

SHT

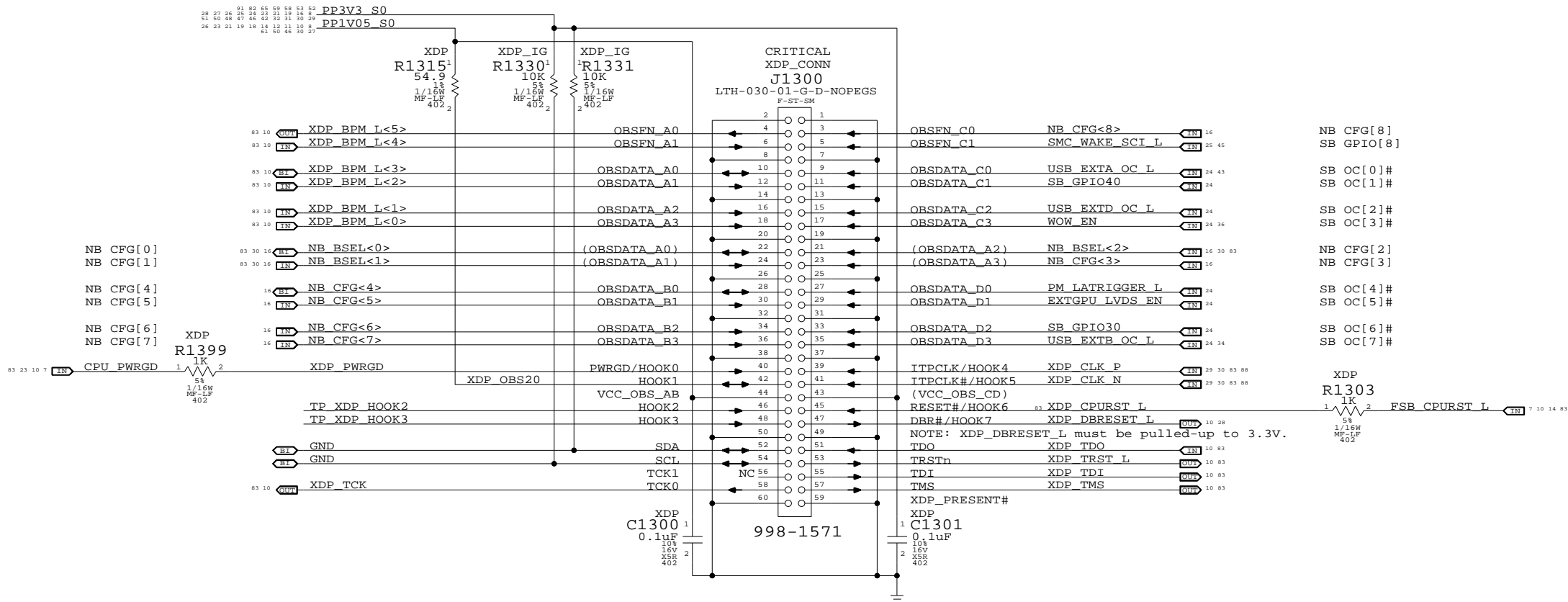
12

OF

92

Mini-XDP Connector

NOTE: This is not the standard XDP pinout.
Use with 920-0451 adapter board to support CPU, NB & SB debugging.



Direction of XDP module
Please avoid any obstructions
on even-numbered side of J1300

eXtended Debug Port (XDP)

SYNC_MASTER=T9_NOME SYNC_DATE=01/22/2007

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SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE	SHT 13 OF 92	
NONE		

D

C

B

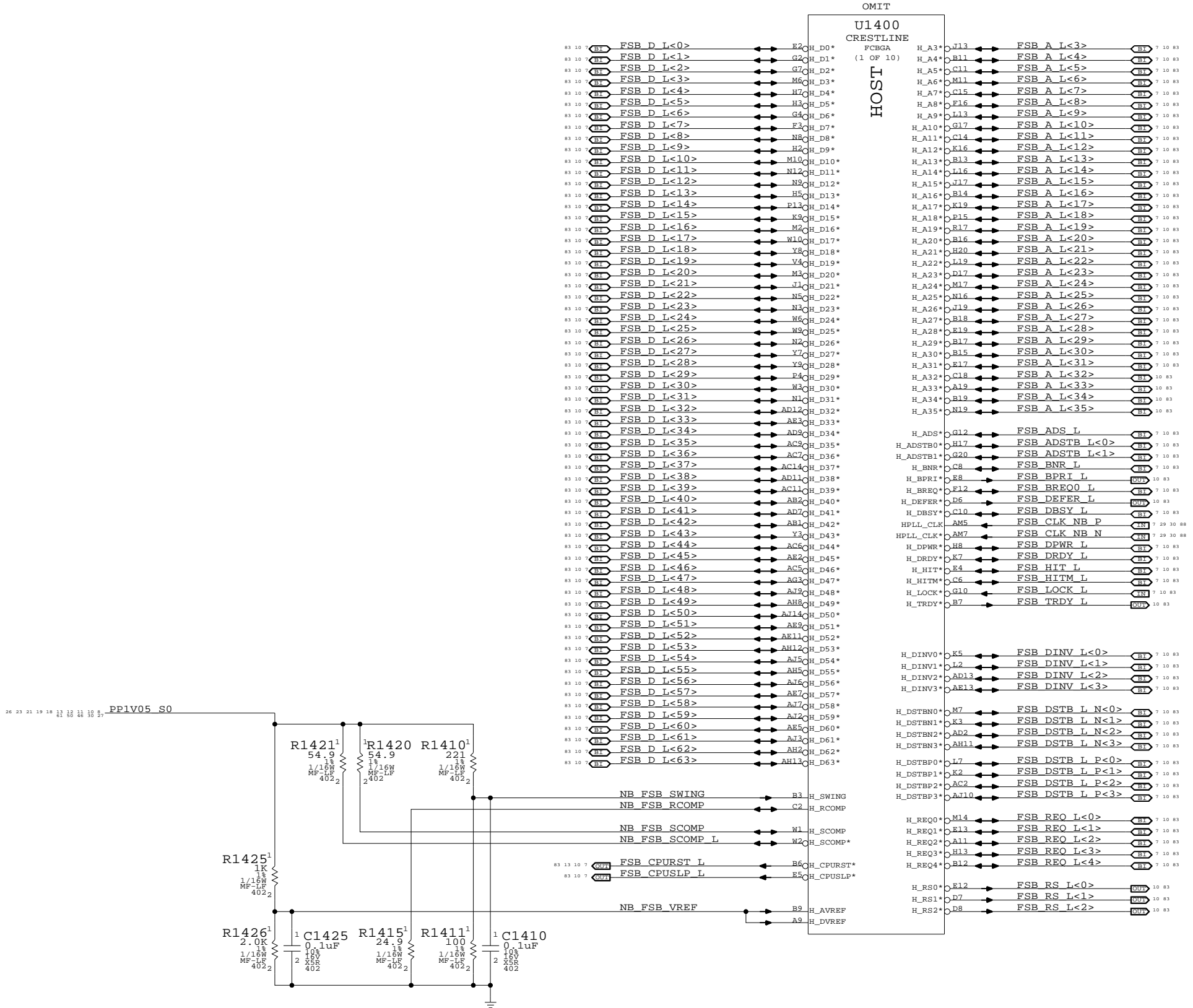
A

D

C

B

A



NB CPU Interface

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

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D

C

B

A

LVDS Disable

Can leave all signals NC if LVDS is not implemented.
Tie VCC_TX_LVDS and VCCA_LVDS to GND.

If SDVO is used, VCCD_LVDS must remain powered with proper decoupling. Otherwise, tie VCCD_LVDS to GND also.

Note: SR DG says to tie LVDS_VREFH/L to GND. This causes a glitch during wake-up on LVDS DATA/CLK pairs. New recommendation is to float both signals, see Radar #5067636.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable / CRT Enable

Tie TVx_DAC and TVx_RTN to GND. Must power all TVDAC rails. VCCA_TVx_DAC and VCCA_DAC_BG can share filtering with VCCA_CRT_DAC.

CRT Disable / TV-Out Enable

Tie R/R#/G/G#/B/B#, HSYNC and VSYNC to GND. All CRT/TVDAC rails must be powered. All rails must be filtered except for VCCA_CRT.

CRT & TV-Out Disable

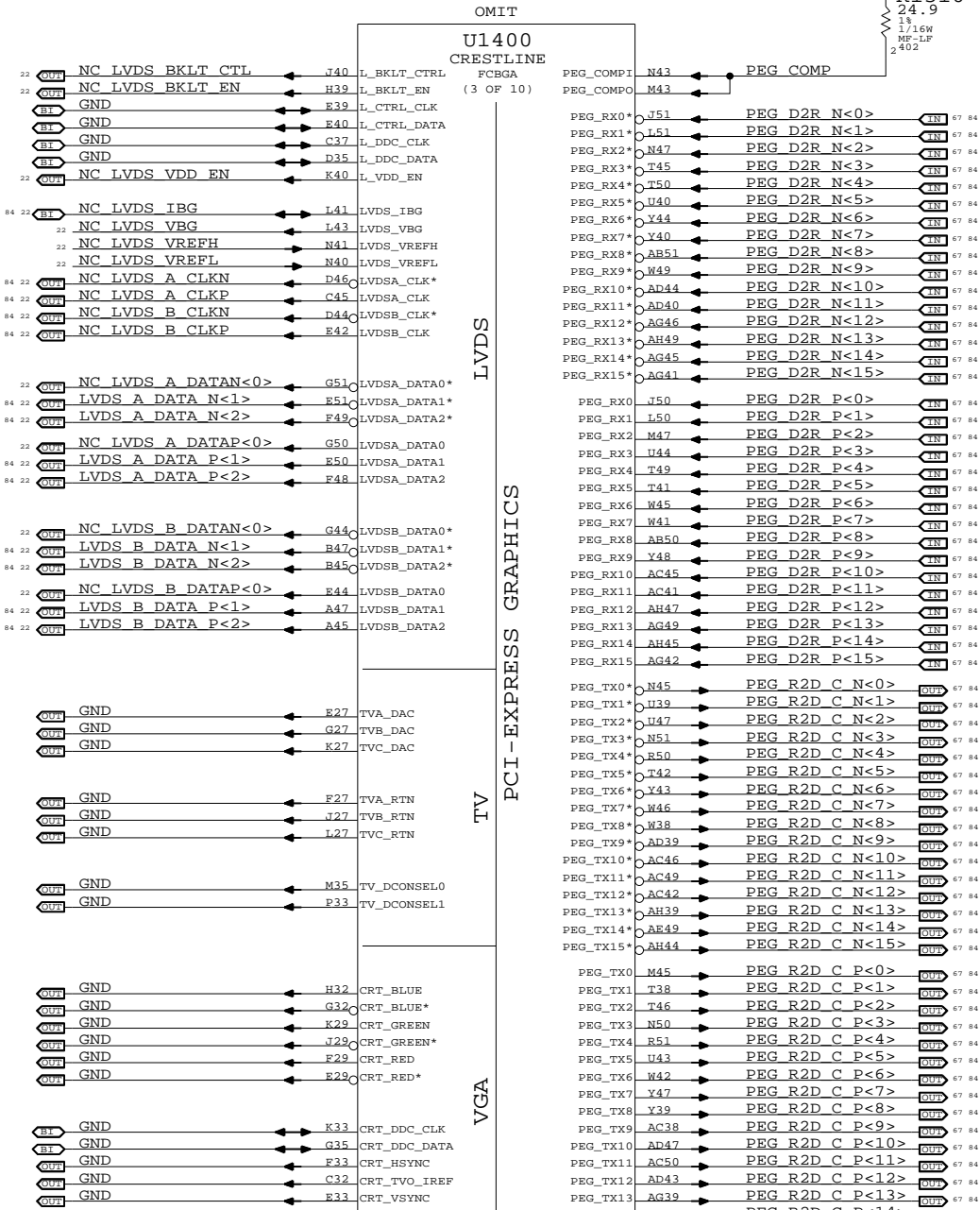
Tie TVx_DAC, TVx_RTN, R/R#/G/G#/B/B#, HSYNC, VSYNC and CRT_TVO_IREF to GND.
Can tie the following rails to GND:
VCCA_CRT_DAC, VCCA_DAC_BG, VCCA_TVx_DAC, VCCD_CRT, VCCD_QDAC and VCC_SYNC.

NOTE: Must keep VDDC_TVDAC powered and filtered at all times!

Internal Graphics Disable

Follow instructions for LVDS and CRT & TV-Out Disable above. Can also tie CRT_DDC_*, L_CTRL_*, L_DDC_*, SDVO_CTRL_* and TV_DCONSELx to GND.

Tie DPLL_REF_CLK and DPLL_REF_SSCLK to GND.
Tie DPLL_REF_CLK* and DPLL_REF_SSCLK* to VCC (VCore).
Tie VCCA_DPLLA and VCCA_DPLLB to VCC (VCore).
Tie VCC_AXG and VCC_AXG_NCTF to GND.
Leave GFX_VID<3..0> and GFX_VR_EN as NC.



SDVO Alternate Function

SDVO_TVCLKIN#
SDVO_INT#
SDVO_FLDSTALL#

SDVO_TVCLKIN
SDVO_INT
SDVO_FLDSTALL

SDVOB_RED#
SDVOB_GREEN#
SDVOB_BLUE#
SDVOB_CLKN
SDVOC_RED#
SDVOC_GREEN#
SDVOC_BLUE#
SDVOC_CLKN

SDVOB_RED
SDVOB_GREEN
SDVOB_BLUE
SDVOB_CLKP
SDVOC_RED
SDVOC_GREEN
SDVOC_BLUE
SDVOC_CLKP

NB PEG / Video Interfaces

SYNC_MASTER=T9_NOME SYNC_DATE=03/19/2007

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APPLE INC.

SIZE

D

DRAWING NUMBER

051-7431

REV.

A.0.0

SCALE

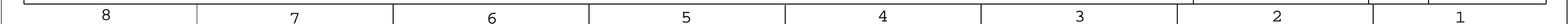
NONE

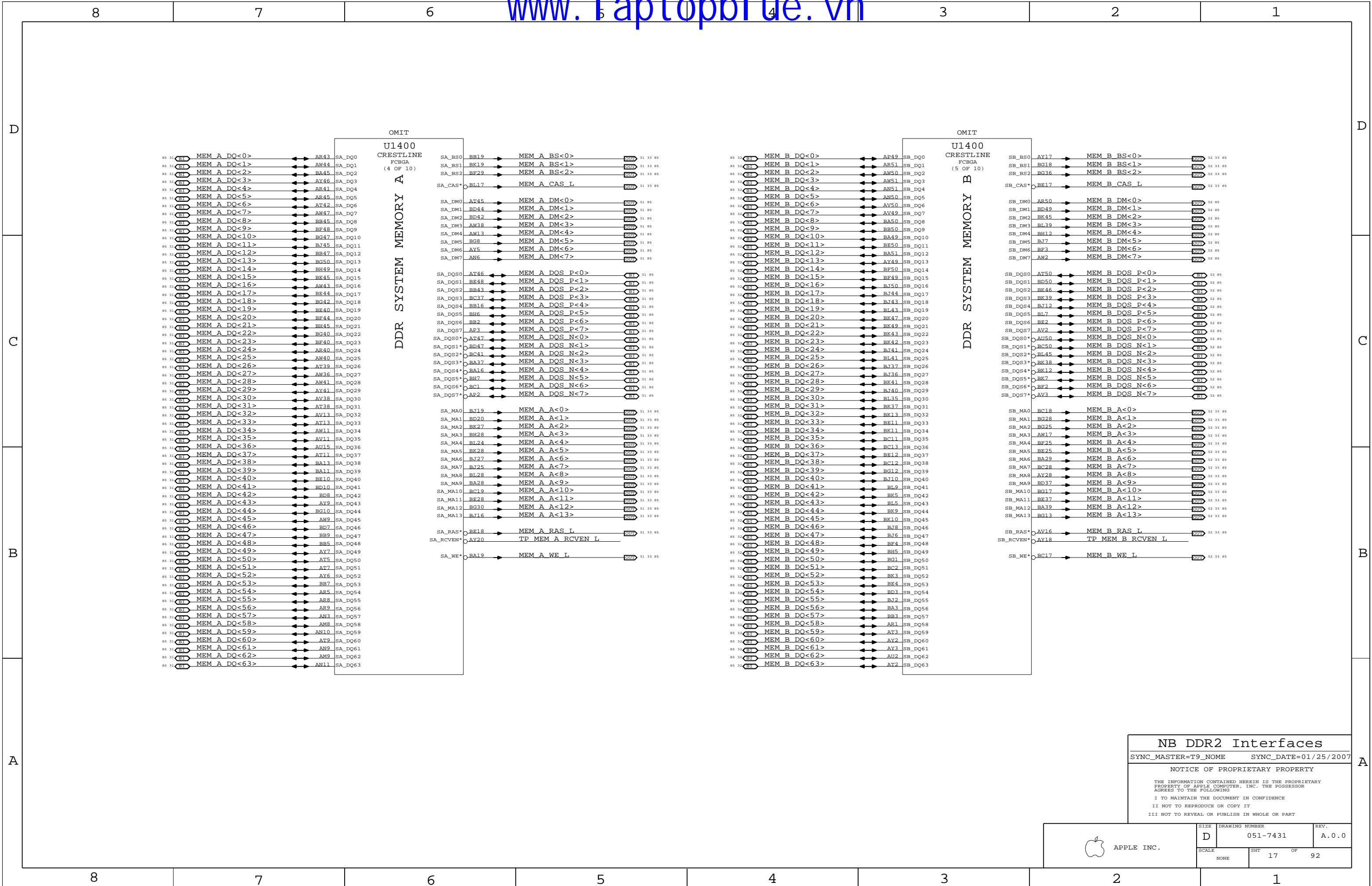
SHT

15

OF

92

DCA |



NB DDR2 Interfaces

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

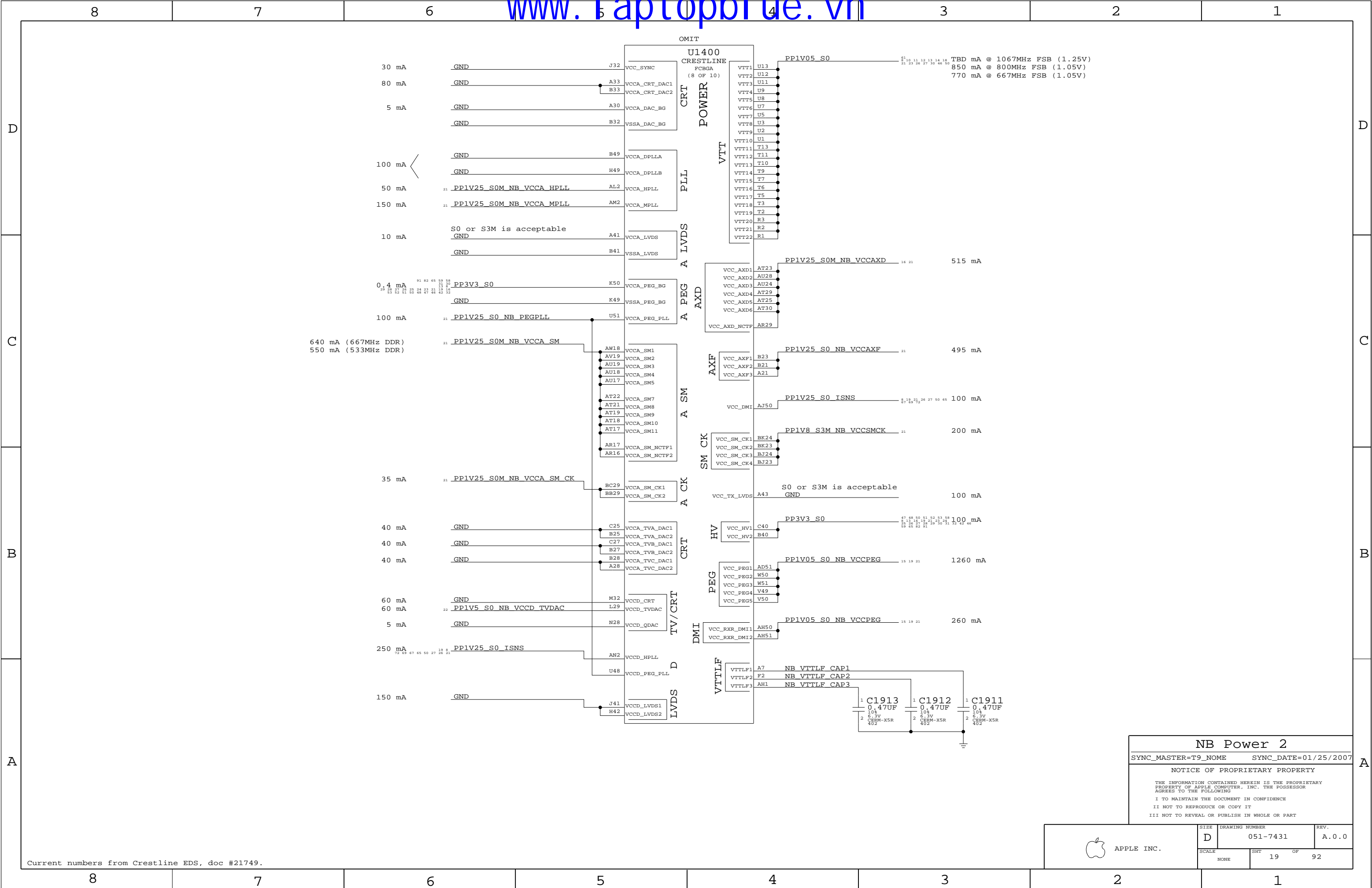
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NB Power 2

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007


NOTICE OF PROPRIETARY PROPERTY

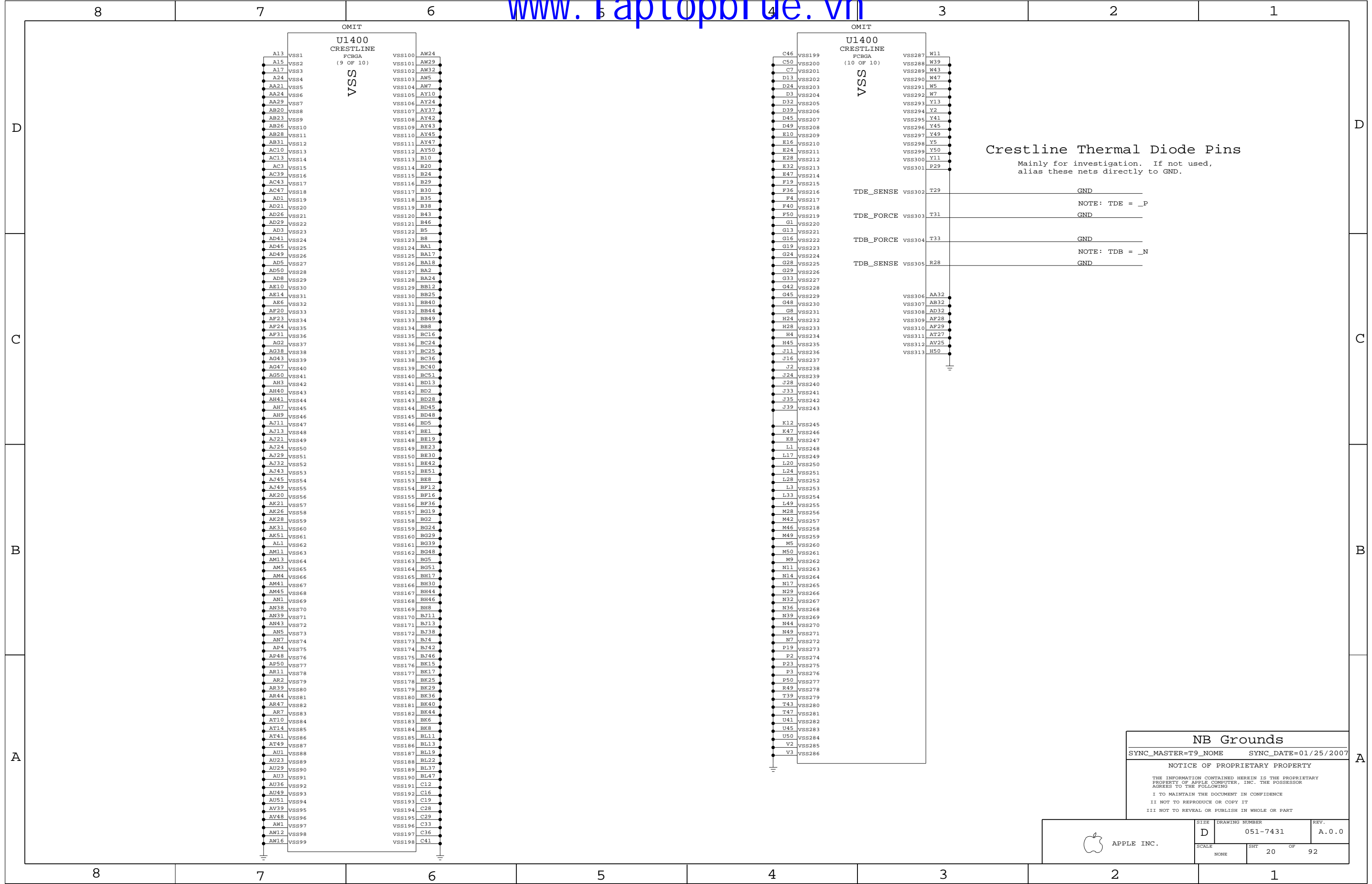
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

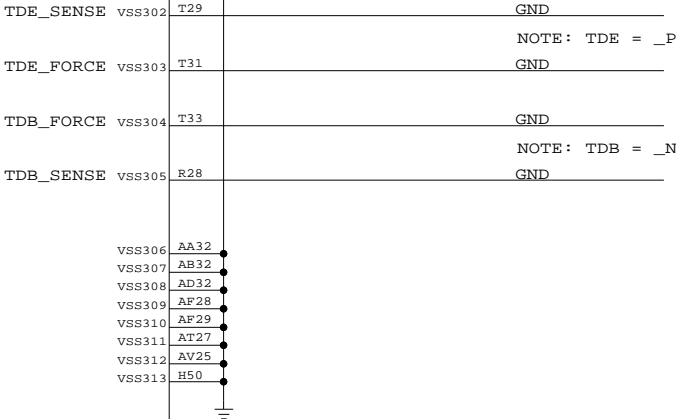
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

 APPLE INC.	SIZE D	DRAWING NUMBER 051-7431	REV. A.0.0
	SCALE NONE	SHT 19	OF 92



Crestline Thermal Diode Pins
Mainly for investigation. If not used,
alias these nets directly to GND.



NB Grounds

SYNC_MASTER=T9_NOME

SYNC_DATE=01/25/2007

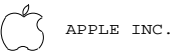
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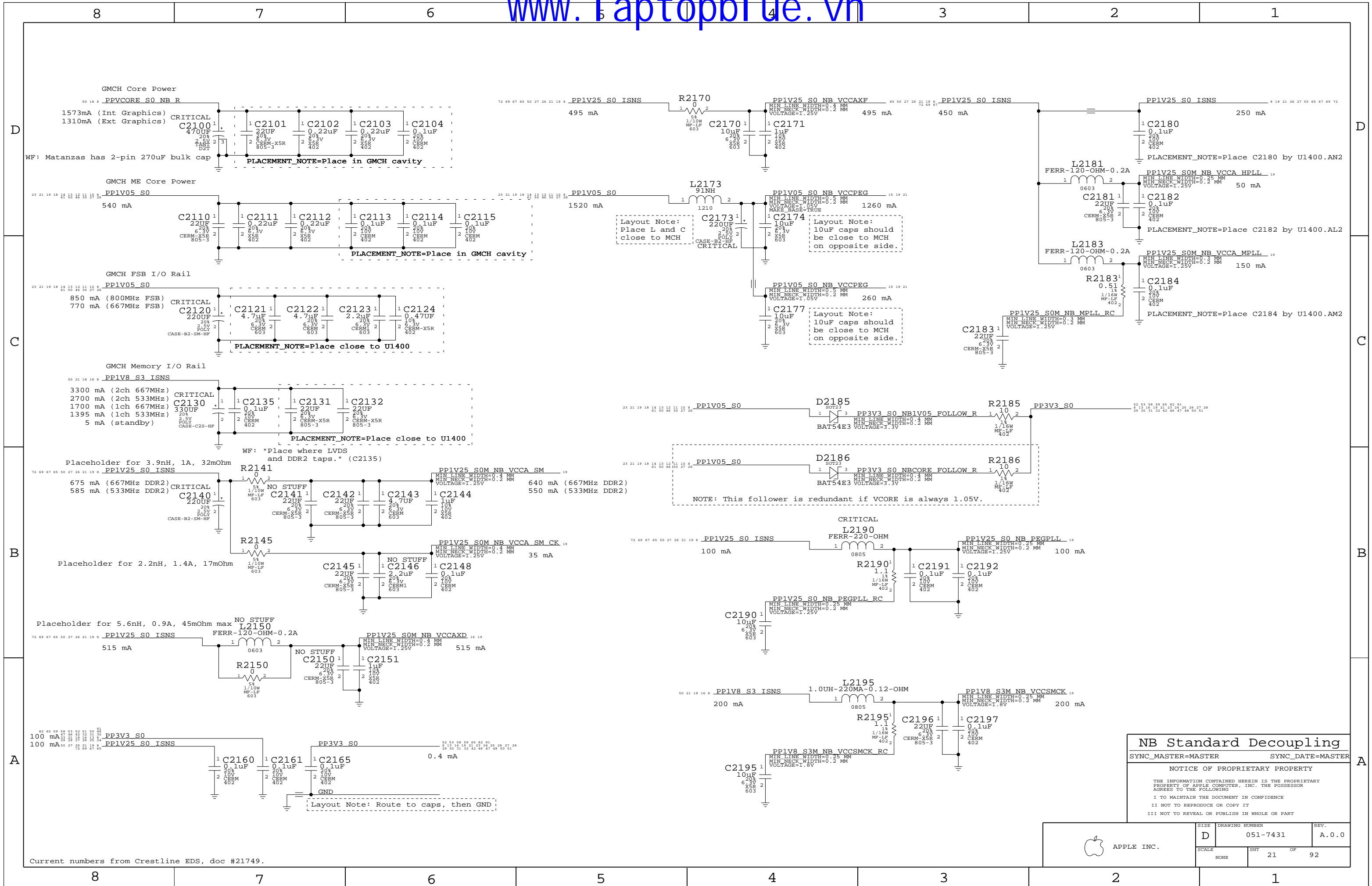
II NOT TO REPRODUCE OR COPY IT

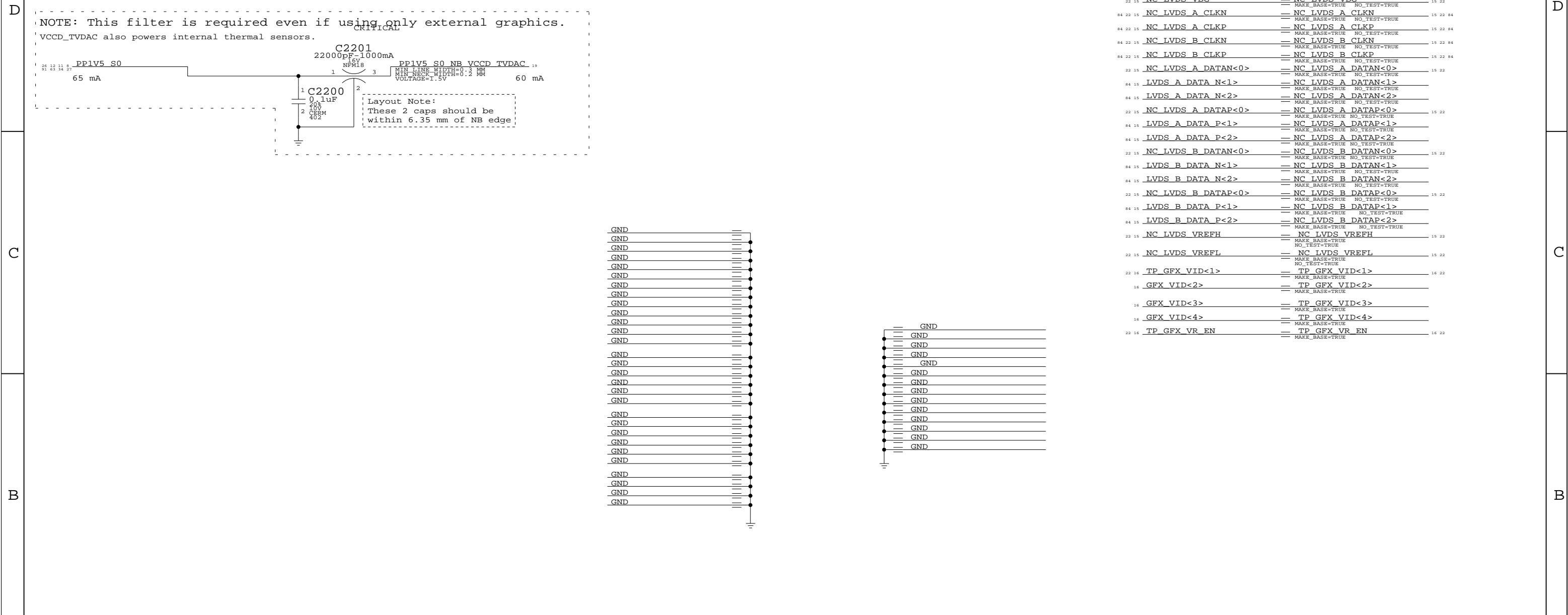
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART




APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE	SHT	OF
NONE	20	92



[illegible]

 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7431	A.0.0
	SCALE	SHT OF	
	NONE	22 92	



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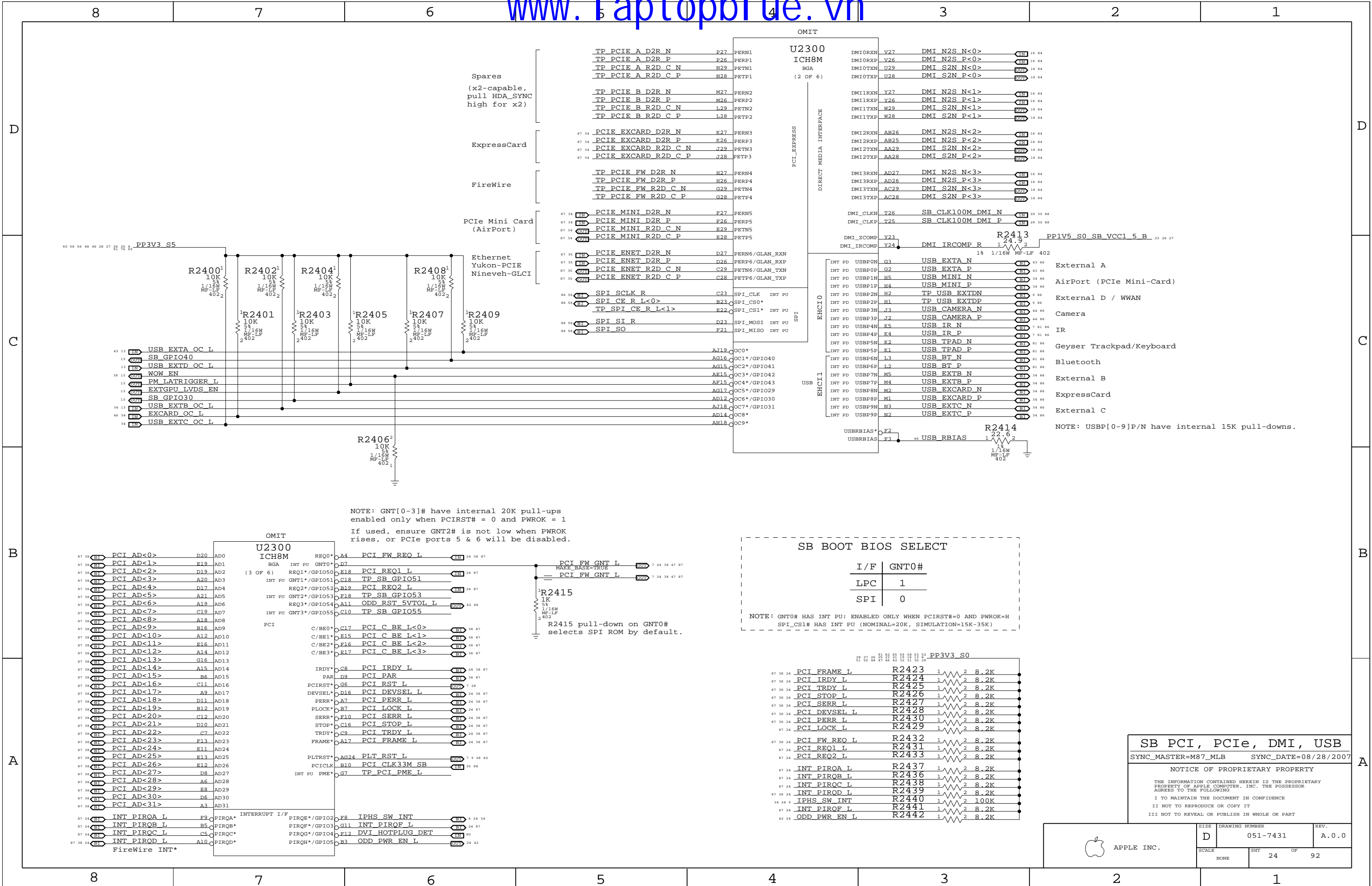
SB Enet, Disk, FSB, LPC
SYNC_MASTER=T9_NOME          SYNC_DATE=01/25/2007

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```

NOTE: GNT[0-3]# have internal 20K pull-ups enabled only when PCIRST# = 0 and PWROK = 1
If used, ensure GNT2# is not low when PWROK rises, or PCIe ports 5 & 6 will be disabled.

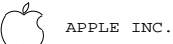
SB BOOT BIOS SELECT

I/F	GNT0#
LPC	1
SPI	0

NOTE: GNT0# HAS INT PU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
SPI_CS1# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)

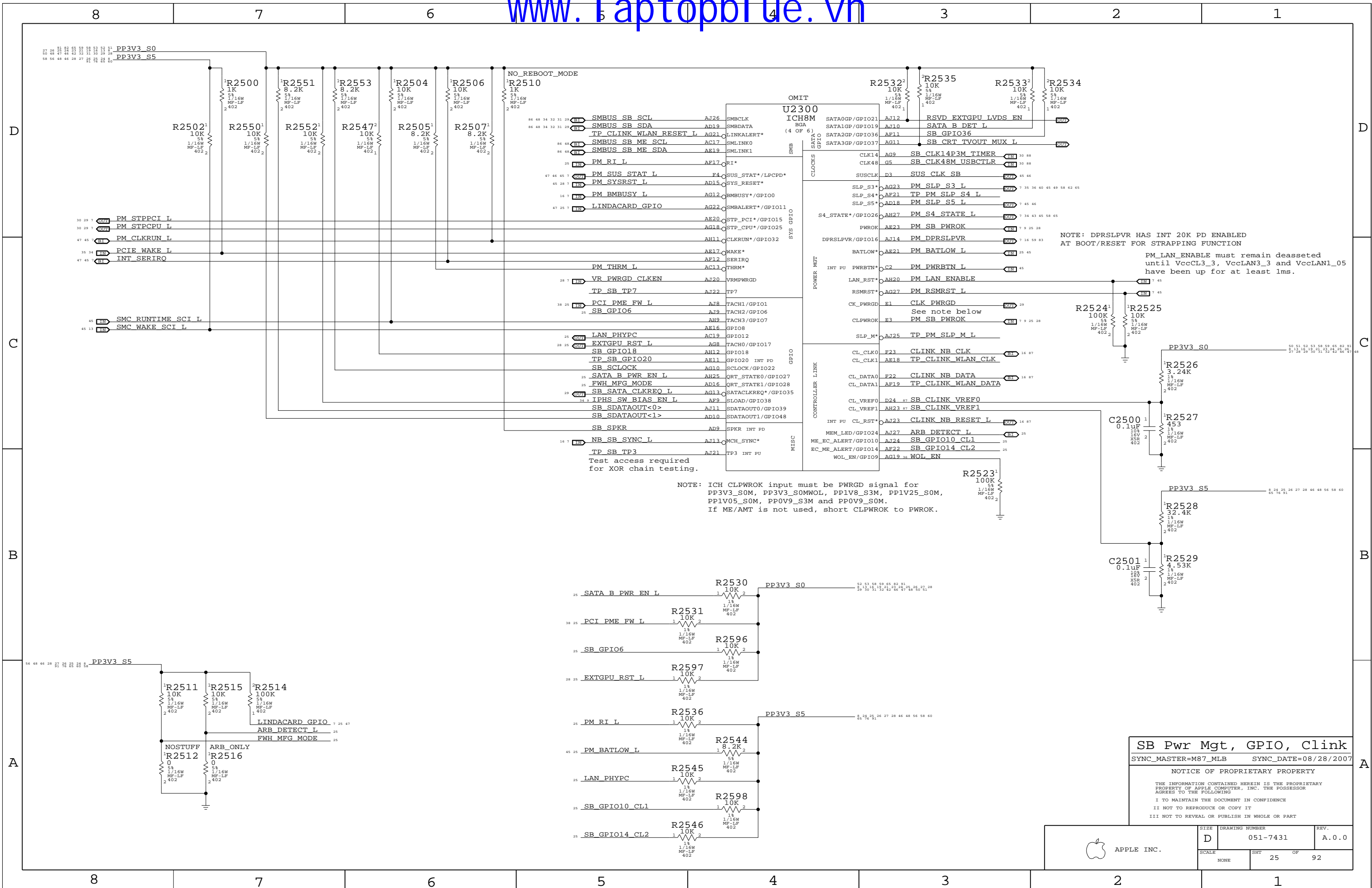
SB PCI, PCIe, DMI, USB
SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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SIZE	DRAWING NUMBER	REV.
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SCALE	SHT	OF
NONE	24	92



SB Pwr Mgt, GPIO, Clink
SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

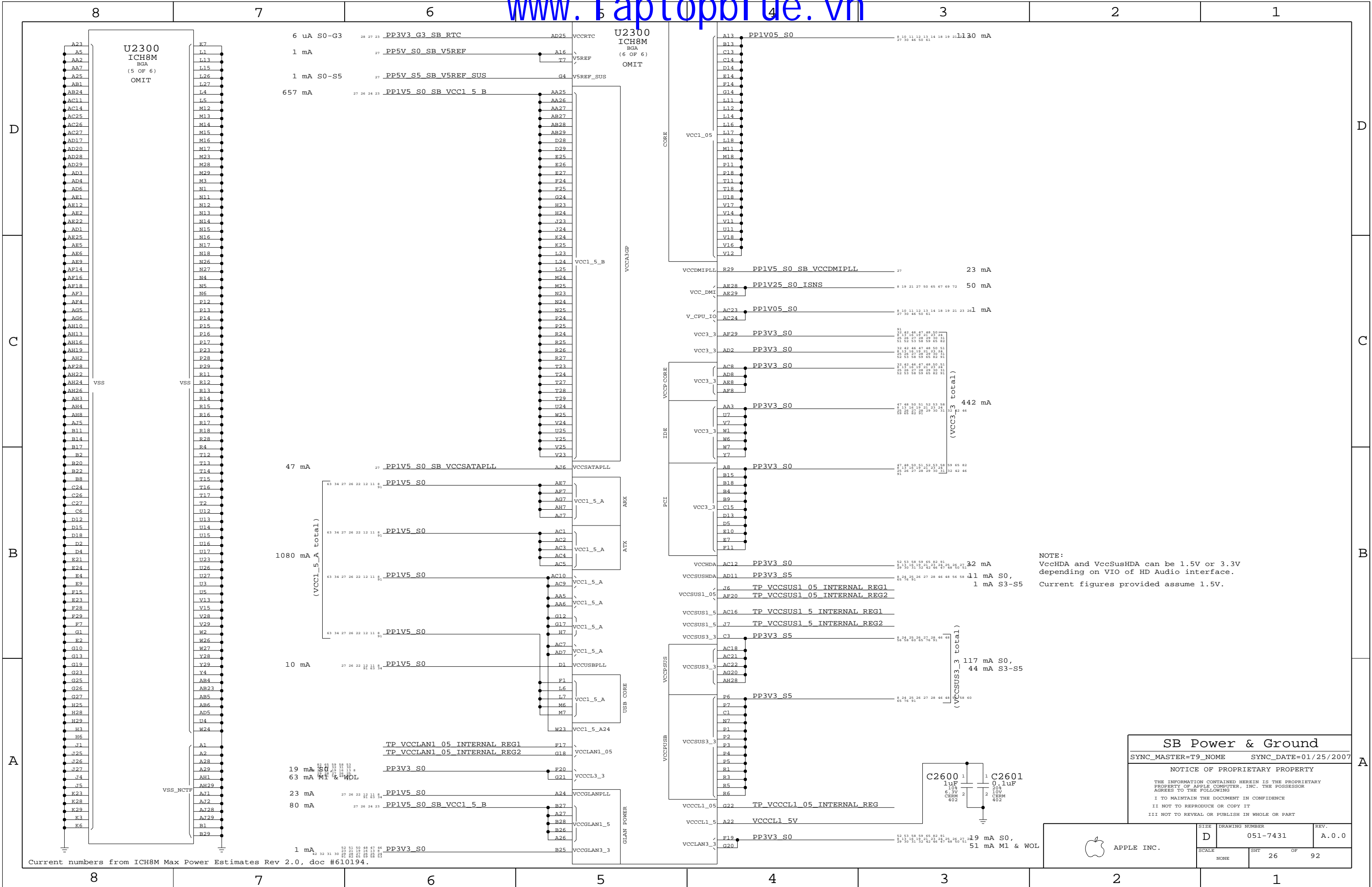
NOTICE OF PROPRIETARY PROPERTY

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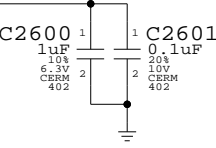
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

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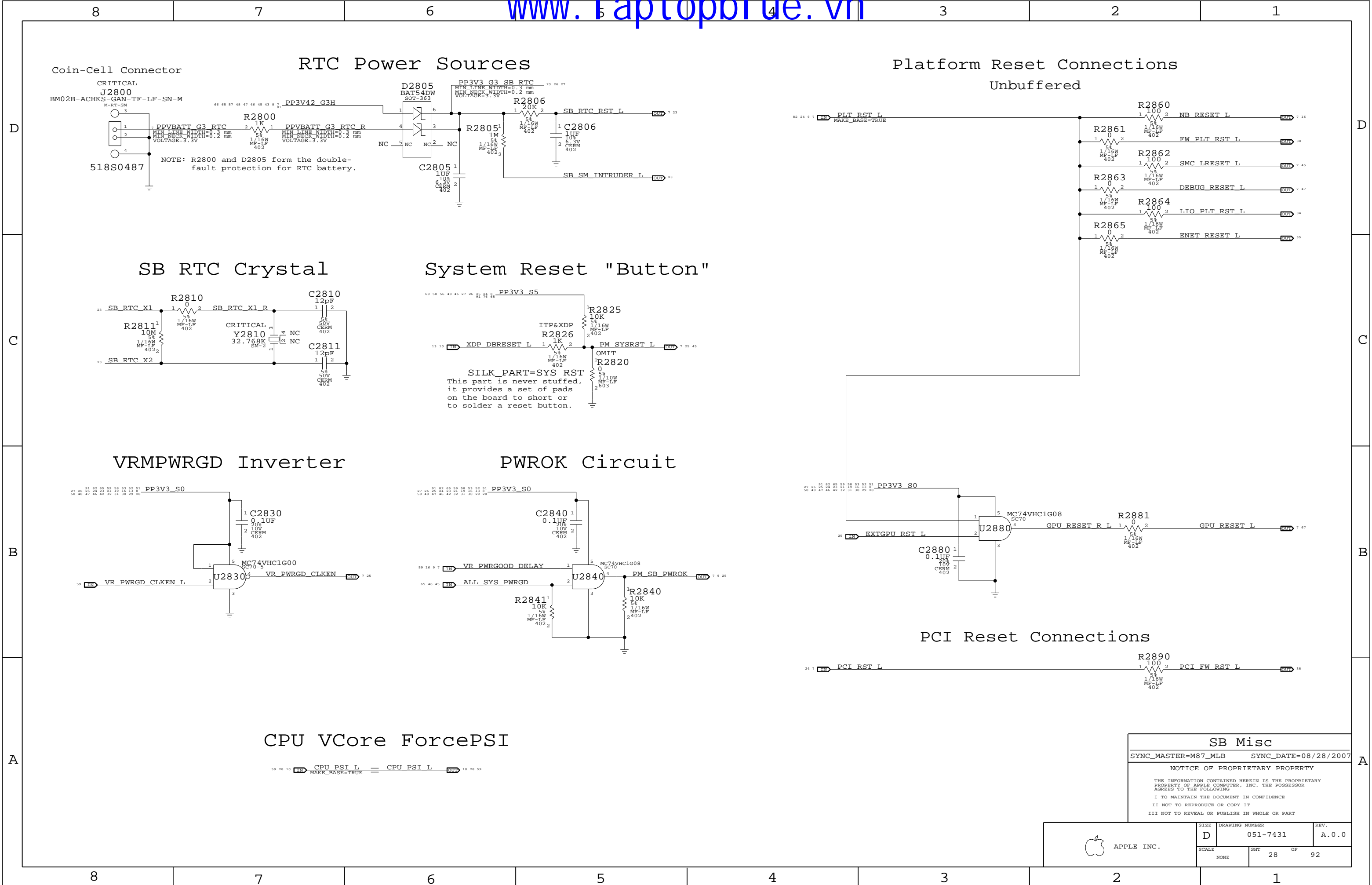


NOTE:
VccHDA and VccSusHDA can be 1.5V or 3.3V depending on VIO of HD Audio interface.
Current figures provided assume 1.5V.



SB Power & Ground		
SYNC_MASTER=T9_NOME		SYNC_DATE=01/25/2007
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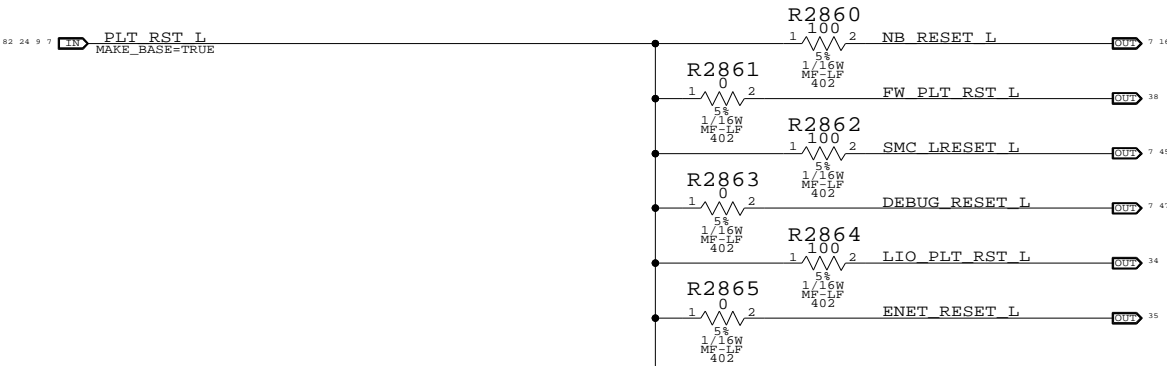
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7431	A.0.0
SCALE		SHT	OF
NONE		26	92



CPU VCore ForcePSI

59 28 10 **PS** CPU_PSI_L == CPU_PSI_L **00P** 30 28 59

Platform Reset Connections
Unbuffered



PCI Reset Connections



SB Misc		
SYNC_MASTER=M87_MLB		SYNC_DATE=08/28/2007
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 APPLE INC.	SIZE D	DRAWING NUMBER 051-7431	REV. A.0.0
	SCALE NONE	SHT 28	OF 92

D

C

B

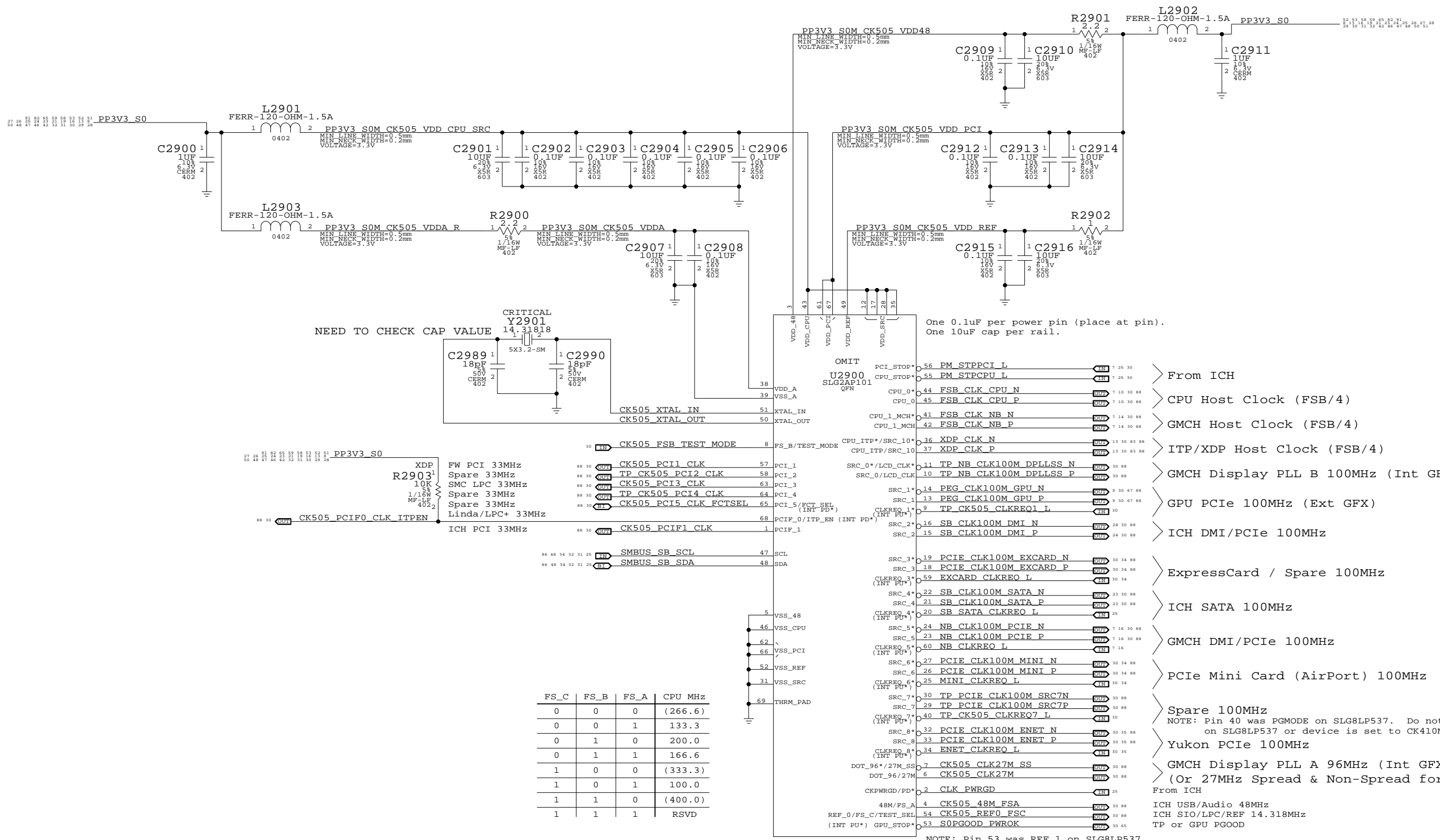
A

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A



FCT_SEL	PIN 6	PIN 7	PIN 10	PIN 11
0	DOT_96+	DOT_96-	LCD_CLK+	LCD_CLK-
1	27M	27M w/SS	SRC_0+	SRC_0-

(For Internal Graphics)
(For External Graphics)

Clock (CK505)

SYNC_MASTER=T9_NAME SYNC_DATE=01/25/2007

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APPLE INC.

SIZE D

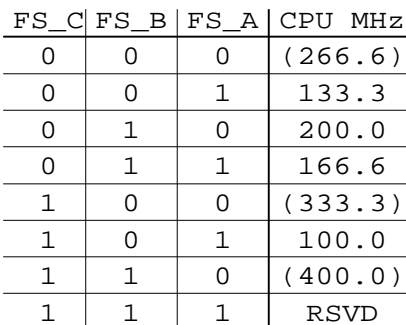
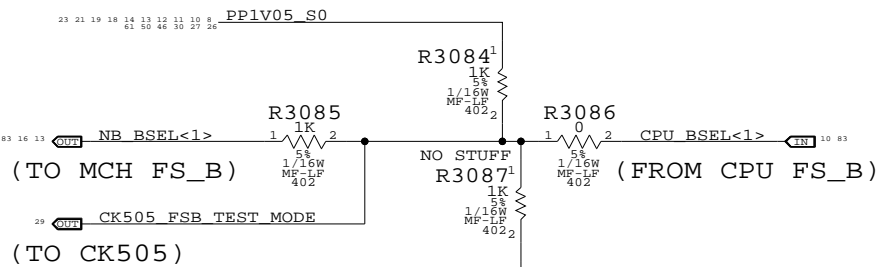
SCALE NONE

DRAWING NUMBER 051-7431

SHT 29 OF 92

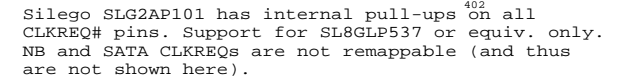
REV. A.0.0

FCT_SEL (GFX clock select)



(Only 100-200MHz supported by
SLG8LP536 and CY28545-5)

(Note: HOST/SRC/GFX clock termination removed. Silago SL8GLP536 or equiv. support only)



```
30 29 S0PGOOD_PWROK = S0PGOOD_PWROK
65 MAKE_BASE=TRUE ==
```

```

88 30 29 TP CK505_PCI2_CLK == TP CK505_PCI2_CLK 29 30 88
      (Reserved for TPM PCI 33MHZ)
88 30 29 TP CK505_PCI4_CLK == TP CK505_PCI4_CLK 29 30 88
      (Spare 33MHZ)

```

SYNC_MASTER=M87_MLB	SYNC_DATE=08/28/2007	7
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SIZE D	DRAWING NUMBER 051-7431	REV. A.0.0
SCALE NONE	SHT 30	OF 92

Page Notes

Power aliases required by this page:

- =PP1V8_S3M_MEM_A
- =PP0V9_S3M_MEM_DIMMVREFA
- =PPSPD_S0M_MEM_A (2.5V - 3.3V)

Signal aliases required by this page:

- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:

(NONE)

"Factory" (thru-hole) slot

DDR2 Bypass Caps
(For return current)

DDR2 SO-DIMM Connector A

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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APPLE INC.

SIZE

DRAWING NUMBER

REV.

D

051-7431

A.0.0

SCALE

NONE

SHT

31

OF

92

Page Notes

Power aliases required by this page:

- =PP1V8_S3M_MEM_B
- =PP0V9_S3M_MEM_DIMMVREFB
- =PPSPD_S0M_MEM_B (2.5V - 3.3V)

Signal aliases required by this page:

- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:

(NONE)

"Expansion" (surface-mount) slot

DDR2 Bypass Caps
(For return current)

DDR2 SO-DIMM Connector B

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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APPLE INC.

SIZE

DRAWING NUMBER

REV.

D

051-7431

A.0.0

SCALE

NONE

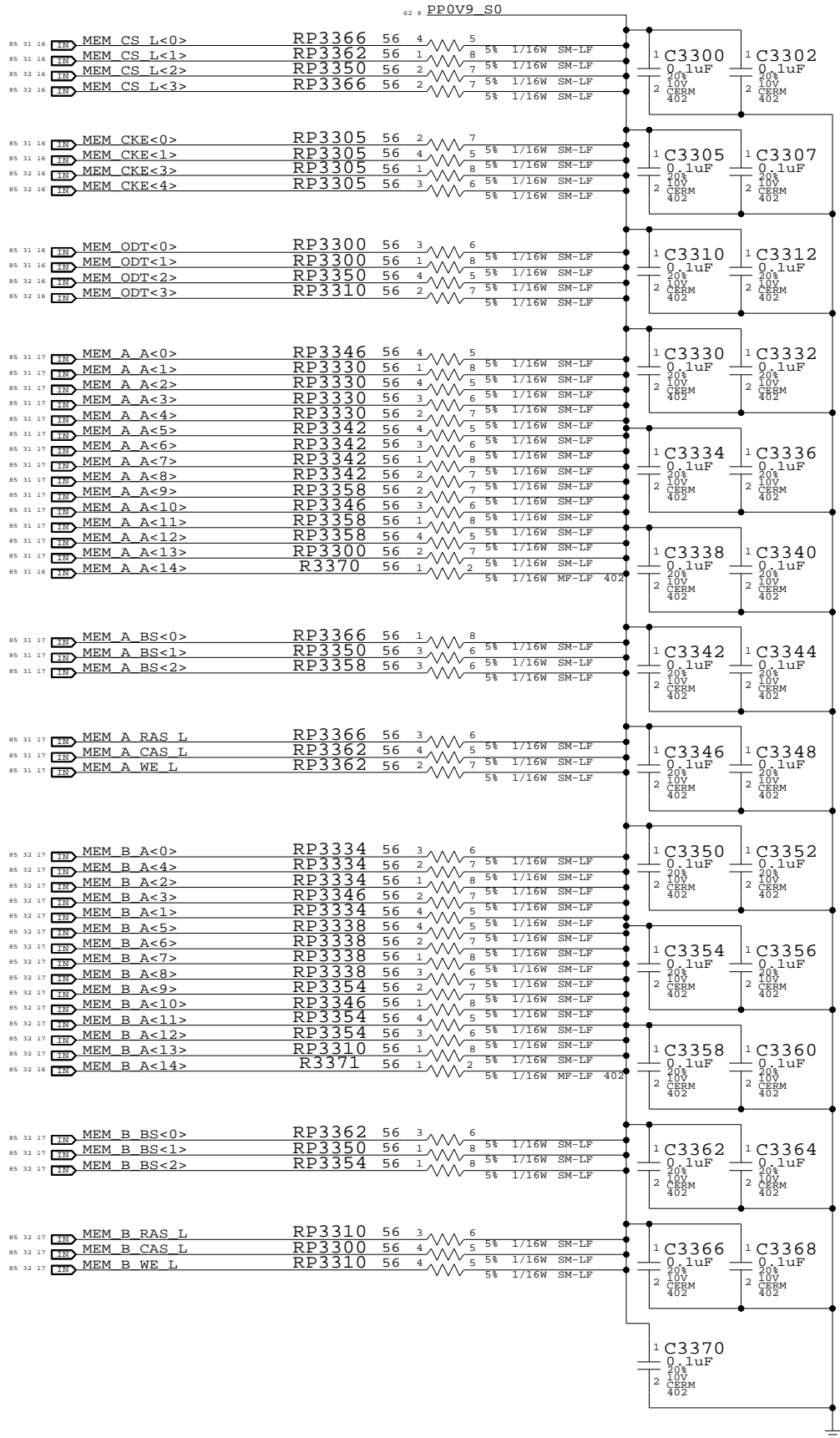
SHT

32

OF

92

One cap for each side of every RPAK, one cap for every two discrete resistors
Ensure CS_L and ODT resistors are close to SO-DIMM connector



Memory Active Termination

SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)

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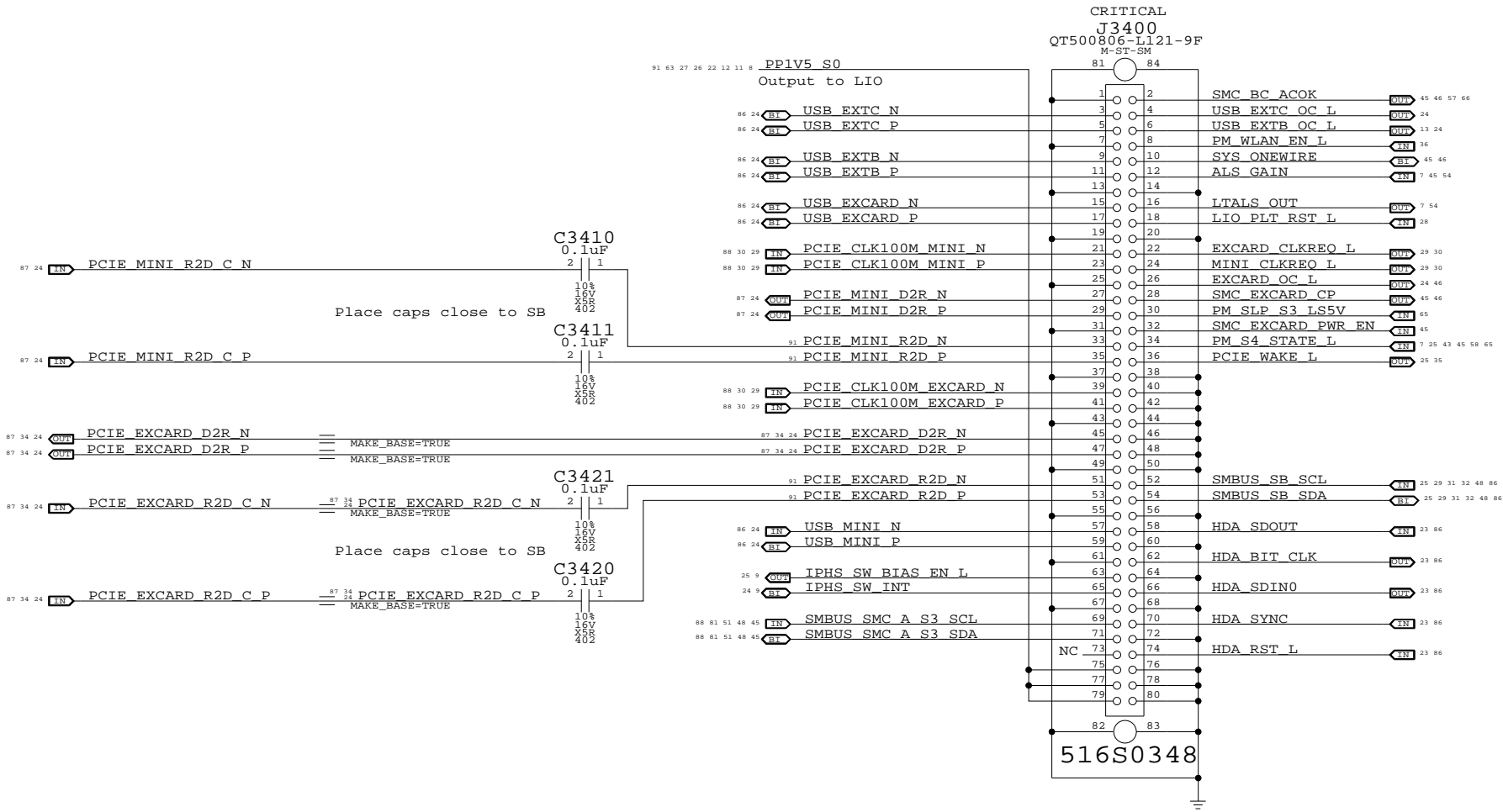
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SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE	SHT	OF
NONE	33	92

Left I/O Board Connector



Left I/O Board Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE

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DRAWING NUMBER

051-7431

REV.

A.0.0

SCALE

NONE

SHT

34

OF

92

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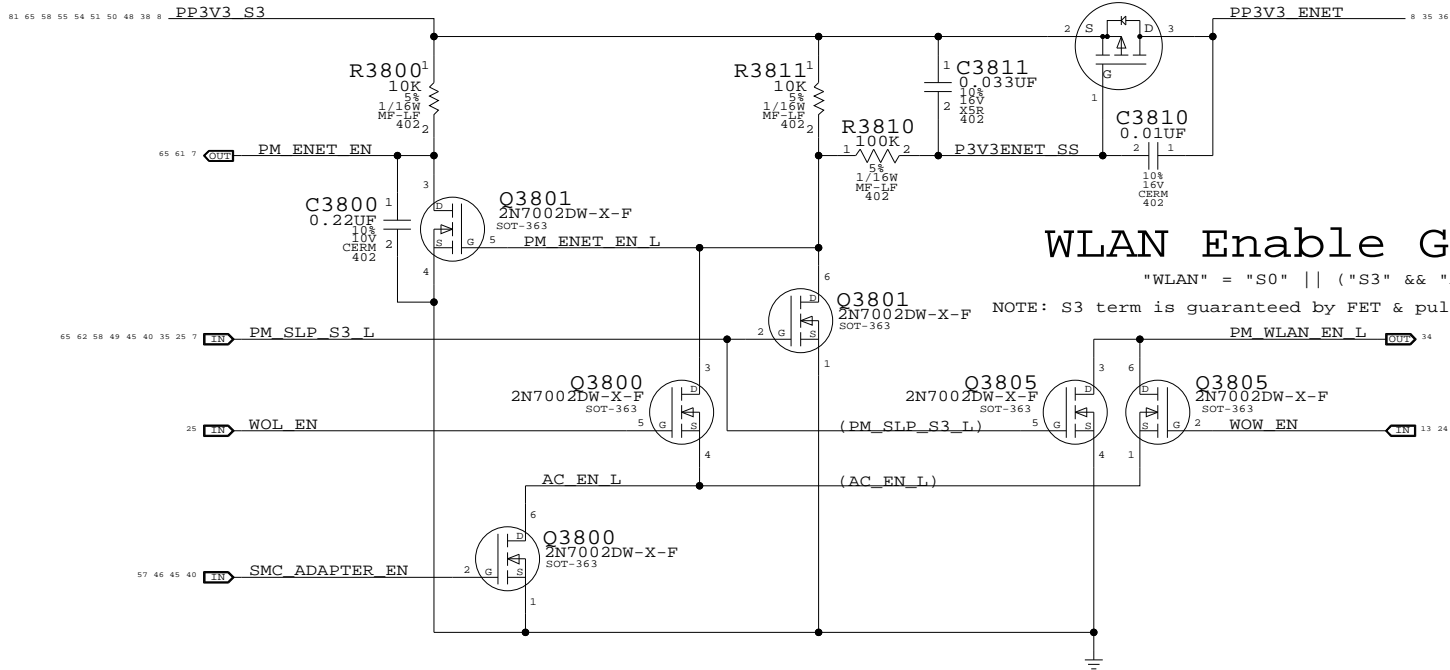
B

A

8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---

ENET Enable Generation

"ENET" = "S0" || ("S3" && "AC" && "WOL_EN")
NOTE: S3 term is guaranteed by source of R3800 & Q3810, MUST BE S3 RAIL.

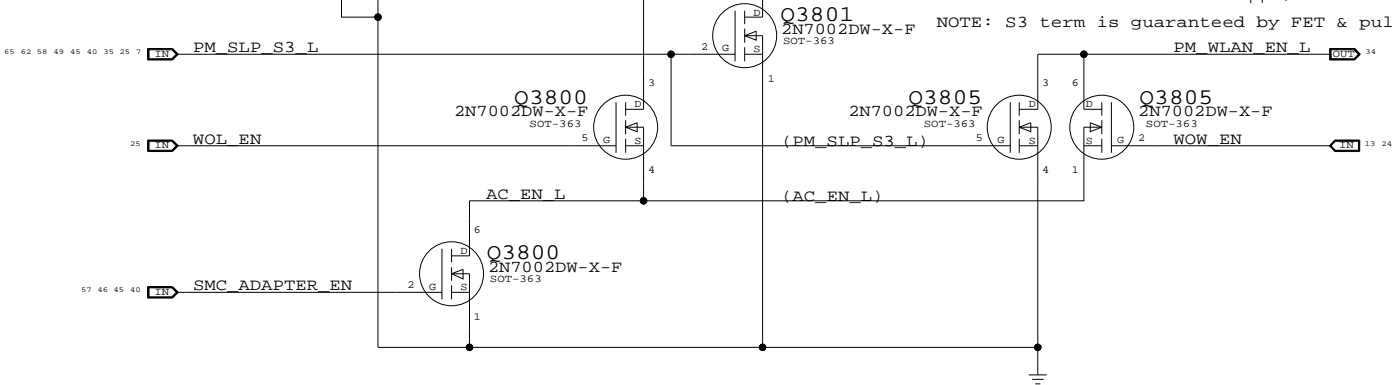


3.3V ENET FET

CRITICAL
Q3810
NTR4101P
SOT-23

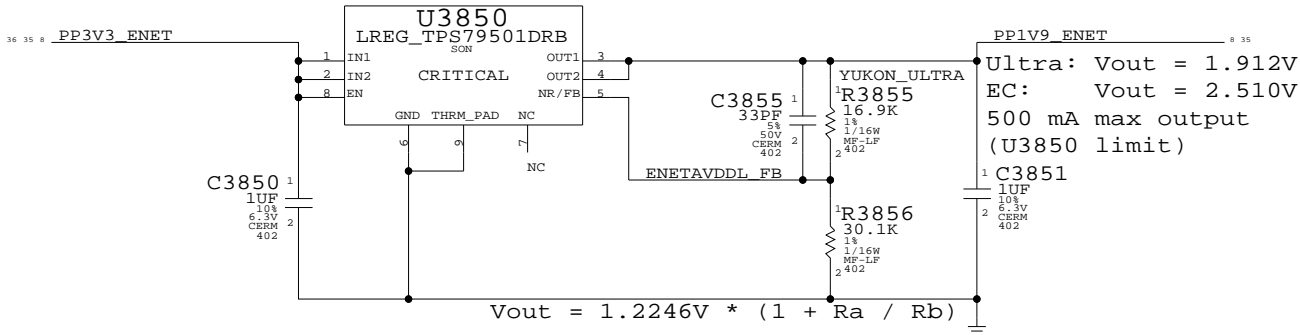
WLAN Enable Generation

"WLAN" = "S0" || ("S3" && "AC" && "WOW_EN")
NOTE: S3 term is guaranteed by FET & pull-up source, MUST BE S3 RAIL.



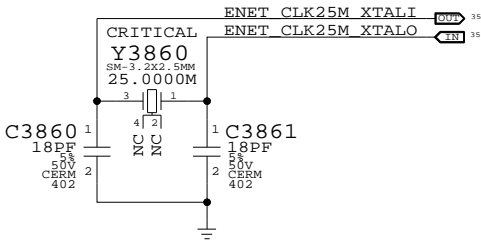
Yukon AVDDL LDO

1.9V for Yukon Ultra, 2.5V for Yukon EC
Yukon Ultra requires 1.9V on its magnetics to pass compliance tests



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0363	1	RES,31.6K,1%,1/16W,402,LF	R3855		YUKON_EC

Yukon Crystal



Yukon Power Control

SYNC_MASTER=T9_NOME SYNC_DATE=03/19/2007

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SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE	SHT	OF
NONE	36	92

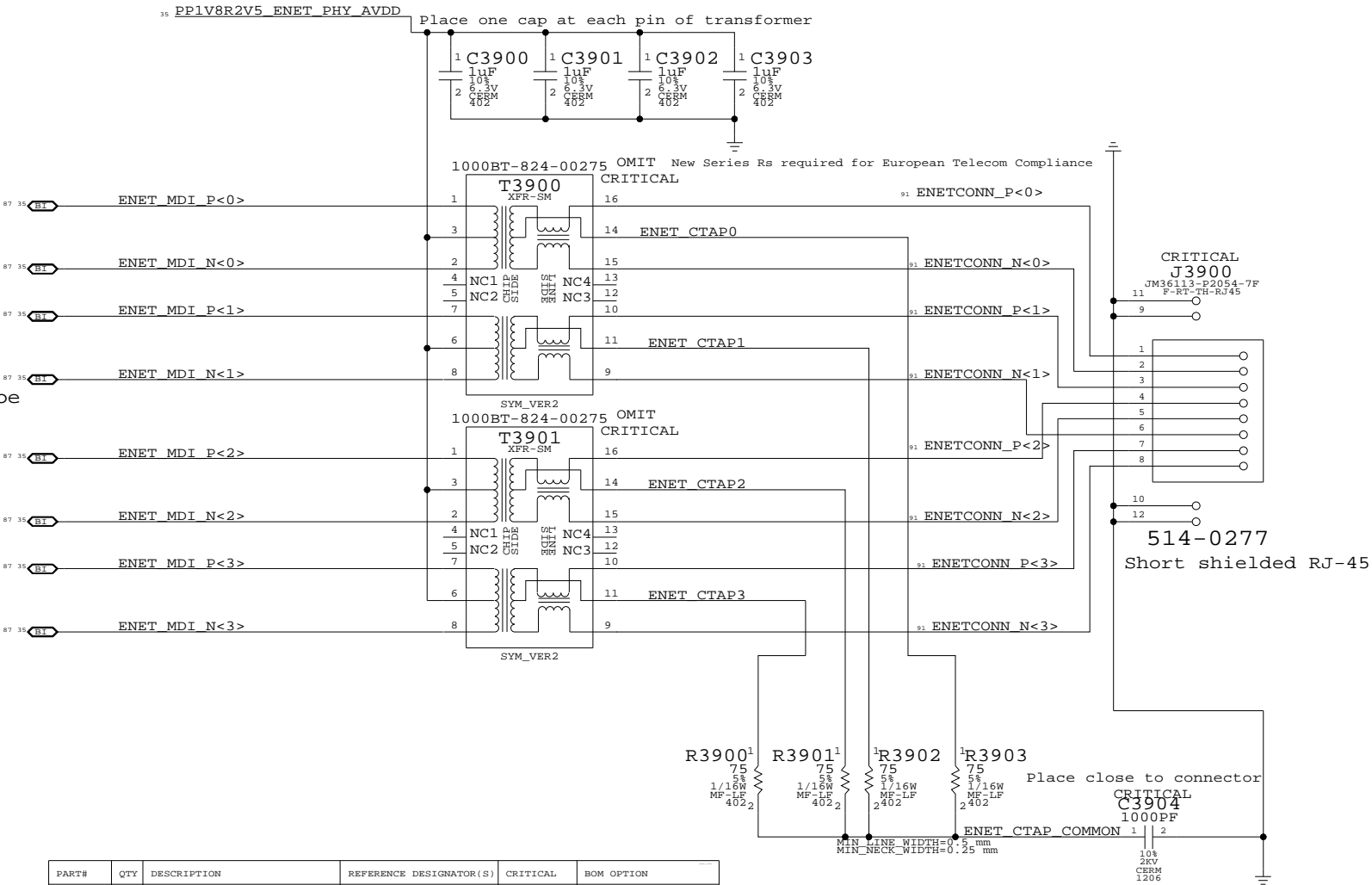
Page Notes

Power aliases required by this page:
- =GND_CHASSIS_ENET

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Transformers should be mirrored on opposite sides of the board



Ethernet Connector

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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SIZE

D

DRAWING NUMBER

051-7431

REV.

A.0.0

SCALE

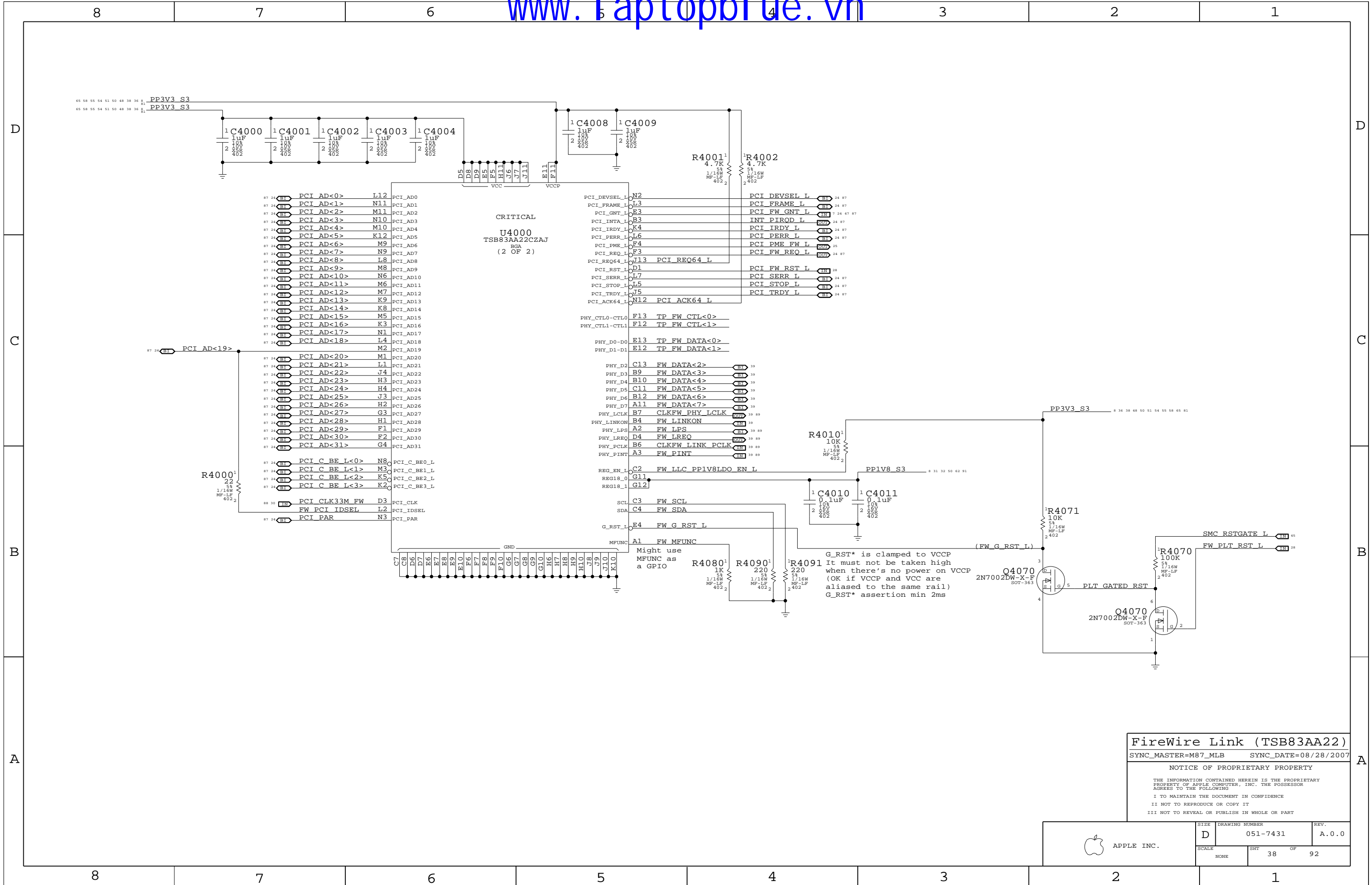
NONE

SHT

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OF

92



FireWire Link (TSB83AA22)

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE	SHT	OF
NONE	38	92

8

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1

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D

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C

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B

A

A

DSx Straps: PP3V3_FW
Hi: Data-Strobe only (1394a).
Lo: Beta Mode enable (1394b).
Strap via alias on port page.

Power Class:

Single-port / Desktop systems are Power Class 0 ('000').
Multi-port Portable systems are Power Class 4 ('100').
Implement 1K pull-up or pull-down on port page.

C4150 with internal
pull-up provides
PHY power-up reset.

No need for DS2 pull-down on TSB83AA22A,
as 3rd FireWire port is not pinned out.

R4160 provides isolation between R4161 and unpowered LLC.

FireWire PHY (TSB83AA22)

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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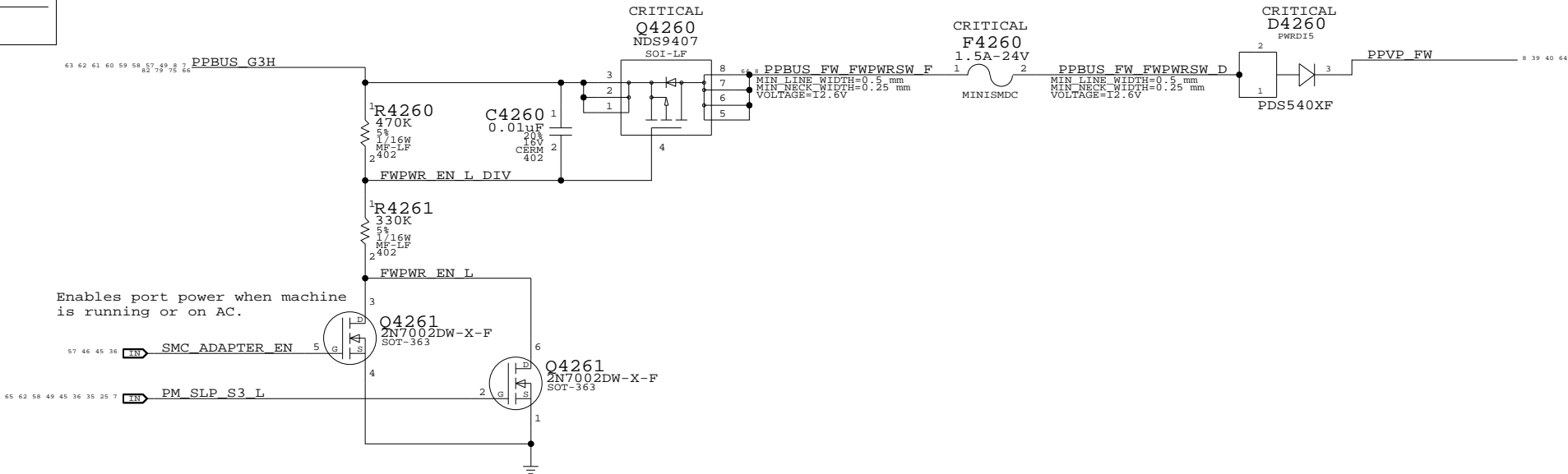
SIZE D DRAWING NUMBER 051-7431 REV. A.0.0

SCALE NONE SHT 39 OF 92

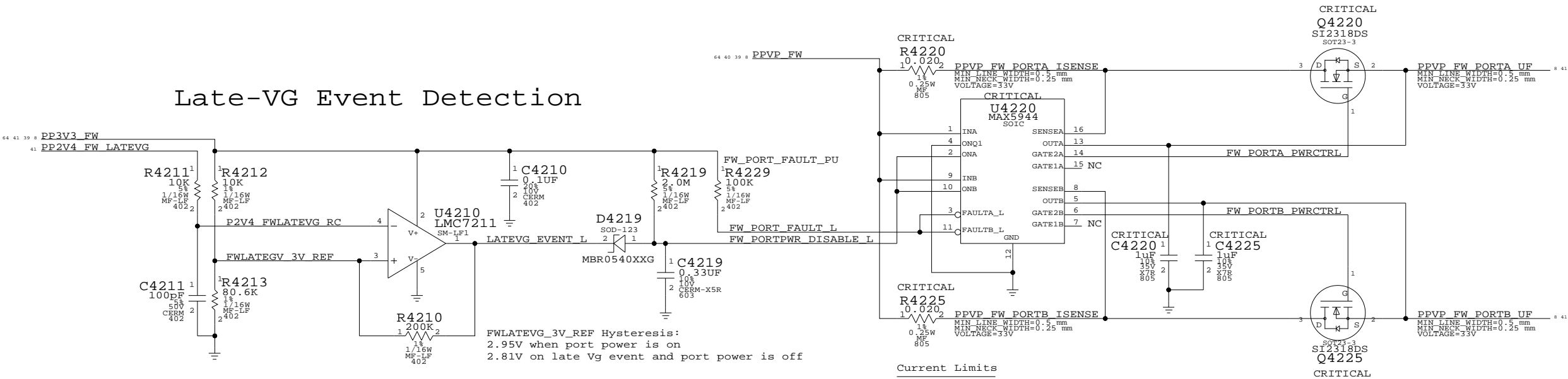
Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
- FW_PORT_FAULT_PU

FireWire Port Power Switch



Current Limit/Active Late-VG Protection



Current Limits
0.020 ohm => 2.4A
0.025 ohm => 2A
0.030 ohm => 1.66A (Ideal)
0.033 ohm => 1.5A

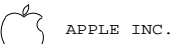
MAX5944 current limiter trips if integrator (counter) reaches 16. A new sample (taken every 125 us) is weighted as +1 if over the limit (at any point during the period) and -1/128 if under the limit. As a result, the device tends to trip easily on devices that produce periodic current spikes. Current limit has been set higher to compensate.

FireWire Port Power

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE	SHT	OF
NONE	40	92

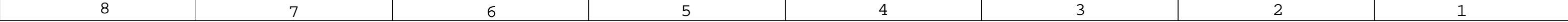
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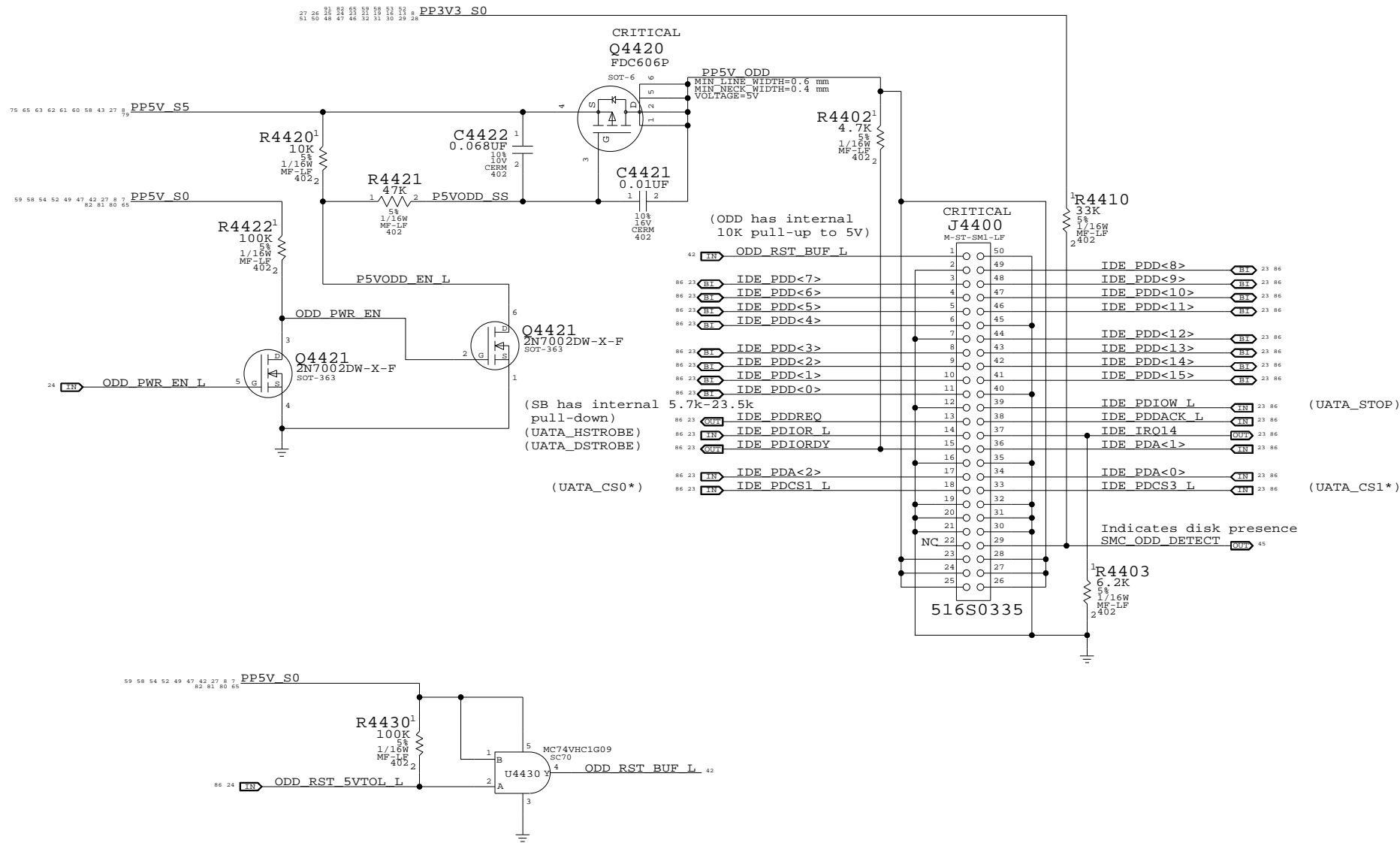
B

A

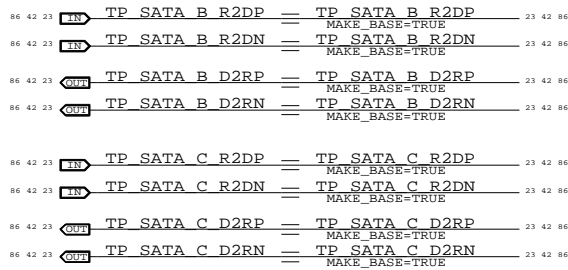
Late-VG Protection Power



IDE (ODD) Connector



Unused SATA Ports



Placement note
Place within 12.7mm
from ball of SB

PATA Connector

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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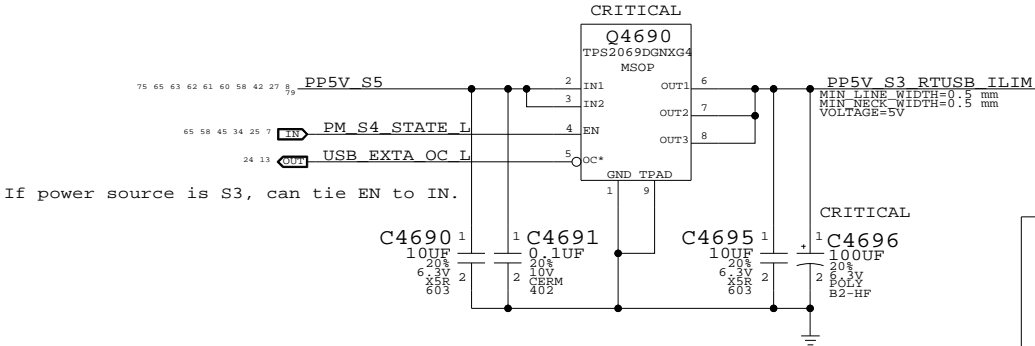
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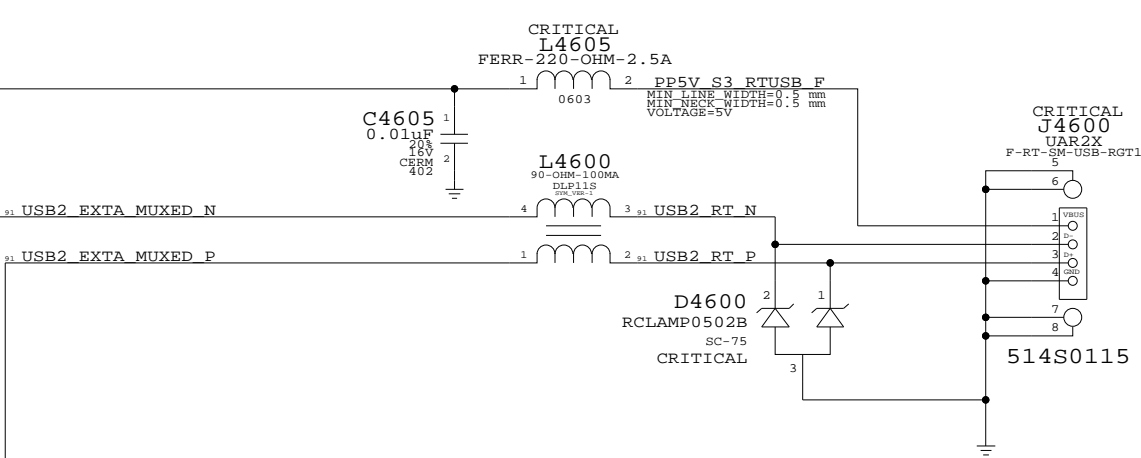
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE	SHT	OF
NONE	42	92

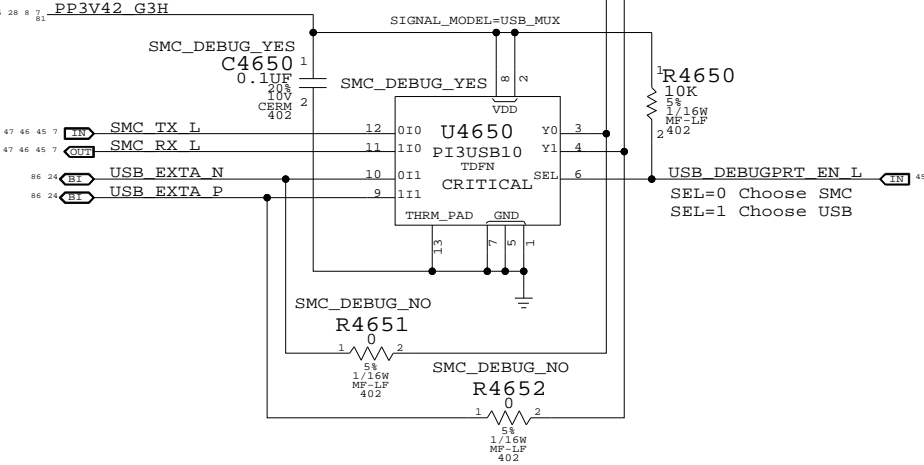
Port Power Switch



Right USB Port



USB/SMC Debug Mux



External USB Connector

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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DRAWING NUMBER

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A.0.0

SCALE

NONE

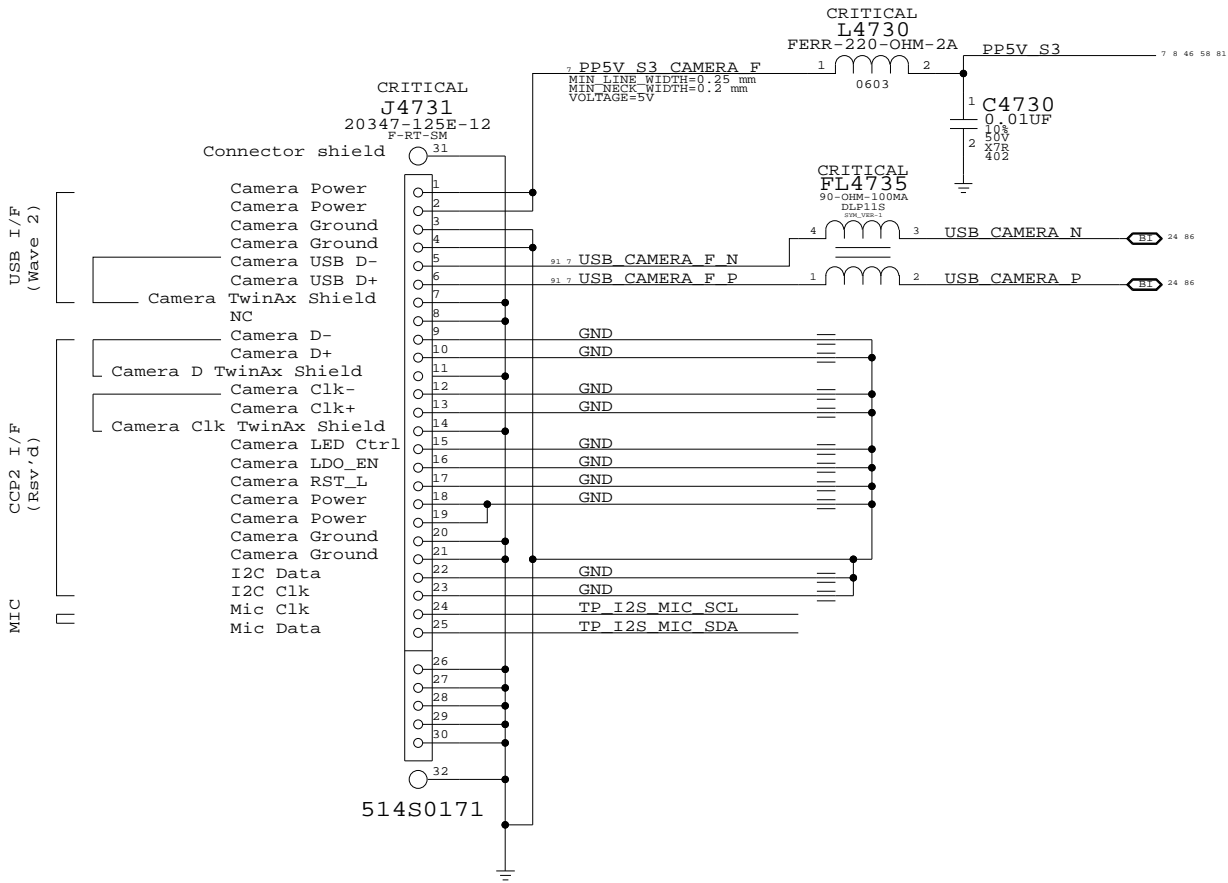
SHT

43

OF

92

Left Clutch Barrel Interconnect



Left Clutch Barrel Interconnect

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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SCALE	SHT	OF
NONE	44	92

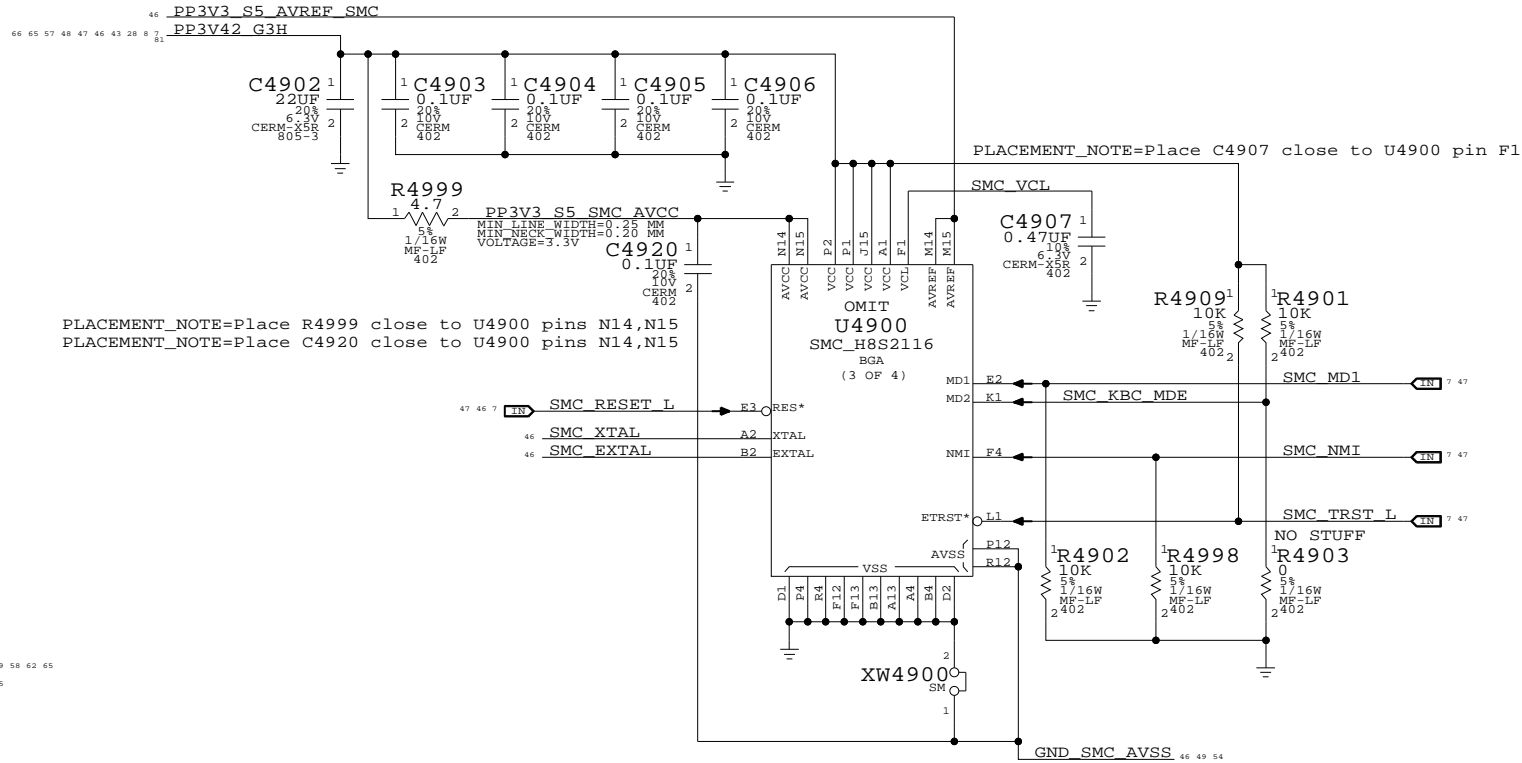
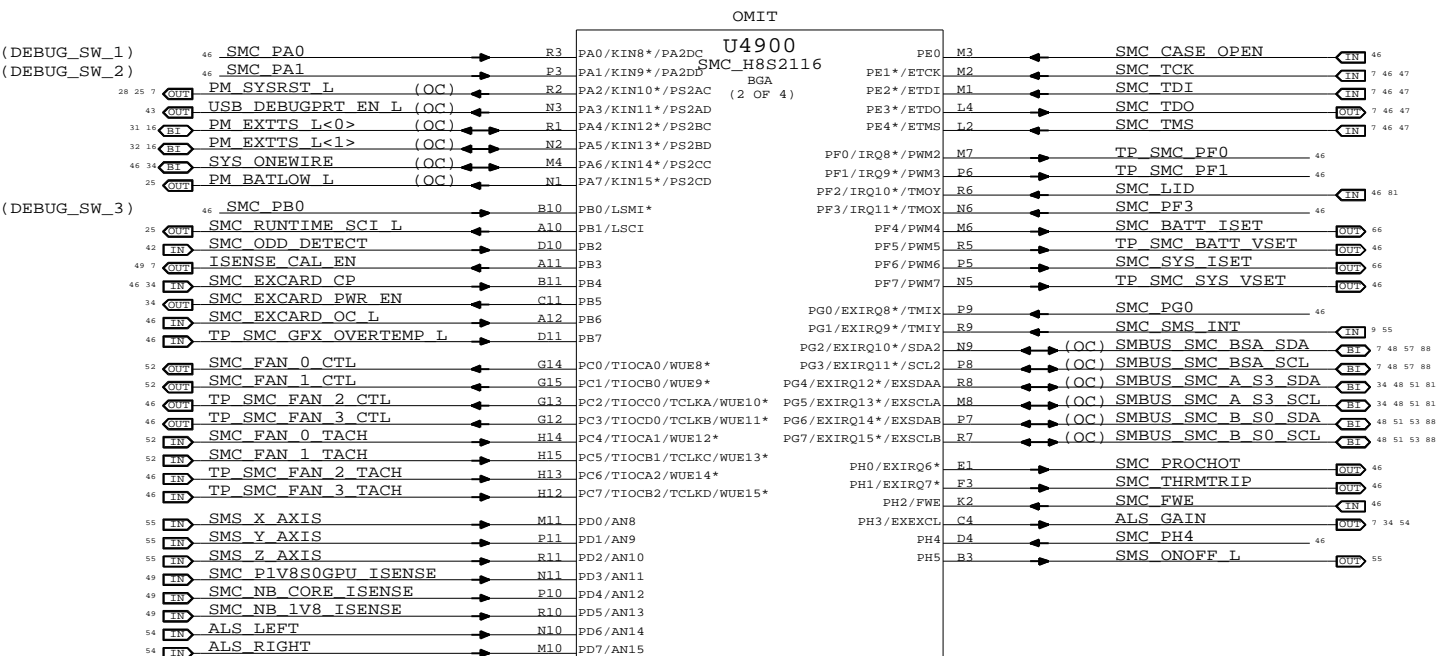
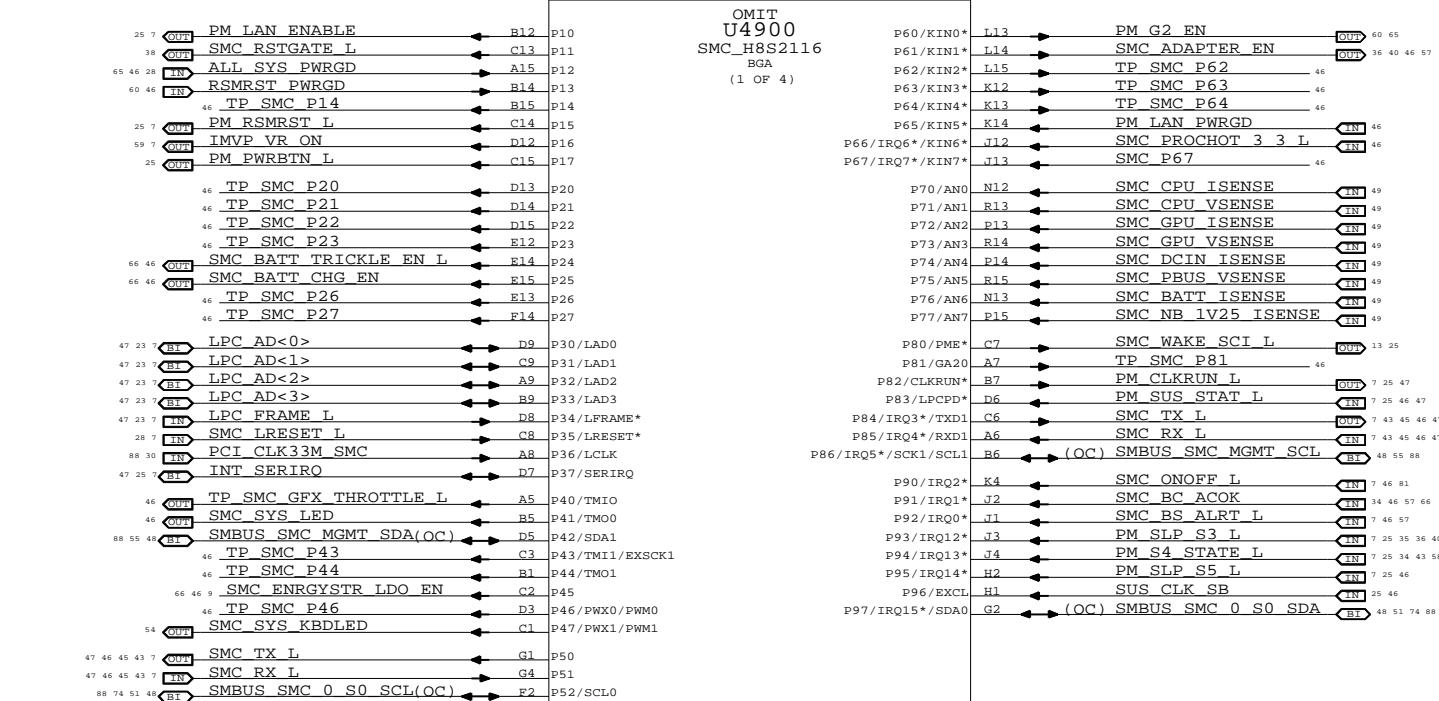
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

D

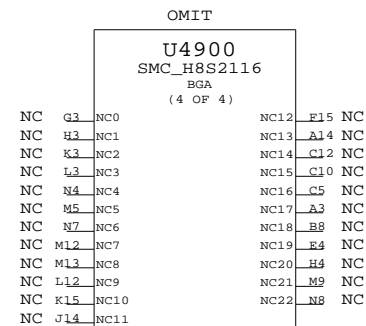
C

B

A



NOTE: SMS Interrupt can be active high or low, rename net accordingly. If SMS interrupt is not used, pull up to SMC rail.



SMC

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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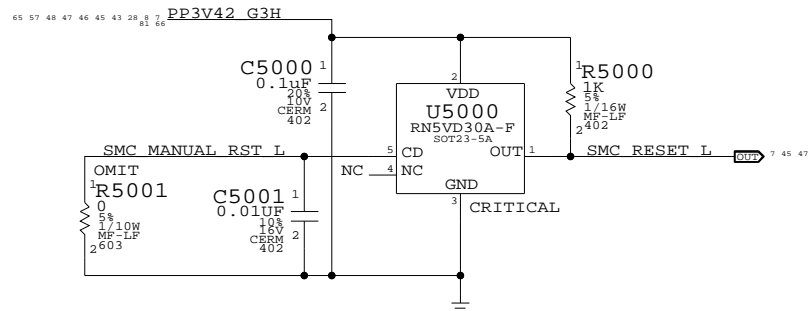
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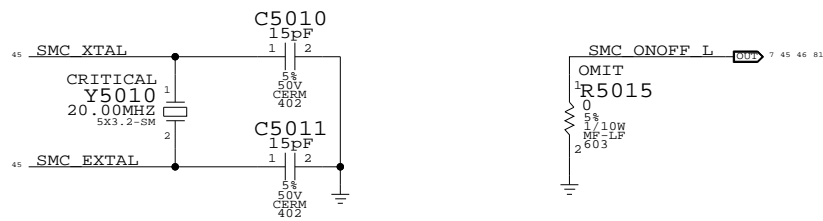
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE	SHT	OF
NONE	45	92

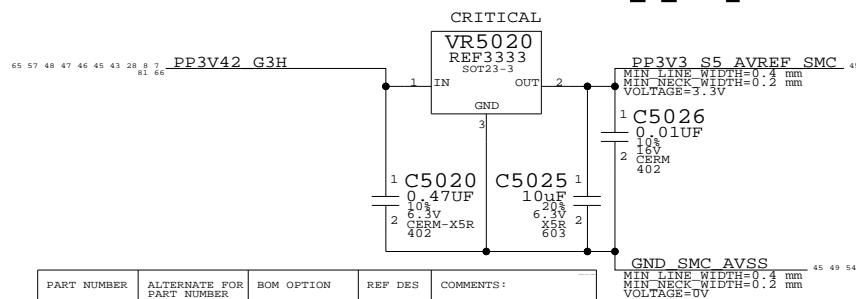
SMC Reset "Button" / Brownout Detect



SMC Crystal Circuit Debug Power "Button"

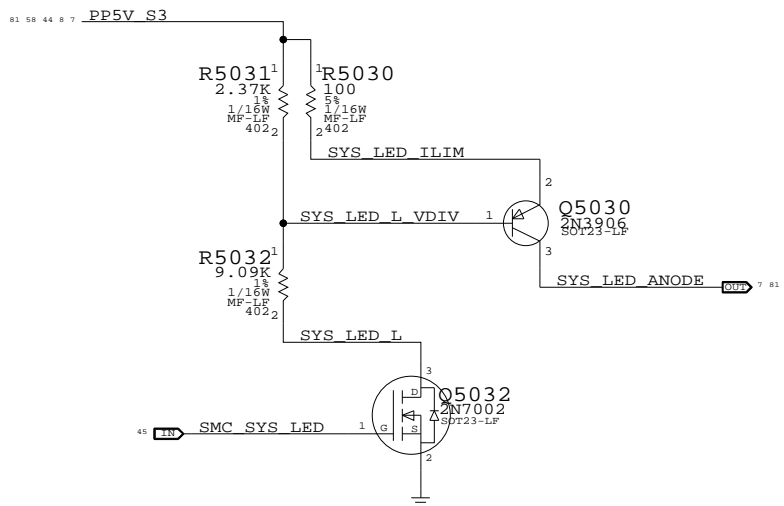


SMC AVREF Supply

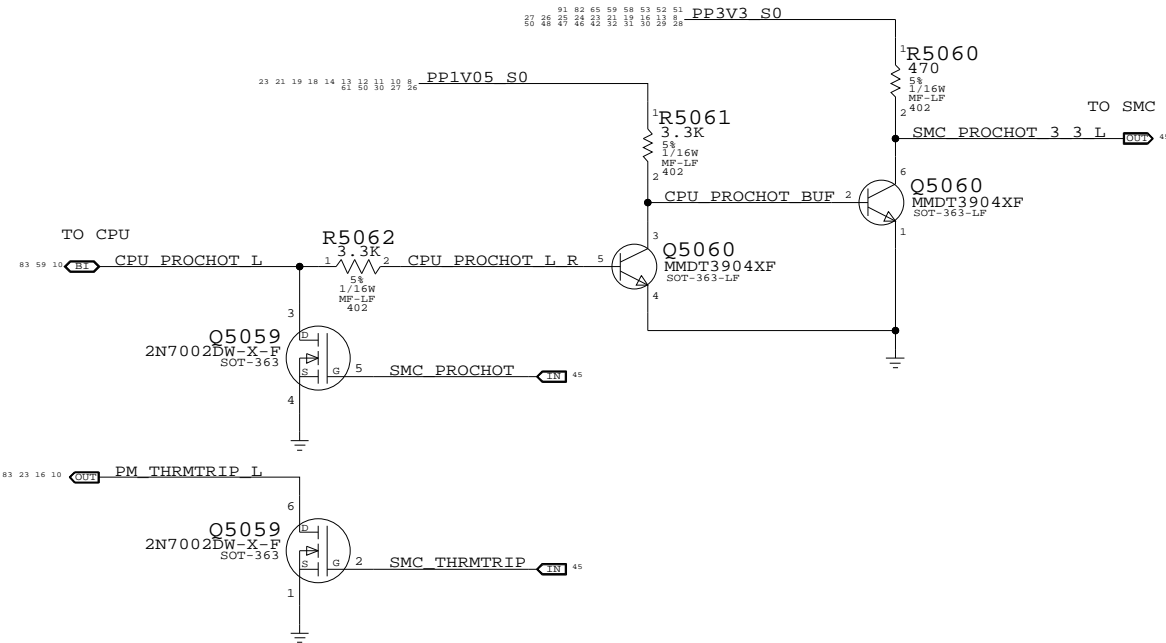


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
35381381	35381278		ALL	Interail ISL60002-33

System (Sleep) LED Circuit



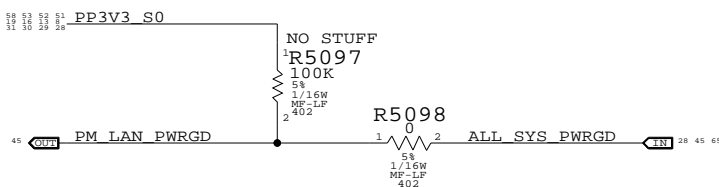
SMC FSB to 3.3V Level Shifting



TP SMC FAN 2 CTL	=	TP SMC FAN 2 CTL	45 46
TP SMC FAN 2 TACH	=	TP SMC FAN 2 TACH	45 46
TP SMC FAN 3 CTL	=	TP SMC FAN 3 CTL	45 46
TP SMC FAN 3 TACH	=	TP SMC FAN 3 TACH	45 46
TP SMC GFX OVERTEMP L	=	TP SMC GFX OVERTEMP L	45 46
TP SMC GFX THROTTLE L	=	TP SMC GFX THROTTLE L	45 46
TP SMC BATT VSET	=	TP SMC BATT VSET	45 46
TP SMC SYS VSET	=	TP SMC SYS VSET	45 46
TP SMC P14	=	TP SMC P14	45 46
TP SMC P20	=	TP SMC P20	45 46
TP SMC P21	=	TP SMC P21	45 46
TP SMC P22	=	TP SMC P22	45 46
TP SMC P23	=	TP SMC P23	45 46
TP SMC P26	=	TP SMC P26	45 46
TP SMC P27	=	TP SMC P27	45 46
TP SMC P43	=	TP SMC P43	45 46
TP SMC P44	=	TP SMC P44	45 46
TP SMC P46	=	TP SMC P46	45 46
TP SMC P62	=	TP SMC P62	45 46
TP SMC P63	=	TP SMC P63	45 46
TP SMC P64	=	TP SMC P64	45 46
TP SMC P81	=	TP SMC P81	45 46
TP SMC PF0	=	TP SMC PF0	45 46
TP SMC PF1	=	TP SMC PF1	45 46

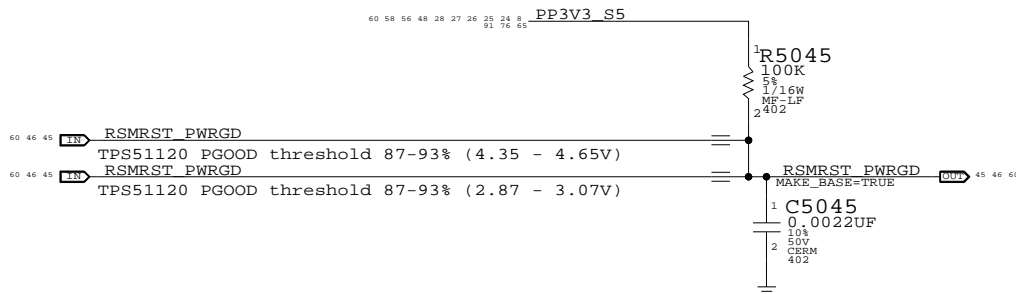
SMC EXCARD_OC_L	=	EXCARD_OC_L	24 34
SUS_CLK_SB	=	SUS_CLK_SB	25 45 46
SMC_ENRGYSTRLDO_EN	=	SMC_ENRGYSTRLDO_EN	45 46 46

LAN PWRGD Circuit



S5 Rail PWRGD Circuit

Reports when 5V S5 and 3.3V S5 are in regulation



SMC_PA0	R5091	100K	1	2	5%	1/16W	MF-LF	402
SMC_PA1	R5092	100K	1	2	5%	1/16W	MF-LF	402
SMC_PB0	R5093	100K	1	2	5%	1/16W	MF-LF	402
SMC_ONOFF_L	R5070	10K	1	2	5%	1/16W	MF-LF	402
SMC_LID	R5071	100K	1	2	5%	1/16W	MF-LF	402
SMC_FWE	R5072	10K	1	2	5%	1/16W	MF-LF	402
SMC_TX_L	R5073	10K	1	2	5%	1/16W	MF-LF	402
SMC_RX_L	R5074	100K	1	2	5%	1/16W	MF-LF	402
SYS_ONEWIRE	R5075	2.0K	1	2	5%	1/16W	MF-LF	402
SMC_BS_ALRT_L	R5076	100K	1	2	5%	1/16W	MF-LF	402
SMC_TMS	R5077	10K	1	2	5%	1/16W	MF-LF	402
SMC_TDO	R5078	10K	1	2	5%	1/16W	MF-LF	402
SMC_TDI	R5079	10K	1	2	5%	1/16W	MF-LF	402
SMC_TCK	R5080	10K	1	2	5%	1/16W	MF-LF	402
SMC_P67	R5094	10K	1	2	5%	1/16W	MF-LF	402
SMC_PF3	R5081	10K	1	2	5%	1/16W	MF-LF	402
SMC_PG0	R5096	10K	1	2	5%	1/16W	MF-LF	402
SMC_PH4	R5082	10K	1	2	5%	1/16W	MF-LF	402
SMC_BATT_TRICKLE_EN_L	R5083	10K	1	2	5%	1/16W	MF-LF	402
SMC_BATT_CHG_EN	R5084	10K	1	2	5%	1/16W	MF-LF	402
SMC_ADAPTER_EN	R5085	10K	1	2	5%	1/16W	MF-LF	402
SMC_CASE_OPEN	R5086	10K	1	2	5%	1/16W	MF-LF	402
SMC_BC_ACOK	R5087	470K	1	2	5%	1/16W	MF-LF	402
SMC_EXCARD_CP	R5088	10K	1	2	5%	1/16W	MF-LF	402
PM_SUS_STAT_L	R5089	100K	1	2	5%	1/16W	MF-LF	402
PM_SLP_S5_L	R5090	100K	1	2	5%	1/16W	MF-LF	402

SMC Support

SYNC_MASTER=M87_MLB SYNC_DATE=10/15/2007

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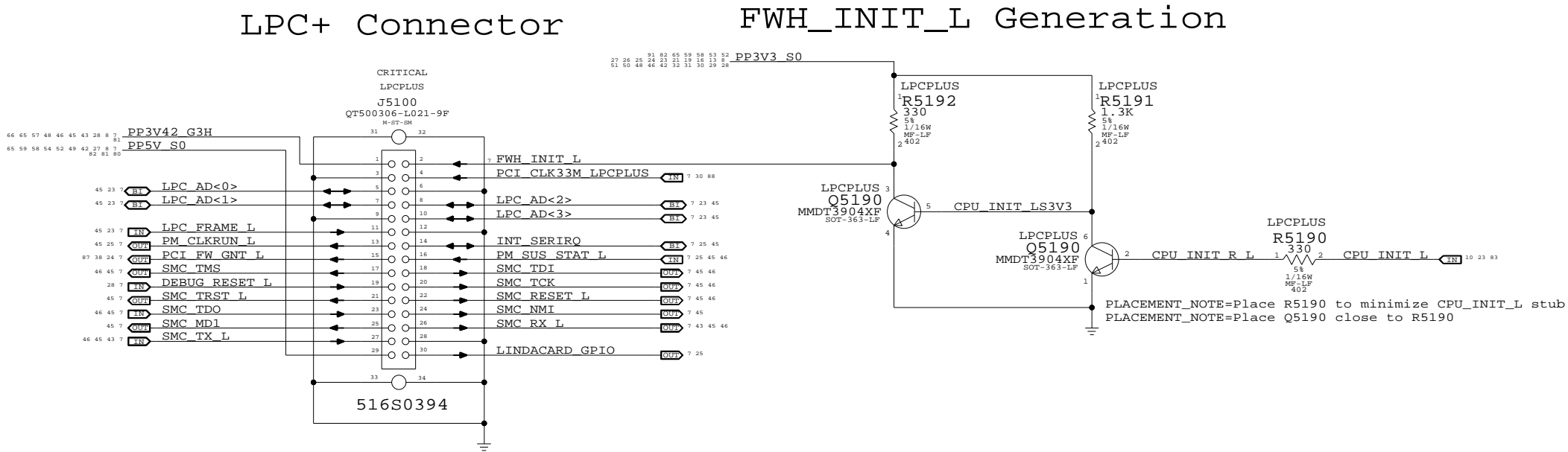
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SIZE D DRAWING NUMBER 051-7431 REV. A.0.0

SCALE NONE SHT 46 OF 92



LPC+ Debug Connector

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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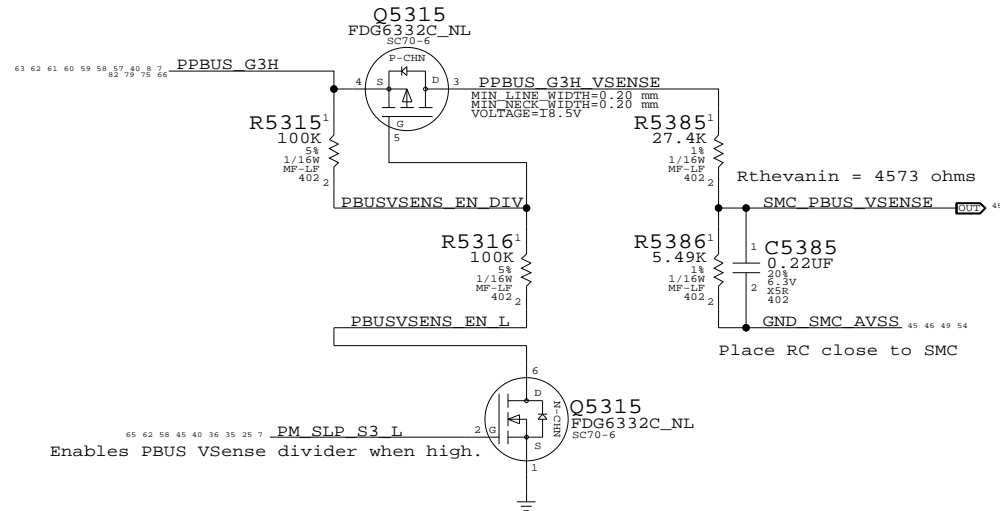
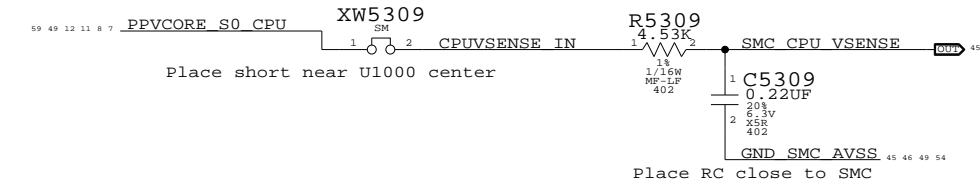
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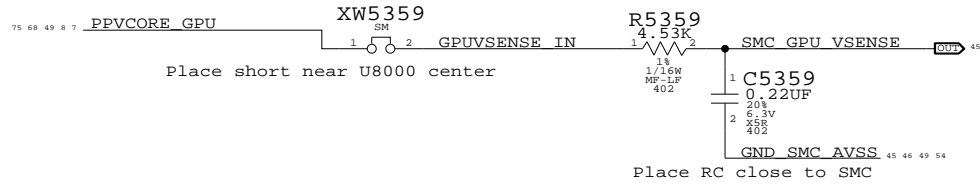
APPLE INC.	SIZE D	DRAWING NUMBER 051-7431	REV. A.0.0
	SCALE NONE	SHT 47	OF 92

CPU Voltage Sense / Filter

PBUS Voltage Sense & Filter

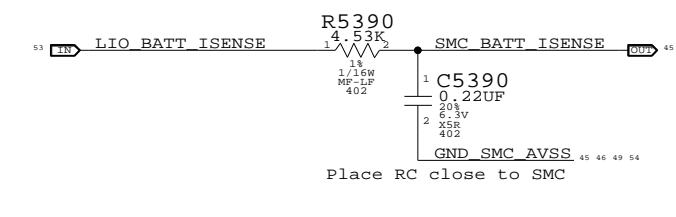
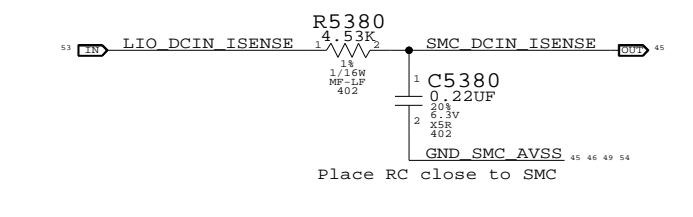
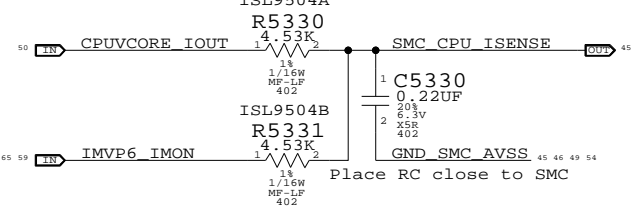
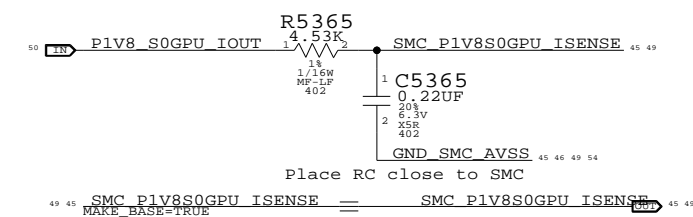


GPU Voltage Sense / Filter



DCIN Current Sense Filter

Battery (PBUS) Current Sense Filter

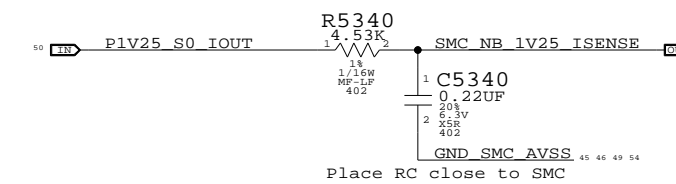
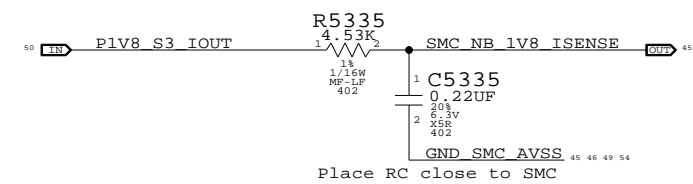
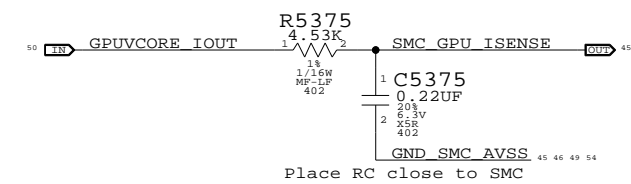
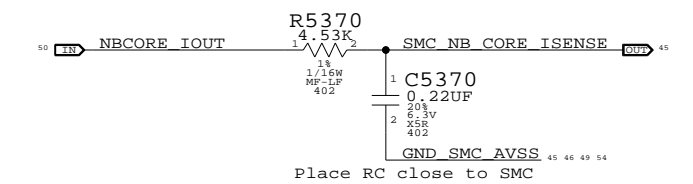


NB Core Current Sense Filter

GPU Current Sense Filter

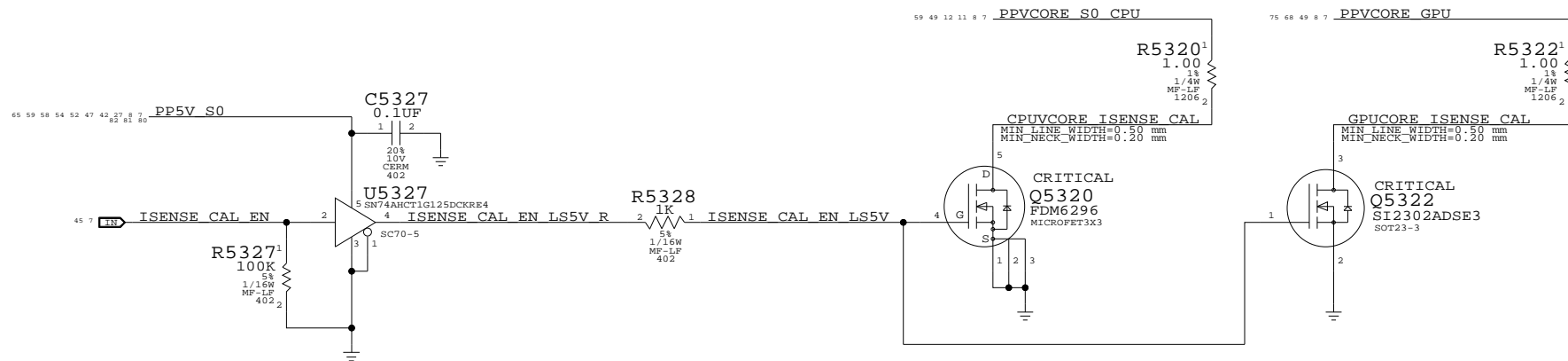
NB 1.8V Current Sense Filter

S0/GPU 1.25V Current Sense Filter



Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits

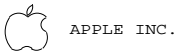


Current & Voltage Sensing

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

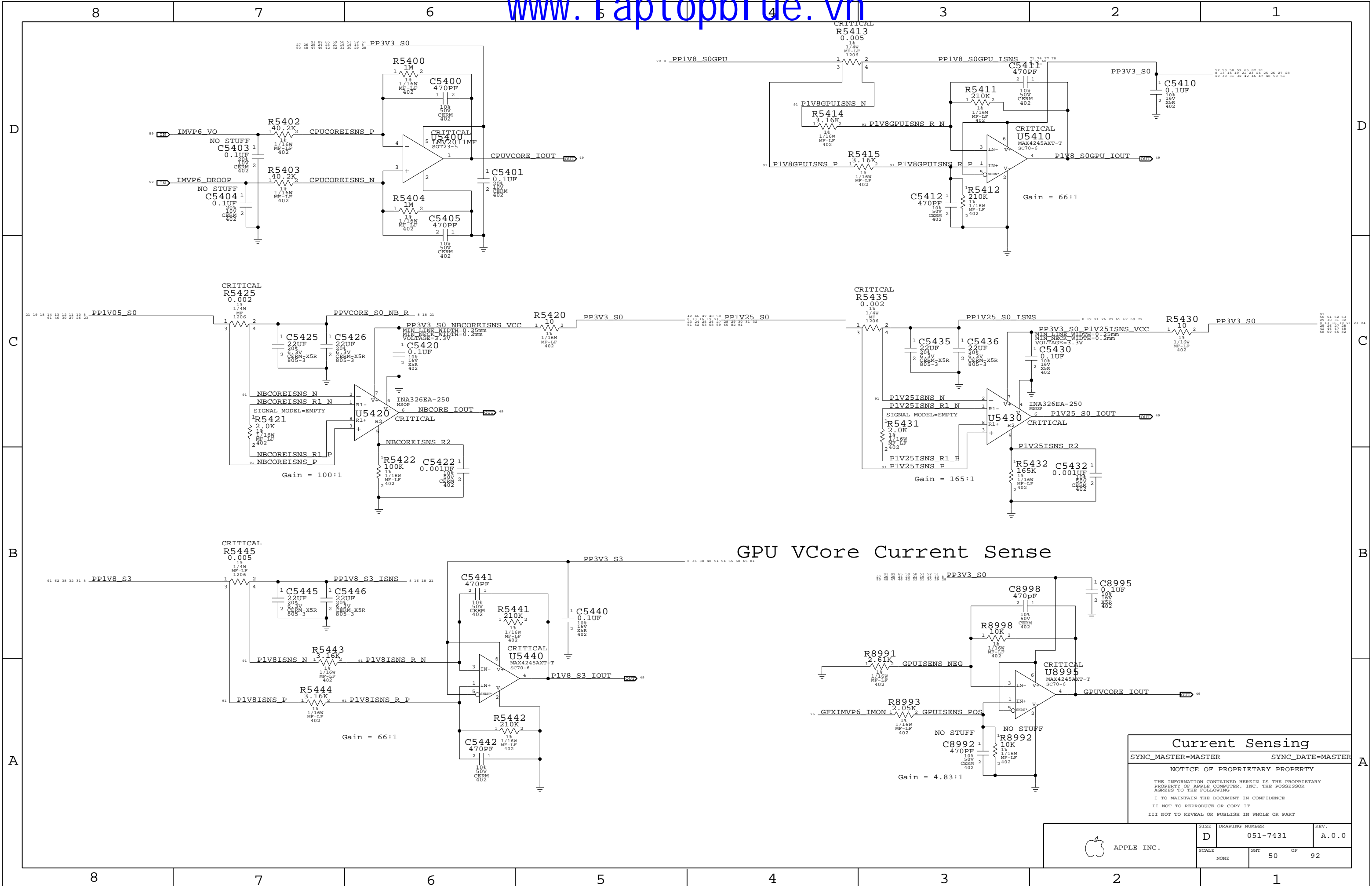
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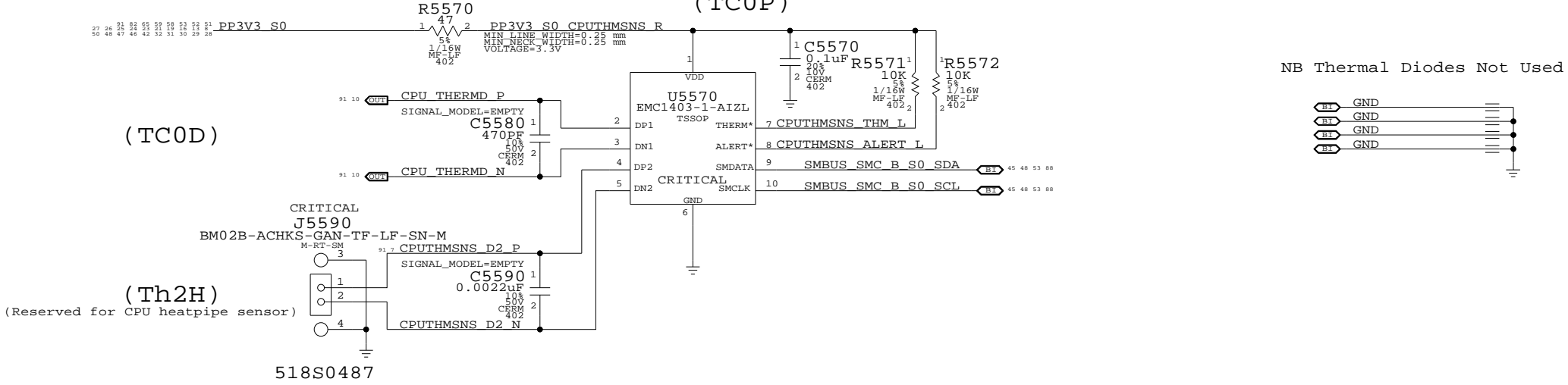


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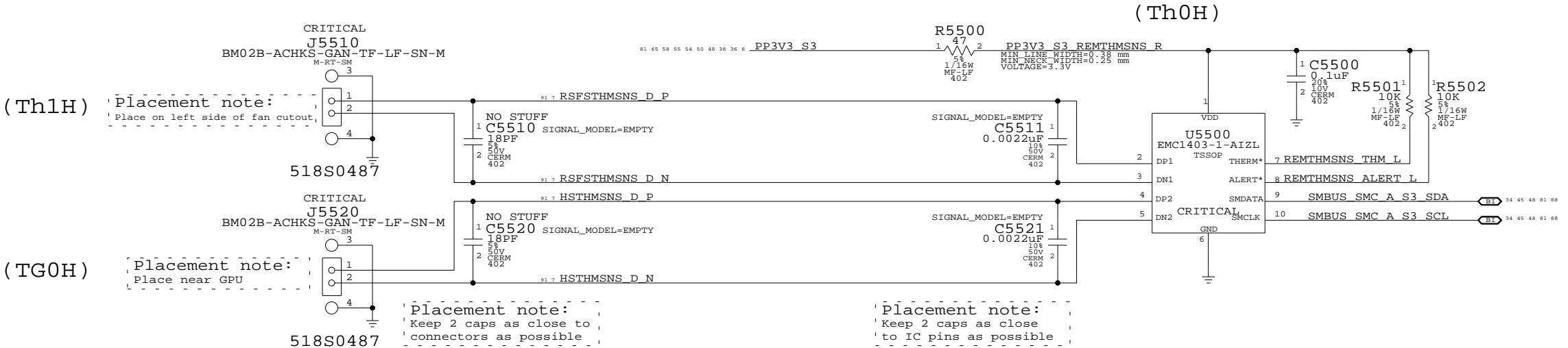
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SCALE	SHT	OF
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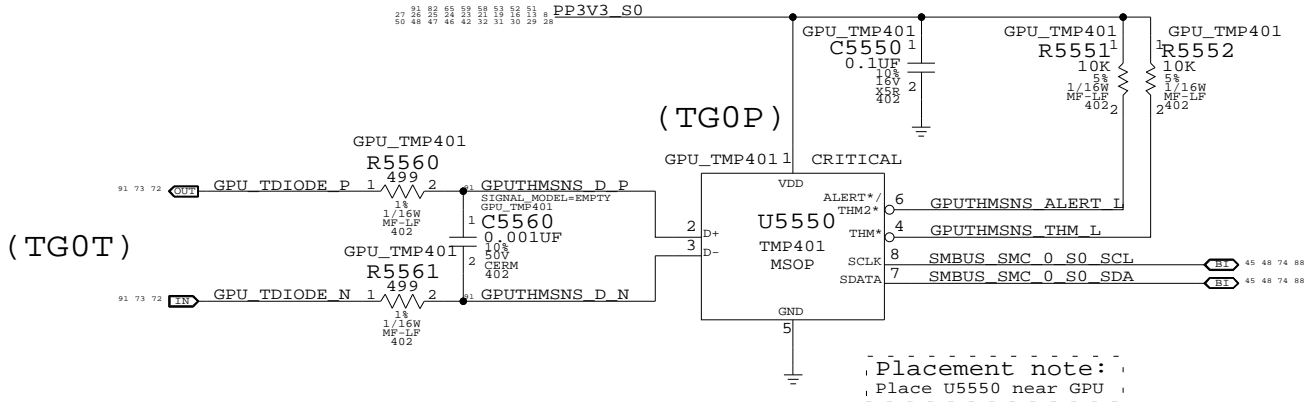
CPU T-Diode Thermal Sensor (TC0P)



GPU/Heat Pipe & Bottom Case Skin Thermal Sensor

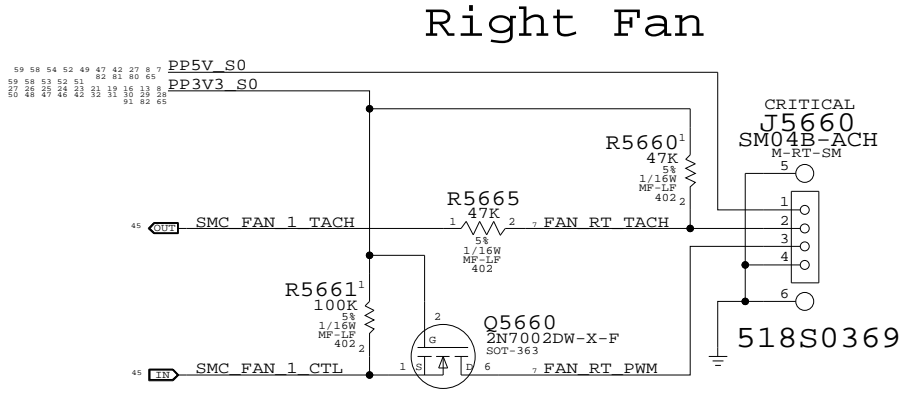
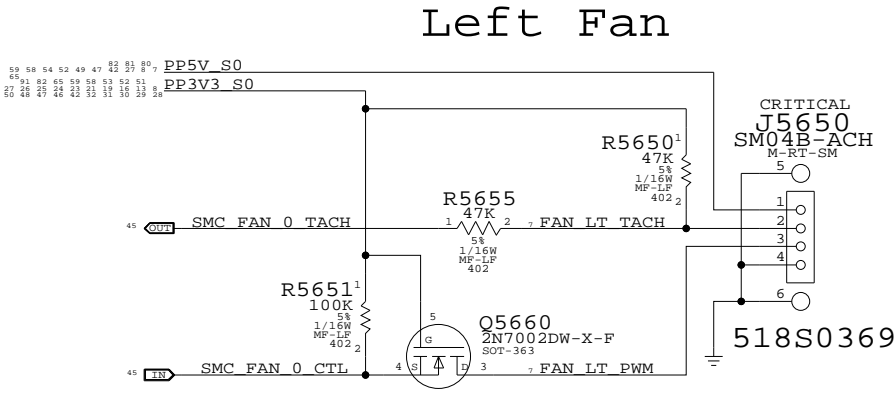


GPU Die Thermal Sensor



Thermal Sensors		
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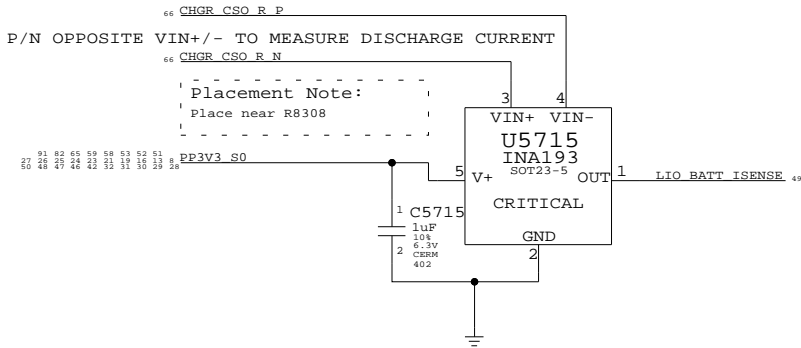
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NONE		51	92



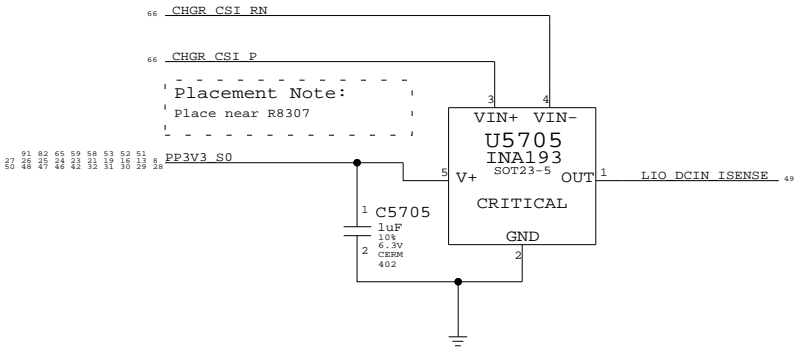
Fan Connectors		
SYNC_MASTER=M87_MLB		SYNC_DATE=08/28/2007
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	SCALE NONE	SHT 52 OF 92	

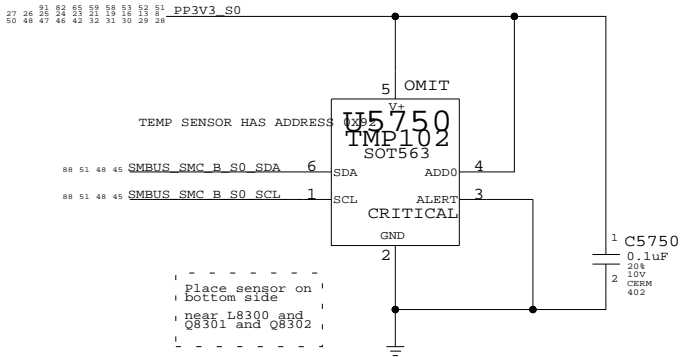
Battery Current Sense



DCIn Current Sense



Battery Charger Thermal Sensor



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S2039	1	revE of TMP102	U5750	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1807	353S2039		U5750	Alternate old version

Current & Thermal Sensors

SYNC_MASTER=M87_LIO SYNC_DATE=11/06/2007

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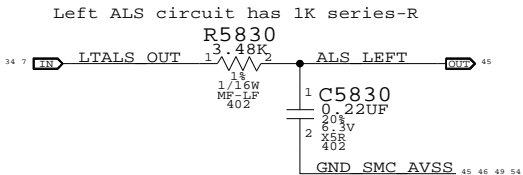
SHT

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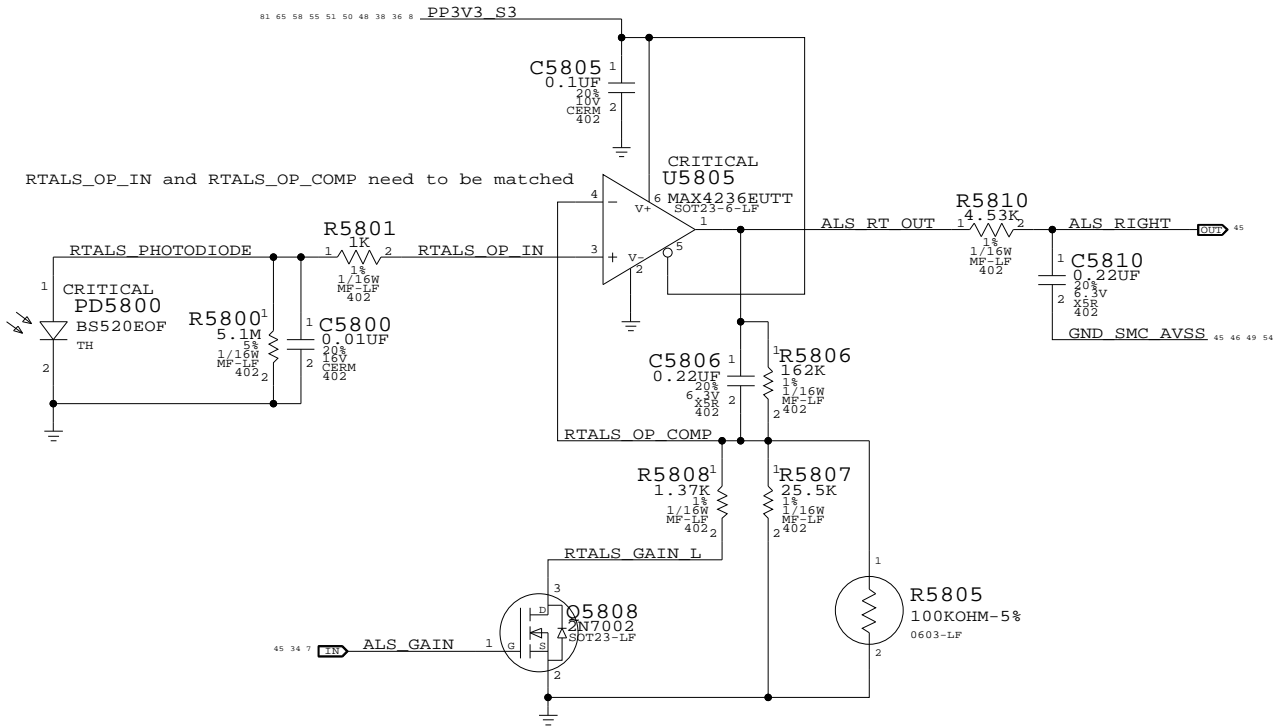
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92

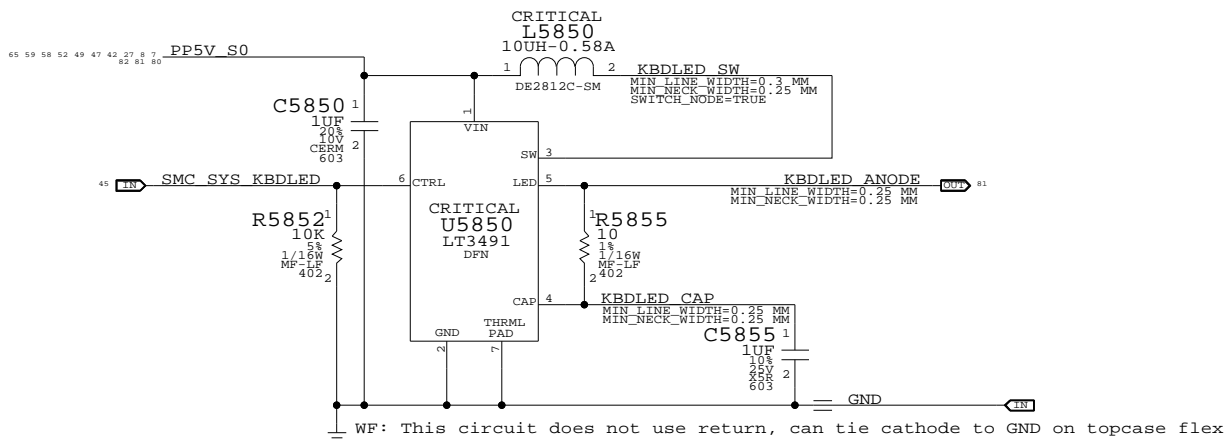
Left ALS Filter



Right ALS Circuit



Keyboard LED Driver



ALS Support

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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DRAWING NUMBER

051-7431

REV.

A.0.0

SCALE

NONE


SHT

54

OF

92

Alias SCL/SDA to GND if using analog outputs only

1 

A diagram showing a coordinate system with three axes: +X (pointing left), +Y (pointing up), and +Z (dn) (pointing down-right). A circle with the number 1 is located in the upper right quadrant.



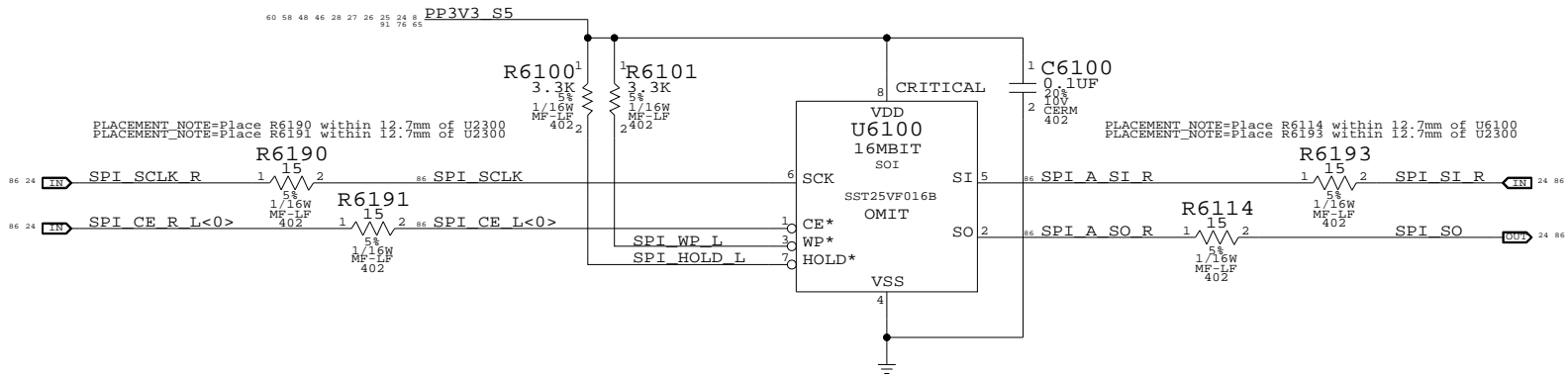
SIZE
D

SIZE	DRAWING NUMBER
D	051-7431

REV.
A.0.0

SCALE	NON
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SHT	55	OF	92
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SPI BootROM

SYNC_MASTER=T9_NOME

SYNC_DATE=01/25/2007


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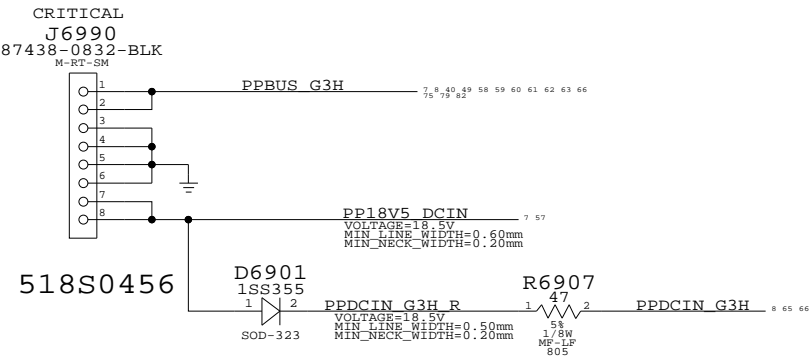
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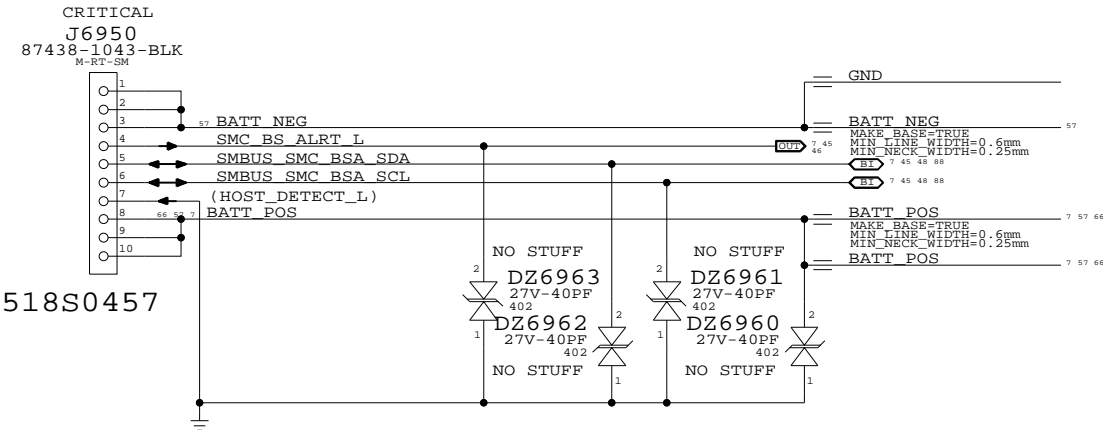
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 APPLE INC.	SIZE D	DRAWING NUMBER 051-7431	REV. A.0.0
	SCALE NONE	SHT 56	OF 92

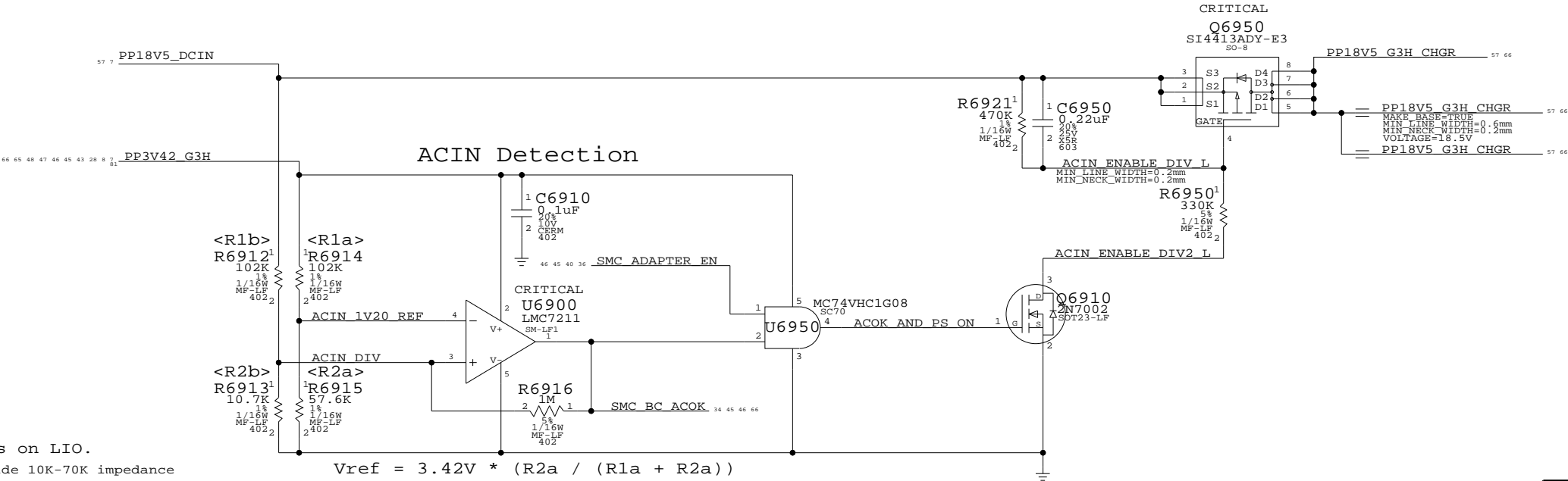
DC-In Connector



Battery Connector



Inrush Limiter



NOTE: R6910 is on LIO.
System must provide 10K-70K impedance to A52 adapter for system load detection.
REQ of R6910 (on LIO), R6912, & R6913 is 36.9K.

$V_{ref} = 3.42V * (R2a / (R1a + R2a))$
 $V_{th} = (V_{ref} / (R2b / (R1b + R2b)))$
 $V_{ref} = 1.23V$
 $V_{th} = 13.0V$
Assuming 1% variance for R6910-R6915 and 3.42V:
Worst case Vth: min:12.47V, max: 13.54V

DC-In & Battery Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

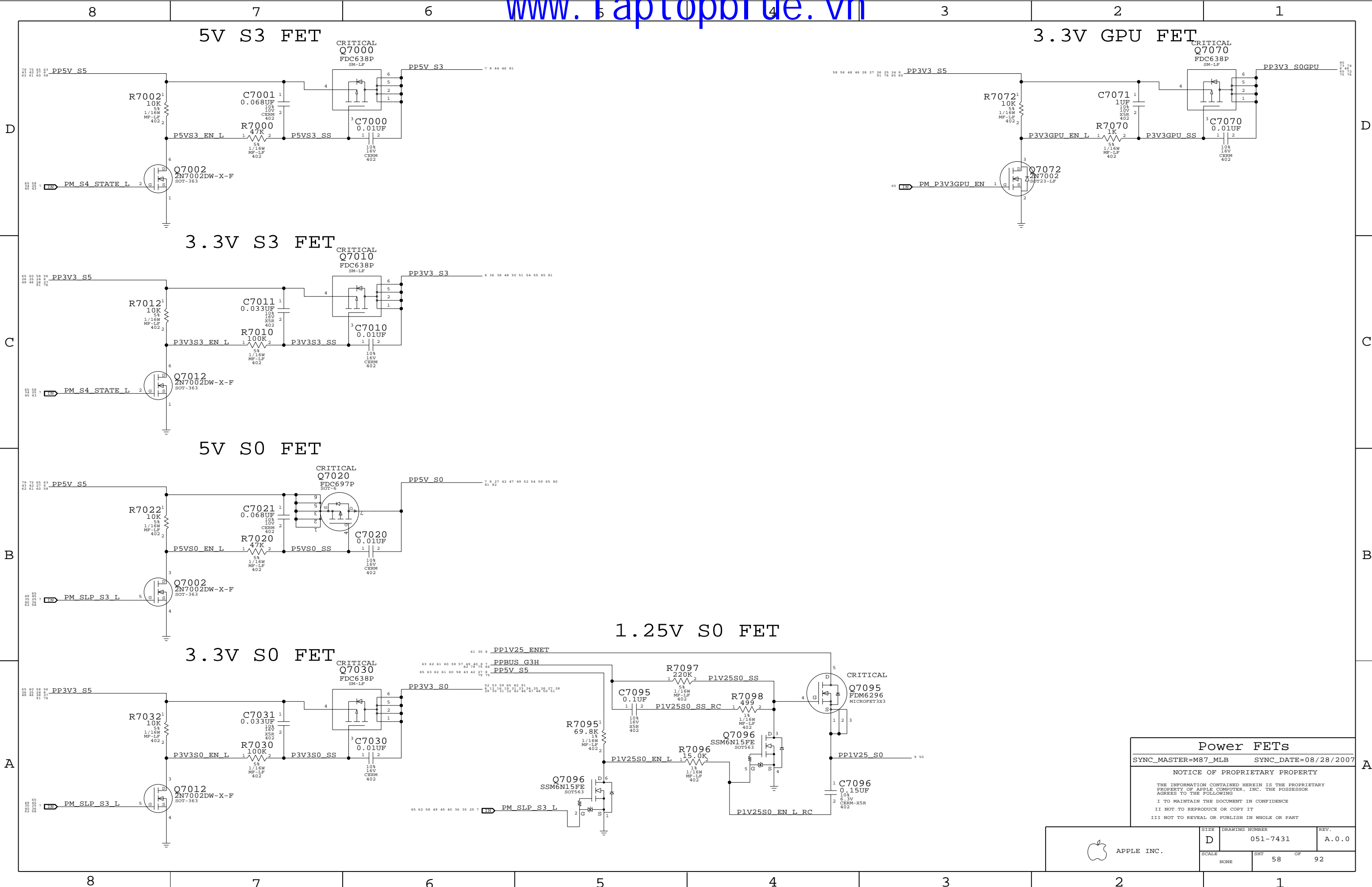
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SCALE	SHT	OF
NONE	57	92



Power FETs

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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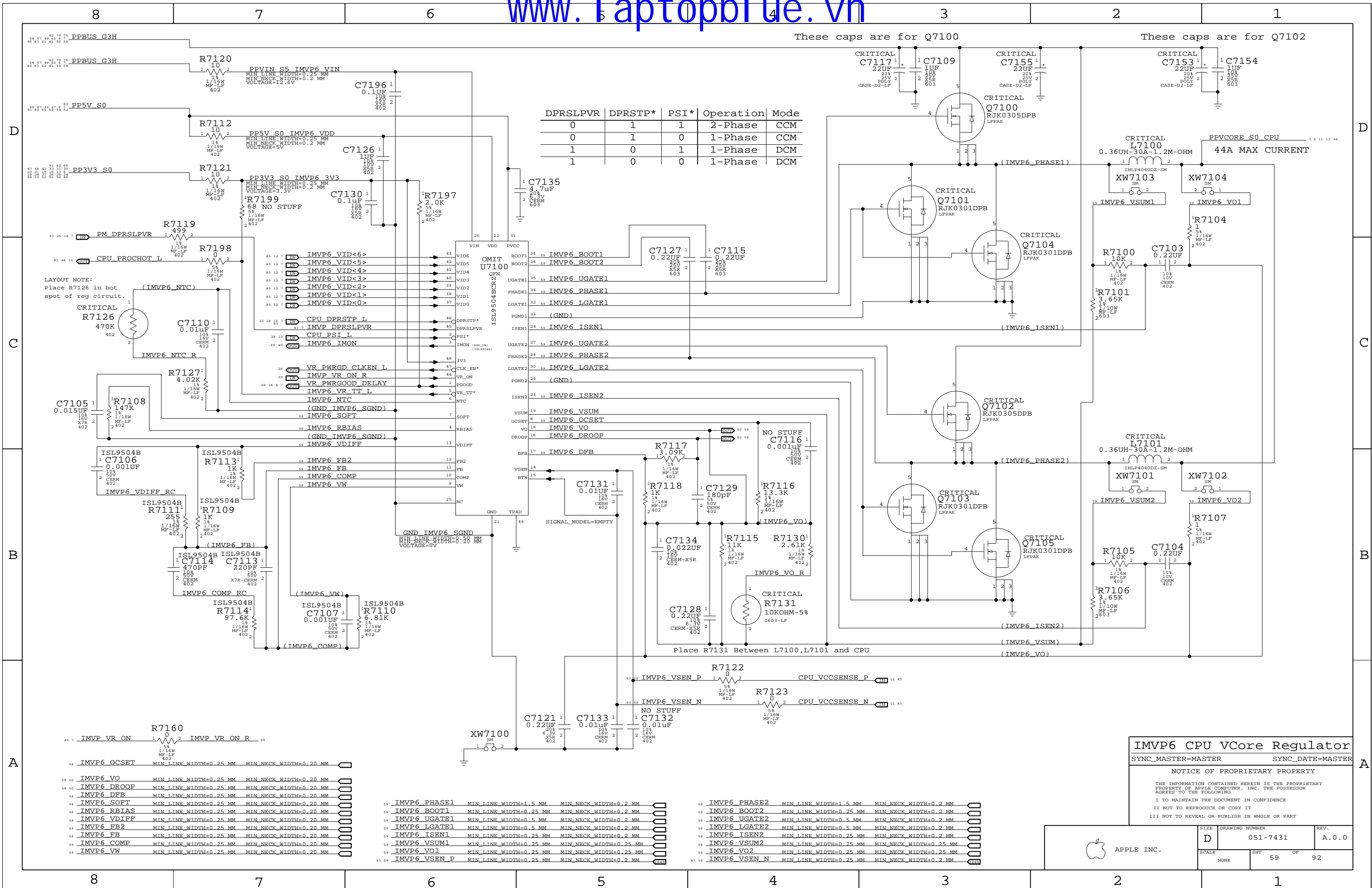
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7431	A.0.0
SCALE		SHT	OF
NONE		58	92



IMVP6 CPU VCore Regulator

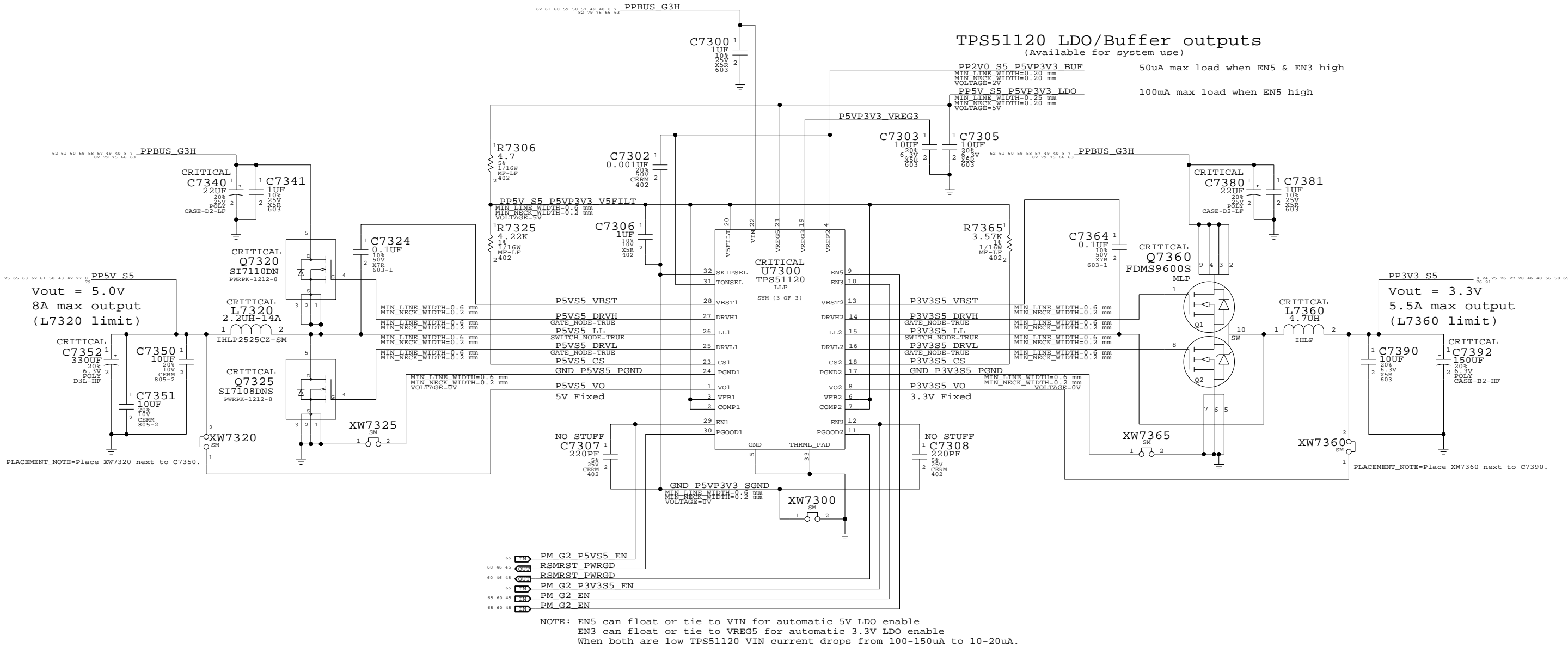
SYNC_MASTER=MASTER SYNC_DATE=MASTER

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SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE	SHT	OF
NONE	59	92



5V / 3.3V Power Supply

SYNC_MASTER=MASTER SYNC_DATE=MASTER

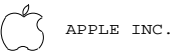
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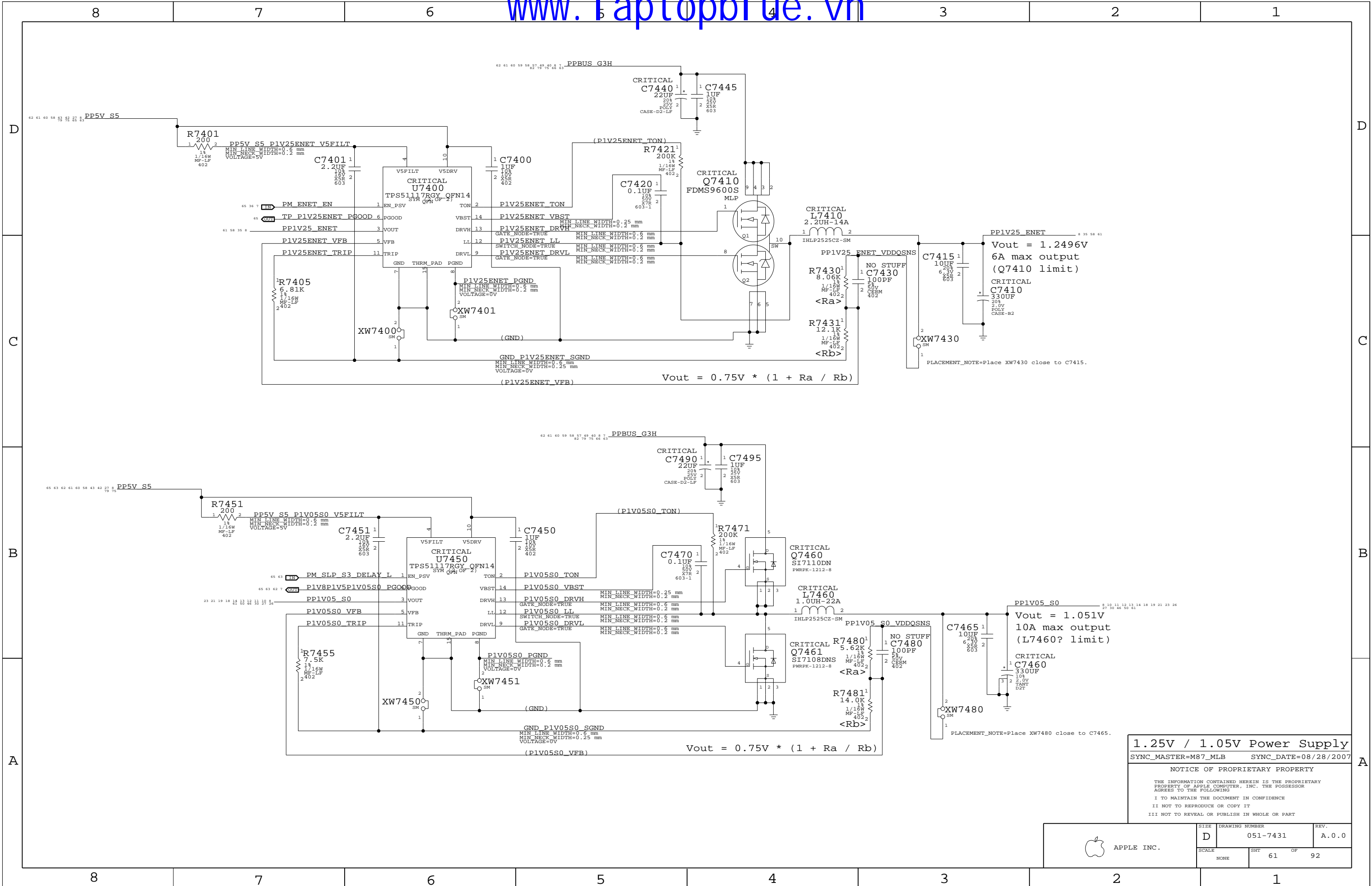
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APPLE INC.

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SCALE	SHT	OF
NONE	60	92



D

D

C

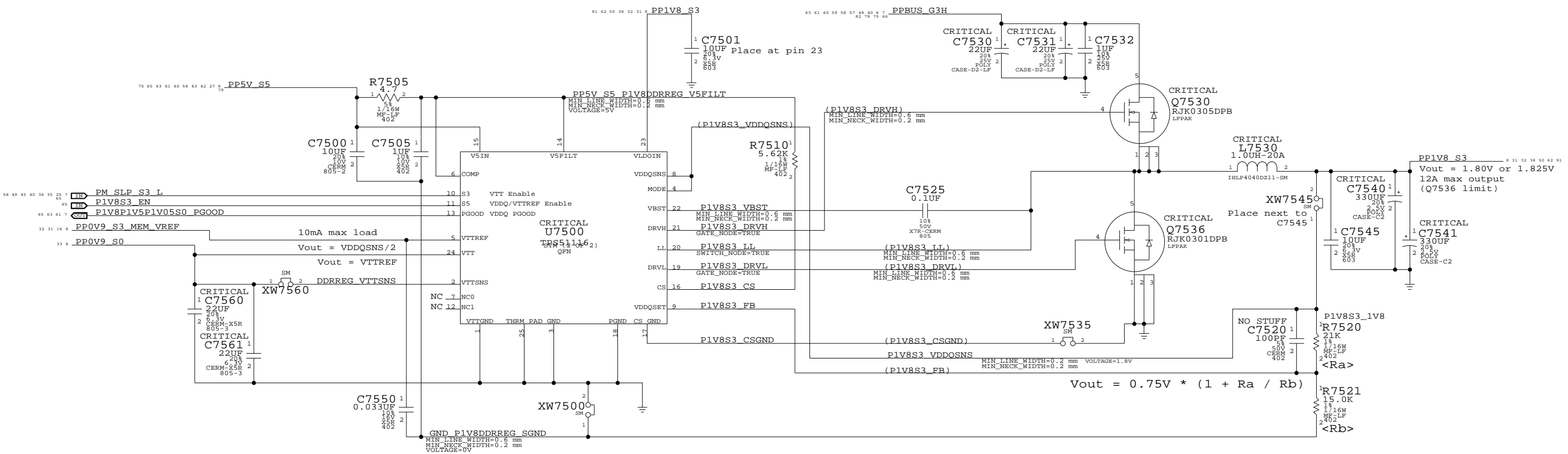
C

B

B

A

A



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0346	1	RES,MTL FILM,21.5K,1%,0402,SM,LF	R7520	CRITICAL	P1V8S3_1V825

1.8V DDR2 Supply

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE	SHT	OF
NONE	62	92

SYNC_MASTER=MASTER	SYNC_DATE=MASTER
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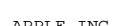
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SIZE
D

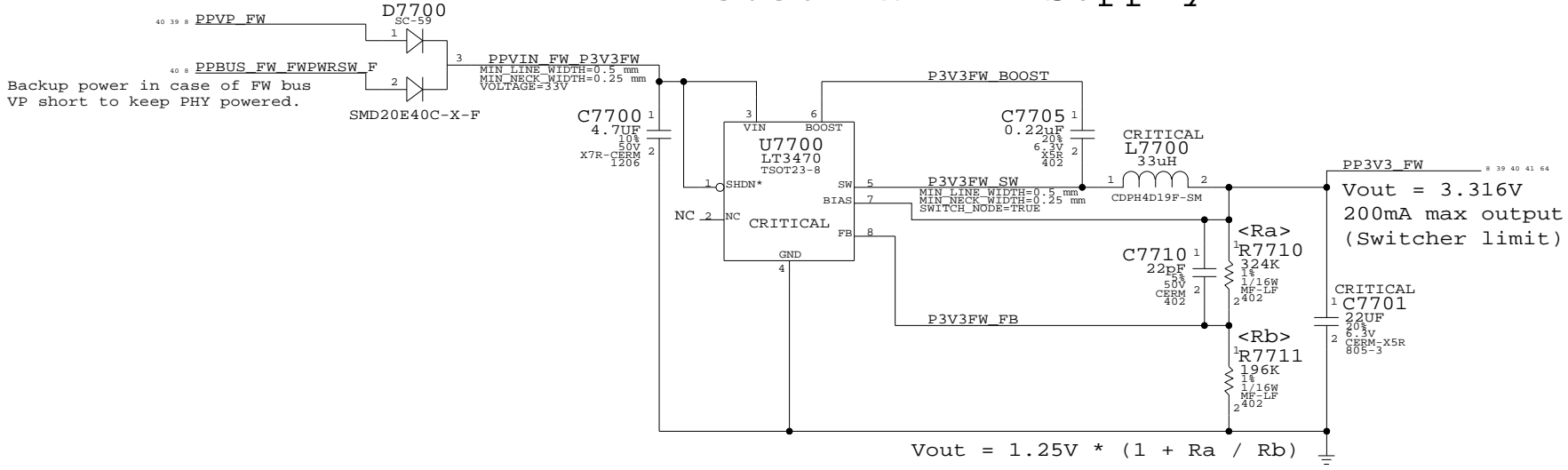
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REV.
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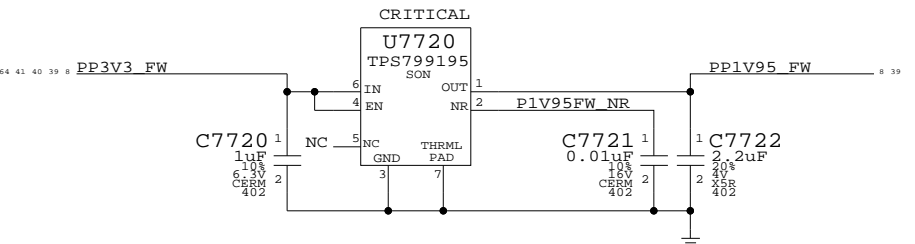
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SHT 63 OF 92

3.3V FW PHY Supply



1.95V FW PHY Supply



FW PHY Power Supplies

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007


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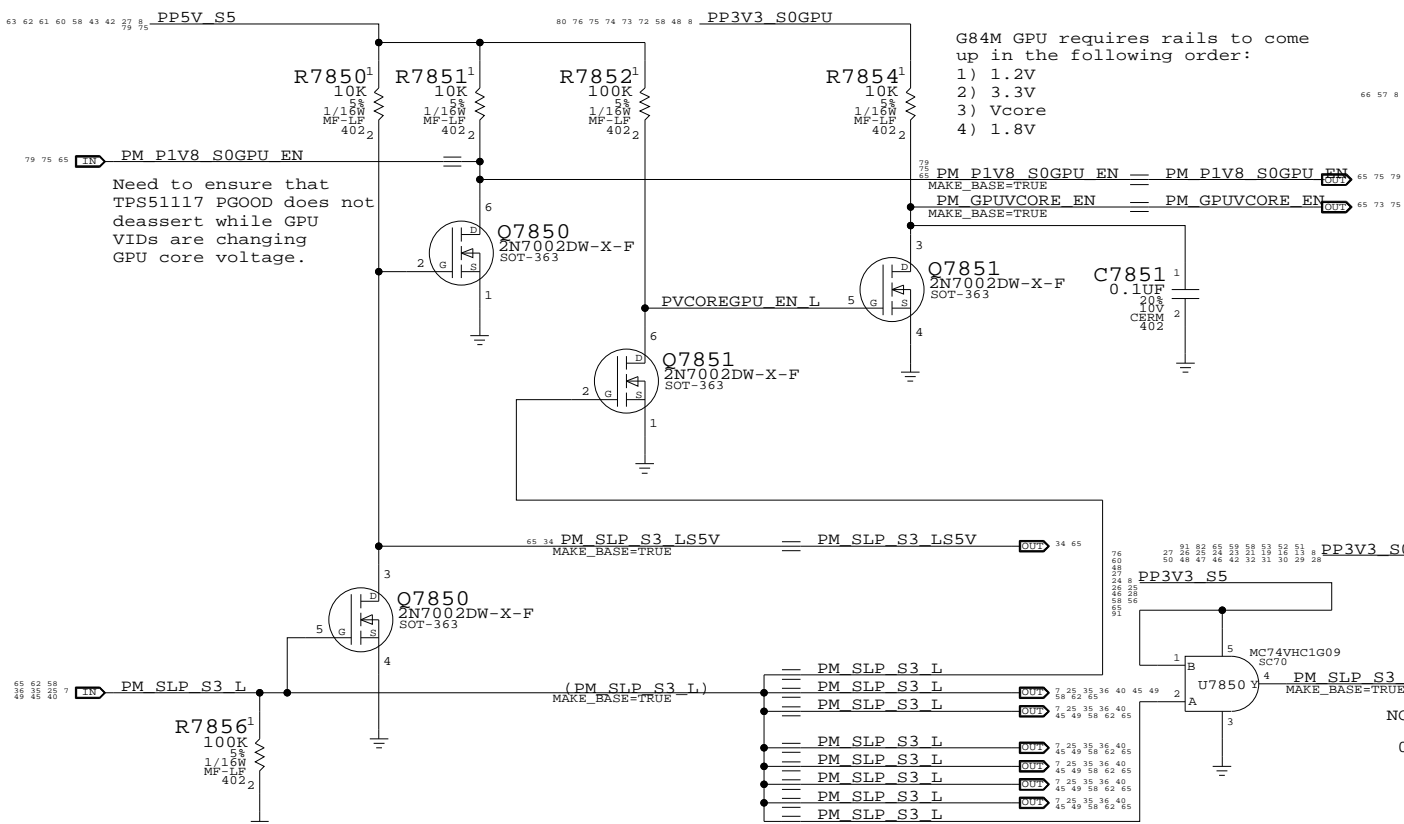
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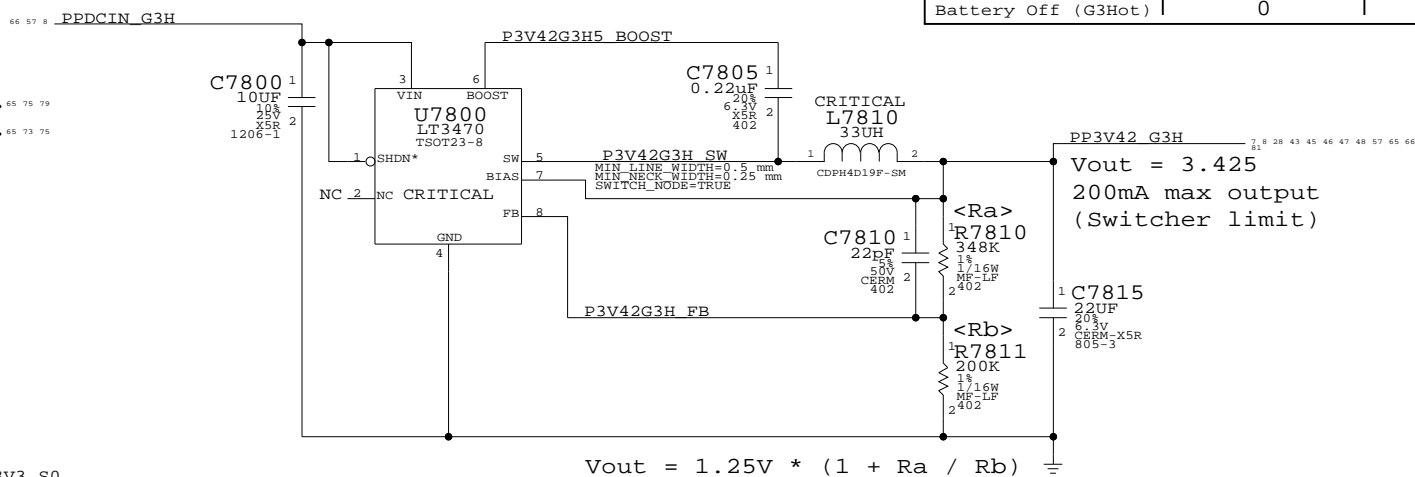
 APPLE INC.	SIZE D	DRAWING NUMBER 051-7431	REV. A.0.0
	SCALE NONE	SHT 64	OF 92

Power Control Signals



3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC Vref generator



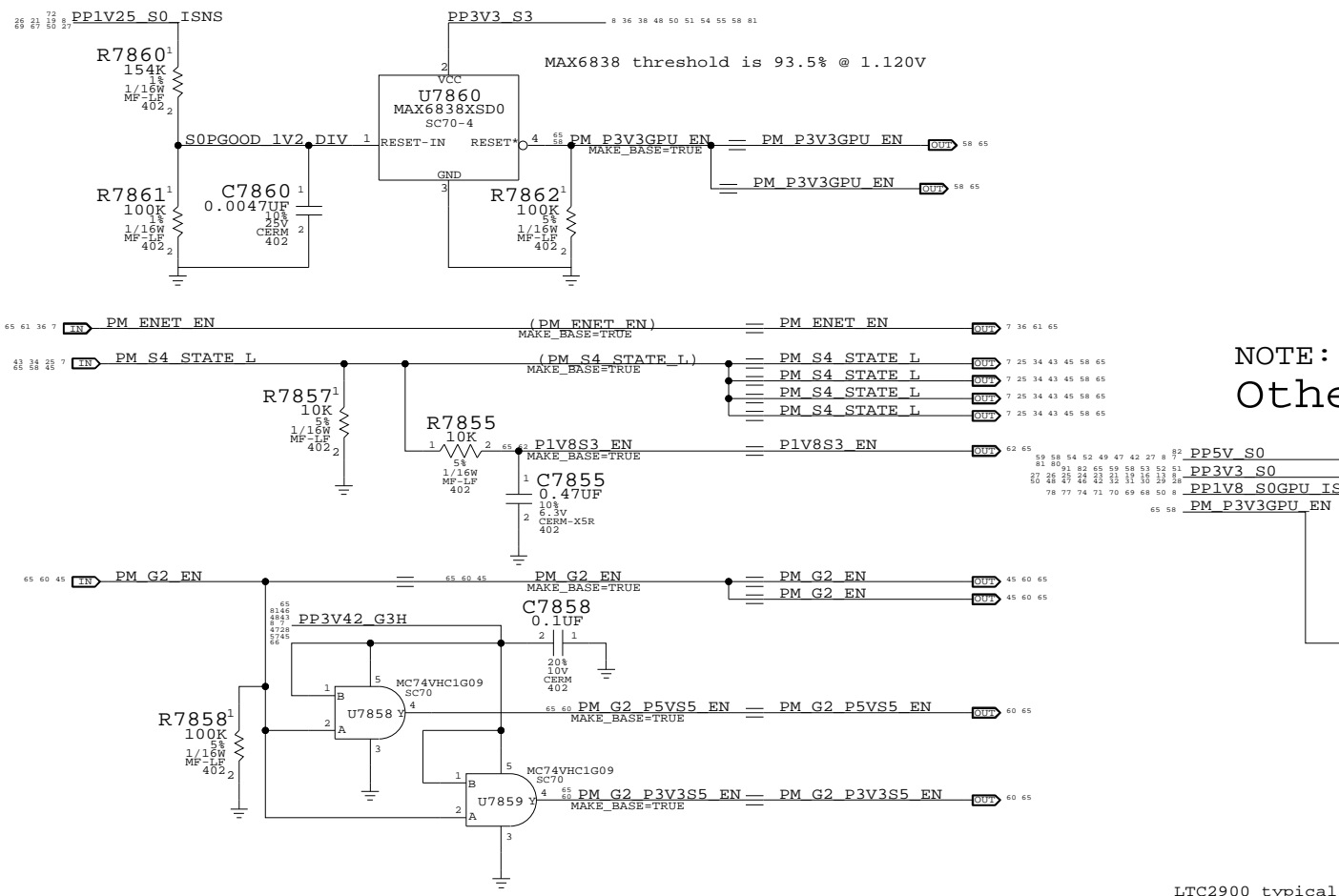
State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

Unused PGOOD Signals

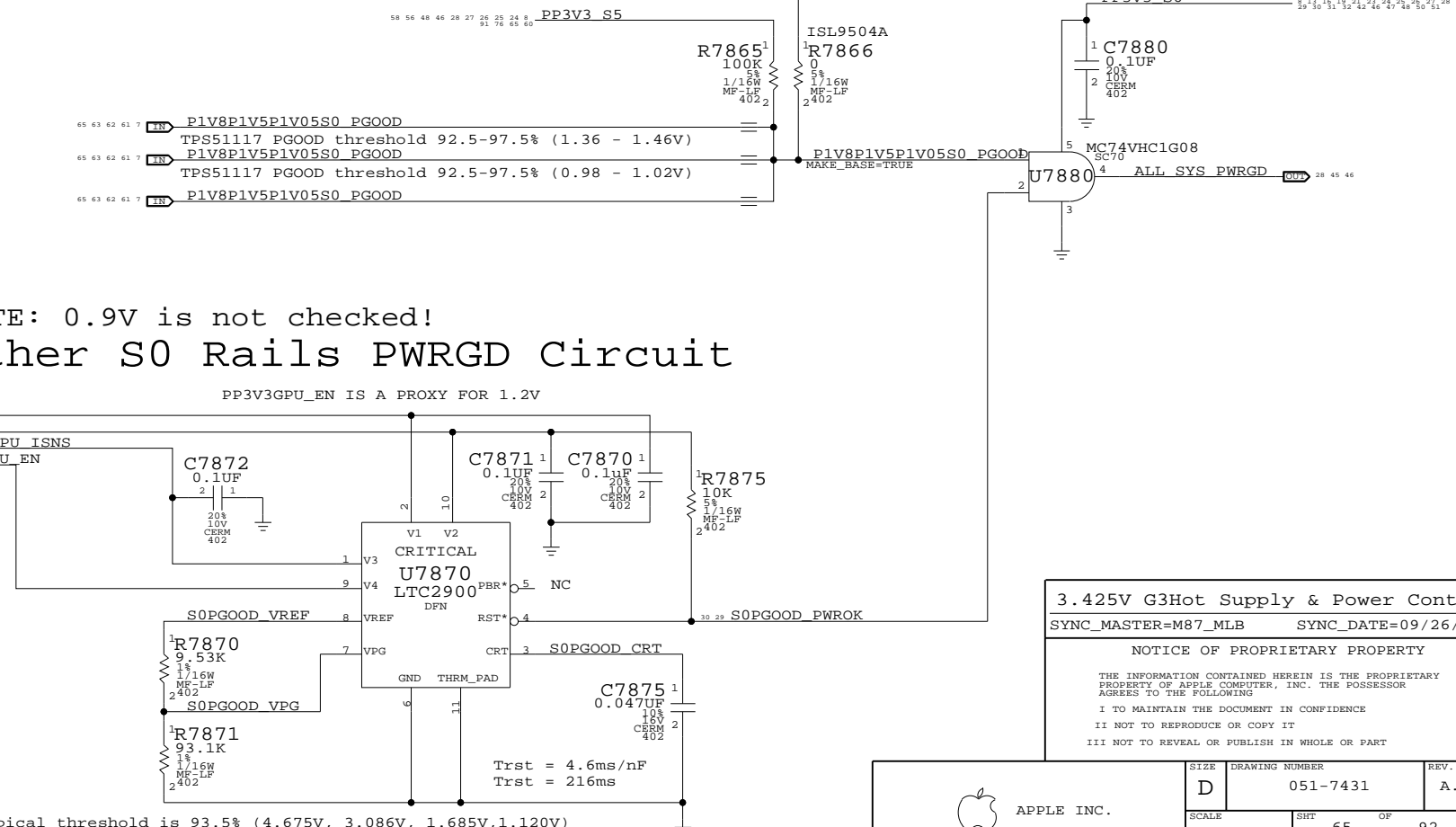
TP P1V25ENET PGOOD = TP P1V25ENET PGOOD
TP P1V8 S0GPU PGOOD = TP P1V8 S0GPU PGOOD

1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation



NOTE: 0.9V is not checked!
Other S0 Rails PWRGD Circuit



3.425V G3Hot Supply & Power Control

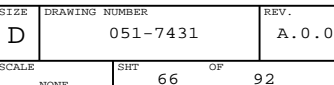
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SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE	SHT	OF
NONE	65	92



Page Notes

Power aliases required by this page:

- =PPIV2_GPU_PEX_PLLXVDD
- =PPIV2_GPU_PEX_IOVDDQ
- =PPIV2_GPU_PEX_IOVDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

PPIV25_S0_ISNS
PPIV25_S0_ISNS
PPIV25_S0_ISNS

PEX 1.2V Current = 2A

250mA

1500mA

180mA

20mA

PPIV2_GPU_PEX_PLLAVDD F
MIN LINE WIDTH=0.25 mm
MIN NC-C-WIDTH=0.25 mm
VOLTAGE=1.2V

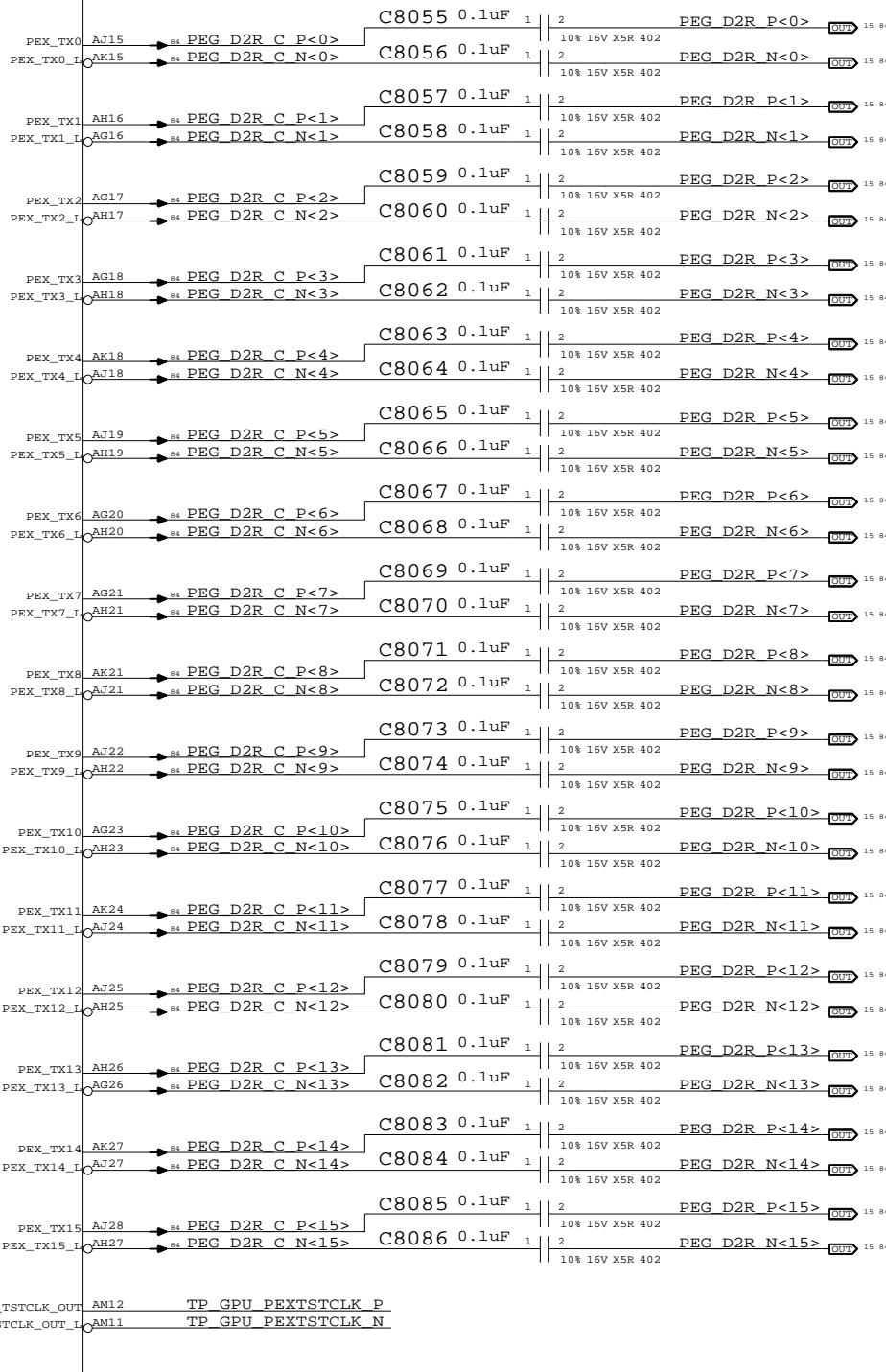
PPIV2_GPU_PEX_PLIVDD F
MIN LINE WIDTH=0.25 mm
MIN NC-C-WIDTH=0.25 mm
VOLTAGE=1.2V



OMIT

U8000
NB8P-GS-W-A2
BGA
(1 OF 8)

PCI-EXPRESS BUS INTERFACE



NV G84M PCI-E

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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APPLE INC.

SIZE

D

DRAWING NUMBER

051-7431

REV.

A.0.0

SCALE

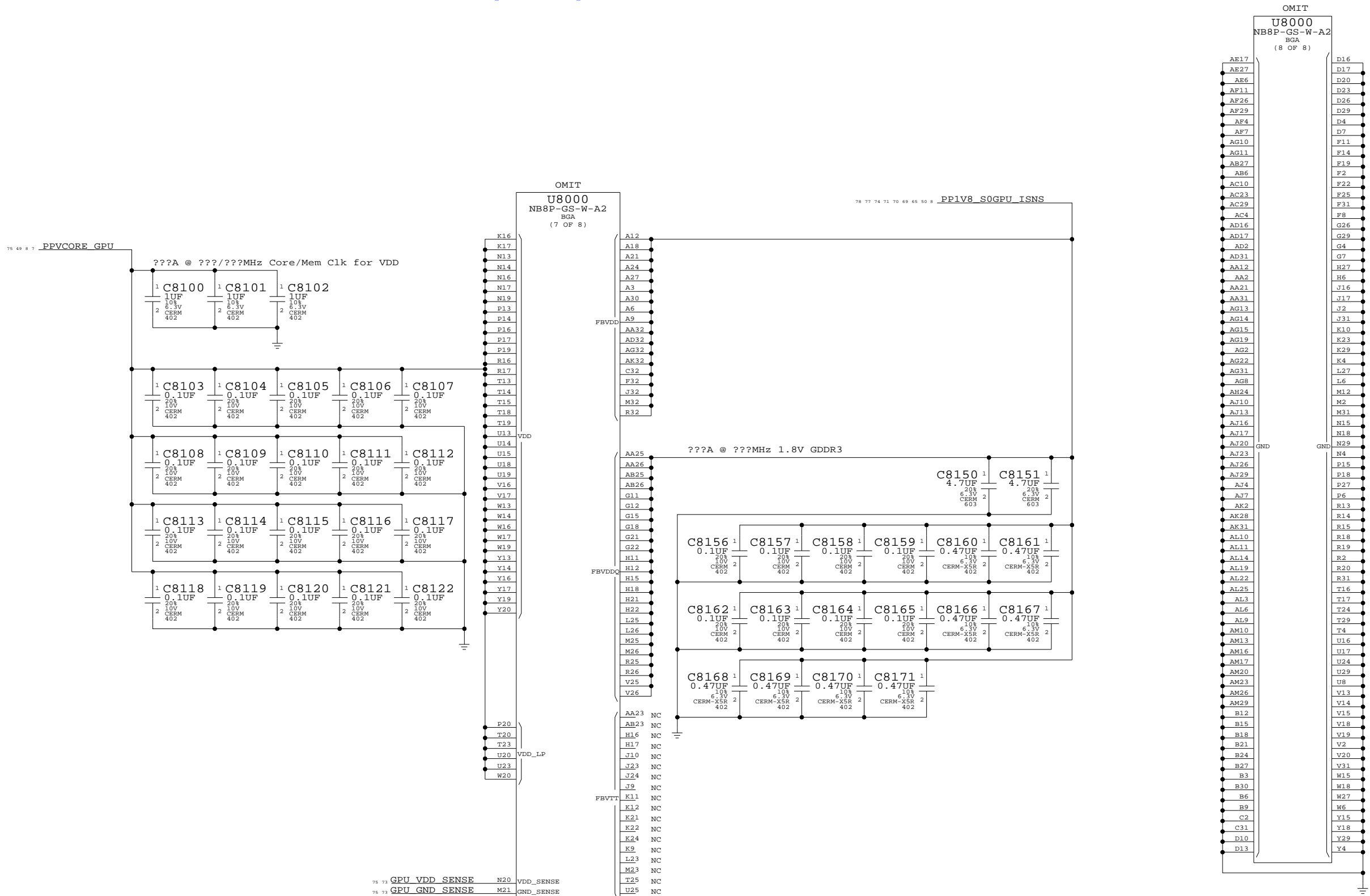
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SHT

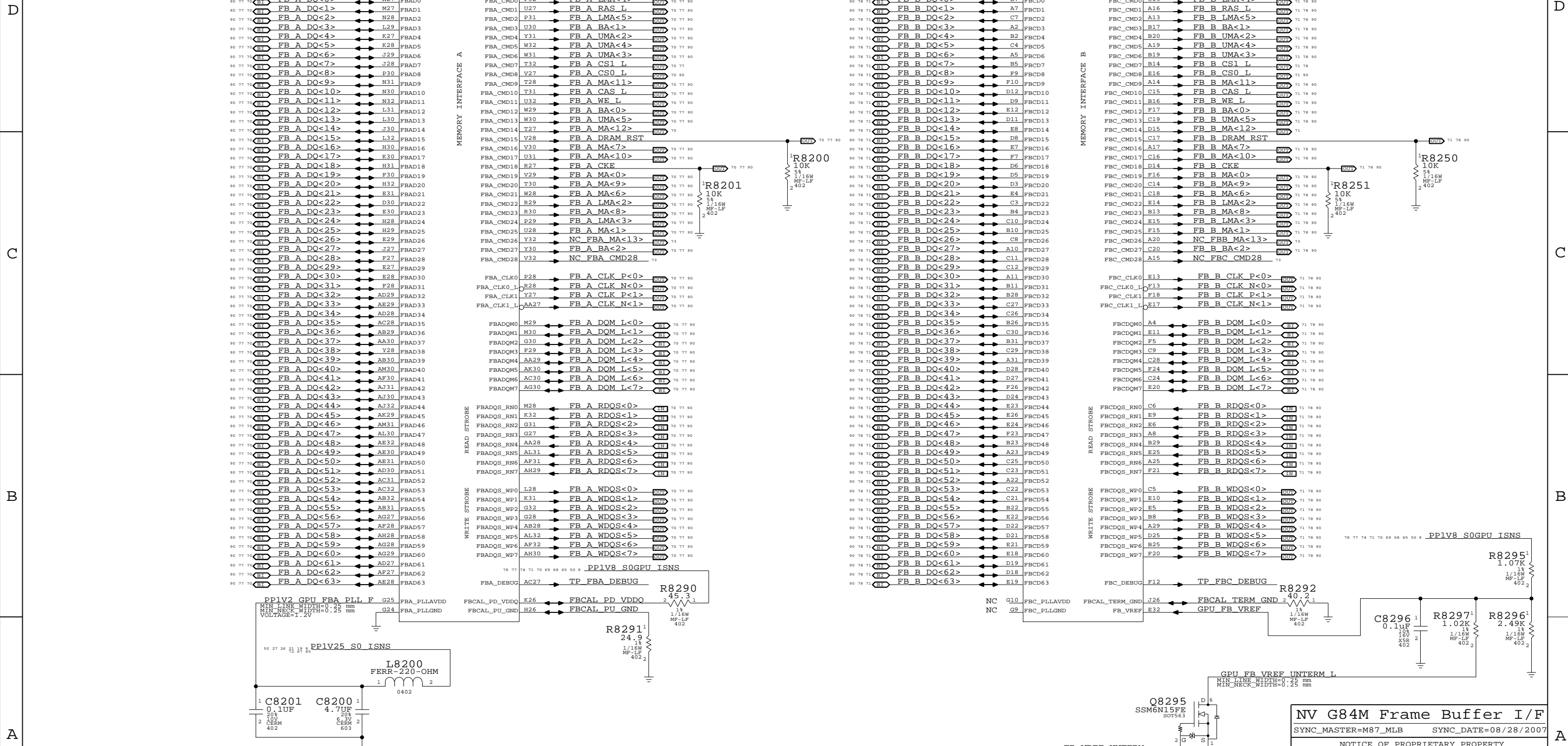
67

OF

92




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- =PP1V2_GPU_FBPLLAVDD
- =PP1V8_GPU_FBIO
Signal aliases required by this page:
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BOM options provided by this page:
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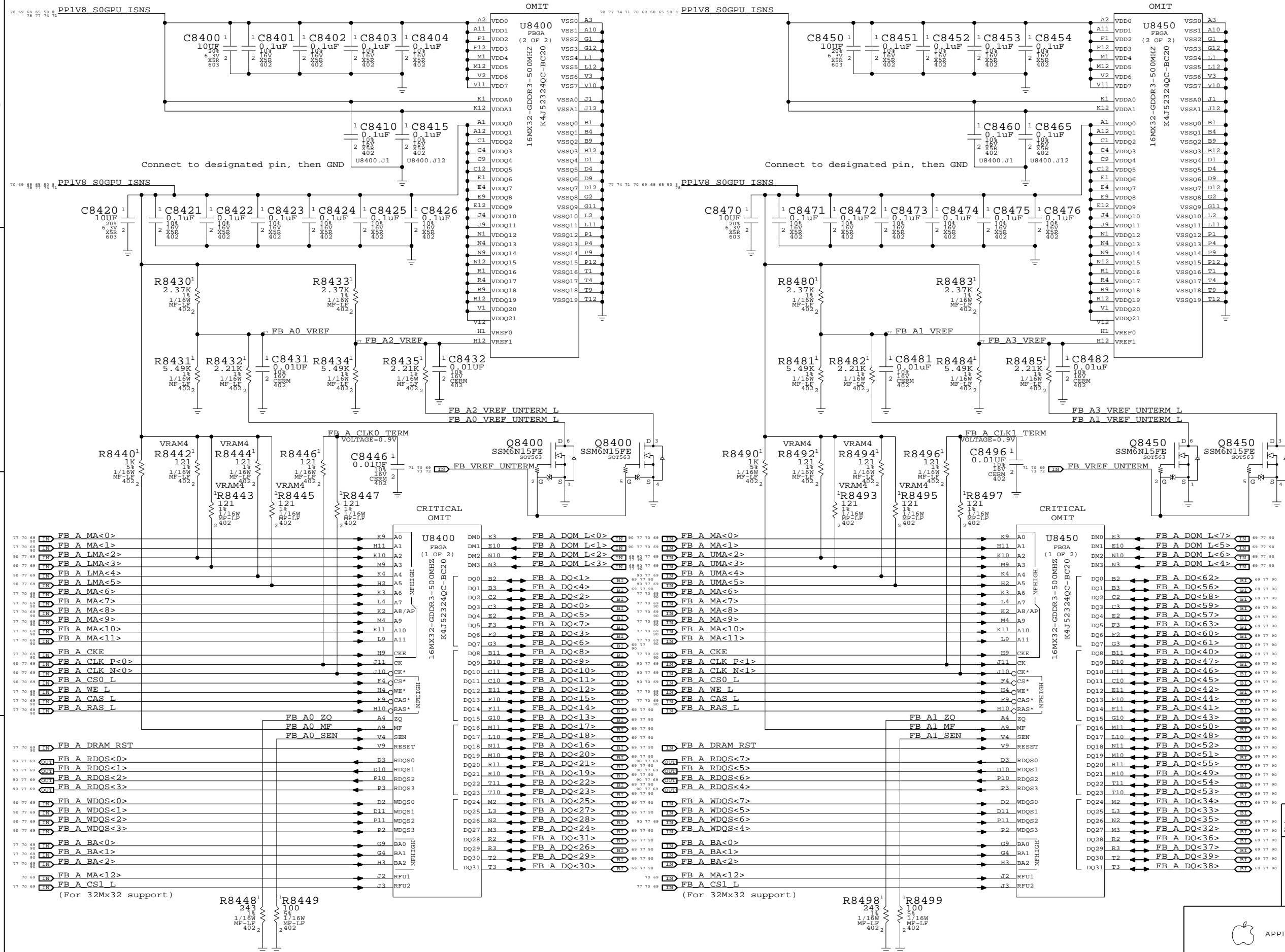
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Power aliases required by this page: - =Pp1v8_S0_FB_VDD - =Pp1v8_S0_FB_VDDQ
Signal aliases required by this page: (NONE)
BOM options provided by this page: (NONE)



GDDR3 Frame Buffer A (Top)

SYNC_MASTER=M87_MLB	SYNC_DATE=08/28/2007
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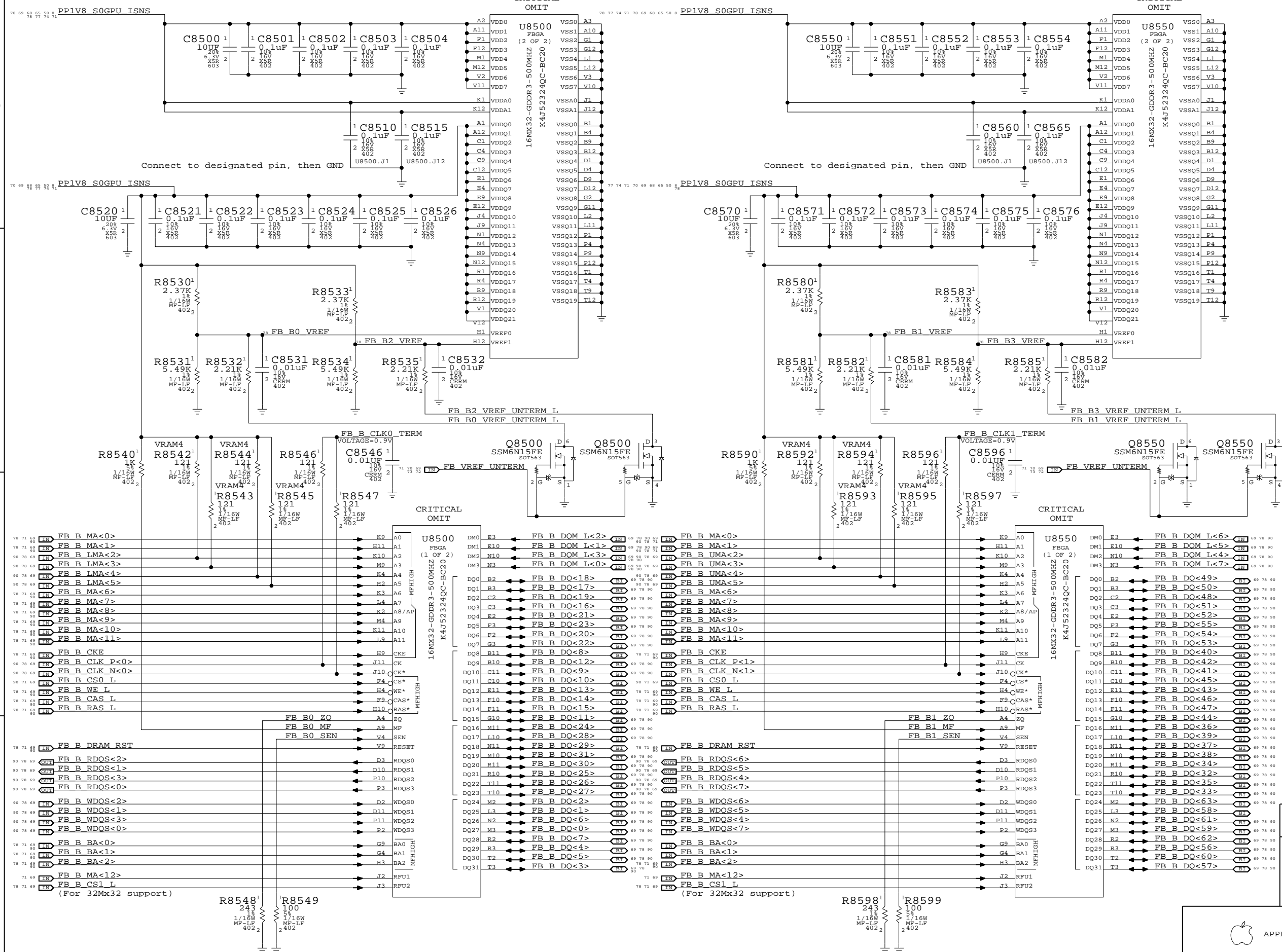
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Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)
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GDDR3 Frame Buffer B (Top)

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2017

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D

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(NONE)



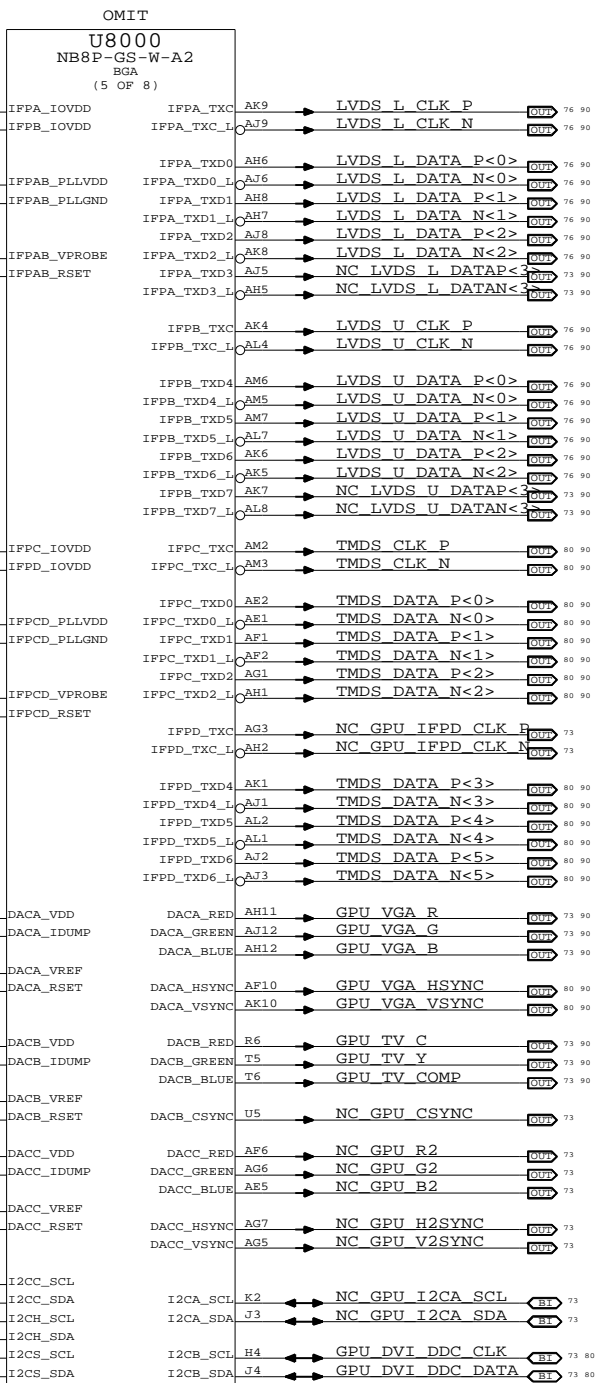
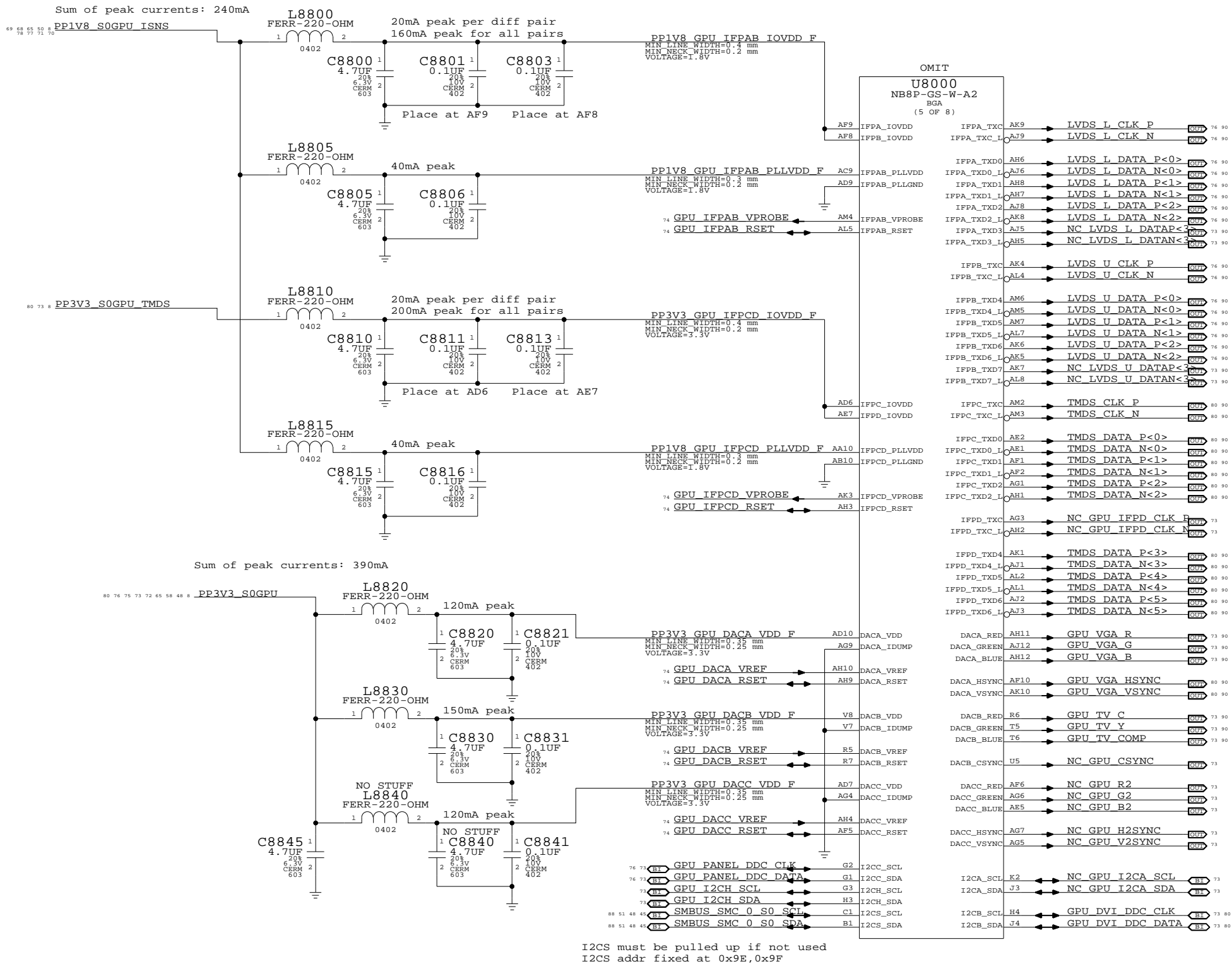
 APPLE INC.	SIZE D	DRAWING NUMBER 051-7431	REV. A.0.0
	SCALE NONE	SHT OF 72 OF 92	

Page Notes

Power aliases required by this page:
- =PP1V8_GPU_IFPX
- =PP3V3_GPU_IFPCD_IOVDD
- =PP3V3_GPU_DAC

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



Composite/S-Video	VGA	Component
C	R	Pr
Y	G	Y
Comp	B	Pb

NV G84M Video Interfaces

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

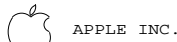
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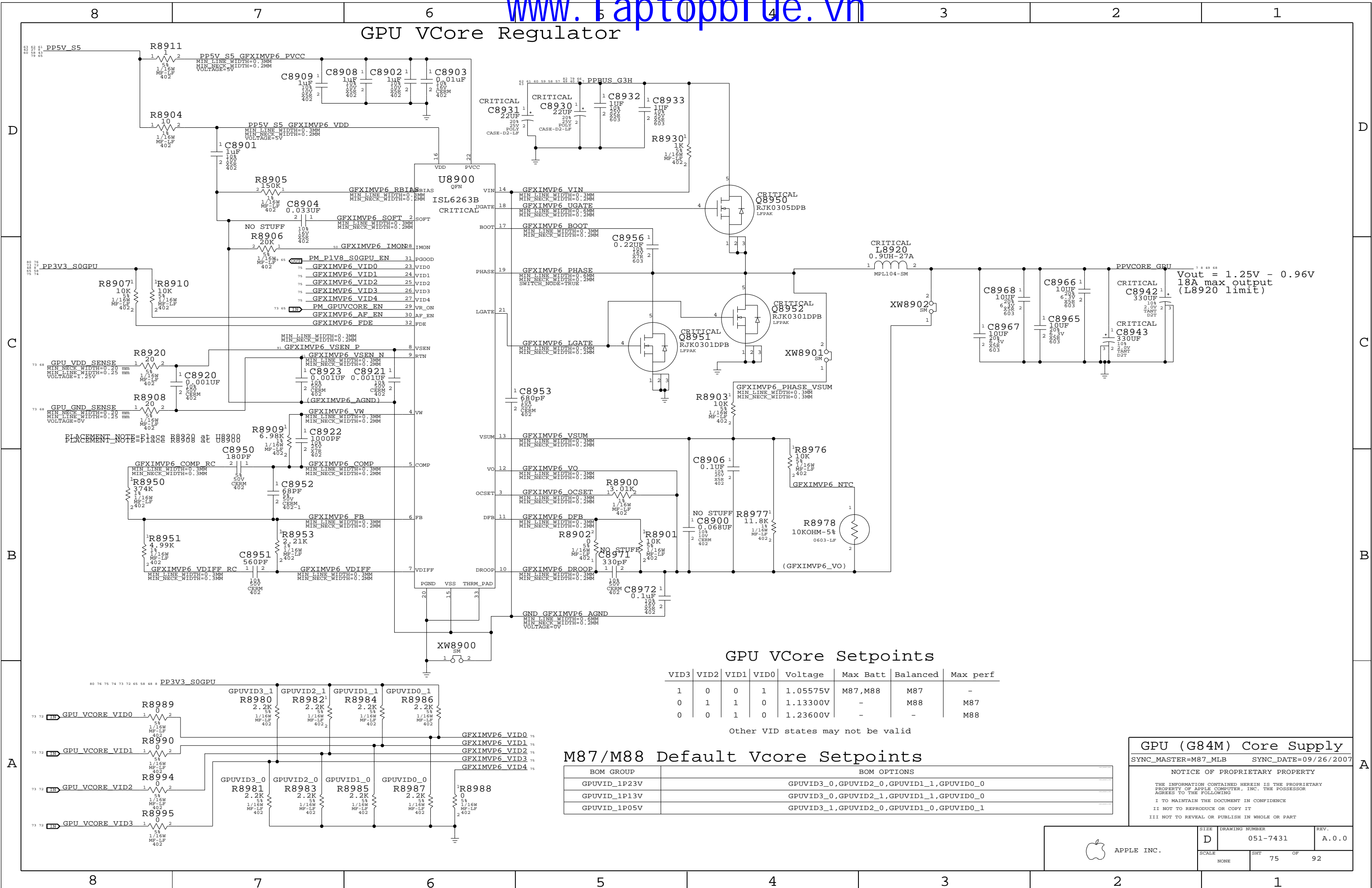
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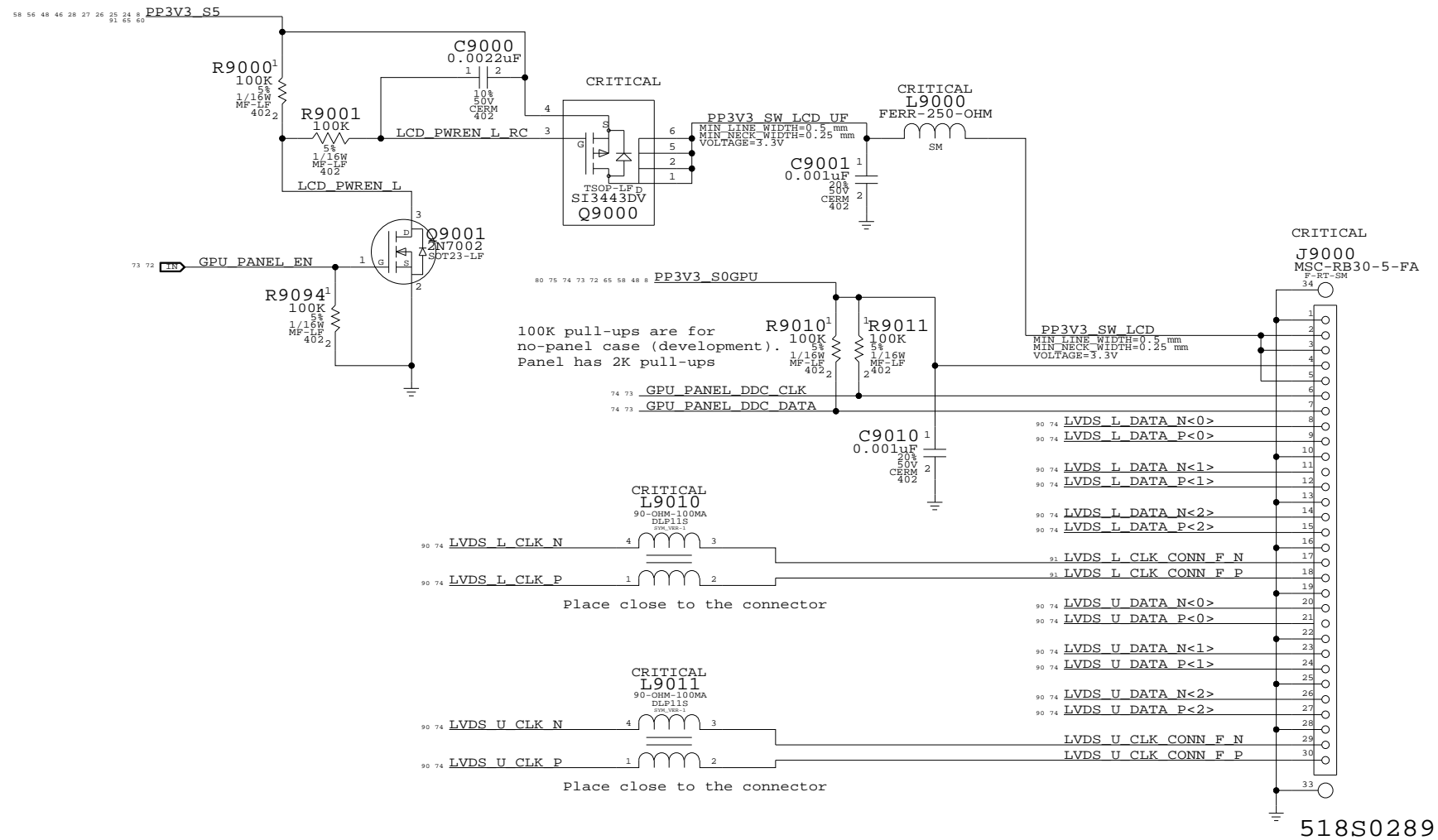
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE	SHT	OF
NONE	74	92

GPU VCore Regulator



LCD (LVDS) INTERFACE



LVDS Display Connector

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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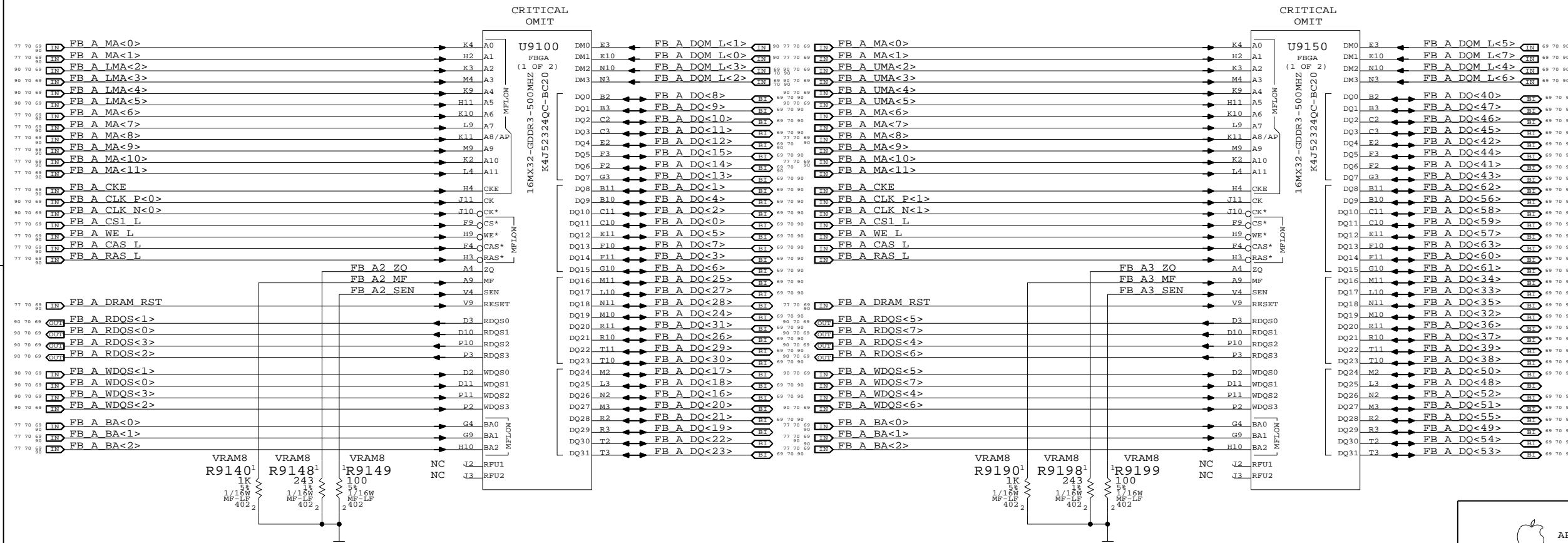
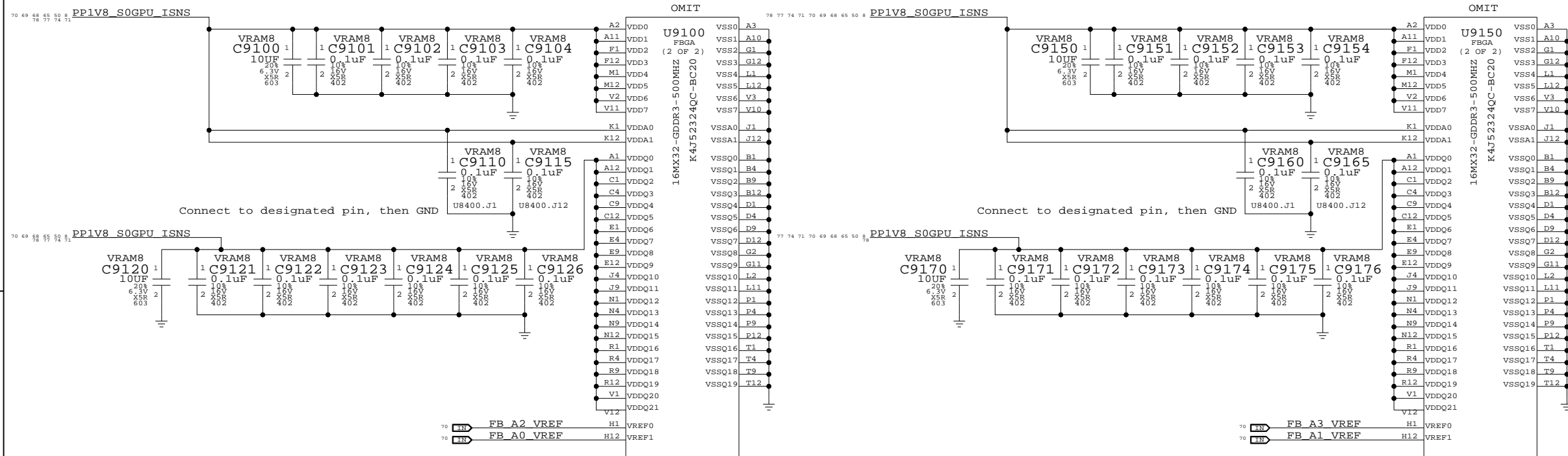
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
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SCALE		SHT	OF
NONE		76	92

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- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
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BOM options provided by this page:
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GDDR3 Frame Buffer A (Bot)

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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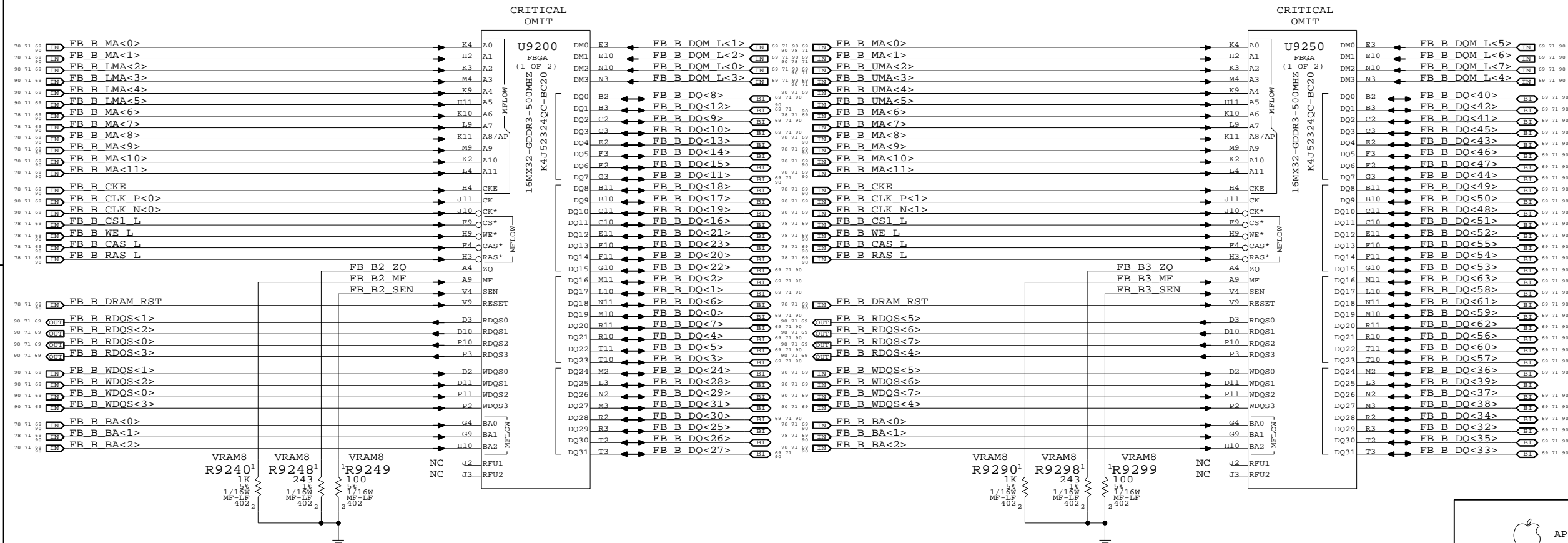
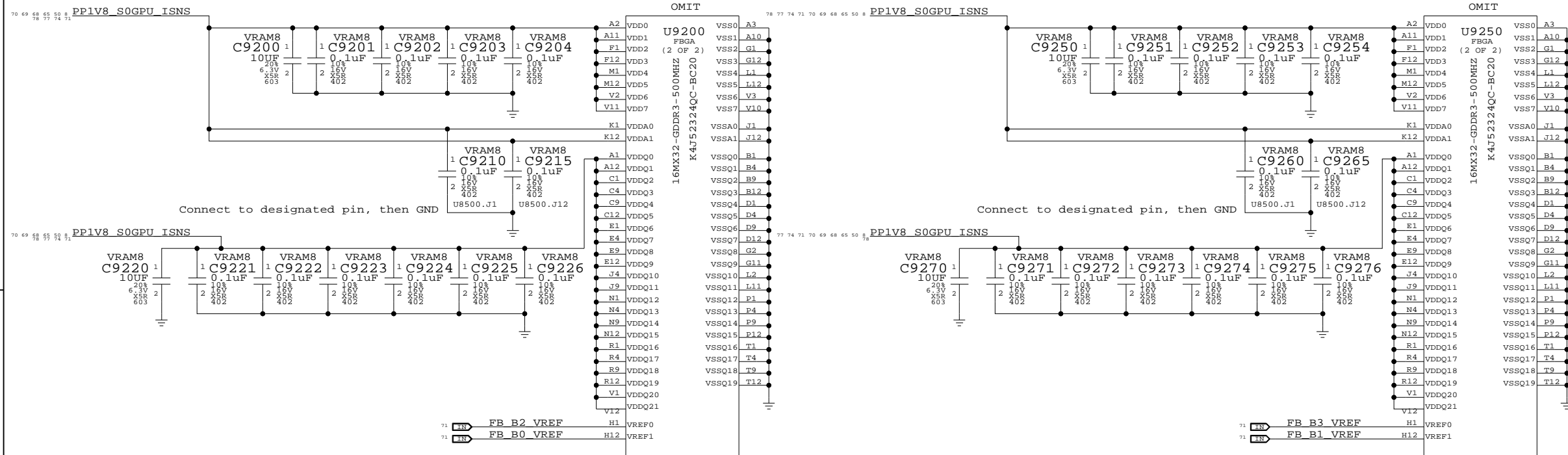
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE	SHT	OF
NONE	77	92

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
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BOM options provided by this page:
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GDDR3 Frame Buffer B (Bot)

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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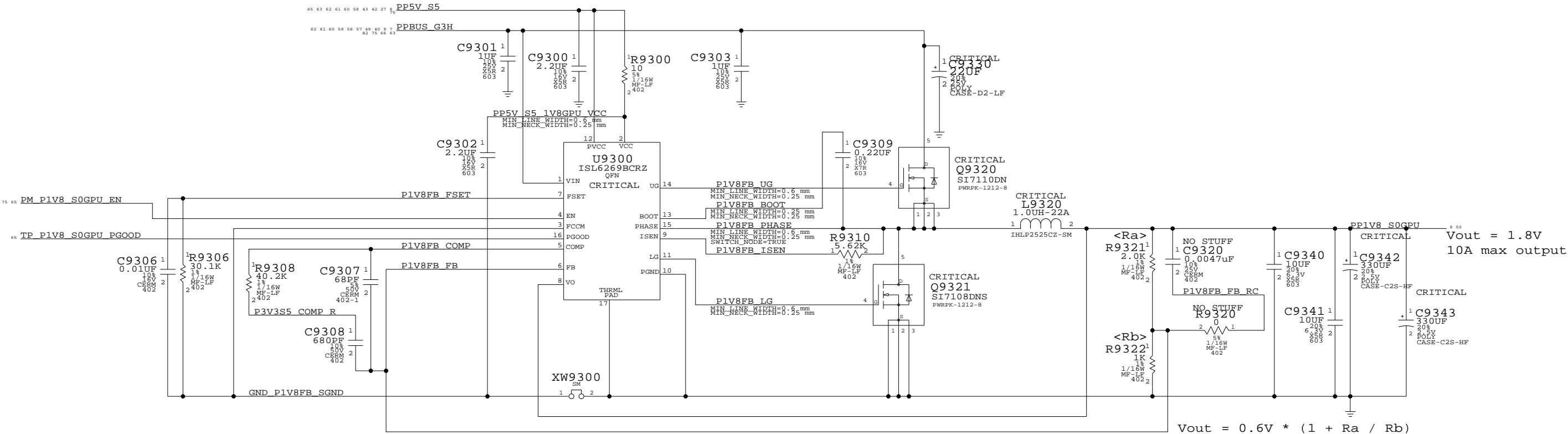


APPLE INC.

SIZE D DRAWING NUMBER 051-7431 REV. A.0.0

SCALE NONE SHT 78 OF 92

1.8V Frame Buffer Regulator



1.8V FB Power Supply

SYNC_MASTER=MASTER SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

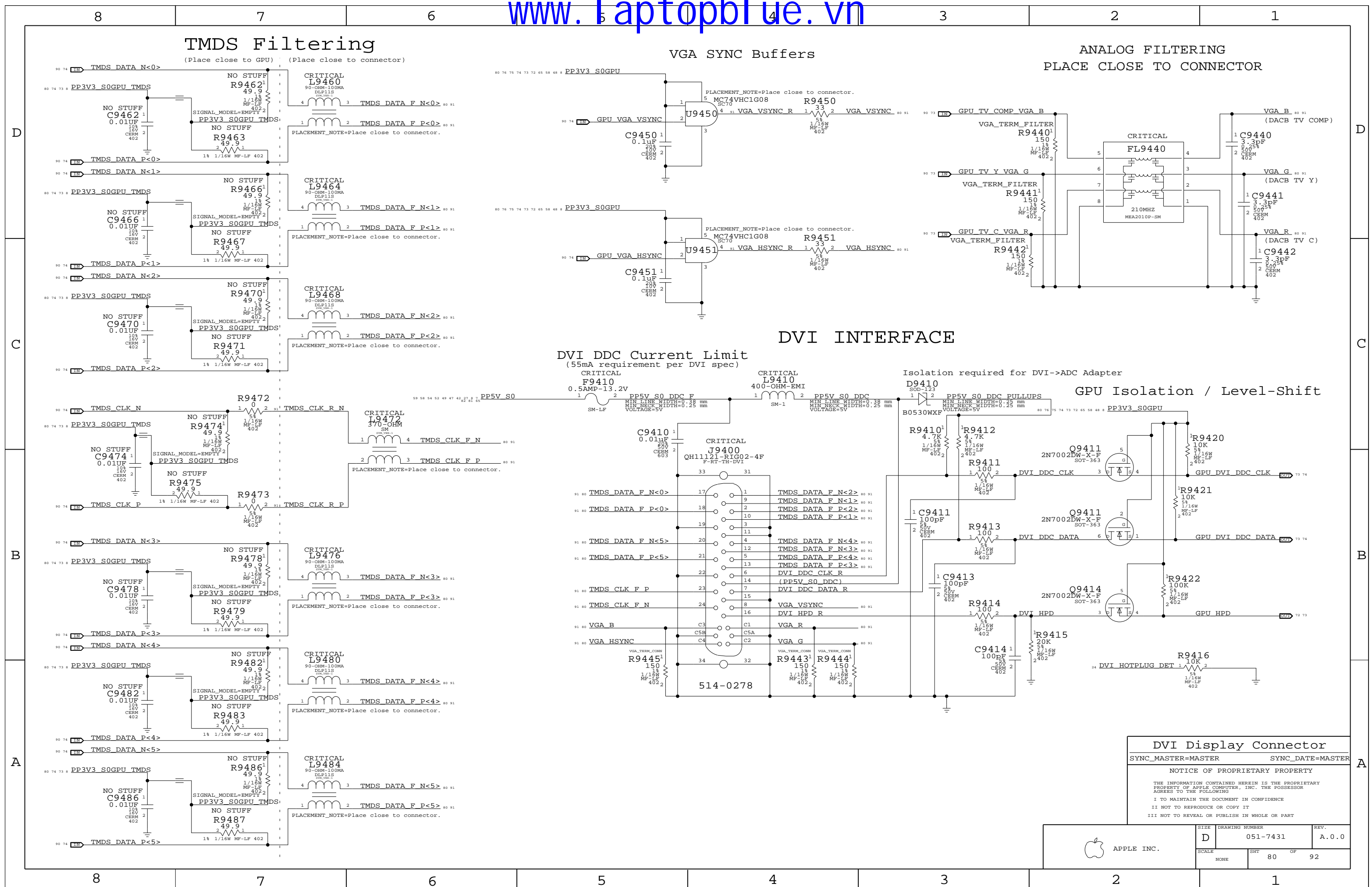
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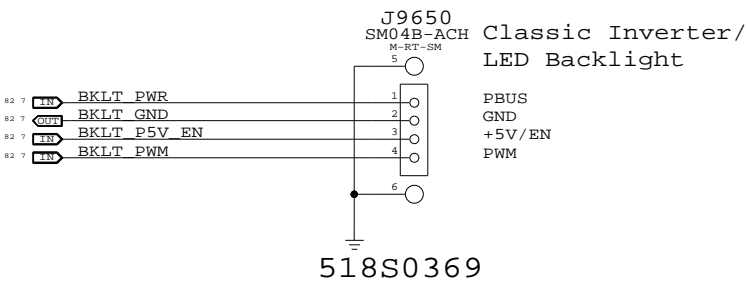
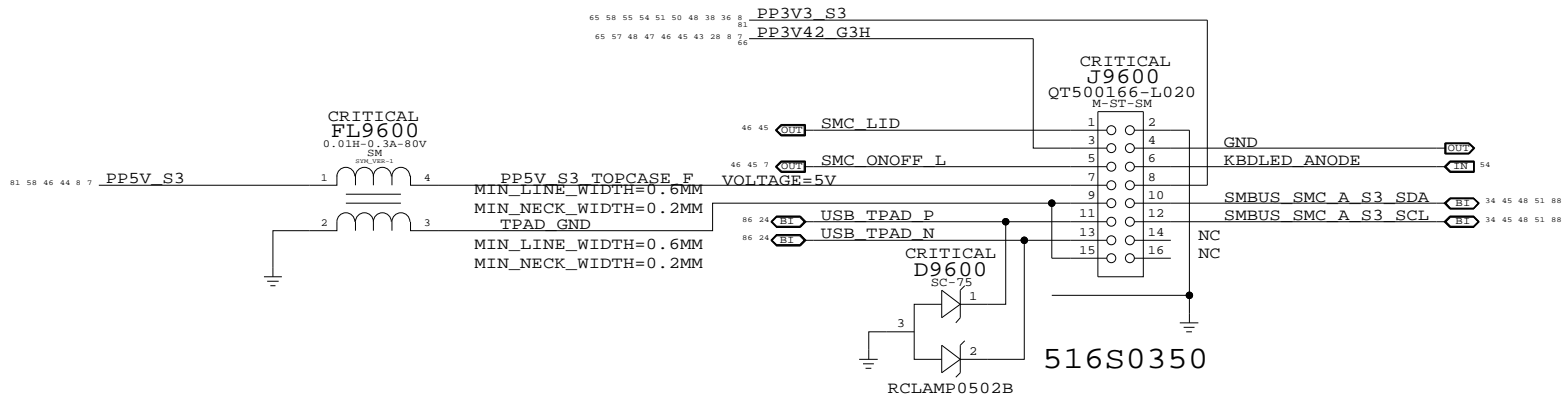
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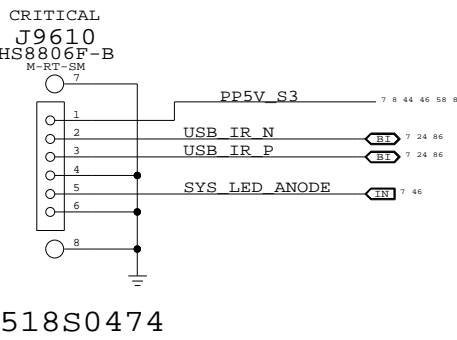
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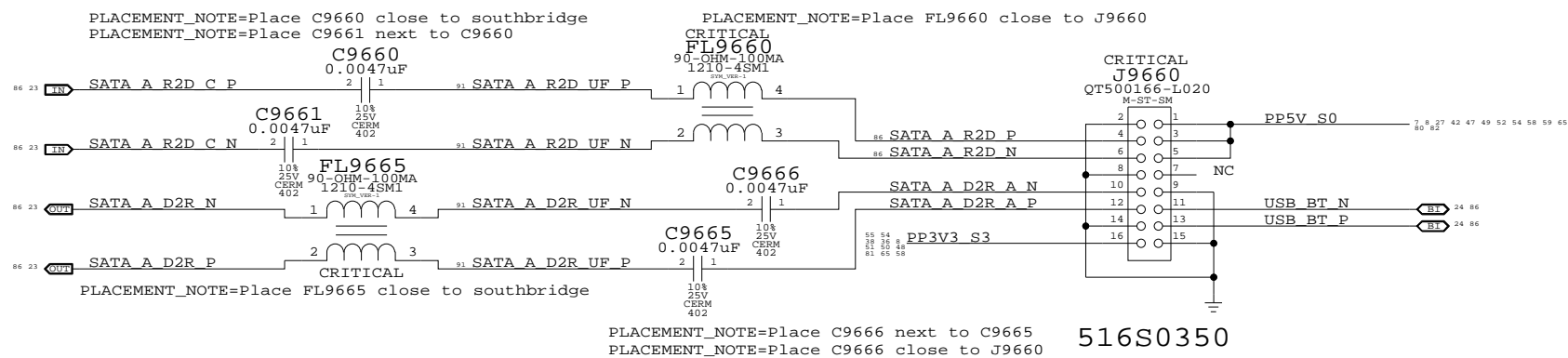
Backlight Connector




IR & Sleep LED Connector

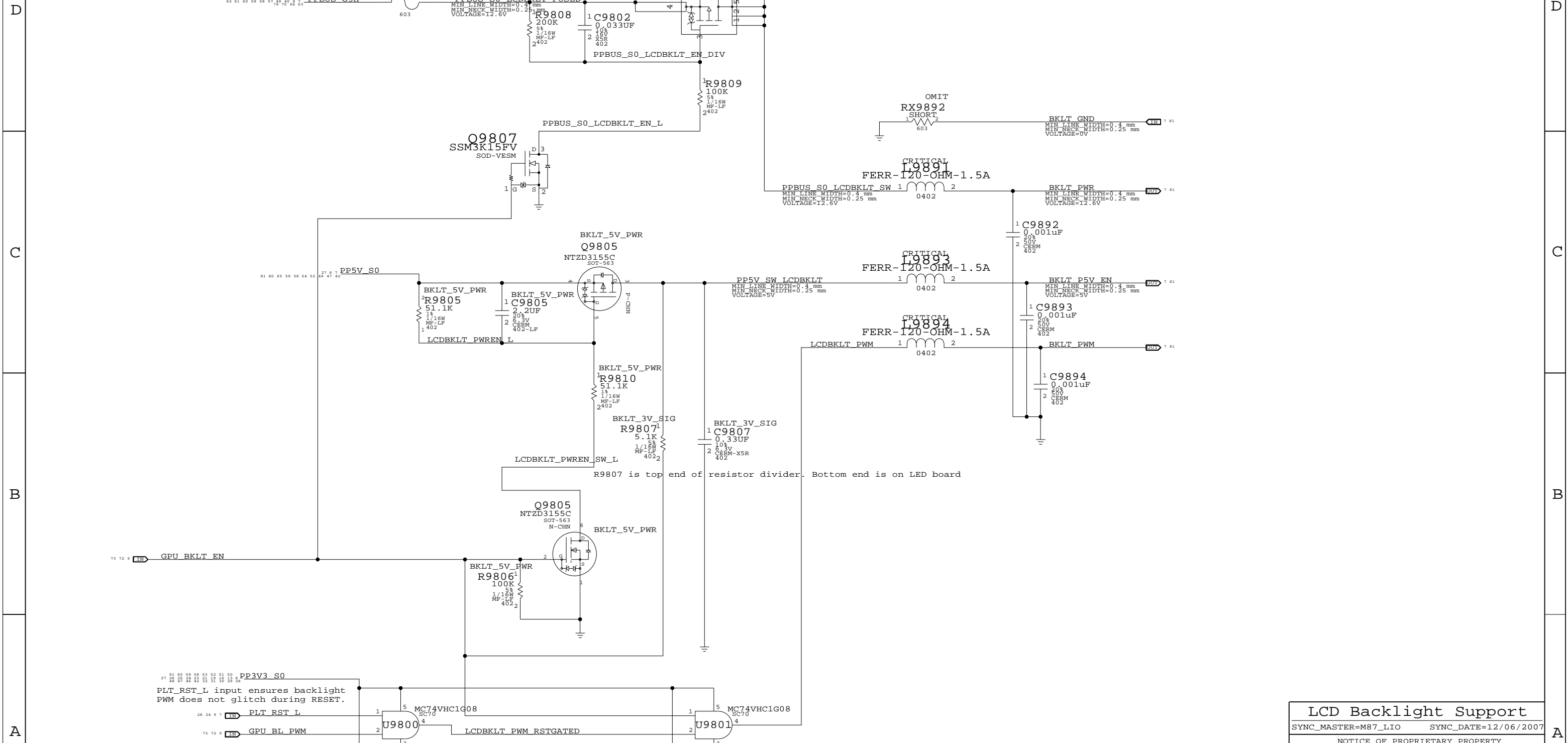


Bluetooth (M13P) & SATA HDD Flex Connector



<h1>Project Specific Connectors</h1>	
<code>SYNC_MASTER=(MASTER)</code>	<code>SYNC_DATE=(MASTER)</code>
<h2>NOTICE OF PROPRIETARY PROPERTY</h2>	
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	D	051-7431	A.0.0
	SCALE	SHT OF	
	NONE	81	92



SYNC_MASTER=M87_LIO SYNC_DATE=12/06/2007

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SIZE D	DRAWING NUMBER 051-7431	REV. A.0.0
SCALE NONE	SHT 82	OF 92

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR	*	=3:1_SPACING	?
FSB_ADDR2ADDR	*	=2:1_SPACING	?
FSB_ADSTB	*	=3:1_SPACING	?
FSB_ADDR2ADSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_COMMON	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended. Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs. Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs. DSTB complementary pairs are spaced 1:1 and routed as differential pairs.

Design Guide recommends each strobe/signal group is routed on the same layer. Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1. NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_2TO1	*	=2:1_SPACING	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

Most CPU signals with impedance requirements are 55-ohm single-ended. Some signals require 27.4-ohm single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target differential impedance.

DG recommends at least 25 mils, >50 mils preferred

CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
FSB_COMMON	FSB_55S	FSB_COMMON	FSB ADS L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB BNR L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB BPRI L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB BREQ0 L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB DBSY L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB DEFER L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB DPWR L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB DRDY L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB HIT L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB HITM L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB LOCK L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB RS L<2..0>	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB TRDY L	10 14
FSB_CPURST_L	FSB_55S	FSB_COMMON	FSB CPURST L	7 10 13 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB D L<15..0>	7 10 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB DINV L<0>	7 10 14
FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<0>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<0>	7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB D L<31..16>	7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB DINV L<1>	7 10 14
FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<1>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<1>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB D L<47..32>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB DINV L<2>	7 10 14
FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<2>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<2>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB D L<63..48>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB DINV L<3>	7 10 14
FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<3>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<3>	7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB A L<16..3>	7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB REQ L<4..0>	7 10 14
FSB_ADSTB0	FSB_55S	FSB_ADSTB	FSB ADSTB L<0>	7 10 14
FSB_ADDR_GROUP1	FSB_55S	FSB_ADDR	FSB A L<35..17>	7 10 14
FSB_ADSTB1	FSB_55S	FSB_ADSTB	FSB ADSTB L<1>	7 10 14
CPU_IERR_L	CPU_55S		CPU IERR L	10
CPU_FERR_L	CPU_55S		CPU FERR L	10 23
CPU_PROCHOT_L	CPU_55S	CPU_2TO1	CPU PROCHOT L	10 46 59
CPU_PWRGD	CPU_55S		CPU PWRGD	7 10 13 23
CPU_FROM_SB	CPU_55S		CPU INTR	10 23
CPU_FROM_SB	CPU_55S		CPU NMI	10 23
CPU_FROM_SB	CPU_55S		CPU A20M L	10 23
CPU_FROM_SB	CPU_55S		CPU DPSLP L	7 10 23
CPU_FROM_SB	CPU_55S		CPU IGNNE L	10 23
CPU_INIT_L	CPU_55S		CPU INIT L	10 23 47
CPU_FROM_SB	CPU_55S		CPU SMI L	10 23
CPU_FROM_SB	CPU_55S		CPU STPCLK L	7 10 33
PM_THRMTRIP_L	CPU_55S	CPU_2TO1	PM THRMTRIP L	10 16 23 46
FSB_CPUSLP_L	CPU_55S		FSB CPUSLP L	7 10 14
PM_DPRSLEVR	CPU_55S	CPU_2TO1	PM DPRSLPVR	7 16 25 59
(See above)	CPU_55S	CPU_2TO1	IMVP DPRSLPVR	7 59
CPU_BSEL0	CPU_55S	CPU_2TO1	CPU BSEL<0>	10 30
(See above)	CPU_55S	CPU_2TO1	NB BSEL<0>	13 16 30
CPU_BSEL1	CPU_55S	CPU_2TO1	CPU BSEL<1>	10 30
(See above)	CPU_55S	CPU_2TO1	NB BSEL<1>	13 16 30
CPU_BSEL2	CPU_55S	CPU_2TO1	CPU BSEL<2>	10 30
(See above)	CPU_55S	CPU_2TO1	NB BSEL<2>	13 16 30
CPU_DPRSTP_L	CPU_55S	CPU_2TO1	CPU DPRSTP L	7 10 16 23 59
CPU_GTLREF	CPU_55S	CPU_GTLREF	CPU GTLREF	10
CPU_COMP	CPU_55S	CPU_COMP	CPU COMP<3>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<2>	10
CPU_COMP	CPU_55S	CPU_COMP	CPU COMP<1>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<0>	10
XDP_TDI	CPU_55S	CPU_ITP	XDP TDI	10 13
XDP_TDO	CPU_55S	CPU_ITP	XDP TDO	10 13
XDP_TMS	CPU_55S	CPU_ITP	XDP TMS	10 13
XDP_TCK	CPU_55S	CPU_ITP	XDP TCK	10 13
XDP_TRST_L	CPU_55S	CPU_ITP	XDP TRST L	10 13
XDP_BPM_L	CPU_55S	CPU_ITP	XDP BPM L<4..0>	10 13
XDP_BPM_L5	CPU_55S	CPU_ITP	XDP BPM L<5>	10 13
CLK_FSB_100D	CLK_FSB		XDP CLK P	13 29 30 88
CLK_FSB_100D	CLK_FSB		XDP CLK N	13 29 30 88
(FSB_CPURST_L)	CPU_55S	CPU_ITP	XDP CPURST L	13
	CPU_55S	CPU_2TO1	CPU VID<6..0>	11 12
	CPU_55S	CPU_2TO1	IMVP6 VID<6..0>	7 12 59
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE_P	11 59
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE_N	11 59
	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN_P	59
	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN_N	59

CPU/FSB Constraints

SYNC_MASTER=T9_NAME SYNC_DATE=01/25/2007

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PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
PCIE	*	20 MIL	?
DMI	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 7.2, 9.2 & 10.5

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CRT_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
LVDS	*	20 MIL	?
CRT	*	25 MIL	?
CRT_2CRT	*	20 MIL	?
CRT_SYNC	*	25 MIL	?
CRT_SYNC2SYNC	*	20 MIL	?
TVDAC	*	25 MIL	?
TVDAC_2TVDAC	*	20 MIL	?

DG Says 40 mil spacing minimum

DG Says 30 mil spacing minimum

DG Says 40 mil spacing minimum

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT
CRT_SYNC	CRT_SYNC	*	CRT_SYNC2SYNC
TVDAC	TVDAC	*	TVDAC_2TVDAC

LVDS signals are 100-ohm +/- 20% differential impedance.
CRT & TVDAC signal single-ended impedance varies by location:
- 37.5-ohm +/- 15% from GMCH to first termination resistor.
- 50-ohm +/- 15% from first to second termination resistor.
- 55-ohm +/- 15% from second termination resistor to connector.
CRT_HSYNC/CRT_VSYNC signals are 55-ohm +/- 15% single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 8.1 - 8.3.

B

A

D

C

B

A

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
PEG_R2D	PCIE_100D	PCIE	PEG R2D P<15..0> 67
	PCIE_100D	PCIE	PEG R2D N<15..0> 67
	PCIE_100D	PCIE	PEG R2D_C P<15..0> 15 67
	PCIE_100D	PCIE	PEG R2D_C_N<15..0> 15 67
PEG_D2R	PCIE_100D	PCIE	PEG D2R P<15..0> 15 67
	PCIE_100D	PCIE	PEG D2R N<15..0> 15 67
	PCIE_100D	PCIE	PEG D2R_C P<15..0> 67
	PCIE_100D	PCIE	PEG D2R_C_N<15..0> 67
DMI_N2S	DMI_100D	DMI	DMI N2S P<3..0> 16 24
	DMI_100D	DMI	DMI N2S N<3..0> 16 24
DMI_S2N	DMI_100D	DMI	DMI S2N P<3..0> 16 24
	DMI_100D	DMI	DMI S2N N<3..0> 16 24
LVDS_A_CLK	LVDS_100D	LVDS	NC LVDS A CLKP 15 22
LVDS_A_CLK	LVDS_100D	LVDS	NC LVDS A CLKN 15 22
LVDS_A_DATA	LVDS_100D	LVDS	LVDS A DATA P<2..0> 15 22
LVDS_A_DATA	LVDS_100D	LVDS	LVDS A DATA N<2..0> 15 22
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS A DATA P<3> 15 22
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS A DATA N<3> 15 22
LVDS_B_CLK	LVDS_100D	LVDS	NC LVDS B CLKP 16 22
LVDS_B_CLK	LVDS_100D	LVDS	NC LVDS B CLKN 16 22
LVDS_B_DATA	LVDS_100D	LVDS	LVDS B DATA P<2..0> 16 22
LVDS_B_DATA	LVDS_100D	LVDS	LVDS B DATA N<2..0> 15 22
LVDS_B_DATA3	LVDS_100D	LVDS	LVDS B DATA P<3> 15 22
LVDS_B_DATA3	LVDS_100D	LVDS	LVDS B DATA N<3> 15 22
LVDS_IBG		LVDS	NC LVDS IBG 15 22
CRT_TVO_IREF		CRT	CRT TVO_IREF
CRT_RED	CRT_50S	CRT	CRT RED
CRT_GREEN	CRT_50S	CRT	CRT GREEN
CRT_BLUE	CRT_50S	CRT	CRT BLUE
CRT_SYNC	CRT_55S	CRT_SYNC	CRT HSYNC R
CRT_SYNC	CRT_55S	CRT_SYNC	CRT VSYNC R
TV_A_DAC	CRT_50S	TVDAC	TV A_DAC
TV_B_DAC	CRT_50S	TVDAC	TV B_DAC
TV_C_DAC	CRT_50S	TVDAC	TV C_DAC

NB Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

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8		7		6		5		4		3		2		1	
DDR2 Memory Bus Constraints															
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
MEM_45S		*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD							
MEM_55S		*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD							
MEM_70D		*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF							
MEM_85D		*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF							
SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT											
MEM_CLK2MEM		*	=4:1_SPACING	?											
MEM_CTRL2CTRL		*	=2:1_SPACING	?											
MEM_CTRL2MEM		*	=3:1_SPACING	?											
MEM_CMD2CMD		*	=1.5:1_SPACING	?											
MEM_CMD2MEM		*	=3:1_SPACING	?											
MEM_DATA2DATA		*	=1.5:1_SPACING	?											
MEM_DATA2MEM		*	=3:1_SPACING	?											
MEM_DQS2MEM		*	=3:1_SPACING	?											
MEM_2OTHER		*	25 MIL	?											
NET_SPACING_TYPE1		NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET											
MEM_CLK		MEM_CLK	*	MEM_CLK2MEM											
MEM_CLK		MEM_CTRL	*	MEM_CLK2MEM											
MEM_CLK		MEM_CMD	*	MEM_CLK2MEM											
MEM_CLK		MEM_DATA	*	MEM_CLK2MEM											
MEM_CLK		MEM_DQS	*	MEM_CLK2MEM											
NET_SPACING_TYPE1		NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET											
MEM_CMD		MEM_CLK	*	MEM_CMD2MEM											
MEM_CMD		MEM_CTRL	*	MEM_CMD2MEM											
MEM_CMD		MEM_CMD	*	MEM_CMD2CMD											
MEM_CMD		MEM_DATA	*	MEM_CMD2MEM											
MEM_CMD		MEM_DQS	*	MEM_CMD2MEM											
NET_SPACING_TYPE1		NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET											
MEM_CTRL		MEM_CLK	*	MEM_CTRL2MEM											
MEM_CTRL		MEM_CTRL	*	MEM_CTRL2CTRL											
MEM_CTRL		MEM_CMD	*	MEM_CTRL2MEM											
MEM_CTRL		MEM_DATA	*	MEM_CTRL2MEM											
MEM_CTRL		MEM_DQS	*	MEM_CTRL2MEM											
NET_SPACING_TYPE1		NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET											
MEM_DATA		MEM_CLK	*	MEM_DATA2MEM											
MEM_DATA		MEM_CTRL	*	MEM_DATA2MEM											
MEM_DATA		MEM_CMD	*	MEM_DATA2MEM											
MEM_DATA		MEM_DATA	*	MEM_DATA2DATA											
MEM_DATA		MEM_DQS	*	MEM_DATA2MEM											
NET_SPACING_TYPE1		NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET											
MEM_DQS		MEM_CLK	*	MEM_DQS2MEM											
MEM_DQS		MEM_CTRL	*	MEM_DQS2MEM											
MEM_DQS		MEM_CMD	*	MEM_DQS2MEM											
MEM_DQS		MEM_DATA	*	MEM_DQS2MEM											
MEM_DQS		MEM_DQS	*	MEM_DQS2MEM											
Need to support MEM_*-style wildcards!															
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2															
Memory Net Properties															
ELECTRICAL_CONSTRAINT_SET		NET_TYPE		PHYSICAL		SPACING									
MEM_A_CLK		MEM_70D	MEM_CLK	MEM_CLK		MEM CLK P<2..0>		16		31					
		MEM_70D	MEM_CLK	MEM_CLK		MEM CLK N<2..0>		16		31					
MEM_A_CNTRL		MEM_45S	MEM_CTRL	MEM_CKE<1..0>		16		31		33					
MEM_A_CNTRL		MEM_45S	MEM_CTRL	MEM CS L<1..0>		16		31		33					
MEM_A_CNTRL		MEM_45S	MEM_CTRL	MEM ODT<1..0>		16		31		33					
MEM_A_CMD		MEM_55S	MEM_CMD	MEM A A<14..0>		16		17		31		33			
MEM_A_CMD		MEM_55S	MEM_CMD	MEM A BS<2..0>		17		31		33					
MEM_A_CMD		MEM_55S	MEM_CMD	MEM A RAS L		17		31		33					
MEM_A_CMD		MEM_55S	MEM_CMD	MEM A CAS L		17		31		33					
MEM_A_CMD		MEM_55S	MEM_CMD	MEM A WE L		17		31		33					
MEM_A_DQ_BYTE0		MEM_55S	MEM_DATA	MEM A DQ<7..0>		17		31							
MEM_A_DQ_BYTE1		MEM_55S	MEM_DATA	MEM A DQ<15..8>		17		31							
MEM_A_DQ_BYTE2		MEM_55S	MEM_DATA	MEM A DQ<23..16>		17		31							
MEM_A_DQ_BYTE3		MEM_55S	MEM_DATA	MEM A DQ<31..24>		17		31							
MEM_A_DQ_BYTE4		MEM_55S	MEM_DATA	MEM A DQ<39..32>		17		31							
MEM_A_DQ_BYTE5		MEM_55S	MEM_DATA	MEM A DQ<47..40>		17		31							
MEM_A_DQ_BYTE6		MEM_55S	MEM_DATA	MEM A DQ<55..48>		17		31							
MEM_A_DQ_BYTE7		MEM_55S	MEM_DATA	MEM A DQ<63..56>		17		31							
MEM_A_DM0		MEM_55S	MEM_DATA	MEM A DM<0>		17		31							
MEM_A_DM1		MEM_55S	MEM_DATA	MEM A DM<1>		17		31							
MEM_A_DM2		MEM_55S	MEM_DATA	MEM A DM<2>		17		31							
MEM_A_DM3		MEM_55S	MEM_DATA	MEM A DM<3>		17		31							
MEM_A_DM4		MEM_55S	MEM_DATA	MEM A DM<4>		17		31							
MEM_A_DM5		MEM_55S	MEM_DATA	MEM A DM<5>		17		31							
MEM_A_DM6		MEM_55S	MEM_DATA	MEM A DM<6>		17		31							
MEM_A_DM7		MEM_55S	MEM_DATA	MEM A DM<7>		17		31							
MEM_A_DQS0		MEM_85D	MEM_DQS	MEM A DQS P<0>		17		31							
MEM_A_DQS1		MEM_85D	MEM_DQS	MEM A DQS N<0>		17		31							
MEM_A_DQS2		MEM_85D	MEM_DQS	MEM A DQS P<1>		17		31							
MEM_A_DQS3		MEM_85D	MEM_DQS	MEM A DQS N<1>		17		31							
MEM_A_DQS4		MEM_85D	MEM_DQS	MEM A DQS P<2>		17		31							
MEM_A_DQS5		MEM_85D	MEM_DQS	MEM A DQS N<2>		17		31							
MEM_A_DQS6		MEM_85D	MEM_DQS	MEM A DQS P<3>		17		31							
MEM_A_DQS7		MEM_85D	MEM_DQS	MEM A DQS N<3>		17		31							
MEM_A_DQS8		MEM_85D	MEM_DQS	MEM A DQS P<4>		17		31							
MEM_A_DQS9		MEM_85D	MEM_DQS	MEM A DQS N<4>		17		31							
MEM_A_DQS10		MEM_85D	MEM_DQS	MEM A DQS P<5>		17		31							
MEM_A_DQS11		MEM_85D	MEM_DQS	MEM A DQS N<5>		17		31							
MEM_A_DQS12		MEM_85D	MEM_DQS	MEM A DQS P<6>		17		31							
MEM_A_DQS13		MEM_85D	MEM_DQS	MEM A DQS N<6>		17		31							
MEM_A_DQS14		MEM_85D	MEM_DQS	MEM A DQS P<7>		17		31							
MEM_A_DQS15		MEM_85D	MEM_DQS	MEM A DQS N<7>		17		31							
MEM_B_CLK		MEM_70D	MEM_CLK	MEM CLK P<5..3>		16		32							
		MEM_70D	MEM_CLK	MEM CLK N<5..3>		16		32							
MEM_B_CNTRL		MEM_45S	MEM_CTRL	MEM CKE<4..3>		16		32		33					
MEM_B_CNTRL		MEM_45S	MEM_CTRL	MEM CS L<3..2>		16		32		33					
MEM_B_CNTRL		MEM_45S	MEM_CTRL	MEM ODT<3..2>		16		32		33					
MEM_B_CMD		MEM_55S	MEM_CMD	MEM B A<14..0>		16		17		32		33			
MEM_B_CMD		MEM_55S	MEM_CMD	MEM B BS<2..0>		17		32		33					
MEM_B_CMD		MEM_55S	MEM_CMD	MEM B RAS L		17		32		33					
MEM_B_CMD		MEM_55S	MEM_CMD	MEM B CAS L		17		32		33					
MEM_B_CMD		MEM_55S	MEM_CMD	MEM B WE L		17		32		33					
MEM_B_DQ_BYTE0		MEM_55S	MEM_DATA	MEM B DQ<7..0>		17		32							
MEM_B_DQ_BYTE1		MEM_55S	MEM_DATA	MEM B DQ<15..8>		17		32							
MEM_B_DQ_BYTE2		MEM_55S	MEM_DATA	MEM B DQ<23..16>		17		32							
MEM_B_DQ_BYTE3		MEM_55S	MEM_DATA	MEM B DQ<31..24>		17		32							
MEM_B_DQ_BYTE4		MEM_55S	MEM_DATA	MEM B DQ<39..32>		17		32							
MEM_B_DQ_BYTE5		MEM_55S	MEM_DATA	MEM B DQ<47..40>		17		32							
MEM_B_DQ_BYTE6		MEM_55S	MEM_DATA	MEM B DQ<55..48>		17		32							
MEM_B_DQ_BYTE7		MEM_55S	MEM_DATA	MEM B DQ<63..56>		17		32							
MEM_B_DM0		MEM_55S	MEM_DATA	MEM B DM<0>		17		32							
MEM_B_DM1		MEM_55S	MEM_DATA	MEM B DM<1>		17		32							
MEM_B_DM2		MEM_55S	MEM_DATA	MEM B DM<2>		17		32							
MEM_B_DM3		MEM_55S	MEM_DATA	MEM B DM<3>		17		32							
MEM_B_DM4		MEM_55S	MEM_DATA	MEM B DM<4>		17		32							
MEM_B_DM5		MEM_55S	MEM_DATA	MEM B DM<5>		17		32							
MEM_B_DM6		MEM_55S	MEM_DATA	MEM B DM<6>		17		32							
MEM_B_DM7		MEM_55S	MEM_DATA	MEM B DM<7>		17		32							
MEM_B_DQS0		MEM_85D	MEM_DQS	MEM B DQS P<0>		17		32							
MEM_B_DQS1		MEM_85D	MEM_DQS	MEM B DQS N<0>		17		32							
MEM_B_DQS2		MEM_85D	MEM_DQS	MEM B DQS P<1>		17		32							
MEM_B_DQS3		MEM_85D	MEM_DQS	MEM B DQS N<1>		17		32							
MEM_B_DQS4		MEM_85D	MEM_DQS	MEM B DQS P<2>		17		32							
MEM_B_DQS5		MEM_85D	MEM_DQS	MEM B DQS N<2>		17		32							
MEM_B_DQS6		MEM_85D	MEM_DQS	MEM B DQS P<3>		17		32							
MEM_B_DQS7		MEM_85D	MEM_DQS	MEM B DQS N<3>		17		32							
MEM_B_DQS8		MEM_85D	MEM_DQS	MEM B DQS P<4>		17		32							
MEM_B_DQS9		MEM_85D	MEM_DQS	MEM B DQS N<4>		17		32							
MEM_B_DQS10		MEM_85D	MEM_DQS	MEM B DQS P<5>		17		32							
MEM_B_DQS11		MEM_85D	MEM_DQS	MEM B DQS N<5>		17		32							
MEM_B_DQS12		MEM_85D	MEM_DQS	MEM B DQS P<6>		17		32							
MEM_B_DQS13		MEM_85D	MEM_DQS	MEM B DQS N<6>		17		32							
MEM_B_DQS14		MEM_85D	MEM_DQS	MEM B DQS P<7>		17		32							
MEM_B_DQS15		MEM_85D	MEM_DQS	MEM B DQS N<7>		17		32							
Memory Constraints															
SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007															
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D 051-7431 A.0.0															
SCALE NONE SHT 85 OF 92															

D

Disk Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IDE_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
IDE	*	=1.8:1_SPACING	?
SATA	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.7 & 10.9

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=1.8:1_SPACING	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_60S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	20 MIL	?
USB_2CLK	*	25 MIL	?

DG says minimum spacing 50 mils to clocks

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 10.13.2

Internal Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=3:1_SPACING	?
SPI	*	=1.8:1_SPACING	?

SOURCE: Santa Platform DG, Rev 1.0 (#21112), Section 10.17

B

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ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
IDE_PDD	IDE_55S	IDE	IDE_PDD<15..0>	23 42
IDE_PDA	IDE_55S	IDE	IDE_PDA<2..0>	23 42
IDE_PDCS	IDE_55S	IDE	IDE_PDCS1_L	23 42
IDE_PDCS	IDE_55S	IDE	IDE_PDCS3_L	23 42
IDE_CNTL	IDE_55S	IDE	IDE_PDIOW_L	23 42
IDE_PDIOR_L	IDE_55S	IDE	IDE_PDIOR_L	23 42
IDE_CNTL	IDE_55S	IDE	IDE_PDDACK_L	23 42
IDE_CNTL	IDE_55S	IDE	IDE_PDDREO	23 42
IDE_PDIORDY	IDE_55S	IDE	IDE_PDIORDY	23 42
IDE_IRQ14	IDE_55S	IDE	IDE_IRQ14	23 42
IDE_RST_L	IDE_55S	IDE	ODD_RST_5VTOL_L	24 42
SATA_A_R2D	SATA_100D	SATA	SATA_A_R2D_C_P	23 81
SATA_100D	SATA		SATA_A_R2D_C_N	23 81
SATA_100D	SATA		SATA_A_R2D_P	81
SATA_100D	SATA		SATA_A_R2D_N	81
SATA_A_D2R	SATA_100D	SATA	SATA_A_D2R_P	23 81
SATA_100D	SATA		SATA_A_D2R_N	23 81
SATA_100D	SATA		SATA_A_D2R_C_P	
SATA_100D	SATA		SATA_A_D2R_C_N	
SATA_B_R2D	SATA_100D	SATA	TP_SATA_B_R2DP	23 42
SATA_100D	SATA		TP_SATA_B_R2DN	23 42
SATA_100D	SATA		SATA_B_R2D_P	
SATA_100D	SATA		SATA_B_R2D_N	
SATA_B_D2R	SATA_100D	SATA	TP_SATA_B_D2RP	23 42
SATA_100D	SATA		TP_SATA_B_D2RN	23 42
SATA_100D	SATA		SATA_B_D2R_C_P	
SATA_100D	SATA		SATA_B_D2R_C_N	
SATA_C_R2D	SATA_100D	SATA	TP_SATA_C_R2DP	23 42
SATA_100D	SATA		TP_SATA_C_R2DN	23 42
SATA_100D	SATA		SATA_C_R2D_P	
SATA_100D	SATA		SATA_C_R2D_N	
SATA_C_D2R	SATA_100D	SATA	TP_SATA_C_D2RP	23 42
SATA_100D	SATA		TP_SATA_C_D2RN	23 42
SATA_100D	SATA		SATA_C_D2R_C_P	
SATA_100D	SATA		SATA_C_D2R_C_N	
SATA_RBIAS	SATA_55S		SATA_RBIAS	23 42
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	23 34
HDA_55S	HDA		HDA_BIT_CLK_R	23
HDA_SYNC	HDA_55S	HDA	HDA_SYNC	23 34
HDA_55S	HDA		HDA_SYNC_R	23
HDA_RST_L	HDA_55S	HDA	HDA_RST_L	23 34
HDA_55S	HDA		HDA_RST_L_R	23
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0	23 34
HDA_55S	HDA		HDA_SDIN_CODEC	
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT	23 34
HDA_55S	HDA		HDA_SDOUT_R	23
USB_EXT_A	USB_90D	USB	USB_EXT_A_P	24 43
USB_90D	USB		USB_EXT_A_N	24 43
USB_90D	USB		USB_EXT_A_MUXED_P	
USB_90D	USB		USB_EXT_A_MUXED_N	
USB_MINI	USB_90D	USB	USB_MINI_P	24 34
USB_90D	USB		USB_MINI_N	24 34
USB_EXTD	USB_90D	USB	TP_USB_EXTDP	9 24
USB_90D	USB		TP_USB_EXTDN	9 24
USB_CAMERA	USB_90D	USB	USB_CAMERA_P	24 44
USB_90D	USB		USB_CAMERA_N	24 44
USB_BT	USB_90D	USB	USB_BT_P	24 81
USB_90D	USB		USB_BT_N	24 81
USB_TPAD	USB_90D	USB	USB_TPAD_P	24 81
USB_90D	USB		USB_TPAD_N	24 81
USB_IR	USB_90D	USB	USB_IR_P	7 24 81
USB_90D	USB		USB_IR_N	7 24 81
USB_EXTB	USB_90D	USB	USB_EXTB_P	24 34
USB_90D	USB		USB_EXTB_N	24 34
USB_EXCARD	USB_90D	USB	USB_EXCARD_P	24 34
USB_90D	USB		USB_EXCARD_N	24 34
USB_EXTC	USB_90D	USB	USB_EXTC_P	24 34
USB_90D	USB		USB_EXTC_N	24 34
USB_RBIAS	USB_60S		USB_RBIAS	24
SMB_SB_SCL	SMB_55S	SMB	SMBUS_SB_SCL	25 29 31 32 34 48
SMB_SB_SDA	SMB_55S	SMB	SMBUS_SB_SDA	25 29 31 32 34 48
SMB_SB_ME_SCL	SMB_55S	SMB	SMBUS_SB_ME_SCL	25 48
SMB_SB_ME_SDA	SMB_55S	SMB	SMBUS_SB_ME_SDA	25 48
SPI_SCLK	SPI_55S	SPI	SPI_SCLK_R	24 56
SPI_55S	SPI		SPI_SCLK	56
SPI_55S	SPI		SPI_A_SCLK_R	
SPI_55S	SPI		SPI_B_SCLK_R	
SPI_SI	SPI_55S	SPI	SPI_SI_R	24 56
SPI_55S	SPI		SPI_SI	
SPI_55S	SPI		SPI_A_SI_R	56
SPI_55S	SPI		SPI_B_SI_R	
SPI_SO	SPI_55S	SPI	SPI_SO	24 56
SPI_55S	SPI		SPI_A_SO_R	56
SPI_55S	SPI		SPI_B_SO	
SPI_55S	SPI		SPI_B_SO_R	
SPI_CE_L0	SPI_55S	SPI	SPI_CE_R_L<0>	24 56
SPI_55S	SPI		SPI_CE_L<0>	56
SPI_CE_L1	SPI_55S	SPI	SPI_CE_R_L<1>	
SPI_55S	SPI		SPI_CE_L<1>	

SB Constraints (1 of 2)

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

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PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=2:1_SPACING	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.18.1 & 10.19

Controller Link (AMT) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLINK_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLINK_12MIL	*	=STANDARD	12 MILS	5 MILS	300 MILS	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLINK	*	=1.8:1_SPACING	?
CLINK_VREF	*	12 MILS	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

Ethernet (Yukon) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MILS	?

SOURCE: Based on Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
PCI_AD	PCI_55S	PCI	PCI AD<18..0> 24 38
PCI_AD19	PCI_55S	PCI	PCI AD<19> 24 38
PCI_AD20	PCI_55S	PCI	PCI AD<20> 24 38
PCI_AD	PCI_55S	PCI	PCI AD<31..21> 24 38
PCI_AD	PCI_55S	PCI	PCI PAR 24 38
PCI_C_BE_L	PCI_55S	PCI	PCI C_BE_L<3..0> 24 38
PCI_CNTRL	PCI_55S	PCI	PCI IRDY_L 24 38
PCI_CNTRL	PCI_55S	PCI	PCI DEVSEL_L 24 38
PCI_CNTRL	PCI_55S	PCI	PCI PERR_L 24 38
PCI_LOCK_L	PCI_55S	PCI	PCI LOCK_L 24
PCI_CNTRL	PCI_55S	PCI	PCI SERR_L 24 38
PCI_CNTRL	PCI_55S	PCI	PCI STOP_L 24 38
PCI_CNTRL	PCI_55S	PCI	PCI TRDY_L 24 38
PCI_CNTRL	PCI_55S	PCI	PCI FRAME_L 24 38
PCI_FW_REQ_L	PCI_55S	PCI	PCI FW_REQ_L 24 38
PCI_FW_GNT_L	PCI_55S	PCI	PCI FW_GNT_L 7 24 38 47
PCI_REQ1_L	PCI_55S	PCI	PCI REQ1_L 24
PCI_GNT1_L	PCI_55S	PCI	PCI GNT1_L 24
PCI_REQ2_L	PCI_55S	PCI	PCI REQ2_L 24
PCI_GNT2_L	PCI_55S	PCI	PCI GNT2_L 24
INT_PIRQA_L	PCI_55S	PCI	INT PIRQA_L 24
INT_PIRQB_L	PCI_55S	PCI	INT PIRQB_L 24
INT_PIRQC_L	PCI_55S	PCI	INT PIRQC_L 24
INT_PIRQD_L	PCI_55S	PCI	INT PIRQD_L 24 38
INT_PIRQF_L	PCI_55S	PCI	INT PIRQF_L 24
PCIE_A_R2D	PCIE_100D	PCIE	PCIE A_R2D_C_P 24
PCIE_A_R2D	PCIE_100D	PCIE	PCIE A_R2D_C_N 24
PCIE_A_D2R	PCIE_100D	PCIE	PCIE A_D2R_P 24
PCIE_A_D2R	PCIE_100D	PCIE	PCIE A_D2R_N 24
PCIE_B_R2D	PCIE_100D	PCIE	PCIE B_R2D_C_P 24
PCIE_B_R2D	PCIE_100D	PCIE	PCIE B_R2D_C_N 24
PCIE_B_D2R	PCIE_100D	PCIE	PCIE B_D2R_P 24
PCIE_B_D2R	PCIE_100D	PCIE	PCIE B_D2R_N 24
PCIE_EXCARD_R2D	PCIE_100D	PCIE	PCIE EXCARD_R2D_C_P 24 34
PCIE_EXCARD_R2D	PCIE_100D	PCIE	PCIE EXCARD_R2D_C_N 24 34
PCIE_EXCARD_D2R	PCIE_100D	PCIE	PCIE EXCARD_D2R_P 24 34
PCIE_EXCARD_D2R	PCIE_100D	PCIE	PCIE EXCARD_D2R_N 24 34
PCIE_FW_R2D	PCIE_100D	PCIE	PCIE FW_R2D_C_P 24
PCIE_FW_R2D	PCIE_100D	PCIE	PCIE FW_R2D_C_N 24
PCIE_FW_D2R	PCIE_100D	PCIE	PCIE FW_D2R_P 24
PCIE_FW_D2R	PCIE_100D	PCIE	PCIE FW_D2R_N 24
PCIE_MINI_R2D	PCIE_100D	PCIE	PCIE MINI_R2D_C_P 24 34
PCIE_MINI_R2D	PCIE_100D	PCIE	PCIE MINI_R2D_C_N 24 34
PCIE_MINI_D2R	PCIE_100D	PCIE	PCIE MINI_D2R_P 24 34
PCIE_MINI_D2R	PCIE_100D	PCIE	PCIE MINI_D2R_N 24 34
GLAN_COMP			GLAN COMP 23
CLINK_NB	CLINK_55S	CLINK	CLINK_NB_CLK 16 25
CLINK_NB	CLINK_55S	CLINK	CLINK_NB_DATA 16 25
CLINK_NB_RESET_L	CLINK_55S	CLINK	CLINK_NB_RESET_L 16 25
CLINK_WLAN	CLINK_55S	CLINK	CLINK_WLAN_CLK 16
CLINK_WLAN	CLINK_55S	CLINK	CLINK_WLAN_DATA 16
CLINK_WLAN_RESET_L	CLINK_55S	CLINK	CLINK_WLAN_RESET_L 16
NB_CLINK_VREF	CLINK_12MIL	CLINK_VREF	NB_CLINK_VREF 25
SB_CLINK_VREF0	CLINK_12MIL	CLINK_VREF	SB_CLINK_VREF0 25
SB_CLINK_VREF1	CLINK_12MIL	CLINK_VREF	SB_CLINK_VREF1 25
PCIE_ENET_R2D	PCIE_100D	PCIE	PCIE ENET_R2D_C_P 24 35
PCIE_ENET_R2D	PCIE_100D	PCIE	PCIE ENET_R2D_C_N 24 35
PCIE_ENET_R2D	PCIE_100D	PCIE	PCIE ENET_R2D_P 35
PCIE_ENET_R2D	PCIE_100D	PCIE	PCIE ENET_R2D_N 35
PCIE_ENET_D2R	PCIE_100D	PCIE	PCIE ENET_D2R_P 24 35
PCIE_ENET_D2R	PCIE_100D	PCIE	PCIE ENET_D2R_N 24 35
PCIE_ENET_D2R	PCIE_100D	PCIE	PCIE ENET_D2R_C_P 35
PCIE_ENET_D2R	PCIE_100D	PCIE	PCIE ENET_D2R_C_N 35
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI P<0> 35 37
ENET_100D	ENET_100D	ENET_MDI	ENET MDI N<0> 35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI P<1> 35 37
ENET_100D	ENET_100D	ENET_MDI	ENET MDI N<1> 35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI P<2> 35 37
ENET_100D	ENET_100D	ENET_MDI	ENET MDI N<2> 35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI P<3> 35 37
ENET_100D	ENET_100D	ENET_MDI	ENET MDI N<3> 35 37

SB Constraints (2 of 2)

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Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	25 MIL	?
CLK_PCIE	*	20 MIL	?
CLK_MED	*	20 MIL	?
CLK_SLOW	*	10 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 14.1 - 14.6

Clock Net Properties

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
CK505_CPUH	CLK_FSB_100D	CLK_FSB	FSB CLK CPU P	7 10 29 30 88
CK505_CPU	CLK_FSB_100D	CLK_FSB	FSB CLK CPU N	7 10 29 30 88
CK505_NB	CLK_FSB_100D	CLK_FSB	FSB CLK NB P	7 14 29 30 88
CK505_NB	CLK_FSB_100D	CLK_FSB	FSB CLK NB N	7 14 29 30 88
CK505_ITP	CLK_FSB_100D	CLK_FSB	XDP CLK P	13 29 30 83 88
CK505_ITP	CLK_FSB_100D	CLK_FSB	XDP CLK N	13 29 30 83 88
CK505_PCIF0	CLK_MED_55S	CLK_MED	CK505 PCIF0 CLK ITPEN	29 30
CK505_PCIF1	CLK_MED_55S	CLK_MED	CK505 PCIF1 CLK	29 30
CK505_PCI1	CLK_MED_55S	CLK_MED	CK505 PCI1 CLK	29 30
CK505_PCI2	CLK_MED_55S	CLK_MED	TP CK505 PCI2 CLK	29 30
CK505_PCI3	CLK_MED_55S	CLK_MED	CK505 PCI3 CLK	29 30
CK505_PCI4	CLK_MED_55S	CLK_MED	TP CK505 PCI4 CLK	29 30
CK505_PCI5	CLK_MED_55S	CLK_MED	CK505 PCI5 CLK FCTSEL	29 30
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505 48M FSA	29 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505 REF0 FSC	29 30
CK505_DOT96	CLK_PCIE_100D	CLK_PCIE	CK505 CLK27M	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505 CLK27M SS	29 30
CK505_LVDS	CLK_PCIE_100D	CLK_PCIE	TP NB CLK100M DPPLLSS P	29 30
	CLK_PCIE_100D	CLK_PCIE	TP NB CLK100M DPPLLSS N	29 30
CK505_SRC1	CLK_PCIE_100D	CLK_PCIE	PEG CLK100M GPU P	9 29 30 67 88
	CLK_PCIE_100D	CLK_PCIE	PEG CLK100M GPU N	9 29 30 67 88
CK505_SRC2	CLK_PCIE_100D	CLK_PCIE	SB CLK100M DMI P	24 29 30 88
	CLK_PCIE_100D	CLK_PCIE	SB CLK100M DMI N	24 29 30 88
CK505_SRC3	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M EXCARD P	29 30 34 88
	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M EXCARD N	29 30 34 88
CK505_SRC4	CLK_PCIE_100D	CLK_PCIE	SB CLK100M SATA P	23 29 30 88
	CLK_PCIE_100D	CLK_PCIE	SB CLK100M SATA N	23 29 30 88
CK505_SRC5	CLK_PCIE_100D	CLK_PCIE	NB CLK100M PCIE P	7 16 29 30 88
	CLK_PCIE_100D	CLK_PCIE	NB CLK100M PCIE N	7 16 29 30 88
CK505_SRC6	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M MINI P	29 30 34 88
	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M MINI N	29 30 34 88
CK505_SRC7	CLK_PCIE_100D	CLK_PCIE	TP PCIE CLK100M SRC7P	29 30
	CLK_PCIE_100D	CLK_PCIE	TP PCIE CLK100M SRC7N	29 30
CK505_SRC8	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M ENET P	29 30 35 88
	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M ENET N	29 30 35 88
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB CLK CPU P	7 10 29 30 88
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB CLK CPU N	7 10 29 30 88
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB CLK NB P	7 14 29 30 88
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB CLK NB N	7 14 29 30 88
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP CLK P	13 29 30 83 88
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP CLK N	13 29 30 83 88
(CK505_PCIF0)	CLK_MED_55S	CLK_MED	PCI CLK33M LPCPLUS	7 30 47
(CK505_PCIF1)	CLK_MED_55S	CLK_MED	PCI CLK33M SB	24 30
(CK505_PCI1)	CLK_MED_55S	CLK_MED	PCI CLK33M FW	30 38
(CK505_PCI2)	CLK_MED_55S	CLK_MED	PCI CLK33M TPM	
(CK505_PCI3)	CLK_MED_55S	CLK_MED	PCI CLK33M SMC	30 45
			CK505 PCI4 is project-specific	
			CK505 PCI5 is project-specific	
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	SB CLK48M USBCTLR	25 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	SB CLK14P3M TIMER	25 30
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505 FSA	30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505 FSC	30
(CK505_DOT96)	CRT_50S	GND	NB CLK96M DOT P	
(CK505_DOT96)	CRT_50S	GND	NB CLK96M DOT N	
(CK505_LVDS)	CRT_50S	GND	NB CLK100M DPPLLSS P	
(CK505_LVDS)	CRT_50S	GND	NB CLK100M DPPLLSS N	
CK505_SRC1	CLK_PCIE_100D	CLK_PCIE	PEG CLK100M GPU P	9 29 30 67 88
CK505_SRC1	CLK_PCIE_100D	CLK_PCIE	PEG CLK100M GPU N	9 29 30 67 88
CK505_SRC2	CLK_PCIE_100D	CLK_PCIE	SB CLK100M DMI P	24 29 30 88
CK505_SRC2	CLK_PCIE_100D	CLK_PCIE	SB CLK100M DMI N	24 29 30 88
CK505_SRC3	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M EXCARD P	29 30 34 88
CK505_SRC3	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M EXCARD N	29 30 34 88
CK505_SRC4	CLK_PCIE_100D	CLK_PCIE	SB CLK100M SATA P	23 29 30 88
CK505_SRC4	CLK_PCIE_100D	CLK_PCIE	SB CLK100M SATA N	23 29 30 88
CK505_SRC5	CLK_PCIE_100D	CLK_PCIE	NB CLK100M PCIE P	7 16 29 30 88
CK505_SRC5	CLK_PCIE_100D	CLK_PCIE	NB CLK100M PCIE N	7 16 29 30 88
CK505_SRC6	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M MINI P	29 30 34 88
CK505_SRC6	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M MINI N	29 30 34 88
			CK505 SRC7 is project-specific	
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M ENET P	29 30 35 88
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M ENET N	29 30 35 88

SMC SMBus Net Properties

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
SMBUS_SMC_A_S3_SCL	SMB_55S	SMB	SMBUS SMC A S3_SCL	34 45 48 51 81
SMBUS_SMC_A_S3_SDA	SMB_55S	SMB	SMBUS SMC A S3_SDA	34 45 48 51 81
SMBUS_SMC_B_S0_SCL	SMB_55S	SMB	SMBUS SMC B S0_SCL	45 48
SMBUS_SMC_B_S0_SDA	SMB_55S	SMB	SMBUS SMC B S0_SDA	45 48
SMBUS_SMC_0_S0_SCL	SMB_55S	SMB	SMBUS SMC 0 S0_SCL	45 48 51 74
SMBUS_SMC_0_S0_SDA	SMB_55S	SMB	SMBUS SMC 0 S0_SDA	45 48 51 74
SMBUS_SMC_BSA_SCL	SMB_55S	SMB	SMBUS SMC BSA_SCL	7 45 48 57
SMBUS_SMC_BSA_SDA	SMB_55S	SMB	SMBUS SMC BSA_SDA	7 45 48 57
SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	SMBUS SMC MGMT_SCL	45 48 55
SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	SMBUS SMC MGMT_SDA	45 48 55

Clock & SMC Constraints

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW	*	=2:1_SPACING	?
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE		
	PHYSICAL	SPACING	
<div></div> FW_D_CTL	FW_55S	FW	FW LINK<7..0>
<div></div> FW_D_CTL	FW_55S	FW	FW CTL<1..0>
<div></div> FW_L_CLK	CLK_MED_55S	CLK_MED	CLKFW LINK_LCLK
<div></div> FW_L_CLK	CLK_MED_55S	CLK_MED	CLKFW PHY_LCLK 38 39
<div></div> FW_P_CLK	CLK_MED_55S	CLK_MED	CLKFW LINK_PCLK 38 39
<div></div> FW_P_CLK	CLK_MED_55S	CLK_MED	CLKFW PHY_PCLK
<div></div> FW_LKON	FW_55S	FW	FW LKON
<div></div> FW_LKON	FW_55S	FW	FW LKON_R
<div></div> FW_LPS	FW_55S	FW	FW LPS 38 39
<div></div> FW_LREQ	FW_55S	FW	FW LREQ 38 39
<div></div> FW_PINT	FW_55S	FW	FW PINT 38 39
<div></div> FWPHY_CLK98P304M_XI	CLK_MED_55S	CLK_MED	CLK98P304M_FW_XI_R
<div></div> FWPHY_CLK98P304M_XI	CLK_MED_55S	CLK_MED	CLK98P304M_FW_XI
<div></div> FW_0_TPA	FW_110D	FW_TP	FW PORT0_TPA_P 39 41
<div></div> FW_0_TPA	FW_110D	FW_TP	FW PORT0_TPA_N 39 41
<div></div> FW_0_TPB	FW_110D	FW_TP	FW PORT0_TPB_P 39 41
<div></div> FW_0_TPB	FW_110D	FW_TP	FW PORT0_TPB_N 39 41
<div></div> FW_1_TPA	FW_110D	FW_TP	FW PORT1_TPA_P 39 41
<div></div> FW_1_TPA	FW_110D	FW_TP	FW PORT1_TPA_N 39 41
<div></div> FW_1_TPB	FW_110D	FW_TP	FW PORT1_TPB_P 39 41
<div></div> FW_1_TPB	FW_110D	FW_TP	FW PORT1_TPB_N 39 41
Port 2 Not Used			

FireWire Constraints

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	8	7	6	5	4	3	2	1
	M75 Board-Specific Spacing & Physical Constraints							
	BOARD LAYERS				BOARD AREAS		BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
	TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM				NO_TYPE, BGA		MM	15.5.1
D	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	DEFAULT	*	Y	=55_OHM_SE	=55_OHM_SE	30 MM	0 MM	0 MM
	STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT
C	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	55_OHM_SE	TOP, BOTTOM	Y	0.100 MM	0.100 MM			
	55_OHM_SE	ISL2, ISL11	Y	0.250 MM	0.076 MM			
B	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	50_OHM_SE	TOP, BOTTOM	Y	0.125 MM	0.125 MM			
	50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD
A	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	46_OHM_SE	TOP, BOTTOM	Y	0.126 MM	0.126 MM			
	46_OHM_SE	*	Y	0.100 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD
D	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	45_OHM_SE	TOP, BOTTOM	Y	0.150 MM	0.150 MM			
	45_OHM_SE	*	Y	0.105 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD
C	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	40_OHM_SE	TOP, BOTTOM	Y	0.185 MM	0.185 MM			
	40_OHM_SE	*	Y	0.131 MM	0.131 MM	=STANDARD	=STANDARD	=STANDARD
B	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	27P4_OHM_SE	TOP, BOTTOM	Y	0.335 MM	0.335 MM			
	27P4_OHM_SE	*	Y	0.240 MM	0.240 MM	=STANDARD	=STANDARD	=STANDARD
A	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
	70_OHM_DIFF	ISL3, ISL4	Y	0.149 MM	0.149 MM		0.125 MM	0.125 MM
D	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
	80_OHM_DIFF	ISL3, ISL4	Y	0.115 MM	0.115 MM		0.125 MM	0.125 MM
C	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	80_OHM_DIFF	ISL9, ISL10	Y	0.115 MM	0.115 MM		0.125 MM	0.125 MM
	80_OHM_DIFF	ISL2, ISL11	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM
B	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	85_OHM_DIFF	TOP, BOTTOM	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM
	85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
A	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	85_OHM_DIFF	ISL3, ISL4	Y	0.101 MM	0.101 MM		0.125 MM	0.125 MM
	85_OHM_DIFF	ISL9, ISL10	Y	0.101 MM	0.101 MM		0.125 MM	0.125 MM
D	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	85_OHM_DIFF	ISL2, ISL11	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM
	85_OHM_DIFF	TOP, BOTTOM	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM
C	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
	90_OHM_DIFF	ISL3, ISL4	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
B	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	90_OHM_DIFF	ISL9, ISL10	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
	90_OHM_DIFF	ISL2, ISL11	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM
A	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	90_OHM_DIFF	TOP, BOTTOM	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM
	90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
D	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	100_OHM_DIFF	ISL3, ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
	100_OHM_DIFF	ISL9, ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
C	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	100_OHM_DIFF	ISL2, ISL11	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM
	100_OHM_DIFF	TOP, BOTTOM	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM
B	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	110_OHM_DIFF	ISL3, ISL4	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
	110_OHM_DIFF	ISL9, ISL10	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
A	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	110_OHM_DIFF	ISL2, ISL11	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM
	110_OHM_DIFF	TOP, BOTTOM	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM
	8	7	6	5	4	3	2	1

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_MED	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

PCB Rule Definitions

SYNC_MASTER=M87_MLB

SYNC_DATE=10/03/2007


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