1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
C	0000734528	PRODUCTION RELEASED	2009-06-04

K24 MLB SCHEMATIC

6/12/2009

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60	72	5V/3.3V SUPPLY	RAYMOND	02/08/2008
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67	79	POWER FETS	YUAN.MA	12/11/2008
68	90	LVDS CONNECTOR	NMARTIN	04/04/2008
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71	97	LCD BACKLIGHT DRIVER	KIRAN	12/05/2008
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Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7898	1	SCHEM,MLB,K24	SCH	CRITICAL	
820-2530	1	PCBF,MLB,K24	PCB	CRITICAL	

DRAWING TITLE: SCHEM,MLB,K24

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REVISION: C.0.0

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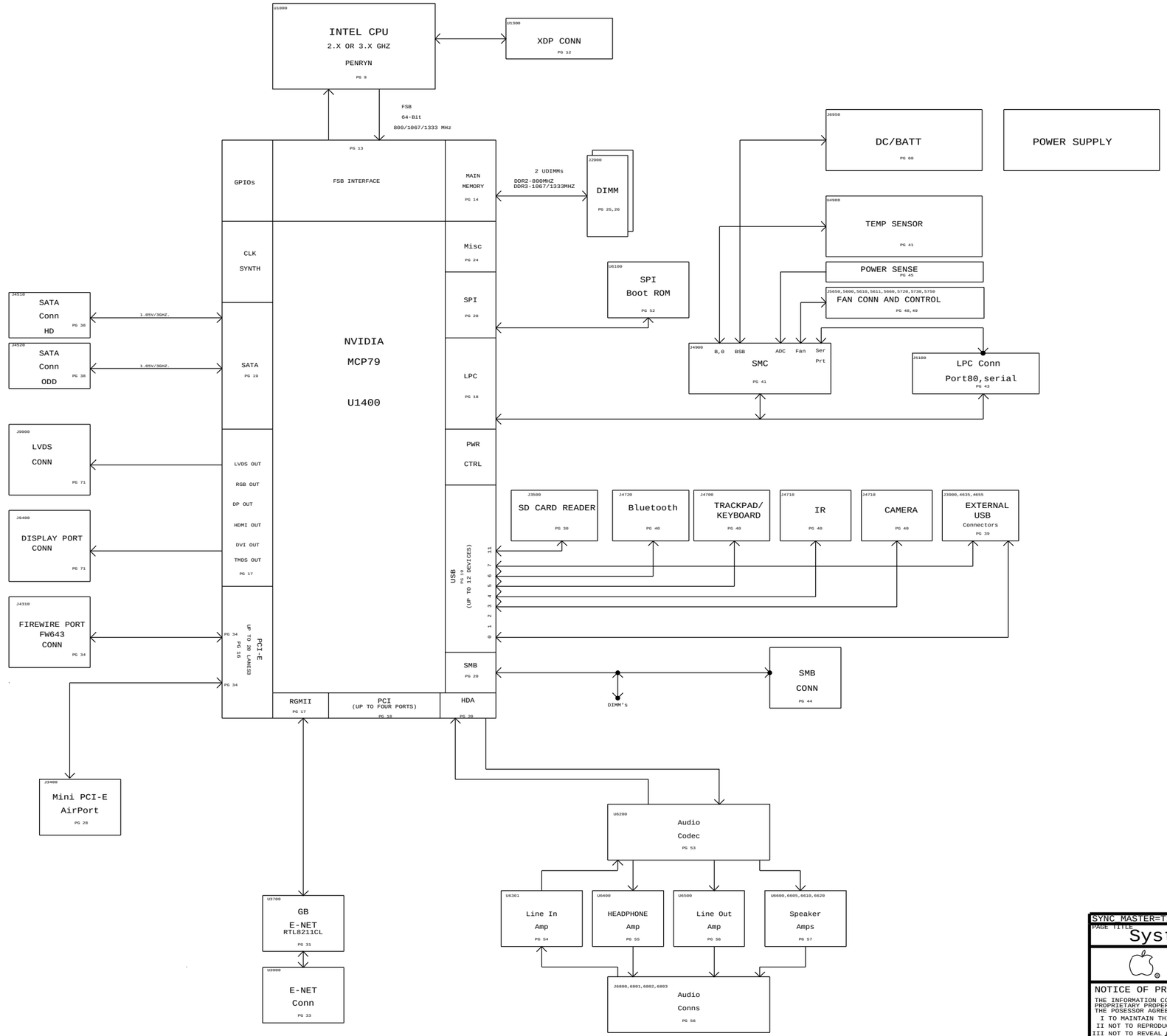

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2007

PAGE TITLE
System Block Diagram

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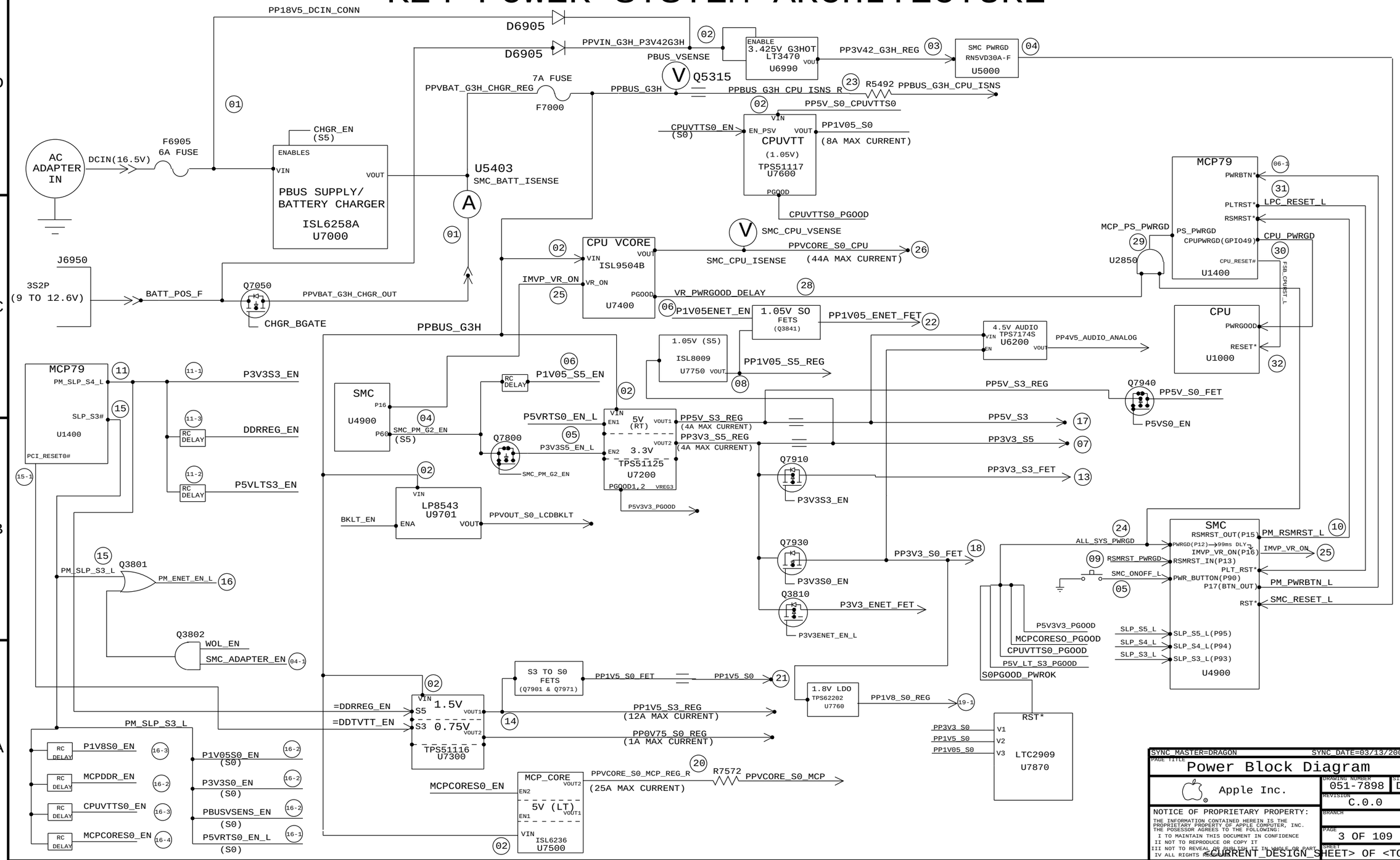
K24 POWER SYSTEM ARCHITECTURE



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Power Block Diagram

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9923	PCBA,MLB,BETTER,K24	K24_COMMON,CPU_2_26GHZ,EEE_6GC,KB_BL
630-9924	PCBA,MLB,BEST,K24	K24_COMMON,CPU_2_53GHZ,EEE_6GD,KB_BL

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:6G4]	CRITICAL	EEE_6G4
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:6GC]	CRITICAL	EEE_6GC
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:6GD]	CRITICAL	EEE_6GD

BOM Groups

BOM GROUP	BOM OPTIONS
K24_COMMON	COMMON,ALTERNATE,K24_MCP,K24_MISC,K24_DEBUG_PROD,K24_PROGPARTS
K24_MCP	MCP_B03,BOOT_MODE_USER,MCPSEQ_SMC
K24_MISC	ONEWIRE_PU,DP_ESD,MIKEY,BKLT_PROD,SUPERCAP_NO,LDO_NO
K24_PROGPARTS	BOOTROM_PROG,SMC_PROG,IR_PROG,WELLSPRING_PROG
K24_DEBUG_ENG	DEVEL_BOM,SMC_DEBUG_YES,XDP
K24_DEBUG_PVT	DEVEL_BOM,BMON_PROD,SMC_DEBUG_YES,XDP,NO_VREFMRGN
K24_DEBUG_PROD	BMON_PROD,SMC_DEBUG_YES,XDP,LPCPLUS_NOT,NO_VREFMRGN
K24_DEVEL_ENG	BMON_ENG,XDP_CONN,LPCPLUS,VREFMRGN,FWPHY_WAKE_YES
K24_DEVEL_PVT	LPCPLUS

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3646	1	PDC,SLGBE,PRQ,2.0,25W,1066,M0,3M,BGA	U1000	CRITICAL	CPU_2_0GHZ
337S3704	1	PDC,SLGE2,PRQ,2.26,25W,1066,R0,3M,BGA	U1000	CRITICAL	CPU_2_26GHZ
337S3639	1	PDC,SLB4N,PRQ,2.4,25W,1066,M0,3M,BGA	U1000	CRITICAL	CPU_2_4GHZ
337S3756	1	PDC,SLGFG,PRQ,2.53,25W,1066,R0,3M,BGA	U1000	CRITICAL	CPU_2_53GHZ
337S3761	1	PDC,SLGLA,PRQ,2.66,25W,1066,E0,3M,BGA	U1000	CRITICAL	CPU_2_66GHZ
338S0710	1	IC,GMCP,MCP79,35X35MM,BGA1437,B03	U1400	CRITICAL	MCP_B03

Programmable Parts

338S0563	1	IC,SMC,HS8/2117,9X9MM,TLP,HF	U4900	CRITICAL	SMC_BLANK
341S2445	1	IC,SMC,K24	U4900	CRITICAL	SMC_PROG
335S0610	1	IC,FLASH,SPI,32MBIT,3.3V,86MHZ,8-SOP	U6100	CRITICAL	BOOTROM_BLANK
341S2441	1	IC,PRGRM,EFI BOOTROM,UNLOCK,K24	U6100	CRITICAL	BOOTROM_PROG
338S0375	1	IC,CY7C63833,ENCORE II,USB CONTROLLER	U4800	CRITICAL	IR_BLANK
341S2093	1	IC,IR CONTROLLER,M97	U4800	CRITICAL	IR_PROG
337S2983	1	IC,PSOC+ W/ USB,56 PIN,MLF,CY8C24794	U5701	CRITICAL	WELLSPRING_BLANK
341S2503	1	IC,PRGRM,WELLSPRING CONTROLLER	U5701	CRITICAL	WELLSPRING_PROG

LOCKED BOOTROM APN IS 341S2443

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S0778	152S0693		ALL	CYNTEC AS ALTERNATE
152S0796	152S0685		ALL	CYNTEC AS ALTERNATE
157S0058	157S0055		ALL	DELTA AS ALTERNATE
104S0018	104S0023		ALL	DALE/VISHAY AS ALTERNATE
128S0093	128S0218		ALL	KEMET AS ALTERNATE
152S0874	152S0516		ALL	MAGLAYERS AS ALTERNATE
152S0847	152S0586		ALL	MAGLAYERS AS ALTERNATE
152S1025	152S1024		ALL	TOKO AS ALTERNATE
337S3769	337S3704		ALL	INTEL P7550 CPU AS ALTERNATE
353S2718	353S2310		ALL	INTERSIL AS ALTERNATE

DEVELOPMENT BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-0741	1	K24 MLB DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM

K24 BOARD STACK-UP

Top	SIGNAL
2	GROUND
3	SIGNAL(High Speed)
4	SIGNAL(High Speed)
5	GROUND
6	POWER
7	POWER
8	GROUND
9	SIGNAL(High Speed)
10	SIGNAL(High Speed)
11	GROUND
BOTTOM	SIGNAL

SYNC MASTER=M97 MLB

PAGE TITLE: BOM Configuration

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Revision History

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SYNC MASTER=M97 MLB

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Functional Test Points

Fan Connectors

TRUE	PP5V_S0	(NEED 3 TP)	6D3 7D5
TRUE	FAN_RT_PWM		47B4
TRUE	FAN_RT_TACH		47C4

(NEED TO ADD 3 GND TP)

MIC FUNC_TEST

TRUE	BI_MIC_LO	56C2 57B1
TRUE	BI_MIC_HI	56C2 57B1
TRUE	BI_MIC_SHIELD	56C2 57B1

SPEAKER FUNC_TEST

TRUE	SPKRAMP_L_N_OUT	55A2 56B2
TRUE	SPKRAMP_L_P_OUT	55B2 56B2
TRUE	SPKRAMP_R_N_OUT	55C2 56A2
TRUE	SPKRAMP_R_P_OUT	55C2 56B2
TRUE	SPKRAMP_SUB_N_OUT	55B2 56B2
TRUE	SPKRAMP_SUB_P_OUT	55C2 56B2

THERMAL FUNC_TEST

TRUE	MCPTHMSNS_D2_P	46B5 80D3
TRUE	MCPTHMSNS_D2_N	46B5 80D3

LVDS FUNC_TEST

TRUE	PP3V3_LCDVDD_SW_F	6C3 68C2
TRUE	PP3V3_S0_LCD_F	68C3
TRUE	PPVOUT_S0_LCDBKLT	6C3 68B2 71C1
TRUE	LVDS_IG_DDC_CLK	17B3 68C5
TRUE	LVDS_IG_DDC_DATA	17A3 68C5
TRUE	LVDS_IG_A_DATA_N<0>	17B3 68C2 75B3
TRUE	LVDS_IG_A_DATA_P<0>	17B3 68C2 75B3
TRUE	LVDS_IG_A_DATA_N<1>	17B3 68C2 75B3
TRUE	LVDS_IG_A_DATA_P<1>	17B3 68C2 75B3
TRUE	LVDS_IG_A_DATA_N<2>	17B3 68C2 75B3
TRUE	LVDS_IG_A_DATA_P<2>	17B3 68C2 75B3
TRUE	LVDS_IG_A_CLK_F_N	68C2 75B3
TRUE	LVDS_IG_A_CLK_F_P	68C2 75B3
TRUE	LED_RETURN_1	68B3 71B1
TRUE	LED_RETURN_2	68B3 71B1
TRUE	LED_RETURN_3	68B3 71B1
TRUE	LED_RETURN_4	68B3 71B1
TRUE	LED_RETURN_5	68B3 71B1
TRUE	LED_RETURN_6	68B3 71A1
TRUE	TP_BKL_SYNC	68C2

(NEED TO ADD 5 GND TP)

SATA ODD CONN

TRUE	PP5V_SW_ODD	(NEED 4 TP)	6C3 37D3
TRUE	SMC_ODD_DETECT		37C7 40B8
TRUE	SATA_ODD_D2R_C_P		37C6 75A3
TRUE	SATA_ODD_D2R_C_N		37C6 75A3
TRUE	SATA_ODD_R2D_P		37C6 75A3
TRUE	SATA_ODD_R2D_N		6A7 37C6 75A3

(NEED TO ADD 4 GND TP)

SATA HDD/IR/SIL

TRUE	PP5V_S0_HDD_FLT	(NEED 4 TP)	6C3 37B6
TRUE	SATA_HDD_R2D_P		37A5 75A3
TRUE	SATA_HDD_R2D_N		37A5 75A3
TRUE	SATA_HDD_D2R_C_P		37B5 75A3
TRUE	SATA_HDD_D2R_C_N		37B5 75A3
TRUE	SYS_LED_ANODE_R		37A7
TRUE	IR_RX_OUT		37A7 39D4
TRUE	PP5V_S3_IR_R		37A7

(NEED TO ADD 4 GND TP)

BATT POWER CONN

TRUE	SMBUS_SMC_BSA_SCL		6A7 43C5 79D3
TRUE	SMBUS_SMC_BSA_SDA		43C5 79D3
TRUE	SYS_DETECT_L		58A8
TRUE	BATT_POS_F	(NEED 3 TP)	58A7 58B8 59A3

(NEED TO ADD 3 GND TP)

BATT SIGNAL CONN

TRUE	PP3V42_G3H	(NEED 3 TP)	6B5 6D3 7D1
TRUE	SMBUS_SMC_BSA_SCL		6A7 43C5 79D3
TRUE	SMBUS_SMC_BSA_SCL		6A7 43C5 79D3
TRUE	SMC_BIL_BUTTON_L		40C5 58C4
TRUE	SMC_LID_R		58C2

(NEED TO ADD 5 GND TP)

RIGHT CLUTCH CONN

TRUE	PP5V_S3_BTCAMERA_F		29C7
TRUE	PCIE_MINI_D2R_P		16B6 29C7 75D3
TRUE	PCIE_MINI_D2R_N		16B6 29C7 75D3
TRUE	PCIE_MINI_R2D_P		29C7 75D3
TRUE	PCIE_MINI_R2D_N		29C7 75D3
TRUE	PCIE_CLK100M_MINI_CONN_P		29C7 75D3
TRUE	PCIE_CLK100M_MINI_CONN_N		29C7 75D3
TRUE	USB_CAMERA_CONN_P		29B7 76C3
TRUE	USB_CAMERA_CONN_N		29B7 76C3
TRUE	PP5V_WLAN	(NEED 2 TP)	6C3 29C5
TRUE	PCIE_WAKE_L		16B6 29C7
TRUE	SMBUS_SMC_A_S3_SCL		6C5 43D2 79D3
TRUE	SMBUS_SMC_A_S3_SDA		6C5 43D2 79D3
TRUE	CONN_USB2_BT_P		29B7 76C3
TRUE	CONN_USB2_BT_N		29B7 76B3
TRUE	MINI_CLKREQ_O_L		29C7
TRUE	MINI_RESET_CONN_L		29A7

(NEED TO ADD 6 GND TP)

IPD_FLEX_CONN

TRUE	PP3V3_S3_LDO	6C3 49B4 49C3
TRUE	PP18V5_S3	6C3 49C1 49D3
TRUE	Z2_CS_L	48C8 49C3
TRUE	Z2_DEBUG3	48C8 49C3
TRUE	Z2_MOSI	48C8 49C3
TRUE	Z2_MISO	48C8 49C3
TRUE	Z2_SCLK	48C8 49C3
TRUE	Z2_BOOST_EN	49C3 49C5
TRUE	Z2_HOST_INTN	48D8 49C3
TRUE	Z2_CLKIN	48C6 49C3
TRUE	Z2_KEY_ACT_L	48C8 49C1
TRUE	Z2_RESET	48C8 49C1
TRUE	PSOC_MISO	48C8 49C1
TRUE	PSOC_MOSI	48C8 49C1
TRUE	PSOC_SCLK	48C8 49C1
TRUE	SMBUS_SMC_A_S3_SDA	6D5 43D2 79D3
TRUE	SMBUS_SMC_A_S3_SCL	6D5 43D2 79D3
TRUE	PSOC_F_CS_L	48C8 49C1
TRUE	PICKB_L	48D8 49C1

KEYBOARD CONN

TRUE	PP3V3_S3	6D3 7D3
TRUE	PP3V42_G3H	6A7 6D3 7D1
TRUE	WS_KBD1	48C6 48D2
TRUE	WS_KBD2	48C6 48D2
TRUE	WS_KBD3	48C6 48D2
TRUE	WS_KBD4	48C6 48D2
TRUE	WS_KBD5	48C6 48D2
TRUE	WS_KBD6	48C6 48D2
TRUE	WS_KBD7	48C6 48D2
TRUE	WS_KBD8	48C6 48D2
TRUE	WS_KBD9	48C6 48D2
TRUE	WS_KBD10	48C6 48D2
TRUE	WS_KBD11	48C6 48D2
TRUE	WS_KBD12	48C6 48D2
TRUE	WS_KBD13	48C6 48D2
TRUE	WS_KBD14	48C2 48C6
TRUE	WS_KBD15_CAP	48C2
TRUE	WS_KBD16_NUM	48C2
TRUE	WS_KBD17	48C2 48D6
TRUE	WS_KBD18	48C2 48D7
TRUE	WS_KBD19	48C2 48D7
TRUE	WS_KBD20	48C2 48D7
TRUE	WS_KBD21	48C2 48D7
TRUE	WS_KBD22	48C2 48D7
TRUE	WS_KBD23	48C2 48D7
TRUE	WS_KBD_ONOFF_L	48C2
TRUE	WS_LEFT_SHIFT_KBD	48B3 48B5 48C2
TRUE	WS_LEFT_OPTION_KBD	48B3 48B5 48C2
TRUE	WS_CONTROL_KBD	48B3 48B5 48C2

(NEED TO ADD 1 GND TP)

KBD BACKLIGHT CONN

TRUE	KBDLED_ANODE	(NEED 2 TP)	49A4
TRUE	SMC_KDBLED_PRESENT_L		49A4 49A6

(NEED TO ADD 2 GND TP)

DEBUG VOLTAGE

TRUE	PPVCORE_S0_CPU	7D7
TRUE	PPVCORE_S0_MCP	7C7
TRUE	PP0V75_S0	7C7
TRUE	PP1V05_S0	7D7
TRUE	PP1V5_S0	7C6
TRUE	PP1V8_S0	7B6
TRUE	PP5V_S0	6D7 7D5
TRUE	PP3V3_S0	7D5
TRUE	PP1V5_S3	7D3
TRUE	PP3V3_S3	6B5 7D3
TRUE	PP5V_S3	7C3
TRUE	PP1V1R1V05_S5	7B3
TRUE	PP3V3_S5	7B3
TRUE	PP3V42_G3H	6A7 6B5 7D1
TRUE	PPBUS_G3H	7C1
TRUE	PP3V3_ENET_PHY	7B5
TRUE	PP1V2R1V05_ENET	7B5
TRUE	PP3V3_G3_RTC	20C8 21A5 24D4
TRUE	PP5V_WLAN	6D5 29C5
TRUE	PP5V_SW_ODD	6B7 37D3
TRUE	PP5V_S0_HDD_FLT	6B7 37B6
TRUE	PP3V3_S5_AVREF_SMC	40D4 41C6
TRUE	PP18V5_S3	6C5 49C1 49D3
TRUE	PP3V3_S3_LDO	6C5 49B4 49C3
TRUE	PP3V3_LCDVDD_SW_F	6C7 68C2
TRUE	PPVOUT_S0_LCDBKLT	6C7 68B2 71C1
TRUE	PP4V5_AUDIO_ANALOG	52A5 52D2 52D7
TRUE	SMC_PM_G2_EN	40D5 60C5 66D8
TRUE	PM_SLP_S4_L	20C3 40C5 41A2 66C8
TRUE	PM_SLP_S3_L	20C3 32B7 35A5 40C5 66D5 78D8

(NEED TO ADD 4 GND TP)

DC POWER CONN

TRUE	PP18V5_DCIN_FUSE	(NEED 3 TP)	58D6
TRUE	ADAPTER_SENSE		58D7

(NEED TO ADD 4 GND TP)

SYNC_MASTER=M97_MLB

PAGE TITLE: FUNC TEST

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

BRANCH:

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SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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"S0,S0M" RAILS

62D1 =PPVCORE_S0_CPU_REG
(CPU VCORE PWR)
- PPVCORE_S0_CPU 6D3
  MIN_LINE_WIDTH=0.6 MM
  MIN_NECK_WIDTH=0.3 MM
  VOLTAGE=1.25V
  MAKE_BASE=TRUE
  - =PPVCORE_S0_CPU 10B5 10D6 11D6
  - =PPVCORE_S0_CPU_VSENSE 44D8

64C2 =PPCPUVTT_S0_REG
- PP1V05_S0 6D3
  MIN_LINE_WIDTH=0.6 mm
  MIN_NECK_WIDTH=0.2 mm
  VOLTAGE=1.05V
  MAKE_BASE=TRUE
  - =PP1V05_S0_CPU 9D5 10C6 11B6 12D6
  - =PP1V05_S0_MCP_FSB 13A2 13B7 21D3 22C8
  - =PP1V05_S0_SMC_LS
  - =PP1V05_S0_MCP_PEX_DVDD 7A8 22D8
  - =PP1V05_S0_MCP_AVDD_UF 22D4
  - =PP1V05_S0_MCP_SATA_DVDD 7A8 22D6
  - =PP1V05_S0_MCP_HDMI_VDD 17A6 23D7
  - =PP1V05_S0_VMON 66A8
  - =PP1V05_S0_MCP_PLL_UF_R 65B3
  - =PP1V05_FW_P1V05FWFET 35C6
  - =PP1V05_FWPWRCTL 35B4

63C7 63C1 63B8 =PPMCPCORE_S0_REG
(MCP VCORE AFTER SENSE RES)
- PPVCORE_S0_MCP 6D3
  MIN_LINE_WIDTH=0.6 MM
  MIN_NECK_WIDTH=0.2 MM
  VOLTAGE=1.25V
  MAKE_BASE=TRUE
  - =PPVCORE_S0_MCP 21D5 22D8
  - =PPVCORE_S0_MCP_VSENSE 44D8

61C8 =PP0V75_S0_REG
- PP0V75_S0 6D3
  MIN_LINE_WIDTH=0.4 mm
  MIN_NECK_WIDTH=0.2 mm
  VOLTAGE=0.75V
  MAKE_BASE=TRUE
  - =PPVTT_S0_VTTCLAMP 67B3
  - =PP0V75_S0_MEM_VTT_A 26A4
  - =PP0V75_S0_MEM_VTT_B 27A4

67D1 =PP1V5_S0_FET
- PP1V5_S0 6D3
  MIN_LINE_WIDTH=0.5 mm
  MIN_NECK_WIDTH=0.2 mm
  VOLTAGE=1.5V
  MAKE_BASE=TRUE
  - =PP1V5_S0_CPU 10B6 11B6
  - =PP1V5_S0_VMON 66A8
  - =PP1V8R1V5_S0_MCP_MEM 15C3 15C7 22C8
  - =PP1V5_S0_MEM_MCP 27B3
  - =PP1V5_S0_MCP_PLL_VLDO 65B6

65C5 =PP1V8_S0_REG
- PP1V8_S0 6D3
  MIN_LINE_WIDTH=0.5 MM
  MIN_NECK_WIDTH=0.2 mm
  VOLTAGE=1.8V
  MAKE_BASE=TRUE
  - =PP3V3R1V8_S0_MCP_IFP_VDD 17B6 23D7
  - =PP1V8_S0_AUDIO 52D7

65B1 22C4 =PP1V05_S0_MCP_PLL_UF
- PP1V05_S0_MCP_PLL_UF
  MIN_LINE_WIDTH=0.6 MM
  MIN_NECK_WIDTH=0.2 mm
  VOLTAGE=1.05V
  MAKE_BASE=TRUE

67B6 =PP5V_S0_FET
- PP5V_S0 6D3 6D7
  MIN_LINE_WIDTH=0.6 mm
  MIN_NECK_WIDTH=0.2 mm
  VOLTAGE=5V
  MAKE_BASE=TRUE
  - =PP5V_S0_HDD 37B3
  - =PP5V_S0_LPCPLUS 42D5
  - =PP5V_S0_FAN_RT 47C5
  - =PP5V_S0_CPU_IMVP 62D8
  - =PP5V_S0_KBDLED 49A5
  - =PP5V_S0_DP_AUX_MUX 69B6
  - =PP5V_S0_CPUVTTS0 64C8
  - =PP5V_S0_BKL 71D4
  - =PP5V_S0_MCPREG 63D4
  - =PP5V_S0_VMON 66B5

67C6 =PP3V3_S0_FET
- PP3V3_S0 6D3
  MIN_LINE_WIDTH=0.6 mm
  MIN_NECK_WIDTH=0.2 mm
  VOLTAGE=3.3V
  MAKE_BASE=TRUE
  - =PP3V3_S0_XDP 12D6
  - =PP3V3_S0_MCP 20C2 21B3 22B8
  - =PP3V3_S0_MCP_DAC_UF 23D4
  - =PP3V3_S0_MCP_VPLL_UF 23C7
  - =PP3V3_S0_ODD 37C7 37D6
  - =PP3V3_S0_SMBUS_SMC_0_S0 43D5
  - =PP3V3_S0_SMBUS_SMC_B_S0 43C3
  - =PP3V3_S0_SMBUS_MCP_0 43D8
  - =PP3V3_S0_FAN_RT 47C5
  - =PP3V3_S0_AUDIO 52A8 52D2 56D8 57B8 57D3
  - =PP3V3_S0_IMVP 62D8
  - =PP3V3_S0_LCD 68C5
  - =PP3V3_S0_MCP_GPIO 17C1 18D1 20A4
  - =PP3V3_S0_MCP_PLL_UF 22B6
  - =PP3V3R1V5_S0_MCP_HDA 29D3 20D8 22A8
  - =PP3V3_S0_SMC 41A1 41D3
  - =PP3V3_S0_MCPTHMSNS 46B6
  - =PP3V3_S0_CPUTHMSNS 46D6
  - =PP3V3_S0_DPCONN 70B8 70C8
  - =PPSPD_S0_MEM_A 26A8
  - =PPSPD_S0_MEM_B 27A8
  - =PP3V3_S0_PWRCTL 66A5
  - =PP3V3_S0_VMON 66A8
  - =PP3V3_S0_CPUVTTISNS 45C7
  - =PP3V3_S0_TPAD 49A6
  - =PP3V3_S0_SMBUS_MCP_1 43C8
  - =PP3V3_S0_P1V8S0 65D8
  - =PP3V3_S0_BKL_VDDIO 71C7
  - =PP3V3_S0_MCPDDRISNS 45D8
  - =PP3V3_S0_MCP_PLL_VLDO 65C6
  - =PP3V3_S0_P3V3FWFET 35D6
  - =PP3V3_S0_FWPWRCTL 35B1 35D2

"ENET" RAILS

32D2 =PP3V3_ENET_FET
- PP3V3_ENET_PHY 6C3
  MIN_LINE_WIDTH=0.4 MM
  MIN_NECK_WIDTH=0.2 MM
  VOLTAGE=3.3V
  MAKE_BASE=TRUE
  - =PP3V3_ENET_MCP_RMGT 17D3 17D7 22A5 22B6
  - =PP3V3_ENET_PHY 31D7

32B2 =PP1V05_ENET_FET
- PP1V2R1V05_ENET 6C3
  MIN_LINE_WIDTH=0.4 MM
  MIN_NECK_WIDTH=0.2 MM
  VOLTAGE=1.05V
  MAKE_BASE=TRUE
  - =PP1V05_ENET_MCP_PLL_MAC 22A8
  - =PP1V05_ENET_MCP_RMGT 17D3 22D6
  - =PP1V05_ENET_PHY 31D2

PEX & SATA AVDD/DVDD aliases

22D1 PP1V05_S0_MCP_PEX_AVDD
MAKE_BASE=TRUE
206 mA (A01)
- =PP1V05_S0_MCP_PEX_AVDD0 16B3
- =PP1V05_S0_MCP_PEX_AVDD1 16A3

206 mA (A01)

22D8 7D7 =PP1V05_S0_MCP_PEX_DVDD
206 mA (A01)
- =PP1V05_S0_MCP_PEX_DVDD0 16B6
- =PP1V05_S0_MCP_PEX_DVDD1 16A6

57 mA (A01)

22D2 PP1V05_S0_MCP_SATA_AVDD
MAKE_BASE=TRUE
127 mA (A01)
- =PP1V05_S0_MCP_SATA_AVDD0 19B6
- =PP1V05_S0_MCP_SATA_AVDD1 19B6

127 mA (A01)

22D6 7D7 =PP1V05_S0_MCP_SATA_DVDD
127 mA (A01)
- =PP1V05_S0_MCP_SATA_DVDD0 19B6
- =PP1V05_S0_MCP_SATA_DVDD1 19B6

43 mA (A01)

"S3" RAILS

61C1 =PP1V5_S3_REG
- PP1V5_S3 6D3
  MIN_LINE_WIDTH=0.6 mm
  MIN_NECK_WIDTH=0.2 mm
  VOLTAGE=1.5V
  MAKE_BASE=TRUE
  - =PP1V5_S3_P1V5S0FET 67D3
  - =PP1V5_S3_MEM_A 26D7
  - =PP1V5_S3_MEM_B 27D7
  - =PP1V5_S3_MEMRESET 28C6
  - =PP1V5_S3_HDD 37B8

67D6 =PP3V3_S3_FET
- PP3V3_S3 6B5 6D3
  MIN_LINE_WIDTH=0.6 mm
  MIN_NECK_WIDTH=0.2 mm
  VOLTAGE=3.3V
  MAKE_BASE=TRUE
  - =PP3V3_S3_SMBUS_SMC_A_S3 43D3
  - =PP3V3_S3_PDCISENS 61B3
  - =PP3V3_S3_SMBUS_SMC_MGMT 43B5
  - =PP3V3_S3_VREFMRGN 25D8
  - =PP3V3_S3_WLAN 29A6
  - =PP3V3_S3_MCP_GPIO 20A3
  - =PP3V3_S3_TPAD 48A6 48B5 48C5 48D2
  - =PP3V3_S3_SMS 50B7
  - =PP3V3_S3_CARDREADER 30D7

60B8 =PP5V_S3_REG
- PP5V_S3 6D3
  MIN_LINE_WIDTH=0.6 mm
  MIN_NECK_WIDTH=0.2 mm
  VOLTAGE=5V
  MAKE_BASE=TRUE
  - =PP5V_S3_EXTUSB 38C7
  - =PP5V_S3_IR 37A8 39D7
  - =PP5V_S3_BTCAMERA 29C3
  - =PP5V_S3_VTTCLAMP 67A3
  - =PP5V_S3_MCPDDRFET 67D4
  - =PP5V_S3_SYSLED 41B8
  - =PP5V_S3_TPAD 49B6 49D7
  - =PP5V_S3_WLAN 29C1
  - =PP5V_S3_1V5S30V75S0 61C5
  - =PP5V_S3_AUDIO 52A8 52D2 54D5 56B6
  - =PP5V_S3_AUDIO_AMP 55B7 55C7 55D7
  - =PP5V_S3_P5VS0FET 67B8
  - =PP5V_S3_ODD 37D5

61D8 25D3 =PPVTT_S3_DDR_BUF
- PPVTT_S3_DDR_BUF
  MIN_LINE_WIDTH=0.3 MM
  MIN_NECK_WIDTH=0.2 MM
  VOLTAGE=0.75V
  MAKE_BASE=TRUE

"G3H" RAILS

58B4 =PP3V42_G3H_REG
- PP3V42_G3H 6A7 6B5 6D3
  MIN_LINE_WIDTH=0.6 MM
  MIN_NECK_WIDTH=0.2 MM
  VOLTAGE=3.42V
  MAKE_BASE=TRUE
  - =PPVIN_S5_SMCVREF 41C8
  - =PP3V42_G3H_SMBUS_SMC_BSA 43C5
  - =PP3V42_G3H_PWRCTL 66B3 66C8 66D8
  - =PP3V42_G3H_CHGR 59A8 59C6 59D5
  - =PP3V42_G3H_SMCUSBMUX 38B8
  - =PP3V42_G3H_TPAD 48B5 48C2 48C3 48C6
  - =PP3V42_G3H_BATT 58C2 58C4
  - =PP3V3_S5_SMC 20D4 41C1 41C3 41C7 41D8
  - =PP3V3_S5_LPCPLUS 42C7 42C8 42D5
  - =PP3V42_G3H_RTC_D 24D8
  - =PP3V42_G3H_BMON_ISNS 45B8
  - =PP3V42_G3H_ONEWIRE 58D2
  - =PP3V42_G3H_AUDIO 66B6

58D1 58C8 =PP18V5_DCIN_CONN
- PP18V5_G3H
  MIN_LINE_WIDTH=0.6 MM
  MIN_NECK_WIDTH=0.3 MM
  VOLTAGE=18.5V
  MAKE_BASE=TRUE
  - =PP18V5_G3H_CHGR 59D8

59C1 =PPBUS_G3H
- PPBUS_G3H 6C3
  MIN_LINE_WIDTH=0.6 mm
  MIN_NECK_WIDTH=0.3 MM
  VOLTAGE=12.6V
  MAKE_BASE=TRUE
  - =PPBUS_S0_LCDBKLT 72D8
  - =PPVIN_S0_MCPCORE 63D5
  - =PPVIN_S5_1V5S30V75S0 61C2
  - =PPVIN_S5_3V3S5 69C3
  - =PPVIN_S3_5VS3 69C6 69C7
  - =PPBUS_G3HRS5 44B8
  - =PPBUS_S5_FWPWRSW 35B7
  - =PPCPUVCORE_VTT_ISNS_R 45B8

(BEFORE HIGH SIDE SENSING RES.)

45B7 =PPCPUVCORE_VTT_ISNS
(AFTER HIGH SIDE CPU VCORE
& CPU VTT SENSING RES.)
- PPBUS_G3H_CPU_ISNS
  MIN_LINE_WIDTH=0.6 mm
  MIN_NECK_WIDTH=0.3 MM
  VOLTAGE=12.6V
  MAKE_BASE=TRUE
  - =PPVIN_S0_CPUVTTS0 64C6
  - =PPVIN_S5_CPU_IMVP 62C3 62D4 62D8

"S5" RAILS

65A5 =PP1V05_S5_REG
- PP1V1R1V05_S5 6D3
  MIN_LINE_WIDTH=0.6 MM
  MIN_NECK_WIDTH=0.2 MM
  VOLTAGE=1.05V
  MAKE_BASE=TRUE
  - =PP1V05_S5_MCP_VDD_AUXC 21A3 22D8
  - =PP1V05_ENET_P1V05ENETFET 32C4

60B1 =PP3V3_S5_REG
- PP3V3_S5 6D3
  MIN_LINE_WIDTH=0.6 mm
  MIN_NECK_WIDTH=0.2 mm
  VOLTAGE=3.3V
  MAKE_BASE=TRUE
  - =PP3V3_S5_MCP_GPIO 17C7 19C1
  - =PP3V3_S5_ROM 42B5 42C7 51C6
  - =PP3V3_S5_LCD 68C8
  - =PP3V3_S5_MCP 21B3 22B8
  - =PP3V3_S5_MCPPWRGD 24B8
  - =PP3V3_S5_PWRCTL 66B3
  - =PP3V3_S5_P1V05ENETFET 32C5
  - =PP3V3_S5_P3V3S3FET 67D8
  - =PP3V3_S5_P3V3S0FET 67C8
  - =PP3V3_S5_P1V05S5 65B8
  - =PP3V3_S5_MEMRESET 28C4
  - =PP3V3_S5_P3V3ENETFET 32D5
  - =PP3V3_S5_DP_PORT_PWR 70D8
  - =PP3V3_FW_LATEVG 36A7
  - =PP3V3_FW_LATEVG_ACTIVE 35A8
  - =PP3V3_S5_P1V05FWFET 35C7

"FIREWIRE" RAILS

35D4 =PP3V3_FW_FET
- PP3V3_FW
  MIN_LINE_WIDTH=0.6 MM
  MIN_NECK_WIDTH=0.2 MM
  VOLTAGE=3.3V
  MAKE_BASE=TRUE
  - =PP3V3_FW_FWPHY 35D5 35D8 35D6 34B1 34D1
  - =PP3V3_S0_P1V05FWFET 35C7

35B1 =PPBUS_S5_FW_FET
- PPVP_FW
  MIN_LINE_WIDTH=0.4 mm
  MIN_NECK_WIDTH=0.2 mm
  VOLTAGE=12.6V
  MAKE_BASE=TRUE
  - =PPVP_FW_PORT1 36C3
  - =PPVP_FW_PHY_CPS_FET 36C6

35C5 =PP1V0_FW_FET
- PP1V05_FW
  MIN_LINE_WIDTH=0.6 MM
  MIN_NECK_WIDTH=0.2 MM
  VOLTAGE=1.05V
  MAKE_BASE=TRUE
  - =PP1V0_FW_FWPHY 34D6 35D3

SYNC_MASTER=BEN SYNC_DATE=04/21/2008
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Power Aliases

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HEATSINK STANDOFFS

Z0902 STDOFF-4.50D.98H-1.1-3.48-TH — LEFT OF CPU

Z0901 STDOFF-4.50D.98H-1.1-3.48-TH — ABOVE CPU

Z0903 STDOFF-4.50D.98H-1.1-3.48-TH — BELOW MCP

Z0904 STDOFF-4.50D.98H-1.1-3.48-TH — BELOW CPU

FAN STANDOFF

Z0905 STDOFF-4.50D.98H-1.1-3.48-TH

MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V

MLB MOUNTING (TO C. BRACKET) SCREW HOLES

OMIT Z0906 3R2P5

OMIT Z0907 3R2P5

MLB MOUNTING (TO TOPCASE) SCREW HOLES

OMIT Z0908 3R2P5

OMIT Z0909 3R2P5

OMIT Z0910 3R2P5

OMIT Z0911 3R2P5

OMIT Z0912 3R2P5

PCI-E ALIASES

UNUSED GPU LANES

16D6 16C6	=PEG_D2R_N<15:0>	NC_PEG_D2R_N<15:0>	NO_TEST=TRUE, MAKE_BASE=TRUE
16D6 16C6	=PEG_D2R_P<15:0>	NC_PEG_D2R_P<15:0>	NO_TEST=TRUE, MAKE_BASE=TRUE
16D3 16C3	=PEG_R2D_C_N<15:0>	NC_PEG_R2D_C_N<15:0>	NO_TEST=TRUE, MAKE_BASE=TRUE
16D3 16C3	=PEG_R2D_C_P<15:0>	NC_PEG_R2D_C_P<15:0>	NO_TEST=TRUE, MAKE_BASE=TRUE
16C6	PEG_PRSNT_L	TP_PEG_PRSNT_L	MAKE_BASE=TRUE
16C3	PEG_CLK100M_P	TP_PEG_CLK100M_P	MAKE_BASE=TRUE
16C3	PEG_CLK100M_N	TP_PEG_CLK100M_N	MAKE_BASE=TRUE

UNUSED EXPRESS CARD LANE

16B6	PCIE_EXCARD_D2R_P	TP_PCIE_EXCARD_D2R_P	MAKE_BASE=TRUE
16B6	PCIE_EXCARD_D2R_N	TP_PCIE_EXCARD_D2R_N	MAKE_BASE=TRUE
16B3	PCIE_EXCARD_R2D_C_P	TP_PCIE_EXCARD_R2D_C_P	MAKE_BASE=TRUE
16B3	PCIE_EXCARD_R2D_C_N	TP_PCIE_EXCARD_R2D_C_N	MAKE_BASE=TRUE
16C6	PCIE_EXCARD_PRSNT_L	TP_PCIE_EXCARD_PRSNT_L	MAKE_BASE=TRUE
16C6	EXCARD_CLKREQ_L	TP_EXCARD_CLKREQ_L	MAKE_BASE=TRUE
16C3	PCIE_CLK100M_EXCARD_P	TP_PCIE_CLK100M_EXCARD_P	MAKE_BASE=TRUE
16C3	PCIE_CLK100M_EXCARD_N	TP_PCIE_CLK100M_EXCARD_N	MAKE_BASE=TRUE

FIREWIRE PRESENT SIGNALS

35D3 16C6 PCIE_FW_PRSNT_L — R0950 0 5% 1/16W MF-LF 402 — NOSTUFF

USB ALIASES

UNUSED USB PORTS

19C3	USB_EXTC_P	TP_USB_EXTC_P	MAKE_BASE=TRUE
19C3	USB_EXTC_N	TP_USB_EXTC_N	MAKE_BASE=TRUE
19D3	USB_EXTD_P	TP_USB_EXTD_P	MAKE_BASE=TRUE
19D3	USB_EXTD_N	TP_USB_EXTD_N	MAKE_BASE=TRUE
19C3	USB_EXCARD_P	TP_USB_EXCARD_P	MAKE_BASE=TRUE
19C3	USB_EXCARD_N	TP_USB_EXCARD_N	MAKE_BASE=TRUE
19D3	USB_MINI_P	TP_USB_MINI_P	MAKE_BASE=TRUE
19D3	USB_MINI_N	TP_USB_MINI_N	MAKE_BASE=TRUE

DACS ALIASES

UNUSED CRT & TV-OUT INTERFACE

17C6	MCP_TV_DAC_RSET	NC_MCP_TV_DAC_RSET	NO_TEST=TRUE, MAKE_BASE=TRUE
17C6	MCP_TV_DAC_VREF	NC_MCP_TV_DAC_VREF	NO_TEST=TRUE, MAKE_BASE=TRUE
17C6	MCP_CLK27M_XTALIN	NC_MCP_CLK27M_XTALIN	NO_TEST=TRUE, MAKE_BASE=TRUE
17C6	MCP_CLK27M_XTALOUT	NC_MCP_CLK27M_XTALOUT	NO_TEST=TRUE, MAKE_BASE=TRUE
17C3	CRT_IG_R_C_PR	NC_CRT_IG_R_C_PR	NO_TEST=TRUE, MAKE_BASE=TRUE
17C3	CRT_IG_G_Y_Y	NC_CRT_IG_G_Y_Y	NO_TEST=TRUE, MAKE_BASE=TRUE
17C3	CRT_IG_B_COMP_PB	NC_CRT_IG_B_COMP_PB	NO_TEST=TRUE, MAKE_BASE=TRUE
17C3	CRT_IG_HSYNC	NC_CRT_IG_HSYNC	NO_TEST=TRUE, MAKE_BASE=TRUE
17C3	CRT_IG_VSYNC	NC_CRT_IG_VSYNC	NO_TEST=TRUE, MAKE_BASE=TRUE

LVDS ALIASES

UNUSED LVDS SIGNALS

17B3	LVDS_IG_A_DATA_P<3>	NC_LVDS_IG_A_DATA_P3	NO_TEST=TRUE, MAKE_BASE=TRUE
17B3	LVDS_IG_A_DATA_N<3>	NC_LVDS_IG_A_DATA_N3	NO_TEST=TRUE, MAKE_BASE=TRUE
17B3	LVDS_IG_B_CLK_P	NC_LVDS_IG_B_CLK_P	NO_TEST=TRUE, MAKE_BASE=TRUE
17B3	LVDS_IG_B_CLK_N	NC_LVDS_IG_B_CLK_N	NO_TEST=TRUE, MAKE_BASE=TRUE
17B3	LVDS_IG_B_DATA_P<3:0>	NC_LVDS_IG_B_DATA_P<3:0>	NO_TEST=TRUE, MAKE_BASE=TRUE
17B3	LVDS_IG_B_DATA_N<3:0>	NC_LVDS_IG_B_DATA_N<3:0>	NO_TEST=TRUE, MAKE_BASE=TRUE

MISC MCP79 ALIASES

13B6	CPU_PECI_MCP	TP_CPU_PECI_MCP	MAKE_BASE=TRUE
16B6	GMUX_JTAG_TCK_L	TP_GMUX_JTAG_TCK_L	MAKE_BASE=TRUE
16B6	GMUX_JTAG_TDO	TP_GMUX_JTAG_TDO	MAKE_BASE=TRUE
18D4	GMUX_JTAG_TDI	TP_GMUX_JTAG_TDI	MAKE_BASE=TRUE
18D4	GMUX_JTAG_TMS	TP_GMUX_JTAG_TMS	MAKE_BASE=TRUE

LAN ALIASES

17D6 =MCP_MII_RXER, 17D6 =MCP_MII_COL, 17D6 =MCP_MII_CRS — MCP_MII_PD (MAKE_BASE=TRUE) — R0930 47K 5% 1/16W MF-LF 402

DP HOTPLUG PULL-DOWN

17B6 =DVI_HPD_GMUX_INT — HPLUG_DET2 (MAKE_BASE=TRUE) — R0940 20K 5% 1/16W MF-LF 402

SO-DIMM ALIASES

UNUSED ADDRESS PINS

26D5	MEM_A_A<15>	TP_MEM_A_A15	MAKE_BASE=TRUE
27D5	MEM_B_A<15>	TP_MEM_B_A15	MAKE_BASE=TRUE

ETHERNET ALIASES

32C5	=P3V3ENET_EN	PM_SLP_RMGT_L (29C3)	MAKE_BASE=TRUE
32B5	=P1V05ENET_EN		
31C2	=PP3V3_ENET_PHY_VDDREG	TP_PP3V3_ENET_PHY_VDDREG	MAKE_BASE=TRUE
31C2	=RTL8211_REGOUT	NC_RTL8211_REGOUT	MAKE_BASE=TRUE
31C6	=RTL8211_ENSWREG		MAKE_BASE=TRUE
31B6	TP_RTL8211_CLK125		

R0931 22 5% 1/16W MF-LF 402

FW ALIASES

18B7	FW_PME_L	FW_PLUG_DET_L (35B1 35D7)	MAKE_BASE=TRUE
35C8 34B2	=FW_PME_L	FW643_WAKE_L	MAKE_BASE=TRUE

CPU FSB FREQUENCY STRAPS

73C3 9B4 IN CPU_BSEL<0:2> (MAKE_BASE=TRUE) — =MCP_BSEL<0:2> OUT 13A7

BSEL<2..0>	FSB MHZ
0 0 0	266
0 0 1	133
0 1 0	200
0 1 1	(166)
1 0 0	333
1 0 1	166
1 1 0	(400)
1 1 1	(RSVD)

EMI IO POGO PINS

ZS0900 1.4DIA-SHORT-EMI-MLB-M97-M98 SM OMIT

ZS0901 1.4DIA-SHORT-EMI-MLB-M97-M98 SM OMIT

ZS0902 1.4DIA-SHORT-EMI-MLB-M97-M98 SM OMIT

ZS0903 1.4DIA-SHORT-EMI-MLB-M97-M98 SM OMIT

ZS0908 1.4DIA-SHORT-EMI-MLB-M97-M98 SM OMIT

ZS0909 1.4DIA-SHORT-EMI-MLB-M97-M98 SM OMIT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
870-1801	6	POGO PIN,SHORT,EMI,MLB,K19/K24	ZS0900,ZS0901,ZS0902,ZS0903,ZS0908,ZS0909	CRITICAL	

EMI POGO PINS

ZS0904 2.0DIA-TALL-EMI-MLB-M97-M98 SM

ZS0905 2.0DIA-TALL-EMI-MLB-M97-M98 SM

ZS0906 2.0DIA-TALL-EMI-MLB-M97-M98 SM

ZS0907 2.0DIA-TALL-EMI-MLB-M97-M98 SM

SYNC_MASTER=M97_MLB

PAGE TITLE: SIGNAL ALIAS

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

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PAGE: 9 OF 109

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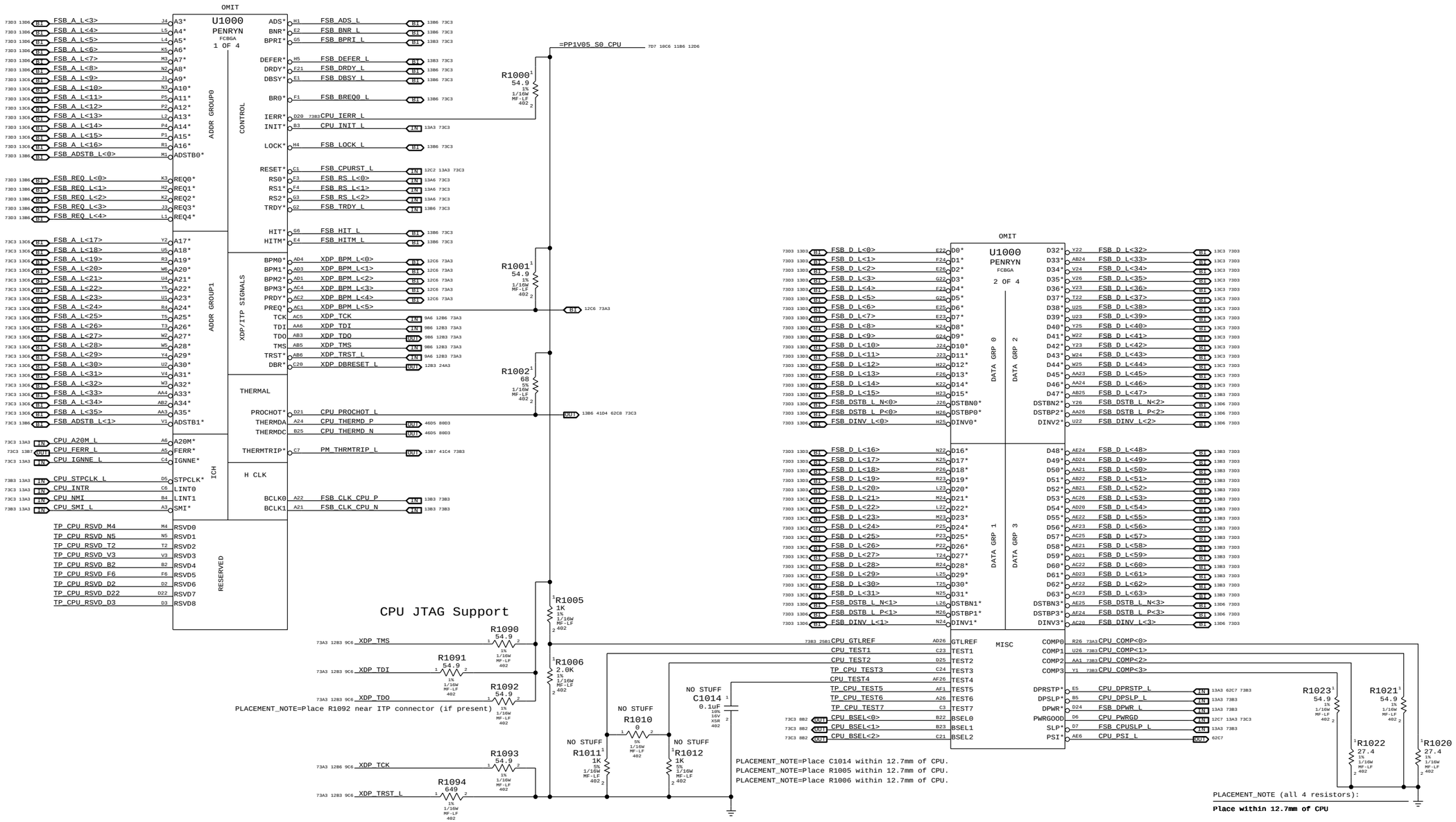

SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL

SYNC MASTER=T18_MLB SYNC DATE=12/12/2007

PAGE TITLE
CPU FSB

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D
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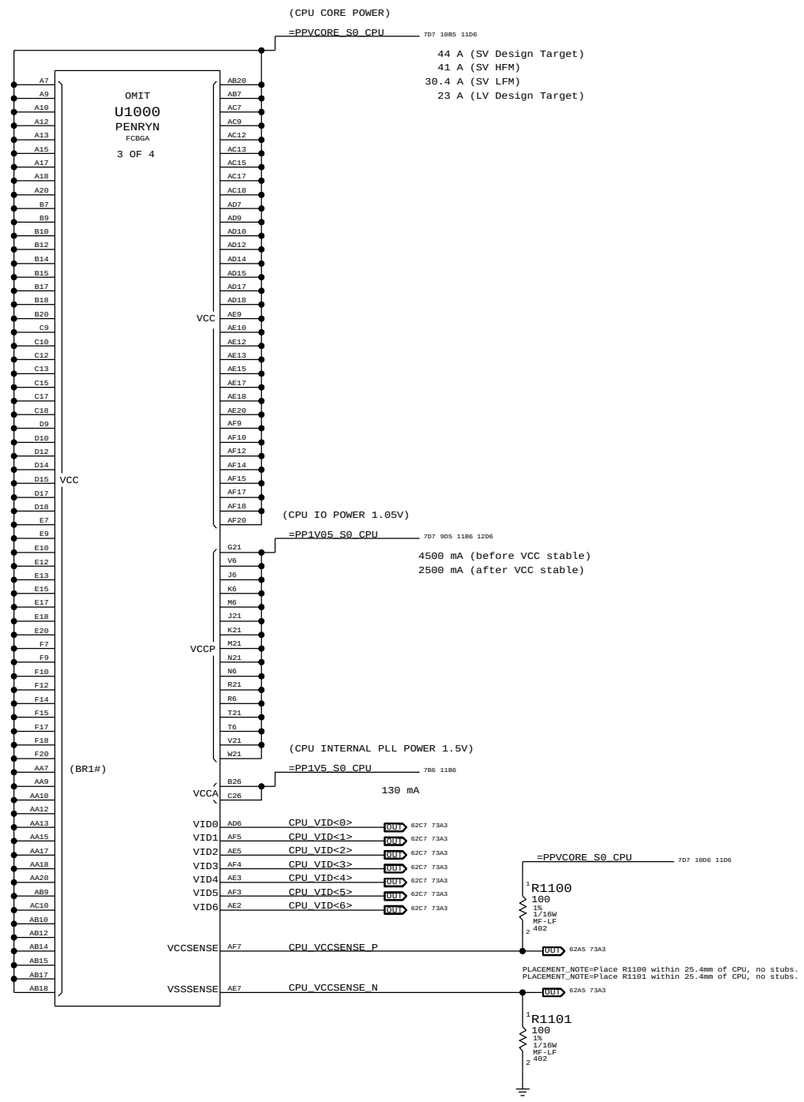

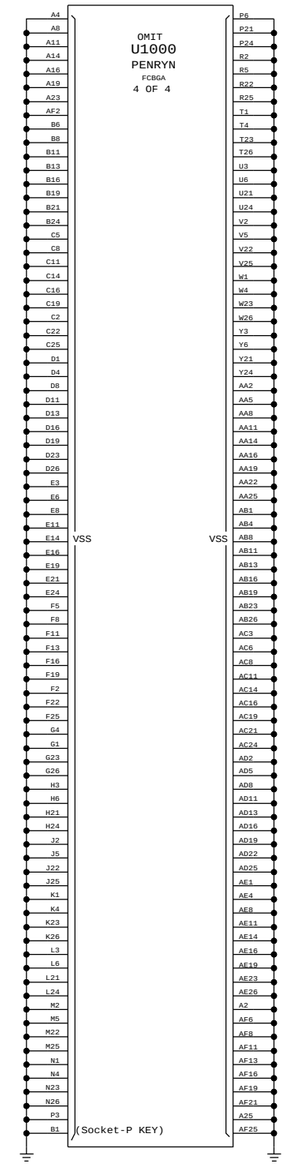

SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL

Current numbers from Merom for Santa Rosa EMTS, doc #20905.

SYNC MASTER=T18_MLB SYNC DATE=12/12/2007

PAGE TITLE
CPU Power & Ground

Apple Inc.

DRAWING NUMBER 051-7898
SIZE D
REVISION C.0.0
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PAGE 11 OF 109
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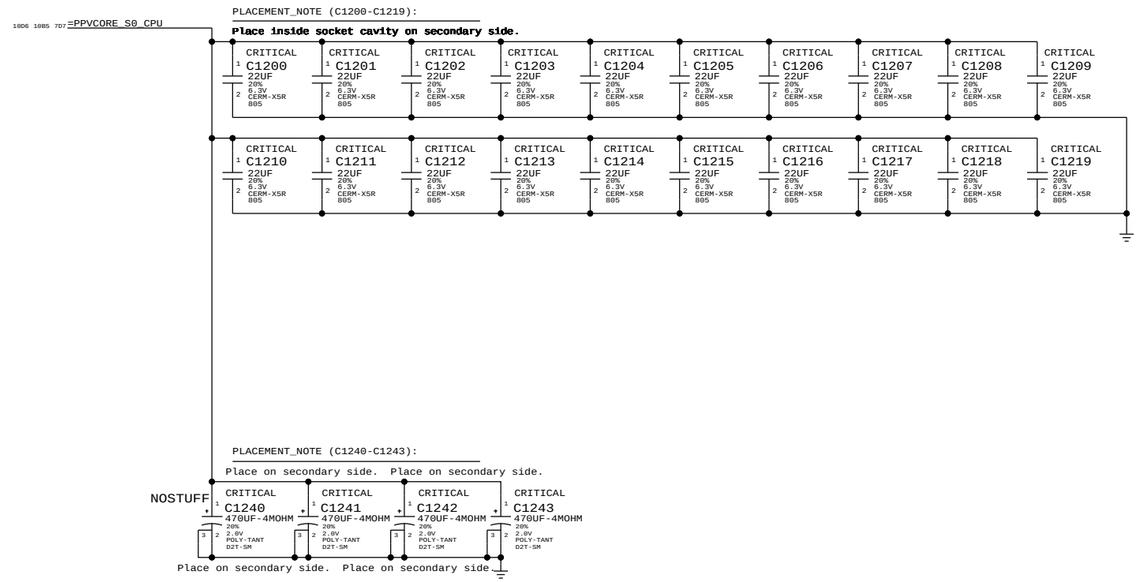
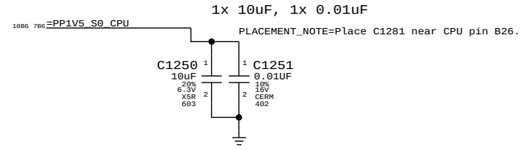
CPU VCore HF and Bulk Decoupling

4X 330UF. 20X 22UF 0805



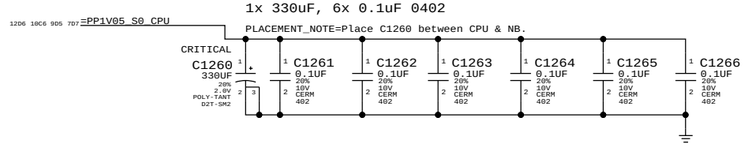
VCCA (CPU AVdd) DECOUPLING

1x 10uF, 1x 0.01uF



VCCP (CPU I/O) DECOUPLING

1x 330uF, 6x 0.1uF 0402



SYNC FROM T18
REMOVE NO STUFF CAPS C1220 TO C1231
REMOVE C1244 & C1245
CHANGE C1240-C1243 AND C1260 FROM 128S0241(9 MILLI-OHM) TO 128S0231(6 MILLI-OHM)

SYNC_MASTER=RAYMOND SYNC_DATE=03/31/2008

PAGE TITLE: CPU Decoupling

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DRAWING NUMBER: 051-7898 SIZE: D

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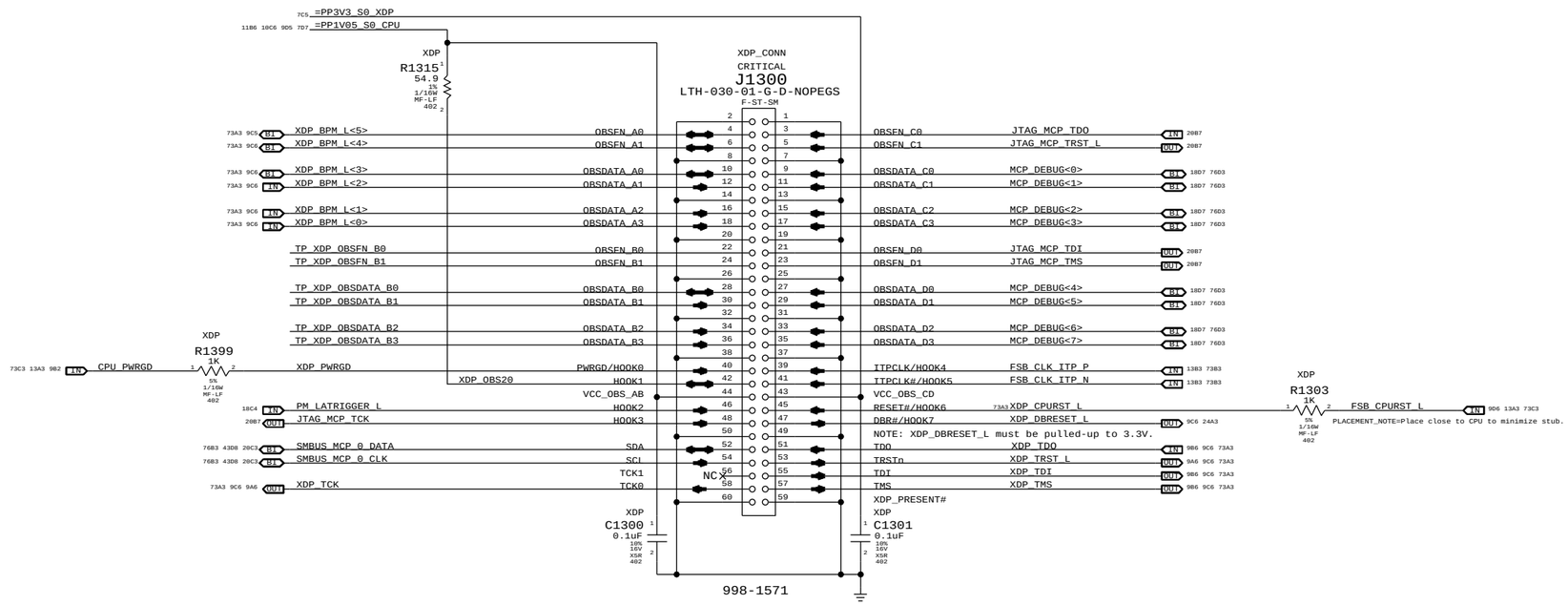
Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0620 adapter board to support CPU, MCP debugging.

MCP79-specific pinout



Direction of XDP module

Please avoid any obstructions on even-numbered side of J1300

SYNC_MASTER=K19_MLB SYNC_DATE=11/07/2008

PAGE TITLE: eXtended Debug Port(MiniXDP)

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

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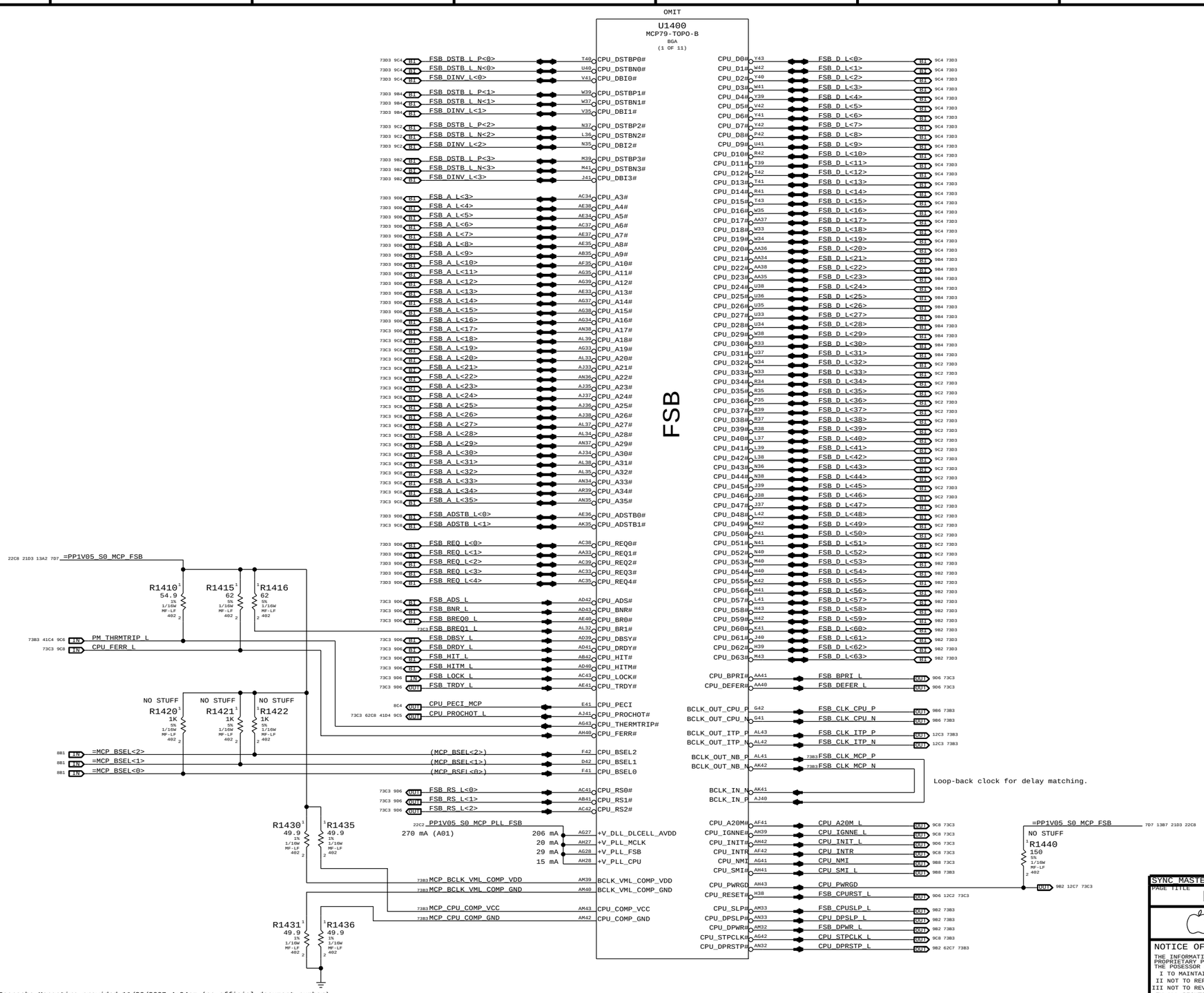

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SYNC MASTER=T18 MLB SYNC DATE=04/04/2008

PAGE TITLE

MCP CPU Interface

Apple Inc.

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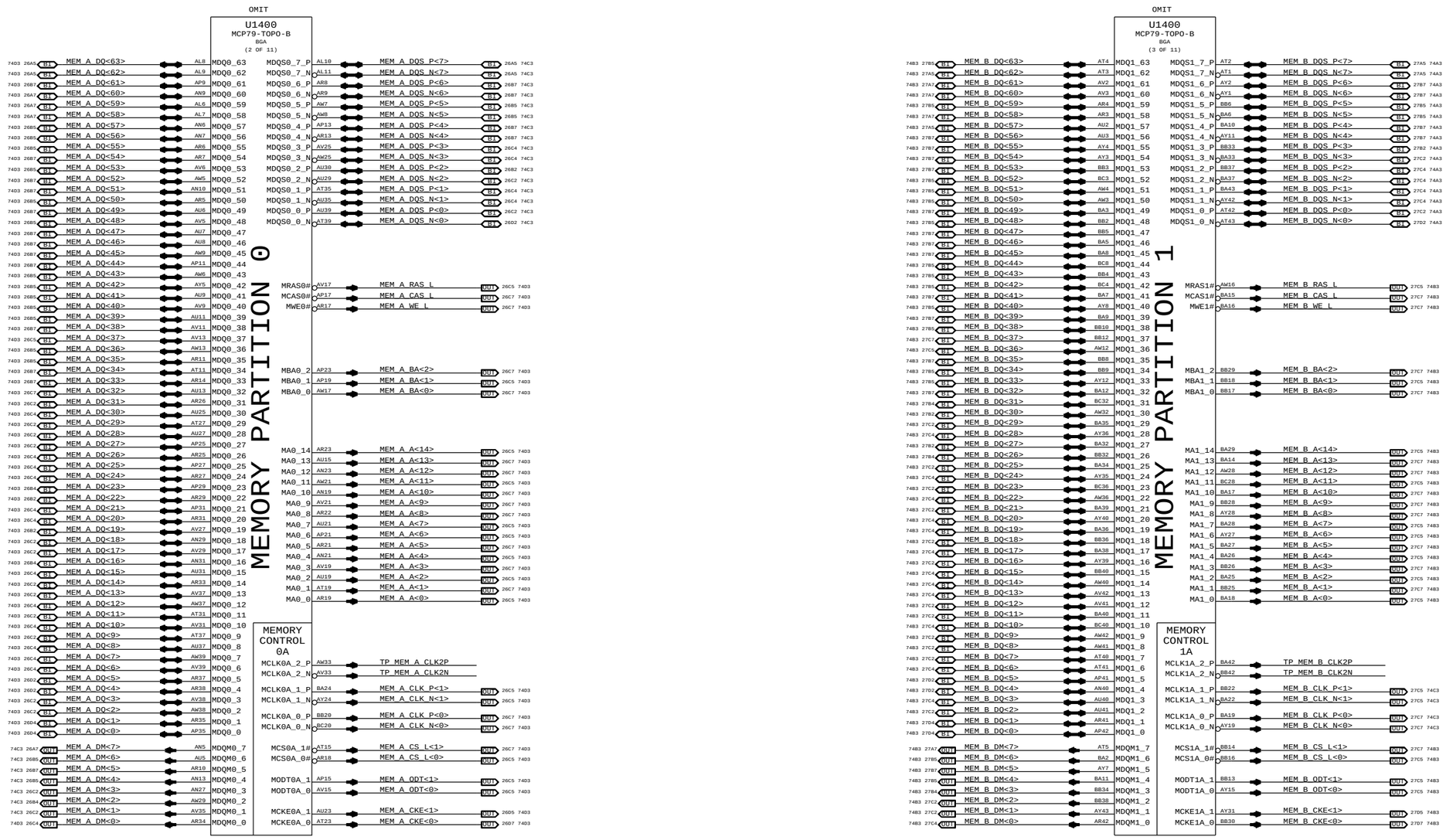

SYNC MASTER=T18 MLB SYNC DATE=04/04/2008

PAGE TITLE
MCP Memory Interface

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

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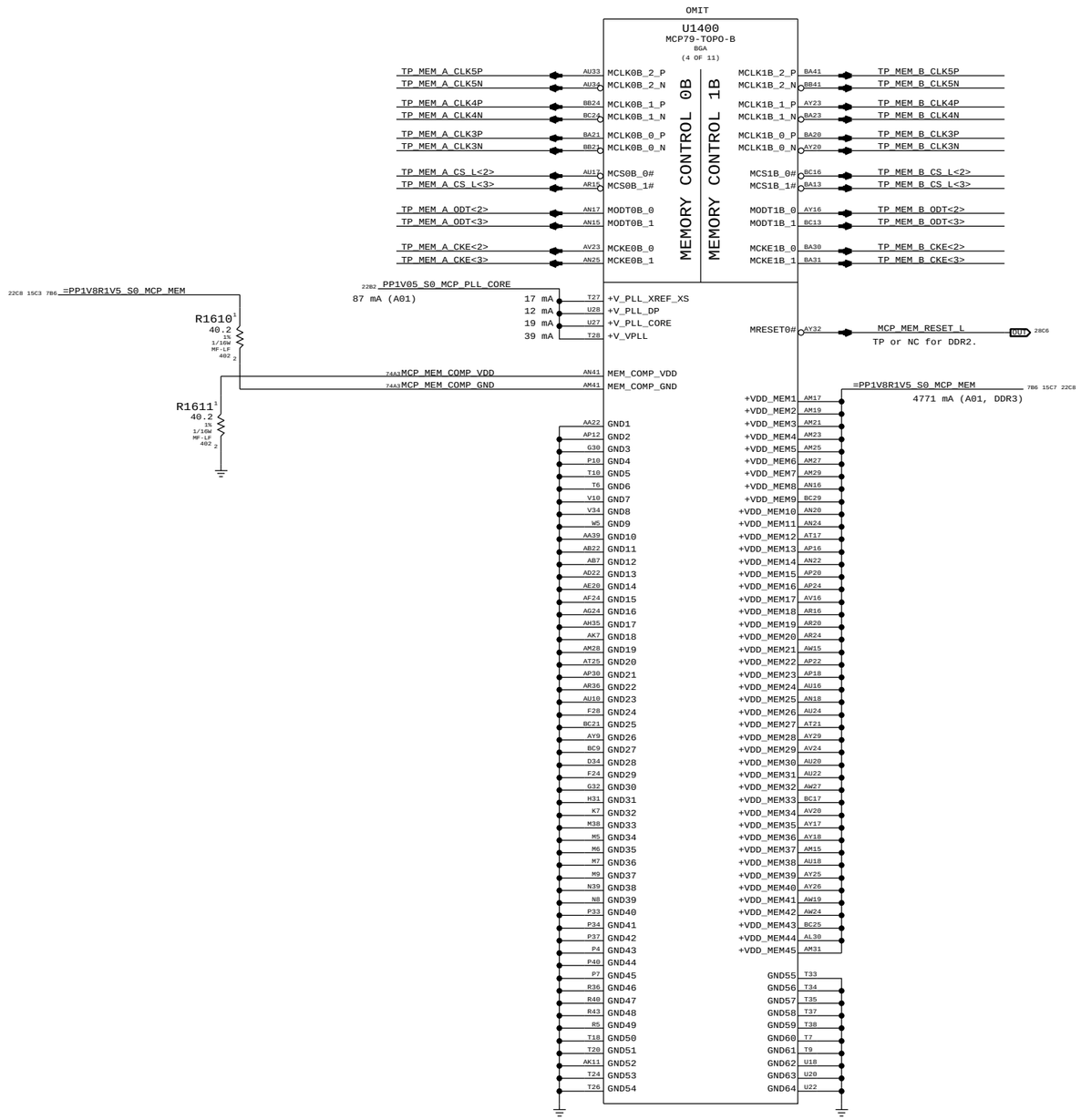

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SYNC MASTER=T18 MLB SYNC DATE=04/04/2008

PAGE TITLE
MCP Memory Misc

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

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OMIT

U1400
MCP79-TOPO-B
BGA
(5 OF 11)

PCI EXPRESS

8D6	IN	=PEG_D2R_P<0>	F7	PE0_RX0_P	C5	PE0_TX0_P	=PEG_R2D_C_P<0>	OUT 8D6
8D6	IN	=PEG_D2R_N<0>	E7	PE0_RX0_N	D4	PE0_TX0_N	=PEG_R2D_C_N<0>	OUT 8D6
8D6	IN	=PEG_D2R_P<1>	D7	PE0_RX1_P	C4	PE0_TX1_P	=PEG_R2D_C_P<1>	OUT 8D6
8D6	IN	=PEG_D2R_N<1>	C7	PE0_RX1_N	B4	PE0_TX1_N	=PEG_R2D_C_N<1>	OUT 8D6
8D6	IN	=PEG_D2R_P<2>	E6	PE0_RX2_P	A4	PE0_TX2_P	=PEG_R2D_C_P<2>	OUT 8D6
8D6	IN	=PEG_D2R_N<2>	F6	PE0_RX2_N	A3	PE0_TX2_N	=PEG_R2D_C_N<2>	OUT 8D6
8D6	IN	=PEG_D2R_P<3>	E5	PE0_RX3_P	B3	PE0_TX3_P	=PEG_R2D_C_P<3>	OUT 8D6
8D6	IN	=PEG_D2R_N<3>	F5	PE0_RX3_N	B2	PE0_TX3_N	=PEG_R2D_C_N<3>	OUT 8D6
8D6	IN	=PEG_D2R_P<4>	E4	PE0_RX4_P	C1	PE0_TX4_P	=PEG_R2D_C_P<4>	OUT 8D6
8D6	IN	=PEG_D2R_N<4>	E3	PE0_RX4_N	D1	PE0_TX4_N	=PEG_R2D_C_N<4>	OUT 8D6
8D6	IN	=PEG_D2R_P<5>	C3	PE0_RX5_P	D2	PE0_TX5_P	=PEG_R2D_C_P<5>	OUT 8D6
8D6	IN	=PEG_D2R_N<5>	D3	PE0_RX5_N	E1	PE0_TX5_N	=PEG_R2D_C_N<5>	OUT 8D6
8D6	IN	=PEG_D2R_P<6>	G5	PE0_RX6_P	E2	PE0_TX6_P	=PEG_R2D_C_P<6>	OUT 8D6
8D6	IN	=PEG_D2R_N<6>	H5	PE0_RX6_N	F2	PE0_TX6_N	=PEG_R2D_C_N<6>	OUT 8D6
8D6	IN	=PEG_D2R_P<7>	J7	PE0_RX7_P	F3	PE0_TX7_P	=PEG_R2D_C_P<7>	OUT 8D6
8D6	IN	=PEG_D2R_N<7>	J6	PE0_RX7_N	E4	PE0_TX7_N	=PEG_R2D_C_N<7>	OUT 8D6
8D6	IN	=PEG_D2R_P<8>	J5	PE0_RX8_P	G3	PE0_TX8_P	=PEG_R2D_C_P<8>	OUT 8D6
8D6	IN	=PEG_D2R_N<8>	J4	PE0_RX8_N	H4	PE0_TX8_N	=PEG_R2D_C_N<8>	OUT 8D6
8D6	IN	=PEG_D2R_P<9>	L11	PE0_RX9_P	H3	PE0_TX9_P	=PEG_R2D_C_P<9>	OUT 8D6
8D6	IN	=PEG_D2R_N<9>	L10	PE0_RX9_N	H2	PE0_TX9_N	=PEG_R2D_C_N<9>	OUT 8D6
8D6	IN	=PEG_D2R_P<10>	L9	PE0_RX10_P	H1	PE0_TX10_P	=PEG_R2D_C_P<10>	OUT 8D6
8D6	IN	=PEG_D2R_N<10>	L8	PE0_RX10_N	J1	PE0_TX10_N	=PEG_R2D_C_N<10>	OUT 8D6
8D6	IN	=PEG_D2R_P<11>	L7	PE0_RX11_P	J2	PE0_TX11_P	=PEG_R2D_C_P<11>	OUT 8D6
8D6	IN	=PEG_D2R_N<11>	L6	PE0_RX11_N	J3	PE0_TX11_N	=PEG_R2D_C_N<11>	OUT 8D6
8D6	IN	=PEG_D2R_P<12>	N11	PE0_RX12_P	K2	PE0_TX12_P	=PEG_R2D_C_P<12>	OUT 8D6
8D6	IN	=PEG_D2R_N<12>	N10	PE0_RX12_N	K3	PE0_TX12_N	=PEG_R2D_C_N<12>	OUT 8D6
8D6	IN	=PEG_D2R_P<13>	N9	PE0_RX13_P	L4	PE0_TX13_P	=PEG_R2D_C_P<13>	OUT 8D6
8D6	IN	=PEG_D2R_N<13>	P9	PE0_RX13_N	L3	PE0_TX13_N	=PEG_R2D_C_N<13>	OUT 8D6
8D6	IN	=PEG_D2R_P<14>	N7	PE0_RX14_P	M4	PE0_TX14_P	=PEG_R2D_C_P<14>	OUT 8D6
8D6	IN	=PEG_D2R_N<14>	N6	PE0_RX14_N	M3	PE0_TX14_N	=PEG_R2D_C_N<14>	OUT 8D6
8D6	IN	=PEG_D2R_P<15>	N5	PE0_RX15_P	M2	PE0_TX15_P	=PEG_R2D_C_P<15>	OUT 8D6
8D6	IN	=PEG_D2R_N<15>	N4	PE0_RX15_N	M1	PE0_TX15_N	=PEG_R2D_C_N<15>	OUT 8D6
8D6	IN	PEG_PRSNT_L	C9	Int PU PE0_PRSNT_16#	E11	PE0_REFCLK_P	PEG_CLK100M_P	OUT 8D6
					D11	PE0_REFCLK_N	PEG_CLK100M_N	OUT 8D6
2907	IN	MINI_CLKREQ_L	D5	Int PU PEB_CLKREQ#/GPIO_49	G11	PE1_REFCLK_P	PCIE_CLK100M_MINI_P	OUT 29C5 75D3
2907	IN	PCIE_MINI_PRSNT_L	D9	PEB_PRSNT# Int PU	F11	PE1_REFCLK_N	PCIE_CLK100M_MINI_N	OUT 29C5 75D3
3503	IN	FW_CLKREQ_L	E8	Int PU PEC_CLKREQ#/GPIO_50	J11	PE2_REFCLK_P	PCIE_CLK100M_FW_P	OUT 34C2
3503 8C6	IN	PCIE_FW_PRSNT_L	C10	PEC_PRSNT# Int PU	J10	PE2_REFCLK_N	PCIE_CLK100M_FW_N	OUT 34C2
8D6	IN	EXCARD_CLKREQ_L	M15	Int PU PED_CLKREQ#/GPIO_51	G13	PE3_REFCLK_P	PCIE_CLK100M_EXCARD_P	OUT 8D6
8D6	IN	PCIE_EXCARD_PRSNT_L	B10	PED_PRSNT# Int PU	F13	PE3_REFCLK_N	PCIE_CLK100M_EXCARD_N	OUT 8C6
		TP_PE4_CLKREQ_L	L16	Int PU PEE_CLKREQ#/GPIO_16	J13	PE4_REFCLK_P	TP_PCIE_CLK100M_PE4P	
		TP_PE4_PRSNT_L	L18	PEE_PRSNT#/GPIO_46 Int PU	H13	PE4_REFCLK_N	TP_PCIE_CLK100M_PE4N	
57A4		AUD_IP_PERIPHERAL_DET	M16	Int PU PEF_CLKREQ#/GPIO_17	L14	PE5_REFCLK_P	TP_PCIE_CLK100M_PE5P	
8C4	OUT	GMUX_JTAG_TCK_L	M18	PEF_PRSNT#/GPIO_47 Int PU	K14	PE5_REFCLK_N	TP_PCIE_CLK100M_PE5N	
30B7	OUT	CARDREADER_RESET	M17	Int PU PEG_CLKREQ#/GPIO_18	N14	PE6_REFCLK_P	TP_PCIE_CLK100M_PE6P	
8C4	IN	GMUX_JTAG_TDO	M19	PEG_PRSNT#/GPIO_48 Int PU	M14	PE6_REFCLK_N	TP_PCIE_CLK100M_PE6N	
29C7 6D5	IN	PCIE_WAKE_L	F17	PE_WAKE# Int PU (S5)	K11	PEX_RST0#	PCIE_RESET_L	OUT 24C4
75D3 29C7 6D5	IN	PCIE_MINI_D2R_P	K9	PE1_RX0_P	D8	PE1_TX0_P	PCIE_MINI_R2D_C_P	OUT 29C5 75D3
75D3 29C7 6D5	IN	PCIE_MINI_D2R_N	J9	PE1_RX0_N	C8	PE1_TX0_N	PCIE_MINI_R2D_C_N	OUT 29C5 75D3
75D3 34C1	IN	PCIE_FW_D2R_P	H9	PE1_RX1_P	B8	PE1_TX1_P	PCIE_FW_R2D_C_P	OUT 34C1 75D3
75D3 34C1	IN	PCIE_FW_D2R_N	G9	PE1_RX1_N	A8	PE1_TX1_N	PCIE_FW_R2D_C_N	OUT 34C1 75D3
8D6	IN	PCIE_EXCARD_D2R_P	F9	PE1_RX2_P	A7	PE1_TX2_P	PCIE_EXCARD_R2D_C_P	OUT 8D6
8D6	IN	PCIE_EXCARD_D2R_N	E9	PE1_RX2_N	B7	PE1_TX2_N	PCIE_EXCARD_R2D_C_N	OUT 8D6
		TP_PCIE_PE4_D2RP	H7	PE1_RX3_P	B6	PE1_TX3_P	TP_PCIE_PE4_R2D_CP	
		TP_PCIE_PE4_D2RN	G7	PE1_RX3_N	C6	PE1_TX3_N	TP_PCIE_PE4_R2D_CN	

7A6 =PP1V05_S0_MCP_PEX_DVDD0
57 mA (A01, DVDD0 & 1)

T17	+DVDD0_PEX1
W19	+DVDD0_PEX2
U17	+DVDD0_PEX3
V19	+DVDD0_PEX4
W16	+DVDD0_PEX5
W17	+DVDD0_PEX6
W18	+DVDD0_PEX7
U16	+DVDD0_PEX8

7A6 =PP1V05_S0_MCP_PEX_DVDD1

T19	+DVDD1_PEX1
U19	+DVDD1_PEX2

22C2 PP1V05_S0_MCP_PLL_PEX
84 mA (A01)

T16	+V_PLL_PEX

75C3 MCP_PEX_CLK_COMP

A11	PEX_CLK_COMP

+AVDD0_PEX1	Y12
+AVDD0_PEX2	AA12
+AVDD0_PEX3	AB12
+AVDD0_PEX4	M12
+AVDD0_PEX5	P12
+AVDD0_PEX6	R12
+AVDD0_PEX7	N12
+AVDD0_PEX8	T12
+AVDD0_PEX9	U12
+AVDD0_PEX10	AC12
+AVDD0_PEX11	AD12
+AVDD0_PEX12	V12
+AVDD0_PEX13	W12
+AVDD1_PEX1	M13
+AVDD1_PEX2	N13
+AVDD1_PEX3	P13

=PP1V05_S0_MCP_PEX_AVDD0 7A6
206 mA (A01, AVDD0 & 1)

=PP1V05_S0_MCP_PEX_AVDD1 7A6

NO STUFF
1 R1710 2
2.37K
1%
1/16W
MF-LF
402
PLACEMENT_NOTE=Place within 12.7mm of U1400

If PE0 interface is not used, ground DVDD0_PEX and AVDD0_PEX.
If PE1 interface is not used, ground DVDD1_PEX and AVDD1_PEX.

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

PAGE TITLE
MCP PCIe Interfaces

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D
REVISION C.0.0
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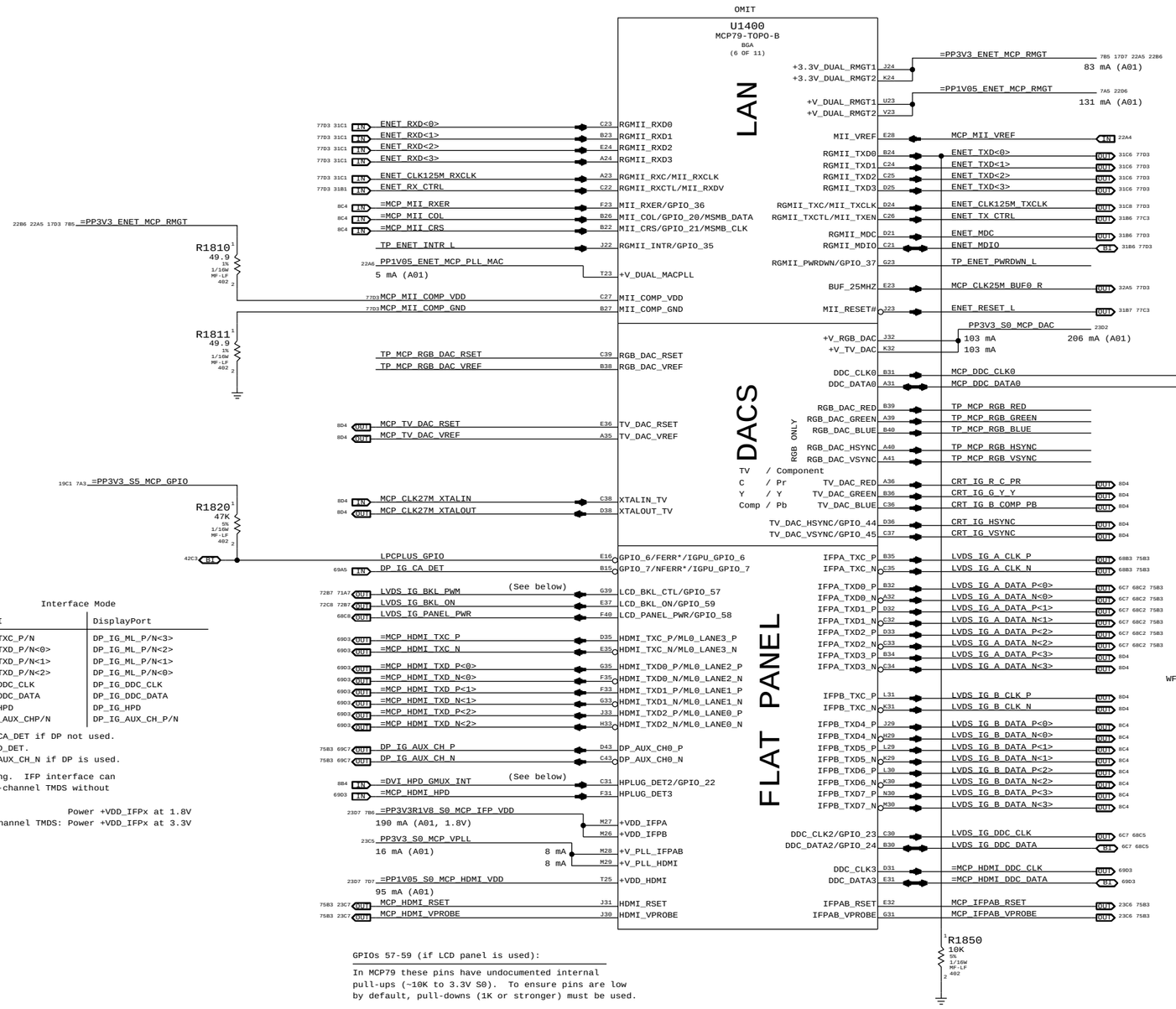
PAGE 17 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



Network Interface Select

Interface	ENET_TXD<0>
RGMII	1
MII	0

NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

RGB DAC Disable:

Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required.

TV DAC Disable:

Okay to float all TV_DAC signals.
Okay to float XTALIN_TV and XTALOUT_TV.
DDC_CLK0/DDC_DATA0 pull-ups still required.

WF: IFP is capable of LVDS (1.8V) or TMDS (3.3V), need aliases

Interface Mode

MCP Signal	TMDS/HDMI	DisplayPort
=MCP_HDMI_TXC_P/N	TMDS_IG_TXC_P/N	DP_IG_ML_P/N<3>
=MCP_HDMI_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	DP_IG_ML_P/N<2>
=MCP_HDMI_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	DP_IG_ML_P/N<1>
=MCP_HDMI_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	DP_IG_ML_P/N<0>
=MCP_HDMI_DDC_CLK	TMDS_IG_DDC_CLK	DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA	TMDS_IG_DDC_DATA	DP_IG_DDC_DATA
=MCP_HDMI_HPD	TMDS_IG_HPD	DP_IG_HPD
DP_IG_AUX_CH_P/N	TP_DP_IG_AUX_CHP/N	DP_IG_AUX_CH_P/N

NOTE: 1M pull-down required on DP_IG_CA_DET if DP not used.
NOTE: 20K pull-down required on DP_HPD_DET.
NOTE: 1K pull-down required on DP_IG_AUX_CH_N if DP is used.

NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.

LVDS: Power +VDD_IFPx at 1.8V
Dual-channel TMDS: Power +VDD_IFPx at 3.3V

GPIOs 57-59 (if LCD panel is used):

In MCP79 these pins have undocumented internal pull-ups (~10K to 3.3V S0). To ensure pins are low by default, pull-downs (1K or stronger) must be used.

=DVI_HPD_GMUX_INT:

Alias to DVI_HPD for systems using IFP for DVI.
Alias to GMUX_INT for systems with GMUX.
Alias to HPLUG_DET2 for other systems.
Pull-down (20k) required in all cases.

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

SYNC MASTER=T18 MLB SYNC DATE=04/04/2008

PAGE TITLE
MCP Ethernet & Graphics

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D
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PAGE 18 OF 109
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SYNC MASTER=T18_MLB SYNC DATE=04/04/2008

PAGE TITLE

MCP PCI & LPC

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

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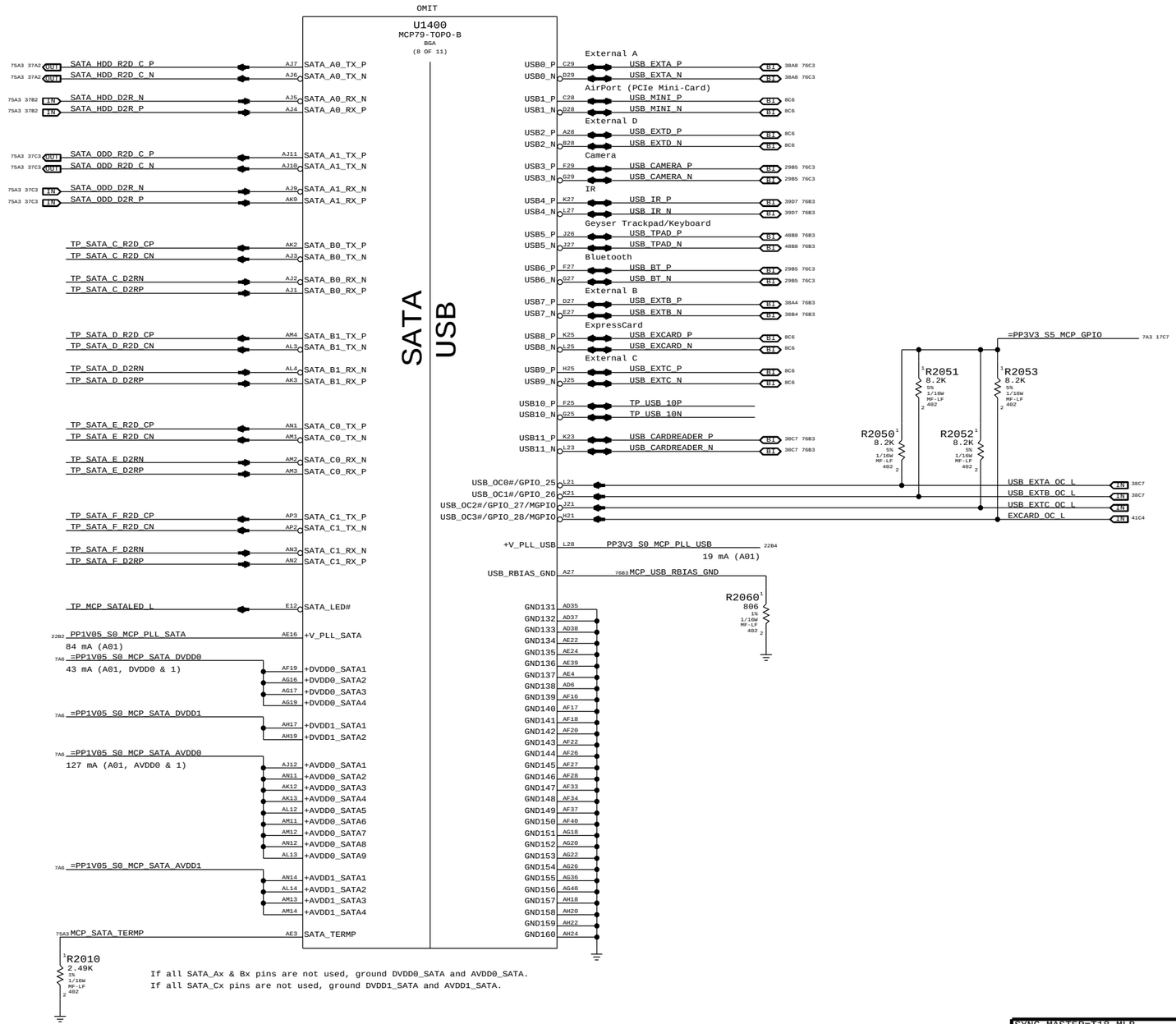

If all SATA_Ax & Bx pins are not used, ground DVDD0_SATA and AVDD0_SATA.
If all SATA_Cx pins are not used, ground DVDD1_SATA and AVDD1_SATA.

SYNC MASTER=T18_MLB	SYNC DATE=04/04/2008
PAGE TITLE: MCP SATA & USB	
Apple Inc.	DRAWING NUMBER: 051-7898 SIZE: D
	REVISION: C.0.0
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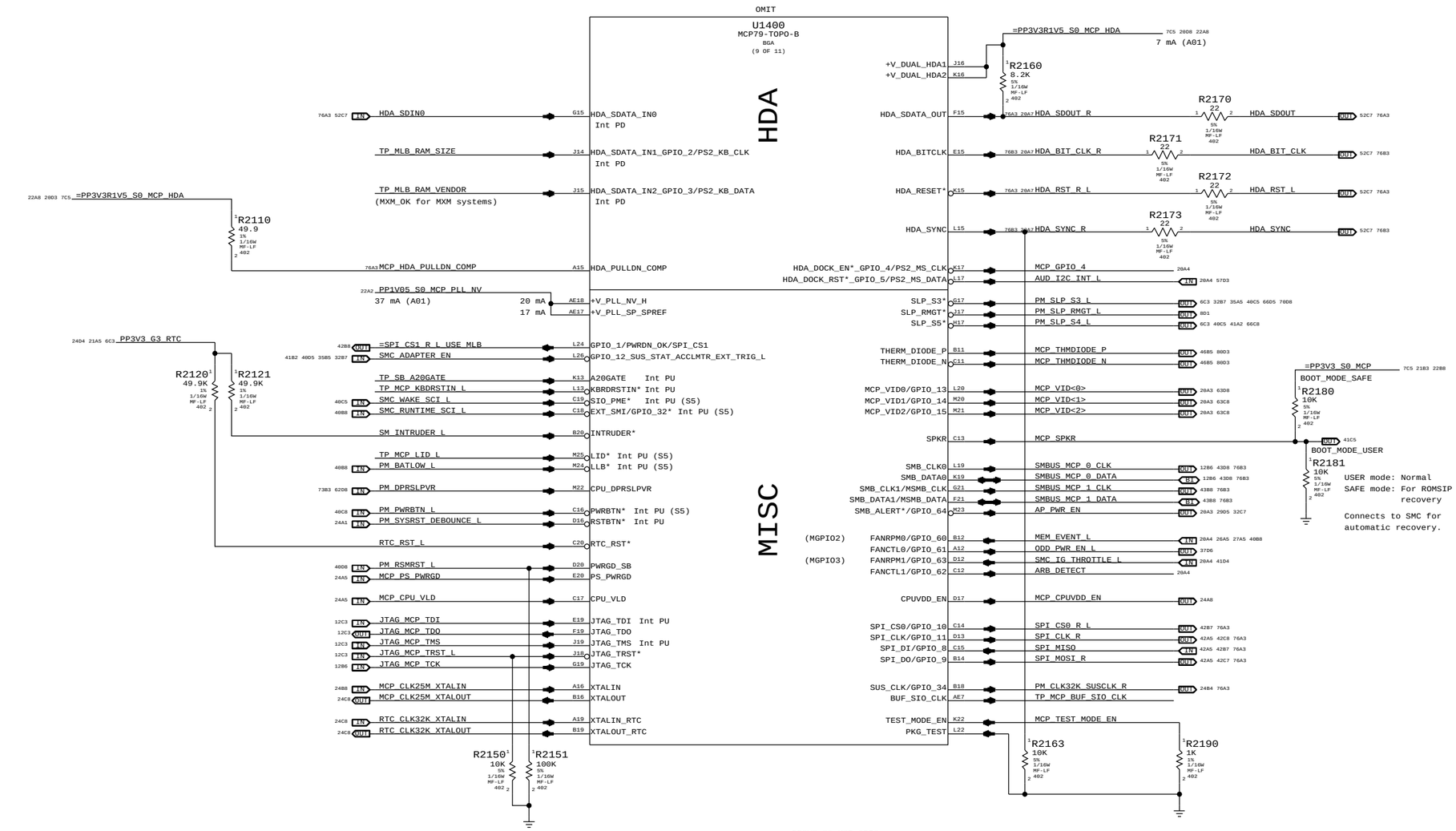


BIOS Boot Select

I/F	HDA_SDOUT	LPC_FRAME#
LPC	0	0
PCI	0	1
SPI0	1	0
SPI1	1	1

SPI0 = SPI_CS0_L, SPI1 = SPI_CS1_L

R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC_FRAME# high for SPI1 ROM override.

NOTE: MCP79 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.

NOTE: MCP79 rev A01 does not support SPI1 option. Rev B01 will.

BUF_SIO_CLK Frequency

Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

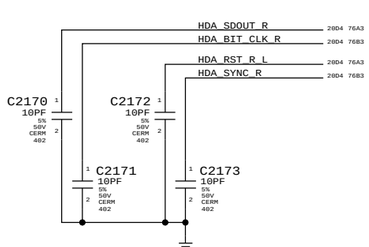
SPI Frequency Select

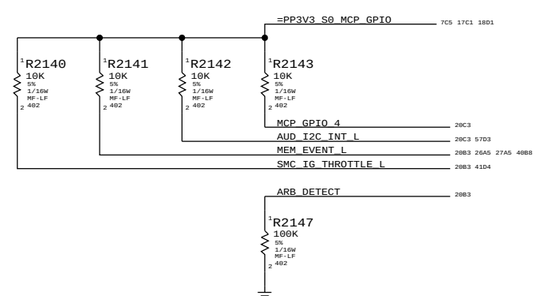
Frequency	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

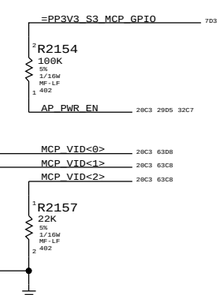
NOTE: Straps not provided on this page.

HDA Output Caps

For EMI Reduction on HDA interface







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SYNC MASTER=T18_MLB SYNC DATE=06/26/2008

PAGE TITLE: MCP HDA & MISC

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

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PAGE: 21 OF 109

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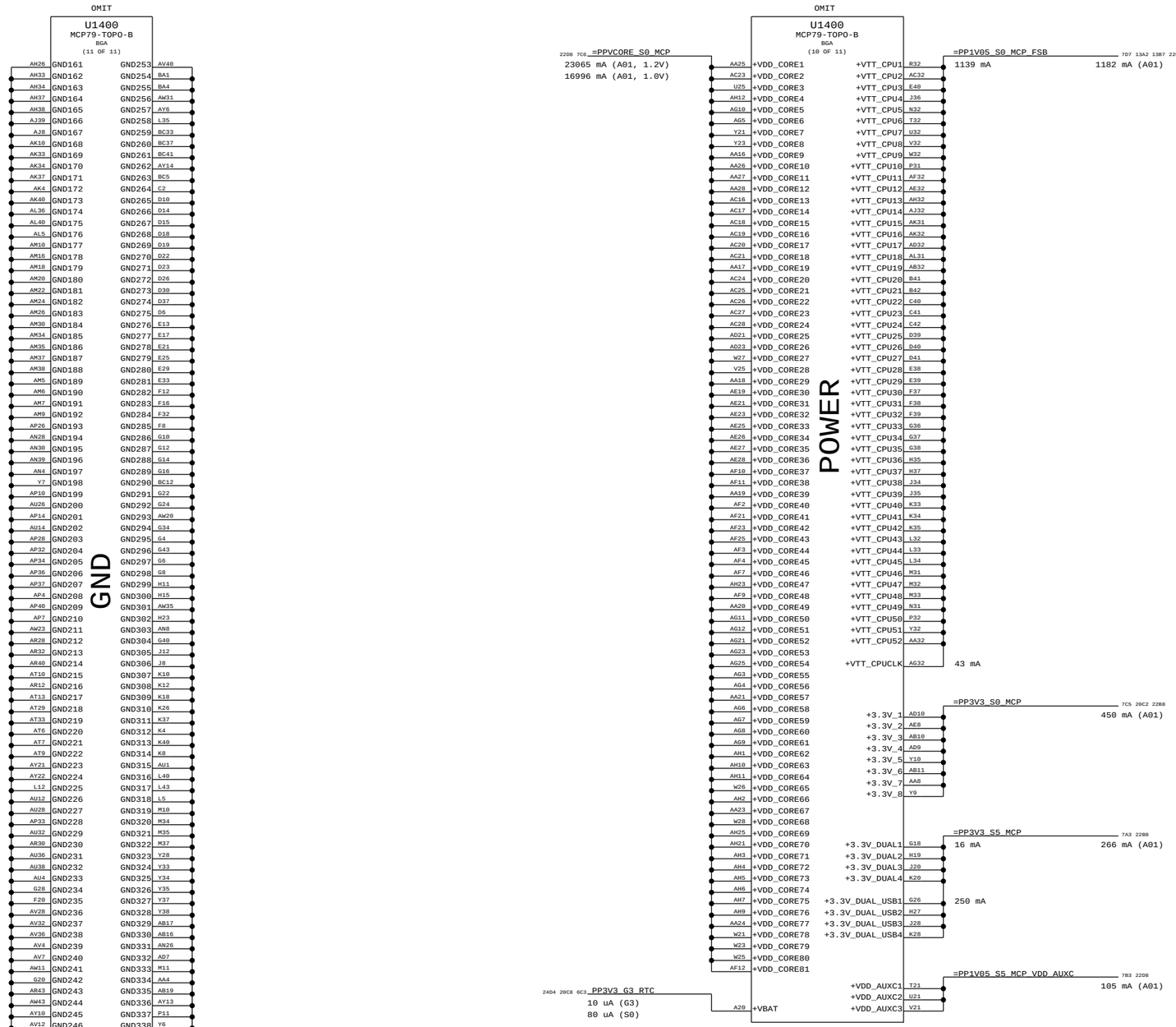

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SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

PAGE TITLE
MCP Power & Ground

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

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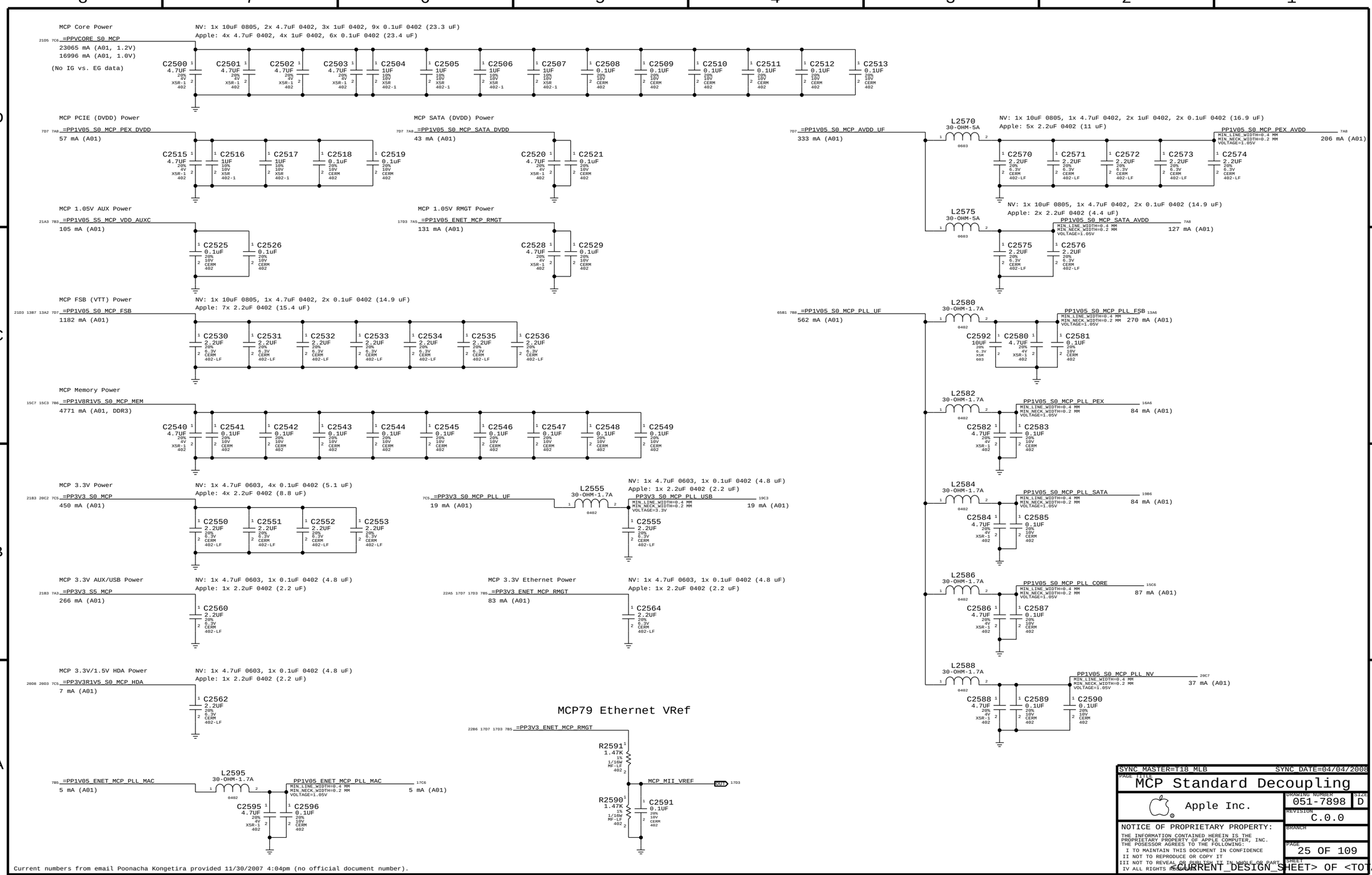

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SYNC MASTER=I18_MLB SYNC DATE=04/04/2008

PAGE TITLE
MCP Standard Decoupling

Apple Inc.

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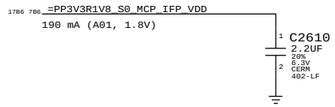
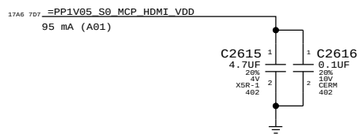
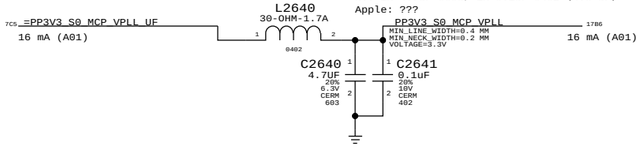
WF: Checklist says 0-ohm resistor placeholder for ferrite bead.
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

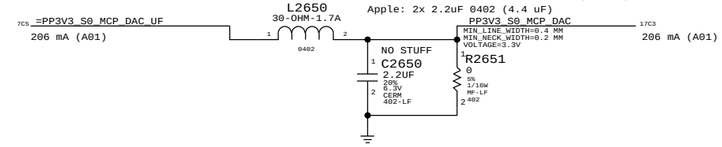




WF: Checklist says 0-ohm resistor placeholder for ferrite bead.
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: ???



NO STUFF
NV: 1x 4.7uF 0603, 2x 0.1uF 0402 (4.9 uF)
Apple: 2x 2.2uF 0402 (4.4 uF)



SYNC FROM T18
REMOVE MCP 27MHZ CRYSTAL CRICUIT SINCE NOT SUPPORTING TV-OUT
REMOVE DAC TERMINATIONS R2665,C2665 AND R2670 TO R2672
NOSTUFF PP3V3_S0_MCP_DAC RAIL COMPONENTS (L2650 AND C2650)
CHANGE C2651 TO R2651 TO GND PP3V3_S0_MCP_DAC
REMOVE HDCP ROMS

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2007

PAGE TITLE: MCP Graphics Support

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D
REVISION: C.0.0
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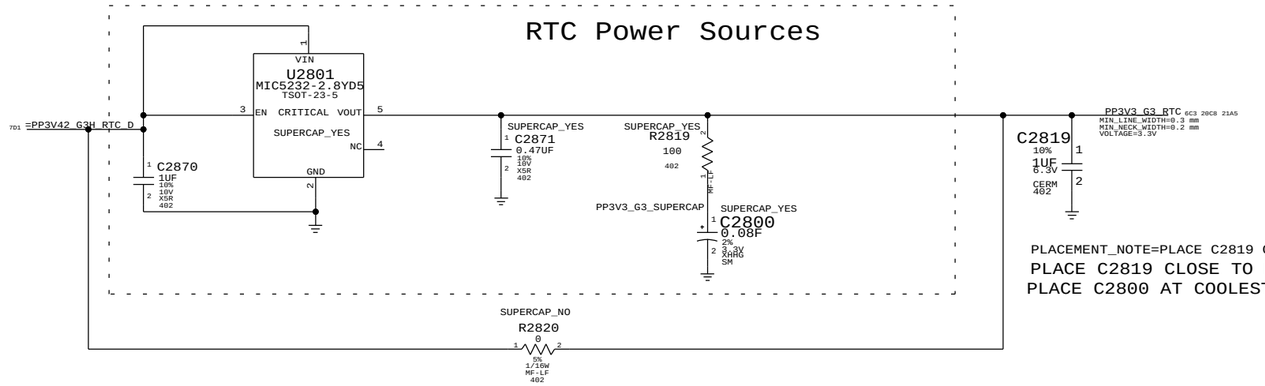
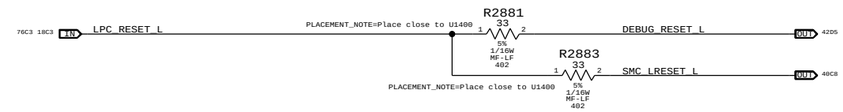


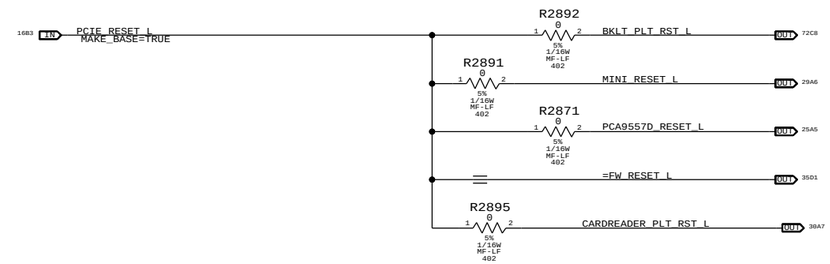
PLACEMENT_NOTE=PLACE C2819 CLOSE TO MCP79
PLACE C2819 CLOSE TO MCP79
PLACE C2800 AT COOLEST SPOT ON MLB

Platform Reset Connections

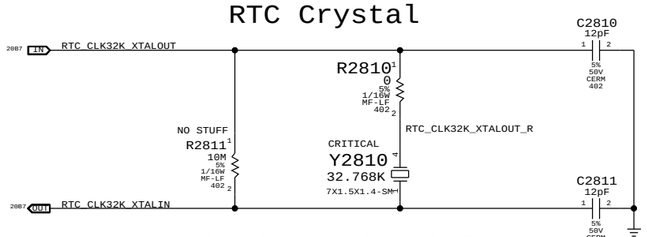
LPC Reset (Unbuffered)



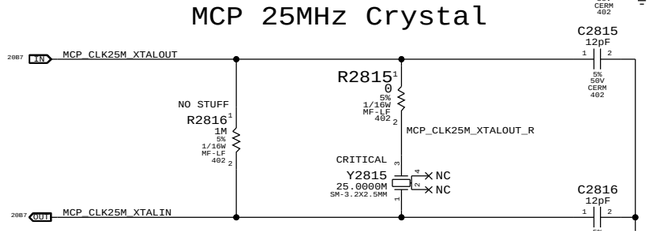
PCIE Reset (Unbuffered)

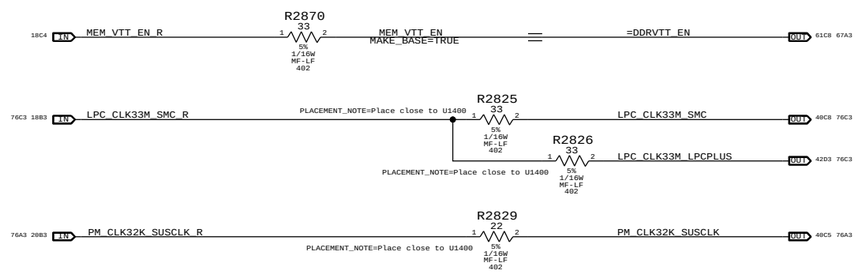


RTC Crystal

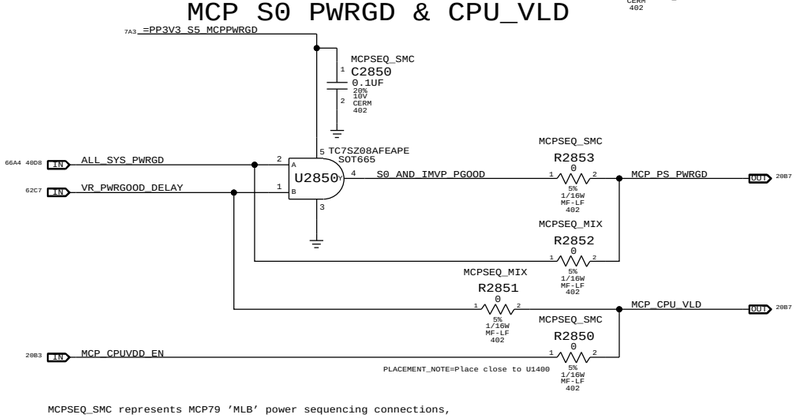


MCP 25MHz Crystal





MCP S0 PWRGD & CPU_VLD



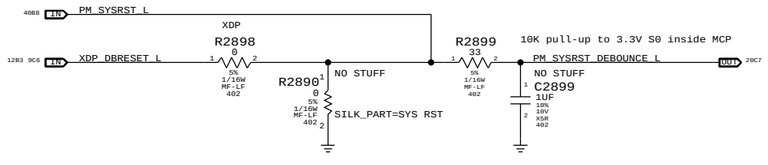
MCPSEQ_SMC represents MCP79 'MLB' power sequencing connections, but results in MCP79 ROMSIP sequence happening after CPU powers up.

MCPSEQ_MIX is cross between MLB and internal power sequencing, which results in earlier ROMSIP and MCP FSB I/O interface initialization.

SMC 99ms delay from ALL_SYS_PWRGD to IMVP_VR_ON plus IMVP6 delay for VR_PWRGOOD_DELAY should guarantee CPU_VLD does not go high before CPUVDD_EN (which is 40-100ms after PS_PWRGD assertion).

NOTE: If CPU_VLD deasserts during S0 MCP79 will take system to S5 immediately.

Reset Button



SYNC FROM T18
CHANGE RESET BUTTOM TO RESET PADS
REMOVE UNUSED PCIE RESET SIGNALS
REMOVE R2824 AND NET PCI_CLK33M_SLOT_A
CHANGE RTC COIN CELL TO LDO & SUPERCAP
ALIAS MEM_VTT_EN TO =DDRVTT_EN
CHANGE Y2810 AND U2850 TO SMALLER PARTS

SYNC MASTER=RAYMOND	SYNC DATE=04/05/2008
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Page Notes

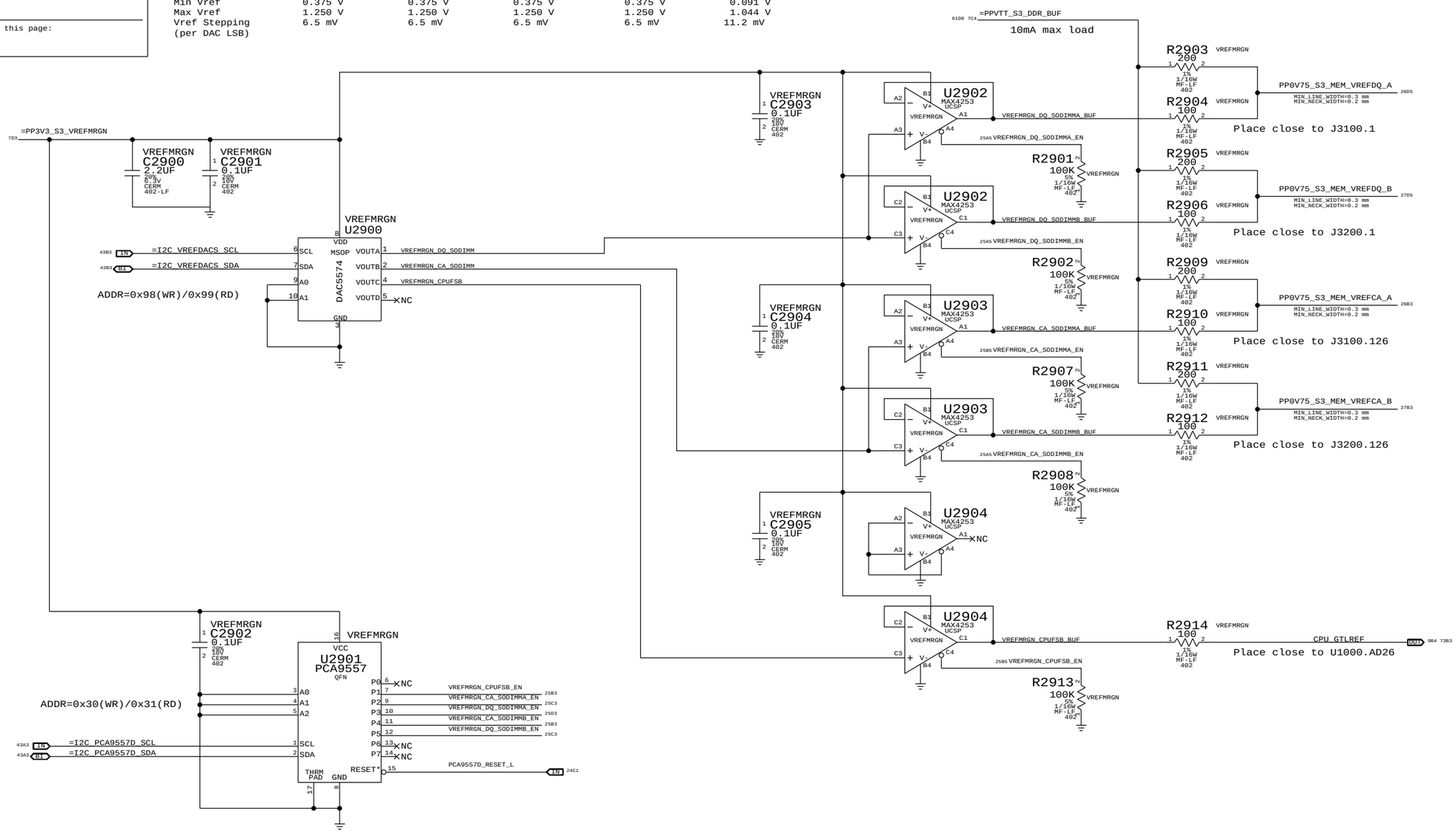
Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PP3V3_S5_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN
NO_VREFMRGN

	MEM A VREF DQ	MEM A VREF CA	MEM B VREF DQ	MEM B VREF CA	CPU FSB VREF
DAC channel	A	B	A	B	C
Min DAC code	0x00	0x00	0x00	0x00	0x00
Max DAC code	0x87	0x87	0x87	0x87	0x55
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA
Max source I	5 mA	5 mA	5 mA	5 mA	0.52 mA
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately
(i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2903	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2905	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2909	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2911	CRITICAL	NO_VREFMRGN

SYNC_MASTER=BEN SYNC_DATE=03/31/2008

PAGE TITLE
FSB/DDR3 Vref Margining

Apple Inc.

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PAGE 29 OF 109
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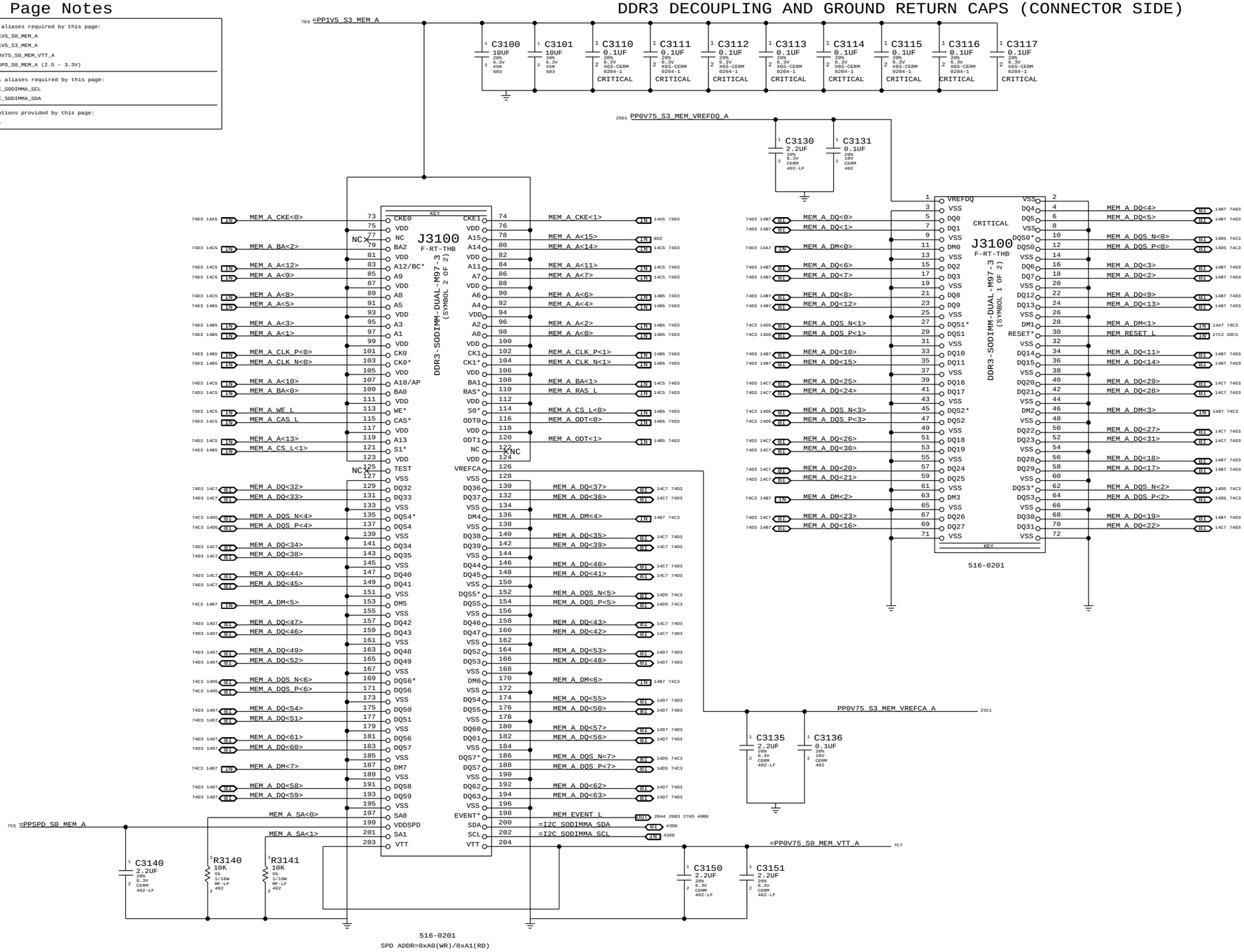
Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)



"Factory" (top) slot

SYNC MASTER=BEN	SYNC DATE=06/30/2008
PAGE TITLE: DDR3 SO-DIMM Connector A	
Apple Inc.	DRAWING NUMBER: 051-7898 SIZE: D
	REVISION: C.0.0
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	PAGE: 31 OF 109
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

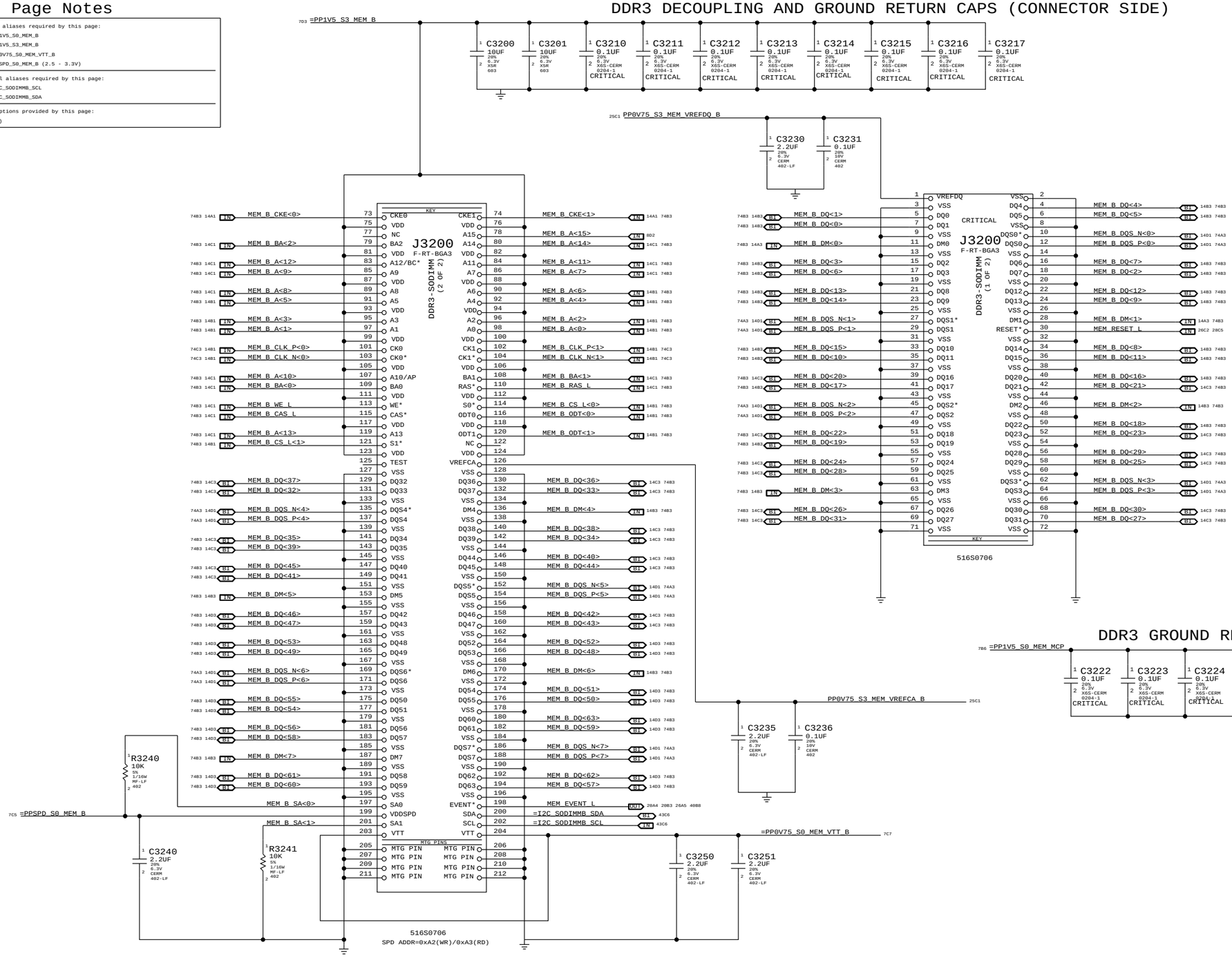
Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

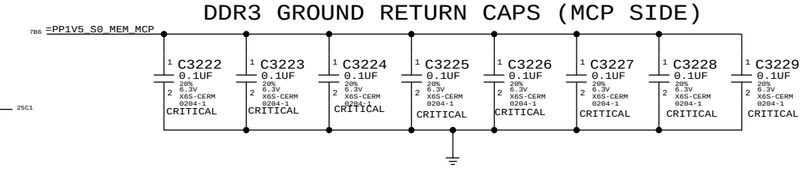
Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)



DDR3 GROUND RETURN CAPS (MCP SIDE)



"Expansion" (bottom) slot

SYNC_MASTER=BEN SYNC_DATE=05/09/2008

PAGE TITLE
DDR3 SO-DIMM Connector B

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D
REVISION C.0.0
BRANCH
PAGE 32 OF 109
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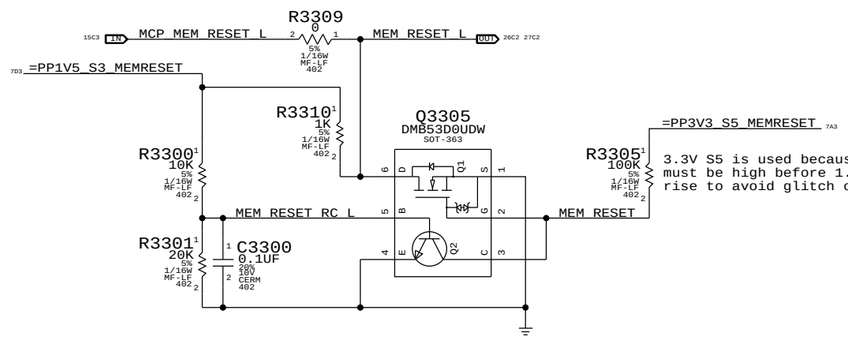
DDR3 RESET Support

Required becaues MCP79 does not meet DDR3 spec power-up reset timing requirement.



3.3V S5 is used because MEM_RESET must be high before 1.5V starts to rise to avoid glitch on MEM_RESET_L.

SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

PAGE TITLE: DDR3 Support

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

BRANCH:

PAGE: 33 OF 109

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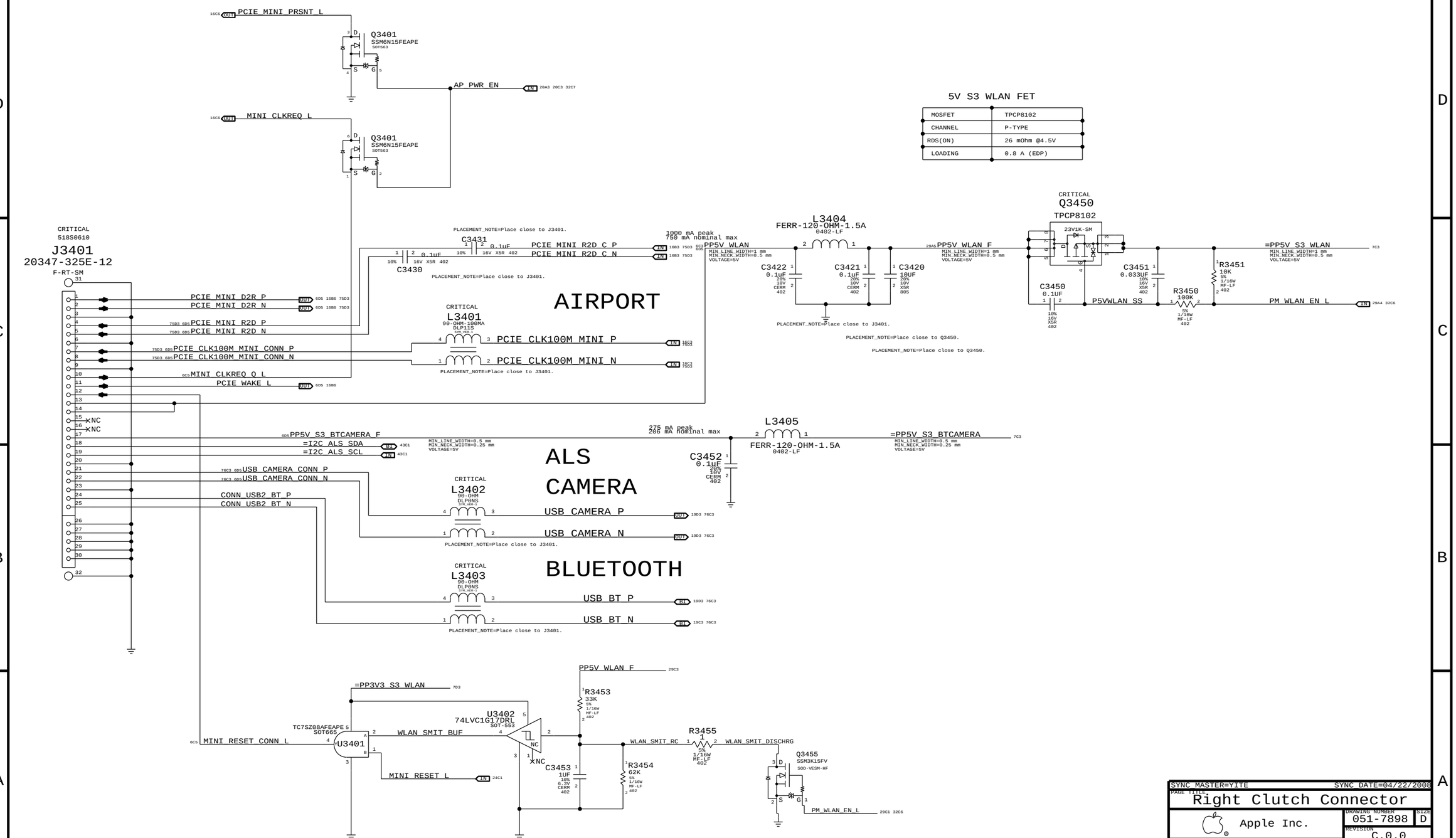

SYNC MASTER=YITE SYNC DATE=04/22/2008

PAGE TITLE
Right Clutch Connector

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

REVISION C.0.0

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PAGE 34 OF 109

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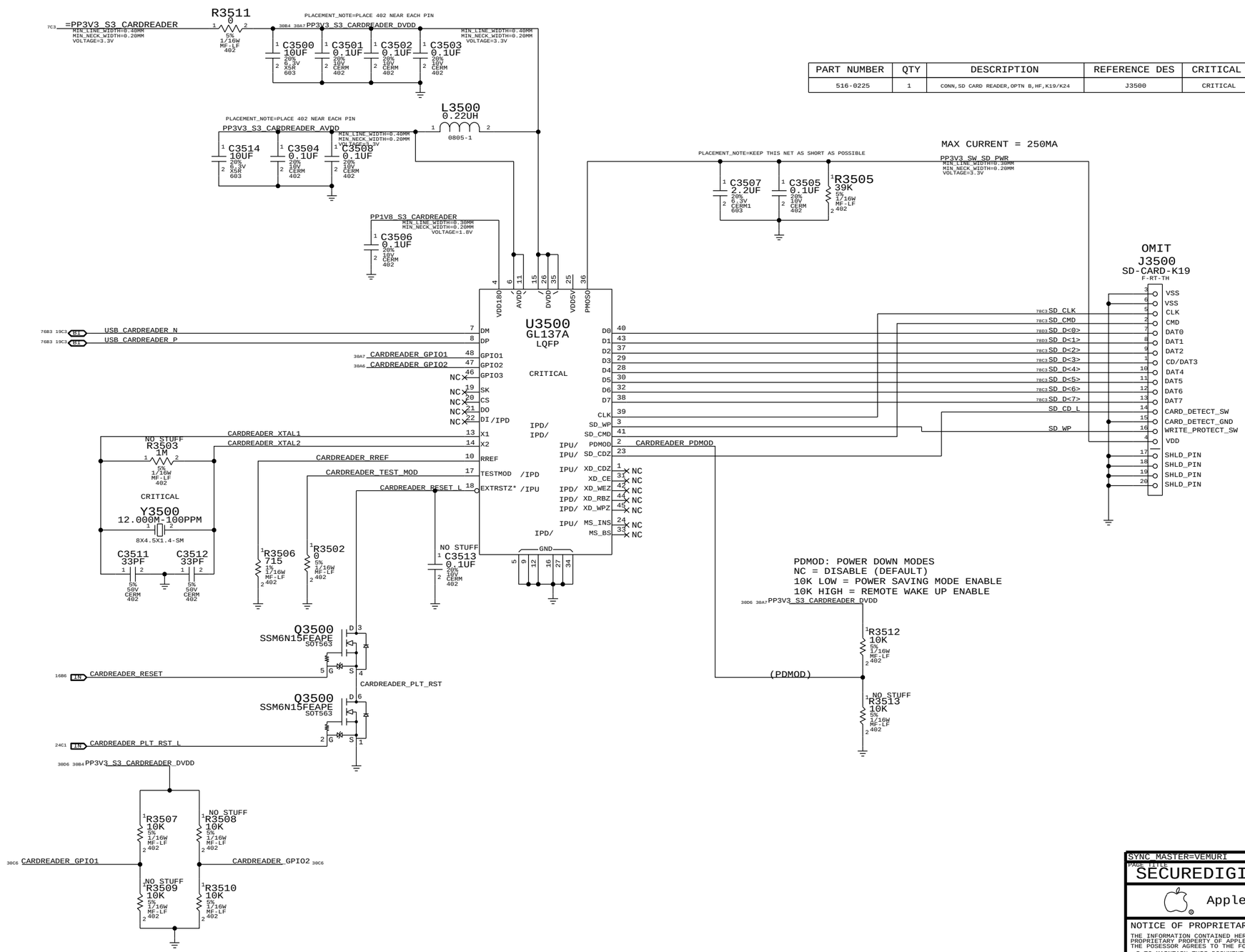
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
516-0225	1	CONN,SD CARD READER,OPTN B,HF,K19/K24	J3500	CRITICAL	



SYNC MASTER=VEMURI SYNC DATE=01/30/2009

PAGE TITLE
SECUREDIGITAL CARD READER

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

REVISION C.0.0

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PAGE 35 OF 109

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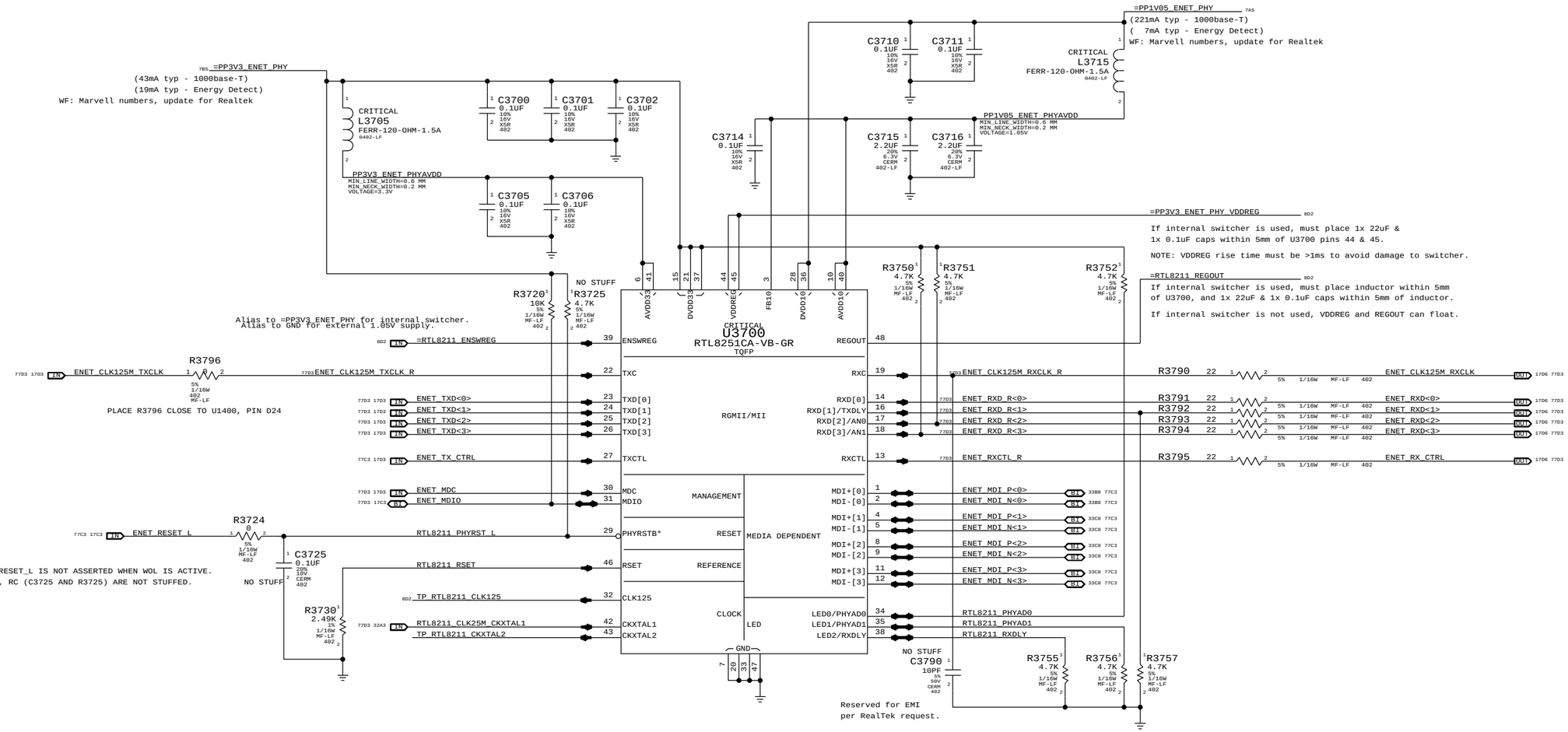

Configuration Settings:

PHYAD = 01 (PHY Address 00001)
AN[1:0] = 11 (Full auto-negotiation)
RXDLY = 0 (RXCLK transitions with data)
TXDLY = 0 (No TXCLK Delay)

SYNC MASTER=SUMA SYNC DATE=05/23/2008

PAGE TITLE
Ethernet PHY (RTL8211CL)

Apple Inc.

DRAWING NUMBER 051-7898
SIZE D
REVISION C.0.0
BRANCH
PAGE 37 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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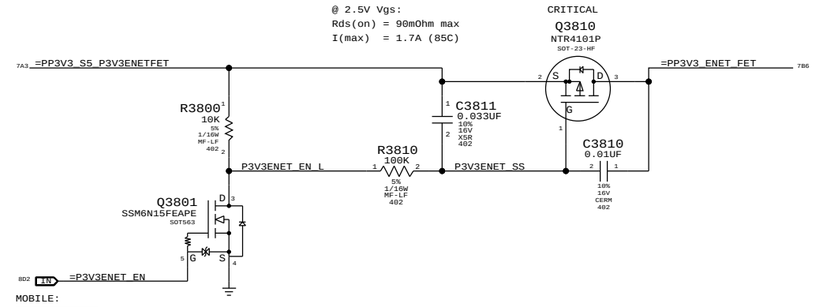
3.3V ENET FET

@ 2.5V Vgs:
Rds(on) = 90mOhm max
I(max) = 1.7A (85C)



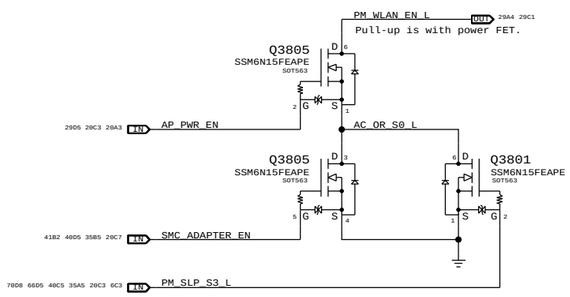
MOBILE:

Recommend aliasing PM_SLP_RMGT_L and =P3V3ENET_EN. Nets separated on ARB for alternate power options.

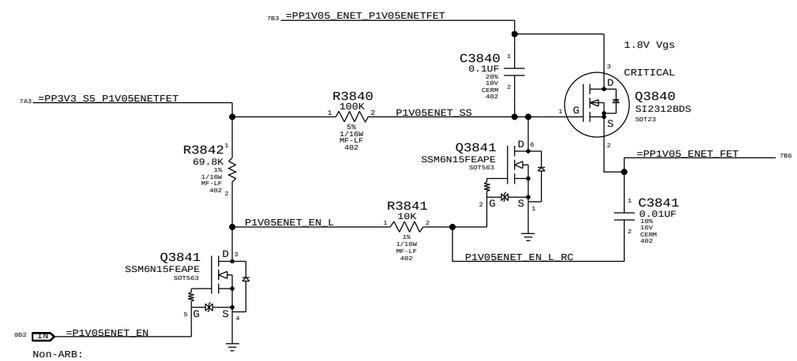
WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.



1.05V ENET FET

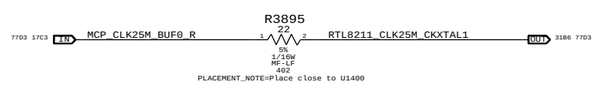


Non-ARB:

Recommend aliasing PM_SLP_RMGT_L and =P1V05ENET_EN. Nets separated on ARB for alternate power options.

RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.
Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.



SYNC MASTER=SUMA SYNC DATE=07/01/2008

PAGE TITLE
Ethernet & AirPort Support

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

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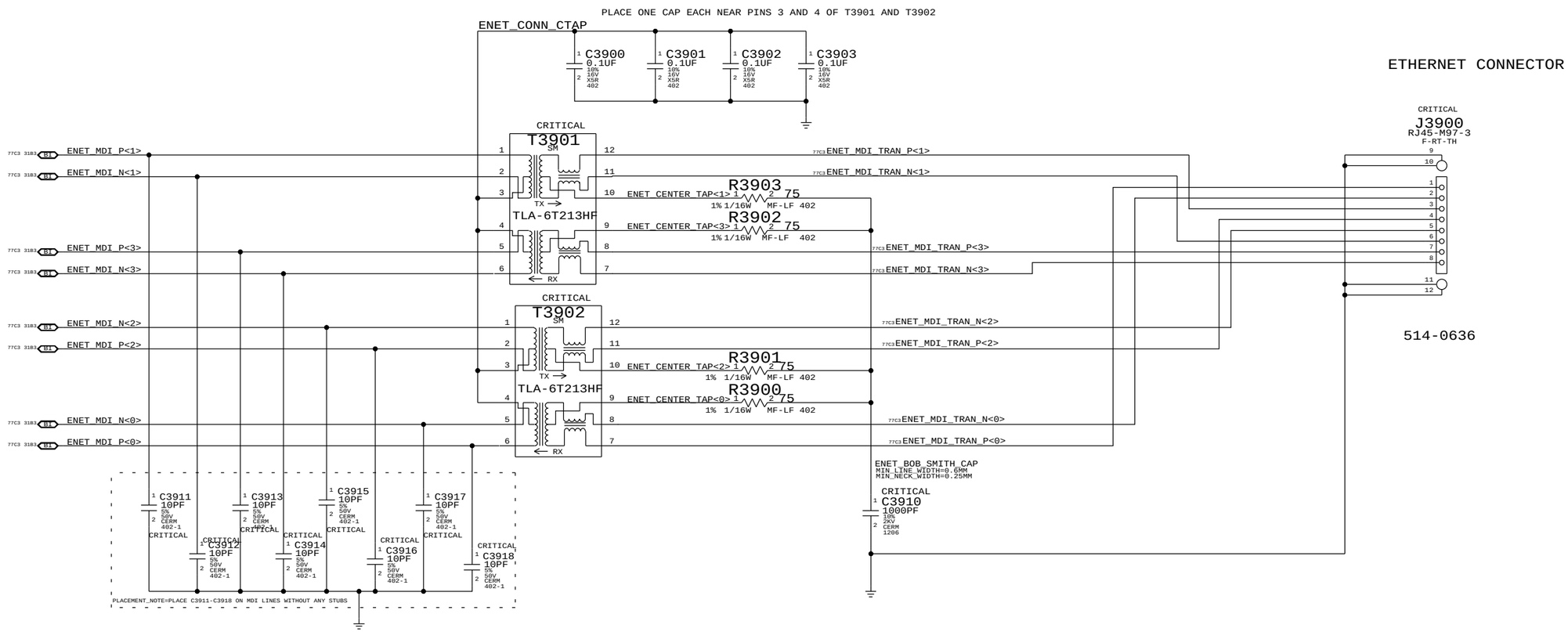
- COPY THIS PAGE FROM K36 CSA.39



SYNC MASTER=SUMA SYNC DATE=04/04/2008

PAGE TITLE: ETHERNET CONNECTOR

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

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PAGE: 39 OF 109

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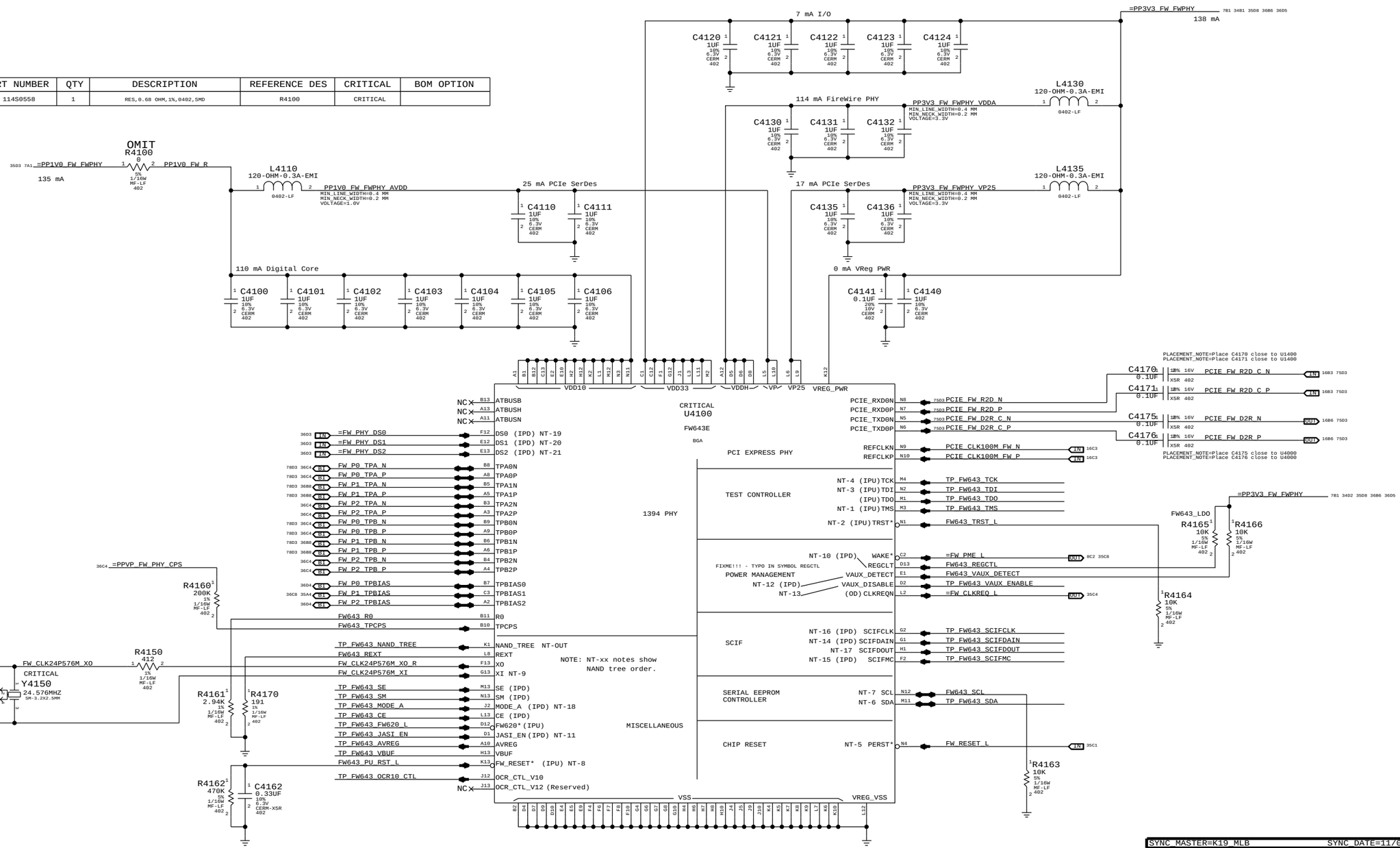
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0558	1	RES,0.68 OHM,1%,0402,SMD	R4100	CRITICAL	



SYNC_MASTER=K19_MLB SYNC_DATE=11/02/2006

PAGE TITLE
FireWire LLC/PHY (FW643)

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

REVISION C.0.0

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PAGE 41 OF 109

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Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:

3.3V FW FET

@ 2.5V Vgs:
Rds(on) = 90mOhm max
I(max) = 1.7A (85C)

=PP3V3_S0_P3V3FWFET
R4290 10K 5% 1/16W MF-LF 402
P3V3FW_EN_L
R4291 100K 5% 1/16W MF-LF 402
C4290 0.033UF 10% 16V X5R 402
CRITICAL Q4291 NTR4101P SOT-23-HF
C4291 0.01UF 10% 16V CERM 402
=PP3V3_FW_FET
P3V3FW_SS
Q4290 SSM6N15FEAPE SOT563
FW_PWR_EN

=PP3V3_S0_FWPWRCTL
R4281 100K 5% 1/16W MF-LF 402
R4280 10K 1% 1/16W MF-LF 402
=PP1V0_FW_FWPHY
P1V0_FW_RC
C4281 1UF 10% 6.3V CERM 402
CRITICAL Q4299 DMB53D0UV SOT-563

=PP3V3_FW_FWPHY
FWPHY_WAKE_YES
R4276 100K 5% 1/16W MF-LF 402
R4277 10K 5% 1/16W MF-LF 402
FW_PLUG_DET_L
FW_WAKE
CRITICAL Q4276 DMB53D0UV SOT-563
=FW_PME_L
CRITICAL Q4276 DMB53D0UV SOT-563

1.05V FW FET

=PP1V05_FW_P1V05FWFET
C4296 0.1UF 20% 16V CERM 402
=PP3V3_S0_P1V05FWFET
R4297 220K 5% 1/16W MF-LF 402
P1V05FW_SS
CRITICAL Q4295 SI2312BDS SOT23
Q4293 SSM6N15FEAPE SOT563
=PP3V3_S5_P1V05FWFET
R4295 10K 5% 1/16W MF-LF 402
=PP1V0_FW_FET
C4295 0.068UF 10% 16V CERM 402
P1V05_FW_EN_L
R4296 100K 5% 1/16W MF-LF 402
P1V05_FW_EN_L_RC
Q4293 SSM6N15FEAPE SOT563
FW_PWR_EN

PCIE_FW_PRSNT
MAKE_BASE=TRUE
Q4264 SSM6N15FEAPE SOT563
FW_CLKREQ_L
Q4264 SSM6N15FEAPE SOT563
FW_PWR_EN
=FW_CLKREQ_L
FW_CLKREQ_PHY_L
MAKE_BASE=TRUE

P1V0_RESET_GATE
R4283 10K 5% 1/16W MF-LF 402
=FW_RESET_L
CRITICAL Q4299 DMB53D0UV SOT-563
FW_RESET_L
PP1V05_FW PGOOD/FW_RESET_L

FireWire Port Power Switch

=PPBUS_S5_FWPWRSW
CRITICAL Q4260 FDC638P_G SM
PPBUS_FW_FWPWRSW_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
CRITICAL F4260 1.1A-24V MINISMDC110H24
PPBUS_FW_FWPWRSW_D
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
CRITICAL D4260 SM CRS08-1.5A-30V
=PPBUS_S5_FW_FET

CRITICAL Q4262 DMB54D0UV SOT-563
R4260 300K 5% 1/16W MF-LF 402
C4260 0.1UF 10% 25V X5R 402
FWPWR_EN_L_DIV
R4261 470K 5% 1/16W MF-LF 402
FWPWR_EN_L

Late-VG Event Detection

R4265 10K 1% 1/16W MF-LF 402
NOSTUFF
R4263 100 1% 1/16W MF-LF 402
LATEVG_FAULT_EVENT_PNP
LATEVG_FAULT_EVENT
LATEVG_RETRY_RC
C4263 1UF 10% 16V X5R 402
NOSTUFF

SMC_ADAPTER_EN
Q4261 2N7002DW-X-G SOT-363
Q4261 2N7002DW-X-G SOT-363
PM_SLP_S3_L

Enables port power when machine is running or on AC.

=PP1V05_FWPWRCTL
R4275 1K 5% 1/16W MF-LF 402
FW_PWR_EN_L
R4270 330K 5% 1/16W MF-LF 402
R4271 56K 5% 1/16W MF-LF 402
FW_DET_MIRROR
FW_PLUG_DET
CRITICAL Q4270 BC847CDXV6TXG SOT563
CRITICAL Q4270 BC847CDXV6TXG SOT563
FW_P1_TPBIAS_R
FW_DET_EMIT
R4272 1K 5% 1/16W MF-LF 402
R4273 12K 5% 1/16W MF-LF 402

=PP3V3_S0_FWPWRCTL
R4274 100K 5% 1/16W MF-LF 402
FW_PLUG_DET_L
CRITICAL Q4275 DMB53D0UV SOT-563
C4270 0.1UF 10% 16V X5R 402

=PP3V3_FW_LATEVG_ACTIVE
PP2V4_FW_LATEVG
R4211 10K 5% 1/16W MF-LF 402
R4212 10K 5% 1/16W MF-LF 402
C4210 0.1UF 20% 16V CERM 402
U4210 LMC7211 SM-HF
FWLATEGV_3V_REF
LATEVG_EVENT
P2V4_FWLATEVG_RC
C4211 100pF 5% 50V CERM 402
R4213 80.6K 1% 1/16W MF-LF 402
R4210 200K 1% 1/16W MF-LF 402

FWLATEVG Hysteresis:
3.08V when port power is on
2.91V when late Vq event and port power is off

CRITICAL Q4275 DMB53D0UV SOT-563
FW_PWR_EN
FW_P1_TPBIAS

SYNC MASTER=YUN K19 MLB	SYNC DATE=12/22/2008
PAGE TITLE: FireWire Port Power	
Apple Inc.	DRAWING NUMBER: 051-7898 SIZE: D
	REVISION: C.0.0
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	PAGE: 42 OF 109
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Page Notes

Power aliases required by this page:

- =PPVP_FW_PORT1
- =PP3V3_FW_LATEVG

- =GND_CHASSIS_FW_PORT1
- =GND_CHASSIS_FW_EMI_R

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

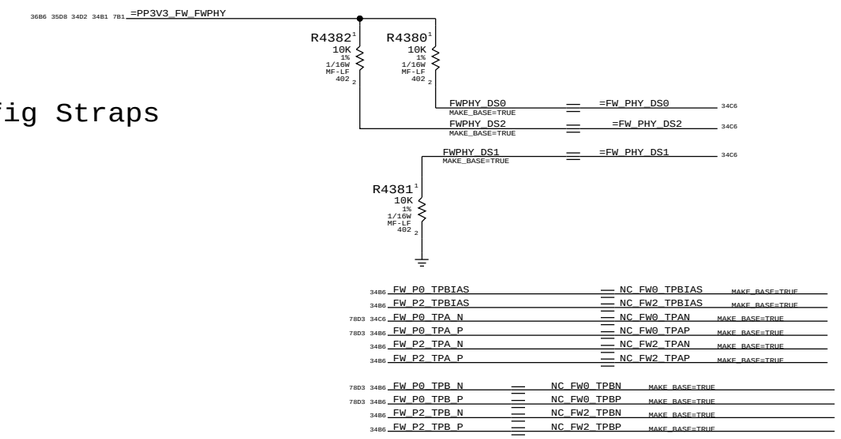
1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

FireWire PHY Config Straps

Configures PHY for:

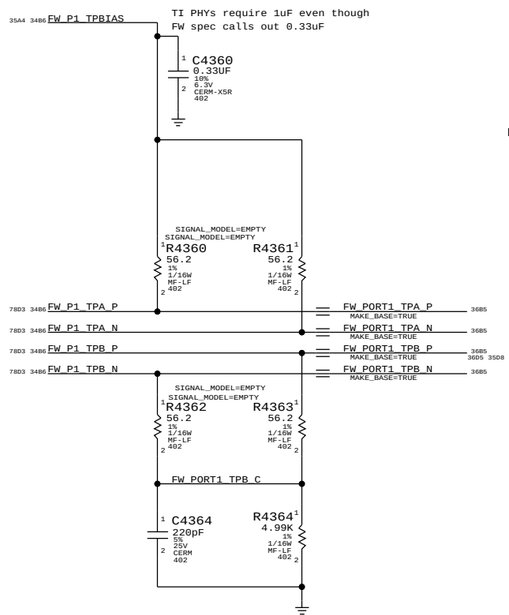
- 1-port Portable Power Class (0)

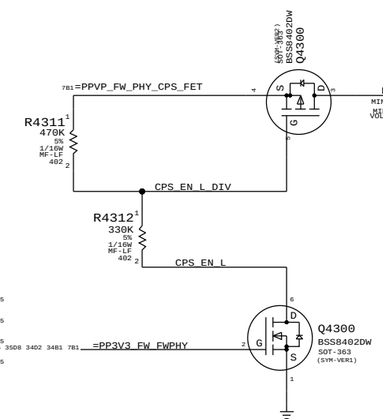
- Port "1" Bilingual (1394B)



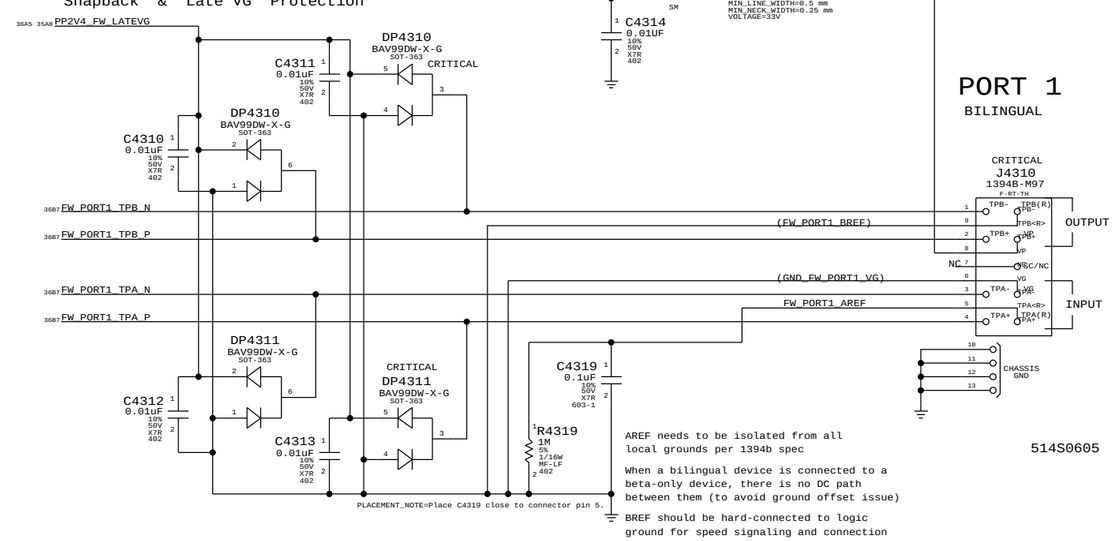
Termination

Place close to FireWire PHY

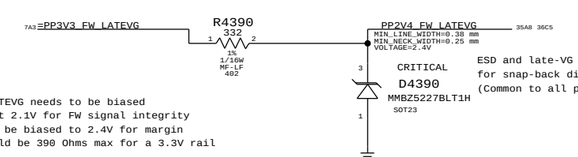




"Snapback" & "Late VG" Protection



Late-VG Protection Power



ESD and late-VG rail for snap-back diodes (Common to all ports)

PP2V4_FWLATEVG needs to be biased to at least 2.1V for FW signal integrity and should be biased to 2.4V for margin
R4390 should be 390 Ohms max for a 3.3V rail

SYNC_MASTER=K19_MLB SYNC_DATE=11/02/2008

PAGE TITLE: FireWire Ports

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

BRANCH:

PAGE: 43 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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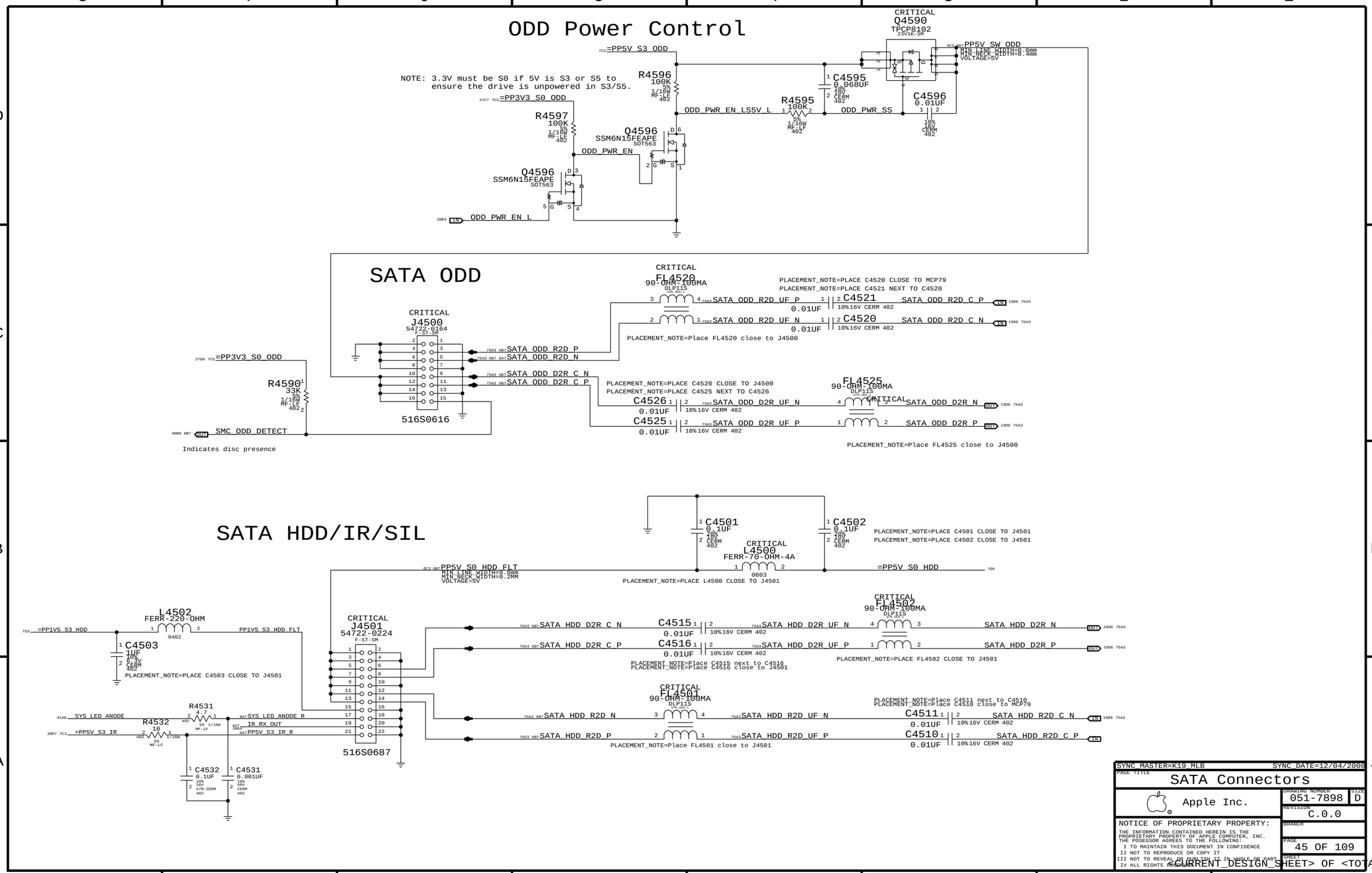

SYNC MASTER=K19 MLB SYNC DATE=12/04/2008

PAGE TITLE: SATA Connectors

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

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PAGE: 45 OF 109

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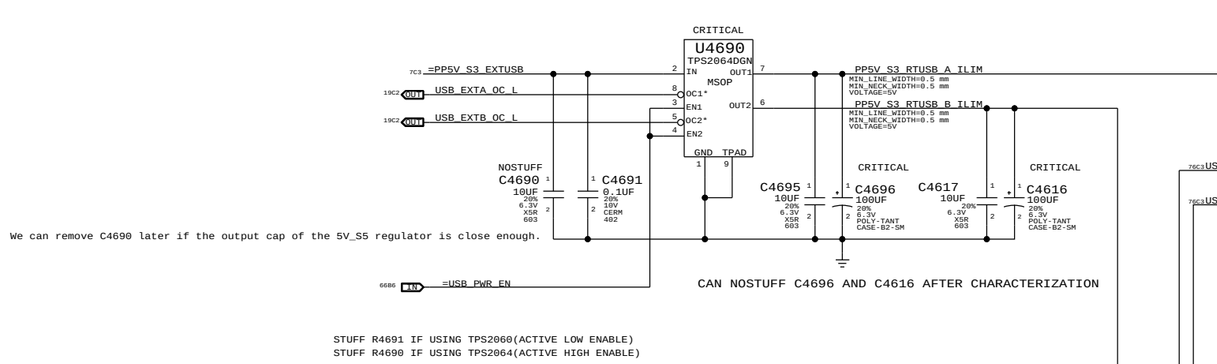
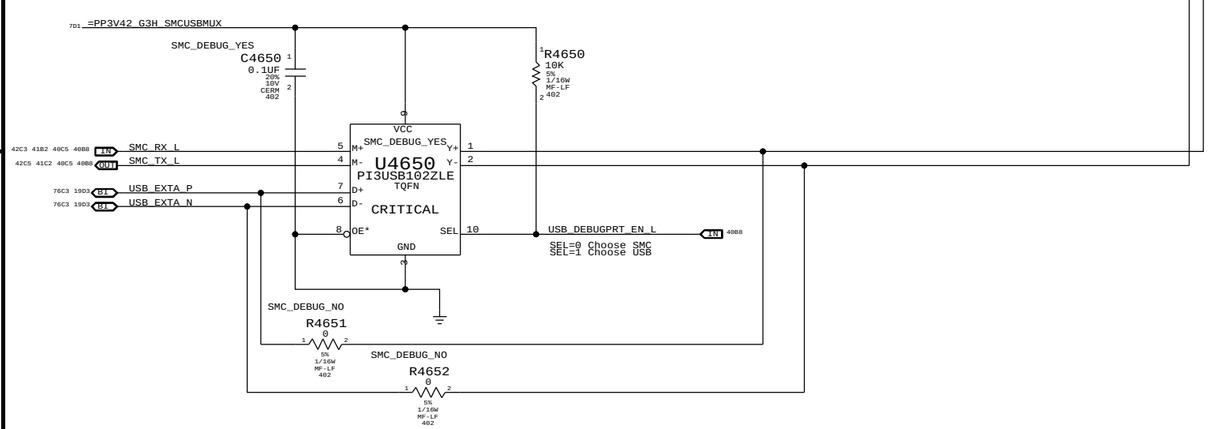
Port Power Switch



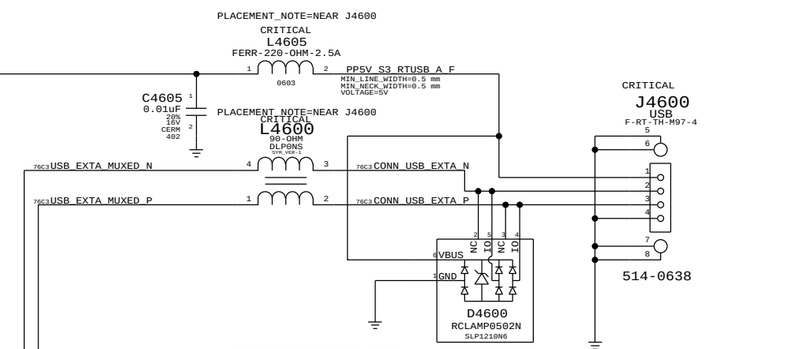
We can remove C4690 later if the output cap of the 5V_S5 regulator is close enough.

STUFF R4691 IF USING TPS2060(ACTIVE LOW ENABLE)
STUFF R4690 IF USING TPS2064(ACTIVE HIGH ENABLE)

USB/SMC Debug Mux

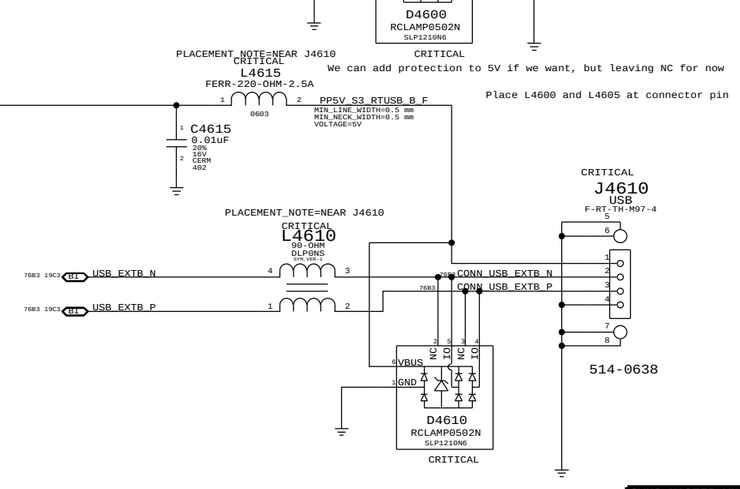


USB PORT A (FRONT PORT)



We can add protection to 5V if we want, but leaving NC for now

Place L4600 and L4605 at connector pin



USB PORT B (BACK PORT)

SYNC_MASTER=YUAN.MA SYNC_DATE=01/18/2008

PAGE TITLE: External USB Connectors

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

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PAGE: 46 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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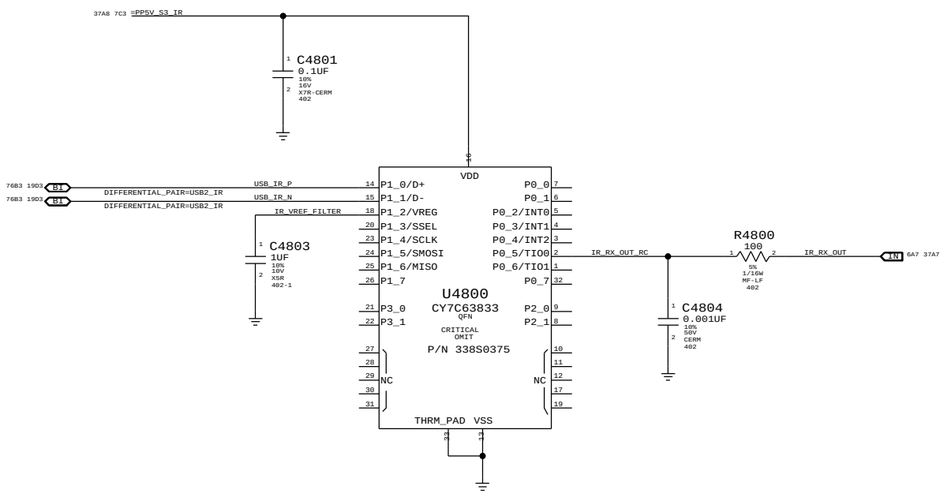

CYPRESS 'ENCORE II' USB CONTROLLER

SYNC_MASTER=YUAN.MA SYNC_DATE=05/28/2008

PAGE TITLE
Front Flex Support

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

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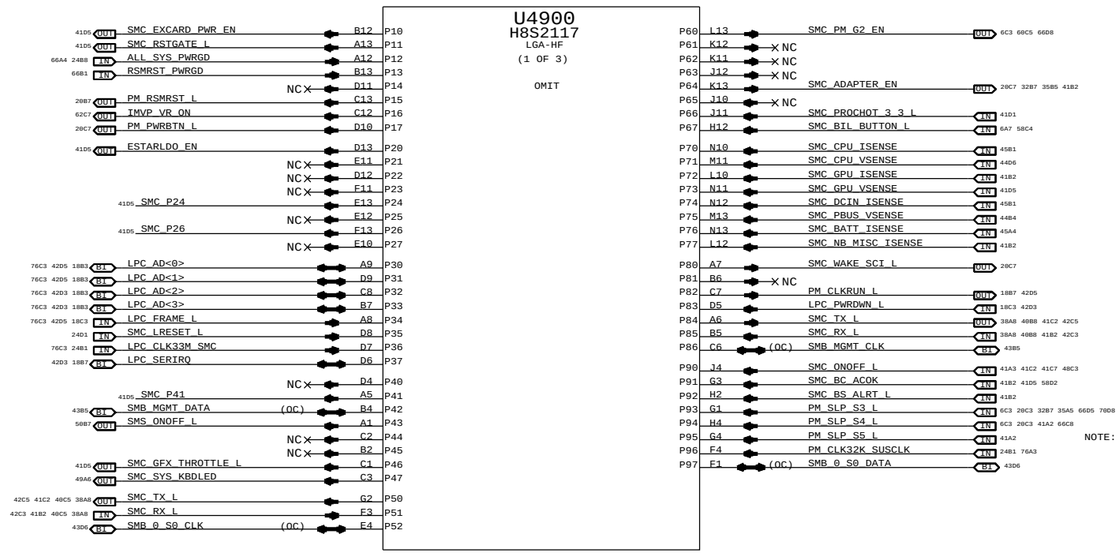
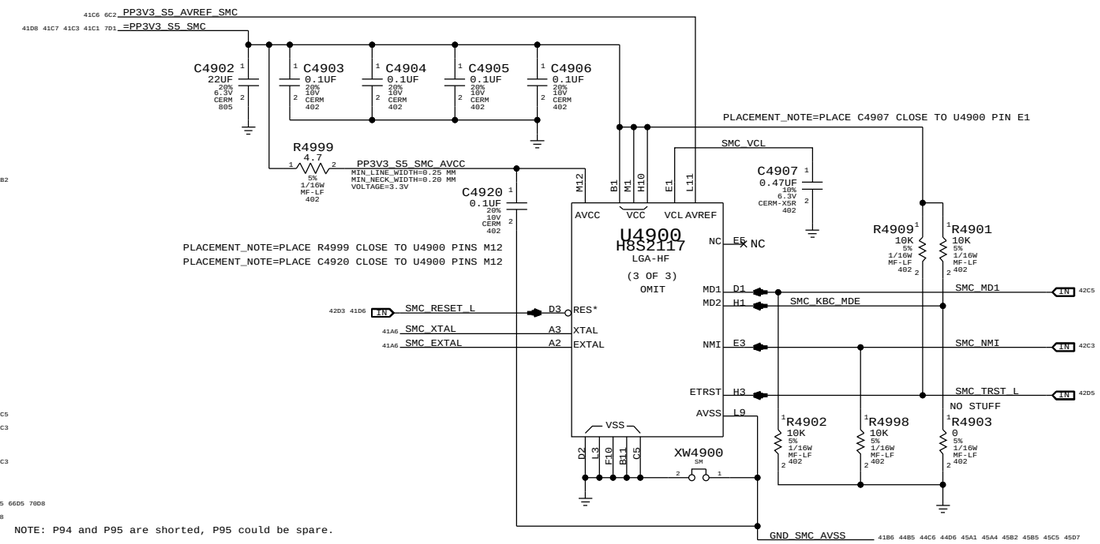
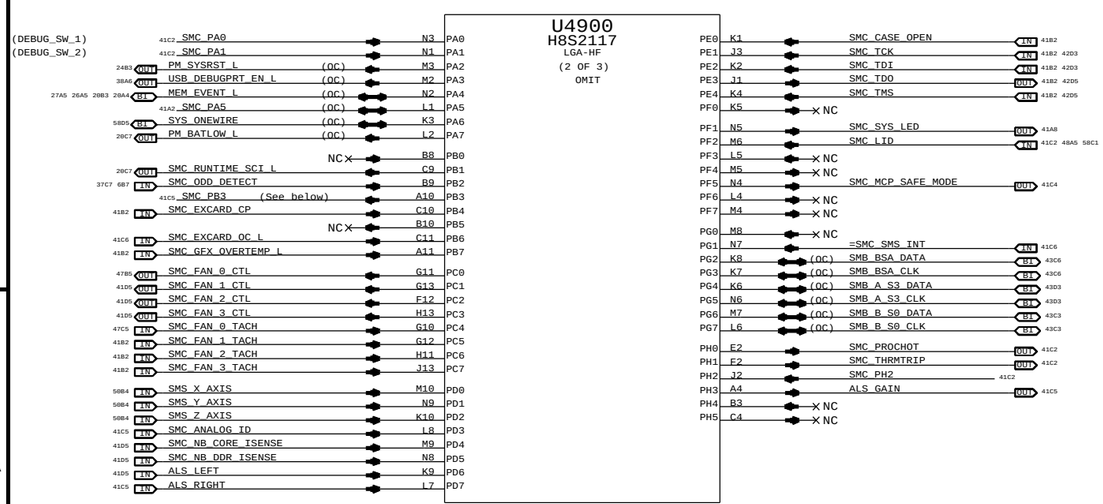
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



NOTE: P94 and P95 are shorted, P95 could be spare.





NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SMC_PB3:
SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)

SYNC_MASTER=T18_MLB SYNC_DATE=06/26/2008

PAGE TITLE: SMC

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

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PAGE: 49 OF 109

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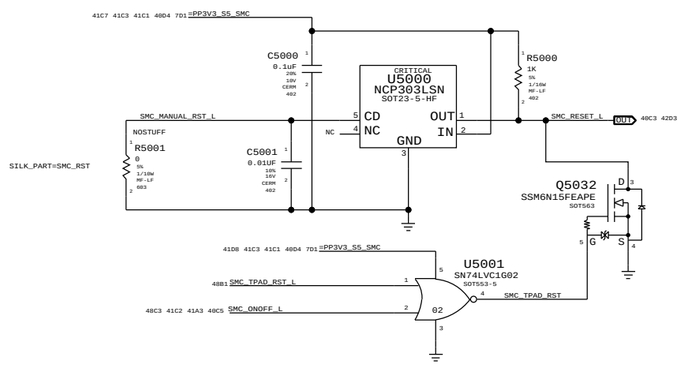
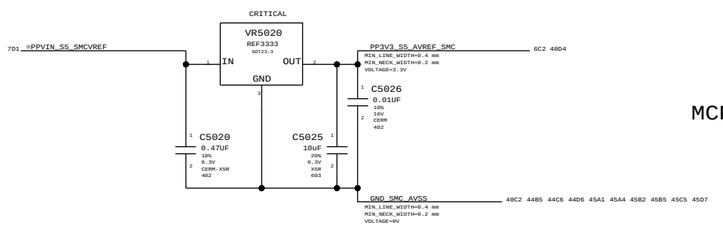
SMC Reset "Button" / Brownout Detect

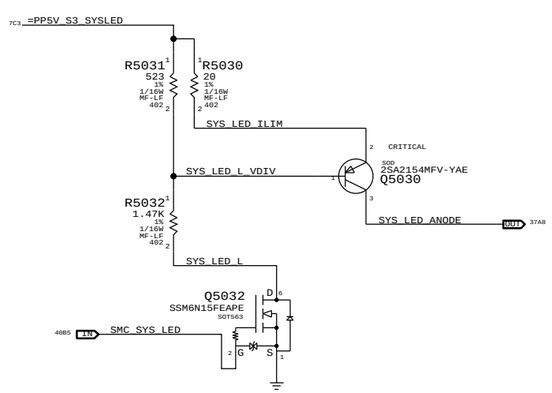


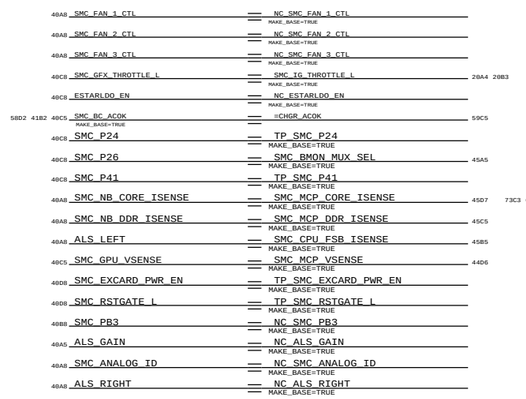
SMC AVREF Supply



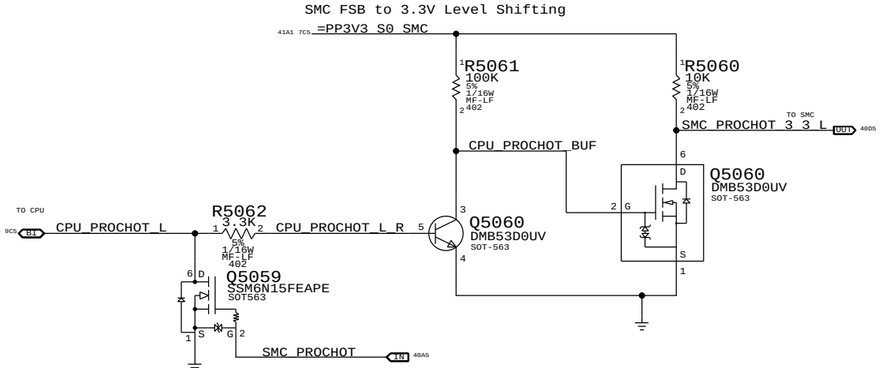
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1912		ALL	ISL60002-33, INTERSIL

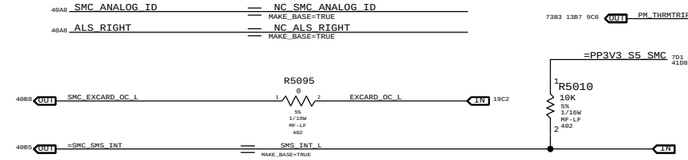
System (Sleep) LED Circuit





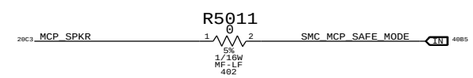
SMC FSB to 3.3V Level Shifting

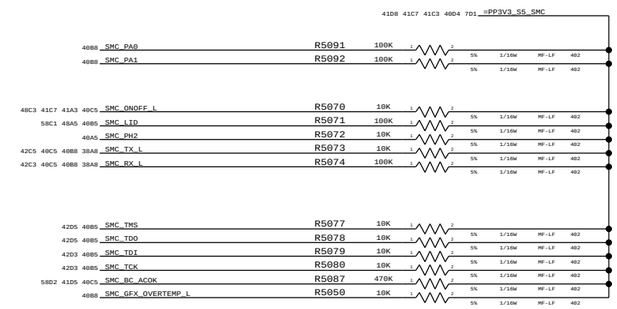


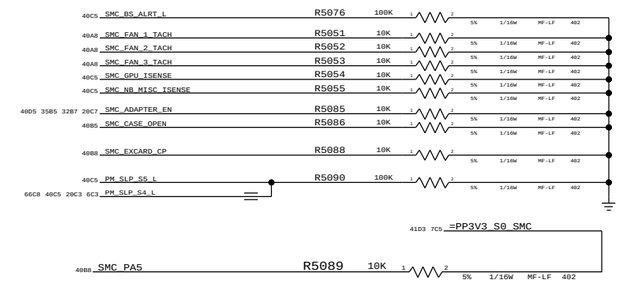


MCP_SAFE_MODE SIGNAL TO SUPPORT ROM FAILURE OVERRIDE

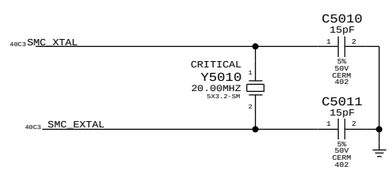
RADAR 5925345



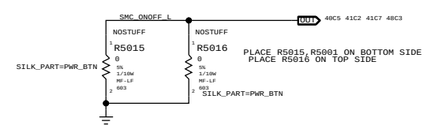




SMC Crystal Circuit



Debug Power "Button"



SYNC_MASTER=YUAN.MA SYNC_DATE=05/28/2008

PAGE TITLE

SMC Support

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

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PAGE 50 OF 109

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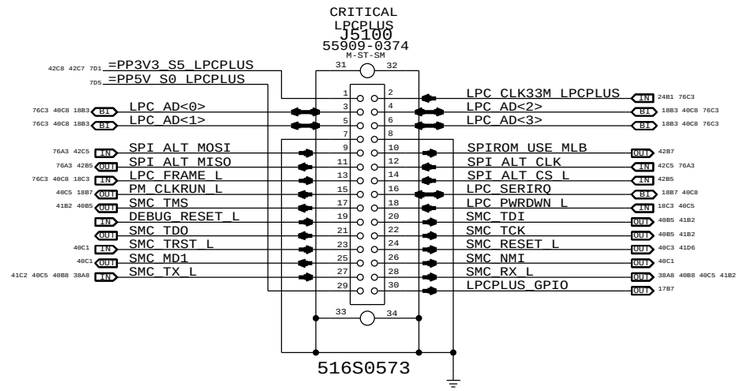
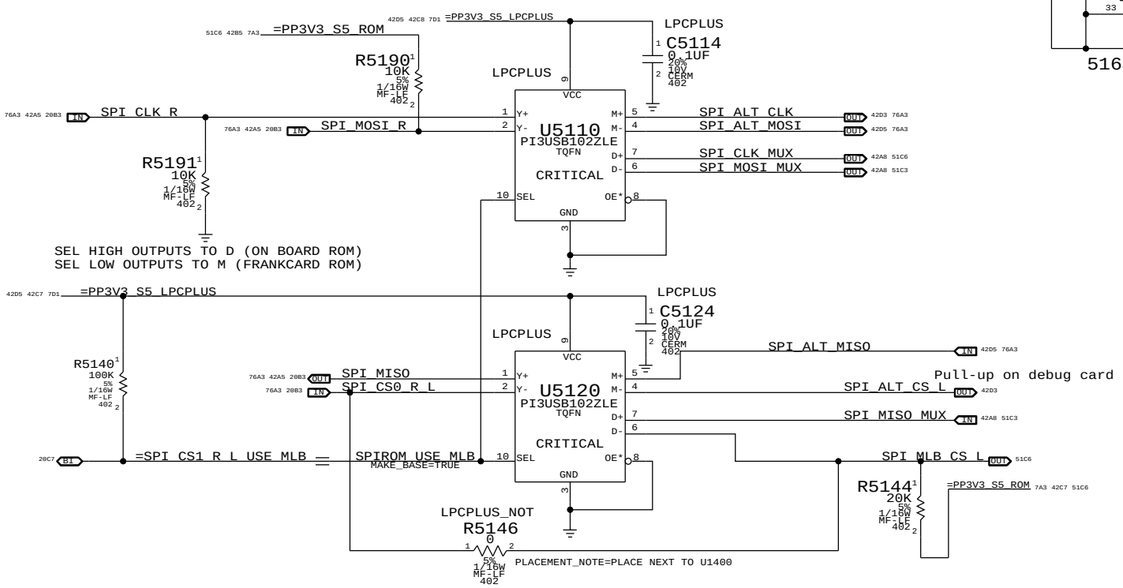
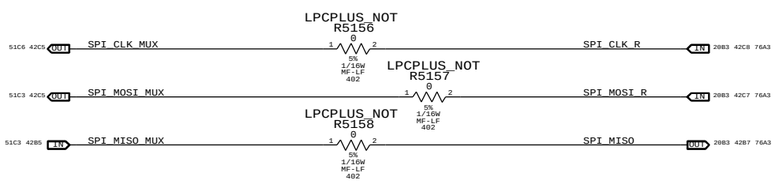
LPC+SPI Connector



Alternate SPI ROM Support



SPI MUX BYPASS



SYNC_MASTER=CHANGZHANG SYNC_DATE=05/09/2008

PAGE TITLE
LPC+SPI Debug Connector

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

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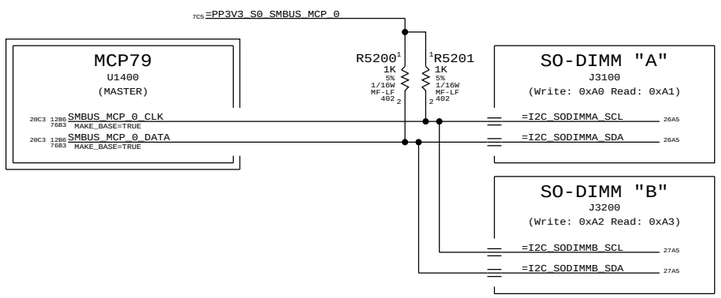
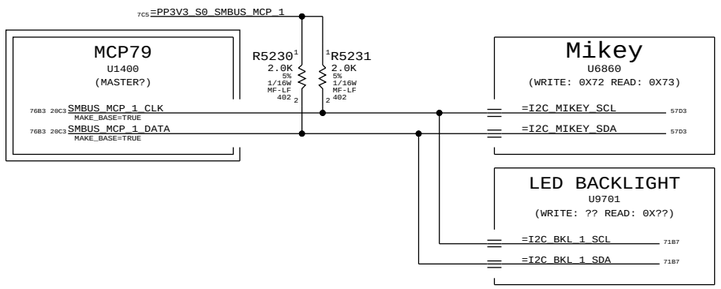
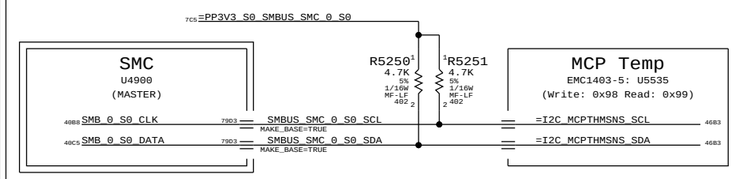
MCP79 SMBUS "0" CONNECTIONS



MCP79 SMBUS "1" CONNECTIONS

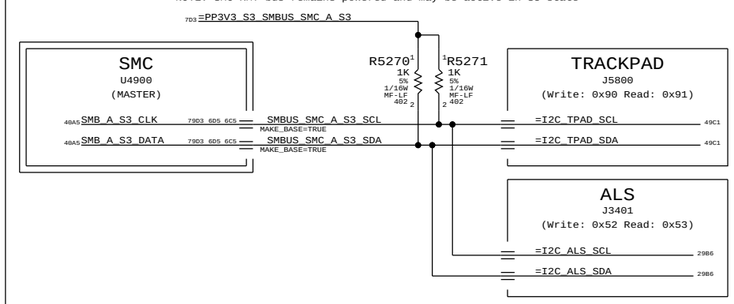


SMC "0" SMBus Connections

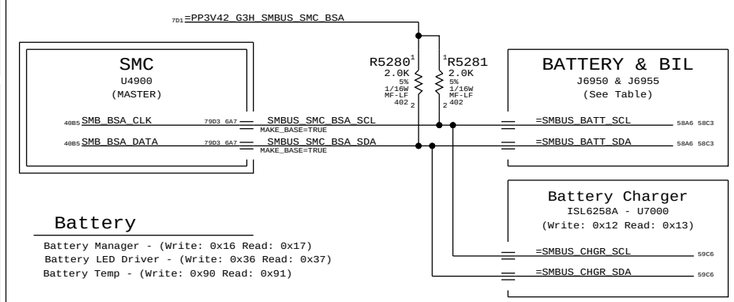


SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state



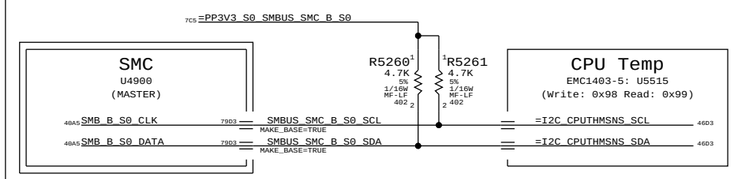
SMC "Battery A" SMBus Connections



Battery

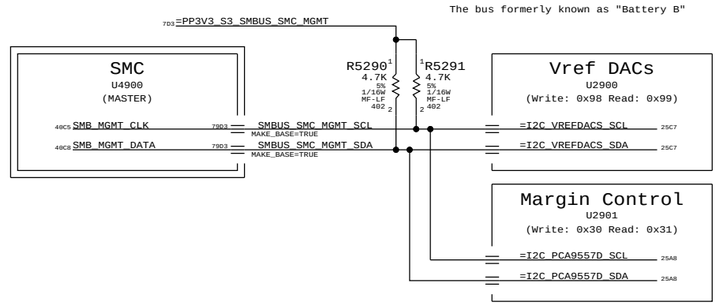
Battery Manager - (Write: 0x16 Read: 0x17)
Battery LED Driver - (Write: 0x36 Read: 0x37)
Battery Temp - (Write: 0x90 Read: 0x91)

SMC "B" SMBus Connections



SMC "Management" SMBus Connections

The bus formerly known as "Battery B"



SYNC MASTER=BEN SYNC DATE=04/21/2008

PAGE TITLE
K24 SMBUS CONNECTIONS

Apple Inc.

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PAGE 52 OF 109
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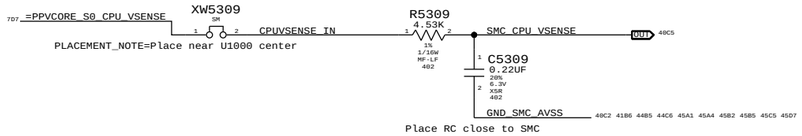
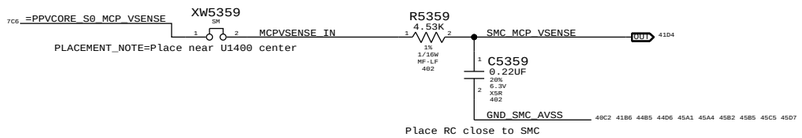
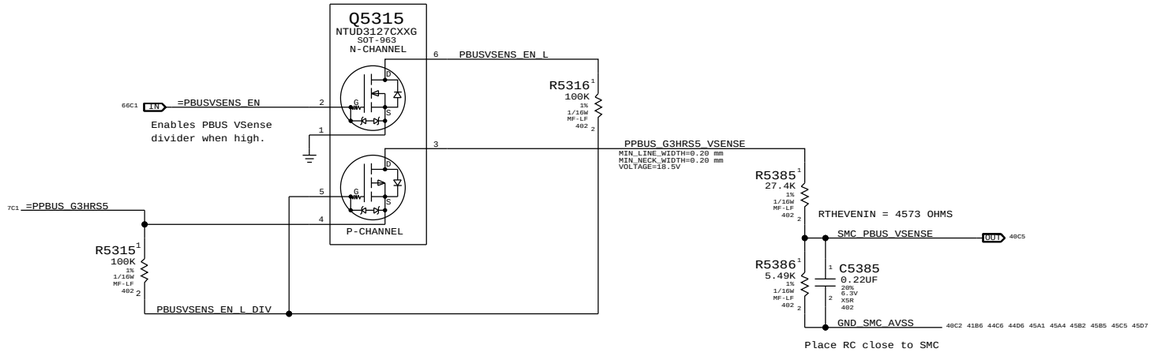
CPU Voltage Sense / Filter



MCP Voltage Sense / Filter



PBUS VOLTAGE SENSE ENABLE & FILTER



SYNC MASTER=YUNWU SYNC DATE=02/04/2008

PAGE TITLE
VOLTAGE SENSING

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

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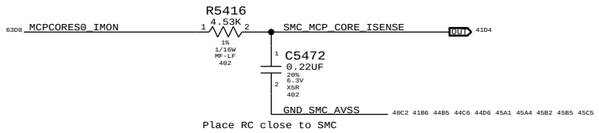
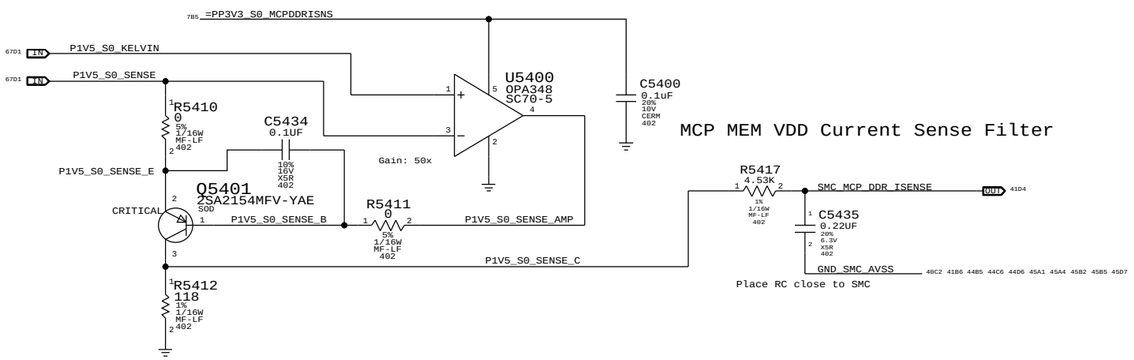
MCP VCore Current Sense Filter

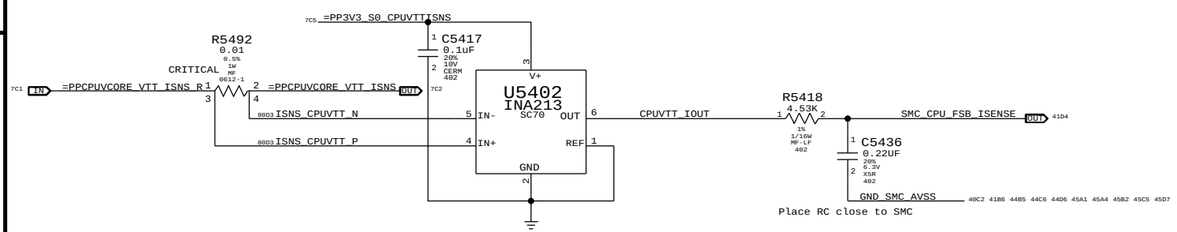


MCP MEM VDD Current Sense

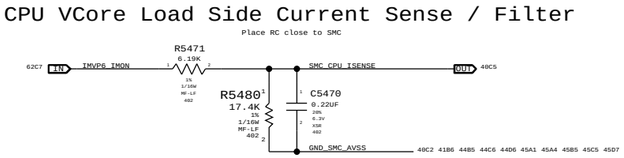


MCP MEM VDD Current Sense Filter

CPU 1.05V AND CPU VCORE HIGH SIDE CURRENT SENSE

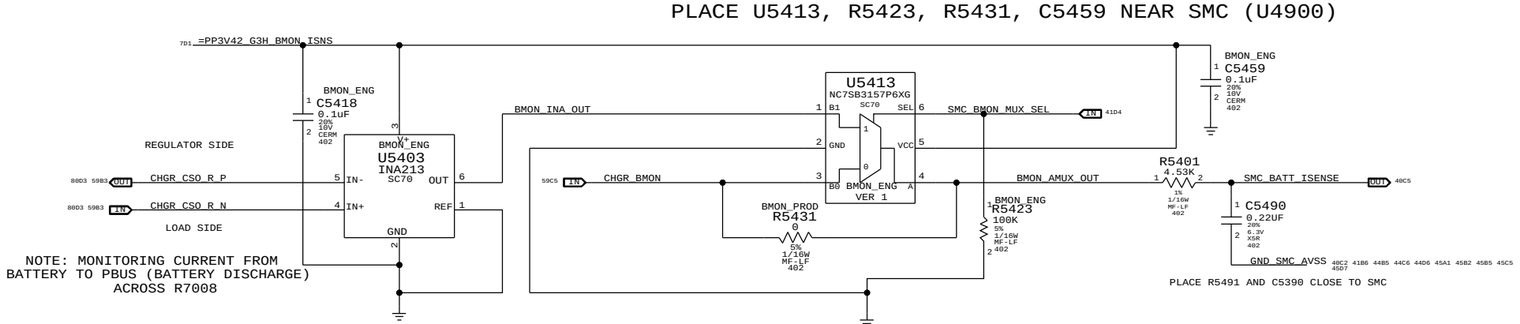


CPU VCore Load Side Current Sense / Filter



BMON CURRENT SENSE

PLACE U5413, R5423, R5431, C5459 NEAR SMC (U4900)



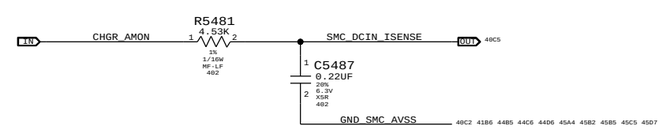
NOTE: MONITORING CURRENT FROM BATTERY TO PBUS (BATTERY DISCHARGE) ACROSS R7008

INA213 has gain of 50V/V

PLACE U5403 AND C5418 NEAR R7008

For engineering, stuff U5313 and unstuff R5330
For production, stuff R5330 and unstuff U5313

DC-IN (AMON) CURRENT SENSE



SYNC MASTER=YUNWU SYNC DATE=12/17/2008

PAGE TITLE
Current Sensing

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

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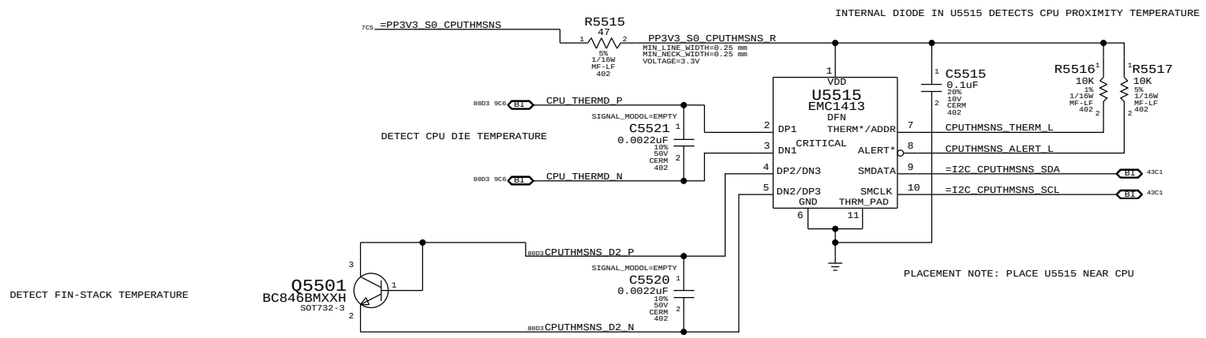
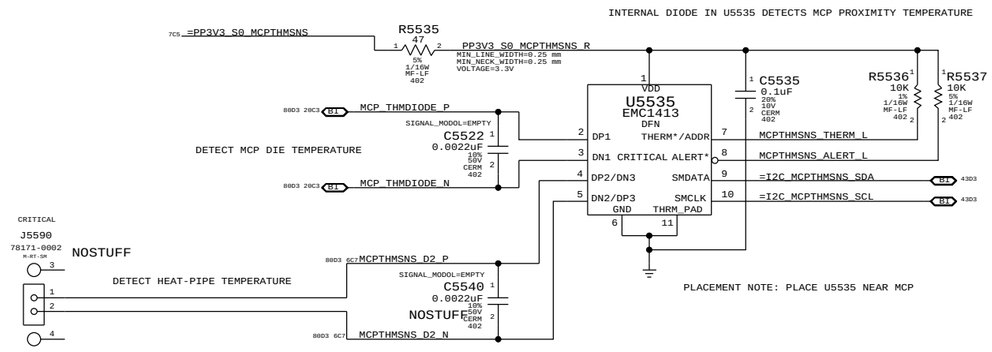
CPU T-Diode Thermal Sensor



MCP T-Diode Thermal Sensor



REPLACED 518S0521 WITH 518S0519

SYNC_MASTER=YUNWU	SYNC_DATE=03/20/2008
PAGE TITLE: Thermal Sensors	
Apple Inc.	DRAWING NUMBER: 051-7898 SIZE: D
	REVISION: C.0.0
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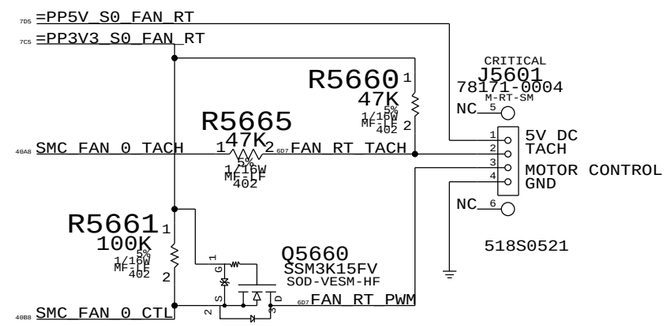
	PAGE: 55 OF 109
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



SYNC_MASTER=CHANGZHANG SYNC_DATE=01/18/2008

PAGE TITLE

Fan

Apple Inc.

DRAWING NUMBER 051-7898

SIZE D

REVISION C.0.0

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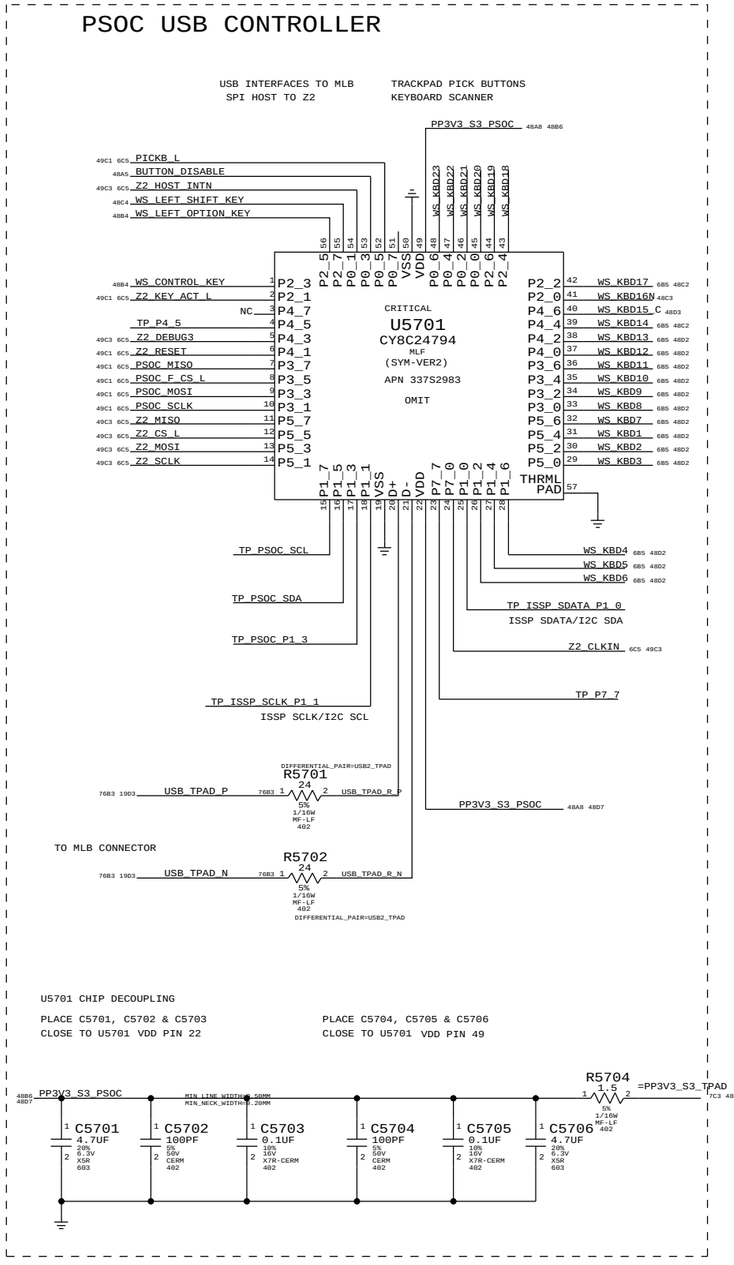
PSOC USB CONTROLLER



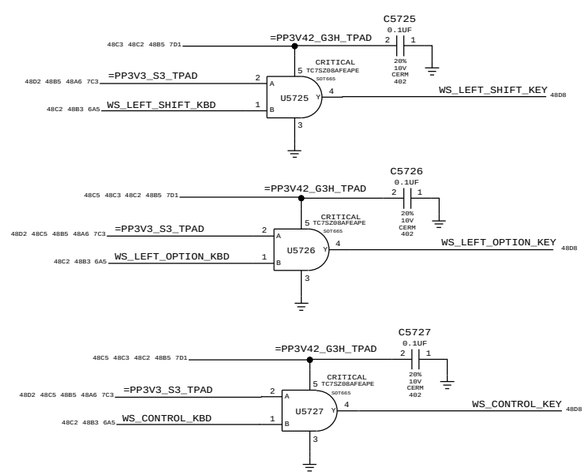
U5701 CHIP DECOUPLING

PLACE C5701, C5702 & C5703
CLOSE TO U5701 VDD PIN 22

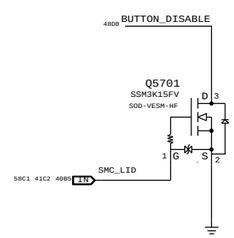
PLACE C5704, C5705 & C5706
CLOSE TO U5701 VDD PIN 49

IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA MAX	10 OHM	0.6 V	36E-3 W
	VOUT	60MA MAX	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

ISOLATION CIRCUIT



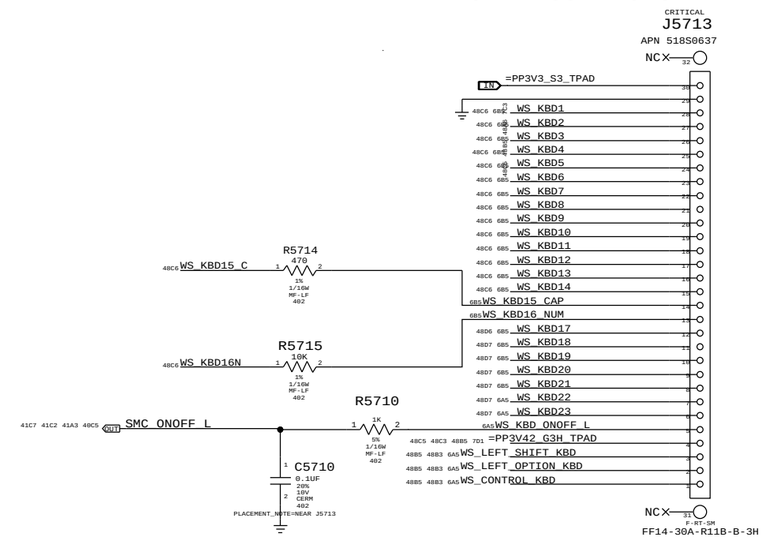
TPAD BUTTONS DISABLE



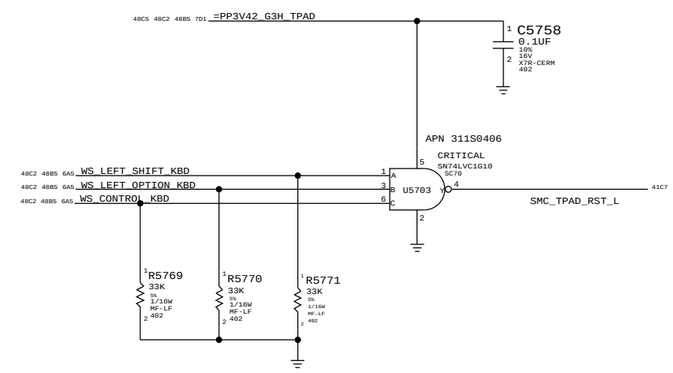
PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

KEYBOARD CONNECTOR



SMC_MANUAL_RESET LOGIC



Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0406	311S0447		ALL	NXP PART AS ALTERNATE

SYNC_MASTER=YUAN.MA SYNC_DATE=04/22/2008

PAGE TITLE
WELLSPRING 1

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

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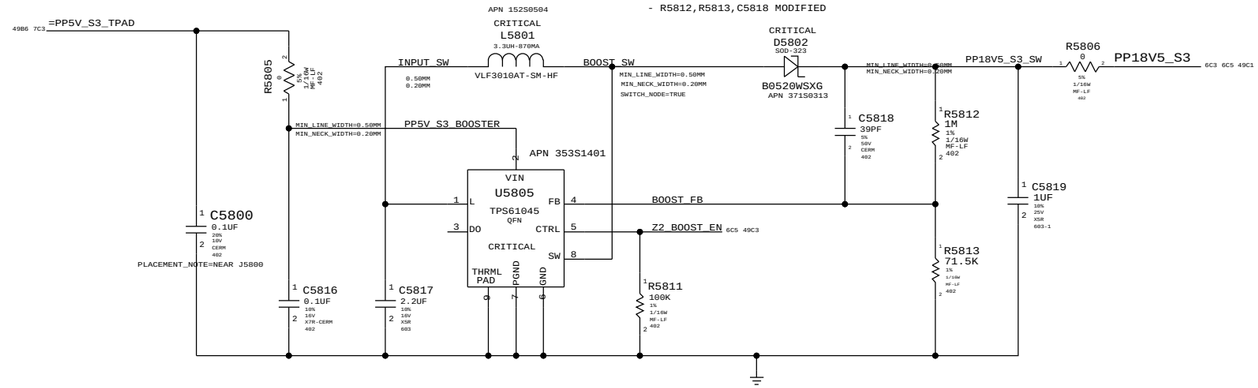
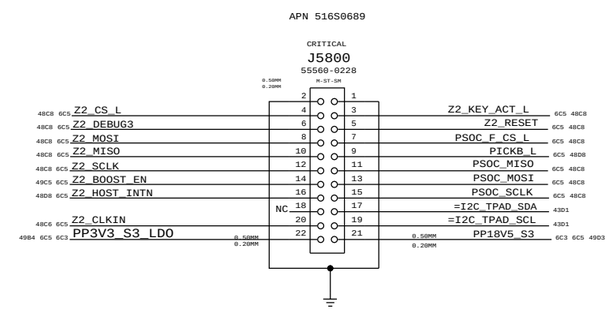
BOOSTER +18.5VDC FOR SENSORS

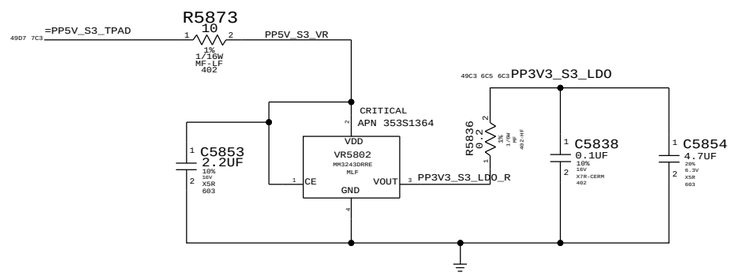
BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED



IPD FLEX CONNECTOR



3V3 LDO FOR IPD



KEYBOARD BACKLIGHT DRIVNG AND DETECTION

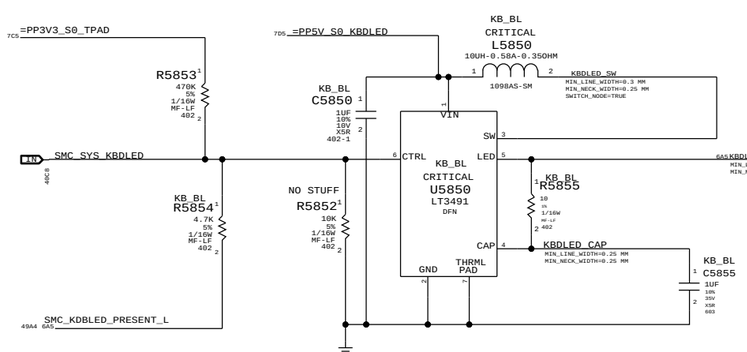
To detect Keyboard backlight, SMC will tristate SMC_SYS_KBDLED:

LOW = keyboard backlight present

HIGH= keyboard backlight not present

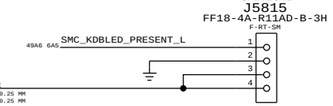
BOM OPTION: KBDLED_YES
TURNED ON FOR BEST MLB CONFIG

R5853 ALWAYS PRESENT



APN 518S0691

J5815 pin 1 is grounded on keyboard backlight flex



KBD BACKLIGHT CONNECTOR

SYNC MASTER=YUAN.MA	SYNC DATE=05/09/2008
PAGE TITLE: WELLSPRING 2	
Apple Inc.	DRAWING NUMBER: 051-7898 SIZE: D
	REVISION: C.0.0
	BRANCH
	PAGE: 58 OF 109
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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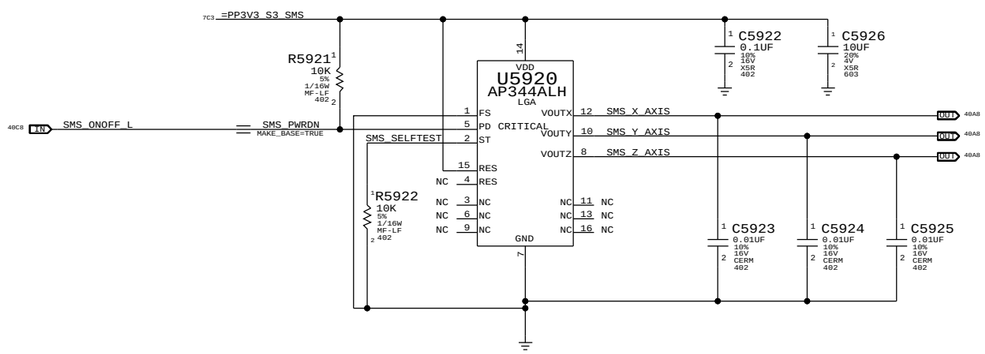
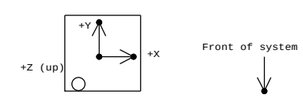
Analog SMS

R5921 PULLS UP SMS_PWRDN TO TURN OFF SMS WHEN PIN IS NOT BEING DRIVEN BY SMC



Desired orientation when placed on board top-side:



Circle indicates pin 1 location when placed in correct orientation

SYNC_MASTER=YUNWU SYNC_DATE=06/26/2008

PAGE TITLE
SMS

Apple Inc.

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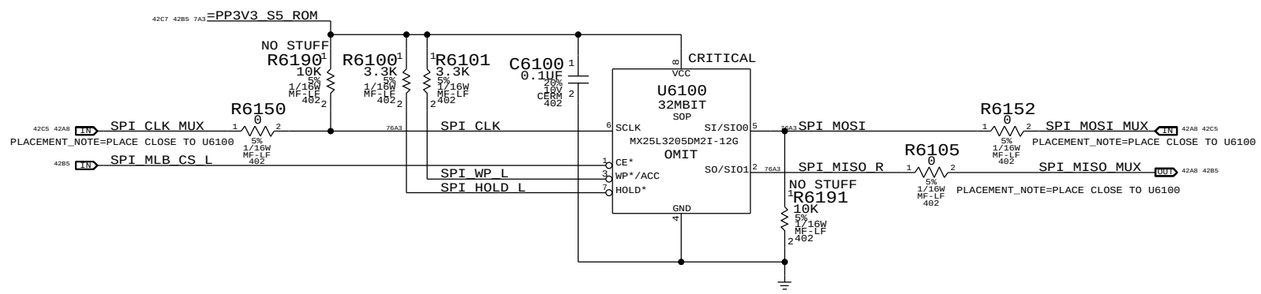

MCP79 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

25MHz is selected with R5190 and R5191
Any of the 4 frequencies can be selected
with R6190, R6191, R5190 and R5191

SYNC_MASTER=CHANGZHANG SYNC_DATE=05/02/2008

PAGE TITLE
SPI ROM

Apple Inc.

DRAWING NUMBER 051-7898
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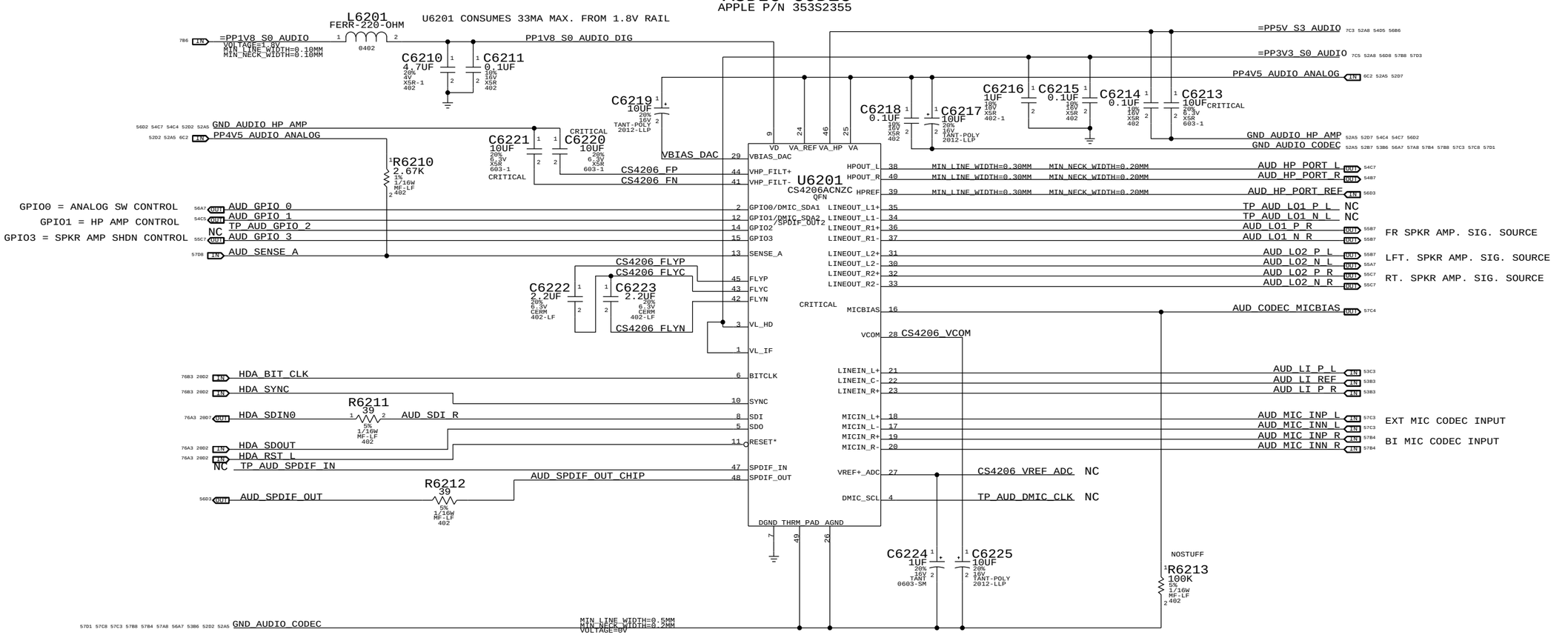
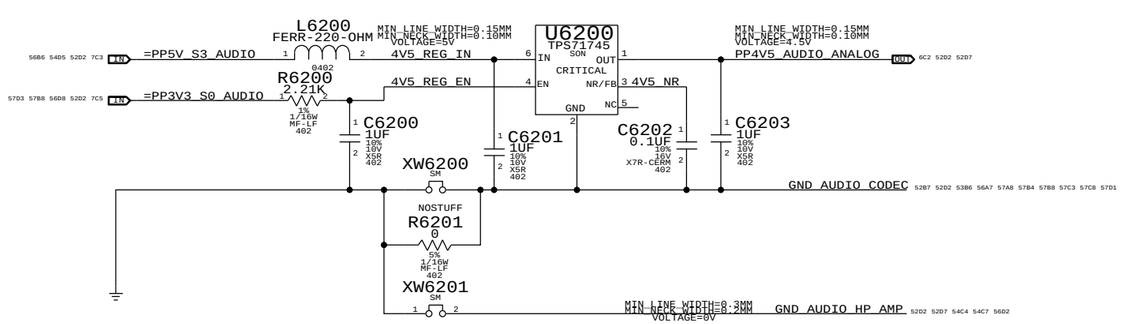
AUDIO CODEC
APPLE P/N 353S2355



4.5V POWER SUPPLY FOR CODEC
APPLE P/N 353S2456



NOTES ON CODEC I/O

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

SYNC MASTER=AUDIO SYNC DATE=03/04/2009

PAGE TITLE
AUDIO: CODEC/REGULATOR

Apple Inc.

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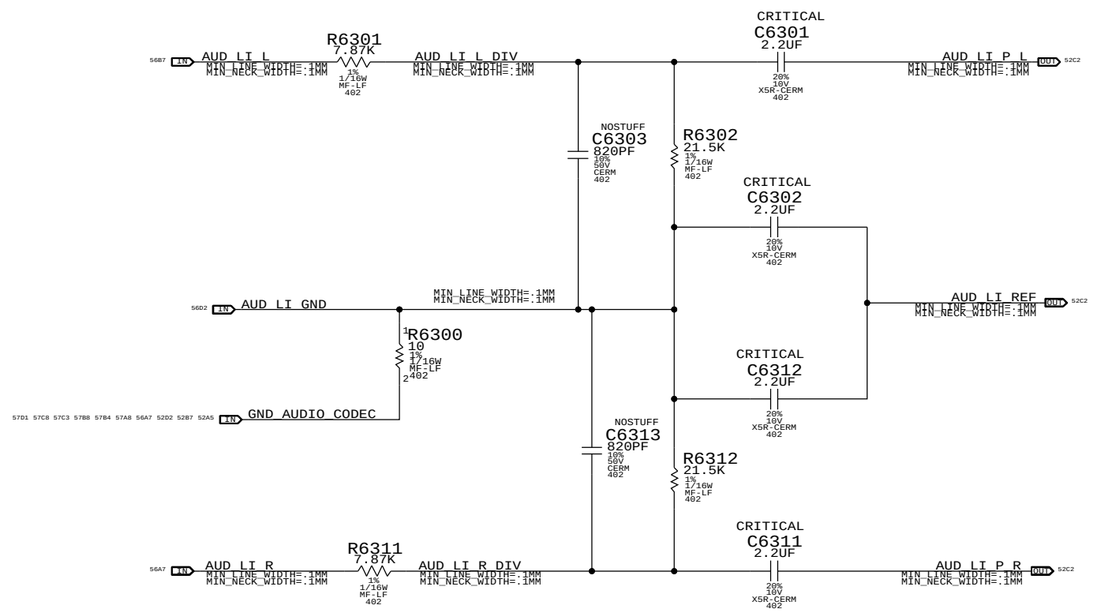
LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS
NET RIN = 10.36K OHMS (INCLUDING PULL-DOWNS AT ANALOG SWITCH COM PINS)
FC_HP = 3.6 HZ
FC_LP = 43KHZ
VIN = 2VRMS, CODEC VIN = 1.14 VRMS



SYNC_MASTER=AUDIO SYNC_DATE=01/31/2009

PAGE TITLE
AUDIO: LINE INPUT FILTER

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D
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PAGE 63 OF 109
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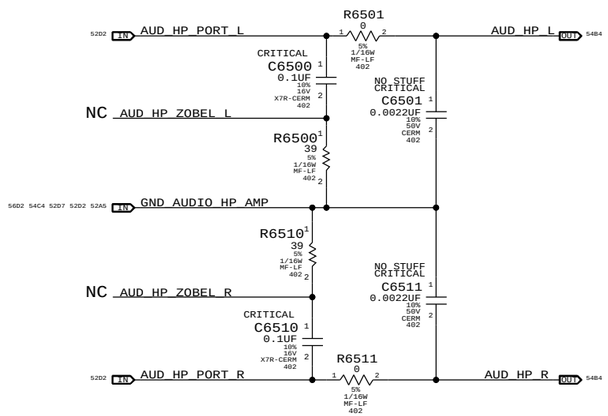
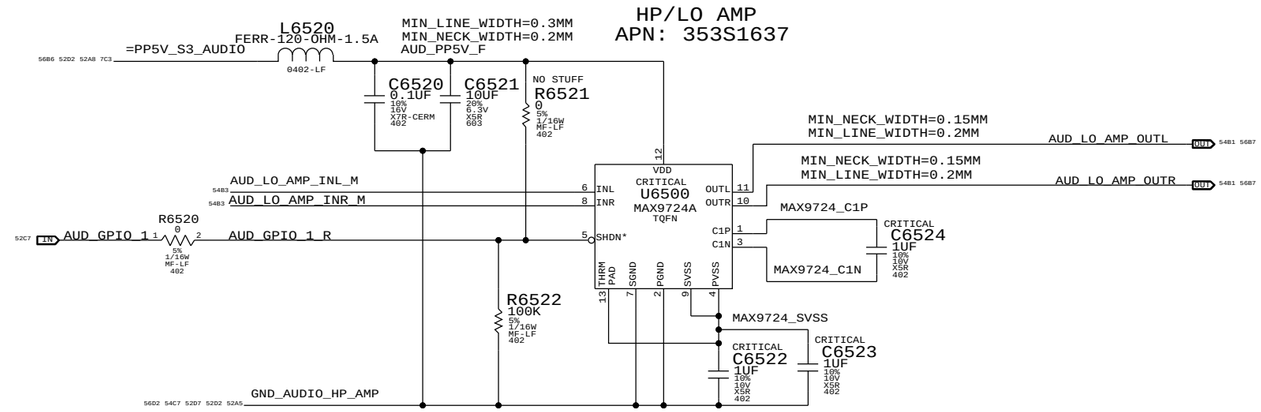
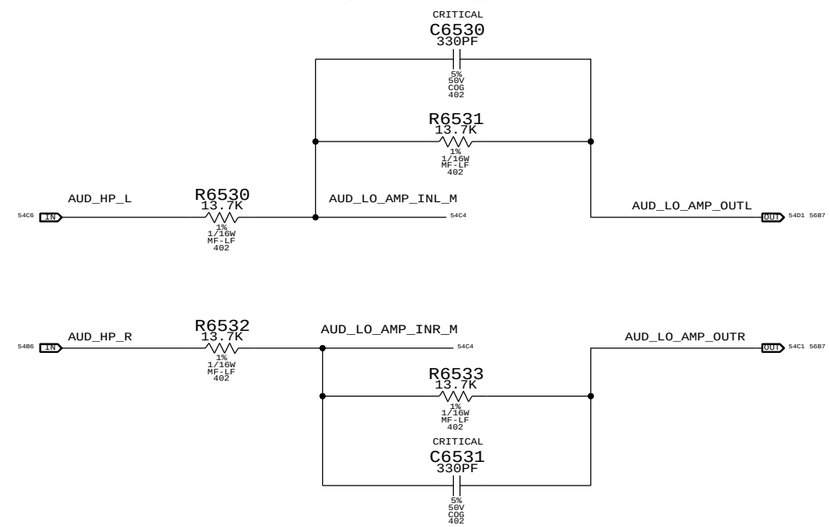
FOR PROTO2, STUFF R6521 AND NO STUFF R6520 AND R6522 UNTIL
RE-TASKABLE IO SW SUPPORT AVAILABLE (FORCES IO INTO OUTPUT MODE).

ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER





MAX9724 GAIN/FILTER COMPONENTS
AV_PB = -1V/V, FC_LPF = 35.2KHZ



SYNC MASTER=AUDIO SYNC DATE=02/03/2009

PAGE TITLE
AUDIO: HEADPHONE FILTER

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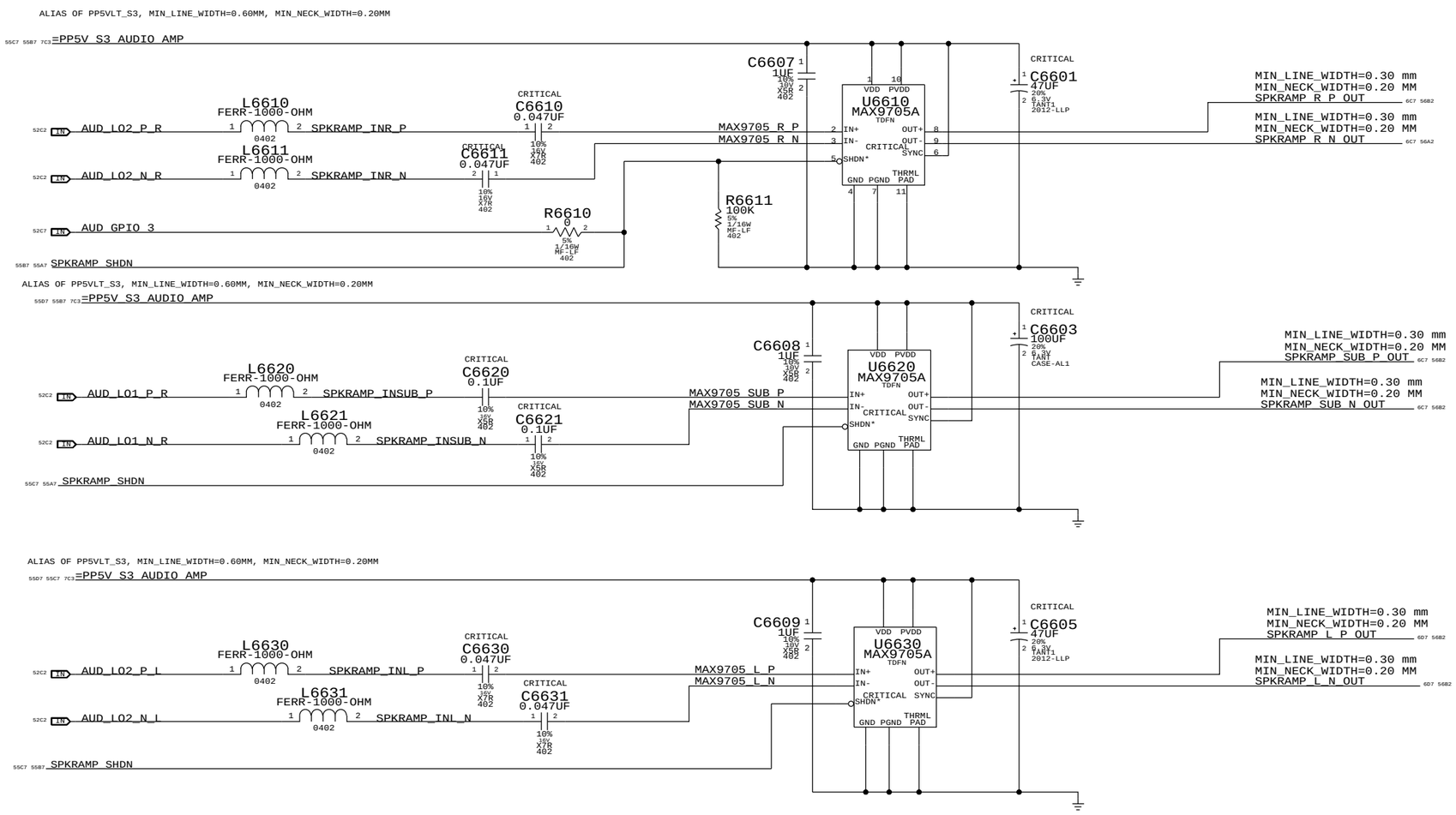
SATELLITE & SUB TWEETER AMPLIFIER

APN:353S2524

SATELLITE	169 HZ < FC < 282 HZ
SUB	80 HZ < FC < 132 HZ
GAIN	6DB



SYNC MASTER=AUDIO SYNC DATE=12/18/2008

PAGE TITLE

AUDI0: SPEAKER AMP

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DRAWING NUMBER 051-7898 SIZE D

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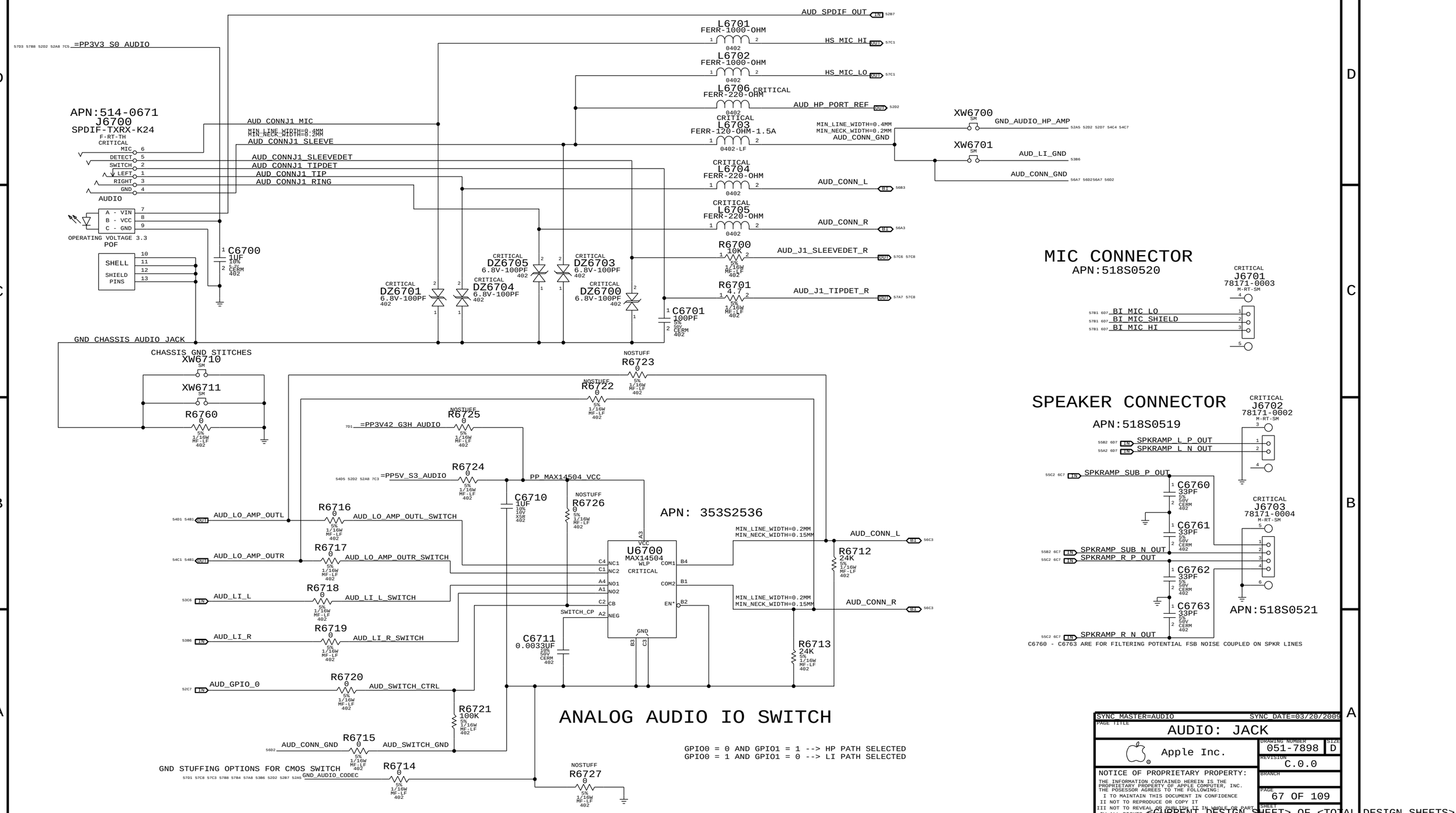
AUDIO JACK: LI/LO/HP CONNECTOR, SPDIF TX



SYNC_MASTER=AUDIO SYNC_DATE=03/20/2009

PAGE TITLE: AUDIO: JACK

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

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PAGE: 67 OF 109

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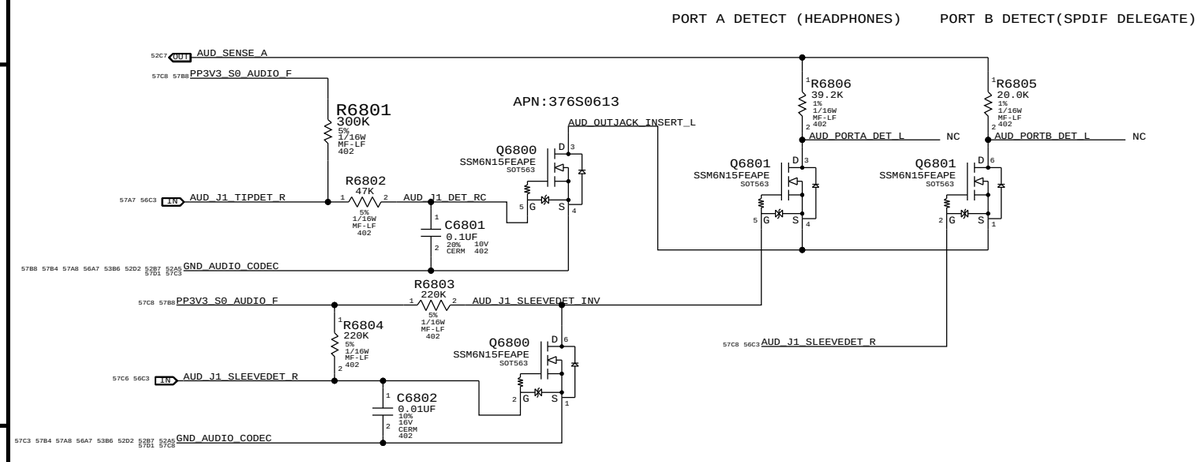
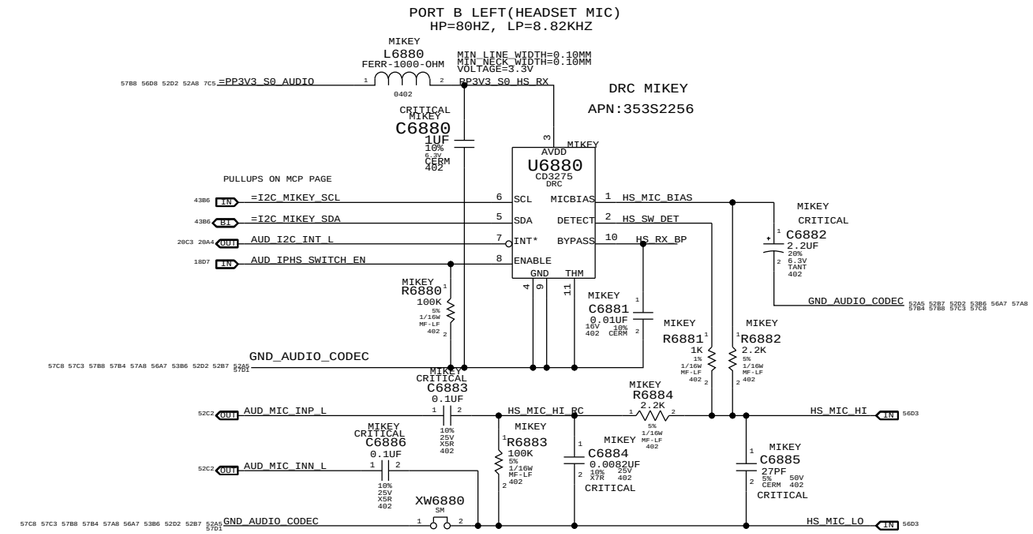
CODEC OUTPUT SIGNAL PATHS

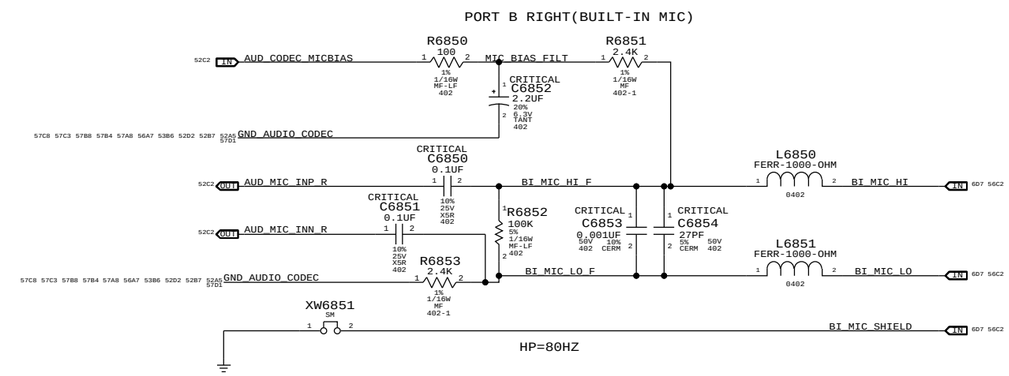
FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	GPIO_0 AND GPIO_1	0X09 (A)
LINE IN	0X05 (5)	0X05 (5)	0X0C (12)	GPIO_0 AND GPIO_1	0X09 (A)AND UI ELEMENT
SATELLITES	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0D (B)

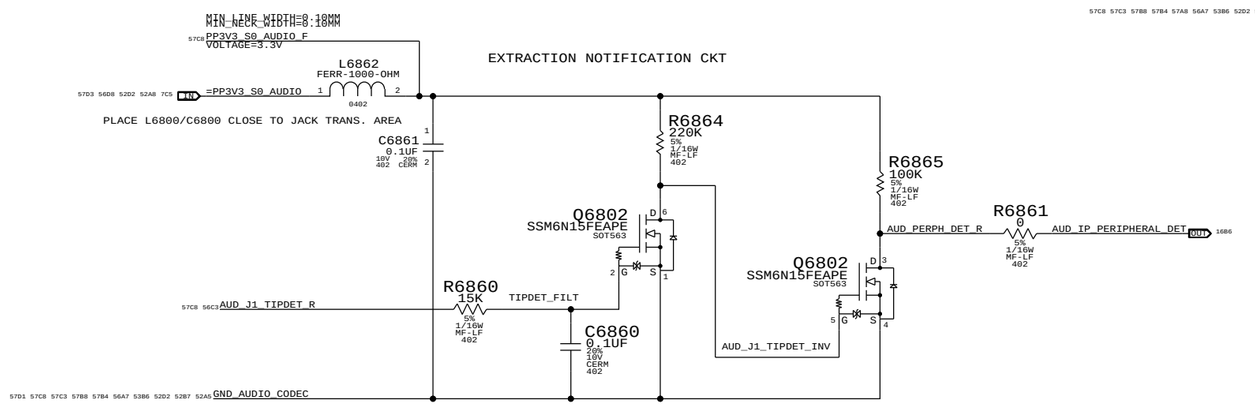
CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
BUILT-IN MIC	0X06 (6)	0X0D (13,B,RIGHT)	MIC_BIAS (80%)	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY









SYNC MASTER=AUDIO SYNC DATE=03/20/2009

PAGE TITLE
AUDIO: JACK TRANSLATORS

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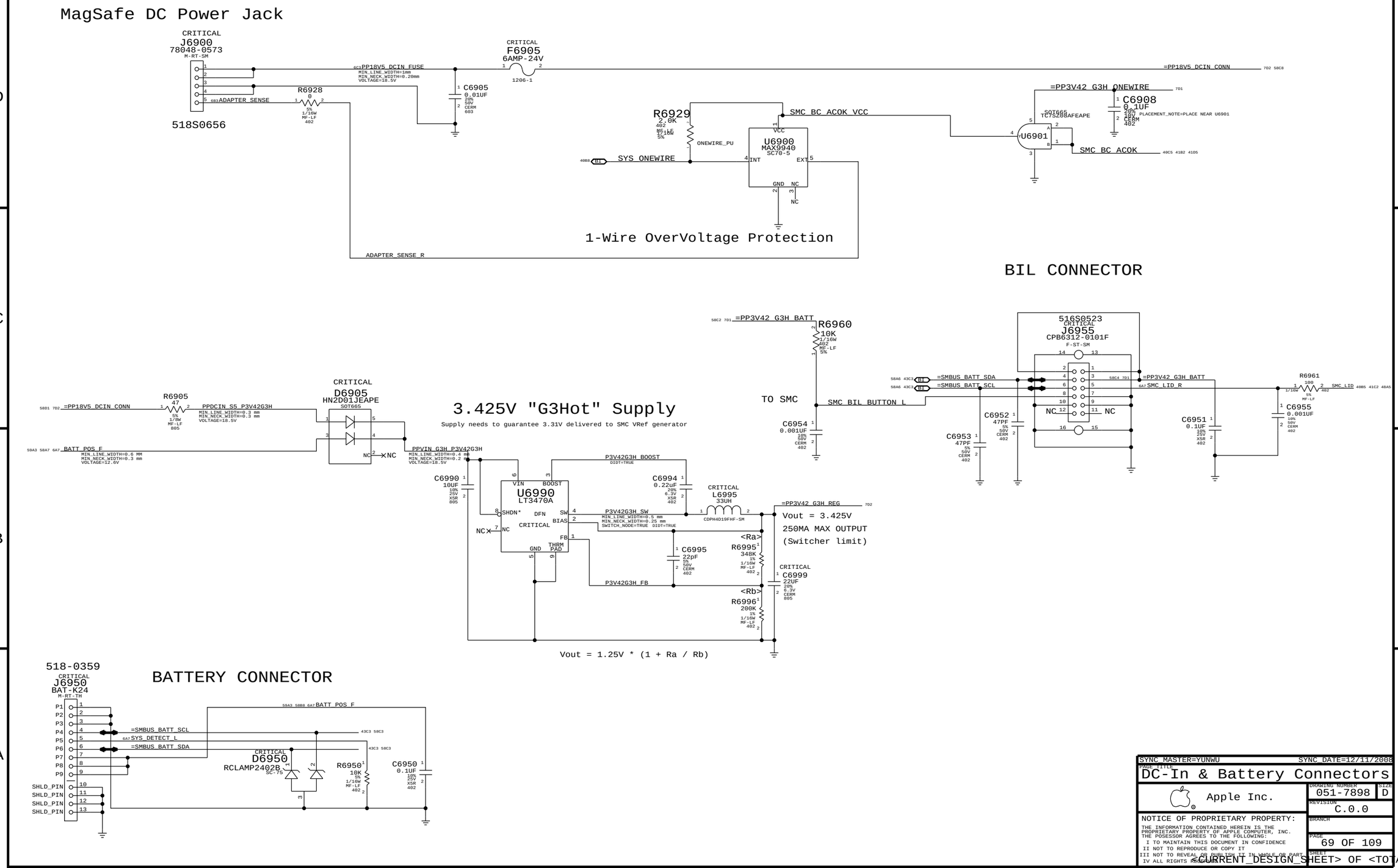

SYNC_MASTER=YUNWU SYNC_DATE=12/11/2008

PAGE TITLE: DC-In & Battery Connectors

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

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PAGE: 69 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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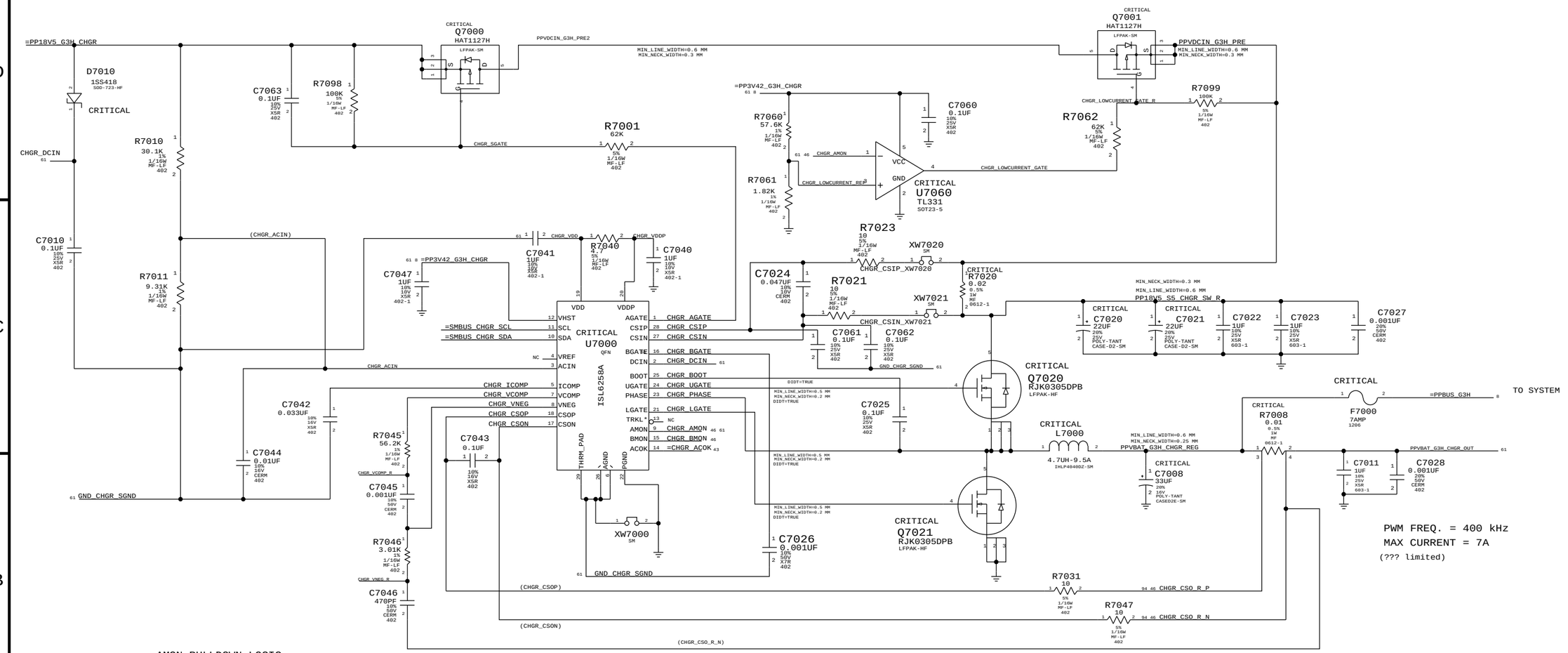
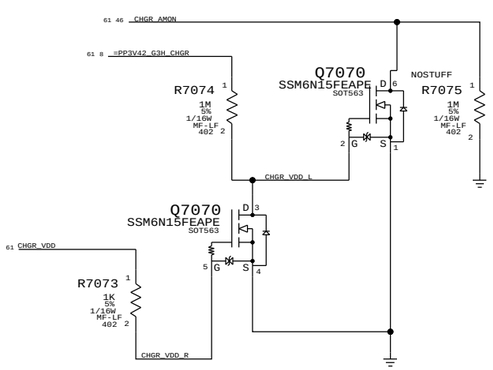
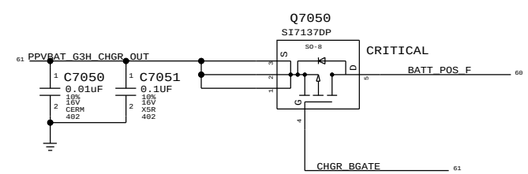
PBUS SUPPLY / BATTERY CHARGER



AMON PULLDOWN LOGIC



BATTERY CHARGE LIMITING FETS



SYNC_MASTER=K24_MLB	SYNC_DATE=05/20/2009
PAGE TITLE: PBUS Supply/Battery Charger	
Apple Inc.	DRAWING NUMBER: 051-7898 SIZE: D
	REVISION: C.0.0
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	PAGE: 70 OF 109
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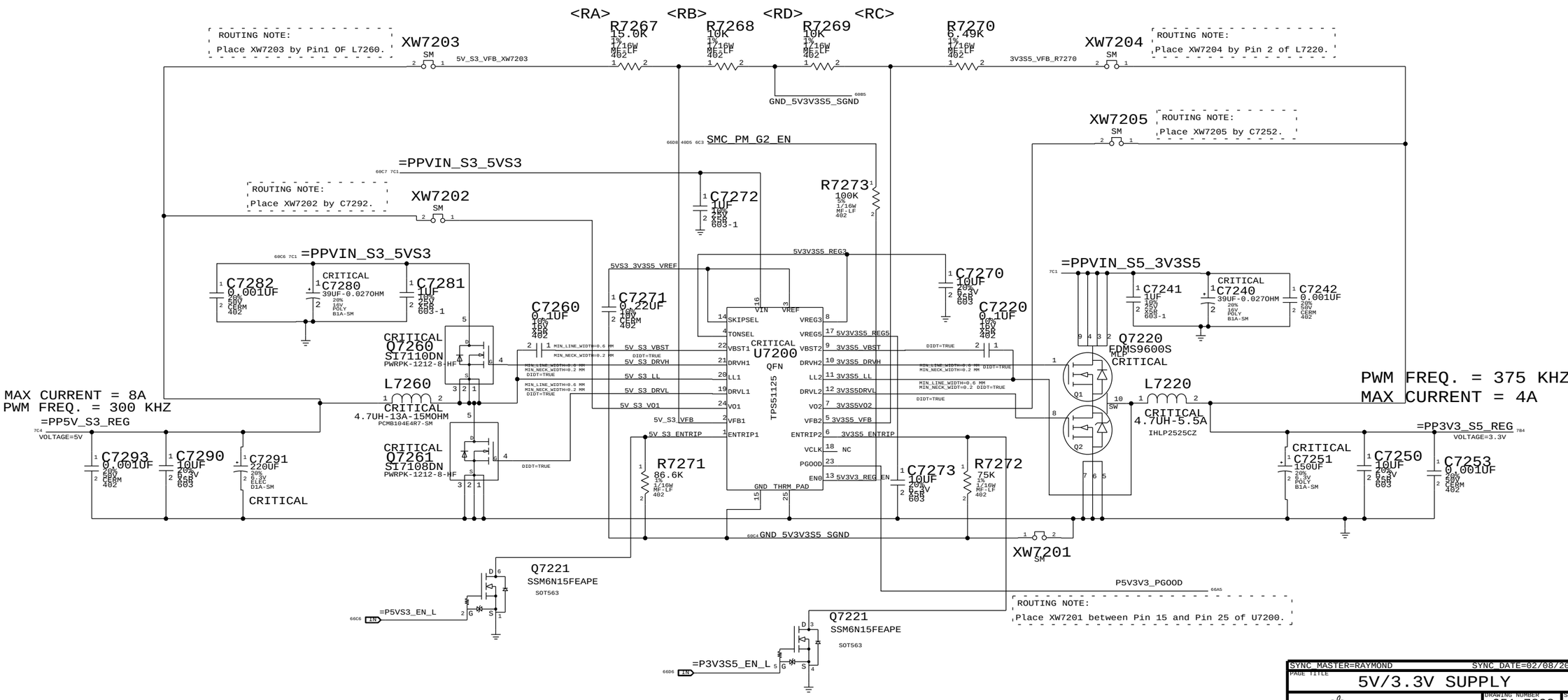
5V_S3/3.3V_S5 POWER SUPPLY

VOUT = (2 * RA / RB) + 2

VOUT = (2 * RC / RD) + 2



SYNC MASTER=RAYMOND SYNC DATE=02/08/2008

PAGE TITLE: 5V/3.3V SUPPLY

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

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PAGE: 72 OF 109

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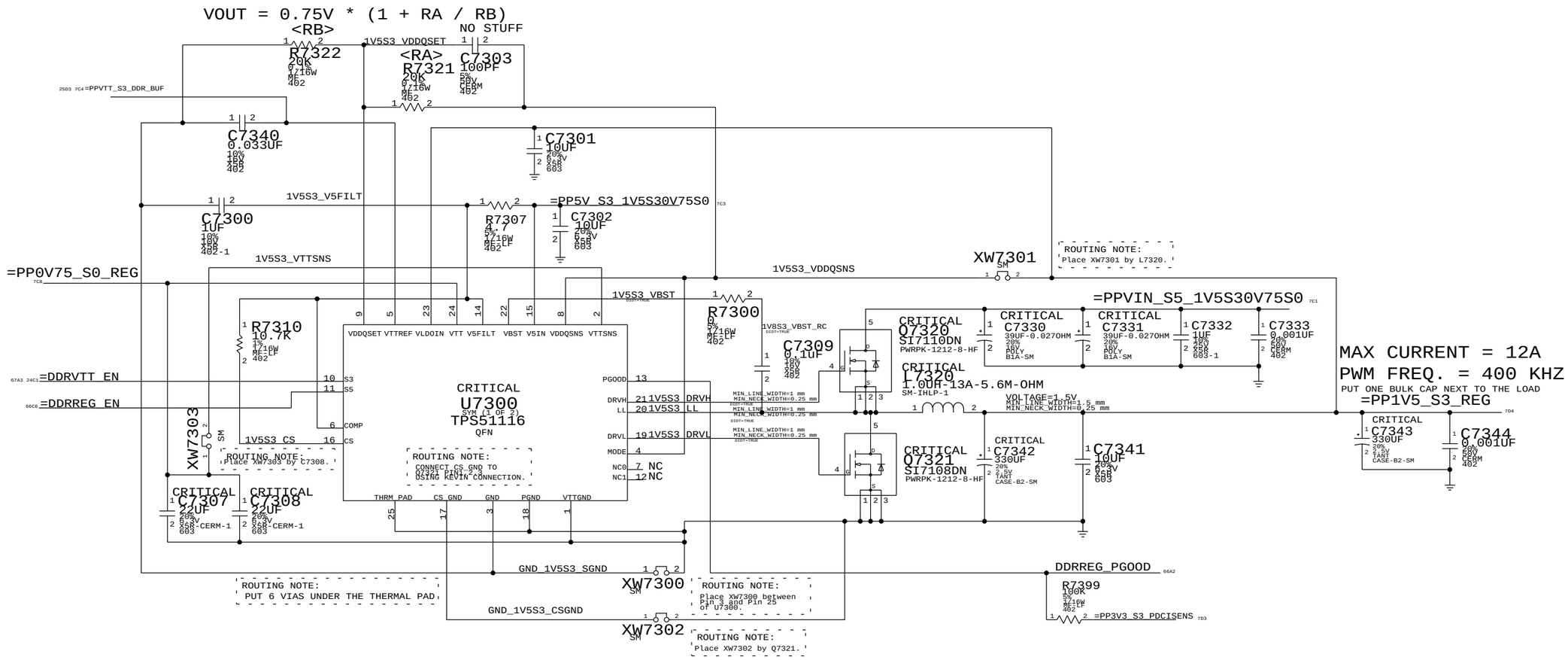
1.5V/0.75V(DDR3) POWER SUPPLY



STATE	PM_SLP_S4_L	PM_SLP_S3_L	PP1V5_S3	PP0V75_S0
S0	HIGH	HIGH	1.5V	0.75V
S3	HIGH	LOW	1.5V	0.0V
S5/G3HOT	LOW	LOW	0.0V	0.0V

SYNC MASTER=RAYMOND SYNC DATE=01/31/2008

PAGE TITLE
1.5V/0.75V DDR3 SUPPLY

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

REVISION C.0.0

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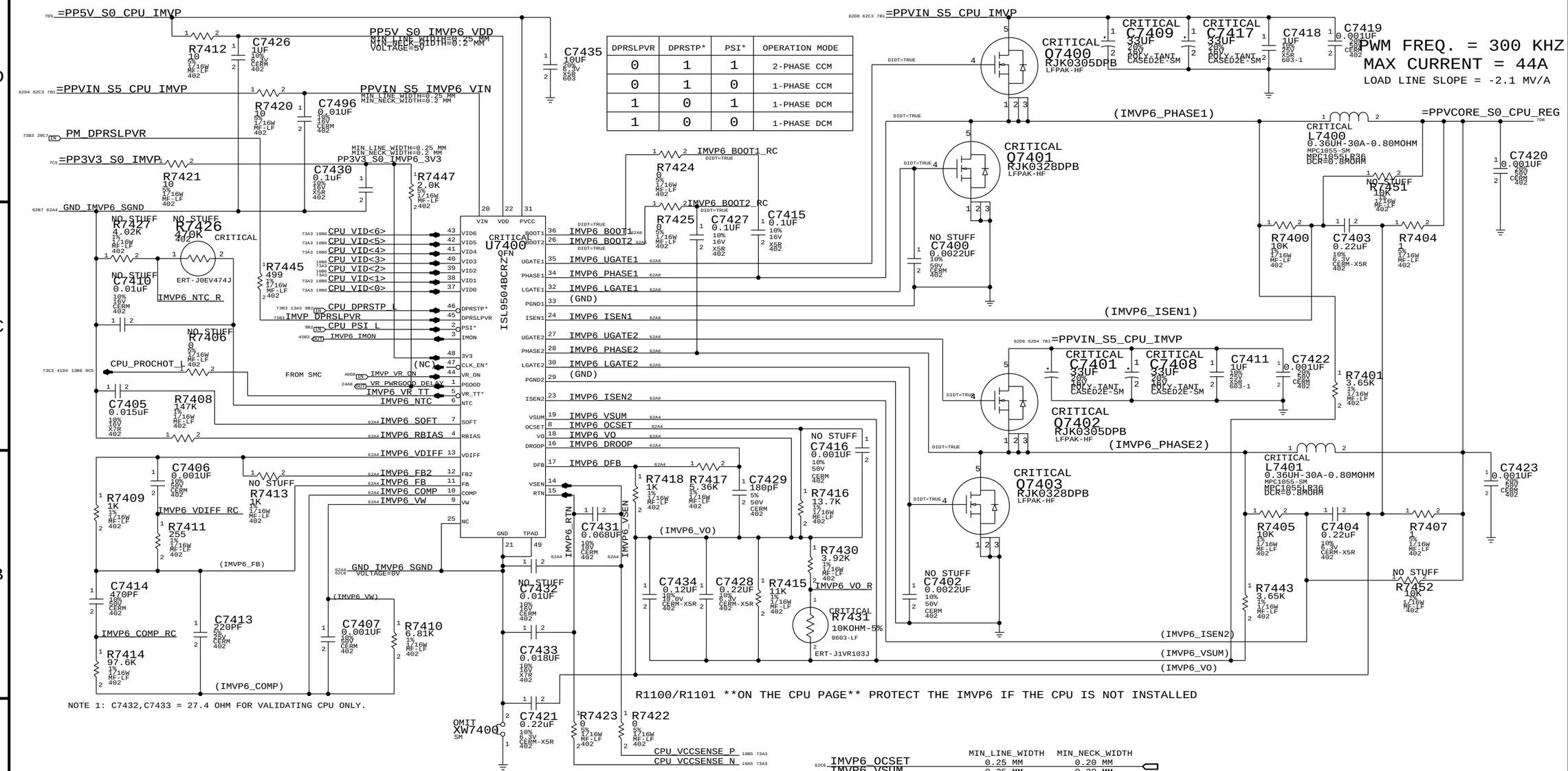

DPRSLPVR	DPRSTP*	PSI*	OPERATION MODE
0	1	1	2-PHASE CCM
0	1	0	1-PHASE CCM
1	0	1	1-PHASE DCM
1	0	0	1-PHASE DCM

NOTE 1: C7432,C7433 = 27.4 OHM FOR VALIDATING CPU ONLY.

R1100/R1101 **ON THE CPU PAGE** PROTECT THE IMVP6 IF THE CPU IS NOT INSTALLED

IMVP6 CPU VCORE REGULATOR

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
IMVP6_RTN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

SYNC_MASTER=RAYMOND SYNC_DATE=01/31/2008

PAGE TITLE: IMVP6 CPU VCore Regulator

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

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PAGE: 74 OF 109

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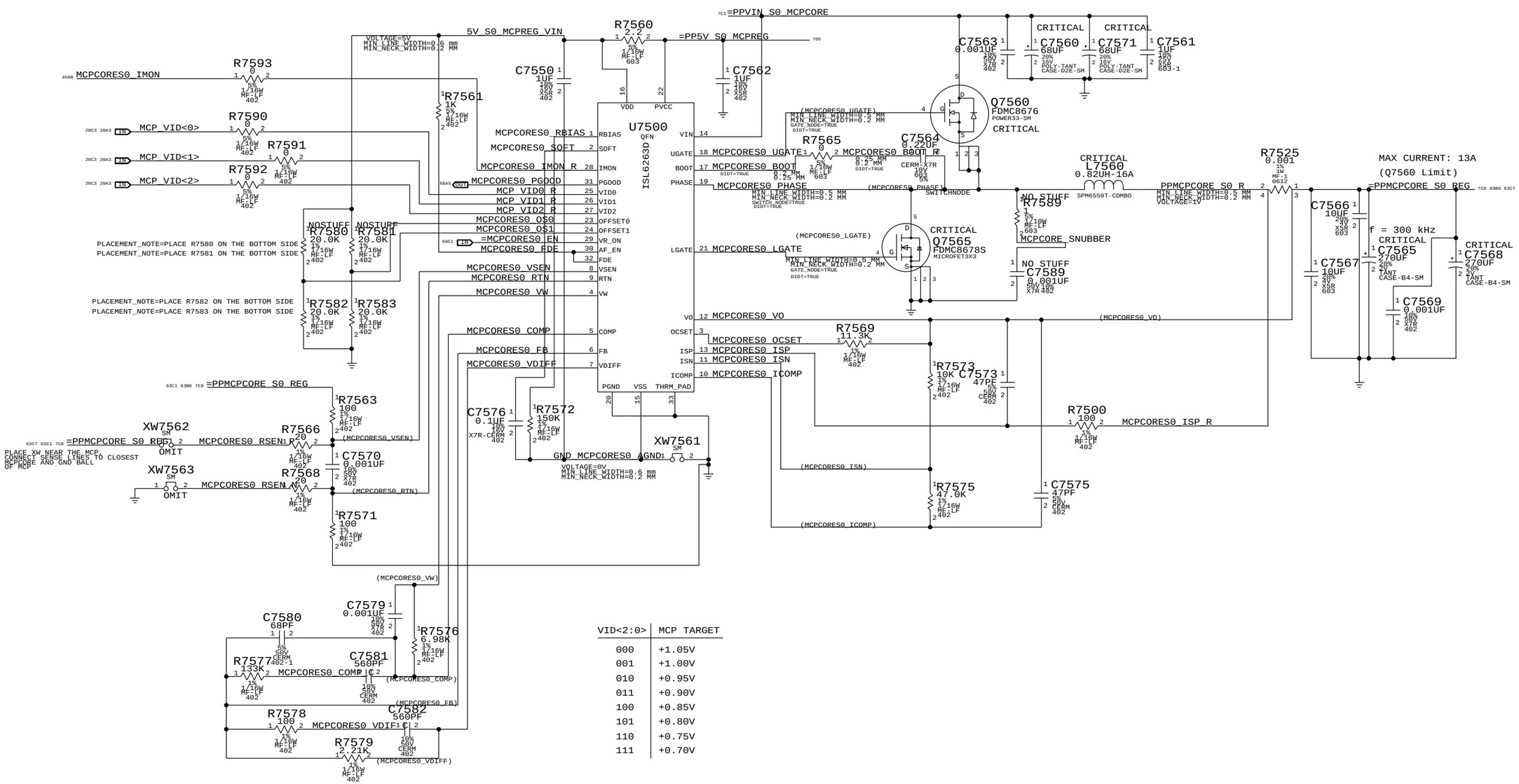
MCP VCORE POWER SUPPLY



VID<2:0>	MCP TARGET
000	+1.05V
001	+1.00V
010	+0.95V
011	+0.90V
100	+0.85V
101	+0.80V
110	+0.75V
111	+0.70V

SYNC MASTER=K19 MLB SYNC DATE=12/10/2008

PAGE TITLE
MCP CORE REGULATOR

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

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PAGE 75 OF 109

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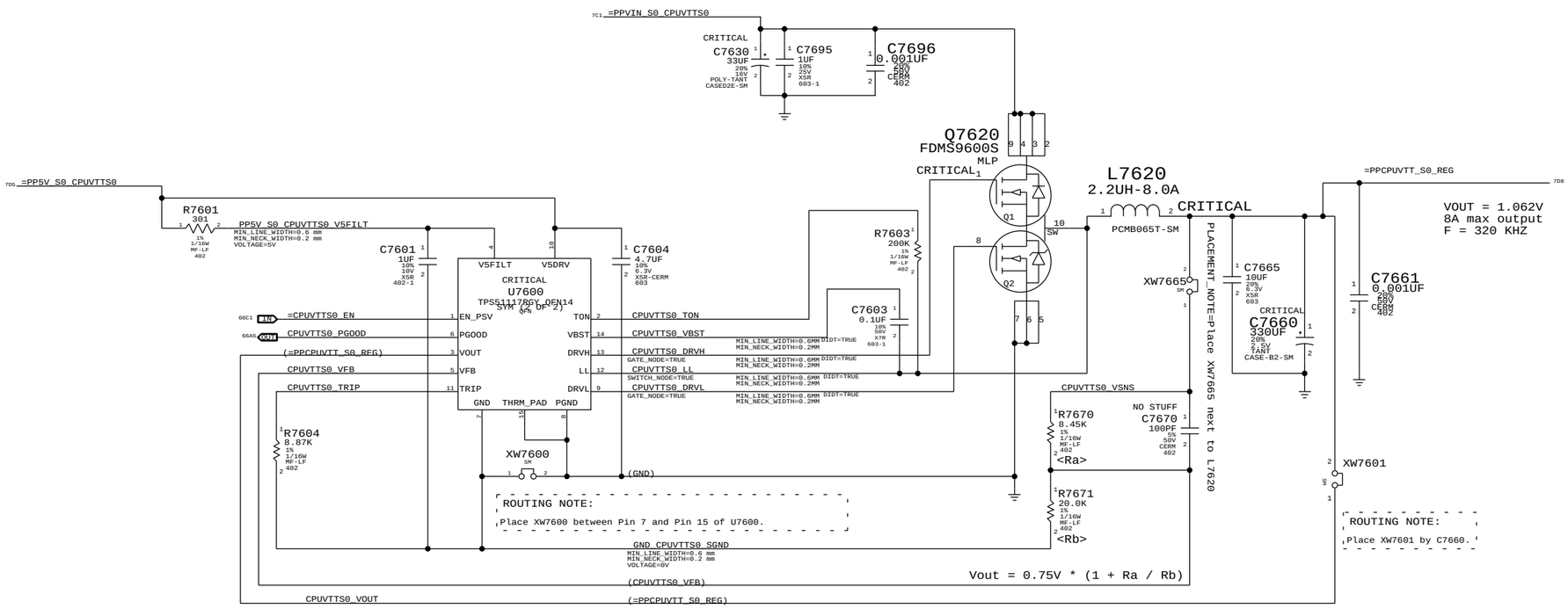
CPUVTT POWER SUPPLY



SYNC_MASTER=RAYMOND SYNC_DATE=02/08/2008

PAGE TITLE
CPU VTT(1.05V) SUPPLY

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

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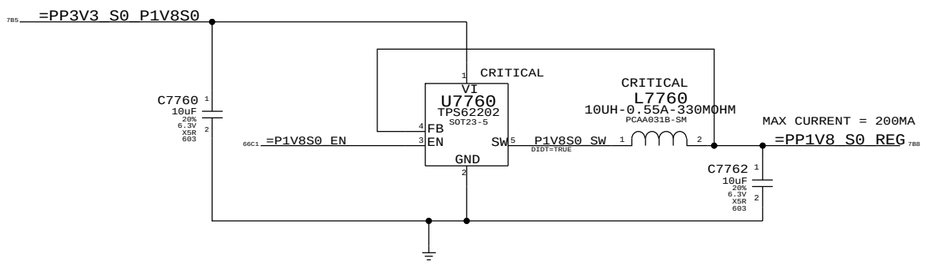
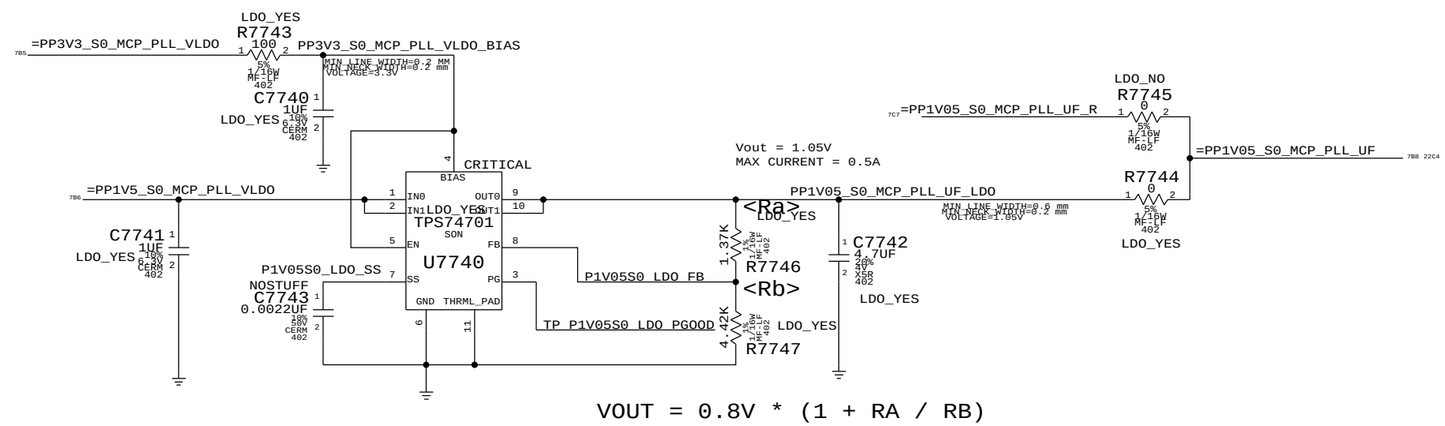
1.8V S0 SWITCHER

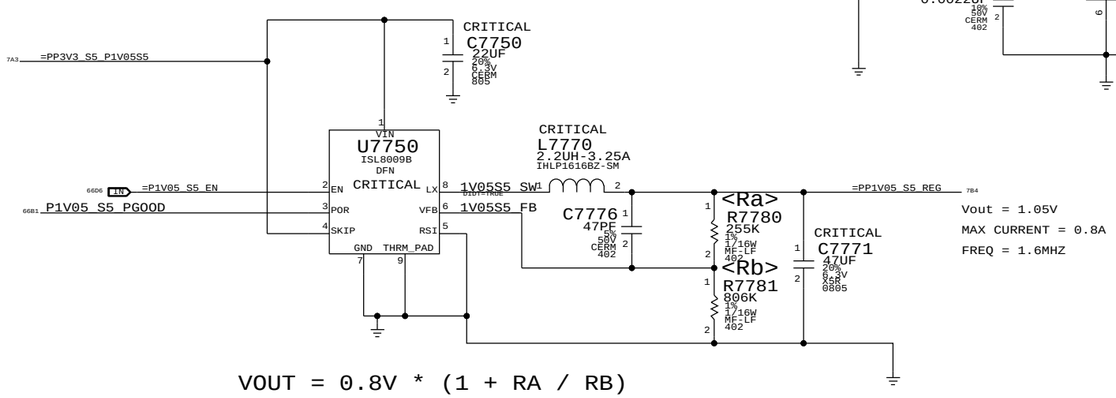


1.05V S0 PLL LDO



VOUT = 0.8V * (1 + RA / RB)

MCP 1.05V S5 (AUXC) SUPPLY



VOUT = 0.8V * (1 + RA / RB)

SYNC_MASTER=RAYMOND SYNC_DATE=01/23/2008

PAGE TITLE
MISC POWER SUPPLIES

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

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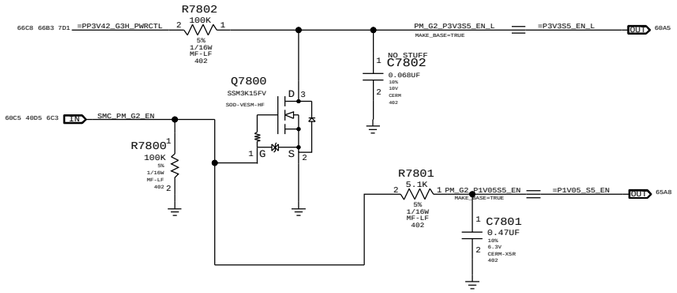
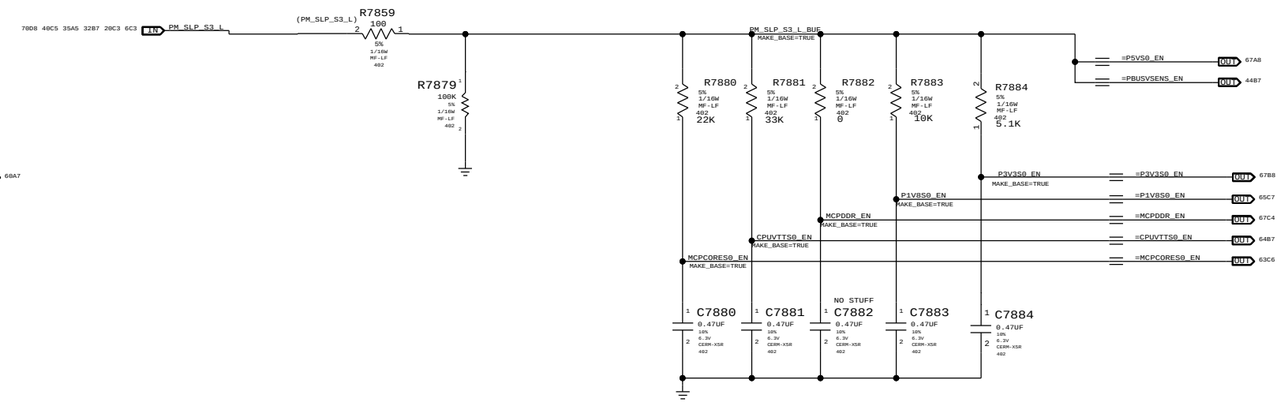
3.3V 1.05V S5 ENABLE



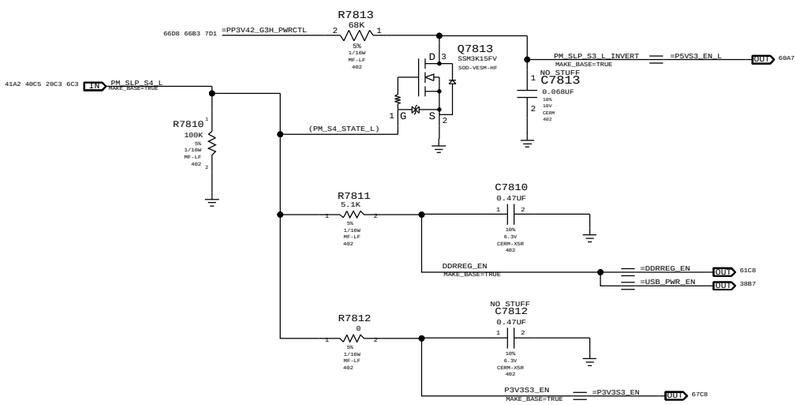
Power Control Signals

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

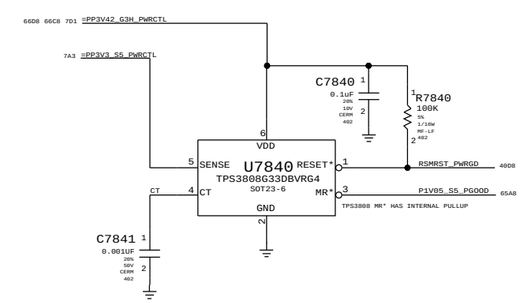
3.3V_S0, 1.8V_S0 ENABLE
MCPDDR, CPUVTT,MCPCORES0 ENABLE
1.5V S0 AND 1.05V S0 ENABLE



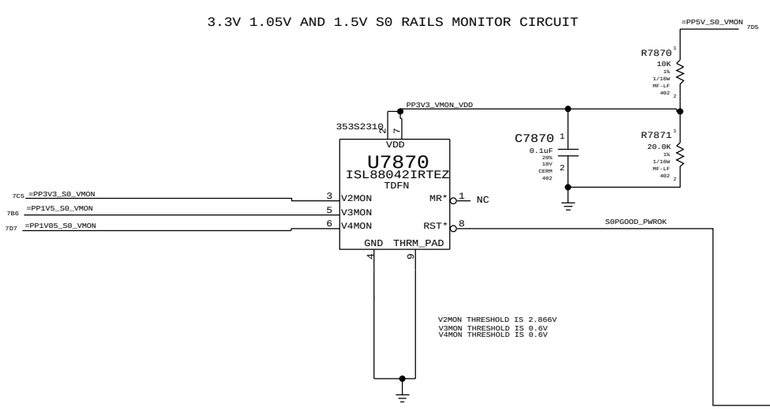
S3 ENABLE



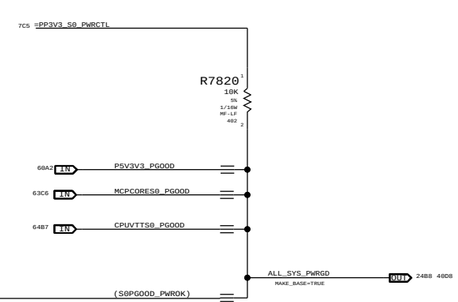
VOLTAGE MONITOR



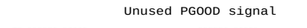
3.3V 1.05V AND 1.5V S0 RAILS MONITOR CIRCUIT



OTHER S0 RAILS PGOOD



Unused PGOOD signal



SYNC MASTER=YUAN.MA SYNC DATE=12/11/2008

PAGE TITLE

POWER SEQUENCING

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

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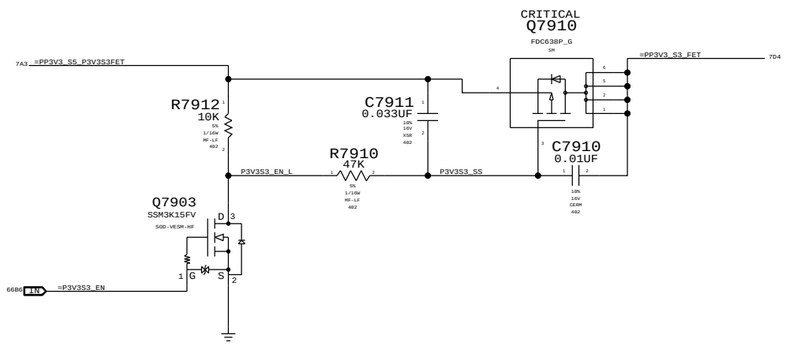
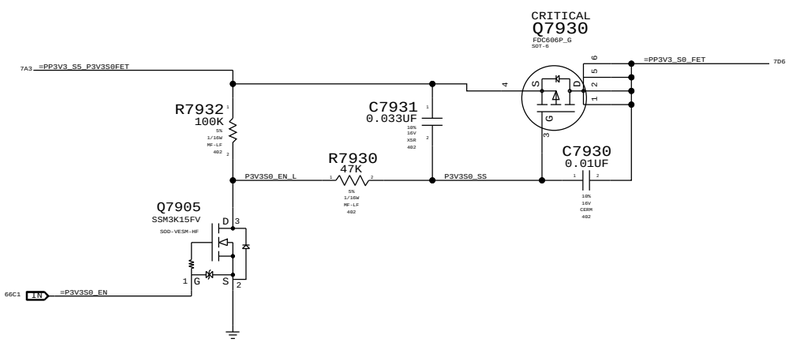
3.3V S3 FET



3.3V S3 FET

MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.182 A (EDP)

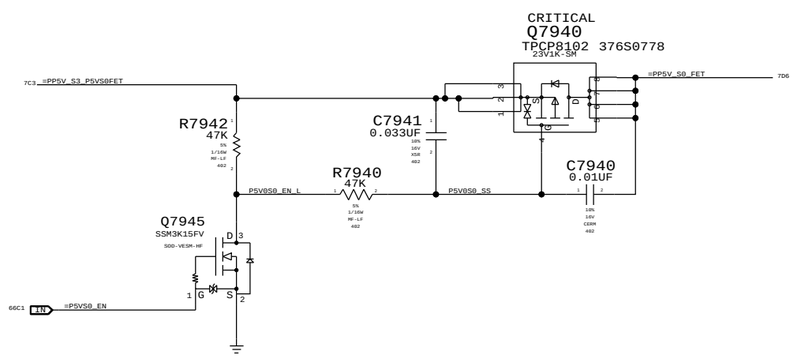
3.3V S0 FET



3.3V S0 FET

MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 MOHM @4.5V
LOADING	1.431 A (EDP)

5.0V S0 FET

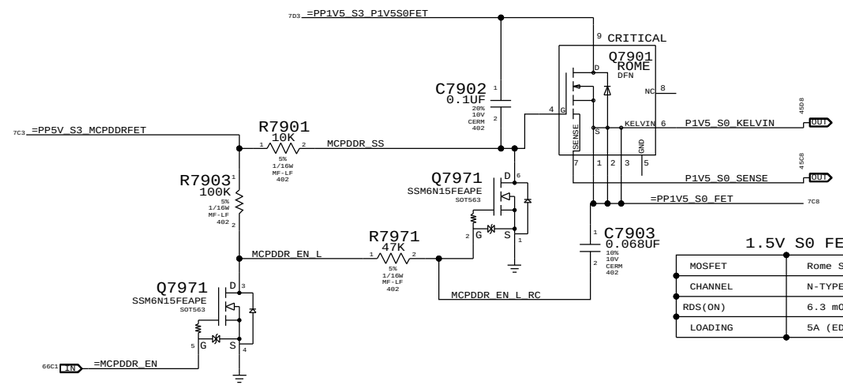


5.0V S0 FET

MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	13.5 MOHM @4.5V
LOADING	1.7 A (EDP)

1.5V S0 FET

(1.5V S0 FET FOR DDR3 MEM, MCP79 AND CPU)

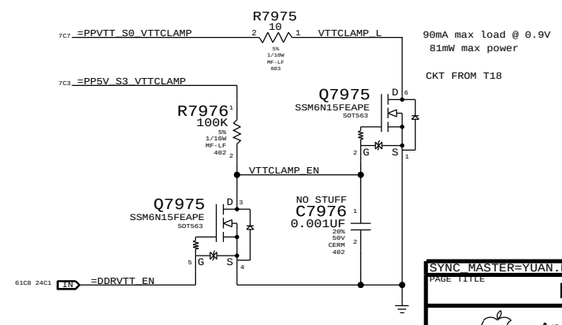


1.5V S0 FET

MOSFET	Rome SenseFET
CHANNEL	N-TYPE
RDS(ON)	6.3 mOHM @4.5V VGS
LOADING	5A (EDP)

MCP79 DDRVTT FET

MCP79 DDR PAD LEAKAGE IS HIGH ENOUGH THAT
NVIDIA RECOMMENDS UNPOWERING DURING SLEEP.
IN ORDER TO SUPPORT UNPOWERING RAIL, HARDWARE
MUST GUARANTEE MEM_CKE SIGNALS ARE LOW
BEFORE RAIL IS TURNED OFF, AND REMAINS LOW
UNTIL AFTER RAIL TURNS BACK ON OR DIMMS
WILL EXIT SELF-REFRESH PREMATURELY.
MEM_VTT_EN OUTPUT FROM MCP79 USED TO ENABLE CLAMP
ON VTT RAIL, WHICH PULLS ALL CKE SIGNALS
LOW THROUGH VTT TERMINATION RESISTORS.



SYNC MASTER=YUAN.MA SYNC DATE=12/11/2008

PAGE TITLE
POWER FETS

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

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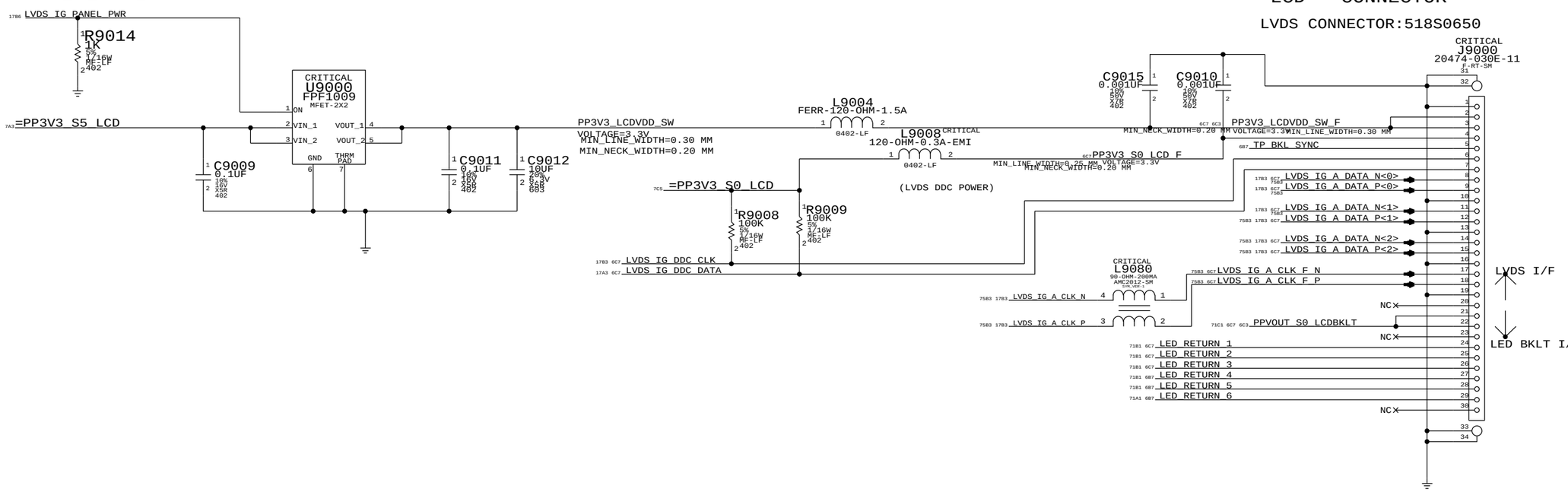
CHECK IF LVDS_IG_PANEL_PWR GLITCHES ON POWER UP



SYNC_MASTER=NMARTIN SYNC_DATE=04/04/2008

PAGE TITLE
LVDS CONNECTOR

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DRAWING NUMBER 051-7898 SIZE D

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178G =MCP_HDMI_TXC_P	DP_ML_P<3>	MAKE_BASE=TRUE	70C8 75C3
178G =MCP_HDMI_TXC_N	DP_ML_N<3>	MAKE_BASE=TRUE	70C8 75C3
178G =MCP_HDMI_TXD_P<0>	DP_ML_P<2>	MAKE_BASE=TRUE	70C1 75C3
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178G =MCP_HDMI_TXD_P<2>	DP_ML_P<0>	MAKE_BASE=TRUE	70C1 75C3
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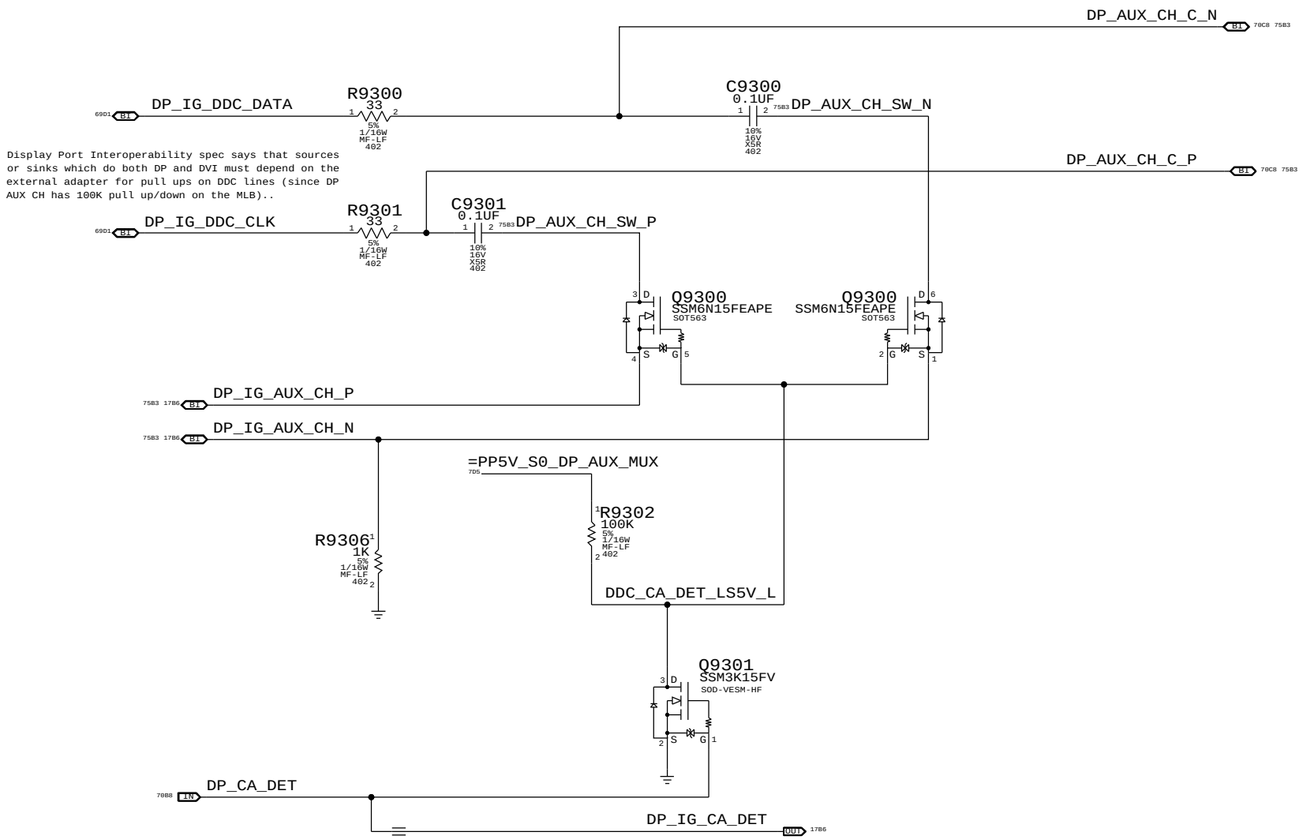
178G =MCP_HDMI_HPD	DP_HPD	MAKE_BASE=TRUE	70A8
17A3 =MCP_HDMI_DDC_CLK	DP_IG_DDC_CLK	MAKE_BASE=TRUE	69C8
17A3 =MCP_HDMI_DDC_DATA	DP_IG_DDC_DATA	MAKE_BASE=TRUE	69C8



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PAGE TITLE
DISPLAYPORT SUPPORT

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

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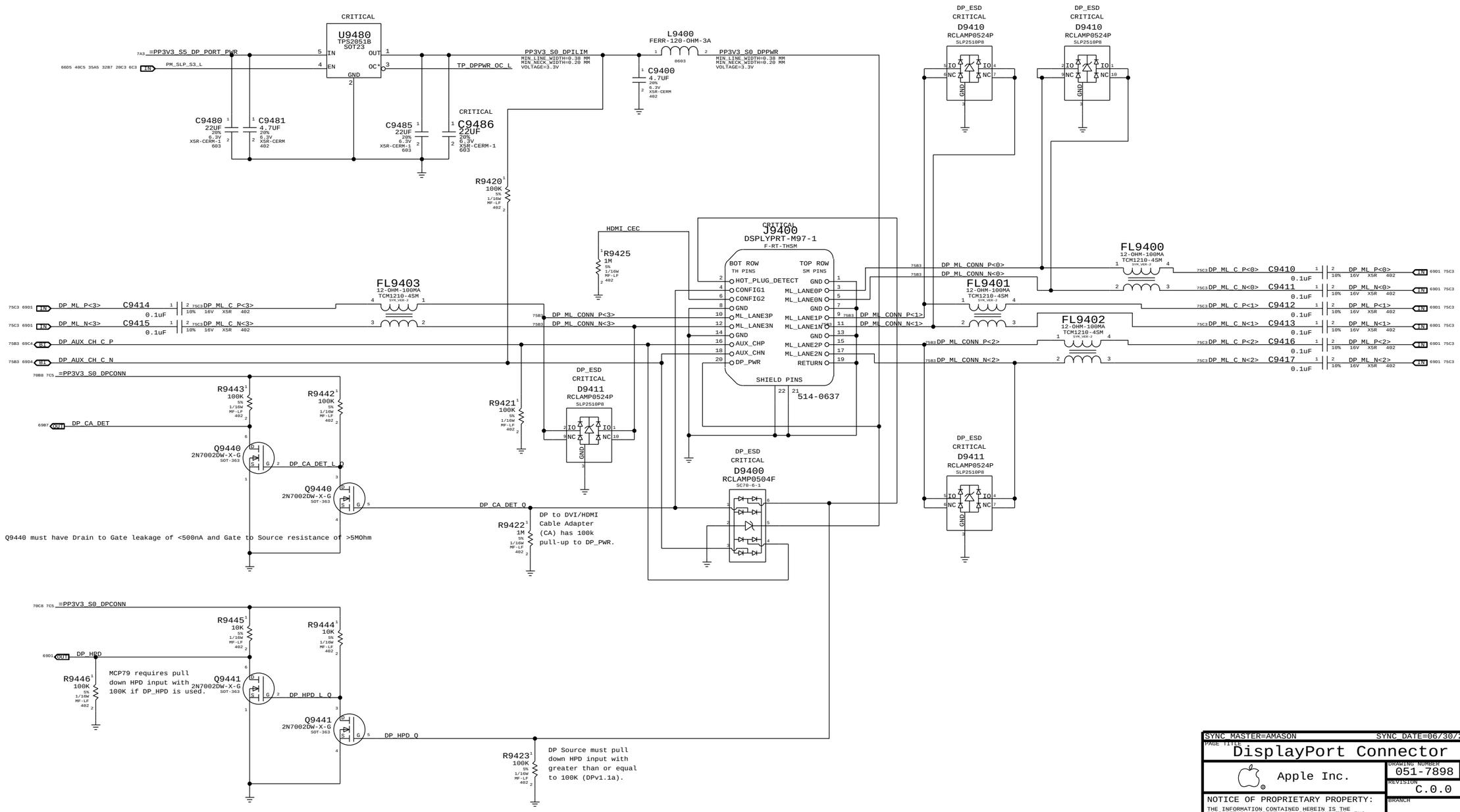
Port Power Switch



SYNC_MASTER=AMASON	SYNC_DATE=06/30/2008
PAGE TITLE: DisplayPort Connector	
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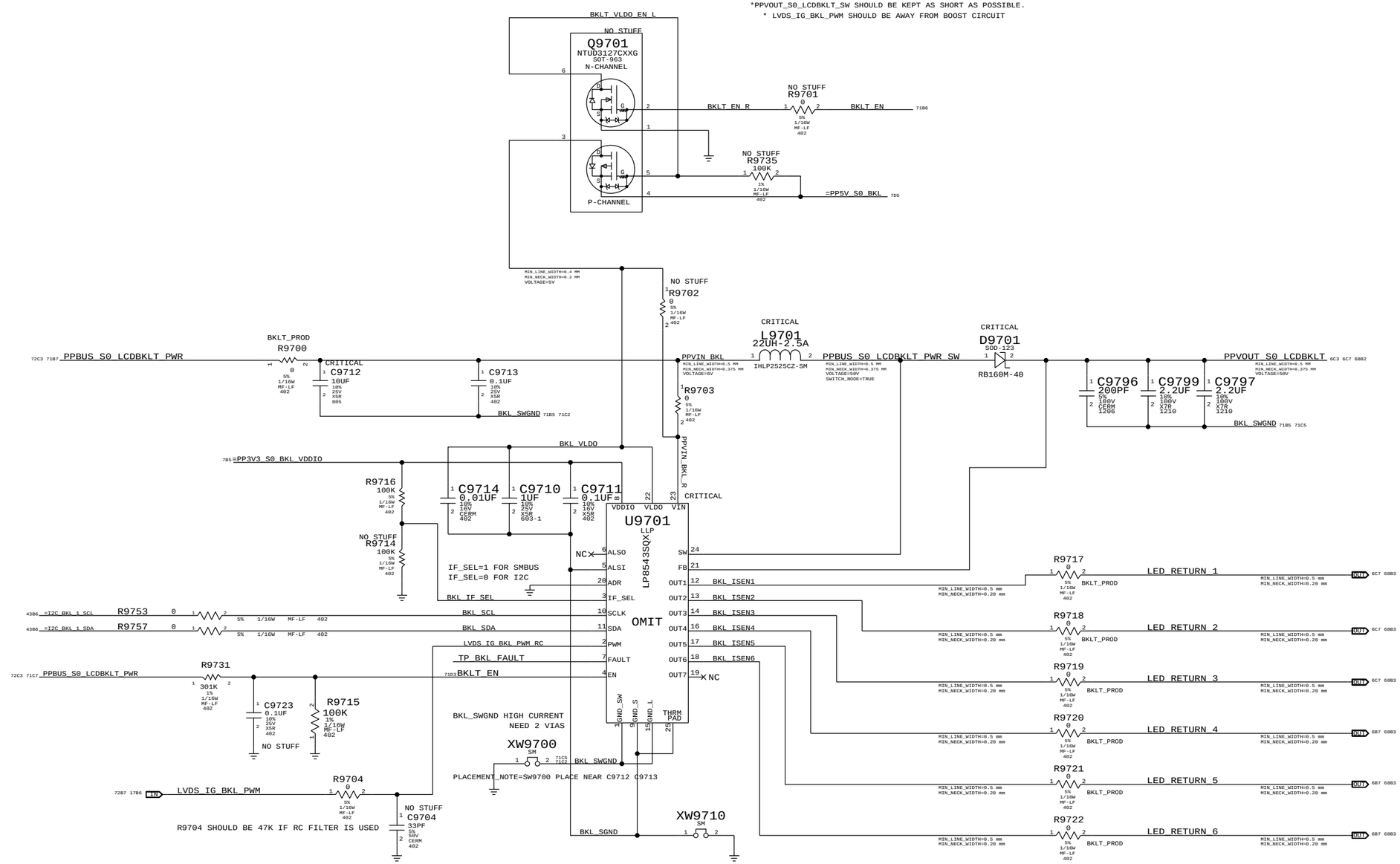
*L9701, D9701, C9796, C9797, C9799, C9712 AND C9713 SHOULD ALL BE PLACED NEAR EACHOTHER.
*PPVOUT_S0_LCDBKLT_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
* LVDS_IG_BKL_PWM SHOULD BE AWAY FROM BOOST CIRCUIT



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	6	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9717,R9718,R9719,R9720,R9721,R9722		BKLT_ENG
116S0005	1	RES,1/16W,0.1 OHM,1%,0402,SM	R9700		BKLT_ENG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S2670	1	IC,LP8543,WHT LED BKLT CTRLR,QFN24,PROD	U9701	CRITICAL	

SYNC MASTER=KIRAN SYNC DATE=12/05/2008

PAGE TITLE
LCD BACKLIGHT DRIVER

Apple Inc.

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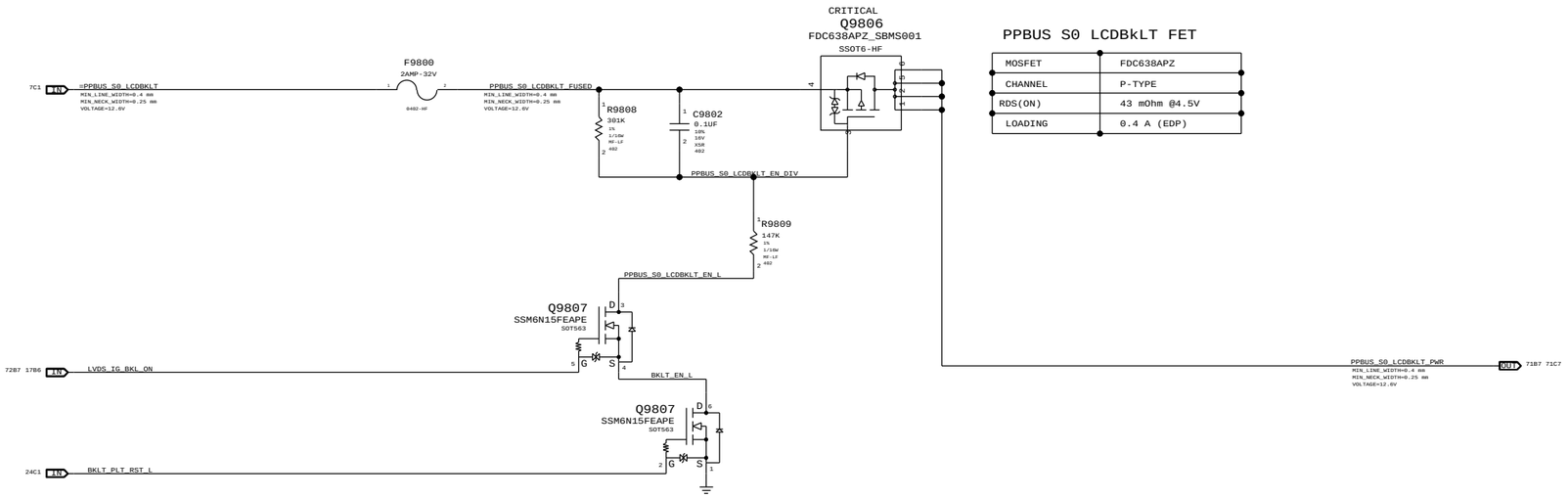
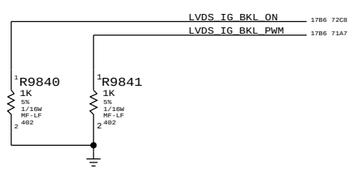


PPBUS S0 LCDBkLT FET

MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.4 A (EDP)



MCP HAS INTERNAL 10K PULL-UP FOR THESE SIGNALS

SYNC MASTER=YITE SYNC DATE=06/30/2008

PAGE TITLE
LCD Backlight Support

Apple Inc.

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FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
Signals within each 4x group should be matched within 5 ps of strobe.
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.
DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.
Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.
Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FSB 4X Signal Groups	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_D_L<15..0>	9C4 13D3
	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_DINV_L<0>	9C4 13D6
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<0>	9C4 13D6
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<0>	9C4 13D6
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_D_L<31..16>	9B4 9C4 13C3 13D3
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_DINV_L<1>	9B4 13D6
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<1>	9B4 13D6
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<1>	9B4 13D6
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_D_L<47..32>	9C2 13B3 13C3
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_DINV_L<2>	9C2 13D6
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<2>	9C2 13D6
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<2>	9C2 13D6
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_D_L<63..48>	9B2 9C2 13B3
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_DINV_L<3>	9B2 13D6
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<3>	9B2 13D6
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<3>	9B2 13D6
FSB 2X Signals	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_A_L<16..3>	9D8 13C6 13D6
	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_REQ_L<4..0>	9D8 13B6
	FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<0>	9D8 13B6
	FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB_A_L<35..17>	9C8 9D8 13C6
	FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<1>	9C8 13B6
FSB 1X Signals	FSB_1X	FSB_50S	FSB_1X	FSB_ADS_L	9D6 13B6
	FSB_RBREQ0_L	FSB_50S	FSB_1X	FSB_BREQ0_L	9D6 13B6
	FSB_RBREQ1_L	FSB_50S	FSB_1X	FSB_BREQ1_L	13B6
	FSB_1X	FSB_50S	FSB_1X	FSB_BNR_L	9D6 13B6
	FSB_1X	FSB_50S	FSB_1X	FSB_BPRI_L	9D6 13B3
	FSB_1X	FSB_50S	FSB_1X	FSB_DBSY_L	9D6 13B6
	FSB_1X	FSB_50S	FSB_1X	FSB_DEFER_L	9D6 13B3
	FSB_1X	FSB_50S	FSB_1X	FSB_DRDY_L	9D6 13B6
	FSB_1X	FSB_50S	FSB_1X	FSB_HIT_L	9D6 13B6
	FSB_1X	FSB_50S	FSB_1X	FSB_HITM_L	9D6 13B6
	FSB_1X	FSB_50S	FSB_1X	FSB_LOCK_L	9D6 13B6
	FSB_CPURST_L	FSB_50S	FSB_1X	FSB_CPURST_L	9D6 12C2 13A3
	FSB_1X	FSB_50S	FSB_1X	FSB_RS_L<2..0>	9D6 13A6
	FSB_1X	FSB_50S	FSB_1X	FSB_TRDY_L	9D6 13B6
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_A20M_L	9C8 13A3
	CPU_BSEL	CPU_50S	CPU_AGTL	CPU_BSEL<2..0>	8B2 9B4
	CPU_FERR_L	CPU_50S	CPU_8MIL	CPU_FERR_L	9C8 13B7
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_IGNNE_L	9C8 13A3
	CPU_INIT_L	CPU_50S	CPU_AGTL	CPU_INIT_L	9D6 13A3
	CPU_ASYNC_P	CPU_50S	CPU_AGTL	CPU_INTR	9C8 13A3
	CPU_ASYNC_P	CPU_50S	CPU_AGTL	CPU_NMI	9B8 13A3
	CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	9C5 13B6 41D4 62C8
	CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	9B2 12C7 13A3
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_SMI_L	9B8 13A3
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_STPCLK_L	9C8 13A3
	PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	9C6 13B7 41C4
	FSB_CPUSLP_L	CPU_50S	CPU_AGTL	FSB_CPUSLP_L	9B2 13A3
	CPU_FROM_SB	CPU_50S	CPU_AGTL	CPU_DPSLP_L	9B2 13A3
	CPU_DPRSTP_L	CPU_50S	CPU_AGTL	CPU_DPRSTP_L	9B2 13A3 62C7
	CPU_ASYNC	CPU_50S	CPU_AGTL	FSB_DPWR_L	9B2 13A3
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_VDD	13A6
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_GND	13A6
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_VCC	13A6
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_GND	13A6
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	9B6 13B3
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	9B6 13B3
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_P	12C3 13B3
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_N	12C3 13B3
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_P	13A4
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_N	13A4
	CPU_IERR_L	CPU_50S		CPU_IERR_L	9D6
	PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR	20C7 62D8
	(See above)	CPU_50S	CPU_AGTL	IMVP_DPRSLPVR	62C7
	CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU_GTLREF	9B4 25B1
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<3>	9B3
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	9B3
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<1>	9B3
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	9B3
	XDP_TDI	CPU_50S	CPU_TTP	XDP_TDI	9B6 9C6 12B3
	XDP_TDO	CPU_50S	CPU_TTP	XDP_TDO	9B6 9C6 12B3
	XDP_TMS	CPU_50S	CPU_TTP	XDP_TMS	9B6 9C6 12B3
	XDP_TCK	CPU_50S	CPU_TTP	XDP_TCK	9A6 9C6 12B6
	XDP_TRST_L	CPU_50S	CPU_TTP	XDP_TRST_L	9A6 9C6 12B3
	XDP_BPM_L	CPU_50S	CPU_TTP	XDP_BPM_L<4..0>	9C6 12C6
	XDP_BPM_L5	CPU_50S	CPU_TTP	XDP_BPM_L<5>	9C5 12C6
	(FSB_CPURST_L)	CPU_50S	CPU_TTP	XDP_CPURST_L	12C4
		CPU_50S	CPU_8MIL	CPU_VID<6..0>	10B6 62C7
		CPU_50S	CPU_8MIL	IMVP6_VID<6..0>	
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	10B5 62A5
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	10A5 62A5
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	

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PAGE TITLE
CPU/FSB Constraints

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR2:
DQ signals should be matched within 20 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.
All DQS pairs should be matched within 100 ps of clocks.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.
A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:
DQ signals should be matched within 5 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 180 ps
No DQS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
A/BA/cmd signals should be matched within 5 ps of CLK pairs.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	7 MIL	7 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_P<5..0>	14B5 26C5 26C7
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_N<5..0>	14B5 26C5 26C7
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CKE<3..0>	14A5 26D5 26D7
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CS_L<3..0>	14B5 26C5 26C7
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_ODT<3..0>	14B5 26C5
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_A<14..0>	14B5 14C5 26C5 26C7
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_BA<2..0>	14C5 26C5 26C7
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_RAS_L	14C5 26C5
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_CAS_L	14C5 26C7
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_WE_L	14C5 26C7
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DQ<7..0>	14B7 26C2 26C4 26D2 26D4
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DQ<15..8>	14B7 26C2 26C4
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DQ<23..16>	14B7 14C7 26B2 26B4 26C2 26C4
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DQ<31..24>	14C7 26C2 26C4
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DQ<39..32>	14C7 26B5 26B7 26C5 26C7
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DQ<47..40>	14C7 14D7 26B5 26B7
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DQ<55..48>	14D7 26B5 26B7
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DQ<63..56>	14D7 26A5 26A7 26B5 26B7
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DM<0>	14A7 26C4
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DM<1>	14A7 26C2
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DM<2>	14B7 26B4
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DM<3>	14B7 26C2
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DM<4>	14B7 26B5
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DM<5>	14B7 26B7
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DM<6>	14B7 26B5
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DM<7>	14B7 26A7
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_P<0>	14D5 26C2
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_N<0>	14D5 26D2
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_P<1>	14D5 26C4
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_N<1>	14D5 26C4
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_P<2>	14D5 26B2
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_N<2>	14D5 26C2
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_P<3>	14D5 26C4
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_N<3>	14D5 26C4
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_P<4>	14D5 26B7
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_N<4>	14D5 26B7
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_P<5>	14D5 26B5
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_N<5>	14D5 26B5
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_P<6>	14D5 26B7
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_N<6>	14D5 26B7
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_P<7>	14D5 26A5
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_N<7>	14D5 26A5
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_P<5..0>	14B1 27C5 27C7
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_N<5..0>	14B1 27C5 27C7
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CKE<3..0>	14A1 27D5 27D7
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CS_L<3..0>	14B1 27C5 27C7
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_ODT<3..0>	14B1 27C5
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_A<14..0>	14B1 14C1 27C5 27C7
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_BA<2..0>	14C1 27C5 27C7
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_RAS_L	14C1 27C5
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_CAS_L	14C1 27C7
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_WE_L	14C1 27C7
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DQ<7..0>	14B3 27C2 27C4 27D2 27D4
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DQ<15..8>	14B3 27C2 27C4
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DQ<23..16>	14B3 14C3 27C2 27C4
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DQ<31..24>	14C3 27B2 27B4 27C2 27C4
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DQ<39..32>	14C3 27B5 27B7 27C5 27C7
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DQ<47..40>	14C3 14D3 27B5 27B7
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DQ<55..48>	14D3 27B5 27B7
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DQ<63..56>	14D3 27A5 27A7 27B5 27B7
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DM<0>	14A3 27C4
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DM<1>	14A3 27C2
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DM<2>	14B3 27C2
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DM<3>	14B3 27B4
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DM<4>	14B3 27B5
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DM<5>	14B3 27B7
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DM<6>	14B3 27B5
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DM<7>	14B3 27A7
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_P<0>	14D1 27C2
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_N<0>	14D1 27D2
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_P<1>	14D1 27C4
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_N<1>	14D1 27C4
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_P<2>	14D1 27C4
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_N<2>	14D1 27C4
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_P<3>	14D1 27B2
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_N<3>	14D1 27C2
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_P<4>	14D1 27B7
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_N<4>	14D1 27B7
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_P<5>	14D1 27B5
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_N<5>	14D1 27B5
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_P<6>	14D1 27B7
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_N<6>	14D1 27B7
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_P<7>	14D1 27A5
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_N<7>	14D1 27A5
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_VDD	15C6
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_GND	15C6

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Memory Constraints

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PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.4

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
SATA_90D_HDD	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_TERMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	PCIE_90D	PCIE	PCIE_MINI_R2D_P	6D5 29C7
	PCIE_90D	PCIE	PCIE_MINI_R2D_N	6D5 29C7
PCIE_MINI_R2D	PCIE_90D	PCIE	PCIE_MINI_R2D_C_P	16B3 29C5
	PCIE_90D	PCIE	PCIE_MINI_R2D_C_N	16B3 29C5
PCIE_MINI_D2R	PCIE_90D	PCIE	PCIE_MINI_D2R_P	6D5 16B6 29C7
	PCIE_90D	PCIE	PCIE_MINI_D2R_N	6D5 16B6 29C7
	PCIE_90D	PCIE	PCIE_FW_R2D_P	34C3
	PCIE_90D	PCIE	PCIE_FW_R2D_N	34C3
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE_FW_R2D_C_P	16B3 34C1
	PCIE_90D	PCIE	PCIE_FW_R2D_C_N	16B3 34C1
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE_FW_D2R_P	16B6 34C1
	PCIE_90D	PCIE	PCIE_FW_D2R_N	16B6 34C1
	PCIE_90D	PCIE	PCIE_FW_D2R_C_P	34C3
	PCIE_90D	PCIE	PCIE_FW_D2R_C_N	34C3
MCP_PE1_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	16C3 29C5
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	16C3 29C5
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_P	6D5 29C7
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_N	6D5 29C7
MCP_PE4_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FC_P	
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FC_N	
MCP_PEX_CLK_COMP		MCP_PEX_COMP	MCP_PEX_CLK_COMP	16A6
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_P	
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_N	
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_P<2..0>	
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_N<2..0>	
DP_ML	DP_100D	DISPLAYPORT	DP_ML_P<3..0>	69D1 70C1 70C8
	DP_100D	DISPLAYPORT	DP_ML_C_P<3..0>	70C2 70C7
DP_ML	DP_100D	DISPLAYPORT	DP_ML_N<3..0>	69D1 70C1 70C8
	DP_100D	DISPLAYPORT	DP_ML_C_N<3..0>	70C2 70C7
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_P	17B6 69C7
	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_N	17B6 69C7
	DP_100D	DISPLAYPORT	DP_AUX_CH_SW_P	69C6
	DP_100D	DISPLAYPORT	DP_AUX_CH_SW_N	69C5
	DP_100D	DISPLAYPORT	DP_AUX_CH_C_P	69C4 70C8
	DP_100D	DISPLAYPORT	DP_AUX_CH_C_N	69D4 70C8
MCP_HDMI_RSET	MCP_DV_COMP		MCP_HDMI_RSET	17A6 23C7
MCP_HDMI_VPROBE	MCP_DV_COMP		MCP_HDMI_VPROBE	17A6 23C7
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_P	17B3 68B3
	LVDS_100D	LVDS	LVDS_IG_A_CLK_F_P	6C7 68C2
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_N	17B3 68B3
	LVDS_100D	LVDS	LVDS_IG_A_CLK_F_N	6C7 68C2
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<2..0>	6C7 17B3 68C2
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<2..0>	6C7 17B3 68C2
1118 DP_ML	DP_100D	DISPLAYPORT	DP_ML_CONN_P<3..0>	70C3 70C4 70C5
1118	DP_100D	DISPLAYPORT	DP_ML_CONN_N<3..0>	70C3 70C4 70C5
MCP_IFPAB_RSET	MCP_DV_COMP		MCP_IFPAB_RSET	17A3 23C6
MCP_IFPAB_VPROBE			MCP_IFPAB_VPROBE	17A3 23C6
SATA_HDD_R2D	SATA_90D_HDD	SATA	SATA_HDD_R2D_C_P	19D6 37A2
	SATA_90D_HDD	SATA	SATA_HDD_R2D_C_N	19D6 37A2
	SATA_90D_HDD	SATA	SATA_HDD_R2D_P	6B7 37A5
	SATA_90D_HDD	SATA	SATA_HDD_R2D_N	6B7 37A5
	SATA_90D_HDD	SATA	SATA_HDD_R2D_UF_P	37A4
	SATA_90D_HDD	SATA	SATA_HDD_R2D_UF_N	37A4
SATA_HDD_D2R	SATA_90D_HDD	SATA	SATA_HDD_D2R_P	19D6 37B2
	SATA_90D_HDD	SATA	SATA_HDD_D2R_N	19D6 37B2
	SATA_90D_HDD	SATA	SATA_HDD_D2R_C_P	6B7 37B5
	SATA_90D_HDD	SATA	SATA_HDD_D2R_C_N	6B7 37B5
	SATA_90D_HDD	SATA	SATA_HDD_D2R_UF_P	37B4
	SATA_90D_HDD	SATA	SATA_HDD_D2R_UF_N	37B4
SATA_ODD_R2D	SATA_100D	SATA	SATA_ODD_R2D_C_P	19D6 37C3
	SATA_100D	SATA	SATA_ODD_R2D_C_N	19D6 37C3
	SATA_100D	SATA	SATA_ODD_R2D_P	6B7 37C6
	SATA_100D	SATA	SATA_ODD_R2D_N	6A7 6B7 37C6
	SATA_100D	SATA	SATA_ODD_R2D_UF_P	37C4
	SATA_100D	SATA	SATA_ODD_R2D_UF_N	37C4
SATA_ODD_D2R	SATA_100D	SATA	SATA_ODD_D2R_P	19D6 37C3
	SATA_100D	SATA	SATA_ODD_D2R_N	19D6 37C3
	SATA_100D	SATA	SATA_ODD_D2R_C_P	6B7 37C6
	SATA_100D	SATA	SATA_ODD_D2R_C_N	6B7 37C6
	SATA_100D	SATA	SATA_ODD_D2R_UF_P	37C4
	SATA_100D	SATA	SATA_ODD_D2R_UF_N	37C4
MCP_SATA_TERMP		SATA_TERMP	MCP_SATA_TERMP	19A6

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PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MCP_DEBUG	PCI_55S	PCI	MCP_DEBUG<7..0>	12C3 18D7
PCI_AD	PCI_55S	PCI	PCI_AD<23..8>	
PCI_AD24	PCI_55S	PCI	PCI_AD<24>	
PCI_AD	PCI_55S	PCI	PCI_AD<31..25>	
PCI_AD	PCI_55S	PCI	PCI_PAR	
PCI_C_BE_L	PCI_55S	PCI	PCI_C_BE_L<3..0>	
PCI_CNTL	PCI_55S	PCI	PCI_IRDY_L	
PCI_CNTL	PCI_55S	PCI	PCI_DEVSEL_L	
PCI_CNTL	PCI_55S	PCI	PCI_PERR_L	
PCI_CNTL	PCI_55S	PCI	PCI_SERR_L	
PCI_CNTL	PCI_55S	PCI	PCI_STOP_L	
PCI_CNTL	PCI_55S	PCI	PCI_TRDY_L	
PCI_CNTL	PCI_55S	PCI	PCI_FRAME_L	
PCI_REQ0_L	PCI_55S	PCI	PCI_REQ0_L	18D2 18D7
PCI_GNT0_L	PCI_55S	PCI	PCI_GNT0_L	
PCI_REQ1_L	PCI_55S	PCI	PCI_REQ1_L	18D2 18D7
PCI_GNT1_L	PCI_55S	PCI	PCI_GNT1_L	
PCI_INTW_L	PCI_55S	PCI	PCI_INTW_L	
PCI_INTX_L	PCI_55S	PCI	PCI_INTX_L	
PCI_INTY_L	PCI_55S	PCI	PCI_INTY_L	
PCI_INTZ_L	PCI_55S	PCI	PCI_INTZ_L	
MCP_PCI_CLK2	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP_R	18C5
	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP	18C5
LPC_AD	LPC_55S	LPC	LPC_AD<3..0>	18B3 40C8 42D3 42D5
LPC_FRAMF_L	LPC_55S	LPC	LPC_FRAME_L	18C3 40C8 42D5
LPC_RESET_L	LPC_55S	LPC	LPC_RESET_L	18C3 24D4
MCP_LPC_CLK0	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R	18B3 24B4
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC	24B1 40C8
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS	24B1 42D3
USB_EXTA	USB_90D	USB	USB_EXTA_P	19D3 38A8
	USB_90D	USB	USB_EXTA_N	19D3 38A8
	USB_90D	USB	USB_EXTA_MUXED_P	38C4
	USB_90D	USB	USB_EXTA_MUXED_N	38C4
	USB_90D	USB	CONN_USB_EXTA_P	38C3
	USB_90D	USB	CONN_USB_EXTA_N	38C3
USB_CAMERA	USB_90D	USB	USB_CAMERA_P	19D3 29B5
	USB_90D	USB	USB_CAMERA_N	19D3 29B5
	USB_90D	USB	USB_CAMERA_CONN_P	6D5 29B7
	USB_90D	USB	USB_CAMERA_CONN_N	6D5 29B7
USB_BT	USB_90D	USB	USB_BT_P	19D3 29B5
	USB_90D	USB	USB_BT_N	19C3 29B5
	USB_90D	USB	CONN_USB2_BT_P	6D5 29B7
	USB_90D	USB	CONN_USB2_BT_N	6D5 29B7
USB_TPAD	USB_90D	USB	USB_TPAD_P	19D3 48B8
	USB_90D	USB	USB_TPAD_N	19D3 48B8
	USB_90D	USB	USB_TPAD_R_P	48B7
	USB_90D	USB	USB_TPAD_R_N	48B7
USB_IR	USB_90D	USB	USB_IR_P	19D3 39D7
	USB_90D	USB	USB_IR_N	19D3 39D7
USB_EXTB	USB_90D	USB	USB_EXTB_P	19C3 38A4
	USB_90D	USB	USB_EXTB_N	19C3 38B4
	USB_90D	USB	CONN_USB_EXTB_P	38B3
	USB_90D	USB	CONN_USB_EXTB_N	38B3
USB_SD	USB_90D	USB	USB_CARDREADER_P	19C3 30C7
	USB_90D	USB	USB_CARDREADER_N	19C3 30C7
MCP_USB_RBIAS	MCP_USB_RBIAS		MCP_USB_RBIAS_GND	19C4
SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS_MCP_0_CLK	12B6 20C3 43D8
SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS_MCP_0_DATA	12B6 20C3 43D8
SMBUS_MCP_1_CLK	SMB_55S	SMB	SMBUS_MCP_1_CLK	20C3 43B8
SMBUS_MCP_1_DATA	SMB_55S	SMB	SMBUS_MCP_1_DATA	20C3 43B8
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	20D2 52C7
	HDA_55S	HDA	HDA_BIT_CLK_R	20A7 20D4
HDA_SYNC	HDA_55S	HDA	HDA_SYNC	20D2 52C7
	HDA_55S	HDA	HDA_SYNC_R	20A7 20D4
HDA_RST_L	HDA_55S	HDA	HDA_RST_R_L	20A7 20D4
	HDA_55S	HDA	HDA_RST_L	20D2 52C7
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0	20D7 52C7
	HDA_55S	HDA	HDA_SDIN_CODEC	
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT	20D2 52C7
	HDA_55S	HDA	HDA_SDOUT_R	20A7 20D4
MCP_HDA_PULLDN_COMP		MCP_HDA_COMP	MCP_HDA_PULLDN_COMP	20C7
MCP_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK_R	20B3 24B4
	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK	24B1 40C5
SPI_CLK	SPI_55S	SPI	SPI_CLK_R	20B3 42A5 42C8
	SPI_55S	SPI	SPI_CLK	51C5
	SPI_55S	SPI	SPI_ALT_CLK	42C5 42D3
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	20B3 42A5 42C7
	SPI_55S	SPI	SPI_MOSI	51C4
	SPI_55S	SPI	SPI_ALT_MOSI	42C5 42D5
SPI_MISO	SPI_55S	SPI	SPI_MISO	20B3 42A5 42B7
	SPI_55S	SPI	SPI_MISO_R	51C4
	SPI_55S	SPI	SPI_ALT_MISO	42B5 42D5
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	20B3 42B7
	SPI_55S	SPI	SPI_CS0_L	
	SPI_55S	SPI	SPI_CS1_R_L	
	SPI_55S	SPI	SPI_CS1_R_L_USE_MLB	

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MCP Constraints 2

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MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_VDD	17C6
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_GND	17C6
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0_R	17C3 32A5
	ENET_MII_55S	MCP_BUF0_CLK	RTL8211_CLK25M_CKXTAL1	31B6 32A3
ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET_INTR_L	
ENET_MDIO	ENET_MII_55S	ENET_MII	ENET_MDIO	17C3 31B6
ENET_MDC	ENET_MII_55S	ENET_MII	ENET_MDC	17D3 31B6
ENET_PWRDWN_L	ENET_MII_55S	ENET_MII	ENET_PWRDWN_L	
	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R	31C4
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK	17D6 31C1
	ENET_MII_55S	ENET_MII	ENET_RXD_R<3..0>	31C4
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RXD<0>	17D6 31C1
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<3..1>	17D6 31C1
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RX_CTRL	17D6 31B1
	ENET_MII_55S	ENET_MII	ENET_RXCTL_R	31B4
	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK_R	31C6
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK	17D3 31C8
ENET_TXD0	ENET_MII_55S	ENET_MII	ENET_TXD<0>	17D3 31C6
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<3..1>	17D3 31C6
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TX_CTRL	17D3 31B6
	ENET_MII_55S	ENET_MII	ENET_RESET_L	17C3 31B7
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_P<3..0>	31B3 33B8 33C8
	ENET_MDI_100D	ENET_MDI	ENET_MDI_N<3..0>	31B3 33B8 33C8
	ENET_MDI_100D	ENET_MDI	ENET_MDI_TRAN_P<3..0>	33B4 33C4 33C5
	ENET_MDI_100D	ENET_MDI	ENET_MDI_TRAN_N<3..0>	33B4 33C4 33C5

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Ethernet Constraints

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FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

SD CARD INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD_INTERFACE	*	=3X_DIELECTRIC	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_P	34B6 36C4
FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_N	34C6 36C4
FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_P	34B6 36C4
FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_N	34B6 36C4
FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_P	34B6 36B8
FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_N	34B6 36B8
FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_P	34B6 36B8
FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_N	34B6 36B8
Port 2 Not Used				

SD CARD NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I23 SD_DATA	SD_55S	SD_INTERFACE	SD_D<0>	30C2
I24 SD_DATA	SD_55S	SD_INTERFACE	SD_D<1>	30C2
I25 SD_DATA	SD_55S	SD_INTERFACE	SD_D<2>	30C2
I26 SD_DATA	SD_55S	SD_INTERFACE	SD_D<3>	30C2
I27 SD_DATA	SD_55S	SD_INTERFACE	SD_D<4>	30C2
I28 SD_DATA	SD_55S	SD_INTERFACE	SD_D<5>	30C2
I29 SD_DATA	SD_55S	SD_INTERFACE	SD_D<6>	30C2
I30 SD_DATA	SD_55S	SD_INTERFACE	SD_D<7>	30C2
I32 SD_CLK	SD_55S	SD_INTERFACE	SD_CLK	30C2
I31 SD_CMD	SD_55S	SD_INTERFACE	SD_CMD	30C2

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SMBUS_SMC_A_S3_SCL	SMB_555	SMB	SMBUS_SMC_A_S3_SCL	6C5 6D5 43D2
SMBUS_SMC_A_S3_SDA	SMB_555	SMB	SMBUS_SMC_A_S3_SDA	6C5 6D5 43D2
SMBUS_SMC_B_S0_SCL	SMB_555	SMB	SMBUS_SMC_B_S0_SCL	43C2
SMBUS_SMC_B_S0_SDA	SMB_555	SMB	SMBUS_SMC_B_S0_SDA	43C2
SMBUS_SMC_0_S0_SCL	SMB_555	SMB	SMBUS_SMC_0_S0_SCL	43D5
SMBUS_SMC_0_S0_SDA	SMB_555	SMB	SMBUS_SMC_0_S0_SDA	43D5
SMBUS_SMC_BSA_SCL	SMB_555	SMB	SMBUS_SMC_BSA_SCL	6A7 43C5
SMBUS_SMC_BSA_SDA	SMB_555	SMB	SMBUS_SMC_BSA_SDA	6A7 43C5
SMBUS_SMC_MGMT_SCL	SMB_555	SMB	SMBUS_SMC_MGMT_SCL	438S
SMBUS_SMC_MGMT_SDA	SMB_555	SMB	SMBUS_SMC_MGMT_SDA	438S

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P
	1TO1_DIFFPAIR		CHGR_CSI_N
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P
	1TO1_DIFFPAIR		CHGR_CSO_N

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

K24 SENSOR NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	DIFFPAIR		CHGR_CSO_R_P	45A8 59B3
	DIFFPAIR		CHGR_CSO_R_N	45A8 59B3
	DIFFPAIR		CPUTHMSNS_D2_P	46C5
	DIFFPAIR		CPUTHMSNS_D2_N	46C5
	DIFFPAIR		CPU_THERMD_P	9C6 46D5
	DIFFPAIR		CPU_THERMD_N	9C6 46D5
	DIFFPAIR		ISNS_CPUVTT_P	45B7
	DIFFPAIR		ISNS_CPUVTT_N	45B7
	DIFFPAIR		ISNS_P1V5S0MCP_P	
	DIFFPAIR		ISNS_P1V5S0MCP_N	
	DIFFPAIR		ISNS_PVCORES0MCP_P	
	DIFFPAIR		ISNS_PVCORES0MCP_N	
	DIFFPAIR		MCPTHMSNS_D2_P	6C7 46B5
	DIFFPAIR		MCPTHMSNS_D2_N	6C7 46B5
	DIFFPAIR		MCP_THMDIODE_P	20C3 46B5
	DIFFPAIR		MCP_THMDIODE_N	20C3 46B5

SYNC MASTER=M97 MLB

PAGE TITLE
K24 SPECIAL CONSTRAINTS

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

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K24 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA_P1MM	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	0.100MM	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.115 MM	0.115 MM			
50_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.100 MM			
40_OHM_SE	*	Y	0.126 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	*	Y	0.222 MM	0.222 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.151 MM	0.100 MM	=STANDARD	0.224 MM	0.224 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.100 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.095 MM	0.095 MM		0.234 MM	0.234 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.112 MM	0.112 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.075 MM	0.075 MM		0.244 MM	0.244 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.091 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	TOP,BOTTOM	0.140 MM	?
3X_DIELECTRIC	TOP,BOTTOM	0.210 MM	?
4X_DIELECTRIC	TOP,BOTTOM	0.280 MM	?
5X_DIELECTRIC	TOP,BOTTOM	0.350 MM	?
2X_DIELECTRIC	*	0.126 MM	?
3X_DIELECTRIC	*	0.189 MM	?
4X_DIELECTRIC	*	0.252 MM	?
5X_DIELECTRIC	*	0.315 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_FSB	*	BGA_P1MM	BGA_P2MM
CLK_LPC	*	BGA_P1MM	BGA_P2MM
CLK_PCI	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P2MM
CLK_SLOW	*	BGA_P1MM	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA_P1MM	BGA_P3MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_40S	BGA_P1MM	STANDARD
MEM_40S_VDD	BGA_P1MM	STANDARD

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K24 RULE DEFINITIONS

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