

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

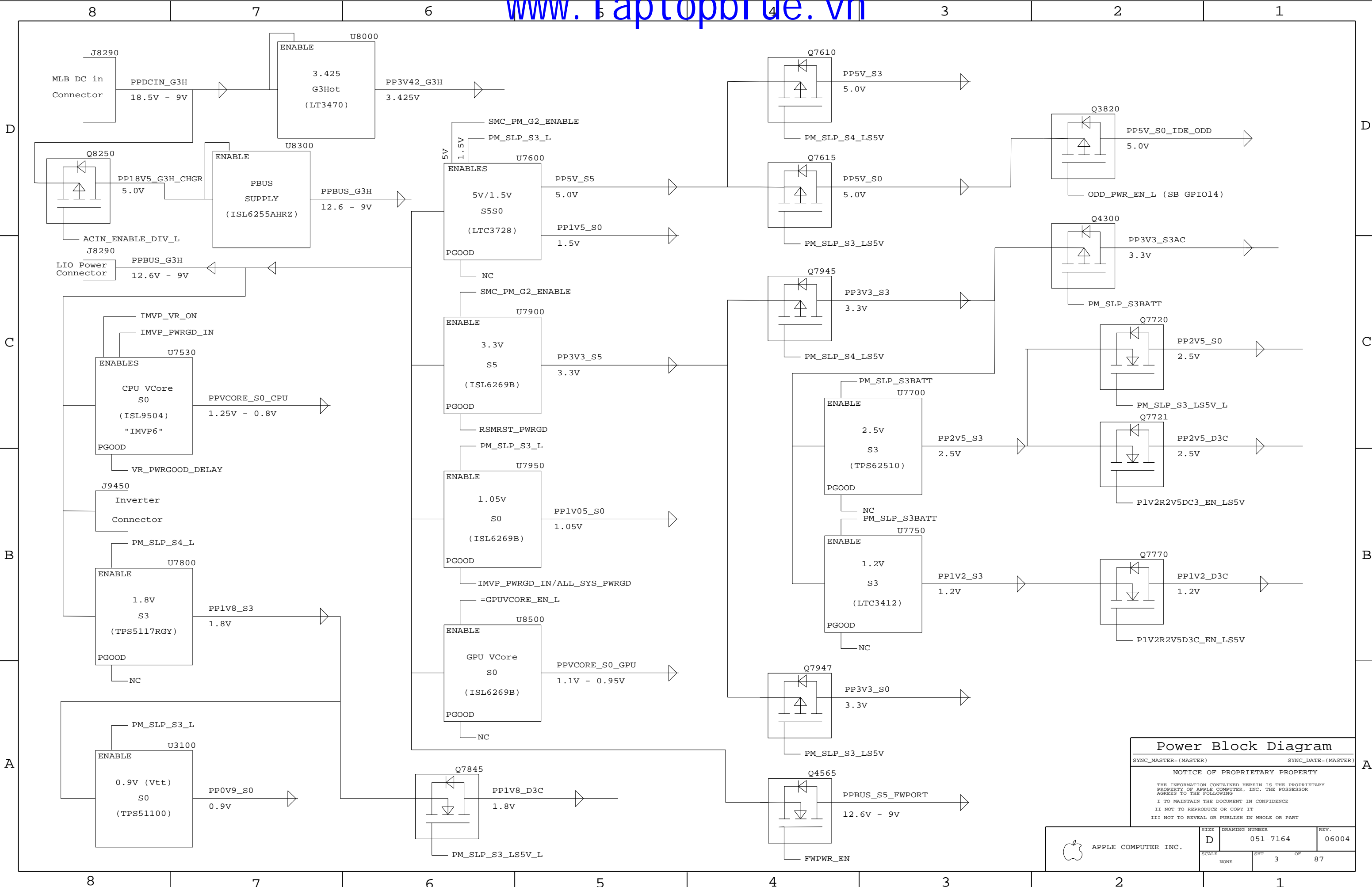
PAGE		CONTENTS	DATE
1	1	Table of Contents	N/A
2	2	System Block Diagram	(MASTER)
3	3	Power Block Diagram	(MASTER)
4	4	BOM CONFIGURATION	(MASTER)
5	5	Functional / ICT Test	(MASTER)
6	6	Signal Aliases	(MASTER)
7	7	CPU 1 OF 2-FSB	M59_MLB 09/15/2006
8	8	CPU 2 OF 2-PWR/GND	M59_MLB 09/15/2006
9	9	CPU Decoupling & VID	M59_MLB 09/15/2006
10	10	CPU MISC1-TEMP SENSOR	M59_MLB 09/15/2006
11	11	CPU ITP700FLEX DEBUG	(MASTER)
12	12	NB CPU Interface	M59_MLB 09/15/2006
13	13	NB PEG / Video Interfaces	M59_MLB 09/15/2006
14	14	NB Misc Interfaces	M59_MLB 09/15/2006
15	15	NB DDR2 Interfaces	M59_MLB 09/15/2006
16	16	NB Power 1	M59_MLB 09/15/2006
17	17	NB Power 2	M59_MLB 09/15/2006
18	18	NB Grounds	M59_MLB 09/15/2006
19	19	NB (GM) Decoupling	M57_MLB_MG 08/08/2006
20	20	NB Config Straps	M59_MLB 09/15/2006
21	21	SB: 1 OF 4	M59_MLB 09/15/2006
22	22	SB: 2 of 4	M59_MLB 09/15/2006
23	23	SB: 3 OF 4	M57_MLB_MG 08/08/2006
24	24	SB: 4 OF 4	M59_MLB 09/15/2006
25	25	SB Decoupling	M59_MLB 09/15/2006
26	26	SB Misc	(MASTER)
27	27	M57 SMBUS CONNECTIONS	(MASTER)
28	28	DDR2 SO-DIMM Connector A	M59_MLB 09/15/2006
29	29	DDR2 SO-DIMM Connector B	M59_MLB 09/15/2006
30	30	Memory Active Termination	(MASTER)
31	31	Memory Vtt Supply	M59_MLB 09/15/2006
32	32	DDR2 VRef	M59_MLB 09/15/2006
33	33	CLOCKS	M59_MLB 09/15/2006
34	34	Clock Termination	M59_MLB 09/15/2006
35	37	Mobile Clocking	M59_MLB 09/15/2006
36	38	PATA Connector	(MASTER)
37	39	FireWire Link (TSB83AA22)	M59_MLB 09/15/2006
38	40	FireWire PHY (TSB83AA22)	M59_MLB 09/15/2006
39	41	ETHERNET CONTROLLER	M59_MLB 09/15/2006
40	42	Ethernet Connector	M59_MLB 09/15/2006
41	43	Yukon Power Control	M59_MLB 09/15/2006
42	44	FW PHY Power Supply	M59_MLB 09/15/2006
43	45	FireWire Port Power	(MASTER)

ALIASES RESOLVED

DRAWING
TITLE=TRUCKEE
ABBREV=DRAWING
LAST_MODIFIED=Tue Sep 26 13:17:56 2006

A

A



Power Block Diagram

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY




THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

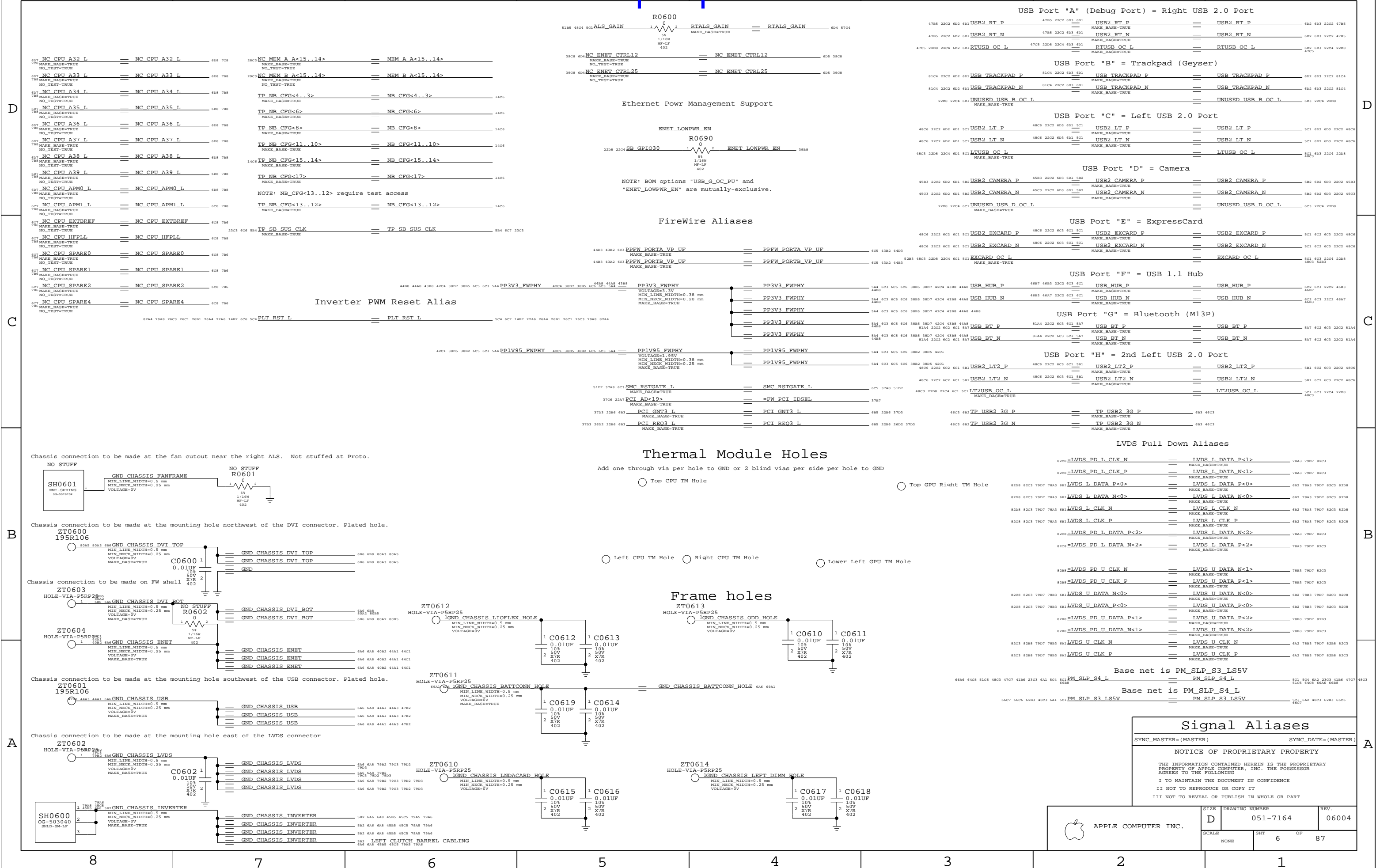
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

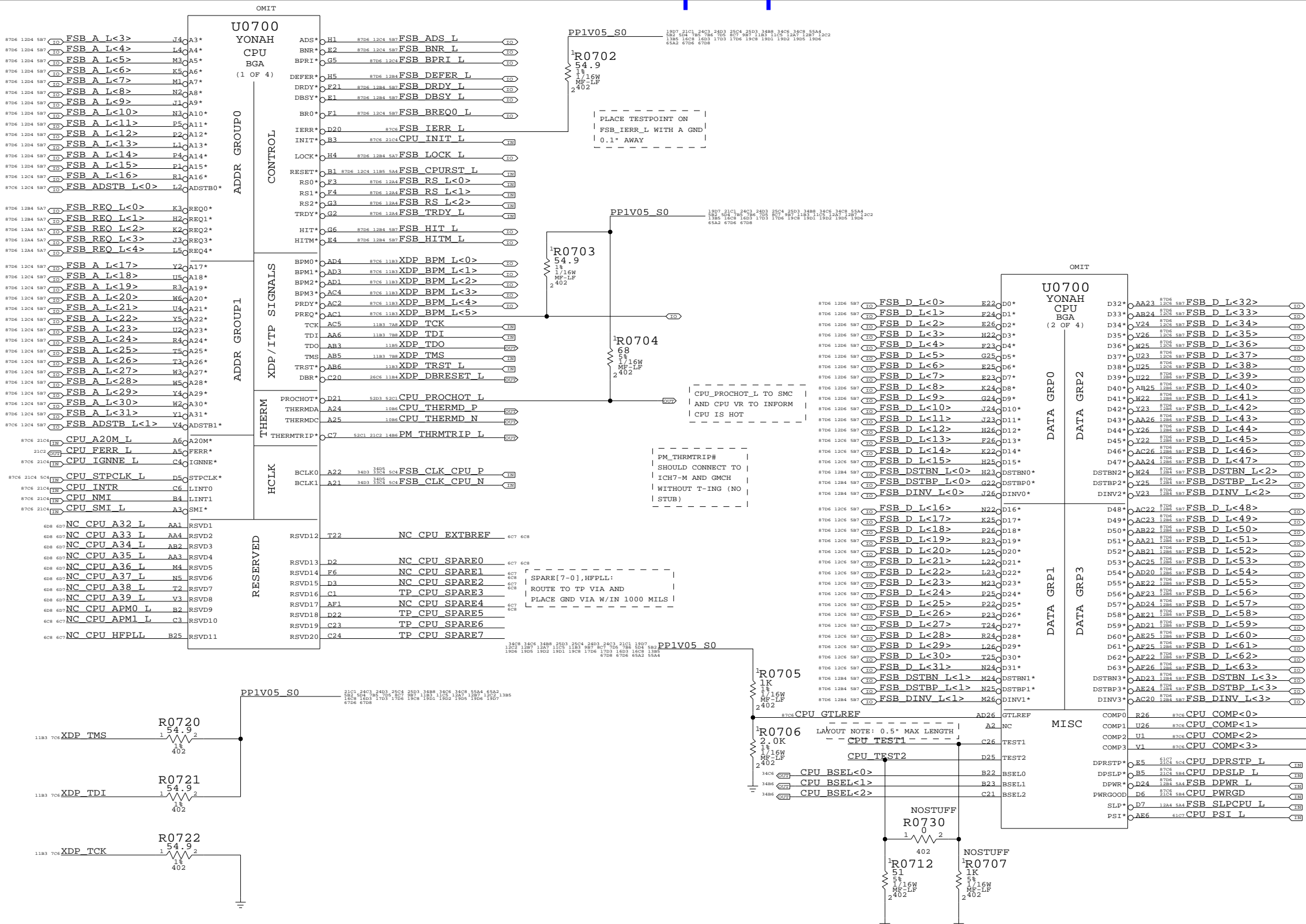
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7164	REV. 06004
	SCALE NONE	SHT 3	OF 87

D	8	7	6	www. Laptop.de.vn		3	2	1																																																																																																									
	<table><tr><th>BOM NUMBER</th><th>BOM NAME</th><th>BOM OPTIONS</th></tr><tr><td>630-7814</td><td>TRUCKEE, 2.33GHZ, B2, 256VRAM, SAM, M57</td><td>VRAM_256SAM, M57_COMMON, CPU_2_33GHZ_B2, EEE_WJK</td></tr></table>			BOM NUMBER	BOM NAME	BOM OPTIONS	630-7814	TRUCKEE, 2.33GHZ, B2, 256VRAM, SAM, M57	VRAM_256SAM, M57_COMMON, CPU_2_33GHZ_B2, EEE_WJK	<table><tr><th>PART NUMBER</th><th>QTY</th><th>DESCRIPTION</th><th>REFERENCE DES</th><th>CRITICAL</th><th>BOM OPTION</th></tr><tr><td>338S0270</td><td>1</td><td>IC, 8888053, GIGABIT ENET XCVR, 64P QFN, NO</td><td>U4101</td><td>CRITICAL</td><td></td></tr><tr><td>338S0274</td><td>1</td><td>IC, SMC, HS8 / 2116</td><td>U5800</td><td>CRITICAL</td><td>SMC_BLANK</td></tr><tr><td>341S1931</td><td>1</td><td>IC, PRGRM, SMC(NEW), M57</td><td>U5800</td><td>CRITICAL</td><td>SMC_PRGRM</td></tr><tr><td>341S1797</td><td>1</td><td>IC, EEPROM, SERIAL IIC, 8KBIT, SO8</td><td>U4102</td><td>CRITICAL</td><td></td></tr><tr><td>335S0384</td><td>1</td><td>IC, 16MBIT 8-PIN SPI SERIAL FLASH, SOIC8</td><td>U6301</td><td>CRITICAL</td><td>BOOTROM_BLANK</td></tr><tr><td>341S1924</td><td>1</td><td>IC, BOOTROM, DEVELOPMENT, UNLOCKED, M57</td><td>U6301</td><td>CRITICAL</td><td>BOOTROM_DEVEL</td></tr><tr><td>341S1925</td><td>1</td><td>IC, BOOTROM, FINAL, LOCKED, M57</td><td>U6301</td><td>CRITICAL</td><td>BOOTROM_FINAL</td></tr><tr><td>353S1461</td><td>1</td><td>IC, ISL9504, SYNC REG CTL, QFN 48</td><td>U7530</td><td>CRITICAL</td><td></td></tr><tr><td>359S0109</td><td>1</td><td>IC, LOW POWER CLOCK SYNTHESIZER, 68PIN</td><td>U3301</td><td>CRITICAL</td><td></td></tr></table>			PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	338S0270	1	IC, 8888053, GIGABIT ENET XCVR, 64P QFN, NO	U4101	CRITICAL		338S0274	1	IC, SMC, HS8 / 2116	U5800	CRITICAL	SMC_BLANK	341S1931	1	IC, PRGRM, SMC(NEW), M57	U5800	CRITICAL	SMC_PRGRM	341S1797	1	IC, EEPROM, SERIAL IIC, 8KBIT, SO8	U4102	CRITICAL		335S0384	1	IC, 16MBIT 8-PIN SPI SERIAL FLASH, SOIC8	U6301	CRITICAL	BOOTROM_BLANK	341S1924	1	IC, BOOTROM, DEVELOPMENT, UNLOCKED, M57	U6301	CRITICAL	BOOTROM_DEVEL	341S1925	1	IC, BOOTROM, FINAL, LOCKED, M57	U6301	CRITICAL	BOOTROM_FINAL	353S1461	1	IC, ISL9504, SYNC REG CTL, QFN 48	U7530	CRITICAL		359S0109	1	IC, LOW POWER CLOCK SYNTHESIZER, 68PIN	U3301	CRITICAL		<table><tr><th>PART NUMBER</th><th>QTY</th><th>DESCRIPTION</th><th>REFERENCE DES</th><th>CRITICAL</th><th>BOM OPTION</th></tr><tr><td>341S1789</td><td>1</td><td>IC, TPM, 28-PIN TSSOP</td><td>U6700</td><td>CRITICAL</td><td>TPM</td></tr></table>			PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	341S1789	1	IC, TPM, 28-PIN TSSOP	U6700	CRITICAL	TPM	<table><tr><th>PART NUMBER</th><th>QTY</th><th>DESCRIPTION</th><th>REFERENCE DES</th><th>CRITICAL</th><th>BOM OPTION</th></tr><tr><td>337S3393</td><td>1</td><td>IC, MDC, B2, FRQ, 2.33GHZ, 34W, 667M, 4M, 479 BGA</td><td>U0700</td><td>CRITICAL</td><td>CPU_2_33GHZ_B2</td></tr><tr><td>338S0269</td><td>1</td><td>IC, 945GM, NORTHBRIDGE</td><td>U1200</td><td>CRITICAL</td><td></td></tr><tr><td>343S0385</td><td>1</td><td>IC, ICH7M, BGA</td><td>U2100</td><td>CRITICAL</td><td></td></tr></table>			PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	337S3393	1	IC, MDC, B2, FRQ, 2.33GHZ, 34W, 667M, 4M, 479 BGA	U0700	CRITICAL	CPU_2_33GHZ_B2	338S0269	1	IC, 945GM, NORTHBRIDGE	U1200	CRITICAL		343S0385	1	IC, ICH7M, BGA	U2100	CRITICAL
BOM NUMBER	BOM NAME	BOM OPTIONS																																																																																																															
630-7814	TRUCKEE, 2.33GHZ, B2, 256VRAM, SAM, M57	VRAM_256SAM, M57_COMMON, CPU_2_33GHZ_B2, EEE_WJK																																																																																																															
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION																																																																																																												
338S0270	1	IC, 8888053, GIGABIT ENET XCVR, 64P QFN, NO	U4101	CRITICAL																																																																																																													
338S0274	1	IC, SMC, HS8 / 2116	U5800	CRITICAL	SMC_BLANK																																																																																																												
341S1931	1	IC, PRGRM, SMC(NEW), M57	U5800	CRITICAL	SMC_PRGRM																																																																																																												
341S1797	1	IC, EEPROM, SERIAL IIC, 8KBIT, SO8	U4102	CRITICAL																																																																																																													
335S0384	1	IC, 16MBIT 8-PIN SPI SERIAL FLASH, SOIC8	U6301	CRITICAL	BOOTROM_BLANK																																																																																																												
341S1924	1	IC, BOOTROM, DEVELOPMENT, UNLOCKED, M57	U6301	CRITICAL	BOOTROM_DEVEL																																																																																																												
341S1925	1	IC, BOOTROM, FINAL, LOCKED, M57	U6301	CRITICAL	BOOTROM_FINAL																																																																																																												
353S1461	1	IC, ISL9504, SYNC REG CTL, QFN 48	U7530	CRITICAL																																																																																																													
359S0109	1	IC, LOW POWER CLOCK SYNTHESIZER, 68PIN	U3301	CRITICAL																																																																																																													
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION																																																																																																												
341S1789	1	IC, TPM, 28-PIN TSSOP	U6700	CRITICAL	TPM																																																																																																												
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION																																																																																																												
337S3393	1	IC, MDC, B2, FRQ, 2.33GHZ, 34W, 667M, 4M, 479 BGA	U0700	CRITICAL	CPU_2_33GHZ_B2																																																																																																												
338S0269	1	IC, 945GM, NORTHBRIDGE	U1200	CRITICAL																																																																																																													
343S0385	1	IC, ICH7M, BGA	U2100	CRITICAL																																																																																																													
C	<table><tr><th>BOM GROUP</th><th>BOM OPTIONS</th></tr><tr><td>VRAM_128SAM</td><td>VRAM_128_SAMSUNG</td></tr><tr><td>VRAM_256SAM</td><td>GPU_MEM_256M, VRAM_256_SAMSUNG</td></tr></table>			BOM GROUP	BOM OPTIONS	VRAM_128SAM	VRAM_128_SAMSUNG	VRAM_256SAM	GPU_MEM_256M, VRAM_256_SAMSUNG																																																																																																								
	BOM GROUP	BOM OPTIONS																																																																																																															
VRAM_128SAM	VRAM_128_SAMSUNG																																																																																																																
VRAM_256SAM	GPU_MEM_256M, VRAM_256_SAMSUNG																																																																																																																
	<table><tr><th>BOM GROUP</th><th>BOM OPTIONS</th></tr><tr><td>M57_COMMON</td><td>ALTERNATE, COMMON, M57_COMMON1, M57_COMMON2, M57_COMMON3, M57_COMMON4, M57_DEBUG</td></tr><tr><td>M57_COMMON1</td><td>ENET_LOW_PWR_EN, ENETPWR_S3AC, GPU_BB_CTL, D3CPGOOD_3V3, ISL6255A, NO_3G</td></tr><tr><td>M57_COMMON2</td><td>KBDLED_HAS, MEMVREF_S3, MEMVTT_EN_PU, RTUSB_ESD, USB_C_OC_PU, USB_D_OC_PU, USB_E_OC_PU</td></tr><tr><td>M57_COMMON3</td><td>LVDS_PD, FW_PORT_FAULT_PU</td></tr><tr><td>M57_COMMON4</td><td>BOOTROM_DEVEL, SMC_PRGRM</td></tr><tr><td>M57_DEBUG</td><td>ITP, LPCPLUS</td></tr><tr><td>M57_TPM</td><td>TPM</td></tr></table>			BOM GROUP	BOM OPTIONS	M57_COMMON	ALTERNATE, COMMON, M57_COMMON1, M57_COMMON2, M57_COMMON3, M57_COMMON4, M57_DEBUG	M57_COMMON1	ENET_LOW_PWR_EN, ENETPWR_S3AC, GPU_BB_CTL, D3CPGOOD_3V3, ISL6255A, NO_3G	M57_COMMON2	KBDLED_HAS, MEMVREF_S3, MEMVTT_EN_PU, RTUSB_ESD, USB_C_OC_PU, USB_D_OC_PU, USB_E_OC_PU	M57_COMMON3	LVDS_PD, FW_PORT_FAULT_PU	M57_COMMON4	BOOTROM_DEVEL, SMC_PRGRM	M57_DEBUG	ITP, LPCPLUS	M57_TPM	TPM																																																																																														
	BOM GROUP	BOM OPTIONS																																																																																																															
M57_COMMON	ALTERNATE, COMMON, M57_COMMON1, M57_COMMON2, M57_COMMON3, M57_COMMON4, M57_DEBUG																																																																																																																
M57_COMMON1	ENET_LOW_PWR_EN, ENETPWR_S3AC, GPU_BB_CTL, D3CPGOOD_3V3, ISL6255A, NO_3G																																																																																																																
M57_COMMON2	KBDLED_HAS, MEMVREF_S3, MEMVTT_EN_PU, RTUSB_ESD, USB_C_OC_PU, USB_D_OC_PU, USB_E_OC_PU																																																																																																																
M57_COMMON3	LVDS_PD, FW_PORT_FAULT_PU																																																																																																																
M57_COMMON4	BOOTROM_DEVEL, SMC_PRGRM																																																																																																																
M57_DEBUG	ITP, LPCPLUS																																																																																																																
M57_TPM	TPM																																																																																																																
B	BAR CODE LABELS / EEE #'S			Extra TPM options: SMC_TPM_GPT02 SMC_TPM_GPT01 SMC_TPM_PP																																																																																																													
	<table><tr><th>PART NUMBER</th><th>QTY</th><th>DESCRIPTION</th><th>REFERENCE DES</th><th>CRITICAL</th><th>BOM OPTION</th></tr><tr><td>826-4393</td><td>1</td><td>LBL, P/N LABEL, PCB, 28MM X 6 MM</td><td>[EEE:WJK]</td><td>CRITICAL</td><td>EEE_WJK</td></tr></table>			PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:WJK]	CRITICAL	EEE_WJK																																																																																																		
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION																																																																																																												
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:WJK]	CRITICAL	EEE_WJK																																																																																																												
	MODULE PARTS																																																																																																																
	<table><tr><th>PART NUMBER</th><th>QTY</th><th>DESCRIPTION</th><th>REFERENCE DES</th><th>CRITICAL</th><th>BOM OPTION</th></tr><tr><td>338S0368</td><td>1</td><td>IC, ATI, M56P, GRAPHICSTR, 880BGA, LP</td><td>U8400</td><td>CRITICAL</td><td></td></tr><tr><td>333S0354</td><td>4</td><td>IC, SDRAM, GDDR3, 8MX32, 700MHZ, 136 FBGA</td><td>U8900, U8950, U9000, U9050</td><td>CRITICAL</td><td>VRAM_128_SAMSUNG</td></tr><tr><td>333S0350</td><td>4</td><td>IC, SDRAM, GDDR3, 16MX32, 700MHZ, 136 FBGA</td><td>U8900, U8950, U9000, U9050</td><td>CRITICAL</td><td>VRAM_256_SAMSUNG</td></tr><tr><td>333S0358</td><td>4</td><td>IC, SDRAM, GDDR3, 8MX32, 700MHZ, 136 FBGA</td><td>U8900, U8950, U9000, U9050</td><td>CRITICAL</td><td>VRAM_128_HYNIX</td></tr><tr><td>333S0351</td><td>4</td><td>IC, SDRAM, GDDR3, 16MX32, 700MHZ, 136 FBGA</td><td>U8900, U8950, U9000, U9050</td><td>CRITICAL</td><td>VRAM_256_HYNIX</td></tr><tr><td>333S0376</td><td>4</td><td>IC, SDRAM, GDDR3, 8MX32, 700MHZ, 136 FBGA</td><td>U8900, U8950, U9000, U9050</td><td>CRITICAL</td><td>VRAM_128_INFINEON</td></tr><tr><td>333S0377</td><td>4</td><td>IC, SDRAM, GDDR3, 16MX32, 600MHZ, 136 FBGA</td><td>U8900, U8950, U9000, U9050</td><td>CRITICAL</td><td>VRAM_256_INFINEON</td></tr></table>			PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	338S0368	1	IC, ATI, M56P, GRAPHICSTR, 880BGA, LP	U8400	CRITICAL		333S0354	4	IC, SDRAM, GDDR3, 8MX32, 700MHZ, 136 FBGA	U8900, U8950, U9000, U9050	CRITICAL	VRAM_128_SAMSUNG	333S0350	4	IC, SDRAM, GDDR3, 16MX32, 700MHZ, 136 FBGA	U8900, U8950, U9000, U9050	CRITICAL	VRAM_256_SAMSUNG	333S0358	4	IC, SDRAM, GDDR3, 8MX32, 700MHZ, 136 FBGA	U8900, U8950, U9000, U9050	CRITICAL	VRAM_128_HYNIX	333S0351	4	IC, SDRAM, GDDR3, 16MX32, 700MHZ, 136 FBGA	U8900, U8950, U9000, U9050	CRITICAL	VRAM_256_HYNIX	333S0376	4	IC, SDRAM, GDDR3, 8MX32, 700MHZ, 136 FBGA	U8900, U8950, U9000, U9050	CRITICAL	VRAM_128_INFINEON	333S0377	4	IC, SDRAM, GDDR3, 16MX32, 600MHZ, 136 FBGA	U8900, U8950, U9000, U9050	CRITICAL	VRAM_256_INFINEON																																																														
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION																																																																																																												
338S0368	1	IC, ATI, M56P, GRAPHICSTR, 880BGA, LP	U8400	CRITICAL																																																																																																													
333S0354	4	IC, SDRAM, GDDR3, 8MX32, 700MHZ, 136 FBGA	U8900, U8950, U9000, U9050	CRITICAL	VRAM_128_SAMSUNG																																																																																																												
333S0350	4	IC, SDRAM, GDDR3, 16MX32, 700MHZ, 136 FBGA	U8900, U8950, U9000, U9050	CRITICAL	VRAM_256_SAMSUNG																																																																																																												
333S0358	4	IC, SDRAM, GDDR3, 8MX32, 700MHZ, 136 FBGA	U8900, U8950, U9000, U9050	CRITICAL	VRAM_128_HYNIX																																																																																																												
333S0351	4	IC, SDRAM, GDDR3, 16MX32, 700MHZ, 136 FBGA	U8900, U8950, U9000, U9050	CRITICAL	VRAM_256_HYNIX																																																																																																												
333S0376	4	IC, SDRAM, GDDR3, 8MX32, 700MHZ, 136 FBGA	U8900, U8950, U9000, U9050	CRITICAL	VRAM_128_INFINEON																																																																																																												
333S0377	4	IC, SDRAM, GDDR3, 16MX32, 600MHZ, 136 FBGA	U8900, U8950, U9000, U9050	CRITICAL	VRAM_256_INFINEON																																																																																																												
A	ALTERNATE PARTS																																																																																																																
	<table><tr><th>PART NUMBER</th><th>IS ALTERNATE FOR PART NUMBER</th><th>BOM OPTION</th><th>REF DES</th><th>COMMENTS:</th></tr><tr><td>376S0448</td><td>376S0445</td><td></td><td>ALL</td><td>SI7806ADN for F0M6296</td></tr><tr><td>128S0083</td><td>128S0073</td><td></td><td>C2516</td><td>1.86 MAX ALT TO 1.9 MAX</td></tr><tr><td>128S0093</td><td>128S0092</td><td></td><td>ALL</td><td>KEMET IS ALT TO SANYO</td></tr><tr><td>353S1465</td><td>353S1461</td><td></td><td>ALL</td><td>Screened ISL6262 for ISL9504</td></tr><tr><td>152S0287</td><td>152S0435</td><td></td><td>ALL</td><td>Alternates for Collicraft M85131</td></tr></table>			PART NUMBER	IS ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	376S0448	376S0445		ALL	SI7806ADN for F0M6296	128S0083	128S0073		C2516	1.86 MAX ALT TO 1.9 MAX	128S0093	128S0092		ALL	KEMET IS ALT TO SANYO	353S1465	353S1461		ALL	Screened ISL6262 for ISL9504	152S0287	152S0435		ALL	Alternates for Collicraft M85131																																																																																
PART NUMBER	IS ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:																																																																																																													
376S0448	376S0445		ALL	SI7806ADN for F0M6296																																																																																																													
128S0083	128S0073		C2516	1.86 MAX ALT TO 1.9 MAX																																																																																																													
128S0093	128S0092		ALL	KEMET IS ALT TO SANYO																																																																																																													
353S1465	353S1461		ALL	Screened ISL6262 for ISL9504																																																																																																													
152S0287	152S0435		ALL	Alternates for Collicraft M85131																																																																																																													
						<table><tr><th colspan="3">BOM CONFIGURATION</th></tr><tr><td colspan="2">SYNC_MASTER=(MASTER)</td><td>SYNC_DATE=(MASTER)</td></tr><tr><td colspan="3">NOTICE OF PROPRIETARY PROPERTY</td></tr><tr><td colspan="3">THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING</td></tr><tr><td colspan="3">I TO MAINTAIN THE DOCUMENT IN CONFIDENCE</td></tr><tr><td colspan="3">II NOT TO REPRODUCE OR COPY IT</td></tr><tr><td colspan="3">III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART</td></tr></table>			BOM CONFIGURATION			SYNC_MASTER=(MASTER)		SYNC_DATE=(MASTER)	NOTICE OF PROPRIETARY PROPERTY			THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING			I TO MAINTAIN THE DOCUMENT IN CONFIDENCE			II NOT TO REPRODUCE OR COPY IT			III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART																																																																																						
BOM CONFIGURATION																																																																																																																	
SYNC_MASTER=(MASTER)		SYNC_DATE=(MASTER)																																																																																																															
NOTICE OF PROPRIETARY PROPERTY																																																																																																																	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING																																																																																																																	
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE																																																																																																																	
II NOT TO REPRODUCE OR COPY IT																																																																																																																	
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART																																																																																																																	
						<table><tr><td rowspan="2"> APPLE COMPUTER INC.</td><td>SIZE D</td><td>DRAWING NUMBER 051-7164</td><td>REV. 06004</td></tr><tr><td>SCALE NONE</td><td>SHT 4</td><td>OF 87</td></tr></table>			 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7164	REV. 06004	SCALE NONE	SHT 4	OF 87																																																																																																		
 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7164	REV. 06004																																																																																																														
	SCALE NONE	SHT 4	OF 87																																																																																																														
8	7	6	5	4	3	2	1																																																																																																										





CHANGE THE PULLS RESISTOR VALUE PER NAPA PLATFORM DG REV 0.9

WE THROUGH THE ITP700FLEX CONNECTOR CONNECT TO PDB XDP BUFFER BOARD--ECM*50
SO THE TDI PULL UP THROUGH 54.9 OHM,TMS PULL UP THROUGH 54.9 OHM
TCK PULL DOWN THROUGH 54.9 OHM(FOLLOW UP XDP DESIGN REFERENCE)

CPU 1 OF 2-FSB

SYNC_MASTER=M59_MLB

SYNC_DATE=09/15/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE D

DRAWING NUMBER 051-7164

REV. 06004

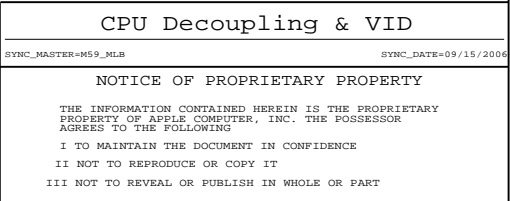
SCALE NONE

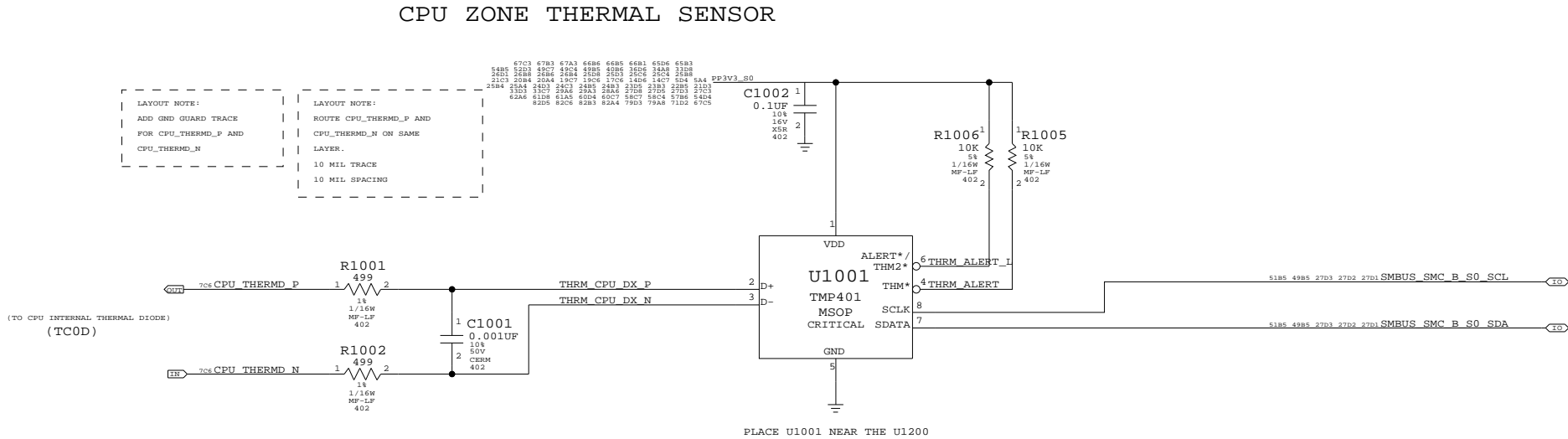
SHT 7 OF 87

C



A

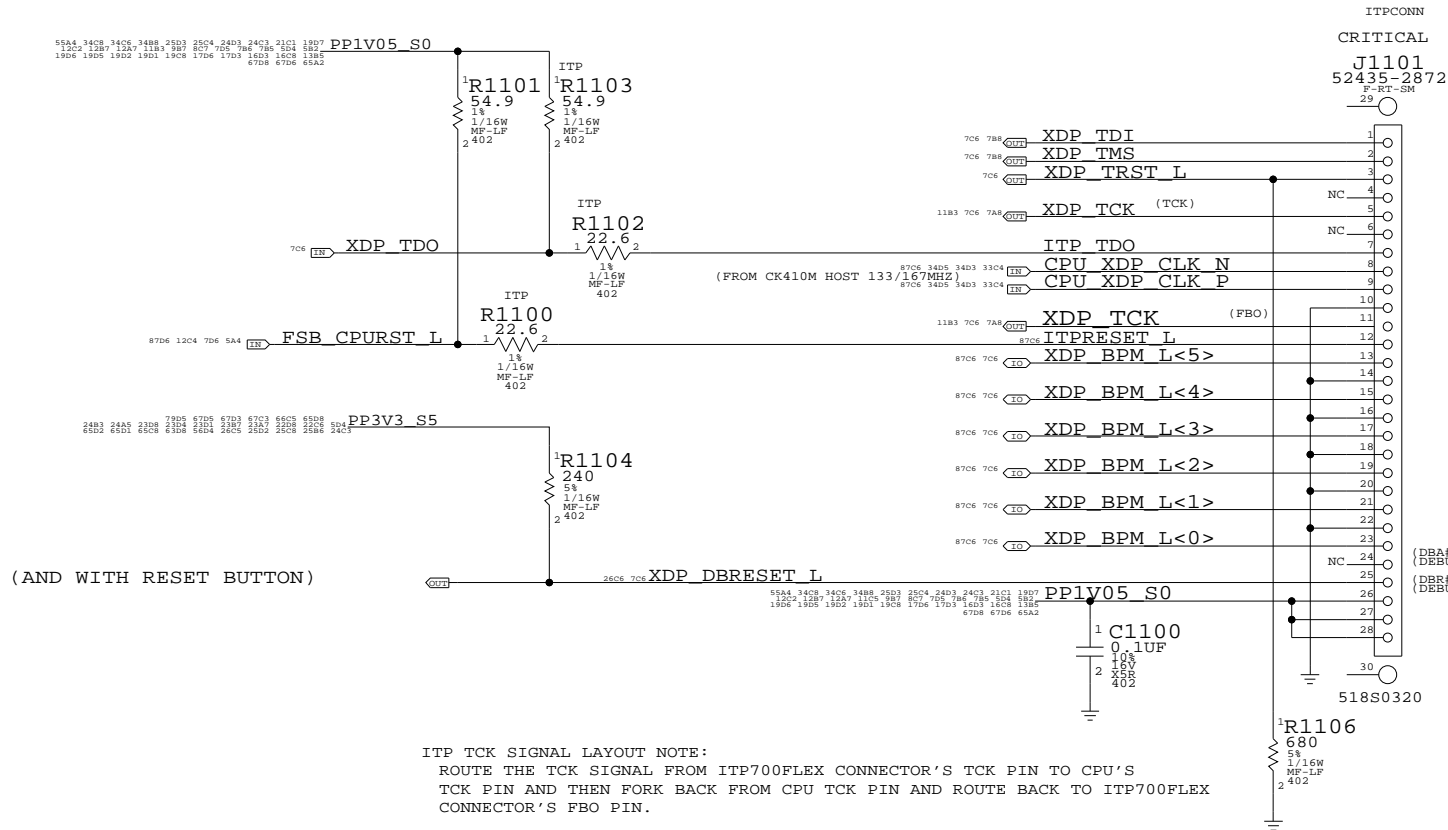




CPU MISC1-TEMP SENSOR		
SYNC_MASTER=M59_MLB		SYNC_DATE=09/15/2006
NOTICE OF PROPRIETARY PROPERTY		
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING		
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE		
II NOT TO REPRODUCE OR COPY IT		
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART		

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7164	REV. 06004
	SCALE NONE	SHT 10 OF 87	

CPU ITP700FLEX DEBUG SUPPORT



CPU ITP700FLEX DEBUG

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

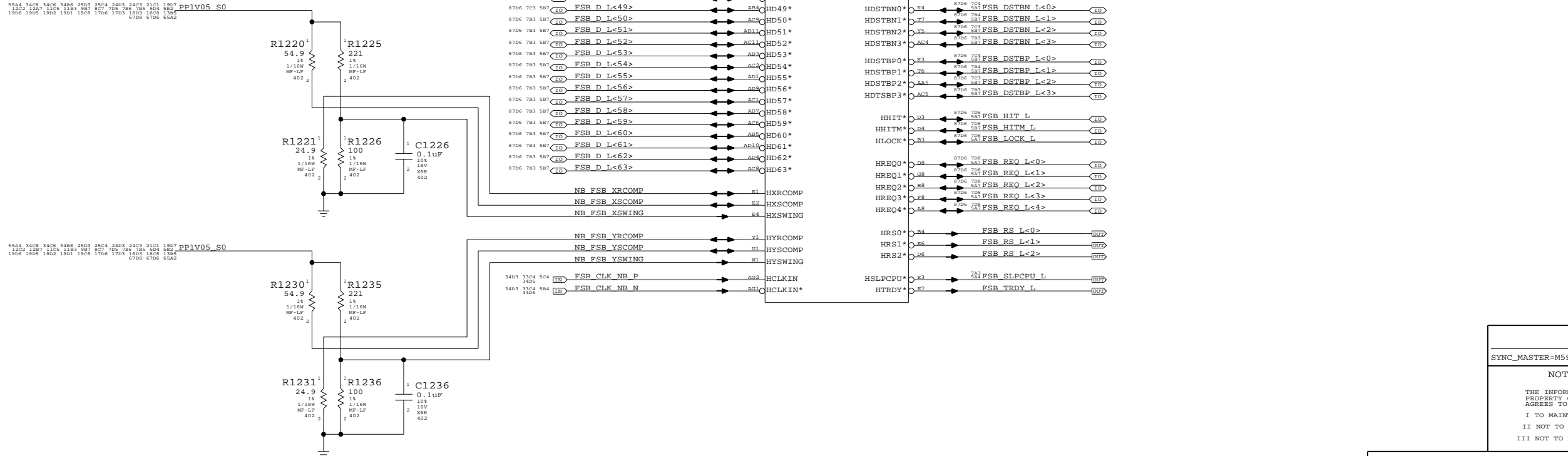
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7164	06004
SCALE		SHT	OF
NONE		11	87



```


NB CPU Interface
-----
SYNC_MASTER=M59_MLB                               SYNC_DATE=09/15/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY
PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR
AGREES TO THE FOLLOWING


I 1 TO MAINTAIN THE DOCUMENT IN CONFIDENCE
I 1 NOT TO REPRODUCE OR COPY IT
I 11 NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

```

 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7164	REV. 06004
	SCALE NONE	SHT 12 OF 87	





 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7164	06004
	SCALE NONE	SHT 14	OF 87

D

C

B

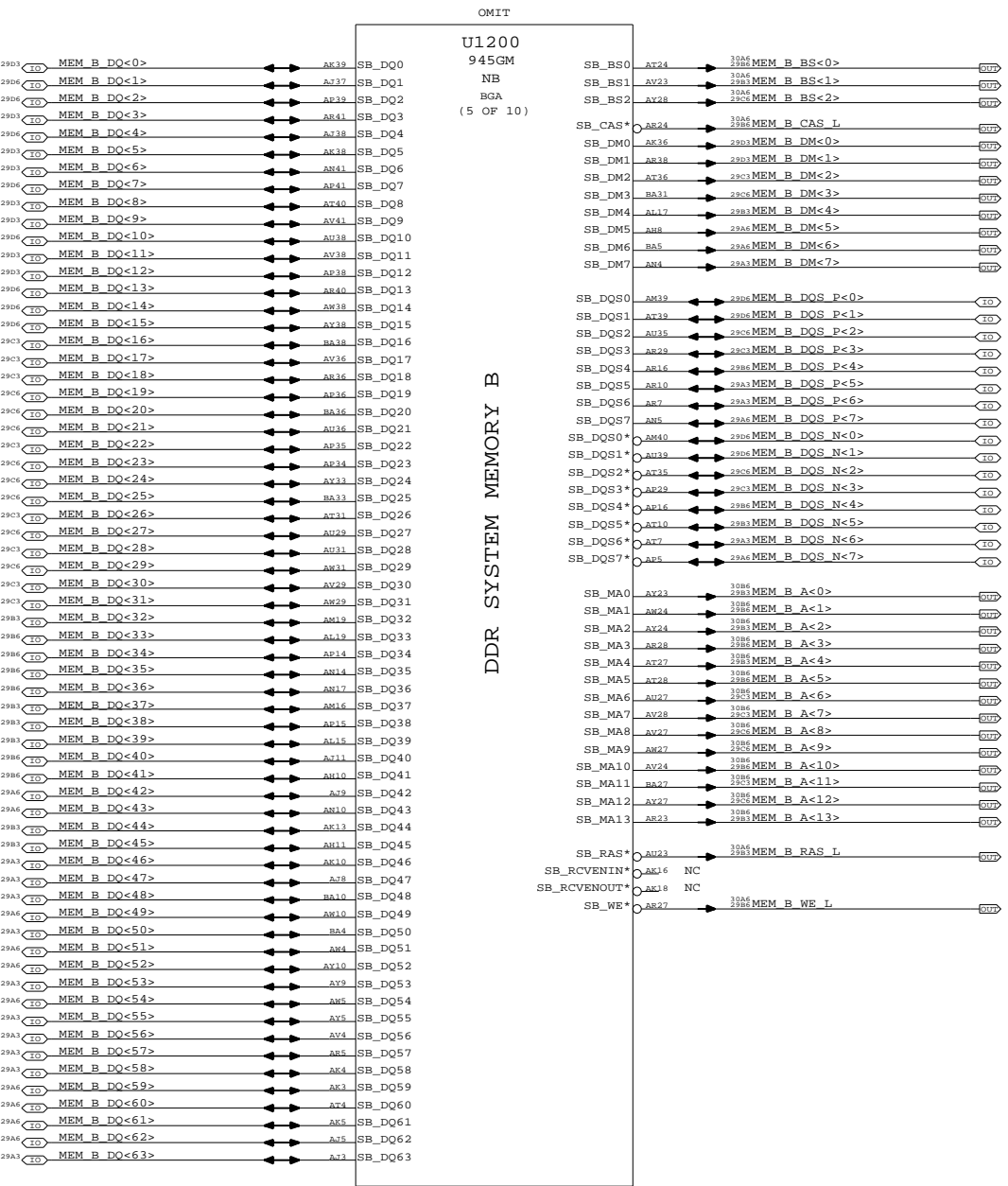
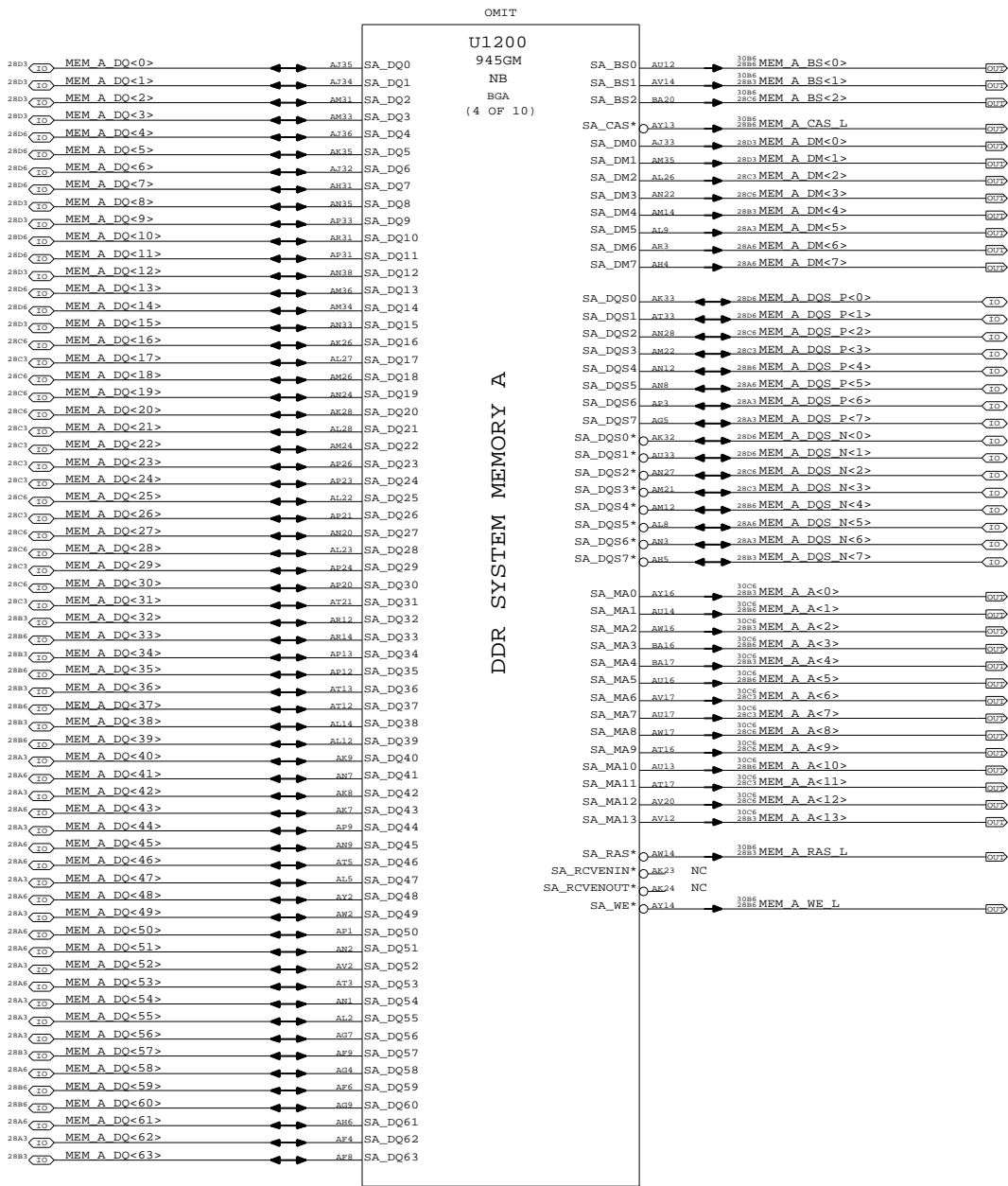
A

D

C

B

A



NB DDR2 Interfaces

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

D

C

B

A

D

C

B

A

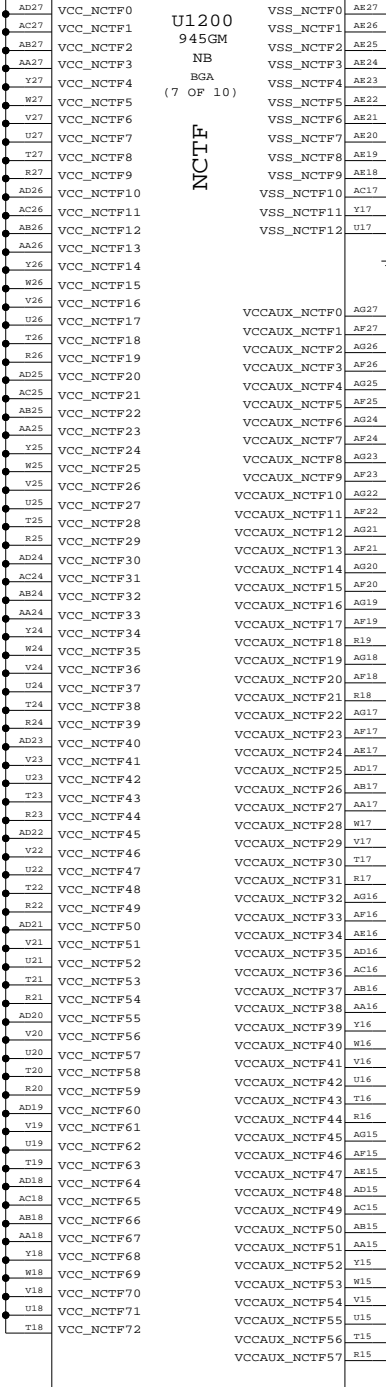
NCTF balls are Not Critical To Function

These connections can break without
impacting part performance.

OMIT

5544 3406 2406 7488 2503 2504 2403 2403 2101 1807
1287 1287 1106 1106 1189 987 807 700 700 700 700
1826 1803 1803 1803 1803 1803 1700 1700 6708 6708 6542

PP1V05_S0



6247 6786
1802 1805
1802 1814
1804 1309
1802 1386
1826 1803
1804 1807
6708 6708

PP1V5_S0 NB

1.05V, Internal Graphics: 3500mA Max

1.05V, External Graphics: 1500mA Max

1.5V, Internal Graphics: 5500mA Max

PP1V05_S0

1.05V or 1.5V

VCC_0 AA33

VCC_1 W33

VCC_2 P33

VCC_3 N33

VCC_4 L33

VCC_5 J33

VCC_6 AA32

VCC_7 Y32

VCC_8 W32

VCC_9 V32

VCC_10 P32

VCC_11 N32

VCC_12 M32

VCC_13 L32

VCC_14 J32

VCC_15 AA31

VCC_16 W31

VCC_17 Y31

VCC_18 W31

VCC_19 P31

VCC_20 N31

VCC_21 M31

VCC_22 L31

VCC_23 AA30

VCC_24 Y30

VCC_25 W30

VCC_26 V30

VCC_27 P30

VCC_28 N30

VCC_29 M30

VCC_30 L30

VCC_31 AA29

VCC_32 Y29

VCC_33 W29

VCC_34 V29

Speed

1 Channel 2 Channel

400MTs 1300mA 2400mA

533MTs 1500mA 2800mA

667MTs 1700mA 3200mA

1.8V Max Current

PP1V8_S3

C1615

0.47UF

104

6.3V

CE8M-XSR

402

Layout Note:

Place near pin BA23

C1620

10uF

204

6.3V

CE8M-XSR

603

Layout Note:

Place in cavity

C1610

0.47UF

104

6.3V

CE8M-XSR

402

Layout Note:

Place near pin BA15

C1612

0.47UF

104

6.3V

CE8M-XSR

402

Layout Note:

Place near pin BA15

NB_VCCSM_LF2

NB_VCCSM_LF1

NB Power 1

SYNC_MASTER=M59_MLB

SYNC_DATE=09/15/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY
PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR
AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE COMPUTER INC.

SIZE

DRAWING NUMBER

REV.

D

051-7164

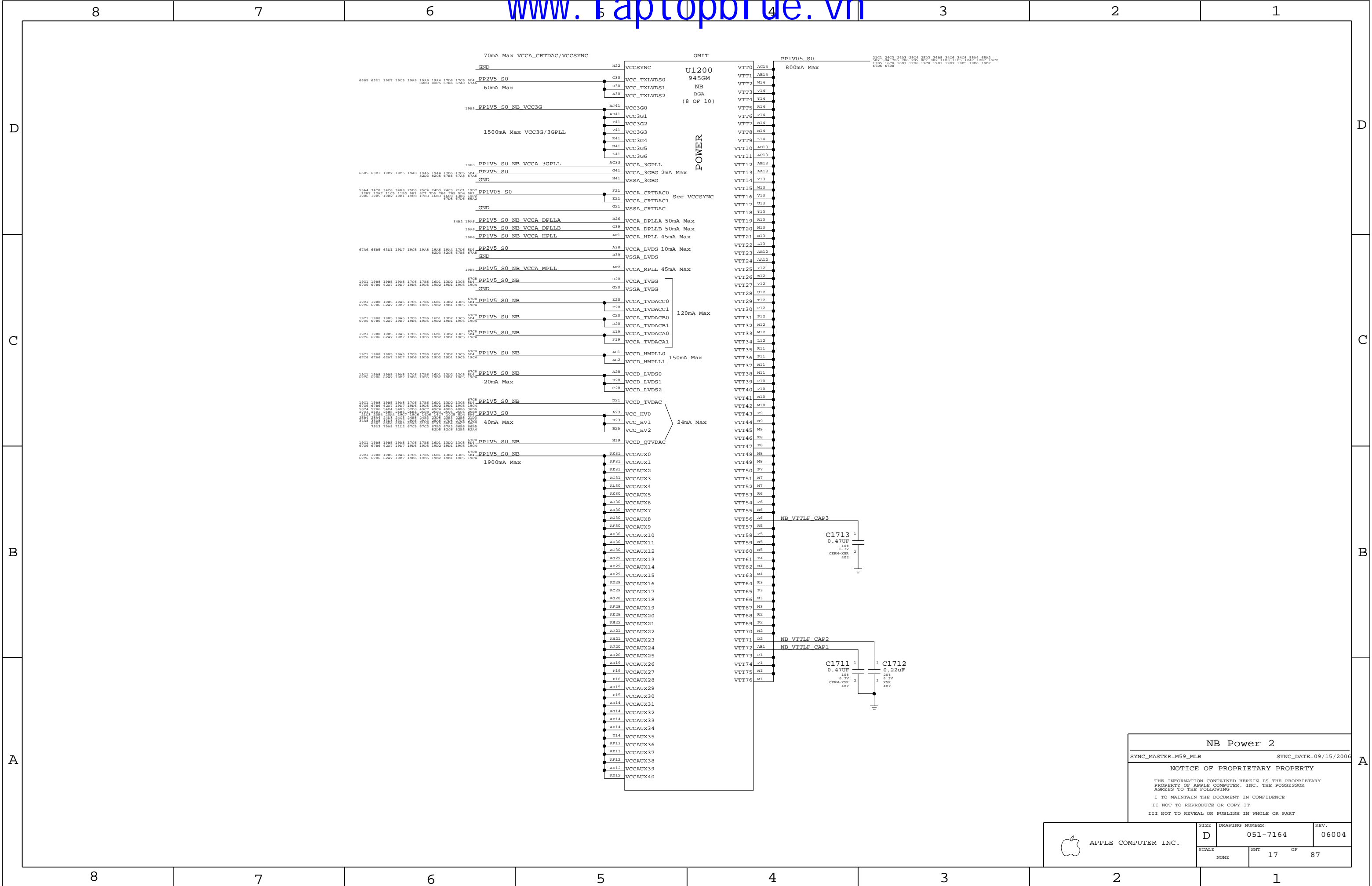
06004

SCALE

SHT

OF

87



NB Power 2

SYNC_MASTER=M59_MLB

SYNC_DATE=09/15/2006


NOTICE OF PROPRIETARY PROPERTY

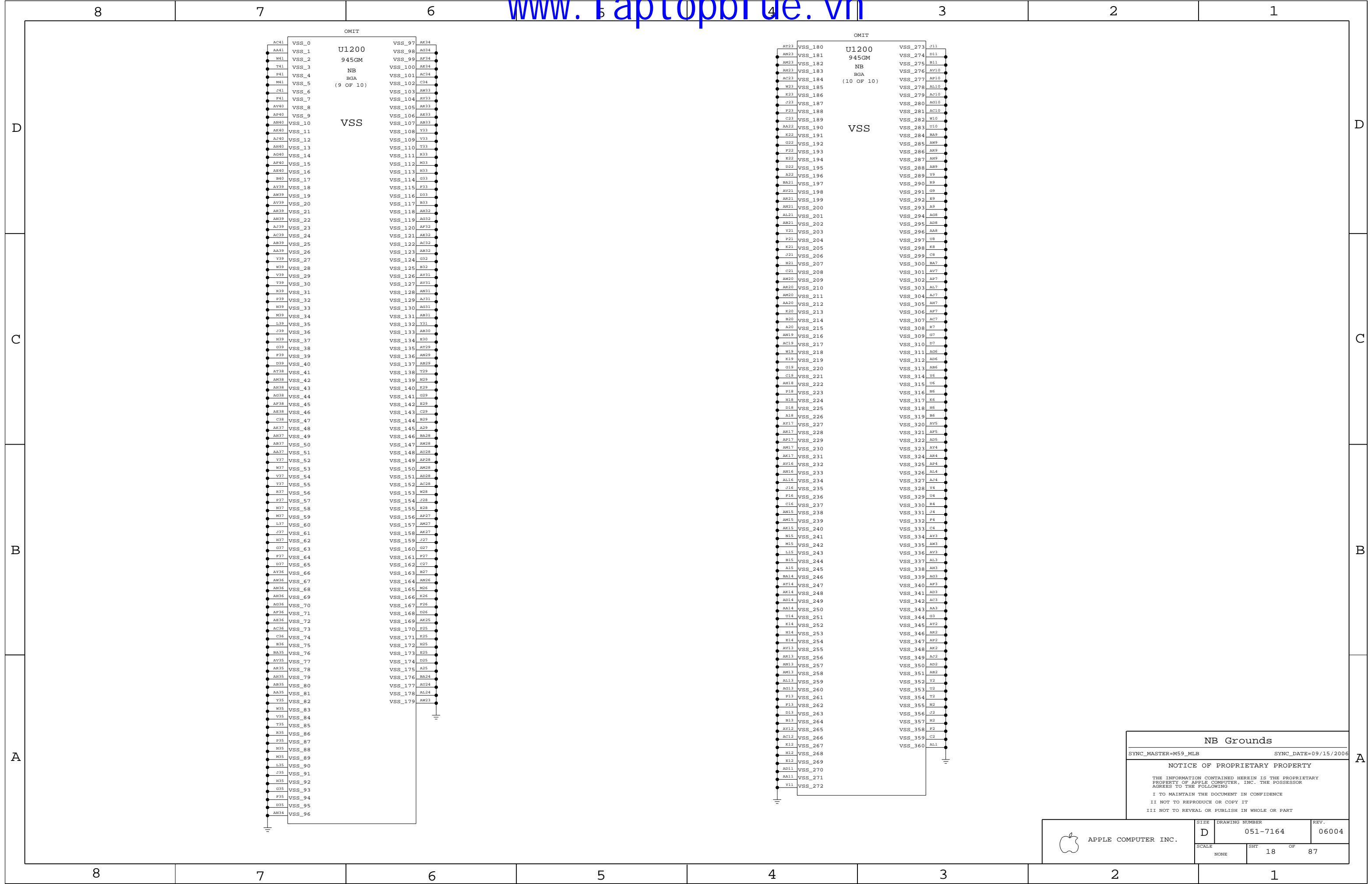
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7164	06004
SCALE		SHT	OF
NONE		17	87



D

C

B

A

D

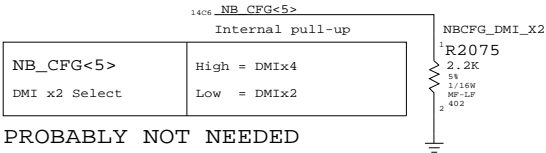
C

B

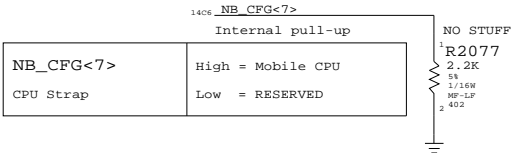
A

NB_CFG<3>	RESERVED
-----------	----------

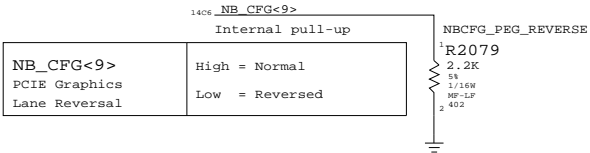
NB_CFG<4>	RESERVED
-----------	----------



NB_CFG<6>	RESERVED
-----------	----------



NB_CFG<8>	RESERVED
-----------	----------



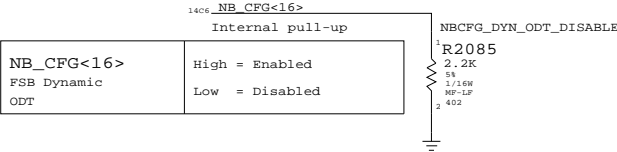
NB_CFG<10>	RESERVED
------------	----------

NB_CFG<11>	RESERVED
------------	----------

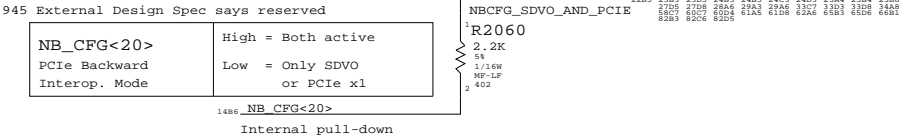
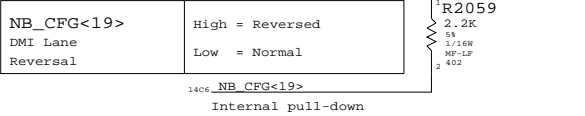
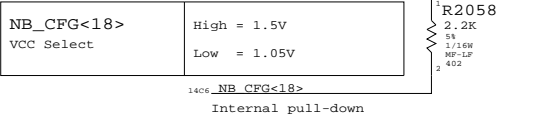
Internal pull-ups	
NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation

NB_CFG<14>	RESERVED
------------	----------

NB_CFG<15>	RESERVED
------------	----------




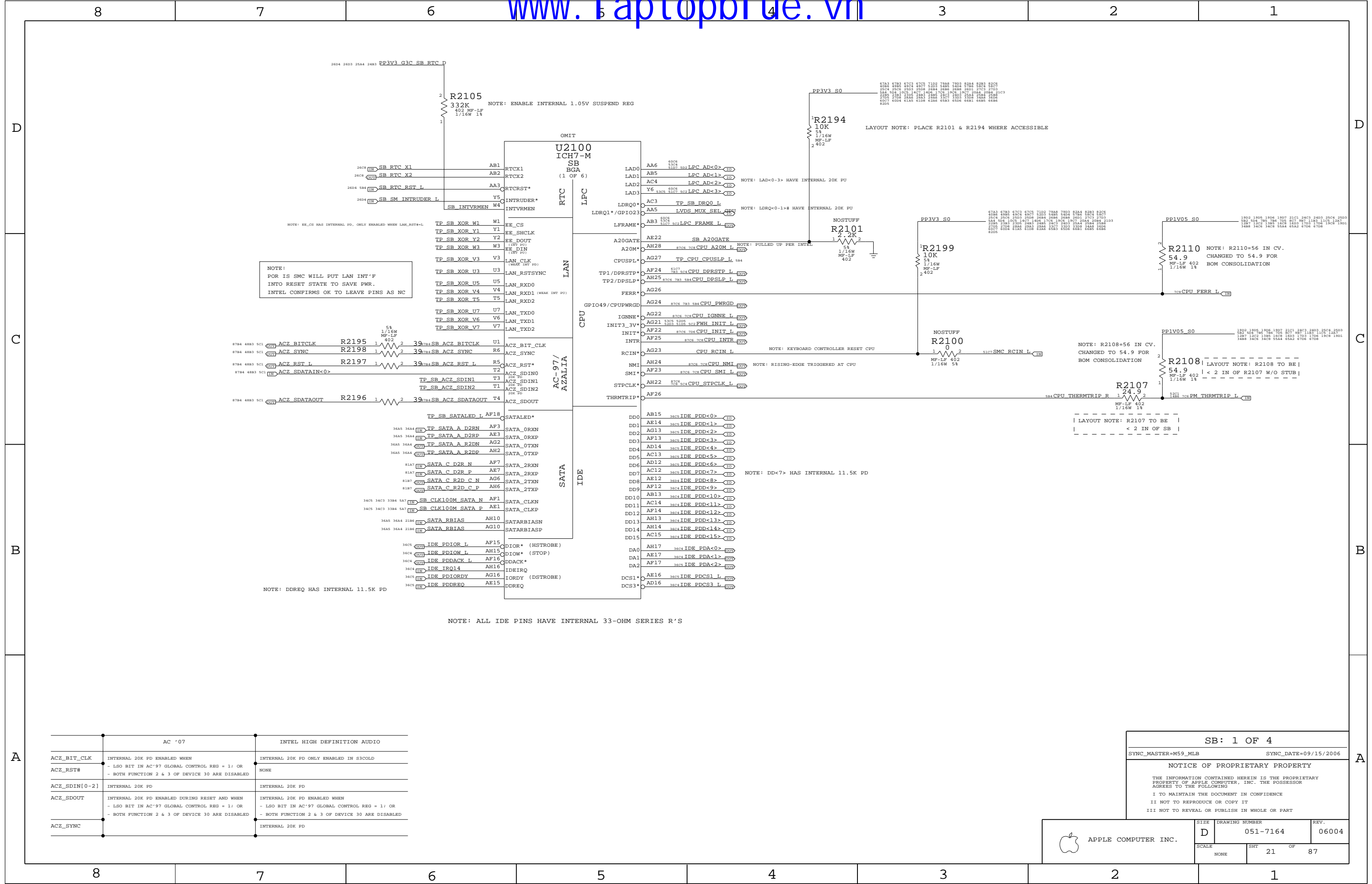
NB_CFG<17>	RESERVED
------------	----------



PROBABLY NOT NEEDED

NB Config Straps	
SYNC_MASTER=M59_MLB	SYNC_DATE=09/15/2006
NOTICE OF PROPRIETARY PROPERTY	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING	
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE	
II NOT TO REPRODUCE OR COPY IT	
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART	

 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7164	REV. 06004
	SCALE NONE	SHT 20	OF 87



SB: 1 OF 4

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

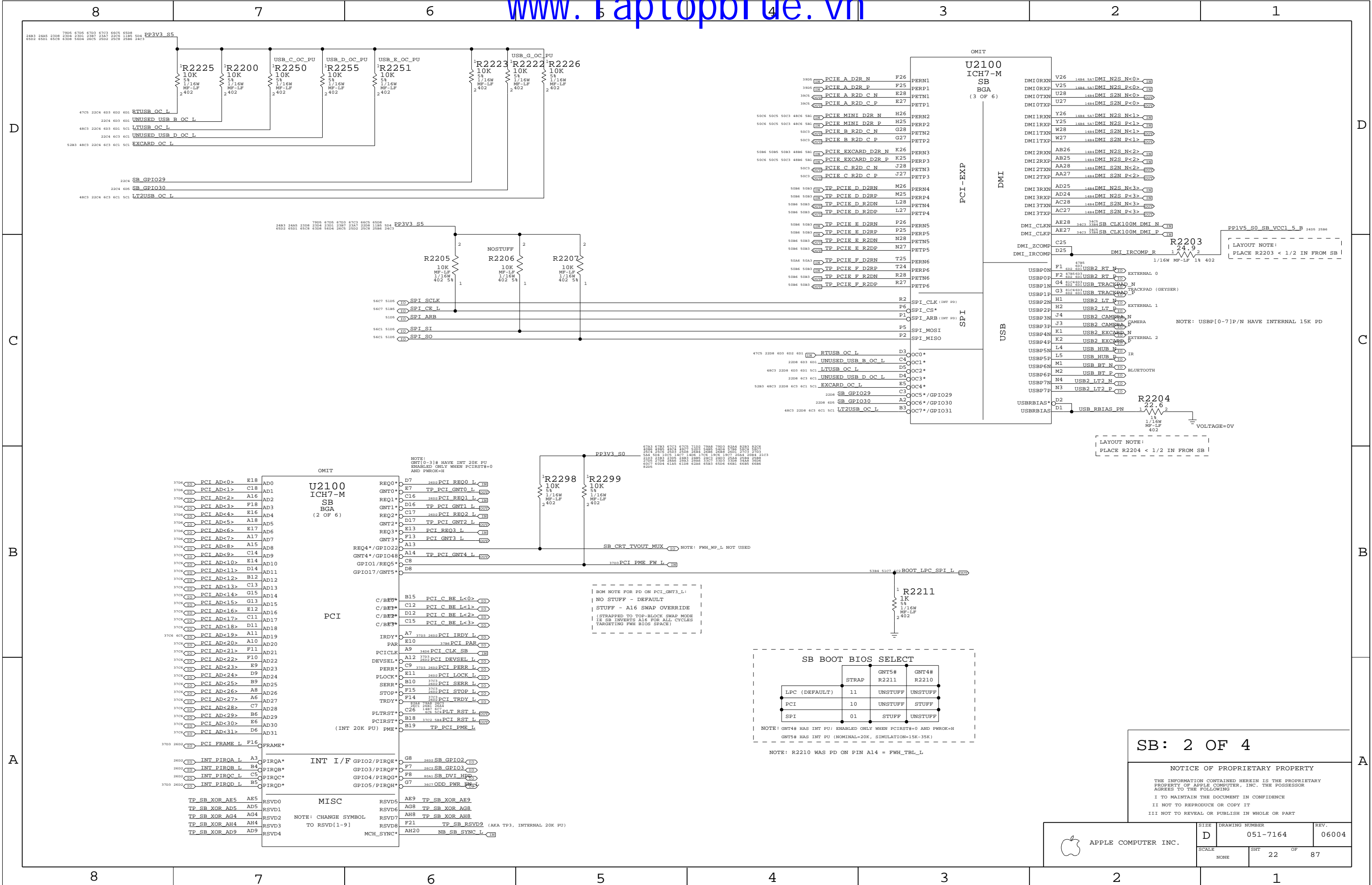
NOTICE OF PROPRIETARY PROPERTY

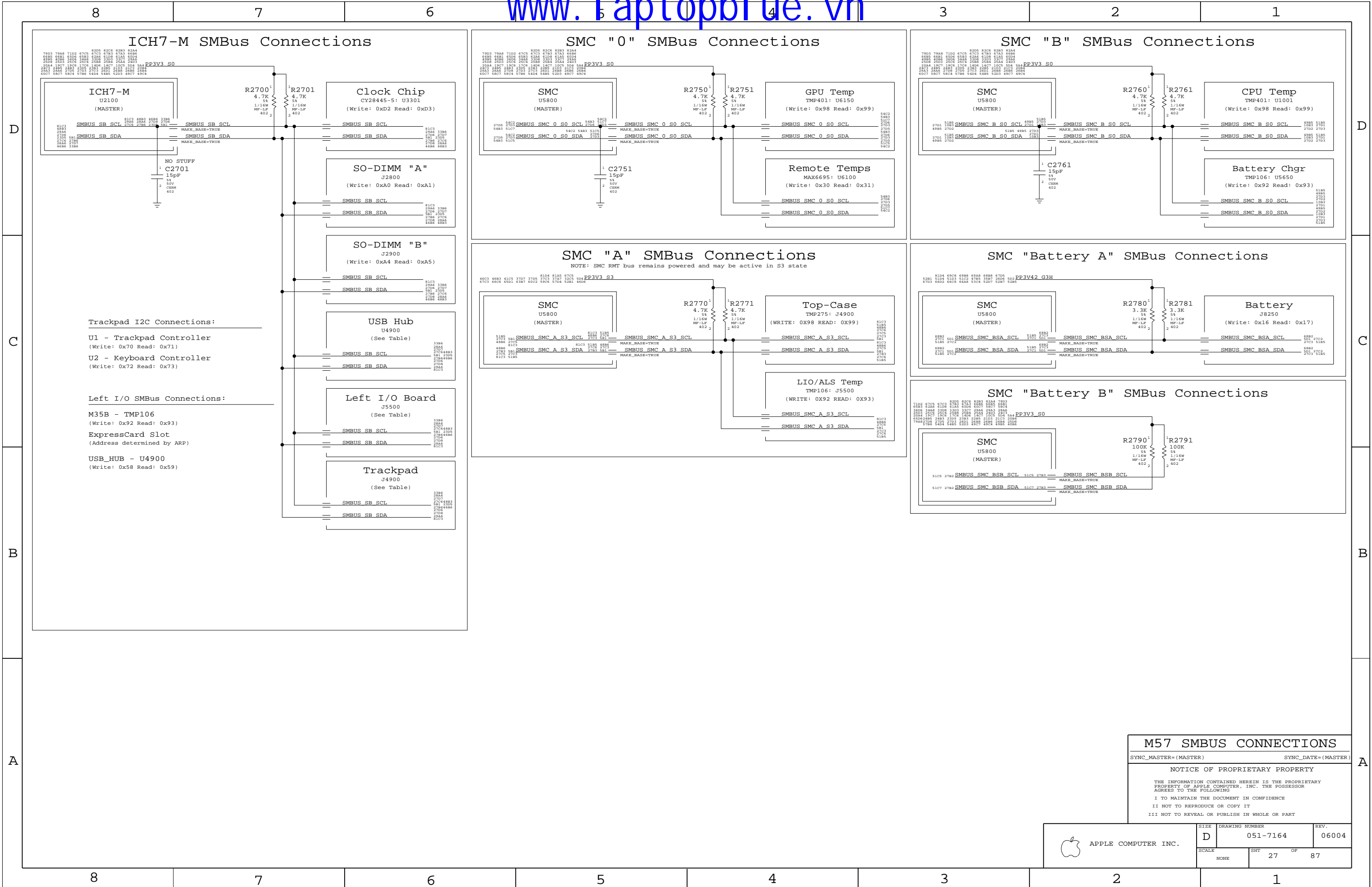
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART





M57 SMBUS CONNECTIONS

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE COMPUTER INC.

SIZE

DRAWING NUMBER

REV.

D

051-7164

06004

SCALE

SHT

OF

87

D

```
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)
```

```
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA
```

(NONE)

C


B

A



(For return current)



 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7164	06004
	SCALE	SHT	OF
	NONE	28	87



APPLE COMPUTER INC.

SIZE D	DRAWING NUMBER 051-7164	REV. 06004
SCALE NONE	SHT 28	OF 87

Power aliases required by this page:

- =PPIV8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:

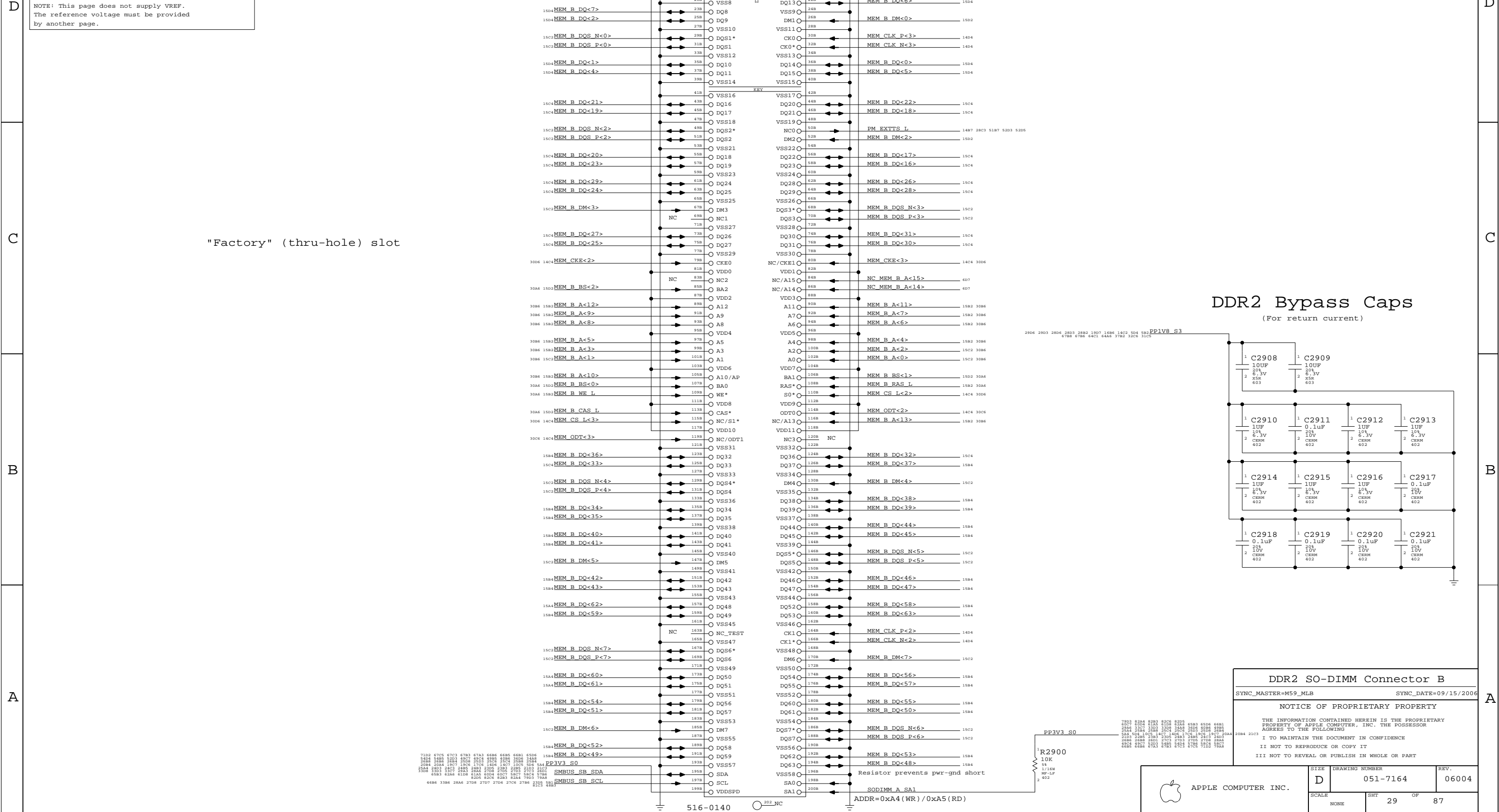
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:

(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.

NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.




20D6 29D3 28D6 28D3 28B2 19D7 16B6 14C7 5D4 5B2
67B8 67B6 64C1 64A8 37B2 32C6 31C5

PP1V8_S3

The schematic diagram illustrates the PP1V8_S3 power supply circuit. It features a multi-stage voltage regulation architecture. The input is connected to a network of capacitors (C2908, C2909, C2910, C2911, C2912, C2913, C2914, C2915, C2916, C2917, C2918, C2919, C2920, C2921) and resistors (R2908, R2909, R2910, R2911, R2912, R2913, R2914, R2915, R2916, R2917, R2918, R2919, R2920, R2921). The output is taken from the positive rail after the final stage of regulation. The circuit is designed to provide a stable 1.8V output from a 5V input.

DDR2 SO-DIMM Connector B	
SYNC_MASTER=M59_MLB	SYNC_DATE=09/15/2006
NOTICE OF PROPRIETARY PROPERTY	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING	
2084 21C1	I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
	II NOT TO REPRODUCE OR COPY IT
	III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7164		REV. 06004
	SCALE NONE		SHT 29 OF 87	

D

C

B

A

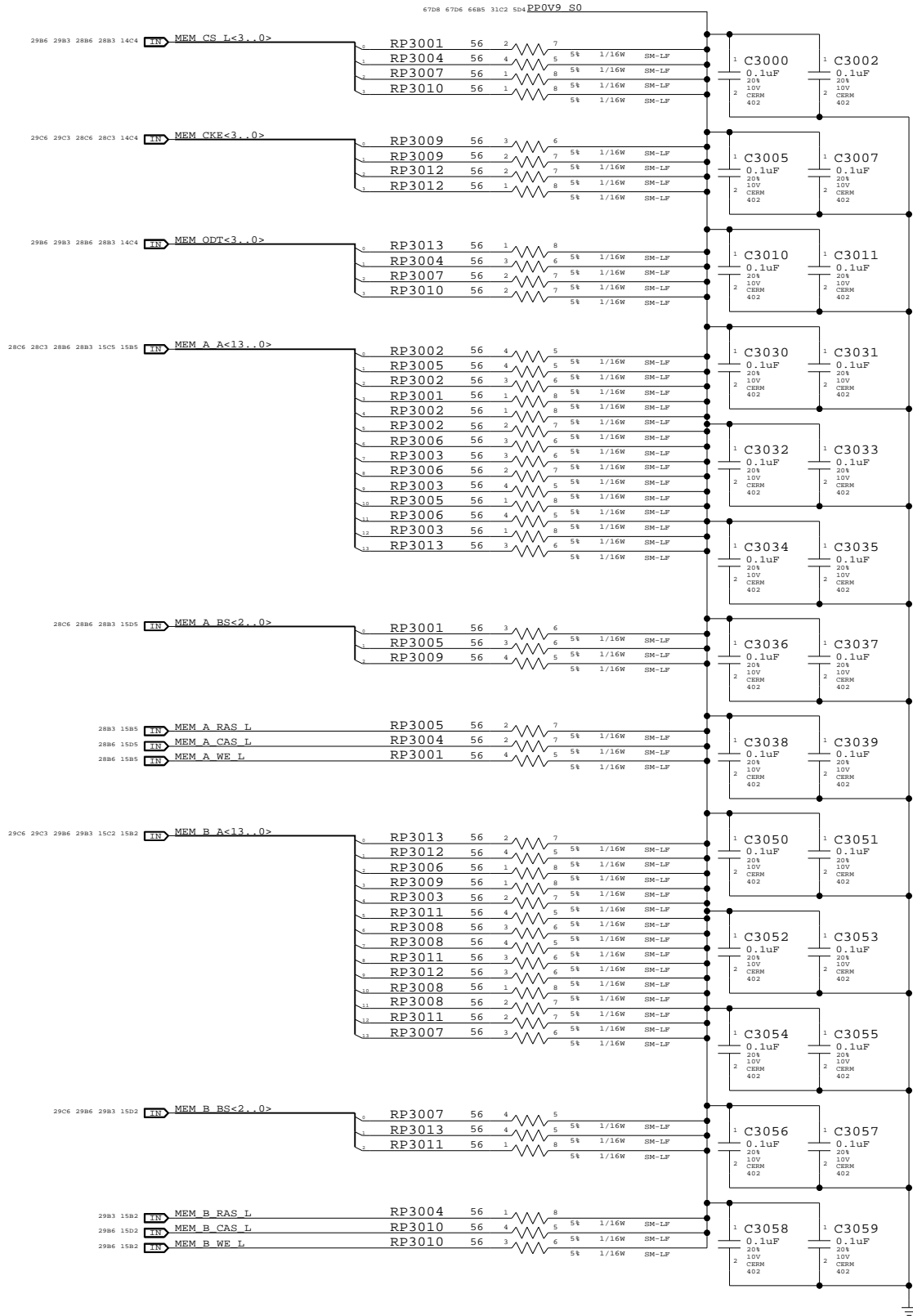
D

C

B

A

One cap for each side of every RPAK, one cap for every two discrete resistors
Ensure CS_L and ODT resistors are close to SO-DIMM connector



Memory Active Termination

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004
SCALE	SHT	OF
NONE	30	87

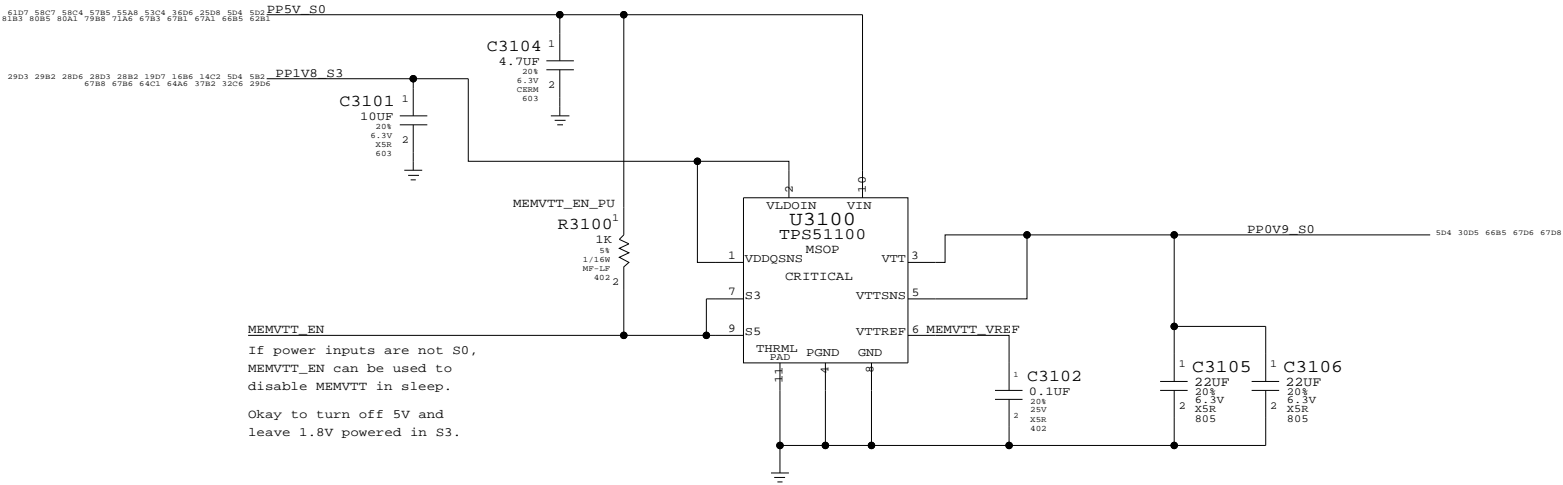
Page Notes

Power aliases required by this page:
- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

DDR2 Vtt Regulator



Memory Vtt Supply

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY
PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR
AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE COMPUTER INC.

SIZE

D

DRAWING NUMBER

051-7164

REV.

06004

SCALE

NONE

SHT

31

OF

87

D

D

C

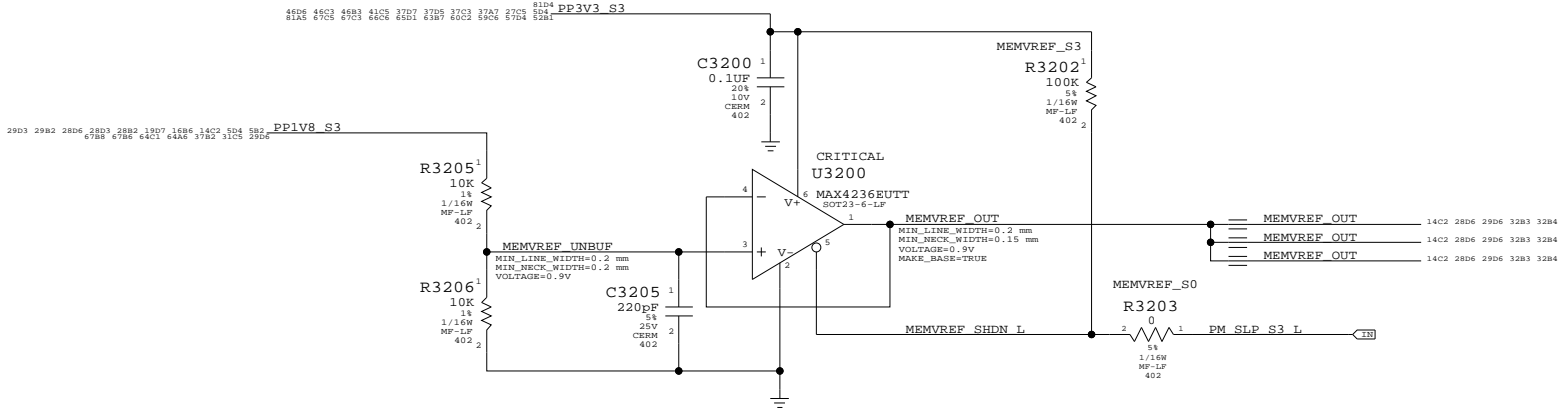
C

B

B

A

A



DDR2 VRef		
SYNC_MASTER=M59_MLB		SYNC_DATE=09/15/2006
NOTICE OF PROPRIETARY PROPERTY		
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING		
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE		
II NOT TO REPRODUCE OR COPY IT		
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART		

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7164	REV. 06004
	SCALE NONE	SHT 32	OF 87

D

C

B

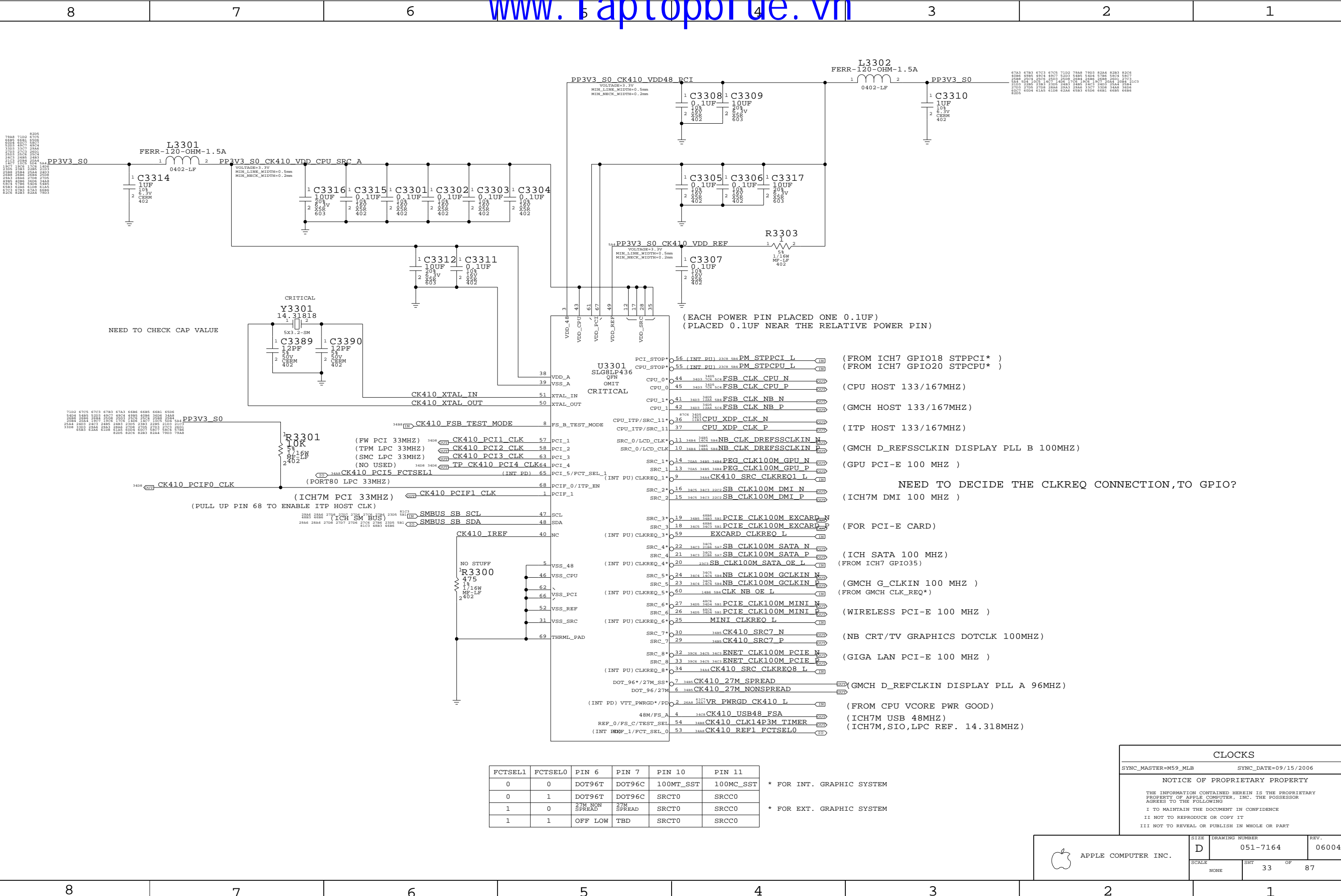
A

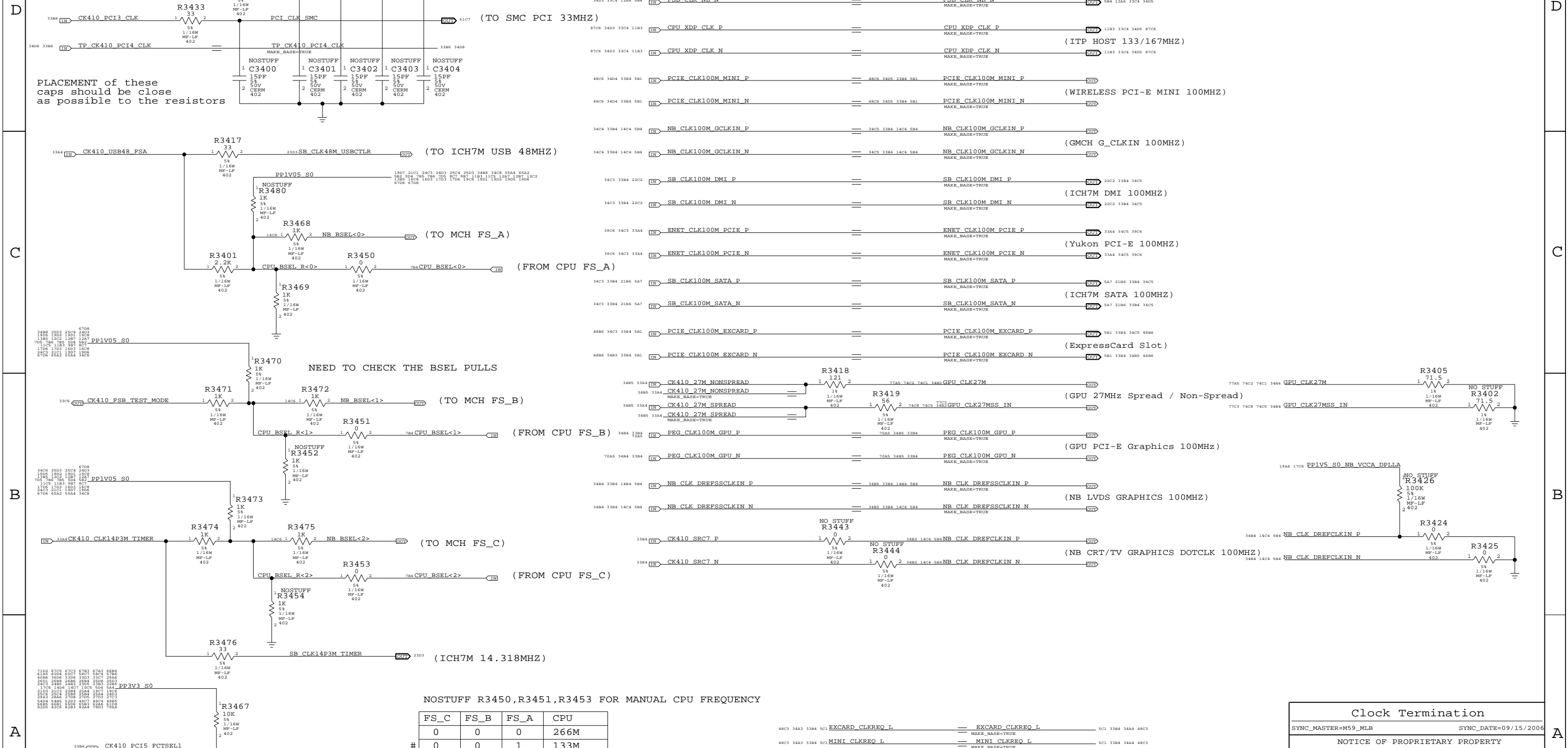
D

C

B

A

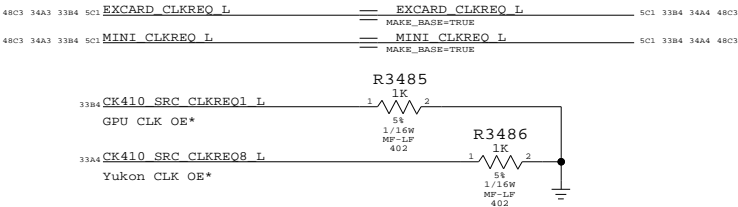





```
NOSTUFF R3450,R3451,R3453 FOR MANUAL CPU FREQUENCY
```

FS_C	FS_B	FS_A	CPU
0	0	0	266M
0	0	1	133M
0	1	0	166M
0	1	1	200M
1	0	0	100M
1	0	1	333M
1	1	0	400M
1	1	1	RESERVED

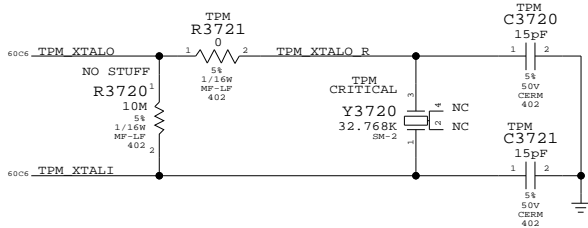
```
# NAPA PLATFORM ONLY SUPPORT 133M/166M CPU SPEED
```



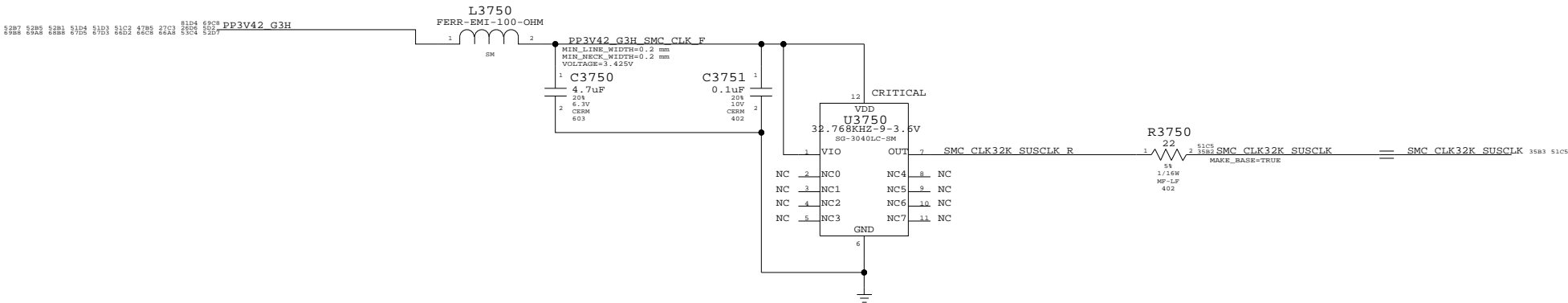
Clock Termination	
SYNCR_MASTER=M59_MLB	SYNCR_DATE=09/15/2006
NOTICE OF PROPRIETARY PROPERTY	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING	
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE	
I I NOT TO REPRODUCE OR COPY IT	
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART	

 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7164	06004
	SCALE	SHT OF	
	NONE	34 87	

TPM Crystal Circuit



SMC G3Hot Oscillator



Mobile Clocking

SYNC_MASTER=M59_MLB

SYNC_DATE=09/15/2006

NOTICE OF PROPRIETARY PROPERTY

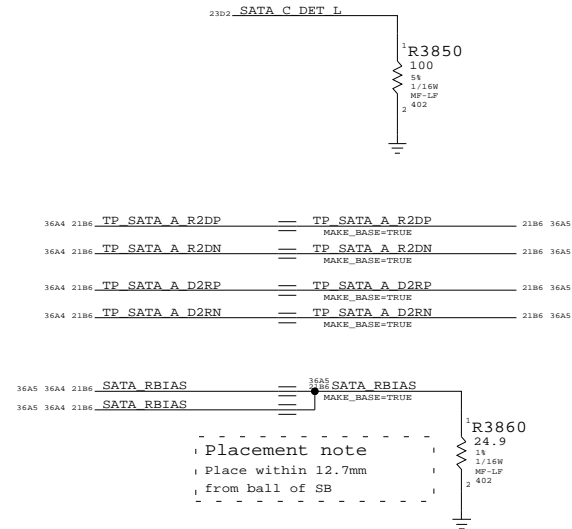
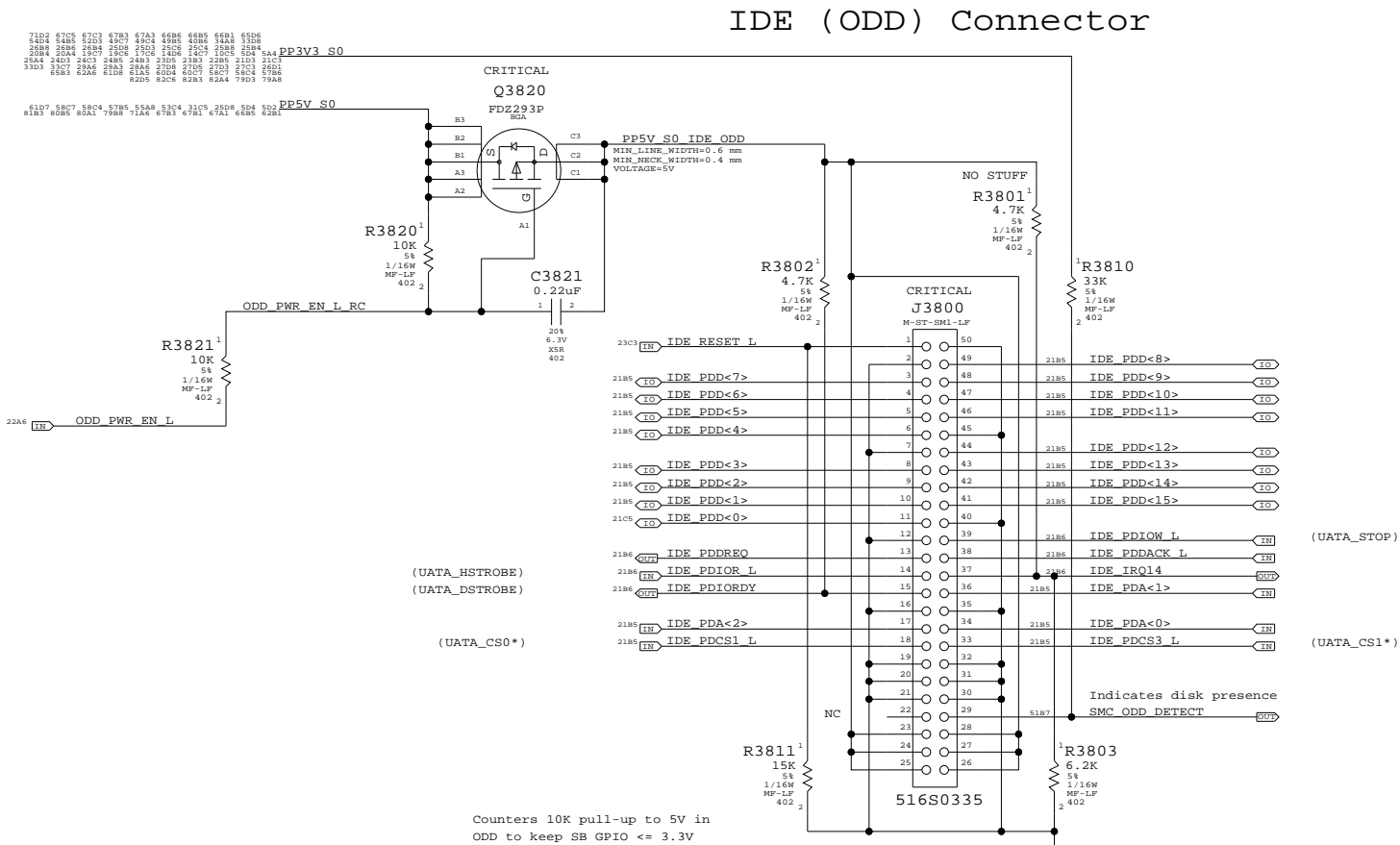
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7164	REV. 06004
	SCALE NONE	SHT 35	OF 87



PATA Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

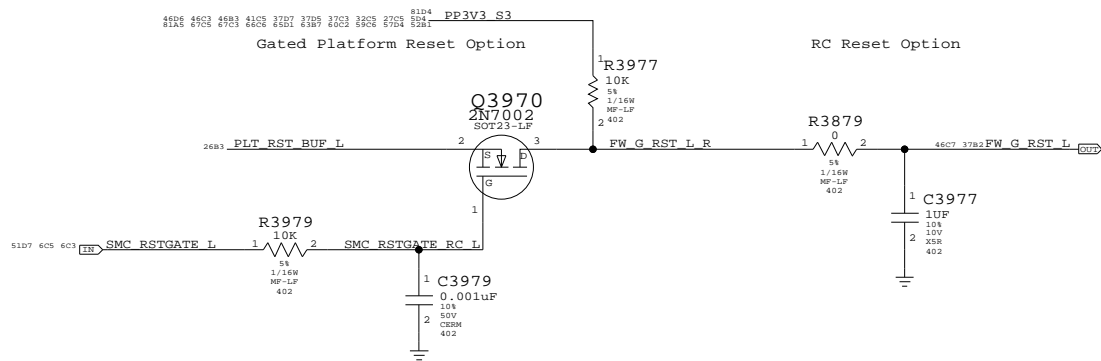
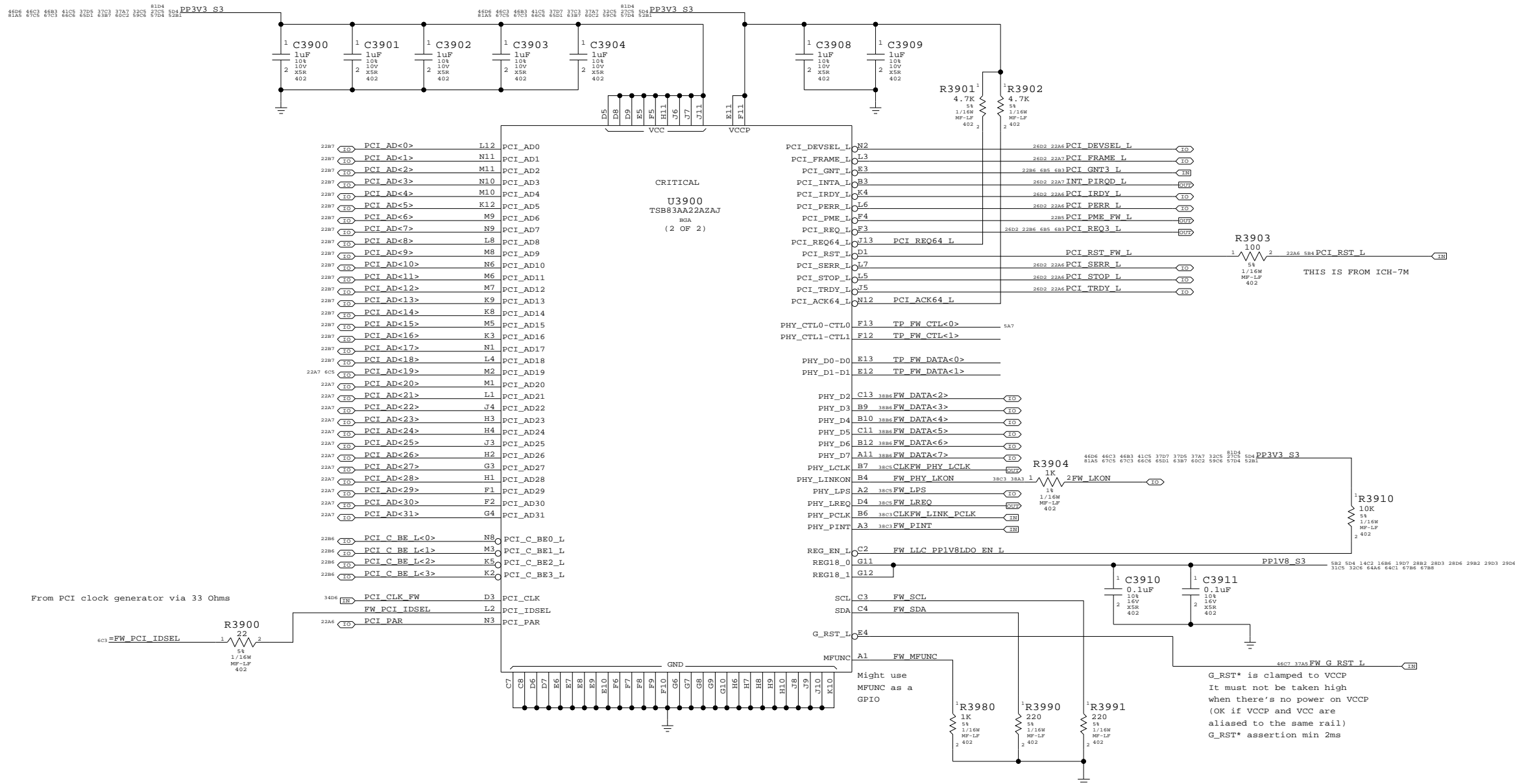
SIZE D

DRAWING NUMBER 051-7164

REV. 06004

SCALE NONE

SHT 36 OF 87



FireWire Link (TSB83AA22)

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

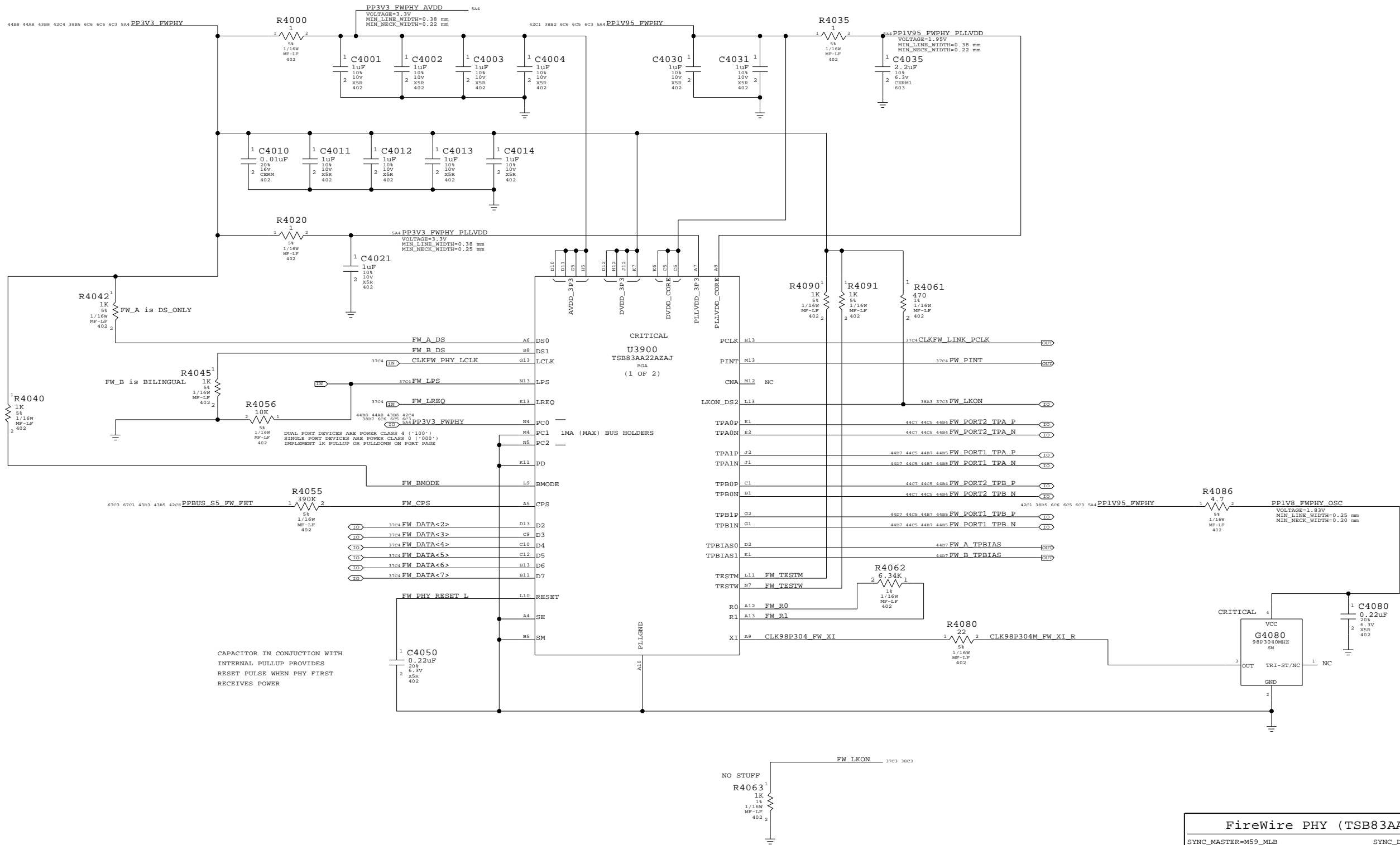
NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



FireWire PHY (TSB83AA22)

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7164	REV. 06004
	SCALE NONE	SHT 38	OF 87



ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		SPACING	PHYSICAL		
PROVIDED		ENETCONN	ENET_100D	ENETCONN_P<0>	40D3
		ENETCONN	ENET_100D	ENETCONN_N<0>	40C3
		ENETCONN	ENET_100D	ENETCONN_P<1>	40C3
BY		ENETCONN	ENET_100D	ENETCONN_N<1>	40C3
		ENETCONN	ENET_100D	ENETCONN_P<2>	40C3
		ENETCONN	ENET_100D	ENETCONN_N<2>	40C3
ETHERNET		ENETCONN	ENET_100D	ENETCONN_P<3>	40C3
		ENETCONN	ENET_100D	ENETCONN_N<3>	40B3
		PHY	ENETCONN	ENETCONN_N<3>	40B3

Page Notes

Power aliases required by this page:

- =PP2V5_ENET
- =GND_CHASSIS_ENET

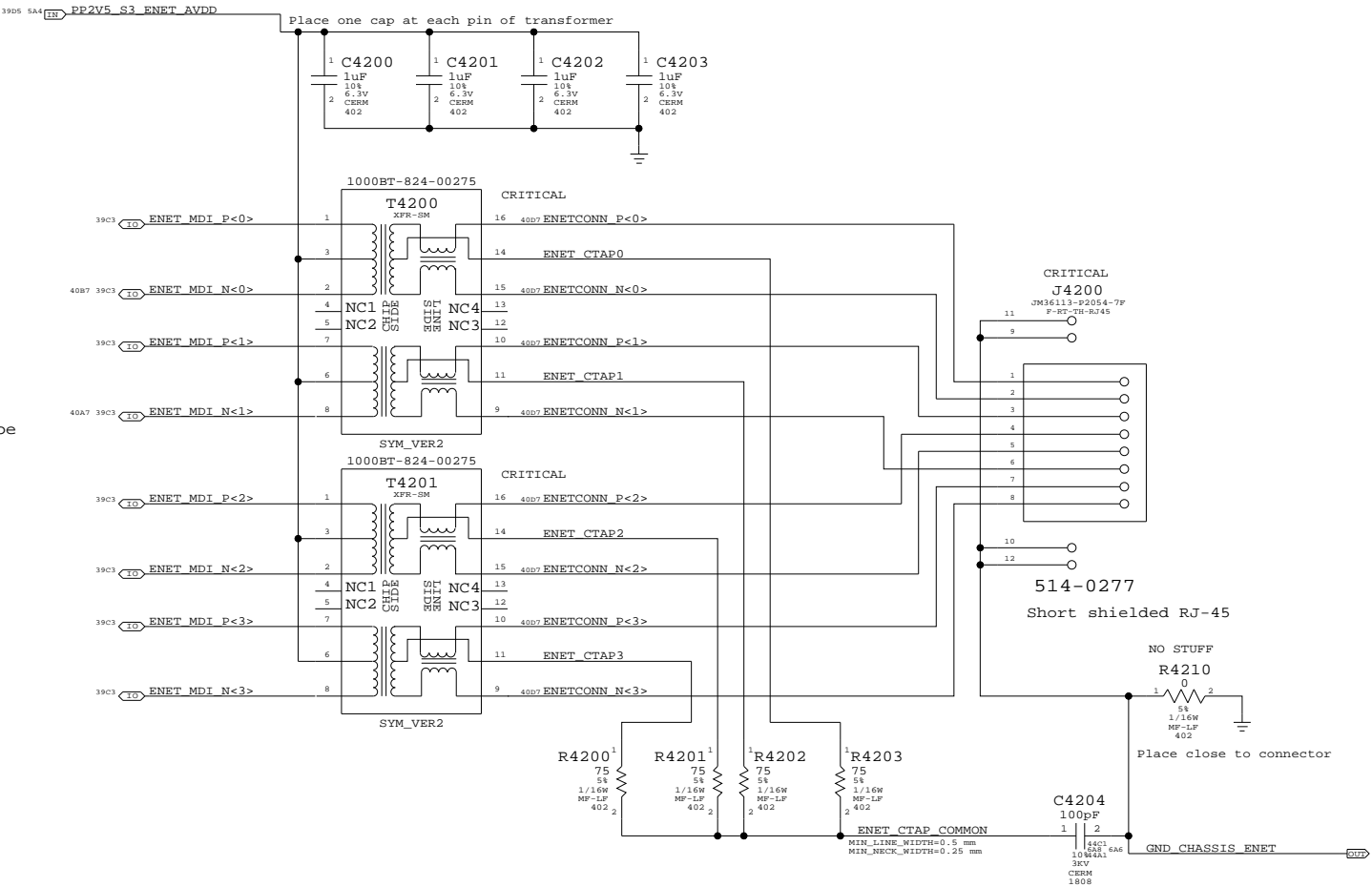
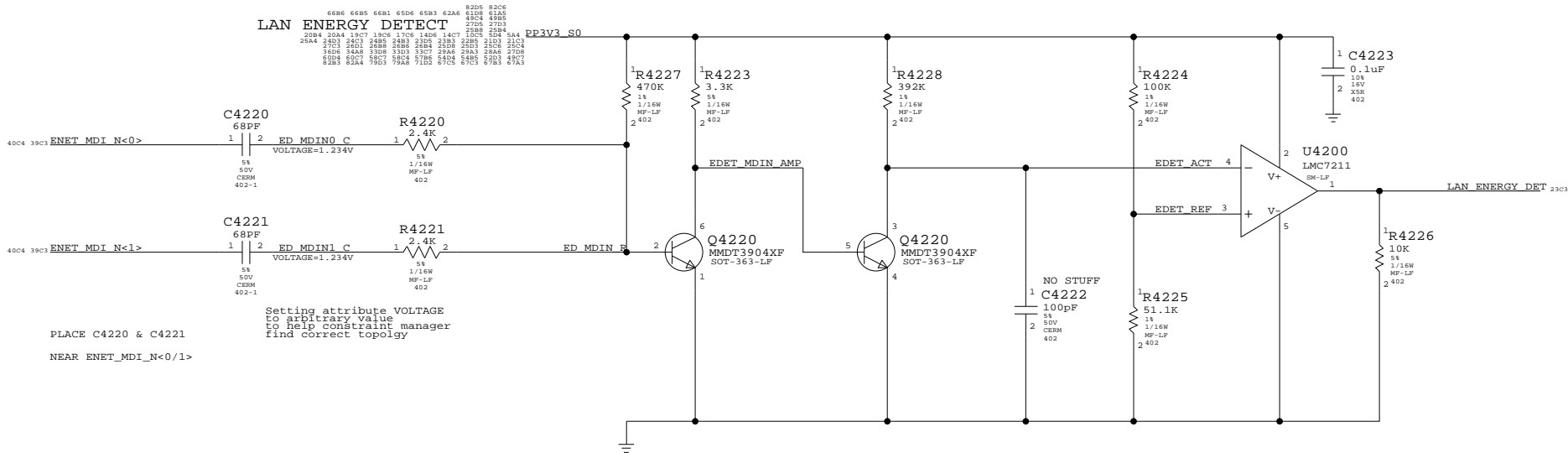
Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

Transformers should be mirrored on opposite sides of the board

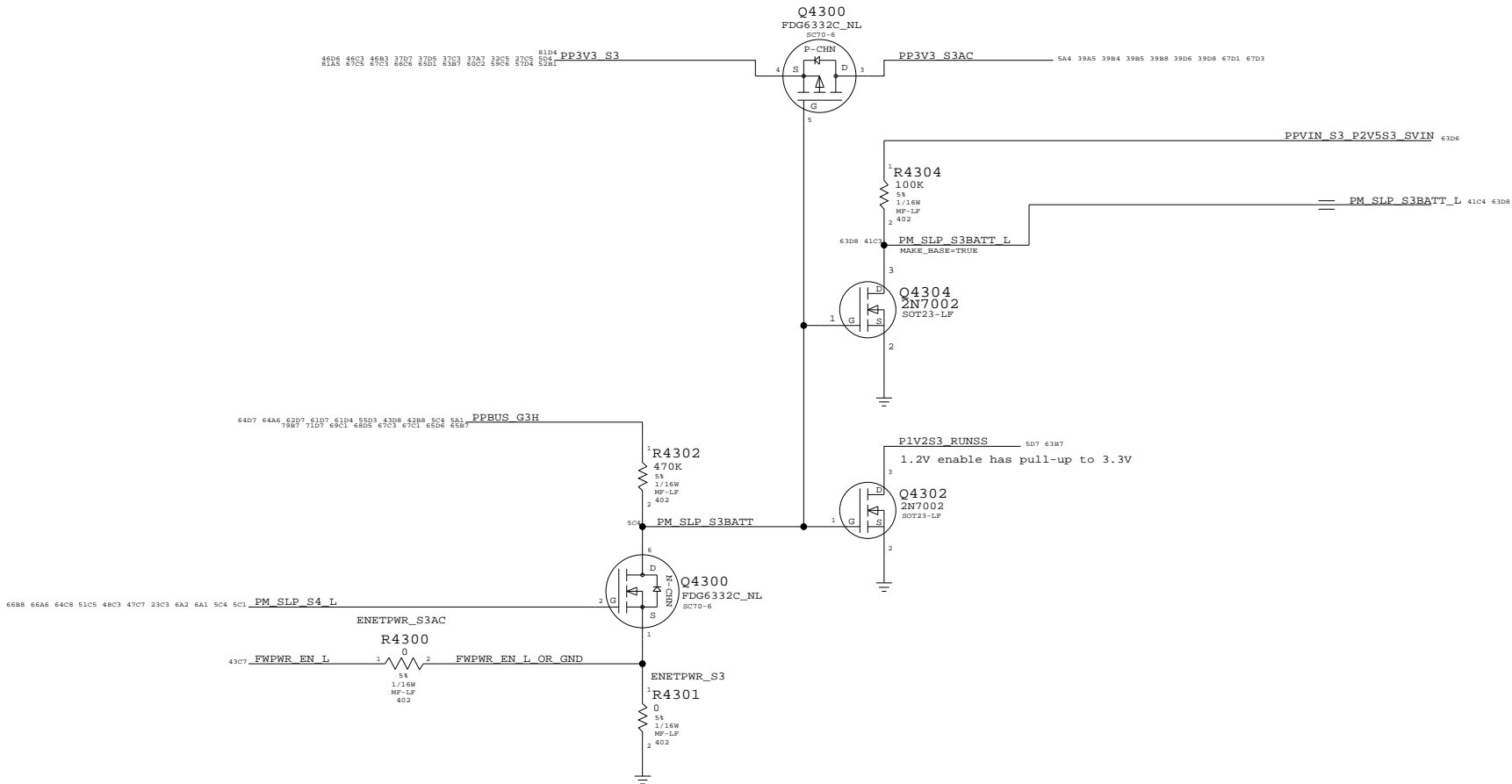


Ethernet Connector	
SYNC_MASTER=M59_MLB	SYNC_DATE=09/15/2006
NOTICE OF PROPRIETARY PROPERTY	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING	
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE	
II NOT TO REPRODUCE OR COPY IT	
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART	

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7164	06004
SCALE		SHT	OF
NONE		40	87

Yukon Power Control

Allows powering Yukon down during battery sleep to save power



When ENETPWR_S3AC BOMOPTION is active:

State	FWPWR_EN_L	PM_SLP_S4_L	PM_SLP_S3BATT	PM_SLP_S3BATT_L	P2V5S3_EN	P1V2S3_RUNSS
S0 AC	0V	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S0 Batt	0V	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S3 AC	0V	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S3 Batt	PBUS	3.3V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)
S5 AC	0V	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)
S5 Batt	PBUS	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)
G3H Batt	PBUS	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)

When ENETPWR_S3 BOMOPTION is active:

State	PM_SLP_S4_L	PM_SLP_S3BATT	PM_SLP_S3BATT_L	P2V5S3_EN	P1V2S3_RUNSS
S0	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S3	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S5	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)
G3H	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)

Yukon Power Control

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE COMPUTER INC.

SIZE

D

DRAWING NUMBER

051-7164

REV.

06004

SCALE

NONE

SHT

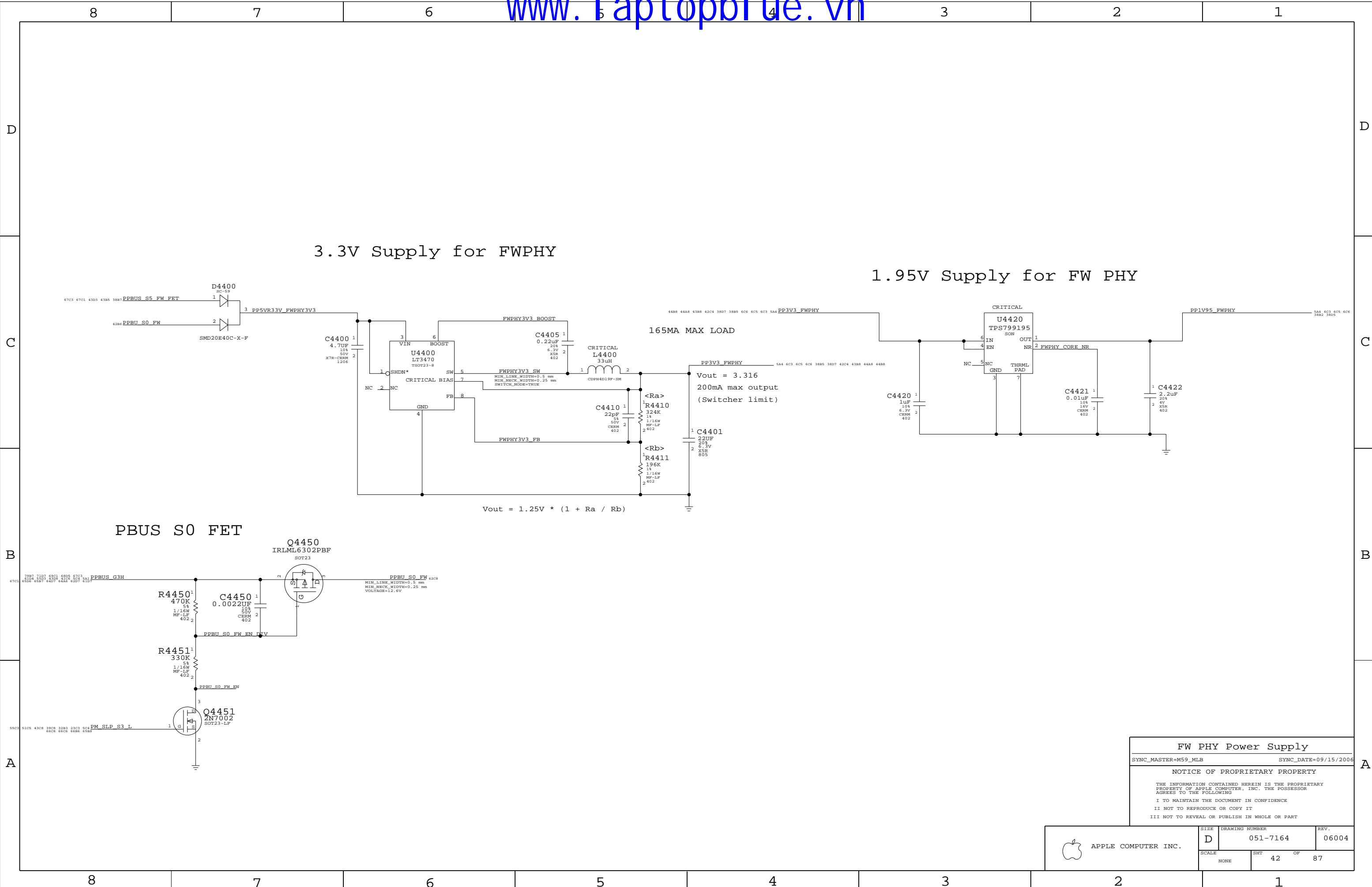
41

OF

87

3.3V Supply for FWPHY

1.95V Supply for FW PHY



Page Notes

Power aliases required by this page:

- =PPBUS_S0_FWPWRSW (system supply for bus power)
- =PP3V3_S0_FWPORTPWRSW

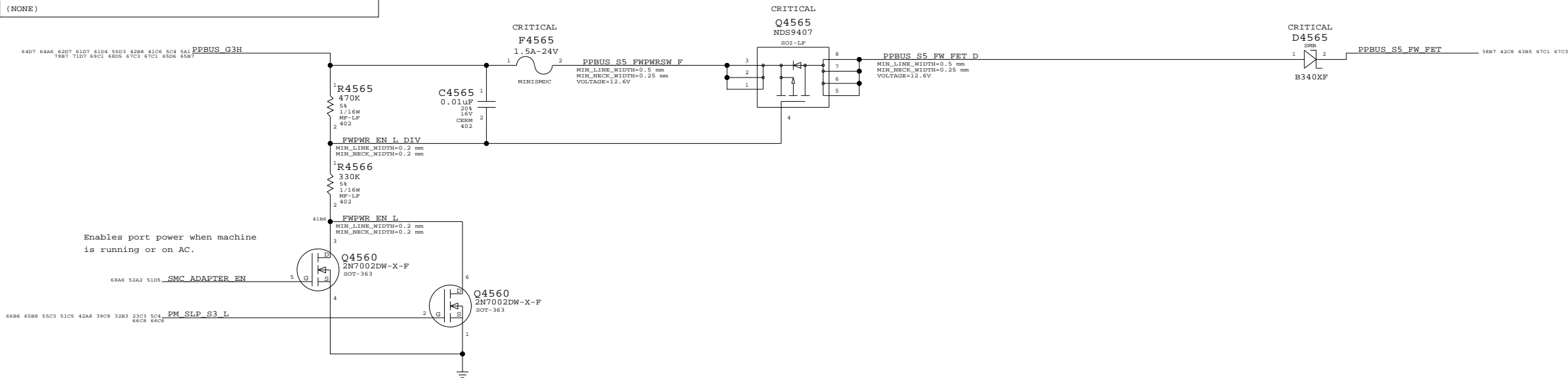
Signal aliases required by this page:

- =FWPWR_PWRON (see related text note below)

BOM options provided by this page:

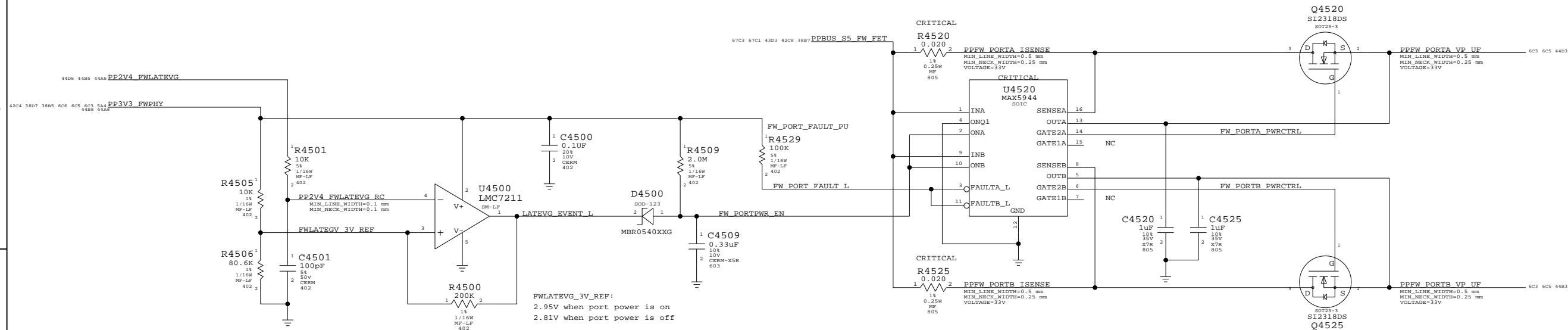
(NONE)

Port Power Switch



Current Limit/Active Late-VG Protection

Late-VG Event Detection



Current Limits

0.020 ohm => 2.4A
0.025 ohm => 2A
0.030 ohm => 1.66A (Ideal)
0.033 ohm => 1.5A

MAX5944 current limiter trips if integrator (counter) reaches 16. A new sample (taken every 125 us) is weighted as +1 if over the limit (at any point during the period) and -1/128 if under the limit. As a result, the device tends to trip easily on devices that produce periodic current spikes. Current limit has been set higher to compensate.

FireWire Port Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE













II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004
SCALE	SHT	OF
NONE	43	87

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		SPACING	PHYSICAL		
  	PROVIDED	FW	FW_110D	FW_PORT1_TPA_P	3803 4485 4487 44C5
		FW	FW_110D	FW_PORT1_TPA_N	3803 4485 4487 44C5
		FW	FW_110D	FW_PORT1_TPB_P	3803 4485 4487 44C5
  	BY	FW	FW_110D	FW_PORT1_TPB_N	3803 4485 4487 44C5
		FW	FW_110D	FW_PORT2_TPA_FL_P	4482
		FW	FW_110D	FW_PORT2_TPA_FL_N	4482
  	PHY	FW	FW_110D	FW_PORT2_TPB_FL_P	4482
		FW	FW_110D	FW_PORT2_TPB_FL_N	4482
		FW	FW_110D	FW_PORT2_TPB_FL_N	4482
  	PAGE	FW	FW_110D		
		FW	FW_110D		

Page Notes

Power aliases required by this page:

```
- =PPFW_PORT1
- =PP3V3_S5_FWLATEVG
- =GND_CHASSIS_FW_PO
```

Signal aliases required by this page:

(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals

BOM options provided by this page:

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple
FireWire Design Guide (FWDG 0.6, 5/14/03)

Termination

Place close to FireWire PHY

TI PHYs require 1uF even though FW spec calls out 0.33uF

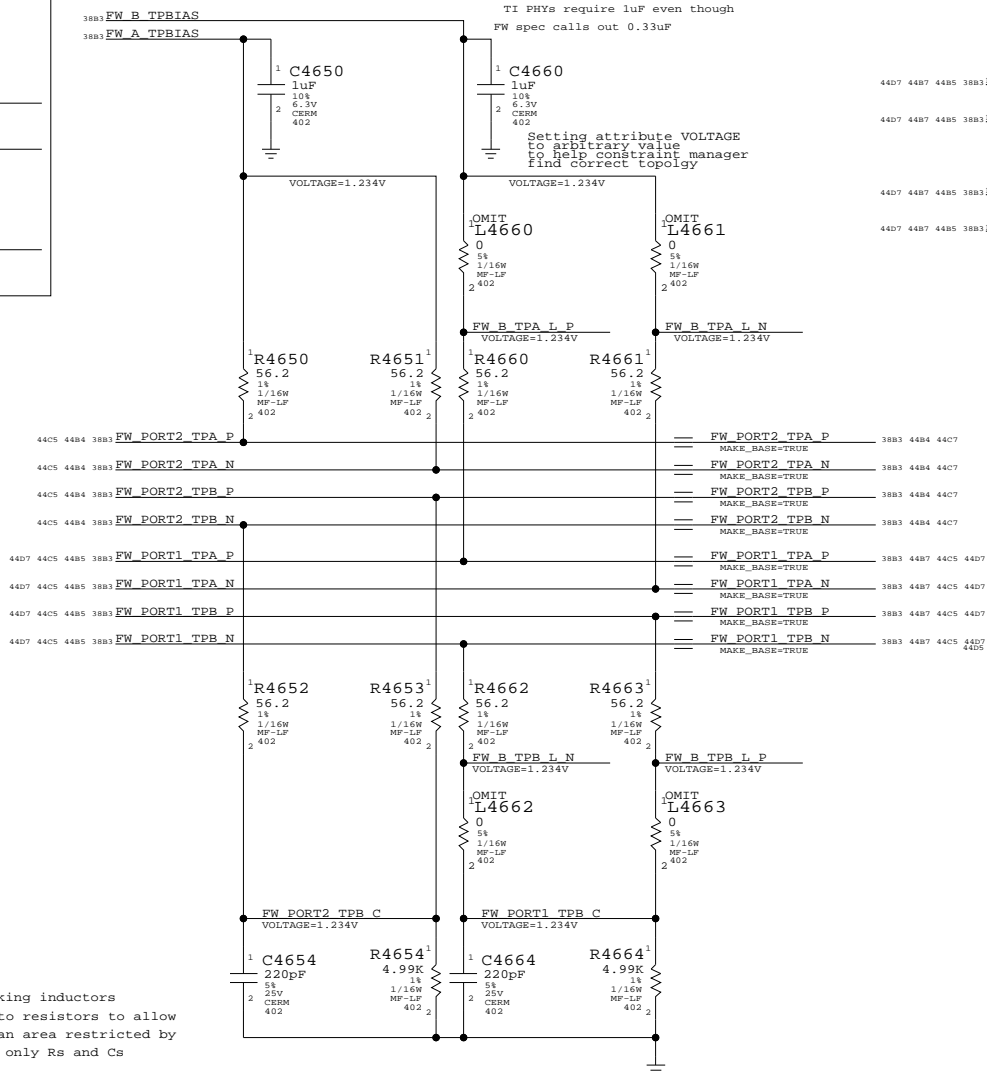
```

C4650
uF
0%
.3V
TERM
02

1
C4660
uF
10%
6.3V
TERM
402

Setting attribute VOLTAGE
to arbitrary value
to help constraint manager
find correct topology

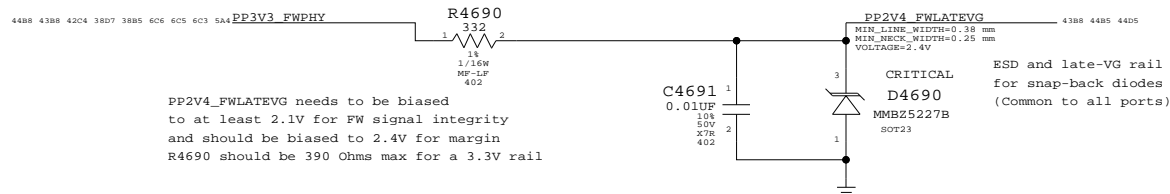
```



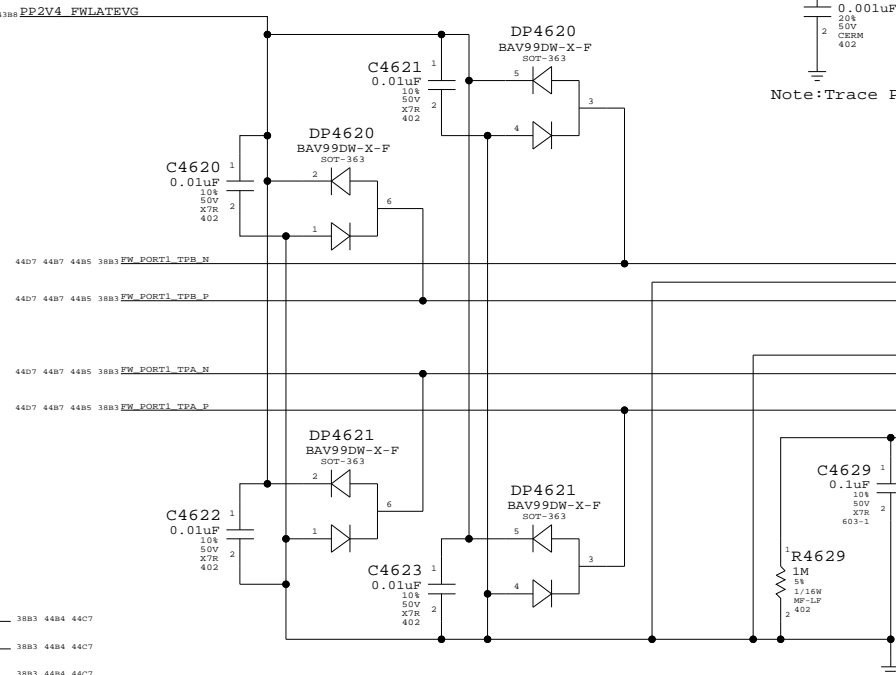
Note: The peaking inductors were changed to resistors to allow placement in an area restricted by DFM rules for only Rs and Cs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
152S0414	4	IND, 18nH-15mA, 0402	L4660, L4661, L4662, L4663	CRITICAL	

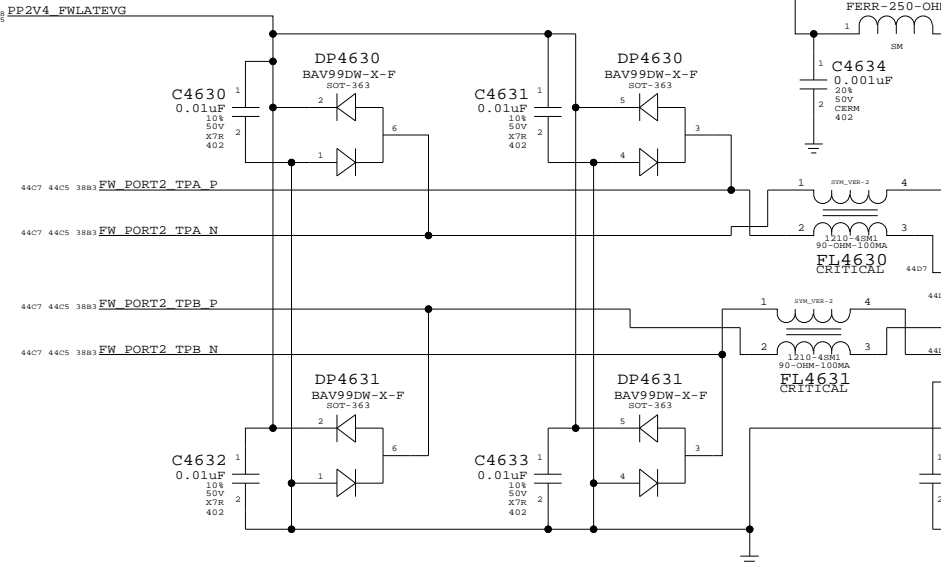
Late-VG Protection Power



"Snapback" & "Late VG" Protection



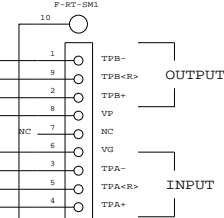
"Snapback" & "Late VG" Protection



PORT 1

CRITICAL

J4620
1394B UC3100

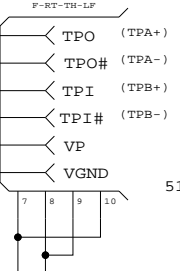


514S0133

PORT 2
1394A

CRITICAL

J4630
13948



FireWire Ports

SYNC_MASTER=M59_MLB

SYNC_DATE=06/27/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY
PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR
AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE COMPUTER INC.

	SIZE
--	------

DRAWING NUMBER

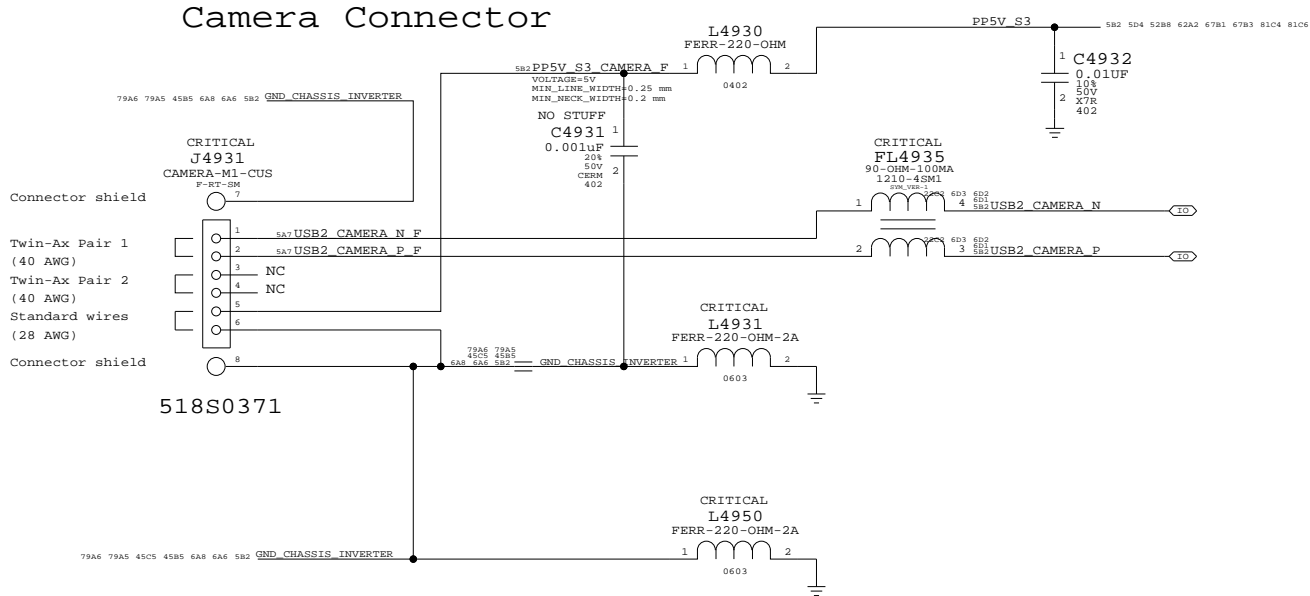
REV.

SCALE

SHT

OF

97



Camera Connector

SYNC_MASTER=M59_MLB

SYNC_DATE=09/15/2006


NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

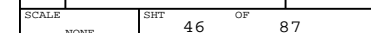
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

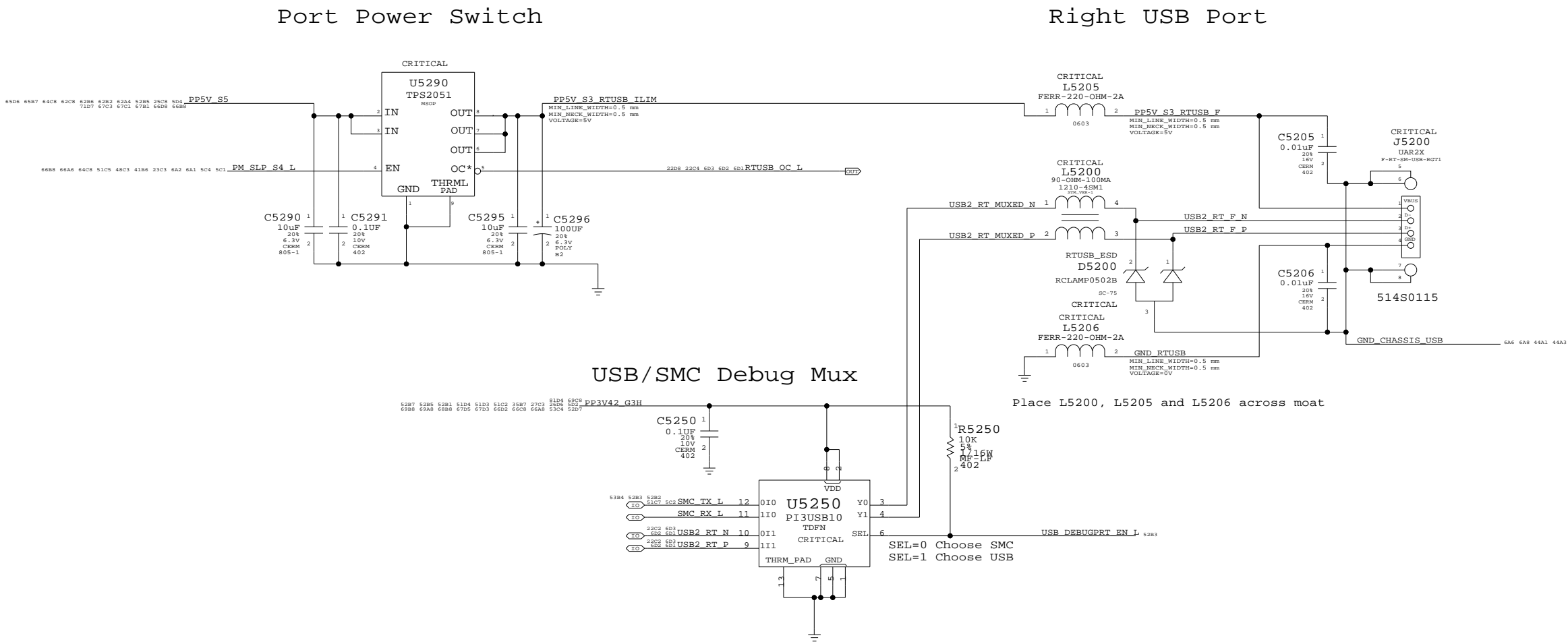
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7164	06004
SCALE		SHT	OF
NONE		45	87







External USB Connector

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

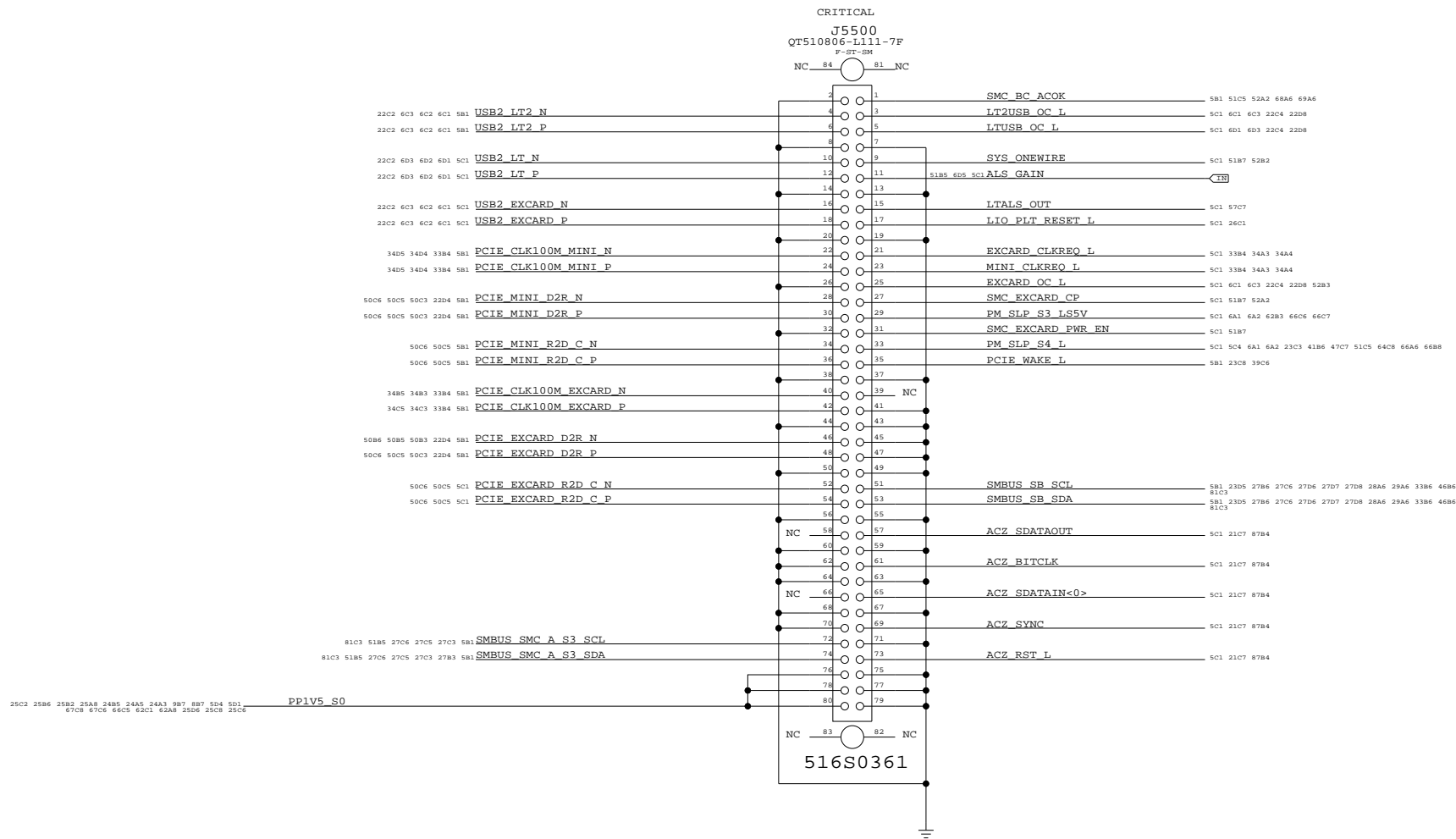
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7164	REV. 06004
	SCALE NONE	SHT 47	OF 87

Left I/O Board Connector



Left I/O Board Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

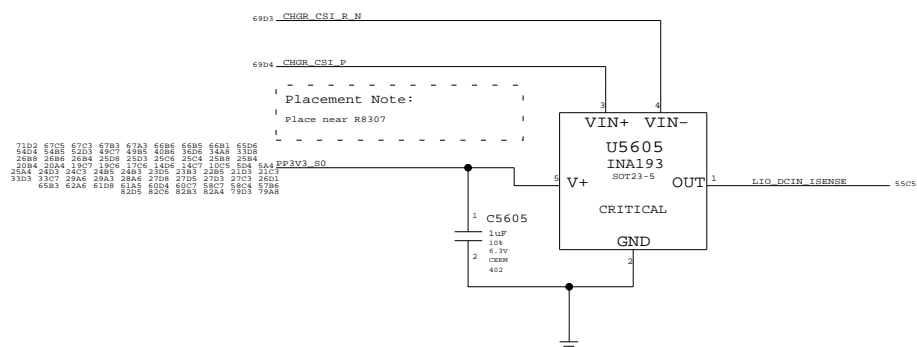
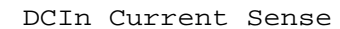
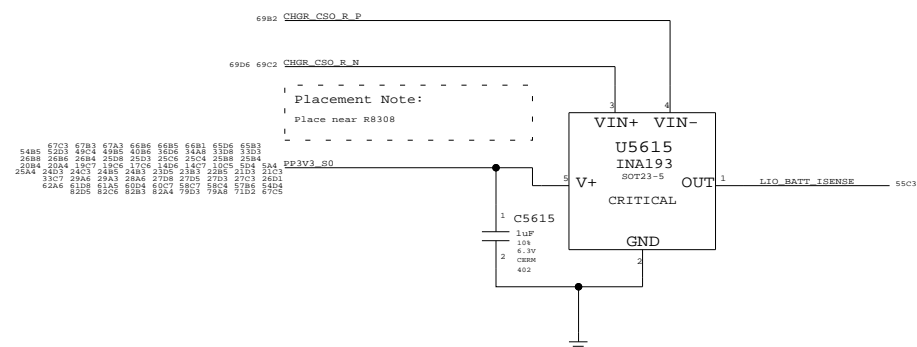
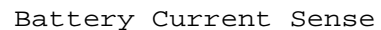
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

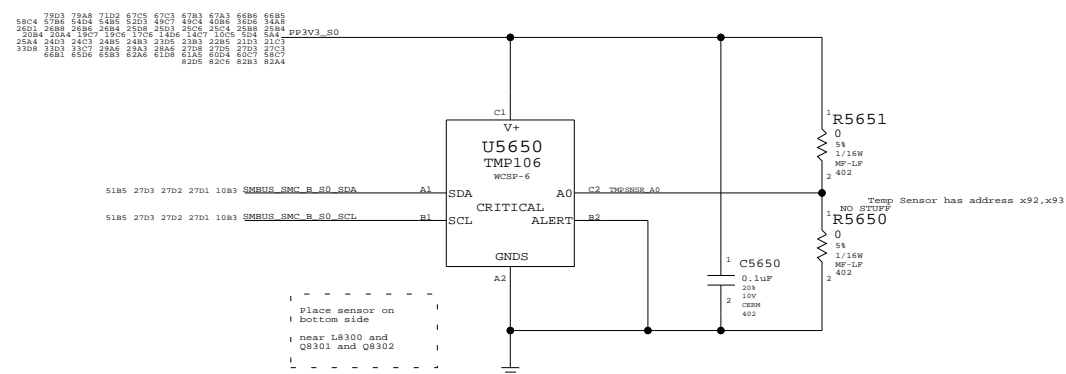


APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004
SCALE	SHT	OF
NONE	48	87



TMP106 Thermal Sensor



Current & Thermal Sensors

SYNC_MASTER= (MASTER)	SYNC_DATE= (MASTER)
-------------------------	-----------------------

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY
PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR
AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004
SCALE	SHT	OF
NONE	49	87

D

D

C

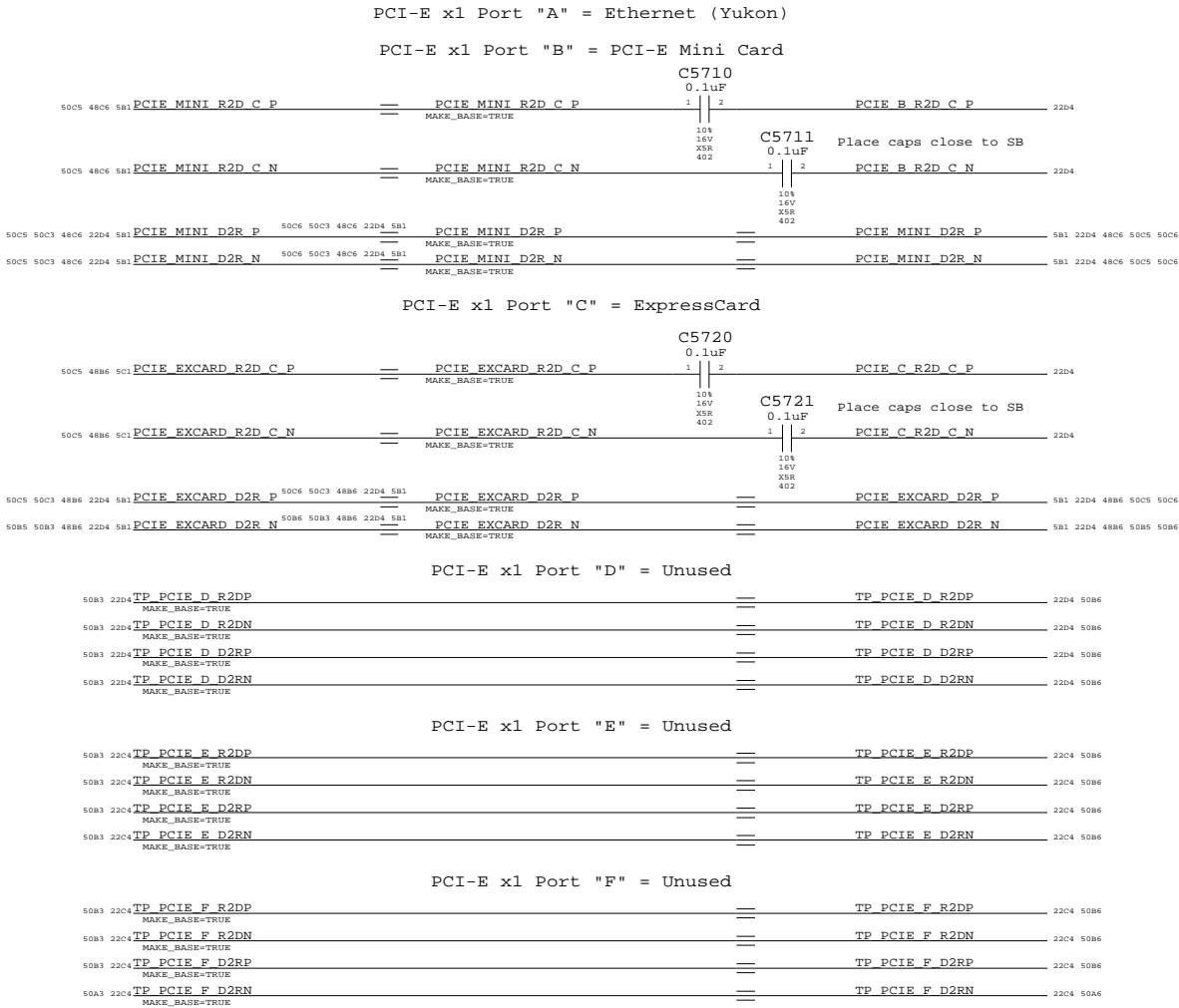
C

B

B

A

A



PCI-E Connections

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

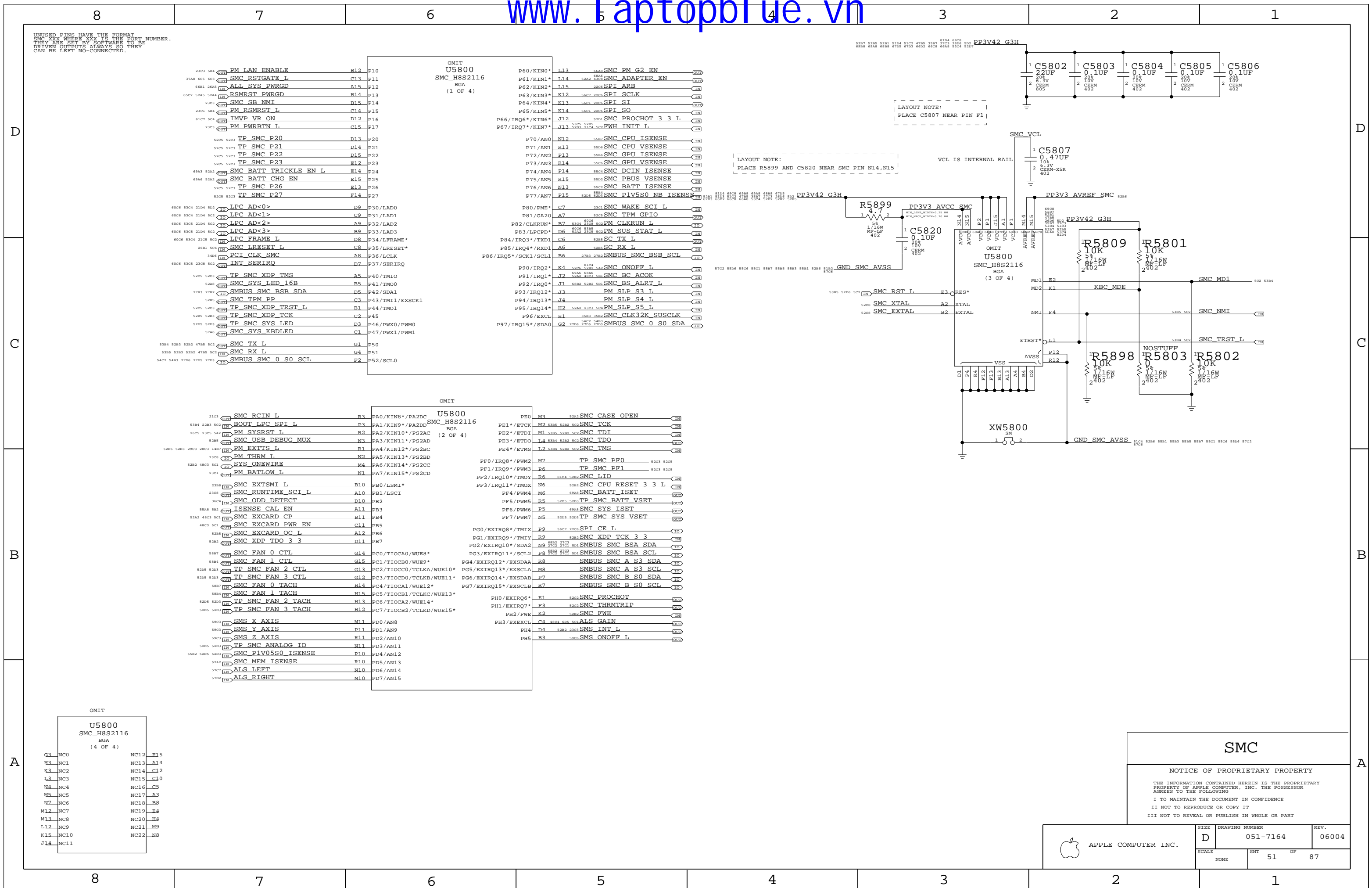
NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004
SCALE	SHT	OF
NONE	50	87



D

D

C

C

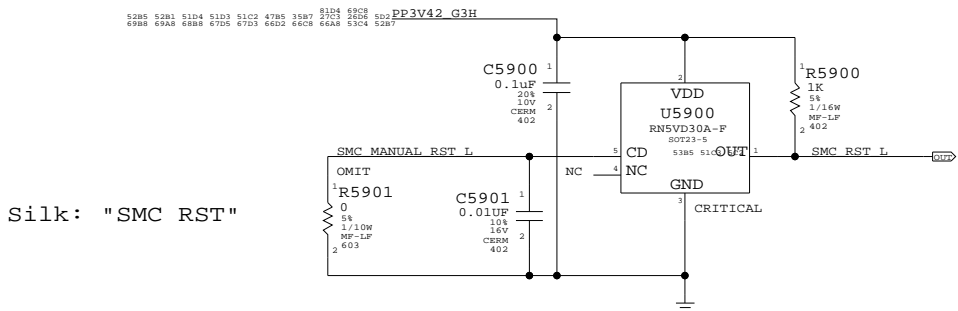
B

B

A

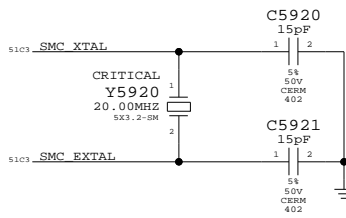
A

SMC Reset Button / Brownout Detect

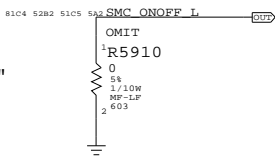


Silk: "SMC RST"

SMC Crystal Circuit

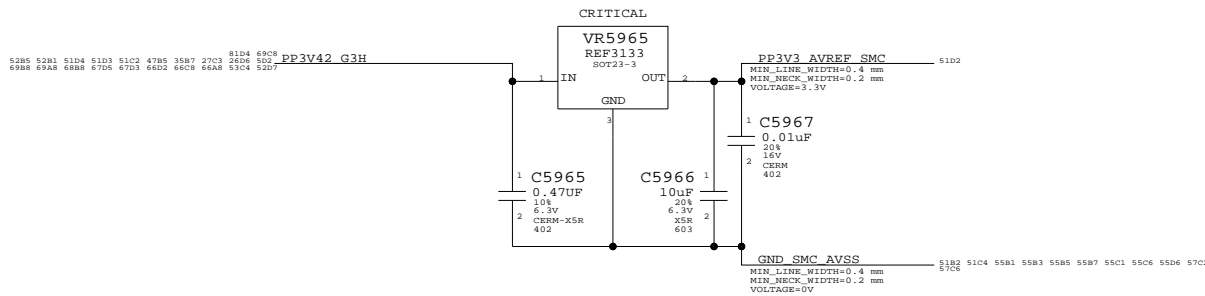


Debug Power Button

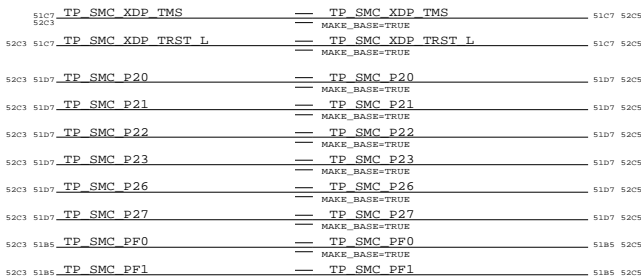
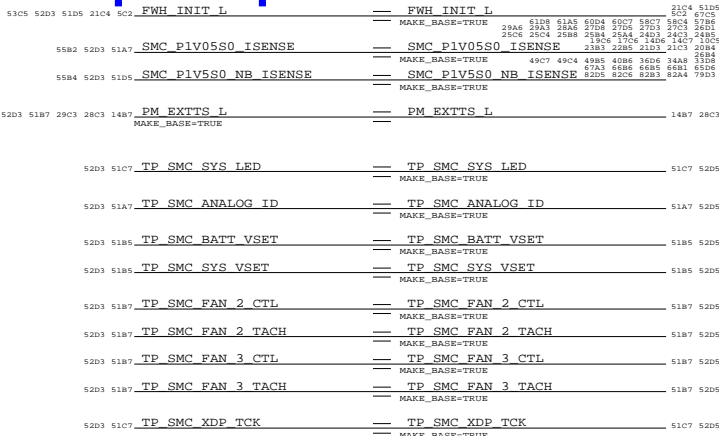
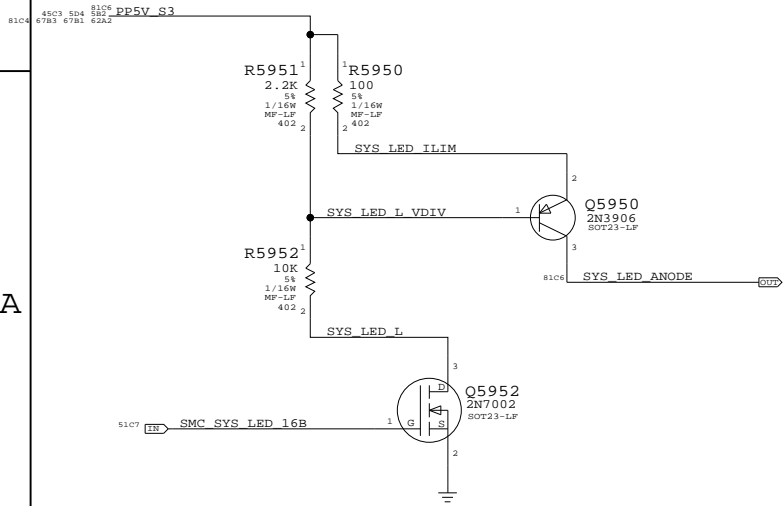


Silk: "PWR BTN"

SMC AVREF Supply

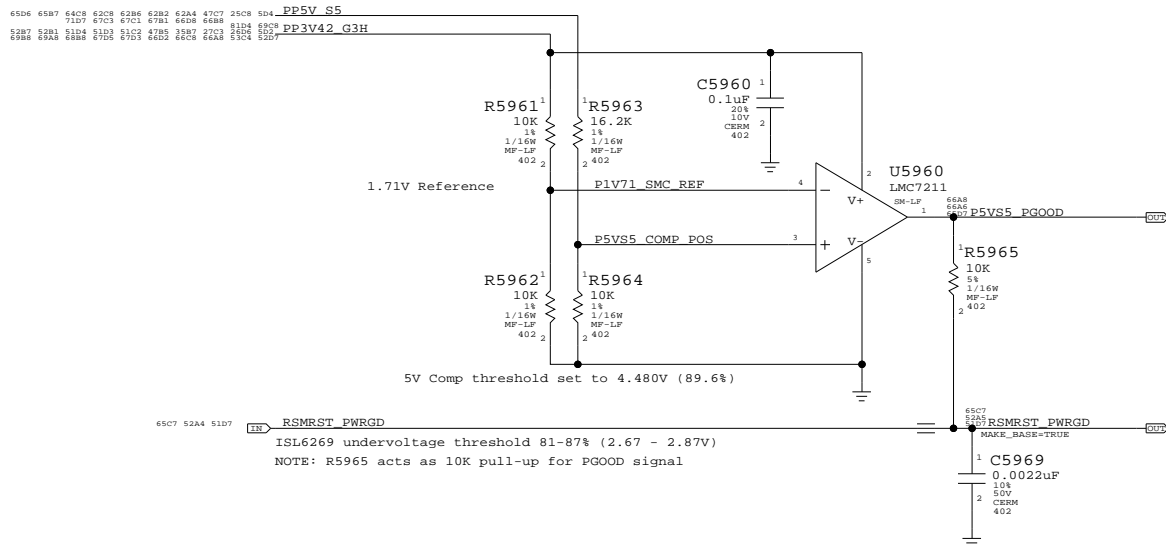


System (Sleep) LED Circuit

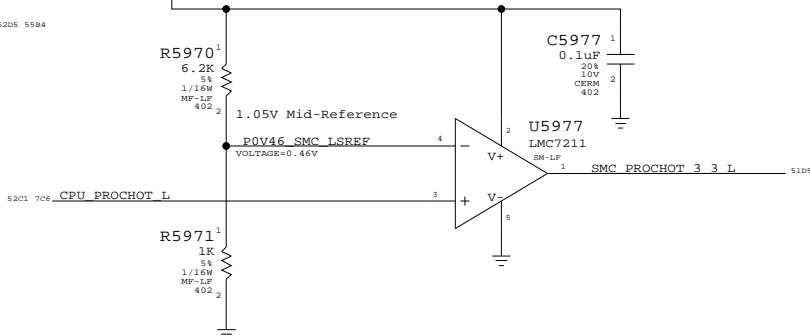


SMC PWRGD Circuit

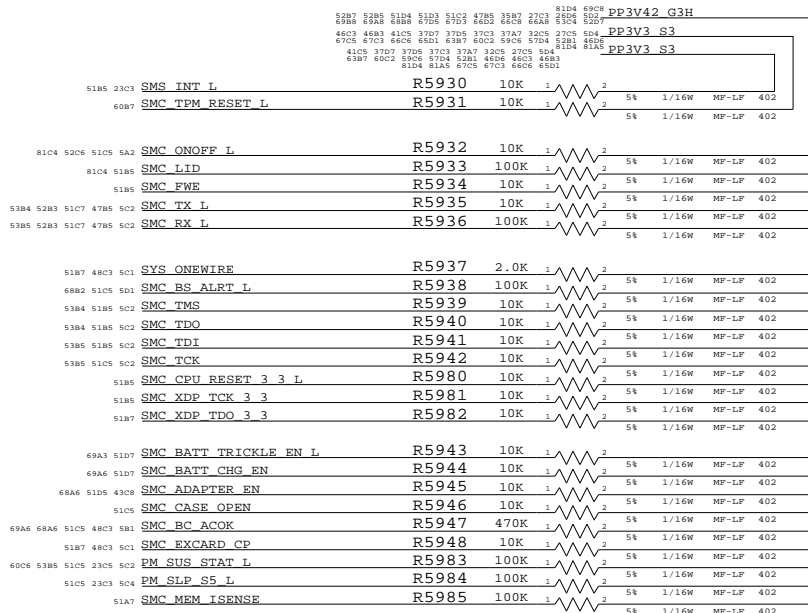
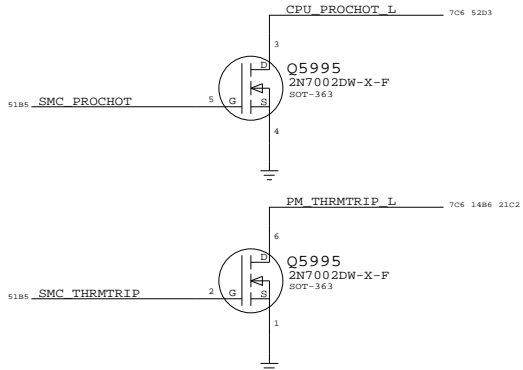
Reports when 5V S5 and 3.3V S5 are in regulation



SMC 1.05V to 3.3V Level Shifting



SMC 3.3V to 1.05V Level Shifting



SMC Support

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

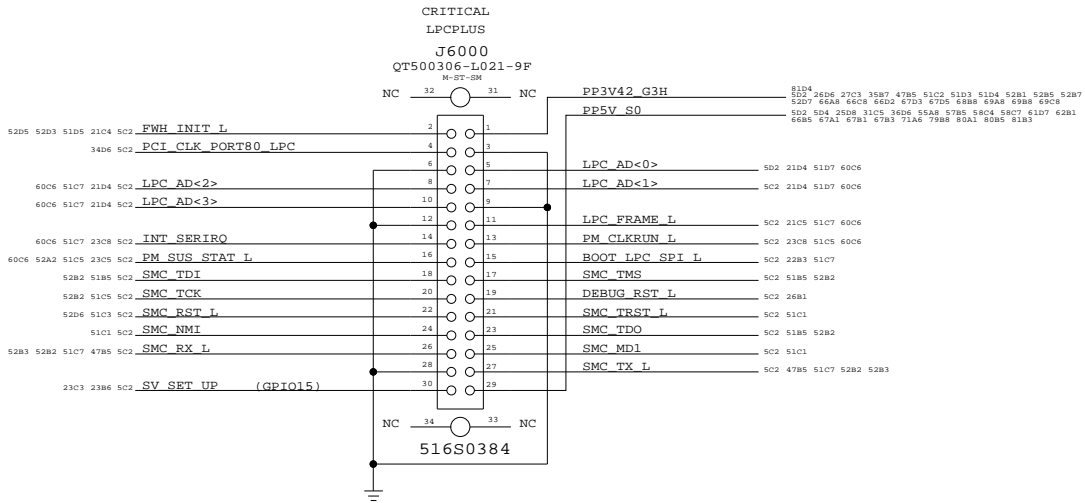
NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



LPC+ Debug Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

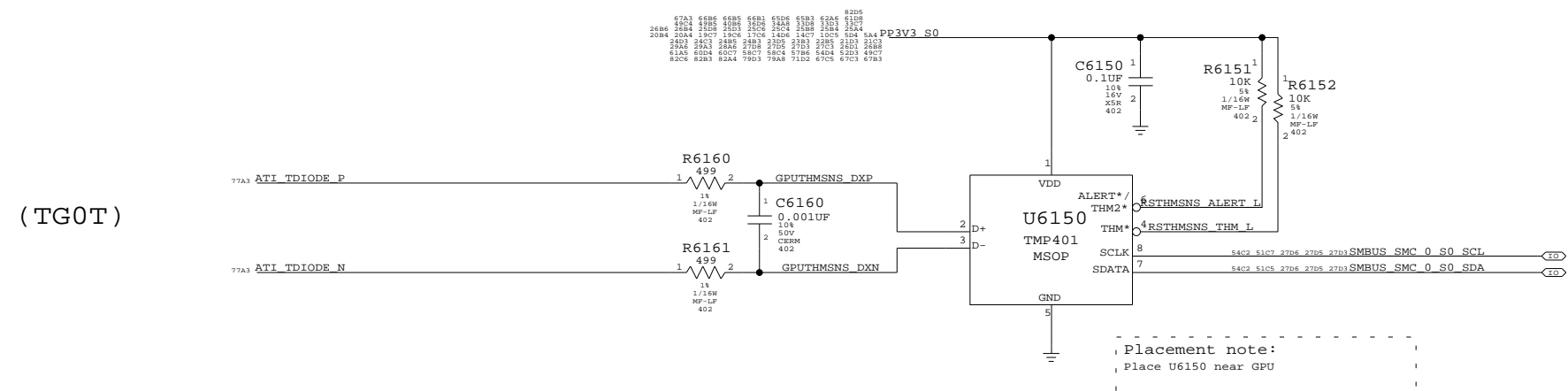
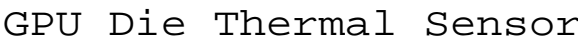
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART




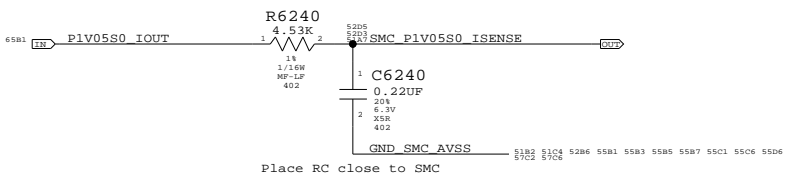
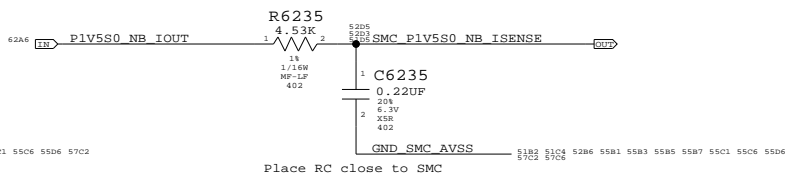
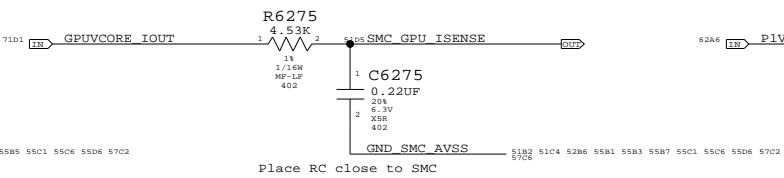
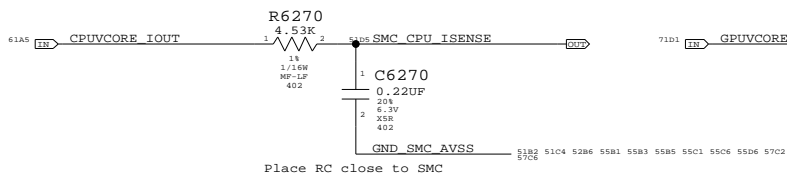
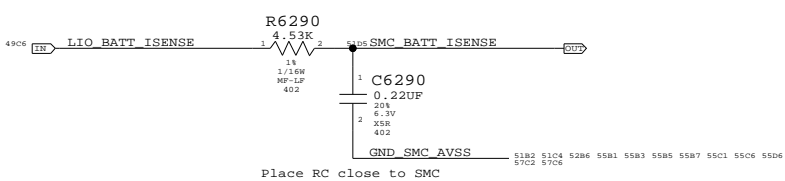
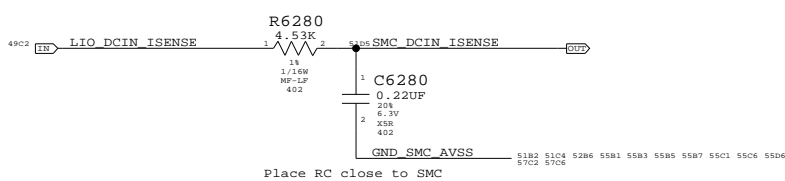
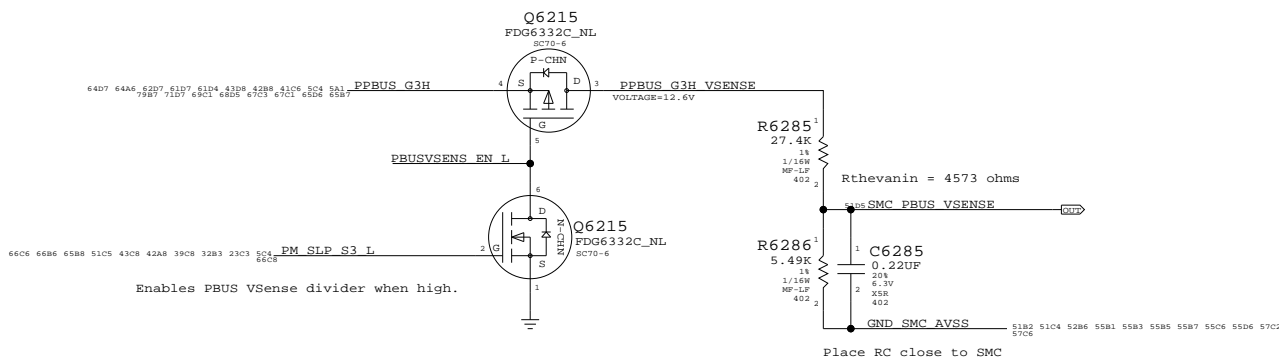
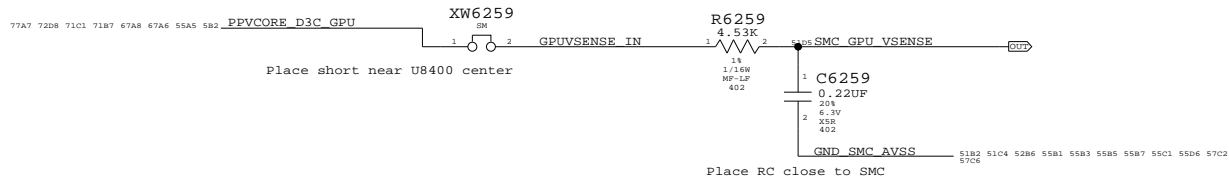
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004
SCALE	SHT	OF
NONE	53	87

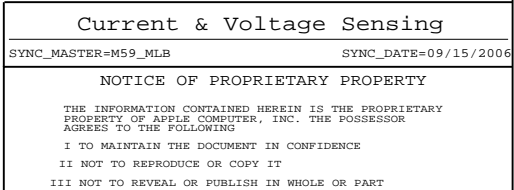
A

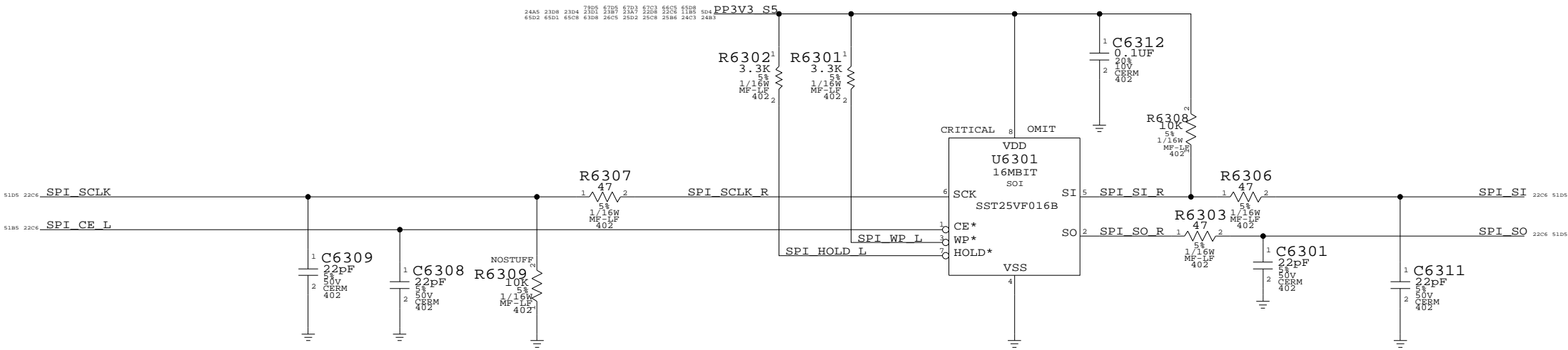


 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7164	REV. 06004
	SCALE NONE	SHT OF 54 OF 87	



Switches in fixed load on power supplies to calibrate current sense circuits





R6309 IS NOT NEEDED WHEN SHARING SPI FLASH WITH ICH7M AND TEKOA(LAN CHIP)

R6307 AND R6306 SHOULD BE PLACED LESS THAN 100 MILS FORM ICH7M
R6303 SHOULD BE PLACED LESS THAN 100 MILS FORM FLASH ROM

SPI BOOTROM

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006


NOTICE OF PROPRIETARY PROPERTY

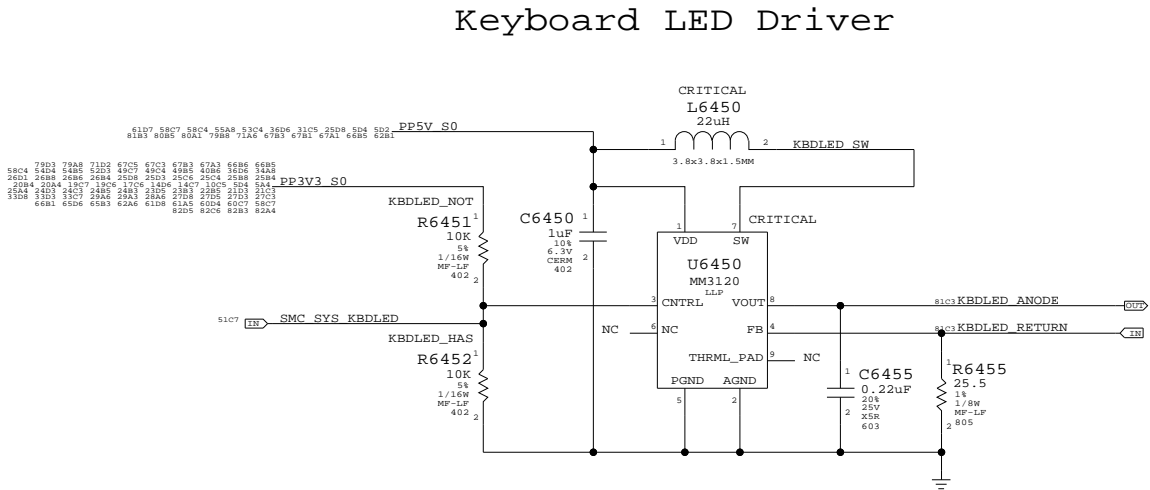
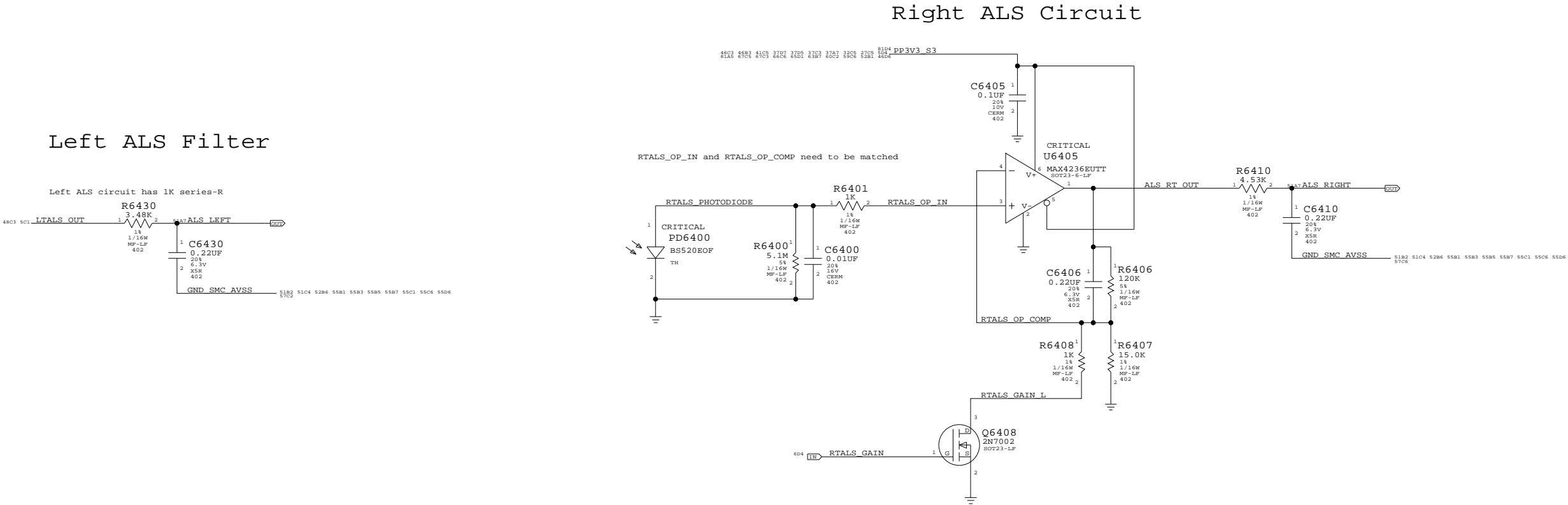
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7164	REV. 06004
	SCALE NONE	SHT 56	OF 87



ALS Support

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

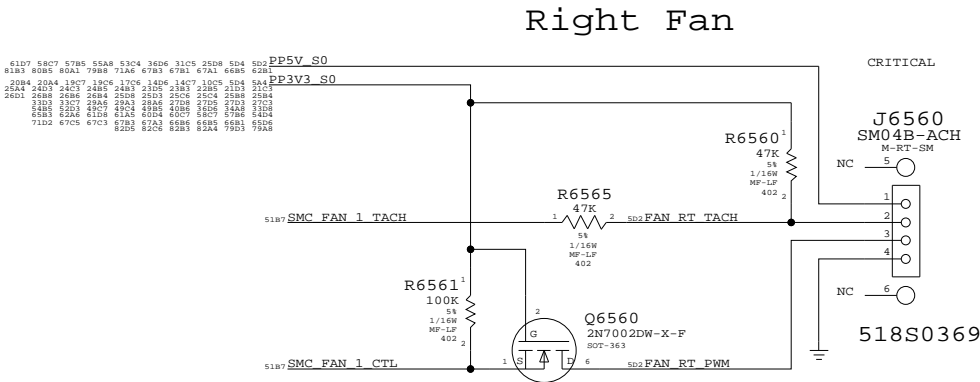
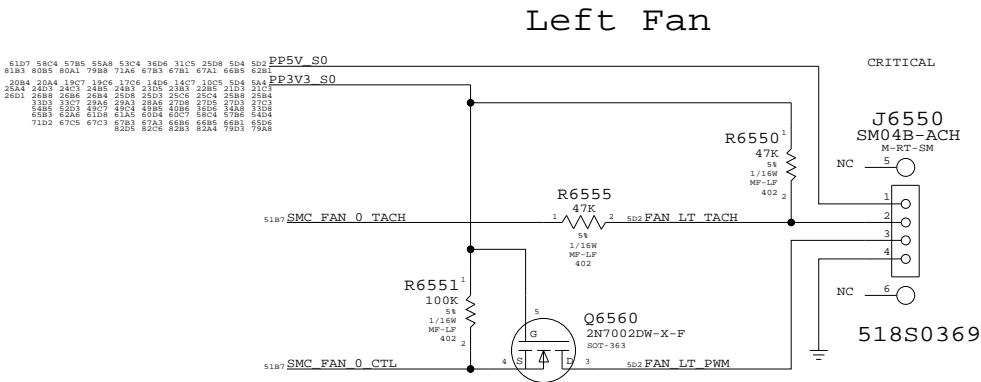
NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



Fan Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SCALE
NONE

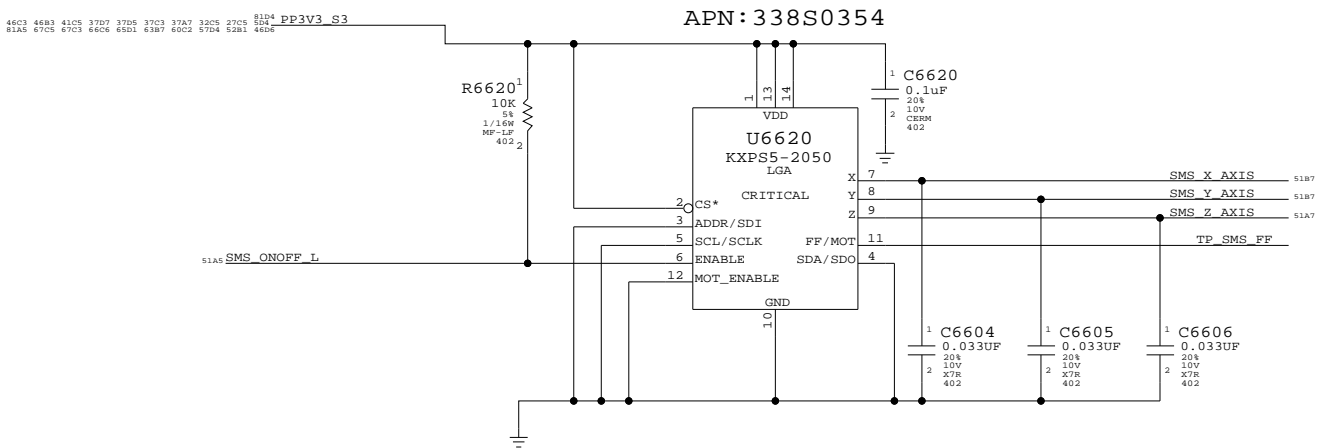
D

DRAWING NUMBER
051-7164

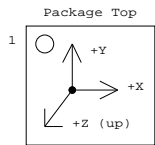
SHT
58

REV.
06004

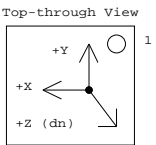
OF
87



Desired orientation when
placed on board top-side:



Desired orientation when
placed on board bottom-side:



M59 placement: Bottom-side

Sudden Motion Sensor (SMS)

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY
PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR
AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT


III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

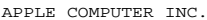


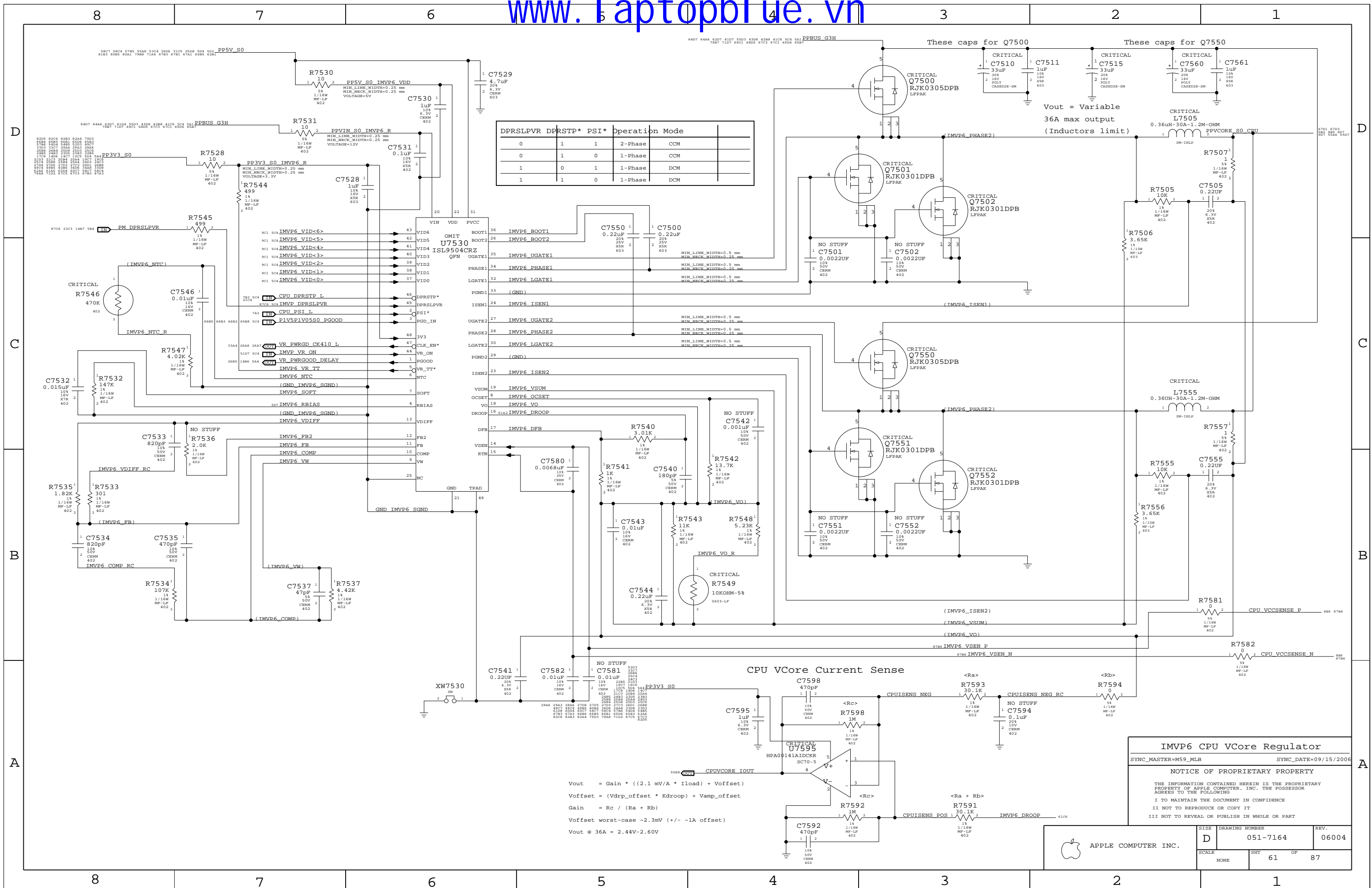
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004
SCALE NONE	SHT 59	OF 87

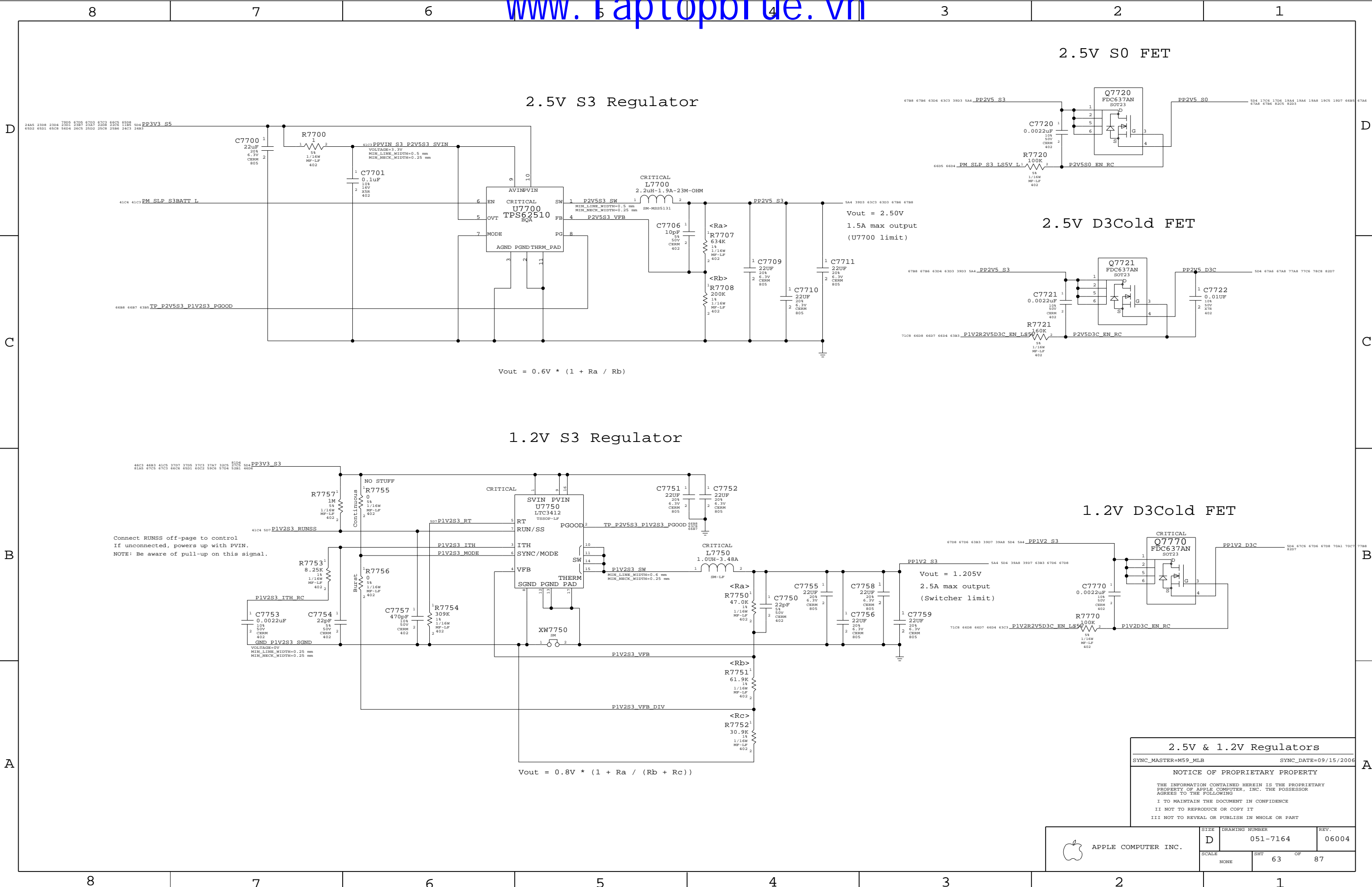


 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7164	06004
	SCALE	SHT	OF
	NONE	60	87









Connect RUNSS off-page to control
If unconnected, powers up with PVIN.
NOTE: Be aware of pull-up on this signal.

2.5V & 1.2V Regulators

SYNC_MASTER=M59_MLB

SYNC_DATE=09/15/2006


NOTICE OF PROPRIETARY PROPERTY

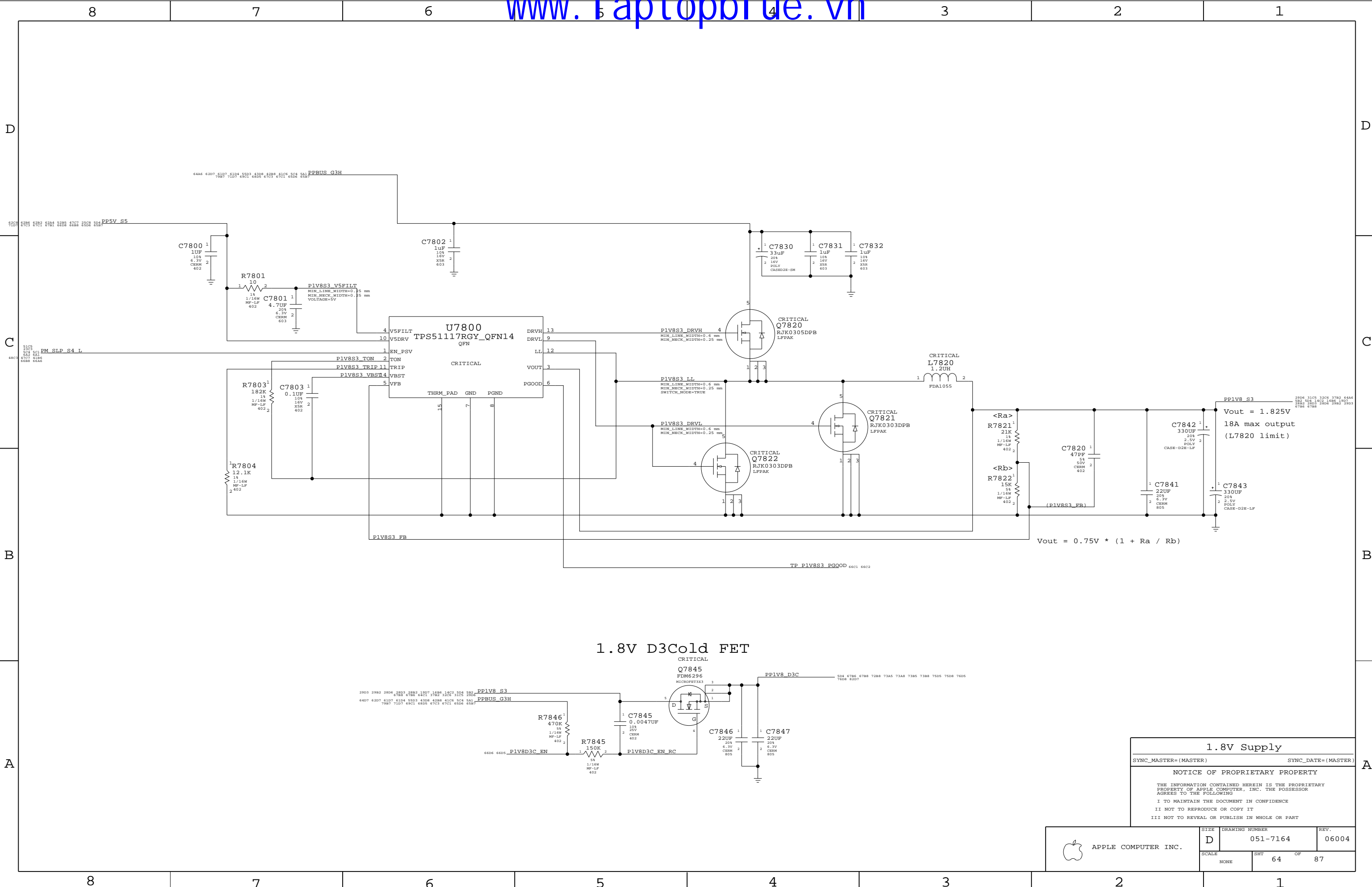
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7164	REV. 06004
	SCALE NONE	SHT 63	OF 87



1.8V D3Cold FET

1.8V Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

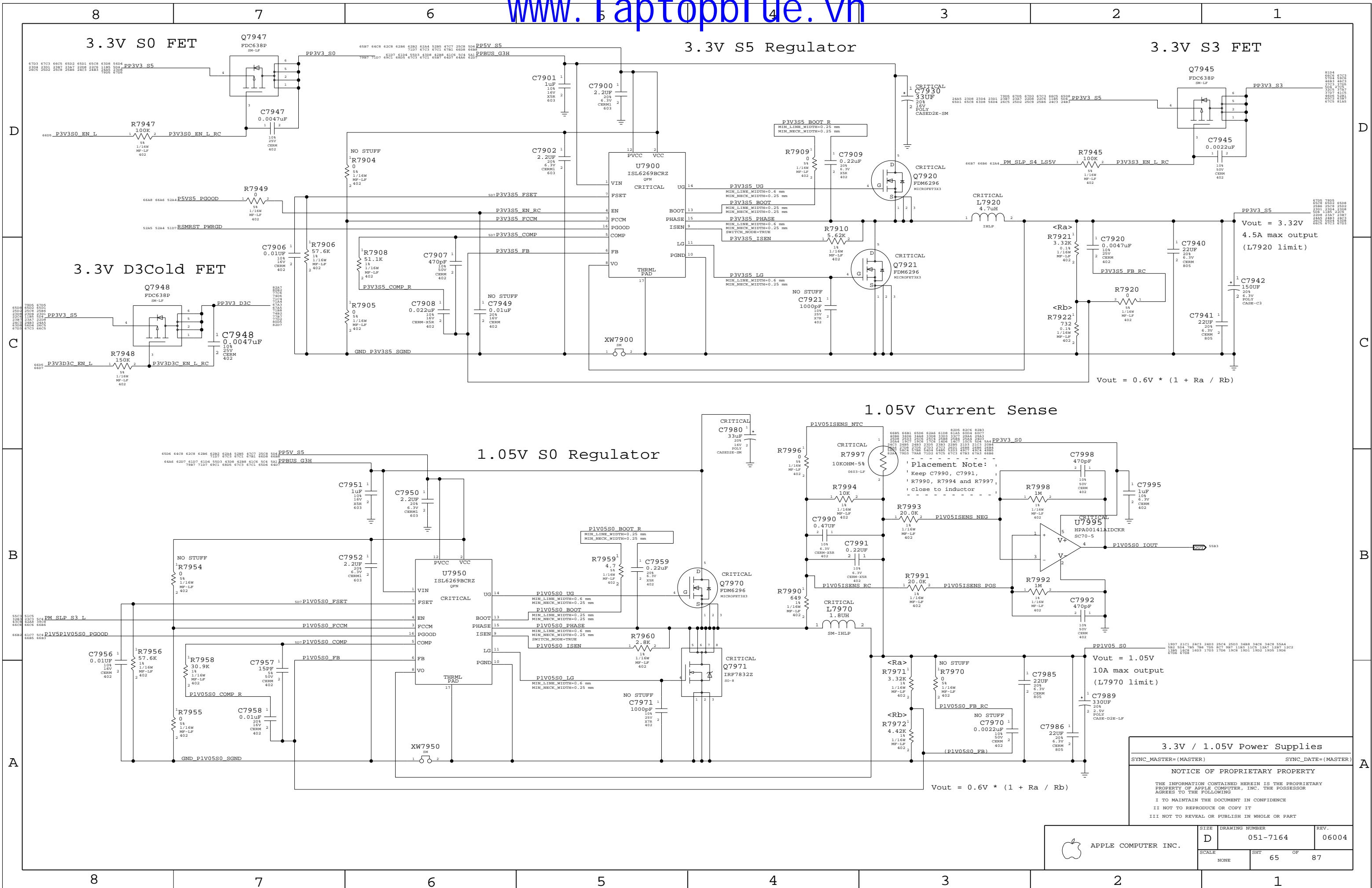
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7164	06004
SCALE		SHT	OF
NONE		64	87



Power Control Signals

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

D

D

C

C

B

B

A

A

1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation

Unused PGOOD Signals

66C1 62B1 TP P5V P1V5 PGOOD	TP P5V P1V5 PGOOD	62B1 66C2
66C1 64B4 TP P1V8S3 PGOOD	TP P1V8S3 PGOOD	64B4 66C2
	MAKE_BASE=TRUE	

Other S0 Rails PWRGD Circuit

Does not include D3C rails for GPU!!

3.3V G3Hot Supply & Power Control

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

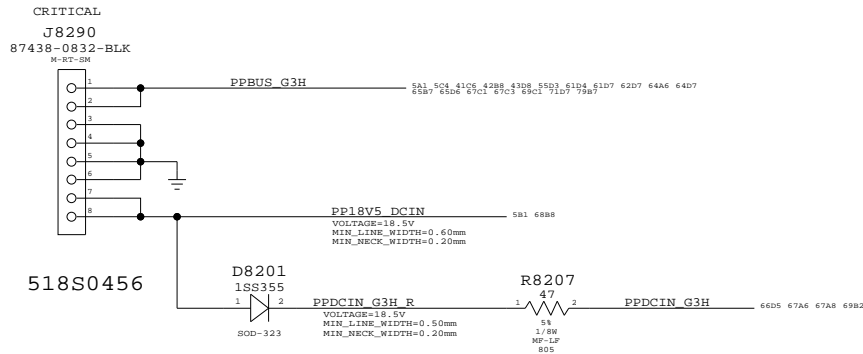
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



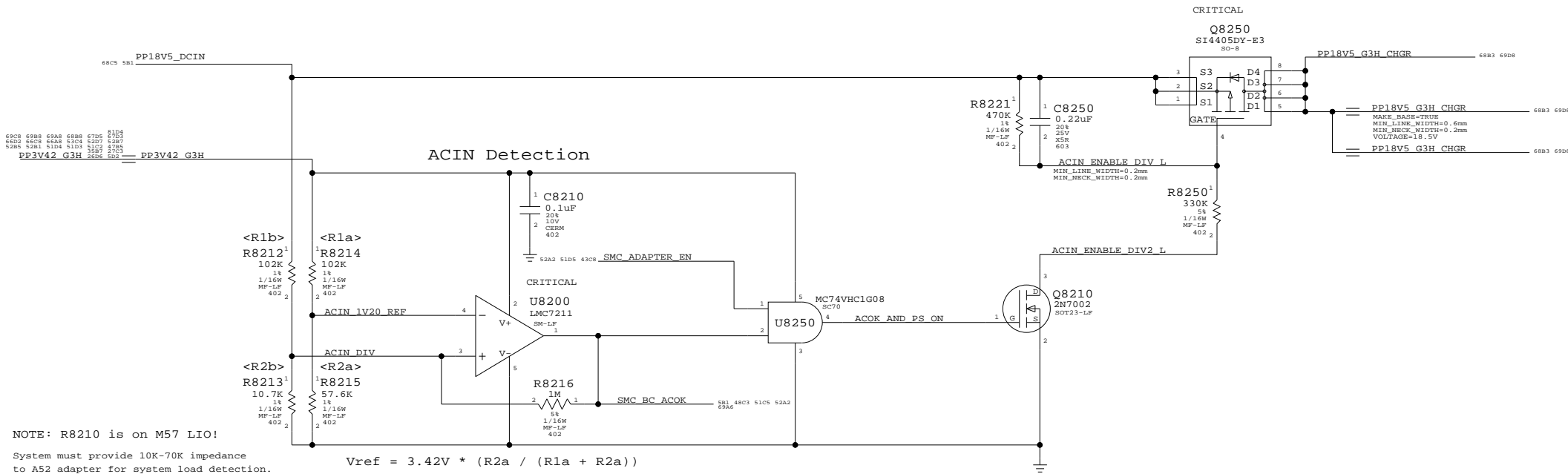
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004
SCALE	SHT	OF
NONE	66	87

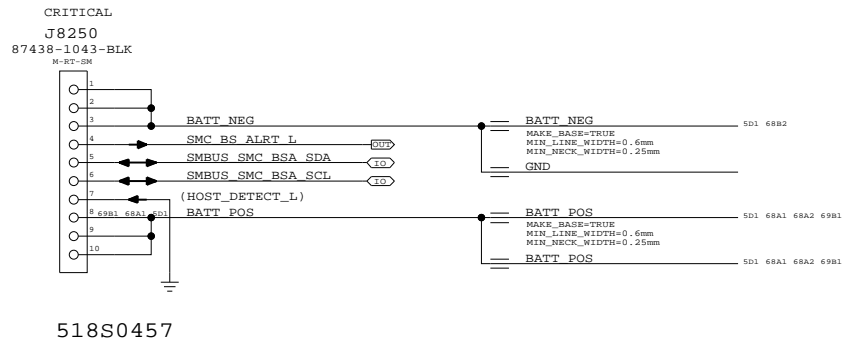
DC-In Connector



Inrush Limiter



Battery Connector



NOTE: R8210 is on M57 LIO!

System must provide 10K-70K impedance to A52 adapter for system load detection. REQ of R8210 (on M57 LIO), R8212, & R8213 is 36.9K. Vth = (Vref / (R2b / (R1b + R2b)))

Vref = 3.42V * (R2a / (R1a + R2a))

Vref = 1.23V

Vth = 13.0V

Assuming 1% variance for R8210-R8215 and 3.42V: Worst case Vth: min:12.47V, max: 13.54V

DC-In & Battery Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

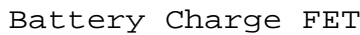
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

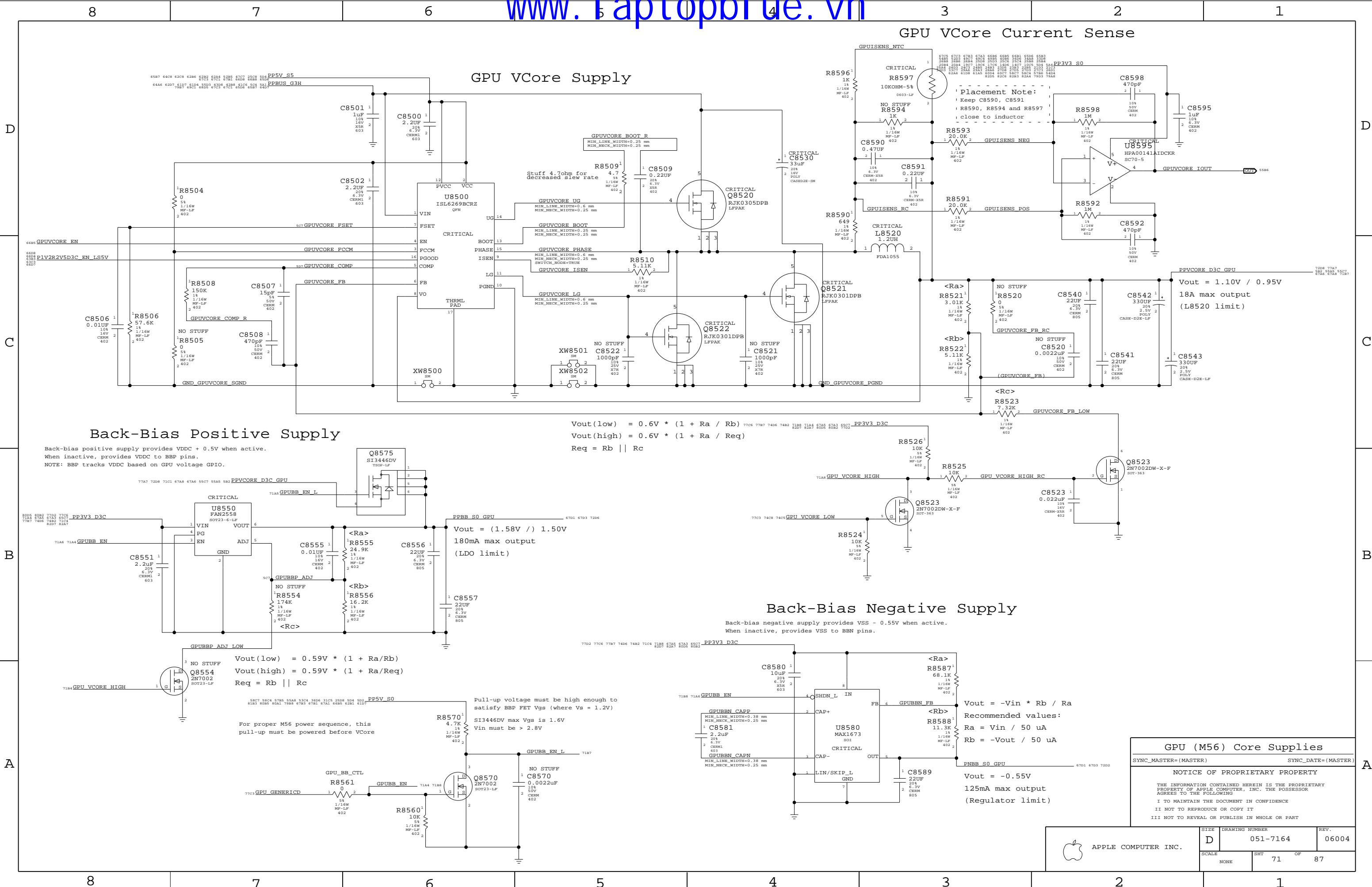


APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004
SCALE	SHT	OF
NONE	68	87



PBus Supply & Batt. Charger	
SYNC_MASTER=MS9_LIO	SYNC_DATE=09/15/2006
NOTICE OF PROPRIETARY PROPERTY	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING	
I 1 TO MAINTAIN THE DOCUMENT IN CONFIDENCE	
I 1 NOT TO REPRODUCE OR COPY IT	
I 11 NOT TO REVEAL OR PUBLISH IN WHOLE OR PART	

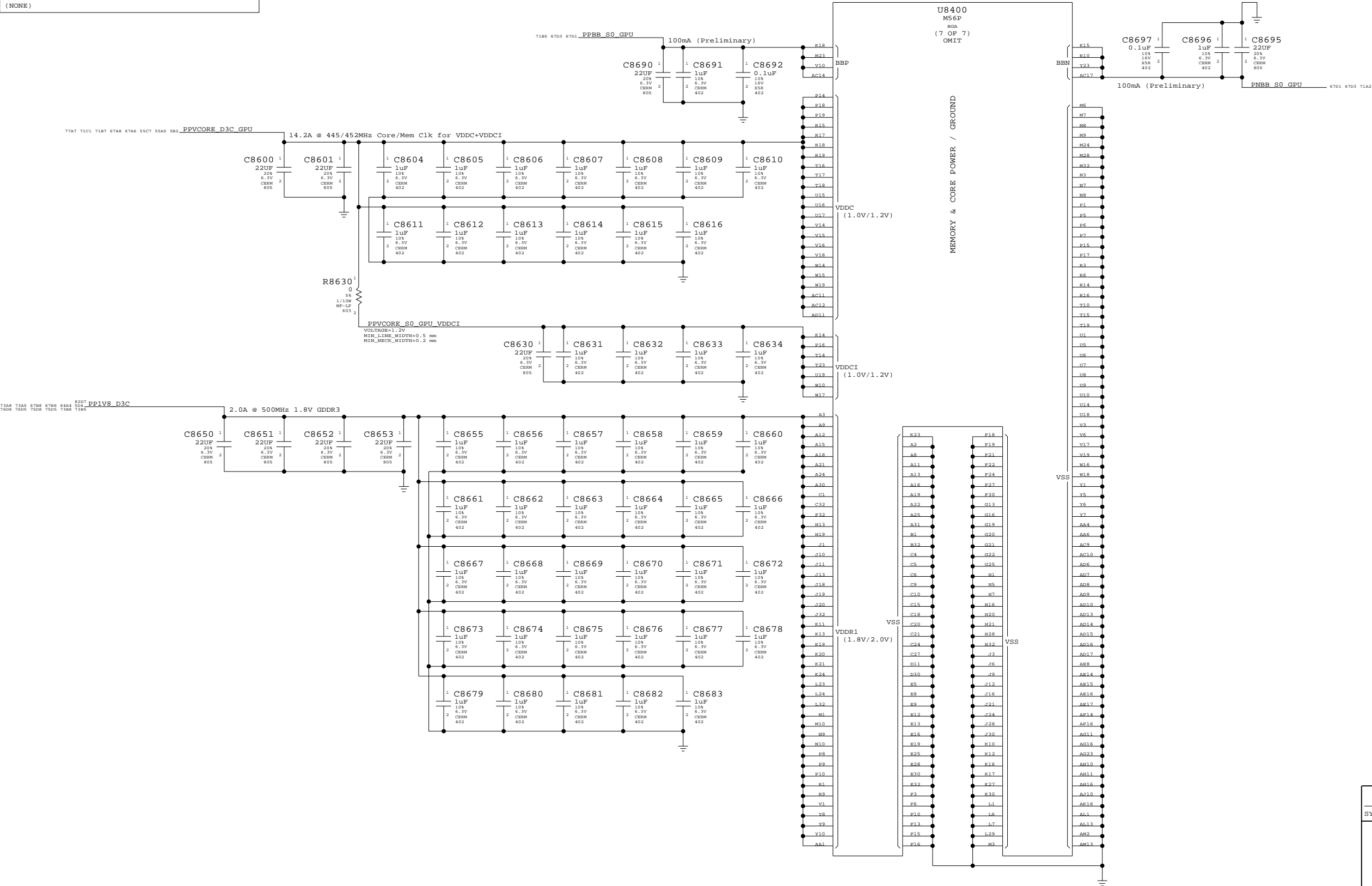


Page Notes

Power aliases required by this page:
- =PP1V5_GPU_VDD15
- =PP1VR1V3_GPU_VCORE

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



ATI M56 Core Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE COMPUTER INC.

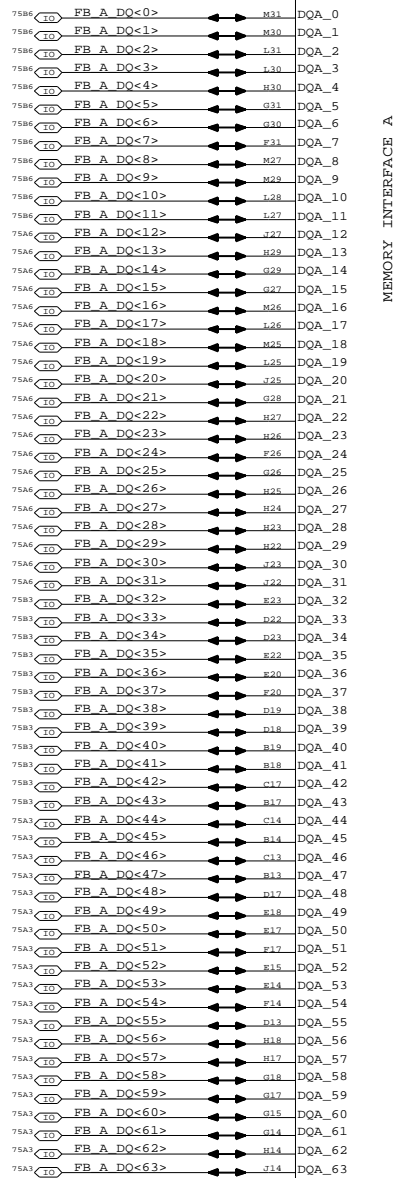
SIZE	DRAWING NUMBER	REV.
D	051-7164	06004
SCALE	SHT	OF
NONE	72	87

Page Notes

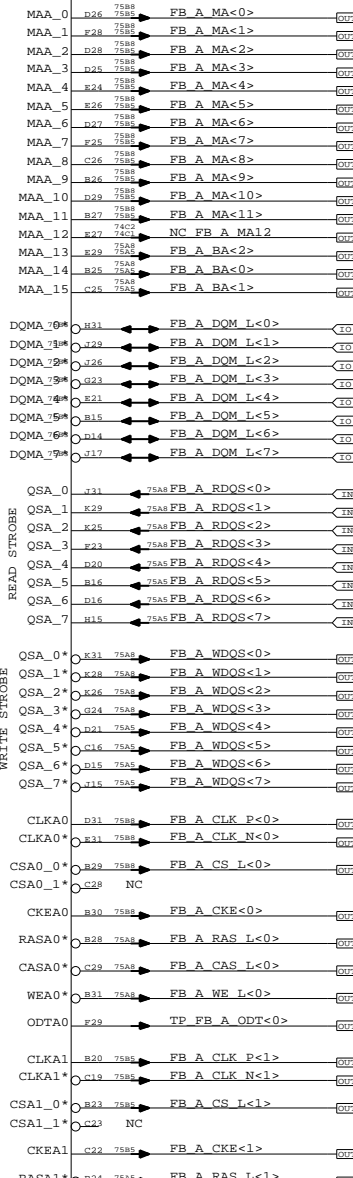
Power aliases required by this page:
- =PPIV8R2V0_S0_FB_GPU

Signal aliases required by this page:
(NONE)

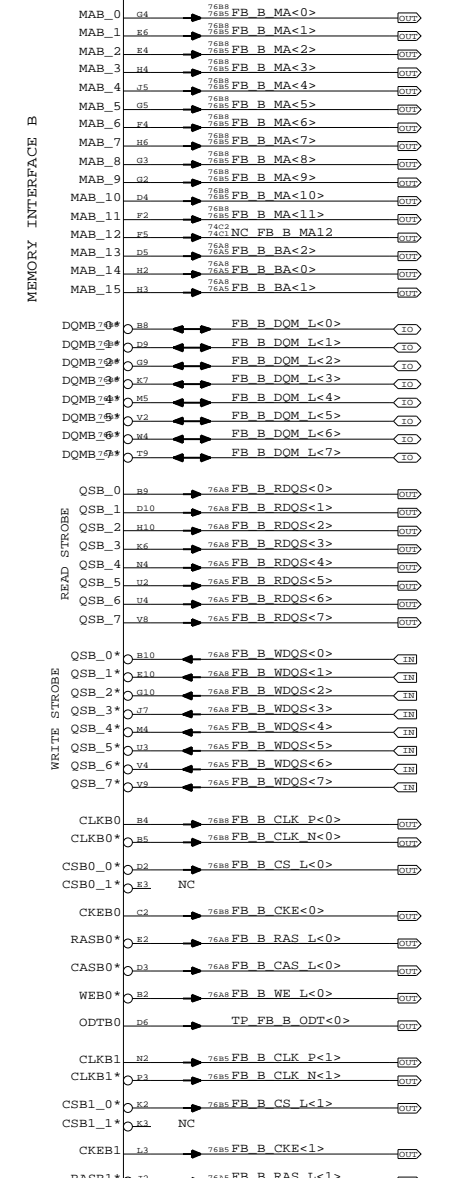
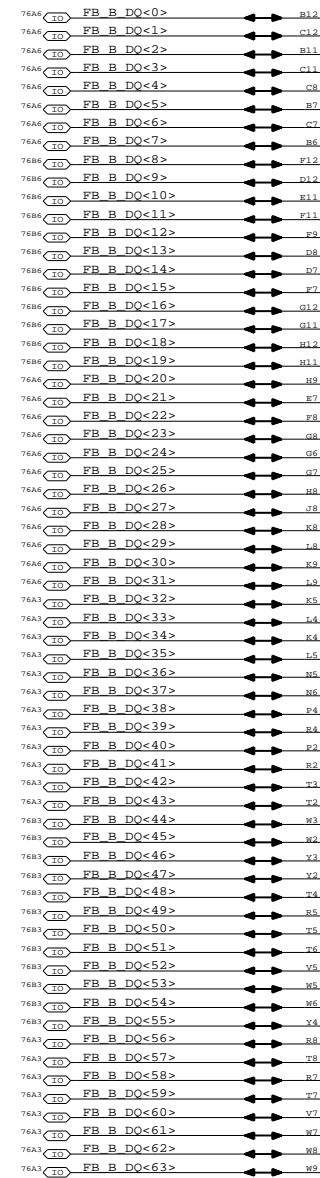
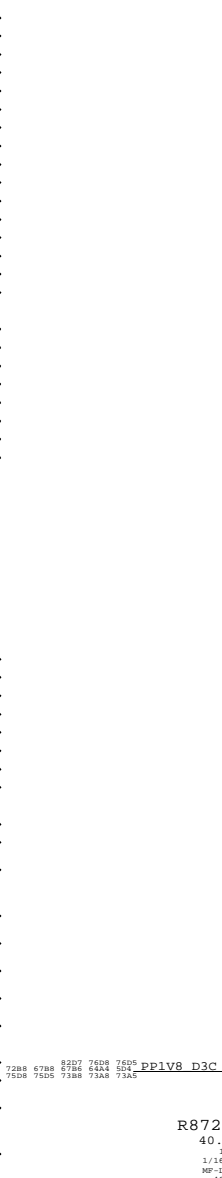
BOM options provided by this page:
(NONE)



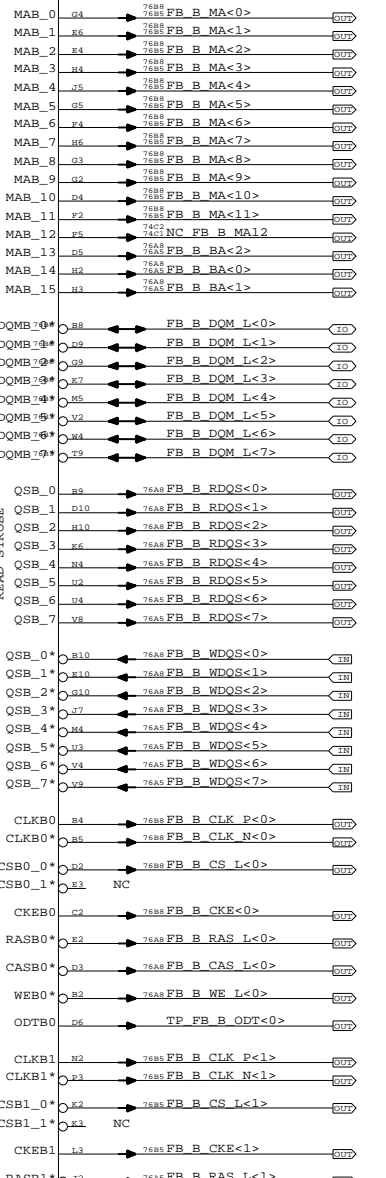
MEMORY INTERFACE A



READ STROBE
WRITE STROBE



MEMORY INTERFACE B



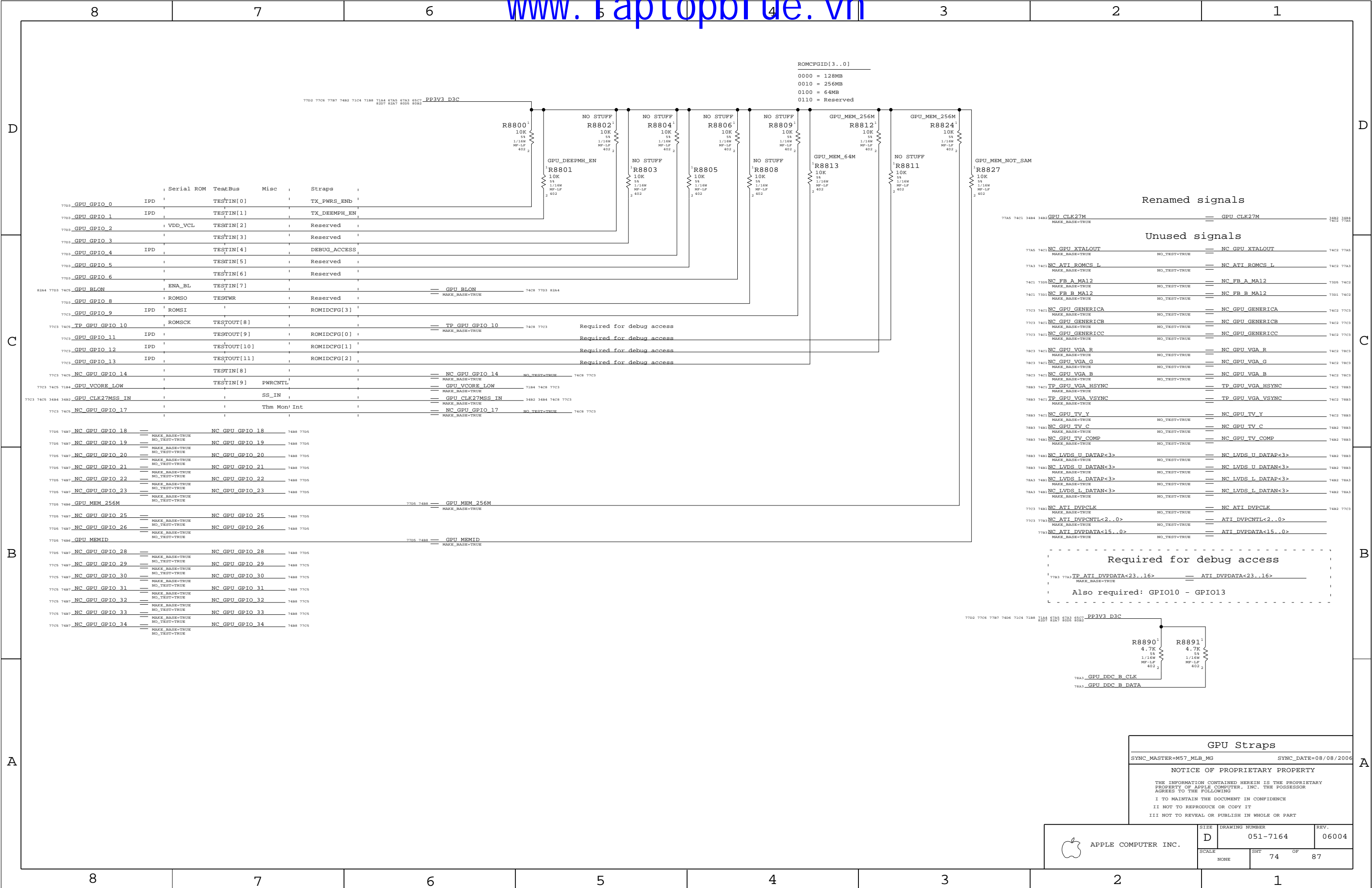
ATI M56 Frame Buffer I/F

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7164	06004
SCALE		SHT	73 OF 87
NONE			

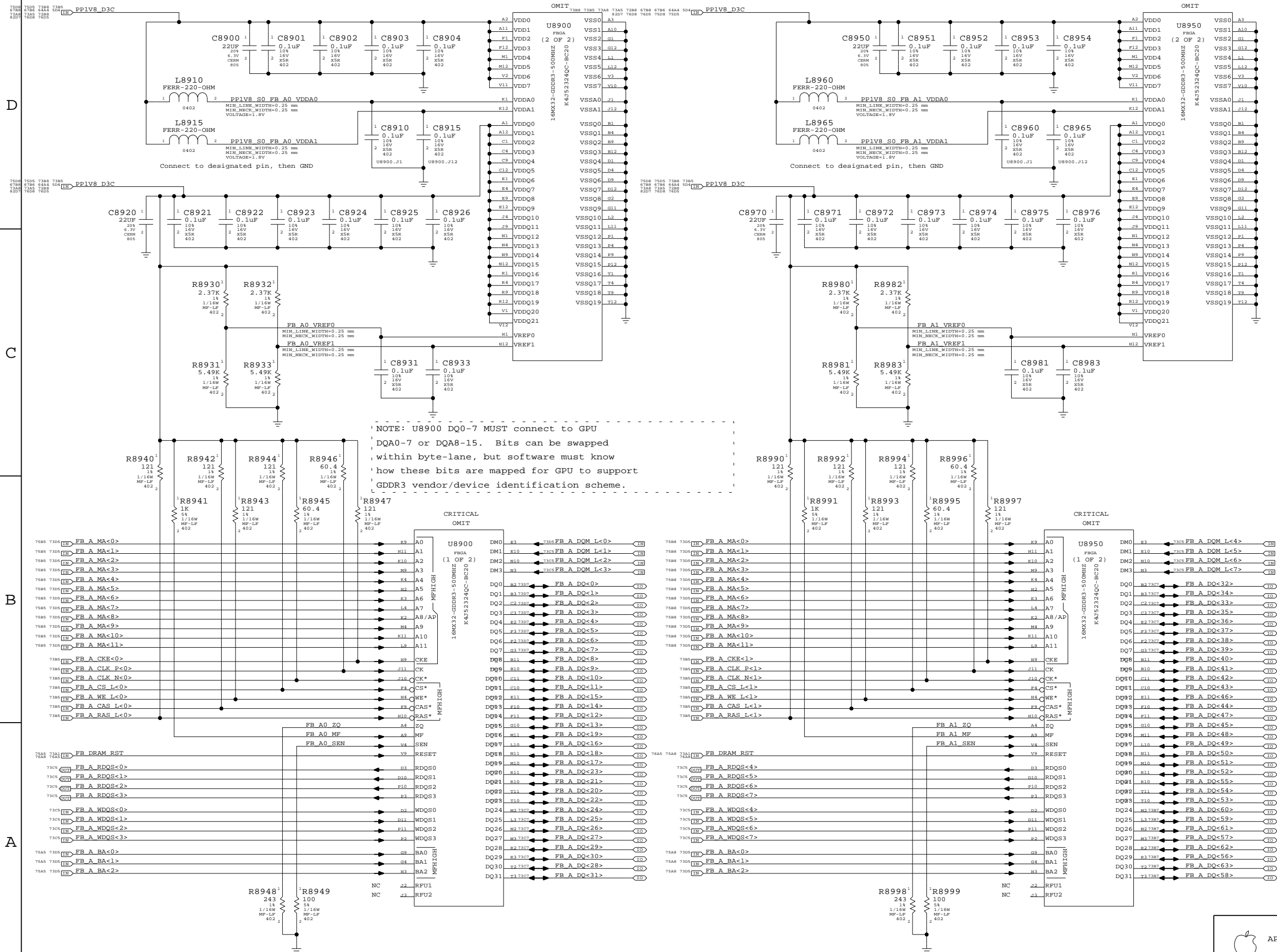


Power aliases required by this page:

```
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ
```

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



GDDR3 Frame Buffer A

SYNC_MASTER= (MASTER)	SYNC_DATE= (MASTER)
-------------------------	-----------------------

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
------	----------------	------

D	051-7164	06004
---	----------	-------

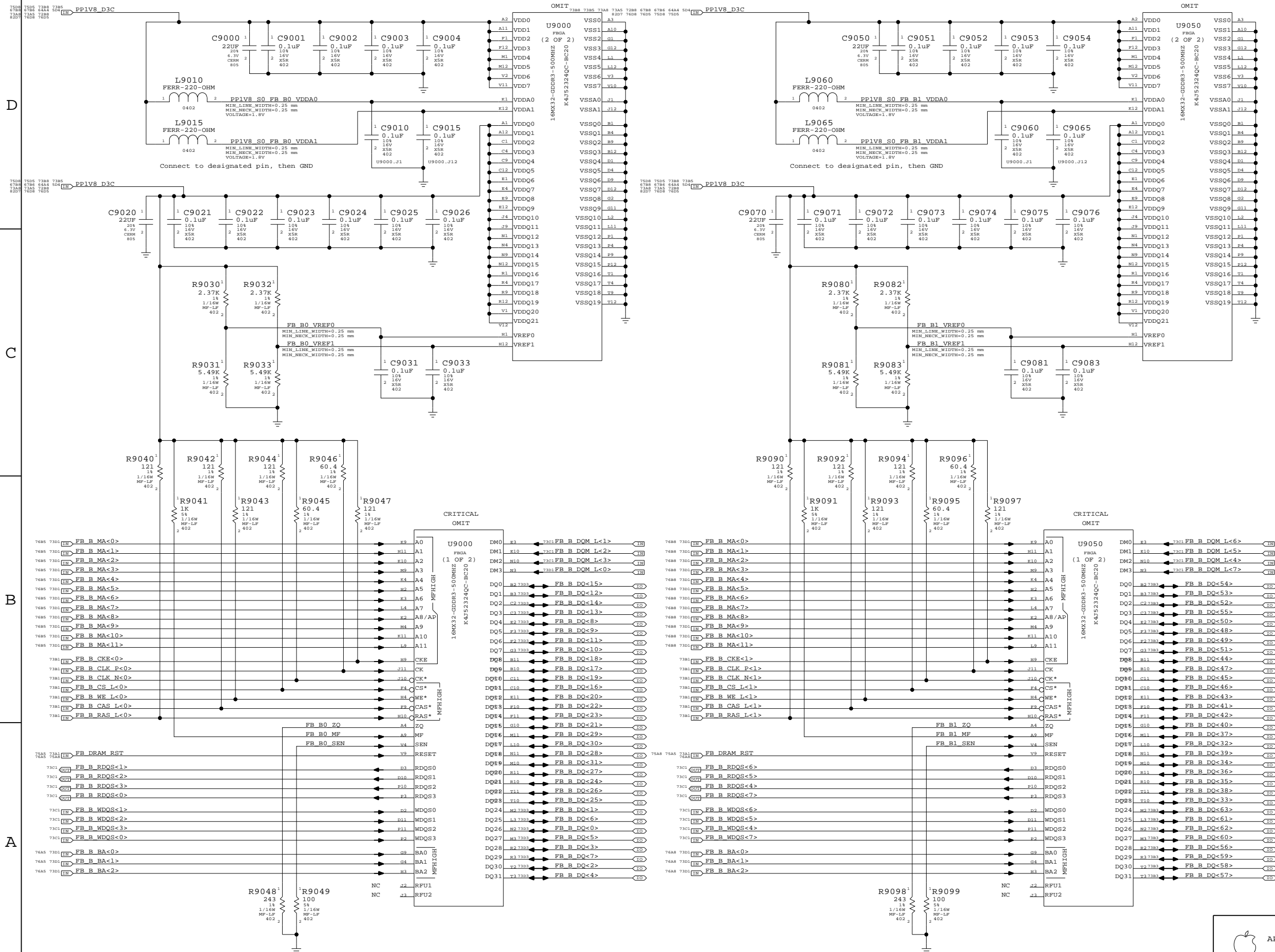
D	991 7101	99991
---	----------	-------

SCALE	SHT	OF
-------	-----	----

Power aliases required by this page:
- =PPIV8_S0_FB_VDD
- =PPIV8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



GDDR3 Frame Buffer B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

- I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
- II NOT TO REPRODUCE OR COPY IT
- III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004
SCALE	SHT	OF
NONE	76	87

Page Notes

Power aliases required by this page:

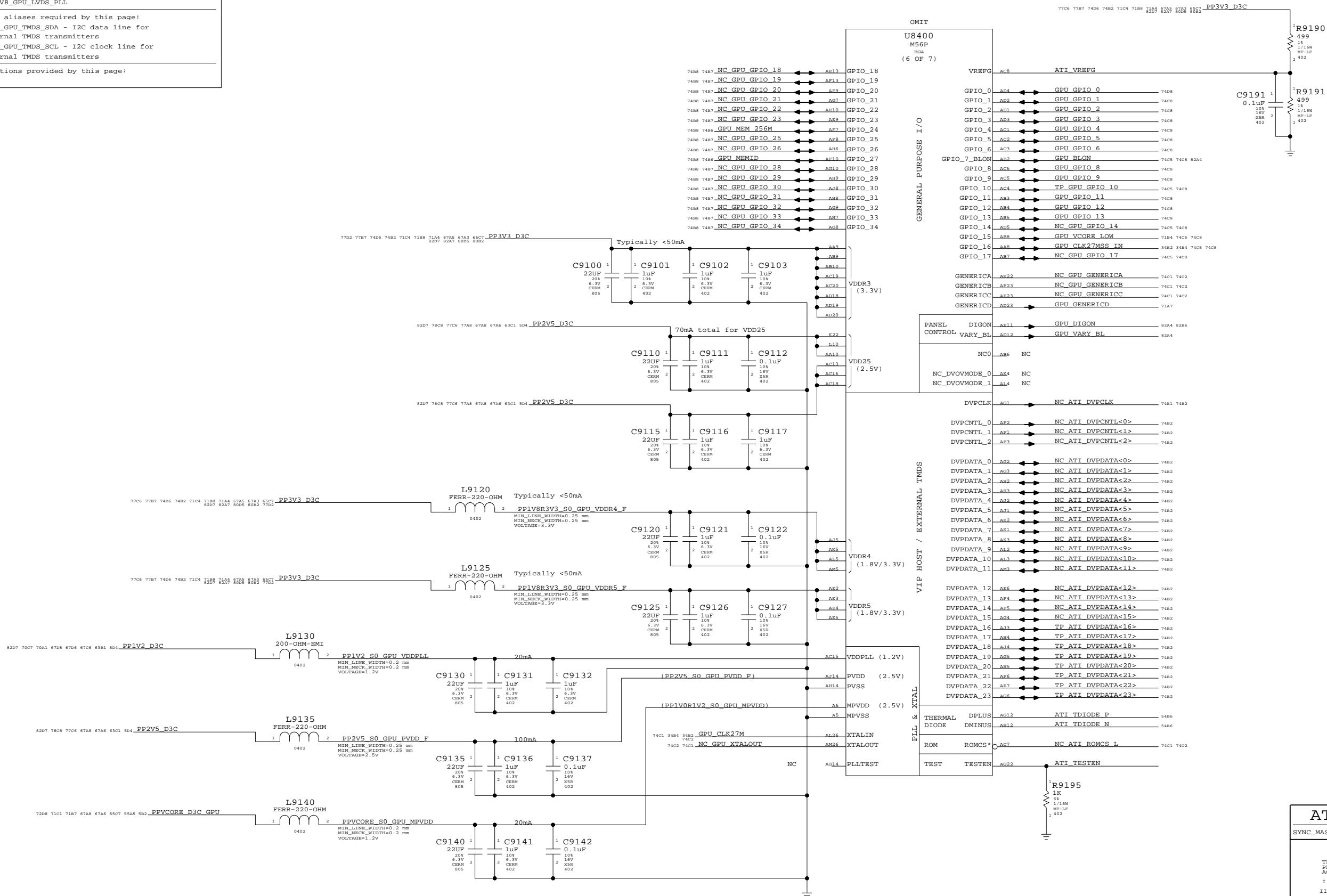
- =PP3V3_GPU_GPIOS
- =PP2V5_PVDD
- =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:

- =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
- =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:

(NONE)



ATI M56 GPIO/DVO/Misc

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE COMPUTER INC.

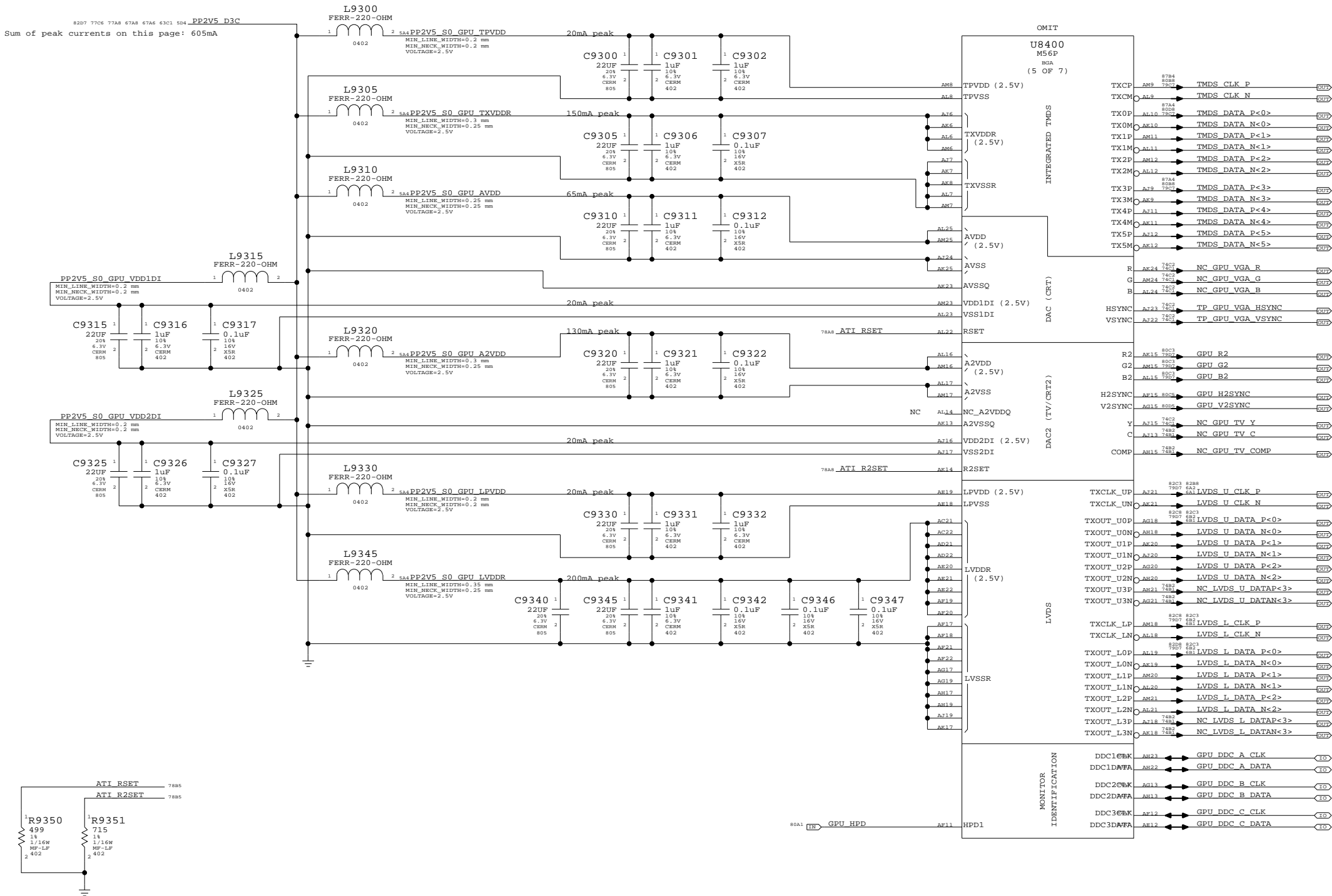
SIZE	DRAWING NUMBER	REV.
D	051-7164	06004
SCALE	SHT	OF
NONE	77	87

Page Notes

Power aliases required by this page:
- =PP2V5_S0_GPU
- =PP1V8R2V5_S0_GPU_LVDDR

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



ATI M56 Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

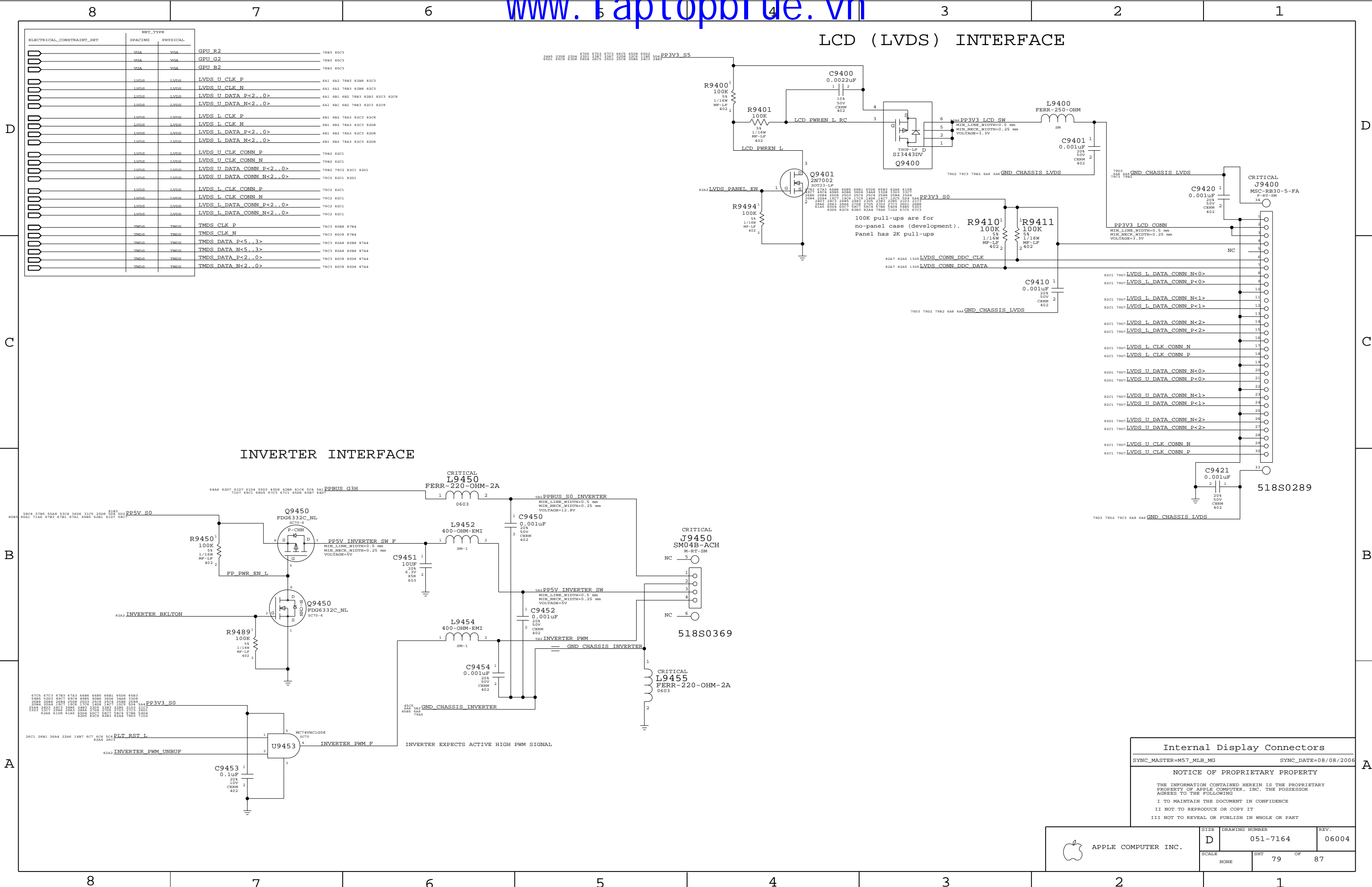
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

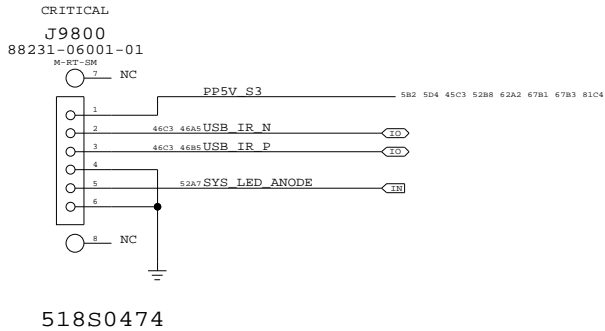


APPLE COMPUTER INC.

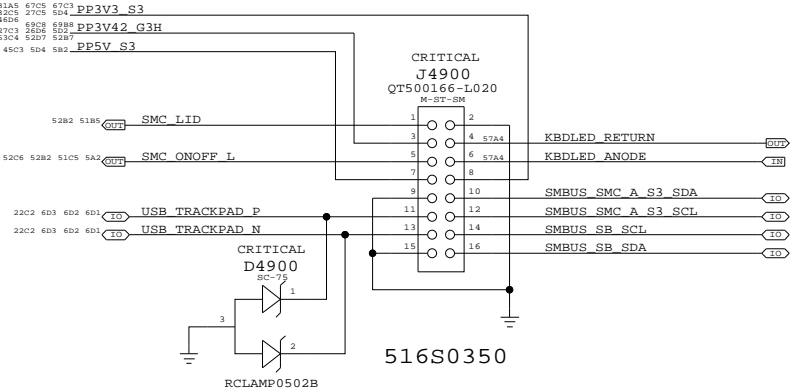
SIZE	DRAWING NUMBER	REV.
D	051-7164	06004
SCALE	SHT	OF
NONE	78	87



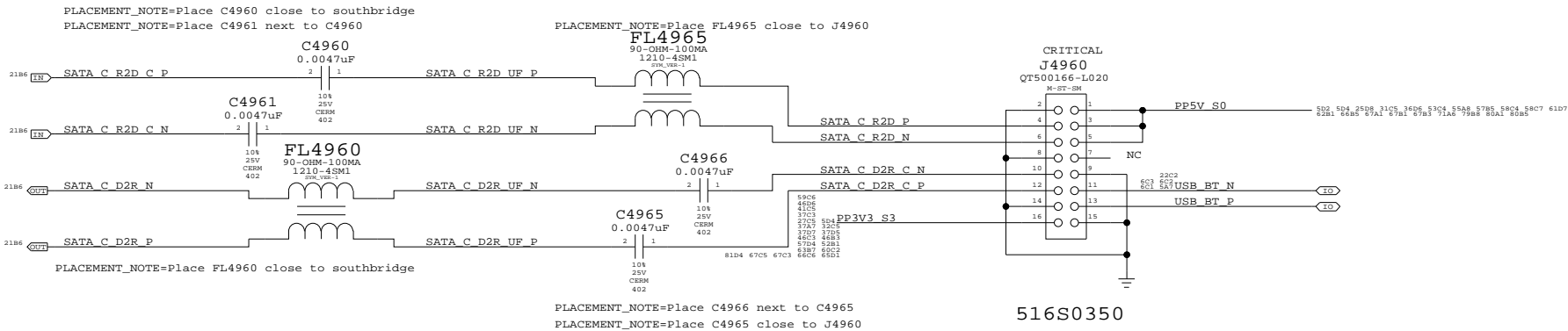
IR & Sleep LED Connector



Top-Case Connector



Bluetooth (M13P) & SATA HDD Flex Connector



M57 SPECIFIC CONNECTORS

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE COMPUTER INC.

SIZE

D

DRAWING NUMBER

051-7164

REV.

06004

SCALE

NONE

SHT

81

OF

87

LVDS Interface Pull-downs

NOTE: These parts are to counter an invalid state caused by the M56 part. Bias voltage is present on LVDS interface pins even when they should be tri-stated to meet panel power sequence requirements. Resulting pump-up in LCD panel can cause startup and long-term reliability issues. Pull-down resistors reduce the pump-up in the panel, though some voltage will still be seen on LVDS signals when they should be 0V.

PGOOD Monitor for GPU Rails

D3CPGOOD_ALL BOM option stuffs LTC2903 circuit to monitor all D3C rails to qualify D3CPGOOD.
D3CPGOOD_3V3 BOM option uses only PP3V3_D3C to qualify D3CPGOOD.

LVDS I/F Mux

NB LVDS I/F

GPU LVDS I/F

LVDS Mux Selection Qualification

Enables the GPU LVDS path in the mux with the qualification that the GPU has turned on panel power and that the panel power has risen to (near) 3.3V. This should eliminate need for LVDS pulldowns

Panel/Backlight Control Mux

GPU DDC Pass FETs

LVDS Interface Pull-downs

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE COMPUTER INC.

SIZE D DRAWING NUMBER 051-7164 REV. 06004

SCALE NONE SHT 82 OF 87

D

D

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR	*	=3:1_SPACING	?
FSB_ADDR2ADDR	*	=2:1_SPACING	?
FSB_ADSTB	*	=3:1_SPACING	?
FSB_ADDR2ADSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=3:1_SPACING	?
FSB_DATA2DATA	*	=2:1_SPACING	?
FSB_DSTB	*	=3:1_SPACING	?
FSB_DATA2DSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_COMMON	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended.
Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs.
Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs.
DSTB complementary pairs are spaced 3:1, even in constraint areas.
Design Guide recommends each strobe/signal group is routed on the same layer.
Design Guide recommends FSB signals be routed only on internal layers.
NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.
NOTE: Design Guide allows closer spacing if signal lengths can be shortened.
SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 4.2 & 4.3

C

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_2T01	*	=2:1_SPACING	?
CPU_COMP	*	25 MIL	?
CPU_OTL&REF	*	25 MIL	?
CPU_1TP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.
SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 4.4, 4.6.2, & 5.8.2.4

DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	Y	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	Y	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_85D	*	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=3:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

Need to support MEM_*-style wildcards!

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 6.2

PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	20 MIL	?
DMI	*	20 MIL	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 7.2, 9.2 & 10.5.2

Disk Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IDE_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
IDE	*	=1.8:1_SPACING	?
SATA	*	20 MIL	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 10.6 & 10.7.2

Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIO_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	=1.8:1_SPACING	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB2_90D	*	Y	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB2	*	=4:1_SPACING	?
USB2_2CLK	*	25 MIL	?

DG says minimum spacing 50 mils to clocks

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.10.1.2

Internal Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=3:1_SPACING	?
SPI	*	=1.8:1_SPACING	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.17.1.1

Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	25 MIL	?
CLK_PCIE	*	20 MIL	?
CLK_MED	*	20 MIL	?
CLK_SLOW	*	10 MIL	?

A

A

Napa Platform Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE COMPUTER INC.

SIZE

D

DRAWING NUMBER

051-7164

REV.

06004

SCALE

NONE

SHT

84

OF

87

D

D

GDDR3 (Frame Buffer) Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
FB_35S_TO_55S	*	Y	=35_OHM_SE	=55_OHM_SE	=35_55_OHM_SE	=STANDARD	=STANDARD
FB_40S	*	Y	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
FB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FB_75D	*	Y	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
FB_ADCTRL	*	=2.5:1_SPACING	?
FB_CLK	*	=2.5:1_SPACING	?
FB_DATA	*	=2.5:1_SPACING	?

ADDR/CTRL lines should route 35-ohms to T, then 55-ohms to each VRAM device.
CTRL lines are 55-ohm single-ended impedance.
DQ/DQM/DQS lines are 40-ohm single-ended impedance.

NOTE: CLK lines are specified in Layout Guide as 40-ohm single-ended. We treat as 75-ohm differential.
NOTE: Layout Guide does not specify LVDS/TMDS spacing to other traces other than "do not run close"
SOURCE: ATI Layout Guide, Rev 0.5 (DSG-216MOBRADEON-05), Sections 7 & 8.1.2.

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
LVDS_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
TMDS_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
VGA_75S	*	Y	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
LVDS	*	=3:1_SPACING	?
TMDS	*	=3:1_SPACING	?
VGA	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
LVDS_PAIR2PAIR	*	25 MIL	?
TMDS_PAIR2PAIR	*	25 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	LVDS	*	LVDS_PAIR2PAIR
TMDS	TMDS	*	TMDS_PAIR2PAIR

LVDS and TMDS signals are 100-ohm +/- 10% differential impedance.
LVDS and TMDS pairs should be kept at least 25 mils apart.
Ground shields can be used around each pair if spacing cannot be met.
VGA should be routed as close to 75-ohms single-ended impedance as possible.
VGA signals should be kept at least 15 mils from other traces.
Ground shields recommended around VGA signals.

NOTE: Layout Guide does not specify LVDS/TMDS spacing to other traces other than "do not run close"
SOURCE: ATI Layout Guide, Rev 0.5 (DSG-216MOBRADEON-05), Sections 7 & 8.1.2.

B

B

A

A

High-Speed I/O Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
ENET_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
FW_110D	*	Y	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
ENET	*	=3:1_SPACING	?
FW	*	=3:1_SPACING	?

note

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
PCI_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
PCI	*	=2:1_SPACING	?

More System Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE COMPUTER INC.

SIZE	D	DRAWING NUMBER	051-7164	REV.	06004
SCALE	NONE	SHT	85	OF	87

	8	7	6	5	4	3	2	1
D	M9 Board-Specific Spacing & Physical Constraints							
	BOARD LAYERS				BOARD AREAS		BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
	TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM				NO_TYPE, BGA		MM	15.2
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	DEFAULT	*	Y	=55_OHM_SE	=55_OHM_SE	30 MM	0 MM	0 MM
	STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	55_OHM_SE	TOP, BOTTOM	Y	0.100 MM	0.100 MM			
	55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
C	50_OHM_SE	TOP, BOTTOM	Y	0.124 MM	0.124 MM			
	50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	45_OHM_SE	TOP, BOTTOM	Y	0.150 MM	0.150 MM			
	45_OHM_SE	*	Y	0.105 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	40_OHM_SE	TOP, BOTTOM	Y	0.185 MM	0.185 MM			
	40_OHM_SE	*	Y	0.131 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	35_OHM_SE	TOP, BOTTOM	Y	0.230 MM	0.230 MM			
	35_OHM_SE	*	Y	0.165 MM	0.165 MM	=STANDARD	=STANDARD	=STANDARD
B	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	27P4_OHM_SE	TOP, BOTTOM	Y	0.335 MM	0.335 MM			
	27P4_OHM_SE	*	Y	0.240 MM	0.240 MM	=STANDARD	=STANDARD	=STANDARD
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	35_55_OHM_SE	TOP, BOTTOM	Y	0.230 MM	0.100 MM			
	35_55_OHM_SE	*	Y	0.165 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD
	Unsupported rule							
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	75_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
A	70_OHM_DIFF	*	Y	0.149 MM	0.149 MM	=STANDARD	0.125 MM	0.125 MM
	70_OHM_DIFF	TOP, BOTTOM	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	75_OHM_DIFF	*	Y	0.131 MM	0.131 MM	=STANDARD	0.125 MM	0.125 MM
	75_OHM_DIFF	TOP, BOTTOM	Y	0.161 MM	0.161 MM		0.125 MM	0.125 MM
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	80_OHM_DIFF	*	Y	0.115 MM	0.111 MM	=STANDARD	0.125 MM	0.125 MM
	80_OHM_DIFF	TOP, BOTTOM	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	85_OHM_DIFF	*	Y	0.101 MM	0.101 MM	=STANDARD	0.125 MM	0.125 MM
	85_OHM_DIFF	TOP, BOTTOM	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	90_OHM_DIFF	*	Y	0.102 MM	0.102 MM	=STANDARD	0.220 MM	0.220 MM
	90_OHM_DIFF	TOP, BOTTOM	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	100_OHM_DIFF	*	Y	0.080 MM	0.080 MM	=STANDARD	0.200 MM	0.200 MM
	100_OHM_DIFF	TOP, BOTTOM	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	110_OHM_DIFF	*	Y	0.077 MM	0.077 MM	=STANDARD	0.330 MM	0.330 MM
	110_OHM_DIFF	TOP, BOTTOM	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM
	8	7	6	5	4	3	2	1

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_MED	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FB_CLK	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

Allow 0.1 MM on blind-to-buried via dogbones (layers 2 & 11)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	ISL2, ISL11	0.1 MM	?
1.8:1_SPACING	ISL2, ISL11	0.1 MM	?
2:1_SPACING	ISL2, ISL11	0.1 MM	?
2.5:1_SPACING	ISL2, ISL11	0.1 MM	?
3:1_SPACING	ISL2, ISL11	0.1 MM	?
4:1_SPACING	ISL2, ISL11	0.1 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	ISL2, ISL11	0.1 MM	?
CLK_PCIE	ISL2, ISL11	0.1 MM	?
CLK_MED	ISL2, ISL11	0.1 MM	?
CLK_SLOW	ISL2, ISL11	0.1 MM	?
CPU_COMP	ISL2, ISL11	0.1 MM	?
CPU_OTLREF	ISL2, ISL11	0.1 MM	?
CPU_VCCSENSE	ISL2, ISL11	0.1 MM	?
DMI	ISL2, ISL11	0.1 MM	?
LVDS_PAIR2PAIR	ISL2, ISL11	0.1 MM	?
MEM_2OTHER	ISL2, ISL11	0.1 MM	?
PCIE	ISL2, ISL11	0.1 MM	?
SATA	ISL2, ISL11	0.1 MM	?
TMDS_PAIR2PAIR	ISL2, ISL11	0.1 MM	?
VGA	ISL2, ISL11	0.1 MM	?

Rules for "Topology #3" for FSB signals, Napa DG tables 4-7 & 4-12.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE
FSB_ADDR2ADDR OVERRIDE	* OVERRIDE	=STANDARD OVERRIDE	? OVERRIDE
FSB_ADSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE
FSB_ADDR2ADSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE
FSB_DATA2DATA OVERRIDE	* OVERRIDE	=STANDARD OVERRIDE	? OVERRIDE
FSB_DSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE
FSB_DATA2DSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS	*	LVDS_100D
TMDS	*	TMDS_100D
TMDSCONN	*	TMDS_100D
VGA	*	VGA_75S

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_2OTHER OVERRIDE	* OVERRIDE	0.5 MM OVERRIDE	? OVERRIDE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI_2PCI OVERRIDE	* OVERRIDE	0.1 MM OVERRIDE	? OVERRIDE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCI	PCI	*	PCI_2PCI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENETCONN	*	*	ENET
TMDSCONN	*	*	TMDS

"Stale" physical / spacing types

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ANALOG	*	*	FSB_COMMON
FSB_P2MM	*	*	FSB_COMMON
I2C	*	*	SMB
GND	*	*	STANDARD
MEM_PP1V8_S3	*	*	STANDARD
FB_PP1V8	*	*	STANDARD

FSB_ANALOG	
FSB_P2MM	
I2C	
GND	
MEM_PP1V8_S3	
FB_PP1V8	
PCI	PCI_55S

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

M9 Spacing & Physical Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE COMPUTER INC.

SIZE D	DRAWING NUMBER 051-7164	REV. 06004
SCALE NONE	SHT 86	OF 87

[illegible]