

SCHEM, MLB, M59

09/19/2006

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
A		463525	PRODUCTION RELEASE	9/19/2006	9/19/2006


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8	CPU 2 OF 2-PWR/GND	(MASTER)
9	CPU Decoupling & VID	(MASTER)
10	CPU MISC1-TEMP SENSOR	(MASTER)
11	CPU ITP700FLEX DEBUG	(MASTER)
12	NB CPU Interface	(MASTER)
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14	NB Misc Interfaces	(MASTER)
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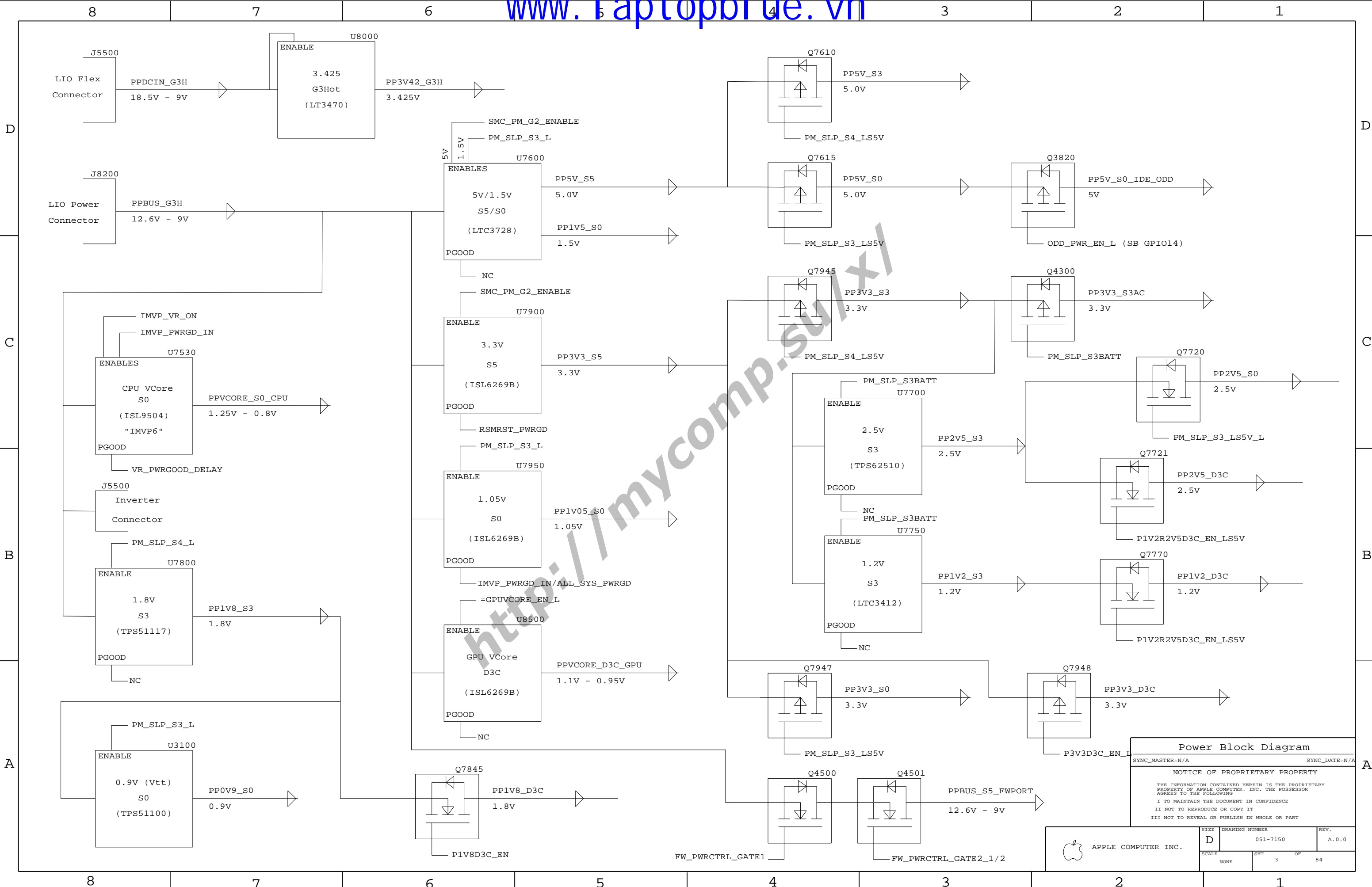
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Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7150	1	SCHEM,MLB,M59	SCH	CRITICAL	
820-2054	1	PCBF,MLB,M59	PCB	CRITICAL	

DRAWING
TITLE=M59_MLB
ABBREV=DRAWING
LAST MODIFIED=Mon Sep 25 10:45:58 2006

DIMENSIONS ARE IN MILLIMETERS XX ± _____ X.XX ± _____ X.XXX ± _____ ANGLES ± _____ DO NOT SCALE DRAWING  THIRD ANGLE PROJECTION	METRIC		Apple Computer Inc.	
	DRAFTER	DESIGN CK	NOTICE OF PROPRIETARY PROPERTY THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING I TO MAINTAIN THE DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART	
	ENG APPD	MFG APPD		
	QA APPD	DESIGNER		
RELEASE	SCALE	TITLE		
MATERIAL/FINISH NOTED AS APPLICABLE		SIZE D	SCHEM,MLB,M59	
		DRAWING NUMBER 051-7150		REV. A.0.0
		SHT 1 OF 84		



Power Block Diagram

SYNC_MASTER=N/A

SYNC_DATE=N/A

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APPLE COMPUTER INC.

SCALE: NONE

SIZE: D

DRAWING NUMBER: 051-7150

SHT: 3 OF 84

REV.: A.0.0

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<div><div>2.16Ghz BOMs</div><table><tr><th>BOM NUMBER</th><th>BOM NAME</th><th>BOM OPTIONS</th></tr><tr><td>630-7849</td><td>PCBA, 2.16GHZ, 128VRAM, M59, MBP15</td><td>EEE_WTE, M59_COMMON, CPU_2_16GHZ, VRAM_SAM128</td></tr></table><div>2.33Ghz BOMs</div><table><tr><th>BOM NUMBER</th><th>BOM NAME</th><th>BOM OPTIONS</th></tr><tr><td>630-7851</td><td>PCBA, 2.33GHZ, 256VRAM, M59, MBP15</td><td>EEE_WTG, M59_COMMON, CPU_2_33GHZ, VRAM_SAM256</td></tr></table><div>Bar Code Label / EEE #'s</div><table><tr><th>PART NUMBER</th><th>QTY</th><th>DESCRIPTION</th><th>REFERENCE DES</th><th>CRITICAL</th><th>BOM OPTION</th></tr><tr><td>826-4393</td><td>1</td><td>LBL, P/N LABEL, PCB, 28MM X 6 MM</td><td>[EEE:WTE]</td><td>CRITICAL</td><td>EEE_WTE</td></tr><tr><td>826-4393</td><td>1</td><td>LBL, P/N LABEL, PCB, 28MM X 6 MM</td><td>[EEE:WTG]</td><td>CRITICAL</td><td>EEE_WTG</td></tr></table></div> <div><div>BOMOPTION Groups</div><table><tr><th>BOM GROUP</th><th>BOM OPTIONS</th></tr><tr><td>M59_COMMON</td><td>ALTERNATE, COMMON, M59_COMMON1, M59_COMMON2, M59_COMMON3</td></tr><tr><td>M59_COMMON1</td><td>BOOTROM_FINAL, ENET_LOWPWR_EN, ENETPWR_S3AC, GPU_BB_CTL, D3CPGOOD_3V3</td></tr><tr><td>M59_COMMON2</td><td>ITP, KBDLED_HAS, LPCPLUS, LVDS_PD, MEMVREF_S3</td></tr><tr><td>M59_COMMON3</td><td>MEMVTT_EN_PU, RTUSB_ESD, SMC_PRGRM, USB_C_OC_PU, USB_D_OC_PU, USB_E_OC_PU</td></tr><tr><td>VRAM_INF128</td><td>GPU_MEM_NOT_SAM, VRAM_128_INFINEON</td></tr><tr><td>VRAM_SAM128</td><td>VRAM_128_SAMSUNG</td></tr><tr><td>VRAM_INF256</td><td>GPU_MEM_256M, GPU_MEM_NOT_SAM, VRAM_256_INFINEON</td></tr><tr><td>VRAM_SAM256</td><td>GPU_MEM_256M, VRAM_256_SAMSUNG</td></tr><tr><td>M59_TPM</td><td>TPM</td></tr></table><div>Module Parts</div><table><tr><th>PART NUMBER</th><th>QTY</th><th>DESCRIPTION</th><th>REFERENCE DES</th><th>CRITICAL</th><th>BOM OPTION</th></tr><tr><td>333S0354</td><td>4</td><td>IC, SGRAM, GDDR3, 8MX32, 700MHZ, 136 FBGA</td><td>U8900, U8950, U9000, U9050</td><td>CRITICAL</td><td>VRAM_128_SAMSUNG</td></tr><tr><td>333S0350</td><td>4</td><td>IC, SGRAM, GDDR3, 16MX32, 700MHZ, 136 FBGA</td><td>U8900, U8950, U9000, U9050</td><td>CRITICAL</td><td>VRAM_256_SAMSUNG</td></tr><tr><td>333S0358</td><td>4</td><td>IC, SGRAM, GDDR3, 8MX32, 700MHZ, 136 FBGA</td><td>U8900, U8950, U9000, U9050</td><td>CRITICAL</td><td>VRAM_128_HYNIX</td></tr><tr><td>333S0351</td><td>4</td><td>IC, SGRAM, GDDR3, 16MX32, 700MHZ, 136 FBGA</td><td>U8900, U8950, U9000, U9050</td><td>CRITICAL</td><td>VRAM_256_HYNIX</td></tr><tr><td>333S0376</td><td>4</td><td>IC, SGRAM, GDDR3, 8MX32, 700MHZ, 136 FBGA</td><td>U8900, U8950, U9000, U9050</td><td>CRITICAL</td><td>VRAM_128_INFINEON</td></tr><tr><td>333S0377</td><td>4</td><td>IC, SGRAM, GDDR3, 16MX32, 600MHZ, 136 FBGA</td><td>U8900, U8950, U9000, U9050</td><td>CRITICAL</td><td>VRAM_256_INFINEON</td></tr><tr><td>337S3391</td><td>1</td><td>IC, MDC, B2, PRQ, 2.16G, 34W, 667M, 4M, 479BGA</td><td>U0700</td><td>CRITICAL</td><td>CPU_2_16GHZ</td></tr><tr><td>337S3393</td><td>1</td><td>IC, MDC, B2, PRQ, 2.33G, 34W, 667M, 4M, 479BGA</td><td>U0700</td><td>CRITICAL</td><td>CPU_2_33GHZ</td></tr><tr><td>341S1922</td><td>1</td><td>IC, EFI, BOOTROM DEVELOPMENT (UNLOCKED), M59</td><td>U6301</td><td>CRITICAL</td><td>BOOTROM_DEVEL</td></tr><tr><td>341S1923</td><td>1</td><td>IC, EFI, BOOTROM FINAL (LOCKED), M59</td><td>U6301</td><td>CRITICAL</td><td>BOOTROM_FINAL</td></tr><tr><td>338S0274</td><td>1</td><td>IC, SMC, HSR, 2116</td><td>U5800</td><td>CRITICAL</td><td>SMC_BLANK</td></tr><tr><td>341S1929</td><td>1</td><td>IC, PRGRM, SMC (NEW), M59</td><td>U5800</td><td>CRITICAL</td><td>SMC_PRGRM</td></tr><tr><td>338S0269</td><td>1</td><td>IC, 945GM, NORTHERIDGE</td><td>U1200</td><td>CRITICAL</td><td></td></tr><tr><td>338S0270</td><td>1</td><td>IC, 888S053, GIGASET ENET SCVR, 64P QFN, NO</td><td>U4101</td><td>CRITICAL</td><td></td></tr><tr><td>338S0368</td><td>1</td><td>IC, ATI, M541-LP, GRAPHICCTL, LP 880BGA</td><td>U8400</td><td>CRITICAL</td><td></td></tr><tr><td>341S1789</td><td>1</td><td>IC, TPM, 28-PIN TSSOP</td><td>U6700</td><td>CRITICAL</td><td>TPM</td></tr><tr><td>341S1797</td><td>1</td><td>IC, EEPROM, SERIAL IIC, 8KBIT, SO8</td><td>U4102</td><td>CRITICAL</td><td></td></tr><tr><td>343S0385</td><td>1</td><td>IC, ICH7M, BGA</td><td>U2100</td><td>CRITICAL</td><td></td></tr><tr><td>353S1461</td><td>1</td><td>IC, ICL9504, SYNC REG CTRL, QFN48</td><td>U7530</td><td>CRITICAL</td><td></td></tr><tr><td>359S0109</td><td>1</td><td>LOW POWER CLOCK SYNTHESIZER, 68PIN</td><td>U3301</td><td>CRITICAL</td><td></td></tr></table><div>Alternate Parts</div><table><tr><th>PART NUMBER</th><th>ALTERNATE FOR PART NUMBER</th><th>BOM OPTION</th><th>REF DES</th><th>COMMENTS:</th></tr><tr><td>128S0094</td><td>128S0060</td><td></td><td>ALL</td><td>330uF, 2V, 5MOHM, D2</td></tr><tr><td>128S0095</td><td>128S0060</td><td></td><td>ALL</td><td>330uF, 2V, 6MOHM, D2</td></tr><tr><td>128S0081</td><td>128S0061</td><td></td><td>ALL</td><td>150uF, 6.3V, 25MOHM, C2</td></tr><tr><td>376S0448</td><td>376S0445</td><td></td><td>ALL</td><td>S17806ADN for P1M6296</td></tr><tr><td>353S1465</td><td>353S1461</td><td></td><td>ALL</td><td>Screwmed ICL9282 for ICL9504</td></tr><tr><td>152S0287</td><td>152S0435</td><td></td><td>ALL</td><td>Alternates for Collins's MEM011</td></tr><tr><td>128S0093</td><td>128S0092</td><td></td><td>ALL</td><td>33uF, 16V, D2</td></tr></table></div> <div><div>BOM Configuration</div><div>SYNC_MASTER=N/A</div><div>SYNC_DATE=N/A</div><div>NOTICE OF PROPRIETARY PROPERTY</div><div>THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. 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A.0.0</div><div>SCALE NONE</div><div>SHT 4 OF 84</div></div>																BOM NUMBER	BOM NAME	BOM OPTIONS	630-7849	PCBA, 2.16GHZ, 128VRAM, M59, MBP15	EEE_WTE, M59_COMMON, CPU_2_16GHZ, VRAM_SAM128	BOM NUMBER	BOM NAME	BOM OPTIONS	630-7851	PCBA, 2.33GHZ, 256VRAM, M59, MBP15	EEE_WTG, M59_COMMON, CPU_2_33GHZ, VRAM_SAM256	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:WTE]	CRITICAL	EEE_WTE	826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:WTG]	CRITICAL	EEE_WTG	BOM GROUP	BOM OPTIONS	M59_COMMON	ALTERNATE, COMMON, M59_COMMON1, M59_COMMON2, M59_COMMON3	M59_COMMON1	BOOTROM_FINAL, ENET_LOWPWR_EN, ENETPWR_S3AC, GPU_BB_CTL, D3CPGOOD_3V3	M59_COMMON2	ITP, KBDLED_HAS, LPCPLUS, LVDS_PD, MEMVREF_S3	M59_COMMON3	MEMVTT_EN_PU, RTUSB_ESD, SMC_PRGRM, USB_C_OC_PU, USB_D_OC_PU, USB_E_OC_PU	VRAM_INF128	GPU_MEM_NOT_SAM, VRAM_128_INFINEON	VRAM_SAM128	VRAM_128_SAMSUNG	VRAM_INF256	GPU_MEM_256M, GPU_MEM_NOT_SAM, VRAM_256_INFINEON	VRAM_SAM256	GPU_MEM_256M, VRAM_256_SAMSUNG	M59_TPM	TPM	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	333S0354	4	IC, SGRAM, GDDR3, 8MX32, 700MHZ, 136 FBGA	U8900, U8950, U9000, U9050	CRITICAL	VRAM_128_SAMSUNG	333S0350	4	IC, SGRAM, GDDR3, 16MX32, 700MHZ, 136 FBGA	U8900, U8950, U9000, U9050	CRITICAL	VRAM_256_SAMSUNG	333S0358	4	IC, SGRAM, GDDR3, 8MX32, 700MHZ, 136 FBGA	U8900, U8950, U9000, U9050	CRITICAL	VRAM_128_HYNIX	333S0351	4	IC, SGRAM, GDDR3, 16MX32, 700MHZ, 136 FBGA	U8900, U8950, U9000, U9050	CRITICAL	VRAM_256_HYNIX	333S0376	4	IC, SGRAM, GDDR3, 8MX32, 700MHZ, 136 FBGA	U8900, U8950, U9000, U9050	CRITICAL	VRAM_128_INFINEON	333S0377	4	IC, SGRAM, GDDR3, 16MX32, 600MHZ, 136 FBGA	U8900, U8950, U9000, U9050	CRITICAL	VRAM_256_INFINEON	337S3391	1	IC, MDC, B2, PRQ, 2.16G, 34W, 667M, 4M, 479BGA	U0700	CRITICAL	CPU_2_16GHZ	337S3393	1	IC, MDC, B2, PRQ, 2.33G, 34W, 667M, 4M, 479BGA	U0700	CRITICAL	CPU_2_33GHZ	341S1922	1	IC, EFI, BOOTROM DEVELOPMENT (UNLOCKED), M59	U6301	CRITICAL	BOOTROM_DEVEL	341S1923	1	IC, EFI, BOOTROM FINAL (LOCKED), M59	U6301	CRITICAL	BOOTROM_FINAL	338S0274	1	IC, SMC, HSR, 2116	U5800	CRITICAL	SMC_BLANK	341S1929	1	IC, PRGRM, SMC (NEW), M59	U5800	CRITICAL	SMC_PRGRM	338S0269	1	IC, 945GM, NORTHERIDGE	U1200	CRITICAL		338S0270	1	IC, 888S053, GIGASET ENET SCVR, 64P QFN, NO	U4101	CRITICAL		338S0368	1	IC, ATI, M541-LP, GRAPHICCTL, LP 880BGA	U8400	CRITICAL		341S1789	1	IC, TPM, 28-PIN TSSOP	U6700	CRITICAL	TPM	341S1797	1	IC, EEPROM, SERIAL IIC, 8KBIT, SO8	U4102	CRITICAL		343S0385	1	IC, ICH7M, BGA	U2100	CRITICAL		353S1461	1	IC, ICL9504, SYNC REG CTRL, QFN48	U7530	CRITICAL		359S0109	1	LOW POWER CLOCK SYNTHESIZER, 68PIN	U3301	CRITICAL		PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	128S0094	128S0060		ALL	330uF, 2V, 5MOHM, D2	128S0095	128S0060		ALL	330uF, 2V, 6MOHM, D2	128S0081	128S0061		ALL	150uF, 6.3V, 25MOHM, C2	376S0448	376S0445		ALL	S17806ADN for P1M6296	353S1465	353S1461		ALL	Screwmed ICL9282 for ICL9504	152S0287	152S0435		ALL	Alternates for Collins's MEM011	128S0093	128S0092		ALL	33uF, 16V, D2
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M59_COMMON	ALTERNATE, COMMON, M59_COMMON1, M59_COMMON2, M59_COMMON3																																																																																																																																																																																																																																						
M59_COMMON1	BOOTROM_FINAL, ENET_LOWPWR_EN, ENETPWR_S3AC, GPU_BB_CTL, D3CPGOOD_3V3																																																																																																																																																																																																																																						
M59_COMMON2	ITP, KBDLED_HAS, LPCPLUS, LVDS_PD, MEMVREF_S3																																																																																																																																																																																																																																						
M59_COMMON3	MEMVTT_EN_PU, RTUSB_ESD, SMC_PRGRM, USB_C_OC_PU, USB_D_OC_PU, USB_E_OC_PU																																																																																																																																																																																																																																						
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333S0358	4	IC, SGRAM, GDDR3, 8MX32, 700MHZ, 136 FBGA	U8900, U8950, U9000, U9050	CRITICAL	VRAM_128_HYNIX																																																																																																																																																																																																																																		
333S0351	4	IC, SGRAM, GDDR3, 16MX32, 700MHZ, 136 FBGA	U8900, U8950, U9000, U9050	CRITICAL	VRAM_256_HYNIX																																																																																																																																																																																																																																		
333S0376	4	IC, SGRAM, GDDR3, 8MX32, 700MHZ, 136 FBGA	U8900, U8950, U9000, U9050	CRITICAL	VRAM_128_INFINEON																																																																																																																																																																																																																																		
333S0377	4	IC, SGRAM, GDDR3, 16MX32, 600MHZ, 136 FBGA	U8900, U8950, U9000, U9050	CRITICAL	VRAM_256_INFINEON																																																																																																																																																																																																																																		
337S3391	1	IC, MDC, B2, PRQ, 2.16G, 34W, 667M, 4M, 479BGA	U0700	CRITICAL	CPU_2_16GHZ																																																																																																																																																																																																																																		
337S3393	1	IC, MDC, B2, PRQ, 2.33G, 34W, 667M, 4M, 479BGA	U0700	CRITICAL	CPU_2_33GHZ																																																																																																																																																																																																																																		
341S1922	1	IC, EFI, BOOTROM DEVELOPMENT (UNLOCKED), M59	U6301	CRITICAL	BOOTROM_DEVEL																																																																																																																																																																																																																																		
341S1923	1	IC, EFI, BOOTROM FINAL (LOCKED), M59	U6301	CRITICAL	BOOTROM_FINAL																																																																																																																																																																																																																																		
338S0274	1	IC, SMC, HSR, 2116	U5800	CRITICAL	SMC_BLANK																																																																																																																																																																																																																																		
341S1929	1	IC, PRGRM, SMC (NEW), M59	U5800	CRITICAL	SMC_PRGRM																																																																																																																																																																																																																																		
338S0269	1	IC, 945GM, NORTHERIDGE	U1200	CRITICAL																																																																																																																																																																																																																																			
338S0270	1	IC, 888S053, GIGASET ENET SCVR, 64P QFN, NO	U4101	CRITICAL																																																																																																																																																																																																																																			
338S0368	1	IC, ATI, M541-LP, GRAPHICCTL, LP 880BGA	U8400	CRITICAL																																																																																																																																																																																																																																			
341S1789	1	IC, TPM, 28-PIN TSSOP	U6700	CRITICAL	TPM																																																																																																																																																																																																																																		
341S1797	1	IC, EEPROM, SERIAL IIC, 8KBIT, SO8	U4102	CRITICAL																																																																																																																																																																																																																																			
343S0385	1	IC, ICH7M, BGA	U2100	CRITICAL																																																																																																																																																																																																																																			
353S1461	1	IC, ICL9504, SYNC REG CTRL, QFN48	U7530	CRITICAL																																																																																																																																																																																																																																			
359S0109	1	LOW POWER CLOCK SYNTHESIZER, 68PIN	U3301	CRITICAL																																																																																																																																																																																																																																			
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:																																																																																																																																																																																																																																			
128S0094	128S0060		ALL	330uF, 2V, 5MOHM, D2																																																																																																																																																																																																																																			
128S0095	128S0060		ALL	330uF, 2V, 6MOHM, D2																																																																																																																																																																																																																																			
128S0081	128S0061		ALL	150uF, 6.3V, 25MOHM, C2																																																																																																																																																																																																																																			
376S0448	376S0445		ALL	S17806ADN for P1M6296																																																																																																																																																																																																																																			
353S1465	353S1461		ALL	Screwmed ICL9282 for ICL9504																																																																																																																																																																																																																																			
152S0287	152S0435		ALL	Alternates for Collins's MEM011																																																																																																																																																																																																																																			
128S0093	128S0092		ALL	33uF, 16V, D2																																																																																																																																																																																																																																			
8		7		6		5		4		3		2		1																																																																																																																																																																																																																									

extra TPM options:
SMC_TPM_GPI02
SMC_TPM_GPI01
SMC_TPM_PP

8

7

6

5

4

3

2

1

Power Supply NO_TESTS

NO_TEST

EXPOSED_VIA

TRUE

IMVP6_RBIAS

59C7

TRUE

IMVP6_COMP

59B7

TRUE

P5VS5_RUNSS

60C5 64A6

TRUE

P1V5S0_RUNSS

5B7 60C4 64C6

TRUE

P1V2S3_RT

61B6

TRUE

P1V2S3_RUNSS

41C4 61B7

TRUE

P3V3S5_COMP

5B7 63C6

TRUE

P3V3S5_FSET

5B7 63D6

TRUE

P1V0S0_COMP

5C7 63A7

TRUE

P1V0S0_FSET

5B7 63B7

TRUE

P3V42G3H_FB

64C3

TRUE

GPUVCORE_COMP

6B07

TRUE

GPUVCORE_FSET

6B07

TRUE

GPUBBP_ADJ

6B87

TRUE

GPUBBN_FB

6B43

TRUE

GPUVCORE_FB

6B07

TRUE

GPUVCORE_FB_RC

6B03

TRUE

GPUVCORE_ISEN

6B05

TRUE

GPUVCORE_LG

6B05

TRUE

GPUVCORE_PHASE

6B05

TRUE

GPUVCORE_UG

6B05

TRUE

IMVP6_COMP_RC

59B8

TRUE

IMVP6_DFB

59B6

TRUE

IMVP6_FB

59B7

TRUE

IMVP6_OCSET

59C6

TRUE

IMVP6_VDIFF

59C7

TRUE

IMVP6_VDIFF_RC

59B8

TRUE

P1V0S0_BOOT

63B5

TRUE

P1V0S0_BOOT_R

63B5

TRUE

P1V0S0_COMP

5D7 63A7

TRUE

P1V0S0_COMP_R

63A7

TRUE

P1V0S0_FB

63A7

TRUE

P1V0S0_FB_RC

63A3

TRUE

P1V0S0_FSET

5D7 63B7

TRUE

P1V0S0_ISEN

63A5

TRUE

P1V0S0_LG

63A5

TRUE

P1V0S0_PHASE

63B5

TRUE

P1V0S0_UG

63B5

TRUE

P1V5S0_RUNSS

5D7 60C4 64C6

TRUE

P3V3S5_BOOT

63D4

TRUE

P3V3S5_BOOT_R

63D4

TRUE

P3V3S5_COMP

5D7 63C6

TRUE

P3V3S5_COMP_R

63C6

TRUE

P3V3S5_FB

63C6

TRUE

P3V3S5_FB_RC

63C2

TRUE

P3V3S5_FSET

5D7 63D6

TRUE

P3V3S5_ISEN

63C4

TRUE

P3V3S5_LG

63C4

TRUE

P3V3S5_UG

63D4

TRUE

CK410_XTAL_IN

33C6

CPU FSB NO_TESTS

NO_TEST

EXPOSED_VIA

TRUE

FSB_A_L<31..3>

7C8 7D8 12C4 12D4 84D6

TRUE

FSB_ADS_L

7D6 12C4 84D6

TRUE

FSB_ADSTB_L<1..0>

7C8 7D8 12C4 84D6

TRUE

FSB_BNR_L

7D6 12C4 84D6

TRUE

FSB_BREQ0_L

7D6 12C4 84D6

TRUE

FSB_D_L<63..0>

7B3 7B4 7C3 7C4 12B6 12C6 12D6 84D6

TRUE

FSB_DBSY_L

7D6 12B4 84D6

TRUE

FSB_DINV_L<3..0>

7B3 7B4 7C3 7C4 12B4 84D6

TRUE

FSB_DRDY_L

7D6 12B4 84D6

TRUE

FSB_DSTBN_L<3..0>

7B3 7B4 7C3 7C4 12B4 84D6

TRUE

FSB_DSTBP_L<3..0>

7B3 7B4 7C3 7C4 12B4 84D6

TRUE

FSB_HIT_L

7D6 12B4 84D6

TRUE

FSB_HITM_L

7D6 12B4 84D6

TRUE

FSB_LOCK_L

7D6 12B4 84D6

TRUE

FSB_REQ_L<4..0>

7D8 12A4 12B4 84D6

Fan Connectors

FUNC_TEST

TRUE

=PP5V_S0_FAN_LT

56C7 65A1

TRUE

FAN_LT_PWM

56B6

TRUE

FAN_LT_TACH

56B6

TRUE

FAN_RT_PWM

56B3

TRUE

FAN_RT_TACH

56B3

Battery Digital Connector

FUNC_TEST

TRUE

SMC_BS_ALERT_L

49C5 50B2 6B85

TRUE

=SMBUS_BATT_SCL

27C1 66B5

TRUE

=SMBUS_BATT_SDA

27C1 66B5

TRUE

GND_BATT

66B5

Left I/O Data Connector

FUNC_TEST

TRUE

=PP1V5_S0_LIO

47D6 65C6

TRUE

=PPDCIN_G3H_LIO

47D6 65A8

TRUE

=PP5V_S5_LIO

47D6 65B1

TRUE

=PP3V42_G3H_LIO

47D6 65D3

TRUE

PP5V_S0_AUDIO_PWR

47D4

TRUE

PP5V_S0_AUDIO

47C4

TRUE

GND_AUDIO_PWR

47A4

TRUE

GND_AUDIO

47A4

TRUE

ACZ_SDATAIN<0>

21C7 47B6 4AB4

TRUE

ACZ_SDATAOUT

21C7 47B6 4AB4

TRUE

ACZ_BITCLK

21C7 47B6 4AB4

TRUE

ACZ_RST_L

21C7 47B6 4AB4

TRUE

EXCARD_OC_L

6C3 47C6 50B3

TRUE

L1USB_OC_L

6D3 47C6

TRUE

LIO_BATT_ISENSE

47D6 53C3

TRUE

SMC_SYS_ISET

47D6 49B5

TRUE

SMC_BATT_ISET

47B6 49B5

TRUE

SMC_BATT_CHG_EN

47D6 49D7 50A2

TRUE

SMC_BC_ACLK

47B6 49C5 50A2

TRUE

SMC_ADAPTER_EN

43B7 47C6 49D5

TRUE

LIO_P3V3S0_EN_L

50A2 47B6 64C6

TRUE

LIO_DCIN_ISENSE

47B6 53C5

TRUE

LIO_P3V3S3_EN

47B6 64A6

TRUE

SMC_BATT_TRICKLE_EN_L

47B6 49D7 50A2

TRUE

SYS_ONEWIRE

47D6 49B7 50B2

TRUE

MINI_CLKREQ_L

34A3 47C6

TRUE

SMC_EXCARD_CP

47B6 49B7 50A2

TRUE

EXCARD_CLKREQ_L

34A3 47C6

TRUE

SMC_EXCARD_PWR_EN

47B6 49B7

TRUE

LIO_PLT_RESET_L

26C1 47C6

TRUE

ACZ_SYNC

21C7 47B6 4AB4

TRUE

=USB2_LT_N

6D3 47C3

TRUE

=USB2_LT_P

6D3 47C3

TRUE

=USB2_EXCARD_N

6C3 47C3

TRUE

=USB2_EXCARD_P

6C3 47C3

TRUE

=PCIE_EXCARD_R2D_N

47B3 48C6

TRUE

=PCIE_EXCARD_R2D_P

47B3 48C6

TRUE

=PCIE_EXCARD_D2R_N

47B3 48B6

TRUE

=PCIE_EXCARD_D2R_P

47B3 48C6

TRUE

PCIE_CLK100M_EXCARD_P

34C3 47B3

TRUE

PCIE_CLK100M_EXCARD_N

34B3 47B3

TRUE

=PCIE_MINI_R2D_N

47B3 48C6

TRUE

=PCIE_MINI_R2D_P

47B3 48C6

TRUE

=PCIE_MINI_D2R_N

47C3 48C6

TRUE

=PCIE_MINI_D2R_P

47C3 48C6

TRUE

PCIE_CLK100M_MINI_P

34D4 47C3

TRUE

PCIE_CLK100M_MINI_N

34D4 47C3

TRUE

=SMBUS_LIO_SMC_SCL

27D1 47C3

TRUE

=SMBUS_LIO_SMC_SCL

27B6 47C3

TRUE

=SMBUS_LIO_SB_SDA

27B6 47C3

TRUE

PCIE_WAKE_L

23C8 39C6 47C3

Left ALS Connector

FUNC_TEST

TRUE

=PP3V3_S3_LTALS

65C3 7B05

TRUE

ALS_GAIN

6D5 49B5 7B06

TRUE

L1ALS_OUT

55C7 7B06

TRUE

GND

Thermal Diode Connectors

FUNC_TEST

TRUE

HSTHMSNS_DX_P

62C5

TRUE

HSTHMSNS_DX_N

62C5

TRUE

RSFSTHMSNS_D_P

62D5

TRUE

RSFSTHMSNS_D_N

62C5

Other Func Test Points

FUNC_TEST

TRUE

=PP1V05_S0_REG

53A4 63A2 65D8

TRUE

PM_SYSRST_L

23C5 26C5 49B7

TRUE

SMC_ONOFF_L

49C5 50B2 50C6 7B02

Current Sense Calibration

FUNC_TEST

TRUE

ISENSE_CAL_EN

49B7 53A8

TRUE

=PP5V_S0_ISENSECAL

63A8 65A1

TRUE

=PP1V8_S3_REG

62C1 65B8

TRUE

=PP1V5_S0_REG

6D01 65C8

TRUE

PPVCORE_S0_GPU

65D1

TRUE

PPVCORE_S0_CPU

65D1

TRUE

GND

2 TPs per

8 TPs, 2 with each of above TP pairs

Camera Connector

FUNC_TEST

TRUE

=PP5V_S3_CAMERA

45C3 65B1

TRUE

=USB2_CAMERA_N

6C3 45C3

TRUE

=USB2_CAMERA_P

6D3 45B3

Inverter Connector

FUNC_TEST

TRUE

GND_CHASSIS_INVERTER

6A8

TRUE

PPBUS_S0_INVERTER

76B5

TRUE

GND_INVERTER

76A5

TRUE

INVERTER_PWM

76A5

TRUE

PP5V_INVERTER_SW

76B5

RTC Battery Connector

FUNC_TEST

TRUE

PPVBATT_G3C_RTC

26D6

TRUE

GND

Functional Test Points

Fan Connectors

FUNC_TEST

TRUE

=PP5V_S0_FAN_LT

56C7 65A1

TRUE

FAN_LT_PWM

56B6

TRUE

FAN_LT_TACH

56B6

TRUE

FAN_RT_PWM

56B3

TRUE

FAN_RT_TACH

56B3

Battery Digital Connector

FUNC_TEST

TRUE

SMC_BS_ALERT_L

49C5 50B2 6B85

TRUE

=SMBUS_BATT_SCL

27C1 66B5

TRUE

=SMBUS_BATT_SDA

27C1 66B5

TRUE

GND_BATT

66B5

Left I/O Data Connector

FUNC_TEST

TRUE

=PP1V5_S0_LIO

47D6 65C6

TRUE

=PPDCIN_G3H_LIO

47D6 65A8

TRUE

=PP5V_S5_LIO

47D6 65B1

TRUE

=PP3V42_G3H_LIO

47D6 65D3

TRUE

PP5V_S0_AUDIO_PWR

47D4

TRUE

PP5V_S0_AUDIO

47C4

TRUE

GND_AUDIO_PWR

47A4

TRUE

GND_AUDIO

47A4

TRUE

ACZ_SDATAIN<0>

21C7 47B6 4AB4

TRUE

ACZ_SDATAOUT

21C7 47B6 4AB4

TRUE

ACZ_BITCLK

21C7 47B6 4AB4

TRUE

ACZ_RST_L

21C7 47B6 4AB4

TRUE

EXCARD_OC_L

6C3 47C6 50B3

TRUE

L1USB_OC_L

6D3 47C6

TRUE

LIO_BATT_ISENSE

47D6 53C3

TRUE

SMC_SYS_ISET

47D6 49B5

TRUE

SMC_BATT_ISET

47B6 49B5

TRUE

SMC_BATT_CHG_EN

47D6 49D7 50A2

TRUE

SMC_BC_ACLK

47B6 49C5 50A2

TRUE

SMC_ADAPTER_EN

43B7 47C6 49D5

TRUE

LIO_P3V3S0_EN_L

50A2 47B6 64C6

TRUE

LIO_DCIN_ISENSE

47B6 53C5

TRUE

LIO_P3V3S3_EN

47B6 64A6

TRUE

SMC_BATT_TRICKLE_EN_L

47B6 49D7 50A2

TRUE

SYS_ONEWIRE

47D6 49B7 50B2

TRUE

MINI_CLKREQ_L

34A3 47C6

TRUE

SMC_EXCARD_CP

47B6 49B7 50A2

TRUE

EXCARD_CLKREQ_L

34A3 47C6

TRUE

SMC_EXCARD_PWR_EN

47B6 49B7

TRUE

LIO_PLT_RESET_L

26C1 47C6

TRUE

ACZ_SYNC

21C7 47B6 4AB4

TRUE

=USB2_LT_N

6D3 47C3

TRUE

=USB2_LT_P

6D3 47C3

TRUE

=USB2_EXCARD_N

6C3 47C3

TRUE

=USB2_EXCARD_P

6C3 47C3

TRUE

=PCIE_EXCARD_R2D_N

47B3 48C6

TRUE

=PCIE_EXCARD_R2D_P

47B3 48C6

TRUE

=PCIE_EXCARD_D2R_N

47B3 48B6

TRUE

=PCIE_EXCARD_D2R_P

47B3 48C6

TRUE

PCIE_CLK100M_EXCARD_P

34C3 47B3

TRUE

PCIE_CLK100M_EXCARD_N

34B3 47B3

TRUE

=PCIE_MINI_R2D_N

47B3 48C6

TRUE

=PCIE_MINI_R2D_P

47B3 48C6

TRUE

=PCIE_MINI_D2R_N

47C3 48C6

TRUE

=PCIE_MINI_D2R_P

47C3 48C6

TRUE

PCIE_CLK100M_MINI_P

34D4 47C3

TRUE

PCIE_CLK100M_MINI_N

34D4 47C3

TRUE

=SMBUS_LIO_SMC_SCL

27D1 47C3

TRUE

=SMBUS_LIO_SMC_SCL

27B6 47C3

TRUE

=SMBUS_LIO_SB_SDA

27B6 47C3

TRUE

PCIE_WAKE_L

23C8 39C6 47C3

Left ALS Connector

FUNC_TEST

TRUE

=PP3V3_S3_LTALS

65C3 7B05

TRUE

ALS_GAIN

6D5 49B5 7B06

TRUE

L1ALS_OUT

55C7 7B06

TRUE

GND

Thermal Diode Connectors

FUNC_TEST

TRUE

HSTHMSNS_DX_P

62C5

TRUE

HSTHMSNS_DX_N

62C5

TRUE

RSFSTHMSNS_D_P

62D5

TRUE

RSFSTHMSNS_D_N

62C5

Other Func Test Points

FUNC_TEST

TRUE

=PP1V05_S0_REG

53A4 63A2 65D8

TRUE

PM_SYSRST_L

23C5 26C5 49B7

TRUE

SMC_ONOFF_L

49C5 50B2 50C6 7B02

Current Sense Calibration

FUNC_TEST

TRUE

ISENSE_CAL_EN

49B7 53A8

TRUE

=PP5V_S0_ISENSECAL

63A8 65A1

TRUE

=PP1V8_S3_REG

62C1 65B8

TRUE

=PP1V5_S0_REG

6D01 65C8

TRUE

PPVCORE_S0_GPU

65D1

TRUE

PPVCORE_S0_CPU

65D1

TRUE

GND

2 TPs per

8 TPs, 2 with each of above TP pairs

Camera Connector

FUNC_TEST

TRUE

=PP5V_S3_CAMERA

45C3 65B1

TRUE

=USB2_CAMERA_N

6C3 45C3

TRUE

=USB2_CAMERA_P

6D3 45B3

Inverter Connector

FUNC_TEST

TRUE

GND_CHASSIS_INVERTER

6A8

TRUE

PPBUS_S0_INVERTER

76B5

TRUE

GND_INVERTER

76A5

TRUE

INVERTER_PWM

76A5

TRUE

PP5V_INVERTER_SW

76B5

RTC Battery Connector

FUNC_TEST

TRUE

PPVBATT_G3C_RTC

26D6

TRUE

GND

Functional Test Points

Fan Connectors

FUNC_TEST

TRUE

=PP5V_S0_FAN_LT

56C7 65A1

TRUE

FAN_LT_PWM

56B6

TRUE

FAN_LT_TACH

56B6

TRUE

FAN_RT_PWM

56B3

TRUE

FAN_RT_TACH

56B3

Battery Digital Connector

FUNC_TEST

TRUE

SMC_BS_ALERT_L

49C5 50B2 6B85

TRUE

=SMBUS_BATT_SCL

27C1 66B5

TRUE

=SMBUS_BATT_SDA

27C1 66B5

TRUE

GND_BATT

66B5

Left I/O Data Connector

FUNC_TEST

TRUE

=PP1V5_S0_LIO

47D6 65C6

TRUE

=PPDCIN_G3H_LIO

47D6 65A8

TRUE

=PP5V_S5_LIO

47D6 65B1

TRUE

=PP3V42_G3H_LIO

47D6 65D3

TRUE

PP5V_S0_AUDIO_PWR

47D4

TRUE

PP5V_S0_AUDIO

47C4

TRUE

GND_AUDIO_PWR

47A4

TRUE

GND_AUDIO

47A4

TRUE

ACZ_SDATAIN<0>

21C7 47B6 4AB4

TRUE

ACZ_SDATAOUT

21C7 47B6 4AB4

TRUE

ACZ_BITCLK

21C7 47B6 4AB4

TRUE

ACZ_RST_L

21C7 47B6 4AB4

TRUE

EXCARD_OC_L

6C3 47C6 50B3

TRUE

L1USB_OC_L

6D3 47C6

TRUE

LIO_BATT_ISENSE

47D6 53C3

TRUE

SMC_SYS_ISET

47D6 49B5

TRUE

SMC_BATT_ISET

47B6 49B5

TRUE

SMC_BATT_CHG_EN

47D6 49D7 50A2

TRUE

SMC_BC_ACLK

47B6 49C5 50A2

TRUE

SMC_ADAPTER_EN

43B7 47C6 49D5

TRUE

LIO_P3V3S0_EN_L

50A2 47B6 64C6

TRUE

LIO_DCIN_ISENSE

47B6 53C5

TRUE

LIO_P3V3S3_EN

47B6 64A6

TRUE

SMC_BATT_TRICKLE_EN_L

47B6 49D7 50A2

TRUE

SYS_ONEWIRE

47D6 49B7 50B2

TRUE

MINI_CLKREQ_L

34A3 47C6

TRUE

SMC_EXCARD_CP

47B6 49B7 50A2

TRUE

EXCARD_CLKREQ_L

34A3 47C6

TRUE

SMC_EXCARD_PWR_EN

47B6 49B7

TRUE

LIO_PLT_RESET_L

26C1 47C6

TRUE

ACZ_SYNC

21C7 47B6 4AB4

TRUE

=USB2_LT_N

6D3 47C3

TRUE

=USB2_LT_P

6D3 47C3

TRUE

=USB2_EXCARD_N

6C3 47C3

TRUE

=USB2_EXCARD_P

6C3 47C3

TRUE

=PCIE_EXCARD_R2D_N

47B3 48C6

TRUE

=PCIE_EXCARD_R2D_P

47B3 48C6

TRUE

=PCIE_EXCARD_D2R_N

47B3 48B6

TRUE

=PCIE_EXCARD_D2R_P

47B3 48C6

TRUE

PCIE_CLK100M_EXCARD_P

34C3 47B3

TRUE

PCIE_CLK100M_EXCARD_N

34B3 47B3

TRUE

=PCIE_MINI_R2D_N

47B3 48C6

TRUE

=PCIE_MINI_R2D_P

47B3 48C6

TRUE

=PCIE_MINI_D2R_N

47C3 48C6

TRUE

=PCIE_MINI_D2R_P

47C3 48C6

TRUE

PCIE_CLK100M_MINI_P

34D4 47C3

TRUE

PCIE_CLK100M_MINI_N

34D4 47C3

TRUE

=SMBUS_LIO_SMC_SCL

27D1 47C3

TRUE

=SMBUS_LIO_SMC_SCL

27B6 47C3

TRUE

=SMBUS_LIO_SB_SDA

27B6 47C3

TRUE

PCIE_WAKE_L

23C8 39C6 47C3

Left ALS Connector

FUNC_TEST

TRUE

=PP3V3_S3_LTALS

65C3 7B05

TRUE

ALS_GAIN

6D5 49B5 7B06

TRUE

L1ALS_OUT

55C7 7B06

TRUE

GND

Thermal Diode Connectors

FUNC_TEST

TRUE

HSTHMSNS_DX_P

62C5

TRUE

HSTHMSNS_DX_N

62C5

TRUE

RSFSTHMSNS_D_P

62D5

TRUE

RSFSTHMSNS_D_N

62C5

Other Func Test Points

FUNC_TEST

TRUE

=PP1V05_S0_REG

53A4 63A2 65D8

TRUE

PM_SYSRST_L

23C5 26C5 49B7

TRUE

SMC_ONOFF_L

49C5 50B2 50C6 7B02

Current Sense Calibration

FUNC_TEST

TRUE

ISENSE_CAL_EN

49B7 53A8

TRUE

=PP5V_S0_ISENSECAL

63A8 65A1

TRUE

=PP1V8_S3_REG

62C1 65B8

TRUE

=PP1V5_S0_REG

6D01 65C8

TRUE

PPVCORE_S0_GPU

65D1

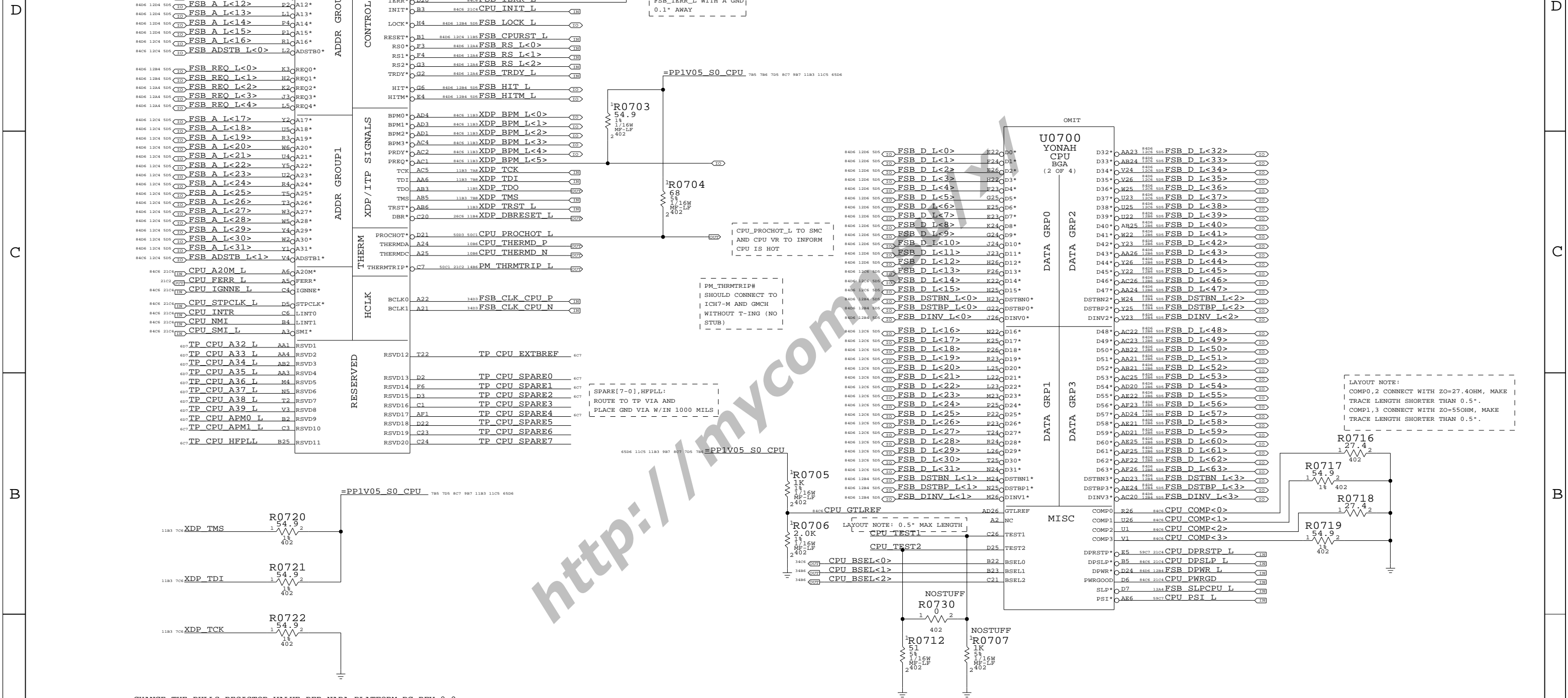
TRUE

PPVCORE_S0_CPU

65D1

TRUE

GND



WE THROUGH THE ITP700FLEX CONNECTOR CONNECT TO PDB XDP BUFFER BOARD--ECM*50
SO THE TDI PULL UP THROUGH 54.9 OHM,TMS PULL UP THROUGH 54.9 OHM
TCK PULL DOWN THROUGH 54.9 OHM(FOLLOW UP XDP DESIGN REFERENCE)

```

CPU 1 OF 2-FSB

SYNC_MASTER=(MASTER)                                SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

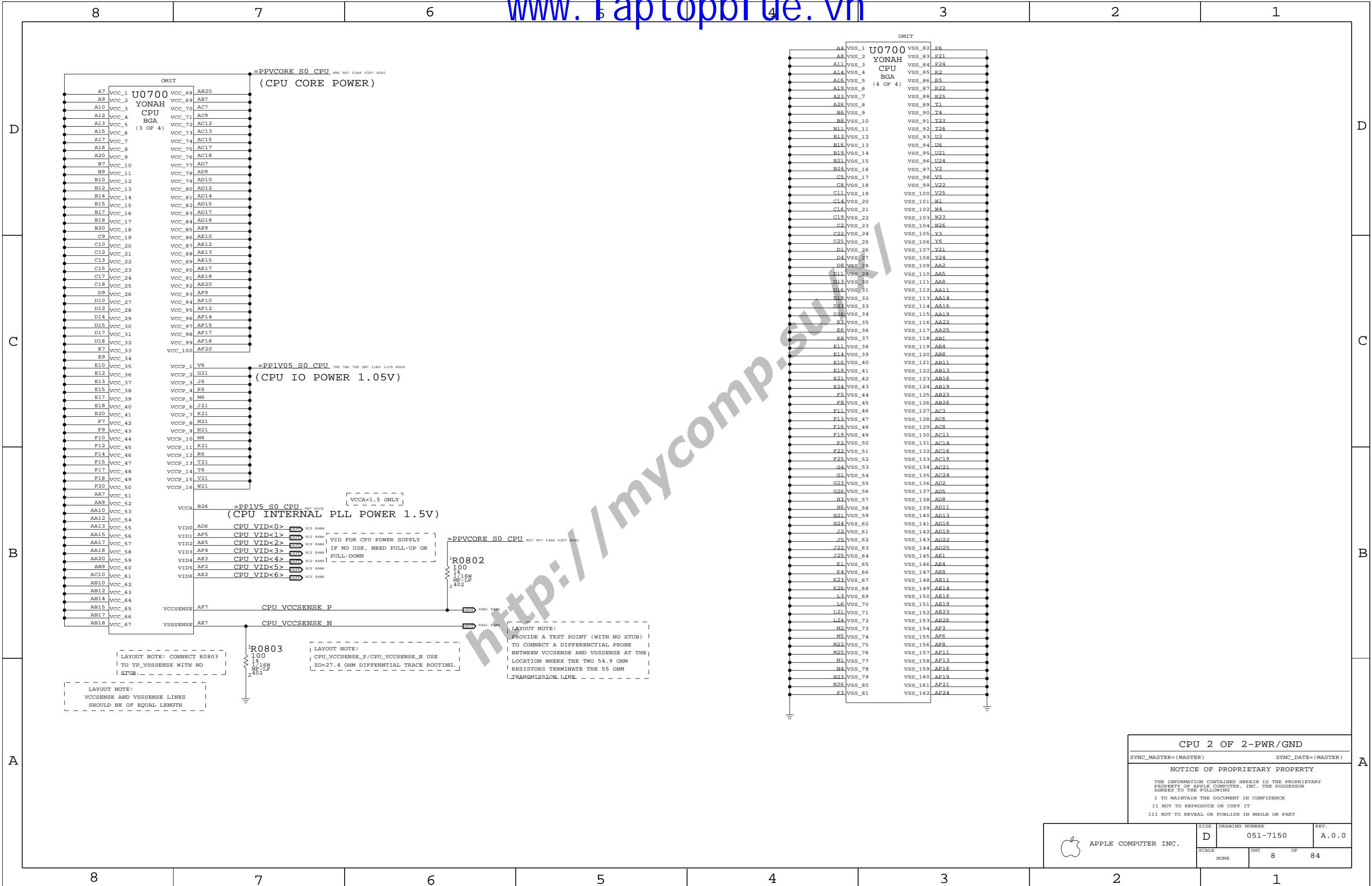
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CPU 2 OF 2-PWR/GND

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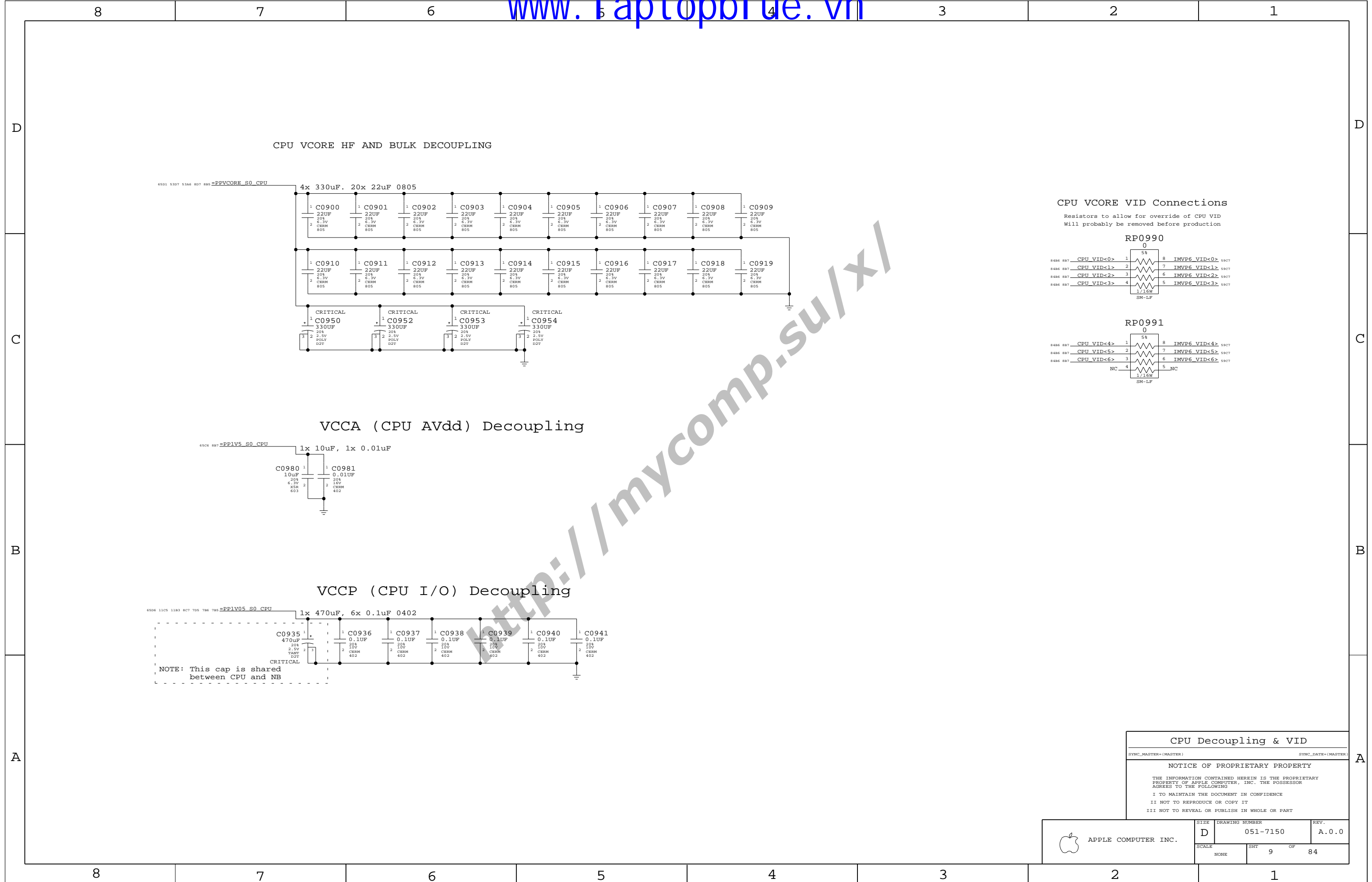
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C0906

22UF

20%

6.3V

CERM

805

C0907

22UF

20%

6.3V

CERM

805

C0908

22UF

20%

6.3V

CERM

805

C0909

22UF

20%

6.3V

CERM

805

C0910

22UF

20%

6.3V

CERM

805

C0911

22UF

20%

6.3V

CERM

805

C0912

22UF

20%

6.3V

CERM

805

C0913

22UF

20%

6.3V

CERM

805

C0914

22UF

20%

6.3V

CERM

805

C0915

22UF

20%

6.3V

CERM

805

C0916

22UF

20%

6.3V

CERM

805

C0917

22UF

20%

6.3V

CERM

805

C0918

22UF

20%

6.3V

CERM

805

C0919

22UF

20%

6.3V

CERM

805

CRITICAL

C0950

330UF

20%

2.5V

POLY

D2T

CRITICAL

C0952

330UF

20%

2.5V

POLY

D2T

CRITICAL

C0953

330UF

20%

2.5V

POLY

D2T

CRITICAL

C0954

330UF

20%

2.5V

POLY

D2T

VCCA (CPU AVdd) Decoupling

1x 10uF, 1x 0.01uF

C0980

10uF

20%

6.3V

X5R

603

C0981

0.01UF

20%

16V

CERM

402

VCCP (CPU I/O) Decoupling

1x 470uF, 6x 0.1uF 0402

C0935

470uF

20%

2.5V

TANT

D2T

C0936

0.1UF

20%

16V

CERM

402

C0937

0.1UF

20%

16V

CERM

402

C0938

0.1UF

20%

16V

CERM

402

C0939

0.1UF

20%

16V

CERM

402

C0940

0.1UF

20%

16V

CERM

402

C0941

0.1UF

20%

16V

CERM

402

NOTE: This cap is shared between CPU and NB

CPU VCORE VID Connections

Resistors to allow for override of CPU VID
Will probably be removed before production

RP0990

CPU VID<0>

CPU VID<1>

CPU VID<2>

CPU VID<3>

IMVP6 VID<0>

IMVP6 VID<1>

IMVP6 VID<2>

IMVP6 VID<3>

RP0991

CPU VID<4>

CPU VID<5>

CPU VID<6>

NC

IMVP6 VID<4>

IMVP6 VID<5>

IMVP6 VID<6>

NC

CPU Decoupling & VID

SYNC_MASTER=(MASTER)

SYNC_DATE=(MASTER)

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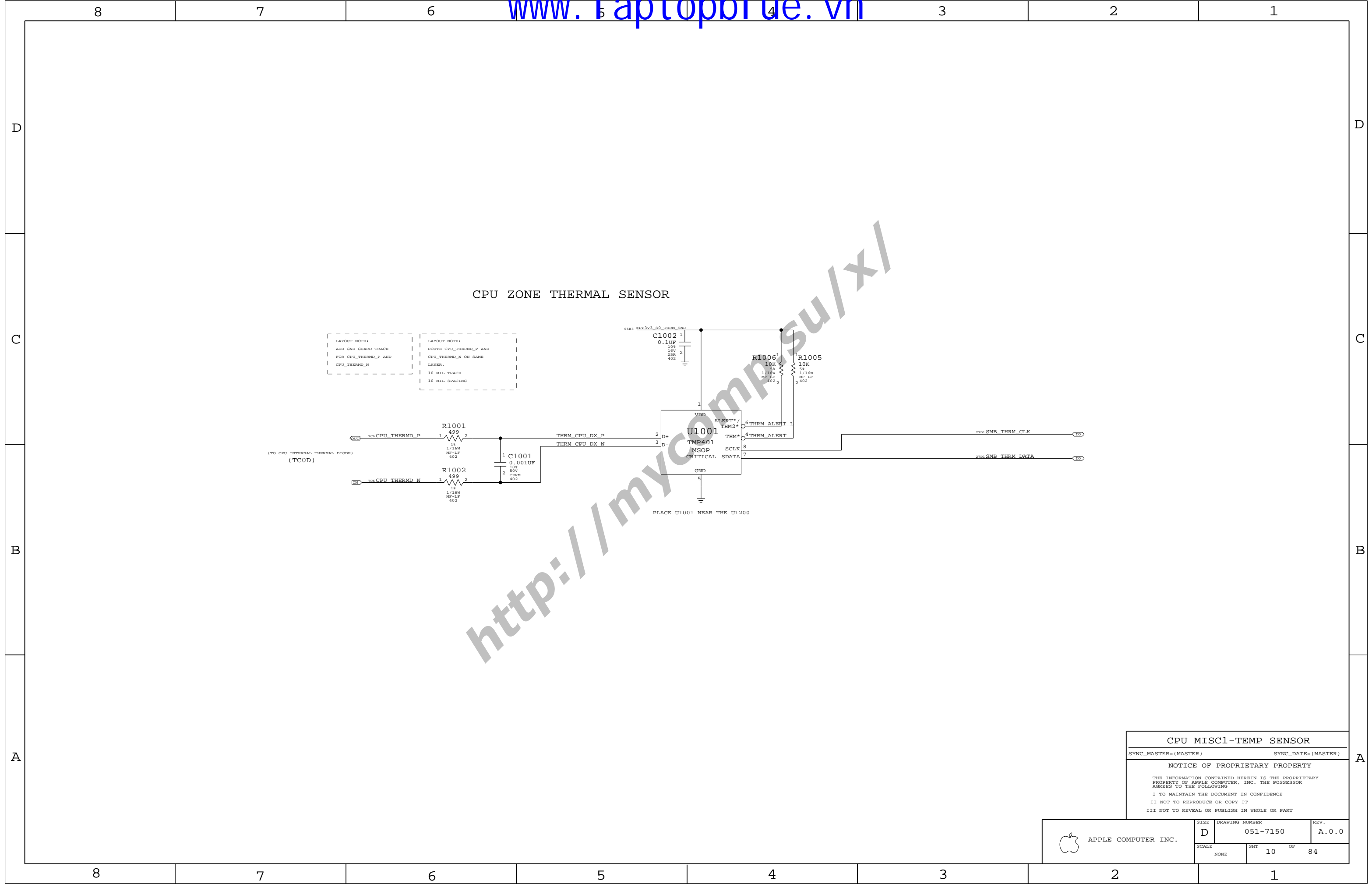
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	D	051-7150	A.0.0
SCALE		SHT	OF
NONE		9	84



CPU MISC1-TEMP SENSOR

SYNC_MASTER=(MASTER)

SYNC_DATE=(MASTER)


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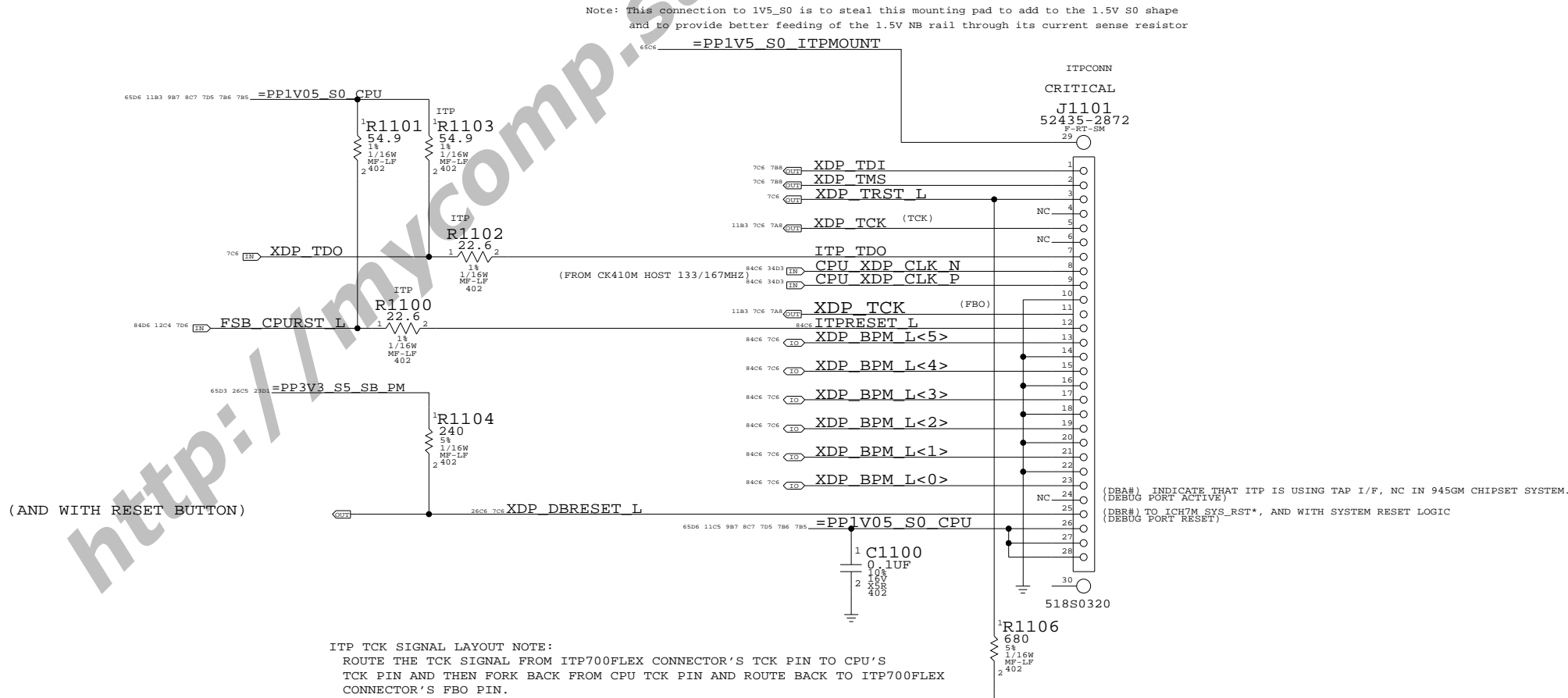
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	SCALE NONE	SHT 10	OF 84

CPU ITP700FLEX DEBUG SUPPORT



CPU ITP700FLEX DEBUG	
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7150	REV. A.0.0
	SCALE NONE	SHT 11	OF 84

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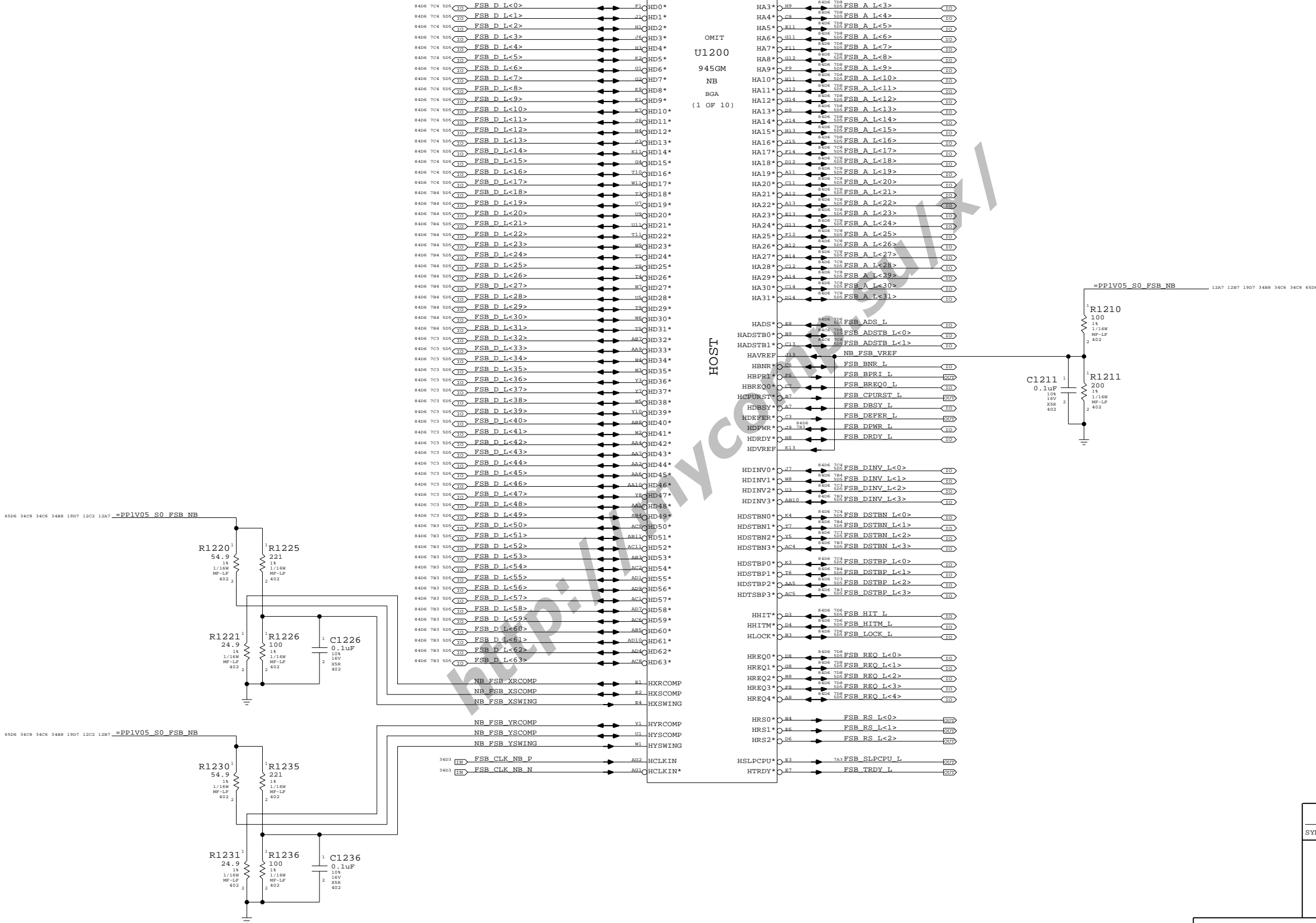
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NB CPU Interface

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LVDS Disable

Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit
filtering components. Unused DAC outputs should
connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



SDVO Alternate Function

SDVO_TVCLKIN#
SDVO_INT#
SDVO_FLDSTALL#

SDVO_TVCLKIN
SDVO_INT
SDVO_FLDSTALL

SDVOB_RED#
SDVOB_GREEN#
SDVOB_BLUE#
SDVOB_CLKN
SDVOC_RED#
SDVOC_GREEN#
SDVOC_BLUE#
SDVOC_CLKN

SDVOB_RED
SDVOB_GREEN
SDVOB_BLUE
SDVOB_CLKP
SDVOC_RED
SDVOC_GREEN
SDVOC_BLUE
SDVOC_CLKP

NB PEG / Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

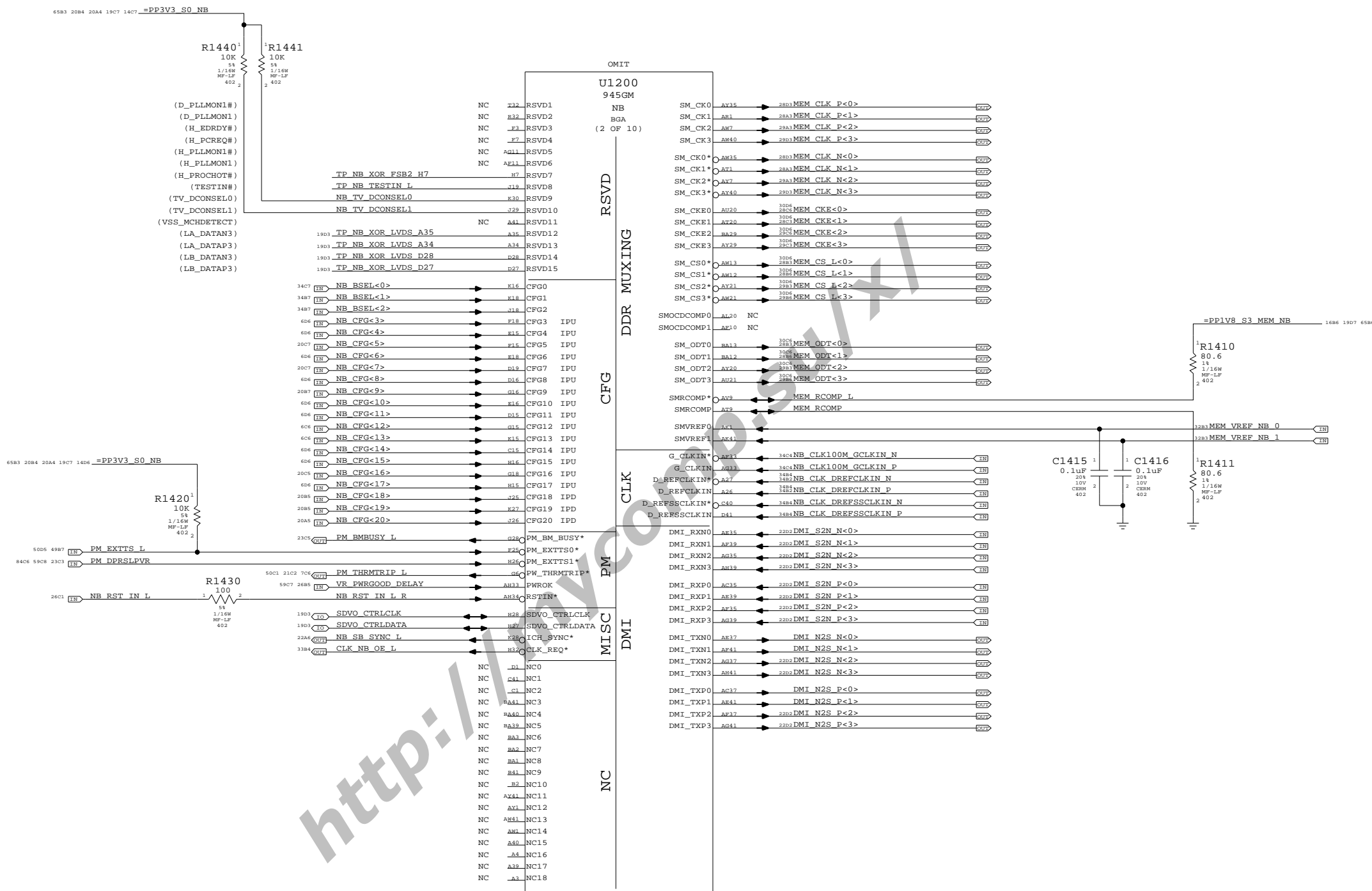
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D	051-7150	A.0.0
SCALE	SHT	OF
NONE	13	84



NB Misc Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

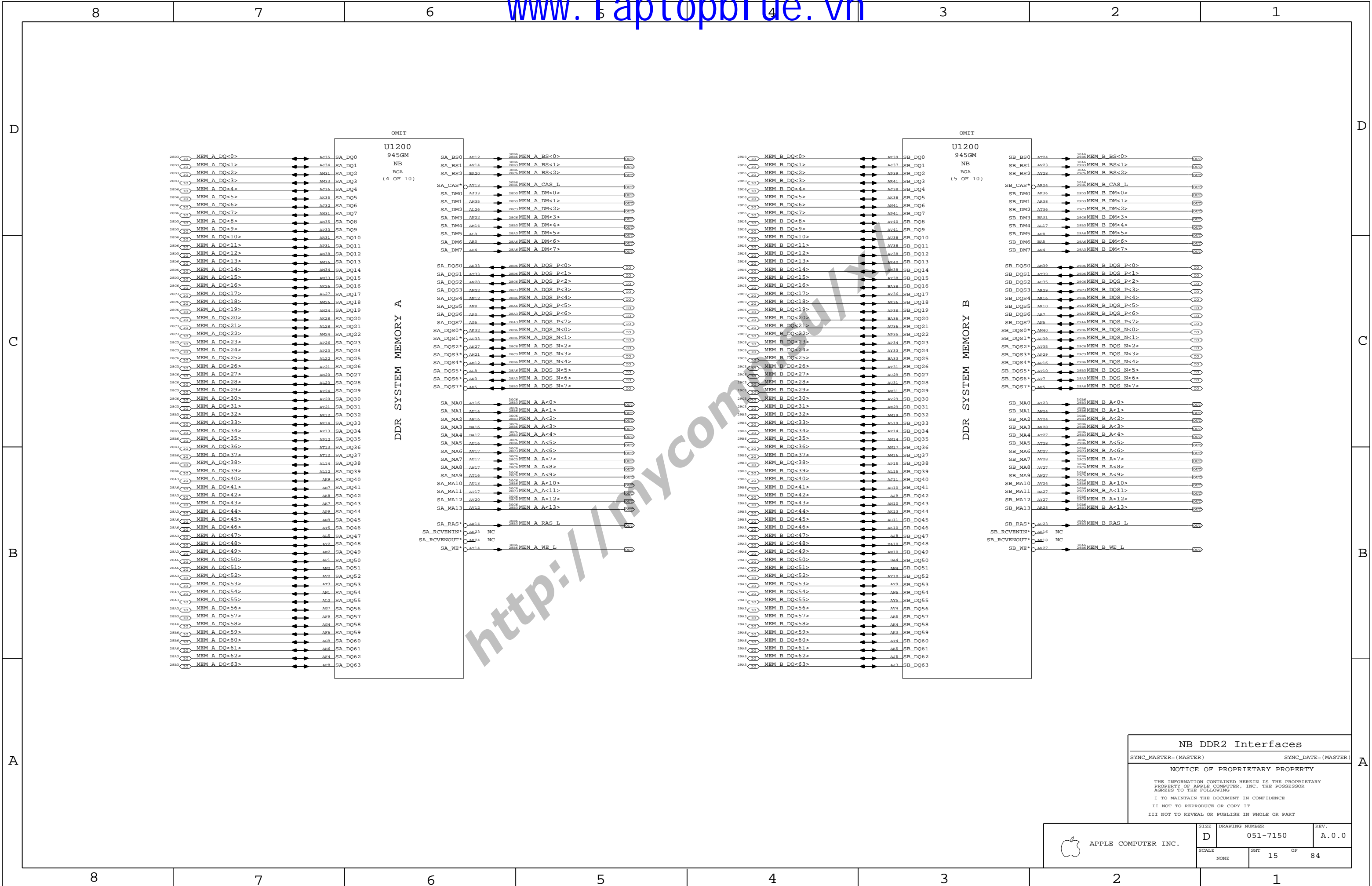
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NB DDR2 Interfaces

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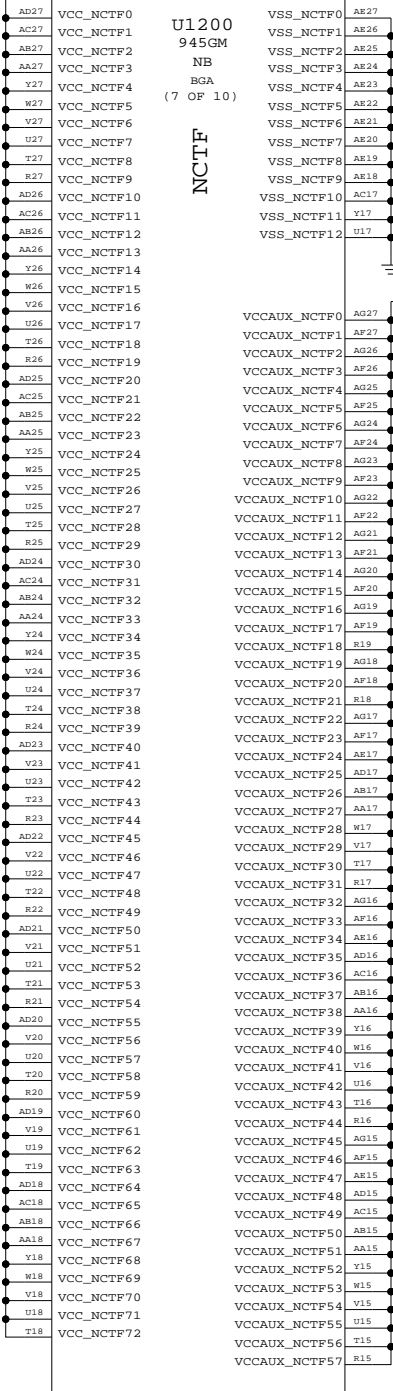
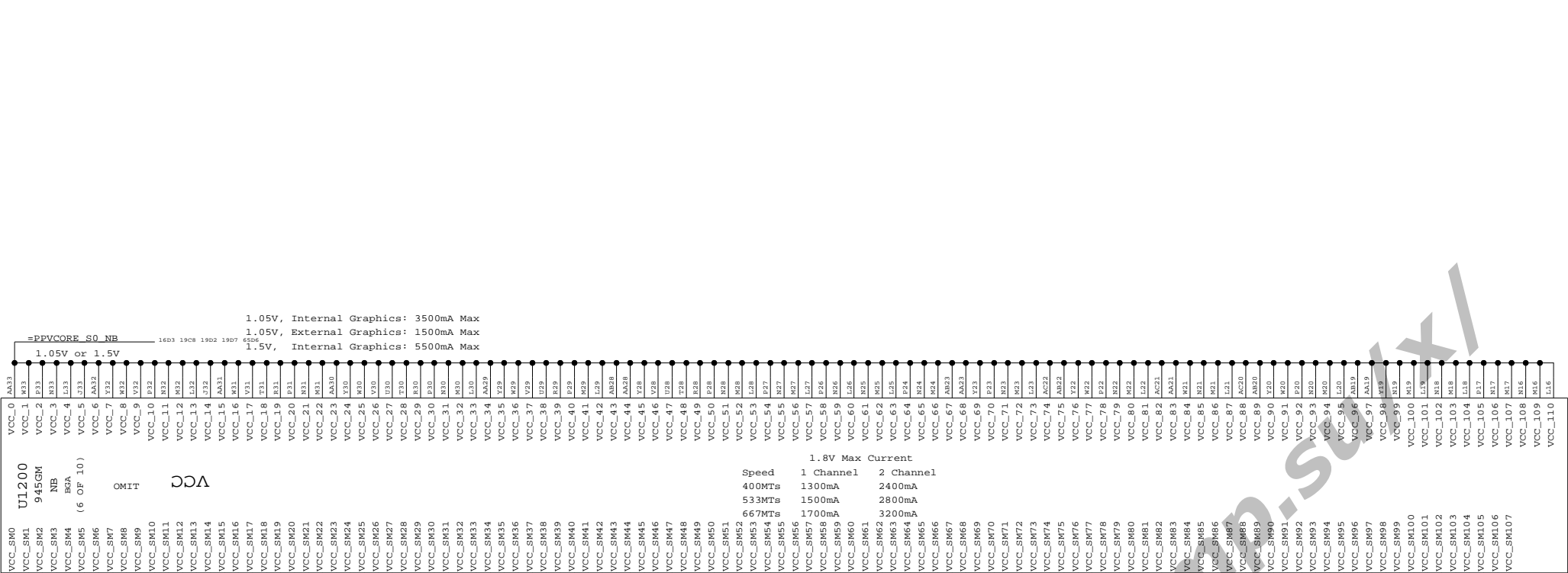
A

NCTF balls are Not Critical To Function

These connections can break without impacting part performance.

OMIT

6506 1907 1902 1908 1608 =PPVCORE_S0_NB



NB Power 1

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE

DRAWING NUMBER

D

051-7150

REV.

A.0.0

SCALE

NONE

SHT

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84

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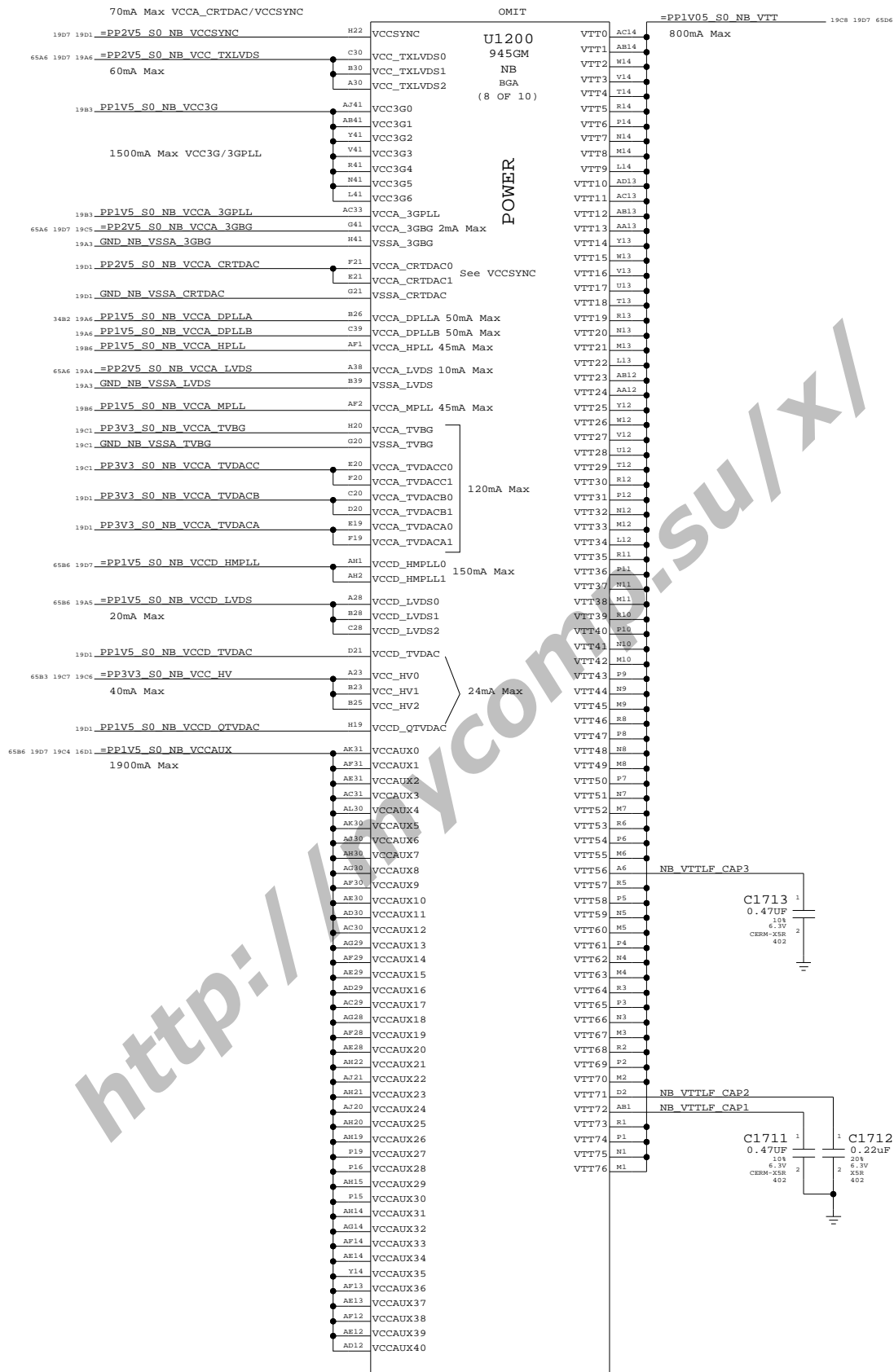
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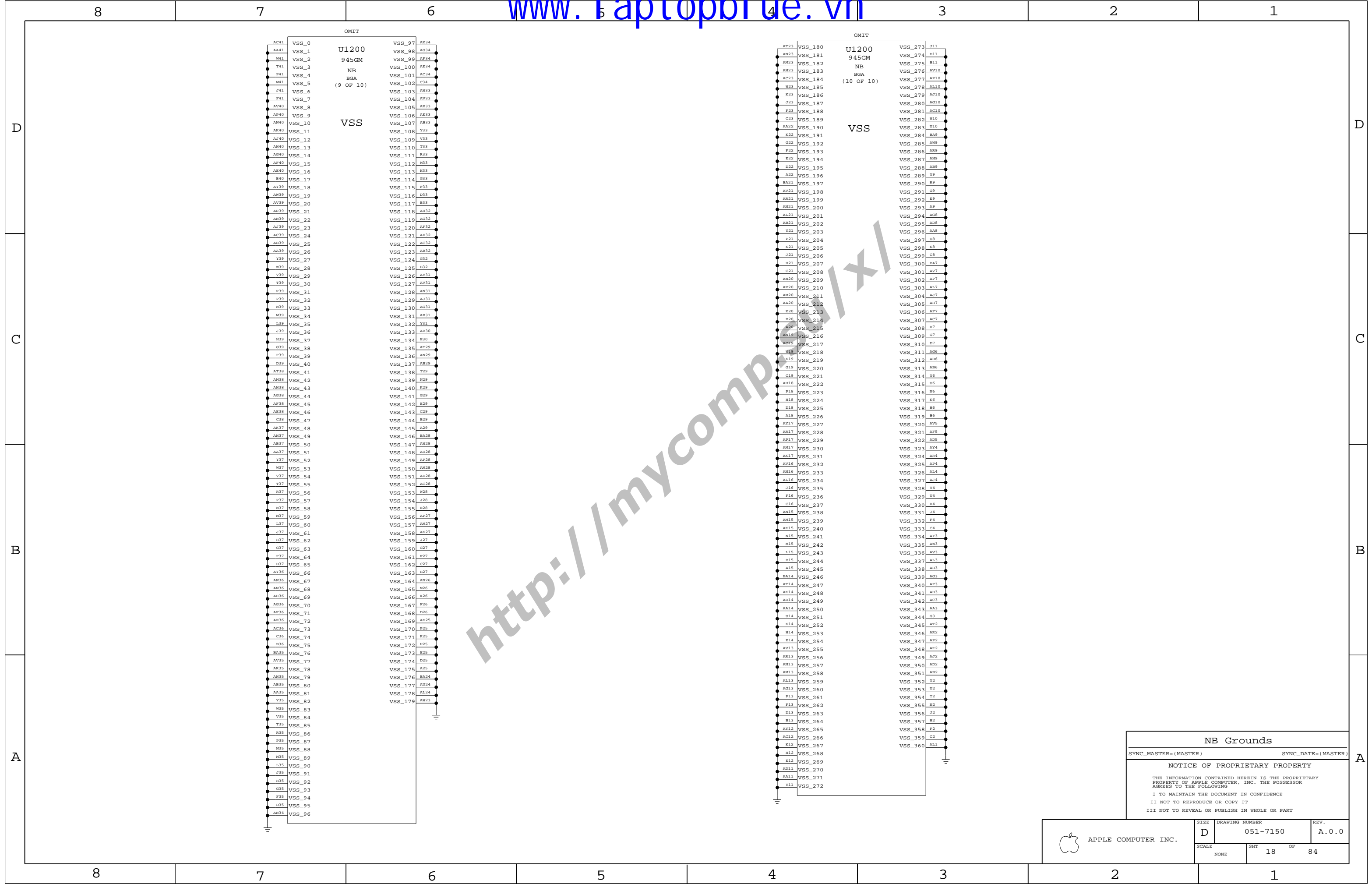
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NB Grounds

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

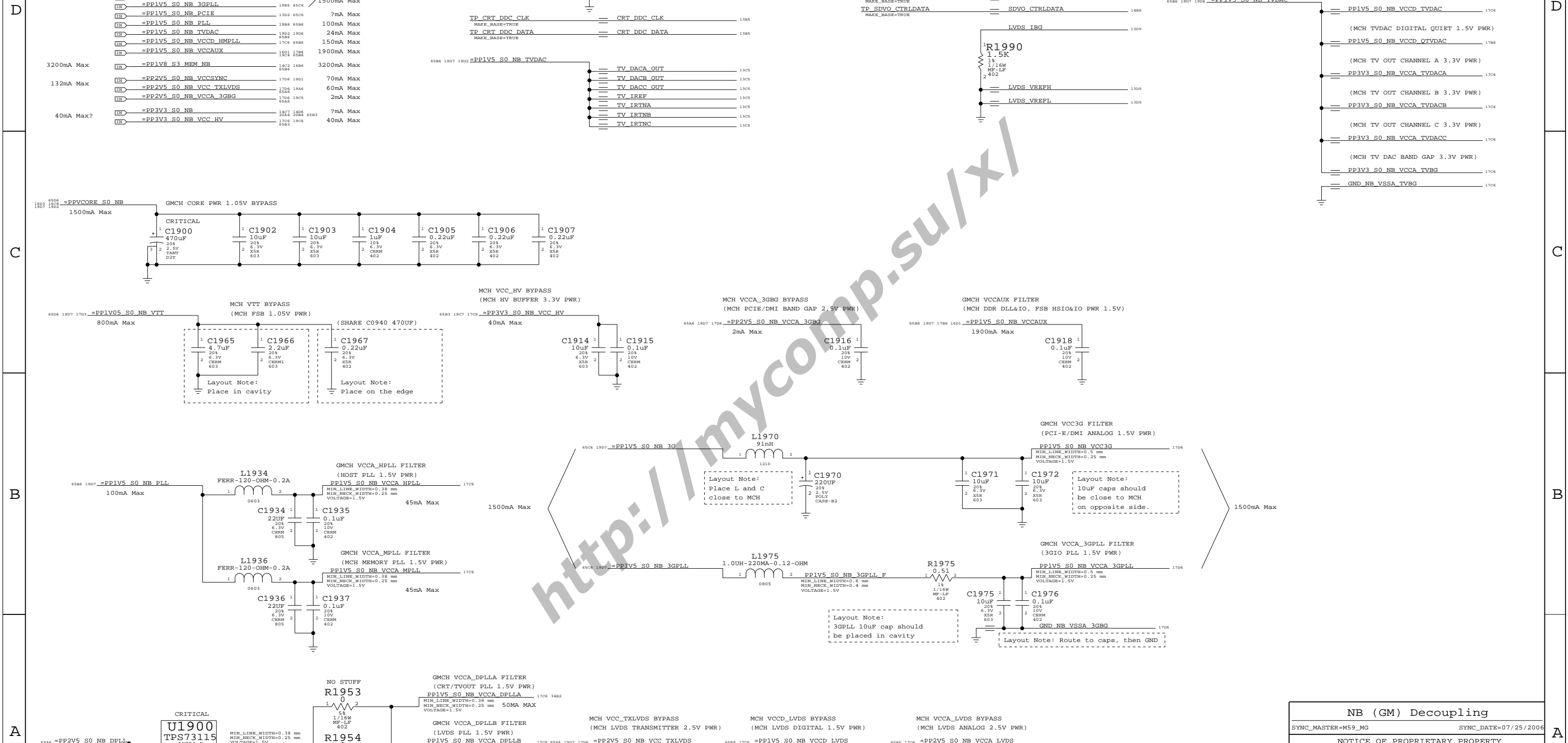
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D

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B

A

NB_CFG<3>	RESERVED
-----------	----------

NB_CFG<4>	RESERVED
-----------	----------

1406_NB_CFG<5> Internal pull-up	
NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2
PROBABLY NOT NEEDED	

NB_CFG<6>	RESERVED
-----------	----------

1406_NB_CFG<7> Internal pull-up	
NB_CFG<7> CPU Strap	High = Mobile CPU Low = RESERVED
NO STUFF	

NB_CFG<8>	RESERVED
-----------	----------

1406_NB_CFG<9> Internal pull-up	
NB_CFG<9> PCIe Graphics Lane Reversal	High = Normal Low = Reversed
NBCFG_PEG_REVERSE	

NB_CFG<10>	RESERVED
------------	----------

NB_CFG<11>	RESERVED
------------	----------

Internal pull-ups	
NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation

NB_CFG<14>	RESERVED
------------	----------

NB_CFG<15>	RESERVED
------------	----------

1406_NB_CFG<16> Internal pull-up	
NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled
NBCFG_DYN_ODT_DISABLE	

NB_CFG<17>	RESERVED
------------	----------


=PP3V3_S0_NB NBCFG_VCC_1V5	
NB_CFG<18> VCC Select	High = 1.5V Low = 1.05V
1406_NB_CFG<18> Internal pull-down	

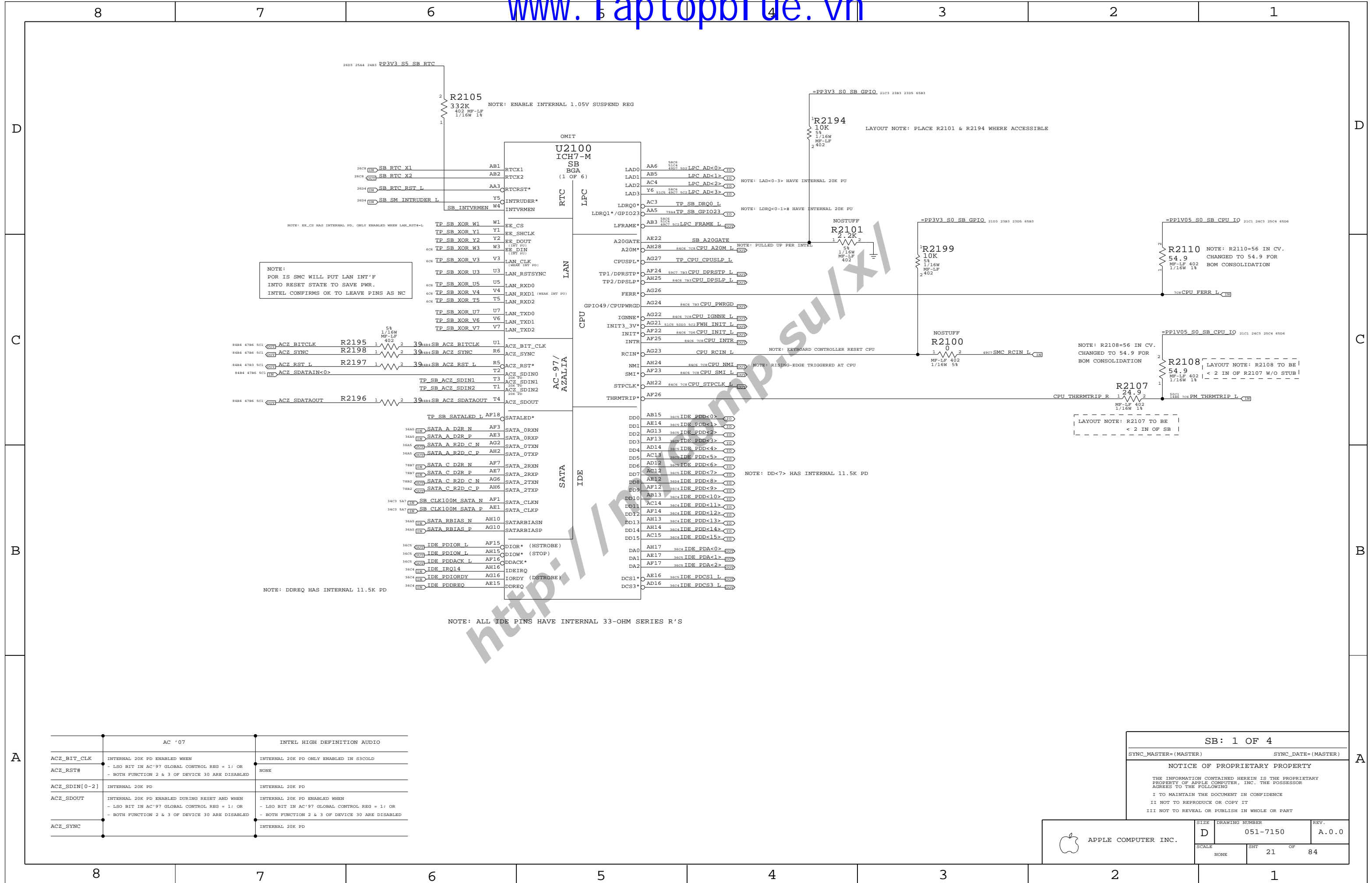
=PP3V3_S0_NB NBCFG_DMI_REVERSE	
NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal
1406_NB_CFG<19> Internal pull-down	

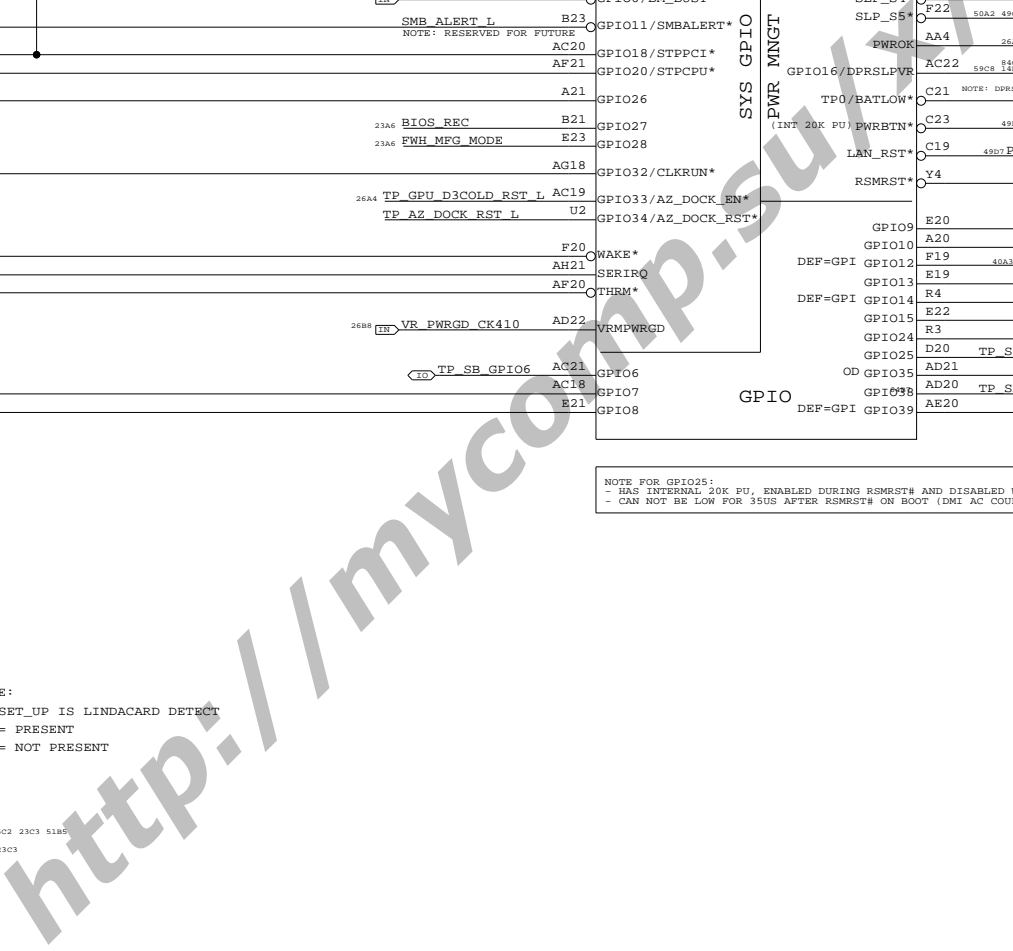
945 External Design Spec says reserved =PP3V3_S0_NB NBCFG_SDVO_AND_PCIE	
NB_CFG<20> PCIe Backward Interop. Mode	High = Both active Low = Only SDVO or PCIe x1
1486_NB_CFG<20> Internal pull-down	

PROBABLY NOT NEEDED

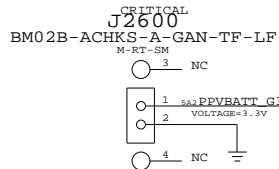
NB Config Straps		
SYNC_MASTER=(MASTER)		SYNC_DATE=(MASTER)
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	SCALE NONE	SHT 20	OF 84



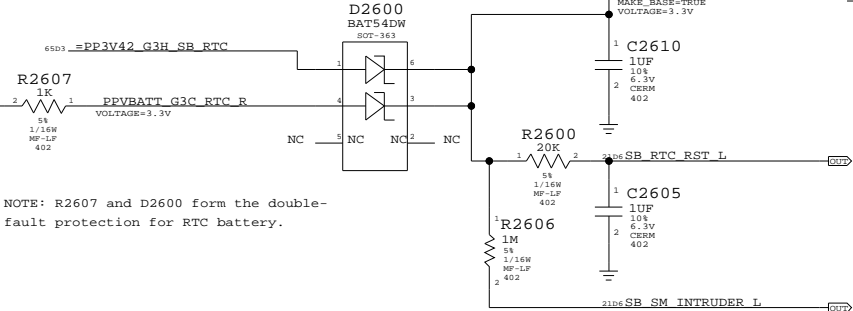


RTC Battery Connector



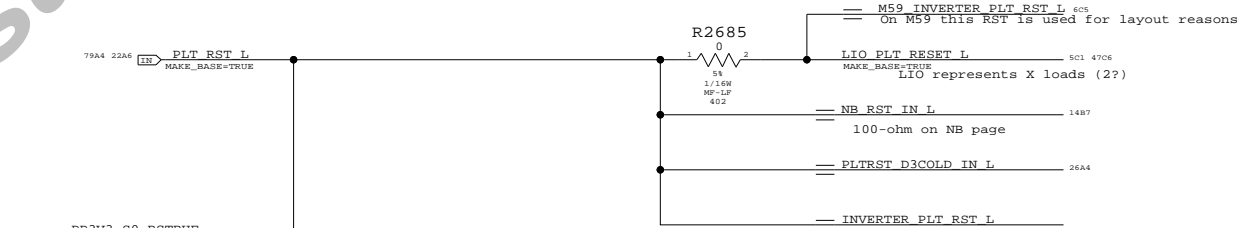
518S0452

NOTE: R2607 and D2600 form the double-fault protection for RTC battery.

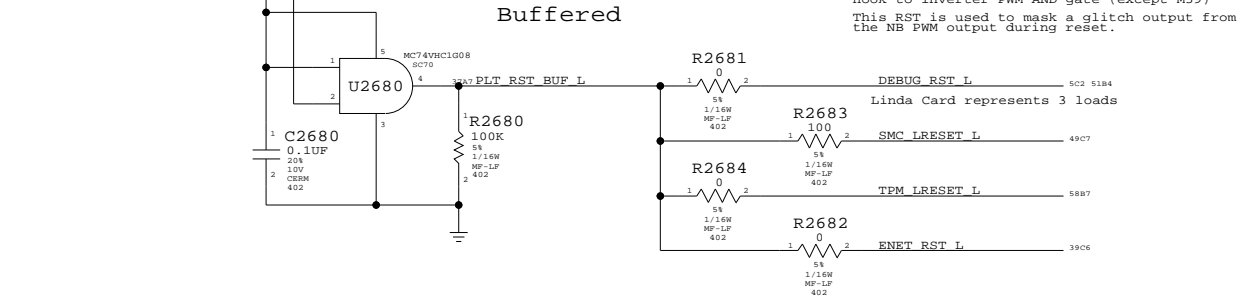


Platform Reset Connections

Unbuffered

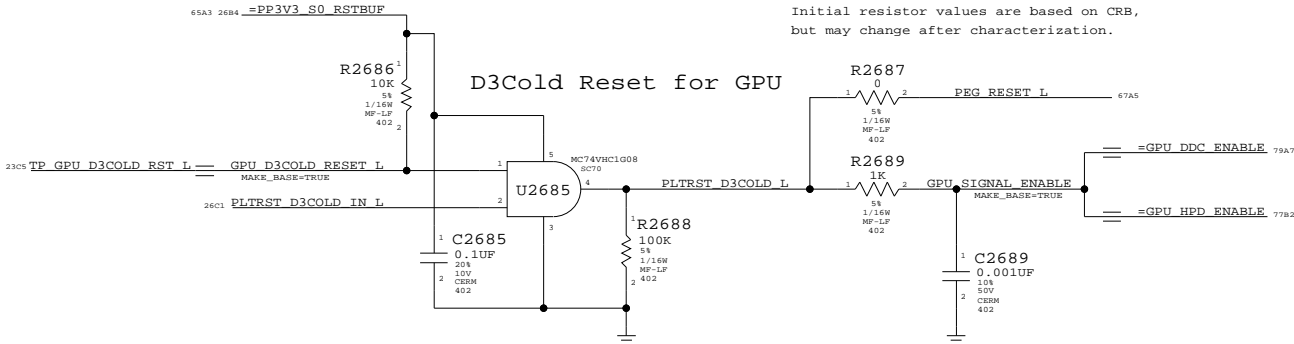


Buffered



Initial resistor values are based on CRB, but may change after characterization.

D3Cold Reset for GPU



SB Misc

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

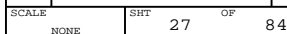
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SIZE	DRAWING NUMBER	REV.
D	051-7164	A.0.0
SCALE	SHT	OF
NONE	26	84



Page Notes

Power aliases required by this page:

- =PPIV8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:

- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

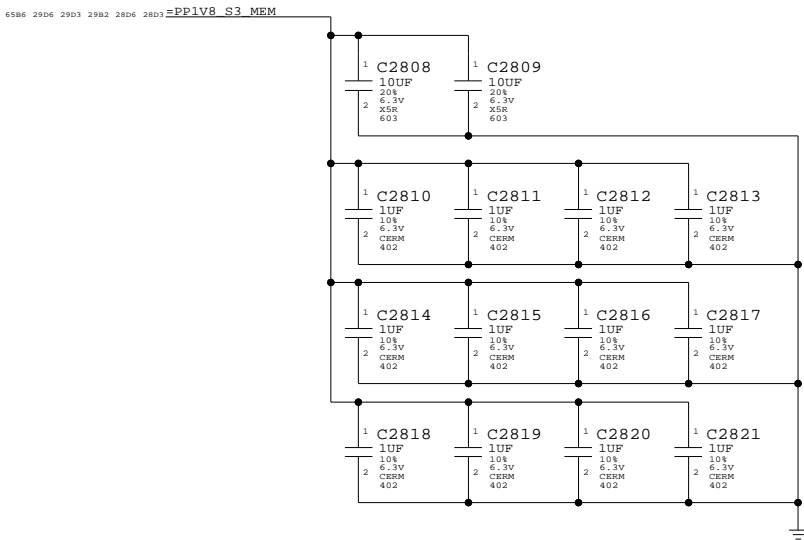
BOM options provided by this page:

(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided by another page.

"Expansion" (surface-mount) slot

DDR2 Bypass Caps
(For return current)



DDR2 SO-DIMM Connector A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE	SHT	OF
NONE	28	84

Page Notes

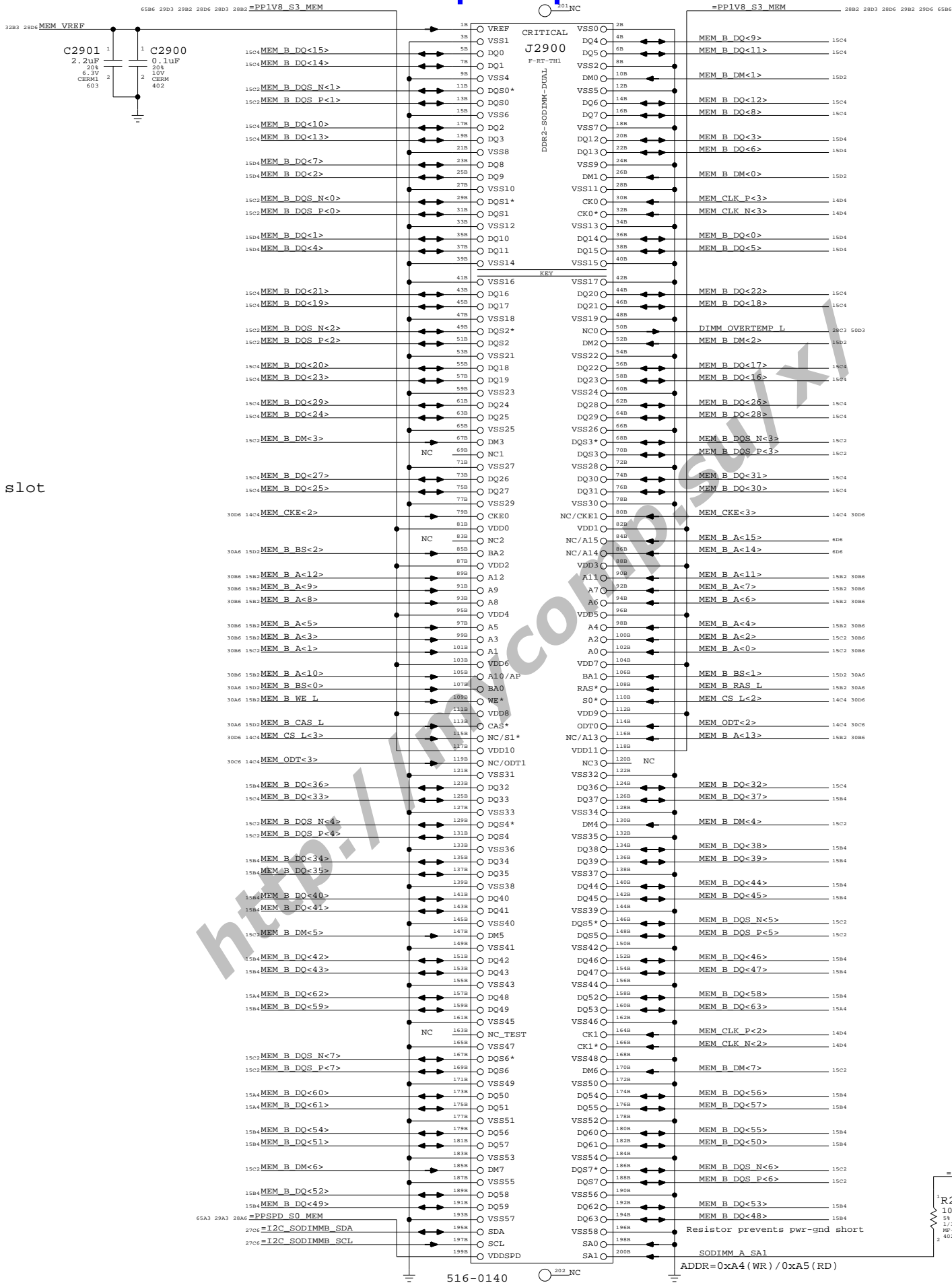
Power aliases required by this page:
- =PPIV8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

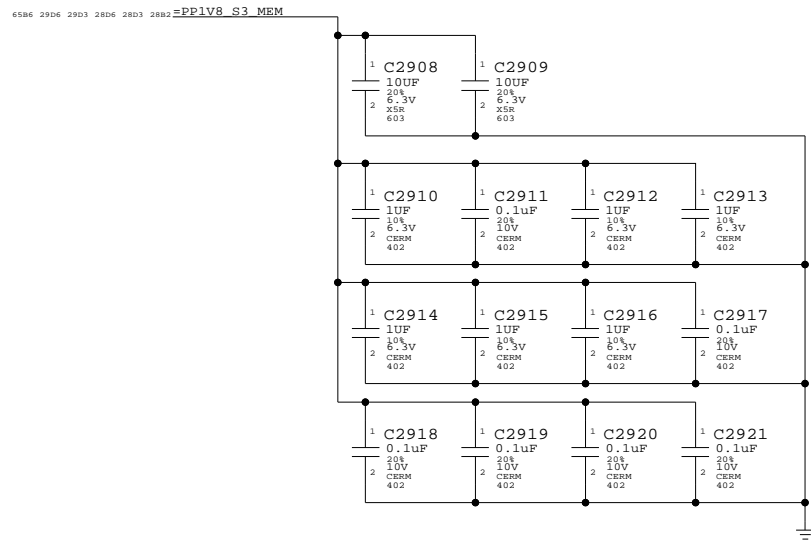
BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided by another page.

"Factory" (thru-hole) slot



DDR2 Bypass Caps
(For return current)



DDR2 SO-DIMM Connector B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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	SCALE NONE	SHT 29	OF 84

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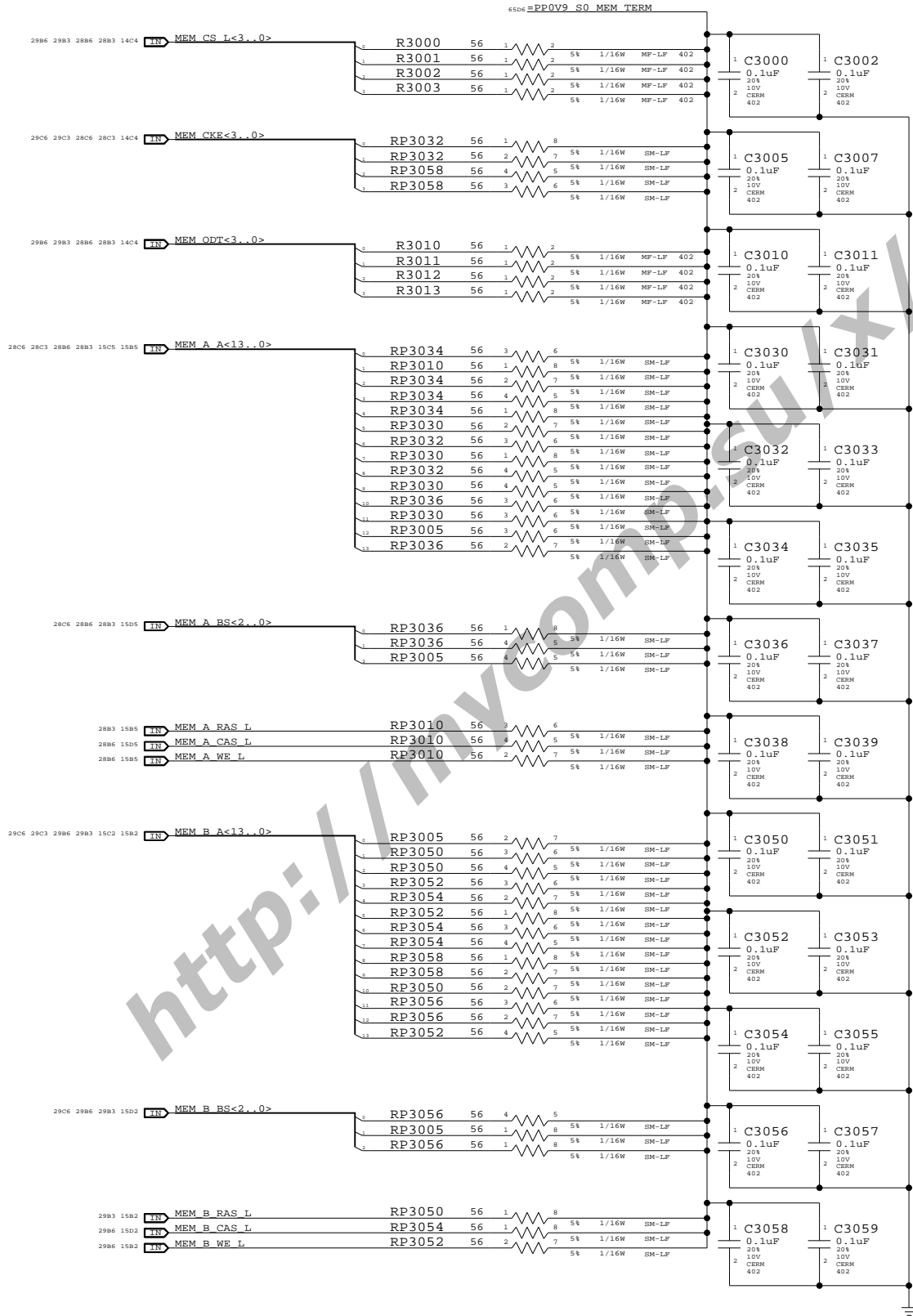
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One cap for each side of every RPAK, one cap for every two discrete resistors
Ensure CS_L and ODT resistors are close to SO-DIMM connector



Memory Active Termination

SYNC_MASTER=(MASTER)SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7150	A.0.0
SCALE	SHT	OF	
NONE	30	84	

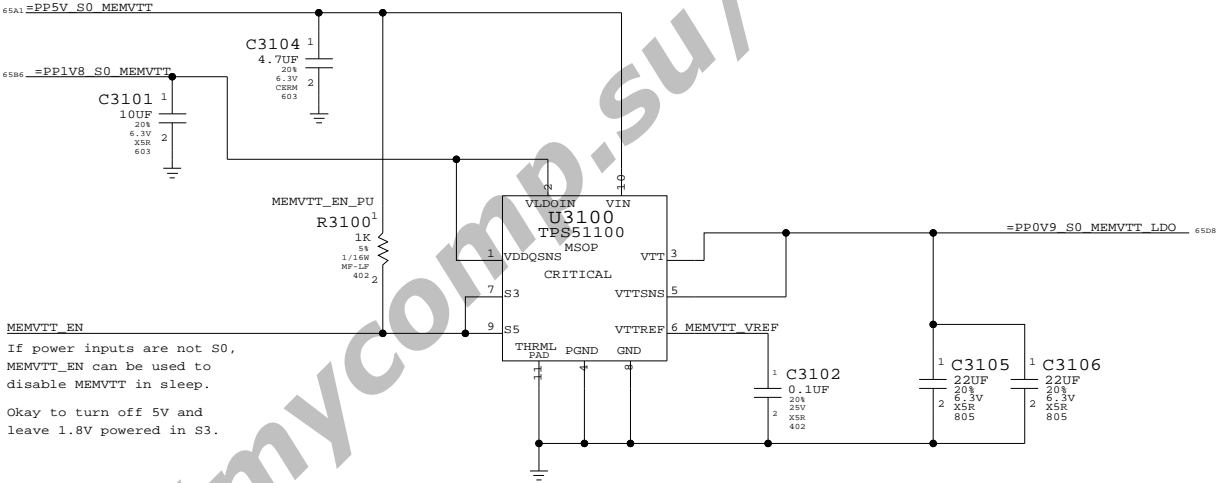
Page Notes

Power aliases required by this page:
- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

DDR2 Vtt Regulator



Memory Vtt Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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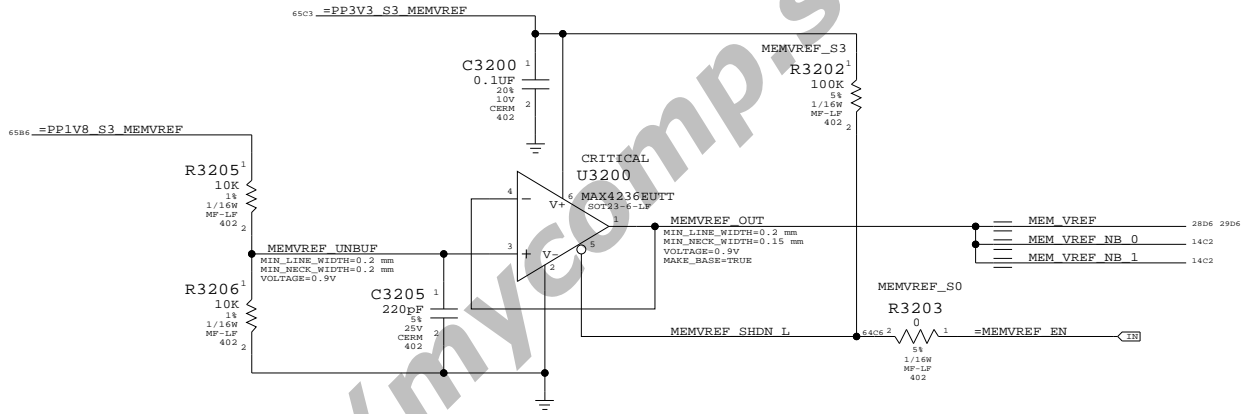
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE	SHT	OF
NONE	31	84



DDR2 Vref

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7150	A.0.0
SCALE		SHT	OF
NONE		32	84

D

C

B

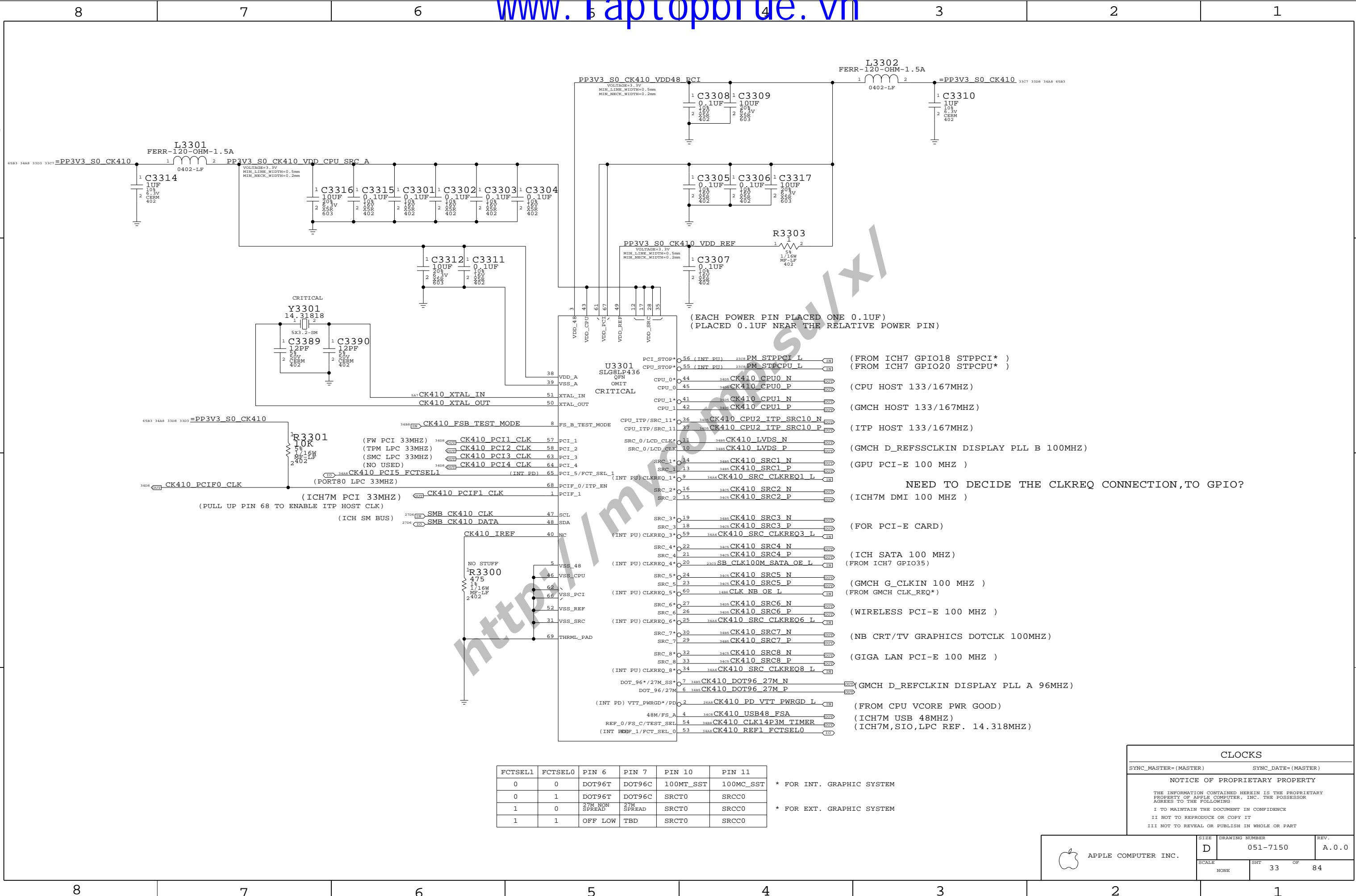
A

D

C

B

A



FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST
0	1	DOT96T	DOT96C	SRCT0	SRCC0
1	0	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0
1	1	OFF LOW	TBD	SRCT0	SRCC0

* FOR INT. GRAPHIC SYSTEM

* FOR EXT. GRAPHIC SYSTEM

CLOCKS

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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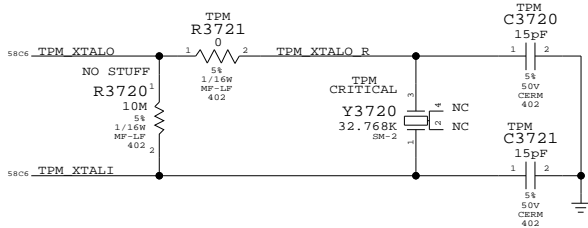
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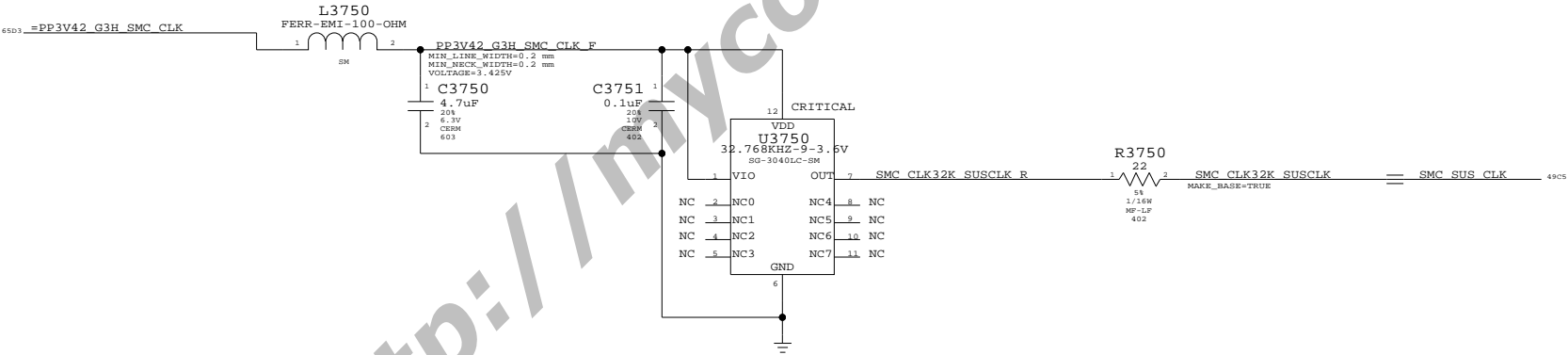
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE	SHT	OF
NONE	33	84

TPM Crystal Circuit



SMC G3Hot Oscillator



Mobile Clocking

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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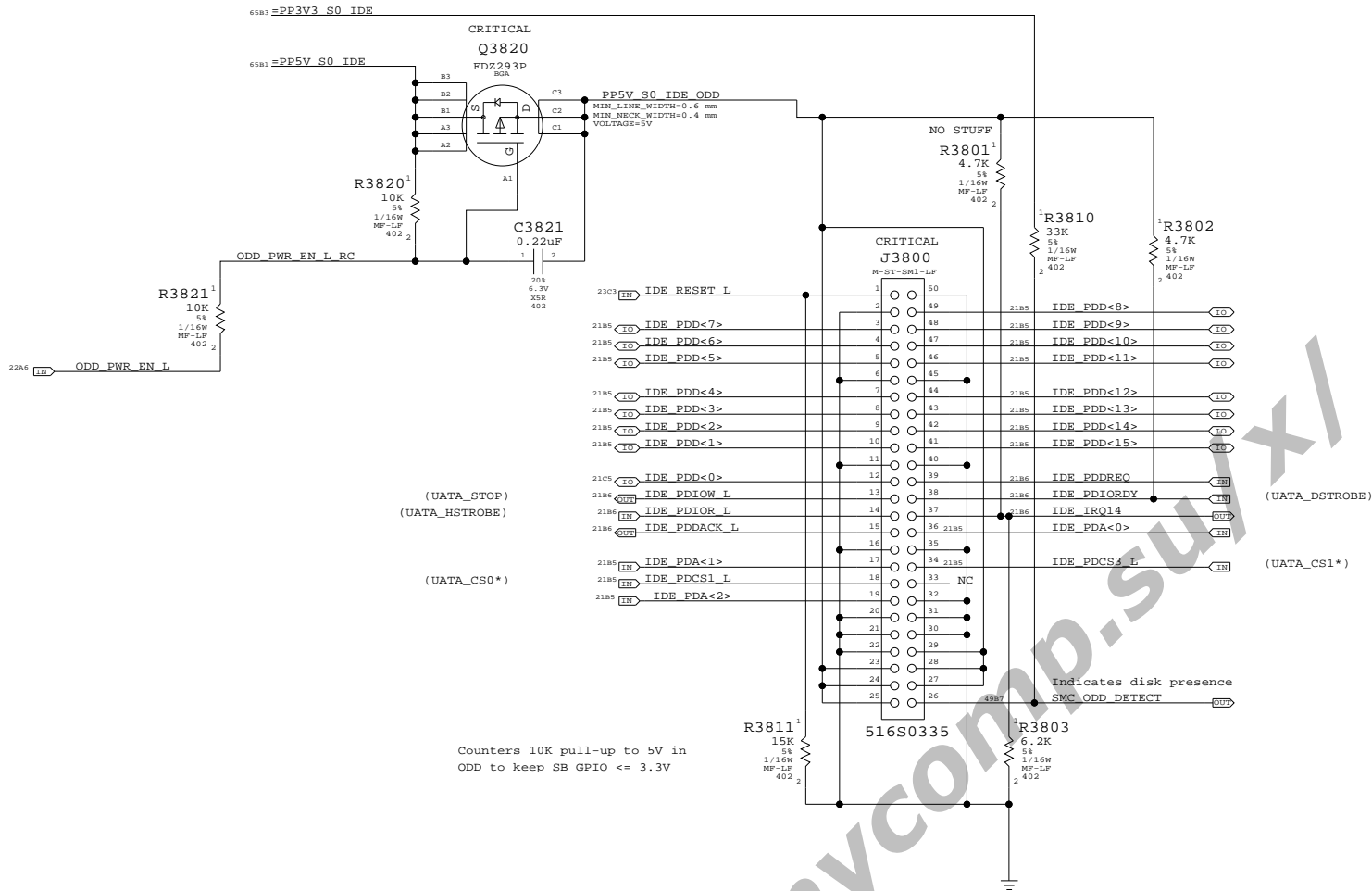
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7150	A.0.0
SCALE		SHT	OF
NONE		35	84

IDE (ODD) Connector



PATA Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

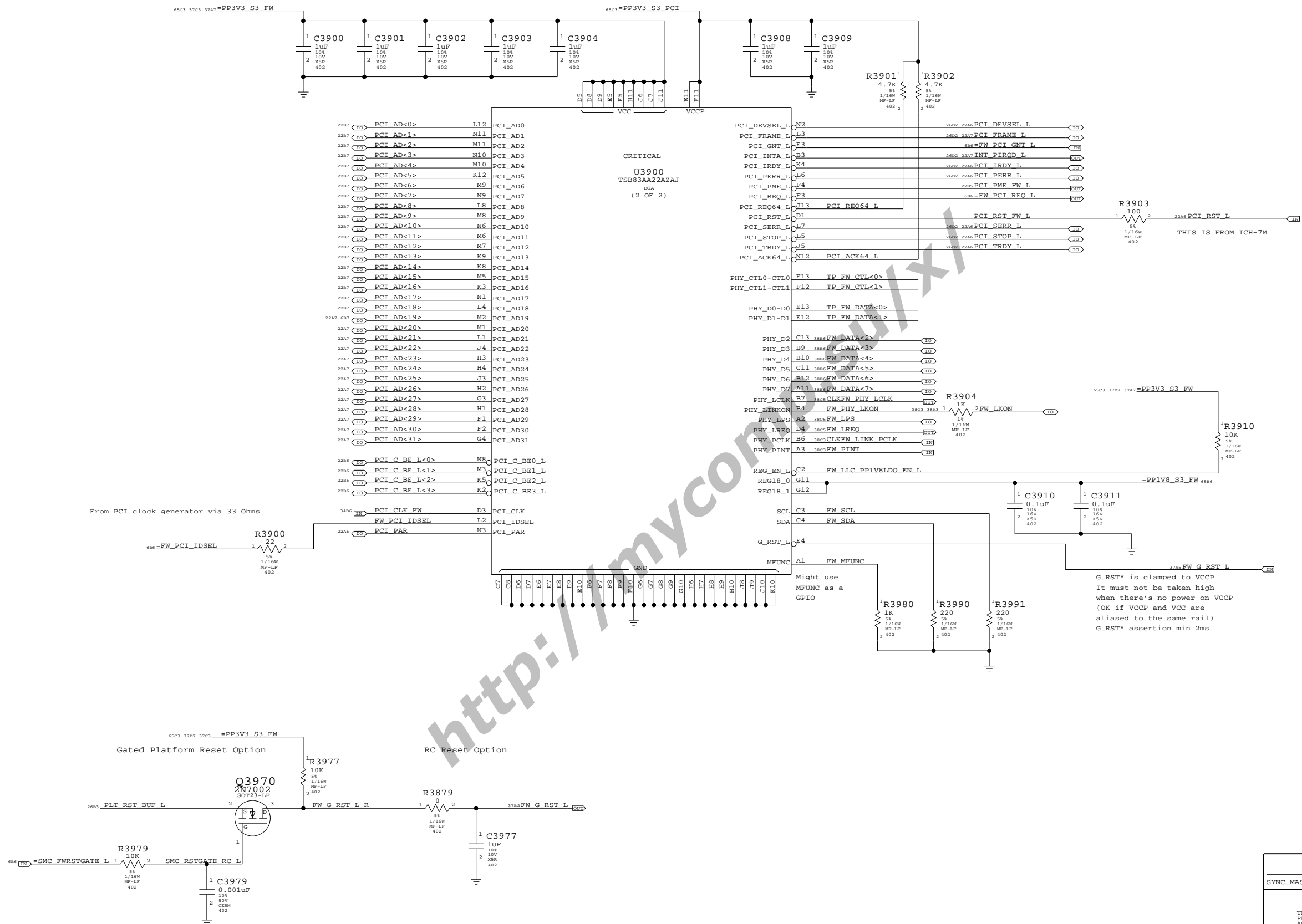
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7150	REV. A.0.0
	SCALE NONE	SHT 36	OF 84



FireWire Link (TSB83AA22)

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

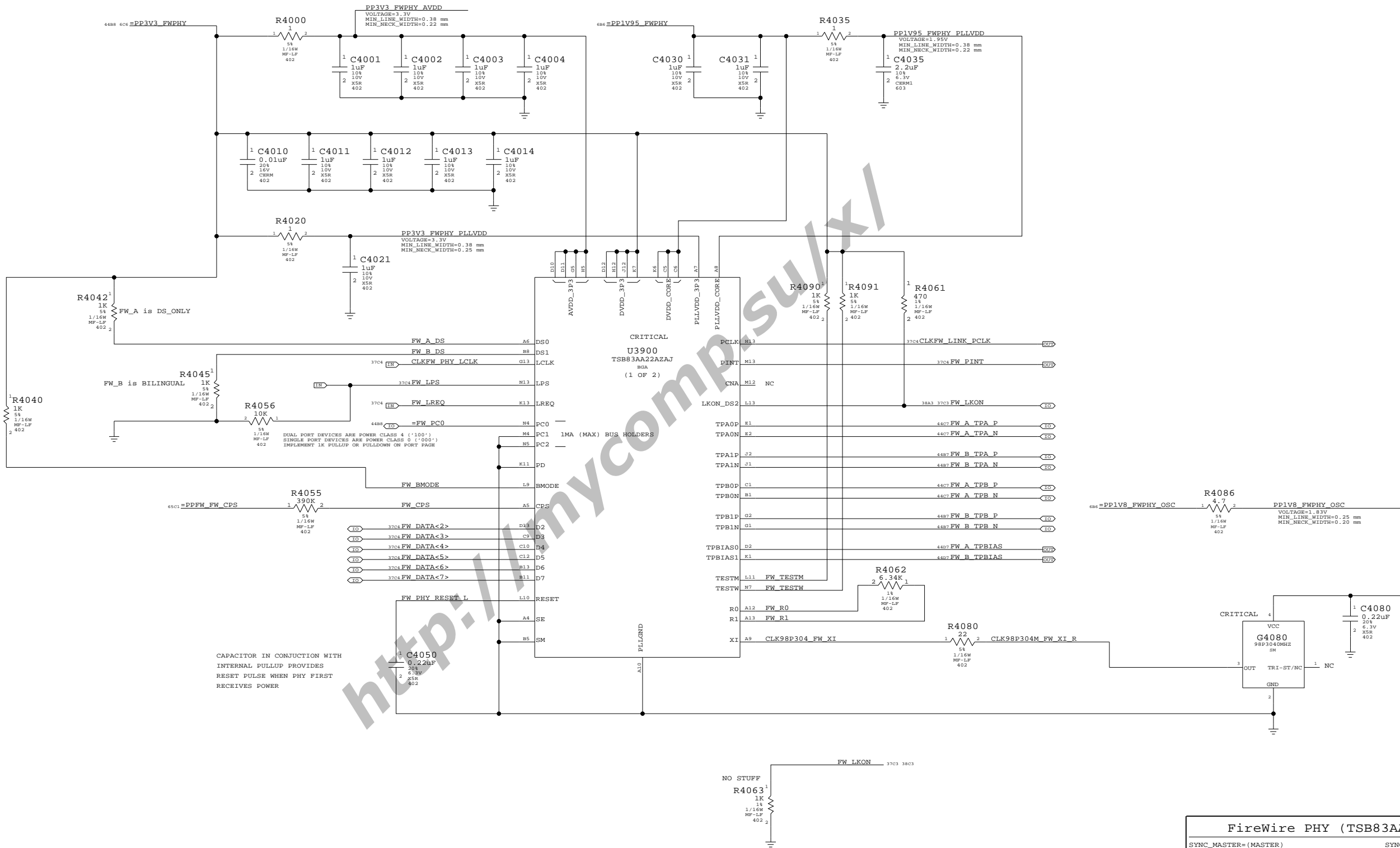
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FireWire PHY (TSB83AA22)

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE	SHT	OF
NONE	38	84



NONE	11	11
------	----	----

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		PHYSICAL	
		SPACING			
PROVIDED		ENETCONN	ENET_100D	ENETCONN_P<0>	40D3
			ENET_100D	ENETCONN_N<0>	40C3
			ENET_100D	ENETCONN_P<1>	40C3
BY		ENETCONN	ENET_100D	ENETCONN_N<1>	40C3
			ENET_100D	ENETCONN_P<2>	40C3
			ENET_100D	ENETCONN_N<2>	40C3
ETHERNET		ENETCONN	ENET_100D	ENETCONN_P<3>	40C3
			ENET_100D	ENETCONN_N<3>	40C3
			ENET_100D	ENETCONN_P<4>	40B3
PHY		ENETCONN	ENET_100D	ENETCONN_N<4>	40B3
			ENET_100D	ENETCONN_P<5>	40B3
			ENET_100D	ENETCONN_N<5>	40B3

Page Notes

Power aliases required by this page:

- =PP2V5_ENET
- =GND_CHASSIS_ENET

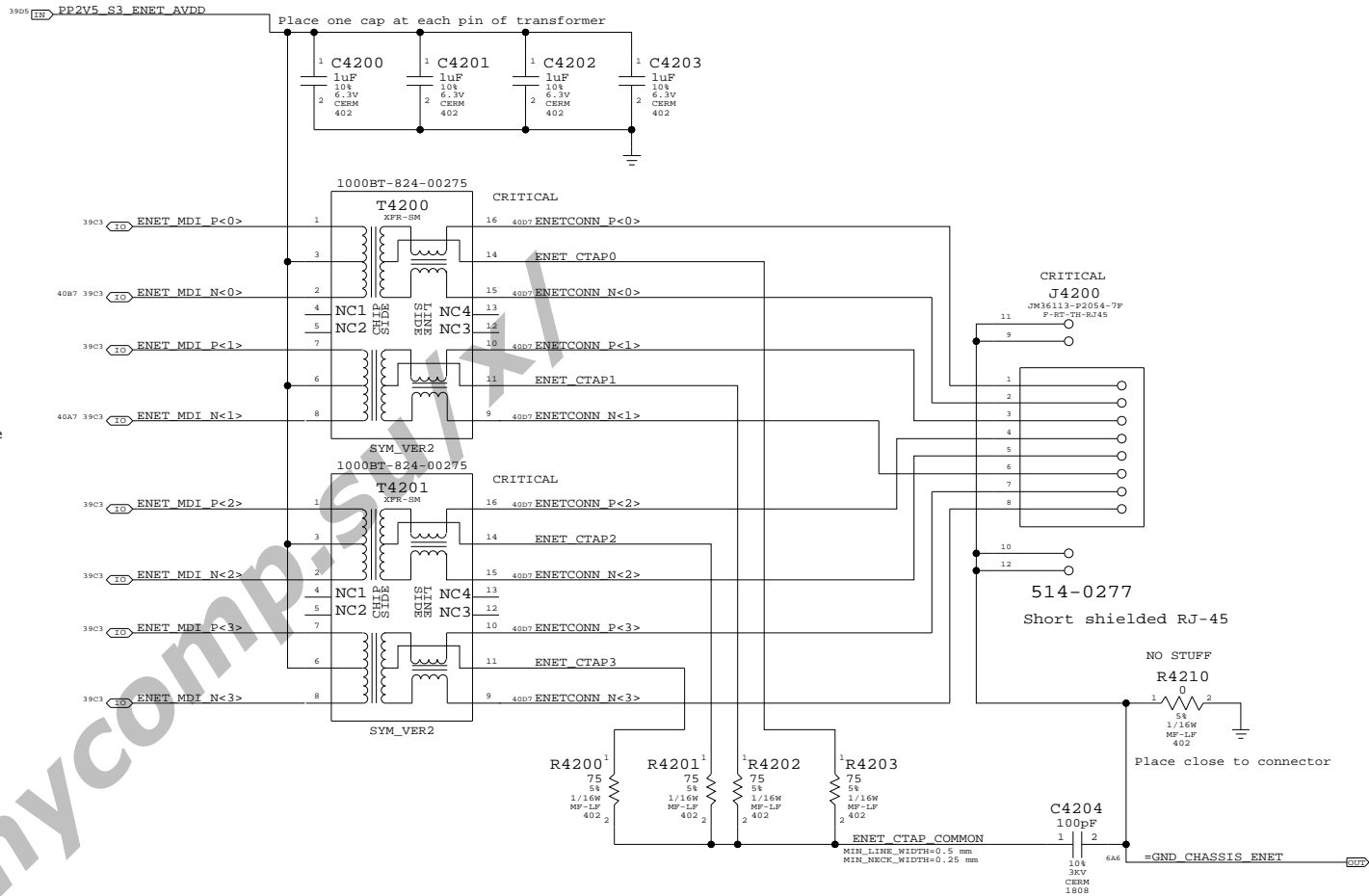
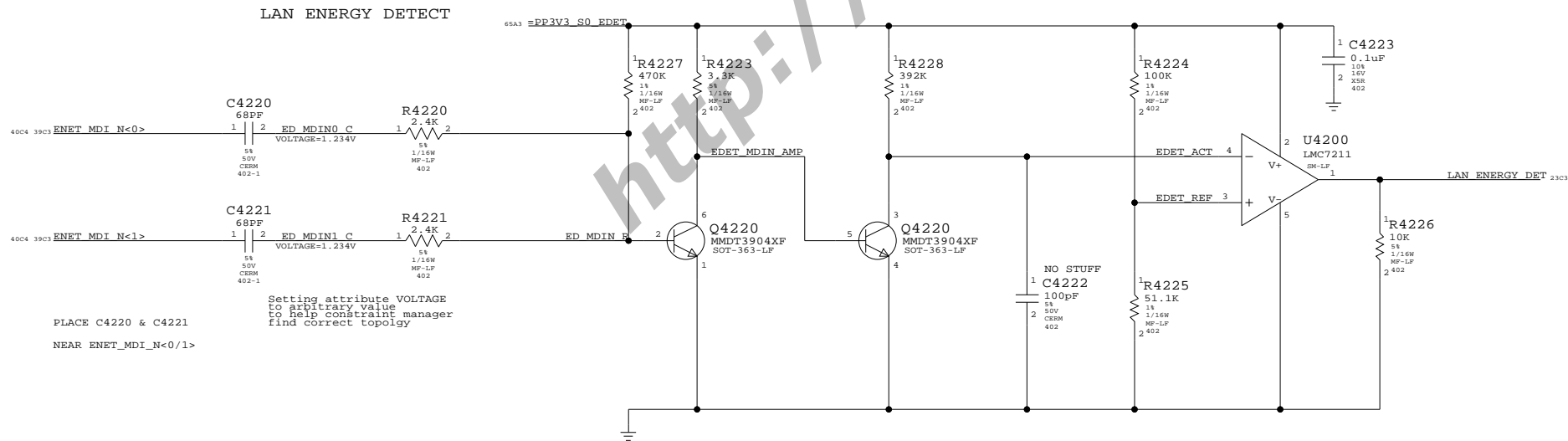
Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

Transformers should be mirrored on opposite sides of the board



Ethernet Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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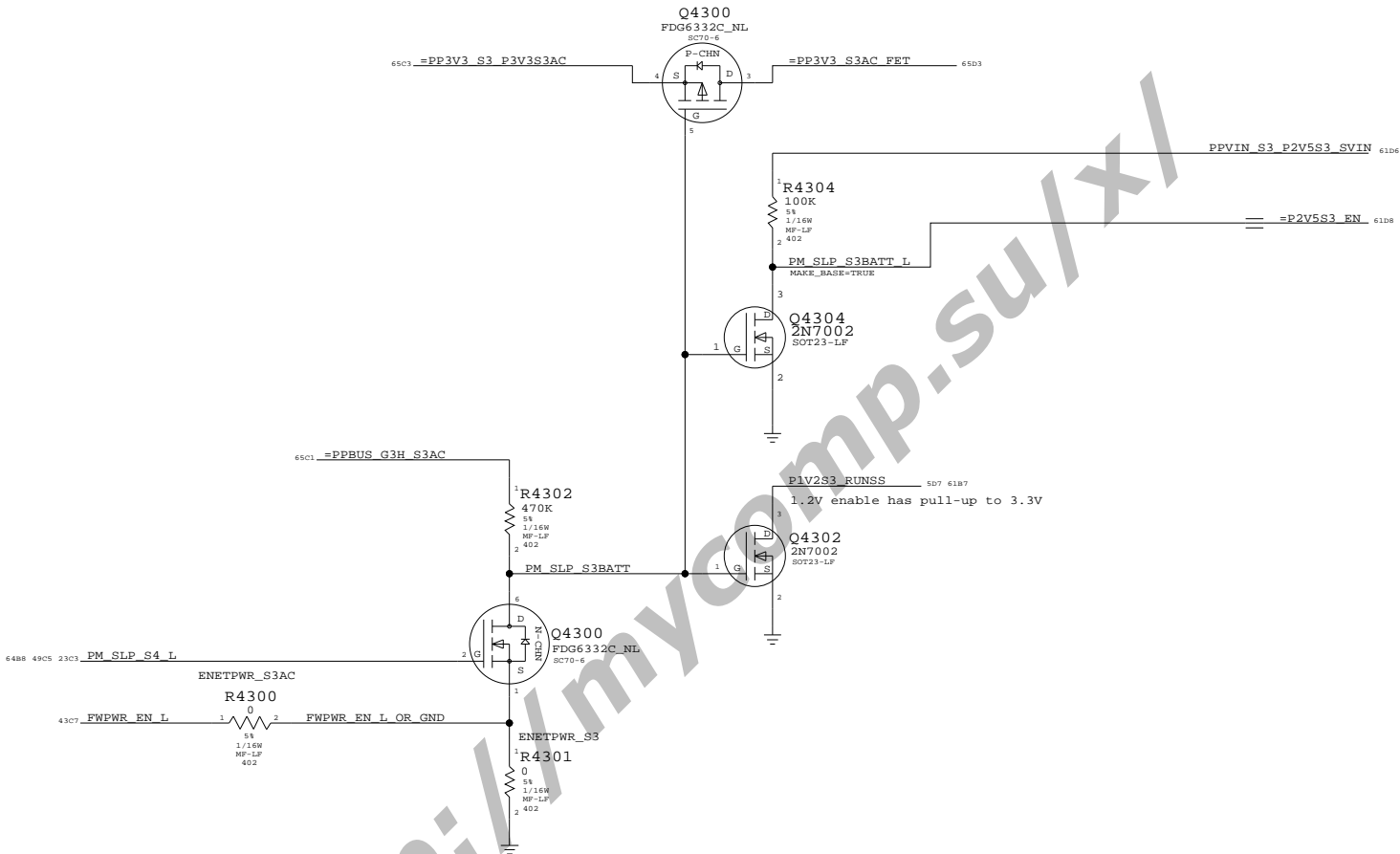


APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE	SHT	OF
NONE	40	84

Yukon Power Control

Allows powering Yukon down during battery sleep to save power



When ENETPWR_S3AC BOMOPTION is active:

State	FWPWR_EN_L	PM_SLP_S4_L	PM_SLP_S3BATT	PM_SLP_S3BATT_L	P2V5S3_EN	P1V2S3_RUNSS
S0 AC	0V	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S0 Batt	0V	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S3 AC	0V	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S3 Batt	PBUS	3.3V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)
S5 AC	0V	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)
S5 Batt	PBUS	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)
G3H Batt	PBUS	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)

When ENETPWR_S3 BOMOPTION is active:

State	PM_SLP_S4_L	PM_SLP_S3BATT	PM_SLP_S3BATT_L	P2V5S3_EN	P1V2S3_RUNSS
S0	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S3	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S5	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)
G3H	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)

Yukon Power Control

SYNC_MASTER=(MASTER)

SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.

SIZE

D

DRAWING NUMBER

051-7150

REV.

A.0.0

SCALE

NONE

SHT

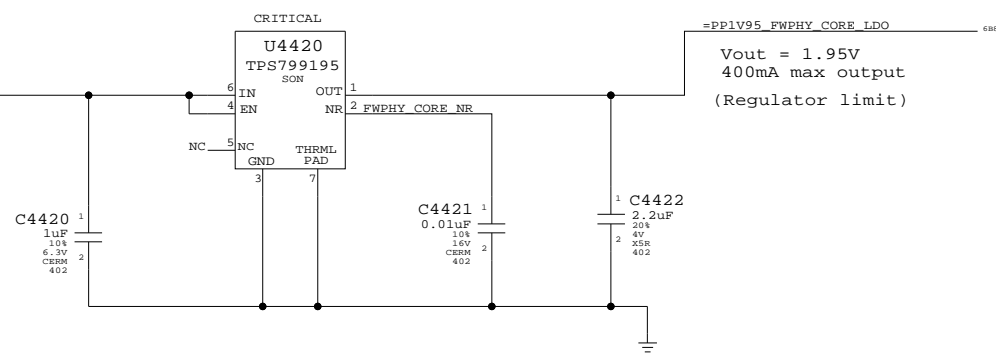
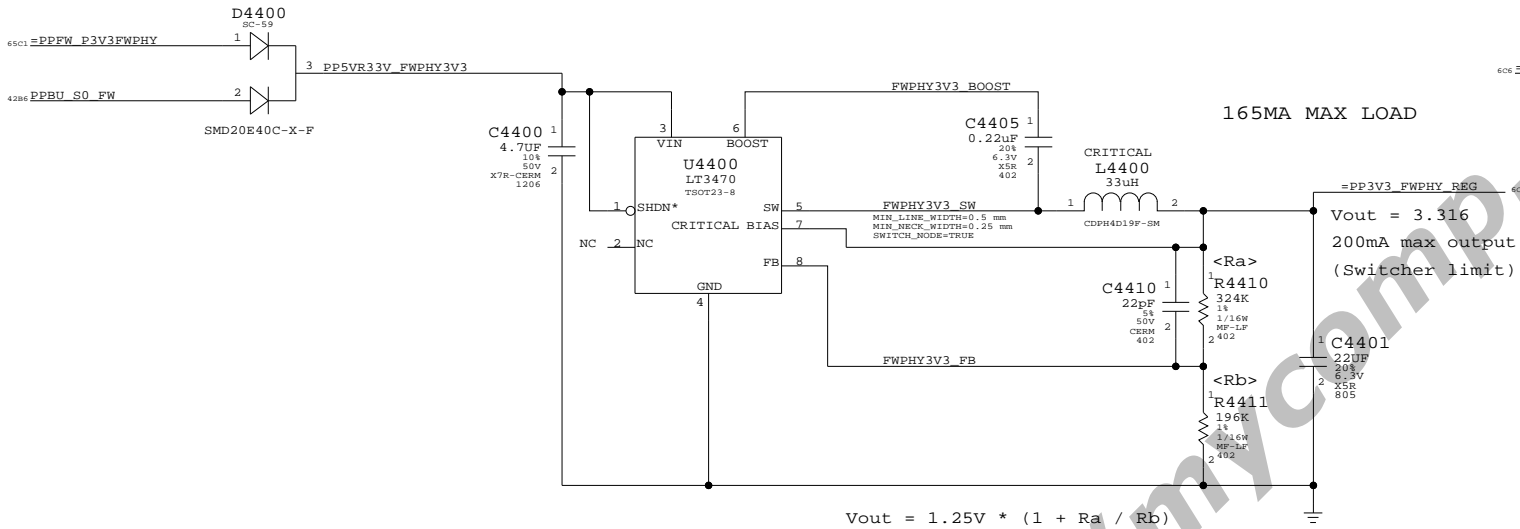
41

OF

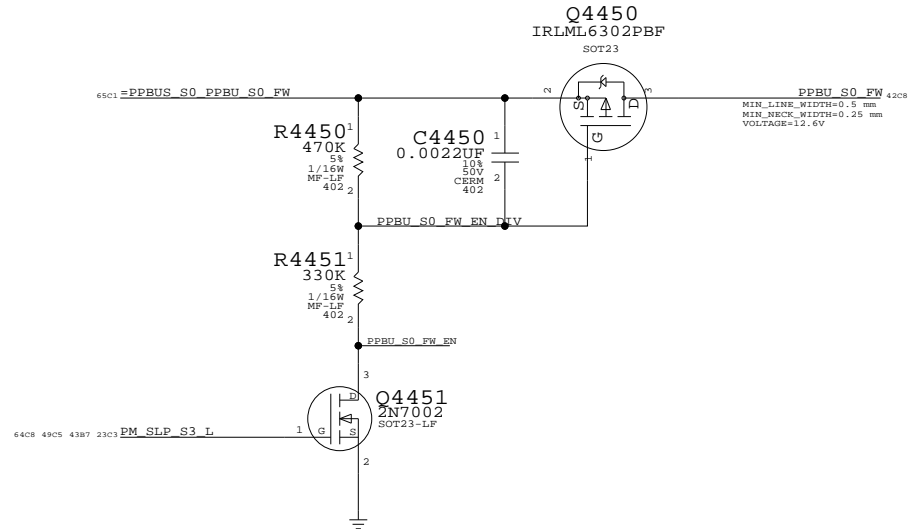
84

3.3V Supply for FWPHY

1.95V Supply for FW PHY



PBUS S0 FET



FW PHY Power Supply

SYNC_MASTER=(MASTER)SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7150	A.0.0
SCALE		SHT	OF
NONE		42	84

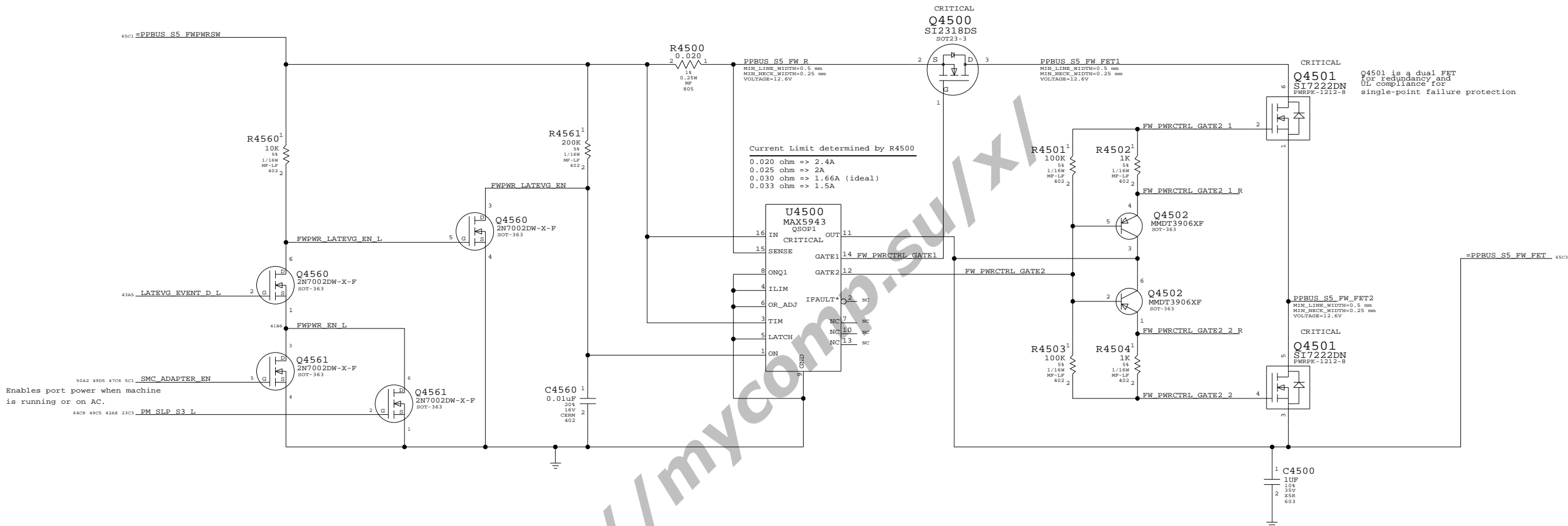
Page Notes

Power aliases required by this page:
- =PPBUS_S0_FWPWRSW (system supply for bus power)
- =PP3V3_S0_FWPORTPWRSW

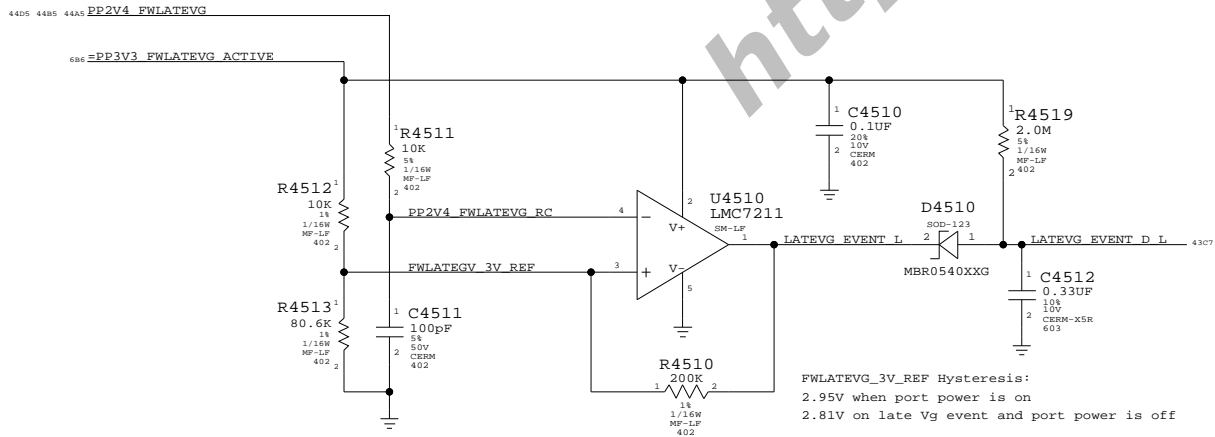
Signal aliases required by this page:
- =FWPWR_PWRON (see related text note below)

BOM options provided by this page:
(NONE)

Current Limit/Active Late-VG Protection



Late-VG Event Detection



FireWire Port Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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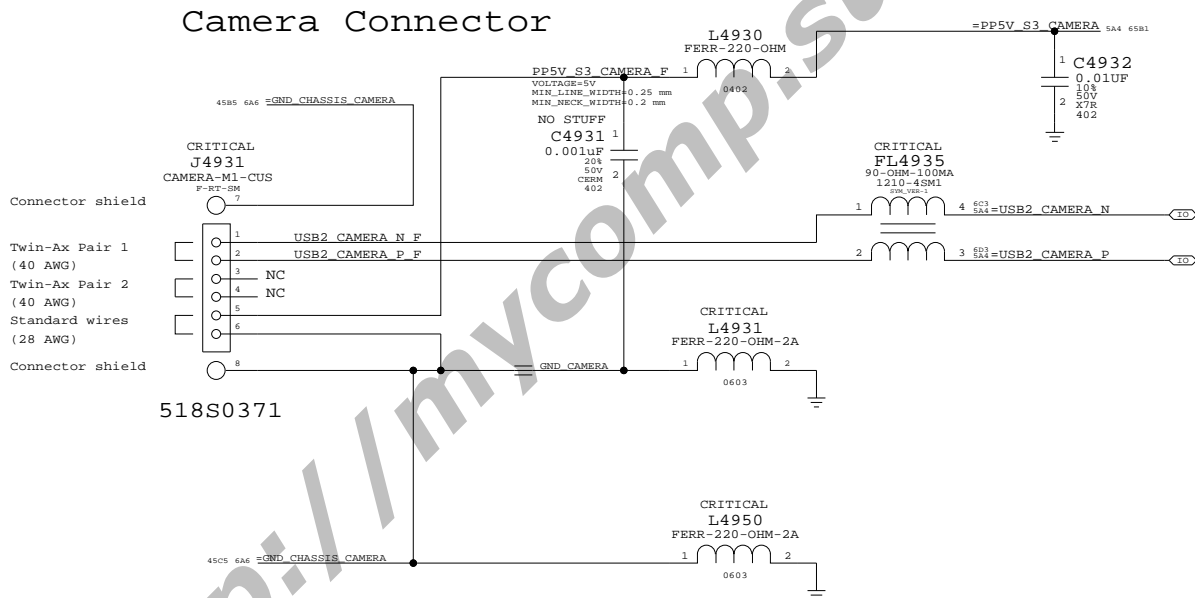
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE	SHT	OF
NONE	43	84



Camera Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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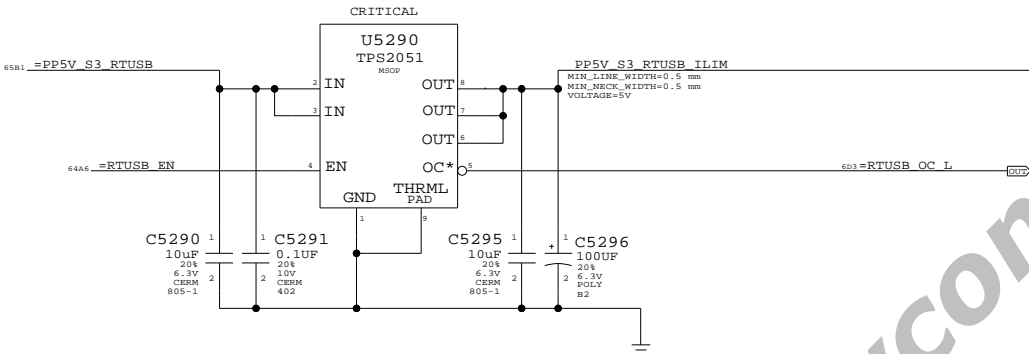
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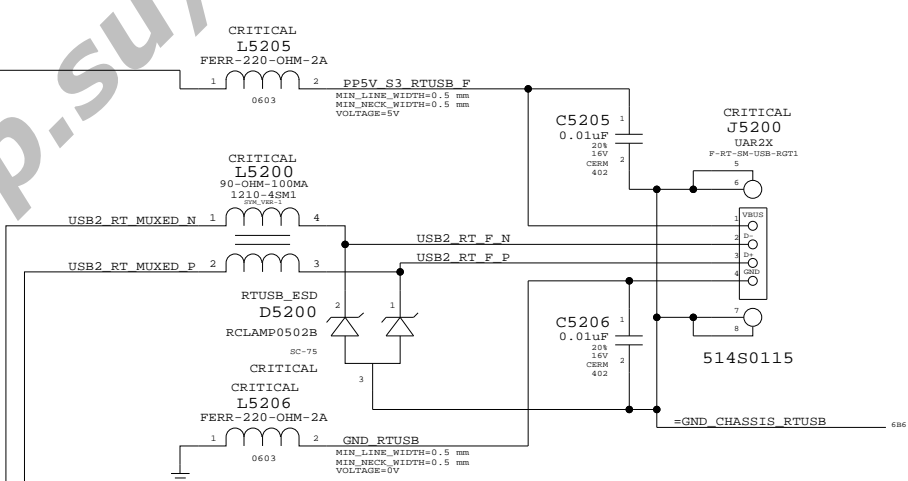
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7150	A.0.0
SCALE		SHT	OF
NONE		45	84

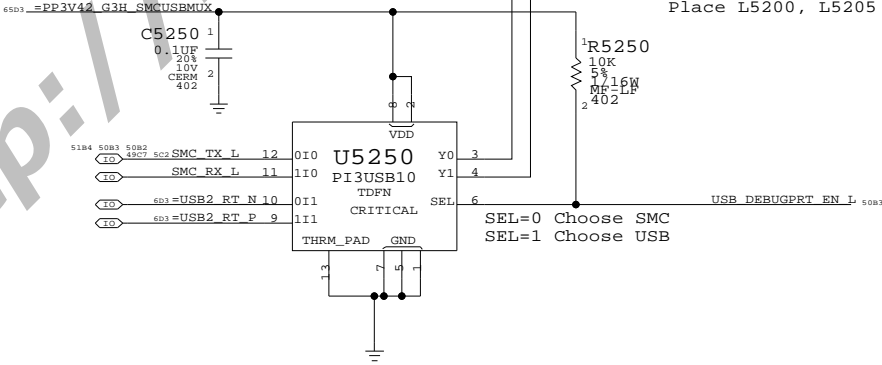
Port Power Switch



Right USB Port



USB/SMC Debug Mux



Place L5200, L5205 and L5206 across moat

External USB Connector

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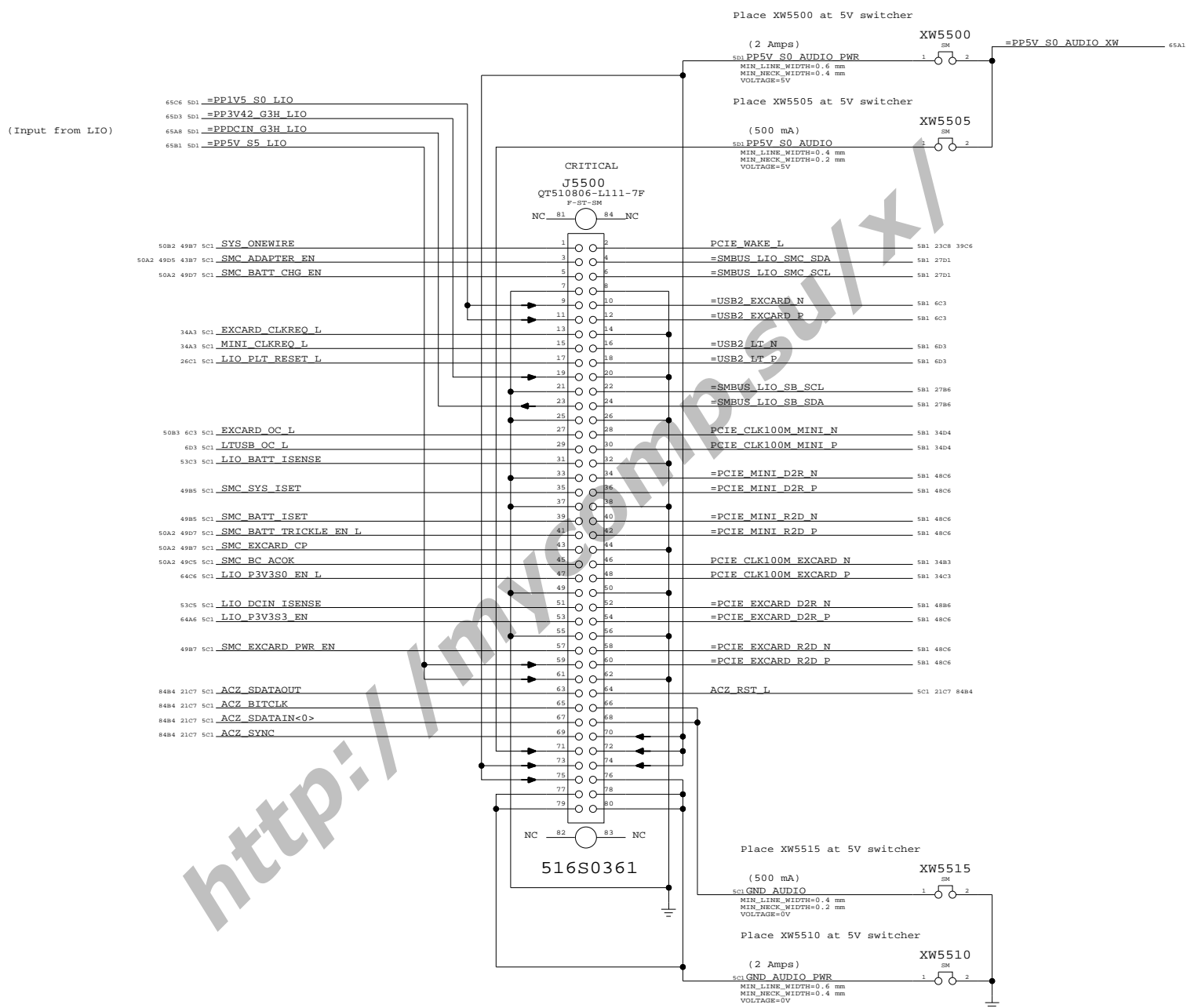
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE	SHT	OF
NONE	46	84

Left I/O Board Connector



Left I/O Board Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7150	A.0.0
SCALE		SHT	OF
NONE		47	84

D

D

C

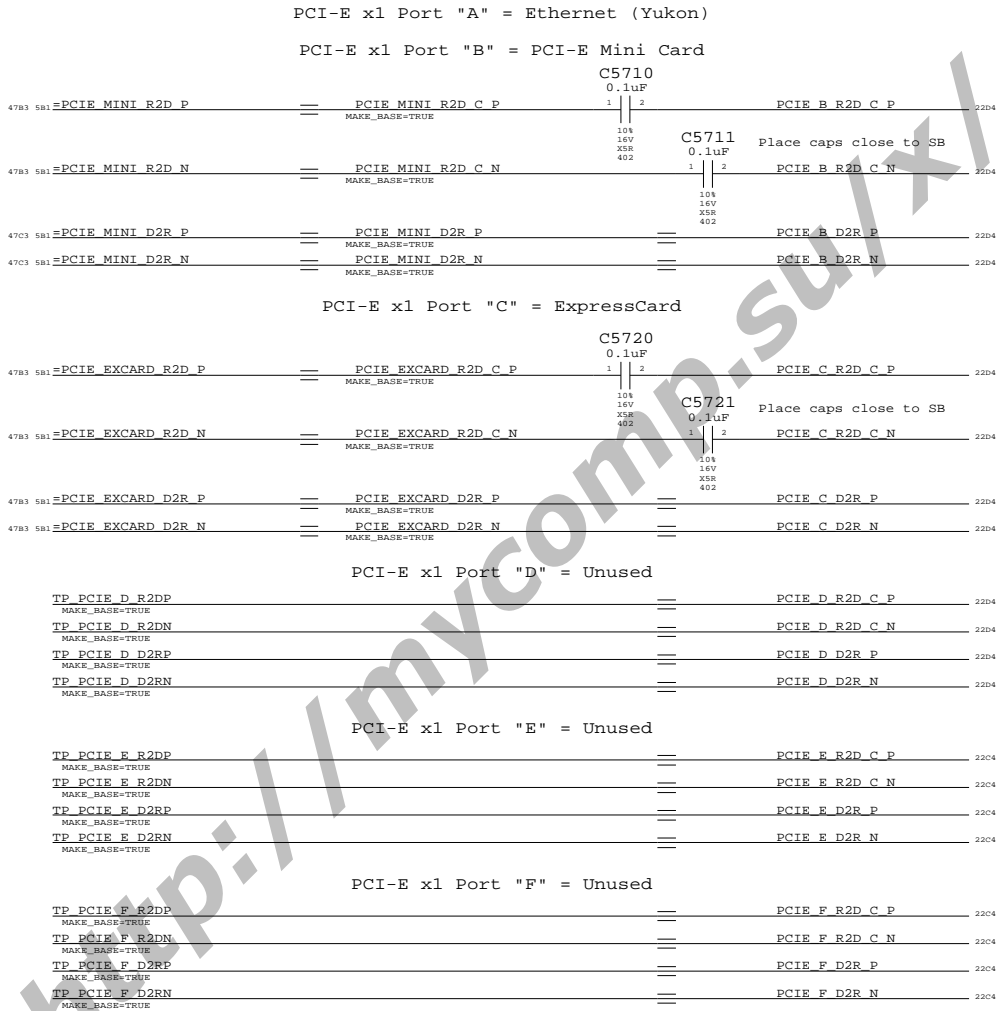
C

B

B

A

A



PCI-E Connections

SYNC_MASTER=(MASTER)SYNC_DATE=(MASTER)

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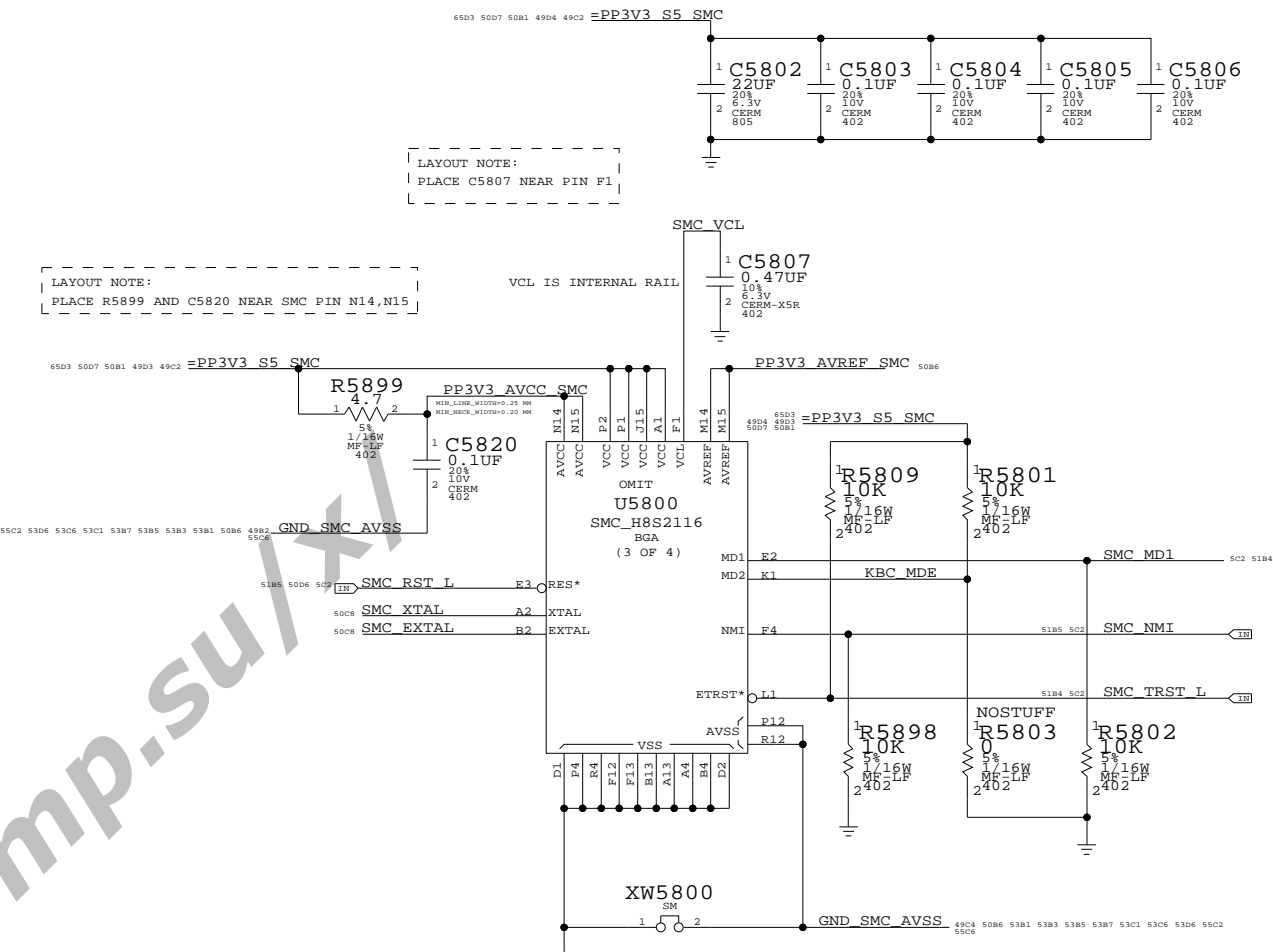
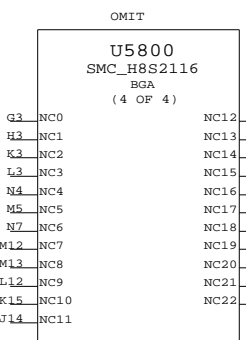
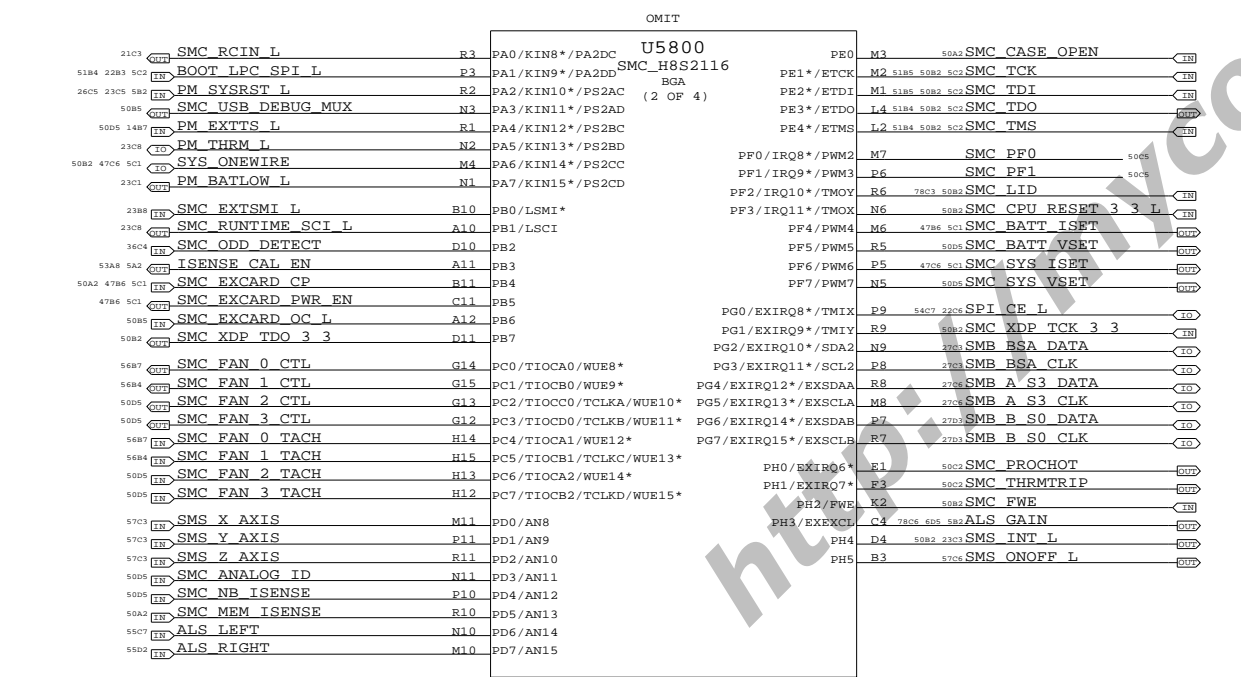
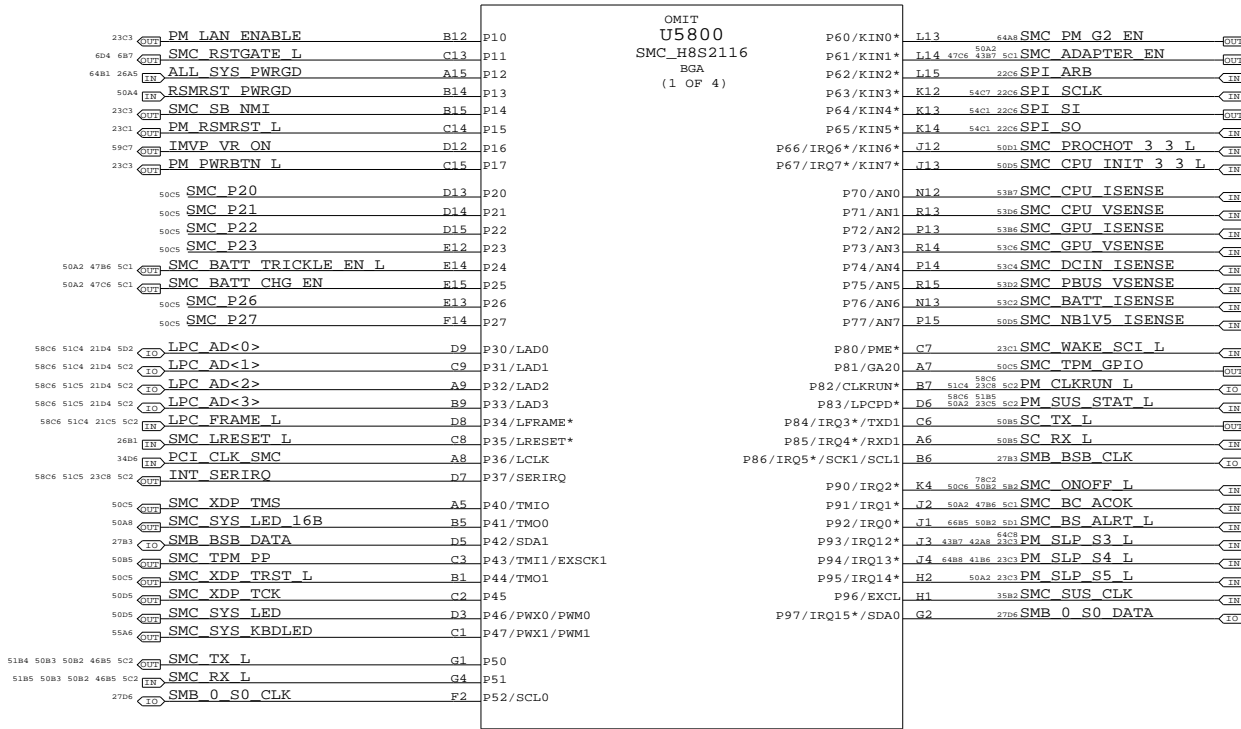
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APPLE COMPUTER INC.

SIZE	D	DRAWING NUMBER	051-7150	REV.	A.0.0
SCALE	NONE	SHT	48	OF	84

UNUSED PINS HAVE THE FORMAT SMC XXX WHERE XXX IS THE PORT NUMBER. THEY ARE SET BY SOFTWARE TO BE DRIVEN OUTPUTS ALWAYS SO THEY CAN BE LEFT NO-CONNECTED.

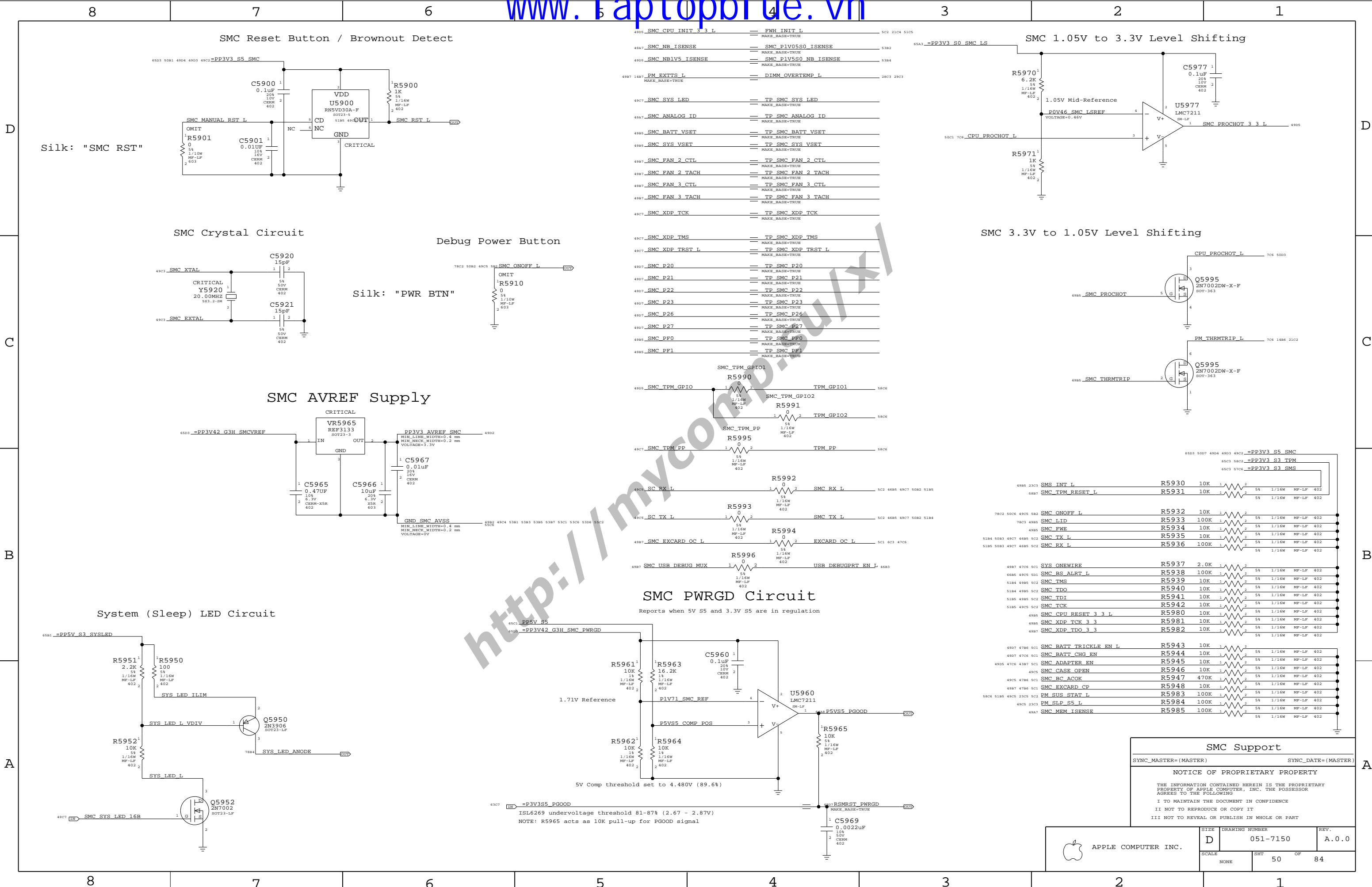


SMC

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7150	A.0.0
SCALE	SHT		
	NONE	49	OF 84



SMC Support

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

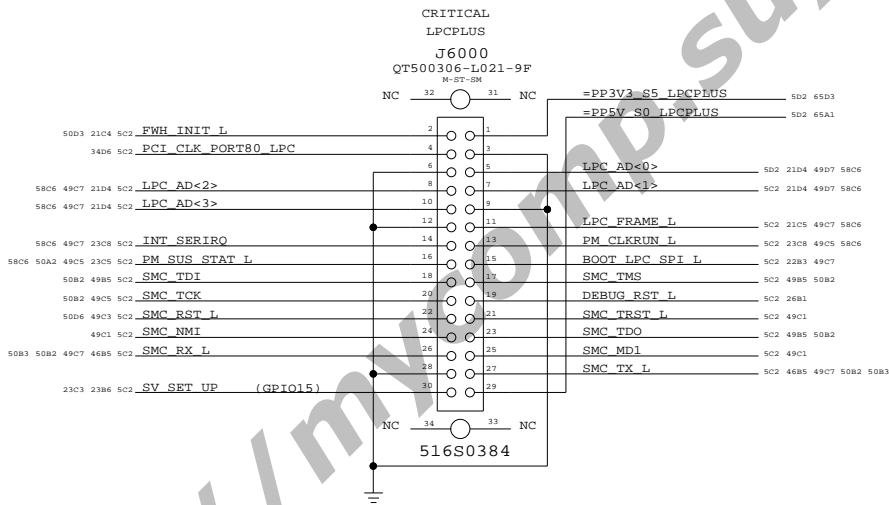
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LPC+ Debug Connector

SYNC_MASTER=(MASTER)SYNC_DATE=(MASTER)

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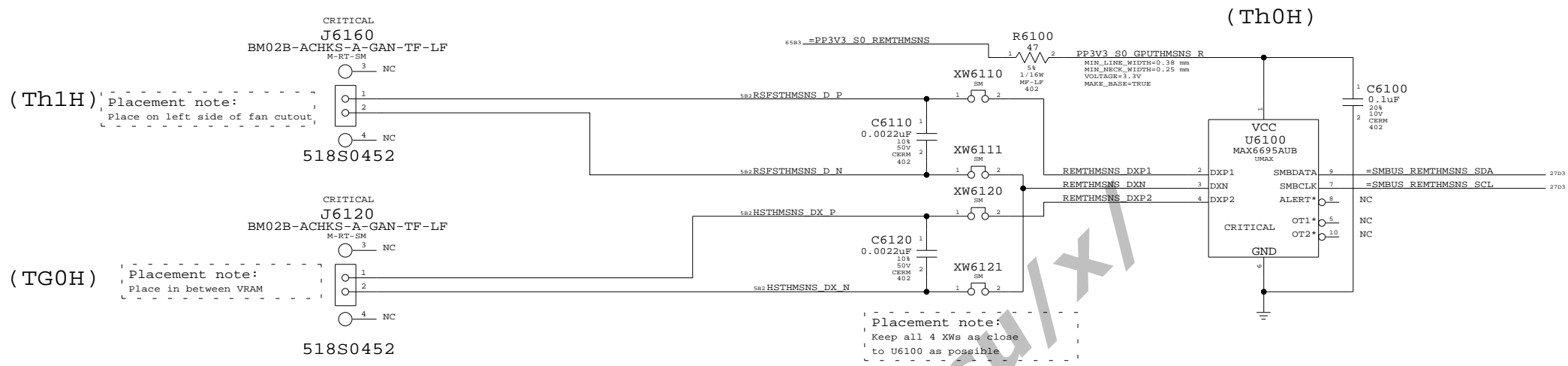
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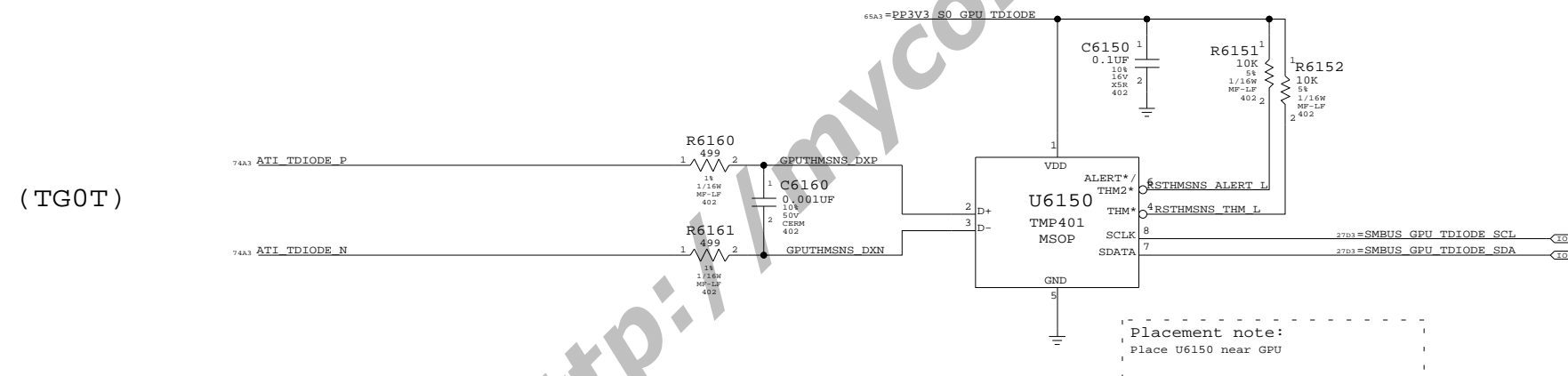
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7150	REV. A.0.0
	SCALE NONE	SHT 51	OF 84

GPU/Heat Pipe & Bottom Case Skin Thermal Sensor



GPU Die Thermal Sensor



Thermal Sensors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

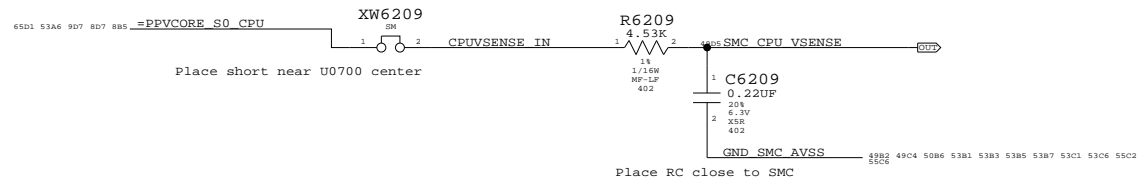
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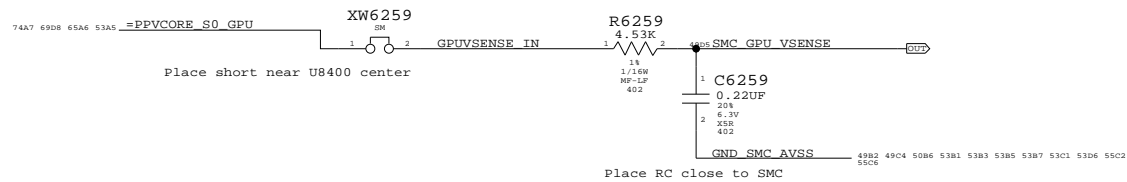
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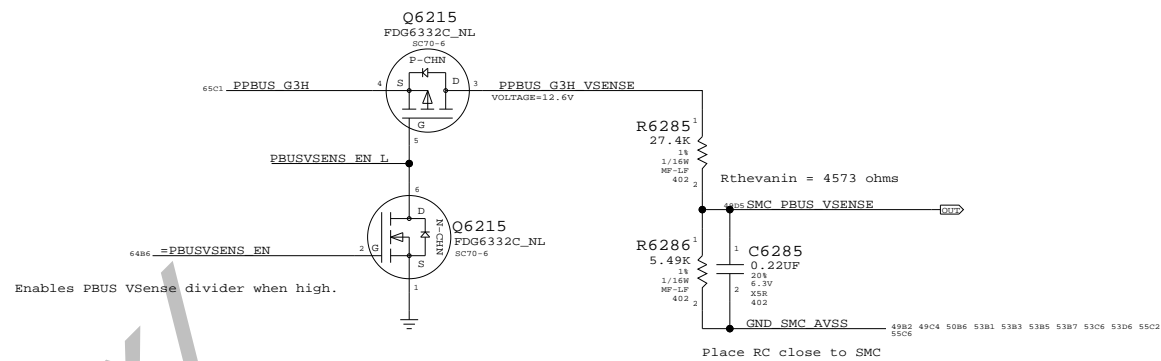
CPU Voltage Sense / Filter



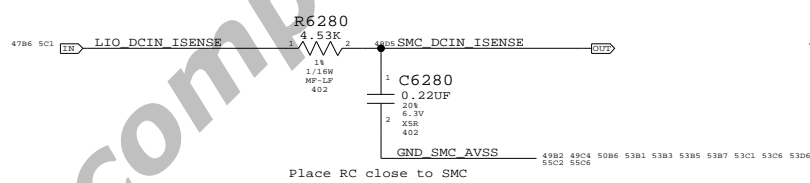
GPU Voltage Sense / Filter



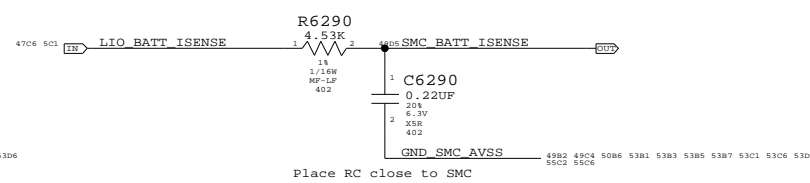
PBUS Voltage Sense Enable & Filter



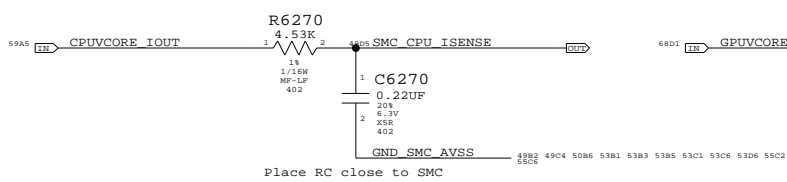
DCIN Current Sense Filter



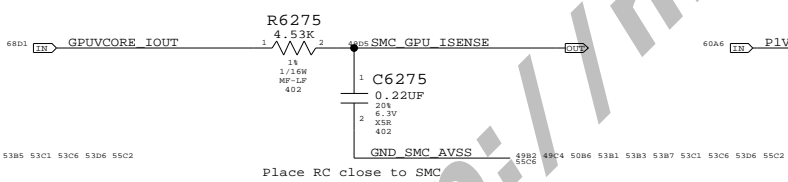
Battery Current Sense Filter



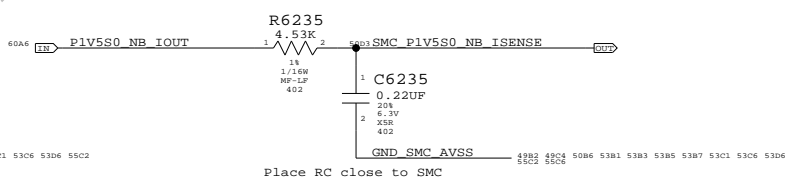
CPU Current Sense Filter



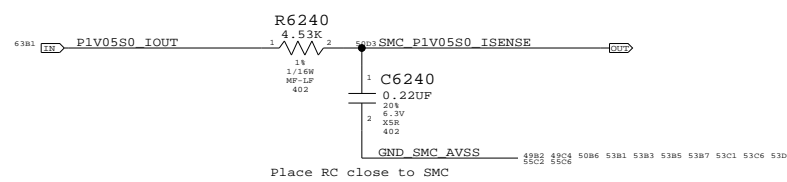
GPU Current Sense Filter



1.5V S0 (NB) Current Sense Filter

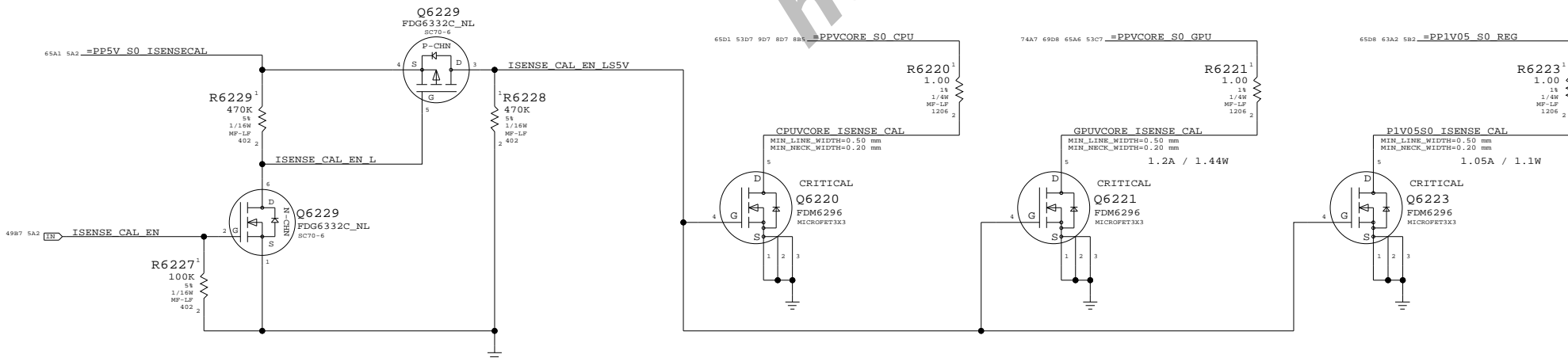


1.05V S0 (NB) Current Sense Filter



Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



Current & Voltage Sensing

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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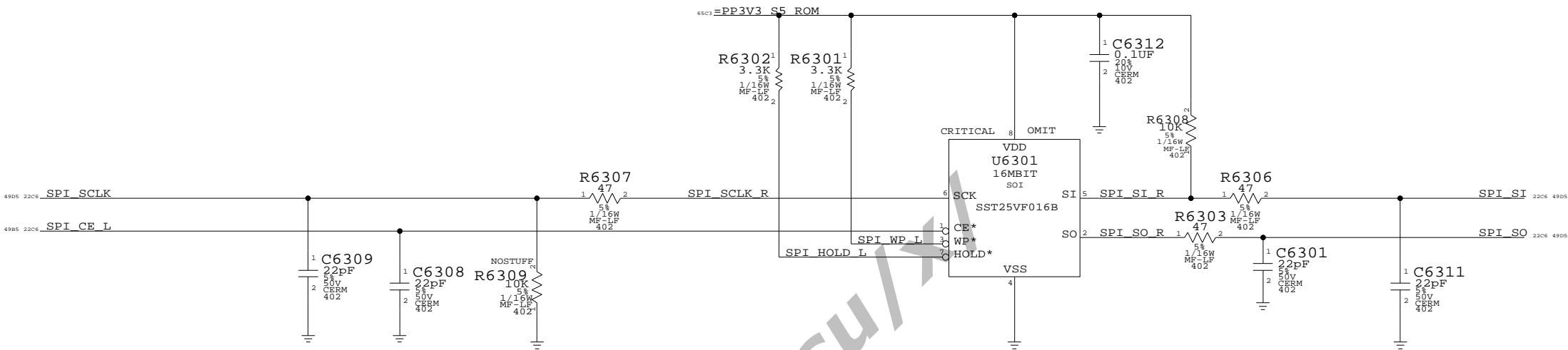
II NOT TO REPRODUCE OR COPY IT

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE	SHT	OF
NONE	53	84



R6309 IS NOT NEEDED WHEN SHARING SPI FLASH WITH ICH7M AND TEKO A (LAN CHIP)

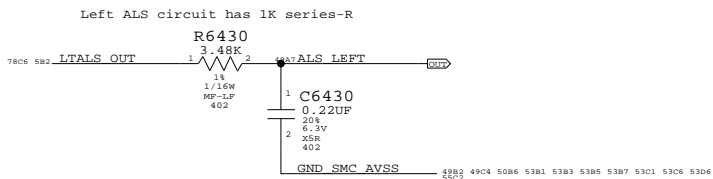
R6307 AND R6306 SHOULD BE PLACED LESS THAN 100 MILS FORM ICH7M

R6303 SHOULD BE PLACED LESS THAN 100 MILS FORM FLASH ROM

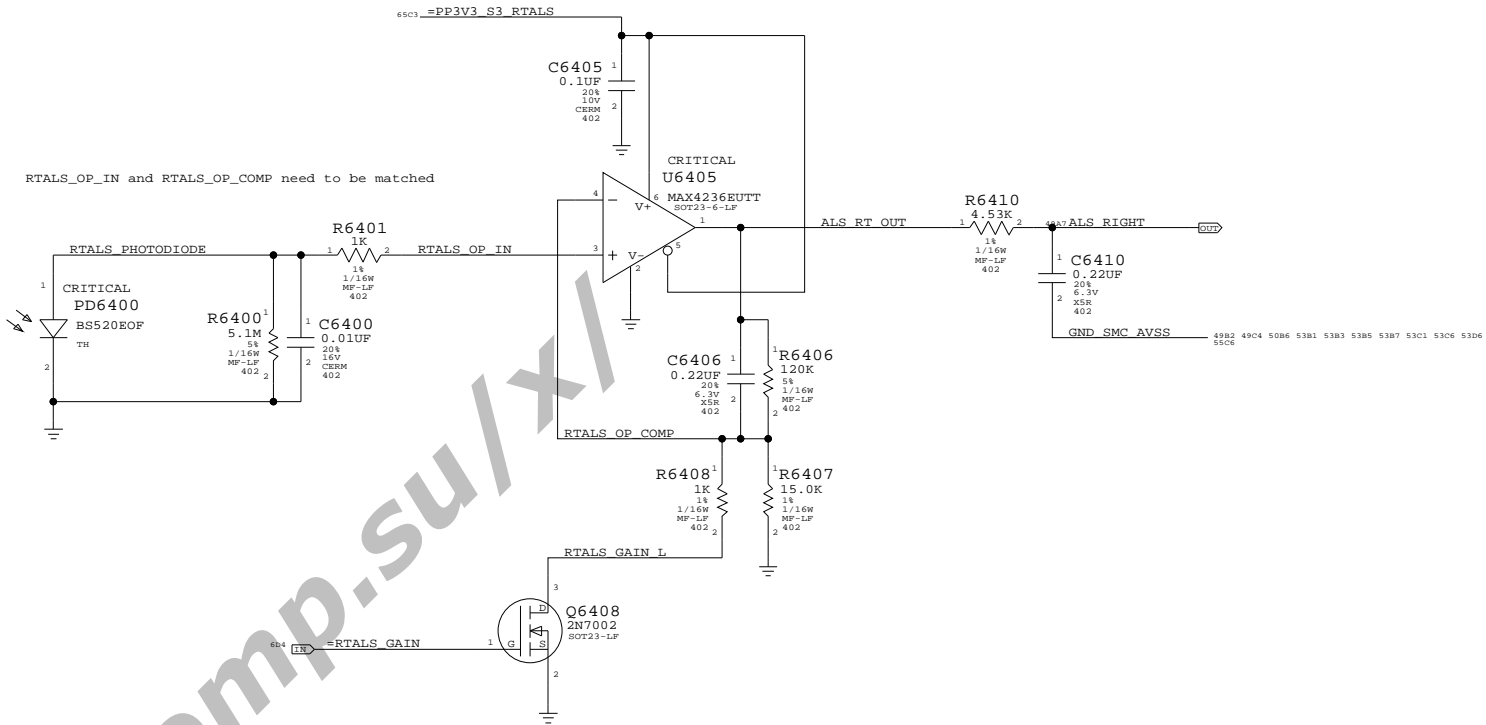
SPI BOOTROM	
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
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SCALE		SHT	OF
NONE		54	84

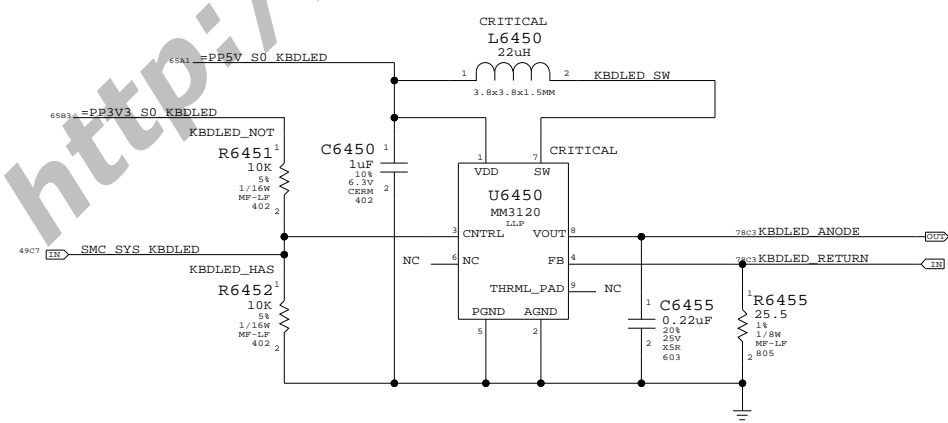
Left ALS Filter



Right ALS Circuit



Keyboard LED Driver



ALS Support

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

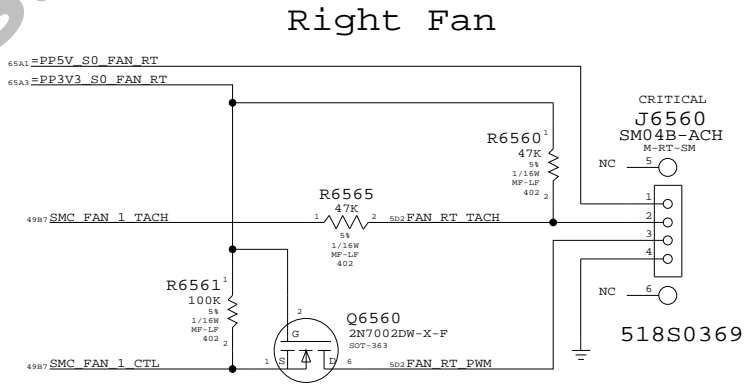
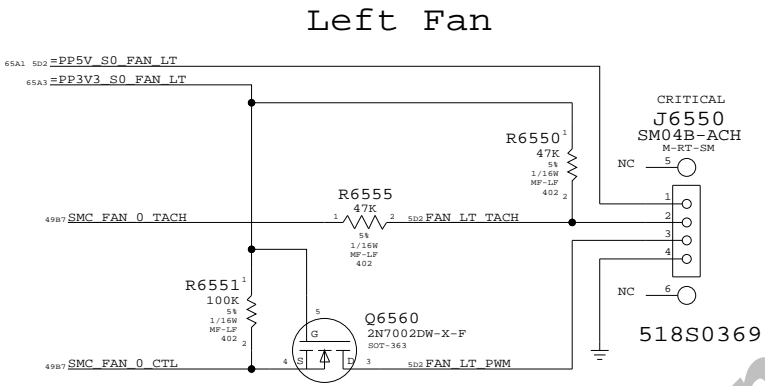
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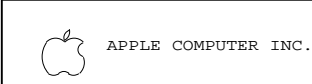
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

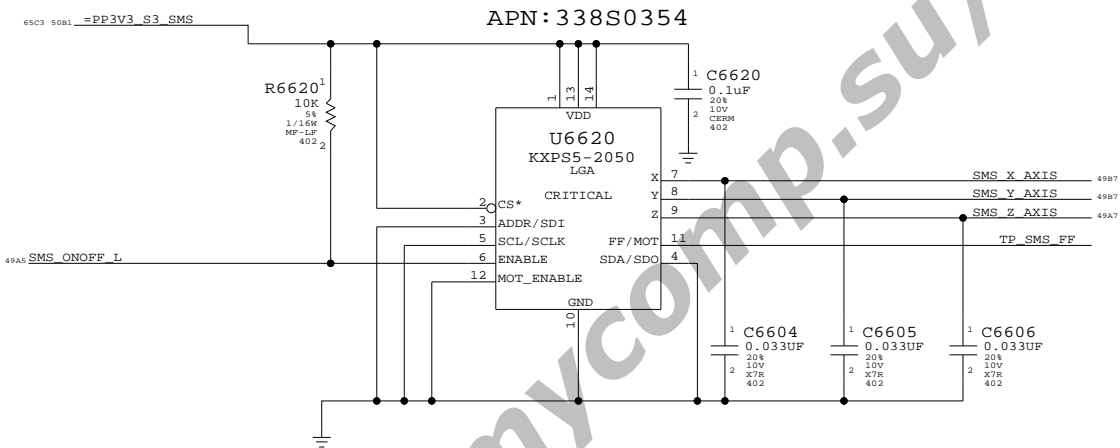
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

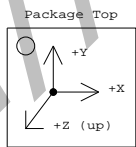


Fan Connectors		
SYNC_MASTER=(MASTER)		SYNC_DATE=(MASTER)
NOTICE OF PROPRIETARY PROPERTY		
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III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART		
SCALE NONE	SIZE D	REV. A.0.0
	DRAWING NUMBER 051-7150	OF 84

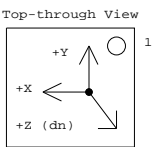




Desired orientation when
placed on board top-side:



Desired orientation when
placed on board bottom-side:



M59 placement: Bottom-side

Sudden Motion Sensor (SMS)

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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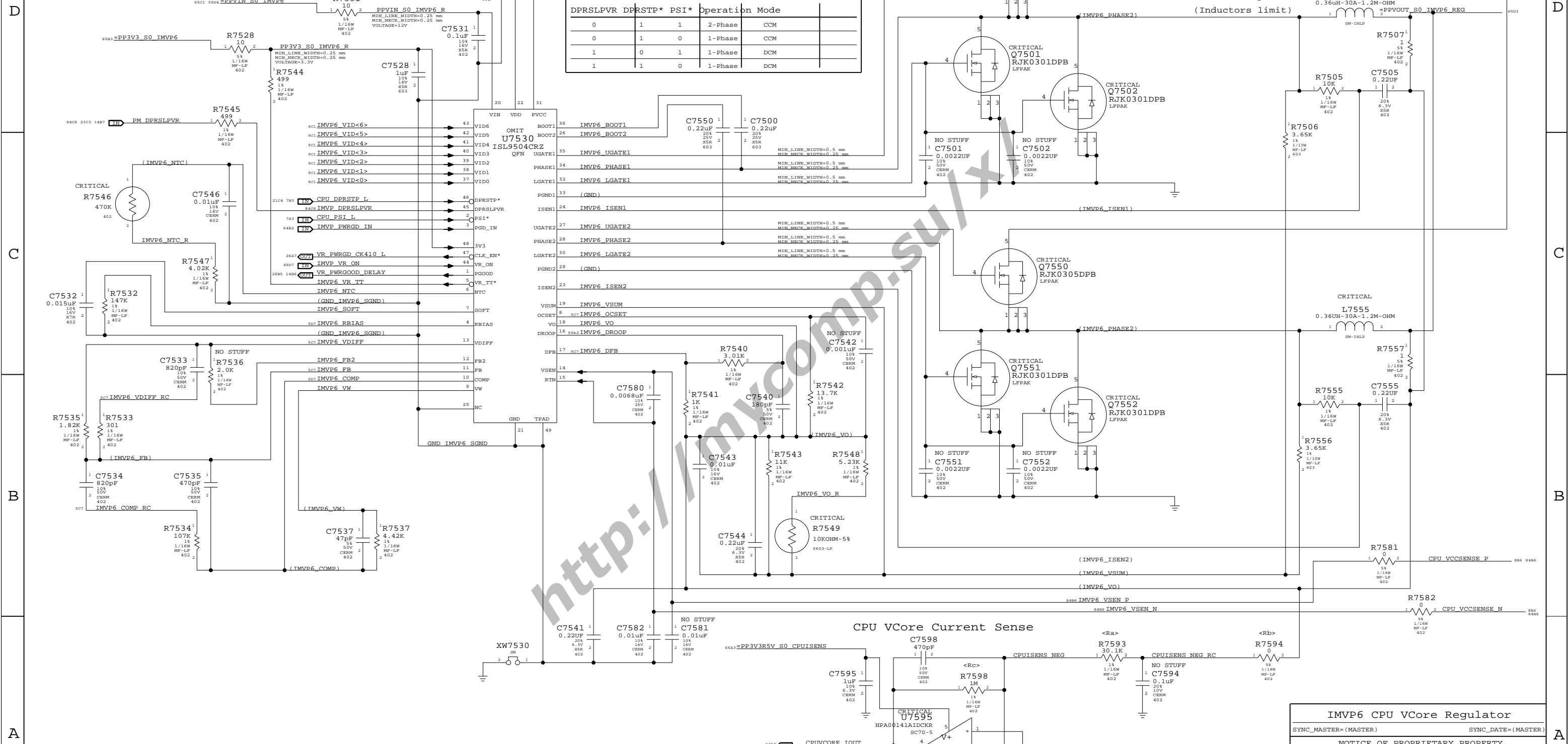


APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE	SHT	OF
NONE	57	84



 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER		REV.
	D	051-7150		A.0.0
	SCALE	SHT	OF	
	NONE	58	84	



```
Vout    = Gain * ((2.1 mV/A * Iload) + Voffset)
Voffset = (Vdrp_offset * Kdroop) + Vamp_offset
Gain    = Rc / (Ra + Rb)
Voffset worst-case -2.3mV (+/- -1A offset)
Vout @ 36A = 2.44V-2.60V
```

```

IMVP6 CPU VCore Regulator
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

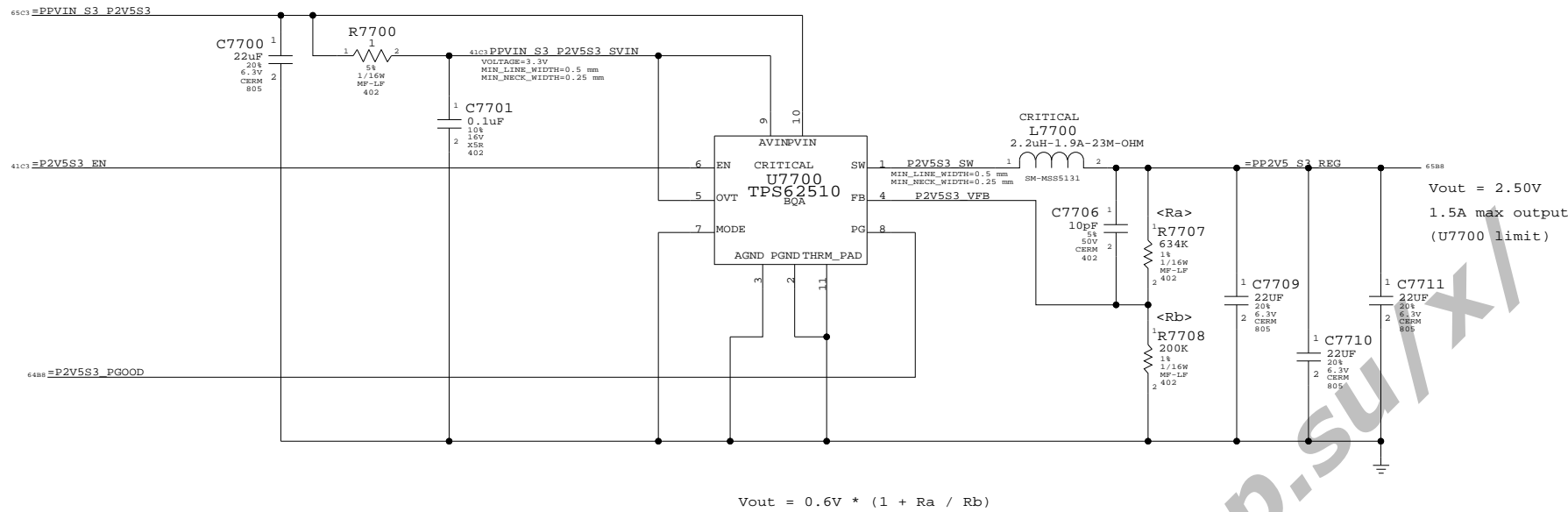
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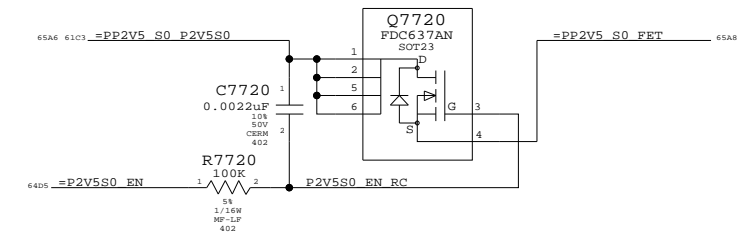
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I I NOT TO REPRODUCE OR COPY IT
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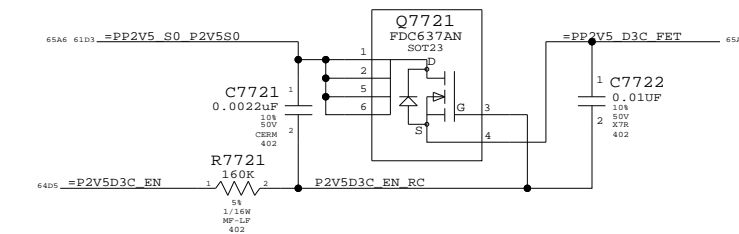

2.5V S3 Regulator



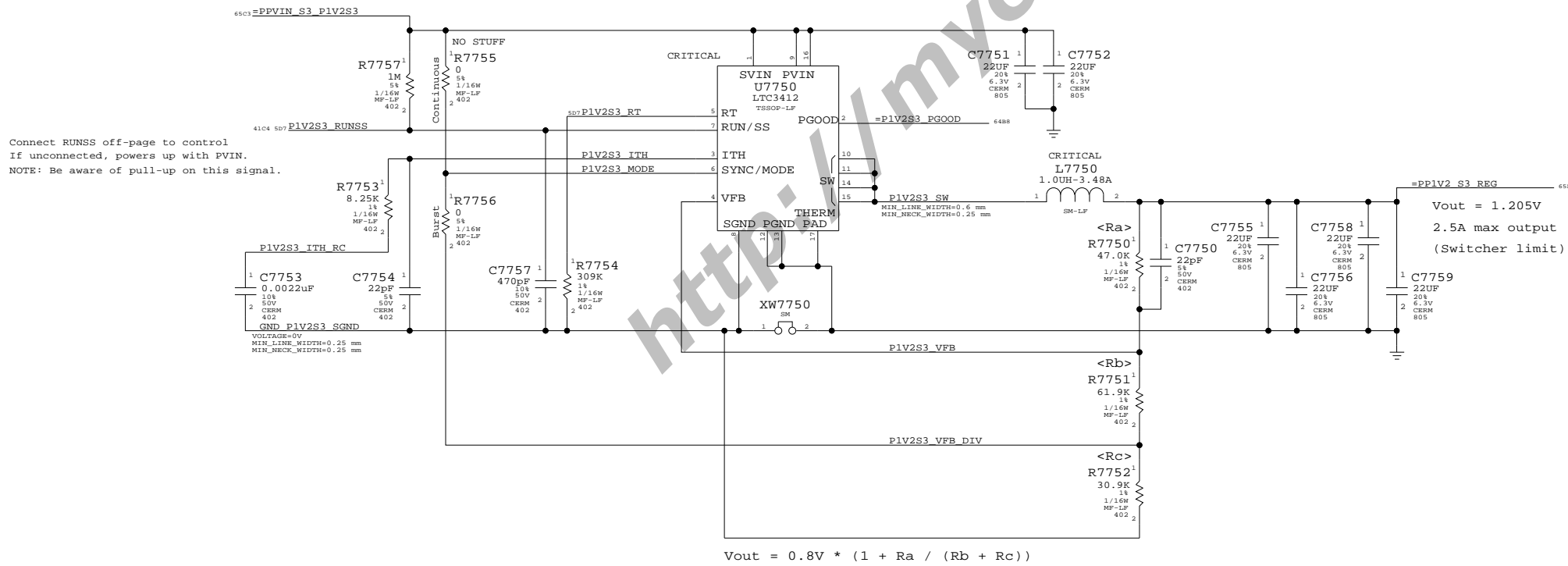
2.5V S0 FET



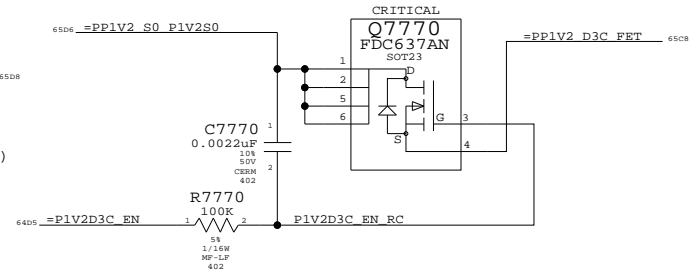
2.5V D3Cold FET



1.2V S3 Regulator



1.2V D3Cold FET



2.5V & 1.2V Regulators

SYNC_MASTER=M59_MG SYNC_DATE=05/07/2006

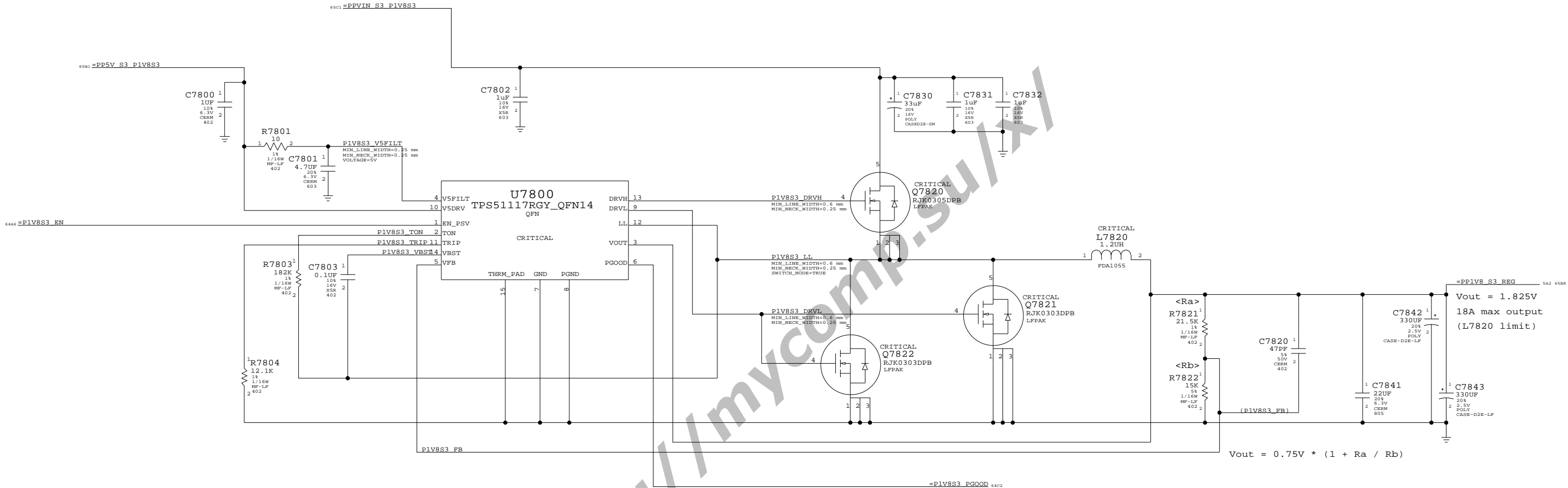
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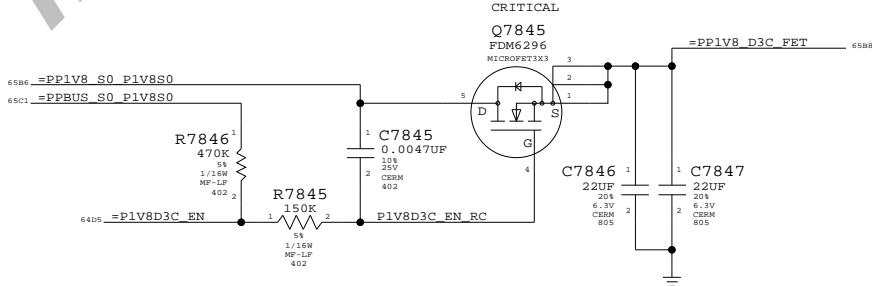
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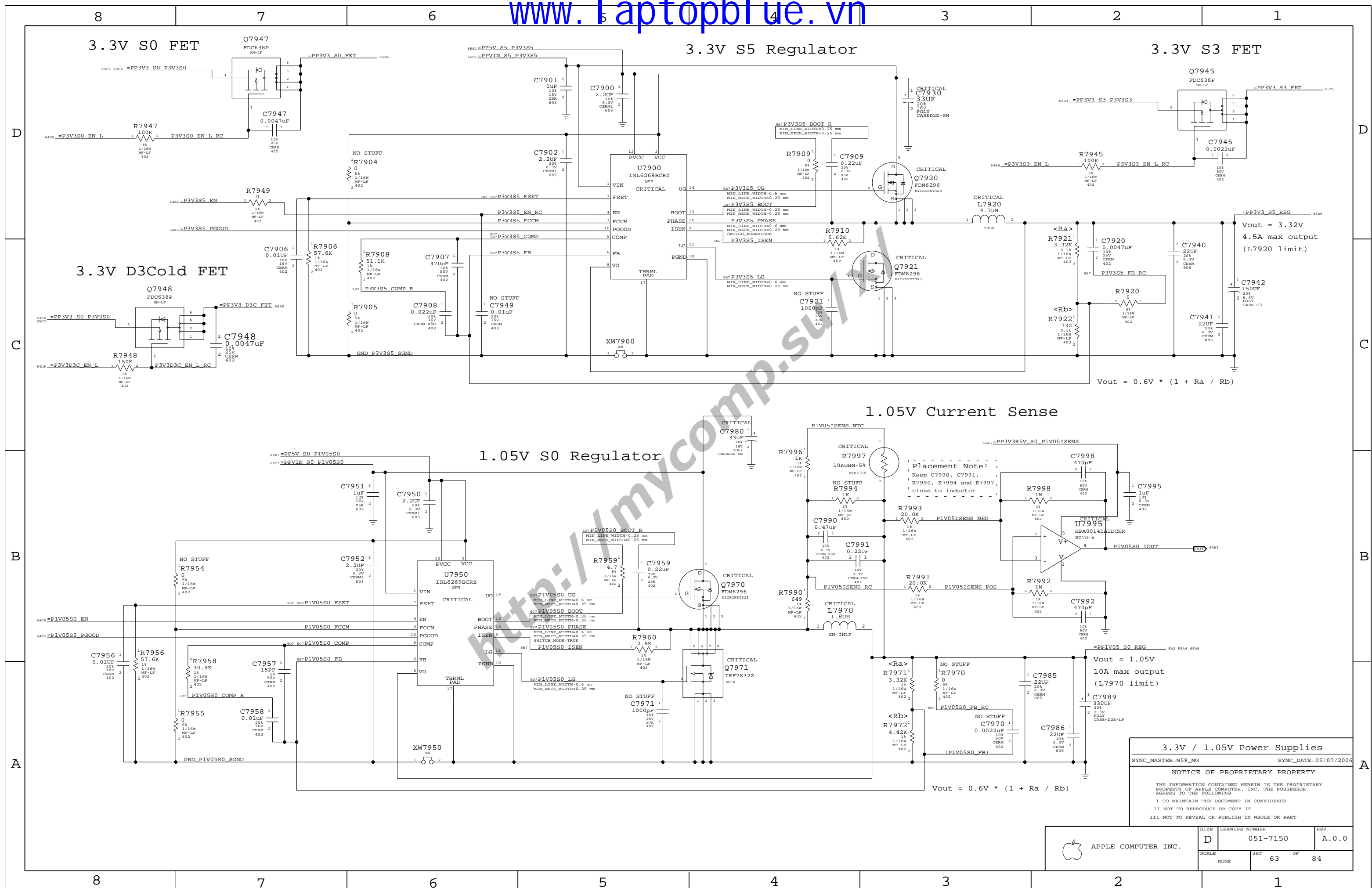


1.8V D3Cold FET

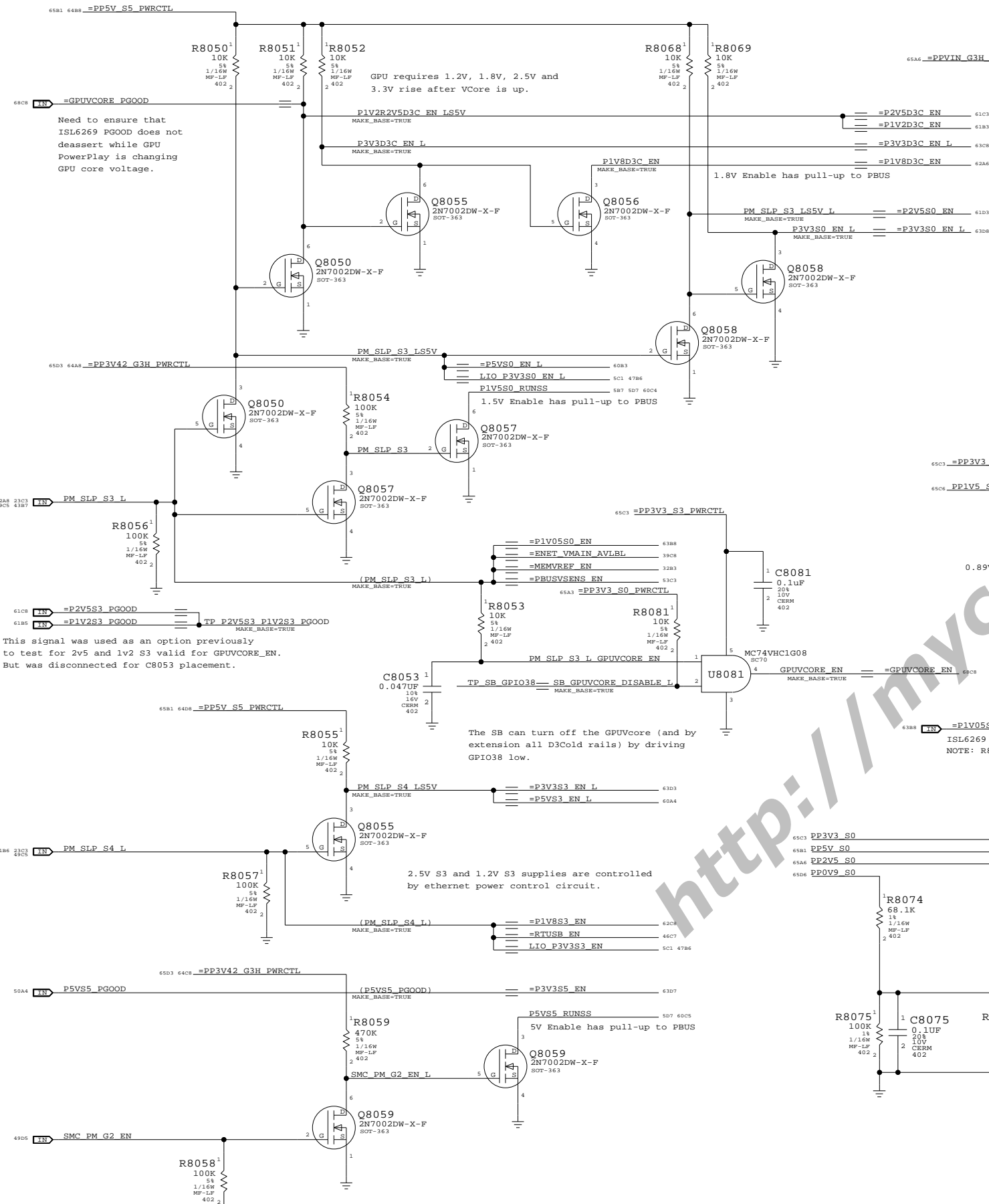


1.8V Supply	
SYNC_MASTER=M59_MG	SYNC_DATE=05/07/2006
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7150	A.0.0
SCALE		SHT	OF
NONE		62	84

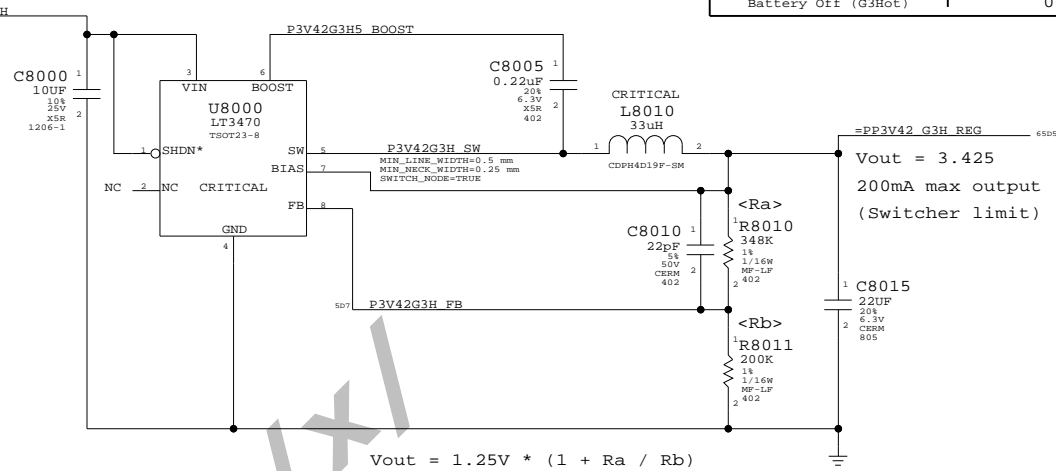


Power Control Signals



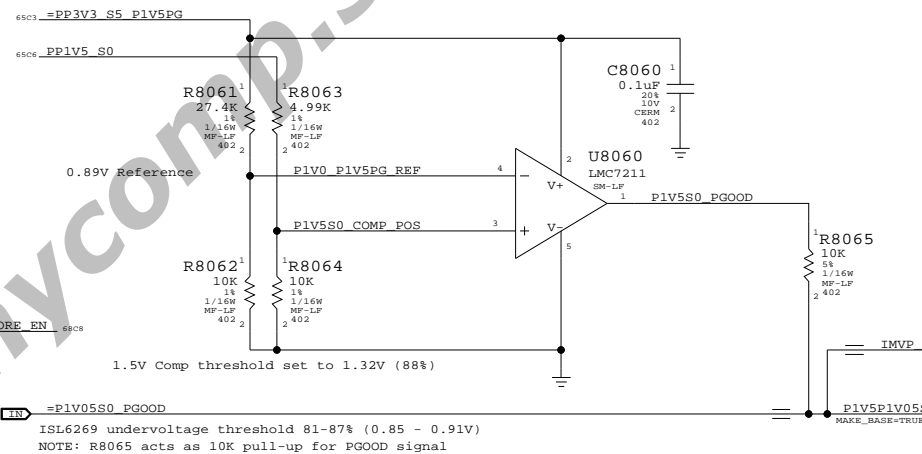
3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation

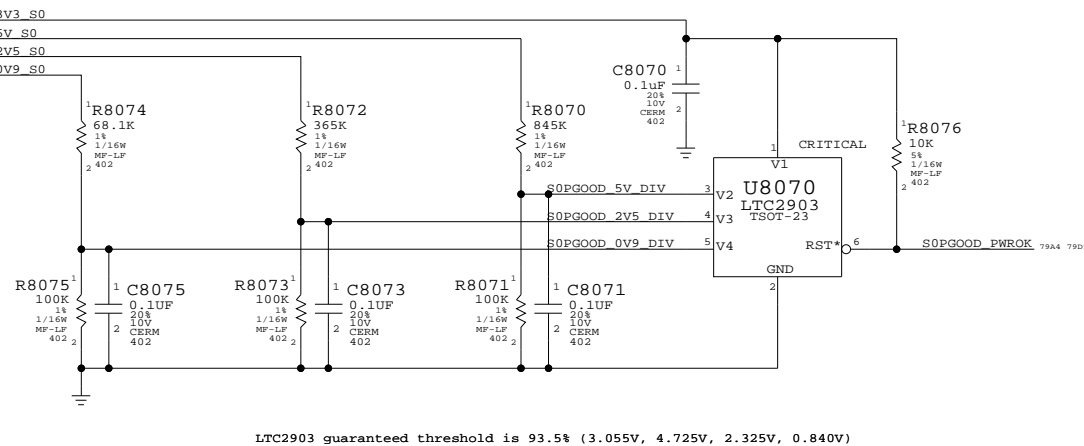


Unused PGOOD Signals

```
60B3  =P5VP1V5 PGOOD      — TP P5V P1V5 PGOOD
                                — MAKE_BASE=TRUE
62B4  =P1V8S3 PGOOD      — TP P1V8S3 PGOOD
                                — MAKE_BASE=TRUE
```

Other S0 Rails PWRGD Circuit

Does not include D3C rails for GPU!!



LTC2903 guaranteed threshold is 93.5% (3.055V, 4.725V, 2.325V, 0.840V)

3.3V G3Hot Supply & Power Control

SYNC_MASTER=M59_MG	SYNC_DATE=08/01/2006
--------------------	----------------------

NOTICE OF PROPRIETARY PROPERTY

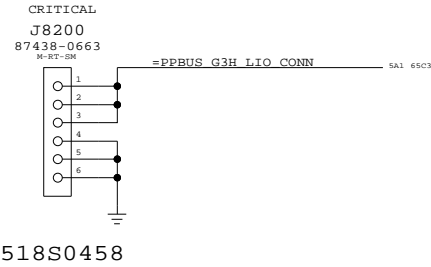
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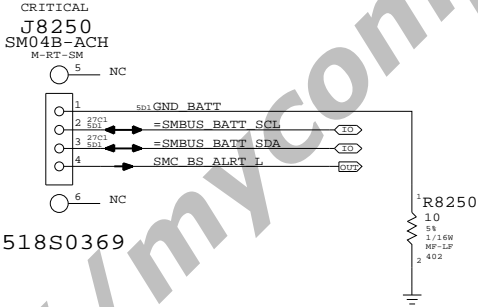
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Left I/O Power Connector

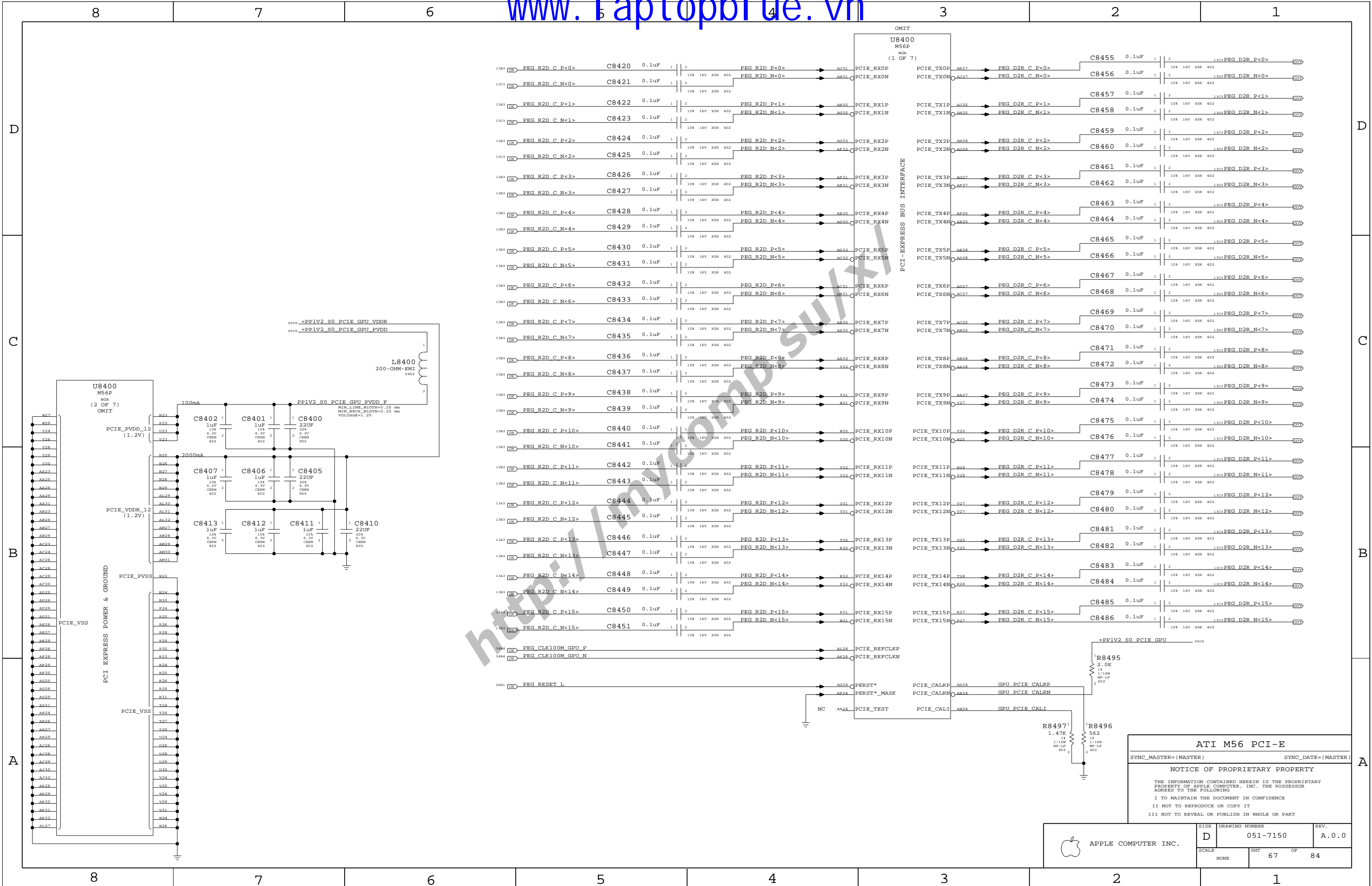


Battery Connector (Digital Signals)



PBus-In, Batt. & 3G Pwr Connectors		
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)		
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7150	REV. A.0.0
	SCALE NONE	SHT 66	OF 84



ATI M56 PCI-E

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

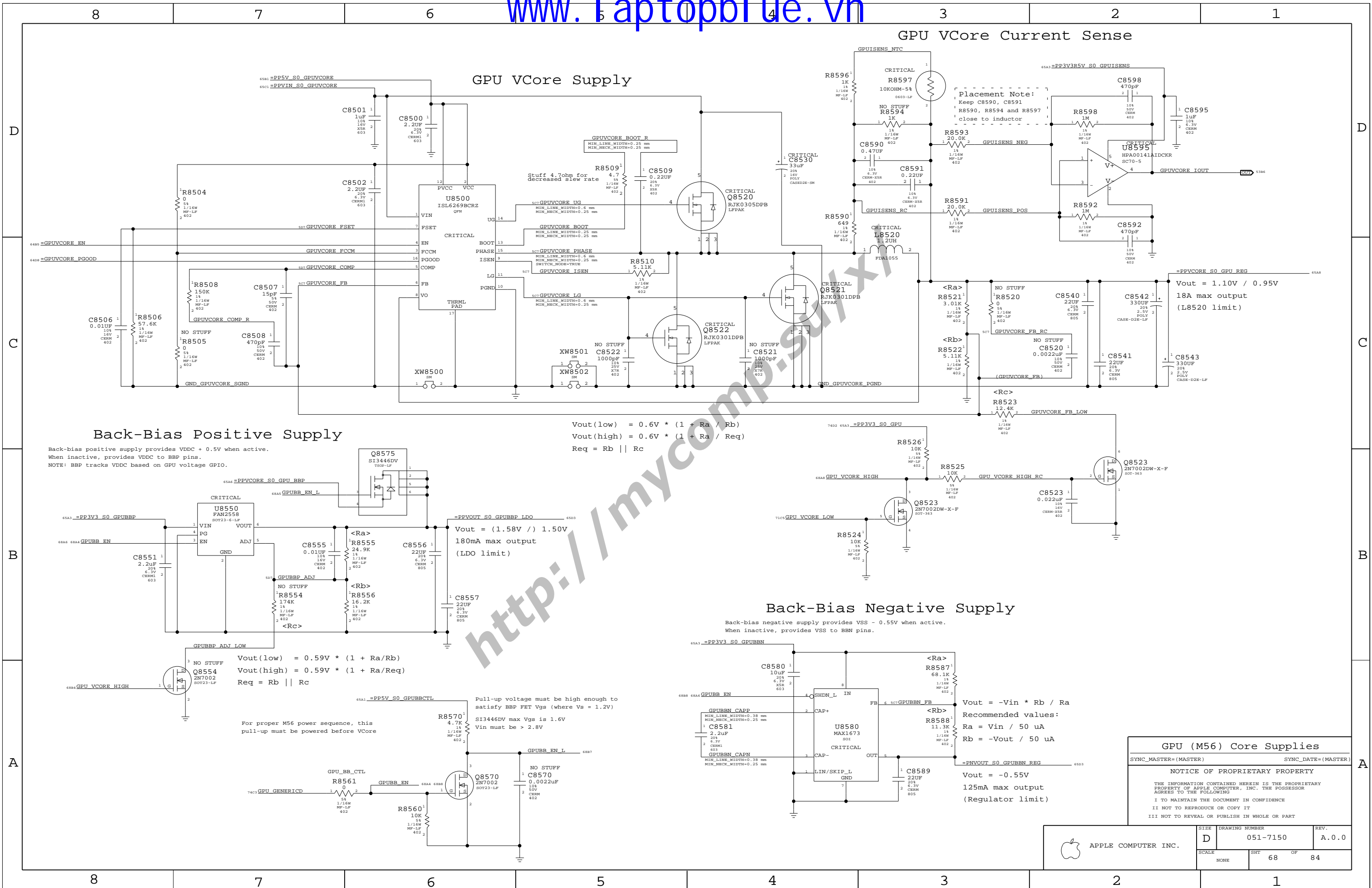
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7150	A.0.0
SCALE	SHT		
	67 OF 84		



D

BOM options provided by this page:
(NONE)



B

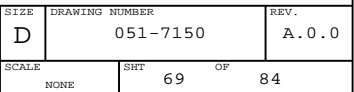
A

D

C

B

A



D

D

C

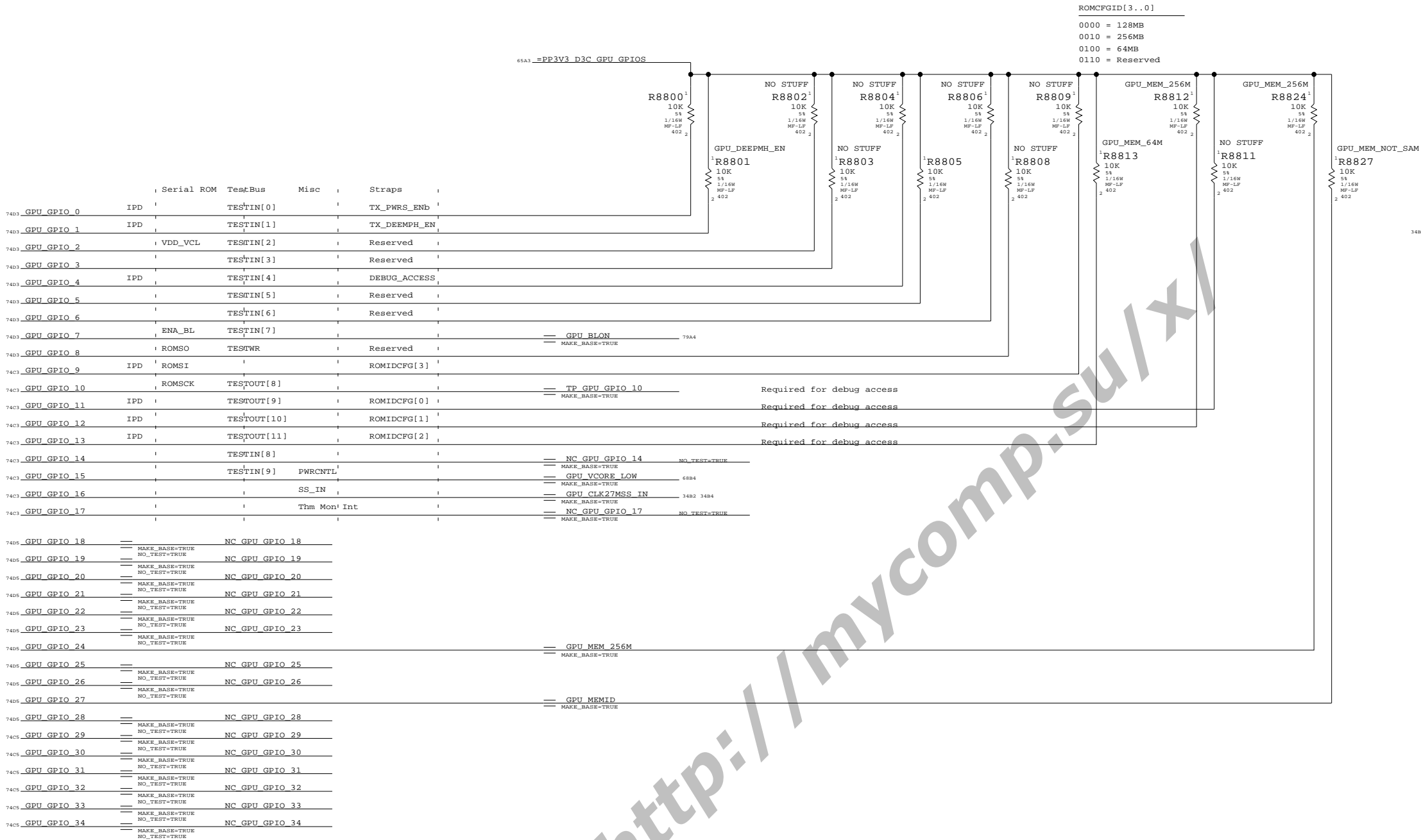
C

B

B

A

A



Renamed signals

34B4 34B2 GPU_CLK27M MAKE_BASE=TRUE GPU_XTALIN 74A5

Unused signals

NC_GPU_XTALOUT MAKE_BASE=TRUE NO_TEST=TRUE GPU_XTALOUT 74A5

NC_ATI_ROMCS_L MAKE_BASE=TRUE NO_TEST=TRUE TP_ATI_ROMCS_L 74A3

NC_FB_A_MAI2 MAKE_BASE=TRUE NO_TEST=TRUE TP_FB_A_MAI2 70D5

NC_FB_B_MAI2 MAKE_BASE=TRUE NO_TEST=TRUE TP_FB_B_MAI2 70D1

NC_GPU_GENERICA MAKE_BASE=TRUE NO_TEST=TRUE GPU_GENERICA 74C3

NC_GPU_GENERICB MAKE_BASE=TRUE NO_TEST=TRUE GPU_GENERICB 74C3

NC_GPU_GENERICC MAKE_BASE=TRUE NO_TEST=TRUE GPU_GENERICC 74C3

NC_GPU_VGA_R MAKE_BASE=TRUE NO_TEST=TRUE GPU_VGA_R 75C3

NC_GPU_VGA_G MAKE_BASE=TRUE NO_TEST=TRUE GPU_VGA_G 75C3

NC_GPU_VGA_B MAKE_BASE=TRUE NO_TEST=TRUE GPU_VGA_B 75C3

TP_GPU_VGA_HSYNC MAKE_BASE=TRUE NO_TEST=TRUE GPU_VGA_HSYNC 75B3

TP_GPU_VGA_VSYNC MAKE_BASE=TRUE NO_TEST=TRUE GPU_VGA_VSYNC 75B3

NC_GPU_TV_Y MAKE_BASE=TRUE NO_TEST=TRUE GPU_TV_Y 75B3

NC_GPU_TV_C MAKE_BASE=TRUE NO_TEST=TRUE GPU_TV_C 75B3

NC_GPU_TV_COMP MAKE_BASE=TRUE NO_TEST=TRUE GPU_TV_COMP 75B3

NC_LVDS_U_DATAP<3> MAKE_BASE=TRUE NO_TEST=TRUE LVDS_U_DATA_P<3> 75B3

NC_LVDS_U_DATAN<3> MAKE_BASE=TRUE NO_TEST=TRUE LVDS_U_DATA_N<3> 75B3

NC_LVDS_L_DATAP<3> MAKE_BASE=TRUE NO_TEST=TRUE LVDS_L_DATA_P<3> 75A3

NC_LVDS_L_DATAN<3> MAKE_BASE=TRUE NO_TEST=TRUE LVDS_L_DATA_N<3> 75A3

NC_ATI_DVPCCLK MAKE_BASE=TRUE NO_TEST=TRUE ATI_DVPCCLK 74C3

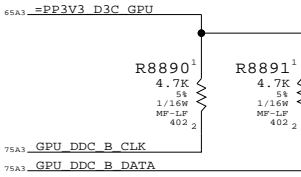
NC_ATI_DVPCNTL<2..0> MAKE_BASE=TRUE NO_TEST=TRUE ATI_DVPCNTL<2..0> 74B3 74C3

NC_ATI_DVPPDATA<15..0> MAKE_BASE=TRUE NO_TEST=TRUE ATI_DVPPDATA<15..0> 74B3

Required for debug access

TP_ATI_DVPPDATA<23..16> MAKE_BASE=TRUE ATI_DVPPDATA<23..16> 74B3 74C3

Also required: GPIO10 - GPIO13



GPU Straps

SYNC_MASTER=M59_MG SYNC_DATE=07/25/2006

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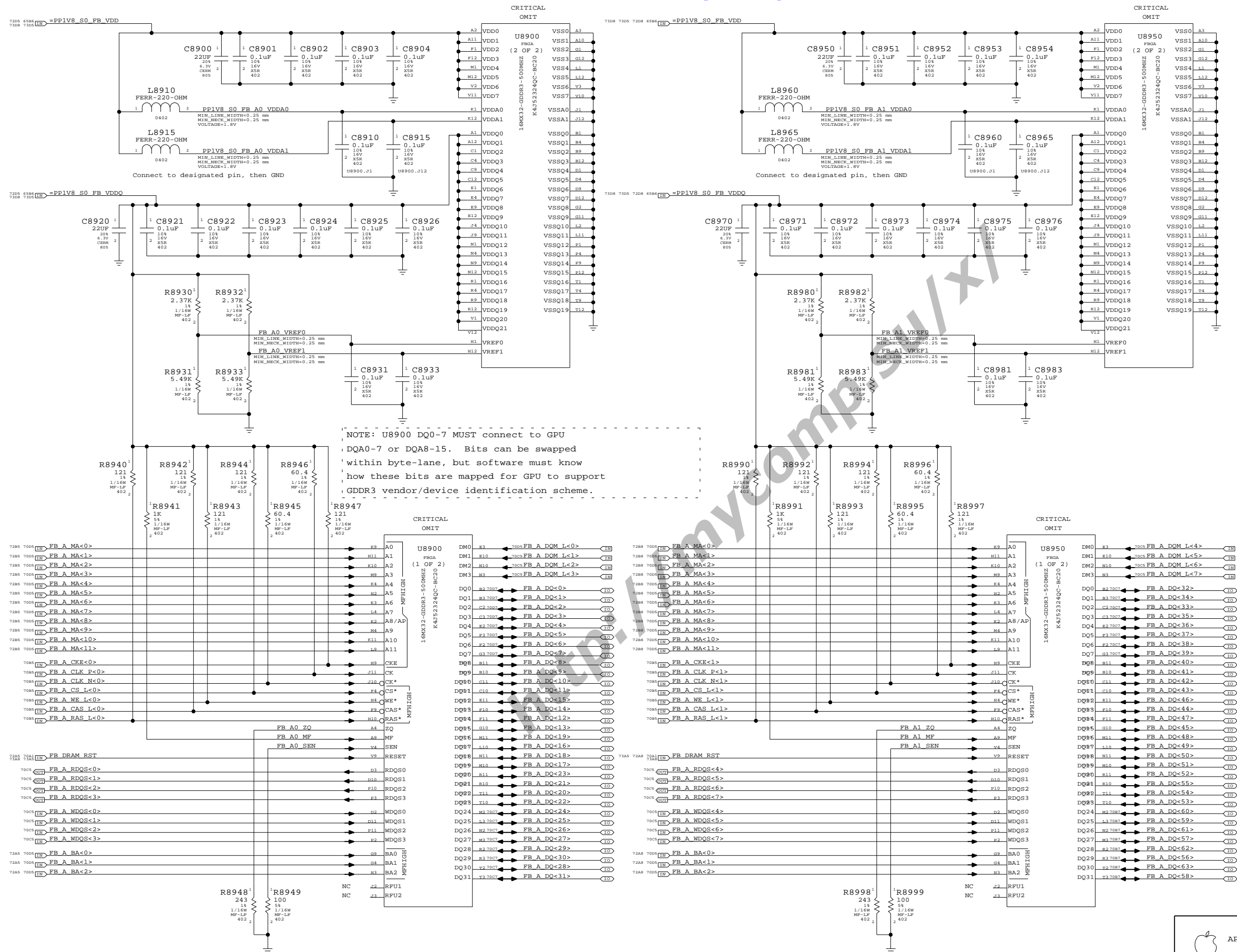
SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE	SHT	OF
NONE	71	84

Power aliases required by this page:

```
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ
```

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



GDDR3 Frame Buffer A

SYNC_MASTER= (MASTER)	SYNC_DATE= (MASTER)
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SIZE	DRAWING NUMBER	REV.
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D	051-7150
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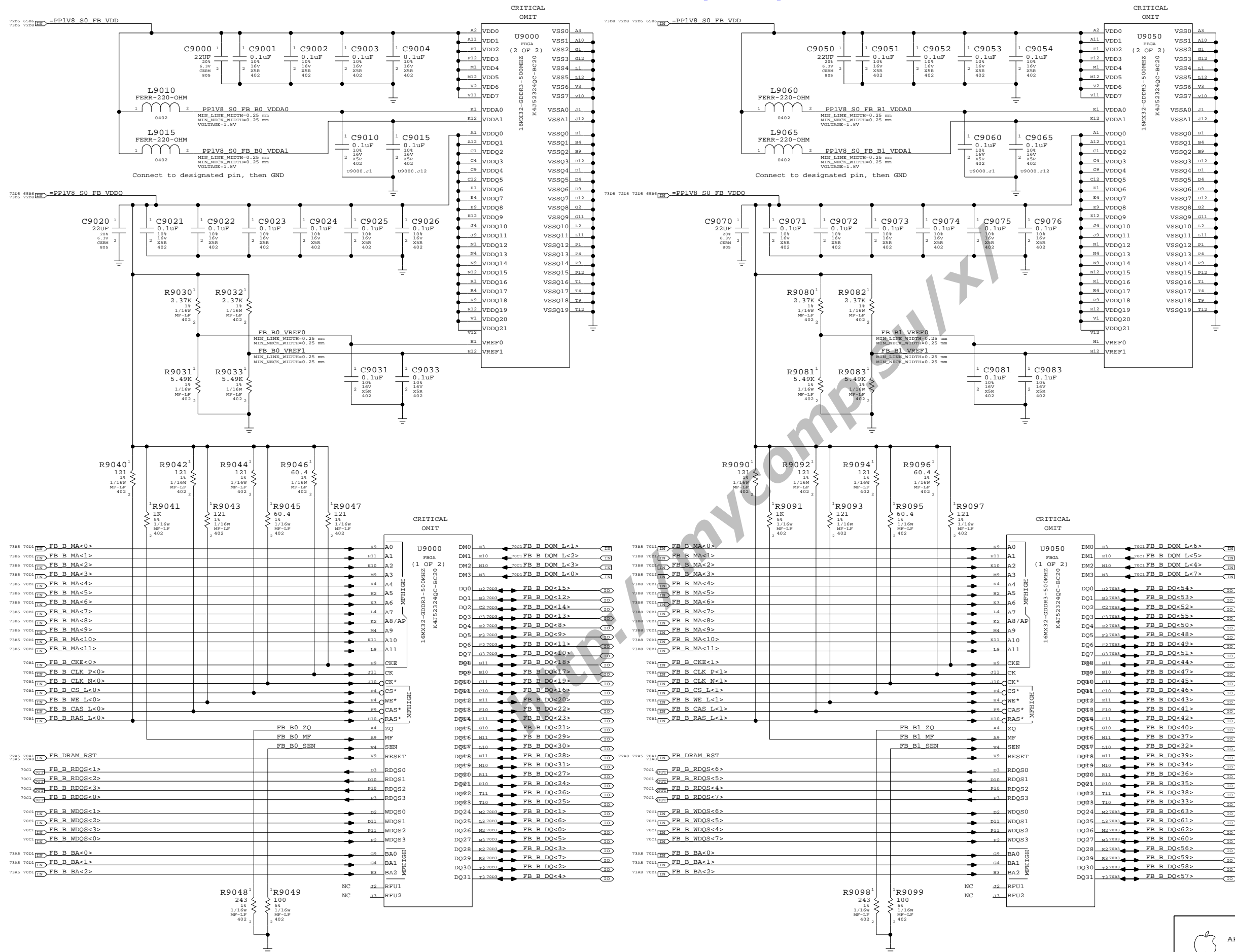
SCALE	SHT 72 OF
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NONE	12
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Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



GDDR3 Frame Buffer B

SYNC_MASTER=(MASTER)

SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.

SIZE

D

DRAWING NUMBER

051-7150

REV.

A.0.0

SCALE

NONE

SHT

73

OF

84

Page Notes

Power aliases required by this page:

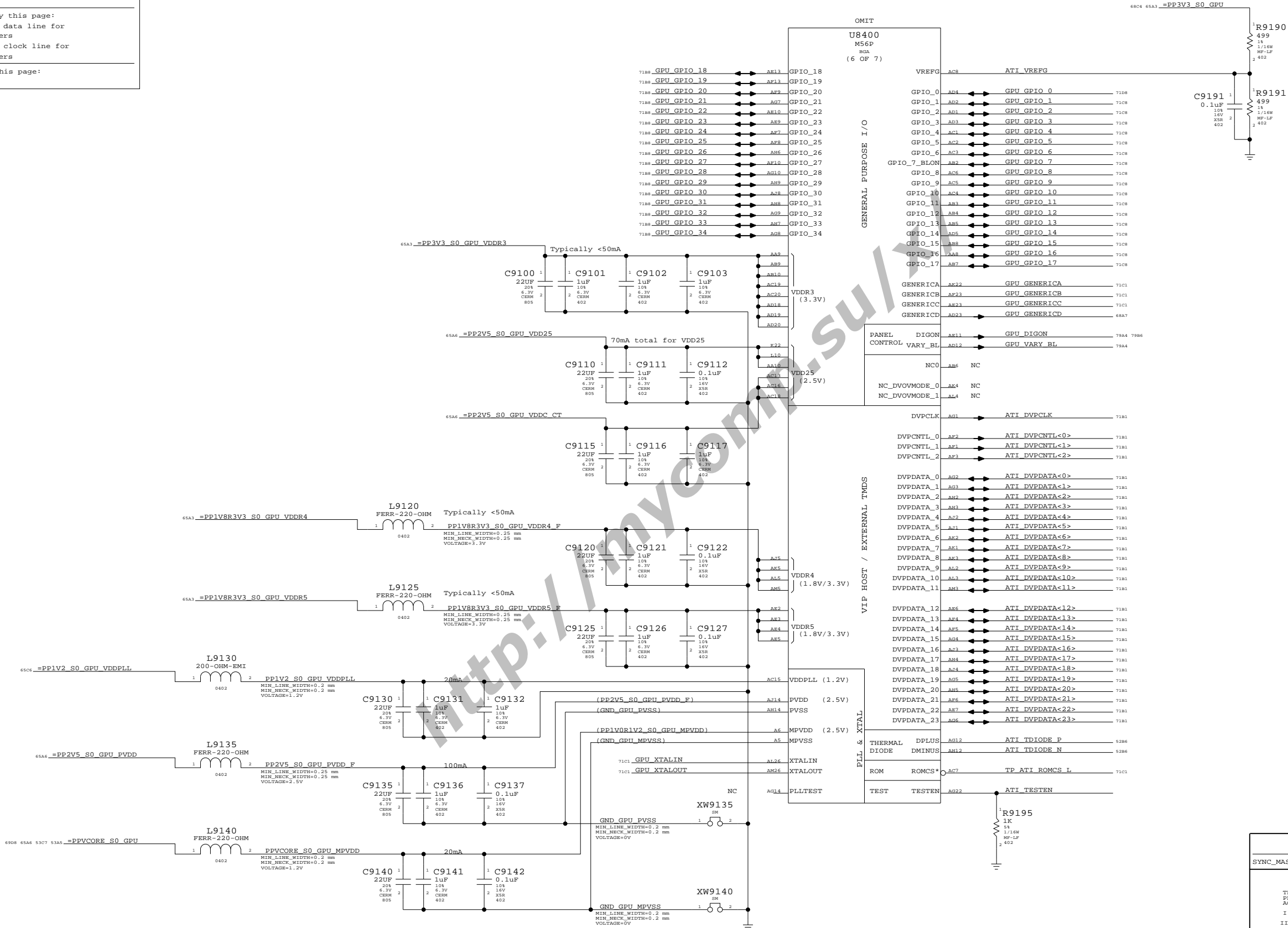
- =PP3V3_GPU_GPIOS
- =PP2V5_PVDD
- =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:

- =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
- =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:

(NONE)



ATI M56 GPIO/DVO/Misc

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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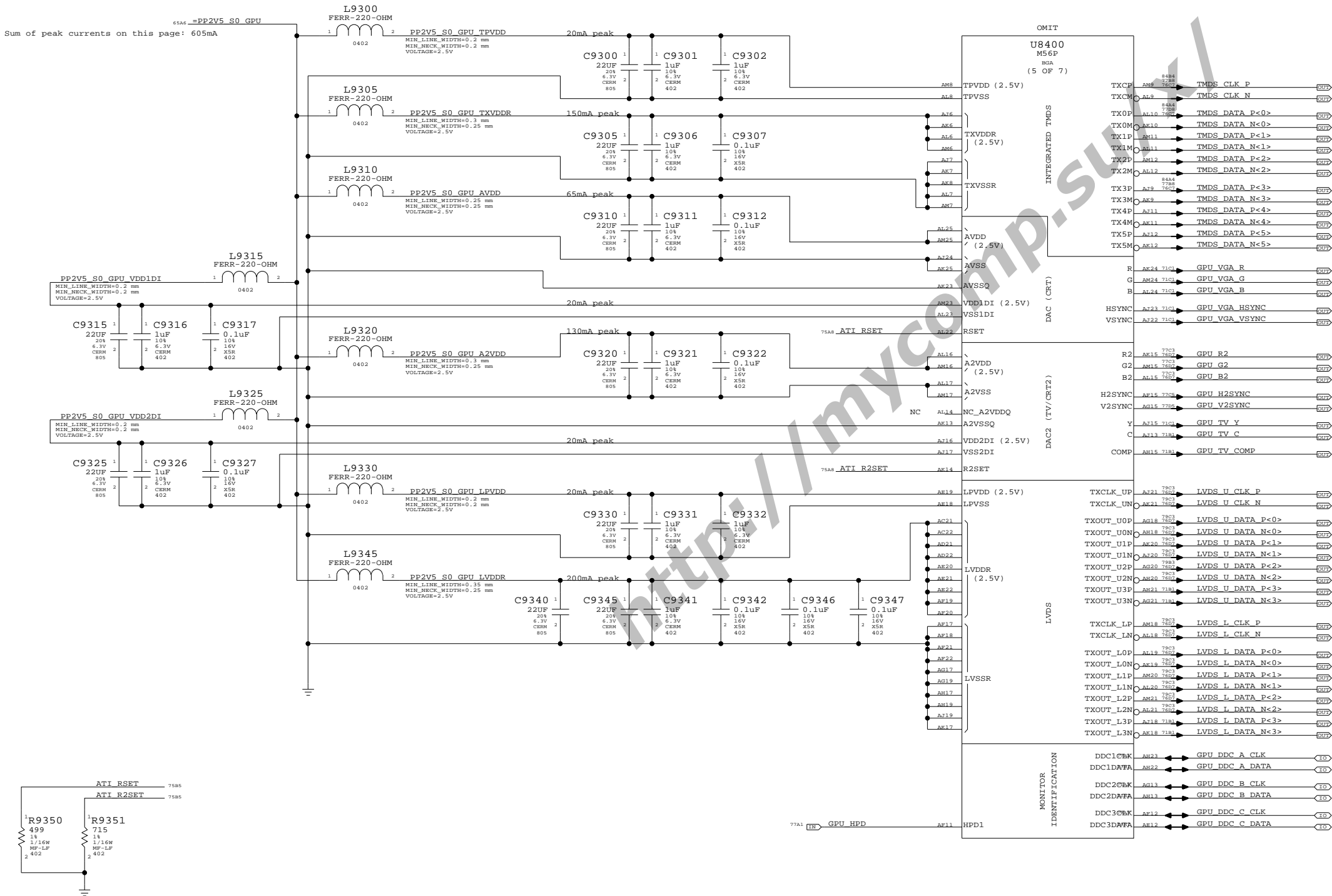
SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE	SHT	OF
NONE	74	84

Page Notes

Power aliases required by this page:
- =PP2V5_S0_GPU
- =PP1V8R2V5_S0_GPU_LVDDR

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



Composite/S-Video	VGA	Component
Y	G	Y
C	R	Pr
Comp	B	Pb

ATI M56 Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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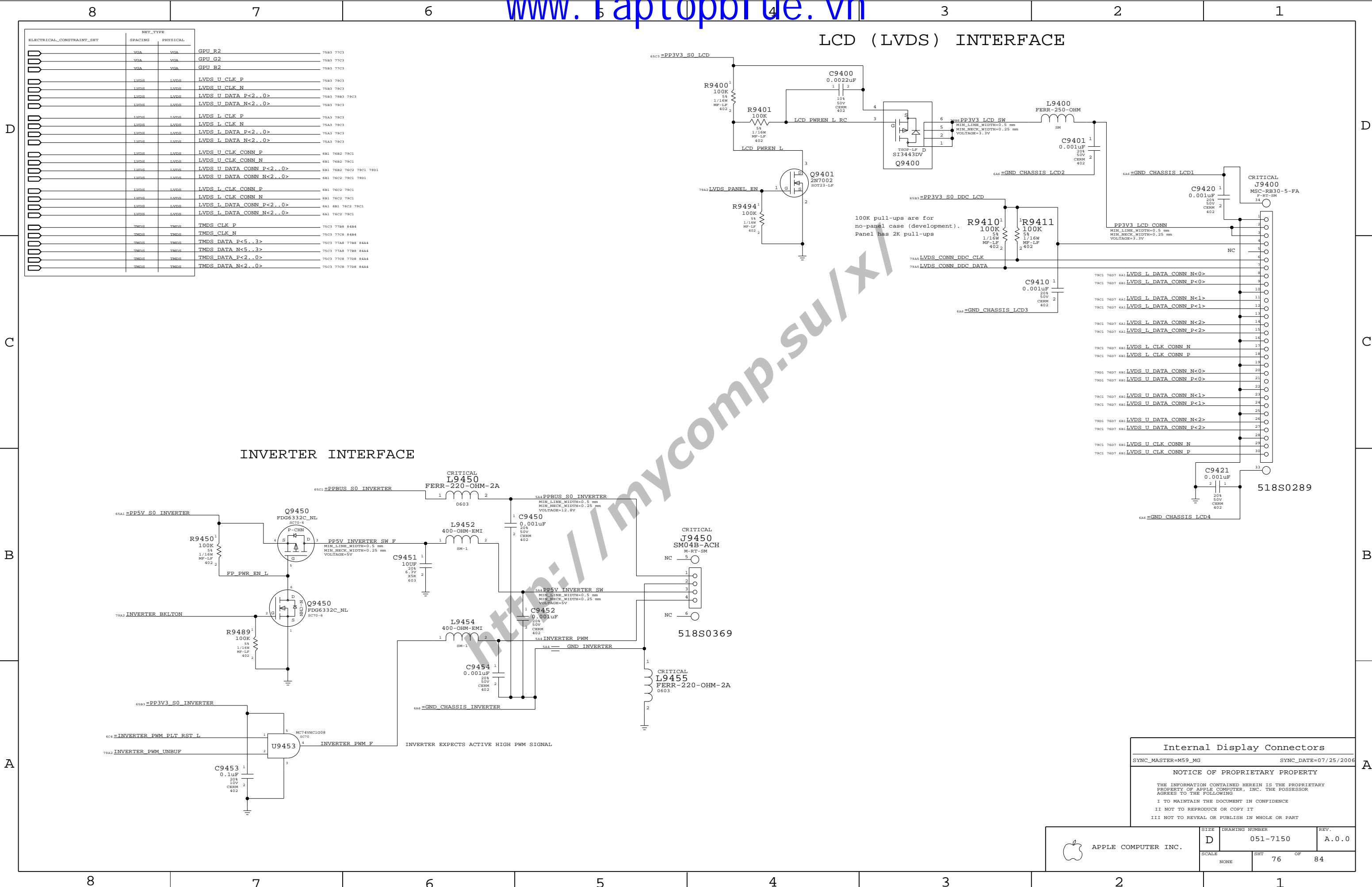
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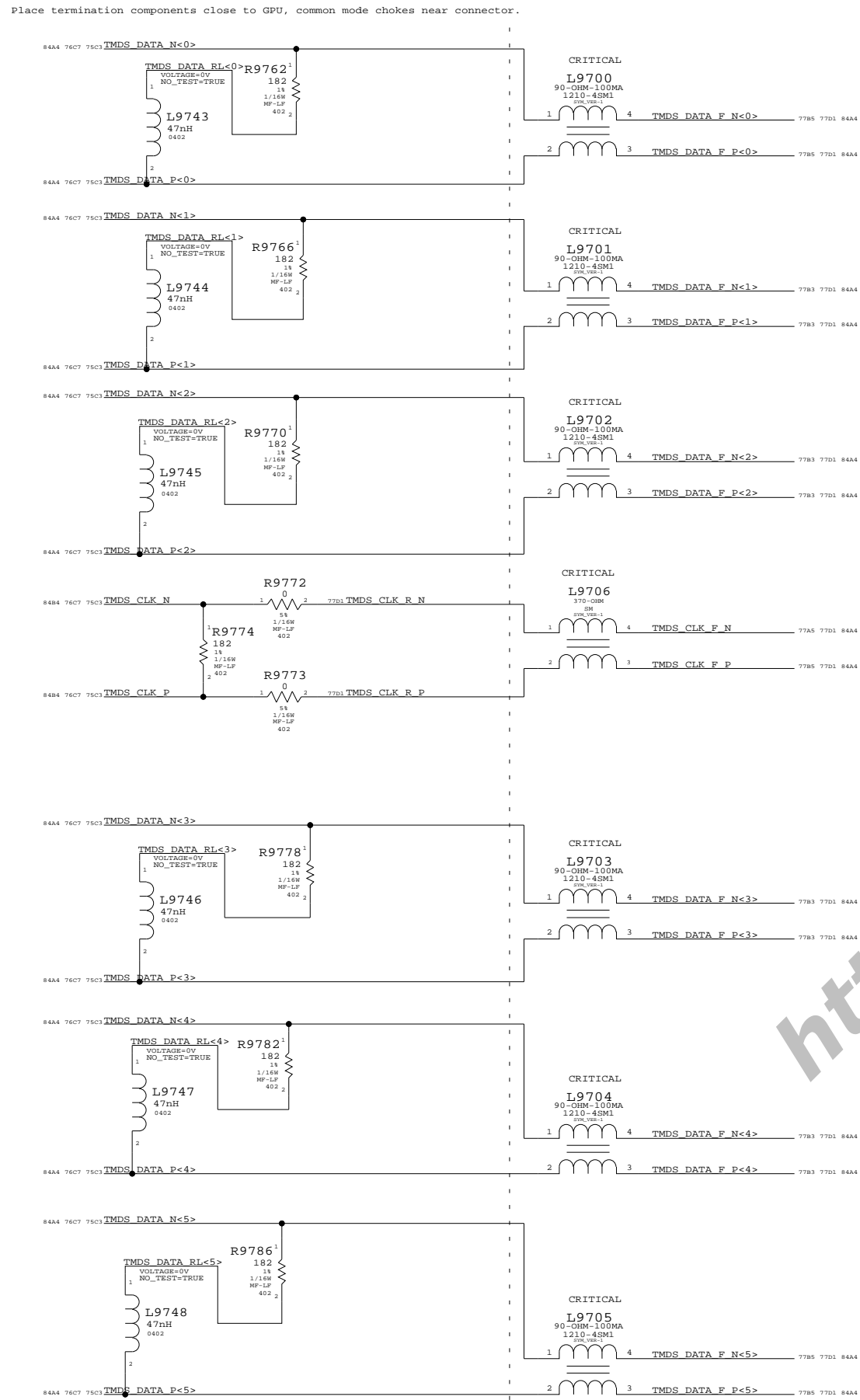
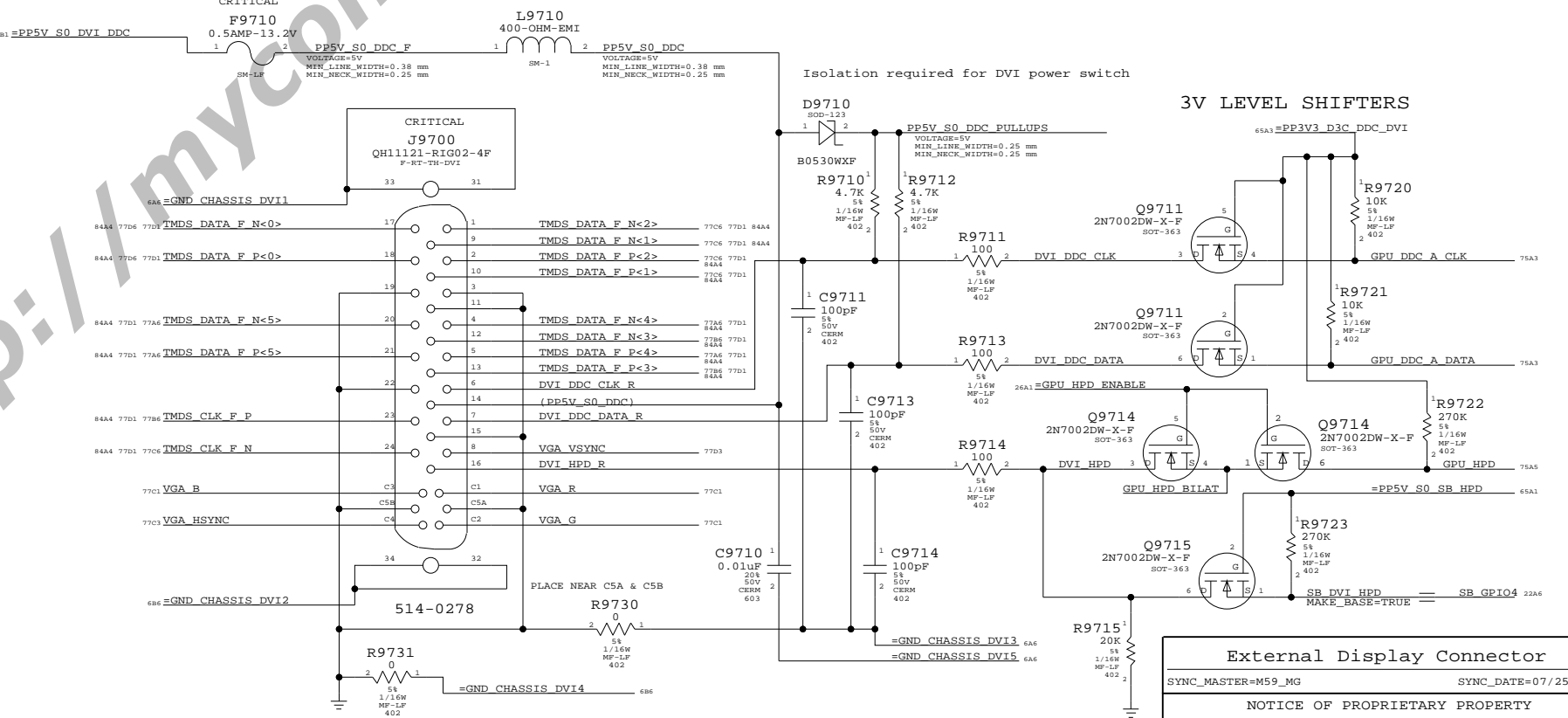
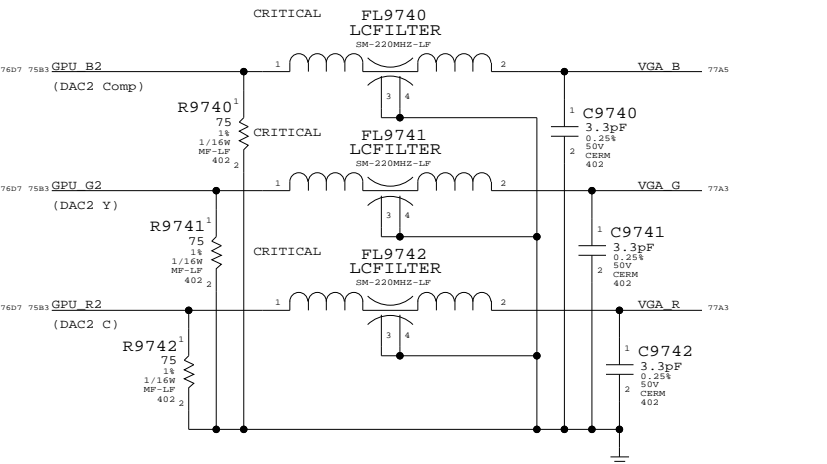
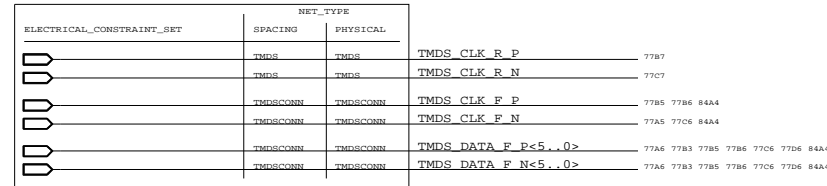
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SCALE	SHT	OF
NONE	75	84



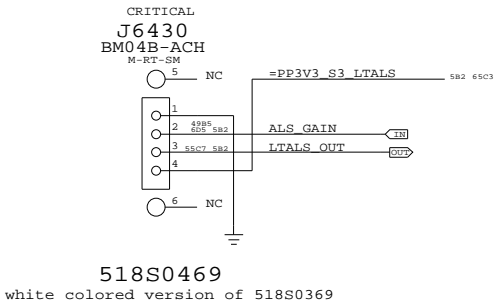
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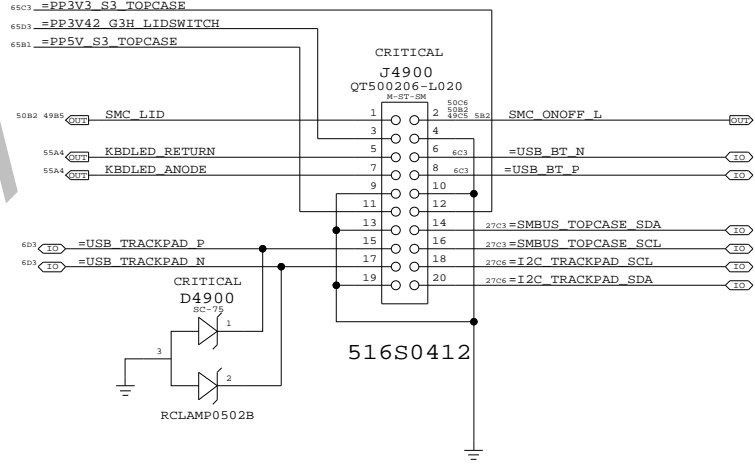
SCALE	SHT	OF
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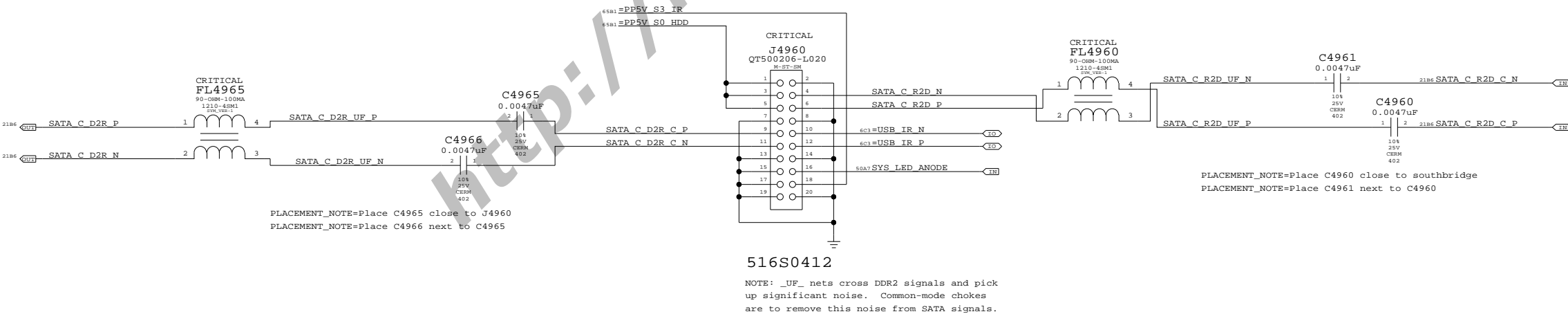
Left ALS Connector



Top-Case Connector



SATA HDD & IR & SIL Flex Connector



M59 Specific Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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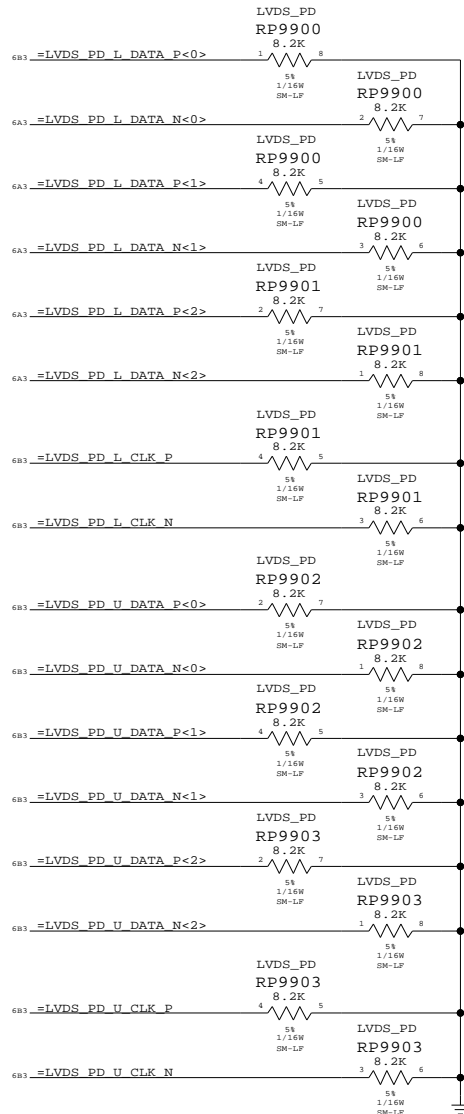


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SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE	SHT	OF
NONE	78	84

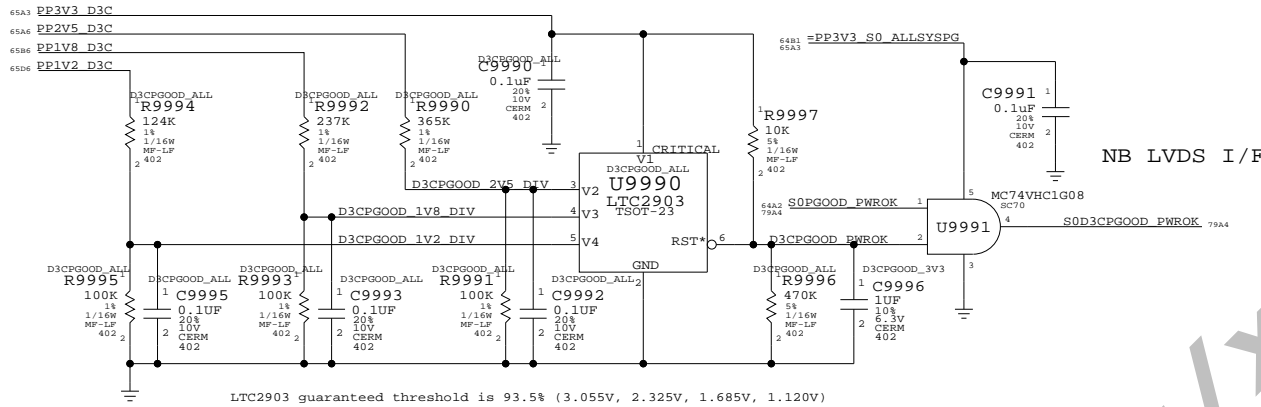
LVDS Interface Pull-downs

NOTE: These parts are to counter an invalid state caused by the M56 part. Bias voltage is present on LVDS interface pins even when they should be tri-stated to meet panel power sequence requirements. Resulting pump-up in LCD panel can cause startup and long-term reliability issues. Pull-down resistors reduce the pump-up in the panel, though some voltage will still be seen on LVDS signals when they should be 0V.



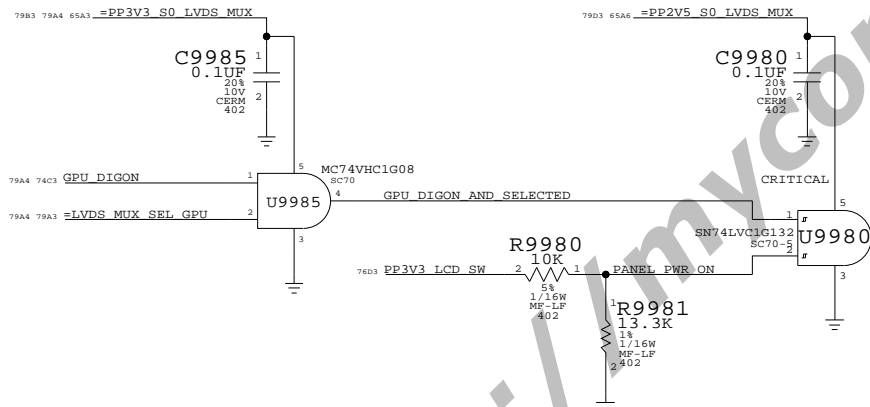
PGOOD Monitor for GPU Rails

D3CPGOOD_ALL BOM option stuffs LTC2903 circuit to monitor all D3C rails to qualify D3CPGOOD. D3CPGOOD_3V3 BOM option uses only PP3V3_D3C to qualify D3CPGOOD.

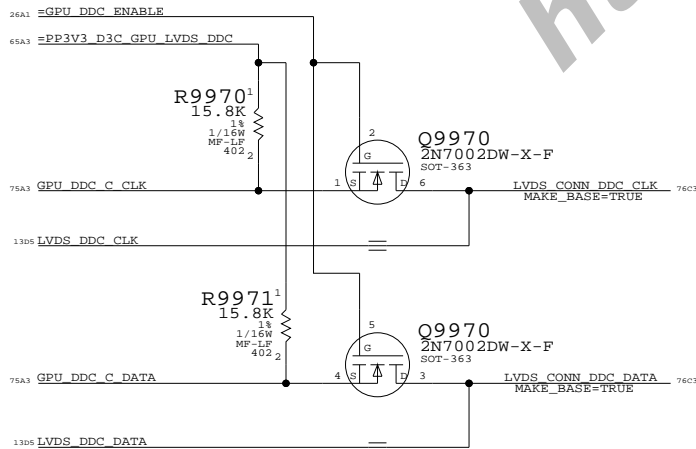


LVDS Mux Selection Qualification

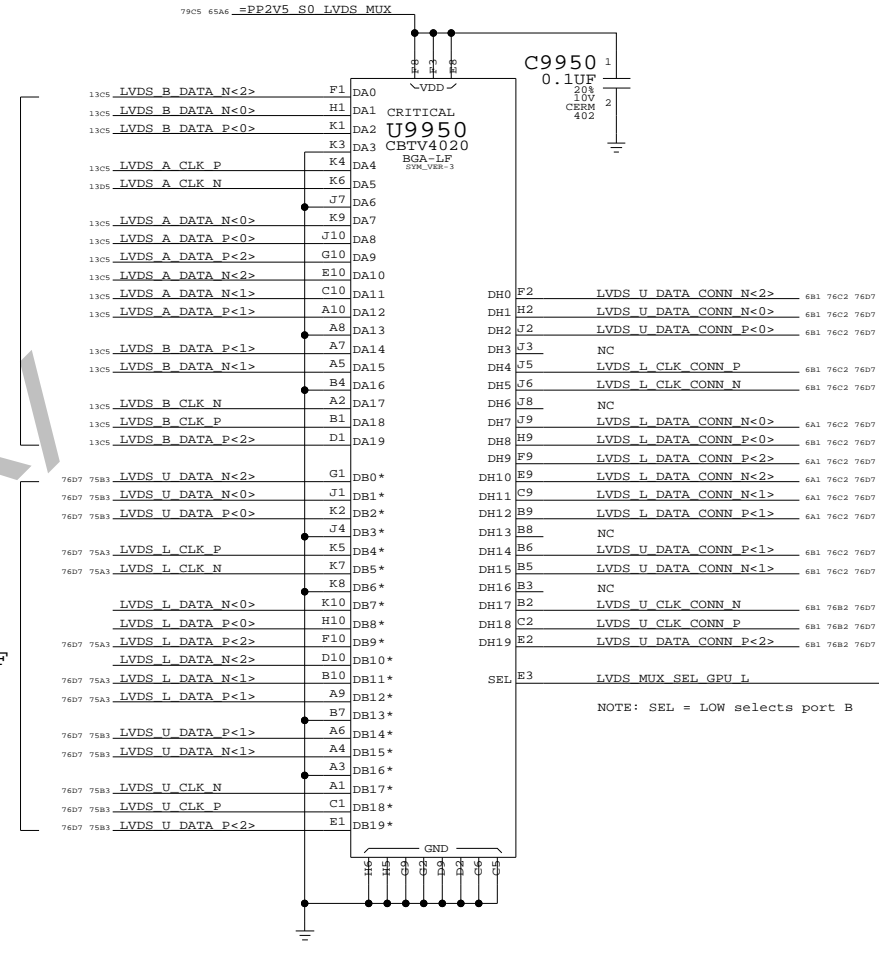
Enables the GPU LVDS path in the mux with the qualification that the GPU has turned on panel power and that the panel power has risen to (near) 3.3V. This should eliminate need for LVDS pulldowns



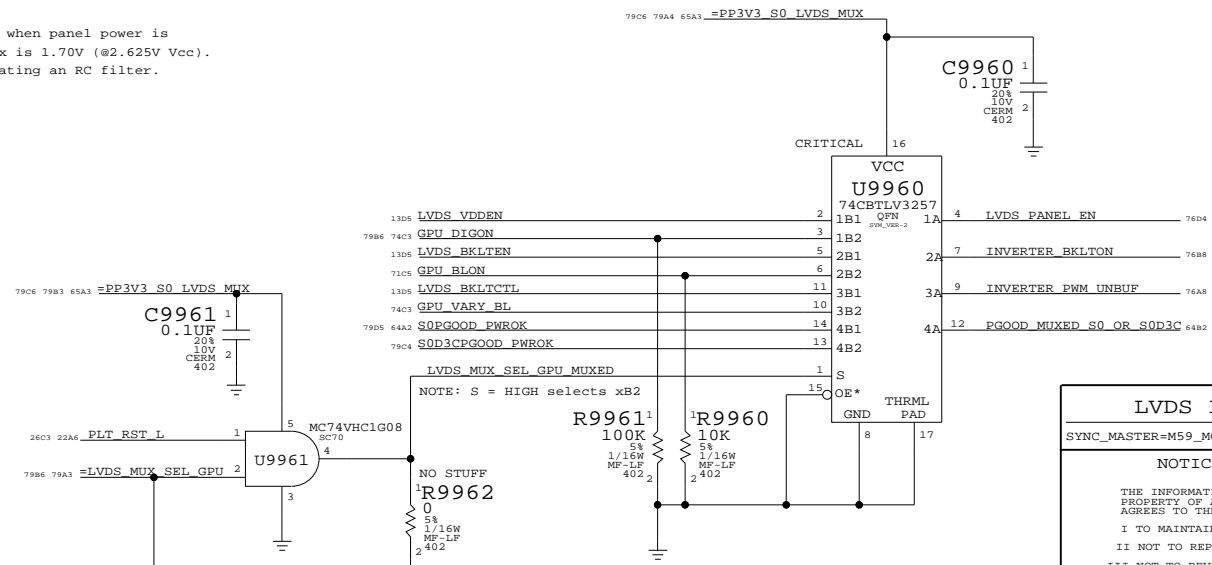
GPU DDC Pass FETs



LVDS I/F Mux



Panel/Backlight Control Mux



LVDS Interface Pull-downs
SYNC_MASTER=M59_MG SYNC_DATE=08/01/2006
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SCALE	SHT	OF
NONE	79	84

D

D

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR	*	=3:1_SPACING	
FSB_ADDR2ADDR	*	=2:1_SPACING	
FSB_ADSTB	*	=3:1_SPACING	
FSB_ADDR2ADSTB	*	=3:1_SPACING	

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=3:1_SPACING	
FSB_DATA2DATA	*	=2:1_SPACING	
FSB_DSTB	*	=3:1_SPACING	
FSB_DATA2DSTB	*	=3:1_SPACING	

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_COMMON	*	=2:1_SPACING	

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended.
Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs.
Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs.
DSTB complementary pairs are spaced 3:1, even in constraint areas.
Design Guide recommends each strobe/signal group is routed on the same layer.
Design Guide recommends FSB signals be routed only on internal layers.
NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.
NOTE: Design Guide allows closer spacing if signal lengths can be shortened.
SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 4.2 & 4.3

C

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_27O1	*	=2:1_SPACING	
CPU_COMP	*	25 MIL	
CPU_OTLREF	*	25 MIL	
CPU_1TP	*	=2:1_SPACING	
CPU_VCCSENSE	*	25 MIL	

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.
SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 4.4, 4.6.2, & 5.8.2.4

DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	Y	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	Y	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_85D	*	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	
MEM_CTRL2CTRL	*	=2:1_SPACING	
MEM_CTRL2MEM	*	=3:1_SPACING	
MEM_CMD2CMD	*	=1.5:1_SPACING	
MEM_CMD2MEM	*	=3:1_SPACING	
MEM_DATA2DATA	*	=1.5:1_SPACING	
MEM_DATA2MEM	*	=3:1_SPACING	
MEM_DQS2MEM	*	=3:1_SPACING	
MEM_2OTHER	*	25 MIL	

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

Need to support MEM_*-style wildcards!

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 6.2

PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	20 MIL	
DMI	*	20 MIL	

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 7.2, 9.2 & 10.5.2

Disk Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IDE_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
IDE	*	=1.8:1_SPACING	
SATA	*	20 MIL	

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 10.6 & 10.7.2

Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIO_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	=1.8:1_SPACING	

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB2_90D	*	Y	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB2	*	=4:1_SPACING	
USB2_2CLK	*	25 MIL	

DG says minimum spacing 50 mils to clocks

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.10.1.2

Internal Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=3:1_SPACING	
SPI	*	=1.8:1_SPACING	

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.17.1.1

Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	25 MIL	
CLK_PCIE	*	20 MIL	
CLK_MED	*	20 MIL	
CLK_SLOW	*	10 MIL	

B

B

A

A

Napa Platform Constraints

SYNC_MASTER=(MASTER)

SYNC_DATE=(MASTER)


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SCALE

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D	GDDR3 (Frame Buffer) Memory Bus Constraints							High-Speed I/O Interface Constraints																																																																
	<table><tr><th>PHYSICAL_RULE_SET</th><th>LAYER</th><th>ALLOW ROUTE ON LAYER?</th><th>MINIMUM LINE WIDTH</th><th>MINIMUM NECK WIDTH</th><th>MAXIMUM NECK LENGTH</th><th>DIFFPAIR PRIMARY GAP</th><th>DIFFPAIR NECK GAP</th></tr><tr><td>FB_35S_TO_55S</td><td>*</td><td>Y</td><td>=35_OHM_SE</td><td>=55_OHM_SE</td><td>=35_55_OHM_SE</td><td>=STANDARD</td><td>=STANDARD</td></tr><tr><td>FB_40S</td><td>*</td><td>Y</td><td>=40_OHM_SE</td><td>=40_OHM_SE</td><td>=40_OHM_SE</td><td>=STANDARD</td><td>=STANDARD</td></tr><tr><td>FB_55S</td><td>*</td><td>Y</td><td>=55_OHM_SE</td><td>=55_OHM_SE</td><td>=55_OHM_SE</td><td>=STANDARD</td><td>=STANDARD</td></tr><tr><td>FB_75D</td><td>*</td><td>Y</td><td>=75_OHM_DIFF</td><td>=75_OHM_DIFF</td><td>=75_OHM_DIFF</td><td>=75_OHM_DIFF</td><td>=75_OHM_DIFF</td></tr></table>							PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	FB_35S_TO_55S	*	Y	=35_OHM_SE	=55_OHM_SE	=35_55_OHM_SE	=STANDARD	=STANDARD	FB_40S	*	Y	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD	FB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD	FB_75D	*	Y	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	<table><tr><th>PHYSICAL_RULE_SET</th><th>LAYER</th><th>ALLOW ROUTE ON LAYER?</th><th>MINIMUM LINE WIDTH</th><th>MINIMUM NECK WIDTH</th><th>MAXIMUM NECK LENGTH</th><th>DIFFPAIR PRIMARY GAP</th><th>DIFFPAIR NECK GAP</th></tr><tr><td>ENET_100D</td><td>*</td><td>Y</td><td>=100_OHM_DIFF</td><td>=100_OHM_DIFF</td><td>=100_OHM_DIFF</td><td>=100_OHM_DIFF</td><td>=100_OHM_DIFF</td></tr><tr><td>FW_110D</td><td>*</td><td>Y</td><td>=110_OHM_DIFF</td><td>=110_OHM_DIFF</td><td>=110_OHM_DIFF</td><td>=110_OHM_DIFF</td><td>=110_OHM_DIFF</td></tr></table>	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	ENET_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	FW_110D	*	Y	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF
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8	7	6	5	4	3	2	1																																																																	

	8	7	6	5	4	3	2	1
D	M59 Board-Specific Spacing & Physical Constraints							
	BOARD LAYERS				BOARD AREAS		BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
	TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM				NO_TYPE, BGA		MM	15.2
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	DEFAULT	*	Y	=55_OHM_SE	=55_OHM_SE	30 MM	0 MM	0 MM
	STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	55_OHM_SE	TOP, BOTTOM	Y	0.100 MM	0.100 MM			
	55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
C	50_OHM_SE	TOP, BOTTOM	Y	0.124 MM	0.124 MM			
	50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	45_OHM_SE	TOP, BOTTOM	Y	0.150 MM	0.150 MM			
	45_OHM_SE	*	Y	0.105 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	40_OHM_SE	TOP, BOTTOM	Y	0.185 MM	0.185 MM			
	40_OHM_SE	*	Y	0.131 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	35_OHM_SE	TOP, BOTTOM	Y	0.230 MM	0.230 MM			
	35_OHM_SE	*	Y	0.165 MM	0.165 MM	=STANDARD	=STANDARD	=STANDARD
B	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	27P4_OHM_SE	TOP, BOTTOM	Y	0.335 MM	0.335 MM			
	27P4_OHM_SE	*	Y	0.240 MM	0.240 MM	=STANDARD	=STANDARD	=STANDARD
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	35_55_OHM_SE	TOP, BOTTOM	Y	0.230 MM	0.100 MM			
	35_55_OHM_SE	*	Y	0.165 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD
	Unsupported rule							
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	75_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
A	70_OHM_DIFF	*	Y	0.149 MM	0.149 MM	=STANDARD	0.125 MM	0.125 MM
	70_OHM_DIFF	TOP, BOTTOM	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	75_OHM_DIFF	*	Y	0.131 MM	0.131 MM	=STANDARD	0.125 MM	0.125 MM
	75_OHM_DIFF	TOP, BOTTOM	Y	0.161 MM	0.161 MM		0.125 MM	0.125 MM
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	80_OHM_DIFF	*	Y	0.115 MM	0.111 MM	=STANDARD	0.125 MM	0.125 MM
	80_OHM_DIFF	TOP, BOTTOM	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	85_OHM_DIFF	*	Y	0.101 MM	0.101 MM	=STANDARD	0.125 MM	0.125 MM
	85_OHM_DIFF	TOP, BOTTOM	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	90_OHM_DIFF	*	Y	0.102 MM	0.102 MM	=STANDARD	0.220 MM	0.220 MM
	90_OHM_DIFF	TOP, BOTTOM	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	100_OHM_DIFF	*	Y	0.080 MM	0.080 MM	=STANDARD	0.200 MM	0.200 MM
	100_OHM_DIFF	TOP, BOTTOM	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
	110_OHM_DIFF	*	Y	0.077 MM	0.077 MM	=STANDARD	0.330 MM	0.330 MM
	110_OHM_DIFF	TOP, BOTTOM	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM
	8	7	6	5	4	3	2	1

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	
STANDARD	*	=DEFAULT	
BGA_P1MM	*	=DEFAULT	
BGA_P2MM	*	=DEFAULT	
BGA_P3MM	*	=DEFAULT	

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_MED	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FB_CLK	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	
1.8:1_SPACING	*	0.18 MM	
2:1_SPACING	*	0.2 MM	
2.5:1_SPACING	*	0.25 MM	
3:1_SPACING	*	0.3 MM	
4:1_SPACING	*	0.4 MM	

Allow 0.1 MM on blind-to-buried via dogbones (layers 2 & 11)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	ISL2, ISL11	0.1 MM	
1.8:1_SPACING	ISL2, ISL11	0.1 MM	
2:1_SPACING	ISL2, ISL11	0.1 MM	
2.5:1_SPACING	ISL2, ISL11	0.1 MM	
3:1_SPACING	ISL2, ISL11	0.1 MM	
4:1_SPACING	ISL2, ISL11	0.1 MM	

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	ISL2, ISL11	0.1 MM	
CLK_PCIE	ISL2, ISL11	0.1 MM	
CLK_MED	ISL2, ISL11	0.1 MM	
CLK_SLOW	ISL2, ISL11	0.1 MM	
CPU_COMP	ISL2, ISL11	0.1 MM	
CPU_OTLREF	ISL2, ISL11	0.1 MM	
CPU_VCCSENSE	ISL2, ISL11	0.1 MM	
DMI	ISL2, ISL11	0.1 MM	
LVDS_PAIR2PAIR	ISL2, ISL11	0.1 MM	
MEM_2OTHER	ISL2, ISL11	0.1 MM	
PCIE	ISL2, ISL11	0.1 MM	
SATA	ISL2, ISL11	0.1 MM	
TMDS_PAIR2PAIR	ISL2, ISL11	0.1 MM	
VGA	ISL2, ISL11	0.1 MM	

Rules for "Topology #3" for FSB signals, Napa DG tables 4-7 & 4-12.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR OVERRIDE	*	=2:1_SPACING OVERRIDE	OVERRIDE
FSB_ADDR2ADDR OVERRIDE	*	=STANDARD OVERRIDE	OVERRIDE
FSB_ADSTB OVERRIDE	*	=2:1_SPACING OVERRIDE	OVERRIDE
FSB_ADDR2ADSTB OVERRIDE	*	=2:1_SPACING OVERRIDE	OVERRIDE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA OVERRIDE	*	=2:1_SPACING OVERRIDE	OVERRIDE
FSB_DATA2DATA OVERRIDE	*	=STANDARD OVERRIDE	OVERRIDE
FSB_DSTB OVERRIDE	*	=2:1_SPACING OVERRIDE	OVERRIDE
FSB_DATA2DSTB OVERRIDE	*	=2:1_SPACING OVERRIDE	OVERRIDE

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS	*	LVDS_100D
TMDS	*	TMDS_100D
TMDSCONN	*	TMDS_100D
VGA	*	VGA_75S

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_2OTHER OVERRIDE	*	0.5 MM OVERRIDE	OVERRIDE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI_2PCI OVERRIDE	*	0.1 MM OVERRIDE	OVERRIDE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCI	PCI	*	PCI_2PCI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENETCONN	*	*	ENET
TMDSCONN	*	*	TMDS


"Stale" physical / spacing types

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ANALOG	*	*	FSB_COMMON
FSB_P2MM	*	*	FSB_COMMON
I2C	*	*	SMB
GND	*	*	STANDARD
MEM_PP1V8_S3	*	*	STANDARD
FB_PP1V8	*	*	STANDARD

FSB_ANALOG	
FSB_P2MM	
I2C	
GND	
MEM_PP1V8_S3	
FB_PP1V8	
PCI	PCI 55S

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S OVERRIDE	*	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D OVERRIDE	*	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	*	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

M59 Spacing & Physical Constraints	
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)
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 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7150	REV. A.0.0
	SCALE NONE	SHT 83	OF 84

8		7		6		5		4		3		2		1	
D	ELECTRICAL_CONSTRAINT_SET	NET_TYPE													
		PHYSICAL		SPACING											
		FSB_55S		FSB_COMMON		FSB_ADS_L		5D5 7D6 12C4							
		FSB_55S		FSB_COMMON		FSB_BNR_L		5D5 7D6 12C4							
		FSB_55S		FSB_COMMON		FSB_BPRT_L		7D6 12C4							
		FSB_55S		FSB_COMMON		FSB_BREQ0_L		5D5 7D6 12C4							
		FSB_55S		FSB_COMMON		FSB_DBSY_L		5D5 7D6 12B4							
		FSB_55S		FSB_COMMON		FSB_DEFER_L		7D6 12B4							
		FSB_55S		FSB_COMMON		FSB_DPWR_L		7B3 12B4							
		FSB_55S		FSB_COMMON		FSB_DRDY_L		5D5 7D6 12B4							
C		FSB_55S		FSB_COMMON		FSB_HIT_L		5D5 7D6 12B4							
		FSB_55S		FSB_COMMON		FSB_HITM_L		5D5 7D6 12B4							
		FSB_55S		FSB_COMMON		FSB_LOCK_L		5D5 7D6 12B4							
		FSB_55S		FSB_COMMON		FSB_RS_L<2..0>		7D6 12A4							
		FSB_55S		FSB_COMMON		FSB_TRDY_L		7D6 12A4							
		FSB_55S		FSB_COMMON		FSB_CPURST_L		7D6 11B5 12C4							
		FSB_55S		FSB_DATA		FSB_D_L<63..0>		5D5 7B3 7B4 7C3 7C4 12B6 12C6 12D6							
		FSB_55S		FSB_DATA		FSB_DINV_L<3..0>		5D5 7B3 7B4 7C3 7C4 12B4							
		FSB_55S		FSB_DATA		FSB_DSTBP_L<3..0>		5D5 7B3 7B4 7C3 7C4 12B4							
		FSB_55S		FSB_DATA		FSB_DSTBN_L<3..0>		5D5 7B3 7B4 7C3 7C4 12B4							
B		FSB_55S		FSB_ADDR		FSB_A_L<31..3>		5D5 7C8 7D8 12C4 12D4							
		FSB_55S		FSB_ADDR		FSB_REQ_L<4..0>		5D5 7D8 12A4 12B4							
		FSB_55S		FSB_ADDR		FSB_ADSTB_L<3..0>		5D5 7C8 7D8 12C4							
		CPU_55S				FSB_IERR_L		7D6							
		CPU_55S				FSB_FERR_L									
		CPU_55S				CPU_PWRGD		7B3 21C4							
		CPU_55S				CPU_INTR		7C8 21C4							
		CPU_55S				CPU_NMI		7C8 21C4							
		CPU_55S				CPU_A20M_L		7C8 21C4							
		CPU_55S				CPU_DPSP_L		7B3 21C4							
A		CPU_55S				CPU_IGNNE_L		7C8 21C4							
		CPU_55S				CPU_INIT_L		7D6 21C4							
		CPU_55S				CPU_SMI_L		7C8 21C4							
		CPU_55S				CPU_STPCLK_L		7C8 21C4							
		CPU_55S		CPU_2T01		CPU_THERMTRIP_L									
		CPU_55S		CPU_2T01		PM_DPRSLEVR		14B7 23C3 59C8							
		CPU_55S		CPU_2T01		IMVP_DPRSLEVR		59C7							
		CPU_55S		CPU_GTLREF		CPU_GTLREF		7B4							
		CPU_55S		CPU_COMP		CPU_COMP<3>		7B3							
		CPU_27F4S		CPU_COMP		CPU_COMP<2>		7B3							
														</	