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1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.

2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.

3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

OROYA

03/20/2007 - DVT

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Sync

N/A

08/23/2006

08/23/2006

N/A

N/A

N/A

N/A

(MASTER)

(MASTER)

(T9_MLB)

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M76_MLB

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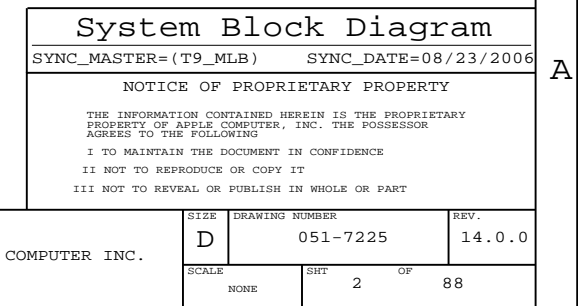
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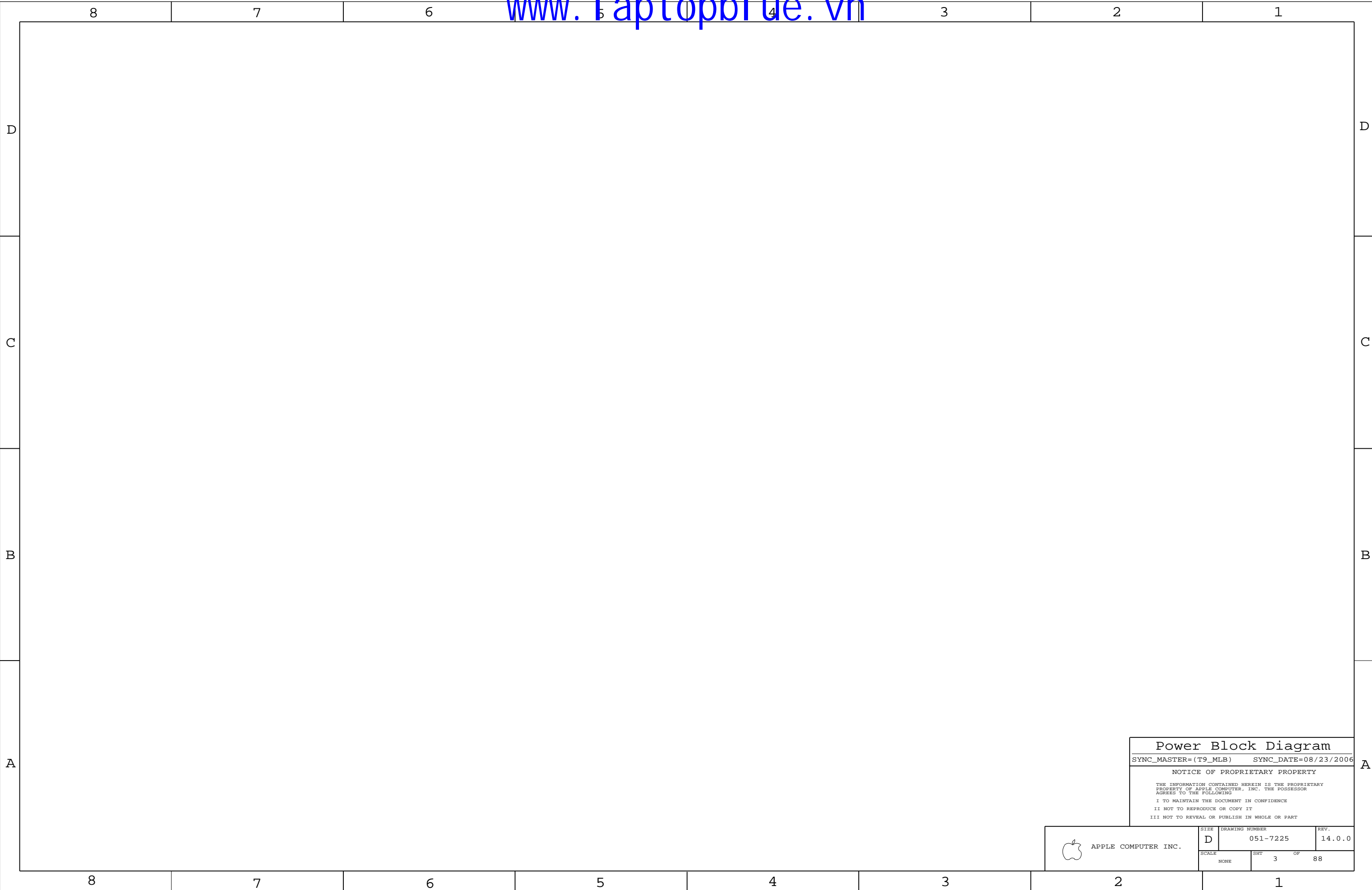
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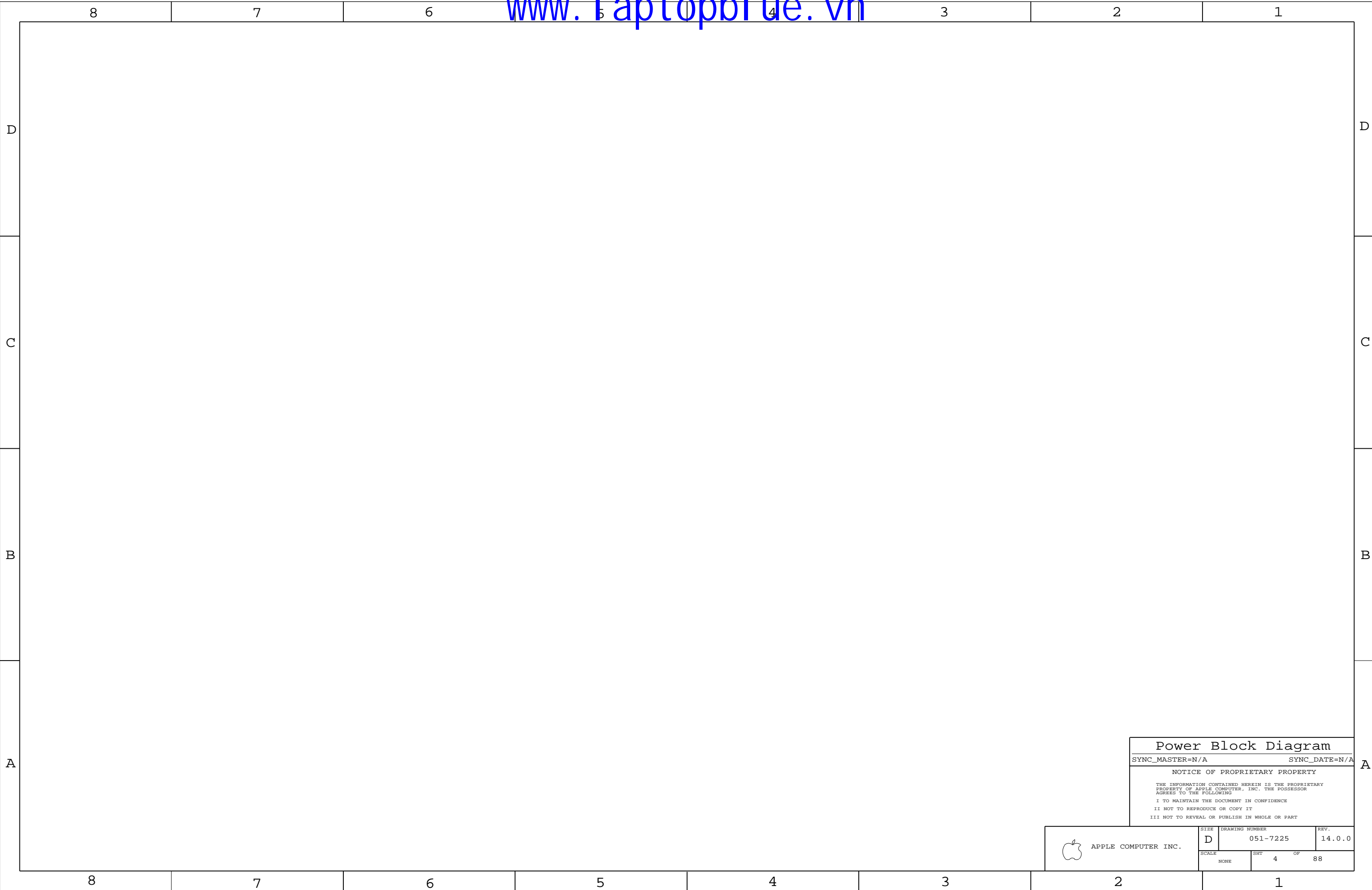
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Power Block Diagram		
SYNC_MASTER=(T9_MLB)		SYNC_DATE=08/23/2006
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 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7225	REV. 14.0.0
	SCALE NONE	SHT 3 OF 88	



Power Block Diagram		
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 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7225	REV. 14.0.0
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	<table><tr><th>BOM NUMBER</th><th>BOM NAME</th><th>BOM OPTIONS</th></tr><tr><td>630-7931</td><td>PCBA,OROYA1,M75</td><td>M75_COMMON,EEE_X5D,CPU_2_2GHZ,FB_128_SAMSUNG</td></tr><tr><td>630-7932</td><td>PCBA,OROYA2,M75</td><td>M75_COMMON,EEE_X5E,CPU_2_4GHZ,FB_256_SAMSUNG</td></tr><tr><td>630-8659</td><td>PCBA,OROYA1,VRAM-HY,M75</td><td>M75_COMMON,EEE_XXS,CPU_2_2GHZ,FB_128_HYNIX</td></tr><tr><td>630-8662</td><td>PCBA,OROYA2,VRAM-HY,M75</td><td>M75_COMMON,EEE_XXT,CPU_2_4GHZ,FB_256_HYNIX</td></tr></table>								BOM NUMBER	BOM NAME	BOM OPTIONS	630-7931	PCBA,OROYA1,M75	M75_COMMON,EEE_X5D,CPU_2_2GHZ,FB_128_SAMSUNG	630-7932	PCBA,OROYA2,M75	M75_COMMON,EEE_X5E,CPU_2_4GHZ,FB_256_SAMSUNG	630-8659	PCBA,OROYA1,VRAM-HY,M75	M75_COMMON,EEE_XXS,CPU_2_2GHZ,FB_128_HYNIX	630-8662	PCBA,OROYA2,VRAM-HY,M75	M75_COMMON,EEE_XXT,CPU_2_4GHZ,FB_256_HYNIX																																																																										
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826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:XXT]	CRITICAL	EEE_XXT																																																																																												
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	8	7	6	5	4	3	2	1
	<div><div>PROTO</div><div>See Perforce change notes for updates before Proto Release 12/22/06 -- Released for Proto (Schem Rev 08, PCB Rev 01)</div><div>EVT</div><div>8.1.0: 01/05/07 -- Clock Termination: Removed NO STUFF property from R3067 01/05/07 -- GPU FB: Corrected FB CLK termination (added cap and removed connection to VDDQ) 8.2.0: 01/08/07 -- GPU FB: Added VREF support for unterminated memory mode (added FETs and pulldown Rs) 9.0.0: 01/09/07 -- Temp Sensors: NO STUFFed C5520 (circuit should have only 1 cap) 01/12/07 -- Power Aliases: Moved Ethernet to PP3V3_S3 from S5 (layout improvements) 01/12/07 -- Power Supplies: Minor power supply feedback connection changes from M76 9.1.0: 01/17/07 -- Power Aliases: Moved LCD panel FET to PP3V3_S5 from S0 01/17/07 -- SMBus: Changed R5260 & R5261 from 4.7K to 3.3K 01/17/07 -- Sync with T9 noME (6.1.4) to pull in WOL_EN and Wake-on-Wireless support 01/17/07 -- Power FETs: Corrected BOM values for 5V/3.3V S3/S0 FETs 01/17/07 -- Power Sequencing: Added RC delay on PP1V8_S3 switcher enable 01/17/07 -- Testpoints: Removed FUNC_TEST from NB_RESET_L and FSB_DPWR_L per PCB request 01/17/07 -- BOM: Consolidated 3 caps on page 59 from 132S0120 to 132S0131 01/17/07 -- BOM: Added Hynix BOM configurations 9.2.0: 01/17/07 -- Power Aliases: Deleted alias that accidentally eliminated filtering on PP1V5_S0_SB_VCC1_5_B 01/18/07 -- Clock Termination: Changed series termination on all single ended clocks to 33 ohms 01/18/07 -- IMVP: Updated BOMOPTIONS and values for ISL9504B 01/18/07 -- Testpoints: Added NO_TEST property to LVDS_L_DATA_N<1>, _N<2>, _P<2> due to lack of layout space for TP 01/18/07 -- ODD Conn: Reconnected ODD power FET gate control circuitry to properly implement soft start (added one cap) 9.3.0: 01/19/07 -- SB Decoupling: Removed filtering for PP1V5_S0_SB_VCCGLANPLL to enable PP1V5_S0 corrections at SB 01/19/07 -- Ethernet Conn: Changed resistor short reference designators from R392x to RX392x 01/19/07 -- Clock Termination: Changed R3050 and R3055 to bypass discrete muxes for pending change to SLG2AP101 01/19/07 -- Power Sequencing: Added C7859 to create RC delay for 1.5 and 1.05V S0 rails 01/19/07 -- Power Sequencing: Changed power rail for U7850 to PP3V3_S5 to eliminate a leakage path 9.4.0: 01/19/07 -- GPU GPIOs: Added 2 TPs on GPIOs to make G-state externally visible 01/19/07 -- SB GPIOs: Changed SB_GPIO42 to WOW_EN and changed pullup to pulldown (T9_noME change 40787) 9.5.0: 01/22/07 -- LIO Conn: Removed unnecessary aliases as T9 reference design now matches M75 (T9_noME change 40998) 01/22/07 -- Clocks: Changed U2900 to SLG2AP101 as primary clock chip (T9_noME change 40975) 01/22/07 -- Clock Termination: Added R3051 for Silego 537/101 compatibility 01/22/07 -- BOM: Added BOMOPTIONS for SLG2AP101 (primary) and SLG8LP537 (backup) 01/22/07 -- BOM: Selected P1V8S3_1V825 BOMOPTION to lift voltage at FB memories 10.0.0: 01/23/07 -- BOM: Changed C3860/61 to 22pF from 27 pF based on -R characterization (T9_noME change 41248) 01/23/07 -- BOM: Changed FB memories to new Samsung and Hynix APNs (also added new BOMOPTIONS to GPU straps) 01/23/07 -- Released for EVT (Schem Rev 10, PCB Rev 02)</div><div><div>EVT_SE</div><div>10.1.0: 01/24/07 -- PATA Conn: Added pass FET Q4430 to allow PCIREQ3 (ODD reset GPIO) to pullup to S0 01/24/07 -- PATA Conn: Changed =PP5V_S0_ODDPWREN to =PP3V3_S0_ODDPWREN for minor power savings 01/24/07 -- Power Aliases: Updated PP3V3_S0 aliases to support above changes 10.2.0: 01/25/07 -- PATA Conn: Replaced PCIREQ pass FET with OD buffer to correct a corner case during PLTRST 01/25/07 -- Power Aliases: Updated PP5V_S0 aliases to support above changes 11.0.0: 01/25/07 -- BOM: Updated gain of PP1V25_ENET current sense amplifier to 165 (R5432 to 165K) 01/25/07 -- BOM: Updated all Intel APNs to use QS parts 01/25/07 -- Released for EVT (Schem Rev 11, PCB Rev 03) 12.0.0: 02/19/07 -- GPU Reset: Changed C2885 to 0.047uF to reduce reset delay on powerup 02/19/07 -- GPU PGOOD: Changed C9595 to 330pF to reduce PGOOD delay on powerup 02/19/07 -- Power Sequencing: NO STUFFed U7885 to remove GPU PGOOD from PWROK chain 02/19/07 -- Power Sequencing Rework: Short pins 2 and 4 of U7885 to complete PWROK chain 02/19/07 -- Released post-EVT to document what was built (Schem Rev 12)</div><div><div>DVT</div><div>12.1.0: 02/20/07 -- GPU FB: Changed cal resistors per Nvidia PUN (R8290 to 45.3 ohm and R8291 to 24.9 ohm) 02/20/07 -- GPU FB: Changed unterminated-mode reference voltage to 40% (R8297 -> 1.02K, R8432/82, R8532/82 -> 2.21K) 02/21/07 -- FireWire: Changed to Rev C of TI FireWire MCM (APN: 338S0435) 02/21/07 -- Power Sequencing: Removed U7885/C7885 to take GFX_PGOOD out of PWR_OK chain (rdar://4974927) 02/26/07 -- GPU Vcore: NO STUFFed all PWRCTL related components (feature not to be supported) 02/26/07 -- GPU Vcore: Updated voltage setpoints to 1.000/1.070/1.125V (rdar://5021453) 02/26/07 -- SB GPIOs: Sync'd page25.csa to T9_MLB to get pullup updates 02/26/07 -- Thermal Sensors: Updated topology of EMC1033 filter caps (added C5515 next to IC, moved other caps to connectors - rdar://5025773) 12.2.0: 02/27/07 -- ODD Conn: Changed ODD power FET to FDC606P (from FDC638P) for reduced Rds(on) (rdar://4993378) 02/28/07 -- Power Aliases: Moving PP1V8_GPU FET source to PP1V8_S3 rather than PP1V8_S3_ISNS to improve power delivery to GPU (rdar://5021462) 12.3.0: 02/28/07 -- Left Clutch IC: Updated both I-PEX connectors to new APN (part update for shell plating) 02/28/07 -- NB GFX Core: Changed Vcore controller to ISL6263B (part consolidation effort between Apple/Intersil - rdar://5009109) 02/28/07 -- Power Supplies: Replaced APN 152S0511 with 152S0368 (duplicate APNs for same part - rdar://5009109) 03/01/07 -- Thermal Sensors: Updated topology of EMC1033 sensors (removed shorts, changed connector caps to 18pF) 03/01/07 -- NB GFX Decoupling/Power Aliases: Connected VCCD_CRT of NB to GND per CRT disable guidelines 12.4.0: 03/01/07 -- LVDS Connector: Changed pin 5 of connector from NC to PP3V3_SW_LCD (in case we add extra cable for power - rdar://5024882) 03/01/07 -- NB GFX Decoupling: Added R2260 (0.3 ohm, 0603) to bring ESR of regulator output cap in spec (rdar://5000272) 12.5.0: 03/02/07 -- Power/Signal Aliases: Added XW0900 to PP5V_S5 to enable layout improvements 12.6.0: 03/06/07 -- Power FETs: Changed Q7080 to RJK0301 which provides much lower Rds(on) 03/06/07 -- FireWire Ports: Changed D4260 to PDS340 for lower height 12.7.0: 03/06/07 -- FireWire Ports: Changed D4260 to PDS540 for higher current capacity 03/06/07 -- Ethernet Connector: Removed RX shorts on Ethernet MDI lines per EMC request 03/06/07 -- SB GPIOs: Changed R2514 from pulldown to pullup to correct auto power-on issue (Linda card detect GPIO) 03/06/07 -- DDR2 Regulator: Changed FB resistors to 0.1% to raise guaranteed lowest output voltage</div></div></div></div>							
	8	7	6	5	4	3	2	1

DVT (cont'd)

12.8.0:
03/08/07 -- Thermal Sensors: Added R5515/R5516 in case low pass filter is needed for EMC1033
13.0.0:
03/12/07 -- Power Control: Corrected alias connections for 5V/3V3 S5 enable signals
13.1.0:
03/13/07 -- BOM Options: Removed HDCP BOM option from stuffing list (feature removed)
03/14/07 -- Constraints: Constrained WWAN_SIM signals to 50 ohms
03/14/07 -- Thermal Sensors/Aliases: Changed mounting pads of Th2H sensor connector to left clutch chassis gnd
13.2.0:
03/16/07 -- Thermal Sensors: Replaced EMC1033 with second EMC1043 for improved noise filtering
03/16/07 -- NB GFX: LVDS_VREFL/VREFH changed to single pin nets to prevent LVDS glitches per Intel
03/16/07 -- Yukon Power Control: Crystal caps changed to 18pF (rdar://4946795 and rdar://4945362)
13.3.0:
03/16/07 -- Thermal Sensors: Moved remote sensor U5500 to SMC SMBus "A" and S3 power rail to clear I2C addr clash
13.4.0:
03/19/07 -- Thermal Sensors: Updated U5500 power alias to indicate device should be on S3 rail
03/19/07 -- Power Control: Added U7858 to level shift PM_G2_EN from 3.42V to 5V
03/19/07 -- Power Supplies: For 1.8, 3.3 and 5V, removed VBST 0-ohm series R (rdar://5070179)
03/19/07 -- Power Supplies: For 1.8, 3.3 and 5V, increased cap size to 0603/0805 on VBST caps (rdar://5070179)
13.5.0:
03/19/07 -- Power Control: Tied all 4 5V/3.3V enables (EN1, EN2, EN3, EN5) together as part of PM_G2_EN
14.0.0:
03/20/07 -- GPU Vcore: Updated setpoints for GPU Vcore based upon Nvidia Vmin (i.e. 1.05V,1.05V,1.05V,1.125V)
03/20/07 -- FB: Changed FB VREF caps to 2x0.0047uF as required in Nvidia PUN 02736-001-v07 (which requests 1x0.01uF)

Revision History

SYNC_MASTER=N/A SYNC_DATE=N/A

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APPLE COMPUTER INC.

SIZE

D

DRAWING NUMBER

051-7225

REV.

14.0.0

SCALE

NONE

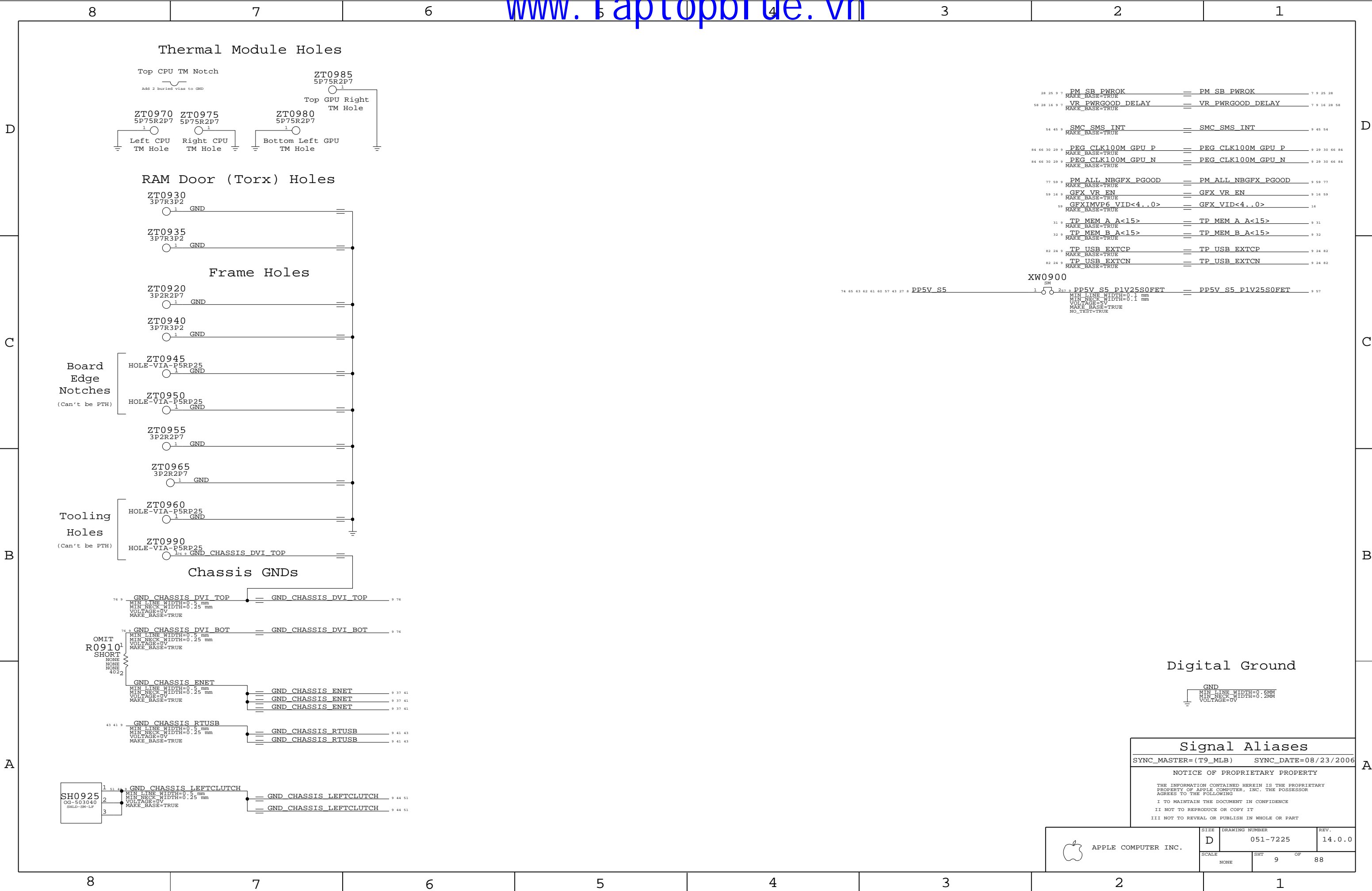
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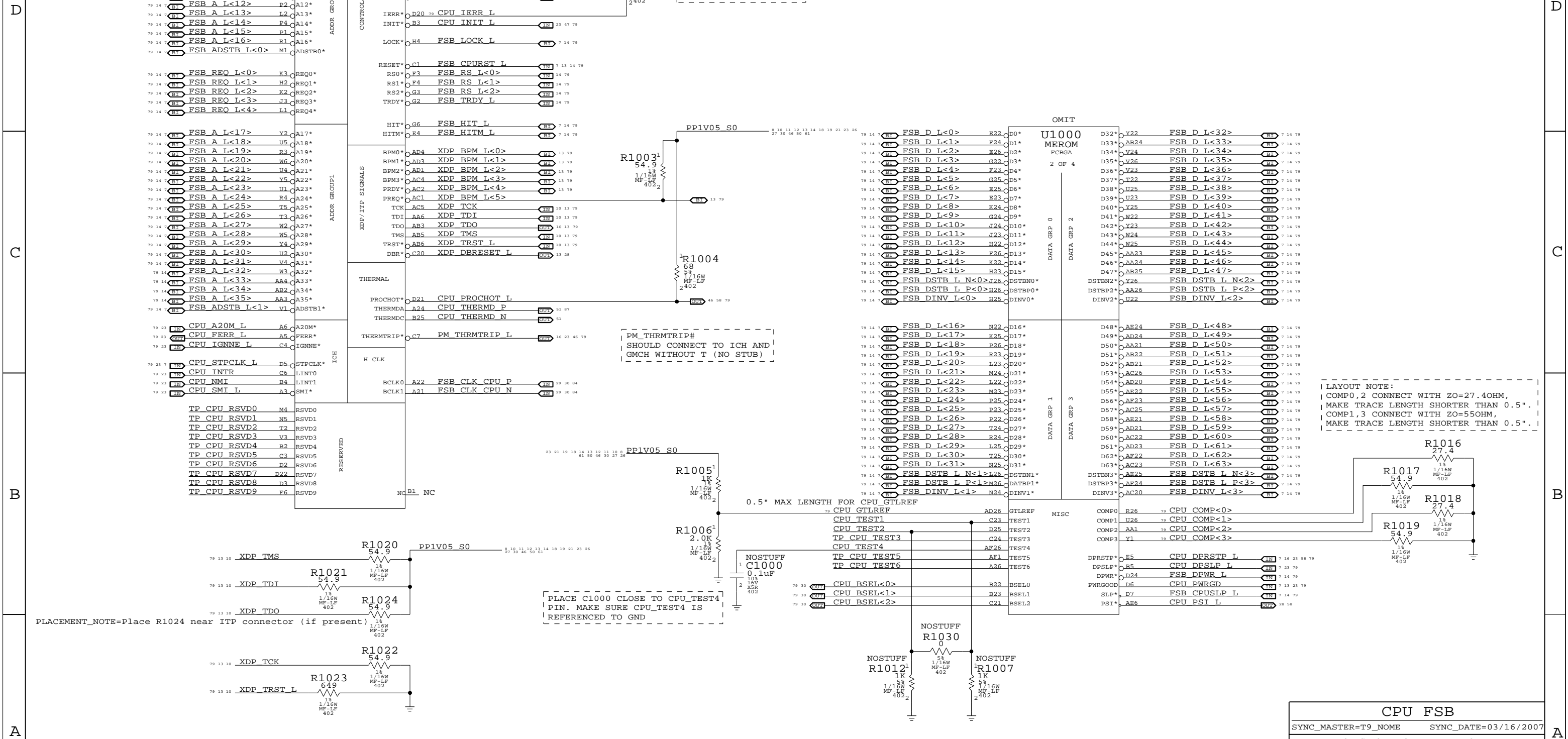
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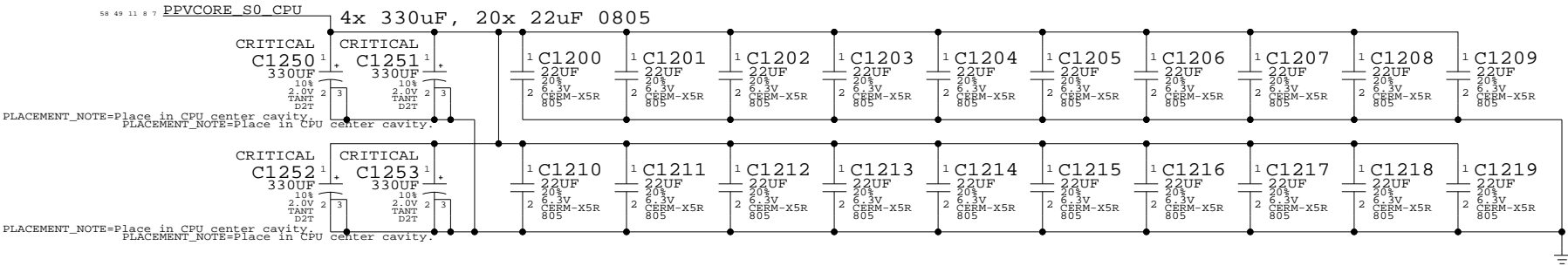
88

8	7	6	5	4	3	2	1
Functional Test Points				ICT Test Points			
Fan Connectors		Battery Digital Connector		CPU FSB NO_TESTS		NB NO_TESTS	
FANC_TEST		FANC_TEST		NO_TEST		NO_TEST	
<div><div></div><div></div><div></div><div></div><div></div><div></div></div> <div>TRUE PP5V S07 8 27 42 47 52 5758 59 65 76 78</div> <div>TRUE FAN LT PWM52</div> <div>TRUE FAN LT TACH52</div> <div>TRUE FAN RT PWM52</div> <div>TRUE FAN RT TACH52</div>		<div><div></div><div></div><div></div><div></div></div> <div>TRUE SMC BS ALRT L45 46 56</div> <div>TRUE SMBUS_SMC_BSA_SCL45 48 56 84</div> <div>TRUE SMBUS_SMC_BSA_SDA45 48 56 84</div> <div>TRUE GND BATT56</div>		<div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></di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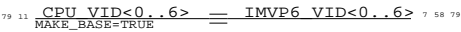




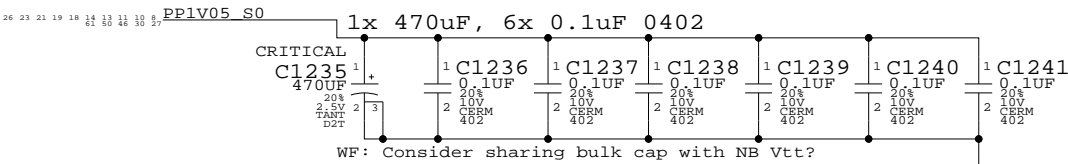
CPU VCORE HF AND BULK DECOUPLING



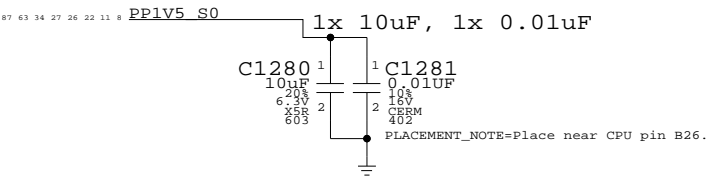
CPU VCORE VID CONNECTIONS



VCCP (CPU I/O) DECOUPLING



VCCA (CPU AVdd) DECOUPLING



CPU Decoupling & VID

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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APPLE COMPUTER INC.

SIZE

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DRAWING NUMBER

051-7225

REV.

14.0.0

SCALE

NONE

SHT

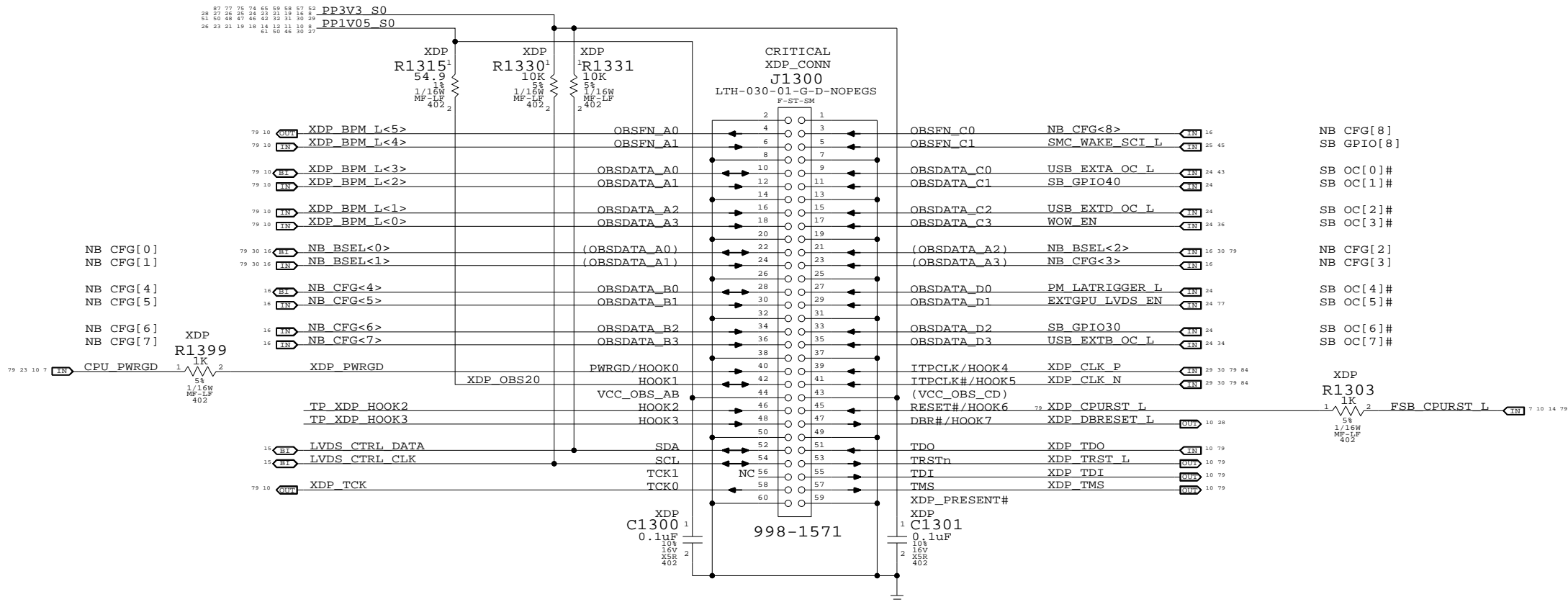
12

OF

88

Mini-XDP Connector

NOTE: This is not the standard XDP pinout.
Use with 920-0451 adapter board to support CPU, NB & SB debugging.



Direction of XDP module

Please avoid any obstructions
on even-numbered side of J1300

eXtended Debug Port (XDP)

SYNC_MASTER=T9_NOME SYNC_DATE=12/12/2006

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
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NONE	13	88

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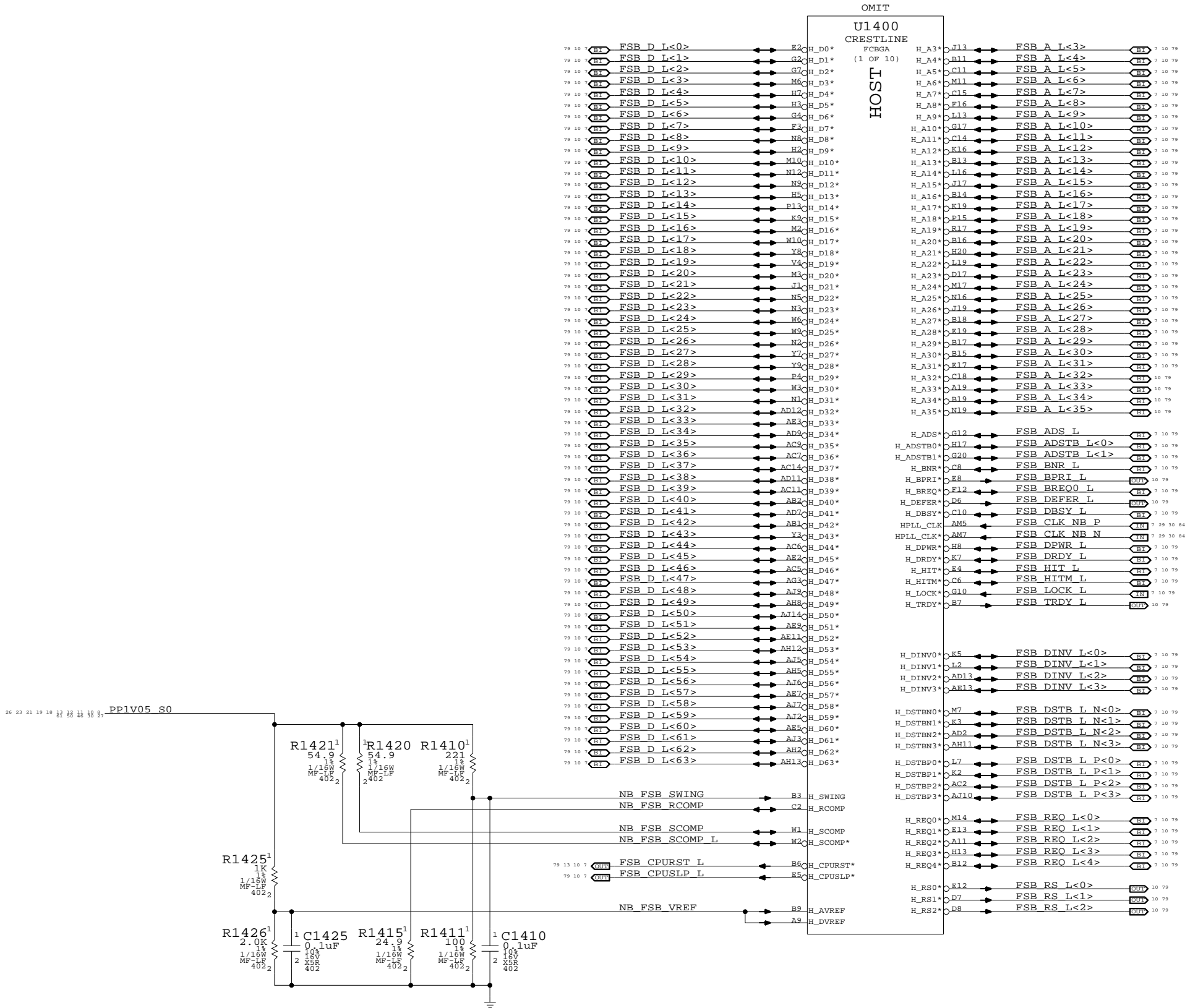
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NB CPU Interface

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

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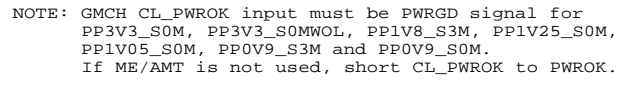
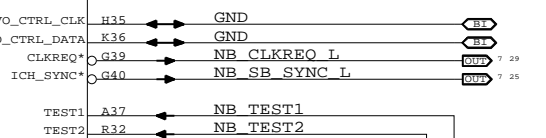
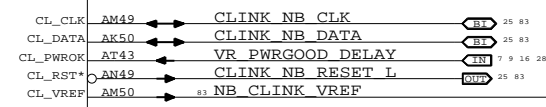
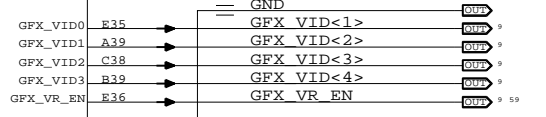
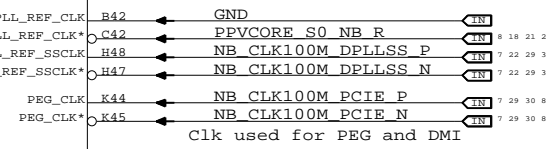
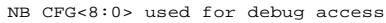
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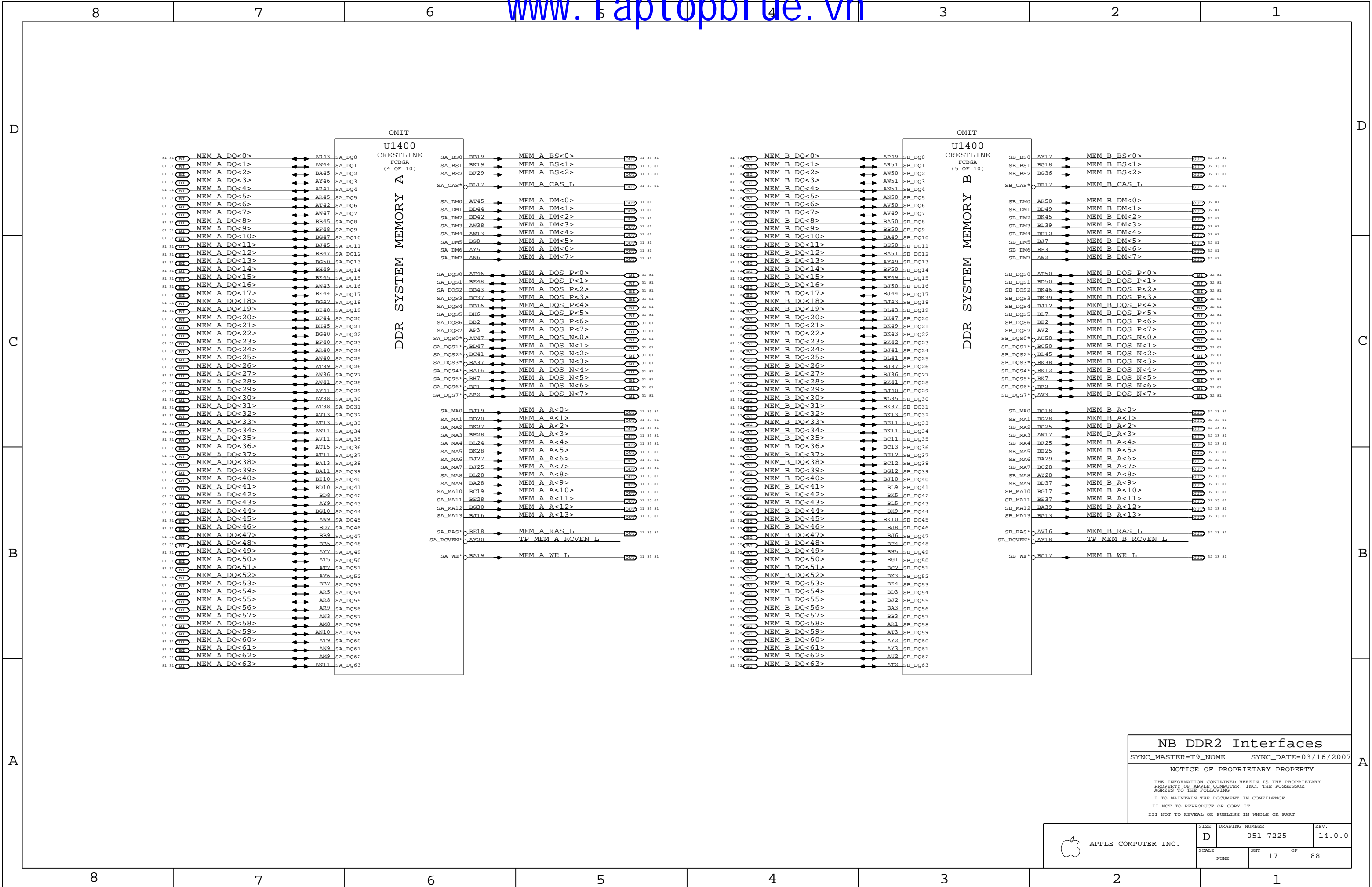
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7225	REV. 14.0.0
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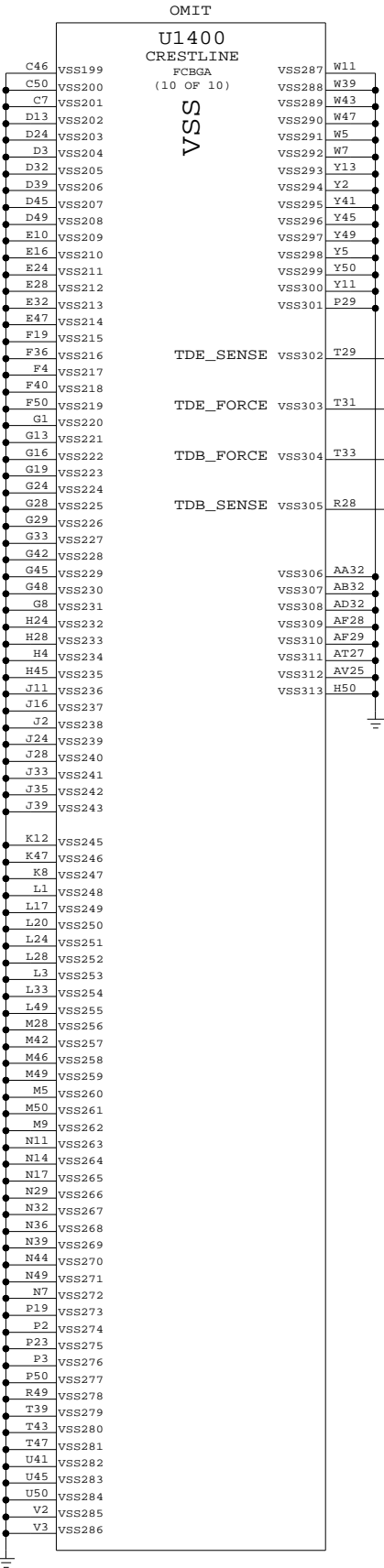
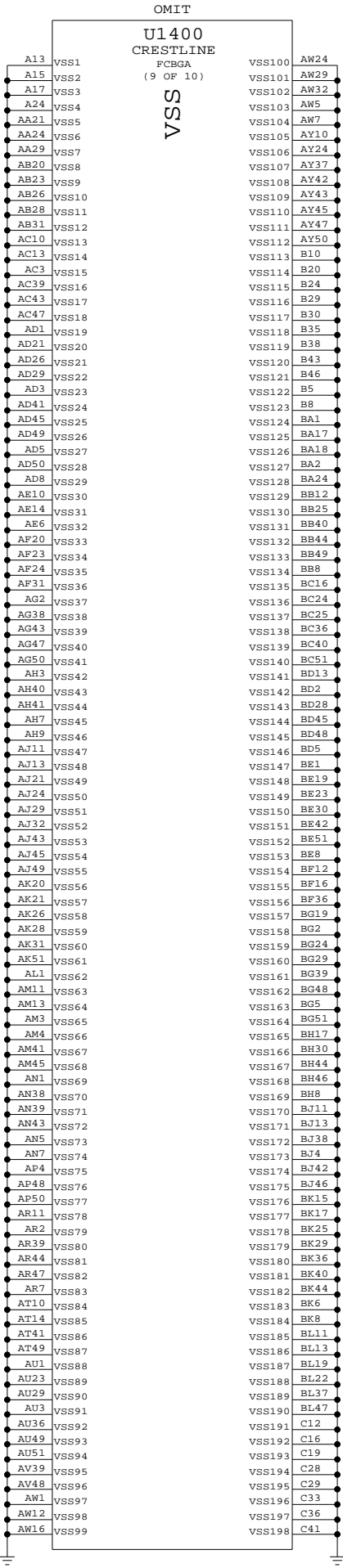
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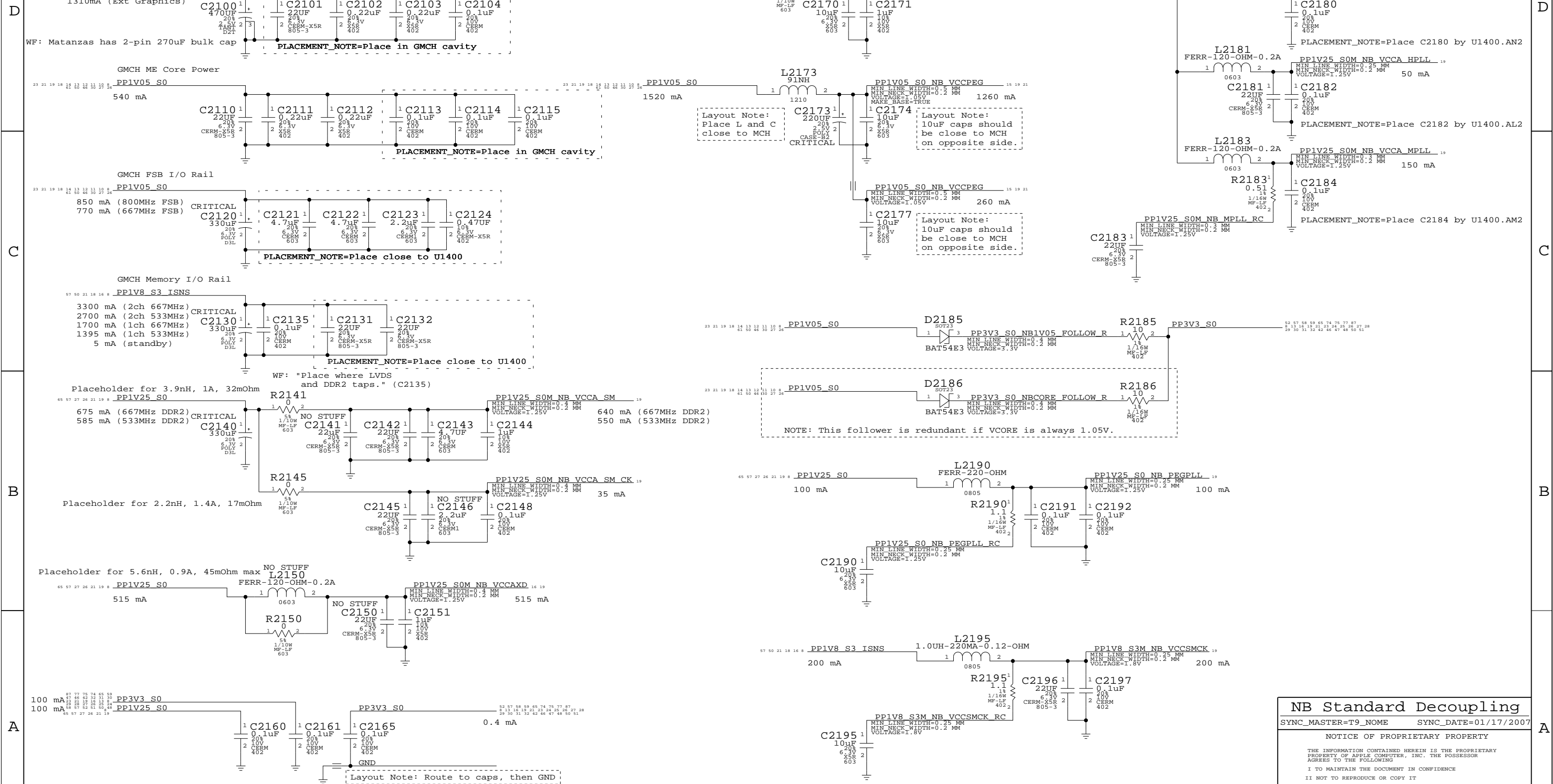
Crestline Thermal Diode Pins

Mainly for investigation. If not used, alias these nets directly to GND.

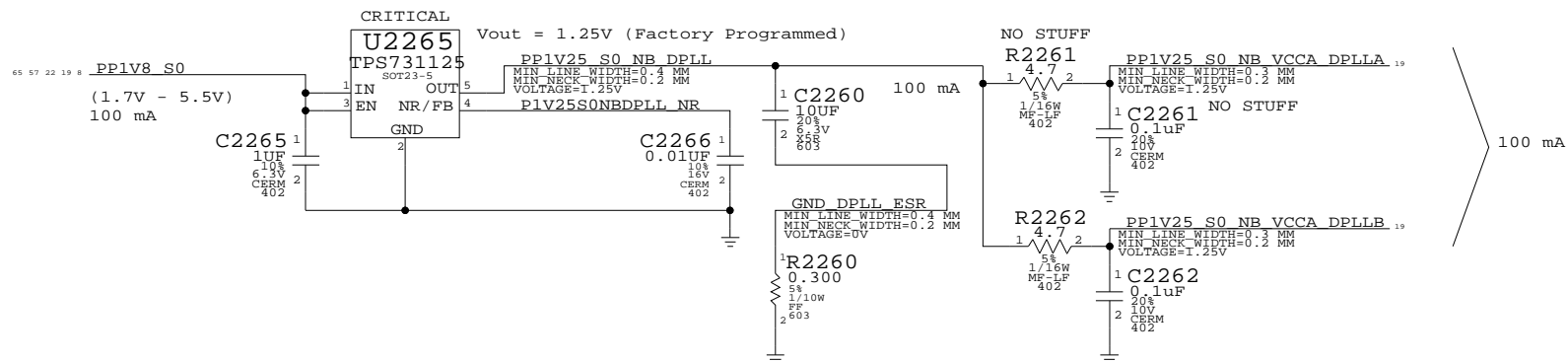
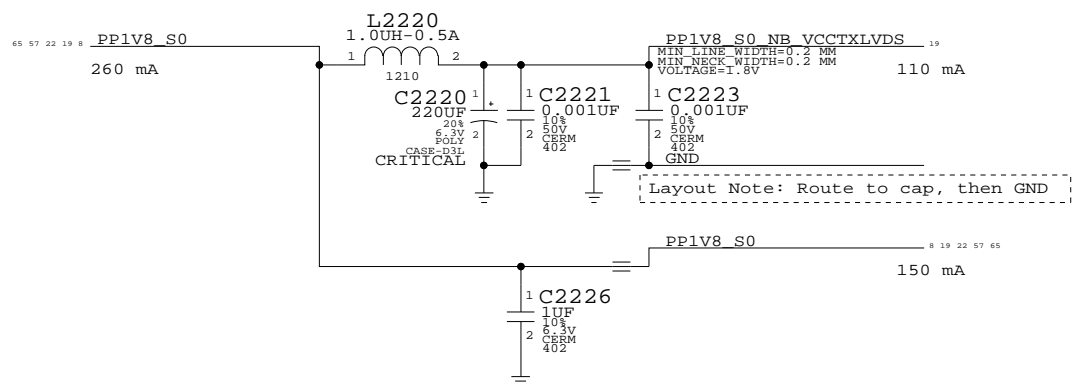
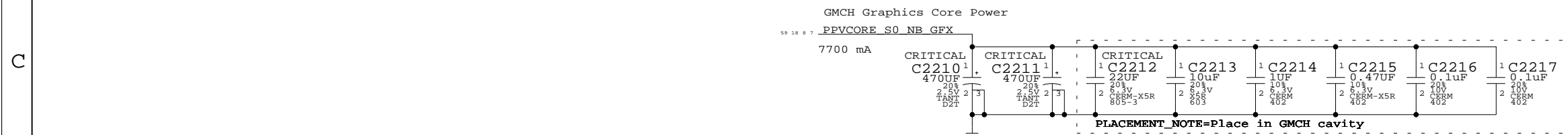
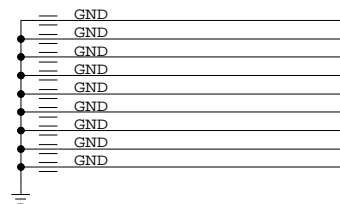
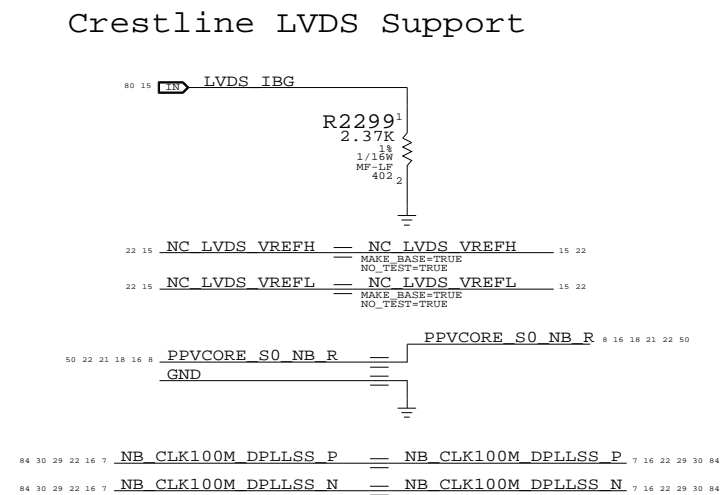
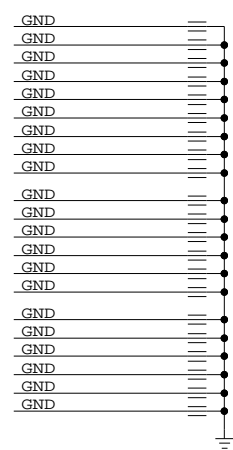
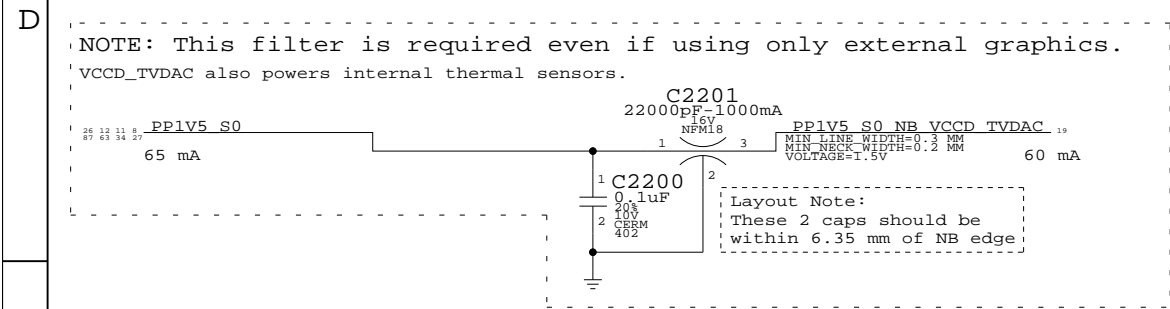
TDE_SENSE	VSS302	T29	GND
TDE_FORCE	VSS303	T31	GND
TDB_FORCE	VSS304	T33	GND
TDB_SENSE	VSS305	R28	GND

NB Grounds		
SYNC_MASTER=T9_NOME		SYNC_DATE=03/16/2007
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	D	051-7225	14.0.0
SCALE		SHT	20 OF 88
NONE			




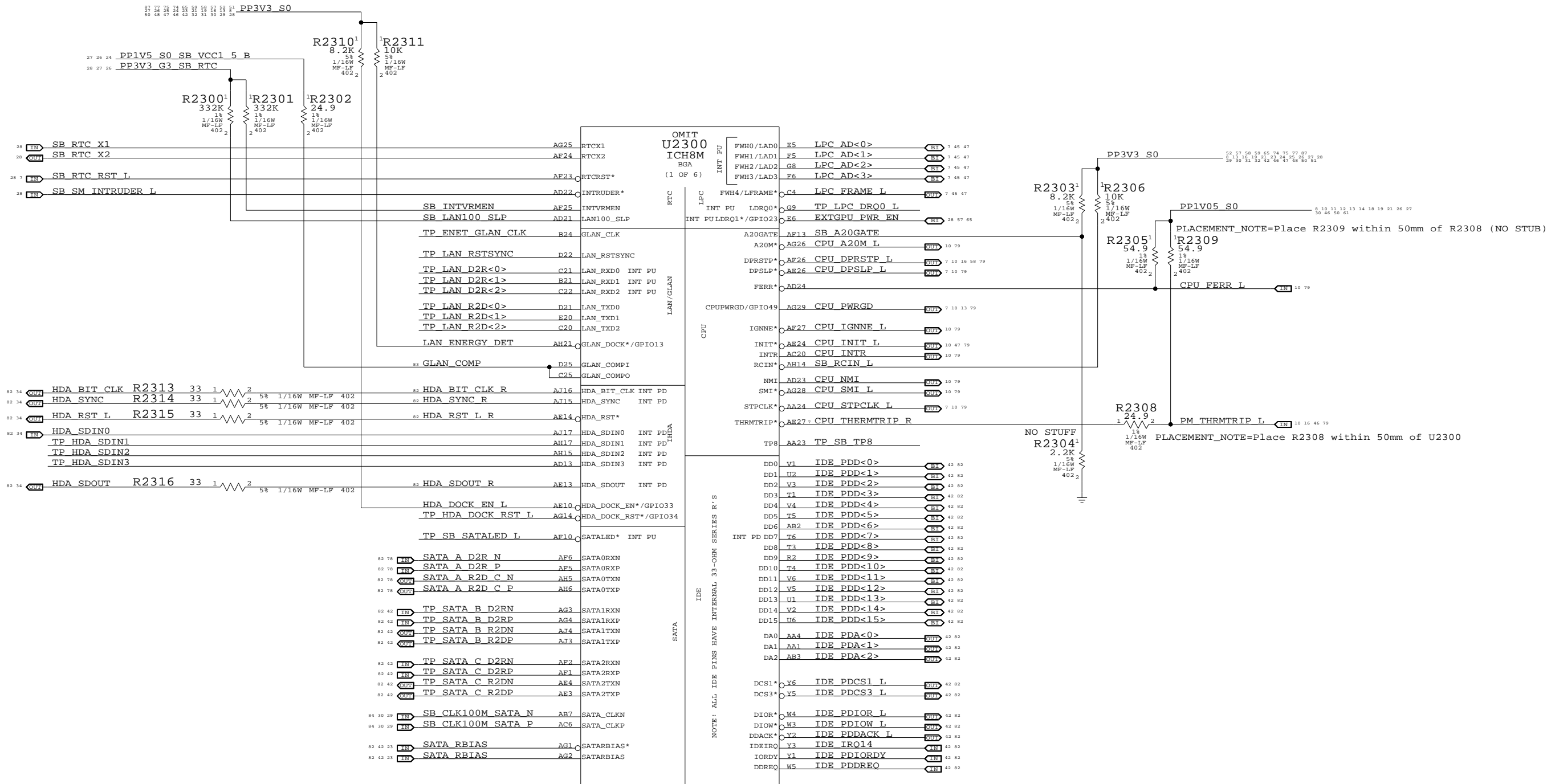
Current numbers from Crestline EDS, doc #21749.

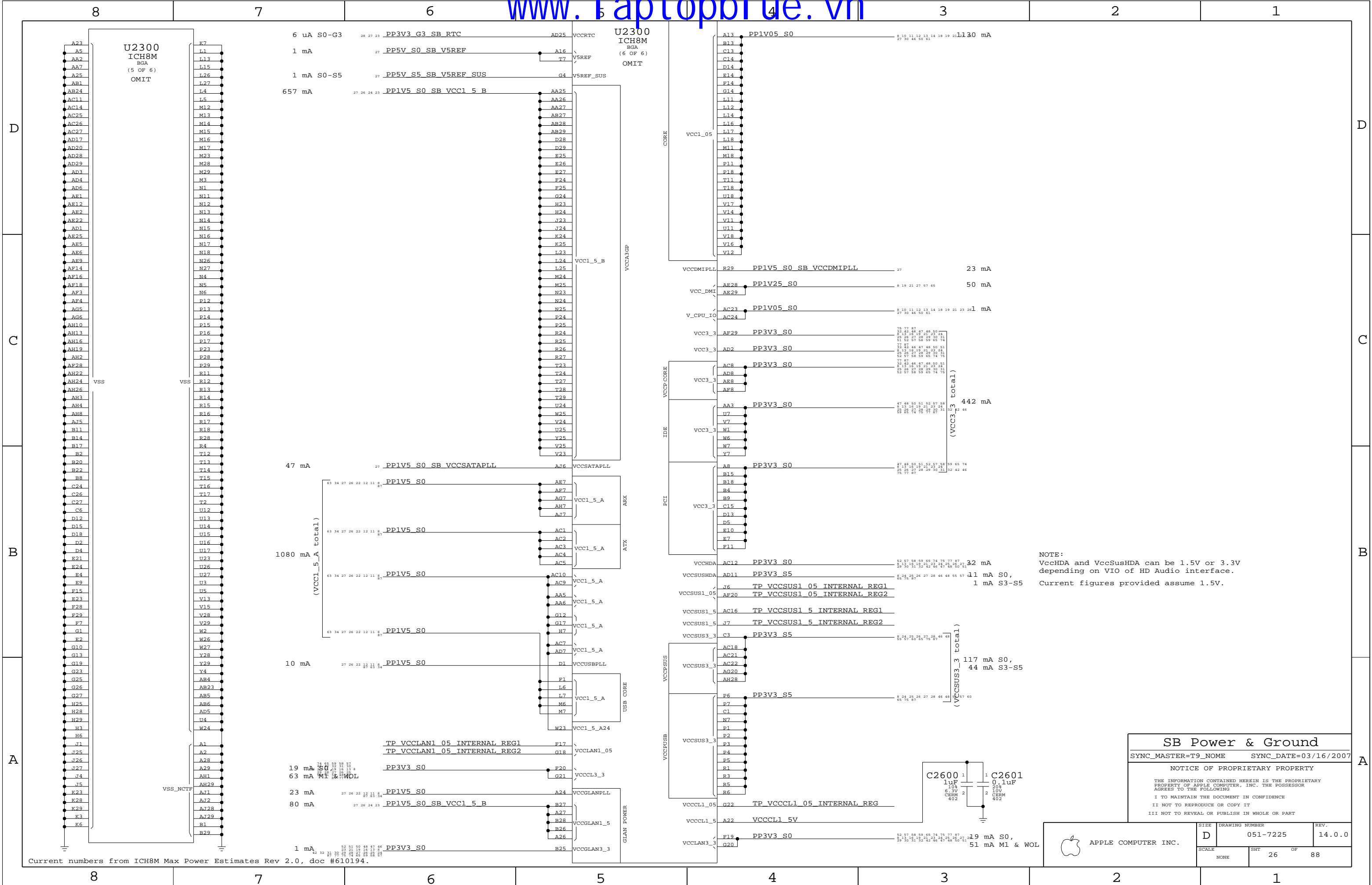


Current numbers from Crestline EDS Addendum, doc #20127.

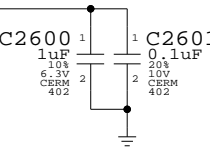
NB Graphics Decoupling	
SYNC_MASTER=M76_MLB	SYNC_DATE=03/12/2007
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 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER		REV.
	D	051-7225		14.0.0
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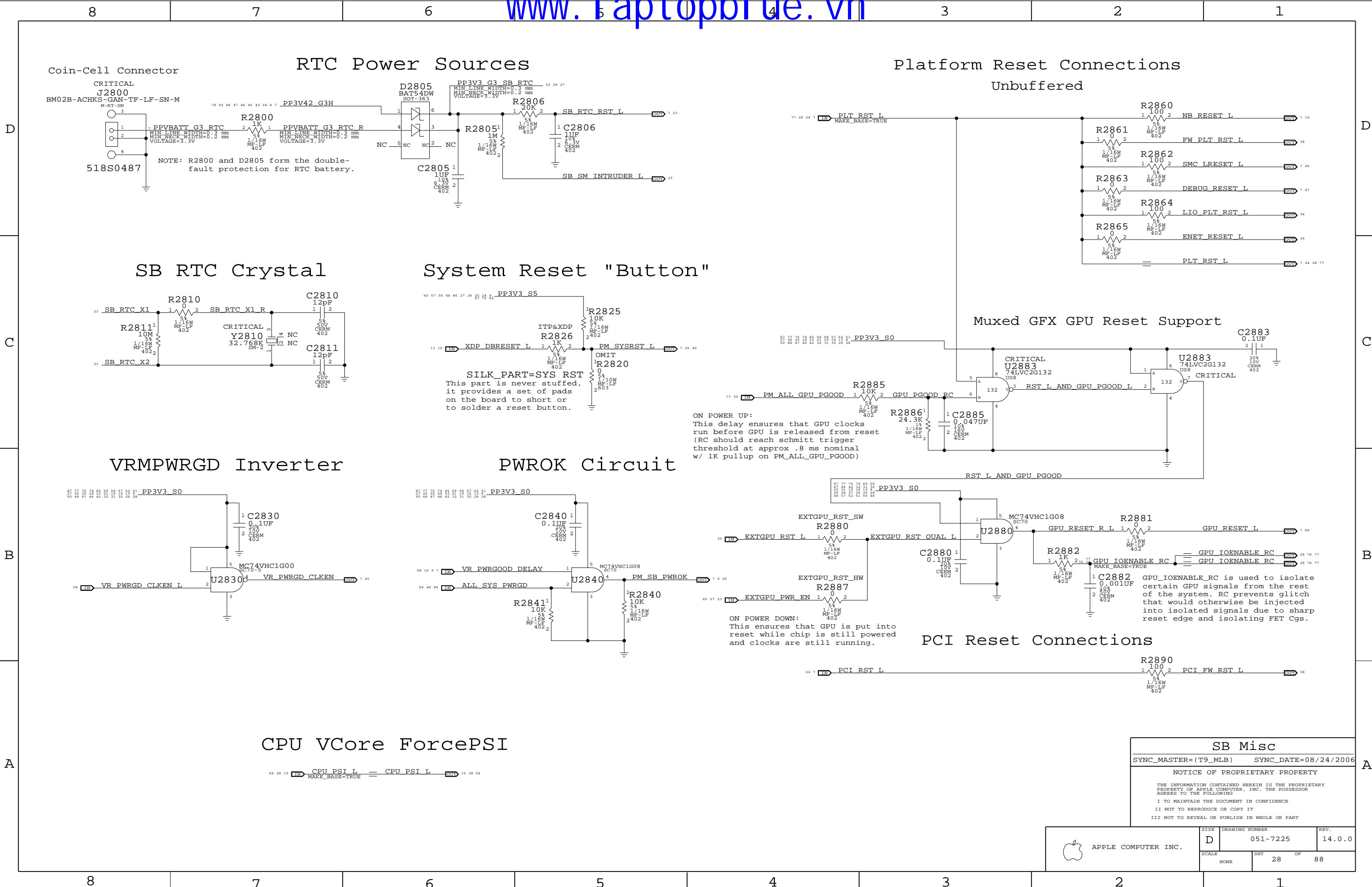


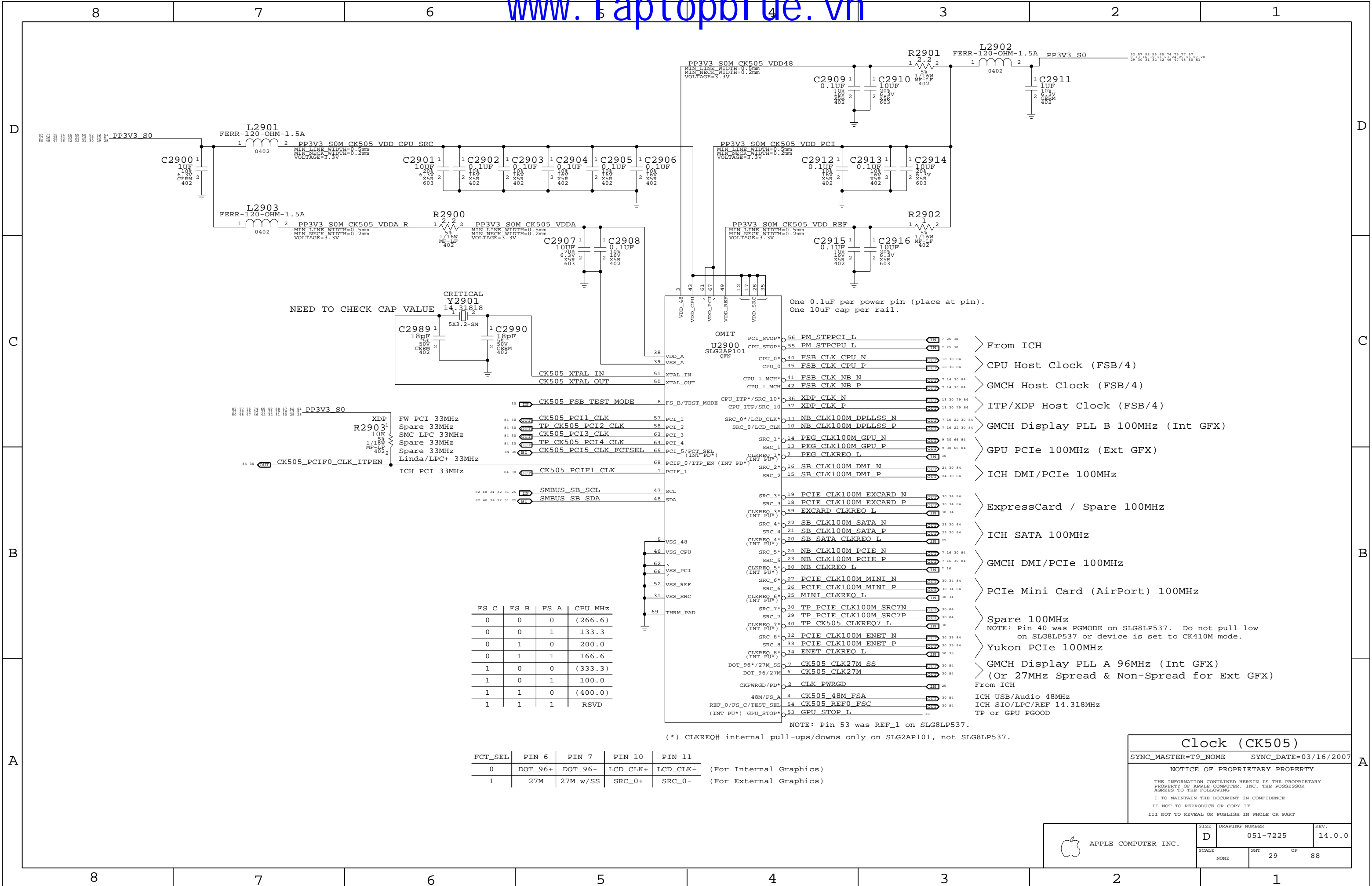
NOTE:
VccHDA and VccSusHDA can be 1.5V or 3.3V depending on VIO of HD Audio interface.
Current figures provided assume 1.5V.



SB Power & Ground		
SYNC_MASTER=T9_NOME		SYNC_DATE=03/16/2007
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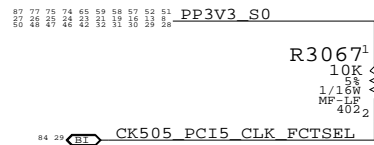
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7225	14.0.0
SCALE		SHT	OF
NONE		26	88



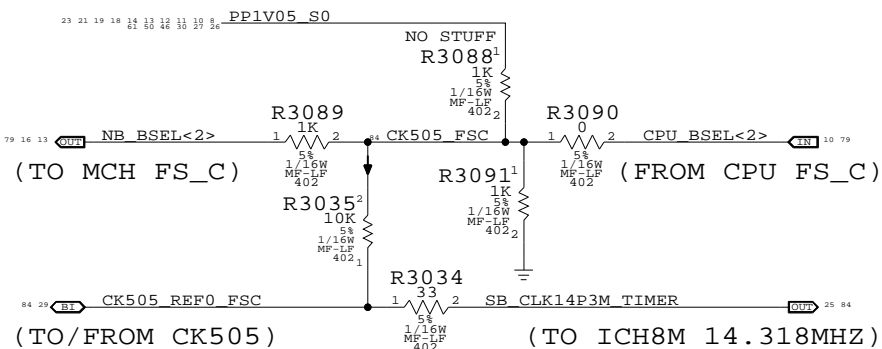
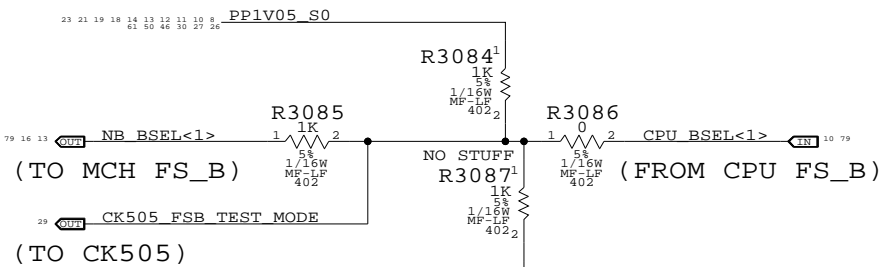
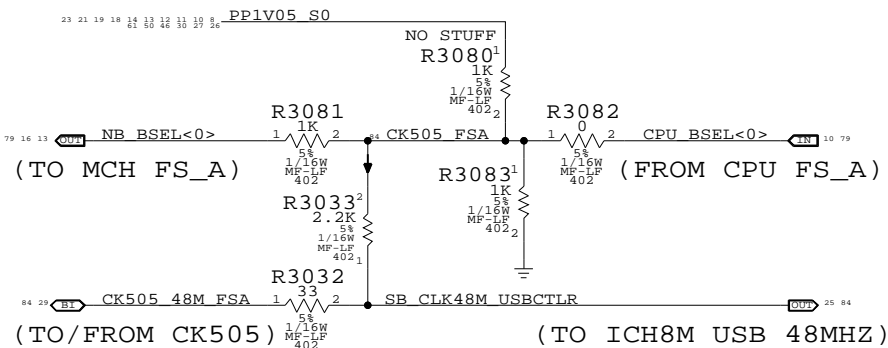


CK505 Configuration Straps

FCT_SEL (GFX clock select)



FS_A, FS_B, FS_C (Host clock freq select)



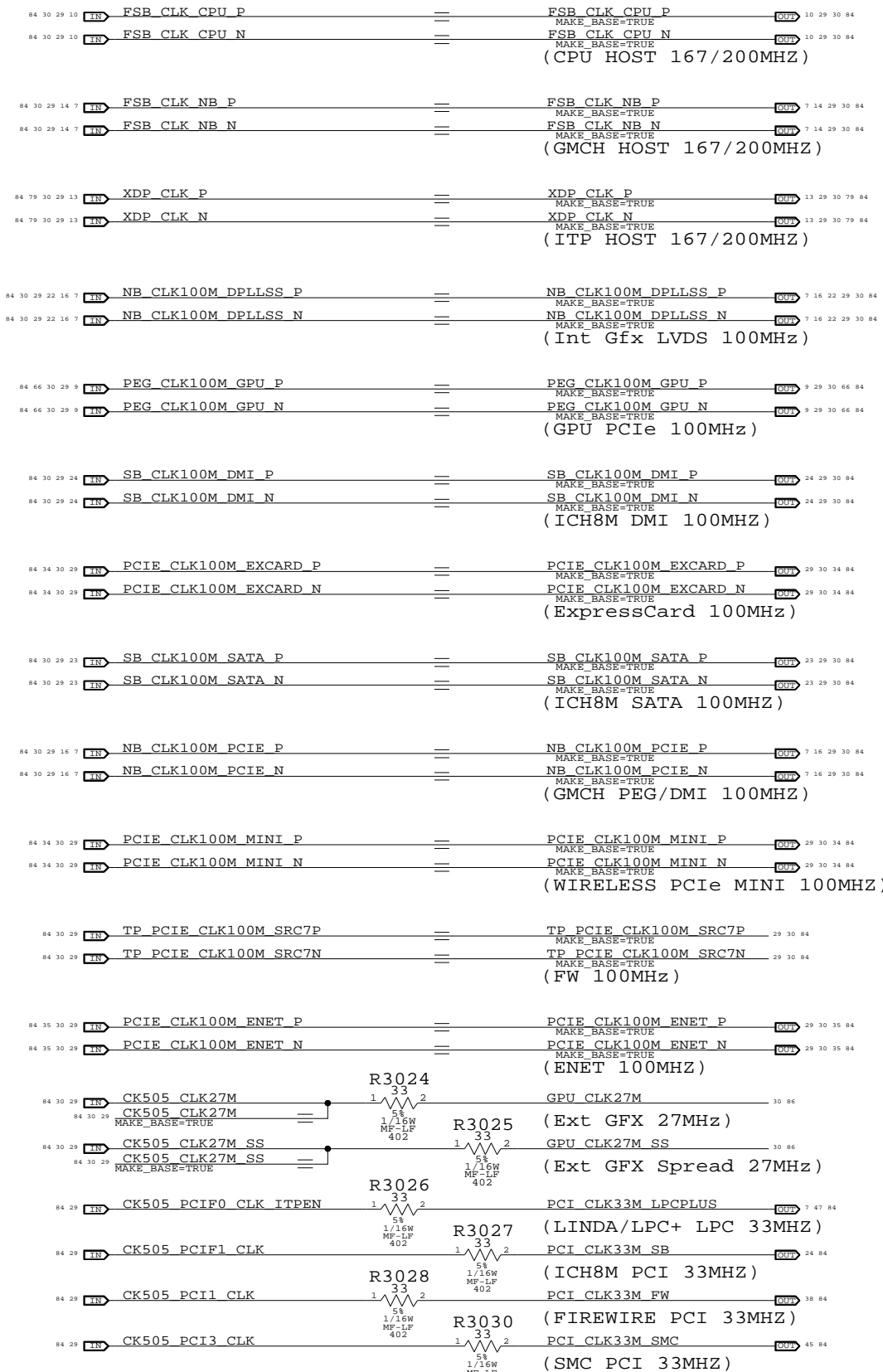
FS_C	FS_B	FS_A	CPU MHz
0	0	0	(266.6)
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	0	0	(333.3)
1	0	1	100.0
1	1	0	(400.0)
1	1	1	RSVD

NO STUFF R3082, R3086 & R3090 for manual CPU clk frequency.

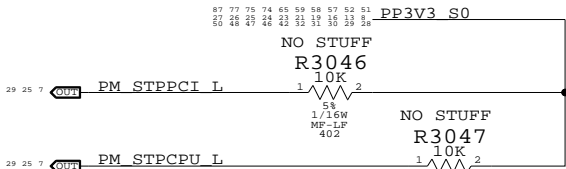
(Only 100-200MHz supported by SLG8LP536 and CY28545-5)

CLK Termination

(Note: HOST/SRC/GFX clock termination removed. Silego SL8LP536 or equiv. support only)

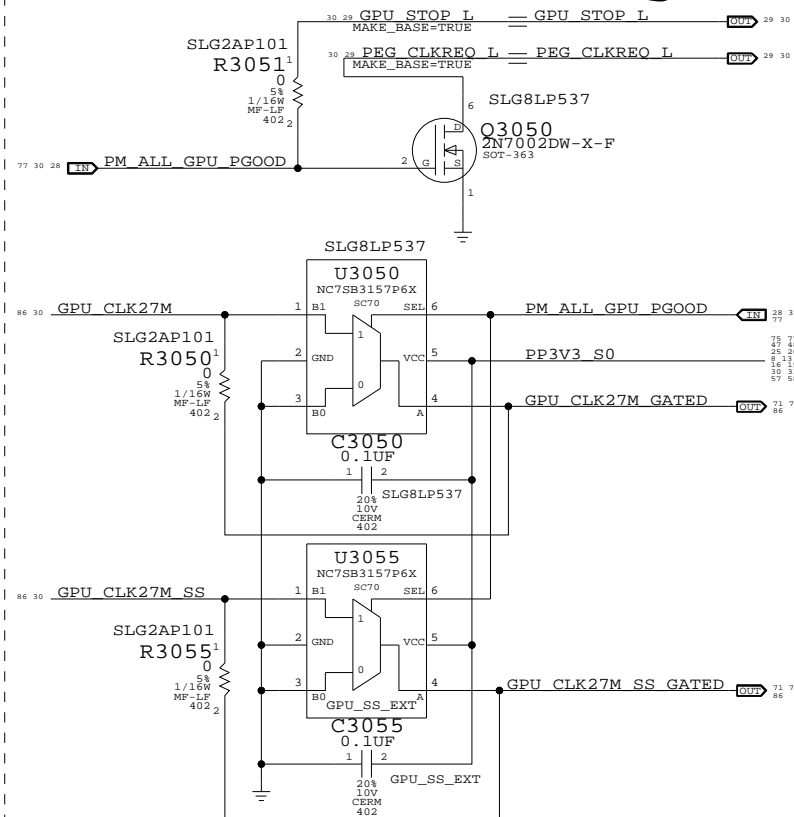


CLKREQ Controls

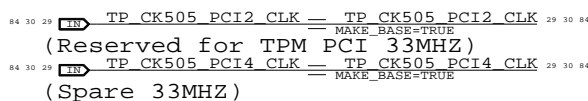


Silego SLG2AP101 has internal pull-ups on all CLKREQ# pins. Support for SL8LP537 or equiv. only. NB and SATA CLKREQs are not remappable (and thus are not shown here).

GPU Clock Gating



Unused Clocks



Clock Termination

SYNC_MASTER=(MASTER) SYNC_DATE=08/23/2006

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	14.0.0
SCALE	SHT	OF
NONE	30	88

Page Notes

Power aliases required by this page:

- =PP1V8_S3M_MEM_A
- =PP0V9_S3M_MEM_DIMMVREFA
- =PPSPD_S0M_MEM_A (2.5V - 3.3V)

Signal aliases required by this page:

- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:

(NONE)

"Factory" (thru-hole) slot

DDR2 Bypass Caps
(For return current)

DDR2 SO-DIMM Connector A

SYNC_MASTER=(M59_SYNC) SYNC_DATE=08/24/2006

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APPLE COMPUTER INC.

SIZE

DRAWING NUMBER

REV.

D

051-7225

14.0.0

SCALE

NONE

SHT

31

OF

88

Page Notes

Power aliases required by this page:

- =PP1V8_S3M_MEM_B
- =PP0V9_S3M_MEM_DIMMVREFB
- =PPSPD_S0M_MEM_B (2.5V - 3.3V)

Signal aliases required by this page:

- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:

(NONE)

"Expansion" (surface-mount) slot

DDR2 Bypass Caps
(For return current)

DDR2 SO-DIMM Connector B

SYNC_MASTER=(M59_SYNC) SYNC_DATE=08/24/2006

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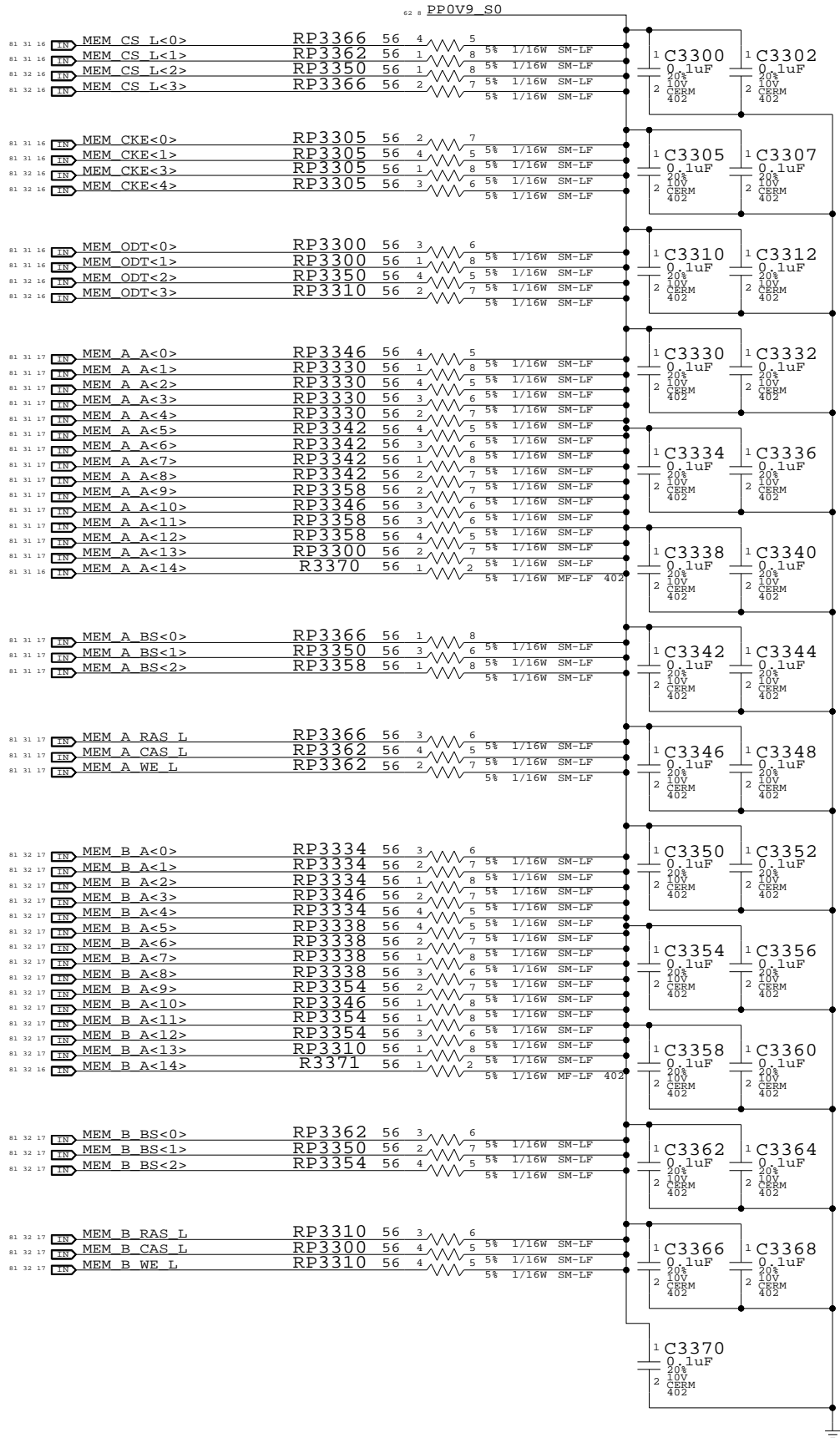
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SIZE	DRAWING NUMBER	REV.
D	051-7225	14.0.0
SCALE	SHT	OF
NONE	32	88

One cap for each side of every RPAK, one cap for every two discrete resistors
Ensure CS_L and ODT resistors are close to SO-DIMM connector



Memory Active Termination

SYNC_MASTER=(T9_NOME) SYNC_DATE=11/14/2006

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APPLE COMPUTER INC.

SIZE

D

SCALE

NONE

DRAWING NUMBER

051-7225

SHT

33

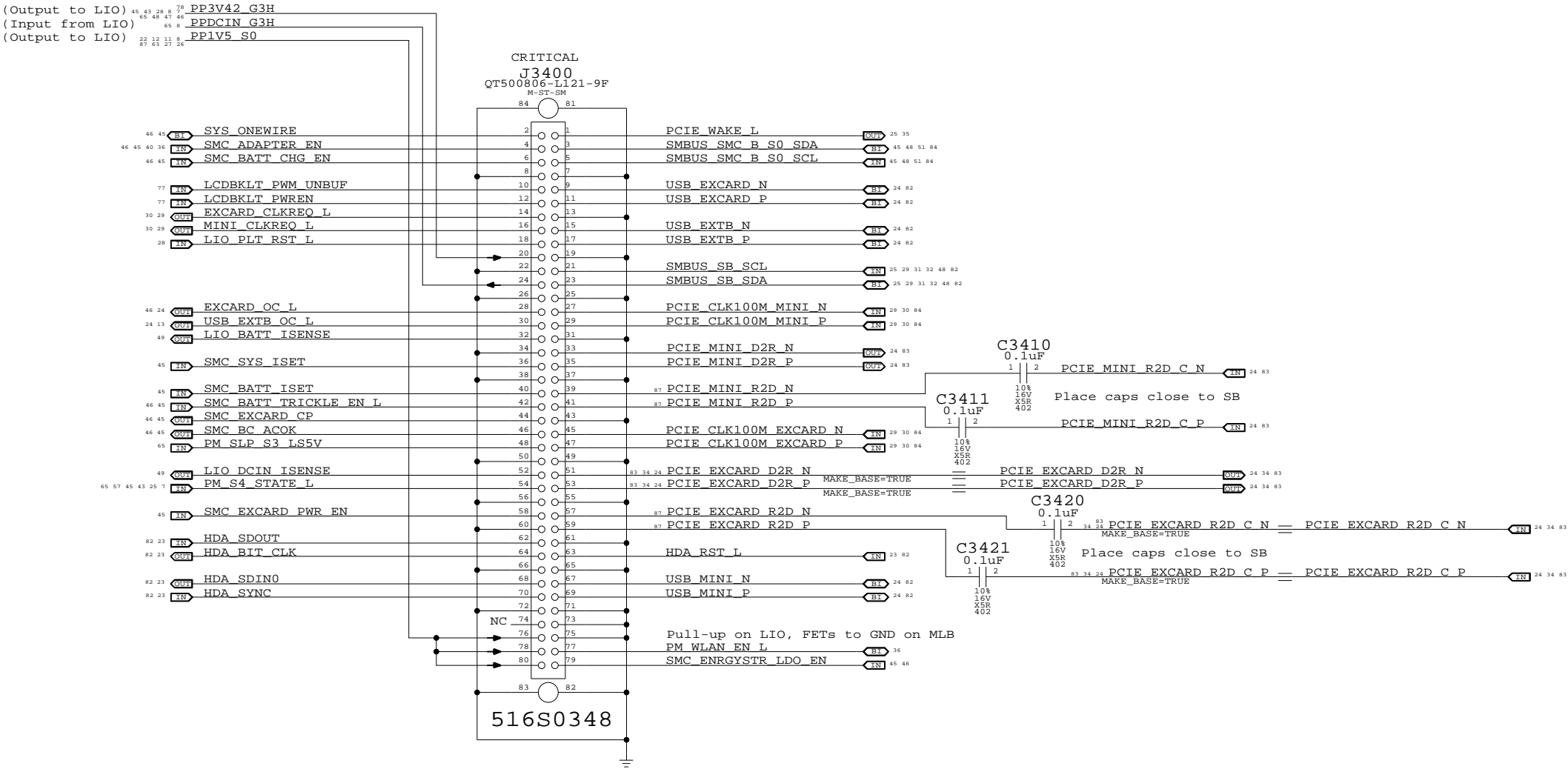
REV.

14.0.0

OF

88

Left I/O Board Connector



Left I/O Board Connector

SYNC_MASTER=(M59_SYNC) SYNC_DATE=08/24/2006

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SIZE	DRAWING NUMBER	REV.
D	051-7225	14.0.0
SCALE	SHT	OF
NONE	34	88

D

C

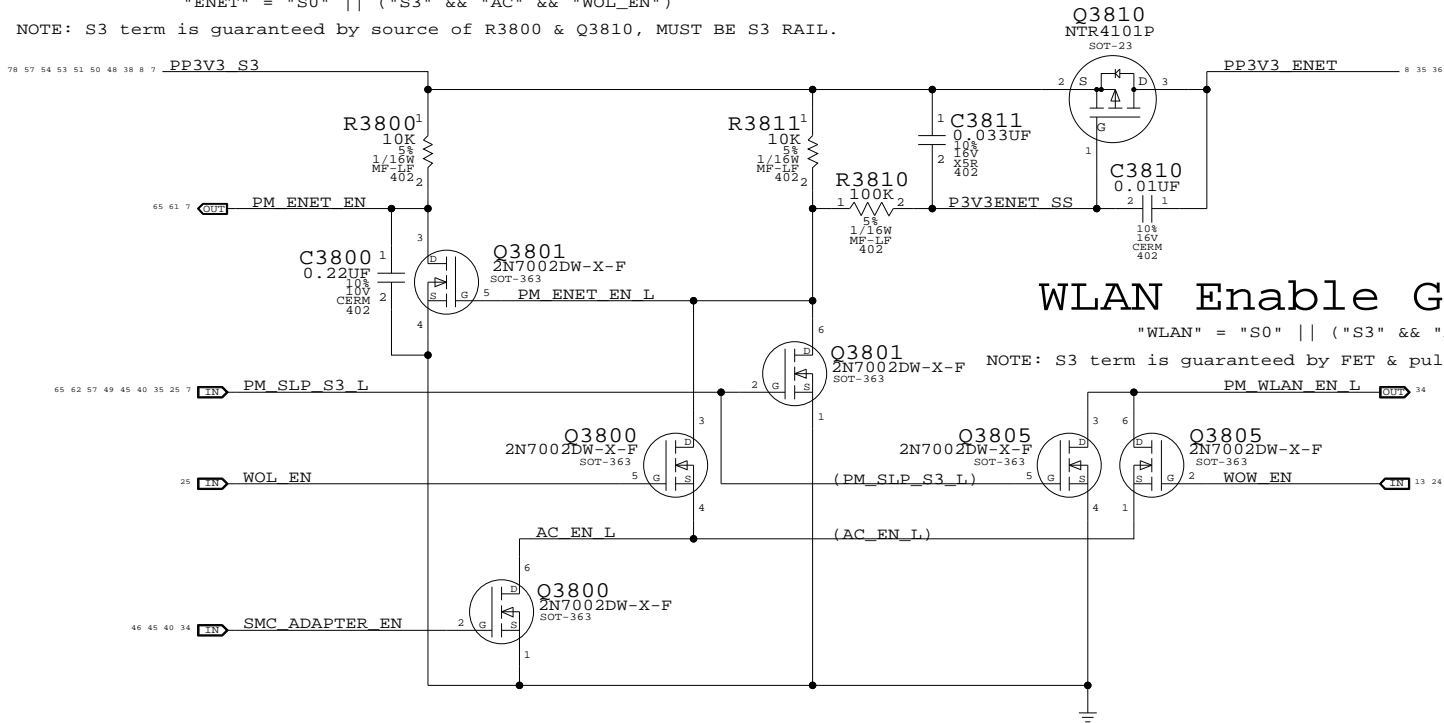
B

A

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0386	1	IC,88E8058,GIGABIT ENET XCVR,64P QFN	U3700	CRITICAL	YUKON_ULTRA
341S2060	1	IC,FLASH,88E8058 ETHERNET VPD,IIC,S08	U3780	CRITICAL	YUKON_ULTRA
338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN	U3700	CRITICAL	YUKON_EC
341S1797	1	IC,EEPROM,SERIAL IIC,8KBIT,S08	U3780	CRITICAL	YUKON_EC
114S0285	1	RES,4.87K,1%,1/16W,0402,LF	R3760		YUKON_EC

ENET Enable Generation

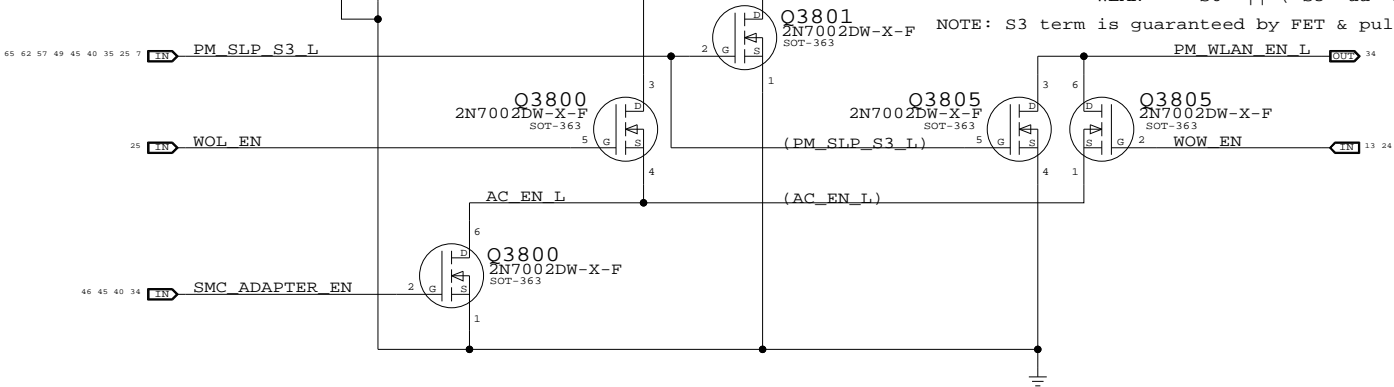
"ENET" = "S0" || ("S3" && "AC" && "WOL_EN")
NOTE: S3 term is guaranteed by source of R3800 & Q3810, MUST BE S3 RAIL.



3.3V ENET FET

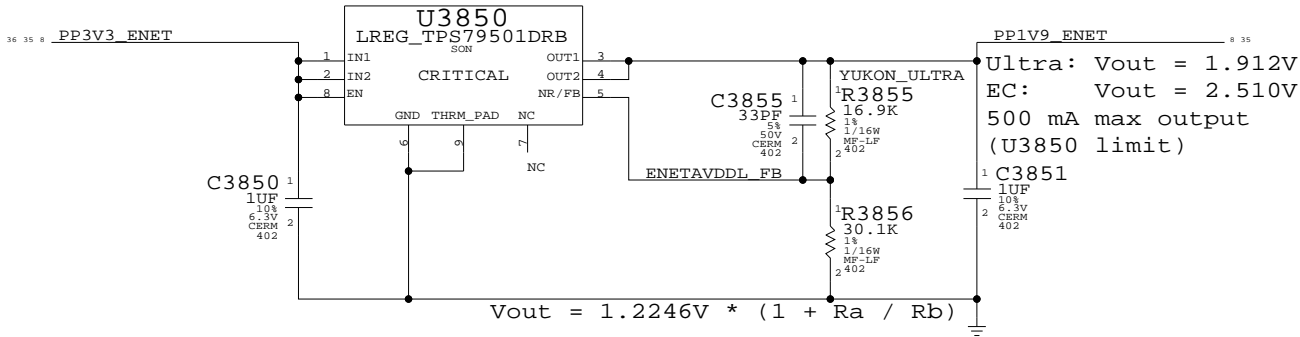
WLAN Enable Generation

"WLAN" = "S0" || ("S3" && "AC" && "WOW_EN")
NOTE: S3 term is guaranteed by FET & pull-up source, MUST BE S3 RAIL.



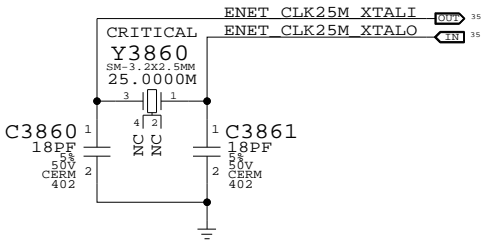
Yukon AVDDL LDO

1.9V for Yukon Ultra, 2.5V for Yukon EC
Yukon Ultra requires 1.9V on its magnetics to pass compliance tests



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0363	1	RES,31.6K,1%,1/16W,402,LF	R3855		YUKON_EC

Yukon Crystal



Yukon Power Control

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

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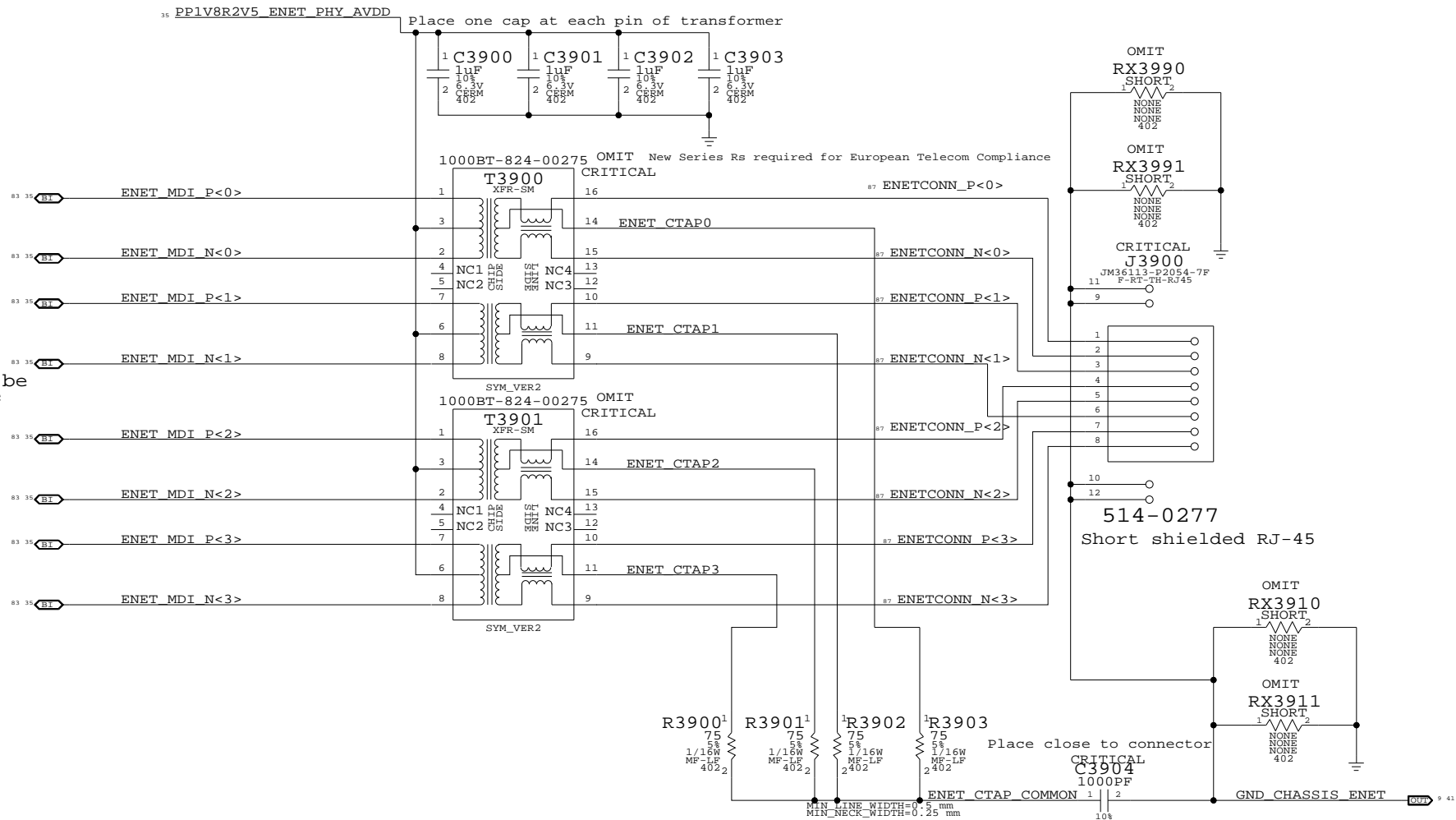
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SIZE	DRAWING NUMBER	REV.
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SCALE	SHT	OF
NONE	36	88

Transformers should be mirrored on opposite sides of the board

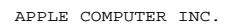


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
157S0030	2	XFMR, ISO, HALF-PORT, 1000T, 16P, SMD, 2MM	T3900, T3901	CRITICAL	

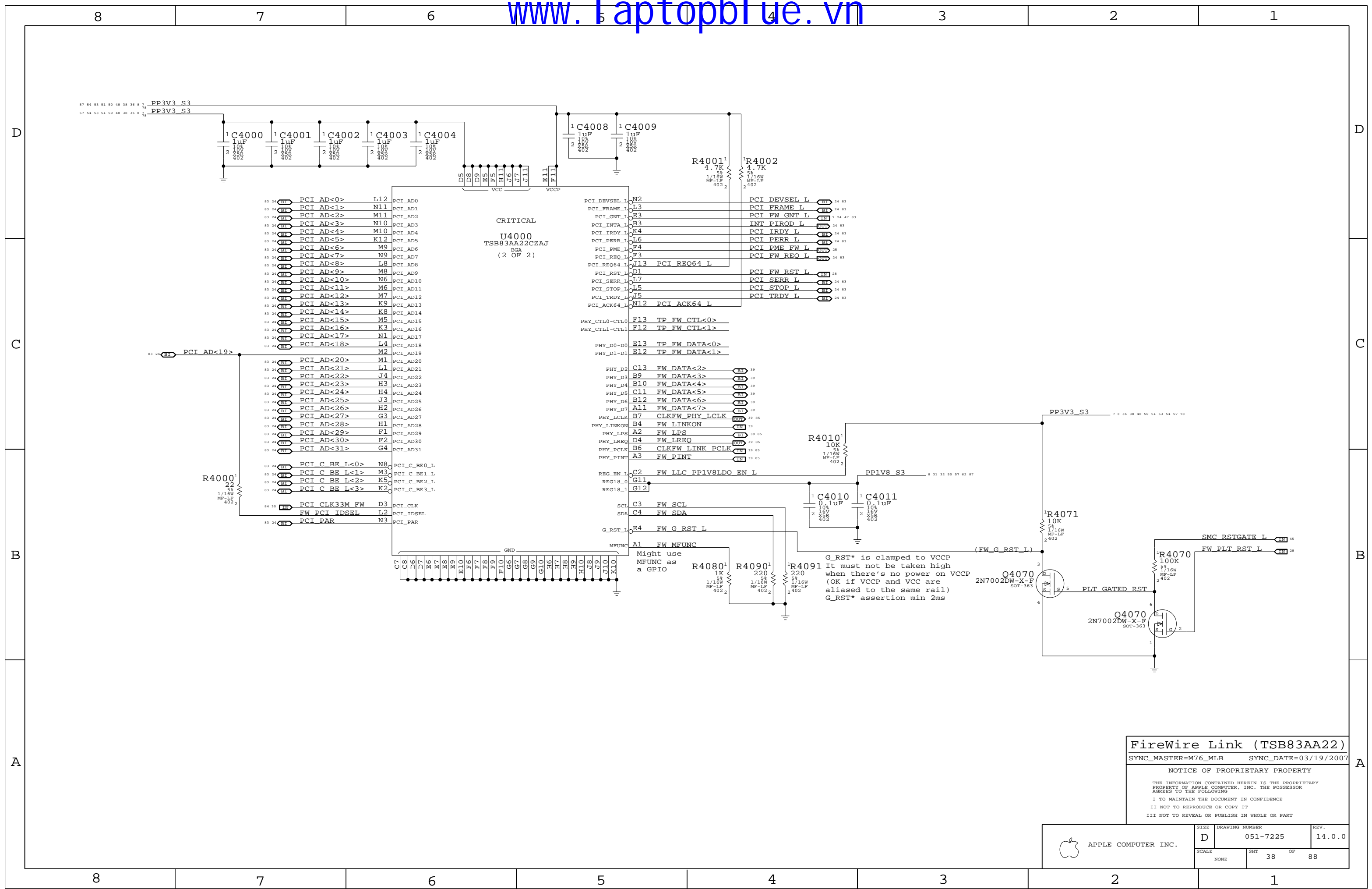
SYNC_MASTER=M76_MLB	SYNC_DATE=03/19/2007
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SIZE D	DRAWING NUMBER 051-7225	REV. 14.0.0
SCALE NONE	SHT 37	OF 88



FireWire Link (TSB83AA22)

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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SIZE	DRAWING NUMBER	REV.
D	051-7225	14.0.0
SCALE	SHT	OF
NONE	38	88

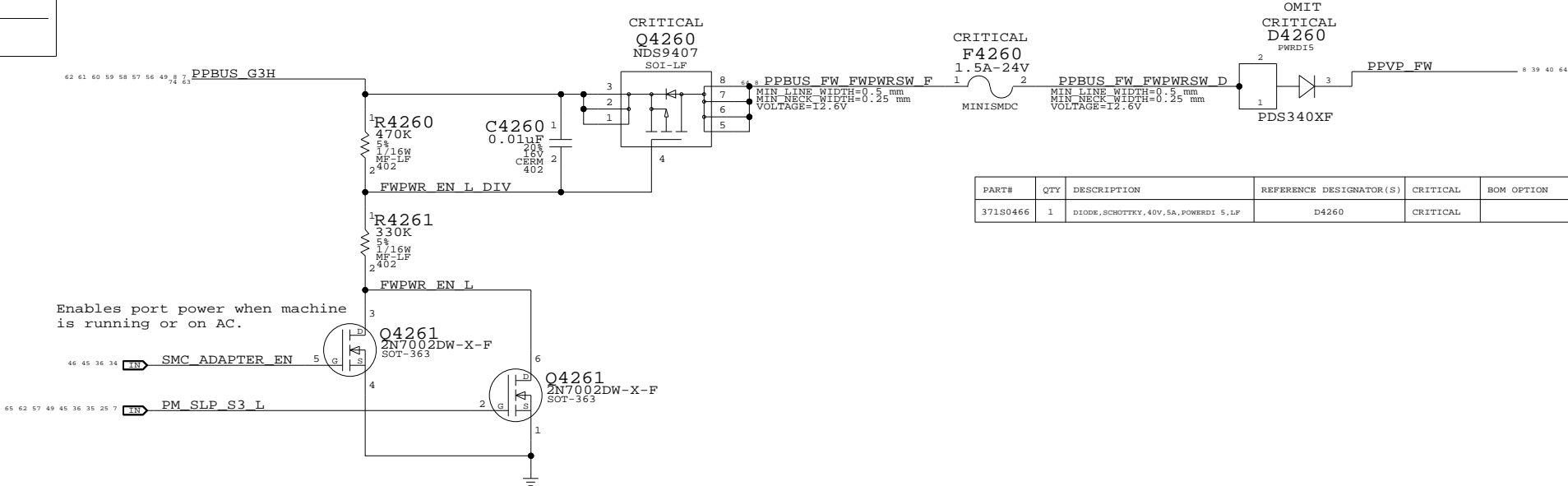


14.0.0

Page Notes

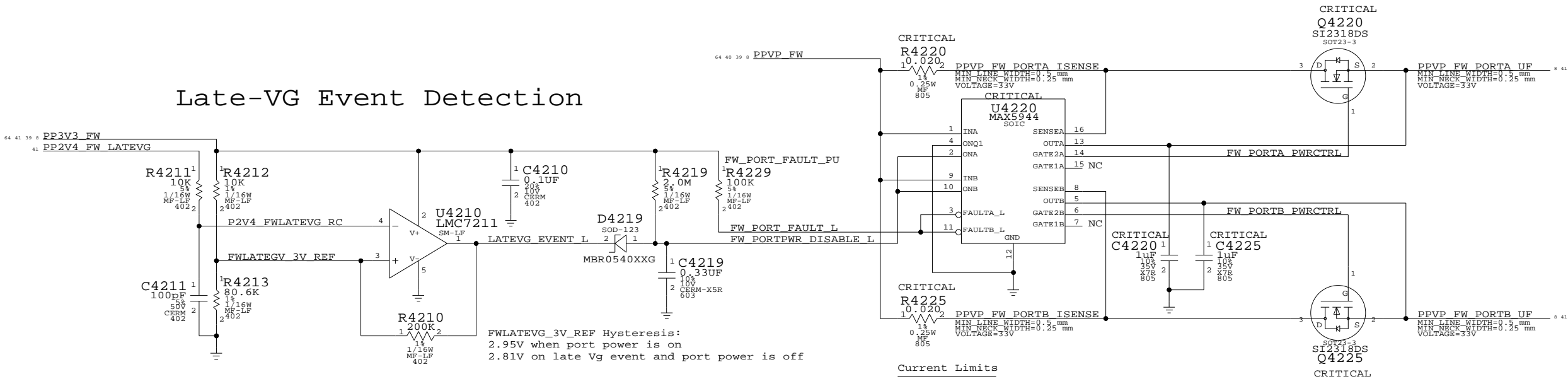
Power aliases required by this page:
- =PPBUS_S5_FWPWSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
- FW_PORT_FAULT_PU

FireWire Port Power Switch



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
371S0466	1	DIODE,SCHOTTKY,40V,5A,POWERDI 5,LF	D4260	CRITICAL	

Current Limit/Active Late-VG Protection



Current Limits
0.020 ohm => 2.4A
0.025 ohm => 2A
0.030 ohm => 1.66A (Ideal)
0.033 ohm => 1.5A

MAX5944 current limiter trips if integrator (counter) reaches 16. A new sample (taken every 125 us) is weighted as +1 if over the limit (at any point during the period) and -1/128 if under the limit. As a result, the device tends to trip easily on devices that produce periodic current spikes. Current limit has been set higher to compensate.

FireWire Port Power

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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SIZE	DRAWING NUMBER	REV.
D	051-7225	14.0.0
SCALE	SHT	OF
NONE	40	88

D

C

B

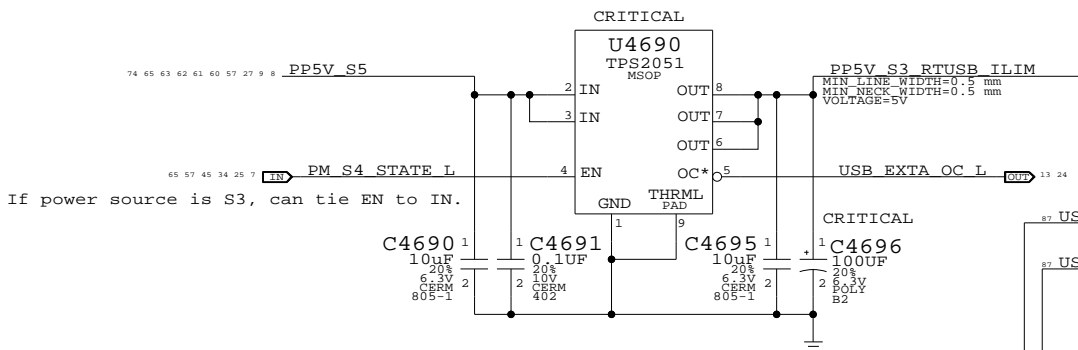
A

D

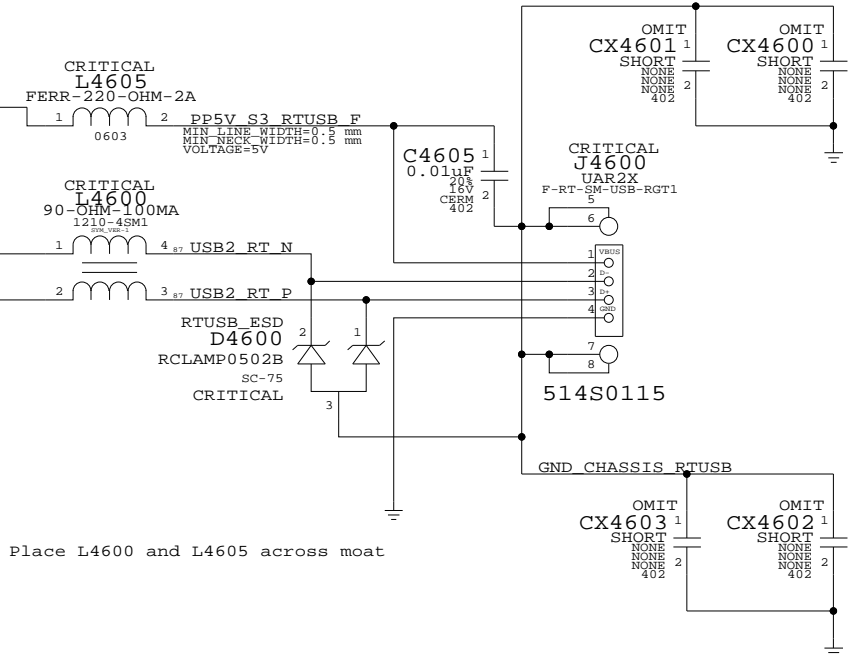
C|

8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---

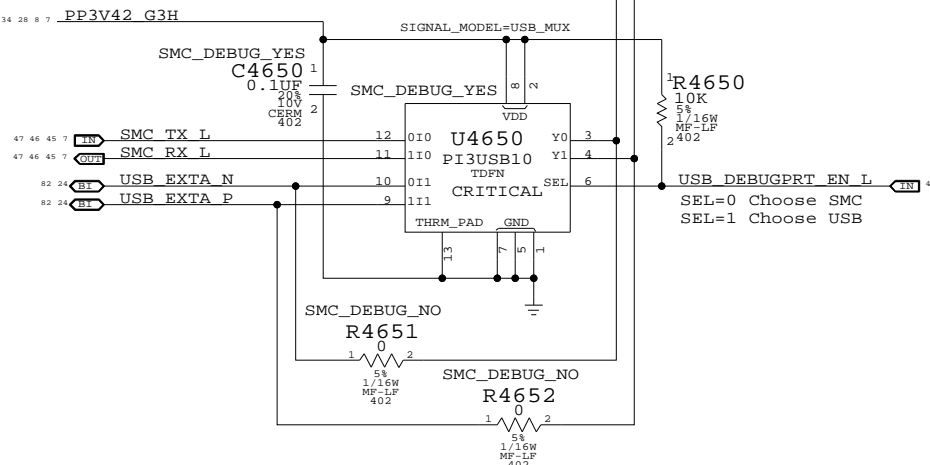
Port Power Switch



Right USB Port



USB/SMC Debug Mux



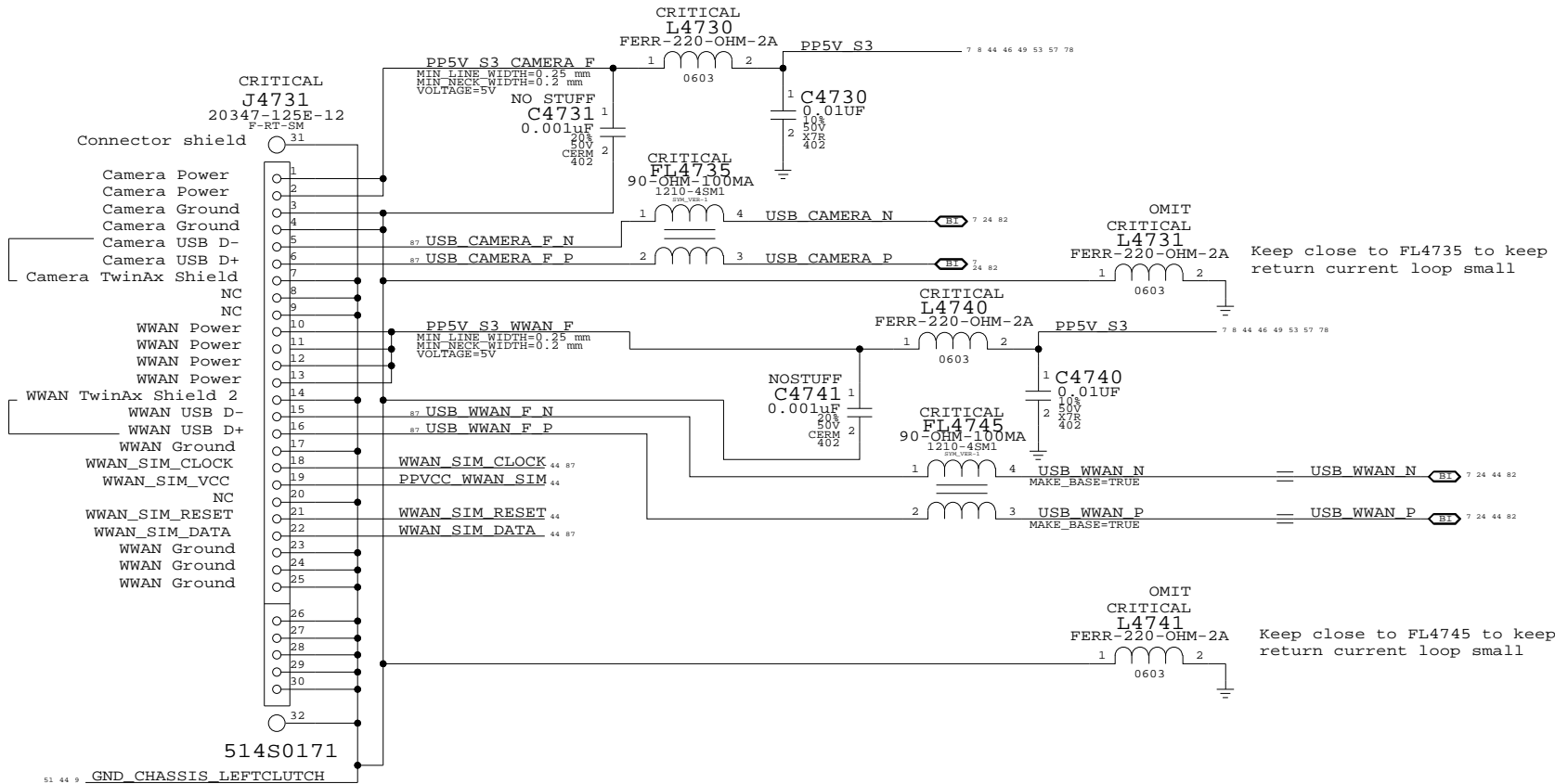
External USB Connector

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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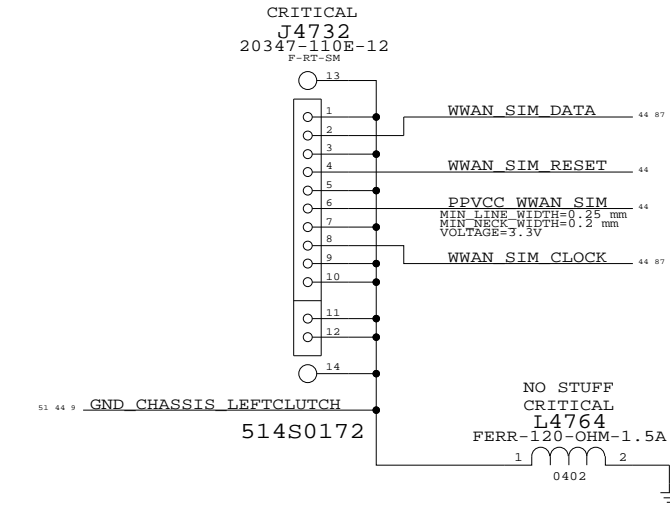
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7225	REV. 14.0.0
	SCALE NONE	SHT 43	OF 88

Left Clutch Barrel Interconnect



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
113S0022	2	RES,MF,1/10W,00HM,5,0603,SM,LF	L4731,L4741	CRITICAL	

SIM Interconnect

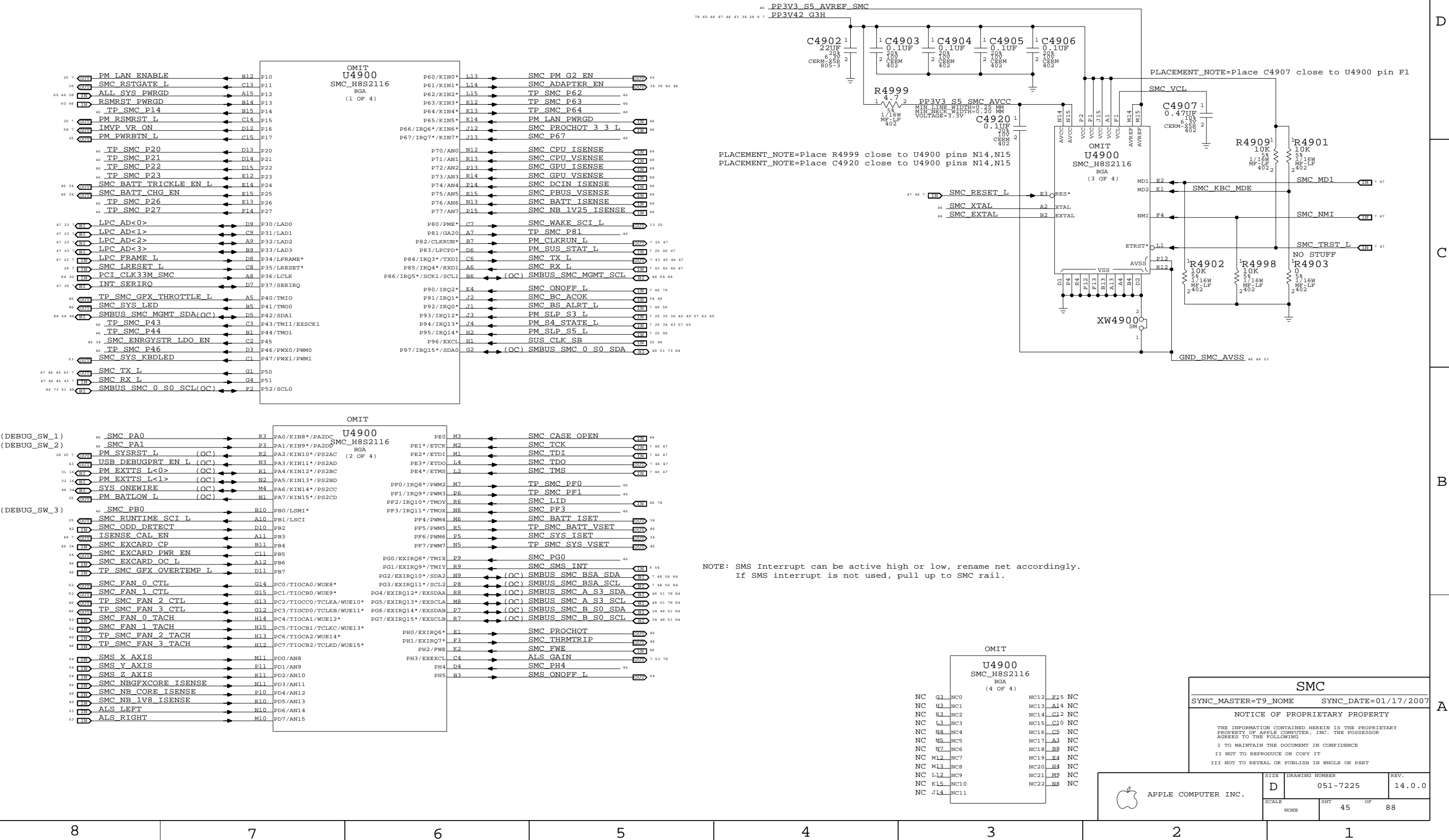


Left Clutch Barrel Interconnect
SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

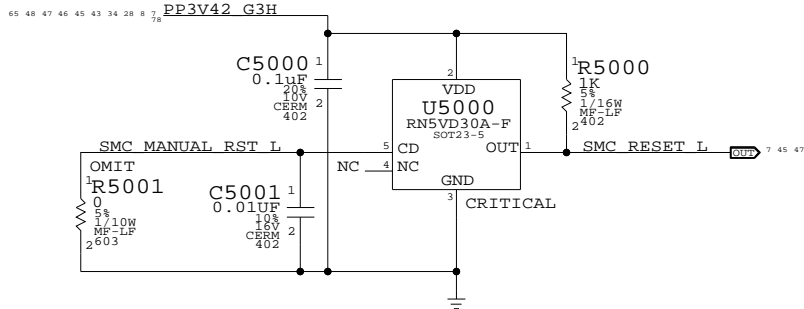
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	SCALE NONE	SHT 44	OF 88

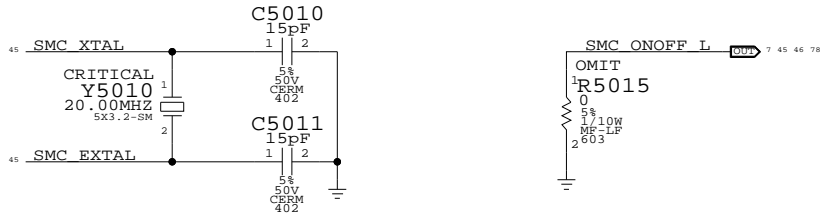
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



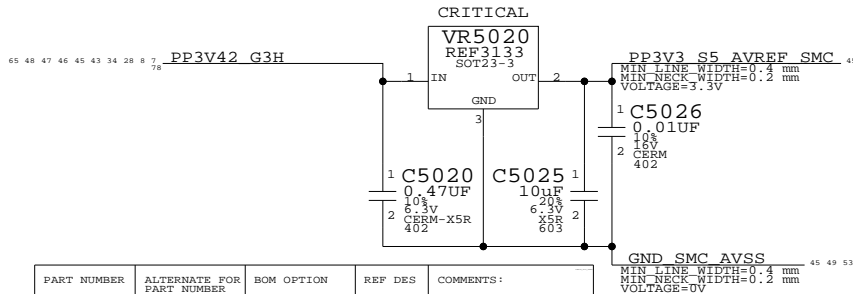
SMC Reset "Button" / Brownout Detect



SMC Crystal Circuit Debug Power "Button"

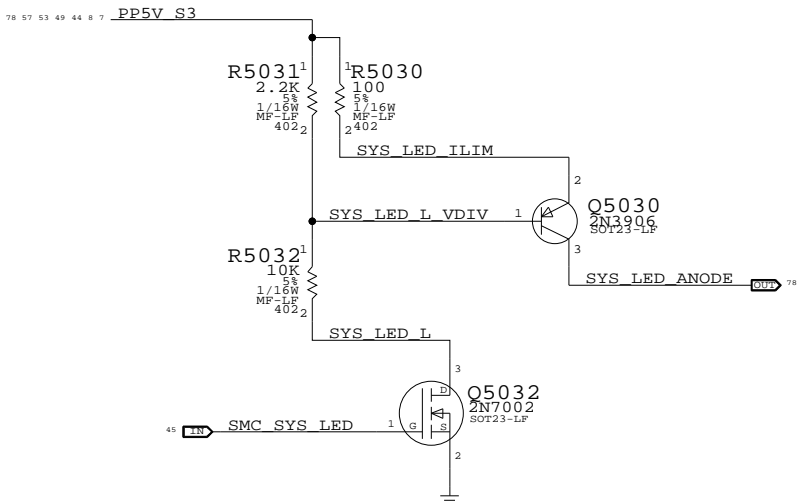


SMC AVREF Supply

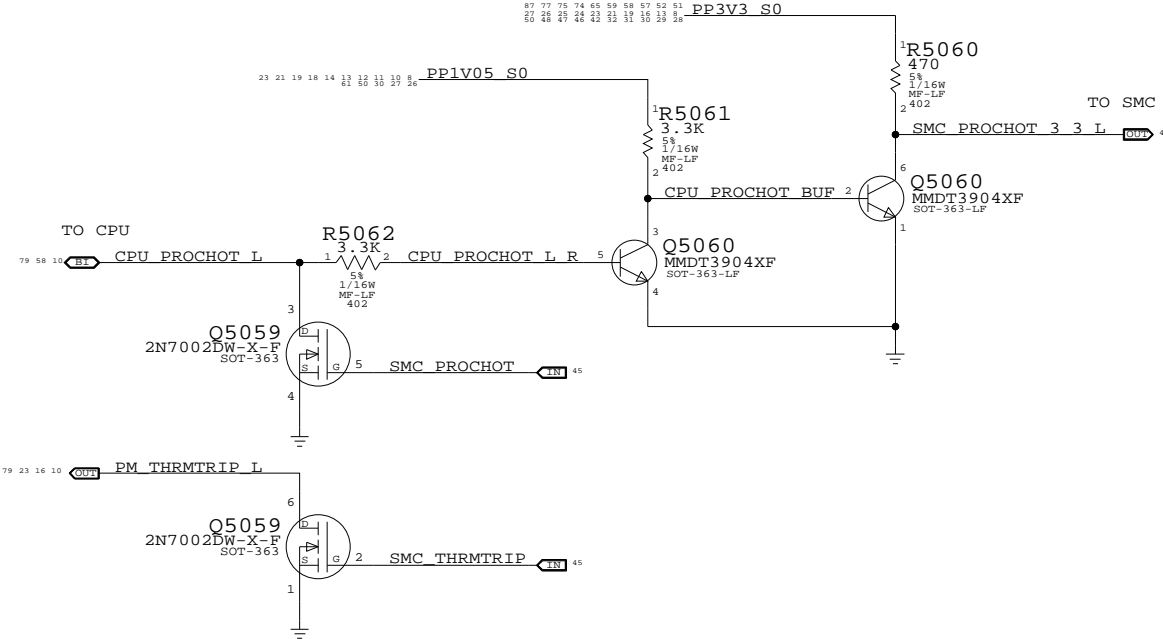


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
35381381	35381278		ALL	Interail ISL60002-33

System (Sleep) LED Circuit



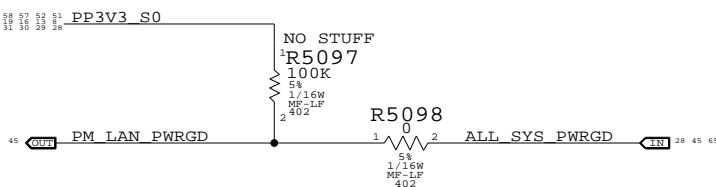
SMC FSB to 3.3V Level Shifting



TP SMC FAN 2 CTL	=	TP SMC FAN 2 CTL	45 46
TP SMC FAN 2 TACH	=	TP SMC FAN 2 TACH	45 46
TP SMC FAN 3 CTL	=	TP SMC FAN 3 CTL	45 46
TP SMC FAN 3 TACH	=	TP SMC FAN 3 TACH	45 46
TP SMC GFX OVERTEMP L	=	TP SMC GFX OVERTEMP L	45 46
TP SMC GFX THROTTLE L	=	TP SMC GFX THROTTLE L	45 46
TP SMC BATT VSET	=	TP SMC BATT VSET	45 46
TP SMC SYS VSET	=	TP SMC SYS VSET	45 46
TP SMC P14	=	TP SMC P14	45 46
TP SMC P20	=	TP SMC P20	45 46
TP SMC P21	=	TP SMC P21	45 46
TP SMC P22	=	TP SMC P22	45 46
TP SMC P23	=	TP SMC P23	45 46
TP SMC P26	=	TP SMC P26	45 46
TP SMC P27	=	TP SMC P27	45 46
TP SMC P43	=	TP SMC P43	45 46
TP SMC P44	=	TP SMC P44	45 46
TP SMC P46	=	TP SMC P46	45 46
TP SMC P62	=	TP SMC P62	45 46
TP SMC P63	=	TP SMC P63	45 46
TP SMC P64	=	TP SMC P64	45 46
TP SMC P81	=	TP SMC P81	45 46
TP SMC PF0	=	TP SMC PF0	45 46
TP SMC PF1	=	TP SMC PF1	45 46

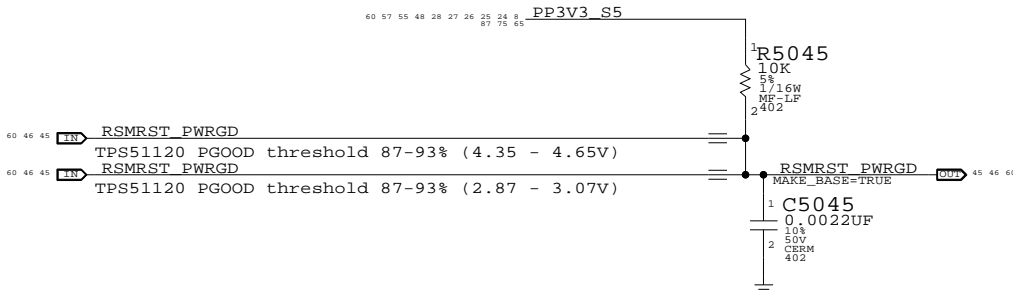
SMC EXCARD_OC_L	=	EXCARD_OC_L	24 34
SUS_CLK_SB	=	SUS_CLK_SB	25 45 46
SMC_ENRGYSTRLDO_EN	=	SMC_ENRGYSTRLDO_EN	34 45 46

LAN PWRGD Circuit



S5 Rail PWRGD Circuit

Reports when 5V S5 and 3.3V S5 are in regulation



SMC_PA0	R5091	100K	1	2	5% 1/16W MF-LF 402
SMC_PA1	R5092	100K	1	2	5% 1/16W MF-LF 402
SMC_PB0	R5093	100K	1	2	5% 1/16W MF-LF 402
SMC_ONOFF_L	R5070	10K	1	2	5% 1/16W MF-LF 402
SMC_LID	R5071	100K	1	2	5% 1/16W MF-LF 402
SMC_FWE	R5072	10K	1	2	5% 1/16W MF-LF 402
SMC_TX_L	R5073	10K	1	2	5% 1/16W MF-LF 402
SMC_RX_L	R5074	100K	1	2	5% 1/16W MF-LF 402
SYS_ONEWIRE	R5075	2.0K	1	2	5% 1/16W MF-LF 402
SMC_BS_ALRT_L	R5076	100K	1	2	5% 1/16W MF-LF 402
SMC_TMS	R5077	10K	1	2	5% 1/16W MF-LF 402
SMC_TDO	R5078	10K	1	2	5% 1/16W MF-LF 402
SMC_TDI	R5079	10K	1	2	5% 1/16W MF-LF 402
SMC_TCK	R5080	10K	1	2	5% 1/16W MF-LF 402
SMC_P67	R5094	10K	1	2	5% 1/16W MF-LF 402
SMC_PF3	R5081	10K	1	2	5% 1/16W MF-LF 402
SMC_PG0	R5096	10K	1	2	5% 1/16W MF-LF 402
SMC_PH4	R5082	10K	1	2	5% 1/16W MF-LF 402
SMC_BATT_TRICKLE_EN_L	R5083	10K	1	2	5% 1/16W MF-LF 402
SMC_BATT_CHG_EN	R5084	10K	1	2	5% 1/16W MF-LF 402
SMC_ADAPTER_EN	R5085	10K	1	2	5% 1/16W MF-LF 402
SMC_CASE_OPEN	R5086	10K	1	2	5% 1/16W MF-LF 402
SMC_BC_ACOK	R5087	470K	1	2	5% 1/16W MF-LF 402
SMC_EXCARD_CP	R5088	10K	1	2	5% 1/16W MF-LF 402
PM_SUS_STAT_L	R5089	100K	1	2	5% 1/16W MF-LF 402
PM_SLP_S5_L	R5090	100K	1	2	5% 1/16W MF-LF 402

SMC Support

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

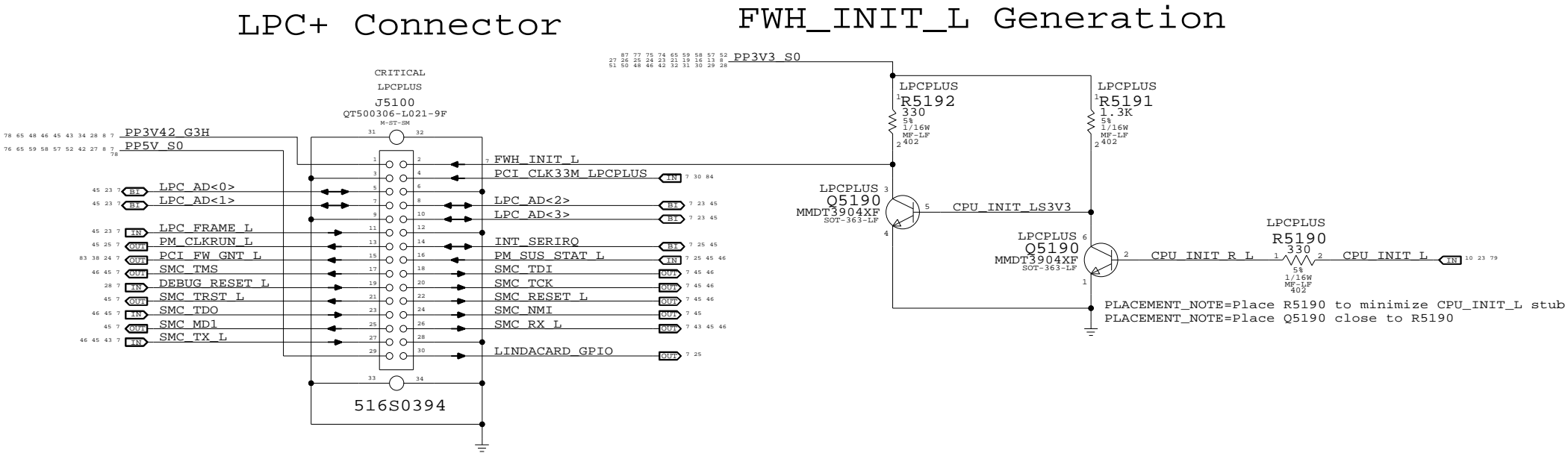
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SCALE	SHT	OF
NONE	46	88



LPC+ Debug Connector

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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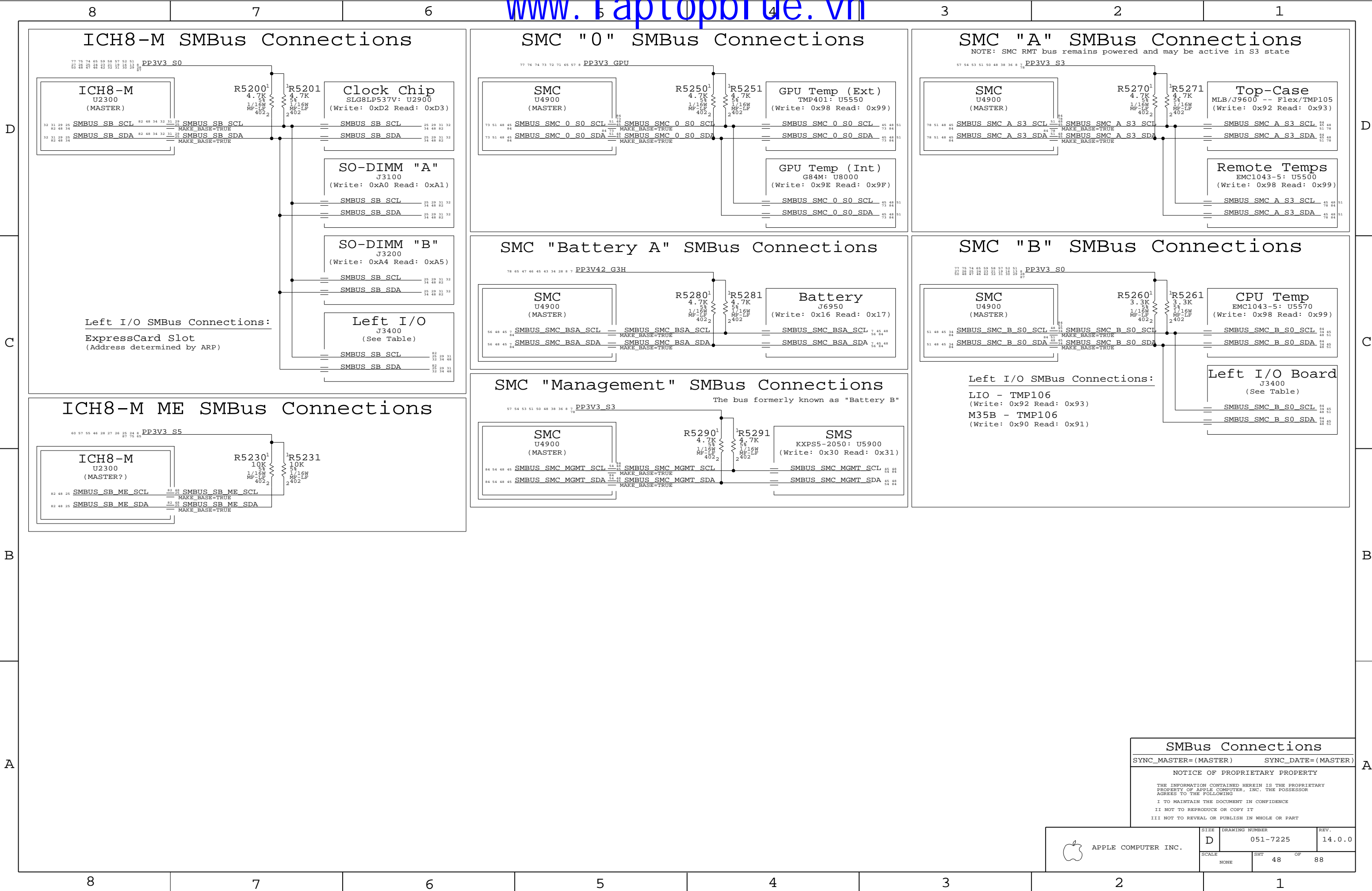
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	SCALE NONE	SHT 47	OF 88



SMBus Connections

SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)

NOTICE OF PROPRIETARY PROPERTY

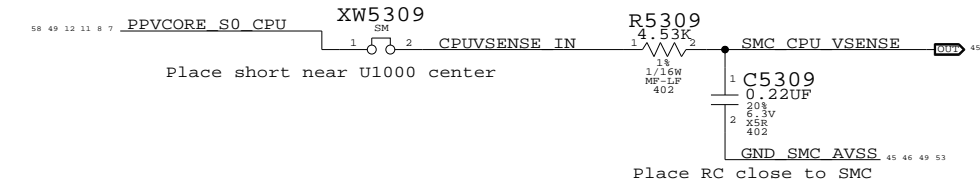
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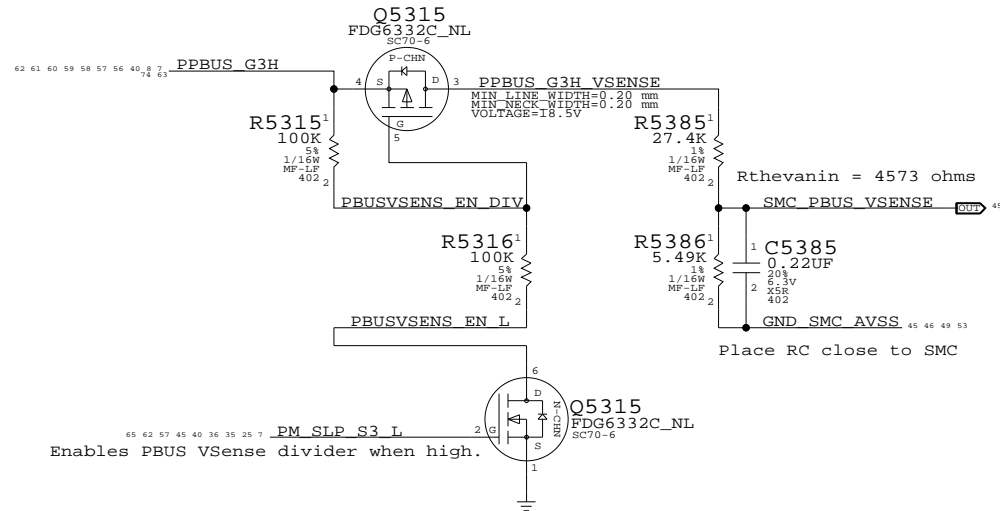
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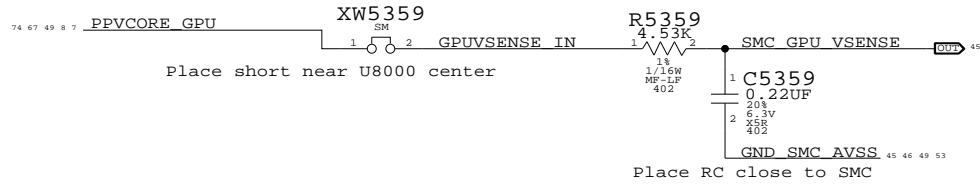
CPU Voltage Sense / Filter



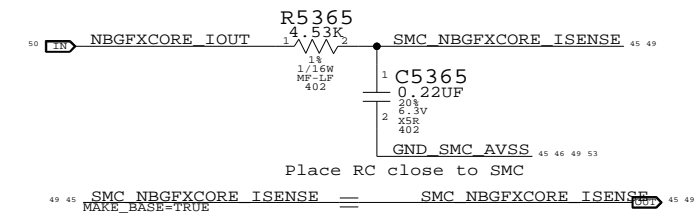
PBUS Voltage Sense & Filter



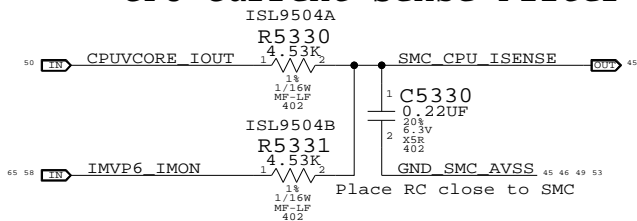
GPU Voltage Sense / Filter



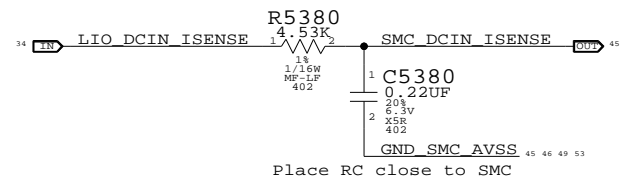
NB GFX Current Sense Filter



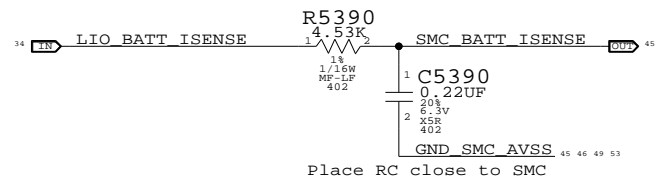
CPU Current Sense Filter



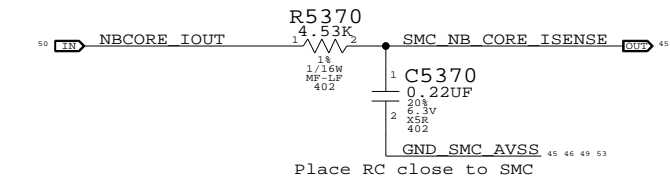
DCIN Current Sense Filter



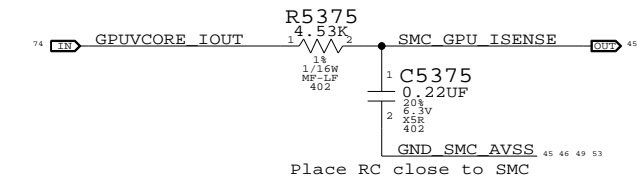
Battery (PBUS) Current Sense Filter



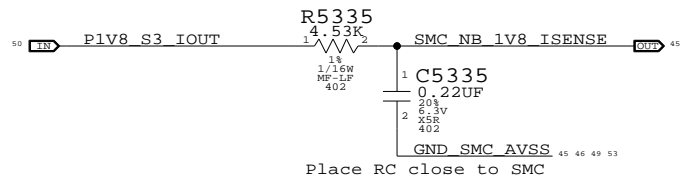
NB Core Current Sense Filter



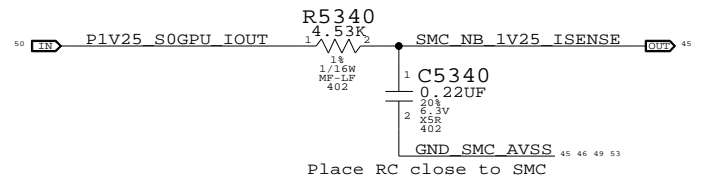
GPU Current Sense Filter



NB 1.8V Current Sense Filter

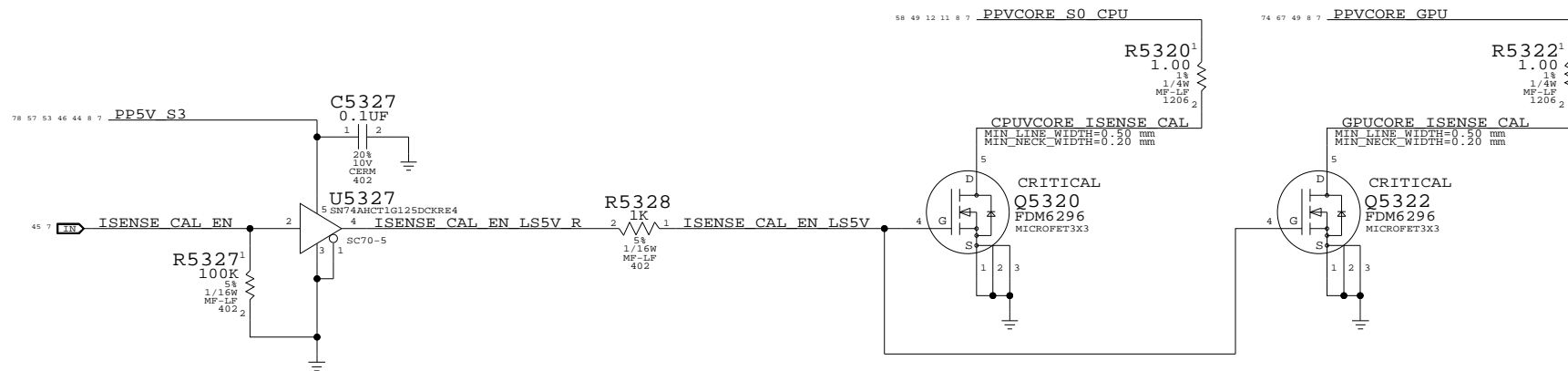


S0/GPU 1.25V Current Sense Filter



Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



Current & Voltage Sensing

SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)

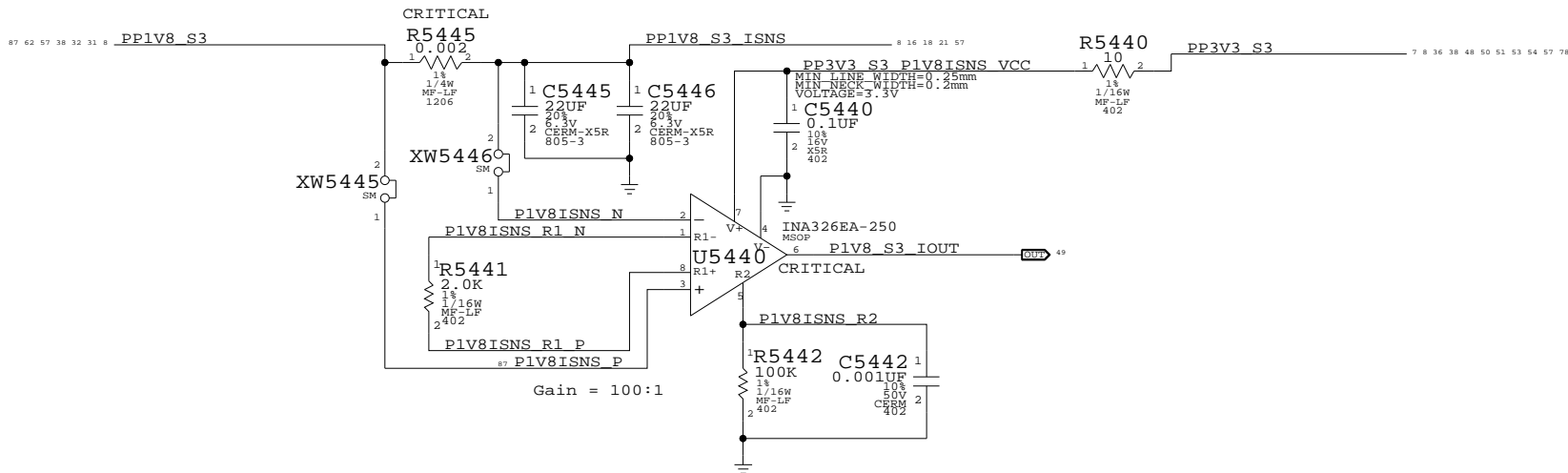
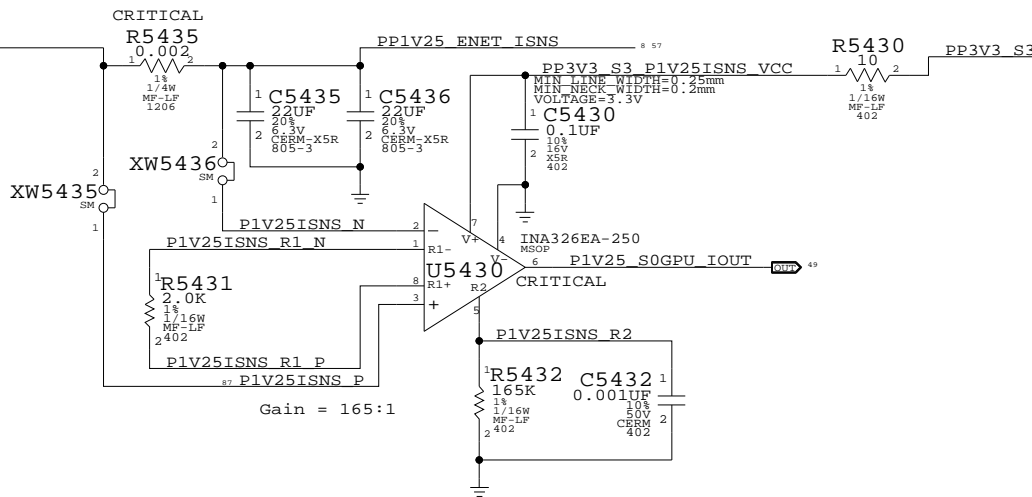
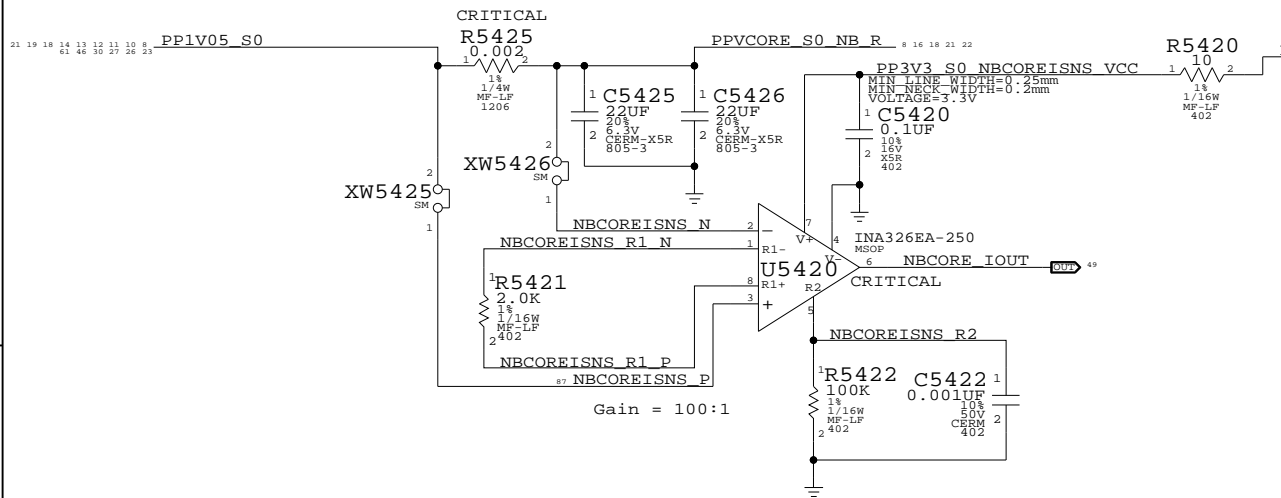
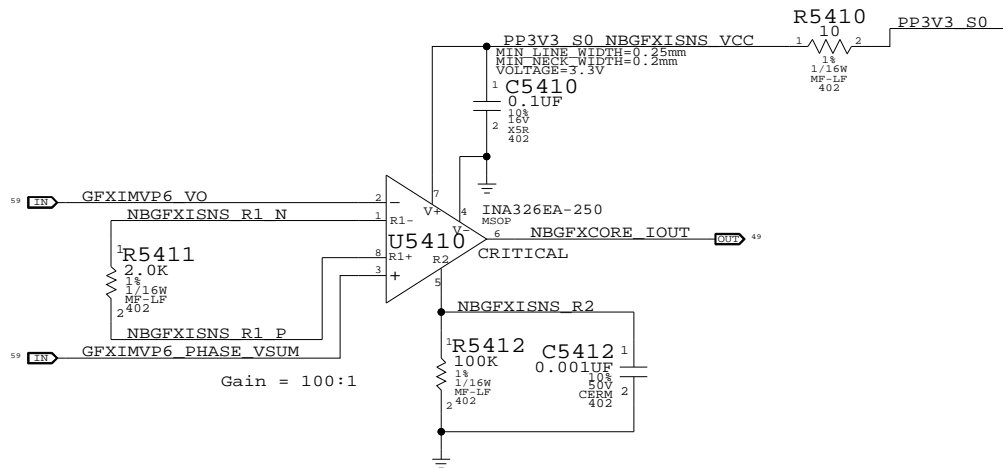
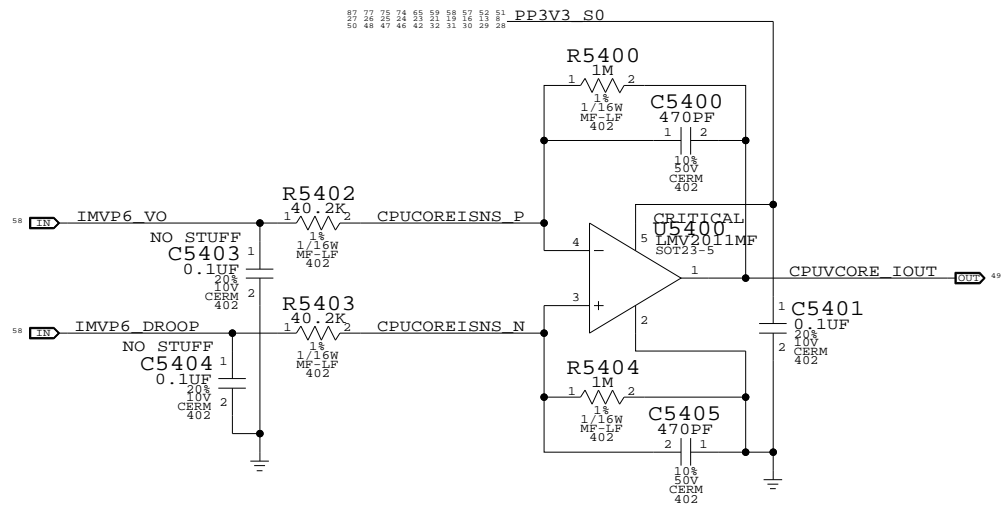
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SCALE	SHT	OF
NONE	49	88



Current Sensing

SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)

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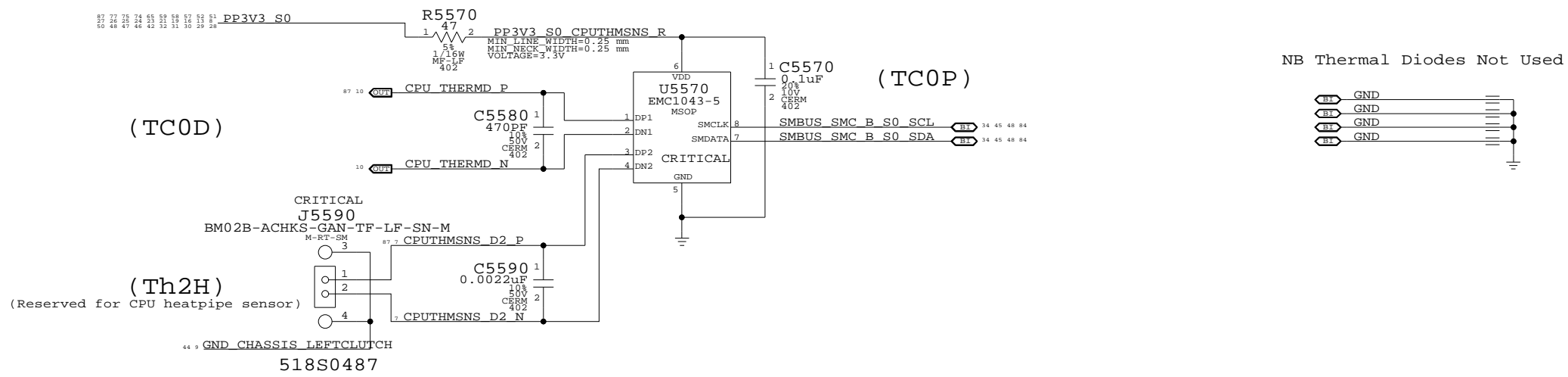
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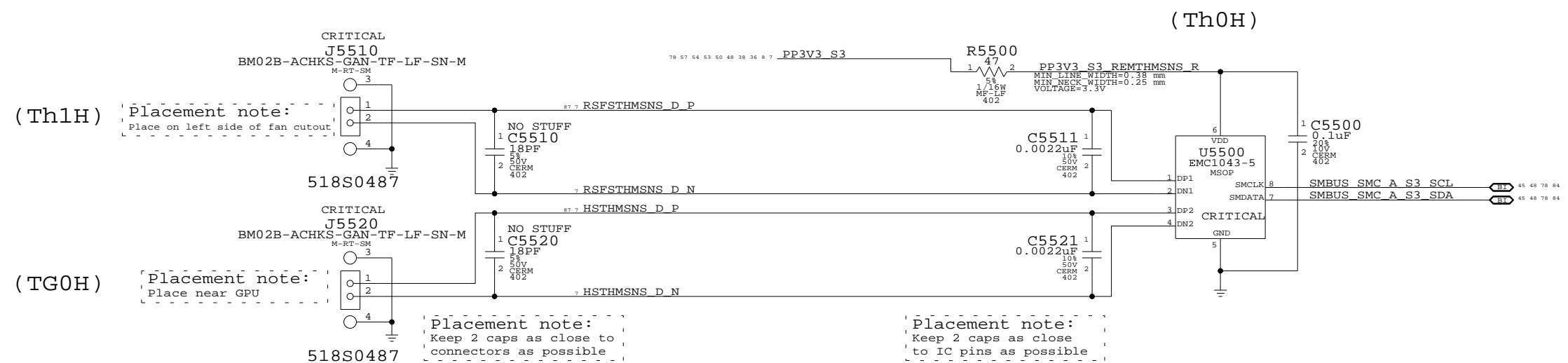
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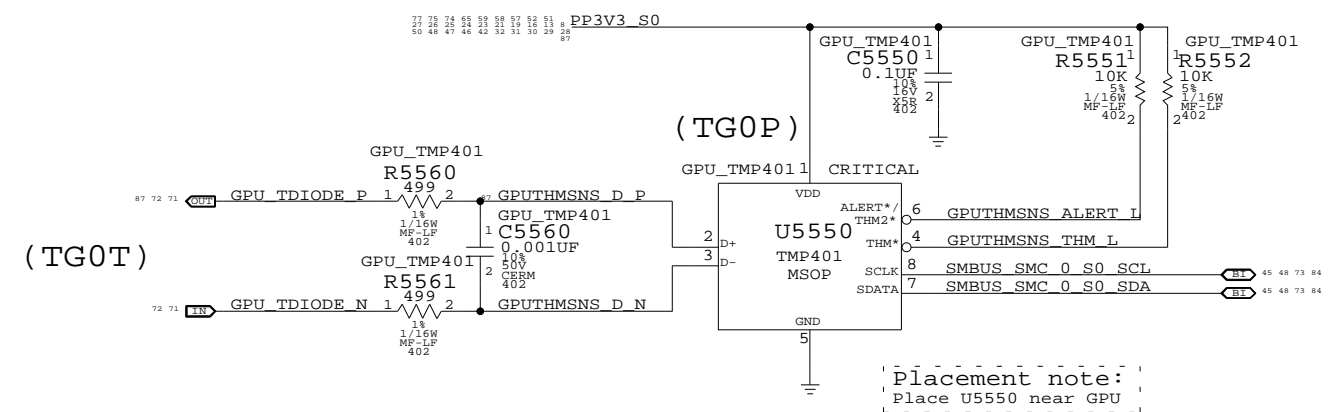
CPU T-Diode Thermal Sensor



GPU/Heat Pipe & Bottom Case Skin Thermal Sensor

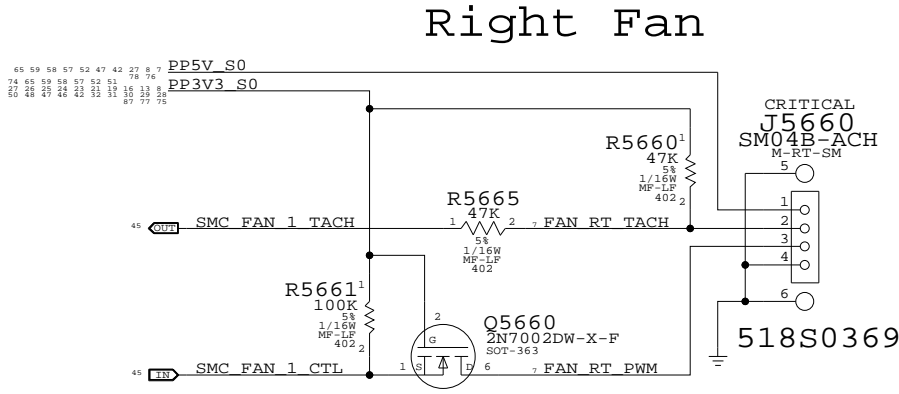
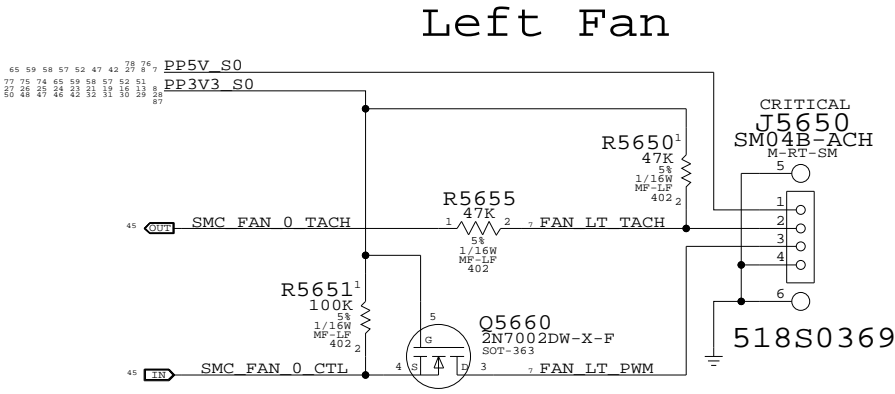


GPU Die Thermal Sensor



Thermal Sensors		
SYNC_MASTER= (MASTER)		SYNC_DATE= (MASTER)
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SCALE		SHT	OF
NONE		51	88



Fan Connectors

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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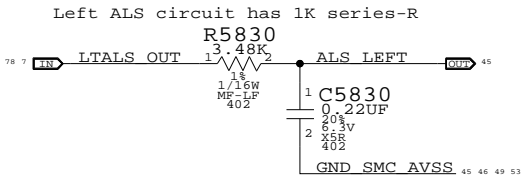
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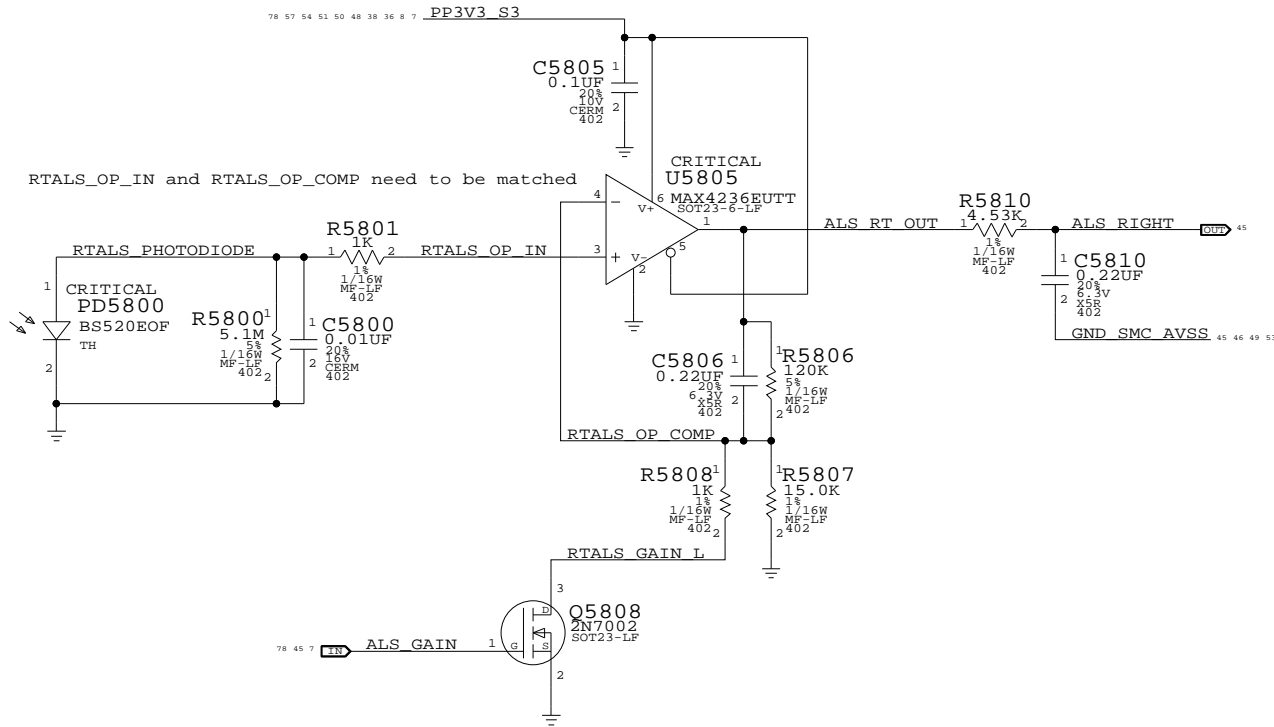
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

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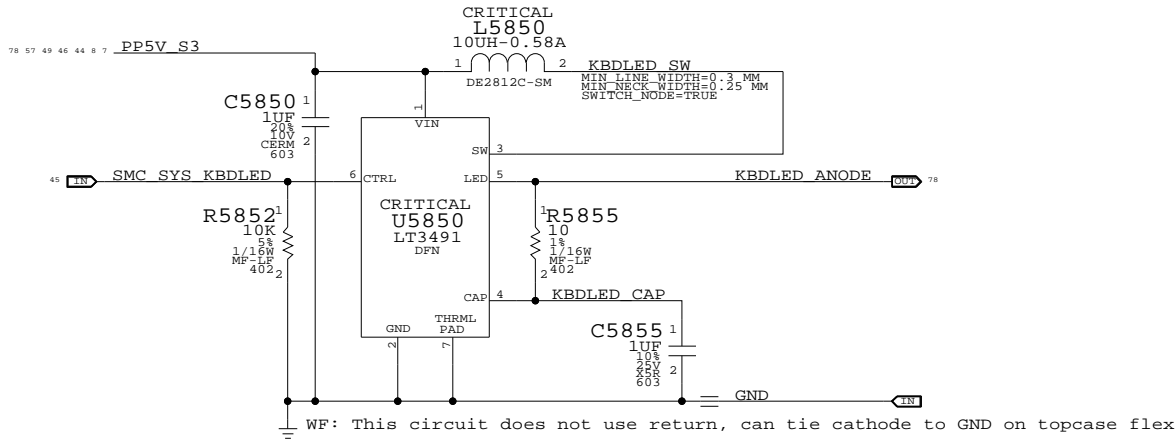
Left ALS Filter



Right ALS Circuit



Keyboard LED Driver



ALS Support

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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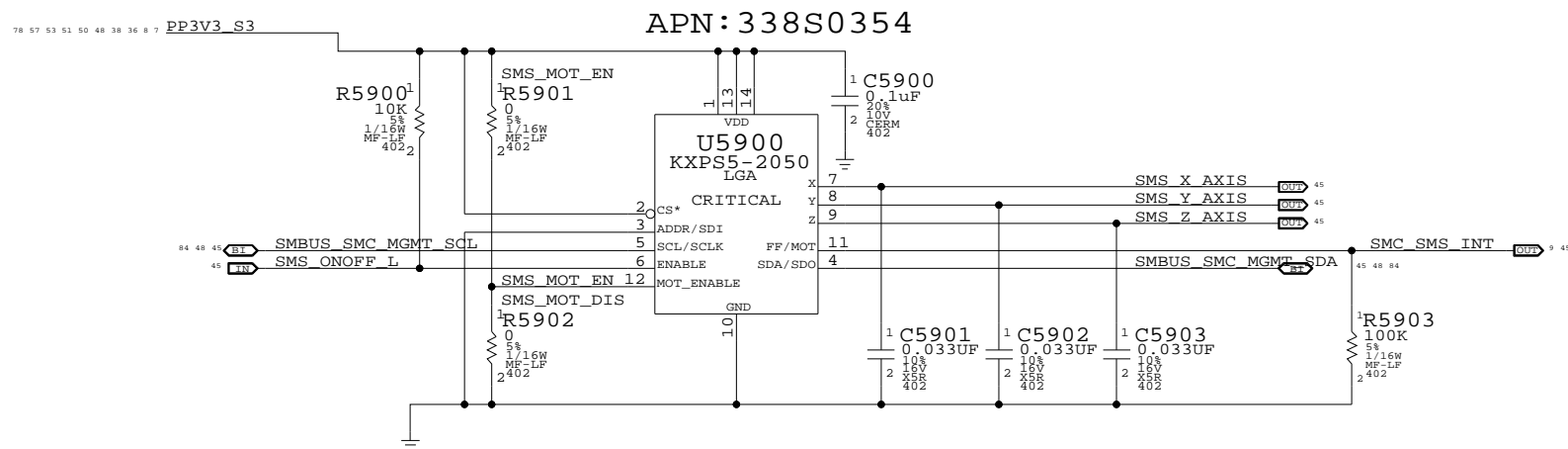



APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	14.0.0
SCALE	SHT	OF
NONE	53	88

Alias SCL/SDA to GND if using analog outputs only

1 

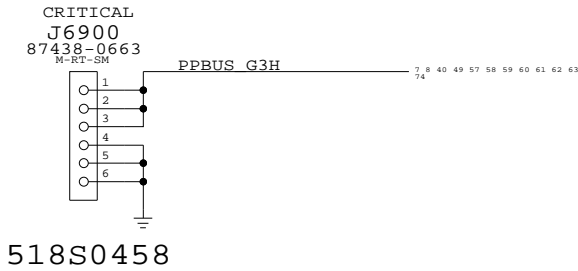


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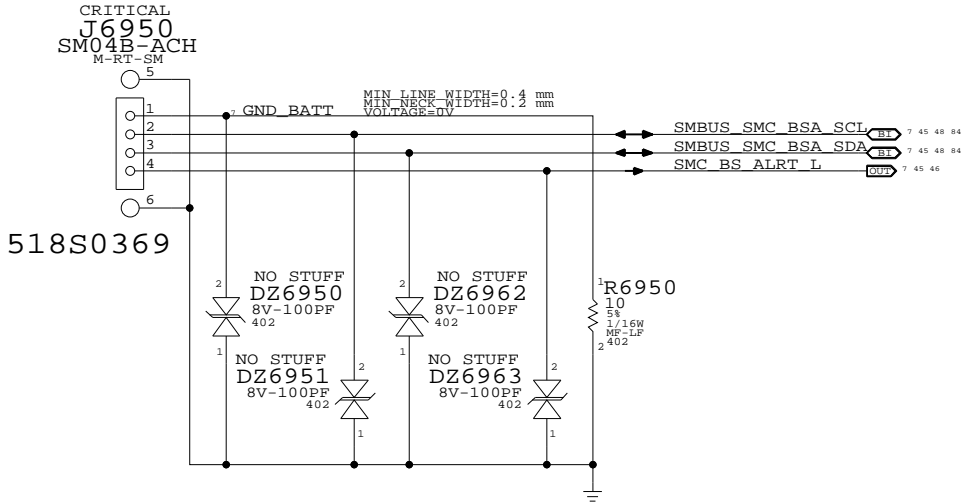


APPLE COMPUTER INC.

Left I/O Power Connector



Battery Connector (Digital Signals)



PBus-In & Battery Connectors

SYNC_MASTER=(M59_SYNC) SYNC_DATE=09/09/2006

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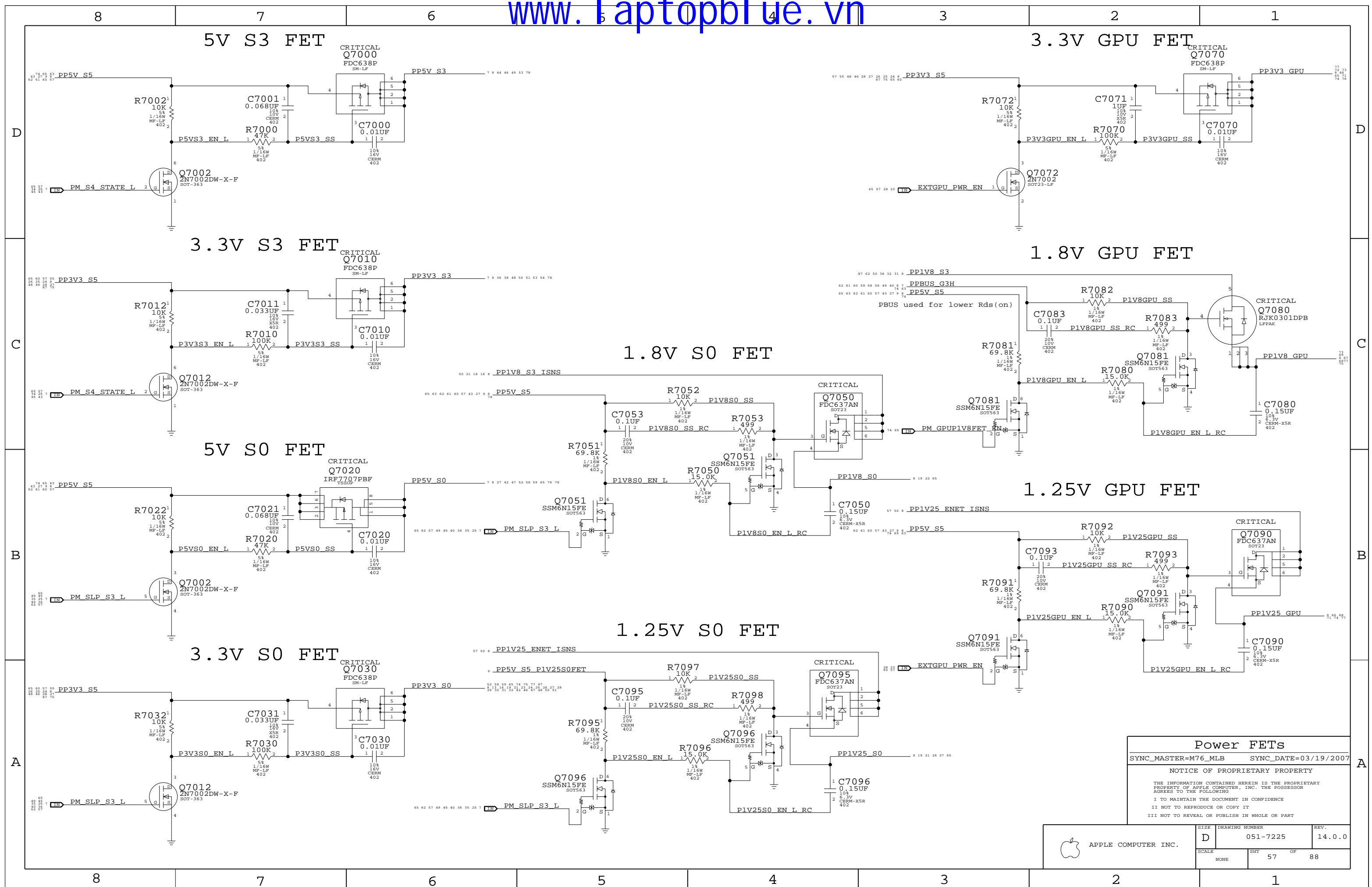
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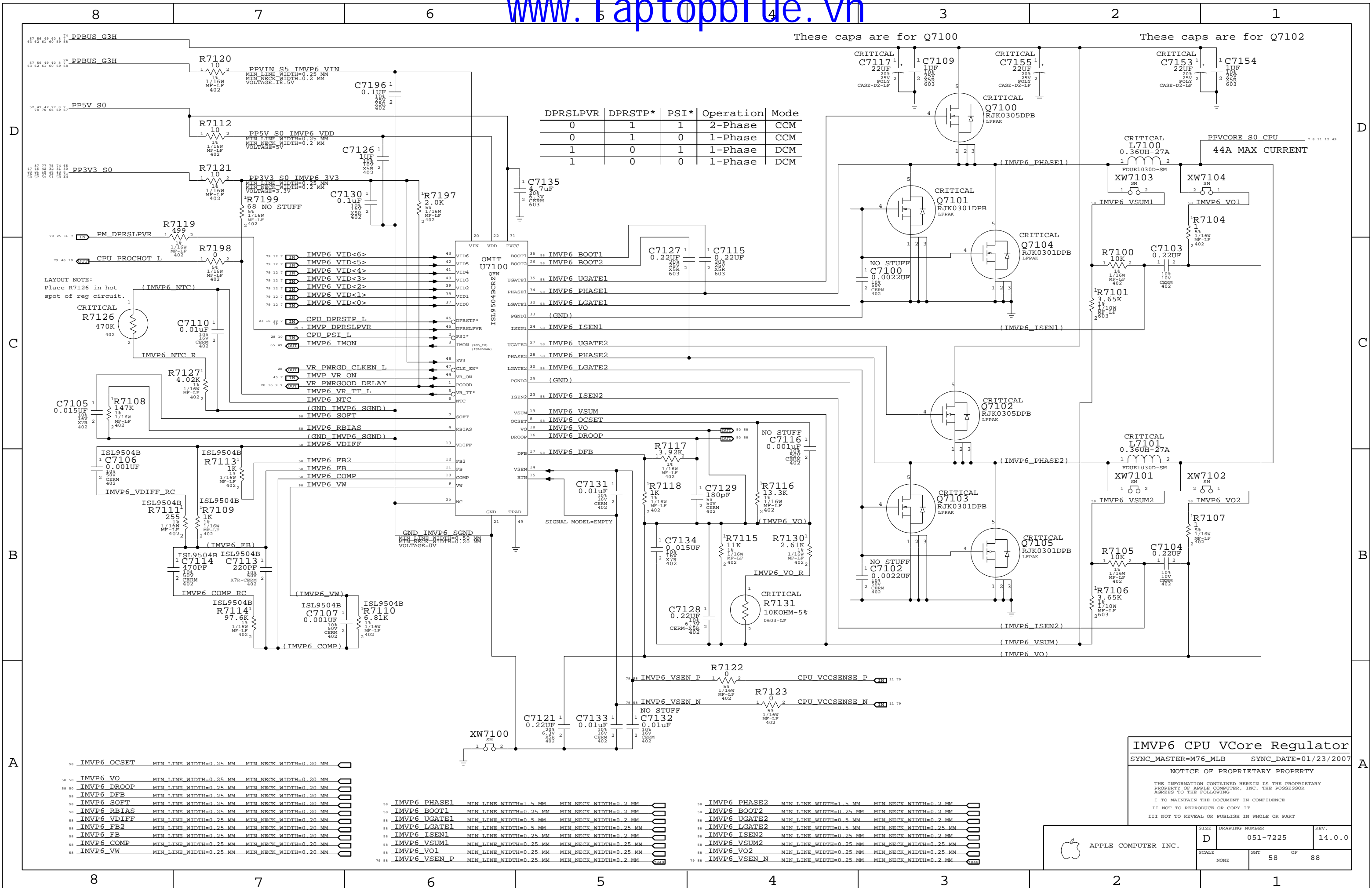
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SIZE	DRAWING NUMBER	REV.
D	051-7225	14.0.0
SCALE	SHT	OF
NONE	56	88



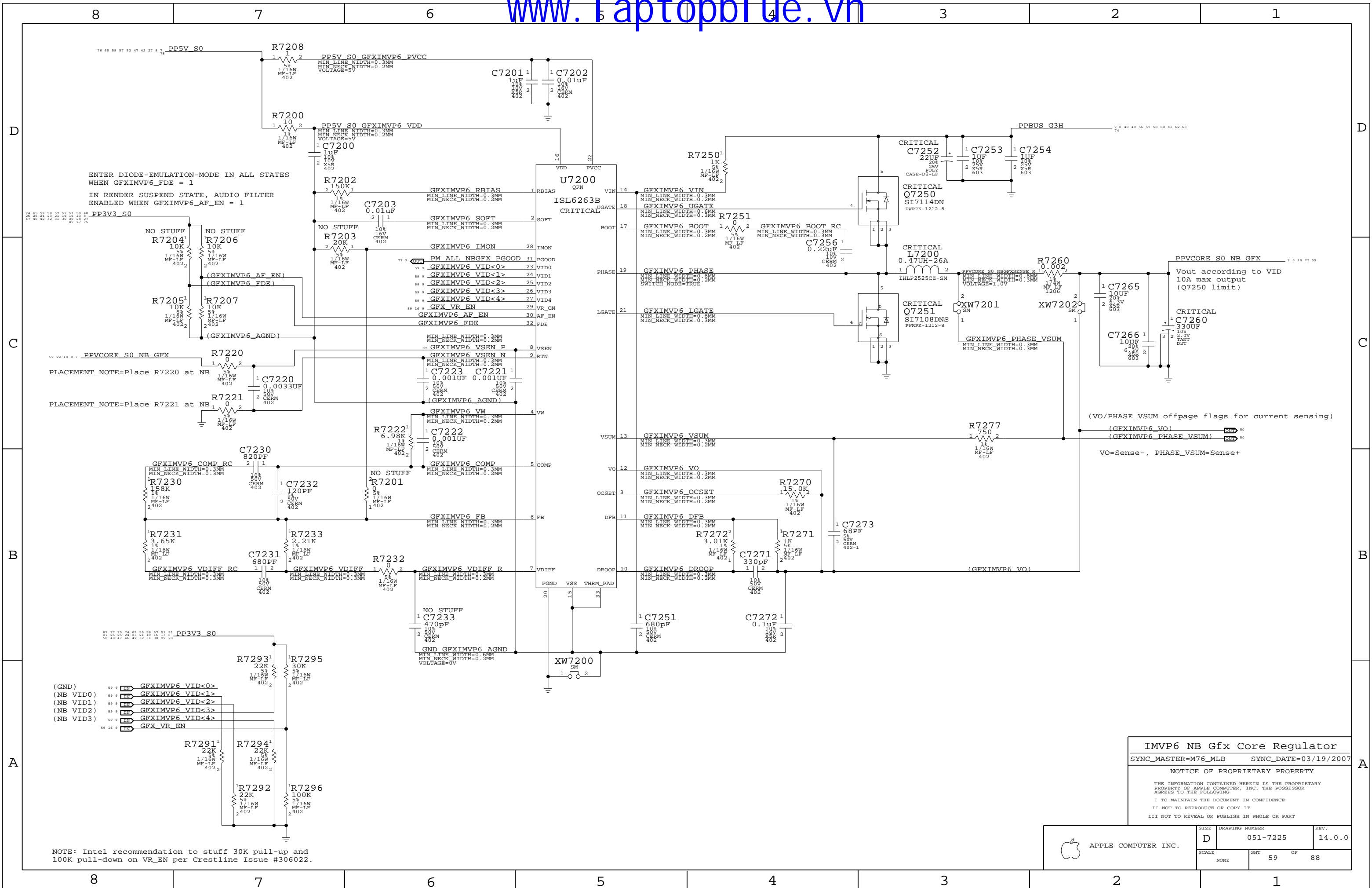


IMVP6 CPU VCore Regulator

SYNC_MASTER=M76_MLB SYNC_DATE=01/23/2007

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IMVP6 NB Gfx Core Regulator
SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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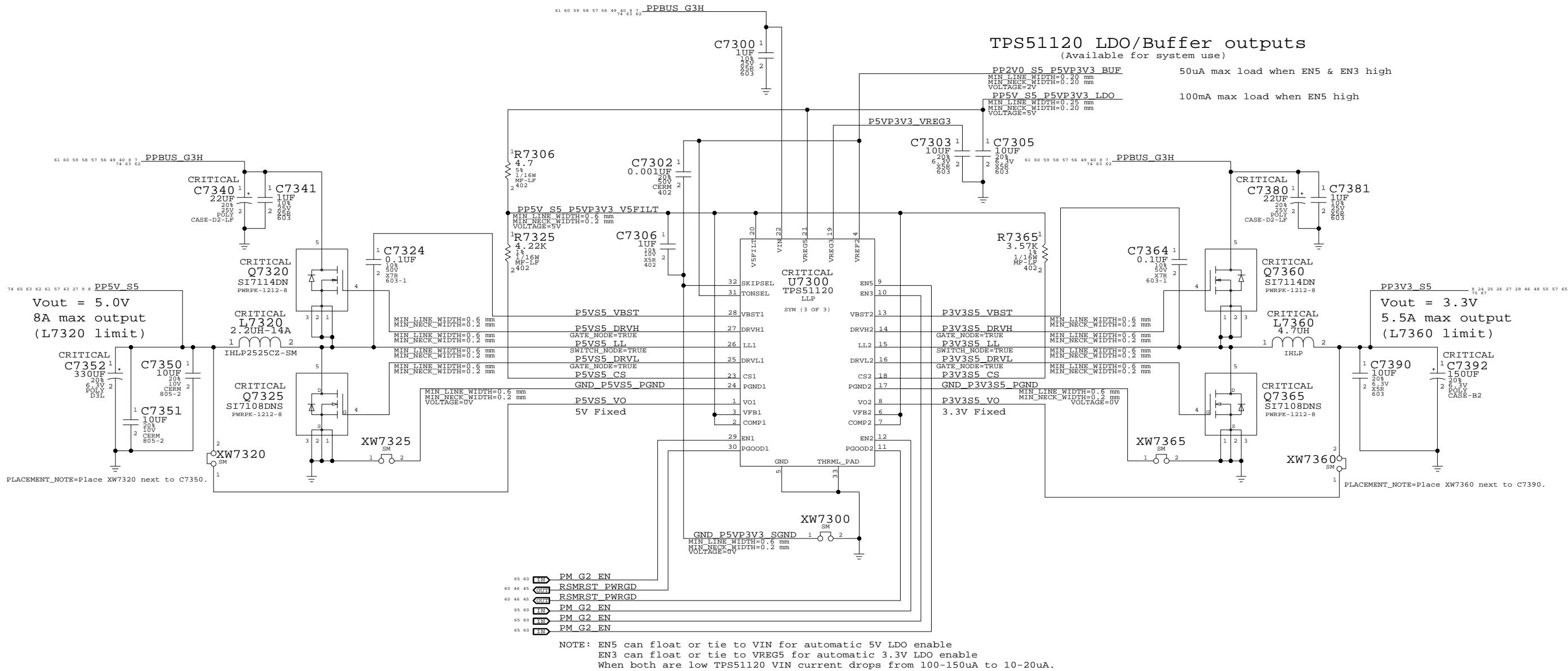
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	D	051-7225	14.0.0
SCALE	SHT		OF
	NONE		59 88

NOTE: Intel recommendation to stuff 30K pull-up and 100K pull-down on VR_EN per Crestline Issue #306022.



5V / 3.3V Power Supply

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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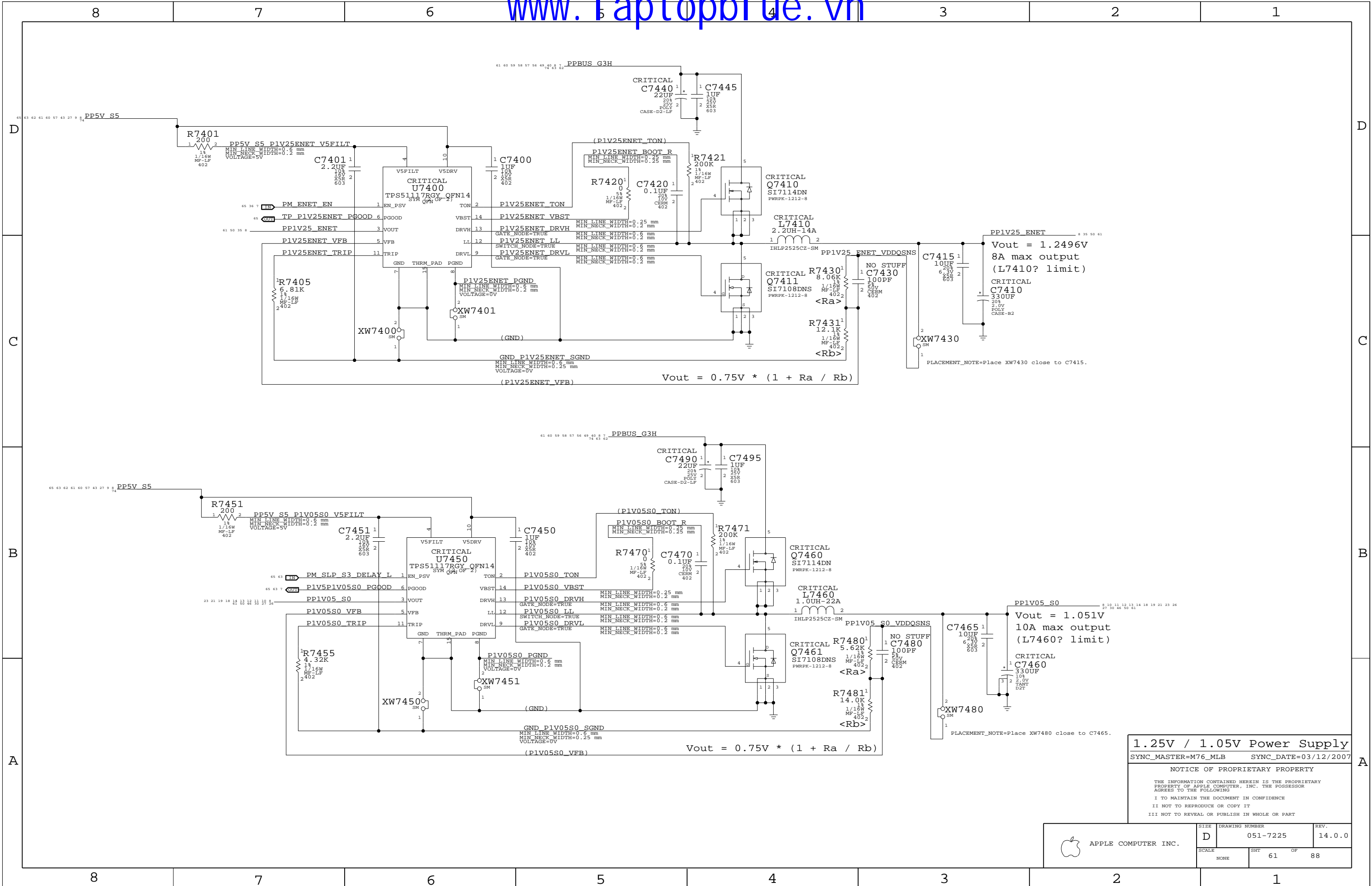
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	14.0.0
SCALE	SHT	OF
NONE	60	88



D

D

C

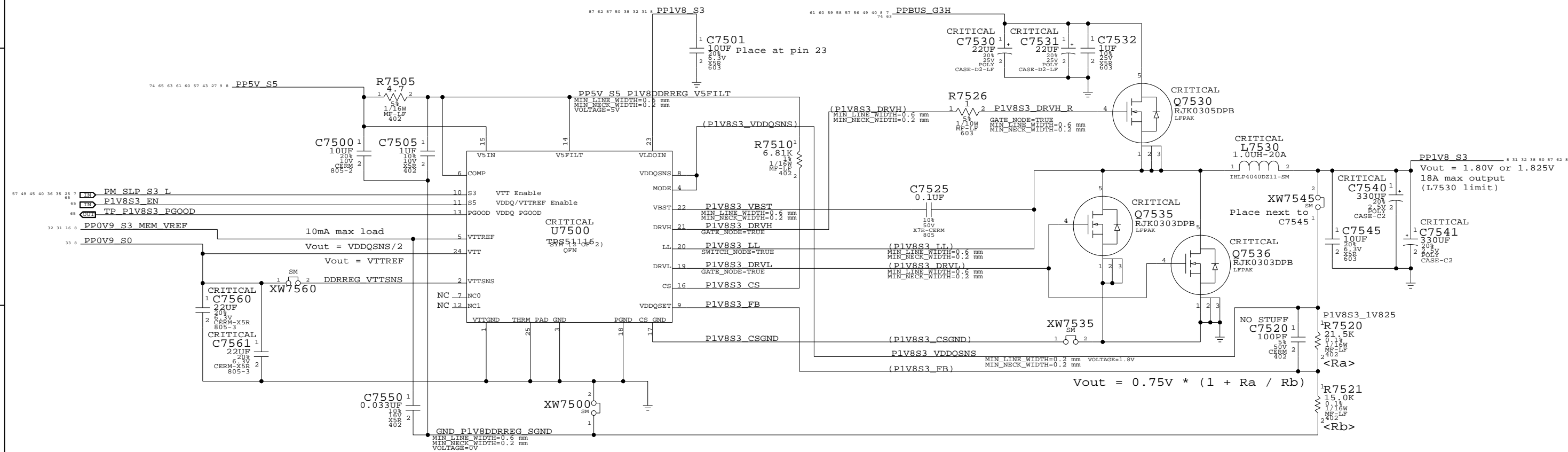
C

B

B

A

A



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
103S0192	1	RES,MTL FILM,21K,0.1,0402,SM,LF	R7520	CRITICAL	P1V8S3_1V8

1.8V DDR2 Supply

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

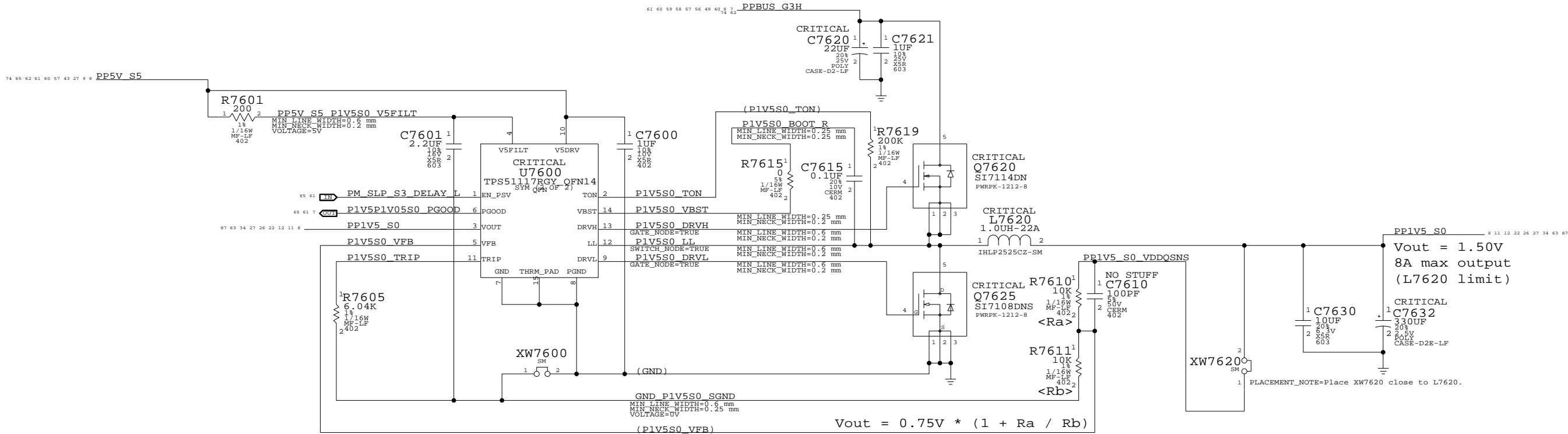
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D	051-7225	14.0.0
SCALE	SHT	OF
NONE	62	88



1.5V Power Supply

SYNC_MASTER=M76_MLB SYNC_DATE=03/12/2007

NOTICE OF PROPRIETARY PROPERTY

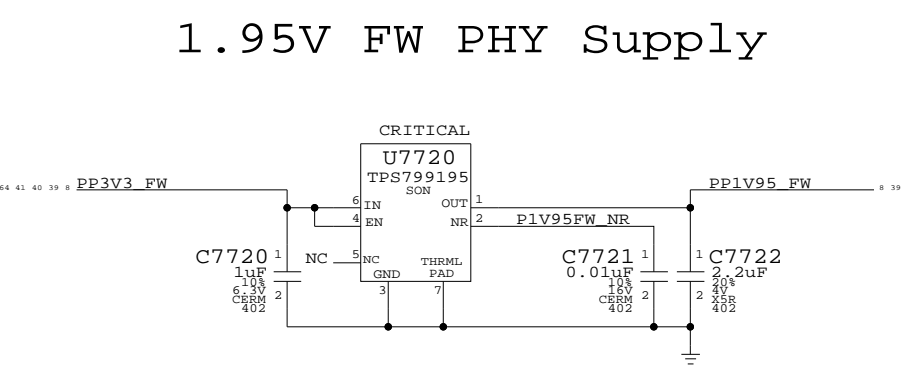
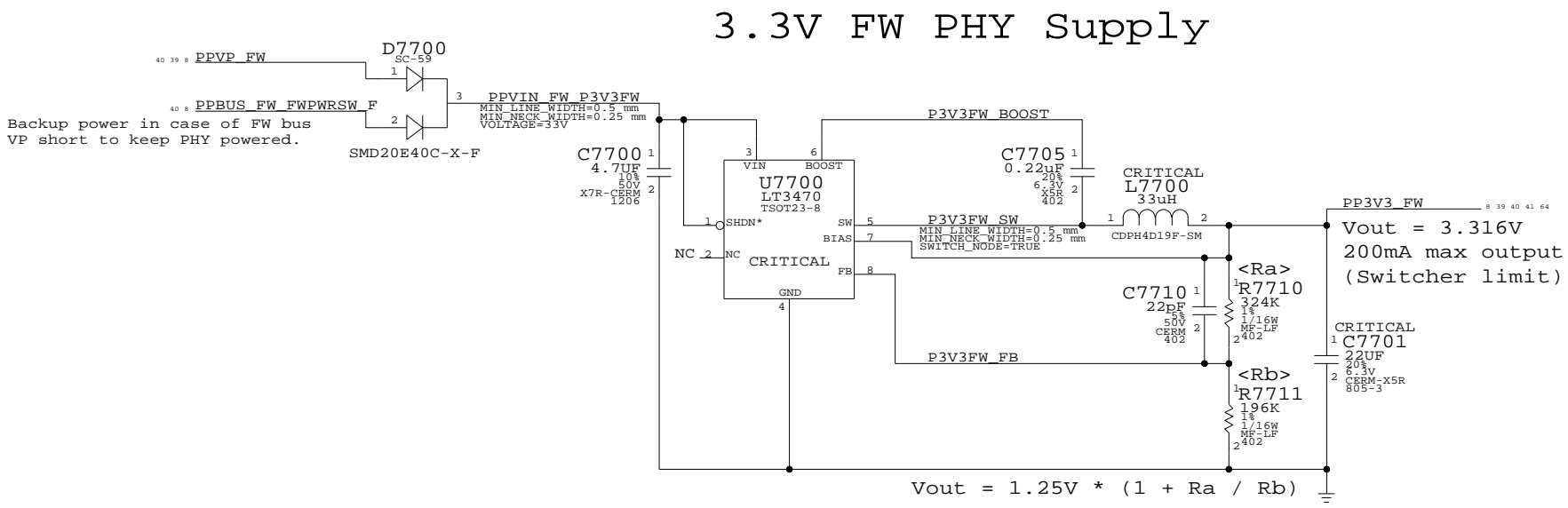
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	D	051-7225	14.0.0
SCALE		SHT	OF
NONE		63	88



FW PHY Power Supplies

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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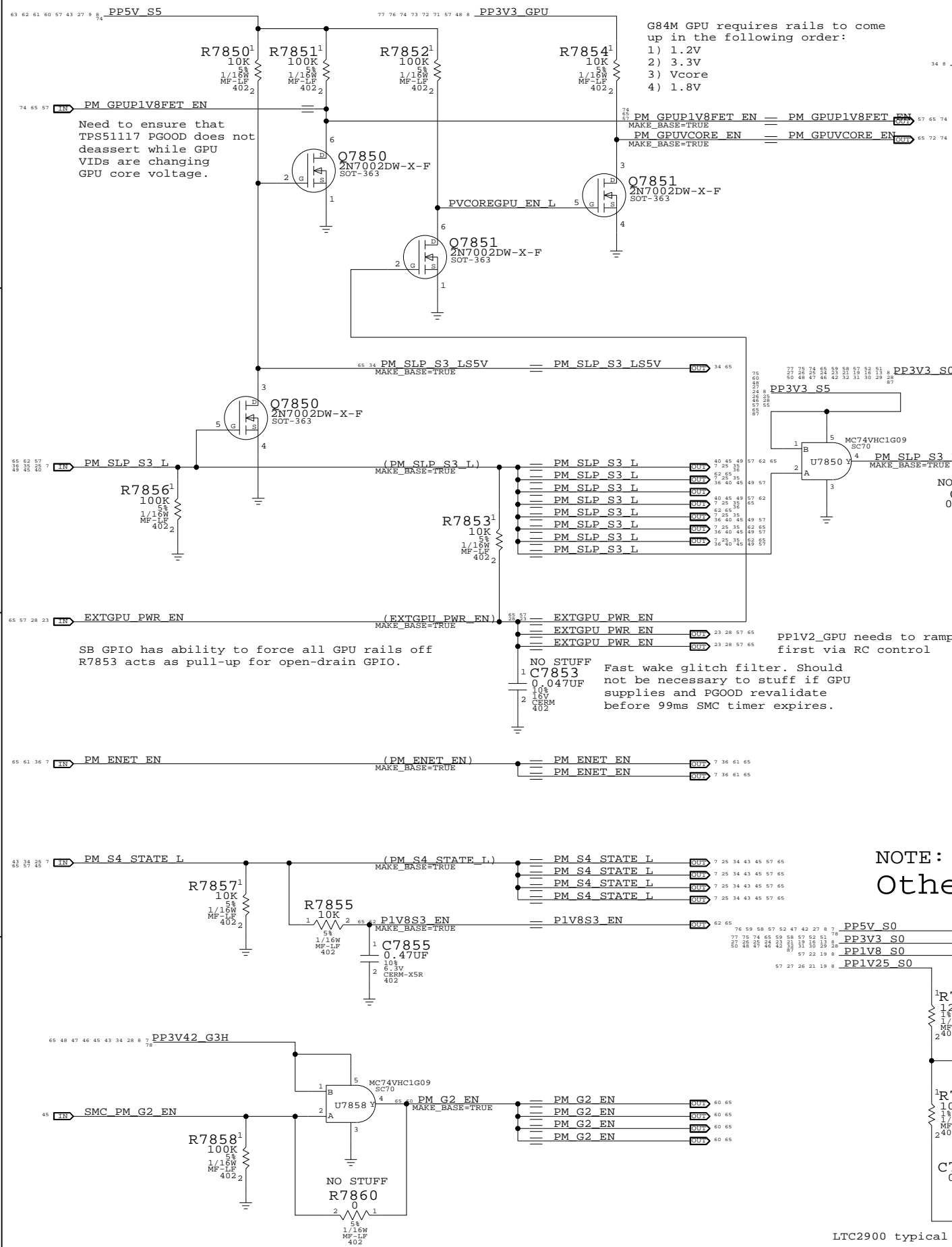
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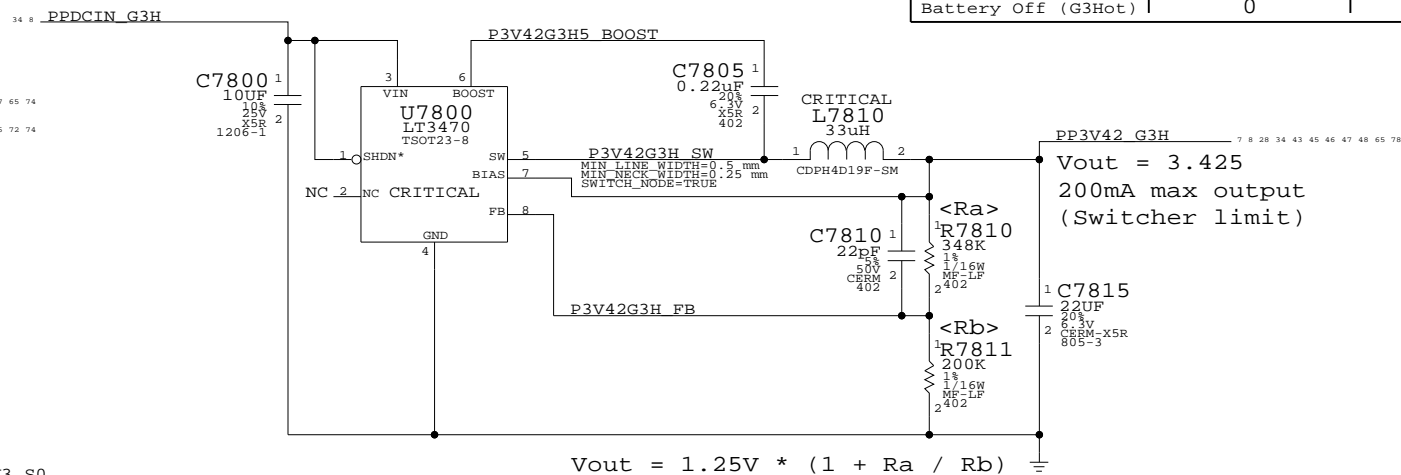
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7225	REV. 14.0.0
	SCALE NONE	SHT 64	OF 88

Power Control Signals



3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



Unused PGOOD Signals

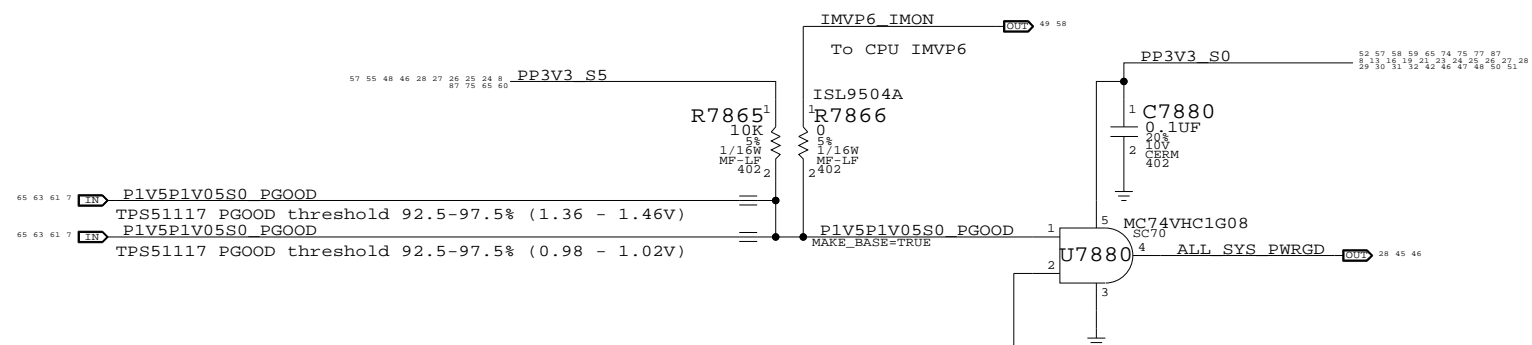
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65 61 TP P1V25ENET PGOOD — TP P1V25ENET PGOOD 61 65
      — MAKE BASE=TRUE
65 62 TP P1V8S3 PGOOD — TP P1V8S3 PGOOD 62 65
      — MAKE BASE=TRUE

```

1.5V / 1.05V PWRGD Circuit

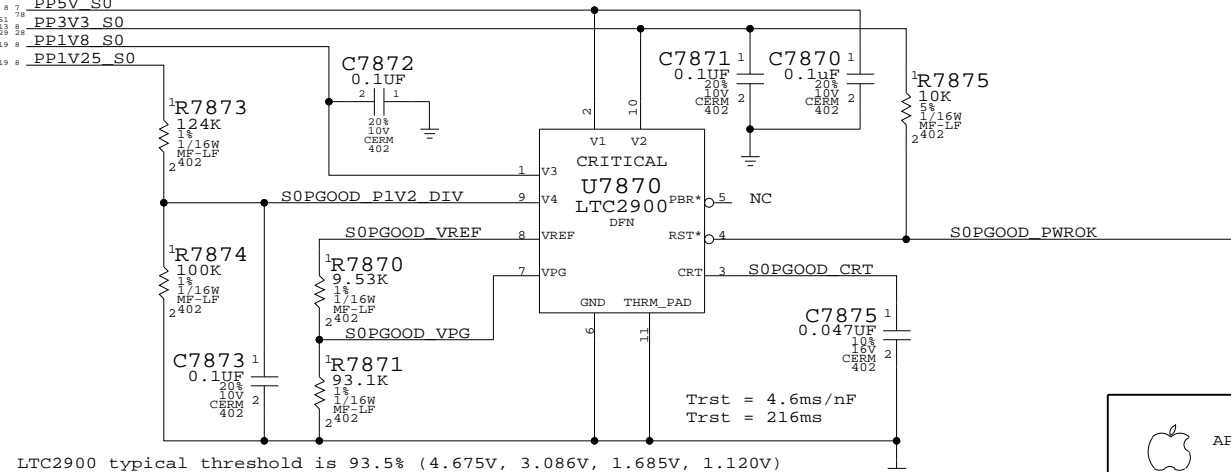
Reports when 1.5V S0 and 1.05V S0 are in regulation



NOTE: 0.9V/2.5V is not checked!

Other S0 Rails PWRGD Circuit

Does not include GFX rails



LTC2900 typical threshold is 93.5% (4.675V, 3.086V, 1.685V, 1.120V)

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

- Vout = 3.425
200mA max output
(Switcher limit)

$$V_{out} = 1.25V * (1 + R_a / R_b) =$$

3.425V G3Hot Supply & Power Control

SYNC_MASTER= (MASTER)	SYNC_DATE= (MASTER)
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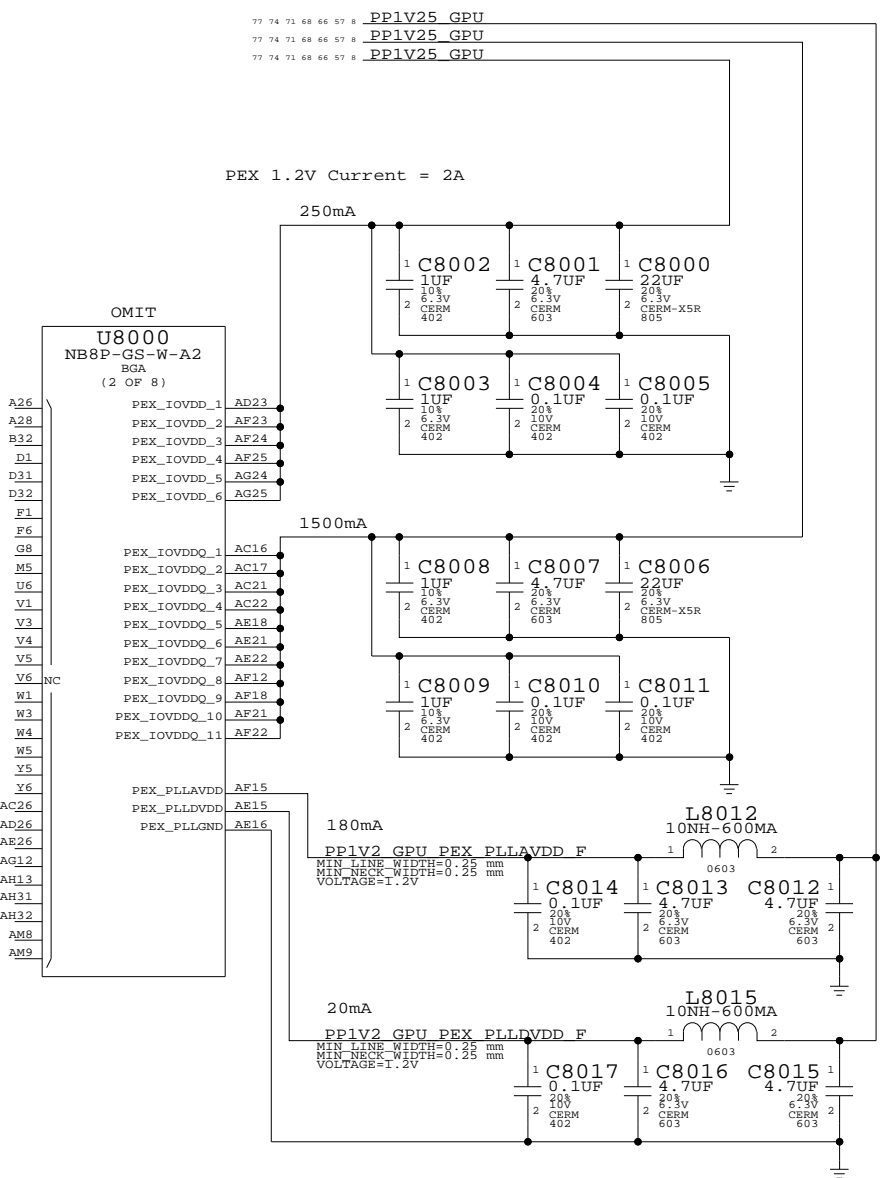
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D	051-7225	14.0.0
SCALE	SHT	OF
NONE	65	88

Page Notes

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- =PPIV2_GPU_PEX_IOVDDQ
- =PPIV2_GPU_PEX_IOVDD

Signal aliases required by this page:
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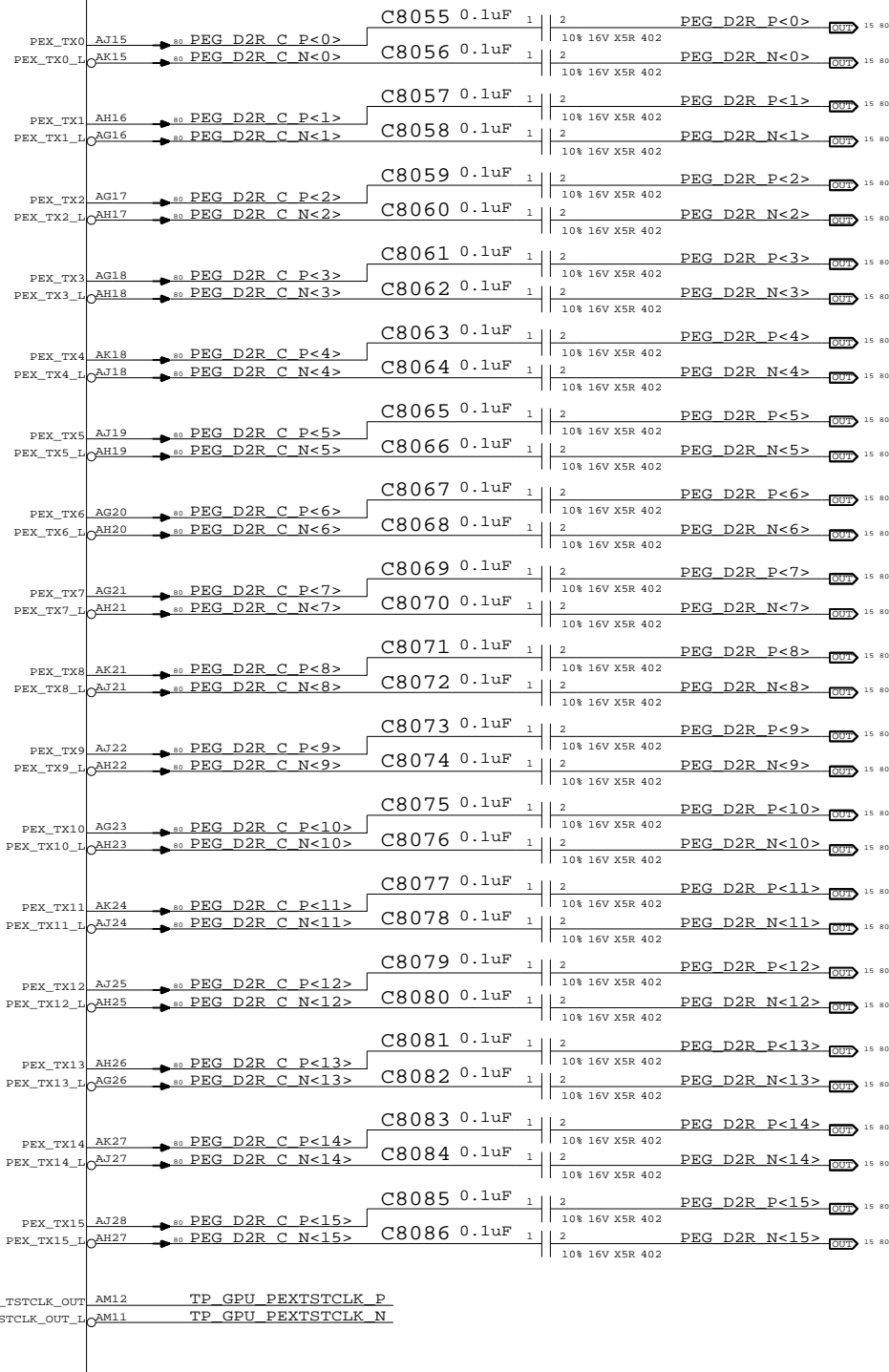
BOM options provided by this page:
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OMIT

U8000
NB8P-GS-W-A2
BGA
(1 OF 8)

PCI-EXPRESS BUS INTERFACE



NV G84M PCI-E

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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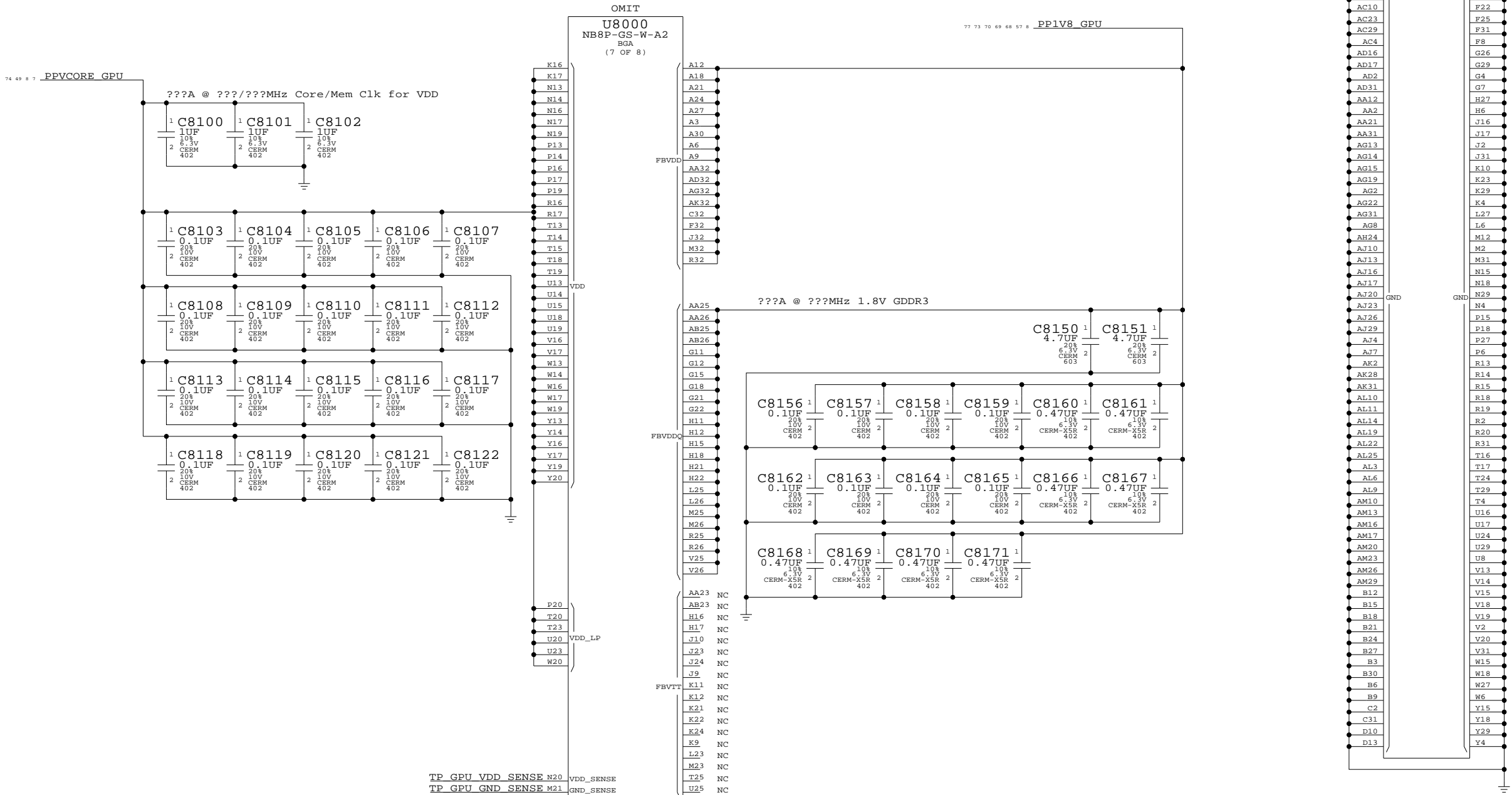
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D	051-7225	14.0.0
SCALE	SHT	OF
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Page Notes

Power aliases required by this page:
- =PPVCORE_GPU
- =PP1V8_GPU_FBVDDQ

Signal aliases required by this page:
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BOM options provided by this page:
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NV G84M Core/FB Power

SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)

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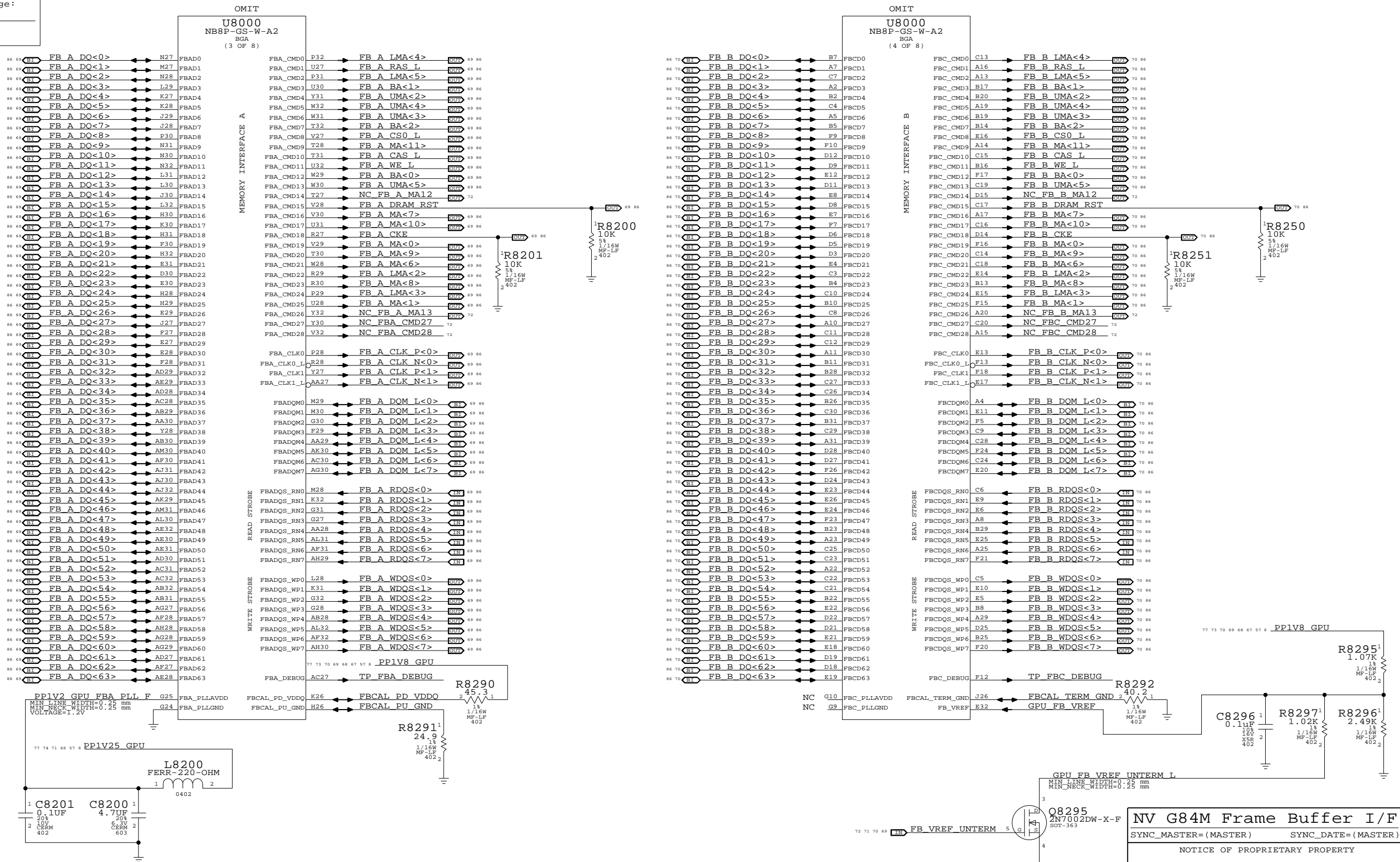
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SCALE	SHT	OF
NONE	67	88

Page Notes

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- =PP1V8_GPU_FBI0

Signal aliases required by this page:
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BOM options provided by this page:
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NV G84M Frame Buffer I/F

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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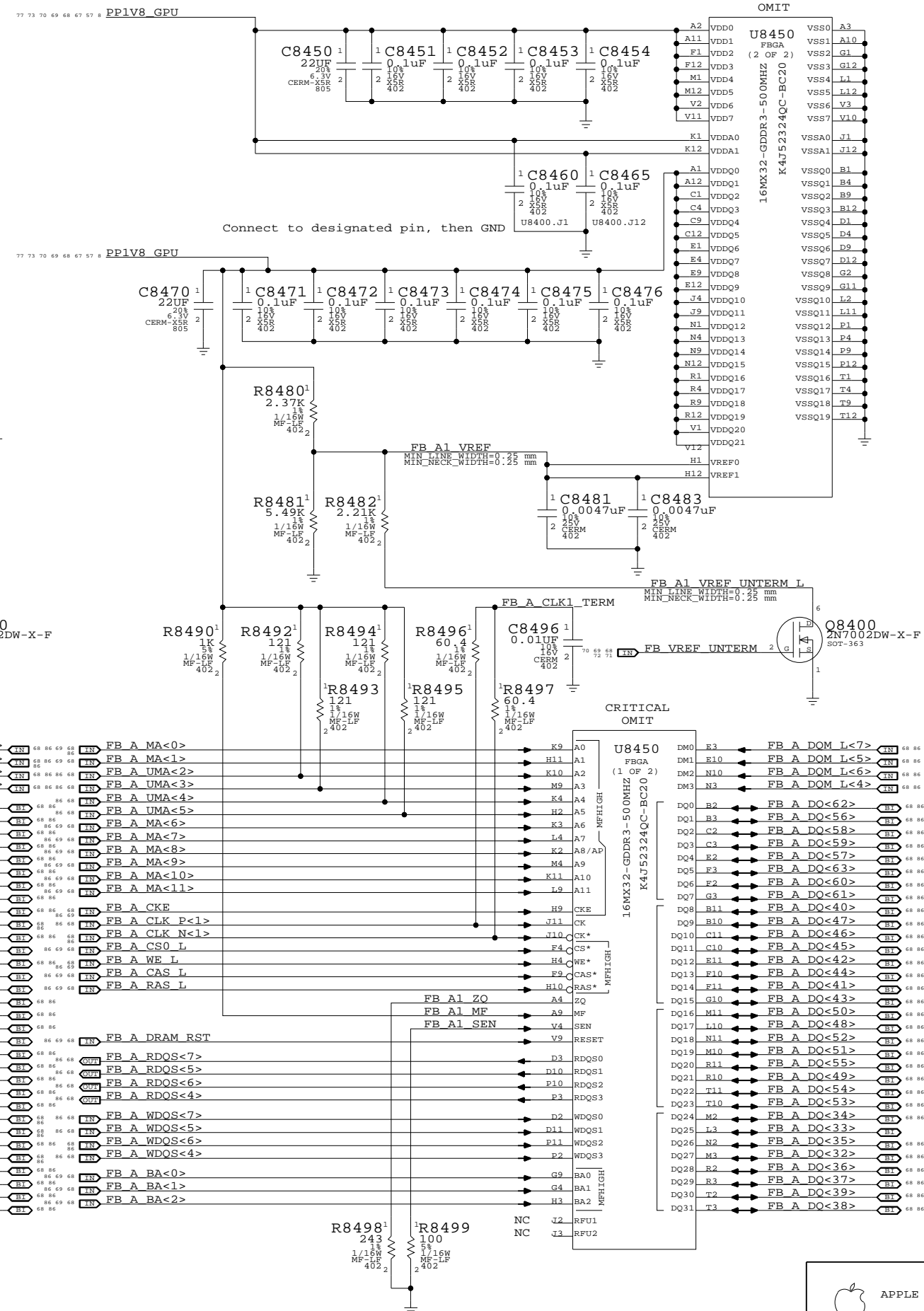
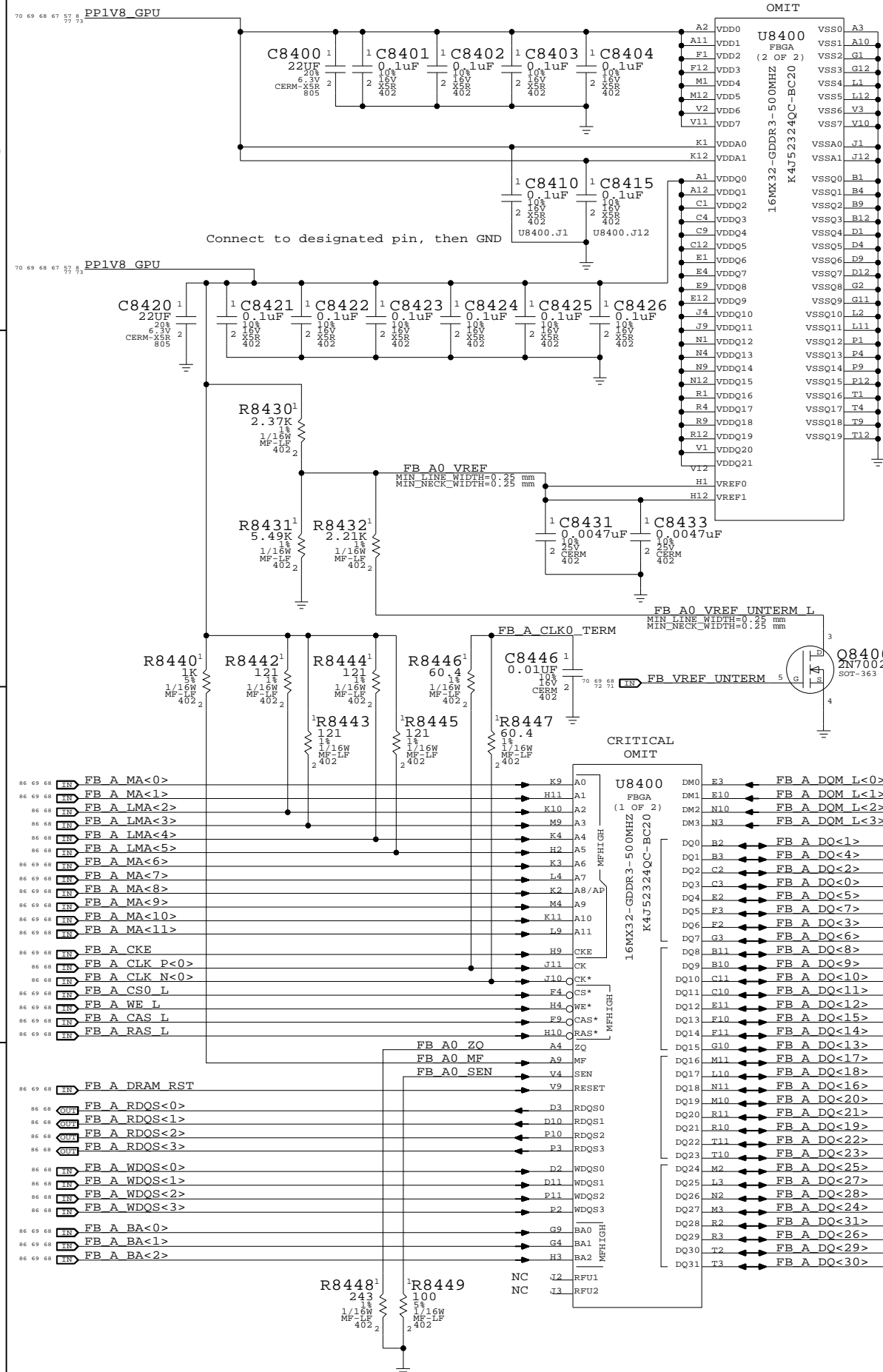
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SIZE	DRAWING NUMBER	REV.
D	051-7225	14.0.0
SCALE	SHT 68 OF 88	

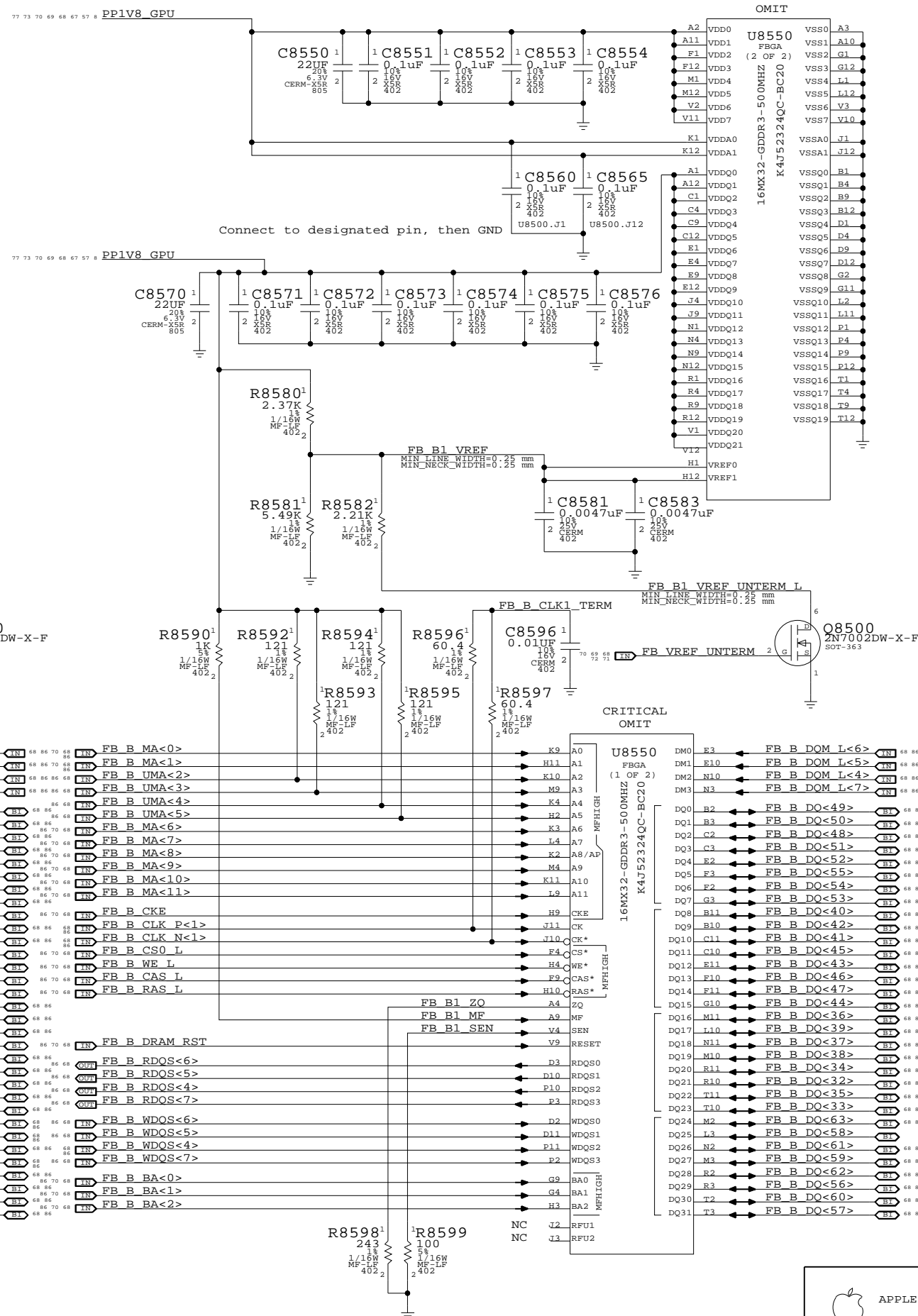
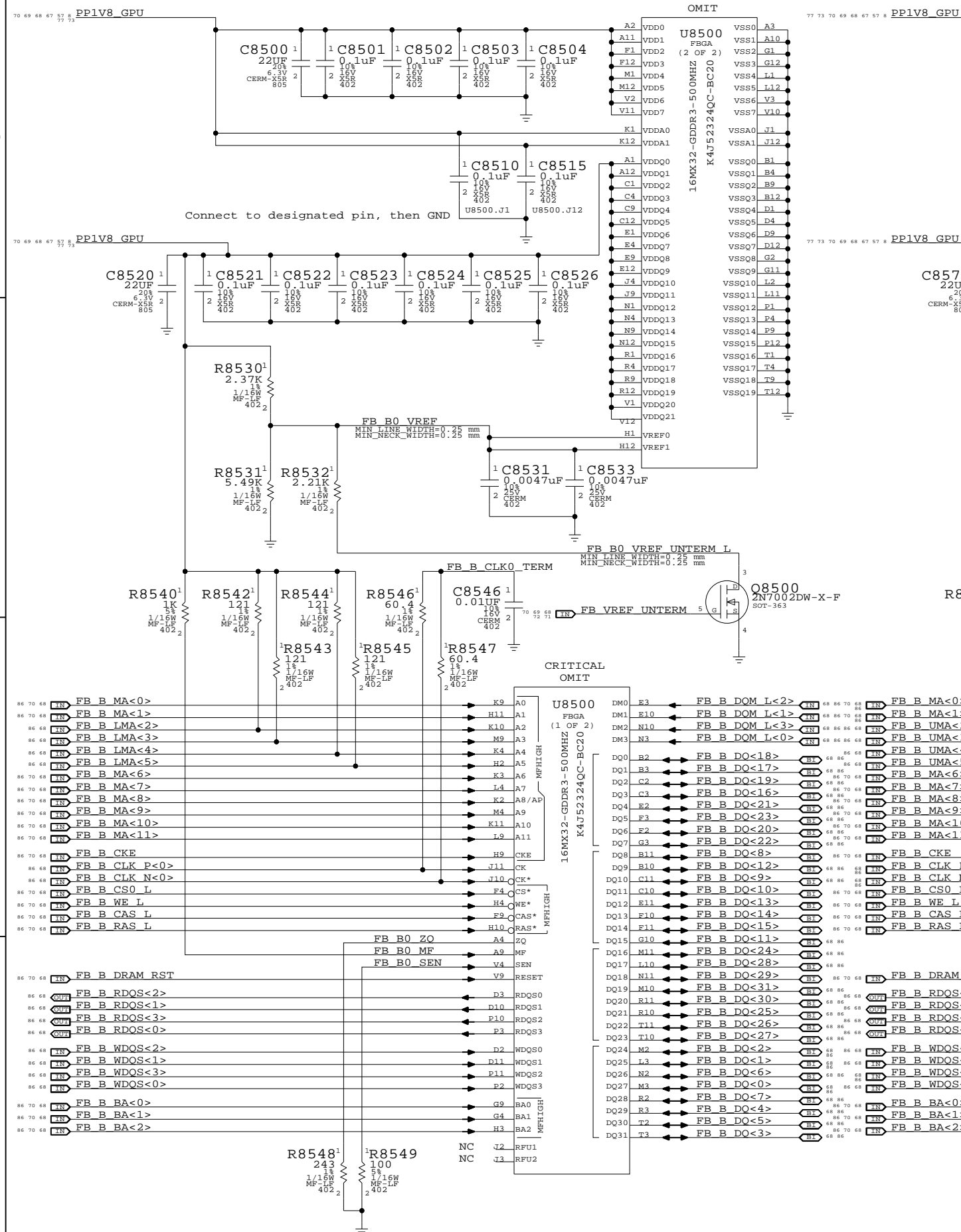
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Signal aliases required by this page: (NONE)
BOM options provided by this page: (NONE)



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DQ25	L3	FB A DQ<33>	BT	68 86
DQ26	N2	FB A DQ<35>	BT	68 86
DQ27	M3	FB A DQ<32>	BT	68 86
DQ28	R2	FB A DQ<36>	BT	68 86
DQ29	R3	FB A DQ<37>	BT	68 86
DQ30	T2	FB A DQ<39>	BT	68 86
DQ31	T3	FB A DQ<38>	BT	68 86

GDDR3 Frame Buffer A	
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)
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Power aliases required by this page: - =Pp1v8_S0_FB_VDD - =Pp1v8_S0_FB_VDDQ
Signal aliases required by this page: (NONE)
BOM options provided by this page: (NONE)



0	DM0	R3	←	FB B DOM L<6>	Q16	68 86
1)	DM1	E10	←	FB B DOM L<5>	Q17	68 86
	DM2	N10	←	FB B DOM L<4>	Q18	68 86
	DM3	N3	←	FB B DOM L<7>	Q19	68 86
0	DQ0	B2	→	FB B DQ<49>	Q20	68 86
	DQ1	B3	→	FB B DQ<50>	Q21	68 86
	DQ2	C2	→	FB B DQ<48>	Q22	68 86
	DQ3	C3	→	FB B DQ<51>	Q23	68 86
	DQ4	E2	→	FB B DQ<52>	Q24	68 86
	DQ5	F3	→	FB B DQ<55>	Q25	68 86
	DQ6	F2	→	FB B DQ<54>	Q26	68 86
	DQ7	G3	→	FB B DQ<53>	Q27	68 86
	DQ8	B11	→	FB B DQ<40>	Q28	68 86
	DQ9	B10	→	FB B DQ<42>	Q29	68 86
	DQ10	C11	→	FB B DQ<41>	Q30	68 86
	DQ11	C10	→	FB B DQ<45>	Q31	68 86
	DQ12	E11	→	FB B DQ<43>	Q32	68 86
	DQ13	F10	→	FB B DQ<46>	Q33	68 86
	DQ14	F11	→	FB B DQ<47>	Q34	68 86
	DQ15	G10	→	FB B DQ<44>	Q35	68 86
DQ16	M11	→	FB B DQ<36>	Q36	68 86	
DQ17	L10	→	FB B DQ<39>	Q37	68 86	
DQ18	N11	→	FB B DQ<37>	Q38	68 86	
DQ19	M10	→	FB B DQ<38>	Q39	68 86	
DQ20	R11	→	FB B DQ<34>	Q40	68 86	
DQ21	R10	→	FB B DQ<32>	Q41	68 86	
DQ22	T11	→	FB B DQ<35>	Q42	68 86	
DQ23	T10	→	FB B DQ<33>	Q43	68 86	
DQ24	M2	→	FB B DQ<63>	Q44	68 86	
DQ25	L3	→	FB B DQ<58>	Q45	68 86	
DQ26	N2	→	FB B DQ<61>	Q46	68 86	
DQ27	M3	→	FB B DQ<59>	Q47	68 86	
DQ28	R2	→	FB B DQ<56>	Q48	68 86	
DQ29	R3	→	FB B DQ<52>	Q49	68 86	
DQ30	T2	→	FB B DQ<60>	Q50	68 86	
DQ31	T3	→	FB B DQ<57>	Q51	68 86	

GDDR3 Frame Buffer B	
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Page Notes

Power aliases required by this page:

- =PP3V3_GPU_VDD33
- =PP3V3_GPU_MIO
- =PP1V2_GPU_PLLVDD
- =PP1V2_GPU_H_PLLVDD
- =PP1V2_GPU_VID_PLLVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

D

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C

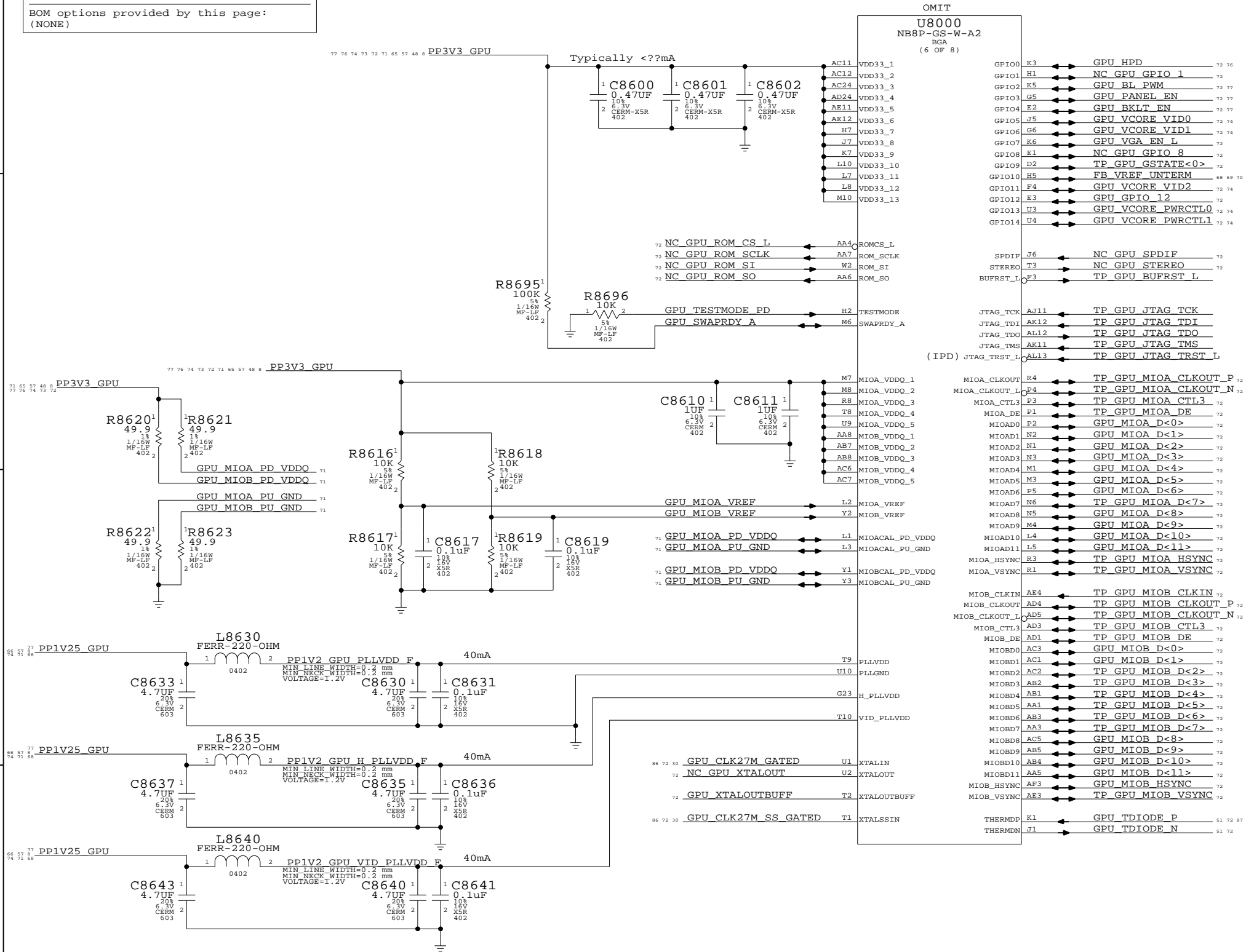
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NV G84M GPIO/MIO/Misc

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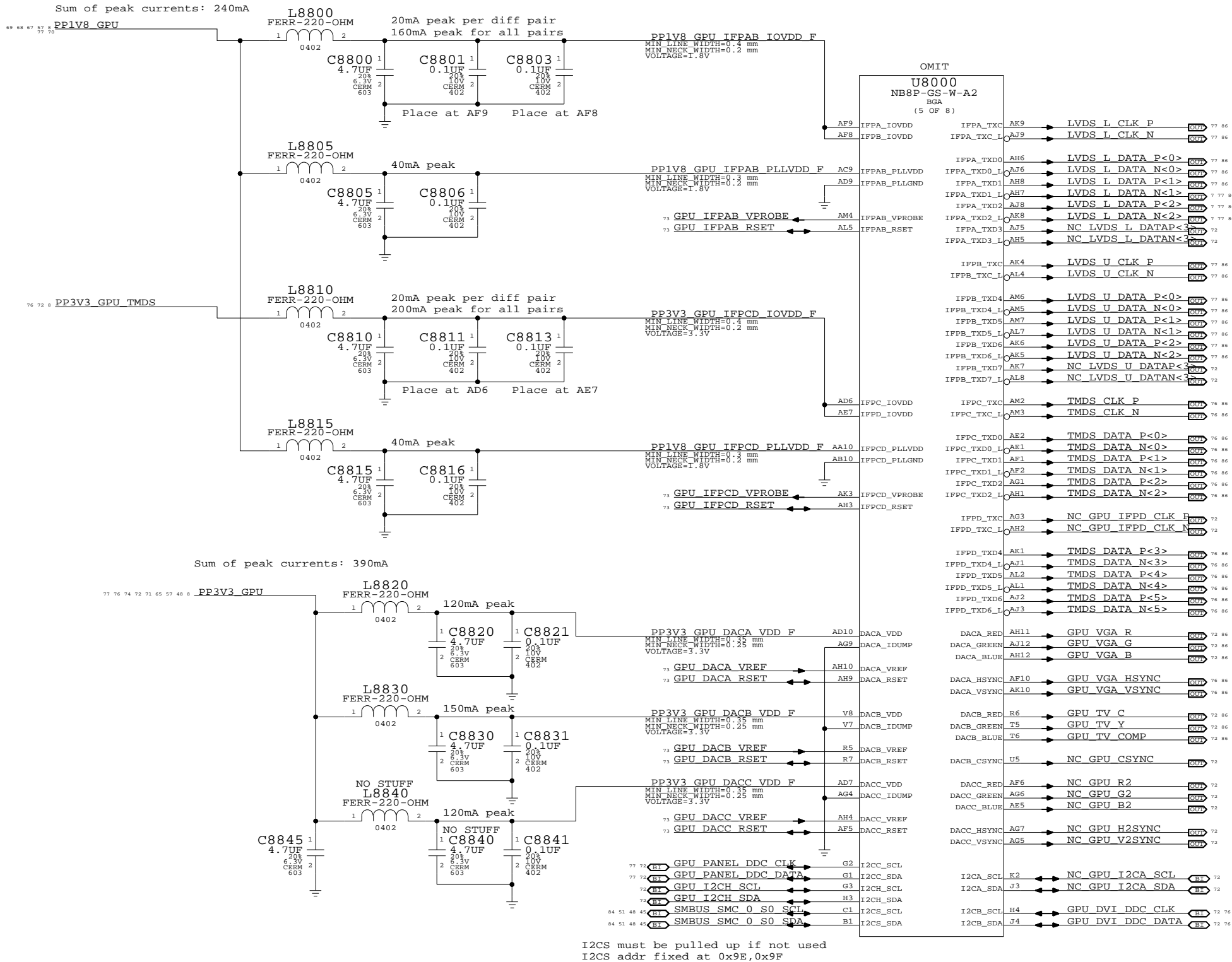
SIZE	DRAWING NUMBER	REV.
D	051-7225	14.0.0
SCALE	SHT	OF
NONE	71	88

Page Notes

Power aliases required by this page:
- =PP1V8_GPU_IFPX
- =PP3V3_GPU_IFPCD_IOVDD
- =PP3V3_GPU_DAC

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



Composite/S-Video	VGA	Component
C	R	Pr
Y	G	Y
Comp	B	Pb

NV G84M Video Interfaces

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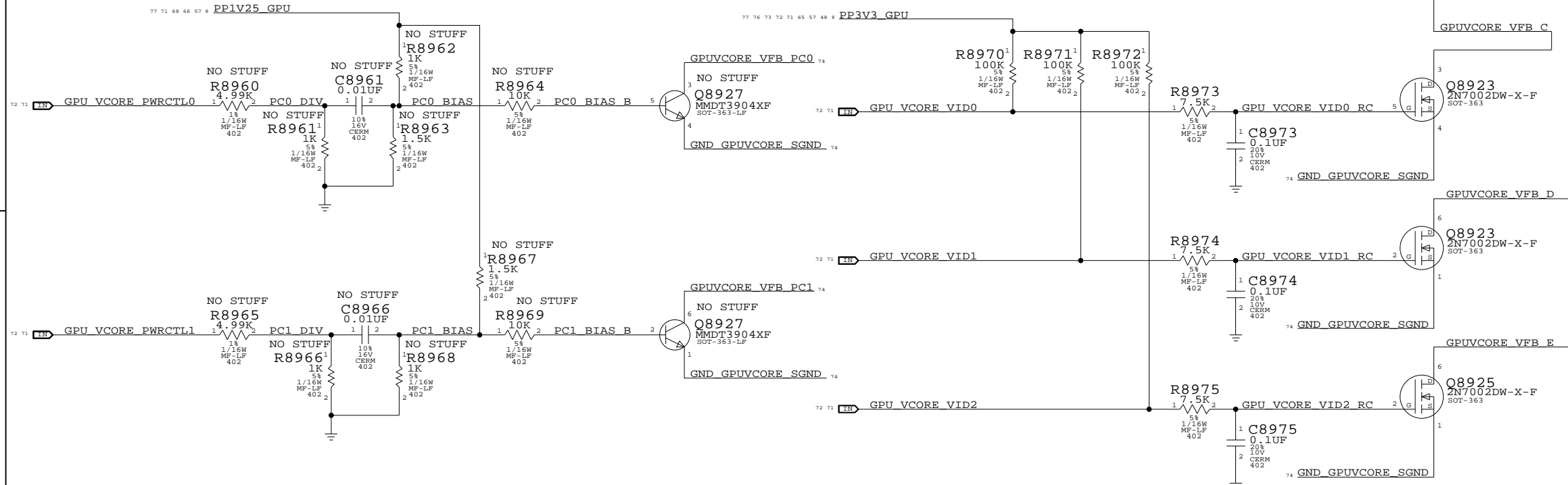
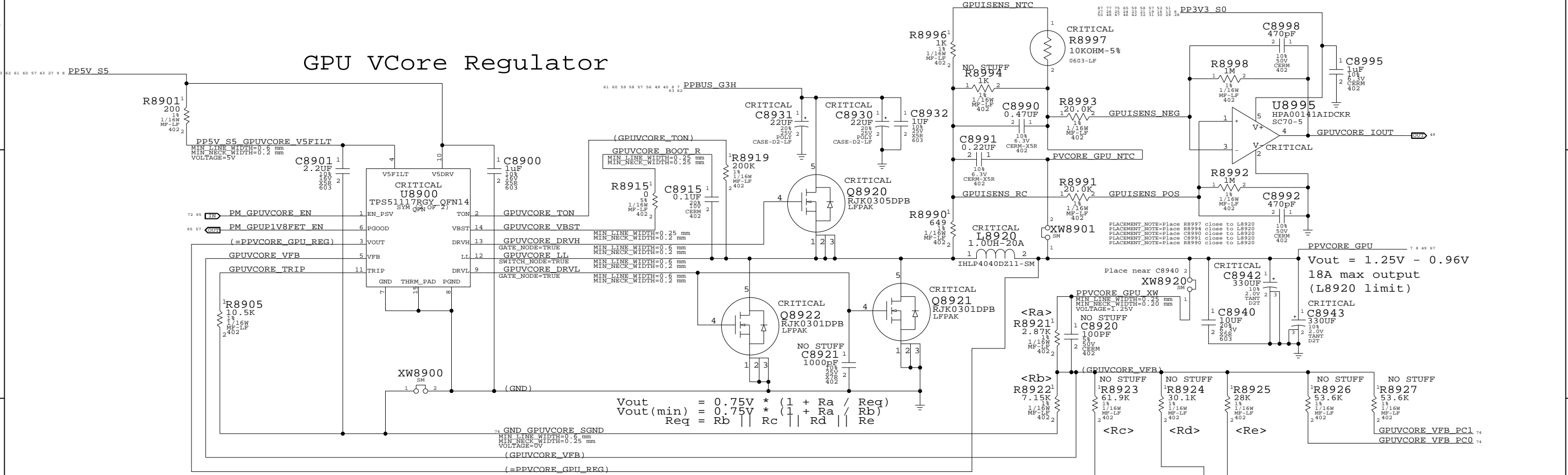


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GPU VCore Regulator

GPU VCore Current Sense



GPU VCore Setpoints

VID2	VID1	VID0	C	D	E	State
0	0	0	-	-	-	1.050V (rsvd state)
0	0	1	Y	-	-	1.050V (max batt)
0	1	1	Y	Y	-	1.050V (balanced)
1	1	1	Y	Y	Y	1.125V (max perf)

All other states not defined

GPU (G84M) Core Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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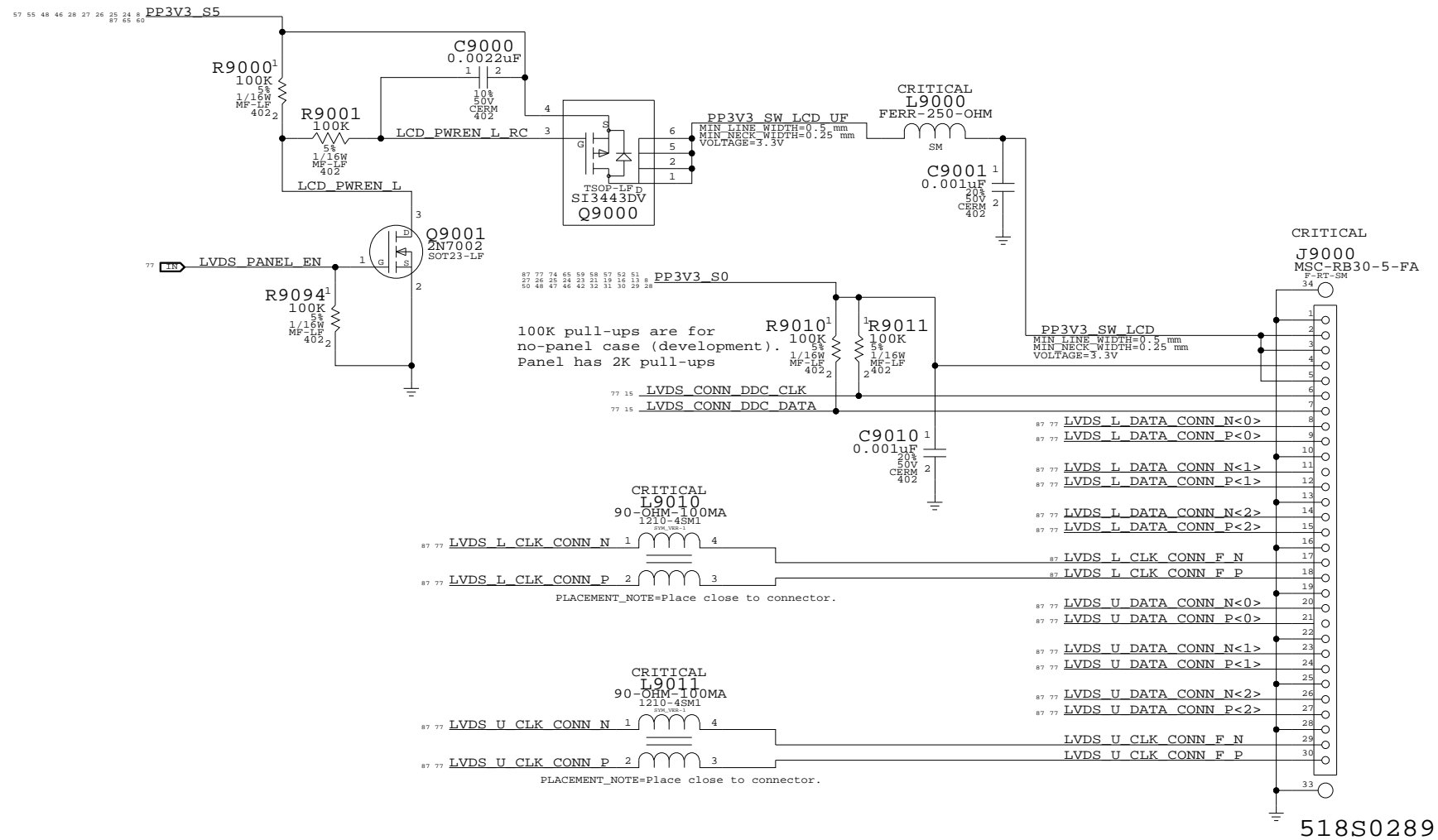
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LCD (LVDS) INTERFACE



LVDS Display Connector

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SYNC_DATE= (MASTER)

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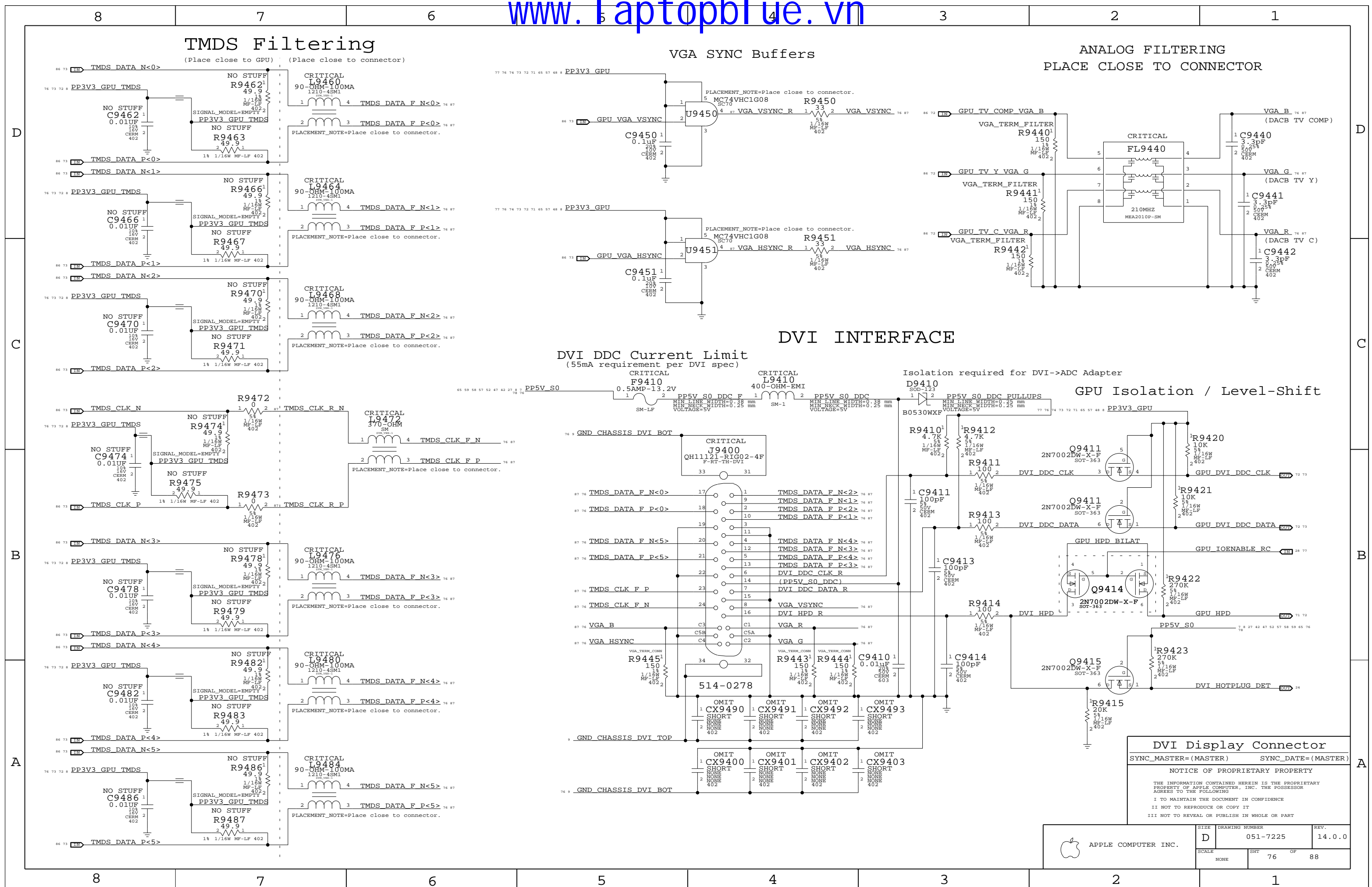
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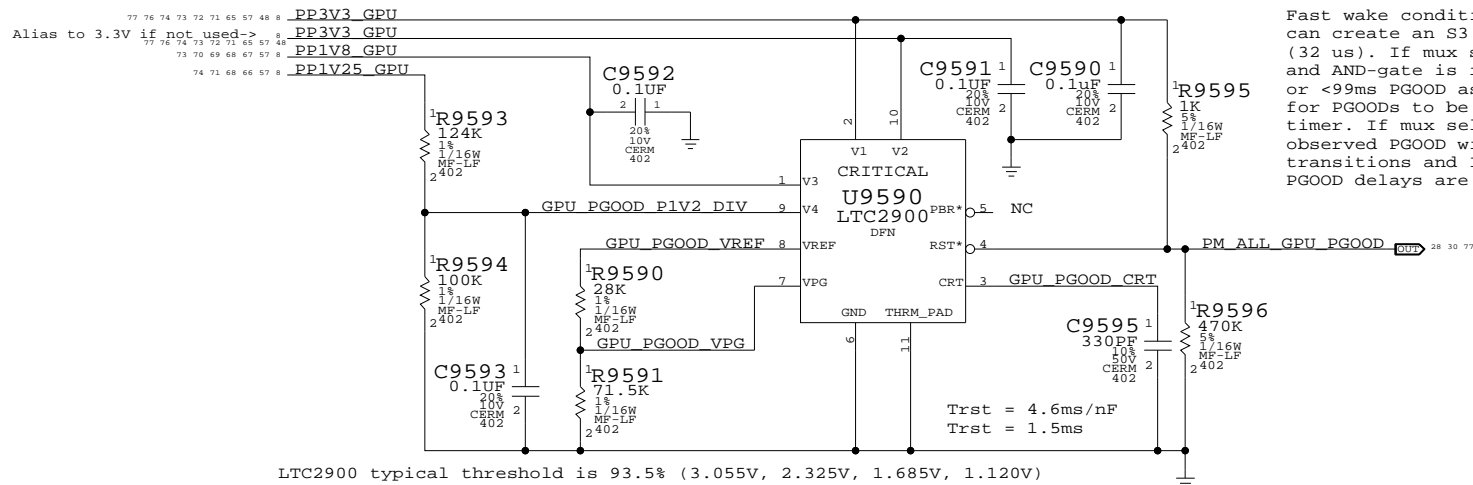
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NONE		75	88



PGOOD Monitor for GPU Rails

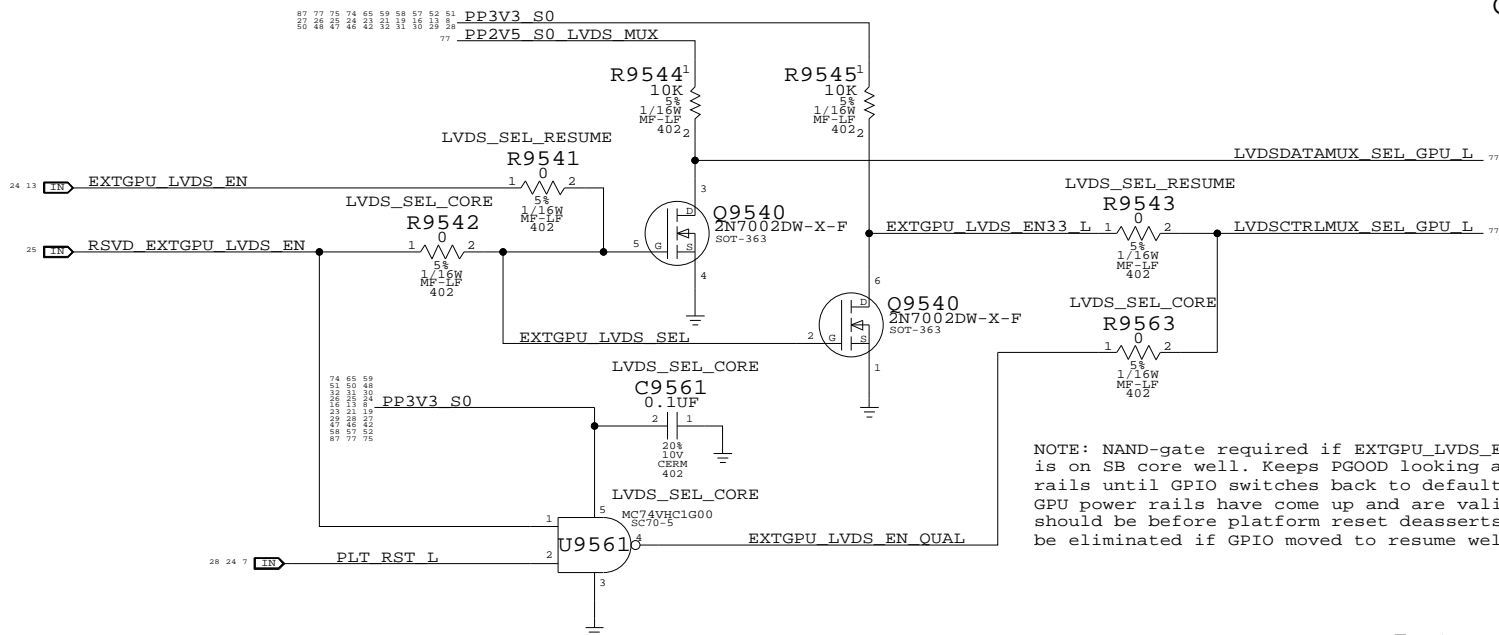
LTC2900 provides programmable reset delay which is required to play nice with ICHx PGOOD circuit



Fast wake condition is worst case. ICHx can create an S3 duration of 1 RTC clock (32 us). If mux select is on core well and AND-gate is implemented, glitch filter or <99ms PGOOD assertion time is required for PGOODs to be valid at end of 99 ms SMC timer. If mux select on resume well, then observed PGOOD will not change during S3 transitions and ICHx will honor whatever PGOOD delays are provided.

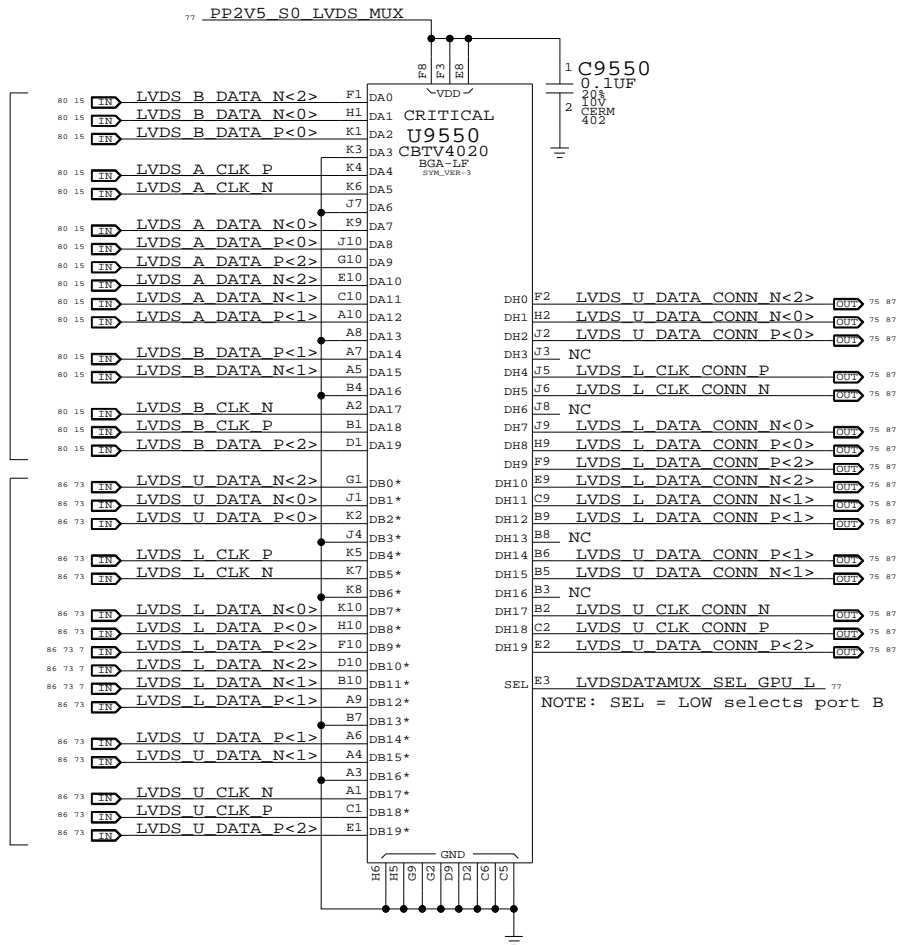
NB LVDS I/F

Mux Select Conditioning

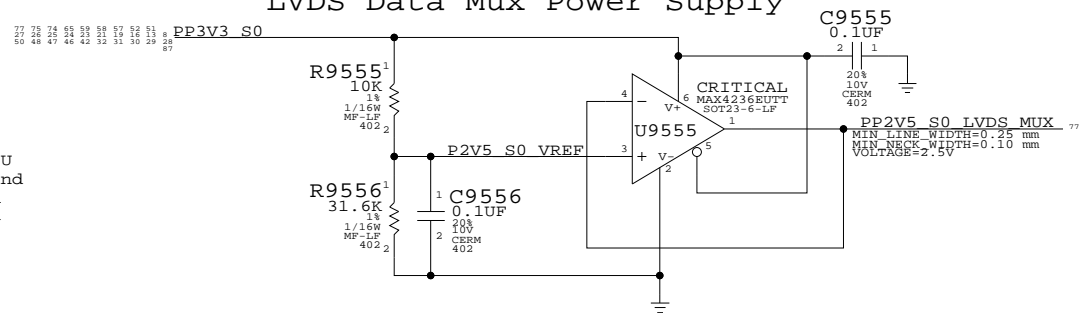


GPU LVDS I/F

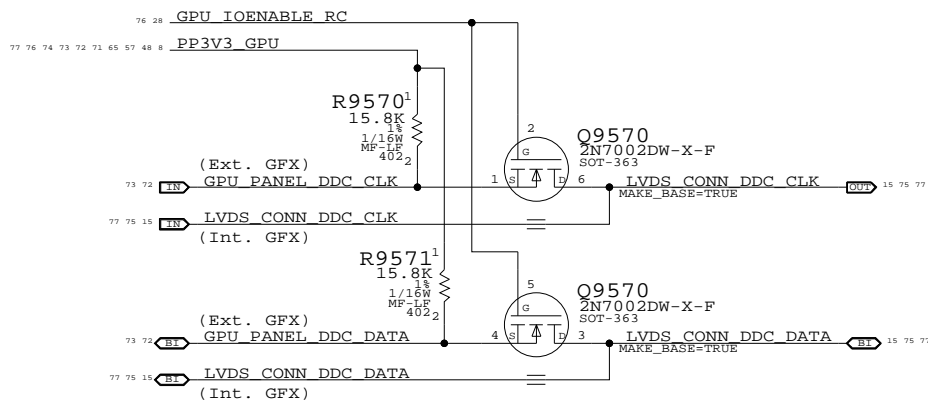
LVDS I/F Mux



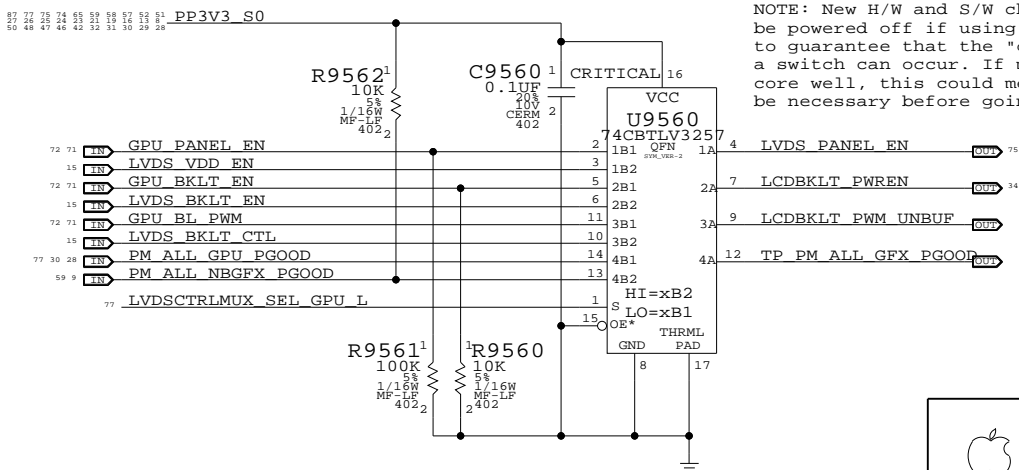
LVDS Data Mux Power Supply



GPU DDC Pass FETs



Panel/Backlight Control Mux



NOTE: New H/W and S/W challenge since NB gfx might be powered off if using external GPU. S/W will have to guarantee that the "other" device is ready before a switch can occur. If mux select GPIO is still on a core well, this could mean powering up IG supply will be necessary before going to sleep to keep PGOODs valid.

LVDS Interface Mux

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NONE	77	88

D

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR	*	=3:1_SPACING	?
FSB_ADDR2ADDR	*	=2:1_SPACING	?
FSB_ADSTB	*	=3:1_SPACING	?
FSB_ADDR2ADSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_COMMON	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended. Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs. Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs. DSTB complementary pairs are spaced 1:1 and routed as differential pairs.

Design Guide recommends each strobe/signal group is routed on the same layer. Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1. NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_2TO1	*	=2:1_SPACING	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

Most CPU signals with impedance requirements are 55-ohm single-ended. Some signals require 27.4-ohm single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target differential impedance.

DG recommends at least 25 mils, >50 mils preferred

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CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
FSB_COMMON	FSB_55S	FSB_COMMON	FSB ADS L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB BNR L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB BPRI L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB BREQ0 L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB DBSY L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB DEFER L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB DPWR L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB DRDY L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB HIT L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB HITM L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB LOCK L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB RS L<2..0>	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB TRDY L	10 14
FSB_CPURST_L	FSB_55S	FSB_COMMON	FSB CPURST L	7 10 13 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB D L<15..0>	7 10 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB DINV L<0>	7 10 14
FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<0>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<0>	7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB D L<31..16>	7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB DINV L<1>	7 10 14
FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<1>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<1>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB D L<47..32>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB DINV L<2>	7 10 14
FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<2>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<2>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB D L<63..48>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB DINV L<3>	7 10 14
FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<3>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<3>	7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB A L<16..3>	7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB REQ L<4..0>	7 10 14
FSB_ADSTB0	FSB_55S	FSB_ADSTB	FSB ADSTB L<0>	7 10 14
FSB_ADDR_GROUP1	FSB_55S	FSB_ADDR	FSB A L<35..17>	7 10 14
FSB_ADSTB1	FSB_55S	FSB_ADSTB	FSB ADSTB L<1>	7 10 14
CPU_IERR_L	CPU_55S		CPU IERR L	10
CPU_FERR_L	CPU_55S		CPU FERR L	10 23
CPU_PROCHOT_L	CPU_55S	CPU_2TO1	CPU PROCHOT L	10 46 58
CPU_PWRGD	CPU_55S		CPU PWRGD	7 10 13 23
CPU_FROM_SB	CPU_55S		CPU INTR	10 23
CPU_FROM_SB	CPU_55S		CPU NMI	10 23
CPU_FROM_SB	CPU_55S		CPU A20M L	10 23
CPU_FROM_SB	CPU_55S		CPU DPSLP L	7 10 23
CPU_FROM_SB	CPU_55S		CPU IGNNE L	10 23
CPU_INIT_L	CPU_55S		CPU INIT L	10 23 47
CPU_FROM_SB	CPU_55S		CPU SMI L	10 23
CPU_FROM_SB	CPU_55S		CPU STPCLK L	7 10 33
PM_THRMTRIP_L	CPU_55S	CPU_2TO1	PM THRMTRIP L	10 16 23 46
FSB_CPUSLP_L	CPU_55S		FSB CPUSLP L	7 10 14
PM_DPRSLEVR	CPU_55S	CPU_2TO1	PM DPRSLPVR	7 16 25 58
(See above)	CPU_55S	CPU_2TO1	IMVP DPRSLPVR	7 58
CPU_BSEL0	CPU_55S	CPU_2TO1	CPU BSEL<0>	10 30
(See above)	CPU_55S	CPU_2TO1	NB BSEL<0>	13 16 30
CPU_BSEL1	CPU_55S	CPU_2TO1	CPU BSEL<1>	10 30
(See above)	CPU_55S	CPU_2TO1	NB BSEL<1>	13 16 30
CPU_BSEL2	CPU_55S	CPU_2TO1	CPU BSEL<2>	10 30
(See above)	CPU_55S	CPU_2TO1	NB BSEL<2>	13 16 30
CPU_DPRSTP_L	CPU_55S	CPU_2TO1	CPU DPRSTP L	7 10 16 23 58
CPU_GTLREF	CPU_55S	CPU_GTLREF	CPU GTLREF	10
CPU_COMP	CPU_55S	CPU_COMP	CPU COMP<3>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<2>	10
CPU_COMP	CPU_55S	CPU_COMP	CPU COMP<1>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<0>	10
XDP_TDI	CPU_55S	CPU_ITP	XDP TDI	10 13
XDP_TDO	CPU_55S	CPU_ITP	XDP TDO	10 13
XDP_TMS	CPU_55S	CPU_ITP	XDP TMS	10 13
XDP_TCK	CPU_55S	CPU_ITP	XDP TCK	10 13
XDP_TRST_L	CPU_55S	CPU_ITP	XDP TRST L	10 13
XDP_BPM_L	CPU_55S	CPU_ITP	XDP BPM L<4..0>	10 13
XDP_BPM_L5	CPU_55S	CPU_ITP	XDP BPM L<5>	10 13
CLK_FSB_100D	CLK_FSB		XDP CLK P	13 29 30 84
CLK_FSB_100D	CLK_FSB		XDP CLK N	13 29 30 84
(FSB_CPURST_L)	CPU_55S	CPU_ITP	XDP CPURST L	13
	CPU_55S	CPU_2TO1	CPU VID<6..0>	11 12
	CPU_55S	CPU_2TO1	IMVP6 VID<6..0>	7 12 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE_P	11 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE_N	11 58
	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN_P	58
	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN_N	58

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CPU/FSB Constraints

SYNC_MASTER=T9_NAME SYNC_DATE=01/17/2007

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SIZE

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DRAWING NUMBER

051-7225

REV.

14.0.0

SCALE

NONE

SHT

79

OF

88

D

PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	20 MIL	?
DMI	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 7.2, 9.2 & 10.5

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CRT_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LVDS	*	20 MIL	?
CRT	*	25 MIL	?
CRT_2CRT	*	20 MIL	?
CRT_SYNC	*	25 MIL	?
CRT_SYNC2SYNC	*	20 MIL	?
TVDAC	*	25 MIL	?
TVDAC_2TVDAC	*	20 MIL	?

DG Says 40 mil spacing minimum

DG Says 30 mil spacing minimum

DG Says 40 mil spacing minimum

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT
CRT_SYNC	CRT_SYNC	*	CRT_SYNC2SYNC
TVDAC	TVDAC	*	TVDAC_2TVDAC

LVDS signals are 100-ohm +/- 20% differential impedance.
CRT & TVDAC signal single-ended impedance varies by location:
- 37.5-ohm +/- 15% from GMCH to first termination resistor.
- 50-ohm +/- 15% from first to second termination resistor.
- 55-ohm +/- 15% from second termination resistor to connector.
CRT_HSYNC/CRT_VSYNC signals are 55-ohm +/- 15% single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 8.1 - 8.3.

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ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
PEG_R2D	PCIE_100D	PCIE	PEG R2D P<15..0> 56
	PCIE_100D	PCIE	PEG R2D N<15..0> 56
	PCIE_100D	PCIE	PEG R2D_C P<15..0> 15 56
	PCIE_100D	PCIE	PEG R2D_C_N<15..0> 15 56
PEG_D2R	PCIE_100D	PCIE	PEG D2R P<15..0> 15 56
	PCIE_100D	PCIE	PEG D2R N<15..0> 15 56
	PCIE_100D	PCIE	PEG D2R_C P<15..0> 56
	PCIE_100D	PCIE	PEG D2R_C_N<15..0> 56
DMI_N2S	DMI_100D	DMI	DMI N2S P<3..0> 16 24
	DMI_100D	DMI	DMI N2S N<3..0> 16 24
DMI_S2N	DMI_100D	DMI	DMI S2N P<3..0> 16 24
	DMI_100D	DMI	DMI S2N N<3..0> 16 24
LVDS_A_CLK	LVDS_100D	LVDS	LVDS A CLK P 15 77
LVDS_A_CLK	LVDS_100D	LVDS	LVDS A CLK N 15 77
LVDS_A_DATA	LVDS_100D	LVDS	LVDS A DATA P<2..0> 15 77
LVDS_A_DATA	LVDS_100D	LVDS	LVDS A DATA N<2..0> 15 77
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS A DATA P<3>
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS A DATA N<3>
LVDS_B_CLK	LVDS_100D	LVDS	LVDS B CLK P 15 77
LVDS_B_CLK	LVDS_100D	LVDS	LVDS B CLK N 15 77
LVDS_B_DATA	LVDS_100D	LVDS	LVDS B DATA P<2..0> 15 77
LVDS_B_DATA	LVDS_100D	LVDS	LVDS B DATA N<2..0> 15 77
LVDS_B_DATA3	LVDS_100D	LVDS	LVDS B DATA P<3>
LVDS_B_DATA3	LVDS_100D	LVDS	LVDS B DATA N<3>
LVDS_IBG		LVDS	LVDS IBG 15 22
CRT_TVO_IREF		CRT	CRT TVO IREF
CRT_RED	CRT_50S	CRT	CRT RED
CRT_GREEN	CRT_50S	CRT	CRT GREEN
CRT_BLUE	CRT_50S	CRT	CRT BLUE
CRT_SYNC	CRT_55S	CRT_SYNC	CRT HSYNC R
CRT_SYNC	CRT_55S	CRT_SYNC	CRT VSYNC R
TV_A_DAC	CRT_50S	TVDAC	TV A DAC
TV_B_DAC	CRT_50S	TVDAC	TV B DAC
TV_C_DAC	CRT_50S	TVDAC	TV C DAC

NB Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

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8		7		6		5		4		3		2		1	
DDR2 Memory Bus Constraints															
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
MEM_45S		*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD							
MEM_55S		*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD							
MEM_70D		*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF							
MEM_85D		*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF							
SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT	NET_SPACING_TYPE1				NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET				
MEM_CLK2MEM		*	=4:1_SPACING	?	MEM_CLK				MEM_CLK	*	MEM_CLK2MEM				
MEM_CTRL2CTRL		*	=2:1_SPACING	?	MEM_CLK				MEM_CTRL	*	MEM_CLK2MEM				
MEM_CTRL2MEM		*	=3:1_SPACING	?	MEM_CLK				MEM_CMD	*	MEM_CLK2MEM				
MEM_CMD2CMD		*	=1.5:1_SPACING	?	MEM_CLK				MEM_DATA	*	MEM_CLK2MEM				
MEM_CMD2MEM		*	=3:1_SPACING	?	MEM_CLK				MEM_DQS	*	MEM_CLK2MEM				
MEM_DATA2DATA		*	=1.5:1_SPACING	?	NET_SPACING_TYPE1				NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET				
MEM_DATA2MEM		*	=3:1_SPACING	?	MEM_CMD				MEM_CLK	*	MEM_CMD2MEM				
MEM_DQS2MEM		*	=3:1_SPACING	?	MEM_CMD				MEM_CTRL	*	MEM_CMD2MEM				
MEM_2OTHER		*	25 MIL	?	MEM_CMD				MEM_CMD	*	MEM_CMD2CMD				
					MEM_CMD				MEM_DATA	*	MEM_CMD2MEM				
					MEM_CMD				MEM_DQS	*	MEM_CMD2MEM				
NET_SPACING_TYPE1		NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	MEM_CTRL				MEM_CLK	*	MEM_CTRL2MEM				
					MEM_CTRL				MEM_CTRL	*	MEM_CTRL2CTRL				
					MEM_CTRL				MEM_CMD	*	MEM_CTRL2MEM				
					MEM_CTRL				MEM_DATA	*	MEM_CTRL2MEM				
					MEM_CTRL				MEM_DQS	*	MEM_CTRL2MEM				
NET_SPACING_TYPE1		NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	MEM_DATA				MEM_CLK	*	MEM_DATA2MEM				
					MEM_DATA				MEM_CTRL	*	MEM_DATA2MEM				
					MEM_DATA				MEM_CMD	*	MEM_DATA2MEM				
					MEM_DATA				MEM_DATA	*	MEM_DATA2DATA				
					MEM_DATA				MEM_DQS	*	MEM_DATA2MEM				
NET_SPACING_TYPE1		NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	MEM_DQS				MEM_CLK	*	MEM_DQS2MEM				
					MEM_DQS				MEM_CTRL	*	MEM_DQS2MEM				
					MEM_DQS				MEM_CMD	*	MEM_DQS2MEM				
					MEM_DQS				MEM_DATA	*	MEM_DQS2MEM				
					MEM_DQS				MEM_DQS	*	MEM_DQS2MEM				
Need to support MEM_*-style wildcards!															
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2															
Memory Net Properties															
ELECTRICAL_CONSTRAINT_SET		NET_TYPE		PHYSICAL		SPACING									
MEM_A_CLK		MEM_70D	MEM_CLK	MEM_CLK	P<2..0>	16	31								
MEM_A_CLK		MEM_70D	MEM_CLK	MEM_CLK	N<2..0>	16	31								
MEM_A_CNTRL		MEM_45S	MEM_CTRL	MEM_CTRL	MEM_CKE<1..0>	16	31	33							
MEM_A_CNTRL		MEM_45S	MEM_CTRL	MEM_CTRL	MEM_CS L<1..0>	16	31	33							
MEM_A_CNTRL		MEM_45S	MEM_CTRL	MEM_CTRL	MEM_ODT<1..0>	16	31	33							
MEM_A_CMD		MEM_55S	MEM_CMD	MEM_CMD	MEM_A A<14..0>	16	17	31	33						
MEM_A_CMD		MEM_55S	MEM_CMD	MEM_CMD	MEM_A BS<2..0>	17	31	33							
MEM_A_CMD		MEM_55S	MEM_CMD	MEM_CMD	MEM_A RAS L	17	31	33							
MEM_A_CMD		MEM_55S	MEM_CMD	MEM_CMD	MEM_A CAS L	17	31	33							
MEM_A_CMD		MEM_55S	MEM_CMD	MEM_CMD	MEM_A WE L	17	31	33							
MEM_A_DQ_BYTE0		MEM_55S	MEM_DATA	MEM_DATA	MEM A DQ<7..0>	17	31								
MEM_A_DQ_BYTE1		MEM_55S	MEM_DATA	MEM_DATA	MEM A DQ<15..8>	17	31								
MEM_A_DQ_BYTE2		MEM_55S	MEM_DATA	MEM_DATA	MEM A DQ<23..16>	17	31								
MEM_A_DQ_BYTE3		MEM_55S	MEM_DATA	MEM_DATA	MEM A DQ<31..24>	17	31								
MEM_A_DQ_BYTE4		MEM_55S	MEM_DATA	MEM_DATA	MEM A DQ<39..32>	17	31								
MEM_A_DQ_BYTE5		MEM_55S	MEM_DATA	MEM_DATA	MEM A DQ<47..40>	17	31								
MEM_A_DQ_BYTE6		MEM_55S	MEM_DATA	MEM_DATA	MEM A DQ<55..48>	17	31								
MEM_A_DQ_BYTE7		MEM_55S	MEM_DATA	MEM_DATA	MEM A DQ<63..56>	17	31								
MEM_A_DM0		MEM_55S	MEM_DATA	MEM_DATA	MEM A DM<0>	17	31								
MEM_A_DM1		MEM_55S	MEM_DATA	MEM_DATA	MEM A DM<1>	17	31								
MEM_A_DM2		MEM_55S	MEM_DATA	MEM_DATA	MEM A DM<2>	17	31								
MEM_A_DM3		MEM_55S	MEM_DATA	MEM_DATA	MEM A DM<3>	17	31								
MEM_A_DM4		MEM_55S	MEM_DATA	MEM_DATA	MEM A DM<4>	17	31								
MEM_A_DM5		MEM_55S	MEM_DATA	MEM_DATA	MEM A DM<5>	17	31								
MEM_A_DM6		MEM_55S	MEM_DATA	MEM_DATA	MEM A DM<6>	17	31								
MEM_A_DM7		MEM_55S	MEM_DATA	MEM_DATA	MEM A DM<7>	17	31								
MEM_A_DQS0		MEM_85D	MEM_DQS	MEM_DQS	MEM A DQS P<0>	17	31								
MEM_A_DQS0		MEM_85D	MEM_DQS	MEM_DQS	MEM A DQS N<0>	17	31								
MEM_A_DQS1		MEM_85D	MEM_DQS	MEM_DQS	MEM A DQS P<1>	17	31								
MEM_A_DQS1		MEM_85D	MEM_DQS	MEM_DQS	MEM A DQS N<1>	17	31								
MEM_A_DQS2		MEM_85D	MEM_DQS	MEM_DQS	MEM A DQS P<2>	17	31								
MEM_A_DQS2		MEM_85D	MEM_DQS	MEM_DQS	MEM A DQS N<2>	17	31								
MEM_A_DQS3		MEM_85D	MEM_DQS	MEM_DQS	MEM A DQS P<3>	17	31								
MEM_A_DQS3		MEM_85D	MEM_DQS	MEM_DQS	MEM A DQS N<3>	17	31								
MEM_A_DQS4		MEM_85D	MEM_DQS	MEM_DQS	MEM A DQS P<4>	17	31								
MEM_A_DQS4		MEM_85D	MEM_DQS	MEM_DQS	MEM A DQS N<4>	17	31								
MEM_A_DQS5		MEM_85D	MEM_DQS	MEM_DQS	MEM A DQS P<5>	17	31								
MEM_A_DQS5		MEM_85D	MEM_DQS	MEM_DQS	MEM A DQS N<5>	17	31								
MEM_A_DQS6		MEM_85D	MEM_DQS	MEM_DQS	MEM A DQS P<6>	17	31								
MEM_A_DQS6		MEM_85D	MEM_DQS	MEM_DQS	MEM A DQS N<6>	17	31								
MEM_A_DQS7		MEM_85D	MEM_DQS	MEM_DQS	MEM A DQS P<7>	17	31								
MEM_A_DQS7		MEM_85D	MEM_DQS	MEM_DQS	MEM A DQS N<7>	17	31								
MEM_B_CLK		MEM_70D	MEM_CLK	MEM_CLK	P<5..3>	16	32								
MEM_B_CLK		MEM_70D	MEM_CLK	MEM_CLK	N<5..3>	16	32								
MEM_B_CNTRL		MEM_45S	MEM_CTRL	MEM_CTRL	MEM_CKE<4..3>	16	32	33							
MEM_B_CNTRL		MEM_45S	MEM_CTRL	MEM_CTRL	MEM_CS L<3..2>	16	32	33							
MEM_B_CNTRL		MEM_45S	MEM_CTRL	MEM_CTRL	MEM_ODT<3..2>	16	32	33							
MEM_B_CMD		MEM_55S	MEM_CMD	MEM_CMD	MEM B A<14..0>	16	17	32	33						
MEM_B_CMD		MEM_55S	MEM_CMD	MEM_CMD	MEM B BS<2..0>	17	32	33							
MEM_B_CMD		MEM_55S	MEM_CMD	MEM_CMD	MEM B RAS L	17	32	33							
MEM_B_CMD		MEM_55S	MEM_CMD	MEM_CMD	MEM B CAS L	17	32	33							
MEM_B_CMD		MEM_55S	MEM_CMD	MEM_CMD	MEM B WE L	17	32	33							
MEM_B_DQ_BYTE0		MEM_55S	MEM_DATA	MEM_DATA	MEM B DQ<7..0>	17	32								
MEM_B_DQ_BYTE1		MEM_55S	MEM_DATA	MEM_DATA	MEM B DQ<15..8>	17	32								
MEM_B_DQ_BYTE2		MEM_55S	MEM_DATA	MEM_DATA	MEM B DQ<23..16>	17	32								
MEM_B_DQ_BYTE3		MEM_55S	MEM_DATA	MEM_DATA	MEM B DQ<31..24>	17	32								
MEM_B_DQ_BYTE4		MEM_55S	MEM_DATA	MEM_DATA	MEM B DQ<39..32>	17	32								
MEM_B_DQ_BYTE5		MEM_55S	MEM_DATA	MEM_DATA	MEM B DQ<47..40>	17	32								
MEM_B_DQ_BYTE6		MEM_55S	MEM_DATA	MEM_DATA	MEM B DQ<55..48>	17	32								
MEM_B_DQ_BYTE7		MEM_55S	MEM_DATA	MEM_DATA	MEM B DQ<63..56>	17	32								
MEM_B_DM0		MEM_55S	MEM_DATA	MEM_DATA	MEM B DM<0>	17	32								
MEM_B_DM1		MEM_55S	MEM_DATA	MEM_DATA	MEM B DM<1>	17	32								
MEM_B_DM2		MEM_55S	MEM_DATA	MEM_DATA	MEM B DM<2>	17	32								
MEM_B_DM3		MEM_55S	MEM_DATA	MEM_DATA	MEM B DM<3>	17	32								
MEM_B_DM4		MEM_55S	MEM_DATA	MEM_DATA	MEM B DM<4>	17	32								
MEM_B_DM5		MEM_55S	MEM_DATA	MEM_DATA	MEM B DM<5>	17	32								
MEM_B_DM6		MEM_55S	MEM_DATA	MEM_DATA	MEM B DM<6>	17	32								
MEM_B_DM7		MEM_55S	MEM_DATA	MEM_DATA	MEM B DM<7>	17	32								
MEM_B_DQS0		MEM_85D	MEM_DQS	MEM_DQS	MEM B DQS P<0>	17	32								
MEM_B_DQS0		MEM_85D	MEM_DQS	MEM_DQS	MEM B DQS N<0>	17	32								
MEM_B_DQS1		MEM_85D	MEM_DQS	MEM_DQS	MEM B DQS P<1>	17	32								
MEM_B_DQS1		MEM_85D	MEM_DQS	MEM_DQS	MEM B DQS N<1>	17	32								
MEM_B_DQS2		MEM_85D	MEM_DQS	MEM_DQS	MEM B DQS P<2>	17	32								
MEM_B_DQS2		MEM_85D	MEM_DQS	MEM_DQS	MEM B DQS N<2>	17	32								
MEM_B_DQS3		MEM_85D	MEM_DQS	MEM_DQS	MEM B DQS P<3>	17	32								
MEM_B_DQS3		MEM_85D	MEM_DQS	MEM_DQS	MEM B DQS N<3>	17	32								
MEM_B_DQS4		MEM_85D	MEM_DQS	MEM_DQS	MEM B DQS P<4>	17	32								
MEM_B_DQS4		MEM_85D	MEM_DQS	MEM_DQS	MEM B DQS N<4>	17	32								
MEM_B_DQS5		MEM_85D	MEM_DQS	MEM_DQS	MEM B DQS P<5>	17	32								
MEM_B_DQS5		MEM_85D	MEM_DQS	MEM_DQS	MEM B DQS N<5>	17	32								
MEM_B_DQS6		MEM_85D	MEM_DQS	MEM_DQS	MEM B DQS P<6>	17	32								
MEM_B_DQS6		MEM_85D	MEM_DQS	MEM_DQS	MEM B DQS N<6>	17	32								
MEM_B_DQS7		MEM_85D	MEM_DQS	MEM_DQS	MEM B DQS P<7>	17	32								
MEM_B_DQS7		MEM_85D	MEM_DQS	MEM_DQS	MEM B DQS N<7>	17	32								
Memory Constraints															
SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007															
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Disk Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IDE_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
IDE	*	=1.8:1_SPACING	?
SATA	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.7 & 10.9

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=1.8:1_SPACING	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_60S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	20 MIL	?
USB_2CLK	*	25 MIL	?

DG says minimum spacing 50 mils to clocks

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 10.13.2

Internal Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=3:1_SPACING	?
SPI	*	=1.8:1_SPACING	?

SOURCE: Santa Platform DG, Rev 1.0 (#21112), Section 10.17

B

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ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
IDE_PDD	IDE_55S	IDE	IDE_PDD<15..0> 23 42
IDE_PDA	IDE_55S	IDE	IDE_PDA<2..0> 23 42
IDE_PDCS	IDE_55S	IDE	IDE_PDCS1_L 23 42
IDE_PDCS	IDE_55S	IDE	IDE_PDCS3_L 23 42
IDE_CNVL	IDE_55S	IDE	IDE_PDIOW_L 23 42
IDE_PDIOR_L	IDE_55S	IDE	IDE_PDIOR_L 23 42
IDE_CNVL	IDE_55S	IDE	IDE_PDDACK_L 23 42
IDE_CNVL	IDE_55S	IDE	IDE_PDDREO 23 42
IDE_PDIOVDY	IDE_55S	IDE	IDE_PDIOVDY 23 42
IDE_IRQ14	IDE_55S	IDE	IDE_IRQ14 23 42
IDE_RST_L	IDE_55S	IDE	ODD_RST_5VTOL_L 24 42
SATA_A_R2D	SATA_100D	SATA	SATA_A_R2D_C_P 23 78
SATA_100D	SATA		SATA_A_R2D_C_N 23 78
SATA_100D	SATA		SATA_A_R2D_P 78
SATA_100D	SATA		SATA_A_R2D_N 78
SATA_A_D2R	SATA_100D	SATA	SATA_A_D2R_P 23 78
SATA_100D	SATA		SATA_A_D2R_N 23 78
SATA_100D	SATA		SATA_A_D2R_C_P 78
SATA_100D	SATA		SATA_A_D2R_C_N 78
SATA_B_R2D	SATA_100D	SATA	TP_SATA_B_R2DP 23 42
SATA_100D	SATA		TP_SATA_B_R2DN 23 42
SATA_100D	SATA		SATA_B_R2D_P 23 42
SATA_100D	SATA		SATA_B_R2D_N 23 42
SATA_B_D2R	SATA_100D	SATA	TP_SATA_B_D2RP 23 42
SATA_100D	SATA		TP_SATA_B_D2RN 23 42
SATA_100D	SATA		SATA_B_D2R_C_P 23 42
SATA_100D	SATA		SATA_B_D2R_C_N 23 42
SATA_C_R2D	SATA_100D	SATA	TP_SATA_C_R2DP 23 42
SATA_100D	SATA		TP_SATA_C_R2DN 23 42
SATA_100D	SATA		SATA_C_R2D_P 23 42
SATA_100D	SATA		SATA_C_R2D_N 23 42
SATA_C_D2R	SATA_100D	SATA	TP_SATA_C_D2RP 23 42
SATA_100D	SATA		TP_SATA_C_D2RN 23 42
SATA_100D	SATA		SATA_C_D2R_C_P 23 42
SATA_100D	SATA		SATA_C_D2R_C_N 23 42
SATA_RB1AS	SATA_55S		SATA_RB1AS 23 42
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK 23 34
HDA_55S	HDA		HDA_BIT_CLK_R 23
HDA_SYNC	HDA_55S	HDA	HDA_SYNC 23 34
HDA_55S	HDA		HDA_SYNC_R 23
HDA_RST_L	HDA_55S	HDA	HDA_RST_L 23 34
HDA_55S	HDA		HDA_RST_L_R 23
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0 23 34
HDA_55S	HDA		HDA_SDIN_CODEC 23
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT 23 34
HDA_55S	HDA		HDA_SDOUT_R 23
USB_EXT_A	USB_90D	USB	USB_EXT_A_P 24 43
USB_90D	USB		USB_EXT_A_N 24 43
USB_90D	USB		USB_EXT_A_MUXED_P 24 43
USB_90D	USB		USB_EXT_A_MUXED_N 24 43
USB_MINI	USB_90D	USB	USB_MINI_P 24 34
USB_90D	USB		USB_MINI_N 24 34
USB_EXT_D	USB_90D	USB	USB_WWAN_P 7 24 44
USB_90D	USB		USB_WWAN_N 7 24 44
USB_CAMERA	USB_90D	USB	USB_CAMERA_P 7 24 44
USB_90D	USB		USB_CAMERA_N 7 24 44
USB_BT	USB_90D	USB	USB_BT_P 24 78
USB_90D	USB		USB_BT_N 24 78
USB_TPAD	USB_90D	USB	USB_TPAD_P 24 78
USB_90D	USB		USB_TPAD_N 24 78
USB_IR	USB_90D	USB	USB_IR_P 24 78
USB_90D	USB		USB_IR_N 24 78
USB_EXTB	USB_90D	USB	USB_EXTB_P 24 34
USB_90D	USB		USB_EXTB_N 24 34
USB_EXCARD	USB_90D	USB	USB_EXCARD_P 24 34
USB_90D	USB		USB_EXCARD_N 24 34
USB_EXTC	USB_90D	USB	TP_USB_EXTCP 9 24
USB_90D	USB		TP_USB_EXTCN 9 24
USB_RB1AS	USB_60S		USB_RB1AS 24
SMB_SB_SCL	SMB_55S	SMB	SMBUS_SB_SCL 25 29 31 32 34 48
SMB_SB_SDA	SMB_55S	SMB	SMBUS_SB_SDA 25 29 31 32 34 48
SMB_SB_ME_SCL	SMB_55S	SMB	SMBUS_SB_ME_SCL 25 48
SMB_SB_ME_SDA	SMB_55S	SMB	SMBUS_SB_ME_SDA 25 48
SPI_SCLK	SPI_55S	SPI	SPI_SCLK_R 24 55
SPI_55S	SPI		SPI_SCLK 55
SPI_55S	SPI		SPI_A_SCLK_R 55
SPI_55S	SPI		SPI_B_SCLK_R 55
SPI_SI	SPI_55S	SPI	SPI_SI_R 24 55
SPI_55S	SPI		SPI_SI 55
SPI_55S	SPI		SPI_A_SI_R 55
SPI_55S	SPI		SPI_B_SI_R 55
SPI_SO	SPI_55S	SPI	SPI_SO 24 55
SPI_55S	SPI		SPI_A_SO_R 55
SPI_55S	SPI		SPI_B_SO_R 55
SPI_CE_L0	SPI_55S	SPI	SPI_CE_R_L<0> 24 55
SPI_55S	SPI		SPI_CE_L<0> 55
SPI_CE_L1	SPI_55S	SPI	SPI_CE_R_L<1>
SPI_55S	SPI		SPI_CE_L<1>

SB Constraints (1 of 2)

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

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051-7225

REV.

14.0.0

SCALE

NONE

SHT

82

OF

88

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=2:1_SPACING	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.18.1 & 10.19

Controller Link (AMT) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLINK_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLINK_12MIL	*	=STANDARD	12 MILS	5 MILS	300 MILS	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLINK	*	=1.8:1_SPACING	?
CLINK_VREF	*	12 MILS	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

Ethernet (Yukon) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MILS	?

SOURCE: Based on Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
PCI_AD	PCI_55S	PCI	PCI AD<18..0> 24 38
PCI_AD19	PCI_55S	PCI	PCI AD<19> 24 38
PCI_AD20	PCI_55S	PCI	PCI AD<20> 24 38
PCI_AD	PCI_55S	PCI	PCI AD<31..21> 24 38
PCI_AD	PCI_55S	PCI	PCI PAR 24 38
PCI_C_BE_L	PCI_55S	PCI	PCI C_BE_L<3..0> 24 38
PCI_CNTRL	PCI_55S	PCI	PCI IRDY_L 24 38
PCI_CNTRL	PCI_55S	PCI	PCI DEVSEL_L 24 38
PCI_CNTRL	PCI_55S	PCI	PCI PERR_L 24 38
PCI_LOCK_L	PCI_55S	PCI	PCI LOCK_L 24
PCI_CNTRL	PCI_55S	PCI	PCI SERR_L 24 38
PCI_CNTRL	PCI_55S	PCI	PCI STOP_L 24 38
PCI_CNTRL	PCI_55S	PCI	PCI TRDY_L 24 38
PCI_CNTRL	PCI_55S	PCI	PCI FRAME_L 24 38
PCI_FW_REQ_L	PCI_55S	PCI	PCI FW_REQ_L 24 38
PCI_FW_GNT_L	PCI_55S	PCI	PCI FW_GNT_L 7 24 38 47
PCI_REQ1_L	PCI_55S	PCI	PCI REQ1_L 24
PCI_GNT1_L	PCI_55S	PCI	PCI GNT1_L 24
PCI_REQ2_L	PCI_55S	PCI	PCI REQ2_L 24
PCI_GNT2_L	PCI_55S	PCI	PCI GNT2_L 24
INT_PIRQA_L	PCI_55S	PCI	INT PIRQA_L 24
INT_PIRQB_L	PCI_55S	PCI	INT PIRQB_L 24
INT_PIROC_L	PCI_55S	PCI	INT PIROC_L 24
INT_PIROD_L	PCI_55S	PCI	INT PIROD_L 24 38
INT_PIROE_L	PCI_55S	PCI	INT PIROE_L 24
INT_PIROF_L	PCI_55S	PCI	INT PIROF_L 24
PCIE_A_R2D	PCIE_100D	PCIE	PCIE A_R2D_C_P 24
PCIE_A_R2D	PCIE_100D	PCIE	PCIE A_R2D_C_N 24
PCIE_A_D2R	PCIE_100D	PCIE	PCIE A_D2R_P 24
PCIE_A_D2R	PCIE_100D	PCIE	PCIE A_D2R_N 24
PCIE_B_R2D	PCIE_100D	PCIE	PCIE B_R2D_C_P 24
PCIE_B_R2D	PCIE_100D	PCIE	PCIE B_R2D_C_N 24
PCIE_B_D2R	PCIE_100D	PCIE	PCIE B_D2R_P 24
PCIE_B_D2R	PCIE_100D	PCIE	PCIE B_D2R_N 24
PCIE_EXCARD_R2D	PCIE_100D	PCIE	PCIE EXCARD_R2D_C_P 24 34
PCIE_EXCARD_R2D	PCIE_100D	PCIE	PCIE EXCARD_R2D_C_N 24 34
PCIE_EXCARD_D2R	PCIE_100D	PCIE	PCIE EXCARD_D2R_P 24 34
PCIE_EXCARD_D2R	PCIE_100D	PCIE	PCIE EXCARD_D2R_N 24 34
PCIE_FW_R2D	PCIE_100D	PCIE	PCIE FW_R2D_C_P 24
PCIE_FW_R2D	PCIE_100D	PCIE	PCIE FW_R2D_C_N 24
PCIE_FW_D2R	PCIE_100D	PCIE	PCIE FW_D2R_P 24
PCIE_FW_D2R	PCIE_100D	PCIE	PCIE FW_D2R_N 24
PCIE_MINI_R2D	PCIE_100D	PCIE	PCIE MINI_R2D_C_P 24 34
PCIE_MINI_R2D	PCIE_100D	PCIE	PCIE MINI_R2D_C_N 24 34
PCIE_MINI_D2R	PCIE_100D	PCIE	PCIE MINI_D2R_P 24 34
PCIE_MINI_D2R	PCIE_100D	PCIE	PCIE MINI_D2R_N 24 34
GLAN_COMP			GLAN COMP 23
CLINK_NB	CLINK_55S	CLINK	CLINK_NB_CLK 16 25
CLINK_NB	CLINK_55S	CLINK	CLINK_NB_DATA 16 25
CLINK_NB_RESET_L	CLINK_55S	CLINK	CLINK_NB_RESET_L 16 25
CLINK_WLAN	CLINK_55S	CLINK	CLINK_WLAN_CLK 24
CLINK_WLAN	CLINK_55S	CLINK	CLINK_WLAN_DATA 24
CLINK_WLAN_RESET_L	CLINK_55S	CLINK	CLINK_WLAN_RESET_L 24
NB_CLINK_VREF	CLINK_12MIL	CLINK_VREF	NB_CLINK_VREF 16
SB_CLINK_VREF0	CLINK_12MIL	CLINK_VREF	SB_CLINK_VREF0 25
SB_CLINK_VREF1	CLINK_12MIL	CLINK_VREF	SB_CLINK_VREF1 25
PCIE_ENET_R2D	PCIE_100D	PCIE	PCIE ENET_R2D_C_P 24 35
PCIE_ENET_R2D	PCIE_100D	PCIE	PCIE ENET_R2D_C_N 24 35
PCIE_ENET_R2D	PCIE_100D	PCIE	PCIE ENET_R2D_P 35
PCIE_ENET_R2D	PCIE_100D	PCIE	PCIE ENET_R2D_N 35
PCIE_ENET_D2R	PCIE_100D	PCIE	PCIE ENET_D2R_P 24 35
PCIE_ENET_D2R	PCIE_100D	PCIE	PCIE ENET_D2R_N 24 35
PCIE_ENET_D2R	PCIE_100D	PCIE	PCIE ENET_D2R_C_P 35
PCIE_ENET_D2R	PCIE_100D	PCIE	PCIE ENET_D2R_C_N 35
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI_P<0> 35 37
ENET_100D	ENET_100D	ENET_MDI	ENET MDI_N<0> 35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI_P<1> 35 37
ENET_100D	ENET_100D	ENET_MDI	ENET MDI_N<1> 35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI_P<2> 35 37
ENET_100D	ENET_100D	ENET_MDI	ENET MDI_N<2> 35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI_P<3> 35 37
ENET_100D	ENET_100D	ENET_MDI	ENET MDI_N<3> 35 37

SB Constraints (2 of 2)

SYNC_MASTER=T9_NAME SYNC_DATE=01/17/2007

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OF

88

Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	25 MIL	?
CLK_PCIE	*	20 MIL	?
CLK_MED	*	20 MIL	?
CLK_SLOW	*	10 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 14.1 - 14.6

Clock Net Properties

NET TYPE				
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
CK505_CPUH	CLK_FSB_100D	CLK_FSB	FSB CLK CPU P	10 29 30 84
CK505_CPU	CLK_FSB_100D	CLK_FSB	FSB CLK CPU N	10 29 30 84
CK505_NB	CLK_FSB_100D	CLK_FSB	FSB CLK NB P	7 14 29 30 84
CK505_NB	CLK_FSB_100D	CLK_FSB	FSB CLK NB N	7 14 29 30 84
CK505_ITP	CLK_FSB_100D	CLK_FSB	XDP CLK P	13 29 30 79 84
CK505_ITP	CLK_FSB_100D	CLK_FSB	XDP CLK N	13 29 30 79 84
CK505_PCIF0	CLK_MED_55S	CLK_MED	CK505 PCIF0 CLK ITPEN	29 30
CK505_PCIF1	CLK_MED_55S	CLK_MED	CK505 PCIF1 CLK	29 30
CK505_PCI1	CLK_MED_55S	CLK_MED	CK505 PCI1 CLK	29 30
CK505_PCI2	CLK_MED_55S	CLK_MED	TP CK505 PCI2 CLK	29 30
CK505_PCI3	CLK_MED_55S	CLK_MED	CK505 PCI3 CLK	29 30
CK505_PCI4	CLK_MED_55S	CLK_MED	TP CK505 PCI4 CLK	29 30
CK505_PCI5	CLK_MED_55S	CLK_MED	CK505 PCI5 CLK FCTSEL	29 30
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505 48M FSA	29 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505 REF0 FSC	29 30
CK505_DOT96	CLK_PCIE_100D	CLK_PCIE	CK505 CLK27M	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505 CLK27M SS	29 30
CK505_LVDS	CLK_PCIE_100D	CLK_PCIE	NB CLK100M DPPLLSS P	7 16 22 29 30 84
	CLK_PCIE_100D	CLK_PCIE	NB CLK100M DPPLLSS N	7 16 22 29 30 84
CK505_SRC1	CLK_PCIE_100D	CLK_PCIE	PEG CLK100M GPU P	9 29 30 66 84
	CLK_PCIE_100D	CLK_PCIE	PEG CLK100M GPU N	9 29 30 66 84
CK505_SRC2	CLK_PCIE_100D	CLK_PCIE	SB CLK100M DMI P	24 29 30 84
	CLK_PCIE_100D	CLK_PCIE	SB CLK100M DMI N	24 29 30 84
CK505_SRC3	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M EXCARD P	29 30 34 84
	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M EXCARD N	29 30 34 84
CK505_SRC4	CLK_PCIE_100D	CLK_PCIE	SB CLK100M SATA P	23 29 30 84
	CLK_PCIE_100D	CLK_PCIE	SB CLK100M SATA N	23 29 30 84
CK505_SRC5	CLK_PCIE_100D	CLK_PCIE	NB CLK100M PCIE P	7 16 29 30 84
	CLK_PCIE_100D	CLK_PCIE	NB CLK100M PCIE N	7 16 29 30 84
CK505_SRC6	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M MINI P	29 30 34 84
	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M MINI N	29 30 34 84
CK505_SRC7	CLK_PCIE_100D	CLK_PCIE	TP PCIE CLK100M SRC7P	29 30
	CLK_PCIE_100D	CLK_PCIE	TP PCIE CLK100M SRC7N	29 30
CK505_SRC8	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M ENET P	29 30 35 84
	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M ENET N	29 30 35 84
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB CLK CPU P	10 29 30 84
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB CLK CPU N	10 29 30 84
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB CLK NB P	7 14 29 30 84
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB CLK NB N	7 14 29 30 84
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP CLK P	13 29 30 79 84
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP CLK N	13 29 30 79 84
(CK505_PCIF0)	CLK_MED_55S	CLK_MED	PCI CLK33M LPCPLUS	7 30 47
(CK505_PCIF1)	CLK_MED_55S	CLK_MED	PCI CLK33M_SB	24 30
(CK505_PCI1)	CLK_MED_55S	CLK_MED	PCI CLK33M_FW	30 38
(CK505_PCI2)	CLK_MED_55S	CLK_MED	PCI CLK33M TPM	
(CK505_PCI3)	CLK_MED_55S	CLK_MED	PCI CLK33M_SMC	30 45
			CK505 PCI4 is project-specific	
			CK505 PCI5 is project-specific	
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	SB CLK48M USBCTLR	25 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	SB CLK14P3M TIMER	25 30
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505 FSA	30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505 FSC	30
(CK505_DOT96)	CLK_PCIE_100D	CLK_PCIE	NB CLK96M DOT P	7
(CK505_DOT96)	CLK_PCIE_100D	CLK_PCIE	NB CLK96M DOT N	7
CK505_LVDS)	CLK_PCIE_100D	CLK_PCIE	NB CLK100M DPPLLSS P	7 16 22 29 30 84
CK505_LVDS)	CLK_PCIE_100D	CLK_PCIE	NB CLK100M DPPLLSS N	7 16 22 29 30 84
CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	PEG CLK100M GPU P	9 29 30 66 84
CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	PEG CLK100M GPU N	9 29 30 66 84
CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB CLK100M DMI P	24 29 30 84
CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB CLK100M DMI N	24 29 30 84
CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M EXCARD P	29 30 34 84
CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M EXCARD N	29 30 34 84
CK505_SRC4)	CLK_PCIE_100D	CLK_PCIE	SB CLK100M SATA P	23 29 30 84
CK505_SRC4)	CLK_PCIE_100D	CLK_PCIE	SB CLK100M SATA N	23 29 30 84
CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB CLK100M PCIE P	7 16 29 30 84
CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB CLK100M PCIE N	7 16 29 30 84
CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M MINI P	29 30 34 84
CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M MINI N	29 30 34 84
			CK505 SRC7 is project-specific	
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M ENET P	29 30 35 84
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M ENET N	29 30 35 84

SMC SMBus Net Properties

NET TYPE				
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
SMBUS_SMC_A_S3_SCL	SMB_55S	SMB	SMBUS_SMC_A_S3_SCL	45 48 51 78
SMBUS_SMC_A_S3_SDA	SMB_55S	SMB	SMBUS_SMC_A_S3_SDA	45 48 51 78
SMBUS_SMC_B_S0_SCL	SMB_55S	SMB	SMBUS_SMC_B_S0_SCL	34 45 48 51
SMBUS_SMC_B_S0_SDA	SMB_55S	SMB	SMBUS_SMC_B_S0_SDA	34 45 48 51
SMBUS_SMC_0_S0_SCL	SMB_55S	SMB	SMBUS_SMC_0_S0_SCL	45 48 51 73
SMBUS_SMC_0_S0_SDA	SMB_55S	SMB	SMBUS_SMC_0_S0_SDA	45 48 51 73
SMBUS_SMC_BSA_SCL	SMB_55S	SMB	SMBUS_SMC_BSA_SCL	7 45 48 56
SMBUS_SMC_BSA_SDA	SMB_55S	SMB	SMBUS_SMC_BSA_SDA	7 45 48 56
SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL	45 48 54
SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA	45 48 54

Clock & SMC Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

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B






















A

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW	*	=2:1_SPACING	?
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
 FW_D_CTL	FW_55S	FW	FW LINK<7..0>
 FW_D_CTL	FW_55S	FW	FW CTL<1..0>
 FW_L_CLK	CLK_MED_55S	CLK_MED	CLKFW LINK_LCLK
 FW_L_CLK	CLK_MED_55S	CLK_MED	CLKFW PHY_LCLK 38 39
 FW_P_CLK	CLK_MED_55S	CLK_MED	CLKFW LINK_PCLK 38 39
 FW_P_CLK	CLK_MED_55S	CLK_MED	CLKFW PHY_PCLK
 FW_LKON	FW_55S	FW	FW LKON
 FW_LKON	FW_55S	FW	FW LKON_R
 FW_LPS	FW_55S	FW	FW LPS 38 39
 FW_LREQ	FW_55S	FW	FW LREQ 38 39
 FW_PINT	FW_55S	FW	FW PINT 38 39
 FWPHY_CLK98P304M_XI	CLK_MED_55S	CLK_MED	CLK98P304M_FW_XI_R
 FWPHY_CLK98P304M_XI	CLK_MED_55S	CLK_MED	CLK98P304M_FW_XI
 FW_0_TPA	FW_110D	FW_TP	FW PORT0_TPA_P 39 41
 FW_0_TPA	FW_110D	FW_TP	FW PORT0_TPA_N 39 41
 FW_0_TPB	FW_110D	FW_TP	FW PORT0_TPB_P 39 41
 FW_0_TPB	FW_110D	FW_TP	FW PORT0_TPB_N 39 41
 FW_1_TPA	FW_110D	FW_TP	FW PORT1_TPA_P 39 41
 FW_1_TPA	FW_110D	FW_TP	FW PORT1_TPA_N 39 41
 FW_1_TPB	FW_110D	FW_TP	FW PORT1_TPB_P 39 41
 FW_1_TPB	FW_110D	FW_TP	FW PORT1_TPB_N 39 41
Port 2 Not Used			

FireWire Constraints

SYNC_MASTER=T9_NOME

SYNC_DATE=01/17/2007


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 APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	14.0.0
SCALE	SHT	OF
NONE	85	88

D

D

C

C

B

B

A

A

GDDR3 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR3_40R50SE	*	=50_OHM_SE	=40_OHM_SE	=50_OHM_SE	12.7 MM	=STANDARD	=STANDARD
GDDR3_50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
GDDR3_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR3_CLK	*	=2.5:1_SPACING	?
GDDR3_CMD	*	=2.5:1_SPACING	?
GDDR3_DATA	*	=2.5:1_SPACING	?
GDDR3_DQS	*	=2.5:1_SPACING	?

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TMDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
VGA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
VGA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TMDS	*	20 MIL	?
VGA	*	20 MIL	?
VGA_SYNC	*	20 MIL	?

GDDR3 FB A/B Net Properties

NET TYPE				
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
FB_A_CLK_P	GDDR3_80D	GDDR3_CLK	FB A CLK P<0>	68 69
FB_A_CLK_N	GDDR3_80D	GDDR3_CLK	FB A CLK N<0>	68 69
FB_B_CLK_P	GDDR3_80D	GDDR3_CLK	FB A CLK P<1>	68 69
FB_B_CLK_N	GDDR3_80D	GDDR3_CLK	FB A CLK N<1>	68 69
FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB A MA<1..0>	68 69
FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB A MA<11..6>	68 69
FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB A BA<2..0>	68 69
FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB A RAS_L	68 69
FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB A CAS_L	68 69
FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB A WE_L	68 69
FB_AB_CMD_PD	GDDR3_40R50SE	GDDR3_CMD	FB A CKE	68 69
FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB A CS0_L	68 69
FB_AB_CMD_PD	GDDR3_40R50SE	GDDR3_CMD	FB A DRAM_RST	68 69
FB_A_CMD	GDDR3_50SE	GDDR3_CMD	FB A LMA<5..2>	68 69
FB_B_CMD	GDDR3_50SE	GDDR3_CMD	FB A UMA<5..2>	68 69
FB_A_WDQS0	GDDR3_50SE	GDDR3_DQS	FB A WDQS<0>	68 69
FB_A_WDQS1	GDDR3_50SE	GDDR3_DQS	FB A WDQS<1>	68 69
FB_A_WDQS2	GDDR3_50SE	GDDR3_DQS	FB A WDQS<2>	68 69
FB_A_WDQS3	GDDR3_50SE	GDDR3_DQS	FB A WDQS<3>	68 69
FB_A_RDQS0	GDDR3_50SE	GDDR3_DQS	FB A RDQS<0>	68 69
FB_A_RDQS1	GDDR3_50SE	GDDR3_DQS	FB A RDQS<1>	68 69
FB_A_RDQS2	GDDR3_50SE	GDDR3_DQS	FB A RDQS<2>	68 69
FB_A_RDQS3	GDDR3_50SE	GDDR3_DQS	FB A RDQS<3>	68 69
FB_A_DQ_BYTE0	GDDR3_50SE	GDDR3_DATA	FB A DQ<7..0>	68 69
FB_A_DQ_BYTE1	GDDR3_50SE	GDDR3_DATA	FB A DQ<15..8>	68 69
FB_A_DQ_BYTE2	GDDR3_50SE	GDDR3_DATA	FB A DQ<23..16>	68 69
FB_A_DQ_BYTE3	GDDR3_50SE	GDDR3_DATA	FB A DQ<31..24>	68 69
FB_A_DQM0	GDDR3_50SE	GDDR3_DATA	FB A DQM_L<0>	68 69
FB_A_DQM1	GDDR3_50SE	GDDR3_DATA	FB A DQM_L<1>	68 69
FB_A_DQM2	GDDR3_50SE	GDDR3_DATA	FB A DQM_L<2>	68 69
FB_A_DQM3	GDDR3_50SE	GDDR3_DATA	FB A DQM_L<3>	68 69
FB_B_WDQS0	GDDR3_50SE	GDDR3_DQS	FB A WDQS<4>	68 69
FB_B_WDQS1	GDDR3_50SE	GDDR3_DQS	FB A WDQS<5>	68 69
FB_B_WDQS2	GDDR3_50SE	GDDR3_DQS	FB A WDQS<6>	68 69
FB_B_WDQS3	GDDR3_50SE	GDDR3_DQS	FB A WDQS<7>	68 69
FB_B_RDQS0	GDDR3_50SE	GDDR3_DQS	FB A RDQS<4>	68 69
FB_B_RDQS1	GDDR3_50SE	GDDR3_DQS	FB A RDQS<5>	68 69
FB_B_RDQS2	GDDR3_50SE	GDDR3_DQS	FB A RDQS<6>	68 69
FB_B_RDQS3	GDDR3_50SE	GDDR3_DQS	FB A RDQS<7>	68 69
FB_B_DQ_BYTE0	GDDR3_50SE	GDDR3_DATA	FB A DQ<39..32>	68 69
FB_B_DQ_BYTE1	GDDR3_50SE	GDDR3_DATA	FB A DQ<47..40>	68 69
FB_B_DQ_BYTE2	GDDR3_50SE	GDDR3_DATA	FB A DQ<55..48>	68 69
FB_B_DQ_BYTE3	GDDR3_50SE	GDDR3_DATA	FB A DQ<63..56>	68 69
FB_B_DQM0	GDDR3_50SE	GDDR3_DATA	FB A DQM_L<4>	68 69
FB_B_DQM1	GDDR3_50SE	GDDR3_DATA	FB A DQM_L<5>	68 69
FB_B_DQM2	GDDR3_50SE	GDDR3_DATA	FB A DQM_L<6>	68 69
FB_B_DQM3	GDDR3_50SE	GDDR3_DATA	FB A DQM_L<7>	68 69

G84M Net Properties

NET TYPE				
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
(CK505_DOT96)	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M	30
	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M_GATED	30 71 72
CK505_CLK27MSS	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M_SS	30
	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M_SS_GATED	30 71 72
	LVDS_100D	LVDS	LVDS_L_CLK_P	73 77
	LVDS_100D	LVDS	LVDS_L_CLK_N	73 77
	LVDS_100D	LVDS	LVDS_L_DATA_P<3..0>	7 73 77
	LVDS_100D	LVDS	LVDS_L_DATA_N<3..0>	7 73 77
	LVDS_100D	LVDS	LVDS_U_CLK_P	73 77
	LVDS_100D	LVDS	LVDS_U_CLK_N	73 77
	LVDS_100D	LVDS	LVDS_U_DATA_P<3..0>	73 77
	LVDS_100D	LVDS	LVDS_U_DATA_N<3..0>	73 77
TMDS_CLK	TMDS_100D	TMDS	TMDS_CLK_P	73 76
TMDS_CLK	TMDS_100D	TMDS	TMDS_CLK_N	73 76
TMDS_DATA	TMDS_100D	TMDS	TMDS_DATA_P<5..0>	73 76
TMDS_DATA	TMDS_100D	TMDS	TMDS_DATA_N<5..0>	73 76
VGA_B_TV_C	VGA_50S	VGA	GPU_TV_C_VGA_R	72 76
VGA_G_TV_Y	VGA_50S	VGA	GPU_TV_Y_VGA_G	72 76
VGA_B_TV_COMP	VGA_50S	VGA	GPU_TV_COMP_VGA_B	72 76
	VGA_50S	VGA	GPU_VGA_R	72 73
	VGA_50S	VGA	GPU_VGA_G	72 73
	VGA_50S	VGA	GPU_VGA_B	72 73
	VGA_50S	VGA	GPU_TV_C	72 73
	VGA_50S	VGA	GPU_TV_Y	72 73
	VGA_50S	VGA	GPU_TV_COMP	72 73
VGA_SYNC	VGA_55S	VGA_SYNC	GPU_VGA_HSYNC	73 76
VGA_SYNC	VGA_55S	VGA_SYNC	GPU_VGA_VSYNC	73 76

GDDR3 FB C/D Net Properties

NET TYPE				
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
FB_C_CLK_P	GDDR3_80D	GDDR3_CLK	FB B CLK P<0>	68 70
FB_C_CLK_N	GDDR3_80D	GDDR3_CLK	FB B CLK N<0>	68 70
FB_D_CLK_P	GDDR3_80D	GDDR3_CLK	FB B CLK P<1>	68 70
FB_D_CLK_N	GDDR3_80D	GDDR3_CLK	FB B CLK N<1>	68 70
FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB B MA<1..0>	68 70
FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB B MA<11..6>	68 70
FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB B BA<2..0>	68 70
FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB B RAS_L	68 70
FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB B CAS_L	68 70
FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB B WE_L	68 70
FB_CD_CMD_PD	GDDR3_40R50SE	GDDR3_CMD	FB B CKE	68 70
FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB B CS0_L	68 70
FB_CD_CMD_PD	GDDR3_40R50SE	GDDR3_CMD	FB B DRAM_RST	68 70
FB_C_CMD	GDDR3_50SE	GDDR3_CMD	FB B LMA<5..2>	68 70
FB_D_CMD	GDDR3_50SE	GDDR3_CMD	FB B UMA<5..2>	68 70
FB_C_WDQS0	GDDR3_50SE	GDDR3_DQS	FB B WDQS<0>	68 70
FB_C_WDQS1	GDDR3_50SE	GDDR3_DQS	FB B WDQS<1>	68 70
FB_C_WDQS2	GDDR3_50SE	GDDR3_DQS	FB B WDQS<2>	68 70
FB_C_WDQS3	GDDR3_50SE	GDDR3_DQS	FB B WDQS<3>	68 70
FB_C_RDQS0	GDDR3_50SE	GDDR3_DQS	FB B RDQS<0>	68 70
FB_C_RDQS1	GDDR3_50SE	GDDR3_DQS	FB B RDQS<1>	68 70
FB_C_RDQS2	GDDR3_50SE	GDDR3_DQS	FB B RDQS<2>	68 70
FB_C_RDQS3	GDDR3_50SE	GDDR3_DQS	FB B RDQS<3>	68 70
FB_C_DQ_BYTE0	GDDR3_50SE	GDDR3_DATA	FB B DQ<7..0>	68 70
FB_C_DQ_BYTE1	GDDR3_50SE	GDDR3_DATA	FB B DQ<15..8>	68 70
FB_C_DQ_BYTE2	GDDR3_50SE	GDDR3_DATA	FB B DQ<23..16>	68 70
FB_C_DQ_BYTE3	GDDR3_50SE	GDDR3_DATA	FB B DQ<31..24>	68 70
FB_C_DQM0	GDDR3_50SE	GDDR3_DATA	FB B DQM_L<0>	68 70
FB_C_DQM1	GDDR3_50SE	GDDR3_DATA	FB B DQM_L<1>	68 70
FB_C_DQM2	GDDR3_50SE	GDDR3_DATA	FB B DQM_L<2>	68 70
FB_C_DQM3	GDDR3_50SE	GDDR3_DATA	FB B DQM_L<3>	68 70
FB_D_WDQS0	GDDR3_50SE	GDDR3_DQS	FB B WDQS<4>	68 70
FB_D_WDQS1	GDDR3_50SE	GDDR3_DQS	FB B WDQS<5>	68 70
FB_D_WDQS2	GDDR3_50SE	GDDR3_DQS	FB B WDQS<6>	68 70
FB_D_WDQS3	GDDR3_50SE	GDDR3_DQS	FB B WDQS<7>	68 70
FB_D_RDQS0	GDDR3_50SE	GDDR3_DQS	FB B RDQS<4>	68 70
FB_D_RDQS1	GDDR3_50SE	GDDR3_DQS	FB B RDQS<5>	68 70
FB_D_RDQS2	GDDR3_50SE	GDDR3_DQS	FB B RDQS<6>	68 70
FB_D_RDQS3	GDDR3_50SE	GDDR3_DQS	FB B RDQS<7>	68 70
FB_D_DQ_BYTE0	GDDR3_50SE	GDDR3_DATA	FB B DQ<39..32>	68 70
FB_D_DQ_BYTE1	GDDR3_50SE	GDDR3_DATA	FB B DQ<47..40>	68 70
FB_D_DQ_BYTE2	GDDR3_50SE	GDDR3_DATA	FB B DQ<55..48>	68 70
FB_D_DQ_BYTE3	GDDR3_50SE	GDDR3_DATA	FB B DQ<63..56>	68 70
FB_D_DQM0	GDDR3_50SE	GDDR3_DATA	FB B DQM_L<4>	68 70
FB_D_DQM1	GDDR3_50SE	GDDR3_DATA	FB B DQM_L<5>	68 70
FB_D_DQM2	GDDR3_50SE	GDDR3_DATA	FB B DQM_L<6>	68 70
FB_D_DQM3	GDDR3_50SE	GDDR3_DATA	FB B DQM_L<7>	68 70

GPU (G84M) Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE

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DRAWING NUMBER

051-7225

REV.

14.0.0

SCALE


NONE

SHT

86

OF

88

8		7		6		5		4		3		2		1		
M75 Board-Specific Spacing & Physical Constraints																
BOARD LAYERS						BOARD AREAS		BOARD UNITS (MIL OR MM)		ALLEGRO VERSION						
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM						NO_TYPE, BGA		MM		15.5.1						
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
DEFAULT		*	Y	=55_OHM_SE	=55_OHM_SE	30 MM	0 MM	0 MM								
STANDARD		*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT								
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
55_OHM_SE		TOP, BOTTOM	Y	0.100 MM	0.100 MM											
55_OHM_SE		ISL2, ISL11	Y	0.250 MM	0.076 MM											
55_OHM_SE		*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD								
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
50_OHM_SE		TOP, BOTTOM	Y	0.125 MM	0.125 MM											
50_OHM_SE		*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD								
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
45_OHM_SE		TOP, BOTTOM	Y	0.150 MM	0.150 MM											
45_OHM_SE		*	Y	0.105 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD								
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
40_OHM_SE		TOP, BOTTOM	Y	0.185 MM	0.185 MM											
40_OHM_SE		*	Y	0.131 MM	0.131 MM	=STANDARD	=STANDARD	=STANDARD								
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
27P4_OHM_SE		TOP, BOTTOM	Y	0.335 MM	0.335 MM											
27P4_OHM_SE		*	Y	0.240 MM	0.240 MM	=STANDARD	=STANDARD	=STANDARD								
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
70_OHM_DIFF		*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD								
70_OHM_DIFF		ISL3, ISL4	Y	0.149 MM	0.149 MM		0.125 MM	0.125 MM								
70_OHM_DIFF		ISL9, ISL10	Y	0.149 MM	0.149 MM		0.125 MM	0.125 MM								
70_OHM_DIFF		ISL2, ISL11	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM								
70_OHM_DIFF		TOP, BOTTOM	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM								
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
80_OHM_DIFF		*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD								
80_OHM_DIFF		ISL3, ISL4	Y	0.115 MM	0.115 MM		0.125 MM	0.125 MM								
80_OHM_DIFF		ISL9, ISL10	Y	0.115 MM	0.115 MM		0.125 MM	0.125 MM								
80_OHM_DIFF		ISL2, ISL11	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM								
80_OHM_DIFF		TOP, BOTTOM	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM								
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
85_OHM_DIFF		*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD								
85_OHM_DIFF		ISL3, ISL4	Y	0.101 MM	0.101 MM		0.125 MM	0.125 MM								
85_OHM_DIFF		ISL9, ISL10	Y	0.101 MM	0.101 MM		0.125 MM	0.125 MM								
85_OHM_DIFF		ISL2, ISL11	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM								
85_OHM_DIFF		TOP, BOTTOM	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM								
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
90_OHM_DIFF		*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD								
90_OHM_DIFF		ISL3, ISL4	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM								
90_OHM_DIFF		ISL9, ISL10	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM								
90_OHM_DIFF		ISL2, ISL11	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM								
90_OHM_DIFF		TOP, BOTTOM	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM								
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
100_OHM_DIFF		*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD								
100_OHM_DIFF		ISL3, ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM								
100_OHM_DIFF		ISL9, ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM								
100_OHM_DIFF		ISL2, ISL11	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM								
100_OHM_DIFF		TOP, BOTTOM	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM								
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
110_OHM_DIFF		*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD								
110_OHM_DIFF		ISL3, ISL4	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM								
110_OHM_DIFF		ISL9, ISL10	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM								
110_OHM_DIFF		ISL2, ISL11	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM								
110_OHM_DIFF		TOP, BOTTOM	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM								
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
100_DIFF_BGA		*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF								
100_DIFF_BGA		ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM								
100_DIFF_BGA		ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM								
NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.																
M75 Rule Definitions																
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)																
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