

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
			2010-08-05

SCHEM, FLYING_CLOUD, MLB, K90i

"EVT3" 11/22/10

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17	19	PCH DMI/FDI/GRAPHICS	K91_MLB	06/18/2010
18	20	PCH PCI/FLASHCACHE/USB	K91_MLB	06/10/2010
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25	27	Clock (CK505)	K91_MLB	06/21/2010
26	28	Chipset Support	LINDA_K90i	07/08/2010
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29	31	DDR3 SO-DIMM Connector B	MASTER	MASTER
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38	40	Ethernet Connector	K91_MLB	05/26/2010
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40	42	FireWire Port & PHY Power	T27_MLB	12/15/2009
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60	66	AUDIO: SPEAKER AMP	LENG_K90i	08/10/2010
61	67	AUDIO: JACK	LENG_K90i	08/10/2010
62	68	AUDIO: JACK TRANSLATORS	LENG_K90i	08/10/2010
63	69	DC-In & Battery Connectors	JACK_K90i	08/20/2010
64	70	PBus Supply & Battery Charger	JACK_K90i	10/11/2010
65	71	System Agent Supply	JACK_K90i	08/19/2010
66	72	5V/3.3V SUPPLY	JACK_K90i	10/04/2010
67	73	1.5V DDR3 Supply	JACK_K90i	10/11/2010
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69	75	CPU IMVP7 & AXG VCore Output	JACK_K90i	09/03/2010
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77	97	LCD Backlight Driver	VENURI_K90i	06/25/2010
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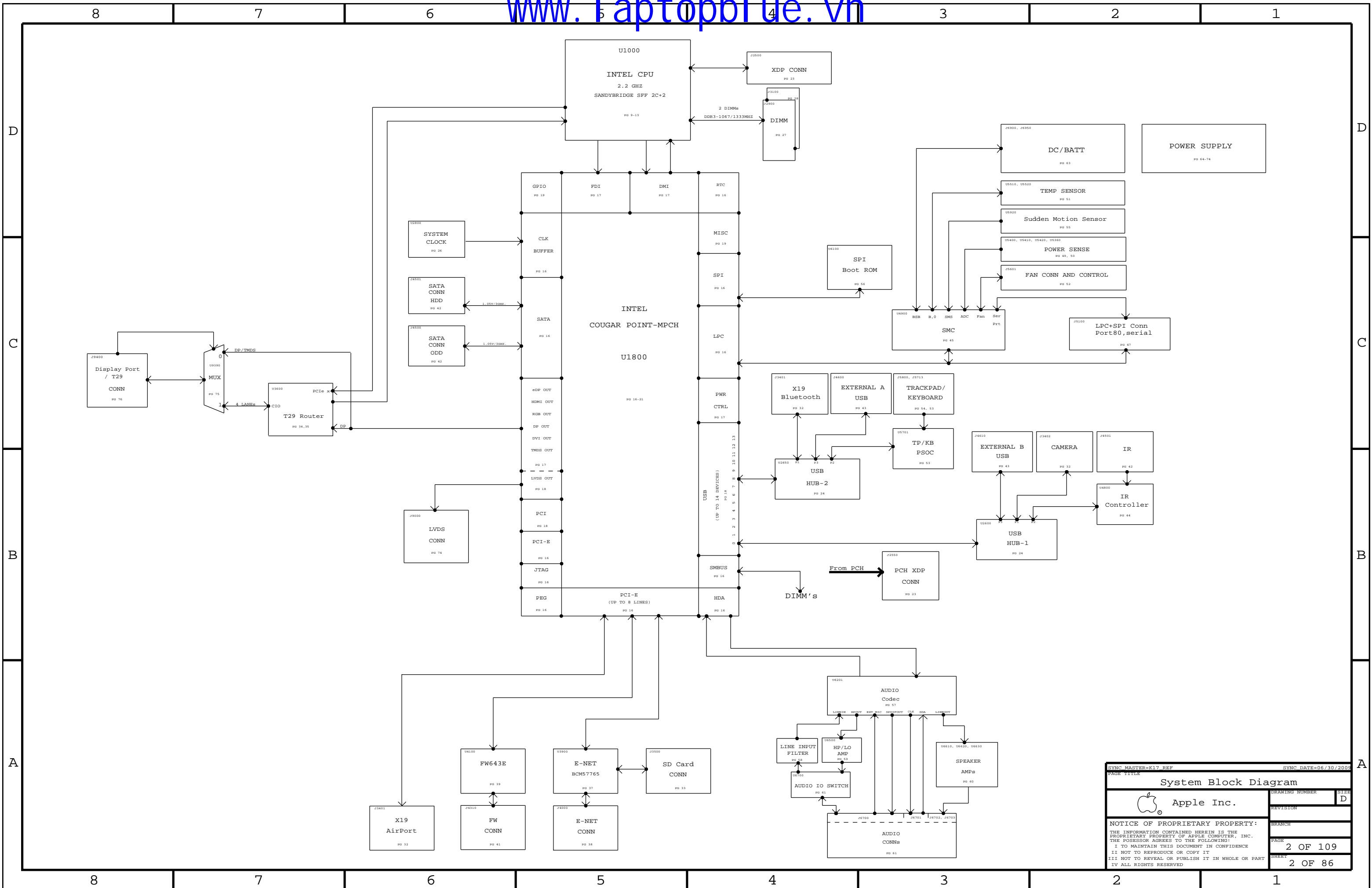
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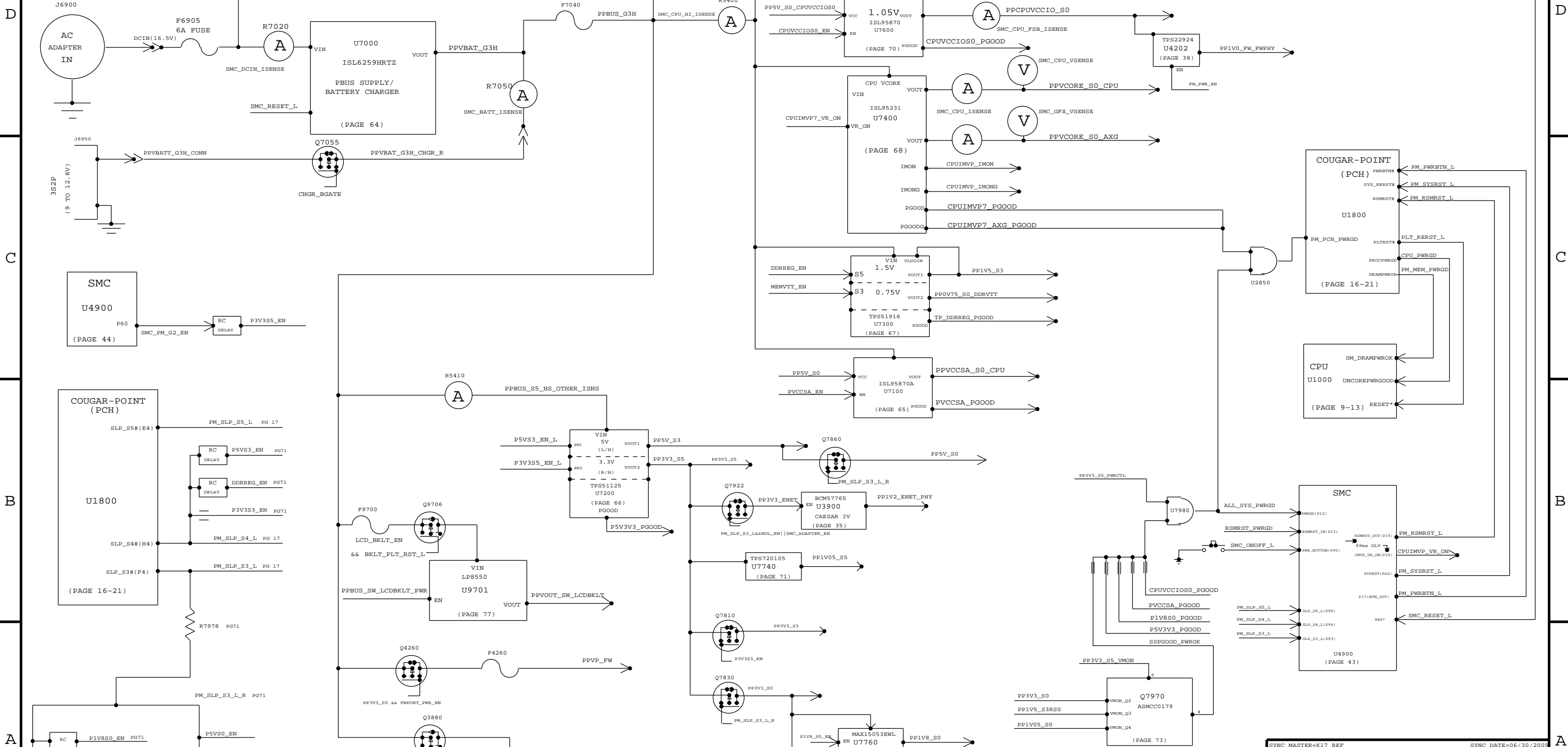
Schematic / PCB #'s

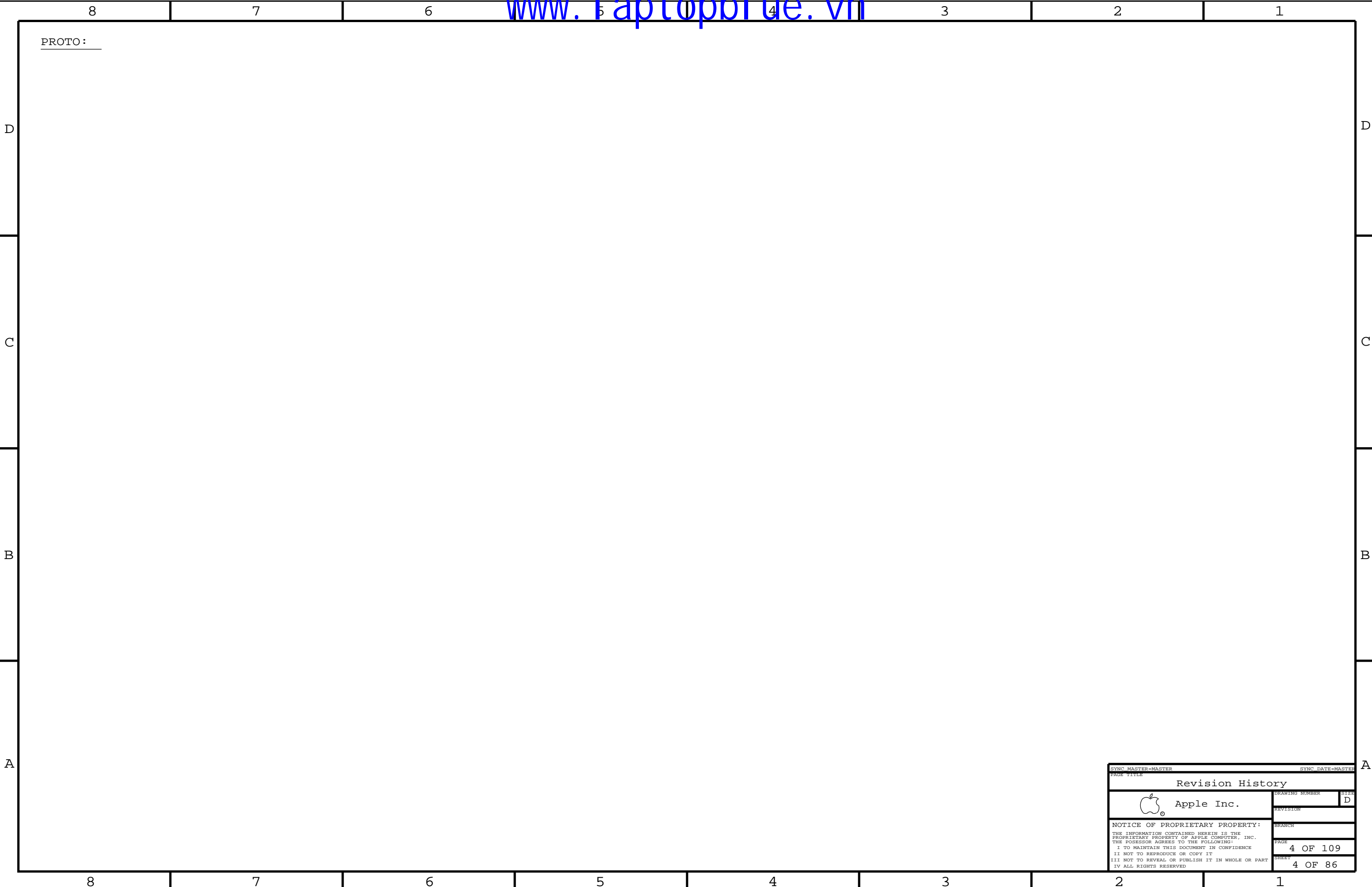
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8658	1	SCHEM, MLB, K90i	SCH	CRITICAL	
820-2936	1	PCBF, MLB, K90i	PCB	CRITICAL	

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ABBREV=DRAWING
LAST MODIFIED=Mon Nov 22 19:21:11 2010


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SCHEM, FLYING_CLOUD, MLB, K90i		
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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-1294	PCBA, 2.5G, K90i	K90i_COMMON, CPU_2_5GHZ, EEEF_DDRQ
639-1581	PCBA, 2.7G, K90i	K90i_COMMON, CPU_2_7GHZ, EEEF_DH78
639-1698	PCBA, 2.6G, K90i	K90i_COMMON, CPU_2_6GHZ, EEEF_DH8F
639-1699	PCBA, 2.3G, K90i	K90i_COMMON, CPU_2_3GHZ, EEEF_DH8G
085-1998	K90i MLB DEVELOPMENT BOM	K90i_DEVEL:ENG

K90i BOM GROUPS

BOM GROUP	BOM OPTIONS
K90i_COMMON	ALTERNATE, COMMON, K90i_COMMON1, K90i_COMMON2, K90i_DEBUG:ENG, K90i_PROGPARTS, USBHUB_2513B, T29BST:Y
K90i_COMMON1	BATT_3S, CPUMEM_S0, SMC_DEBUG_YES, HUB1_2NONREM, HUB2_3NONREM, T29:YES, DP_SDRV:A2, SDRV_PD, SDRV12C:MCU
K90i_COMMON2	MIKEY, KB_BL
K90i_PROGPARTS	BOOTROM_PROG, SMC_PROG, TPAD_PROG, ENET_PROG, T29ROM:PROG, T29MCU:PROG
K90i_DEVEL:ENG	BKLT:ENG, BMON:ENG, XDP_CONN, XDP_CPU:BPM, XDP_PCH, LPCPLUS, VREFMRGN, SDPGOOD_ISL, IMVPISNS_ENG
K90i_DEVEL:PVT	LPCPLUS, XDP_CONN, XDP_PCH
K90i_DEBUG:ENG	DEVEL_BOM, SMC_DEBUG_YES, XDP
K90i_DEBUG:PVT	DEVEL_BOM, BKLT:PROD, BMON:PROD, SMC_DEBUG_YES, XDP, VREFMRGN_NOT
K90i_DEBUG:PROD	BKLT:PROD, BMON:PROD, SMC_DEBUG_YES, XDP, VREFMRGN_NOT, LPCPLUS

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3934	1	SNB, 3C, QXXX, RS1, 2.2, 35W, B2, 3M, GT1, BGA	U1000	CRITICAL	CPU_2_2GHZ
337S4058	1	SNB, Q18A, QS, J1, 2.5, 35W, 2+2, 1.30, 3M, BGA	U1000	CRITICAL	CPU_2_5GHZ
337S4057	1	SNB, Q183, QS, J1, 2.7, 35W, 2+2, 1.30, 4M, BGA	U1000	CRITICAL	CPU_2_7GHZ
337S4024	1	SNB, Q189, QS, J1, 2.3, 35W, 2+2, 1.30, 3M, BGA	U1000	CRITICAL	CPU_2_3GHZ
337S4064	1	SNB, Q187, QS, J1, 2.6, 35W, 2+2, 1.30, 3M, BGA	U1000	CRITICAL	CPU_2_6GHZ
337S4029	1	IC, PCH, COGULARPOINT, SLH9D, FRQ, BD82HM65	U1800	CRITICAL	
343S0534	1	IC, BMC5776580, ENET&SD, 8X8	U3900	CRITICAL	
338S0753	1	IC, P9643-E2, 1394B, 9V, 08C1, 15M, PCI-E, 12	U4100	CRITICAL	
338S0921	1	IC, T29-C0, 220 PCBGA, 15x15MM	U3600	CRITICAL	T29:YES
353S3055	1	IC, P13VEDP212, X2 DISPLAYPORT 2/1 MIX, QFN	U9390	CRITICAL	

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0663	1	IC, FLASH, SERIAL, SPI, 1MBIT, 2V7, EP, 801C	U3990	CRITICAL	ENET_BLANK
341S3026	1	IC, ENET, 11MBITPLA, CIV REV01, K60/K62	U3990	CRITICAL	ENET_PROG
335S0777	1	IC, EEPROM, SERIAL, SPI, 1Kx8, 1.8V, MLP8, LF	U3690	CRITICAL	T29ROM:BLANK
341T0317	1	IC, T29 ASSY	U3690	CRITICAL	T29ROM:PROG
337S3997	1	IC, MCU, 32B, LPC1112A, 16KB/2KB, HVQFN25	U9330	CRITICAL	T29MCU:BLANK
341S2939	1	IC, PROGRAMD, LPC1112A, T29 PORT MCU, HVQFN25	U9330	CRITICAL	T29MCU:PROG
338S0895	1	IC, SMC, HSB /2117/9MMx9MM, TLP	U4900	CRITICAL	SMC_BLANK
341T0300	1	IC, SMC, K90i	U4900	CRITICAL	SMC_PROG
335S0770	1	64 MBIT SPI SERIAL DUAL I/O FLASH	U6100	CRITICAL	BOOTROM_BLANK
335S0769	1	64 MBIT SPI SERIAL DUAL I/O FLASH	U6100	CRITICAL	BOOTROM_BLANK
341T0299	1	IC, EFI ROM, K90i	U6100	CRITICAL	BOOTROM_PROG
341S2384	1	IR, ENCORE II, CY7C53803-LQXC	U4800	CRITICAL	
341S3024	1	IC, TP PSOC, K90, K90i, K91, K91F, K92	U5701	CRITICAL	TPAD_PROG

Development BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-1998	1	K90i MLB DEVELOPMENT	DEVEL	CRITICAL	DEVEL_BOM

Bar Code Labels / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEEE:DDRQ]	CRITICAL	EEEE_DDRQ
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEEE:DH78]	CRITICAL	EEEE_DH78
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEEE:DH8F]	CRITICAL	EEEE_DH8F
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEEE:DH8G]	CRITICAL	EEEE_DH8G


Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0603	138S0602		ALL	Murata alt to Samsung
157S0058	157S0055		ALL	Delia alt to THE Magazine
516S0805	516S0806		ALL	Molex alt to Furcom
128S0303	128S0282		ALL	Danacomic alt to Sanyo
138S0676	138S0691		ALL	Murata alt to Samsung
152S0778	152S0693		ALL	Cyntec alt to Vishay
376S0855	376S0613		ALL	Diodes alt to Toshiba
376S0977	376S0859		ALL	Diodes alt to Toshiba
376S0972	376S0612		ALL	Rohm alt to Toshiba
376S0927	376S0966		ALL	Fairchild alt to Renesas
376S0927	376S0790		ALL	Fairchild alt to CIRCLOW
376S0960	376S0801		ALL	Renesas alt to Renesas
376S0790	376S0928		ALL	CIRCLOW alt to Fairchild
376S0928	376S0895		ALL	Fairchild alt to Renesas
376S0937	376S0845		ALL	Fairchild alt to Renesas
376S0777	376S0761		ALL	ACW alt to Siliconix
376S0957	376S0958		ALL	Fairchild alt to Fairchild
376S0953	376S0958		ALL	Fairchild alt to Renesas
353S3085	353S1658		ALL	STmicro alt to LT

SYNC MASTER=K17 REF

SYNC DATE=05/28/2009

BOM Configuration

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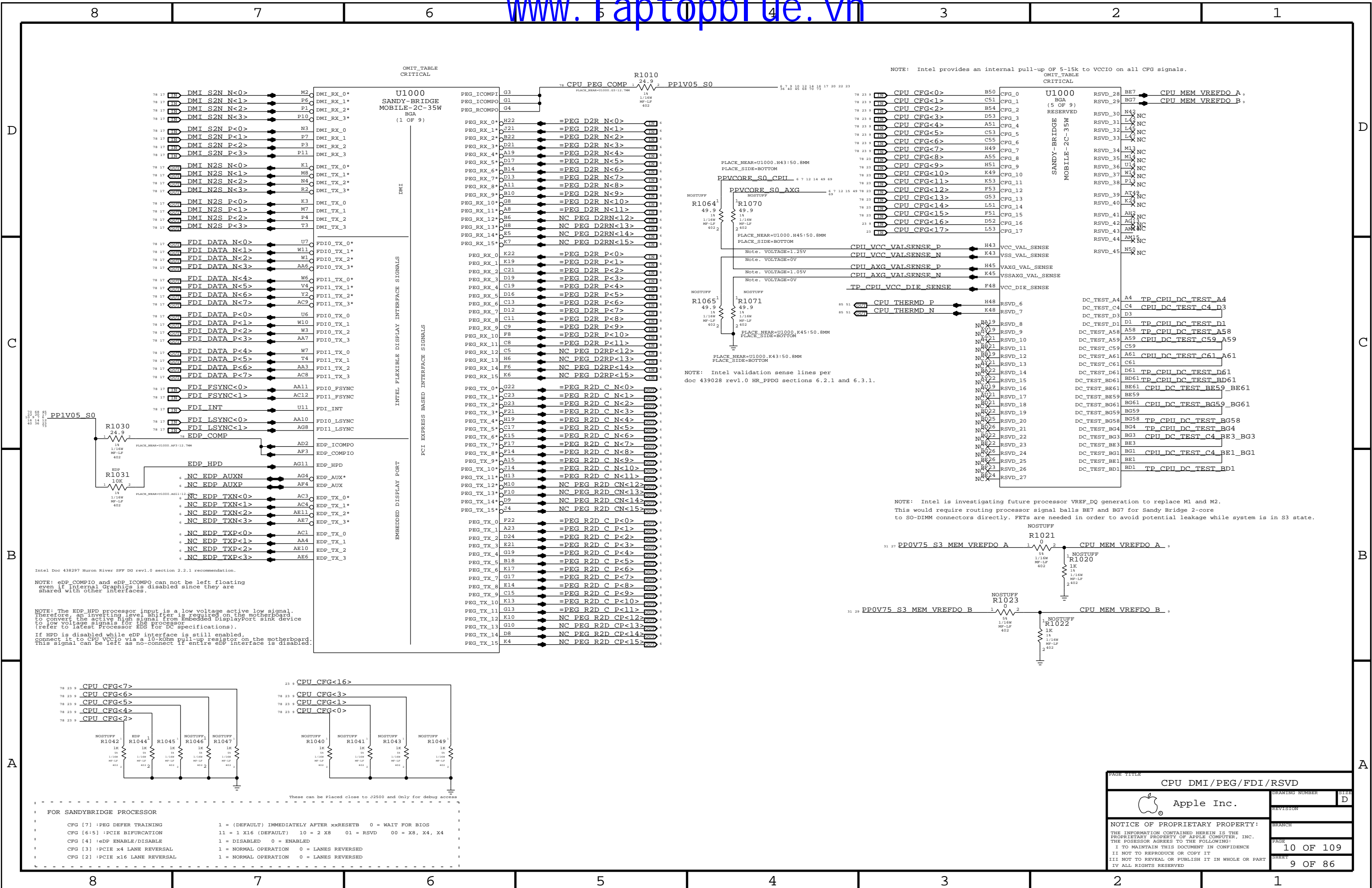
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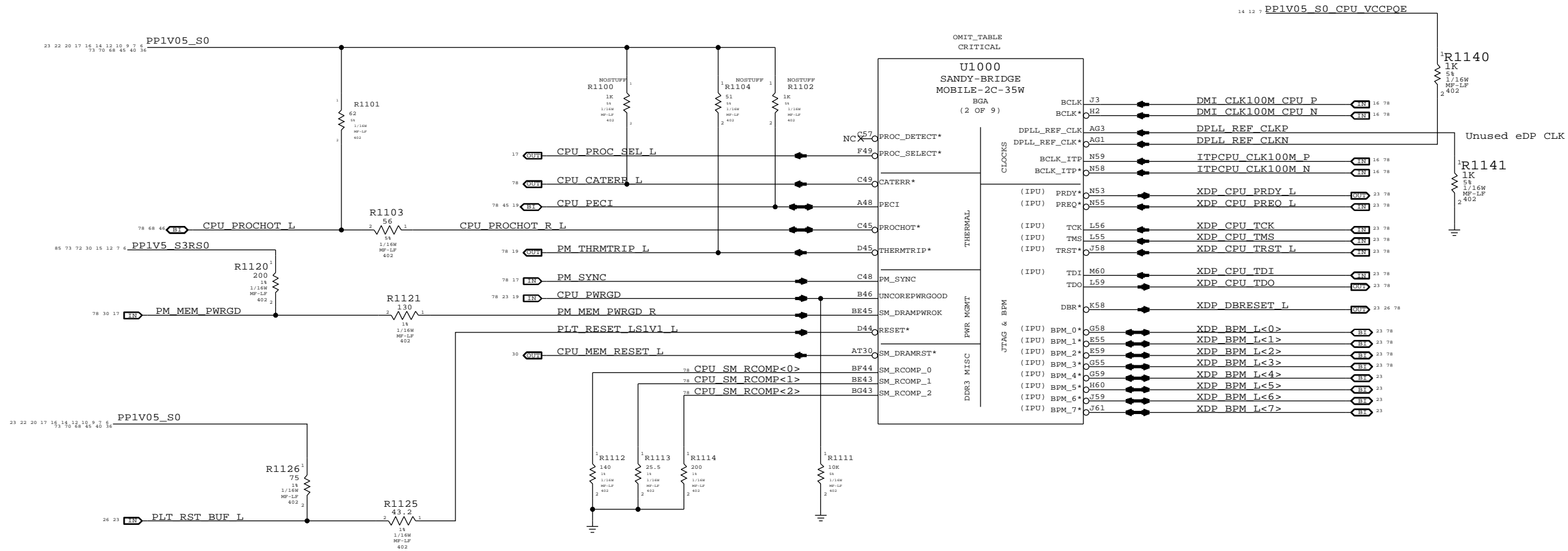
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OMIT_TABLE CRITICAL									
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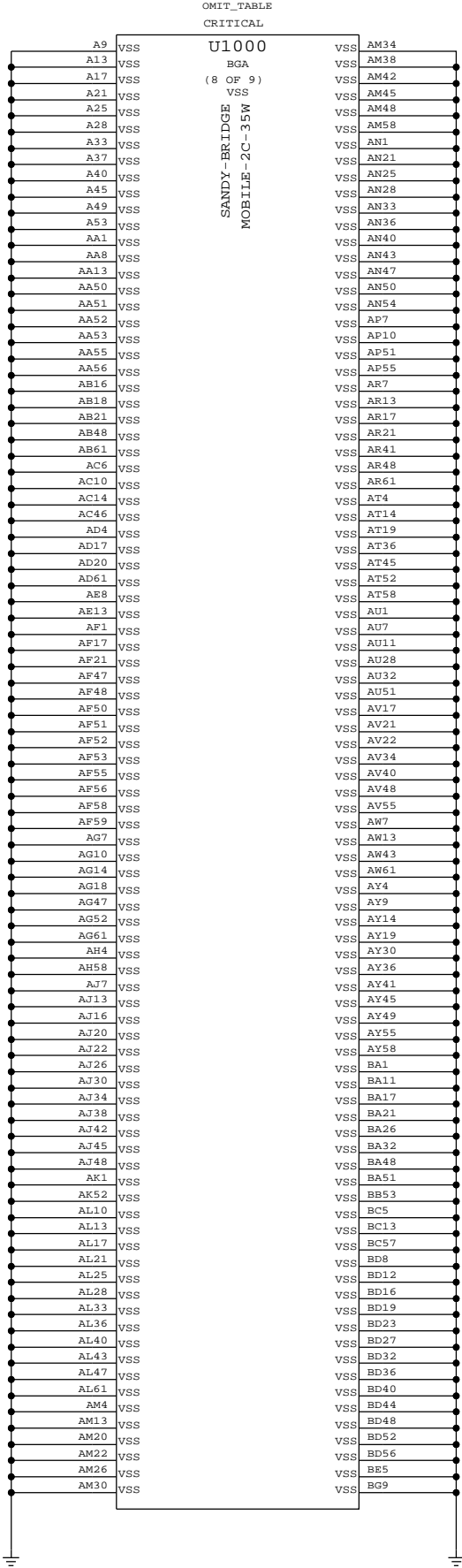
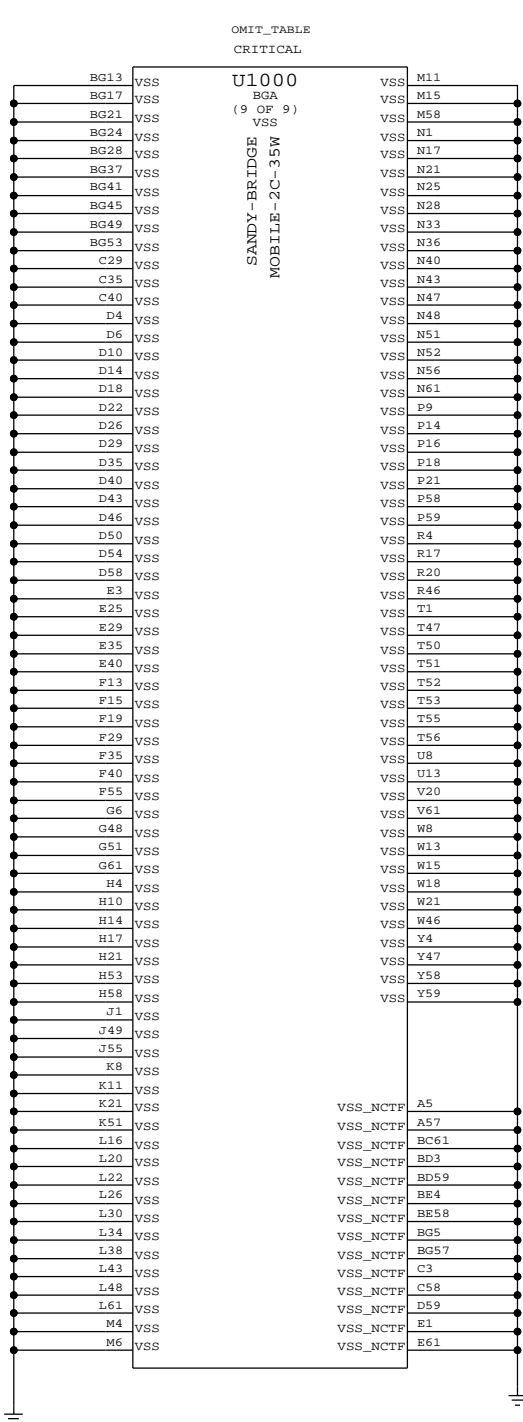
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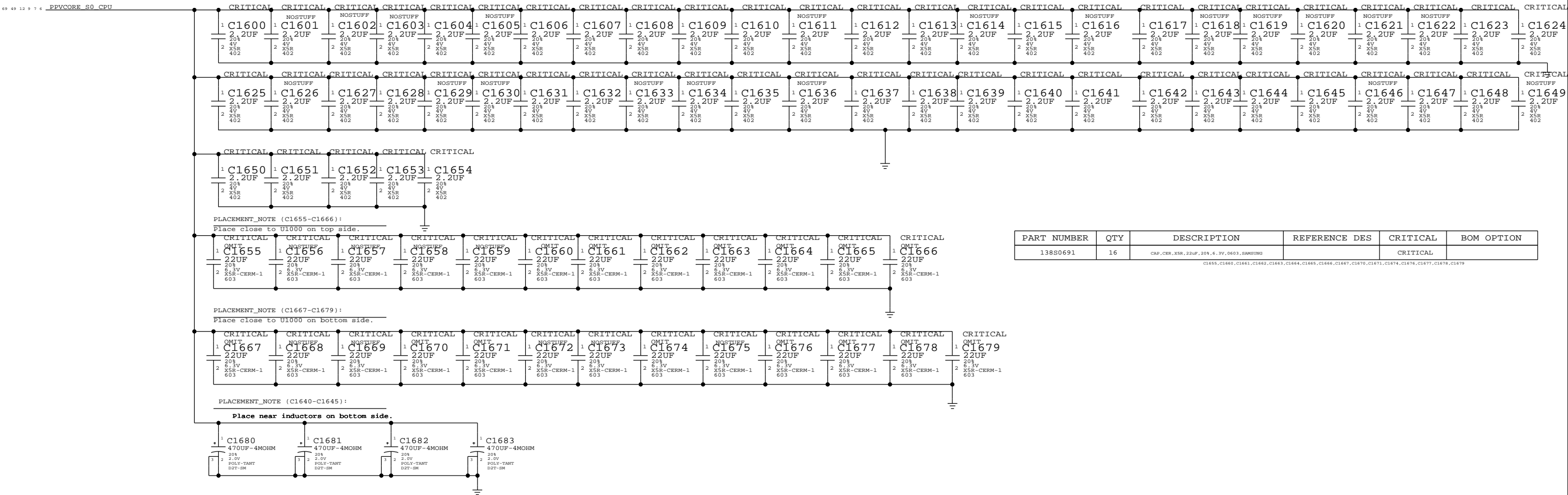
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All INTEL recommendations from Intel doc #4439028 Huron River Platform Power Design Guide

CPU VCORE DECOUPLING

Intel recommendation (Section 6.2): 35x 2.2uF, 25x 22uF, 4x 470uF



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0691	16	CAP, CER, X5R, 22uF, 20%, 6.3V, 0603, SAMSUNG		CRITICAL	

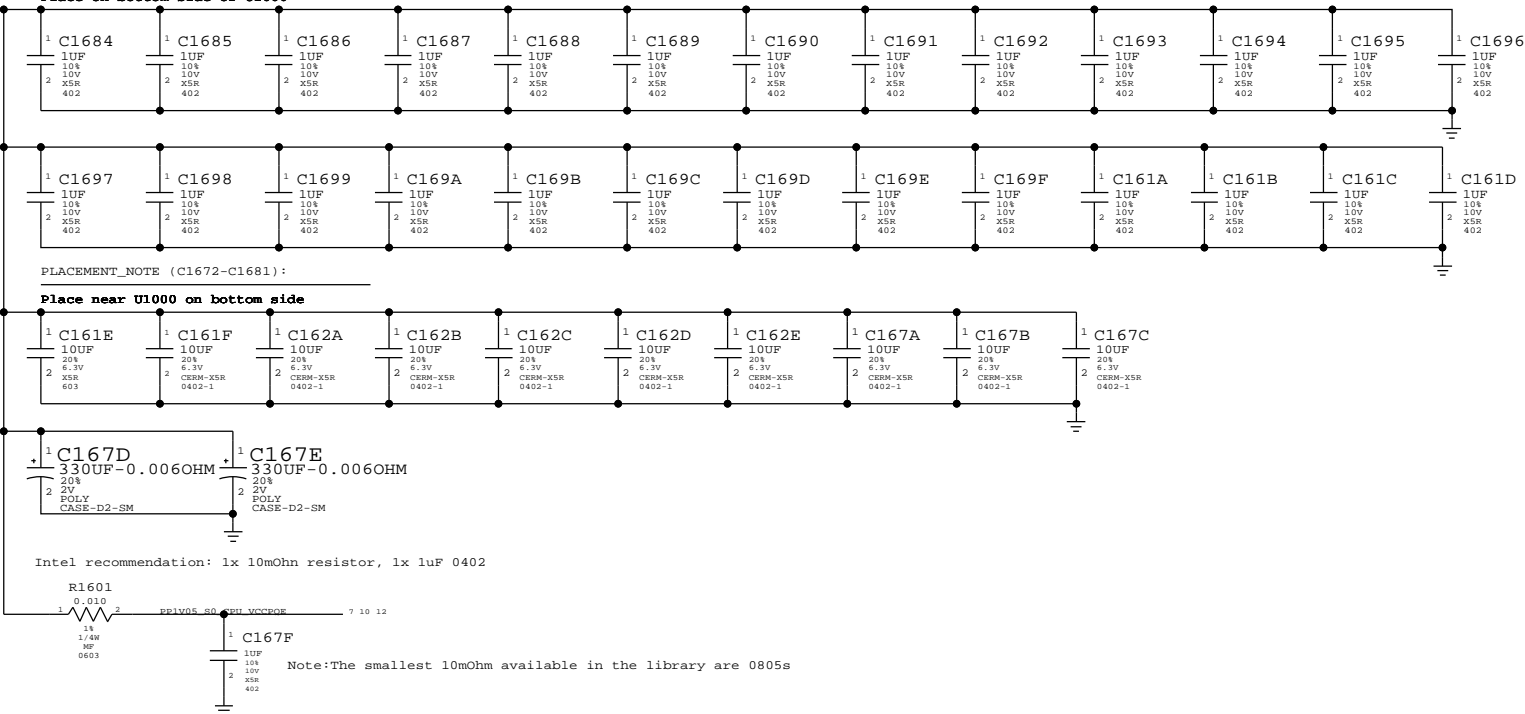
C1655,C1660,C1661,C1662,C1663,C1664,C1665,C1666,C1667,C1670,C1671,C1674,C1676,C1677,C1678,C1679

CPU VCCIO/VCCPQ DECOUPLING

Intel recommendation (Section 6.5): 26x 1uF, 10x 10uF, 2x 330uF

PLACEMENT_NOTE (C1684-C167F):

Place on bottom side of U1000

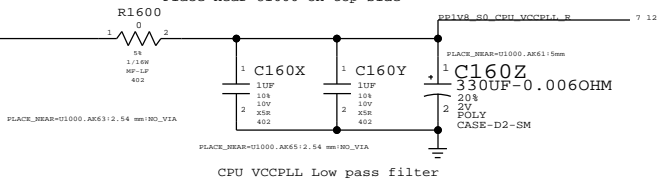



CPU VCCPLL DECOUPLING

Intel recommendation (section 6.4): 2x 1uF, 1x 330uF

PLACEMENT_NOTE (C1646-C1671):

Place near U1000 on top side



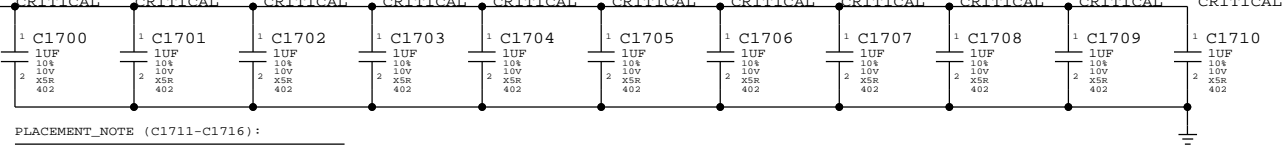
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VAXG DECOUPLING

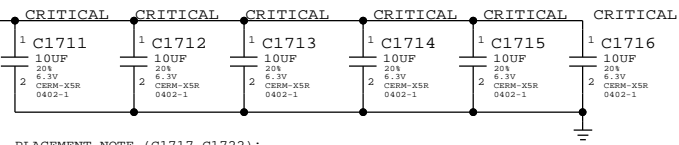
Intel recommendation (section 6.3): 21x 1uF, 6x 10uF, 6x 22uF, 2x 470uF

PLACEMENT_NOTE (C1700-C1710):

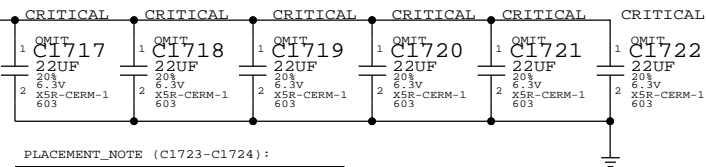
Place on bottom side of U1000



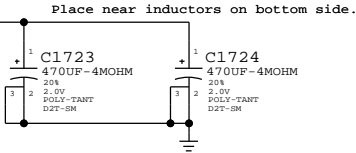
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PLACEMENT_NOTE (C1717-C1722):



PLACEMENT_NOTE (C1723-C1724):



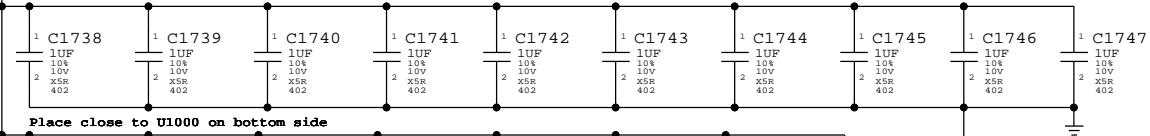
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138S0691	6	CAP, CER, X5R, 22uF, 20V, 6.3V, 0603, SAMSUNG	C1717, C1718, C1719, C1720, C1721, C1722	CRITICAL	

CPU VDDQ/VCCDQ DECOUPLING

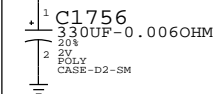
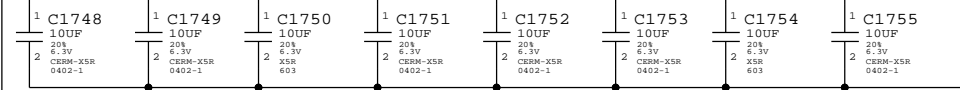
Intel recommendation (Section 6.5): 10x 1uF, 8x 10uF, 1x 330uF

PLACEMENT_NOTE (C1738-C1747):

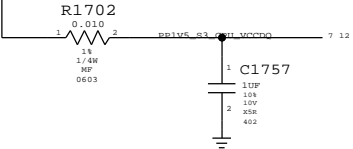
Place on bottom side of U1000



Place close to U1000 on bottom side



Intel recommendation: 1x 10mOhm resistor, 1x 1uF 0402

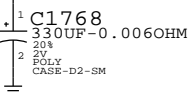
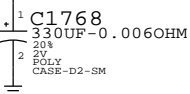
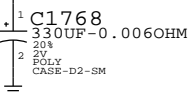
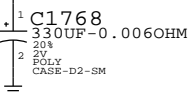
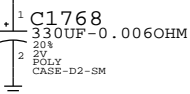
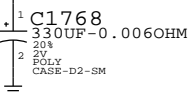
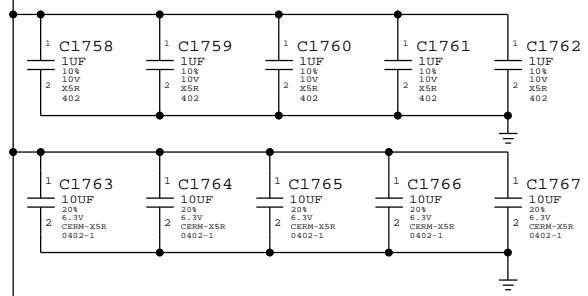


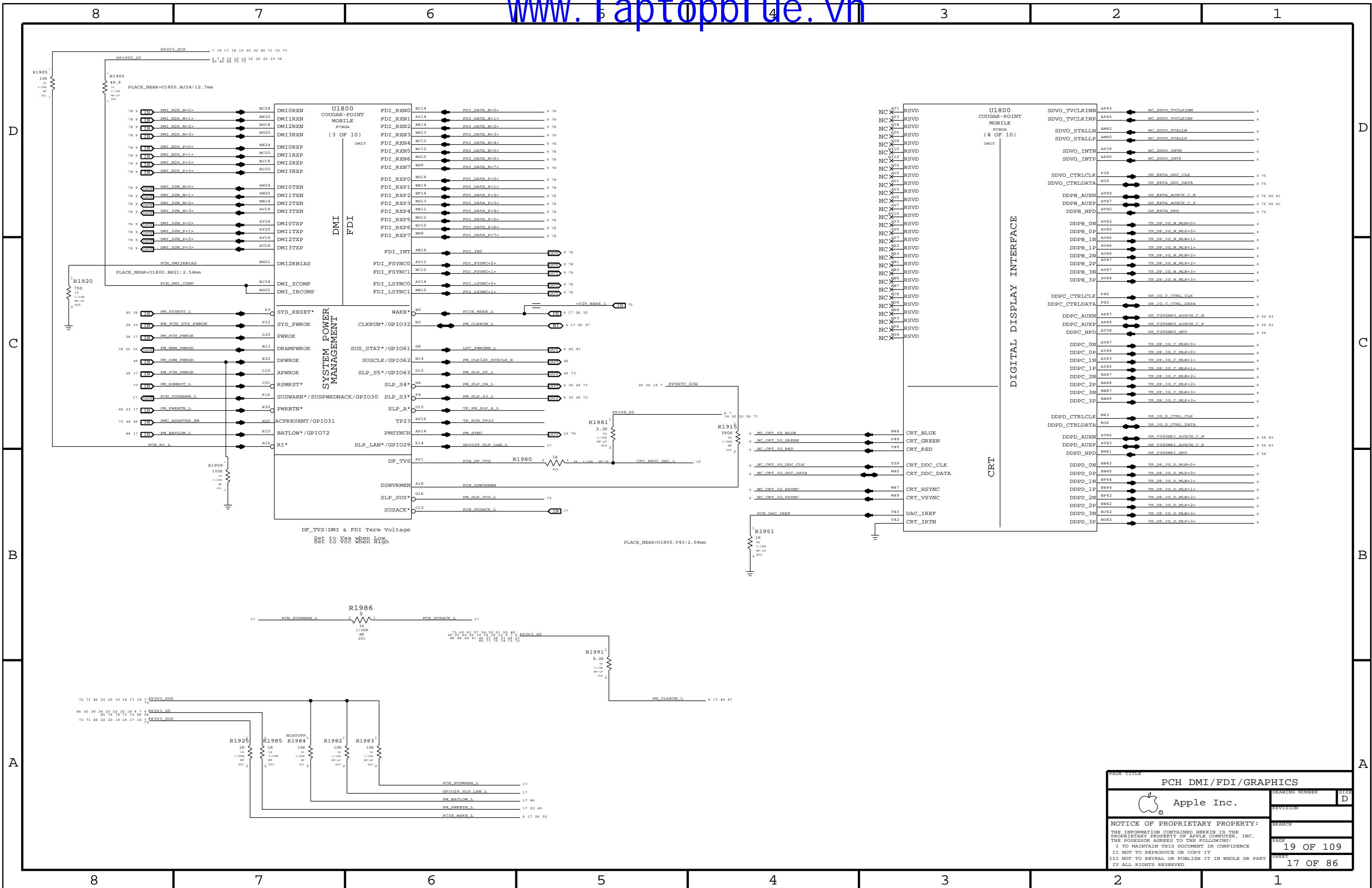
CPU VCCSA DECOUPLING

Intel recommendation (Section 6.6): 6x 1uF, 5x 10uF, 1x 330uF

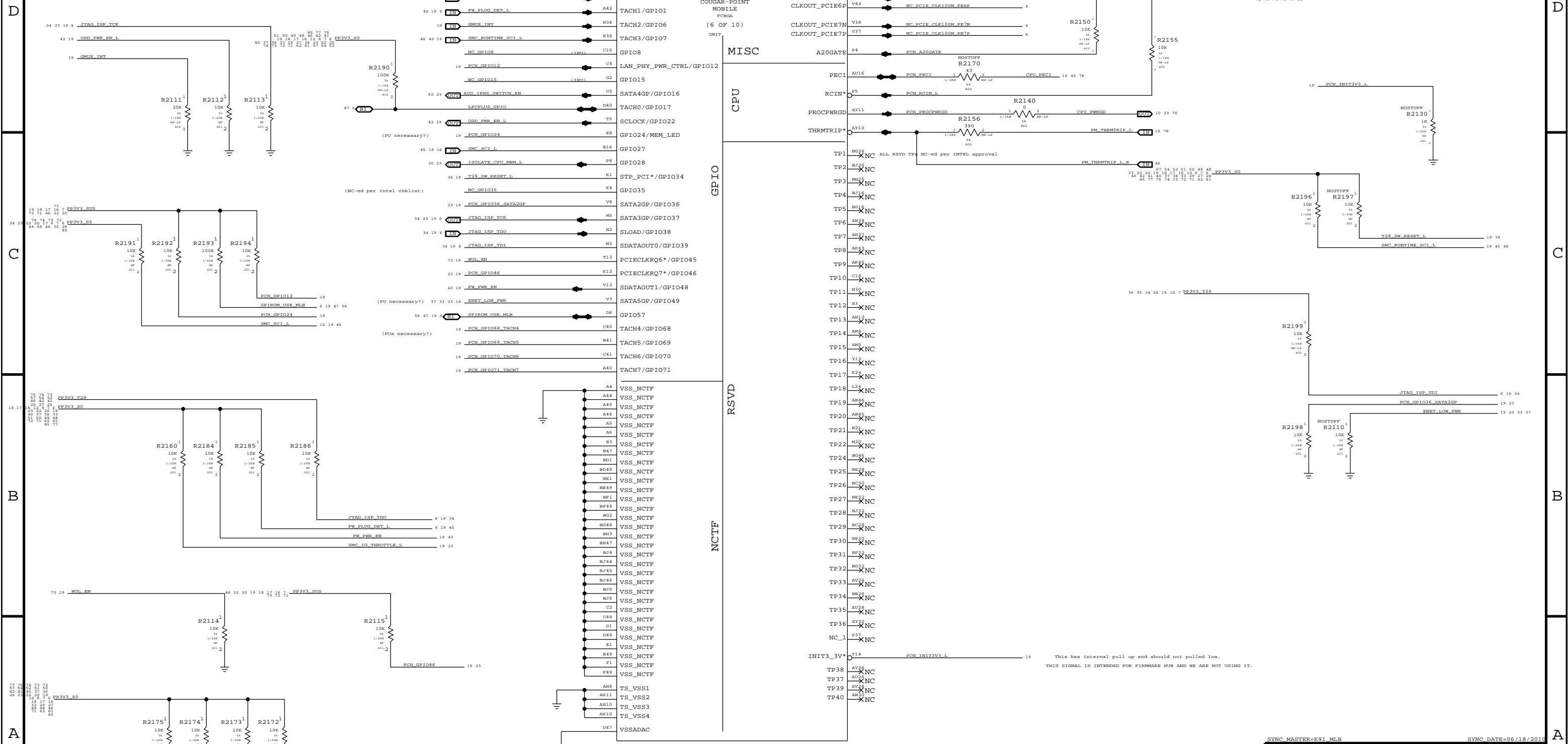
PLACEMENT_NOTE (C1758-C1762):

Place on bottom side of U1000











D

C

B

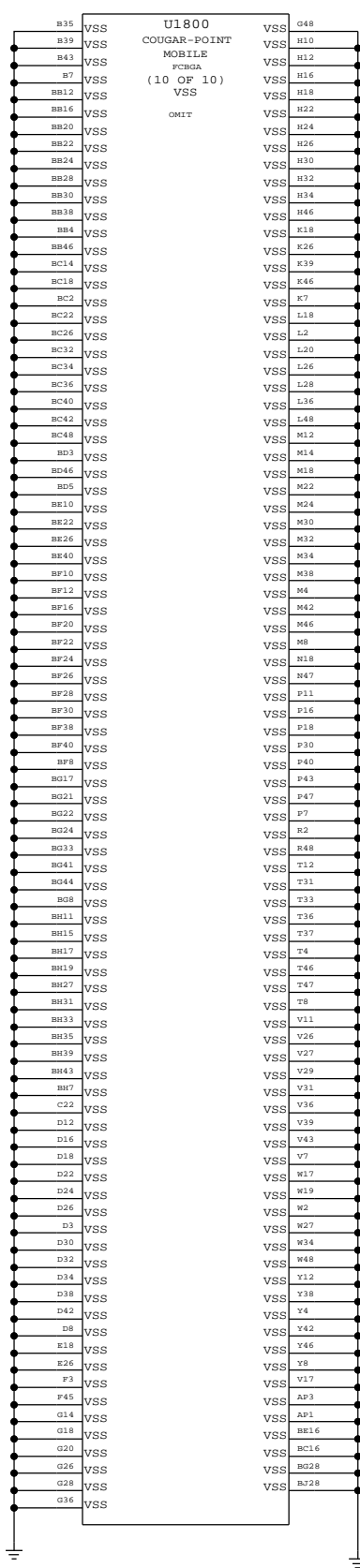
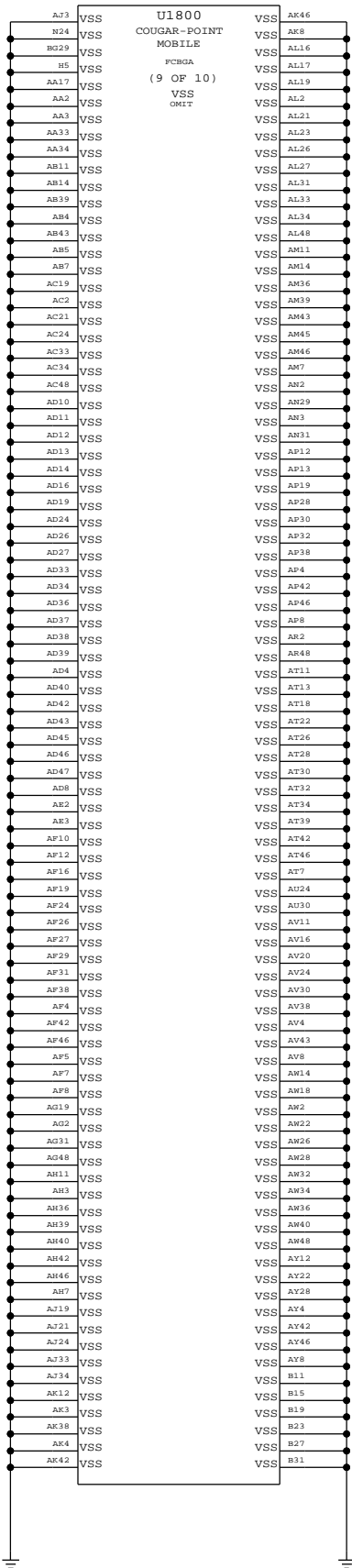
A


D

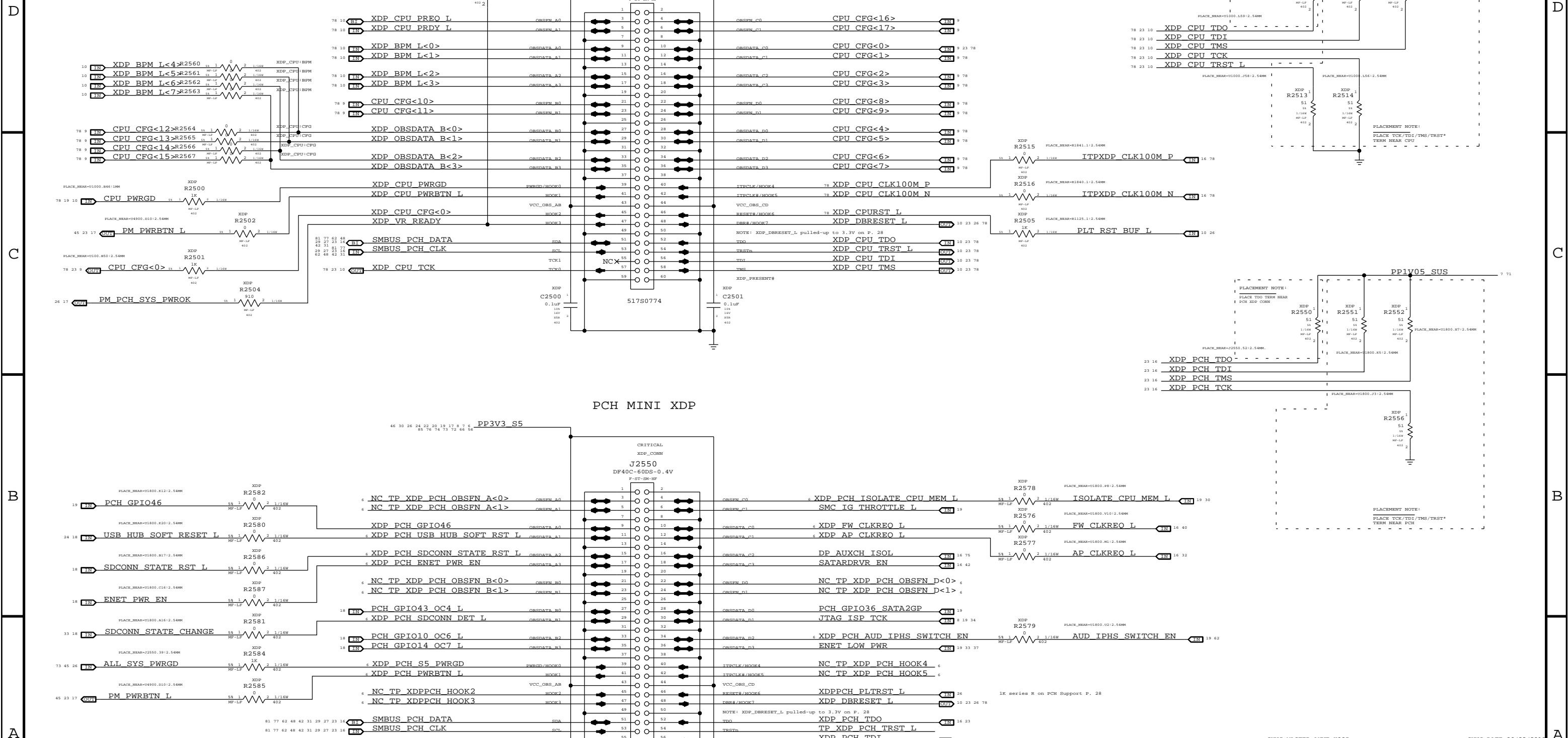
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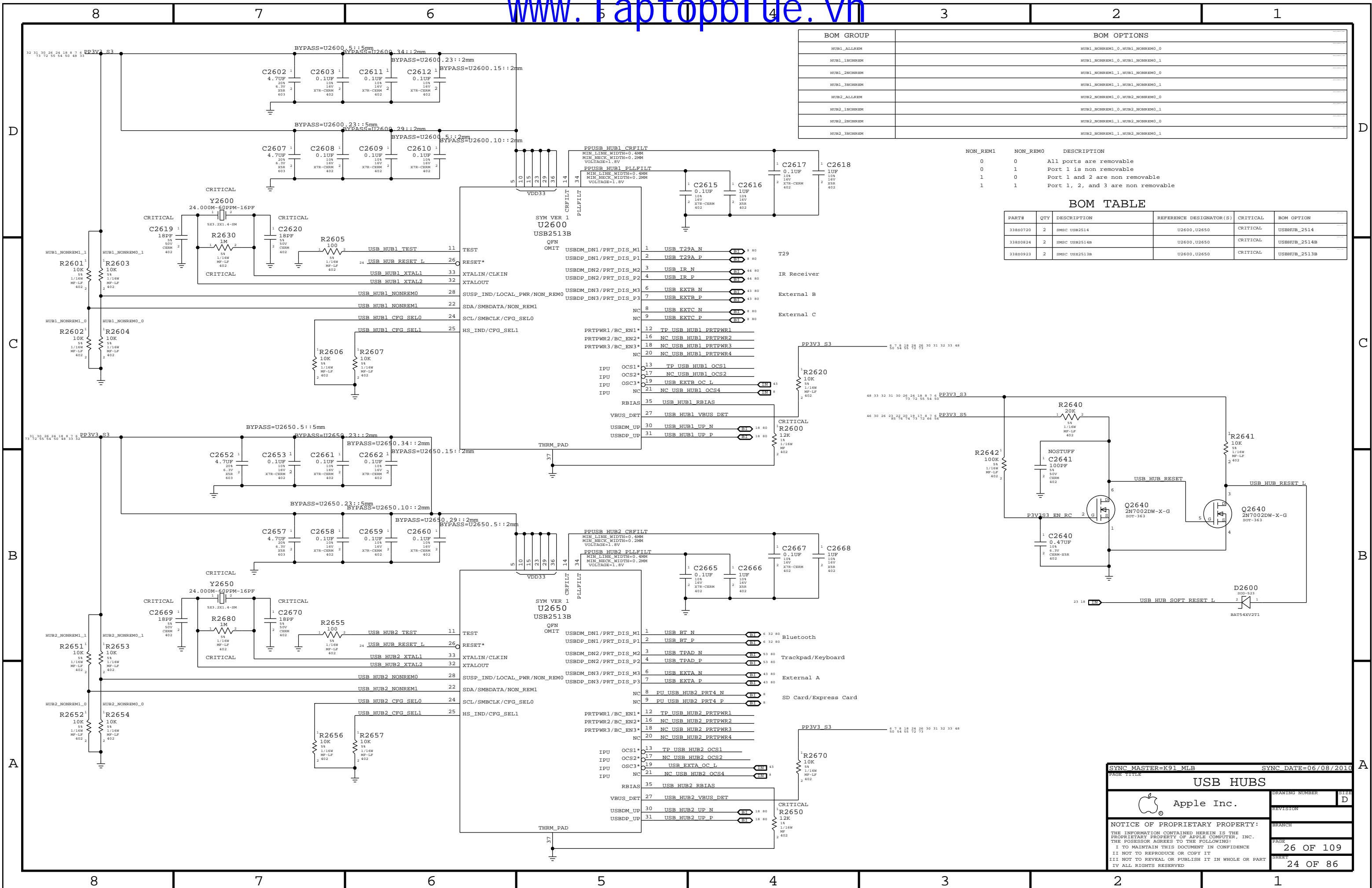
B

A



PAGE TITLE		SYNC MASTER=K91 MLB		SYNC DATE=05/27/2010	
PCH GROUNDS				DRAWING NUMBER	SIZE
 Apple Inc.				REVISION	D
				BRANCH	
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				SHEET	21 OF 86





D

D

C

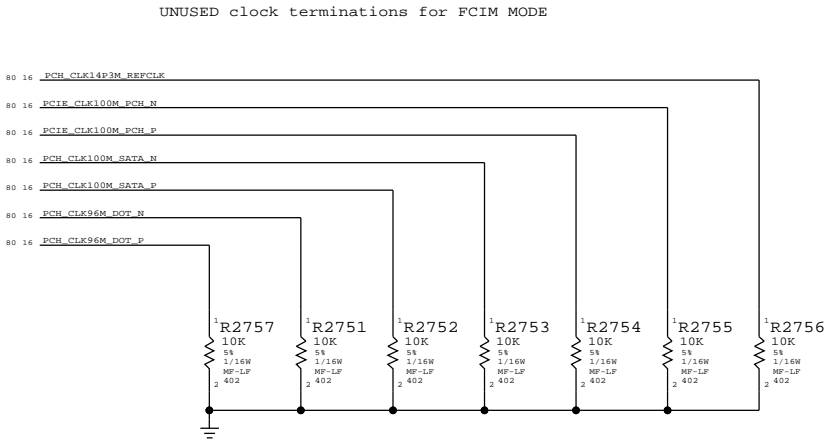
C

B

B

A

A



SYMC MASTER=K11 MCB

SYMC DATE=06/21/2011

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		DRAWING NUMBER	SIZE
		REVISION	D
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		PAGE	27 OF 109
		SHEET	25 OF 86

System RTC Power Source & 32kHz / 25MHz Clock Generator

Platform Reset Connections

Unbuffered


Buffered

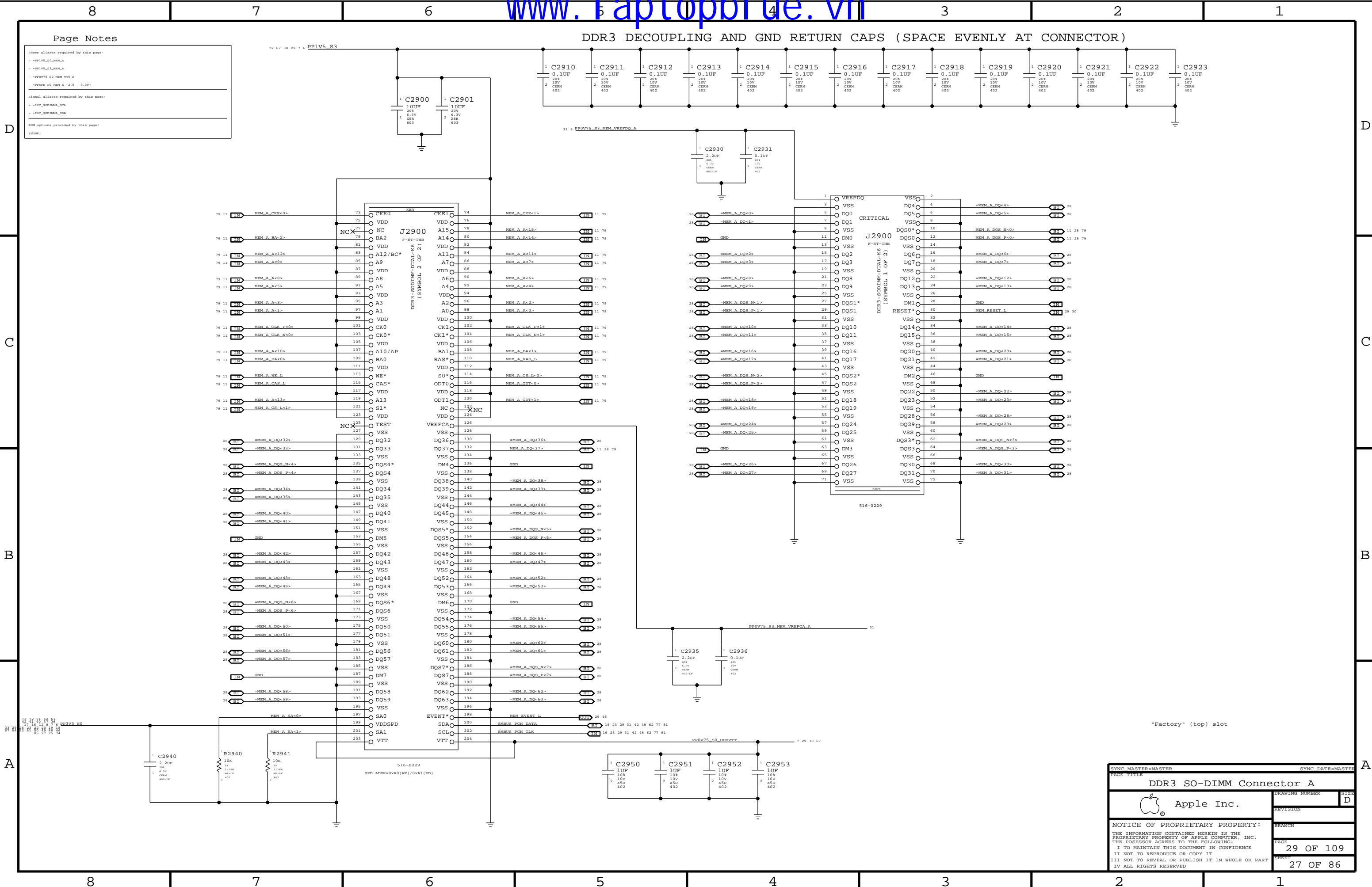
ENET_MEDIA_SENSE ISOLATION CIRCUIT

Ethernet WAKE# Isolation

PCH S0 PWRGD

PCH Reset Button

SYNC MASTER=LINDA K901		SYNC DATE=07/08/2010	
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D

C

B

A

MEM A DQ<0>		MAKE_BASE=TRUE	==	MEM A DQ<0>	27	MEM B DQ<0>		MAKE_BASE=TRUE	==	MEM B DQ<0>	29
CPU CHANNEL A DQS 1 -> DIMM A DQS 1											
MEM A DQS N<1>		MAKE_BASE=TRUE	==	MEM A DQS N<1>	27	MEM B DQS N<1>		MAKE_BASE=TRUE	==	MEM B DQS N<1>	29
MEM A DQS P<1>		MAKE_BASE=TRUE	==	MEM A DQS P<1>	27	MEM B DQS P<1>		MAKE_BASE=TRUE	==	MEM B DQS P<1>	29
		MAKE_BASE=TRUE	==	GND				MAKE_BASE=TRUE	==	GND	
MEM A DQ<15>		MAKE_BASE=TRUE	==	MEM A DQ<11>	27	MEM B DQ<15>		MAKE_BASE=TRUE	==	MEM B DQ<15>	29
MEM A DQ<14>		MAKE_BASE=TRUE	==	MEM A DQ<10>	27	MEM B DQ<14>		MAKE_BASE=TRUE	==	MEM B DQ<14>	29
MEM A DQ<13>		MAKE_BASE=TRUE	==	MEM A DQ<12>	27	MEM B DQ<13>		MAKE_BASE=TRUE	==	MEM B DQ<13>	29
MEM A DQ<12>		MAKE_BASE=TRUE	==	MEM A DQ<9>	27	MEM B DQ<12>		MAKE_BASE=TRUE	==	MEM B DQ<8>	29
MEM A DQ<11>		MAKE_BASE=TRUE	==	MEM A DQ<15>	27	MEM B DQ<11>		MAKE_BASE=TRUE	==	MEM B DQ<11>	29
MEM A DQ<10>		MAKE_BASE=TRUE	==	MEM A DQ<14>	27	MEM B DQ<10>		MAKE_BASE=TRUE	==	MEM B DQ<10>	29
MEM A DQ<9>		MAKE_BASE=TRUE	==	MEM A DQ<13>	27	MEM B DQ<9>		MAKE_BASE=TRUE	==	MEM B DQ<12>	29
MEM A DQ<8>		MAKE_BASE=TRUE	==	MEM A DQ<8>	27	MEM B DQ<8>		MAKE_BASE=TRUE	==	MEM B DQ<9>	29
CPU CHANNEL A DQS 2 -> DIMM A DQS 2											
MEM A DQS N<2>		MAKE_BASE=TRUE	==	MEM A DQS N<2>	27	MEM B DQS N<2>		MAKE_BASE=TRUE	==	MEM B DQS N<2>	29
MEM A DQS P<2>		MAKE_BASE=TRUE	==	MEM A DQS P<2>	27	MEM B DQS P<2>		MAKE_BASE=TRUE	==	MEM B DQS P<2>	29
		MAKE_BASE=TRUE	==	GND				MAKE_BASE=TRUE	==	GND	
MEM A DQ<23>		MAKE_BASE=TRUE	==	MEM A DQ<23>	27	MEM B DQ<23>		MAKE_BASE=TRUE	==	MEM B DQ<23>	29
MEM A DQ<22>		MAKE_BASE=TRUE	==	MEM A DQ<22>	27	MEM B DQ<22>		MAKE_BASE=TRUE	==	MEM B DQ<18>	29
MEM A DQ<21>		MAKE_BASE=TRUE	==	MEM A DQ<21>	27	MEM B DQ<21>		MAKE_BASE=TRUE	==	MEM B DQ<16>	29
MEM A DQ<20>		MAKE_BASE=TRUE	==	MEM A DQ<20>	27	MEM B DQ<20>		MAKE_BASE=TRUE	==	MEM B DQ<17>	29
MEM A DQ<19>		MAKE_BASE=TRUE	==	MEM A DQ<18>	27	MEM B DQ<19>		MAKE_BASE=TRUE	==	MEM B DQ<22>	29
MEM A DQ<18>		MAKE_BASE=TRUE	==	MEM A DQ<19>	27	MEM B DQ<18>		MAKE_BASE=TRUE	==	MEM B DQ<19>	29
MEM A DQ<17>		MAKE_BASE=TRUE	==	MEM A DQ<16>	27	MEM B DQ<17>		MAKE_BASE=TRUE	==	MEM B DQ<21>	29
MEM A DQ<16>		MAKE_BASE=TRUE	==	MEM A DQ<17>	27	MEM B DQ<16>		MAKE_BASE=TRUE	==	MEM B DQ<20>	29
CPU CHANNEL A DQS 3 -> DIMM A DQS 3											
MEM A DQS N<3>		MAKE_BASE=TRUE	==	MEM A DQS N<3>	27	MEM B DQS N<3>		MAKE_BASE=TRUE	==	MEM B DQS N<3>	29
MEM A DQS P<3>		MAKE_BASE=TRUE	==	MEM A DQS P<3>	27	MEM B DQS P<3>		MAKE_BASE=TRUE	==	MEM B DQS P<3>	29
		MAKE_BASE=TRUE	==	GND				MAKE_BASE=TRUE	==	GND	
MEM A DQ<31>		MAKE_BASE=TRUE	==	MEM A DQ<26>	27	MEM B DQ<31>		MAKE_BASE=TRUE	==	MEM B DQ<26>	29
MEM A DQ<30>		MAKE_BASE=TRUE	==	MEM A DQ<24>	27	MEM B DQ<30>		MAKE_BASE=TRUE	==	MEM B DQ<30>	29
MEM A DQ<29>		MAKE_BASE=TRUE	==	MEM A DQ<28>	27	MEM B DQ<29>		MAKE_BASE=TRUE	==	MEM B DQ<28>	29
MEM A DQ<28>		MAKE_BASE=TRUE	==	MEM A DQ<25>	27	MEM B DQ<28>		MAKE_BASE=TRUE	==	MEM B DQ<29>	29
MEM A DQ<27>		MAKE_BASE=TRUE	==	MEM A DQ<31>	27	MEM B DQ<27>		MAKE_BASE=TRUE	==	MEM B DQ<27>	29
MEM A DQ<26>		MAKE_BASE=TRUE	==	MEM A DQ<27>	27	MEM B DQ<26>		MAKE_BASE=TRUE	==	MEM B DQ<31>	29
MEM A DQ<25>		MAKE_BASE=TRUE	==	MEM A DQ<30>	27	MEM B DQ<25>		MAKE_BASE=TRUE	==	MEM B DQ<25>	29
MEM A DQ<24>		MAKE_BASE=TRUE	==	MEM A DQ<29>	27	MEM B DQ<24>		MAKE_BASE=TRUE	==	MEM B DQ<24>	29
CPU CHANNEL A DQS 4 -> DIMM A DQS 4											
MEM A DQS N<4>		MAKE_BASE=TRUE	==	MEM A DQS N<4>	27	MEM B DQS N<4>		MAKE_BASE=TRUE	==	MEM B DQS N<4>	29
MEM A DQS P<4>		MAKE_BASE=TRUE	==	MEM A DQS P<4>	27	MEM B DQS P<4>		MAKE_BASE=TRUE	==	MEM B DQS P<4>	29
		MAKE_BASE=TRUE	==	GND				MAKE_BASE=TRUE	==	GND	
MEM A DQ<39>		MAKE_BASE=TRUE	==	MEM A DQ<38>	27	MEM B DQ<39>		MAKE_BASE=TRUE	==	MEM B DQ<38>	29
MEM A DQ<38>		MAKE_BASE=TRUE	==	MEM A DQ<39>	27	MEM B DQ<38>		MAKE_BASE=TRUE	==	MEM B DQ<39>	29
MEM A DQ<37>		MAKE_BASE=TRUE	==	MEM A DQ<37>	27	MEM B DQ<37>		MAKE_BASE=TRUE	==	MEM B DQ<37>	29
MEM A DQ<36>		MAKE_BASE=TRUE	==	MEM A DQ<33>	27	MEM B DQ<36>		MAKE_BASE=TRUE	==	MEM B DQ<37>	29
MEM A DQ<35>		MAKE_BASE=TRUE	==	MEM A DQ<34>	27	MEM B DQ<35>		MAKE_BASE=TRUE	==	MEM B DQ<34>	29
MEM A DQ<34>		MAKE_BASE=TRUE	==	MEM A DQ<35>	27	MEM B DQ<34>		MAKE_BASE=TRUE	==	MEM B DQ<35>	29
MEM A DQ<33>		MAKE_BASE=TRUE	==	MEM A DQ<32>	27	MEM B DQ<33>		MAKE_BASE=TRUE	==	MEM B DQ<32>	29
MEM A DQ<32>		MAKE_BASE=TRUE	==	MEM A DQ<36>	27	MEM B DQ<32>		MAKE_BASE=TRUE	==	MEM B DQ<36>	29
CPU CHANNEL A DQS 5 -> DIMM A DQS 5											
MEM A DQS N<5>		MAKE_BASE=TRUE	==	MEM A DQS N<5>	27	MEM B DQS N<5>		MAKE_BASE=TRUE	==	MEM B DQS N<5>	29
MEM A DQS P<5>		MAKE_BASE=TRUE	==	MEM A DQS P<5>	27	MEM B DQS P<5>		MAKE_BASE=TRUE	==	MEM B DQS P<5>	29
		MAKE_BASE=TRUE	==	GND				MAKE_BASE=TRUE	==	GND	
MEM A DQ<47>		MAKE_BASE=TRUE	==	MEM A DQ<46>	27	MEM B DQ<47>		MAKE_BASE=TRUE	==	MEM B DQ<43>	29
MEM A DQ<46>		MAKE_BASE=TRUE	==	MEM A DQ<43>	27	MEM B DQ<46>		MAKE_BASE=TRUE	==	MEM B DQ<46>	29
MEM A DQ<45>		MAKE_BASE=TRUE	==	MEM A DQ<45>	27	MEM B DQ<45>		MAKE_BASE=TRUE	==	MEM B DQ<40>	29
MEM A DQ<44>		MAKE_BASE=TRUE	==	MEM A DQ<41>	27	MEM B DQ<44>		MAKE_BASE=TRUE	==	MEM B DQ<45>	29
MEM A DQ<43>		MAKE_BASE=TRUE	==	MEM A DQ<47>	27	MEM B DQ<43>		MAKE_BASE=TRUE	==	MEM B DQ<47>	29
MEM A DQ<42>		MAKE_BASE=TRUE	==	MEM A DQ<42>	27	MEM B DQ<42>		MAKE_BASE=TRUE	==	MEM B DQ<42>	29
MEM A DQ<41>		MAKE_BASE=TRUE	==	MEM A DQ<40>	27	MEM B DQ<41>		MAKE_BASE=TRUE	==	MEM B DQ<41>	29
MEM A DQ<40>		MAKE_BASE=TRUE	==	MEM A DQ<44>	27	MEM B DQ<40>		MAKE_BASE=TRUE	==	MEM B DQ<44>	29
CPU CHANNEL A DQS 6 -> DIMM A DQS 6											
MEM A DQS N<6>		MAKE_BASE=TRUE	==	MEM A DQS N<6>	27	MEM B DQS N<6>		MAKE_BASE=TRUE	==	MEM B DQS N<6>	29
MEM A DQS P<6>		MAKE_BASE=TRUE	==	MEM A DQS P<6>	27	MEM B DQS P<6>		MAKE_BASE=TRUE	==	MEM B DQS P<6>	29
		MAKE_BASE=TRUE	==	GND				MAKE_BASE=TRUE	==	GND	
MEM A DQ<55>		MAKE_BASE=TRUE	==	MEM A DQ<51>	27	MEM B DQ<55>		MAKE_BASE=TRUE	==	MEM B DQ<54>	29
MEM A DQ<54>		MAKE_BASE=TRUE	==	MEM A DQ<54>	27	MEM B DQ<54>		MAKE_BASE=TRUE	==	MEM B DQ<55>	29
MEM A DQ<53>		MAKE_BASE=TRUE	==	MEM A DQ<49>	27	MEM B DQ<53>		MAKE_BASE=TRUE	==	MEM B DQ<53>	29
MEM A DQ<52>		MAKE_BASE=TRUE	==	MEM A DQ<53>	27	MEM B DQ<52>		MAKE_BASE=TRUE	==	MEM B DQ<49>	29
MEM A DQ<51>		MAKE_BASE=TRUE	==	MEM A DQ<50>	27	MEM B DQ<51>		MAKE_BASE=TRUE	==	MEM B DQ<51>	29
MEM A DQ<50>		MAKE_BASE=TRUE	==	MEM A DQ<55>	27	MEM B DQ<50>		MAKE_BASE=TRUE	==	MEM B DQ<50>	29
MEM A DQ<49>		MAKE_BASE=TRUE	==	MEM A DQ<48>	27	MEM B DQ<49>		MAKE_BASE=TRUE	==	MEM B DQ<48>	29
MEM A DQ<48>		MAKE_BASE=TRUE	==	MEM A DQ<52>	27	MEM B DQ<48>		MAKE_BASE=TRUE	==	MEM B DQ<52>	29
CPU CHANNEL A DQS 7 -> DIMM A DQS 7											
MEM A DQS N<7>		MAKE_BASE=TRUE	==	MEM A DQS N<7>	27	MEM B DQS N<7>		MAKE_BASE=TRUE	==	MEM B DQS N<7>	29
MEM A DQS P<7>		MAKE_BASE=TRUE	==	MEM A DQS P<7>	27	MEM B DQS P<7>		MAKE_BASE=TRUE	==	MEM B DQS P<7>	29
		MAKE_BASE=TRUE	==	GND				MAKE_BASE=TRUE	==	GND	
CPU CHANNEL B DQS 1 -> DIMM B DQS 1											
MEM B DQS N<1>		MAKE_BASE=TRUE	==	MEM B DQS N<1>	29	MEM B DQS N<1>		MAKE_BASE=TRUE	==	MEM B DQS N<1>	29
MEM B DQS P<1>		MAKE_BASE=TRUE	==	MEM B DQS P<1>	29	MEM B DQS P<1>		MAKE_BASE=TRUE	==	MEM B DQS P<1>	29
		MAKE_BASE=TRUE	==	GND				MAKE_BASE=TRUE	==	GND	
MEM B DQ<15>		MAKE_BASE=TRUE	==	MEM B DQ<15>	29	MEM B DQ<15>		MAKE_BASE=TRUE	==	MEM B DQ<15>	29
MEM B DQ<14>		MAKE_BASE=TRUE	==	MEM B DQ<10>	29	MEM B DQ<14>		MAKE_BASE=TRUE	==	MEM B DQ<14>	29
MEM B DQ<13>		MAKE_BASE=TRUE	==	MEM B DQ<13>	29	MEM B DQ<13>		MAKE_BASE=TRUE	==	MEM B DQ<13>	29
MEM B DQ<12>		MAKE_BASE=TRUE	==	MEM B DQ<9>	29	MEM B DQ<12>		MAKE_BASE=TRUE	==	MEM B DQ<8>	29
MEM B DQ<11>		MAKE_BASE=TRUE	==	MEM B DQ<15>	29	MEM B DQ<11>		MAKE_BASE=TRUE	==	MEM B DQ<11>	29
MEM B DQ<10>		MAKE_BASE=TRUE	==	MEM B DQ<14>	29	MEM B DQ<10>		MAKE_BASE=TRUE	==	MEM B DQ<10>	29
MEM B DQ<9>		MAKE_BASE=TRUE	==	MEM B DQ<13>	29	MEM B DQ<9>		MAKE_BASE=TRUE	==	MEM B DQ<12>	29
MEM B DQ<8>		MAKE_BASE=TRUE	==	MEM B DQ<8>	29	MEM B DQ<8>		MAKE_BASE=TRUE	==	MEM B DQ<9>	29
CPU CHANNEL B DQS 2 -> DIMM B DQS 2											
MEM B DQS N<2>		MAKE_BASE=TRUE	==	MEM B DQS N<2>	29	MEM B DQS N<2>		MAKE_BASE=TRUE	==	MEM B DQS N<2>	29
MEM B DQS P<2>		MAKE_BASE=TRUE	==	MEM B DQS P<2>	29	MEM B DQS P<2>		MAKE_BASE=TRUE	==	MEM B DQS P<2>	29
		MAKE_BASE=TRUE	==	GND				MAKE_BASE=TRUE	==	GND	
MEM B DQ<23>		MAKE_BASE=TRUE	==	MEM B DQ<23>	29	MEM B DQ<23>		MAKE_BASE=TRUE	==	MEM B DQ<23>	29
MEM B DQ<22>		MAKE_BASE=TRUE	==	MEM B DQ<18>	29	MEM B DQ<22>		MAKE_BASE=TRUE	==	MEM B DQ<18>	29
MEM B DQ<21>		MAKE_BASE=TRUE	==	MEM B DQ<16>	29	MEM B DQ<21>		MAKE_BASE=TRUE	==	MEM B DQ<16>	29
MEM B DQ<20>		MAKE_BASE=TRUE	==	MEM B DQ<17>	29	MEM B DQ<20>		MAKE_BASE=TRUE	==	MEM B DQ<17>	29
MEM B DQ<19>		MAKE_BASE=TRUE	==	MEM B DQ<22>	29	MEM B DQ<19>		MAKE_BASE=TRUE	==	MEM B DQ<22>	29
MEM B DQ<18>		MAKE_BASE=TRUE	==	MEM B DQ<19>	29	MEM B DQ<18>		MAKE_BASE=TRUE	==	MEM B DQ<19>	29
MEM B DQ<17>		MAKE_BASE=TRUE	==	MEM B DQ<21>	29	MEM B DQ<17>		MAKE_BASE=TRUE	==	MEM B DQ<21>	29
MEM B DQ<16>		MAKE_BASE=TRUE	==	MEM B DQ<20>	29	MEM B DQ<16>		MAKE_BASE=TRUE	==	MEM B DQ<20>	29
CPU CHANNEL B DQS 3 -> DIMM B DQS 3											
MEM B DQS N<3>		MAKE_BASE=TRUE	==	MEM B DQS N<3>	29	MEM B DQS N<3>		MAKE_BASE=TRUE	==	MEM B DQS N<3>	29
MEM B DQS P<3>		MAKE_BASE=TRUE	==	MEM B DQS P<3>	29	MEM B DQS P<3>		MAKE_BASE=TRUE	==	MEM B DQS P<3>	29
		MAKE_BASE=TRUE	==	GND				MAKE_BASE=TRUE	==	GND	
MEM B DQ<31>		MAKE_BASE=TRUE	==	MEM B DQ<26>	29	MEM B DQ<31>		MAKE_BASE=TRUE	==	MEM B DQ<26>	29
MEM B DQ<30>		MAKE_BASE=TRUE	==	MEM B DQ<30>	29	MEM B DQ<30>		MAKE_BASE=TRUE	==	MEM B DQ<30>	29
MEM B DQ<29>		MAKE_BASE=TRUE	==	MEM B DQ<28>	29	MEM B DQ<29>		MAKE_BASE=TRUE	==	MEM B DQ<28>	29
MEM B DQ<28>		MAKE_BASE=TRUE	==	MEM B DQ<29>	29	MEM B DQ<28>		MAKE_BASE=TRUE	==	MEM B DQ<29>	29
MEM B DQ<27>		MAKE_BASE=TRUE	==	MEM B DQ<31>	29	MEM B DQ<27>		MAKE_BASE=TRUE	==	MEM B DQ<27>	29
MEM B DQ<26>		MAKE_BASE=TRUE	==	MEM B DQ<31>	29	MEM B DQ<26>		MAKE_BASE=TRUE	==	MEM B DQ<31>	29
MEM B DQ<25>		MAKE_BASE=TRUE	==	MEM B DQ<25>	29	MEM B DQ<25>		MAKE_BASE=TRUE	==	MEM B DQ<25>	29
MEM B DQ<24>		MAKE_BASE=TRUE	==	MEM B DQ<24>	29	MEM B DQ<24>		MAKE_BASE=TRUE	==	MEM B DQ<24>	29
CPU CHANNEL B DQS 4 -> DIMM B DQS 4											
MEM B DQS N<4>		MAKE_BASE=TRUE	==	MEM B DQS N<4>	29	MEM B DQS N<4>		MAKE_BASE=TRUE	==	MEM B DQS N<4>	29
MEM B DQS P<4>		MAKE_BASE=TRUE	==	MEM B DQS P<4>	29	MEM B DQS P<4>		MAKE_BASE=TRUE	==	MEM B DQS P<4>	29
		MAKE_BASE=TRUE	==	GND				MAKE_BASE=TRUE	==	GND	
MEM B DQ<39>		MAKE_BASE=TRUE	==	MEM B DQ<38>	29	MEM B DQ<39>		MAKE_BASE=TRUE	==	MEM B DQ<38>	29
MEM B DQ<38>		MAKE_BASE=TRUE	==	MEM B DQ<39>	29	MEM B DQ<38>		MAKE_BASE=TRUE	==	MEM B DQ<39>	29
MEM B DQ<37>		MAKE_BASE=TRUE	==	MEM B DQ<37>	29	MEM B DQ<37>		MAKE_BASE=TRUE	==	MEM B DQ<37>	29
MEM B DQ<36>		MAKE_BASE=TRUE	==	MEM B DQ<37>	29	MEM B DQ<36>		MAKE_BASE=TRUE	==	MEM B DQ<37>	29
MEM B DQ<35>		MAKE_BASE=TRUE	==	MEM B DQ<34>	29	MEM B DQ<35>		MAKE_BASE=TRUE	==	MEM B DQ<34>	29
MEM B DQ<34>		MAKE_BASE=TRUE	==	MEM B DQ<35>	29	MEM B DQ<34>		MAKE_BASE=TRUE	==	MEM B DQ<35>	29
MEM B DQ<33>		MAKE_BASE=TRUE	==	MEM B DQ<32>	29	MEM B DQ<33>		MAKE_BASE=TRUE	==	MEM B DQ<32>	29
MEM B DQ<32>		MAKE_BASE=TRUE	==	MEM B DQ<36>	29	MEM B DQ<					

Page Notes

Power aliases required by this page:
- ~PP1V5_S3_MEM_B
- ~PP1V5_S3_MEM_B
- ~PP0V75_S3_MEM_VTT_B
- ~PPSPD_S3_MEM_B (2.5 - 3.3V)
Signal aliases required by this page:
- ~I2C_S0D1MMB_SCL
- ~I2C_S0D1MMB_SDA
BOM options provided by this page:
(None)

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

72 67 30 27 7 6 PP1V5_S3

72 67 30 27 7 6 PP1V5_S3

31 9 PP0V75_S3_MEM_VREFDQ_B

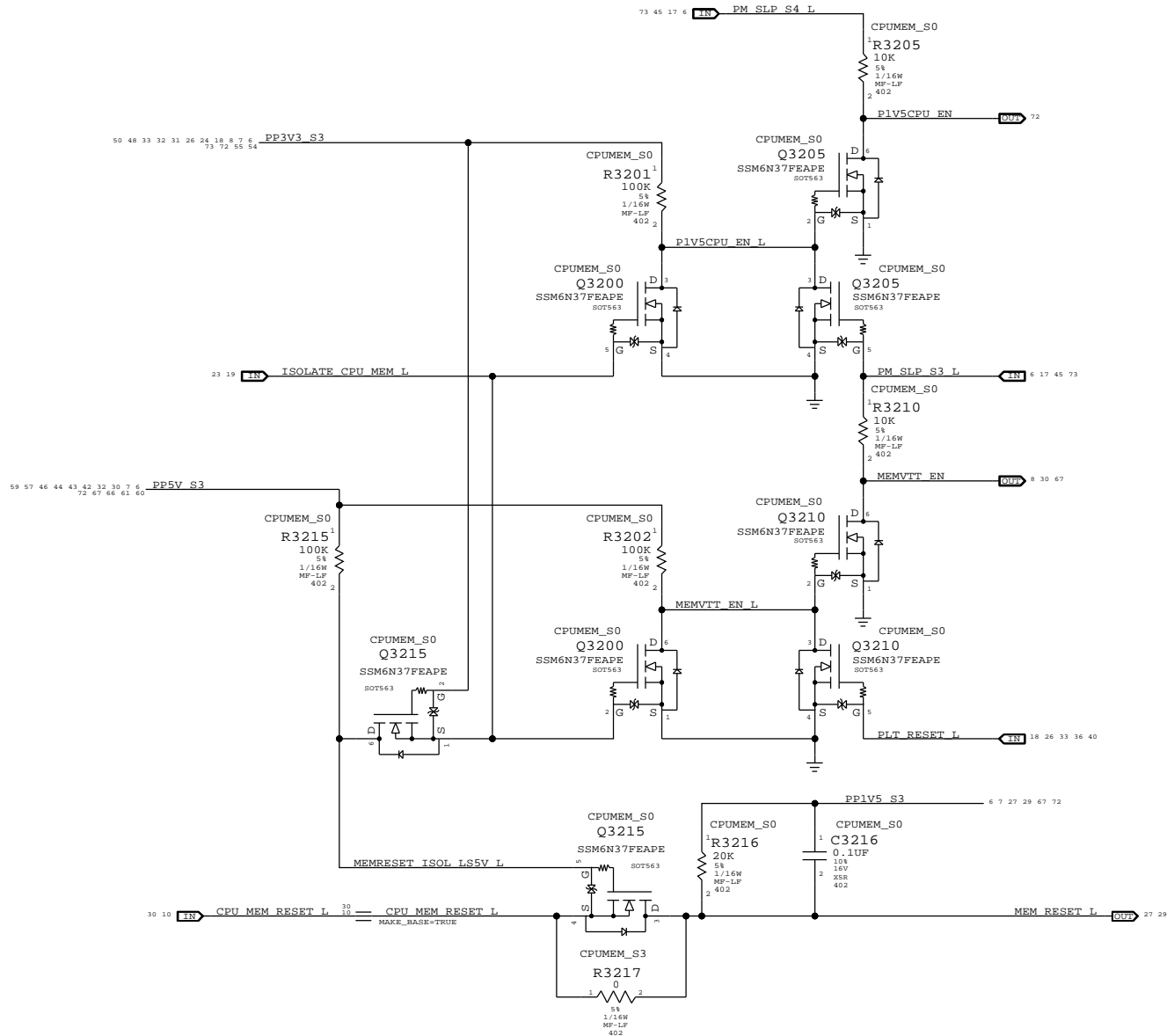
516S0806

"Expansion" (bottom) slot

SYNC MASTER=MASTER		SYNC DATE=MASTER	
PAGE TITLE			
DDR3 SO-DIMM Connector B			
DRAWING NUMBER		SIZE	
REVISION		D	
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PAGE		31 OF 109	
SHEET		29 OF 86	

WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

```
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L
```

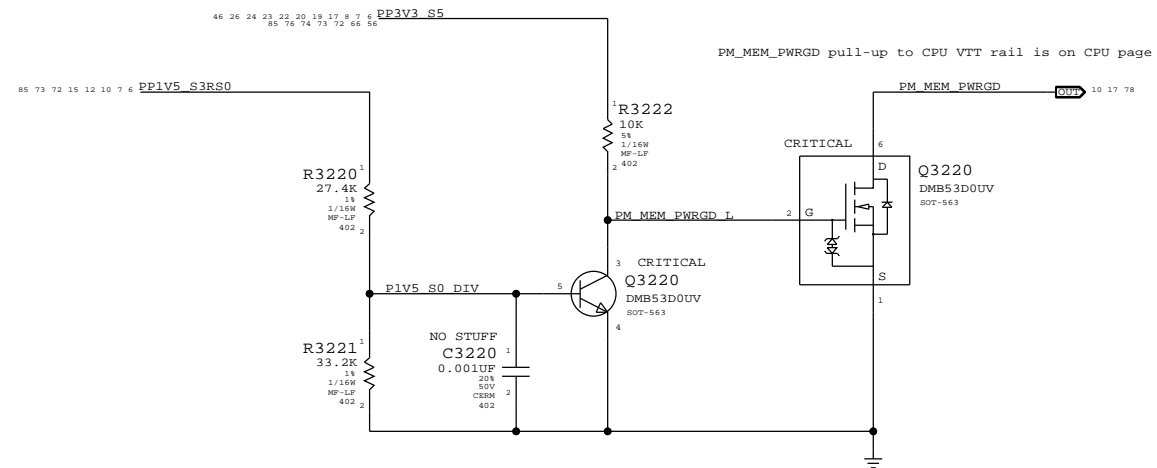


Step	SOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	Plv5CPU_EN		
S0	0	1	1	1	1	CPU_MEM_RESET_L	1	1		
	1	0	1	1	1	1	1	1		
to	2	0	0	1	1	1	0	1		
	3	0	0	0	1	X	1	0	0	
S3	4	0	0	1	1	X	1	0	1	
	5	0	1	1	1	0 (*)	1	1	1	
to	6	0	1	1	1	1	1	1	1	
S0	7	1	1	1	1	CPU_MEM_RESET_L	1	1	1	

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

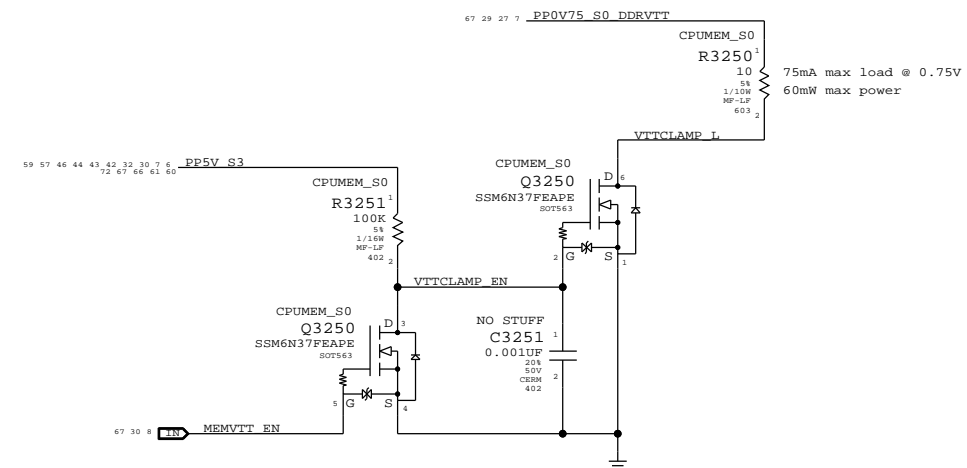
NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

```
1V5 S0 "PGOOD" for CPU
```



MEMVTT Clamp

Ensures CKE signals are held low in S3



D

C

B

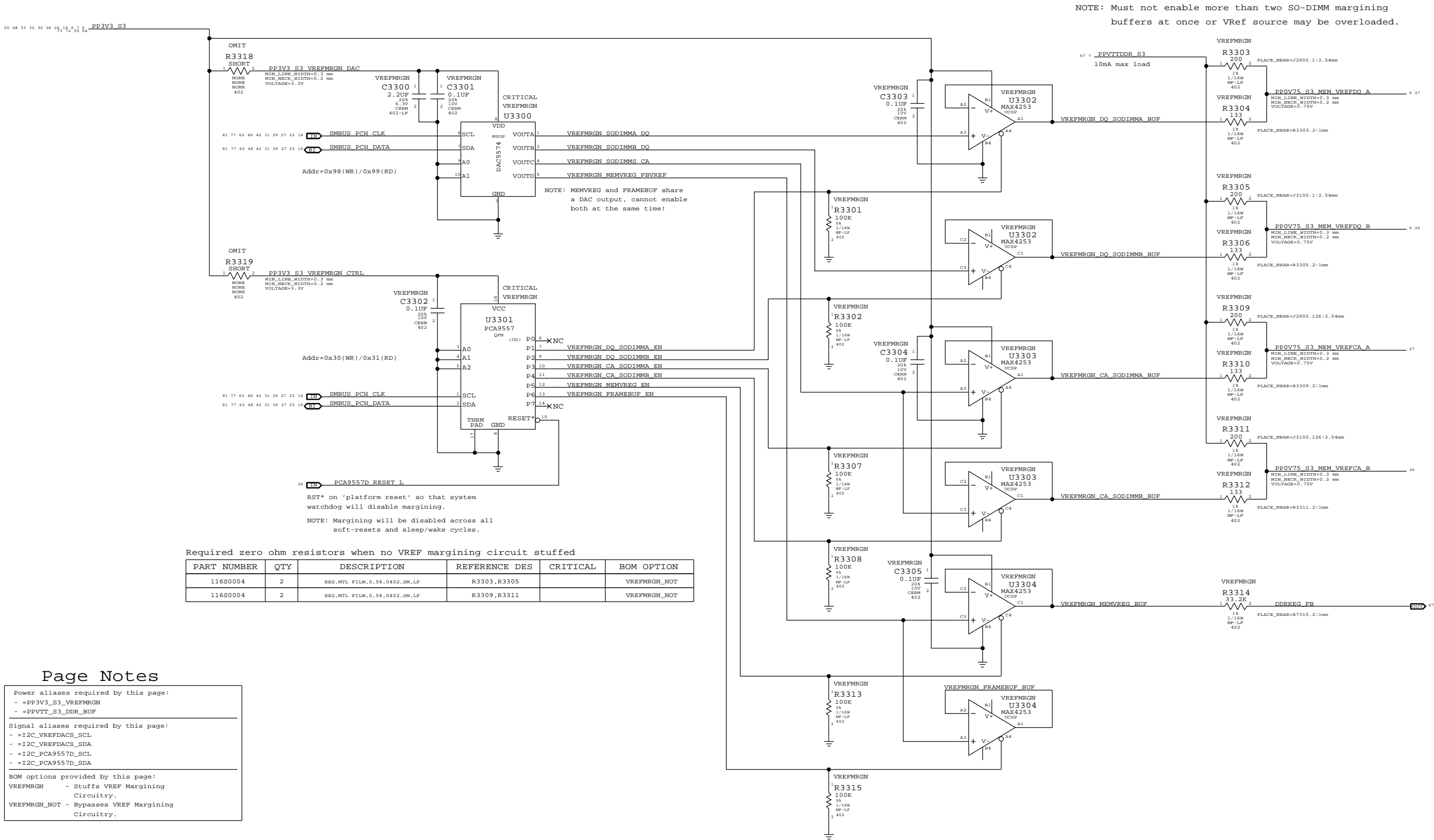
A

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A



Page Notes

Power aliases required by this page:

- PP3V3_S3_VREFMRGN
- PPVTT_S3_DDR_BUF


Signal aliases required by this page:

- I2C_VREFDACS_SCL
- I2C_VREFDACS_SDA
- I2C_PCA9557D_SCL
- I2C_PCA9557D_SDA

BOM options provided by this page:

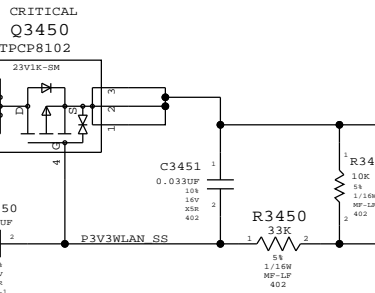
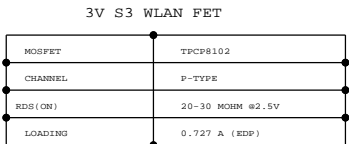
- VREFMRGN - Stuffs VREF Margining Circuitry.
- VREFMRGN_NOT - Bypasses VREF Margining Circuitry.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% Vref)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value		0.75V (DAC: 0x3A)			1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:		0.300V - 1.200V (+/- 450mV)			1.998V - 1.002V (+/- 498mV)	1.056V - 1.442V (+/- 180mV)
DAC range:		0.000V - 1.501V (0x00 - 0x74)			0.000V - 1.501V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
Vref current:		+3.4mA - -3.4mA (- = sourced)			+33uA - -33uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:		7.69mV / step @ output			8.59mV / step @ output	1.51mV / step @ output

SYNC MASTER=K91 MLB		SYNC DATE=06/01/2010	
PAGE TITLE			
FSB/DDR3/FRAMEBUF Vref Margining		DRAWING NUMBER	
 Apple Inc.		SIZE D	
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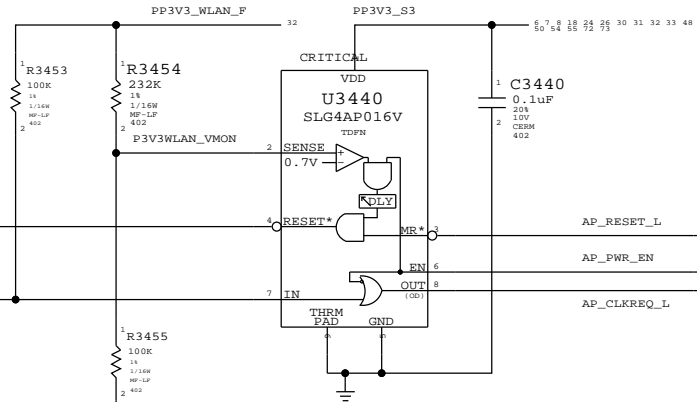



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0002	4	RES, 0ohm, 0201	L3470, L3471, L3472, L3473		



Supervisor & CLKFREG # ISolation

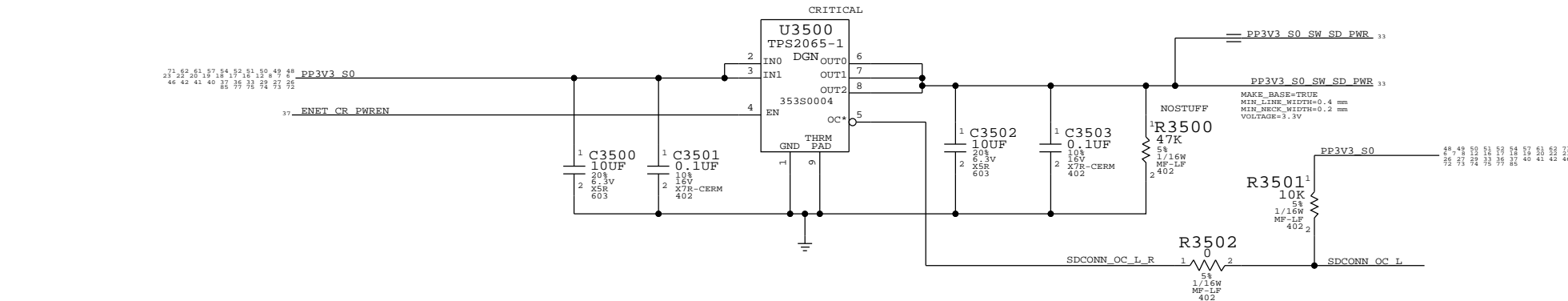
Delay = 60 ms +/- 20%



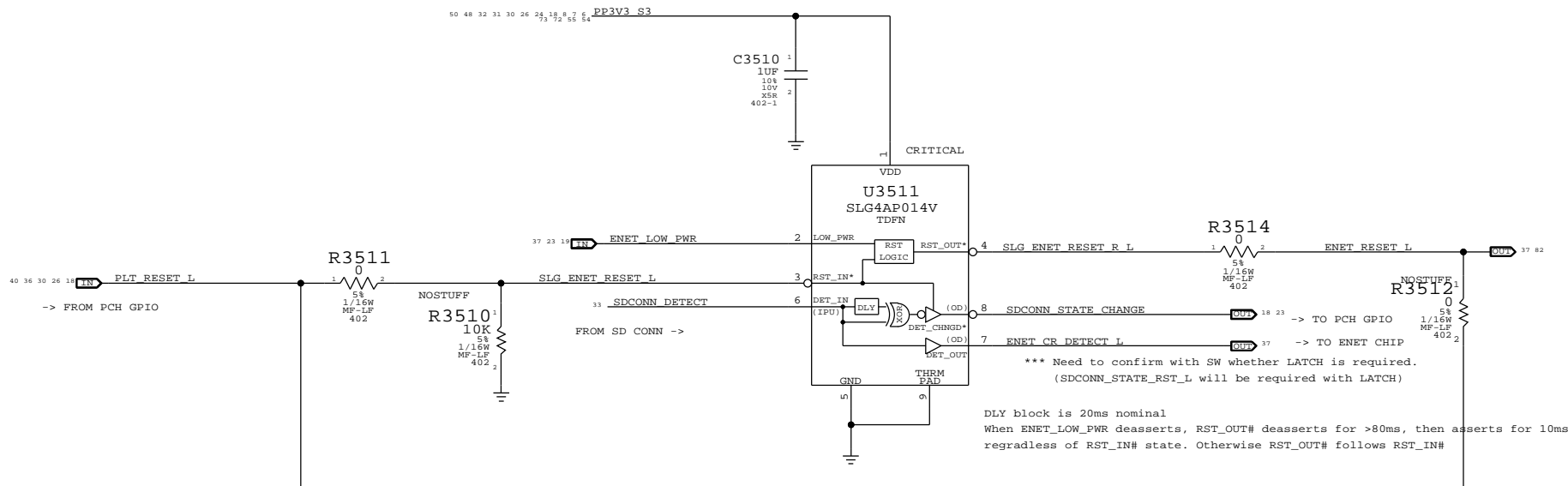
SYNCH MASTER=K91 MLB		SYNCH DATE=05/15/2010	
PAGE TITLE			
X19/ALS CAMERA CONNECTOR			
 Apple Inc.		DRAWING NUMBER <div style="border: 1px solid black; height: 20px; width: 100%;"></div>	
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SD CARD 3.3V OVERCURRENT PROTECTION CHIP WITH ACTIVE LOAD DISCHARGE

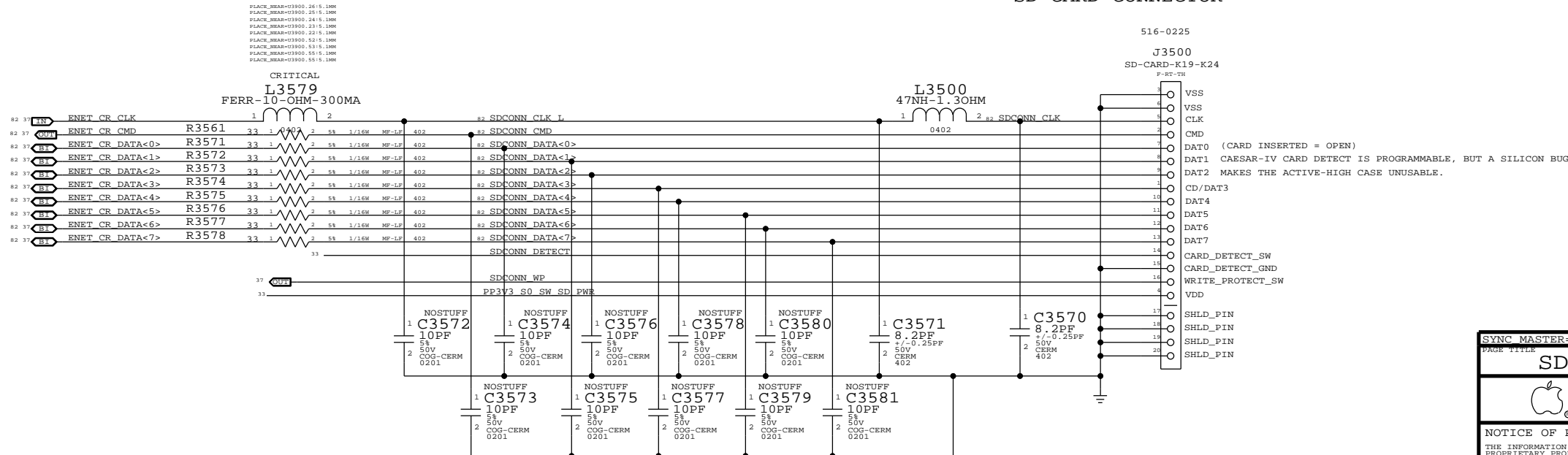
TPS2065-1 (1.0A limit) has active load discharge so R4810 is NOSTUFF.



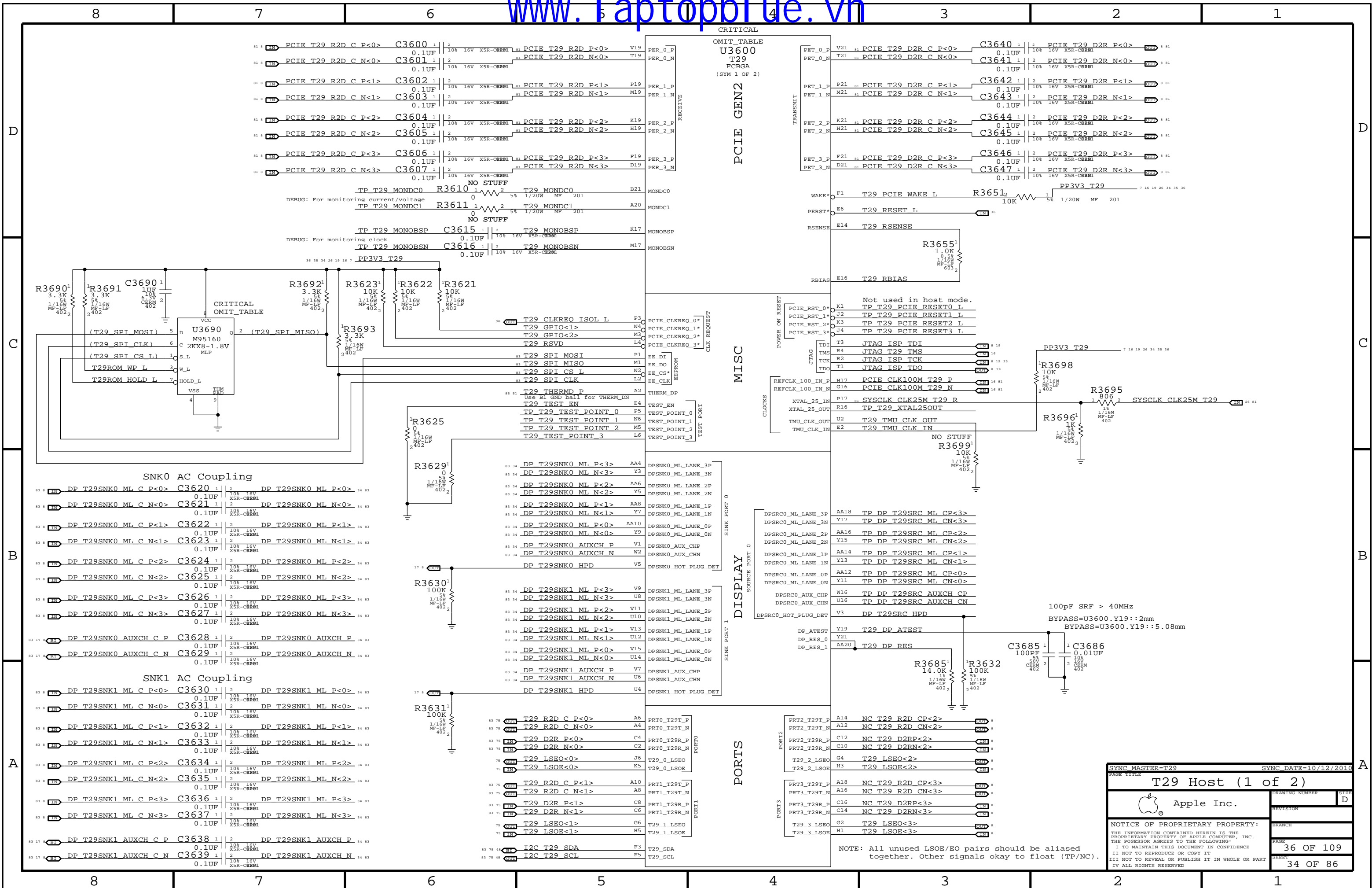
SDCONN DETECT DEBOUNCE. ENET_RESET AND DETECT-CHANGED PCH GPIO PULSE GENERATION.



SD CARD CONNECTOR



SYNC MASTER=K91_MLB		SYNC DATE=05/26/2010	
SD READER CONNECTOR			
Apple Inc.		DRAWING NUMBER	SIZE
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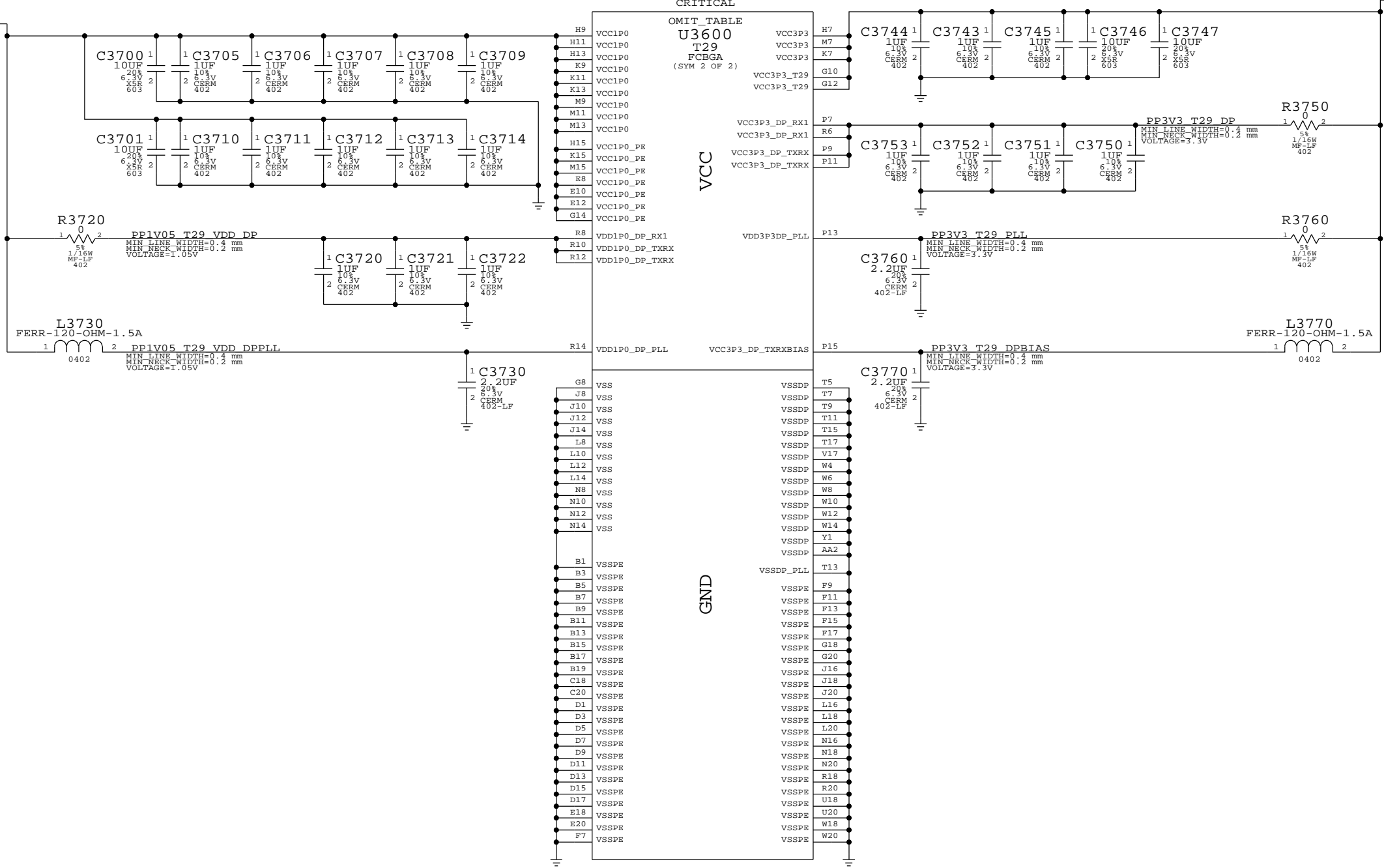
A

8 7 6 5 4 3 2 1

36 7 PP1V05 T29
2100 mA (Single Port)
2250 mA (Dual Port)
EDP: 3000 mA

PP3V3 T29 7 16 19 26 34 36
135 mA (Single-Port)
152 mA (Dual-Port)
EDP: 200 mA

0-ohms are placeholders for now, replace with proper values after characterization.



8 7 6 5 4 3 2 1

SYNC MASTER=T29		SYNC DATE=10/12/2010	
PAGE TITLE			
T29 Host (2 of 2)			
Apple Inc.		DRAWING NUMBER	SIZE
		REVISION	D
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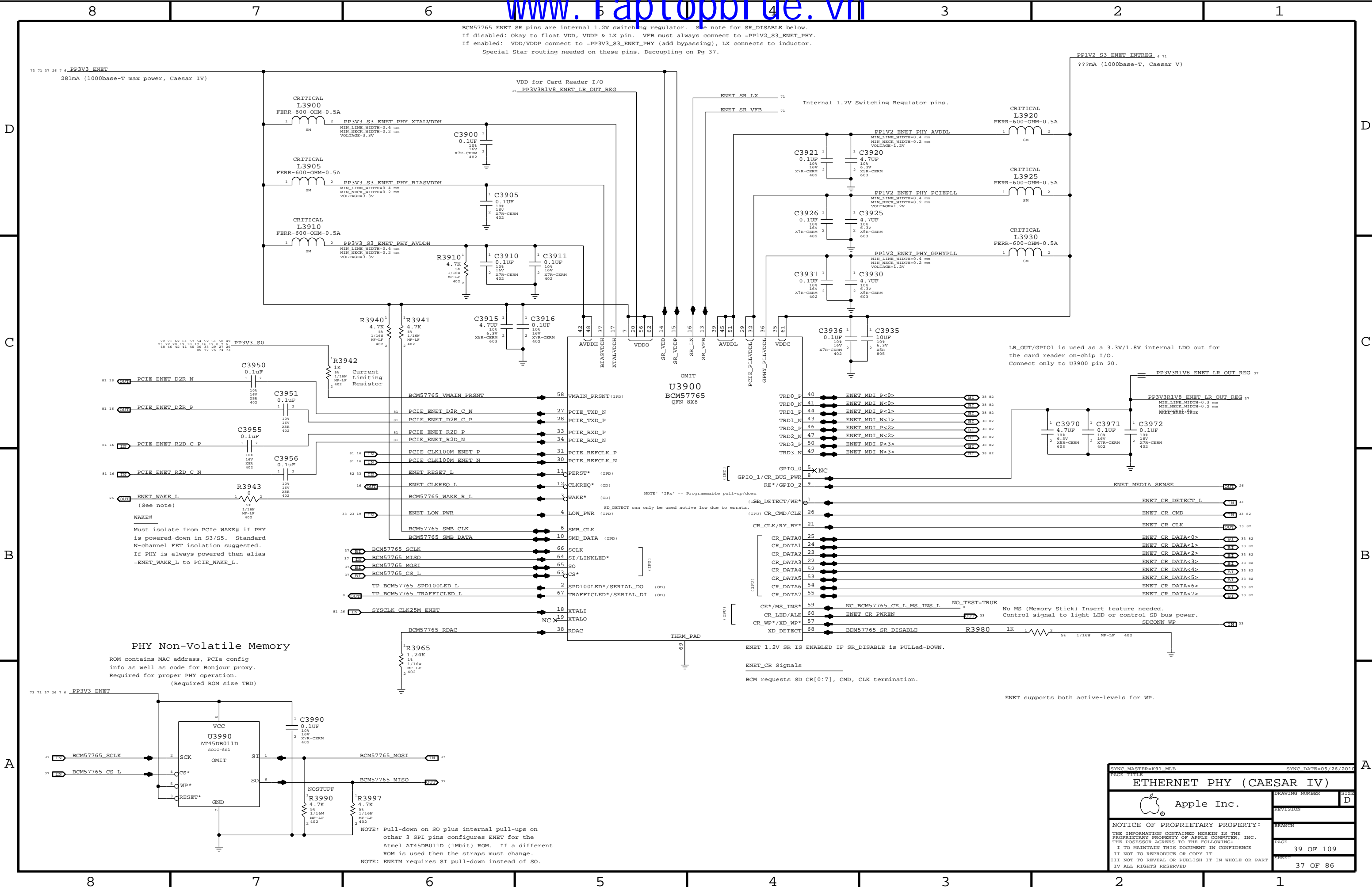
B



A



8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---

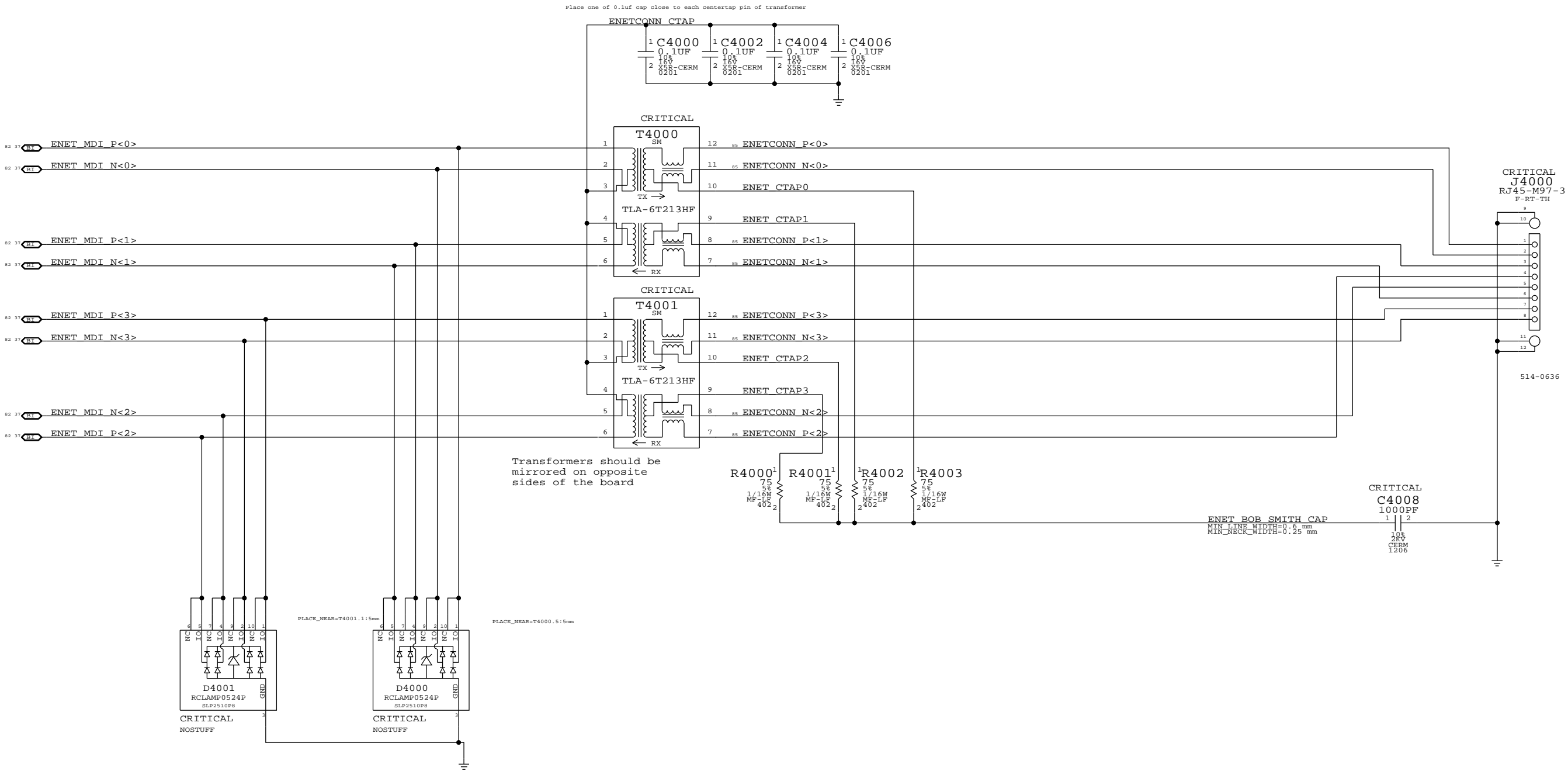


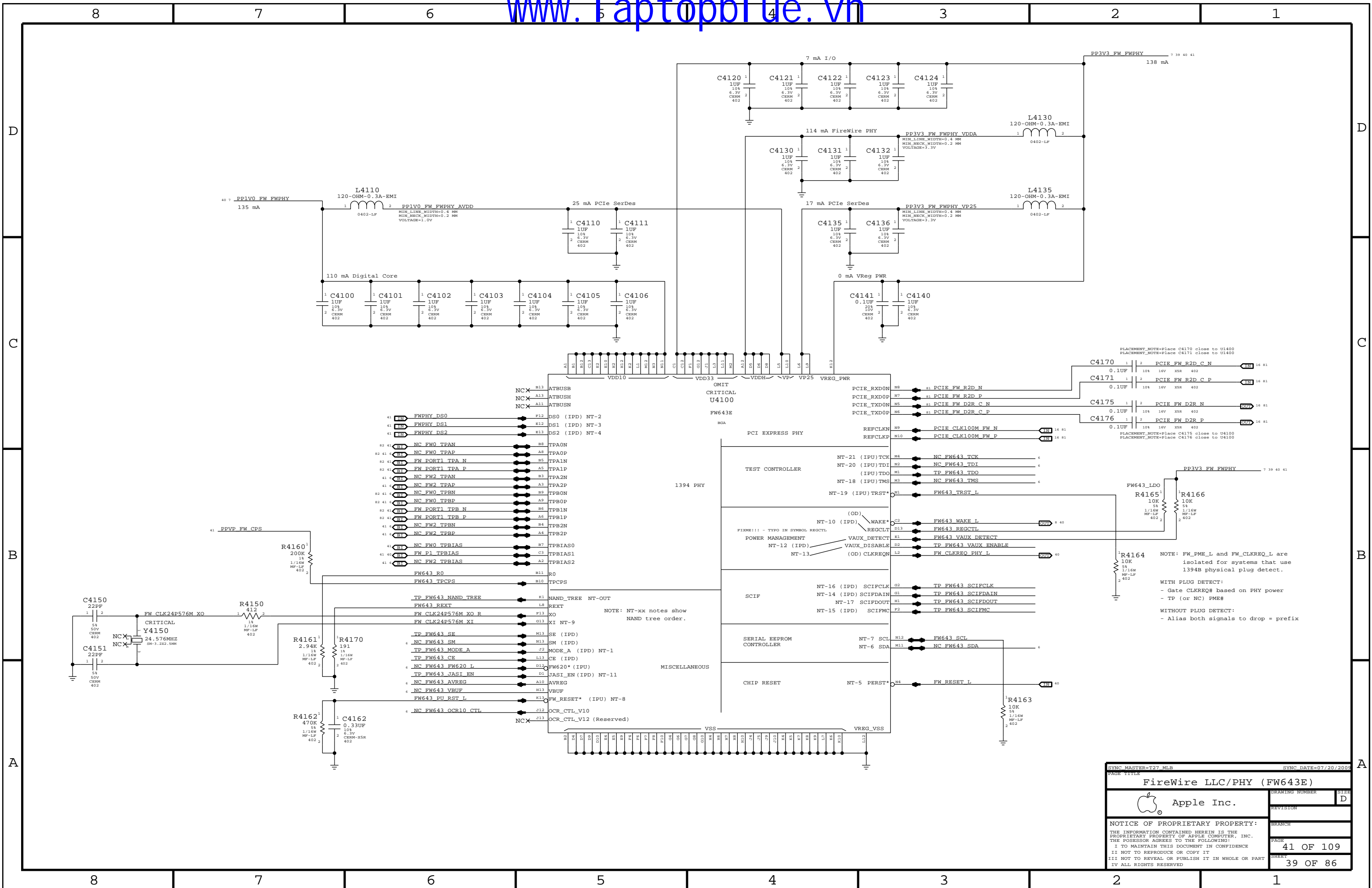
Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)





Page Notes

Power aliases required by this page:

- =PPBUS_S5_FWPWRSW (FW VP FET Input)
- =PPBUS_FW_FET (FW VP FET Output)
- =PP3V3_FW_P3V3FWFET (3.3V FET Input)
- =PP3V3_FW_FET (3.3V FET Output)
- =PP3V3_FW_FWPHY (PHY 3.3V Power)
- =PP3V3_S0_FWLATEVG
- =PP3V3_S0_FWPWRCTL (5KPD Bias Rail)
- =PP1V05_S0_FWPWRCTL (5KPD Bias Rail)
- =PP1V05_FW_P1V0FWFET (1.0V FET Input)
- =PP1V0_FW_FET_R (1.0V FET Output)
- =PP1V0_FW_FWPHY (PHY 1.0V)

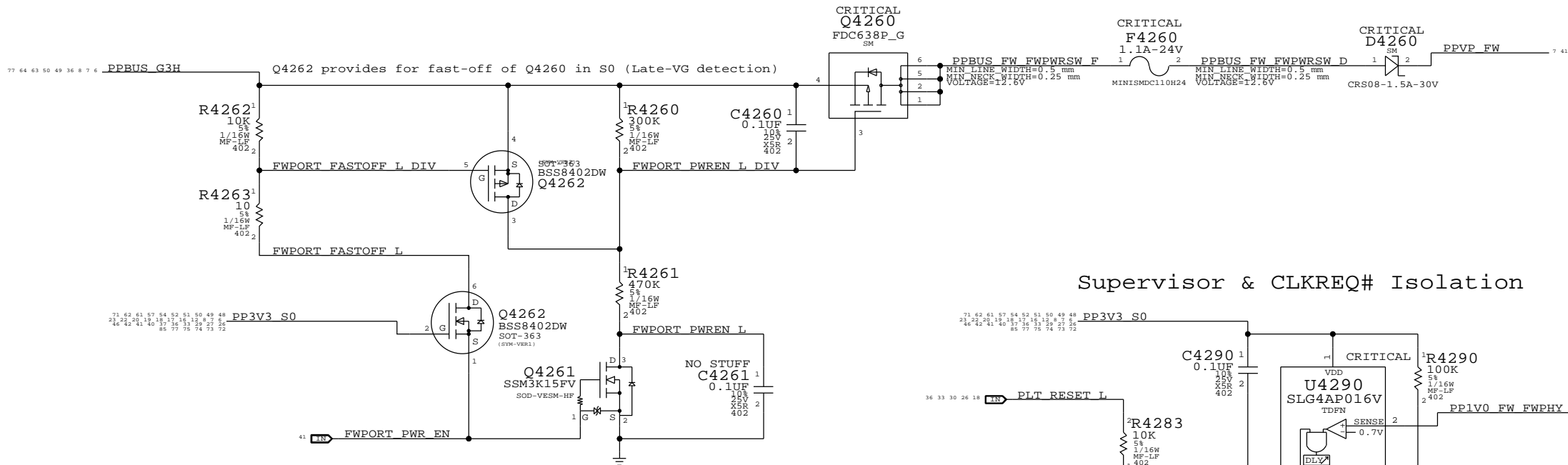
Signal aliases required by this page:

- =FW_CLKREQ_L
- =FW_PME_L

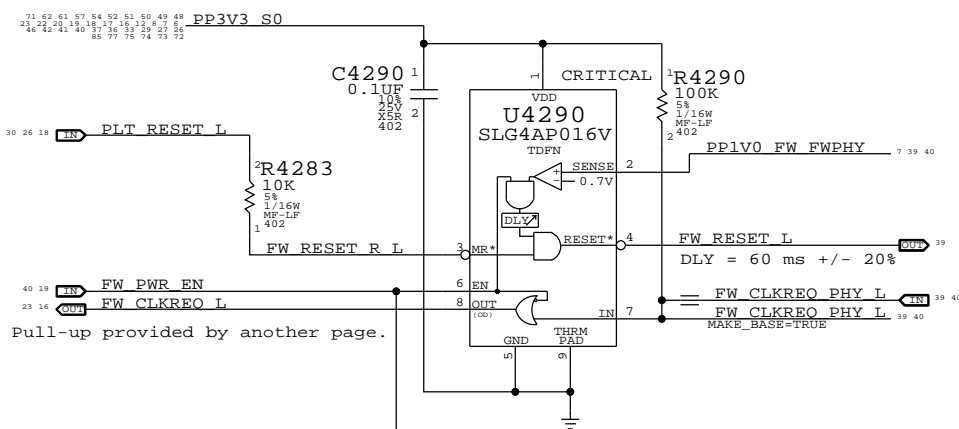
BOM options provided by this page:

(NONE)

FireWire Port Power Switch

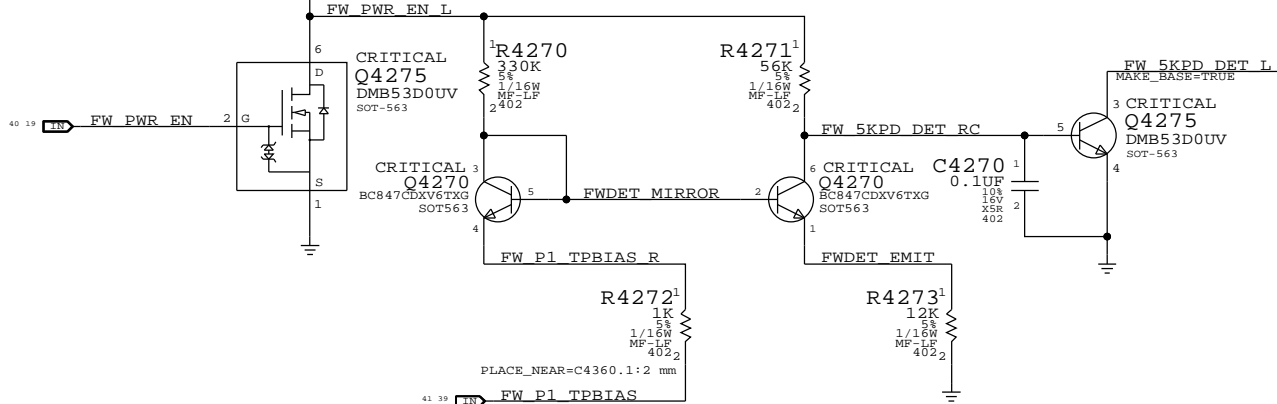


Supervisor & CLKREQ# Isolation



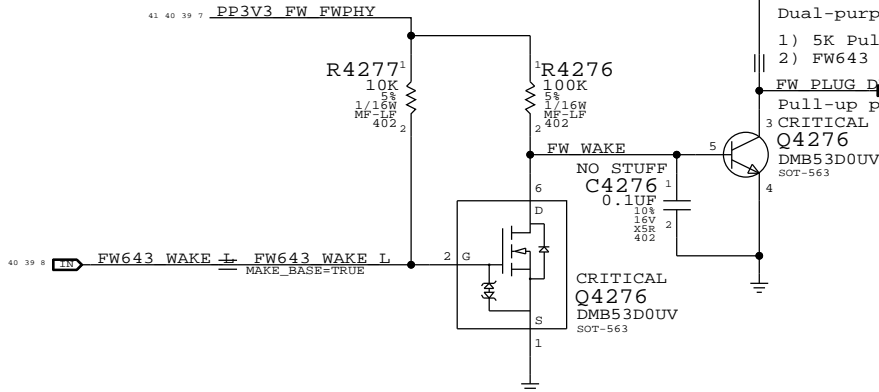
FireWire Port 5K Pull-Down Detect

All FireWire devices require 5K pull-down on TPB pair.
Host can detect as load on TPBIAS signal.
Current source only active when FW_PWR_EN is low.



FireWire PHY WAKE# Support

When PHY is powered, FW_5KPD_DET_L acts as legacy PME# signal.

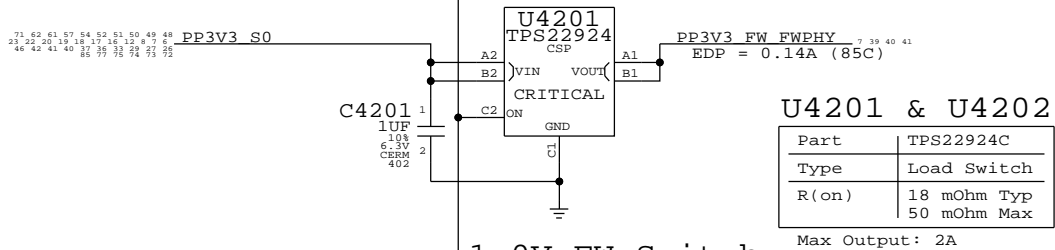


Dual-purpose output:

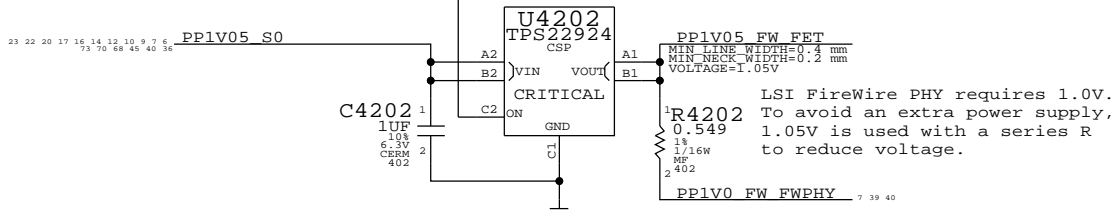
- 1) 5K Pull-down Detect when FW_PWR_EN is low.
- 2) FW643 WAKE# (PME#) when PHY is powered.

Pull-up provided on another page.

3.3V FW Switch



1.0V FW Switch



TEXT NOTE FOR 3.3V RAIL CURRENT CHANGED TO EDP NUMBER.

SYNC MASTER=T27 MLB		SYNC DATE=12/15/2009	
PAGE TITLE		FireWire Port & PHY Power	
Apple Inc.		DRAWING NUMBER	SIZE D
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Page Notes

Power aliases required by this page:

- =PPVP_FW_PORT1
- =PPVP_FW_PHY_CPS_FET (From Port)
- =PPVP_FW_PHY_CPS (To PHY)
- =PP3V3_FW_FWPHY
- =PP3V3_S0_FWLATEVG

Signal aliases required by this page:

- =FW_PHY_DS0
- =FW_PHY_DS1
- =FW_PHY_DS2

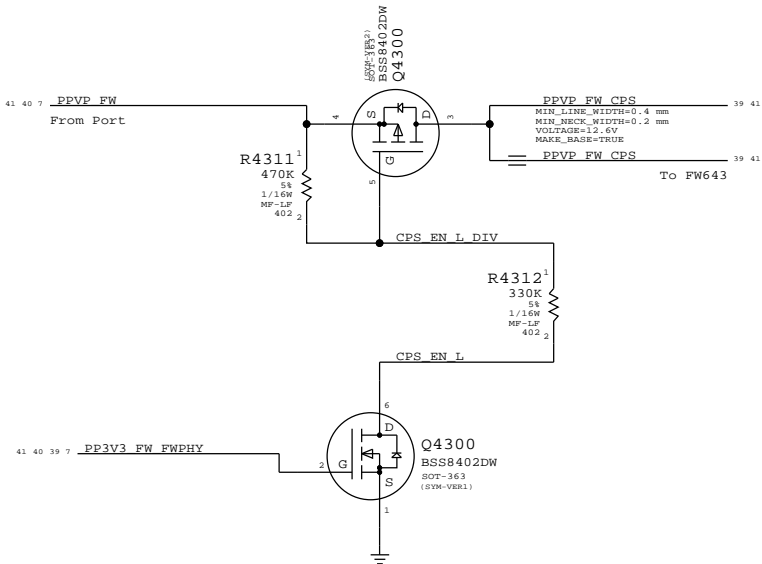
NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:

- (NONE)
- 1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

FW643 TPCPS Leakage Protection

FW643 has internal leakage path from TPCPS pin to VDD33.
FET blocks current to TPCPS until VDD33 is powered.



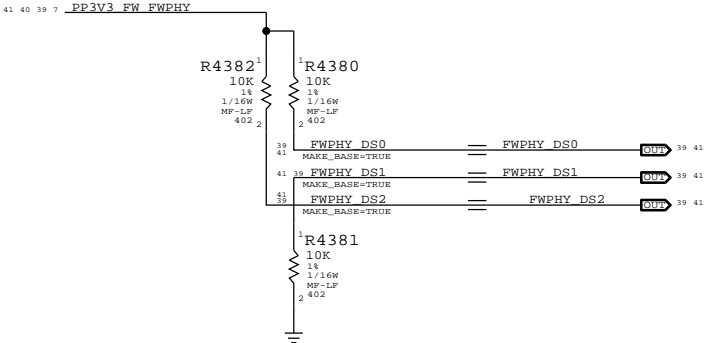
Unused FireWire Ports

Disabled per LSI instructions
(All unused port signals TP/NC)



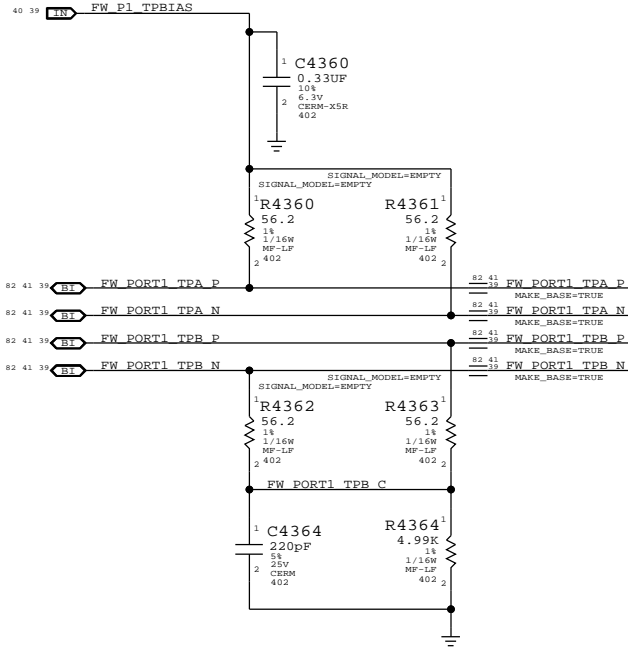
FireWire PHY Config Straps

Configures PHY for:
- Port "1" Bilingual (1394B)

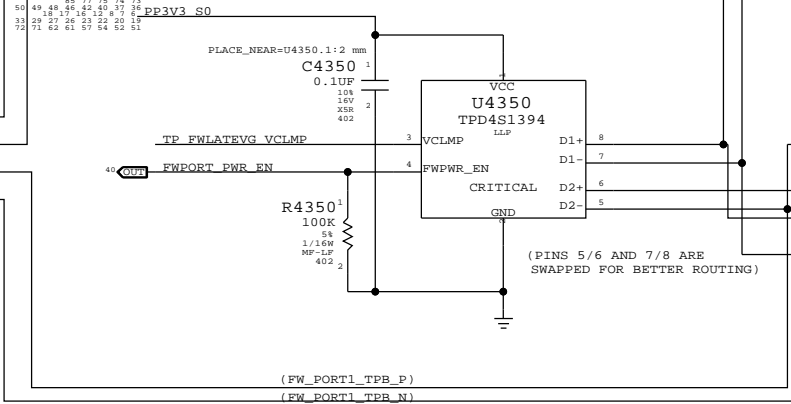


Termination

Place close to FireWire PHY

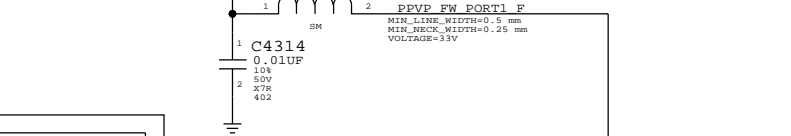


"Snapback" & "Late VG" Protection



Cable Power

Note: Trace PPVP_FW_PORT1 must handle up to 5A



PORT 1

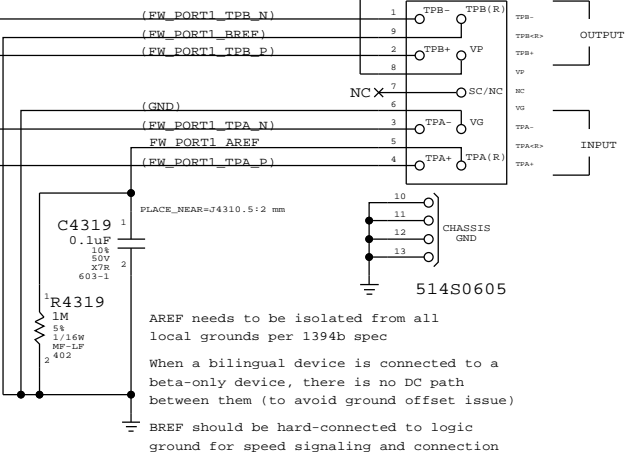
BILINGUAL

CRITICAL

J4310

1394B-M97

F-RT-TH

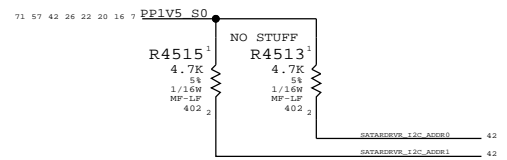
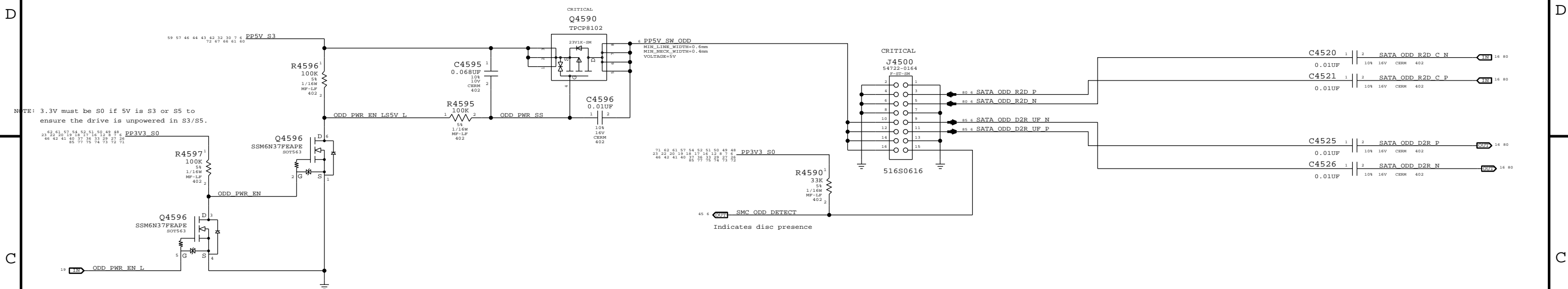


CANNOT SYNC THIS PAGE FROM T27, TPA AND TPB FOR U4350 IS SWAPPED

SYNC MASTER=T27 MLB		SYNC DATE=07/28/2005	
PAGE TITLE		PAGE	
FireWire Connector		DRAWING NUMBER	SIZE
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ODD Power Control

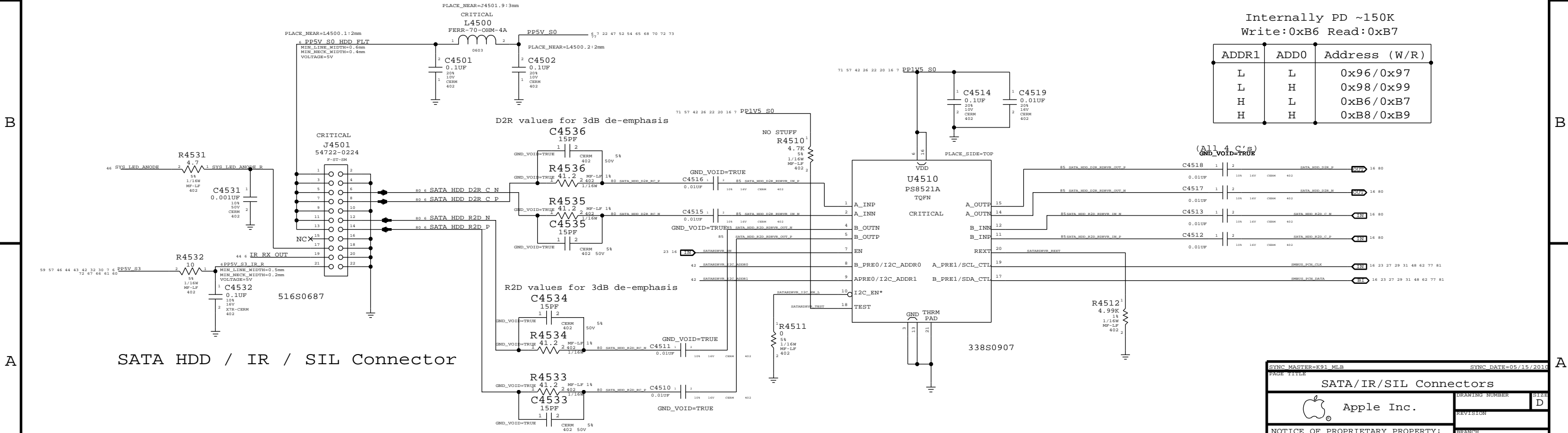
SATA ODD Connector



Internally PD ~150K
Write:0xB6 Read:0xB7

ADDR1	ADD0	Address (W/R)
L	L	0x96/0x97
L	H	0x98/0x99
H	L	0xB6/0xB7
H	H	0xB8/0xB9

SATA HDD / IR / SIL Connector



SYNC MASTER=K91 MLB

SYNC DATE=05/15/2010

SATA/IR/SIL Connectors

Apple Inc.

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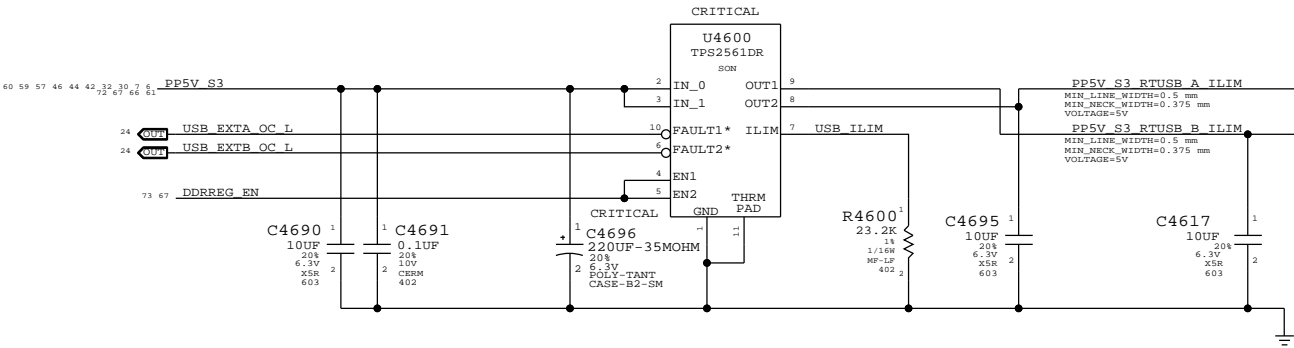
DRAWING NUMBER

45 OF 109

REVISION

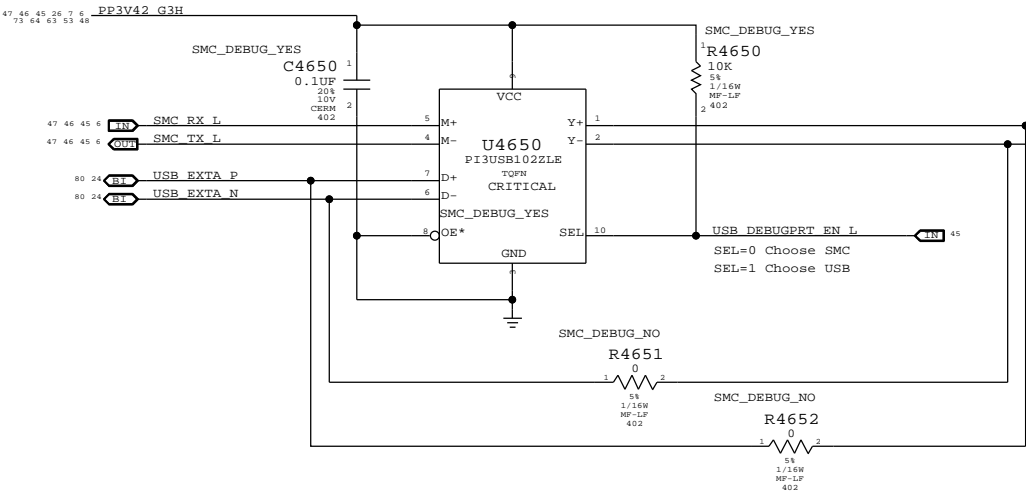
42 OF 86

USB Port Power Switch

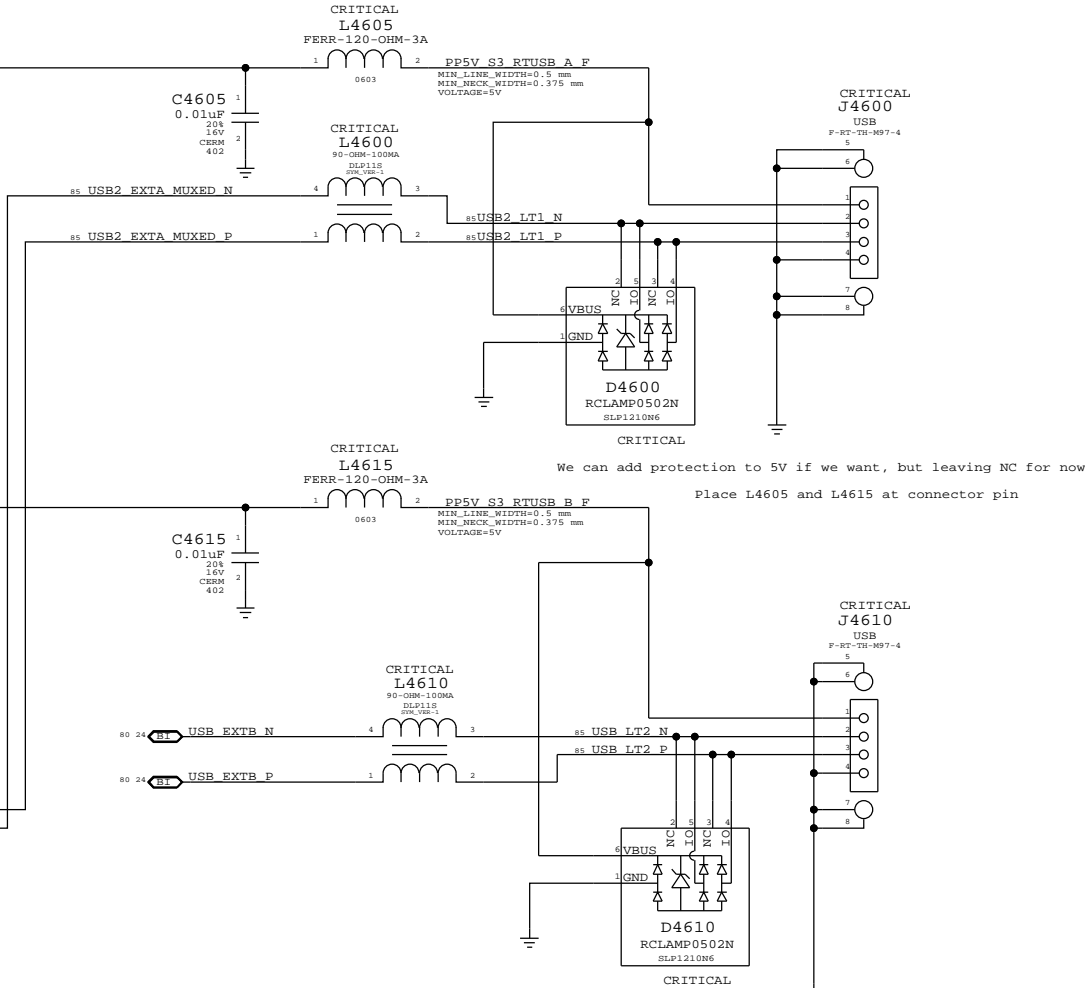


Current limit per port (R4600): 2.18A min / 2.63A max

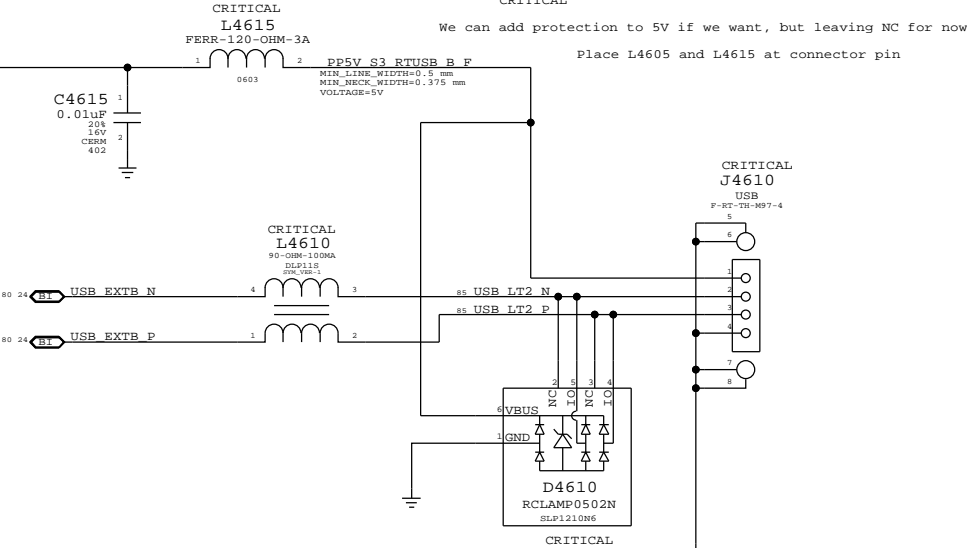
USB/SMC Debug Mux



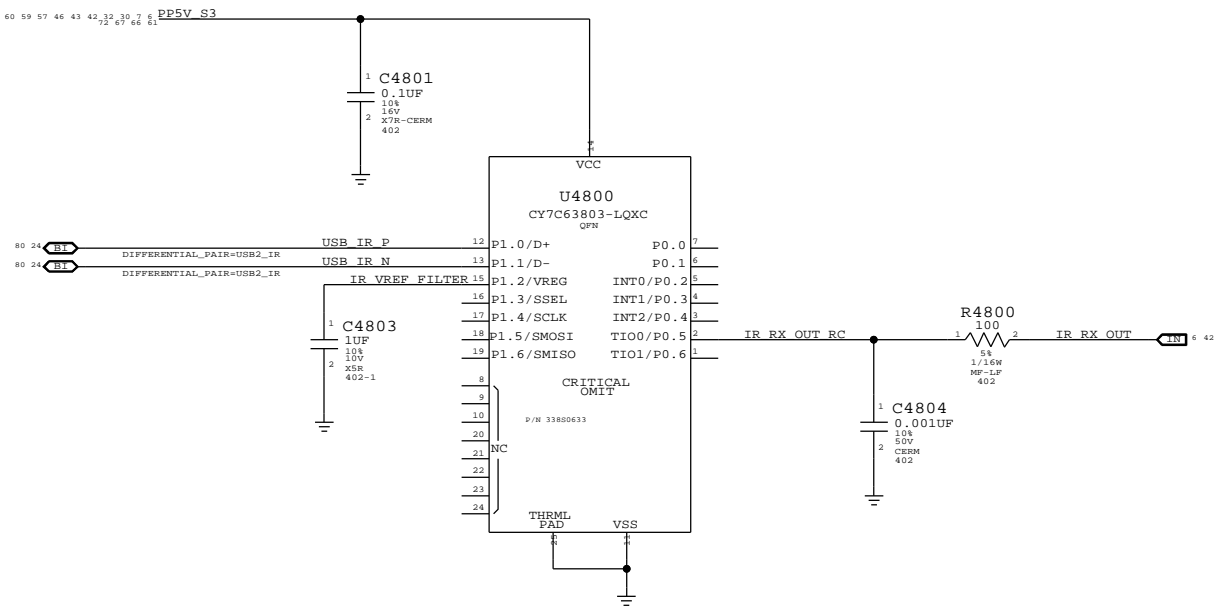
Left USB Port A



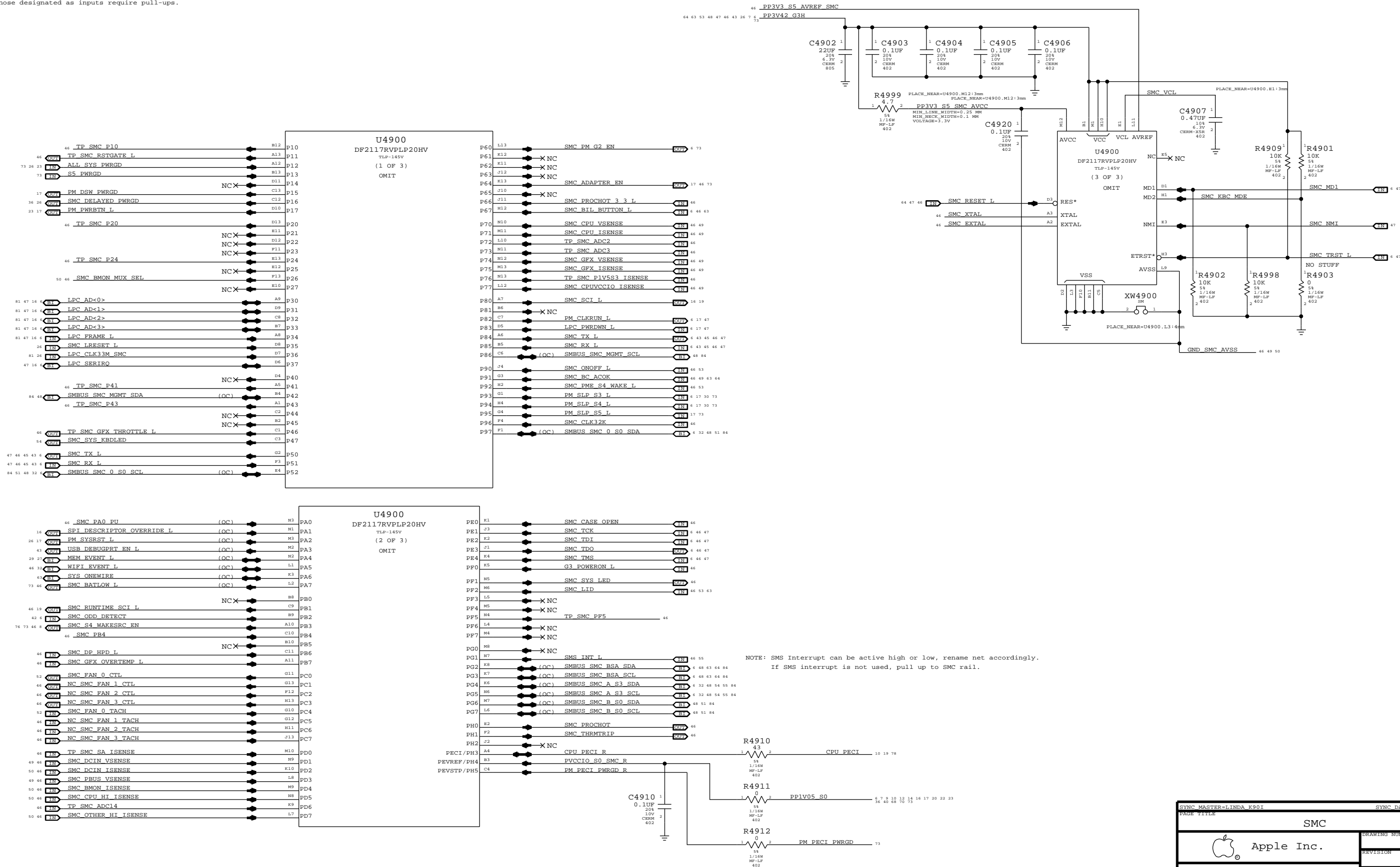
Left USB Port B



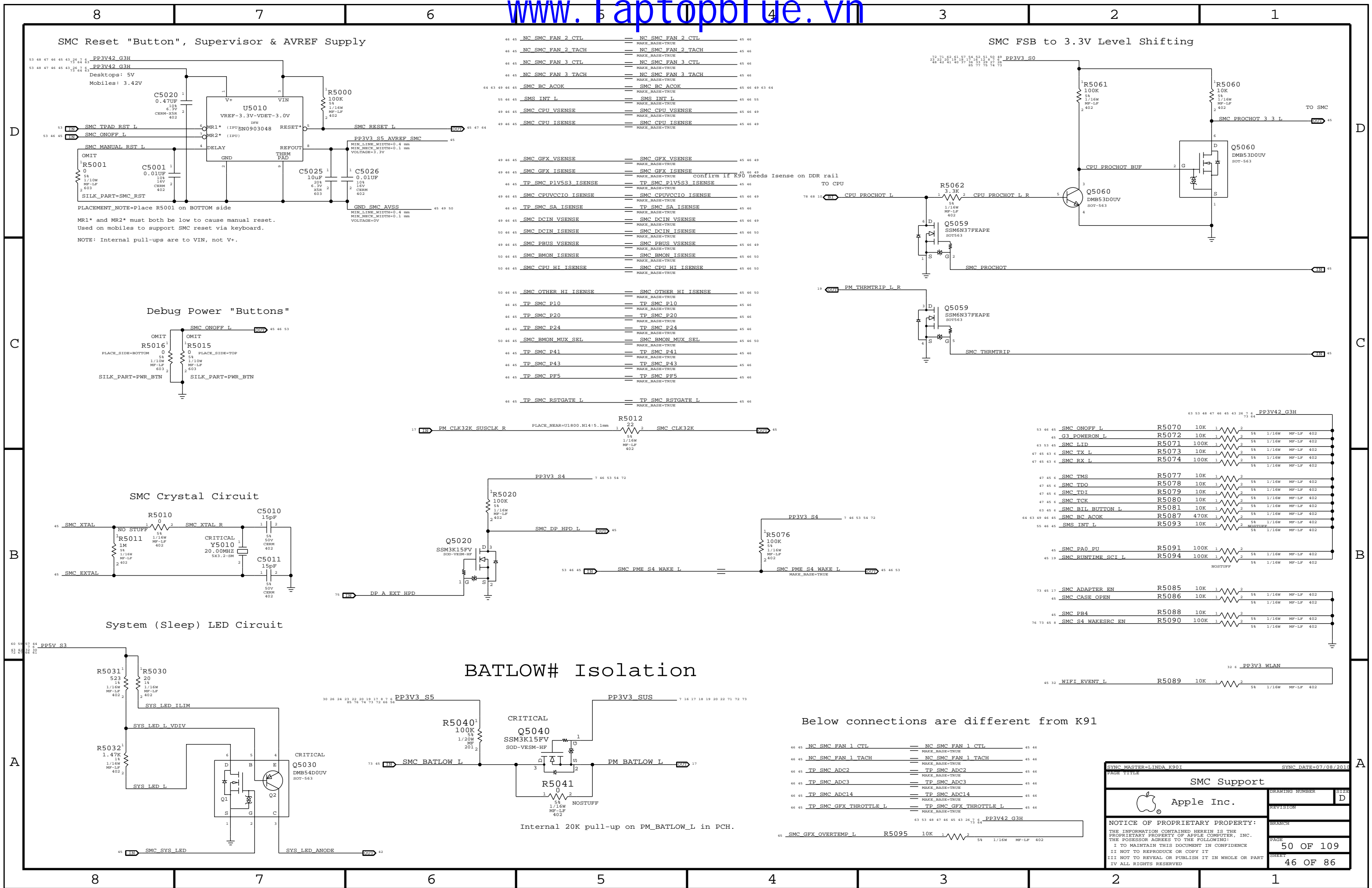
IR SUPPORT



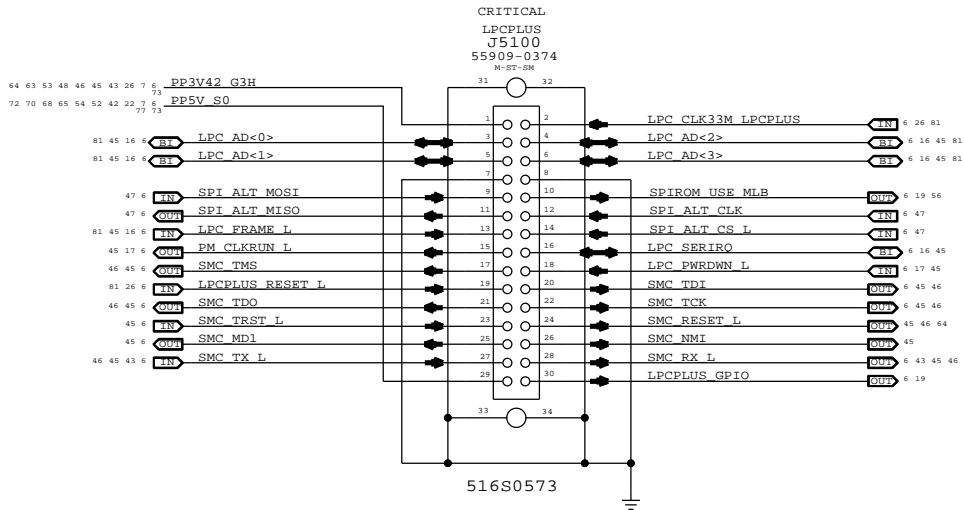
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



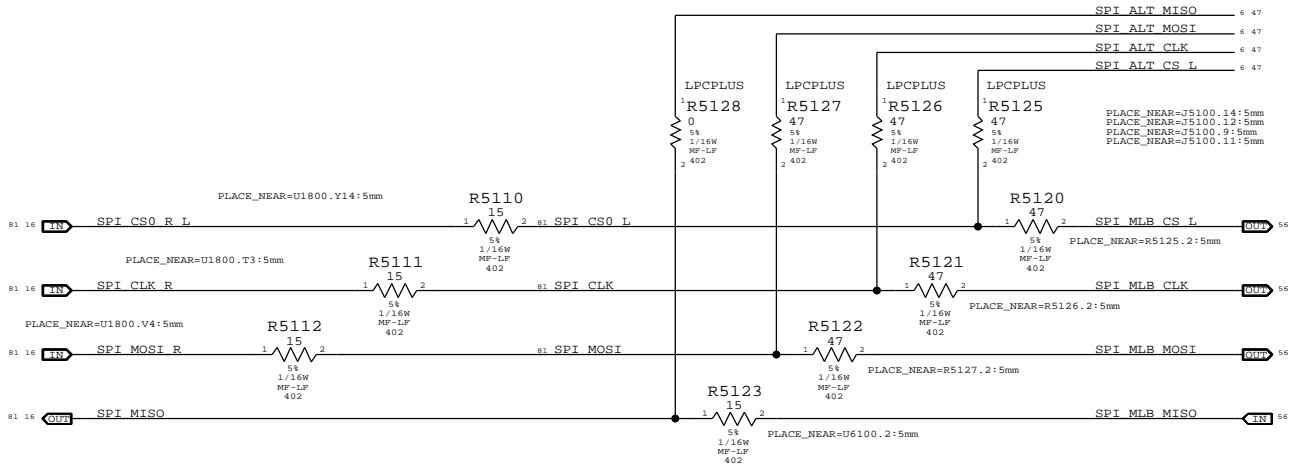
SYNC MASTER=LINDA K901		SYNC DATE=07/07/2010	
PAGE TITLE			
SMC		DRAWING NUMBER	SIZE
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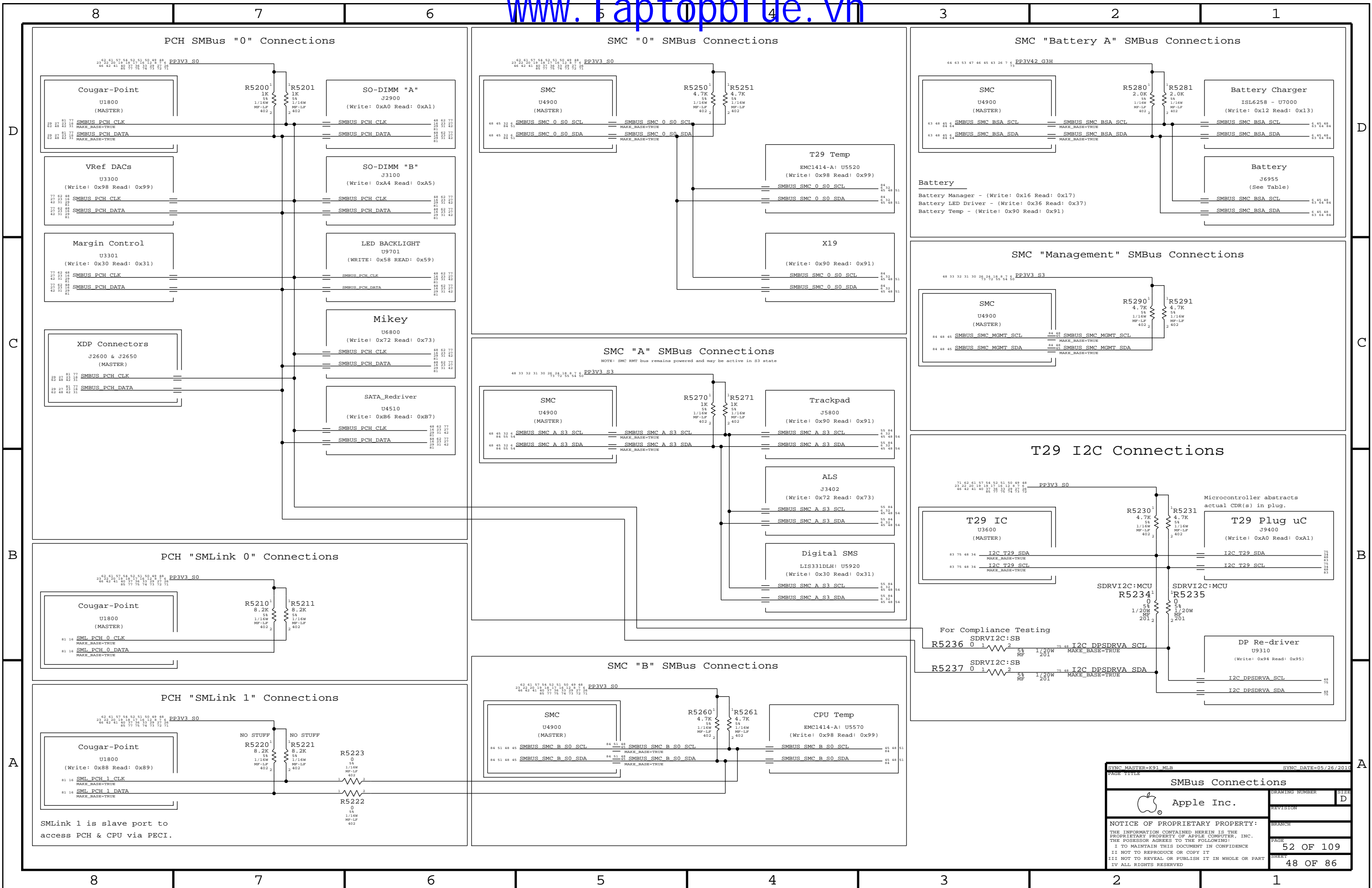


LPC+SPI Connector

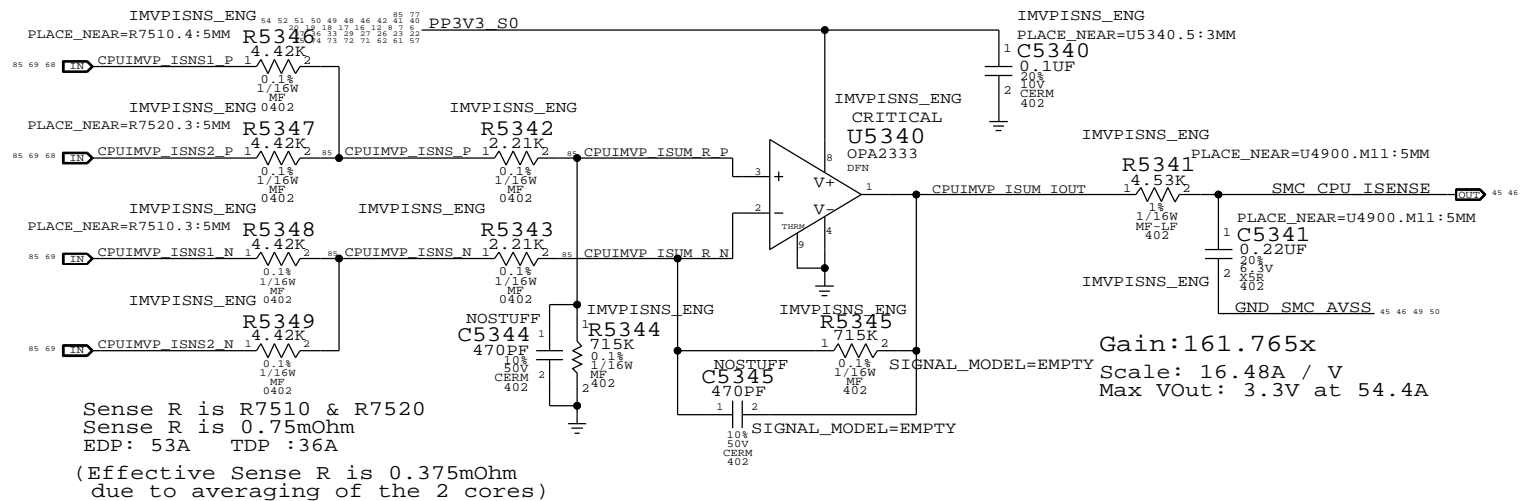
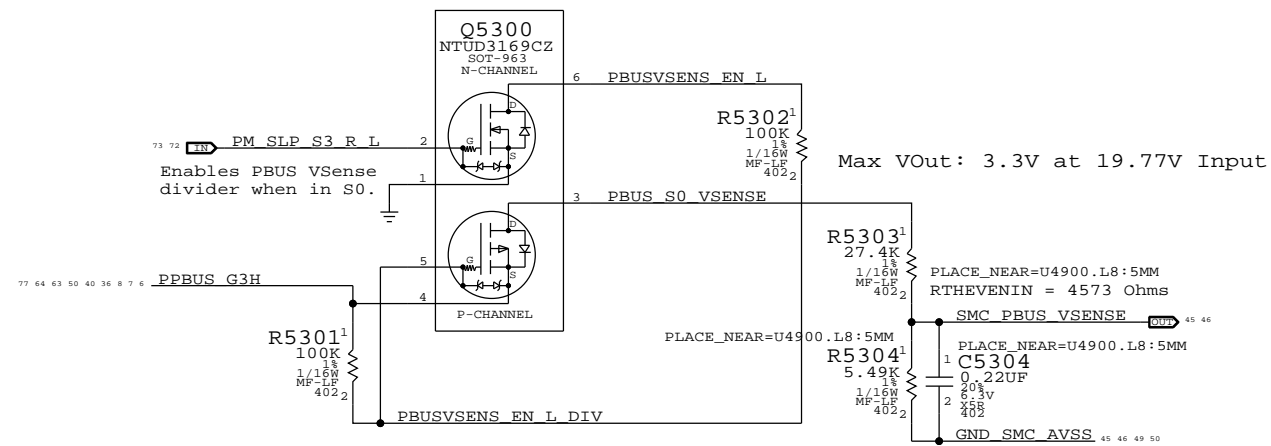


SPI Bus Series Termination

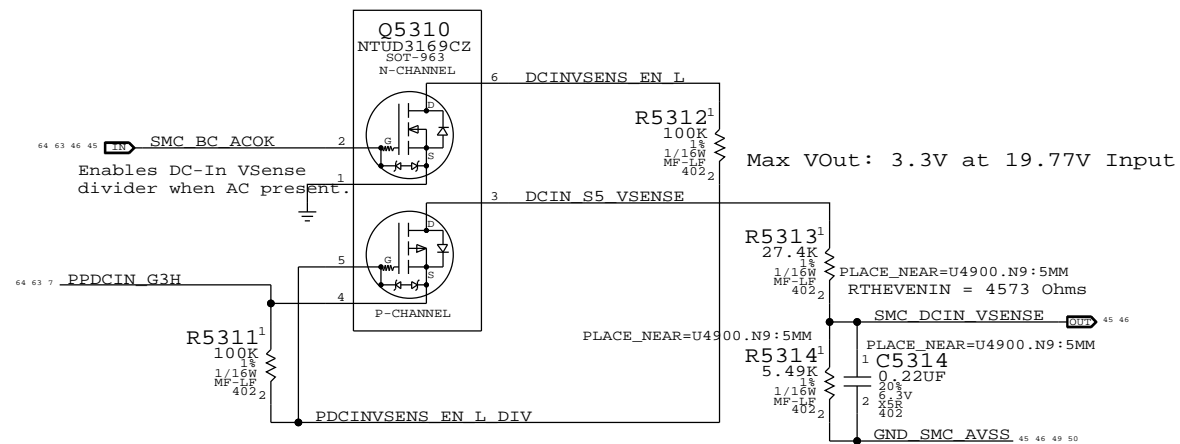




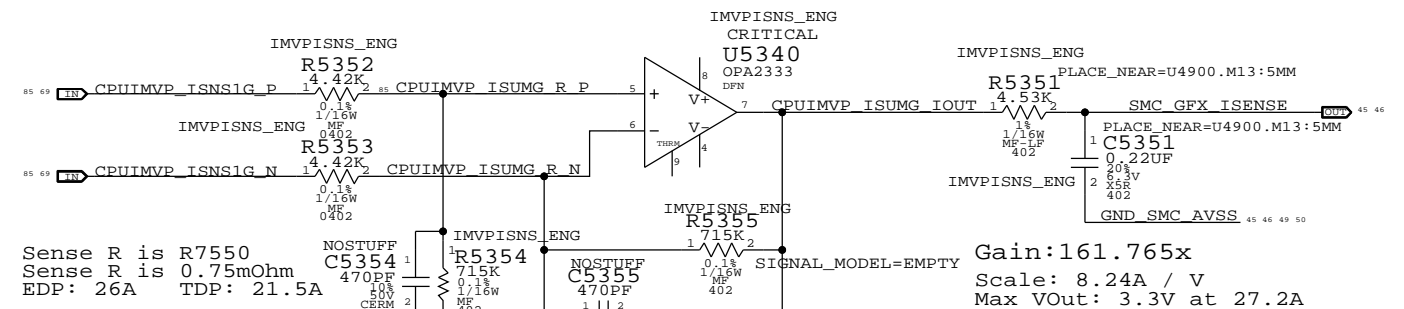
CPU VCore Load Side Current Sense / Filter



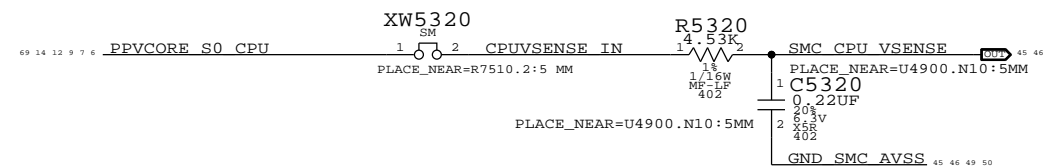
DC-In Voltage Sense Enable & Filter



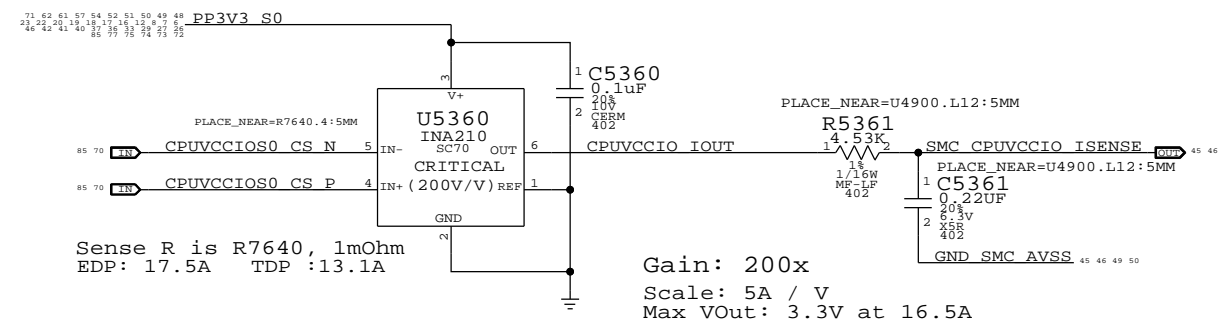
GFX/IG VCore Load Side Current Sense / Filter



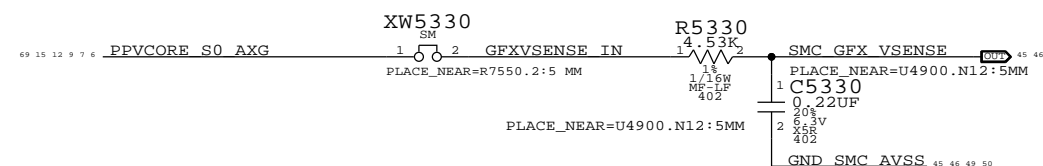
CPU Vcore Voltage Sense / Filter




CPU 1.05V VCCIO Current Sense / Filter

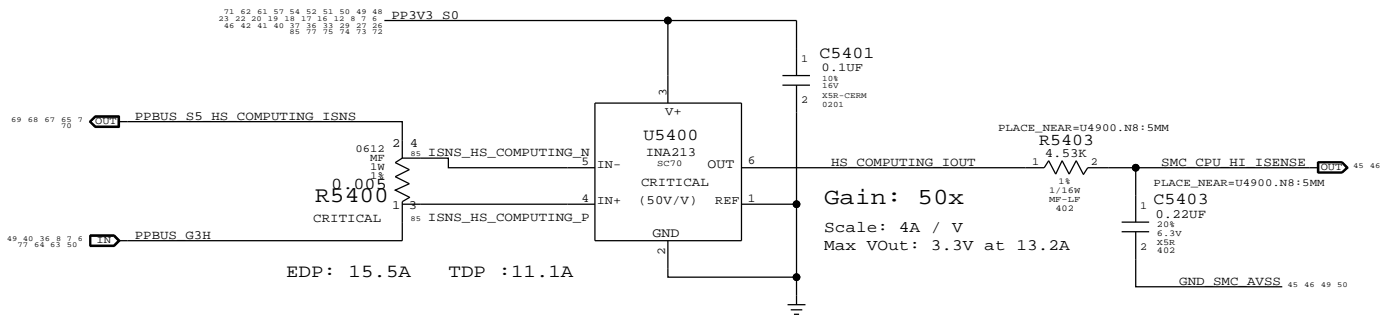


GFX/IG Vcore Voltage Sense / Filter

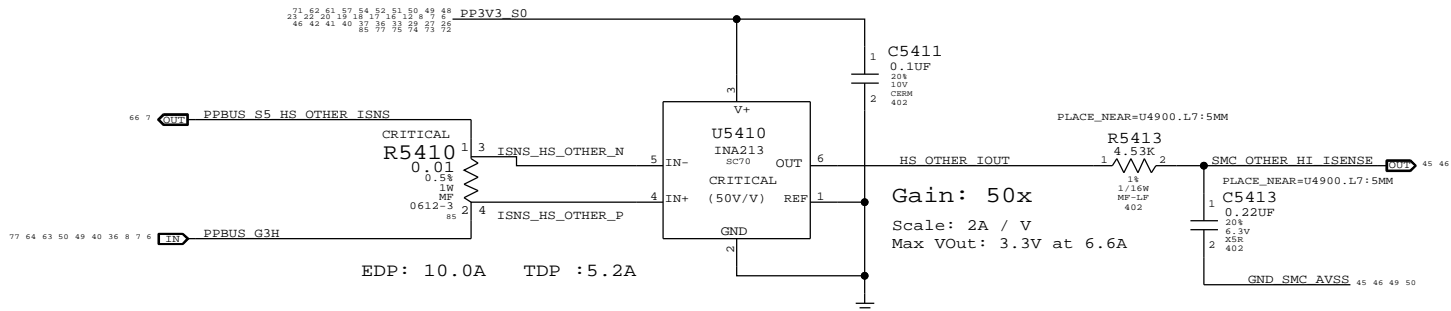


SYNC MASTER=LINDA K901		SYNC DATE=10/22/2010	
PAGE TITLE			
Voltage & Load Side Current Sensing			
		DRAWING NUMBER	
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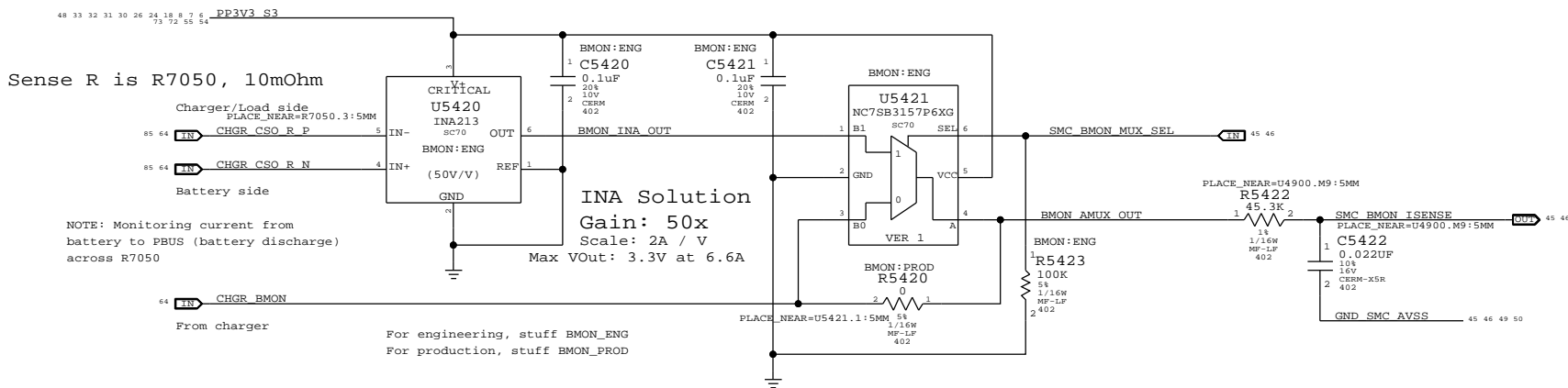
COMPUTING High Side Current Sense / Filter



OTHER High Side Current Sense / Filter



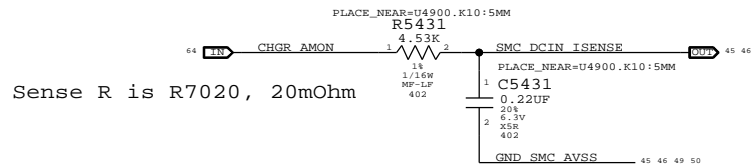
CHARGER BMON High Side (BATTERY DISCHARGE) Current Sense, MUX & Filter




INA (Engineering) Solution
Gain: 50x
Scale: 2A / V
Max VOut: 3.3V at 6.6A

Charger BMON (Production) Solution
ISL6259 Gain: 36x
Scale: 2.78A / V
Max VOut: 3.3V at 9.167A

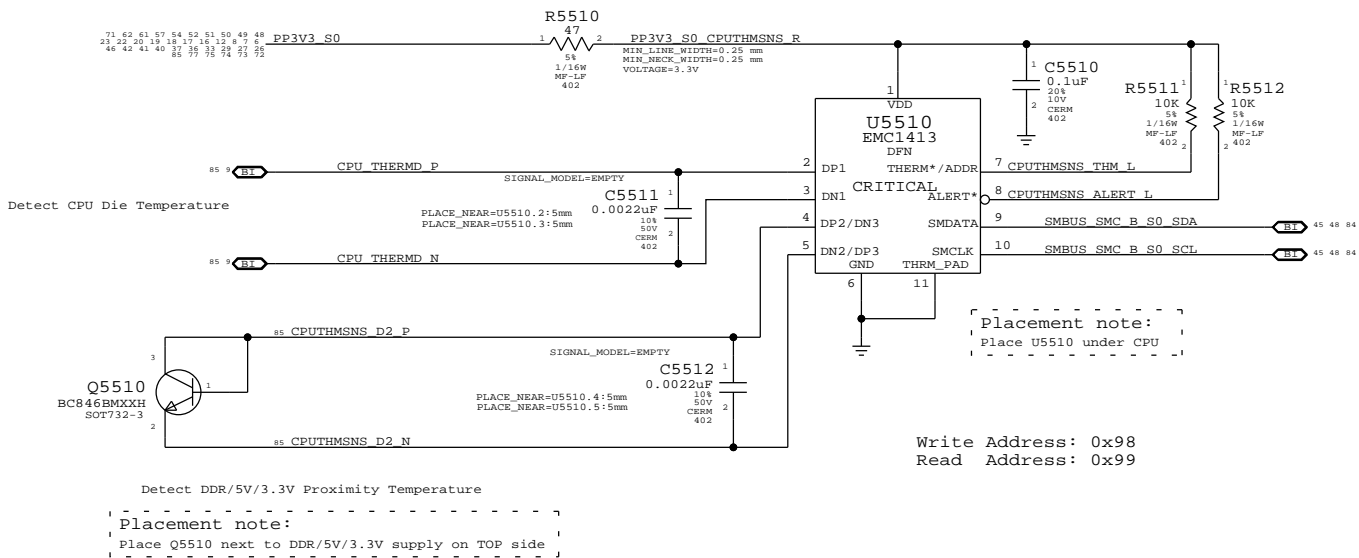
DC-IN (AMON) Current Sense Filter



DC-In AMON
ISL6259 Gain: 20x
Scale: 2.5A / V
Max VOut: 3.3V at 8.25A

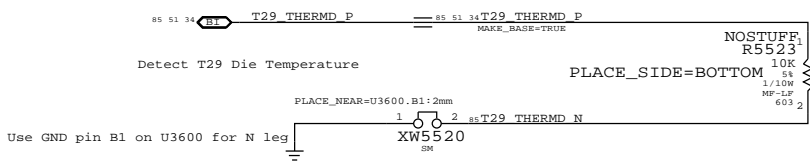
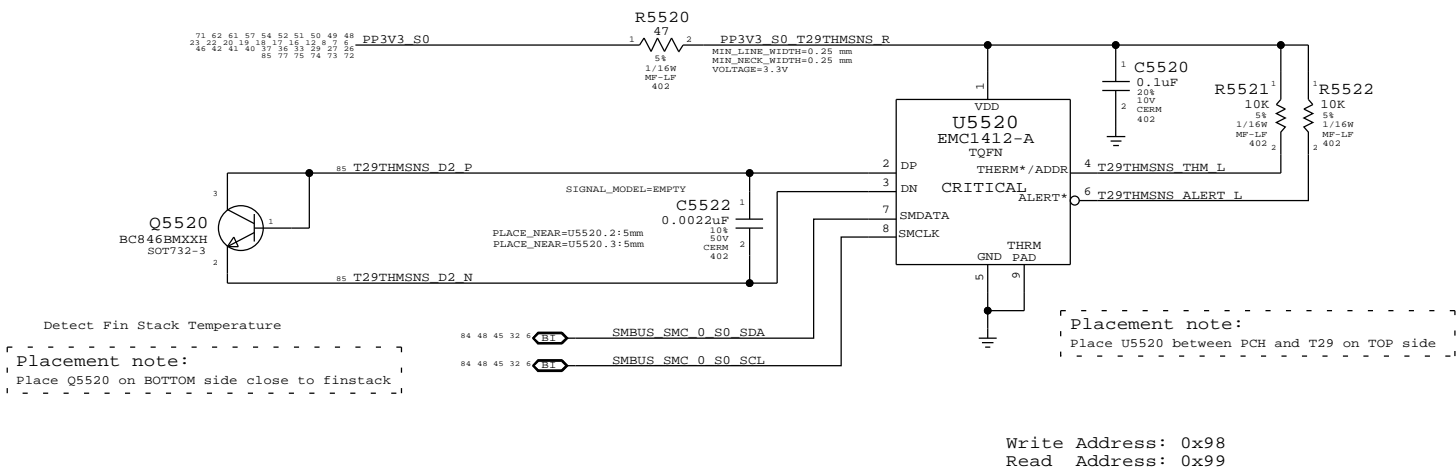
SYNC MASTER=LINDA K901		SYNC DATE=10/22/2010	
PAGE TITLE			
High Side Current Sensing		DRAWING NUMBER	SIZE
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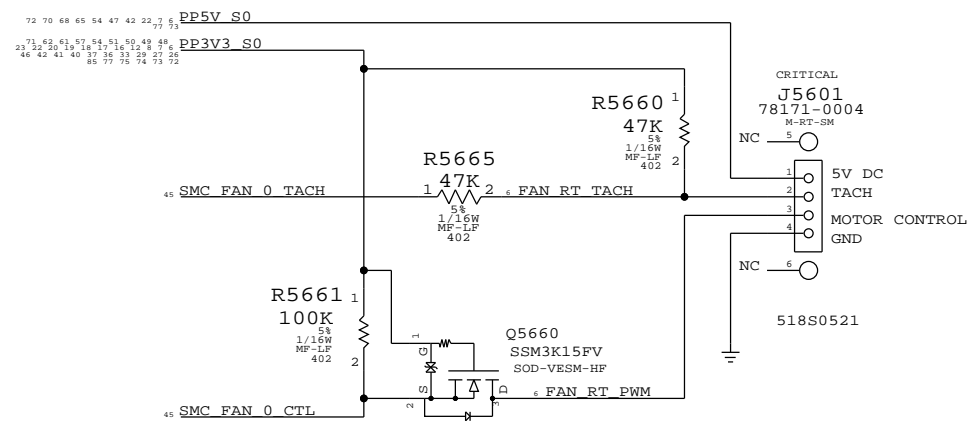
CPU Proximity/CPU Die/5V-3.3V Proximity



T29 Die

PCH-T29 Proximity/FinStack





PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER

IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

Keyboard Connector

SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion.
Keys ANDed with PSOC power to isolate when PSOC is not powered.

TPAD Buttons Disable

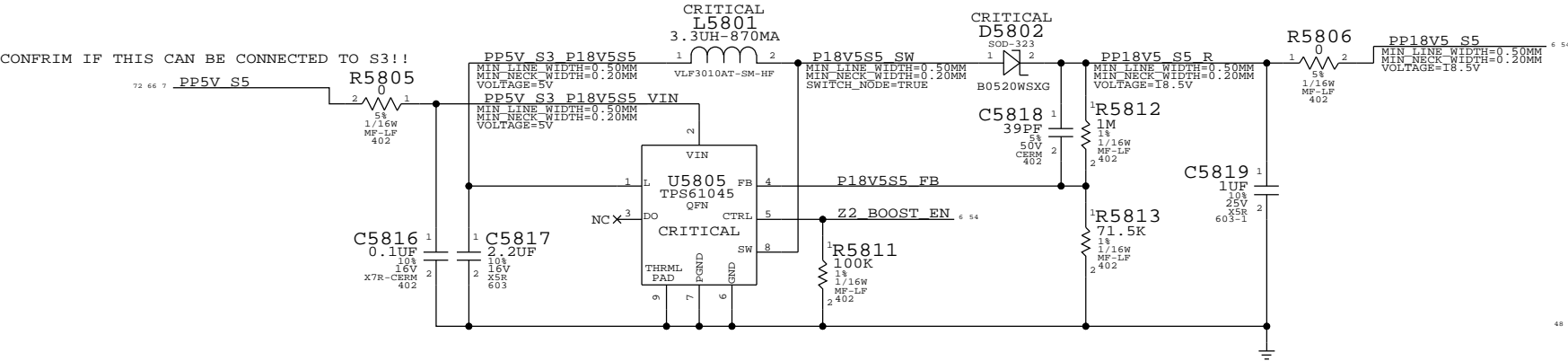
PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

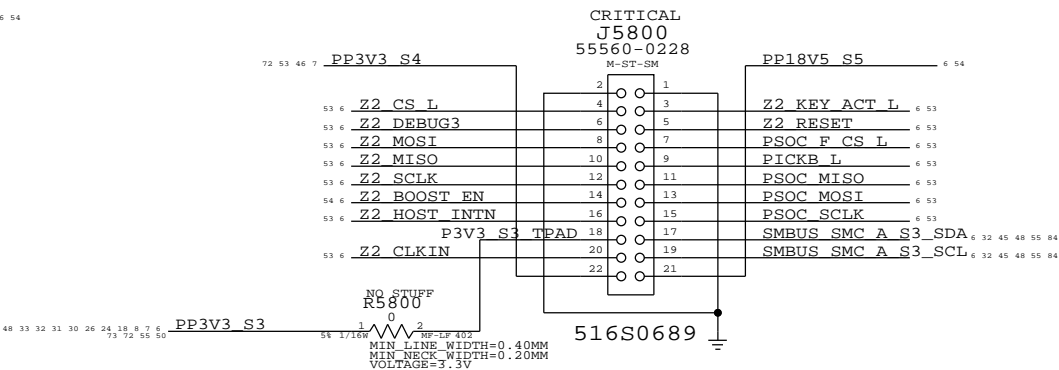
PAGE TITLE		SYNC DATE=07/12/2010	
WELLSPRING 1		DRAWING NUMBER	SIZE D
Apple Inc.		REVISION	
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		PAGE	57 OF 109
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BOOSTER +18.5VDC FOR SENSORS

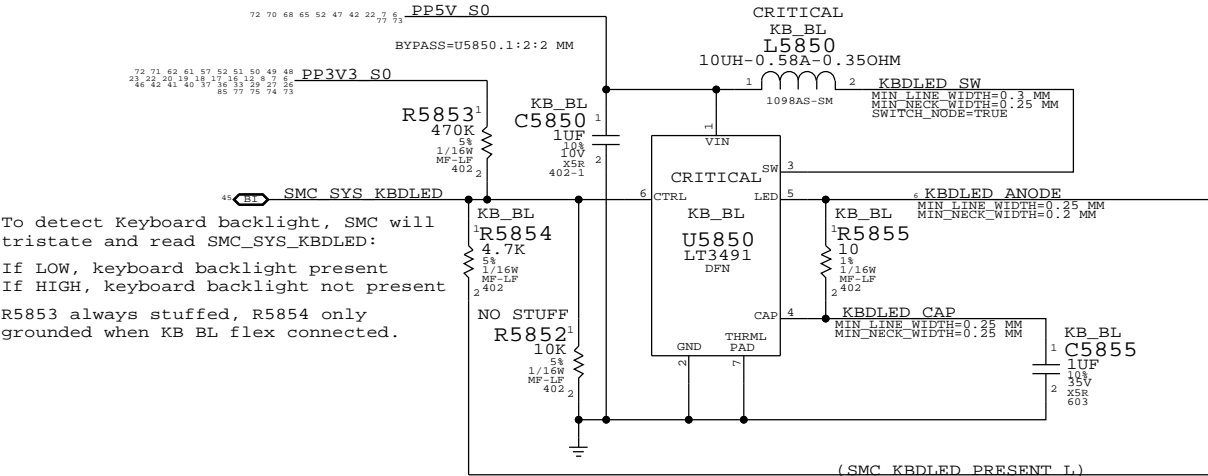
- BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
 - DROOP LINE REGULATION
 - RIPPLE TO MEET ERS
 - 100-300 KHZ CLEAN SPECTRUM
 - STARTUP TIME LESS THAN 2MS
 - R5812,R5813,C5818 MODIFIED



IPD Flex Connector

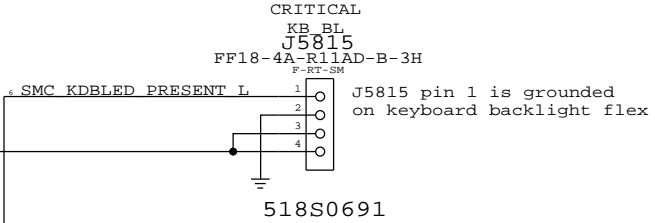


Keyboard Backlight Driver & Detection

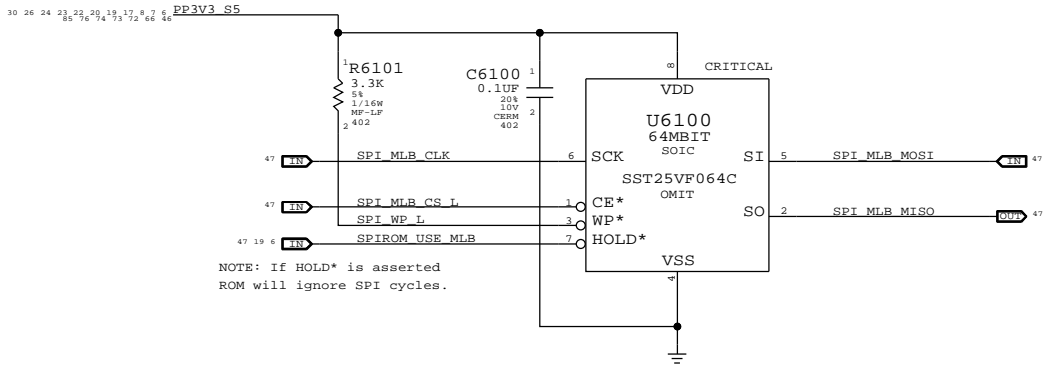


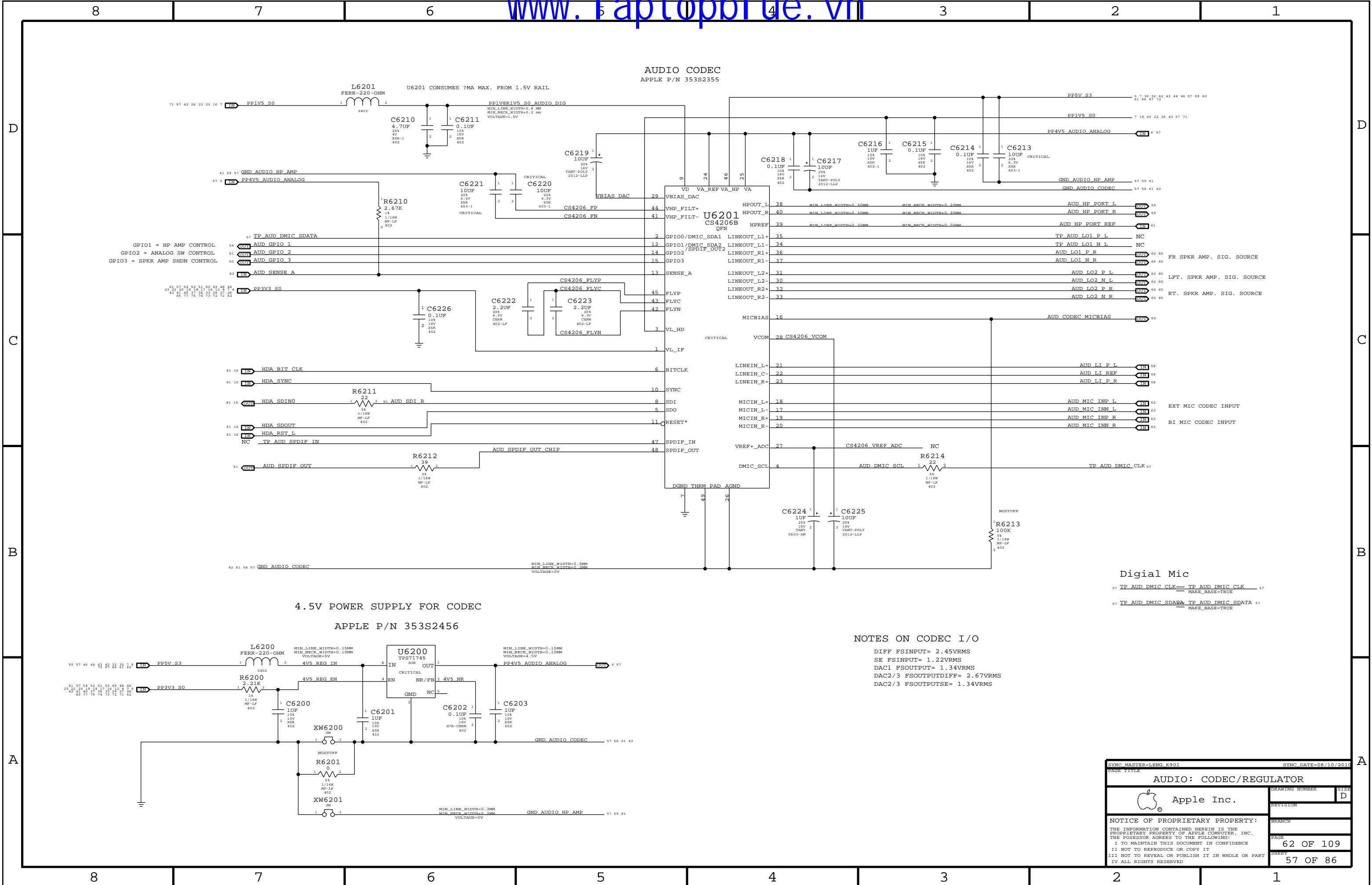
To detect Keyboard backlight, SMC will tristate and read SMC_KBDLED:
If LOW, keyboard backlight present
If HIGH, keyboard backlight not present
R5853 always stuffed, R5854 only grounded when KB BL flex connected.

Keyboard Backlight Connector



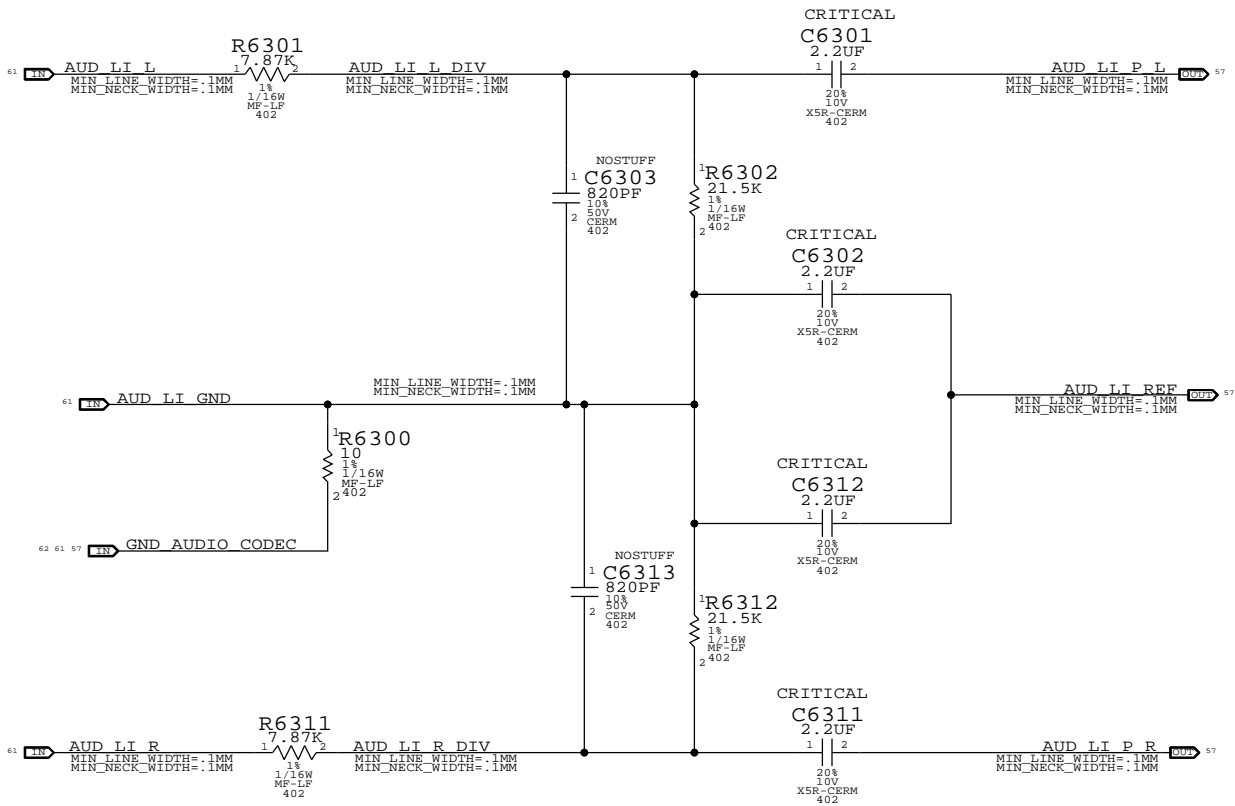
K6 NOTES : C5850 HAS BYPASS PROPERTY, SHOULD BE ADDED INCASE THIS PAGE IS SYNC'ED FROM T27



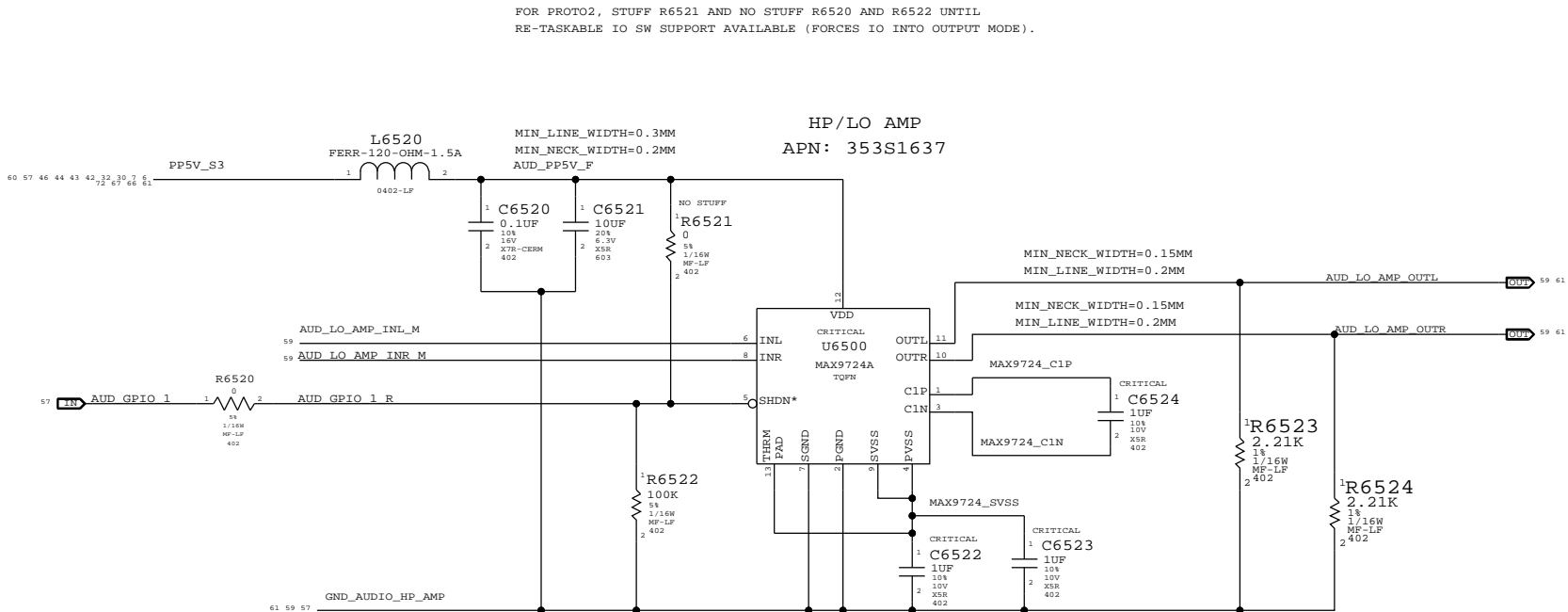
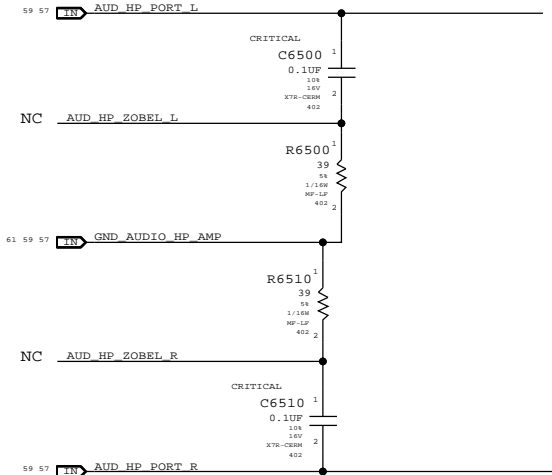


LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS
NET RIN = 10.36K OHMS (INCLUDING PULL-DOWNS AT ANALOG SWITCH COM PINS)
FC_HP = 3.6 HZ
FC_LP = 43KHZ
VIN = 2VRMS, CODEC VIN = 1.14 VRMS

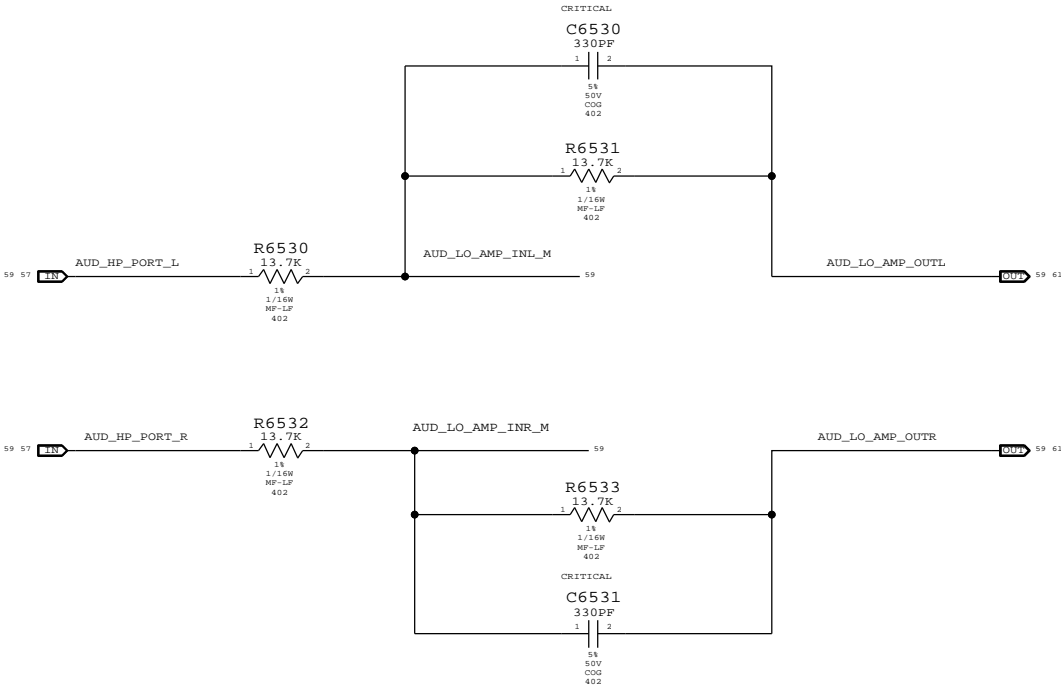



ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER



MAX9724 GAIN/FILTER COMPONENTS

AV_PB = -1V/V, FC_LPF = 35.2KHZ

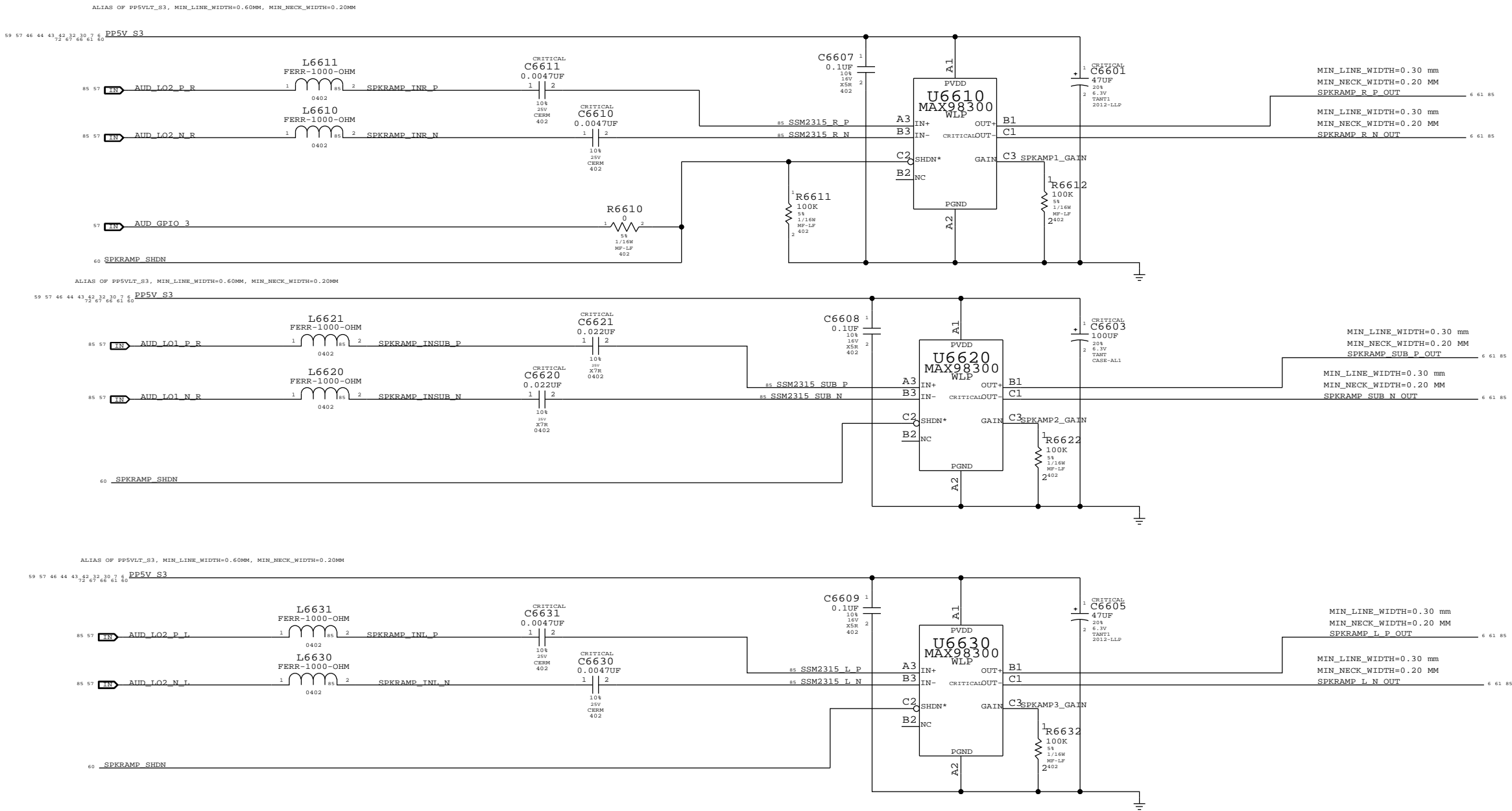


SYNC MASTER=LENG K901		SYNC DATE=08/10/2010	
PAGE TITLE			
AUDIO: HEADPHONE FILTER			
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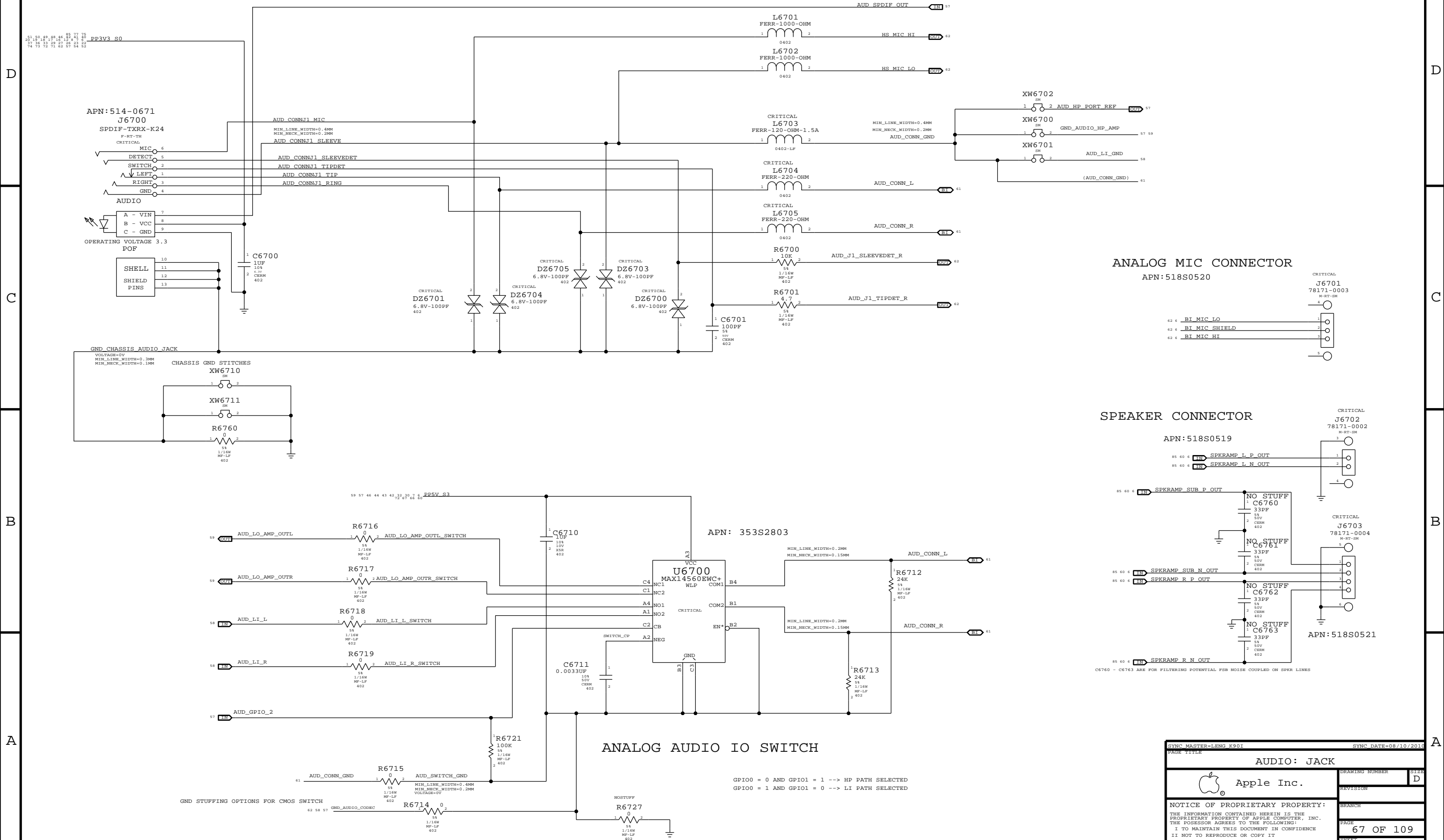
SATELLITE & SUB TWEETER AMPLIFIER

APN:353S2888

SATELLITE 169 HZ < FC < 282 HZ
SUB 80 HZ < FC < 132 HZ
GAIN 3DB



AUDIO JACK: LI/LO/HP CONNECTOR, SPDIF TX



SYNC MASTER=LENG K901		SYNC DATE=08/10/2010	
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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	GPIO_2 AND GPIO_1	0X09 (A)
LINE IN	0X05 (5)	0X05 (5)	0X0C (12)	GPIO_2 AND GPIO_1	0X09 (A)AND UI ELEMENT
SATELLITES	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0D (B)

CODEC INPUT SIGNAL PATHS

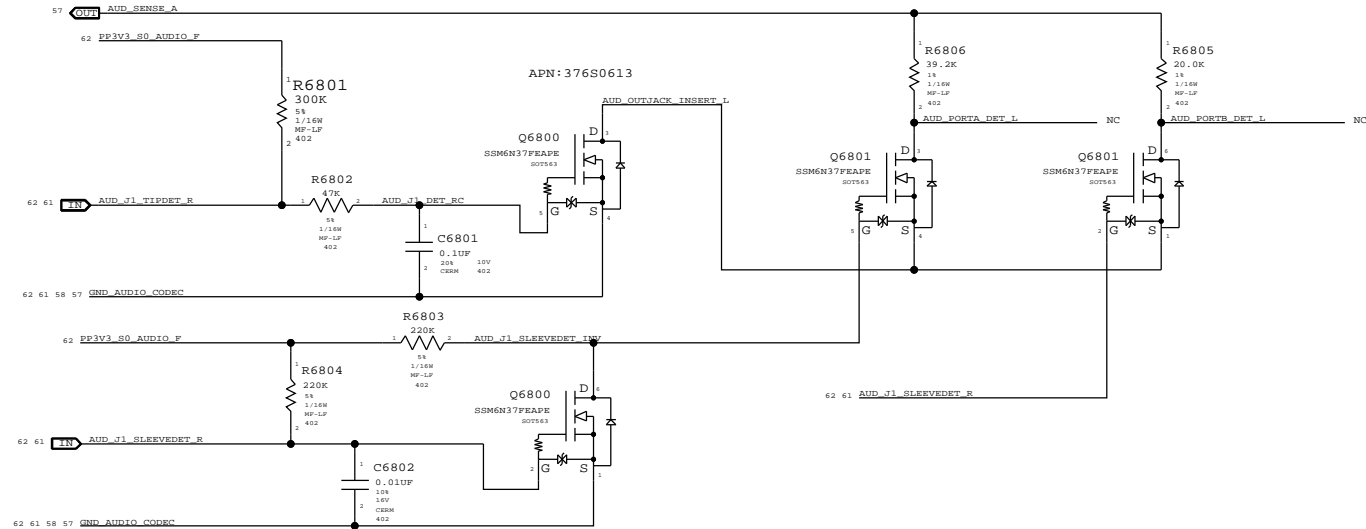
FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
BUILT-IN MIC	0X06 (6)	0X0D (13,B,RIGHT)	MIC_BIAS (80%)	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

SOUTHBRIDGE RESOURCES

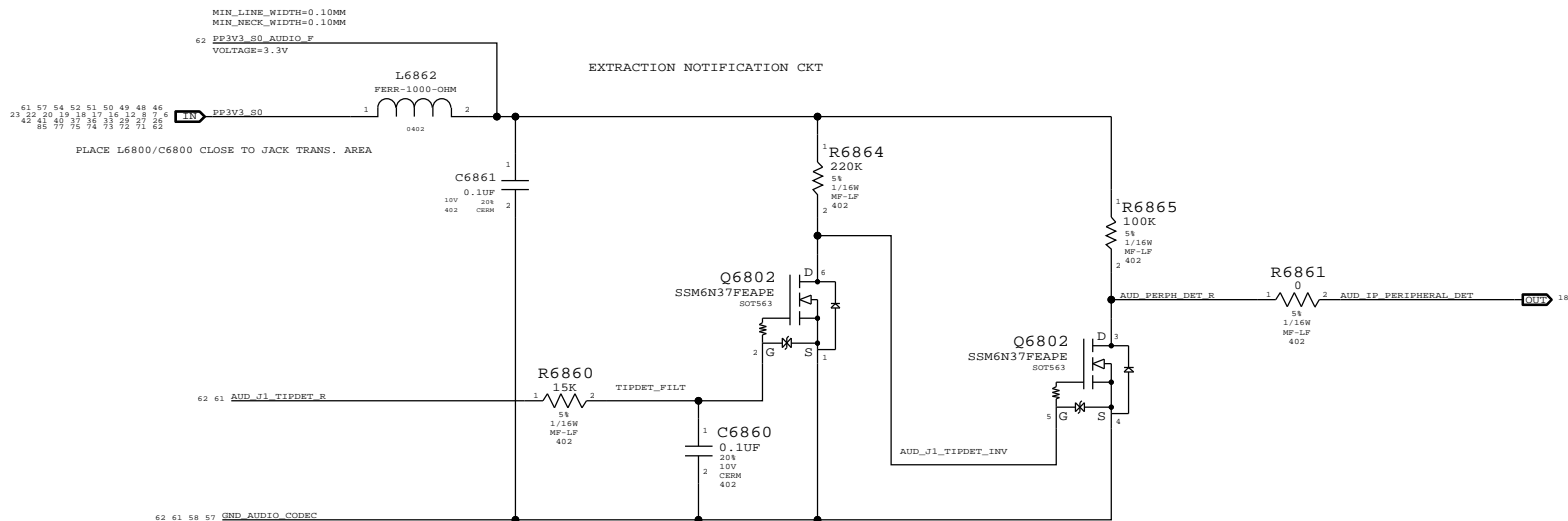
FUNCTION	SYSTEM GPIO	SYSTEM INTERRUPT
AUD_IPHS_SWITCH_EN	COUGAR_POINT GPIO16	N/A
AUD_I2C_INT_L	N/A	COUGAR_POINT GPIO5/PIRQH
AUD_IP_PERIPHERAL_DET	N/A	COUGAR_POINT GPIO3/PIRQH

PORT A DETECT (HEADPHONES)

PORT B DETECT (SPDIF DELEGATE)

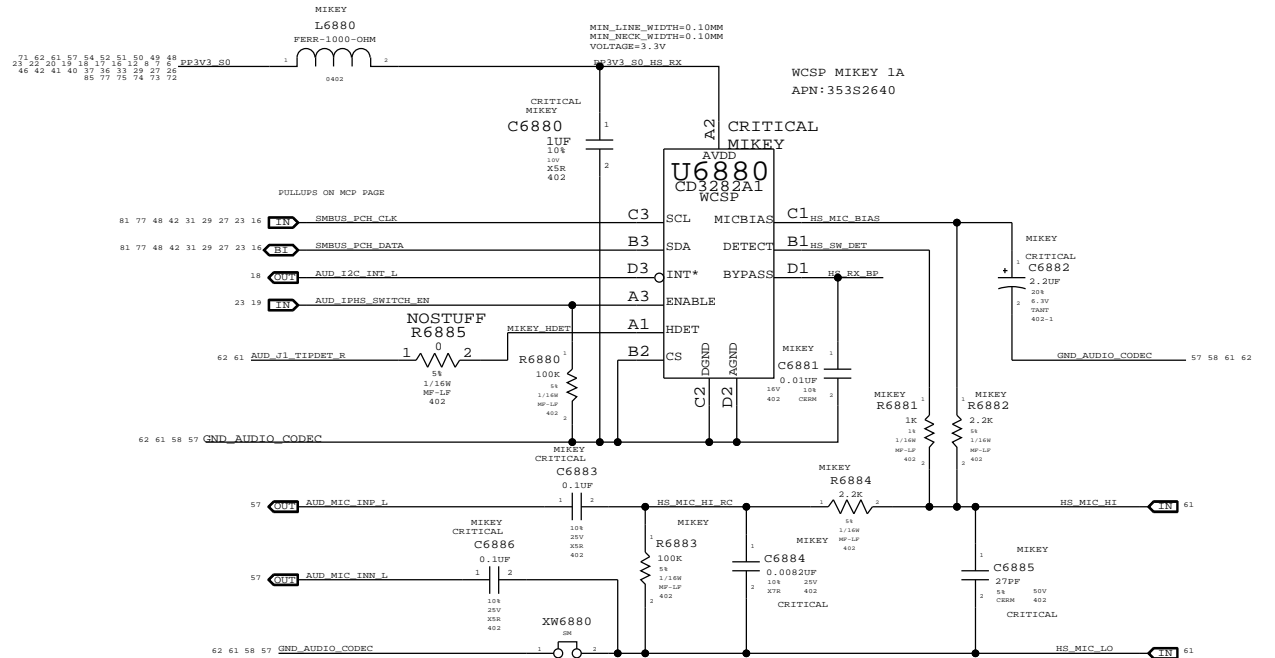


EXTRACTION NOTIFICATION CKT



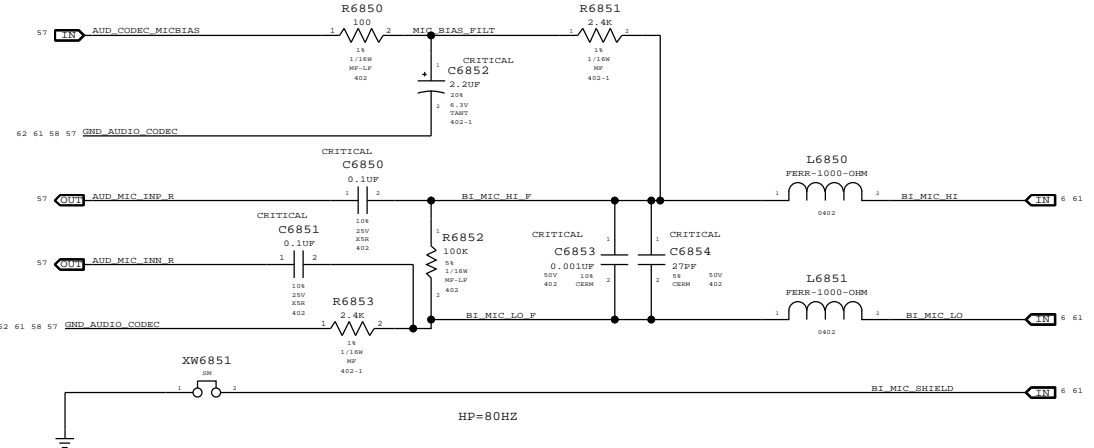
PORT B LEFT (HEADSET MIC)

HP=80HZ, LP=8.82KHZ

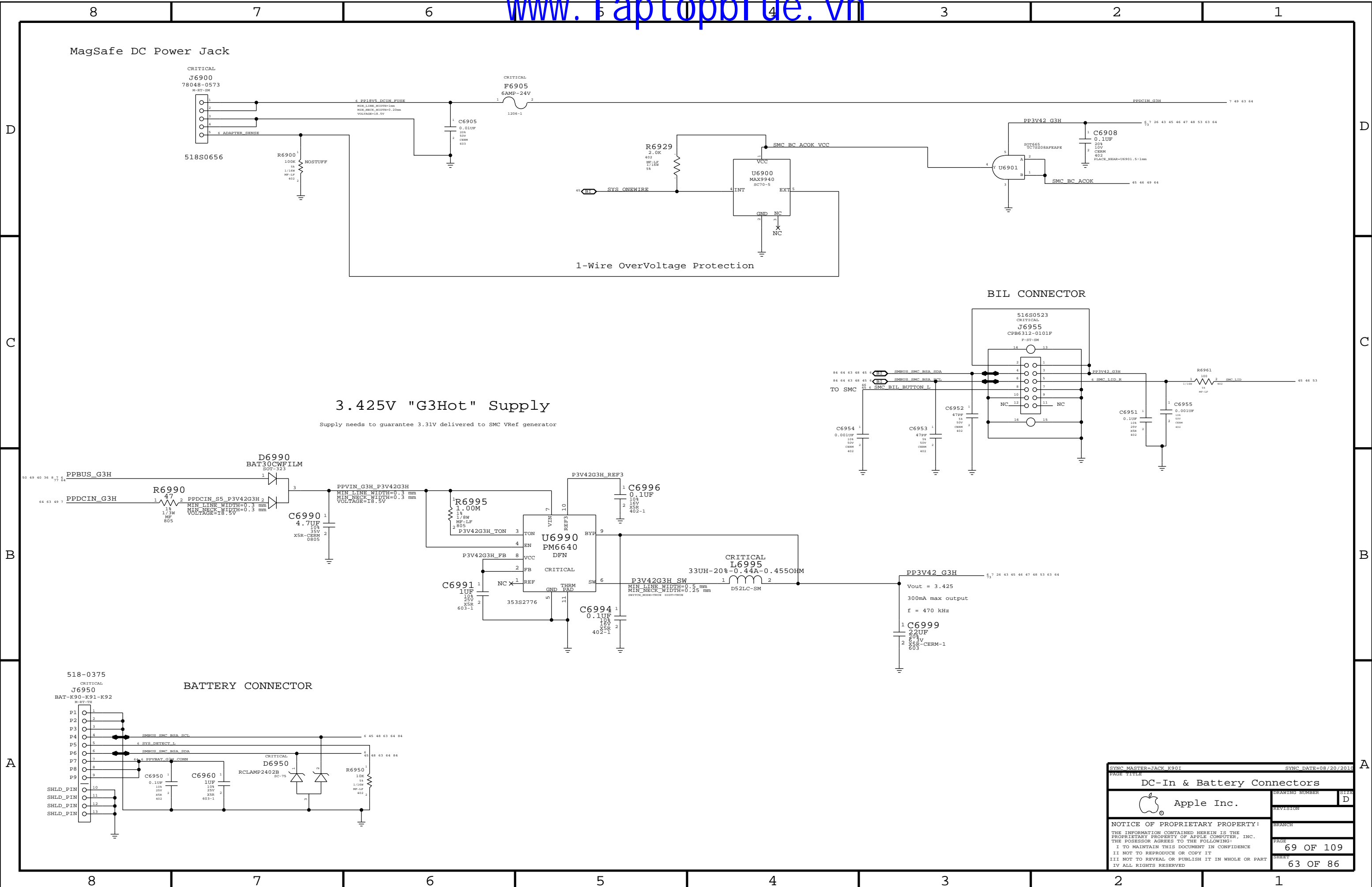


PORT B RIGHT (BUILT-IN MIC)

HP=80HZ



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AUDIO: JACK TRANSLATORS			
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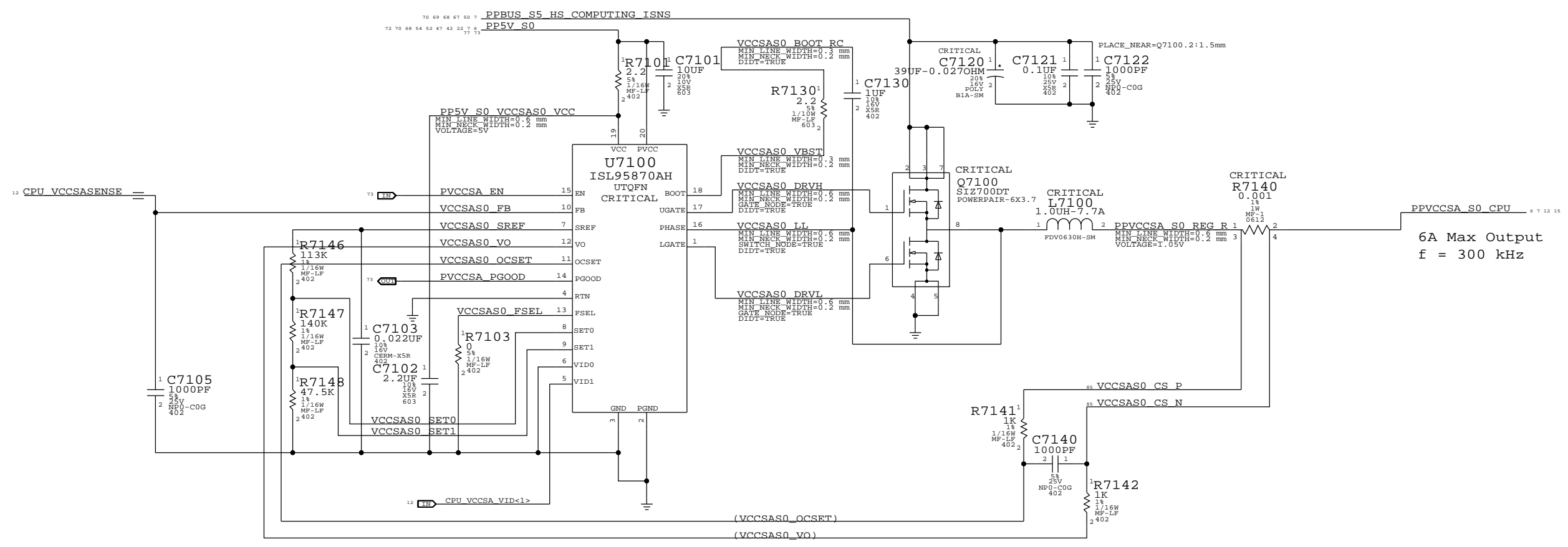
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0966	1	RJK03E1DMS	Q7030	CRITICAL	
376S0966	1	RJK03E1DMS	Q7035	CRITICAL	

TO SYSTEM

TO/FROM BATTERY

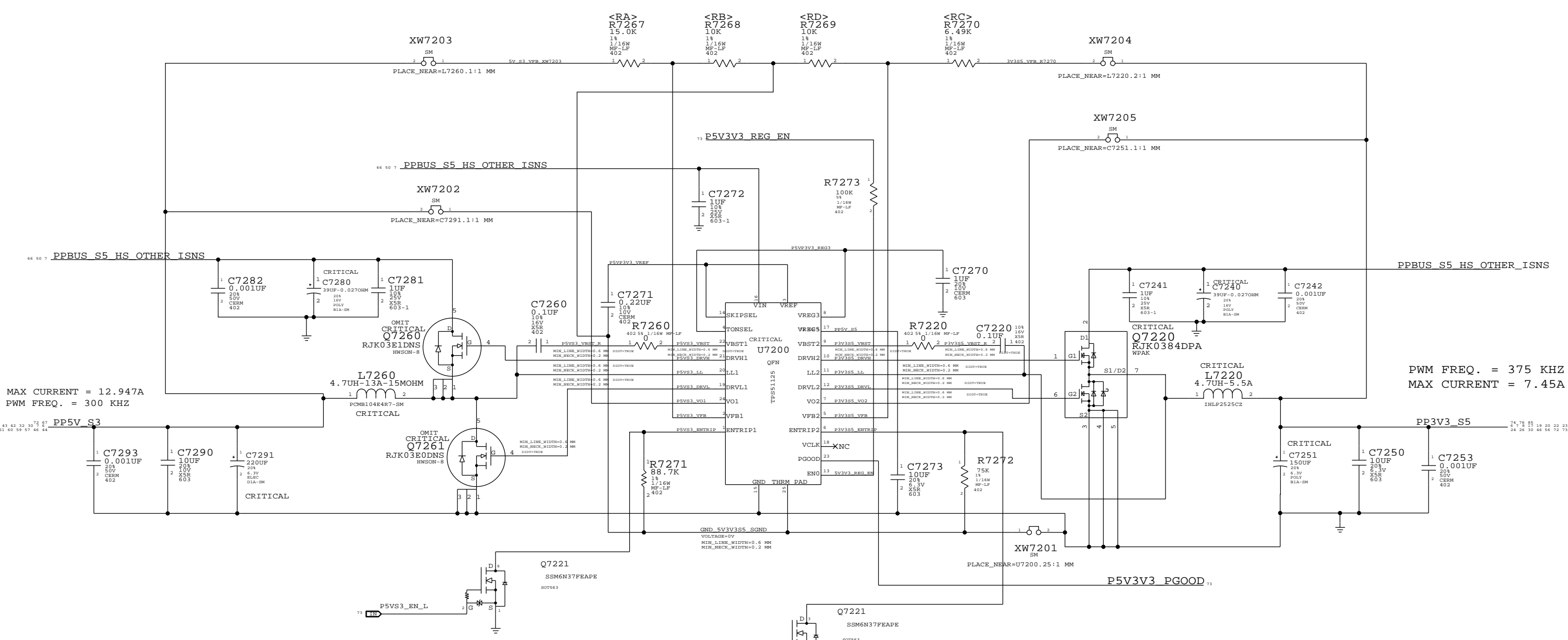
SYNCH MASTER=JACK K901		SYNCH DATE=10/11/2010	
PAGE TITLE			
PBus Supply & Battery Charger			
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System Agent Power Supply



5V_S3 / 3.3V_S5 POWER SUPPLY

$$V_{OUT} = (2 * R_A / R_B) + 2$$
$$V_{OUT} = (2 * R_C / R_D) + 2$$



MAX CURRENT = 12.947A
PWM FREQ. = 300 KHZ

PWM FREQ. = 375 KHZ
MAX CURRENT = 7.45A


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0966	1	RJK03E1DNS	Q7260	CRITICAL	
376S0895	1	RJK03E0DNS	Q7261	CRITICAL	

SEPERATED MASTER PGOOD FOR BOTH 5V AND 3V3.

SYNC MASTER=JACK K901

SYNC DATE=10/04/2010

5V/3.3V SUPPLY

 Apple Inc.

DRAWING NUMBER
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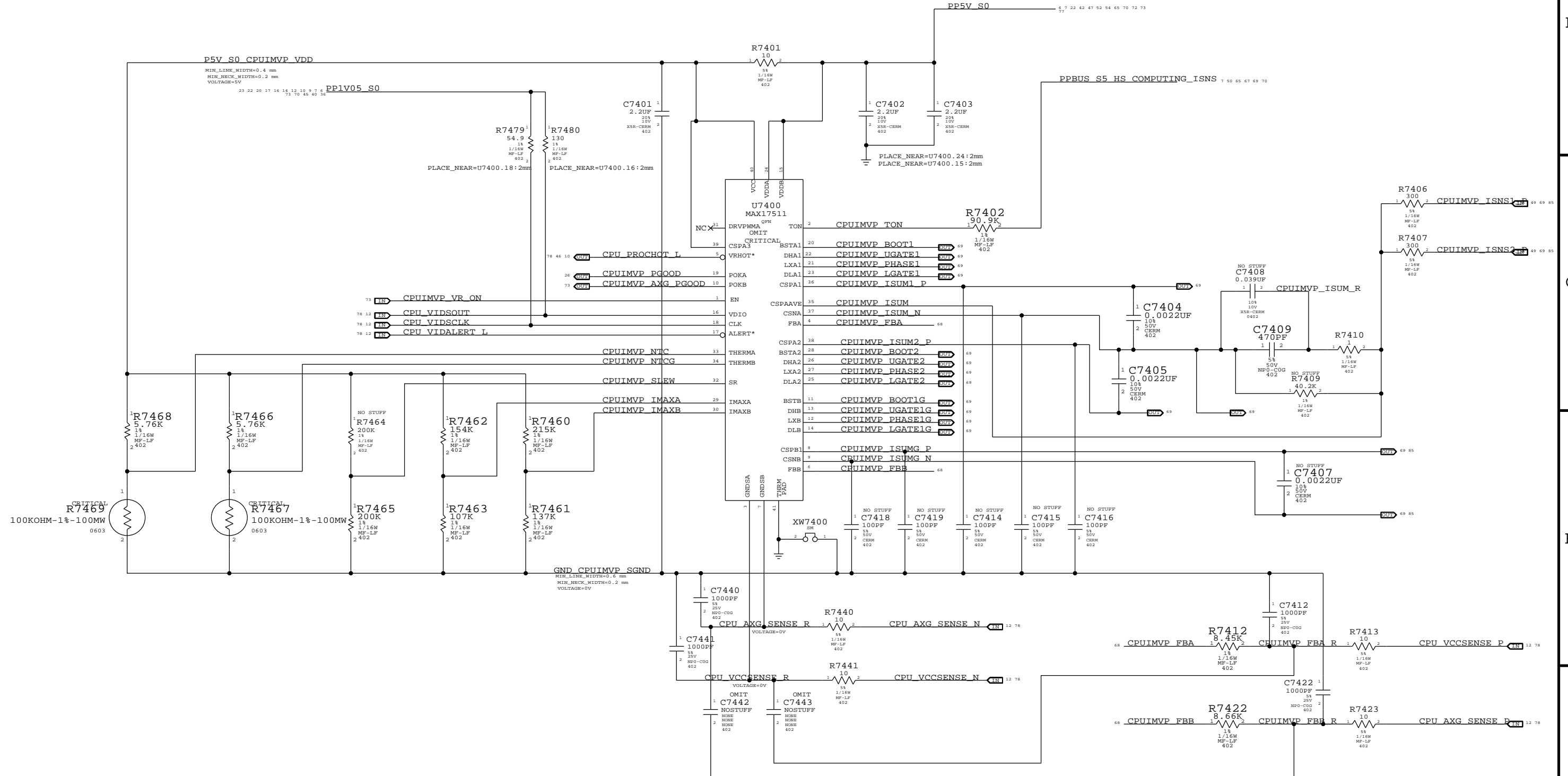




PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0790	1	CSD58859Q1	Q7330	CRITICAL	
376S0928	1	FD8C25143DC	Q7335	CRITICAL	

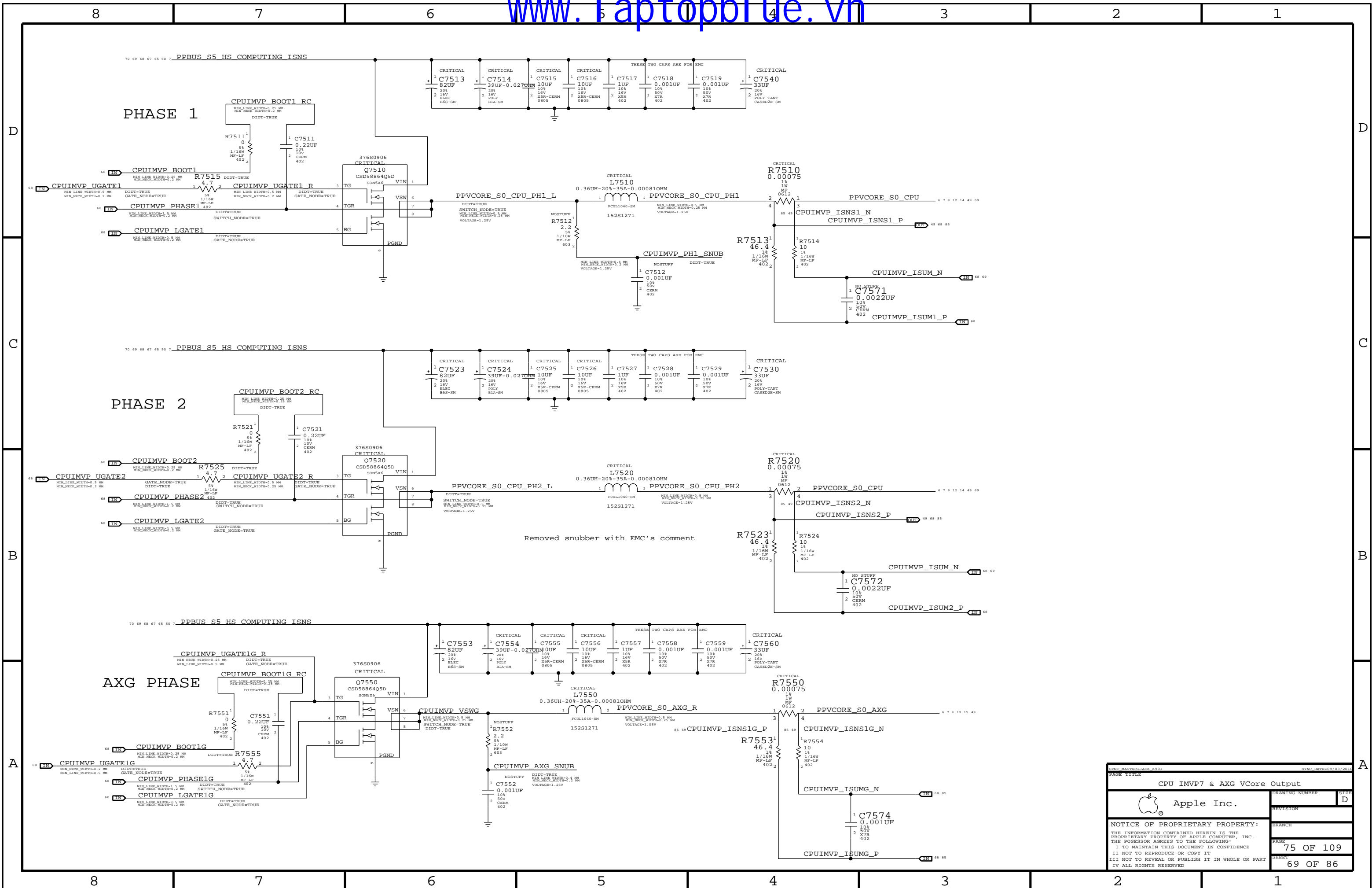
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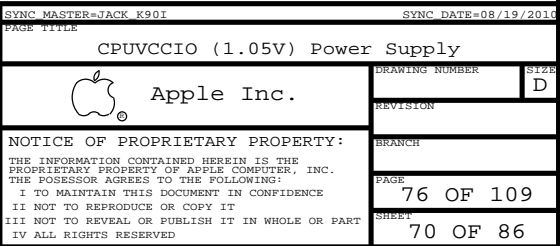
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S3259	1	IC, MAX15092, 3+1PH CPU REG, IMVP7, 5X5QFN40	U7400	CRITICAL	

Need symbol to be re-drawn to clean up this page

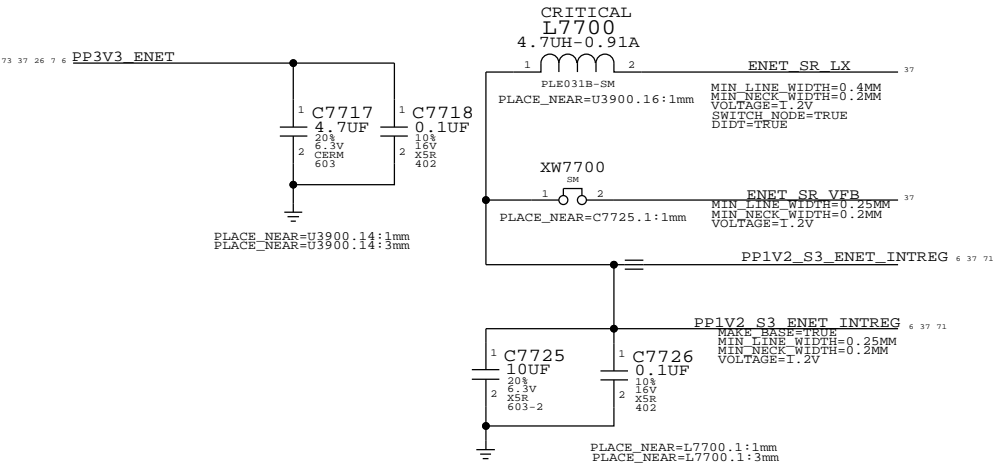


BOND MASTER-JACK #301		SYMC DATE-10/14/2010	
PRICE TITLE			
CPU IMPV7 & AXG VCore Regulator			
		DRAWING NUMBER	
		SIZE D	
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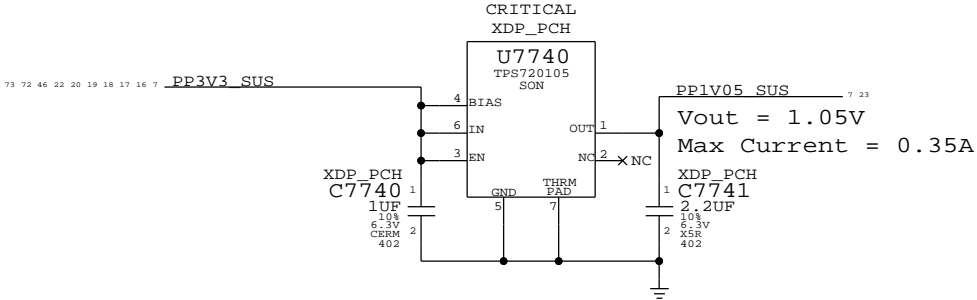
∇ 

CAESAR IV 1.2V INT.VR CMPTS



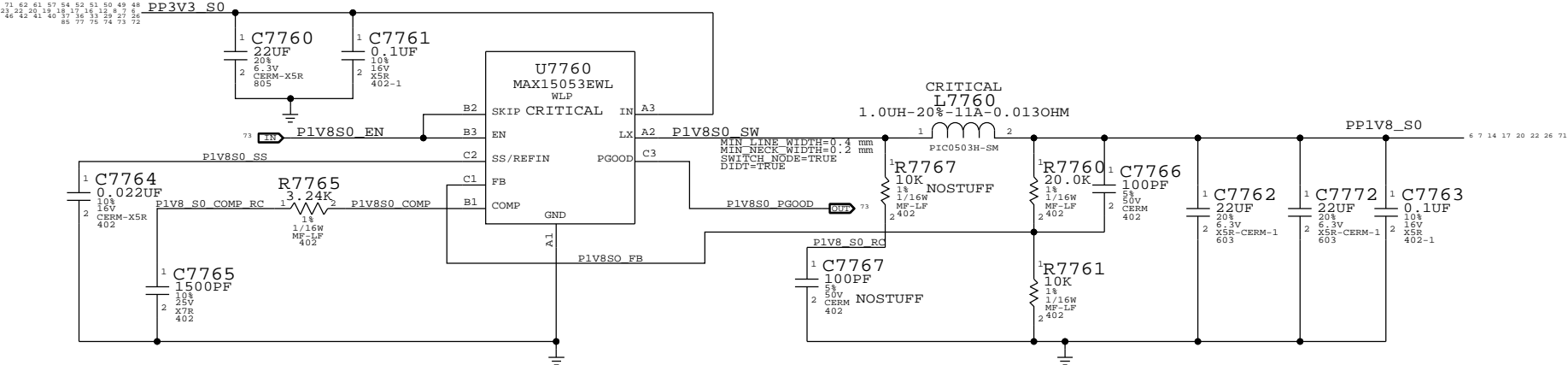
1.05V S5 LDO

Cougar Point requires JTAG pull-ups to be powered at 1.05V in S5. Pull-ups (3) must be 51 ohms to support XDP (not required in production). 70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



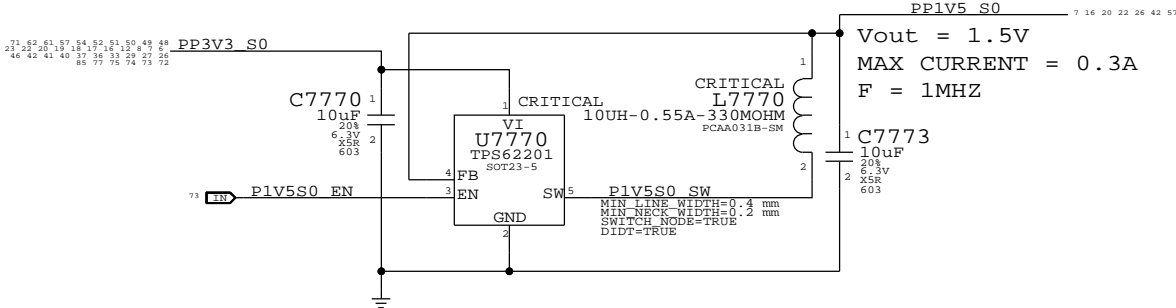
1.8V S0 Switcher

Vout = 1.8V
MAX CURRENT = 2A
F = 1MHZ



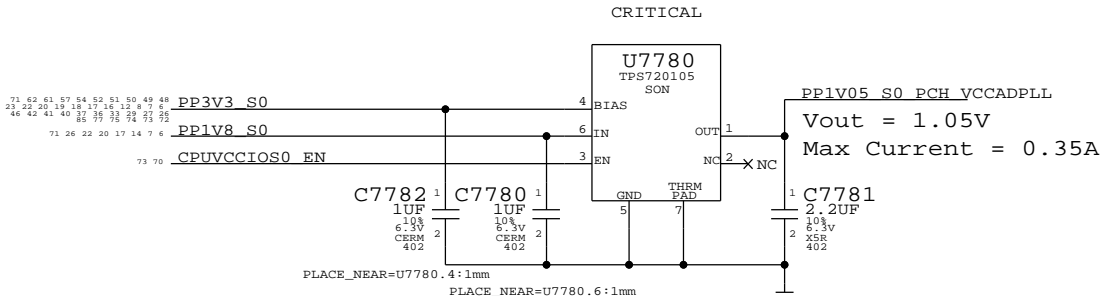
1.5V S0 Switcher

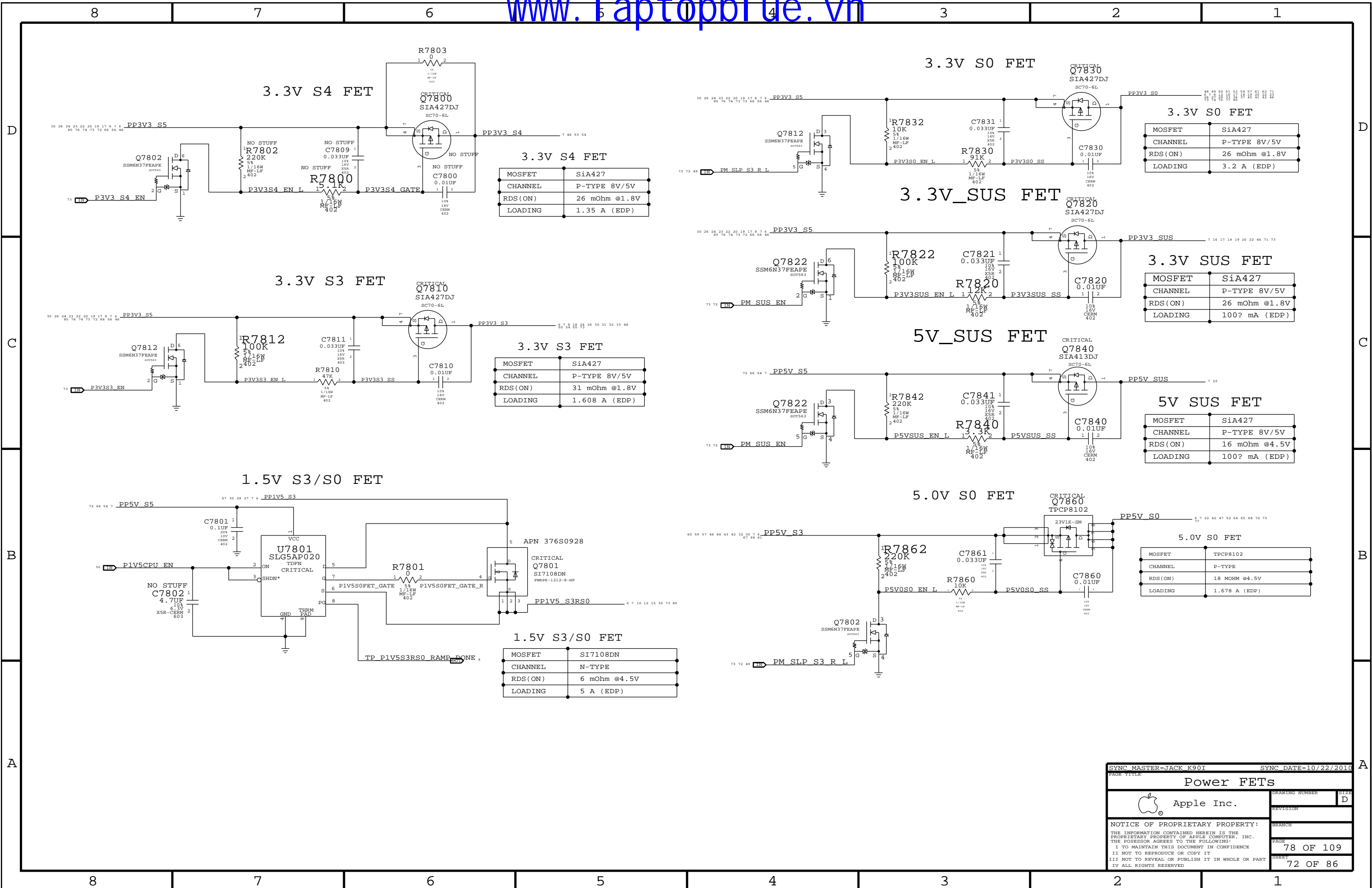
Vout = 1.5V
MAX CURRENT = 0.3A
F = 1MHZ



1.05V S0 LDO

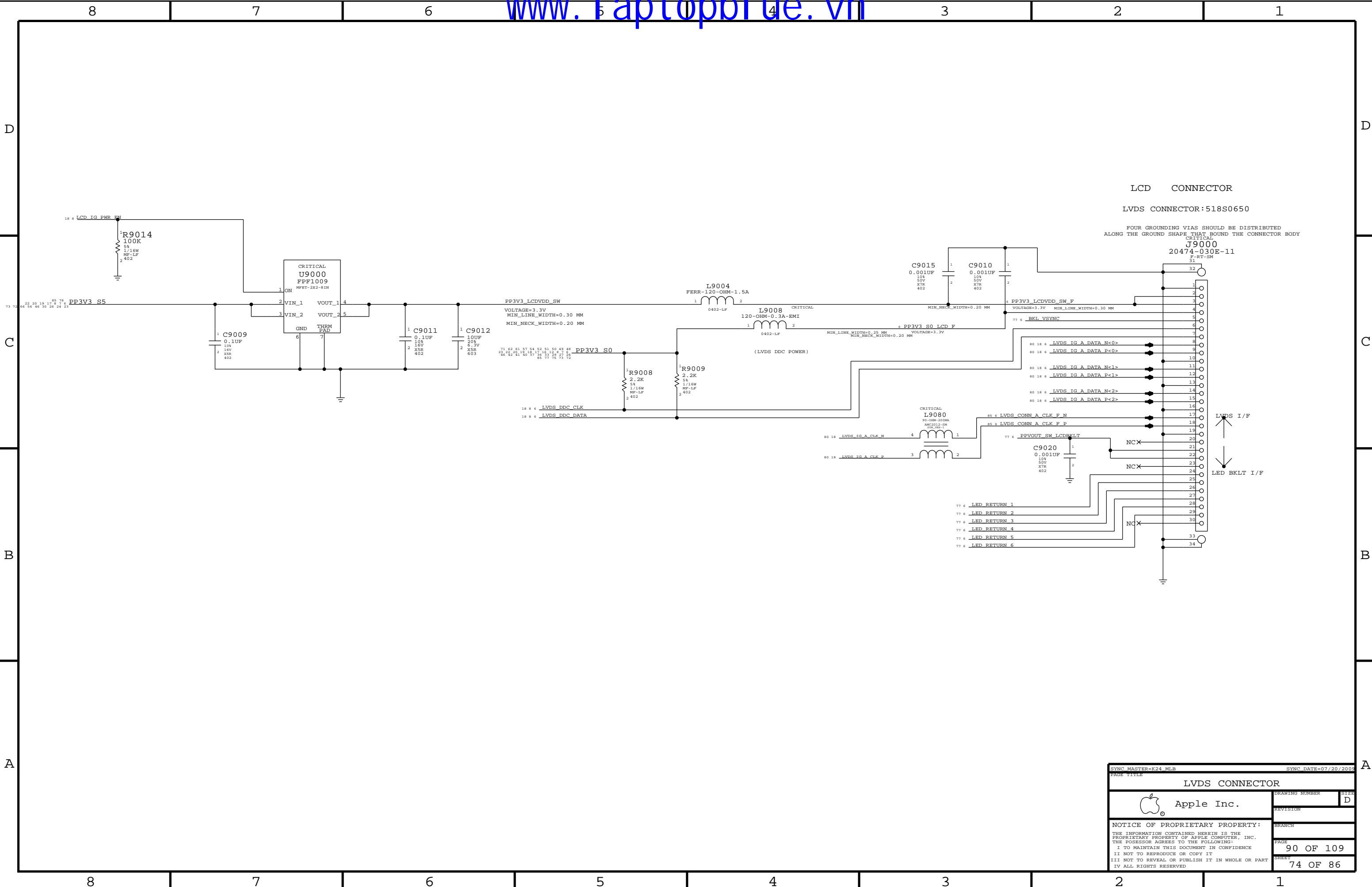
Vout = 1.05V
Max Current = 0.35A





D
C
B
A

D
C
B
A




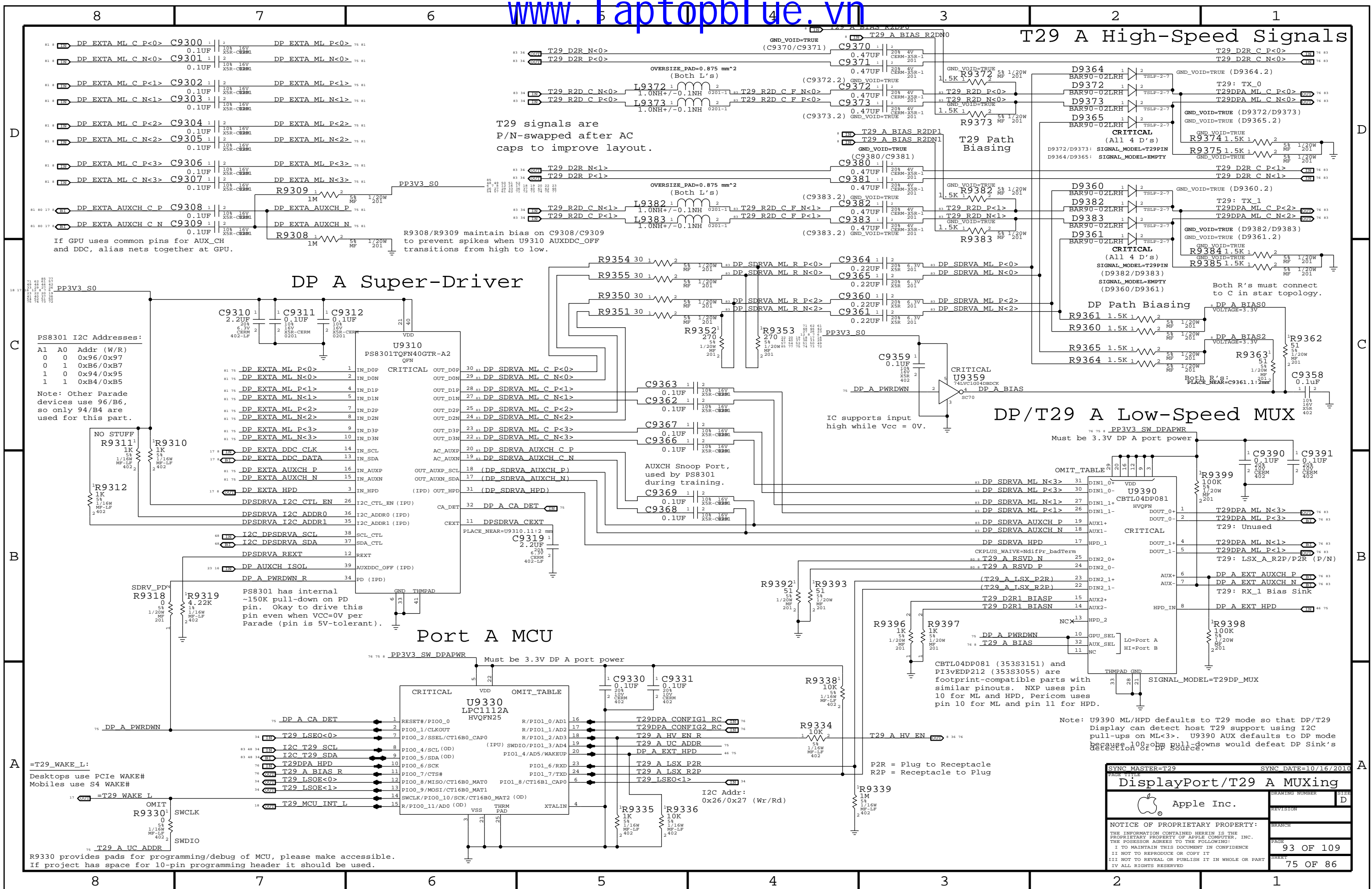
LCD CONNECTOR
LVDS CONNECTOR:518S0650

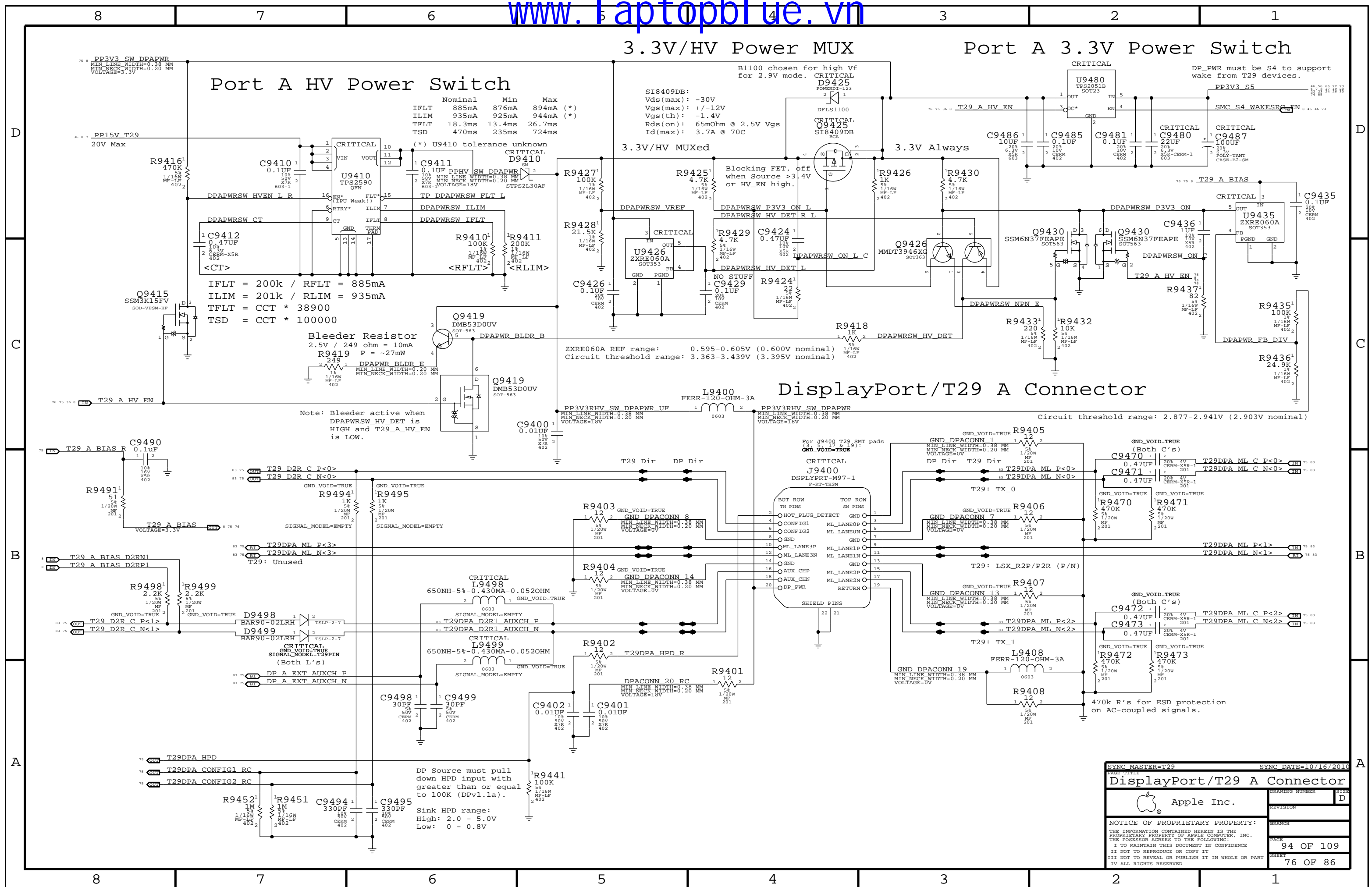
FOUR GROUNDING VIAS SHOULD BE DISTRIBUTED
ALONG THE GROUND SHAPE THAT BOUND THE CONNECTOR BODY

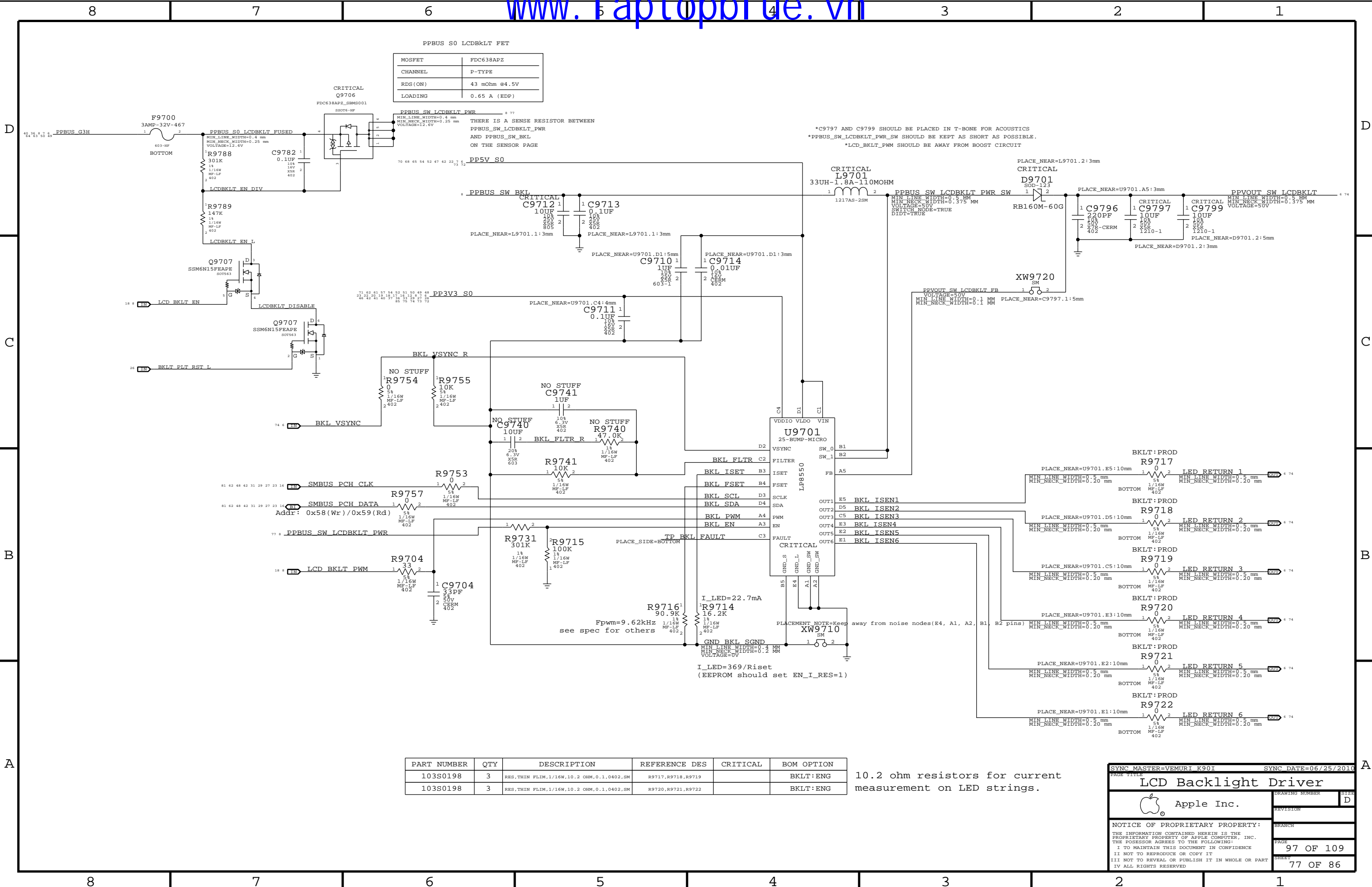
CRITICAL
J9000
20474-030E-11
F-RT-SM

LVDS I/F
LED BLKT I/F

SYNC MASTER=K24 MLB		SYNC DATE=07/20/2005	
PAGE TITLE			
LVDS CONNECTOR			
 Apple Inc.		DRAWING NUMBER	SIZE
			D
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10.2 ohm resistors for current measurement on LED strings.

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?	CPU_AGTL	TOP,BOTTOM	=2X_DIELECTRIC	?
CPU_8MIL	*	8 MIL	?				
CPU_COMP	*	20 MIL	?				
CPU_ITP	*	=2:1_SPACING	?				
CPU_VCCSENSE	*	25 MIL	?				

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Huron River SFF DG (DG-438297_v1.0), Section 4.18 and Huron River Platform Power Delivery DG v1.0 Section 2.7

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?	PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?				

SOURCE: Huron River SFF DG (DG-438297_v1.0), Section 4.18 and Huron River Platform Power Delivery DG v1.0 Section 2.7

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
DMI_S2N	PCIE_85D	PCIE	DMI_S2N P<3:0>	9 17
DMI_S2N	PCIE_85D	PCIE	DMI_S2N N<3:0>	9 17
DMI_N2S	PCIE_85D	PCIE	DMI_N2S P<3:0>	9 17
DMI_N2S	PCIE_85D	PCIE	DMI_N2S N<3:0>	9 17
FDI_DATA	PCIE_85D	PCIE	FDI_DATA P<7:0>	9 17
FDI_DATA	PCIE_85D	PCIE	FDI_DATA N<7:0>	9 17
	CPU_50S	CPU_AGTL	FDI_FSYNC<1..0>	9 17
	CPU_50S	CPU_AGTL	FDI_LSYNC<1..0>	9 17
	CPU_50S	CPU_AGTL	FDI_INT	9 17
CPU_PECI	CPU_50S	PCIE	CPU_PECI	10 19 45
PM_SYNC	CPU_50S	CPU_AGTL	PM_SYNC	10 17
PM_MEM_PWRGD	CPU_50S	CPU_AGTL	PM_MEM_PWRGD	10 17 30
	CPU_50S	CPU_ITP	XDP_DBRESET L	10 23 26
	CPU_50S	CPU_ITP	XDP_CPU_PRDY L	10 23
	CPU_50S	CPU_ITP	XDP_CPU_FREQ L	10 23
	CPU_50S	CPU_AGTL	PM_EXT_TS L<0>	
	CPU_50S	CPU_AGTL	PM_EXT_TS L<1>	
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<0>	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<1>	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2>	10
	CPU_50S	CPU_ITP	CPU_CFG<11..0>	9 23
CPU_CATERR_L	CPU_50S	CPU_AGTL	CPU_CATERR_L	10
	CPU_50S	CPU_AGTL	CPU_VCCIO_SEL	12
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	10 46 68
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	10 19 23
PM_THERMTRIP_L	CPU_50S	CPU_8MIL	PM_THERMTRIP_L	10 19
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_P	10 16
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_N	10 16
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_P	10 16
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_N	10 16
ITPXDPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPXDPCPU_CLK100M_P	16 23
ITPXDPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPXDPCPU_CLK100M_N	16 23
ITPXDPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_P	23
ITPXDPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_N	23
	CPU_27P4S	CPU_COMP	EDP_COMP	9
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	9
XDP_TDI	CPU_50S	CPU_ITP	XDP_CPU_TDI	10 23
XDP_TDO	CPU_50S	CPU_ITP	XDP_CPU_TDO	10 23
XDP_TMS	CPU_50S	CPU_ITP	XDP_CPU_TMS	10 23
XDP_TCK	CPU_50S	CPU_ITP	XDP_CPU_TCK	10 23
XDP_TRST_L	CPU_50S	CPU_ITP	XDP_CPU_TRST_L	10 23
XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM L<3..0>	10 23
XDP_BPM_N_L	CPU_50S	CPU_ITP	CPU_CFG<15..12>	9 23
(FSB_CPUURST_L)	CPU_50S	CPU_ITP	XDP_CPUURST_L	23
CPU_VCCAVG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	12 68
CPU_VCCAVG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	12 68
CPU_VCCIOSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_P	12 70
CPU_VCCIOSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_N	12 70
CPU_VCCAVG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_P	12 68
CPU_VCCAVG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_N	12 68
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDO_SENSE_P	12
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDO_SENSE_N	12
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	9
CPU_VIDALERT_L	CPU_50S	CPU_COMP	CPU_VIDALERT_L	12 68
CPU_VIDSCCLK	CPU_50S	CPU_COMP	CPU_VIDSCCLK	12 68
CPU_VIDSOUT	CPU_50S	CPU_COMP	CPU_VIDSOUT	12 68
PEG_R2D	PCIE_85D	PCIE	PEG_R2D P<15..0>	8
PEG_R2D	PCIE_85D	PCIE	PEG_R2D N<15..0>	8
PEG_R2D	PCIE_85D	PCIE	PEG_R2D C P<15..0>	8
PEG_R2D	PCIE_85D	PCIE	PEG_R2D C N<15..0>	8
PEG_D2R	PCIE_85D	PCIE	PEG_D2R P<15..0>	8
PEG_D2R	PCIE_85D	PCIE	PEG_D2R N<15..0>	8
PEG_D2R	PCIE_85D	PCIE	PEG_D2R C P<15..0>	8
PEG_D2R	PCIE_85D	PCIE	PEG_D2R C N<15..0>	8

CPU_VCCSA_VID<0>
CPU_VCCSA_VID<1>

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_50S	TOP,BOTTOM	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	TOP,BOTTOM	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
MEM_50S	ISL10	N	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	ISL10	N	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
MEM_50S	ISL3,ISL4,ISL9	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	ISL3,ISL4,ISL9	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
MEM_A_CLK	MEM_72D	MEM_CLK	MEM A CLK P<5..0>	11 27
MEM_A_CLK	MEM_72D	MEM_CLK	MEM A CLK N<5..0>	11 27
MEM_A_CMT	MEM_37S	MEM_CTRL	MEM A CKE<3..0>	11 27
MEM_A_CMT	MEM_37S	MEM_CTRL	MEM A CS L<3..0>	11 27
MEM_A_CMT	MEM_37S	MEM_CTRL	MEM A ODT<3..0>	11 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A A<15..0>	11 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A BA<2..0>	11 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A RAS L	11 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A CAS L	11 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A WE L	11 27
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM A DQ<7..0>	11 28
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM A DQ<15..8>	11 28
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM A DQ<23..16>	11 28
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM A DQ<31..24>	11 28
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM A DQ<39..32>	11 27 28
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM A DQ<47..40>	11 28
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM A DQ<55..48>	11 28
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM A DQ<63..56>	11 28
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM A DQS P<0>	11 27 28
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM A DQS N<0>	11 27 28
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM A DQS P<1>	11 28
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM A DQS N<1>	11 28
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM A DQS P<2>	11 28
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM A DQS N<2>	11 28
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM A DQS P<3>	11 28
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM A DQS N<3>	11 28
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM A DQS P<4>	11 28
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM A DQS N<4>	11 28
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM A DQS P<5>	11 28
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM A DQS N<5>	11 28
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM A DQS P<6>	11 28
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM A DQS N<6>	11 28
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM A DQS P<7>	11 28
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM A DQS N<7>	11 28
MEM_B_CLK	MEM_72D	MEM_CLK	MEM B CLK P<5..0>	11 29
MEM_B_CLK	MEM_72D	MEM_CLK	MEM B CLK N<5..0>	11 29
MEM_B_CMT	MEM_37S	MEM_CTRL	MEM B CKE<3..0>	11 29
MEM_B_CMT	MEM_37S	MEM_CTRL	MEM B CS L<3..0>	11 29
MEM_B_CMT	MEM_37S	MEM_CTRL	MEM B ODT<3..0>	11 29
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B A<15..0>	11 29
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B BA<2..0>	11 29
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B RAS L	11 29
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B CAS L	11 29
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B WE L	11 29
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM B DQ<7..0>	11 28
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM B DQ<15..8>	11 28
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM B DQ<23..16>	11 28
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM B DQ<31..24>	11 28
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM B DQ<39..32>	11 28 29
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM B DQ<47..40>	11 28
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM B DQ<55..48>	11 28
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM B DQ<63..56>	11 28
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM B DQS P<0>	11 28 29
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM B DQS N<0>	11 28 29
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM B DQS P<1>	11 28
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM B DQS N<1>	11 28
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM B DQS P<2>	11 28
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM B DQS N<2>	11 28
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM B DQS P<3>	11 28
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM B DQS N<3>	11 28
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM B DQS P<4>	11 28
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM B DQS N<4>	11 28
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM B DQS P<5>	11 28
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM B DQS N<5>	11 28
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM B DQS P<6>	11 28
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM B DQS N<6>	11 28
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM B DQS P<7>	11 28
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM B DQS N<7>	11 28

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=3:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MILS	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM*-style wildcards!

DDR3: Sandybridge SFF 2C when routed on Type-3 (Through hole) should follow rPGA guidelines per Huron River SFF DG rev1.0 (#438297).

DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.

DQ to DQS matching per byte lane should be within 0.127mm.

DQS to clock matching should be within [CLK-63.5mm] and [CLK+38.1mm].

CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.0508mm.

CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0.0mm] of CLK pairs.

A/BA/CMD signals should be matched within [CLK-12.7mm] to [CLK+12.7mm] of CLK pairs A/BA/CMD signals to each other should match within 5.08mm.

DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.

Maximum length of any signal from die pad to SODIMM pad is 119.83mm, from procesor ball to SODIMM pad is 88.9mm.

SOURCE: Huron River Platform DG, Rev 1.01 (#436735), Section 2.5

SYNC MASTER=ANNE K901

SYNC DATE=05/28/2010

Memory Constraints

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SIZE D

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: Calpella Platform Design Guide for Ibox Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibox Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

DisplayPort Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?	DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?

PCI-Express Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3x_DIELECTRIC	?	PCIE	TOP,BOTTOM	=4x_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?				

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_25M_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
LPC_AD	LPC_50S	LPC	LPC AD<3..0>	6 16 45 47
LPC_FRAME_L	LPC_50S	LPC	LPC FRAME L	6 16 45 47
LPC_RESET_L	LPC_50S	LPC	LPCPLUS RESET L	6 26 47
LPC_CLK33M	CLK_LPC_50S	CLK_LPC	LPC CLK33M SMC R	18 26
LPC_CLK33M	CLK_LPC_50S	CLK_LPC	LPC CLK33M SMC	26 45
LPC_CLK33M	CLK_LPC_50S	CLK_LPC	LPC CLK33M LPCPLUS	6 26 47
SMBUS_PCH_CLK	SMB_50S	SMB	SMBUS PCH CLK	16 23 27 29 31 42 48 62 77
SMBUS_PCH_DATA	SMB_50S	SMB	SMBUS PCH DATA	16 23 27 29 31 42 48 62 77
SMBUS_PCH_0_CLK	SMB_50S	SMB	SML PCH 0 CLK	16 48
SMBUS_PCH_0_DATA	SMB_50S	SMB	SML PCH 0 DATA	16 48
SMBUS_PCH_1_CLK	SMB_50S	SMB	SML PCH 1 CLK	16 48
SMBUS_PCH_1_DATA	SMB_50S	SMB	SML PCH 1 DATA	16 48
HDA_BIT_CLK	HDA_50S	HDA	HDA BIT CLK	16 57
HDA_BIT_CLK_R	HDA_50S	HDA	HDA BIT CLK R	16
HDA_SYNC	HDA_50S	HDA	HDA SYNC	16 57
HDA_SYNC_R	HDA_50S	HDA	HDA SYNC R	16
HDA_RST_L	HDA_50S	HDA	HDA RST R L	16
HDA_RST_L	HDA_50S	HDA	HDA RST L	16 57
HDA_SDIN0	HDA_50S	HDA	HDA SDIN0	16 57
AUD_SDI_R	HDA_50S	HDA	AUD SDI R	57
HDA_SDOUT	HDA_50S	HDA	HDA SDOUT	16 57
HDA_SDOUT_R	HDA_50S	HDA	HDA SDOUT R	16
PM_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM CLK32K SUSCLK	
SPI_CLK	SPI_55S	SPI	SPI CLK R	16 47
SPI_CLK	SPI_55S	SPI	SPI CLK	47
SPI_MOSI	SPI_55S	SPI	SPI MOSI R	16 47
SPI_MOSI	SPI_55S	SPI	SPI MOSI	47
SPI_MISO	SPI_55S	SPI	SPI MISO	16 47
SPI_CS0	SPI_55S	SPI	SPI CS0 R L	16 47
SPI_CS0	SPI_55S	SPI	SPI CS0 L	47
PCIE_ENET_R2D_P	PCIE_85D	PCIE	PCIE ENET R2D P	37
PCIE_ENET_R2D_N	PCIE_85D	PCIE	PCIE ENET R2D N	37
PCIE_ENET_R2D_C_P	PCIE_85D	PCIE	PCIE ENET R2D C P	16 37
PCIE_ENET_R2D_C_N	PCIE_85D	PCIE	PCIE ENET R2D C N	16 37
PCIE_ENET_D2R_P	PCIE_85D	PCIE	PCIE ENET D2R P	16 37
PCIE_ENET_D2R_N	PCIE_85D	PCIE	PCIE ENET D2R N	16 37
PCIE_ENET_D2R_C_P	PCIE_85D	PCIE	PCIE ENET D2R C P	37
PCIE_ENET_D2R_C_N	PCIE_85D	PCIE	PCIE ENET D2R C N	37
PCIE_AP_R2D_P	PCIE_85D	PCIE	PCIE AP R2D P	6 32
PCIE_AP_R2D_N	PCIE_85D	PCIE	PCIE AP R2D N	6 32
PCIE_AP_R2D_C_P	PCIE_85D	PCIE	PCIE AP R2D C P	16 32
PCIE_AP_R2D_C_N	PCIE_85D	PCIE	PCIE AP R2D C N	16 32
PCIE_AP_D2R_P	PCIE_85D	PCIE	PCIE AP D2R P	16 32
PCIE_AP_D2R_N	PCIE_85D	PCIE	PCIE AP D2R N	16 32
PCIE_FW_R2D_P	PCIE_85D	PCIE	PCIE FW R2D P	39
PCIE_FW_R2D_N	PCIE_85D	PCIE	PCIE FW R2D N	39
PCIE_FW_R2D_C_P	PCIE_85D	PCIE	PCIE FW R2D C P	16 39
PCIE_FW_R2D_C_N	PCIE_85D	PCIE	PCIE FW R2D C N	16 39
PCIE_FW_D2R_P	PCIE_85D	PCIE	PCIE FW D2R P	16 39
PCIE_FW_D2R_N	PCIE_85D	PCIE	PCIE FW D2R N	16 39
PCIE_FW_D2R_C_P	PCIE_85D	PCIE	PCIE FW D2R C P	39
PCIE_FW_D2R_C_N	PCIE_85D	PCIE	PCIE FW D2R C N	39
PCIE_AP_D2R_PI_P	PCIE_85D	PCIE	PCIE AP D2R PI P	6 32
PCIE_AP_D2R_PI_N	PCIE_85D	PCIE	PCIE AP D2R PI N	6 32
PCIE_AP_R2D_PI_P	PCIE_85D	PCIE	PCIE AP R2D PI P	32
PCIE_AP_R2D_PI_N	PCIE_85D	PCIE	PCIE AP R2D PI N	32
NC_PEG_CLK100MP	CLK_PCIE_90D	CLK_PCIE	NC PEG CLK100MP	8 16
NC_PEG_CLK100MN	CLK_PCIE_90D	CLK_PCIE	NC PEG CLK100MN	8 16
PCIE_CLK100M_ENET_P	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M ENET P	16 37
PCIE_CLK100M_ENET_N	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M ENET N	16 37
PCIE_CLK100M_AP_P	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M AP P	16 32
PCIE_CLK100M_AP_N	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M AP N	16 32
PCIE_CLK100M_FW_P	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M FW P	16 39
PCIE_CLK100M_FW_N	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M FW N	16 39
NC_PCIE_CLK100M_EXCARDP	CLK_PCIE_90D	CLK_PCIE	NC PCIE CLK100M EXCARDP	8 16
NC_PCIE_CLK100M_EXCARDN	CLK_PCIE_90D	CLK_PCIE	NC PCIE CLK100M EXCARDN	8 16
PCH_VSS_NCTF<1>	CPU_2704S	CPU_COMP	PCH VSS NCTF<1>	6
PCH_VSS_NCTF<2>	CPU_2704S	CPU_COMP	PCH VSS NCTF<2>	6
PCH_VSS_NCTF<5>	CPU_2704S	CPU_COMP	PCH VSS NCTF<5>	6
TP_PCH_VSS_NCTF<7>	CPU_2704S	CPU_COMP	TP PCH VSS NCTF<7>	
PCH_VSS_NCTF<9>	CPU_2704S	CPU_COMP	PCH VSS NCTF<9>	6 81
PCH_VSS_NCTF<9>	CPU_2704S	CPU_COMP	PCH VSS NCTF<9>	6 81
PCH_VSS_NCTF<11>	CPU_2704S	CPU_COMP	PCH VSS NCTF<11>	6
PCH_VSS_NCTF<12>	CPU_2704S	CPU_COMP	PCH VSS NCTF<12>	6
PCH_VSS_NCTF<15>	CPU_2704S	CPU_COMP	PCH VSS NCTF<15>	6
PCH_VSS_NCTF<17>	CPU_2704S	CPU_COMP	PCH VSS NCTF<17>	6
PCH_VSS_NCTF<19>	CPU_2704S	CPU_COMP	PCH VSS NCTF<19>	6
PCH_VSS_NCTF<21>	CPU_2704S	CPU_COMP	PCH VSS NCTF<21>	6
PCH_VSS_NCTF<22>	CPU_2704S	CPU_COMP	PCH VSS NCTF<22>	6
PCH_VSS_NCTF<25>	CPU_2704S	CPU_COMP	PCH VSS NCTF<25>	6
PCH_VSS_NCTF<27>	CPU_2704S	CPU_COMP	PCH VSS NCTF<27>	6
PCH_VSS_NCTF<29>	CPU_2704S	CPU_COMP	PCH VSS NCTF<29>	6

Chipset Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
DP_EXTM_ML	DP_85D	DISPLAYPORT	DP_EXTM_ML_C P<3..0>	8 75
DP_EXTM_ML	DP_85D	DISPLAYPORT	DP_EXTM_ML_C N<3..0>	8 75
DP_EXTM_ML	DP_85D	DISPLAYPORT	DP_EXTM_ML_P<3..0>	75
DP_EXTM_ML_N<3..0>	DP_85D	DISPLAYPORT	DP_EXTM_ML_N<3..0>	8 75
DP_EXTM_AUXCH_C_P	DP_85D	DISPLAYPORT	DP_EXTM_AUXCH_C P	8 17 75
DP_EXTM_AUXCH_C_N	DP_85D	DISPLAYPORT	DP_EXTM_AUXCH_C N	80
DP_EXTM_AUXCH_P	DP_85D	DISPLAYPORT	DP_EXTM_AUXCH P	75
DP_EXTM_AUXCH_N	DP_85D	DISPLAYPORT	DP_EXTM_AUXCH N	75
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C P<3..0>	
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C N<3..0>	
DP_INT_AUXCH_C_P	DP_85D	DISPLAYPORT	DP_INT_AUXCH_C P	
DP_INT_AUXCH_C_N	DP_85D	DISPLAYPORT	DP_INT_AUXCH_C N	
PCIE_T29_R2D_C_P<3..0>	PCIE_85D	PCIE	PCIE T29 R2D C P<3..0>	8 34
PCIE_T29_R2D_C_N<3..0>	PCIE_85D	PCIE	PCIE T29 R2D C N<3..0>	8 34
PCIE_T29_R2D_P<3..0>	PCIE_85D	PCIE	PCIE T29 R2D P<3..0>	34
PCIE_T29_R2D_N<3..0>	PCIE_85D	PCIE	PCIE T29 R2D N<3..0>	34
PCIE_T29_D2R_P<3..0>	PCIE_85D	PCIE	PCIE T29 D2R P<3..0>	8 34
PCIE_T29_D2R_N<3..0>	PCIE_85D	PCIE	PCIE T29 D2R N<3..0>	8 34
PCIE_T29_D2R_C_P<3..0>	PCIE_85D	PCIE	PCIE T29 D2R C P<3..0>	34
PCIE_T29_D2R_C_N<3..0>	PCIE_85D	PCIE	PCIE T29 D2R C N<3..0>	34
PCIE_CLK100M_T29_P	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M T29 P	16 34
PCIE_CLK100M_T29_N	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M T29 N	16 34

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
SYSCLK_CLK32K_RTC	CLK_SLOW_55S	CLK_SLOW	SYSCLK CLK32K RTC	16 26
SYSCLK_CLK25M_SB	CLK_25M_55S	CLK_25M	SYSCLK CLK25M SB	16 26
SYSCLK_CLK25M_SB_R	CLK_25M_55S	CLK_25M	SYSCLK CLK25M SB R	16
SYSCLK_CLK25M_ENET	CLK_25M_55S	CLK_25M	SYSCLK CLK25M ENET	26 37
SYSCLK_CLK25M_ENET_R	CLK_25M_55S	CLK_25M	SYSCLK CLK25M ENET R	
SYSCLK_CLK25M_T29	CLK_25M_55S	CLK_25M	SYSCLK CLK25M T29	26 34
SYSCLK_CLK25M_T29_R	CLK_25M_55S	CLK_25M	SYSCLK CLK25M T29 R	34

CAESAR IV (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_3X	*	=3:1_SPACING	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_CR_DATA	*	5MIL	?

CAESAR IV (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	0.6 MM	?













SOURCE: Broadcom 5764-DS04-RDS Page 38

FireWire Interface Constraints









PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

Ethernet Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALI	
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALO	
	ENET_50S	ENET_3X	ENET_RESET_L	33 37
	ENET_MDI		ENET_MDI_P<3..0>	37 38
	ENET_100D	ENET_MDI	ENET_MDI_N<3..0>	37 38
	ENET_50S	ENET_CR_DATA	ENET_CR_DATA<7..0>	33 37
	ENET_50S	ENET_CR_DATA	ENET_CR_CMD	33 37
	ENET_50S	ENET_CR_DATA	ENET_CR_CLK	33 37
	ENET_50S	ENET_CR_DATA	SDCONN_DATA<7..0>	33
	ENET_50S	ENET_CR_DATA	SDCONN_CMD	33
	ENET_50S	ENET_CR_DATA	SDCONN_CLK	33
	ENET_50S	ENET_CR_DATA	SDCONN_CLK_L	33

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
	FW_P0_TPA	FW_110D	FW_TP	NC_FW0_TPAP
	FW_P0_TPA	FW_110D	FW_TP	NC_FW0_TPAP
	FW_P0_TPB	FW_110D	FW_TP	NC_FW0_TPB
	FW_P0_TPB	FW_110D	FW_TP	NC_FW0_TPB
	FW_P1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_P
	FW_P1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_N
	FW_P1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_P
	FW_P1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_N
Port 2 Not Used				

DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

T29 I2C Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_I2C	*	=2x_DIELECTRIC	?

T29 SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SPI	*	=2x_DIELECTRIC	?

T29/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
T29DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	*	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	TOP,BOTTOM	=7x_DIELECTRIC	?

SOURCE: Bill Cornelius's T29 Routing Notes

T29 IC Net Properties

NET TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
DP_85D	DP_85D	DISPLAYPORT	DP T29SNK0 ML C P<3..0> 8 34
DP_85D	DP_85D	DISPLAYPORT	DP T29SNK0 ML C N<3..0> 8 34
DP_T29SNK0_ML	DP_85D	DISPLAYPORT	DP T29SNK0 ML P<3..0> 34
DP_T29SNK0_ML	DP_85D	DISPLAYPORT	DP T29SNK0 ML N<3..0> 34
DP_85D	DP_85D	DISPLAYPORT	DP T29SNK0 AUXCH C P 8 17 34
DP_85D	DP_85D	DISPLAYPORT	DP T29SNK0 AUXCH C N 8 17 34
DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP T29SNK0 AUXCH P 34
DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP T29SNK0 AUXCH N 34
DP_85D	DP_85D	DISPLAYPORT	DP T29SNK1 ML C P<3..0> 8 34
DP_85D	DP_85D	DISPLAYPORT	DP T29SNK1 ML C N<3..0> 8 34
DP_T29SNK1_ML	DP_85D	DISPLAYPORT	DP T29SNK1 ML P<3..0> 34
DP_T29SNK1_ML	DP_85D	DISPLAYPORT	DP T29SNK1 ML N<3..0> 34
DP_85D	DP_85D	DISPLAYPORT	DP T29SNK1 AUXCH C P 8 17 34
DP_85D	DP_85D	DISPLAYPORT	DP T29SNK1 AUXCH C N 8 17 34
DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP T29SNK1 AUXCH P 34
DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP T29SNK1 AUXCH N 34
DP_85D	DP_85D	DISPLAYPORT	DP T29SRC ML C P<3..0>
DP_85D	DP_85D	DISPLAYPORT	DP T29SRC ML C N<3..0>
DP_85D	DP_85D	DISPLAYPORT	DP T29SRC AUXCH C P
DP_85D	DP_85D	DISPLAYPORT	DP T29SRC AUXCH C N
DP_85D	T29_I2C_55S	T29_I2C	I2C T29_SCL 34 48 75
DP_85D	T29_I2C_55S	T29_I2C	I2C T29_SDA 34 48 75
DP_85D	T29_SPI_CLK	T29_SPI	T29_SPI_CLK 34
DP_85D	T29_SPI_MOSI	T29_SPI	T29_SPI_MOSI 34
DP_85D	T29_SPI_MISO	T29_SPI	T29_SPI_MISO 34
DP_85D	T29_SPI_CS_L	T29_SPI	T29_SPI_CS_L 34
DP_85D	T29DP_80D	T29DP	T29_R2D C P<3..0> 8 34 75
DP_85D	T29DP_80D	T29DP	T29_R2D C N<3..0> 8 34 75
DP_85D	T29DP_100D	T29DP	T29_D2R P<3..0> 8 34 75
DP_85D	T29DP_100D	T29DP	T29_D2R N<3..0> 8 34 75

Only used on hosts supporting T29 video-in

T29/DP Net Properties

NET TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
DP_85D	T29DP_80D	T29DP	T29_R2D P<0> 75
DP_85D	T29DP_80D	T29DP	T29_R2D N<0> 75
DP_85D	T29DP_80D	T29DP	T29_R2D P<1> 75
DP_85D	T29DP_80D	T29DP	T29_R2D N<1> 75
DP_85D	T29DP_80D	T29DP	T29_R2D C F P<1..0> 75
DP_85D	T29DP_80D	T29DP	T29_R2D C F N<1..0> 75
DP_85D	T29DP_100D	T29DP	T29_D2R C P<0> 75 76
DP_85D	T29DP_100D	T29DP	T29_D2R C N<0> 75 76
DP_85D	T29DP_100D	T29DP	T29_D2R C P<1> 75 76
DP_85D	T29DP_100D	T29DP	T29_D2R C N<1> 75 76
DP_85D	T29DP_100D	T29DP	T29DPA_D2R1_AUXCH_P 76
DP_85D	T29DP_100D	T29DP	T29DPA_D2R1_AUXCH_N 76
DP_85D	T29DP_80D	T29DP	DP_SDRVA_ML_C_P<3..0> 75
DP_85D	T29DP_80D	T29DP	DP_SDRVA_ML_C_N<3..0> 75
DP_85D	T29DP_80D	T29DP	DP_SDRVA_ML_R_P<3..0> 75
DP_85D	T29DP_80D	T29DP	DP_SDRVA_ML_R_N<3..0> 75
DP_85D	T29DP_80D	T29DP	DP_SDRVA_ML_P<2..0:2> 75 83
DP_85D	T29DP_80D	T29DP	DP_SDRVA_ML_N<2..0:2> 75 83
DP_85D	T29DP_80D	T29DP	DP_SDRVA_ML_P<3..1:2> 75
DP_85D	T29DP_80D	T29DP	DP_SDRVA_ML_N<3..1:2> 75
DP_85D	T29DP_80D	T29DP	DP_SDRVA_AUXCH_P 75
DP_85D	T29DP_80D	T29DP	DP_SDRVA_AUXCH_N 75
DP_85D	T29DP_80D	T29DP	DP_SDRVA_AUXCH_C_P 75
DP_85D	T29DP_80D	T29DP	DP_SDRVA_AUXCH_C_N 75
DP_85D	T29DP_80D	T29DP	T29DPA_ML_P<3..0> 75 76
DP_85D	T29DP_80D	T29DP	T29DPA_ML_N<3..0> 75 76
DP_85D	T29DP_80D	T29DP	T29DPA_ML_C_P<3..0> 75 76
DP_85D	T29DP_80D	T29DP	T29DPA_ML_C_N<3..0> 75 76
DP_85D	T29DP_80D	T29DP	DP_A_EXT_AUXCH_P 75 76
DP_85D	T29DP_80D	T29DP	DP_A_EXT_AUXCH_N 75 76
DP_85D	T29DP_80D	T29DP	T29_R2D P<2>
DP_85D	T29DP_80D	T29DP	T29_R2D N<2>
DP_85D	T29DP_80D	T29DP	T29_R2D P<3>
DP_85D	T29DP_80D	T29DP	T29_R2D N<3>
DP_85D	T29DP_80D	T29DP	T29_R2D C F P<3..2>
DP_85D	T29DP_80D	T29DP	T29_R2D C F N<3..2>
DP_85D	T29DP_100D	T29DP	T29_D2R C P<2>
DP_85D	T29DP_100D	T29DP	T29_D2R C N<2>
DP_85D	T29DP_100D	T29DP	T29_D2R C P<3>
DP_85D	T29DP_100D	T29DP	T29_D2R C N<3>
DP_85D	T29DP_100D	T29DP	T29DPB_D2R3_AUXCH_P
DP_85D	T29DP_100D	T29DP	T29DPB_D2R3_AUXCH_N
DP_85D	T29DP_80D	T29DP	DP_SDRVB_ML_C_P<3..0>
DP_85D	T29DP_80D	T29DP	DP_SDRVB_ML_C_N<3..0>
DP_85D	T29DP_80D	T29DP	DP_SDRVB_ML_R_P<3..0>
DP_85D	T29DP_80D	T29DP	DP_SDRVB_ML_R_N<3..0>
DP_85D	T29DP_80D	T29DP	DP_SDRVB_ML_P<2..0:2> 83
DP_85D	T29DP_80D	T29DP	DP_SDRVB_ML_N<2..0:2> 83
DP_85D	T29DP_80D	T29DP	DP_SDRVB_ML_P<3..1:2>
DP_85D	T29DP_80D	T29DP	DP_SDRVB_ML_N<3..1:2>
DP_85D	T29DP_80D	T29DP	DP_SDRVB_AUXCH_P
DP_85D	T29DP_80D	T29DP	DP_SDRVB_AUXCH_N
DP_85D	T29DP_80D	T29DP	DP_SDRVB_AUXCH_C_P
DP_85D	T29DP_80D	T29DP	DP_SDRVB_AUXCH_C_N
DP_85D	T29DP_80D	T29DP	T29DPB_ML_P<3..0>
DP_85D	T29DP_80D	T29DP	T29DPB_ML_N<3..0>
DP_85D	T29DP_80D	T29DP	T29DPB_ML_C_P<3..0>
DP_85D	T29DP_80D	T29DP	T29DPB_ML_C_N<3..0>
DP_85D	T29DP_80D	T29DP	DP_B_EXT_AUXCH_P
DP_85D	T29DP_80D	T29DP	DP_B_EXT_AUXCH_N

Only used on dual-port hosts.

A Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.


PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MDX_720	BOTTOM			0.127 MM	6.35 MM		
MDX_850	TOP			0.1 MM	6.35 MM		

K90i Specific Net Properties

ELECTRICAL CONSTRAINT SET		NET_TYPE		
		PHYSICAL	SPACING	
		ENETCONN	ENETCONN	ENETCONN P<3..0>
		ENETCONN	ENETCONN	ENETCONN N<3..0>
		SATA_00D	SATA	SATA_ODD_D2R_0UF_P
		SATA_00D	SATA	SATA_ODD_D2R_0UF_N
		SATA_00D	SATA	SATA_HDD_D2R_RDRVR_OUT_P
		SATA_00D	SATA	SATA_HDD_D2R_RDRVR_OUT_N
		SATA_00D	SATA	SATA_HDD_R2D_RDRVR_IN_P
		SATA_00D	SATA	SATA_HDD_R2D_RDRVR_IN_N
		SATA_00D	SATA	SATA_HDD_D2R_RDRVR_IN_P
		SATA_00D	SATA	SATA_HDD_D2R_RDRVR_IN_N
		SATA_00D	SATA	SATA_HDD_R2D_RDRVR_OUT_P
		SATA_00D	SATA	SATA_HDD_R2D_RDRVR_OUT_N
		CPUTHIMNS	CPUTHIMNS	CPUTHIMNS_D2_P
		CPUTHIMNS	CPUTHIMNS	CPUTHIMNS_D2_N
		CPU_THERMD	CPU_THERMD	CPU_THERMD_P
		CPU_THERMD	CPU_THERMD	CPU_THERMD_N
		T29_THERMD	T29_THERMD	T29_THERMD_P
		T29_THERMD	T29_THERMD	T29_THERMD_N
		T29TIMMNS	T29TIMMNS	T29TIMMNS_D2_P
		T29TIMMNS	T29TIMMNS	T29TIMMNS_D2_N
		ISNS_HS_COMPUTING	ISNS_HS_COMPUTING	ISNS_HS_COMPUTING_P
		ISNS_HS_COMPUTING	ISNS_HS_COMPUTING	ISNS_HS_COMPUTING_N
		ISNS_HS_OTHER	ISNS_HS_OTHER	ISNS_HS_OTHER_P
		ISNS_HS_OTHER	ISNS_HS_OTHER	ISNS_HS_OTHER_N
		CPUVCCIOS0_CS	CPUVCCIOS0_CS	CPUVCCIOS0_CS_P
		CPUVCCIOS0_CS	CPUVCCIOS0_CS	CPUVCCIOS0_CS_N
		CPUIUMVP_ISNS1	CPUIUMVP_ISNS1	CPUIUMVP_ISNS1_P
		CPUIUMVP_ISNS1	CPUIUMVP_ISNS1	CPUIUMVP_ISNS1_N
		CPUIUMVP_ISNS2	CPUIUMVP_ISNS2	CPUIUMVP_ISNS2_P
		CPUIUMVP_ISNS2	CPUIUMVP_ISNS2	CPUIUMVP_ISNS2_N
		CPUIUMVP_ISNS1G	CPUIUMVP_ISNS1G	CPUIUMVP_ISNS1G_P
		CPUIUMVP_ISNS1G	CPUIUMVP_ISNS1G	CPUIUMVP_ISNS1G_N
		CPUIUMVP_ISUM_R	CPUIUMVP_ISUM_R	CPUIUMVP_ISUM_R_P
		CPUIUMVP_ISUM_R	CPUIUMVP_ISUM_R	CPUIUMVP_ISUM_R_N
		CPUIUMVP_ISUMG_R	CPUIUMVP_ISUMG_R	CPUIUMVP_ISUMG_R_P
		CPUIUMVP_ISUMG_R	CPUIUMVP_ISUMG_R	CPUIUMVP_ISUMG_R_N
		CPUIUMVP_ISNS_P	CPUIUMVP_ISNS_P	CPUIUMVP_ISNS_P
		CPUIUMVP_ISNS_P	CPUIUMVP_ISNS_P	CPUIUMVP_ISNS_N
		VCCHSAS0_CS_P	VCCHSAS0_CS_P	VCCHSAS0_CS_P
		VCCHSAS0_CS_P	VCCHSAS0_CS_P	VCCHSAS0_CS_N
		CPUIUMVP_ISUMG_P	CPUIUMVP_ISUMG_P	CPUIUMVP_ISUMG_P
		CPUIUMVP_ISUMG_P	CPUIUMVP_ISUMG_P	CPUIUMVP_ISUMG_N
		ISNS_CPU_N	ISNS_CPU_N	ISNS_CPU_N
		ISNS_CPU_P	ISNS_CPU_P	ISNS_CPU_P
		ISNS_HDD_N	ISNS_HDD_N	ISNS_HDD_N
		ISNS_HDD_P	ISNS_HDD_P	ISNS_HDD_P
		ISNS_HDD_R_N	ISNS_HDD_R_N	ISNS_HDD_R_N
		ISNS_HDD_R_P	ISNS_HDD_R_P	ISNS_HDD_R_P
		ISNS_LCDBKLT_N	ISNS_LCDBKLT_N	ISNS_LCDBKLT_N
		ISNS_LCDBKLT_P	ISNS_LCDBKLT_P	ISNS_LCDBKLT_P
		ISNS_ODD_N	ISNS_ODD_N	ISNS_ODD_N
		ISNS_ODD_P	ISNS_ODD_P	ISNS_ODD_P
		ISNS_ODD_R_N	ISNS_ODD_R_N	ISNS_ODD_R_N
		ISNS_ODD_R_P	ISNS_ODD_R_P	ISNS_ODD_R_P
		ISNS_P1V8GPU_N	ISNS_P1V8GPU_N	ISNS_P1V8GPU_N
		ISNS_P1V8GPU_P	ISNS_P1V8GPU_P	ISNS_P1V8GPU_P
		ISNS_P1V8GPU_R_N	ISNS_P1V8GPU_R_N	ISNS_P1V8GPU_R_N
		ISNS_P1V8GPU_R_P	ISNS_P1V8GPU_R_P	ISNS_P1V8GPU_R_P
		LVDS_CONN_A_CLK_P_N	LVDS_CONN_A_CLK_P_N	LVDS_CONN_A_CLK_P_N
		LVDS_CONN_A_CLK_P_P	LVDS_CONN_A_CLK_P_P	LVDS_CONN_A_CLK_P_P

K90i Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	
PCIE_C1K100M_AP	CLK_PCIE_S0D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P
	CLK_PCIE_S0D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N
	170I_DIFFEAIR		CHGR_CSI_R_P
	170I_DIFFEAIR		CHGR_CSI_R_N
	170I_DIFFEAIR		CHGR_CSO_R_P
	170I_DIFFEAIR		CHGR_CSO_R_N
(USB_EXT2)	USB_S0D	USB	USB2_EXT2_MIXED_P
(USB_EXT2)	USB_S0D	USB	USB2_EXT2_MIXED_N
(USB_EXT2)	USB_S0D	USB	USB2_LT1_P
(USB_EXT2)	USB_S0D	USB	USB2_LT1_N
	USB_S0D	USB	CONN_USB2_BT_P
	USB_S0D	USB	CONN_USB2_BT_N
	USB_S0D	USB	USB_LT2_P
	USB_S0D	USB	USB_LT2_N
	DP_S0D	DISPLAYPORT	DP_IG_AUX_CH_C_P
	DP_S0D	DISPLAYPORT	DP_IG_AUX_CH_C_N
SPK_OUT	DIFFEAIR	AUDIO	SPKRAMP_L_P_OUT
SPK_OUT	DIFFEAIR	AUDIO	SPKRAMP_L_N_OUT
SPK_OUT	DIFFEAIR	AUDIO	SPKRAMP_SUB_P_OUT
SPK_OUT	DIFFEAIR	AUDIO	SPKRAMP_SUB_N_OUT
SPK_OUT	DIFFEAIR	AUDIO	SPKRAMP_R_P_OUT
SPK_OUT	DIFFEAIR	AUDIO	SPKRAMP_R_N_OUT
AUD_DIFF	170I_DIFFEAIR	AUDIO	SSM2315_SUB_N
AUD_DIFF	170I_DIFFEAIR	AUDIO	SSM2315_SUB_P
AUD_DIFF	170I_DIFFEAIR	AUDIO	SSM2315_L_N
AUD_DIFF	170I_DIFFEAIR	AUDIO	SSM2315_L_P
AUD_DIFF	170I_DIFFEAIR	AUDIO	SSM2315_R_N
AUD_DIFF	170I_DIFFEAIR	AUDIO	SSM2315_R_P
AUD_DIFF	170I_DIFFEAIR	AUDIO	AUD_LO2_N_R
AUD_DIFF	170I_DIFFEAIR	AUDIO	AUD_LO2_P_R
AUD_DIFF	170I_DIFFEAIR	AUDIO	AUD_LO1_N_R
AUD_DIFF	170I_DIFFEAIR	AUDIO	AUD_LO1_P_R
AUD_DIFF	170I_DIFFEAIR	AUDIO	AUD_LO2_N_L
AUD_DIFF	170I_DIFFEAIR	AUDIO	AUD_LO2_P_L
AUD_DIFF	170I_DIFFEAIR	AUDIO	SPKRAMP_INL_P
AUD_DIFF	170I_DIFFEAIR	AUDIO	SPKRAMP_INL_N
AUD_DIFF	170I_DIFFEAIR	AUDIO	SPKRAMP_INR_P
AUD_DIFF	170I_DIFFEAIR	AUDIO	SPKRAMP_INR_N
AUD_DIFF	170I_DIFFEAIR	AUDIO	SPKRAMP_INSUB_P
AUD_DIFF	170I_DIFFEAIR	AUDIO	SPKRAMP_INSUB_N
	USB_S0D	USB	USB_TPAD_R_P
	USB_S0D	USB	USB_TPAD_R_N
	SR_POWER		PPIV3_05
	SR_POWER		PPIV3_00
	SR_POWER		PPIV5_03R00
	GND		GND

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