

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM, WHITE_ARROW, MLB, K18

02/01/10

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
<REV>	<ECN>	<ECO_DESCRIPTION>	<ECODATE>

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29	DDR3 Byte/Bit Swaps	MASTER	MASTER
30	DDR3 SO-DIMM Connector B	MASTER	MASTER
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32	FSB/DDR3/FRAMEBUF Vref Margining	K17_REF	06/15/2009
33	X16/ALS/CAMERA CONNECTOR	K18_COMMS	06/15/2009
34	SecureDigital Card Reader	T27_REF	08/26/2009
35	USB HUB 1	K18_MLB	10/07/2009
36	USB HUB 2	K23F	10/06/2009
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44	Front Flex Support	K19_MLB	05/29/2009
45	SMC	K17_REF	06/15/2009

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56	DEBUG SENSORS AND ADC	K18_SENSORS	07/07/2009
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64	DC-In & Battery Connectors	K18_POWER	06/30/2009
65	PBus Supply & Battery Charger	K18_POWER	06/30/2009
66	5V / 3.3V Power Supply	K18_POWER	07/13/2009
67	1.5V DDR3 Supply	K18_POWER	07/14/2009
68	CPU IMVP VCore Regulator	K18_POWER	06/29/2009
69	GFX IMVP VCore Regulator	K18_POWER	07/08/2009
70	CPUVTT (1.05V) Power Supply	K18_POWER	07/14/2009
71	Misc Power Supplies	K18_POWER	06/29/2009
72	Power FETs	K18_POWER	06/10/2009
73	Power Control	K17_REF	06/15/2009
74	NV GT216 PCI-E	K17_REF	06/15/2009
75	NV GT216 CORE/FB POWER	K17_REF	06/15/2009
76	NV GT216 FRAME BUFFER I/F	K17_REF	06/15/2009
77	GDDR3 Frame Buffer A (Top)	K17_REF	06/15/2009
78	GDDR3 Frame Buffer B (Top)	K17_REF	06/15/2009
79	NV GT216 GPIO/MIO/MISC	K17_REF	06/15/2009
80	GT216 GPIOs & STRAPS	K17_REF	06/15/2009
81	NV GT216 VIDEO INTERFACES	K17_REF	06/15/2009
82	GPU (GT216) CORE SUPPLY	K18_POWER	07/14/2009
83	LVDS Display Connector	K19_MLB	05/29/2009
84	Muxed Graphics Support	K17_REF	06/15/2009
85	DisplayPort Connector	K17_REF	06/15/2009
86	1V8 / 1V55 FB Power Supply	K18_POWER	06/26/2009
87	Graphics MUX (GMUX)	K17_REF	06/15/2009
88	LCD BACKLIGHT DRIVER	K18_BKLT	07/29/2009
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90	Misc Power Supplies	K18_POWER	06/10/2009


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97	SMC Constraints	K17_REF	06/15/2009
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100	PCB Rule Definitions	K17_REF	06/15/2009
101	BluRay Decrypter Card Connector	K17_REF	06/15/2009

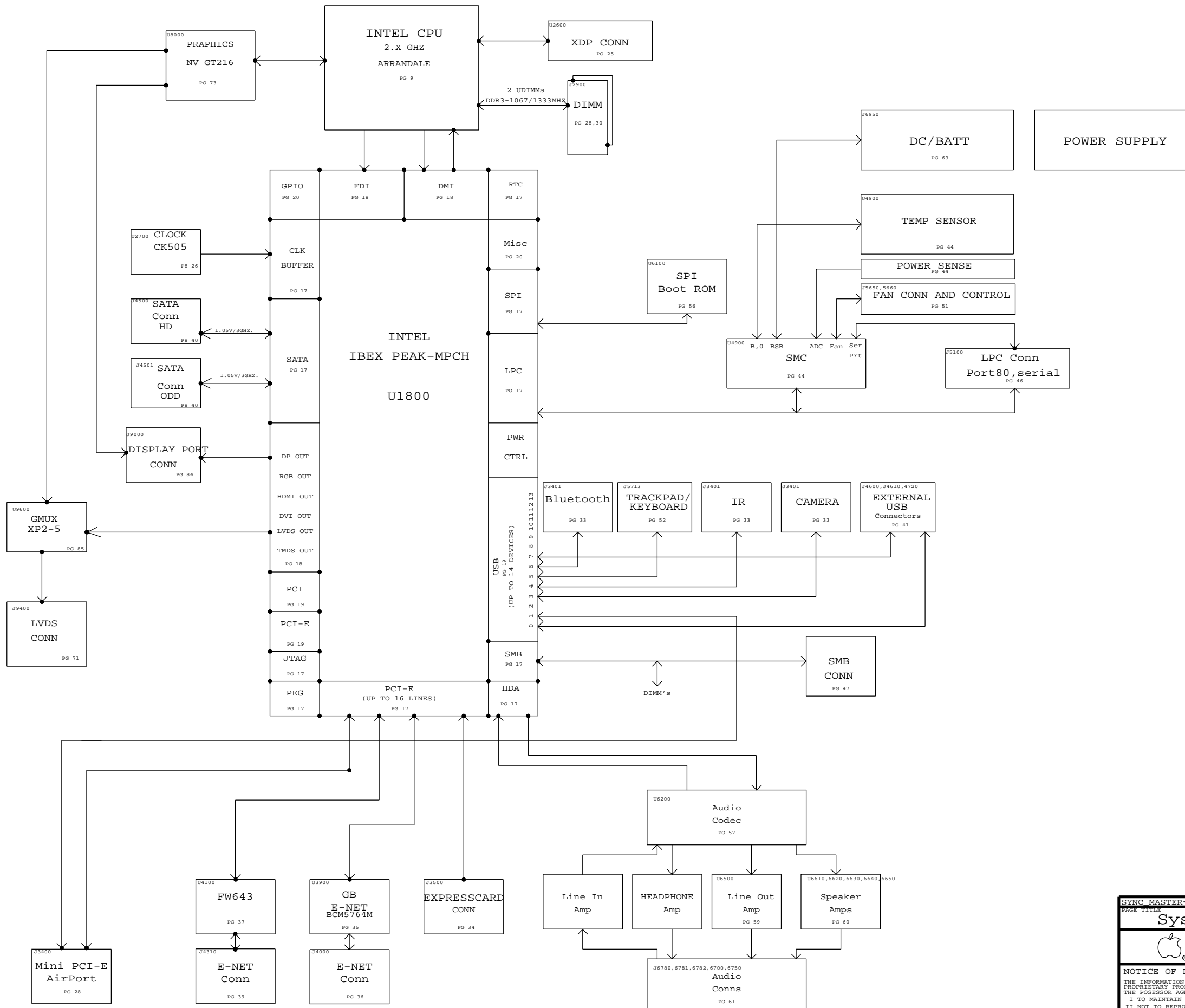
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Schematic / PCB #'s

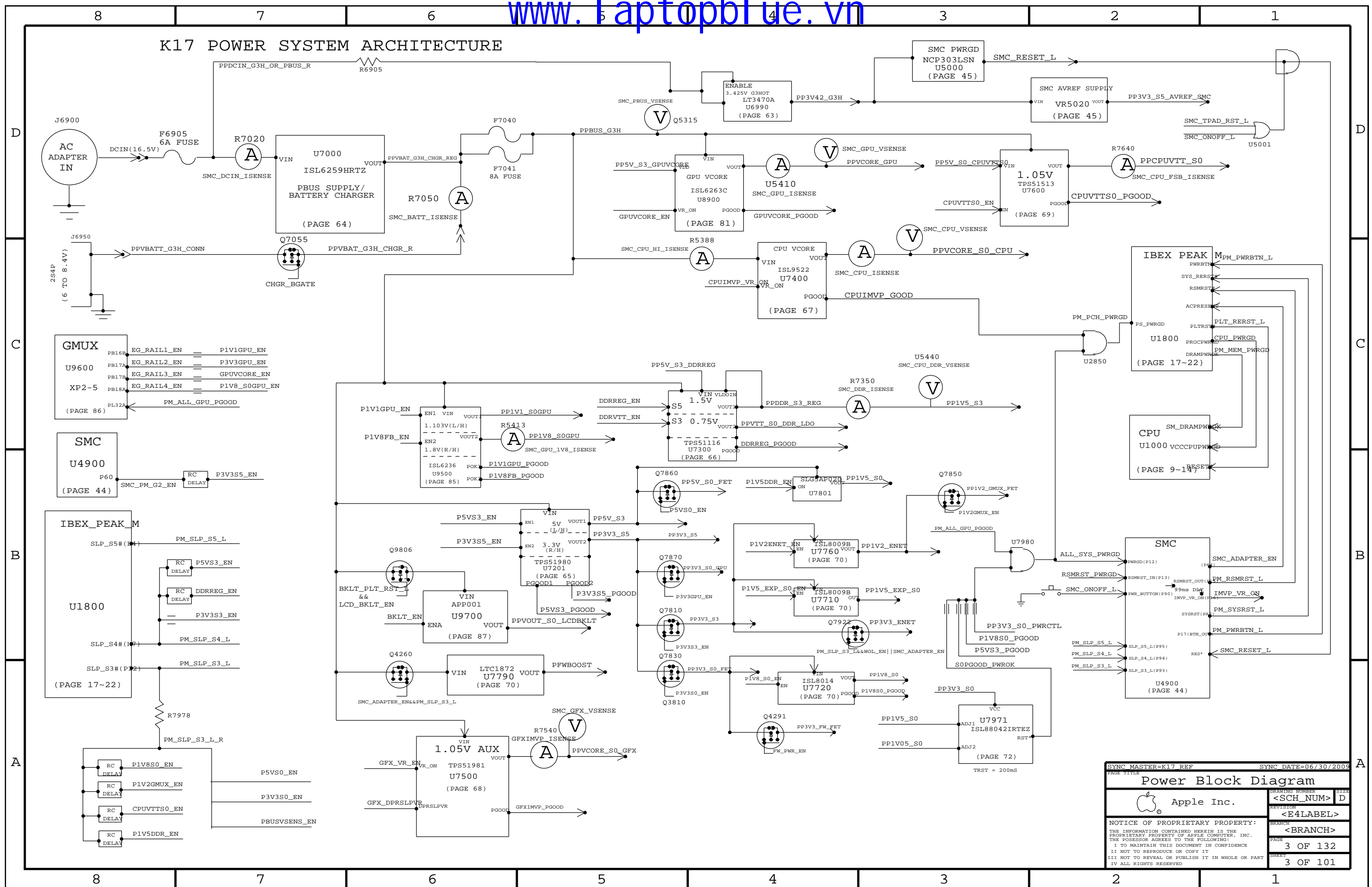
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820-2850	1	PCBF, WHITE_ARROW, MLB, K18	PCB	CRITICAL	

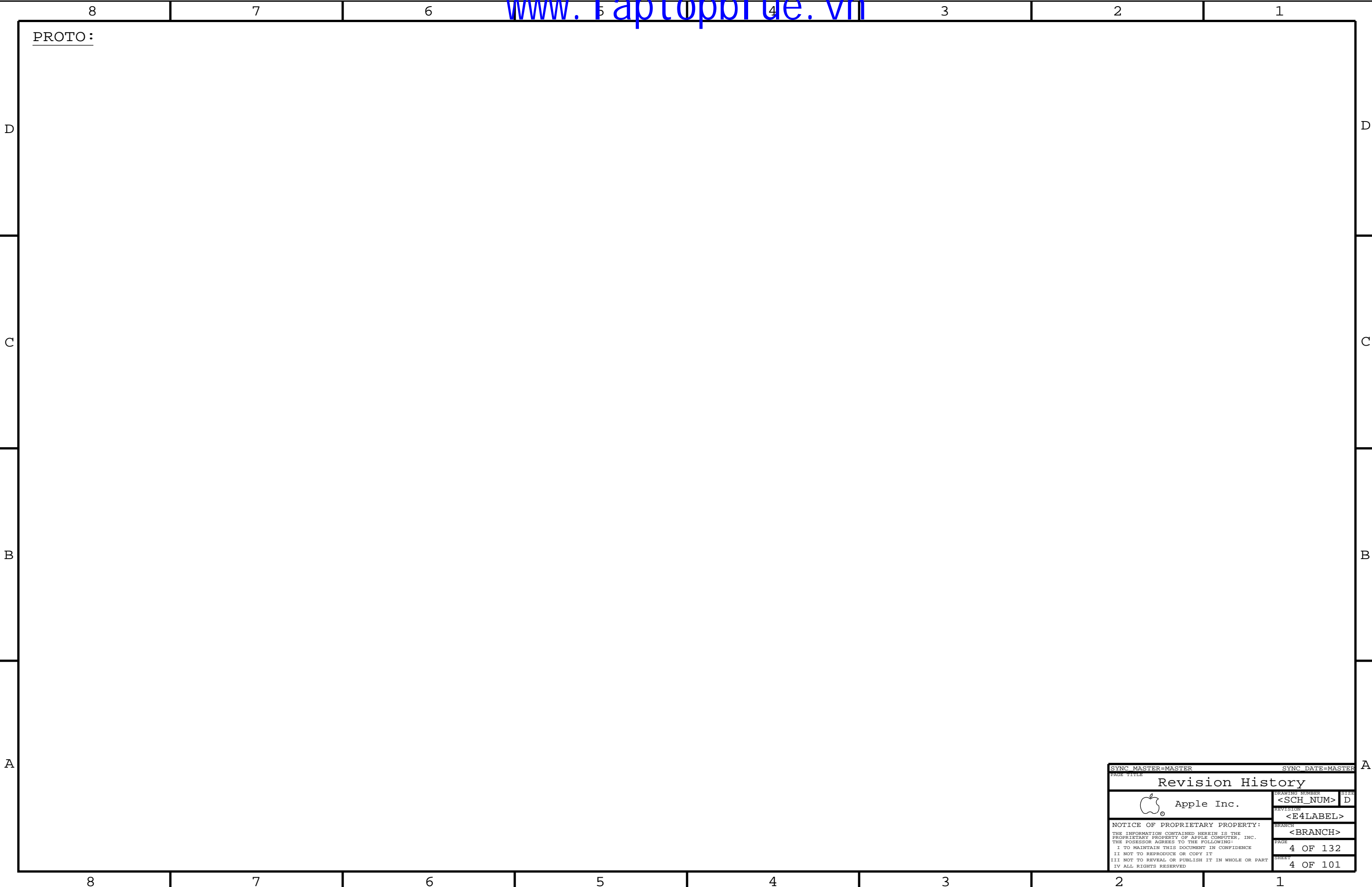
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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-0952	PCBA, 2.0G, 512SAM_VRAM, K18	K18_COMMON, CPU_2_4GHZ, FB_256_SAMSUNG, K18_PVT, EEEE_DCJ7
639-0953	PCBA, 2.0G, 512HYN_VRAM, K18	K18_COMMON, CPU_2_4GHZ, FB_256_HYNIX, K18_PVT, EEEE_DCJ8
639-0954	PCBA, 2.13G, 512SAM_VRAM, K18	K18_COMMON, CPU_2_53GHZ, FB_512_SAMSUNG, K18_PVT, EEEE_DCJ9
639-0955	PCBA, 2.13G, 512HYN_VRAM, K18	K18_COMMON, CPU_2_53GHZ, FB_512_HYNIX, K18_PVT, EEEE_DCJC
639-0956	PCBA, 2.4G, 512SAM_VRAM, K18	K18_COMMON, CPU_2_66GHZ, FB_512_SAMSUNG, K18_PVT, EEEE_DCJD
639-0957	PCBA, 2.4G, 512HYN_VRAM, K18	K18_COMMON, CPU_2_66GHZ, FB_512_HYNIX, K18_PVT, EEEE_DCJF
085-1404	K18 DEVELOPMENT BOM	

K18 BOM GROUPS

BOM GROUP	BOM OPTIONS
K18_COMMON	ALTERNATE, COMMON, K18_COMMON1, K18_COMMON2, K18_PROGPARTS, USBHUB_2061, RDRV:8515A2, DCI
K18_COMMON1	BATT_3S, BCM5764M, GL137, CPUPOC_IMAX_40_50, CPUMEM_S0, SMC_EXCARD_NOT, SMC_DEBUG_YES, HUB1_2NONREM, HUB2_3NONREM
K18_COMMON2	GMUXPLL_3V3, GPU_SS_INT, MIKEY, GPUVID_0P90V, DPMUX_EN_PLD, DP_CA_DET_EG_PLD, DP_ESD, VFRQ_SLPS3, SMC_OSC_YES, RAIL_MON
K18_PVT	BMON_PROD, VREFMRGN_NOT, XDP, XDP_NORMAL, XDP_CPU_BPM
K18_PROGPARTS	GMUX_PROG, BOOTROM_PROG, SMC_PROG, TPAD_PROG

BOM GROUP	BOM OPTIONS
FB_256_SAMSUNG	VRAM4, VRAM_256_SAMSUNG, FB1V55
FB_256_HYNIX	VRAM4, VRAM_256_HYNIX, FB1V55
FB_512_SAMSUNG	VRAM4, VRAM_512_SAMSUNG, FB1V35
FB_512_HYNIX	VRAM4, VRAM_512_HYNIX, FB1V35

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Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEEE:DCJ7]	CRITICAL	EEEE_DCJ7
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEEE:DCJ8]	CRITICAL	EEEE_DCJ8
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEEE:DCJ9]	CRITICAL	EEEE_DCJ9
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEEE:DCJC]	CRITICAL	EEEE_DCJC
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEEE:DCJD]	CRITICAL	EEEE_DCJD
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEEE:DCJF]	CRITICAL	EEEE_DCJF

B

B

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3848	1	ARD, SLBPE, PRQ, 2.66G, 35W, C2, 3M, BGA	U1000	CRITICAL	CPU_2_66GHZ
337S3847	1	ARD, SLBPF, PRQ, 2.53G, 35W, C2, 3M, BGA	U1000	CRITICAL	CPU_2_53GHZ
337S3846	1	ARD, SLBNA, PRQ, 2.4G, 35W, C2, 4M, BGA	U1000	CRITICAL	CPU_2_4GHZ
337S3849	1	IC, PCH, IBEX PEAK-M, SLG2S, PRQ, B3, BGA	U1800	CRITICAL	
337S3839	1	IC, GPU, NV GT216 LP++, 969BGA, 40NM, A03	U8000	CRITICAL	
343S0493	1	IC, ASIC, BCM5764M, ENET CONTROLLER, 8x8, 64 QFN	U3900	CRITICAL	BCM5764M
341S2731	1	IC, 1MBIT, SPI FLASH, K17/K18	U3990	CRITICAL	
338S0753	1	IC, FW643-E2, 1394B PHY/OHCI LINK/PCI-E, 12	U4100	CRITICAL	
338S0563	1	IC, SMC, HS8/2117, 9MMX9MM, TLP	U4900	CRITICAL	SMC_BLANK
341T0233	1	IC, SMC, K18	U4900	CRITICAL	SMC_PROG
335S0610	1	IC, FLASH, SPI, 32MBIT, 3.3V, 86MHZ, 8-SOP	U6100	CRITICAL	BOOTROM_BLANK
341S2562	1	IC, EFI ROM, DEVELOPMENT, K18	U6100	CRITICAL	BOOTROM_PROG
341S2384	1	IR, ENCORE II, CY7C63833-LFXC	U4800	CRITICAL	
341S2616	1	IC, PSOC +W/USB, 56PIN, MLF, K18	U5701	CRITICAL	TPAD_PROG
336S0025	1	IC, XP2-5, HF, CPLD, BLANK	U9600	CRITICAL	GMUX_5K_BLANK
341S2566	1	IC, CPLD, LATTICE, 132CSBGA, K18	U9600	CRITICAL	GMUX_PROG
333S0507	4	IC, SGRAM, GDDR3, 16MX32, 1000MHZ, 136 FBGA	U8400, U8450, U8500, U8550	CRITICAL	VRAM_256_SAMSUNG
333S0483	4	IC, SDRAM, GDDR3, 16MX32, 900MHZ, 136 FBGA	U8400, U8450, U8500, U8550	CRITICAL	VRAM_256_HYNIX
333S0533	4	IC, SGRAM, GDDR3, 32MX32, 1000MHZ, 136 FBGA	U8400, U8450, U8500, U8550	CRITICAL	VRAM_512_SAMSUNG
333S0535	4	IC, SDRAM, GDDR3, 32MX32, 1000MHZ, 136 FBGA	U8400, U8450, U8500, U8550	CRITICAL	VRAM_512_HYNIX

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Development BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-1404	1	K18 MLB DEVELOPMENT	DEVEL	CRITICAL	DEVEL_BOM


Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0603	138S0602		ALL	Murata alt to Samsung
157S0058	157S0055		ALL	Delta alt to TDK Magnetics
152S0896	152S0518		ALL	MAG LAYERS ALT TO CYWRC
155S0457	155S0329		ALL	MAG LAYERS ALT TO MURATA
333S0506	333S0535		ALL	Hynix 900M alt to 1000M
516S0805	516S0806		ALL	Molex alt to Foxconn
152S1102	152S1088		ALL	Mag layer alt to Vishay
353S2805	353S2603		ALL	Fairchild wafer option
333S0542	333S0507		ALL	Samsung 1 die alt to H
128S0264	128S0257		ALL	Sanyo alt to Kemet
128S0303	128S0282		ALL	Panasonic alt to Sanyo
337S3808	337S3839		ALL	A02 alt to A03 GPU
128S0305	128S0294		ALL	6.3V alt to 11V Sanyo

SYNC MASTER=K17 REF

SYNC DATE=05/28/2009

BOM Configuration

 Apple Inc.

DRAWING NUMBER<SCH_NUM>D

REVISION<E4LABEL>

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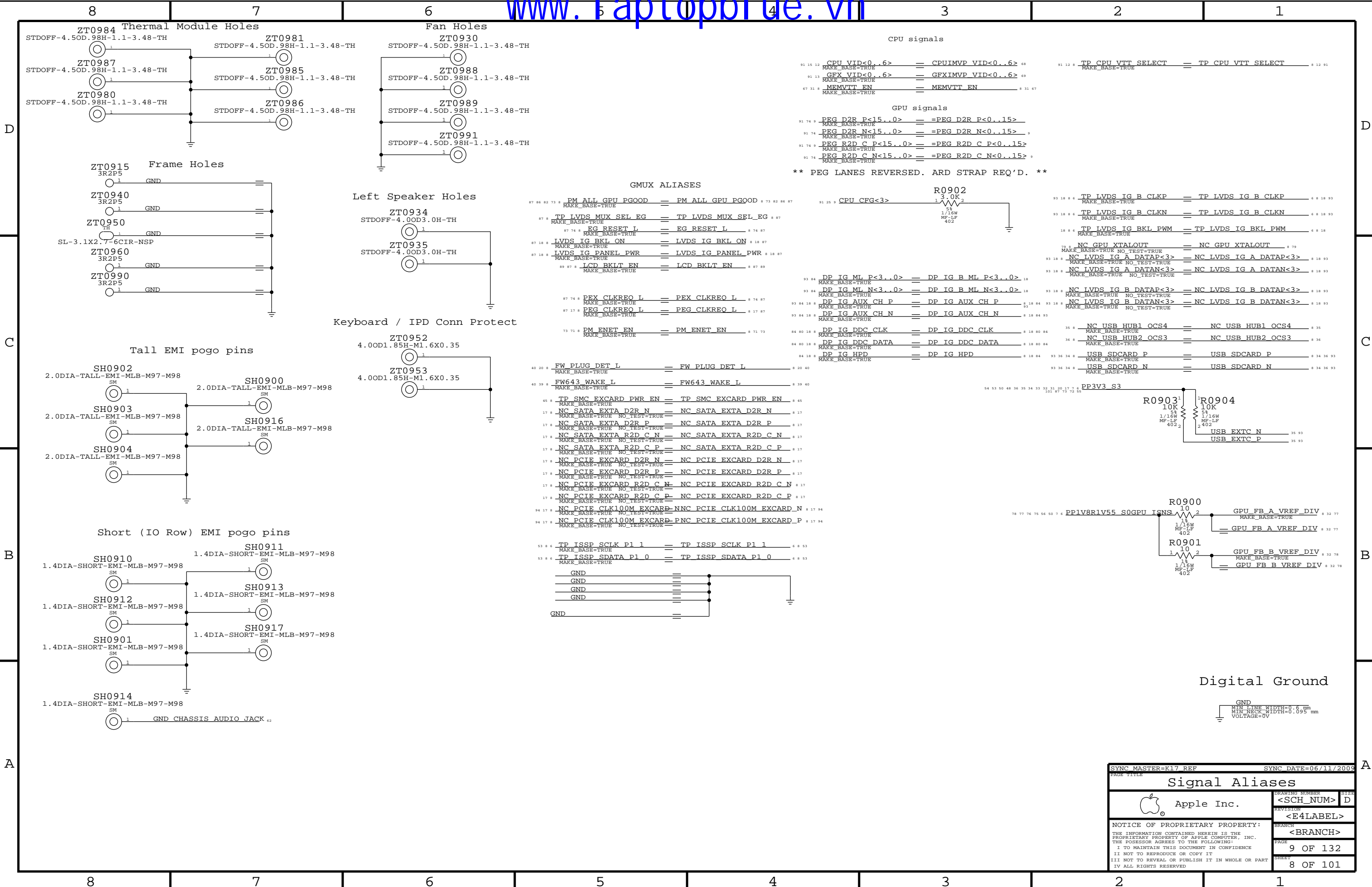
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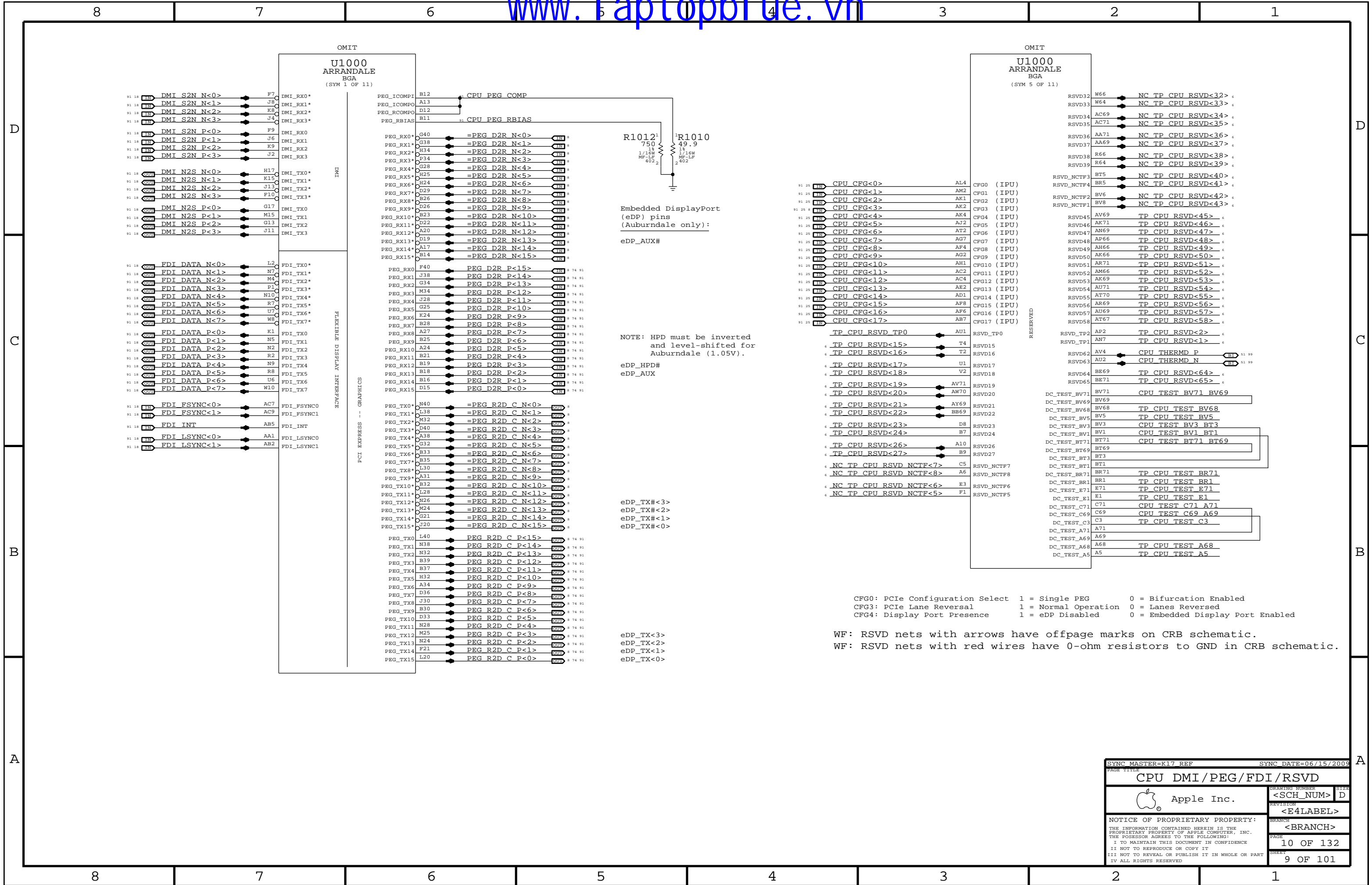
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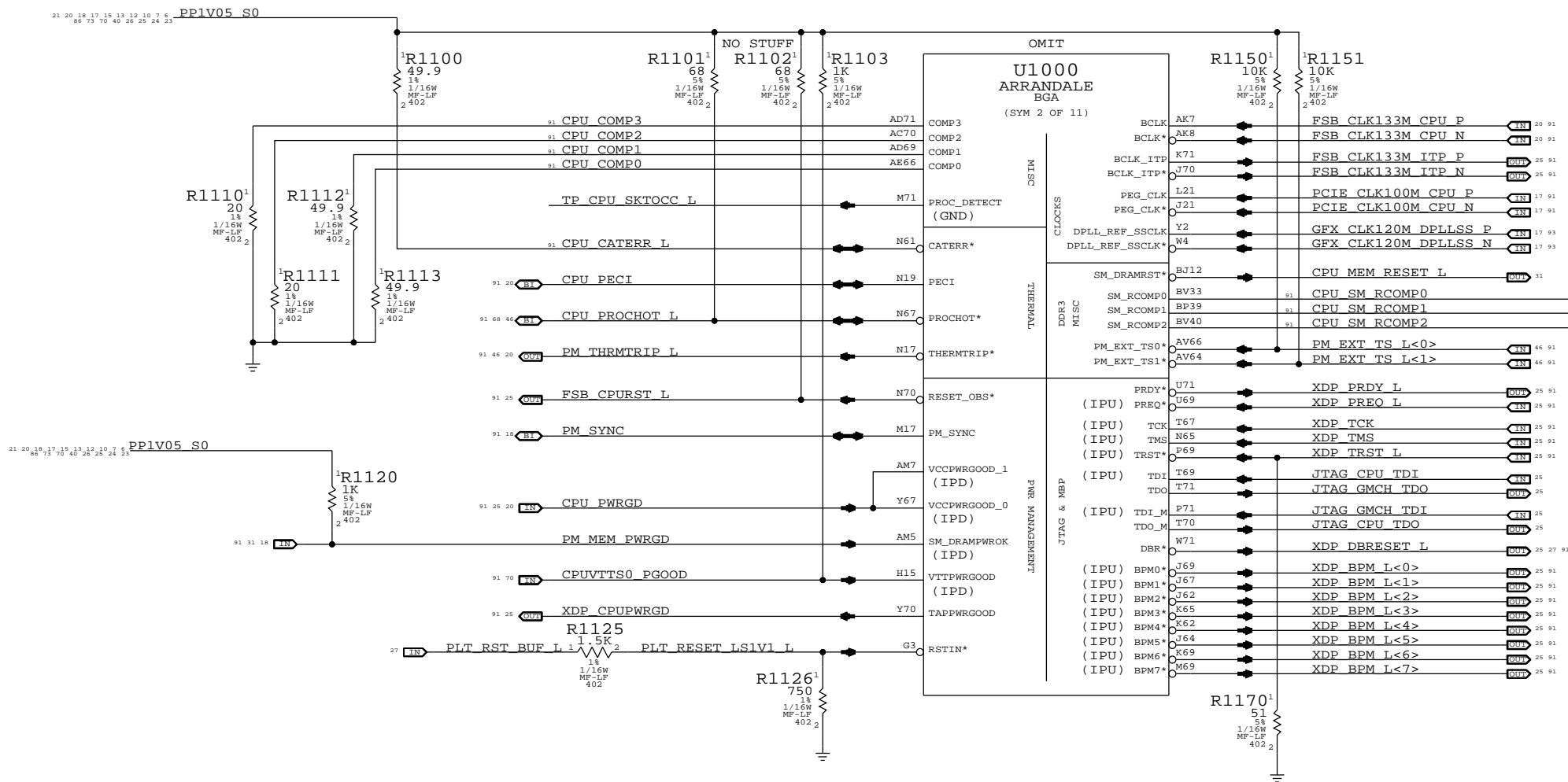
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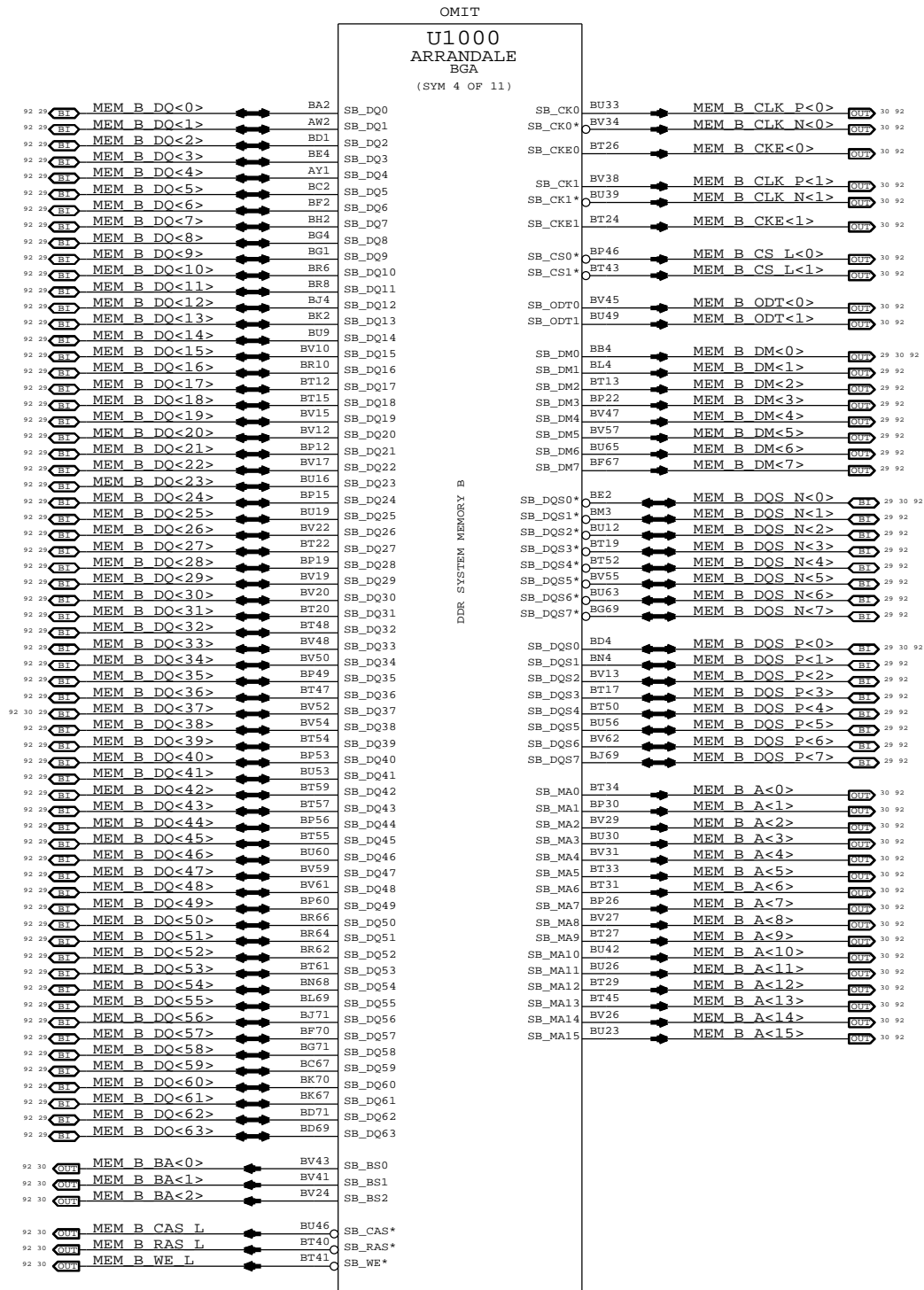
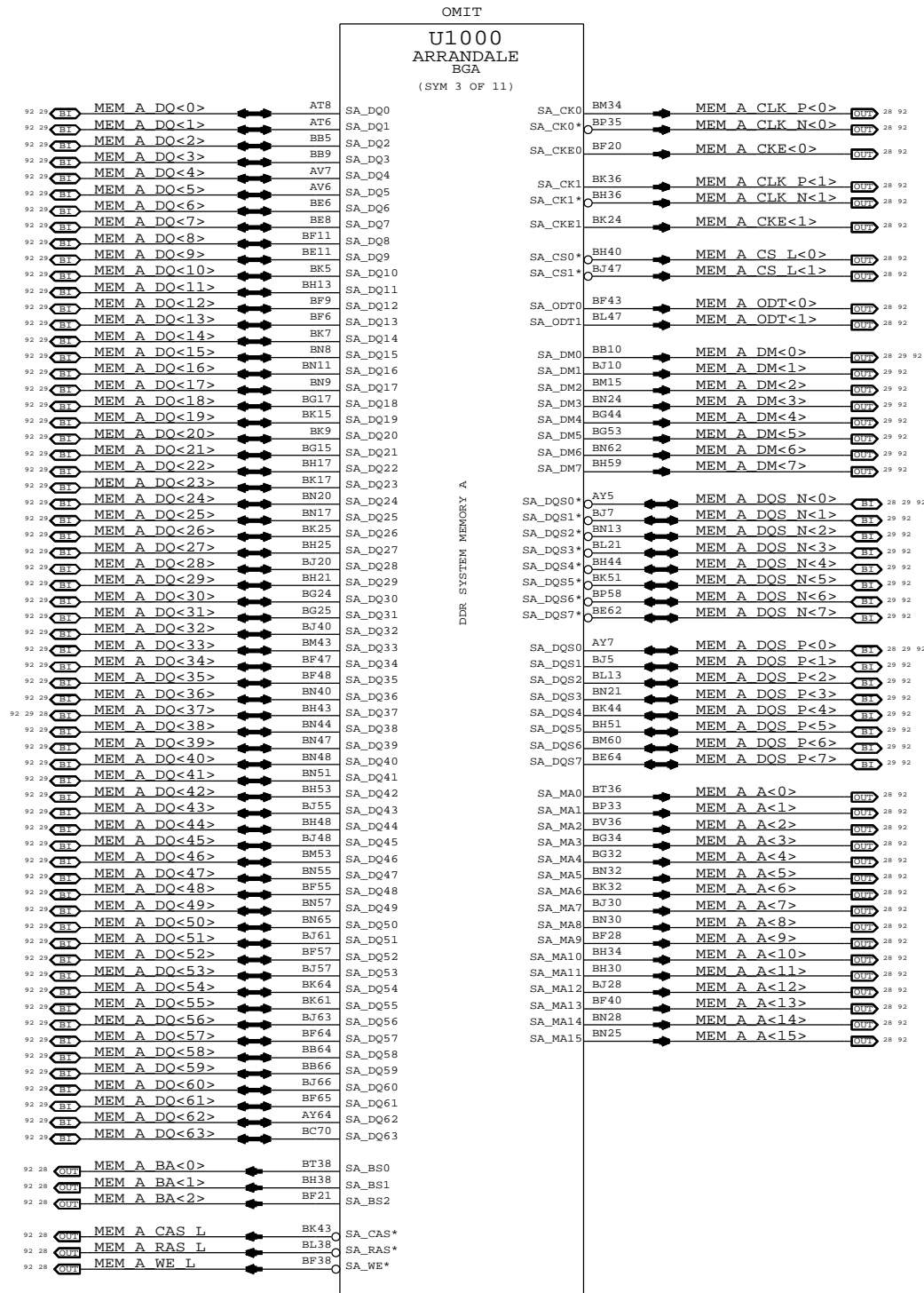
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16 7 PPVCORE S0 CPU VCAP1

NOTE: VCAP1 is sourced by CPU
Do not connect to power supply,
but provide bypass caps on PCB.

POWER

CPU CORE SUPPLY

PPVCORE S0 CPU 6 7 12 15 49 68

21 20 18 17 15 13 12 10 7 6 PP1V05 S0

PLACE_NEAR=U1000.F64:25.4MM

PLACE_NEAR=U1000.F63:25.4MM

```

91 68 15 CPU_PST_L
91 15 8 CPU_VID<0>
91 15 8 CPU_VID<1>
91 15 8 CPU_VID<2>
91 15 8 CPU_VID<3>
91 15 8 CPU_VID<4>
91 15 8 CPU_VID<5>
91 15 8 CPU_VID<6>
91 8 TP_CPU_VTT_SELECT
91 68 15 PM_DPRSLEVR
VTT_SELECT: 1 = 1.05V, 0 = 1.

```

91 68 50 CPUIMVP IMON

25.4MM CPU VCCSENSE P

CPU VCCSENSE N

CPU VTTSENSE P

CPU VTTSENSE N

11 16 7 6 PP1V8_S0

16 PP1V5 S3 CPU VCCDDR CLK
MIN_LINE_WIDTH=0.4mm
MIN_NECK_WIDTH=0.2mm
VOLTAGE=1.5V


OMIT

U1000
ARRANDALE
BGA
(SYM 6 OF 11)

```

PP1V05 S0
Arrandale: 1.05V
Clarksfield: 1.1V
(Controlled by VTT_SELECT pin)

```

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CPU Power (1 of 2)			
 Apple Inc.		DRAWING NUMBER <SCH_NUM>	
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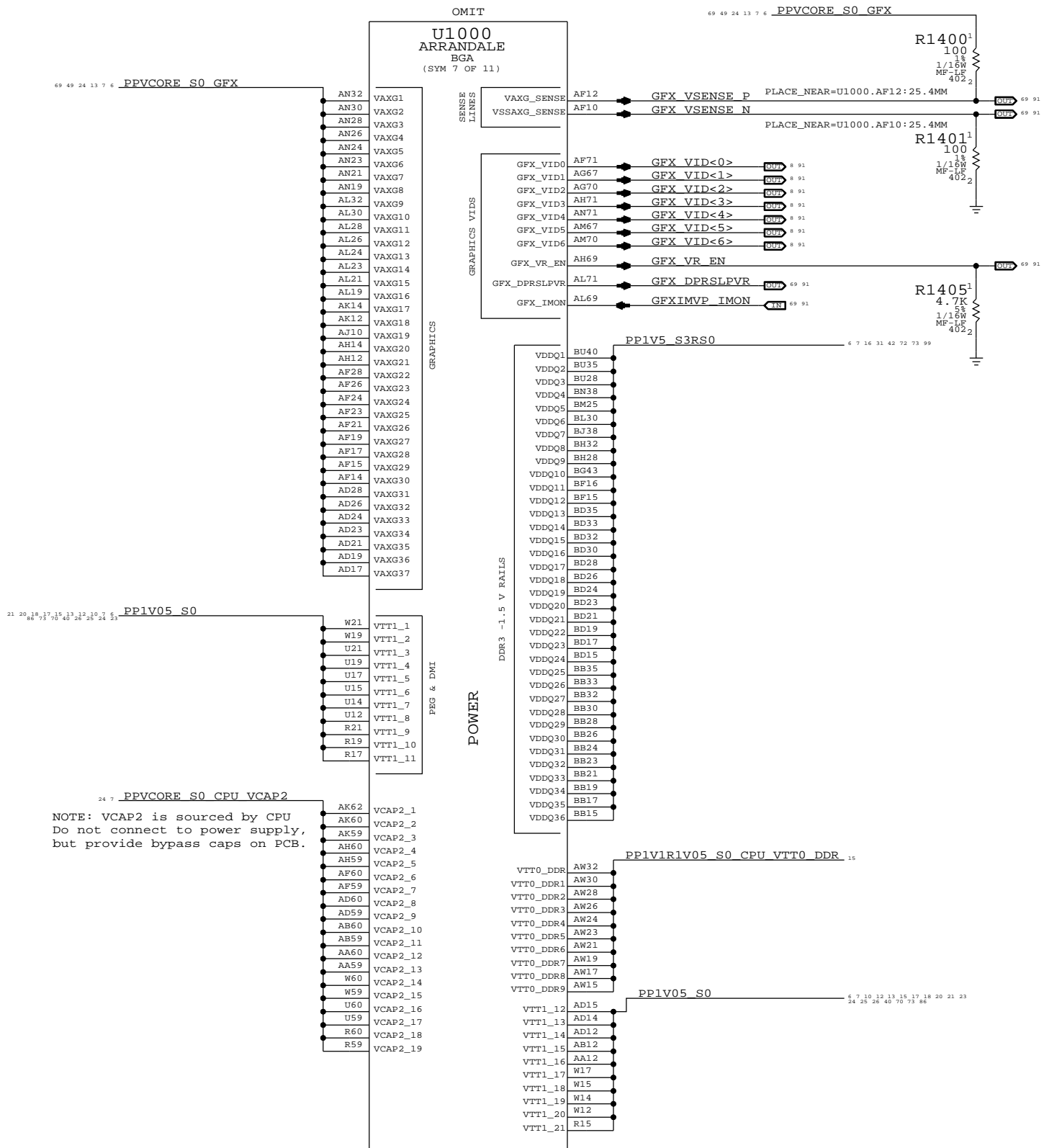
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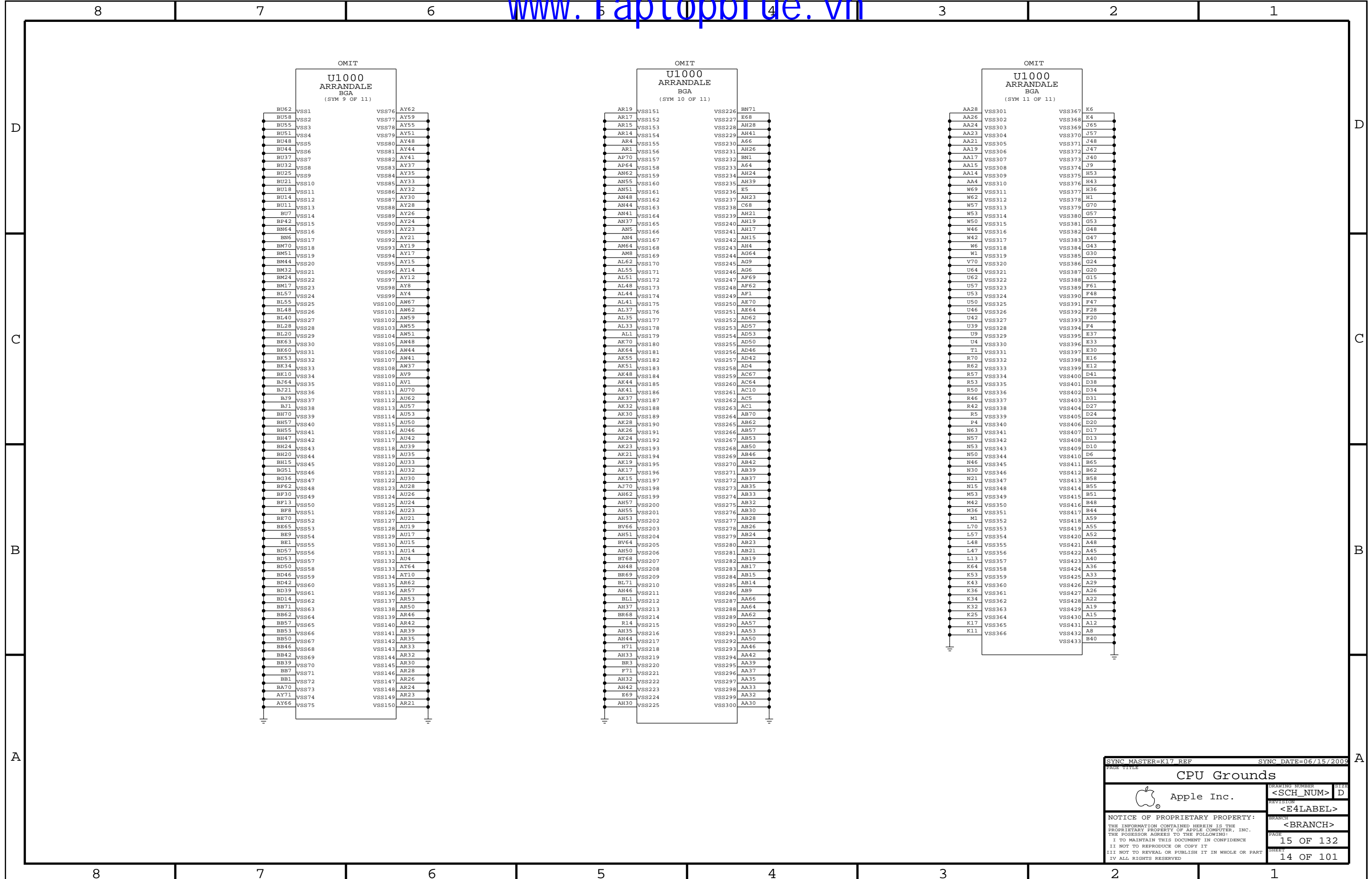
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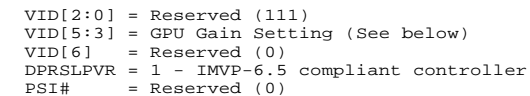


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Intel recommends all option straps should be provided in layout

63 PP1V05 S0



NOTE: BOM Configurations should not call out CPUPOCnU/D BOMOPTIONS directly.
Instead call out appropriate BOM GROUP defined in tables above.

PP1V1R1V05 S0 CPU VTT0 DDR 1
MIN LINE WIDTH=0.4 mm
MIN NECK WIDTH=0.2 mm
VOLTAGE=1.1V

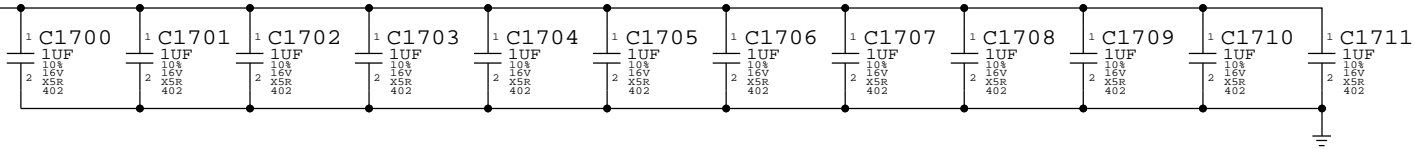
VCAP0 (CPU BSC Package) DECOUPLING

12x 1uF 0402

PLACEMENT_NOTE (C1700-C1711):

Place on bottom side of U1000.

12 7 PPVCORE_S0_CPU_VCAP0



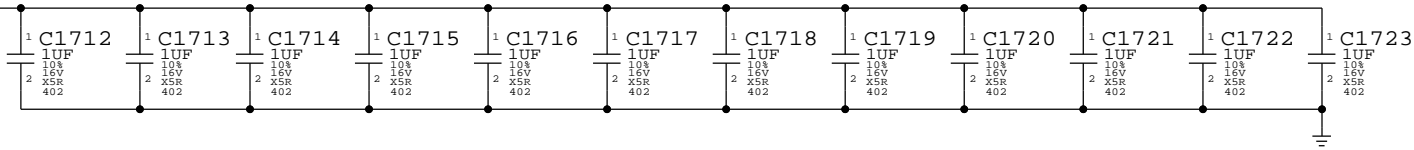
VCAP1 (CPU BSC Package) DECOUPLING

12x 1uF 0402

PLACEMENT_NOTE (C1712-C1723):

Place on bottom side of U1000.

12 7 PPVCORE_S0_CPU_VCAP1

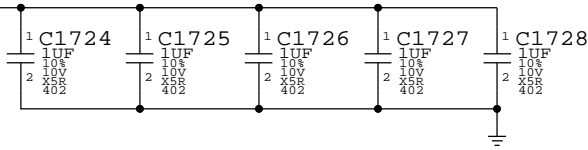


Memory (CPU VCCDDR) DECOUPLING

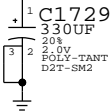
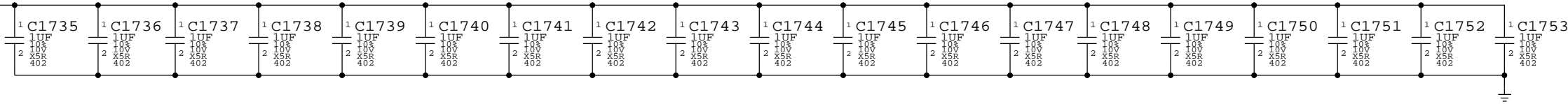
5x 1uF 0402

NOTE: 3x 330uF 6 mOhm caps to be shared between CPU and SO-DIMMs. DG recommends 2x 22uF at SO_DIMM not provided. Decoupling caps at SO-DIMMs on CSA 29 and CSA 31.

42 31 16 13 7 6 PP1V5_S3RS0



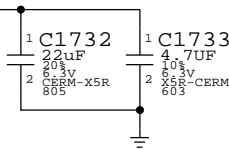
NOTE: 19x 1uF 0402 caps per Apple SI for CMD and CNTRL lines.



PLL (CPU VCCSFR) DECOUPLING

1x 22uF 0805, 1x 4.7uF 0603

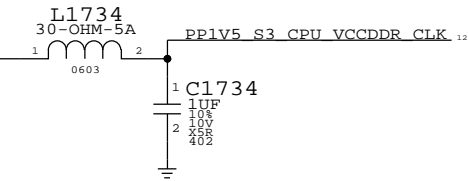
24 23 21 12 7 6 PP1V8_S0




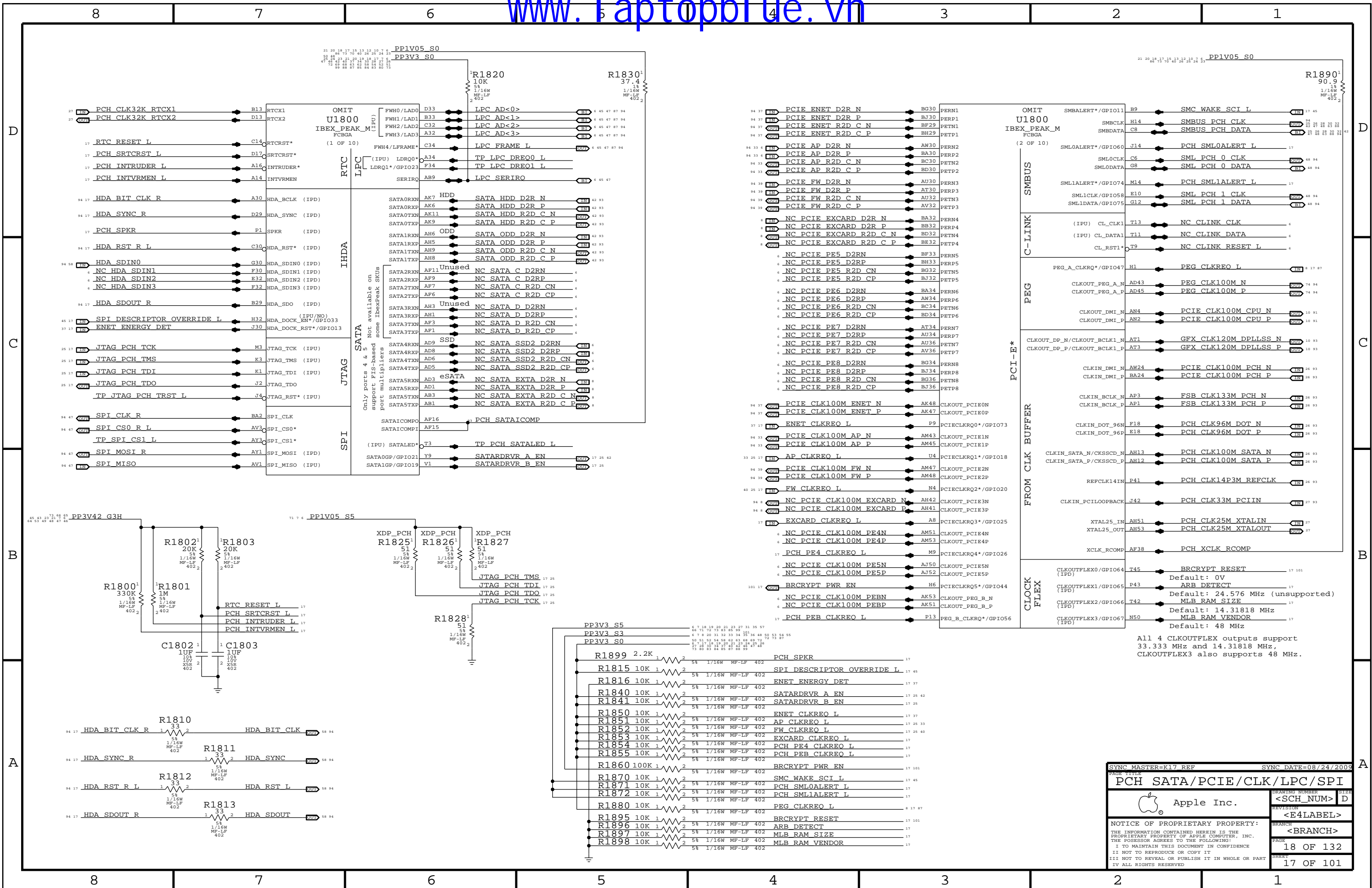
DDR Clock (CPU VDDQ_CK) DECOUPLING

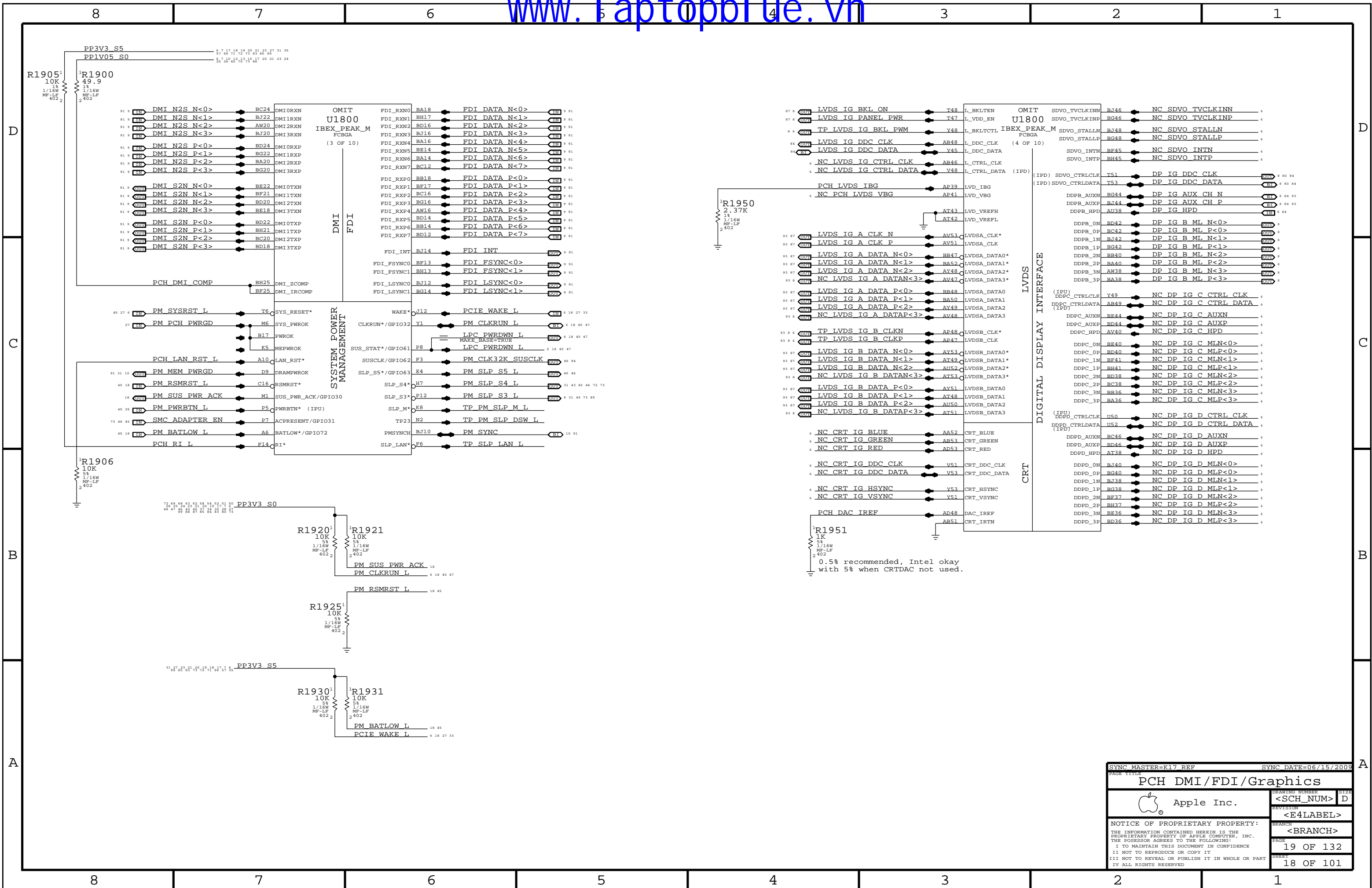
1x 1uF 0402

42 31 16 13 7 6 PP1V5_S3RS0



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CPU Non-GFX Decoupling (2 of 2)				
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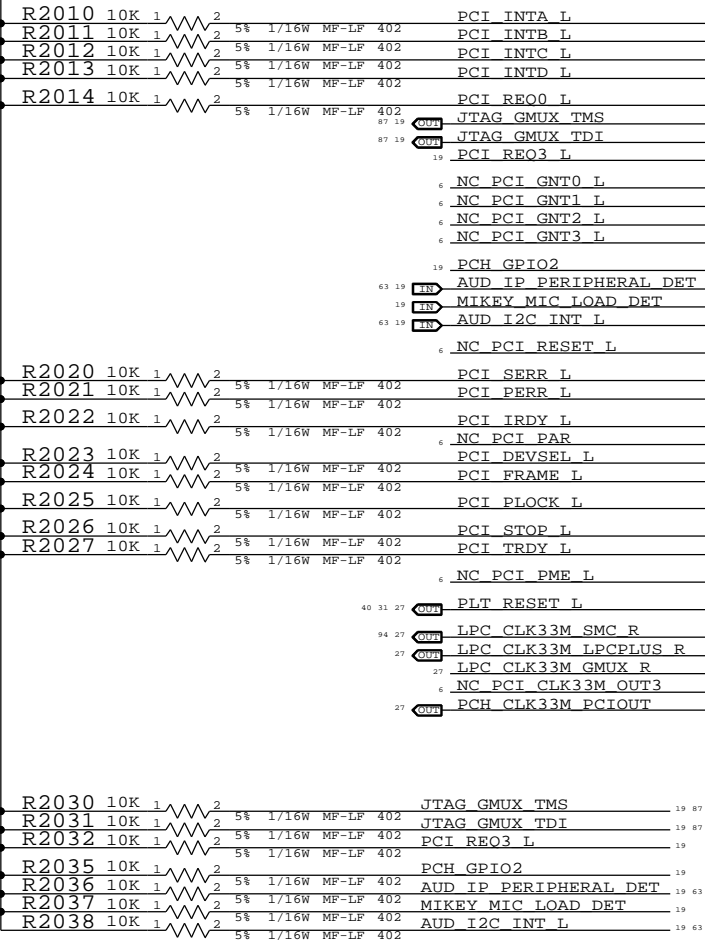
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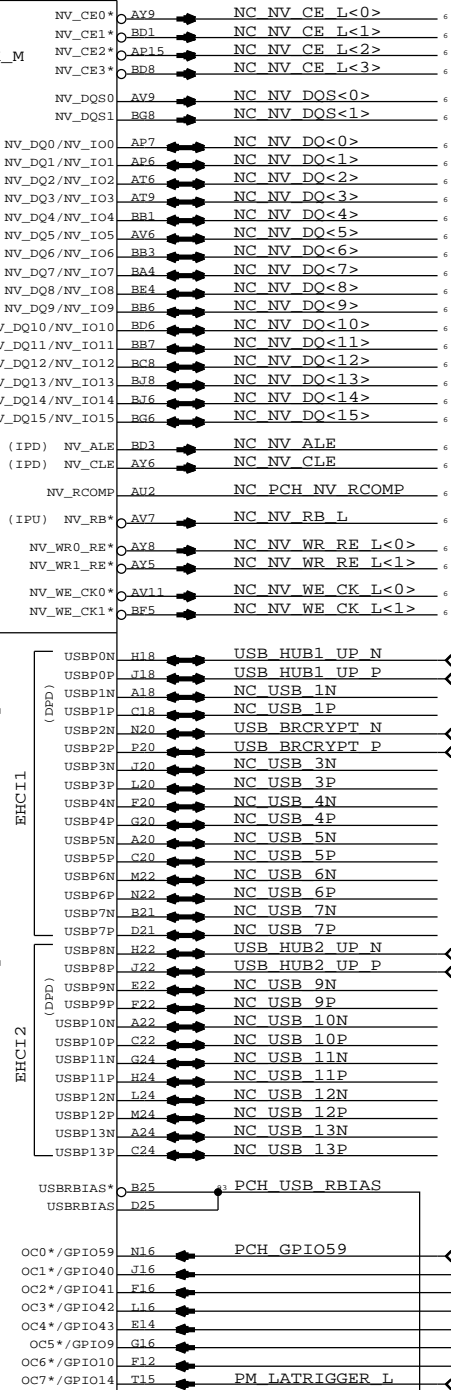
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OMIT
U1800
IBEX PEAK_M
FCBGA
(5 OF 10)

NVRAM

PCI

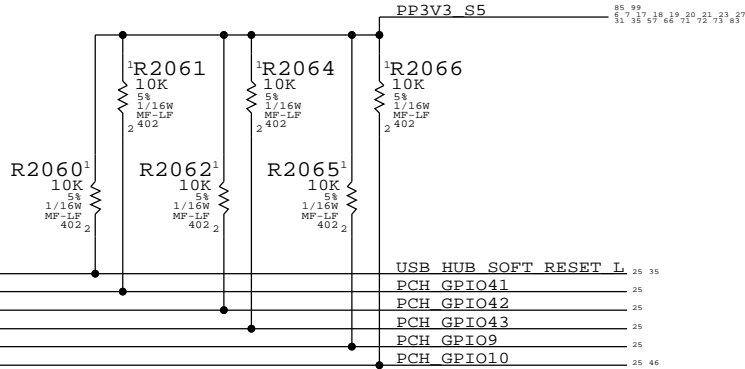
NOTE: Internal pull-downs on all USB pins



External Hub 1

T57

External Hub 2



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Apple Inc.		DRAWING NUMBER	
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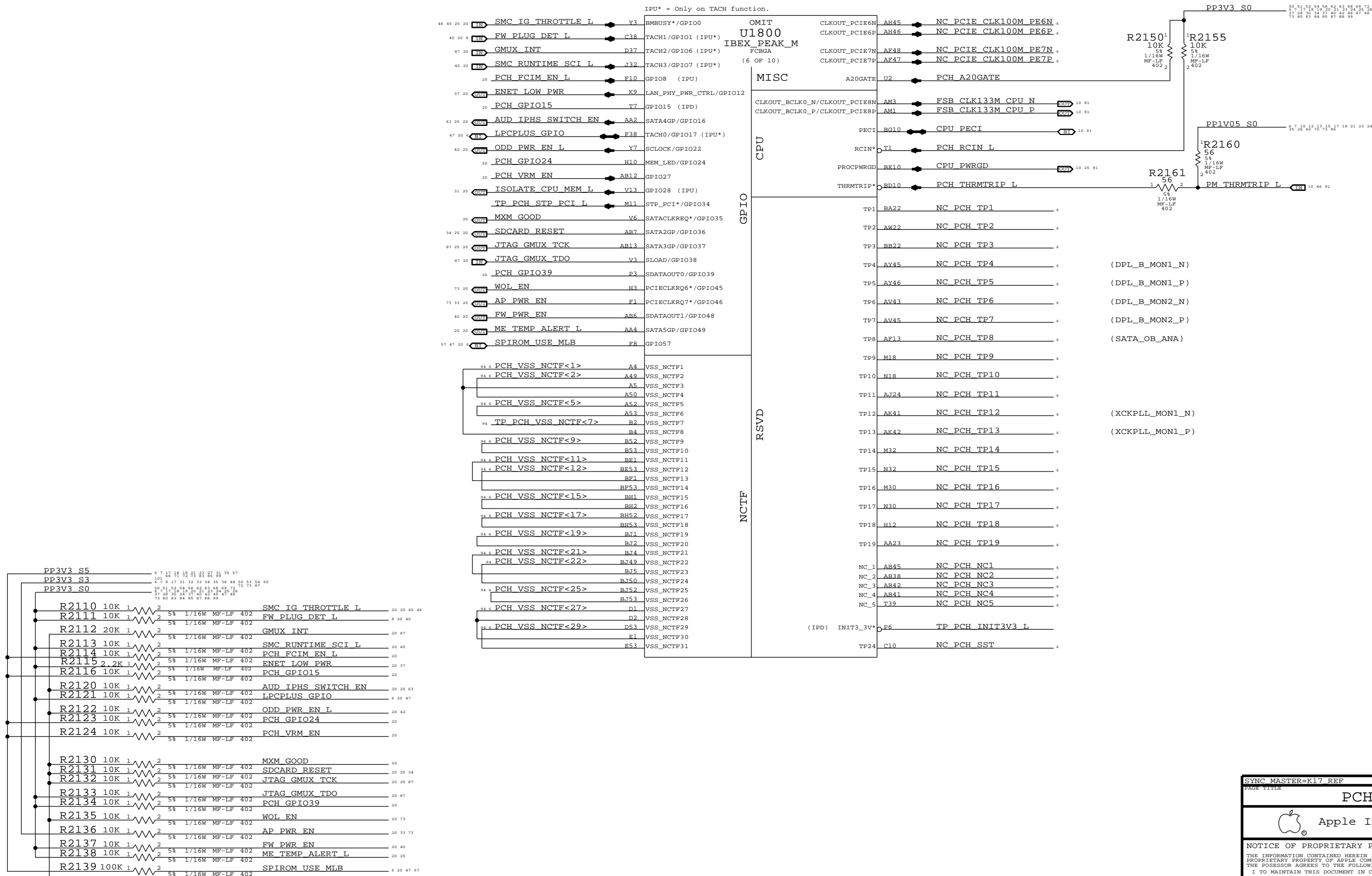
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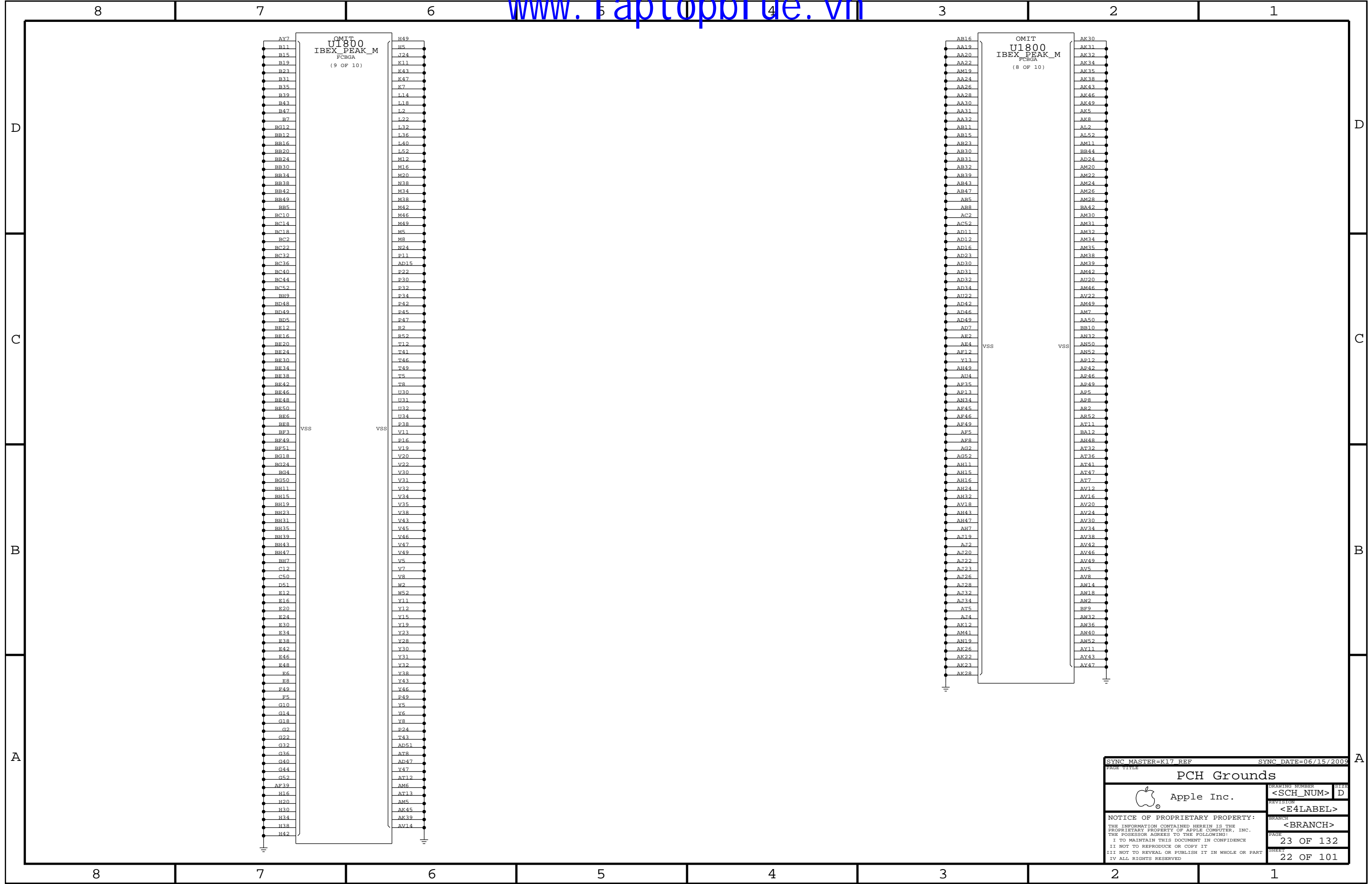
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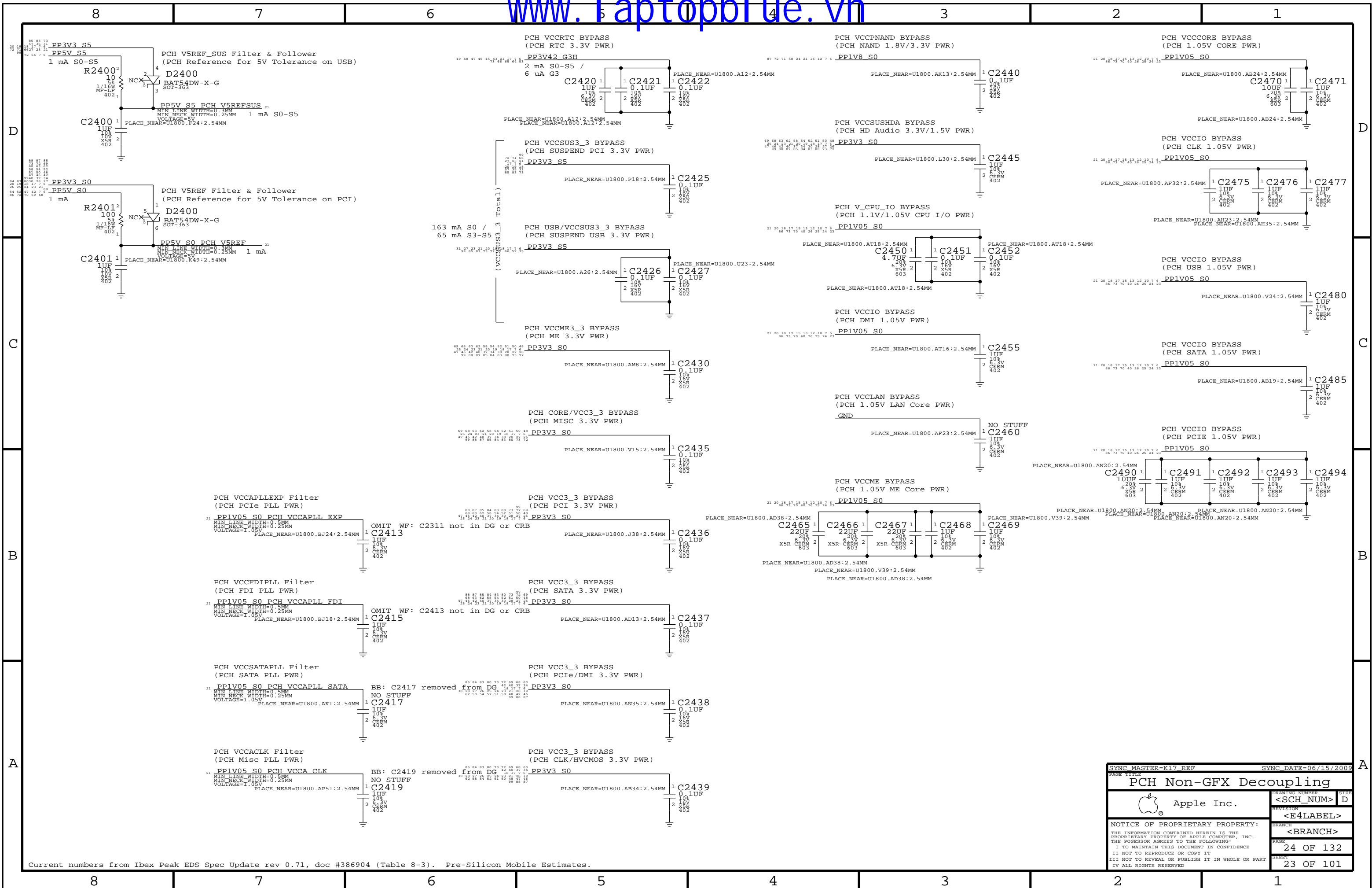
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SYNC DATE=06/15/2009

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		SHEET	22 OF 101



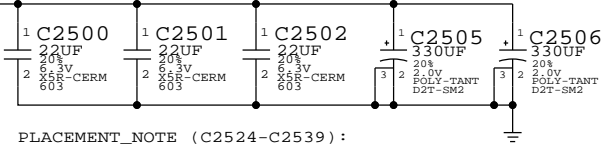
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GFX (CPU VCCAXG) DECOUPLING

3x 330uF 6 mOhm (2 stuffed), 3x 22uF 0603, 16x 1uF 0402

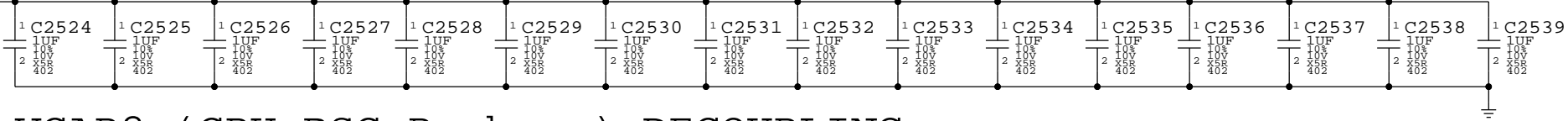
PLACEMENT_NOTE (C2500-C2506):

Place on bottom side of U1000.



PLACEMENT_NOTE (C2524-C2539):

Place on bottom side of U1000.

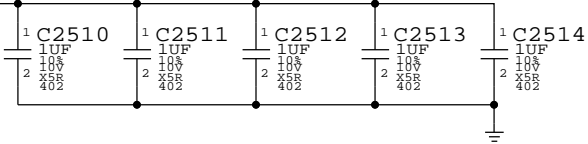


VCAP2 (CPU BSC Package) DECOUPLING

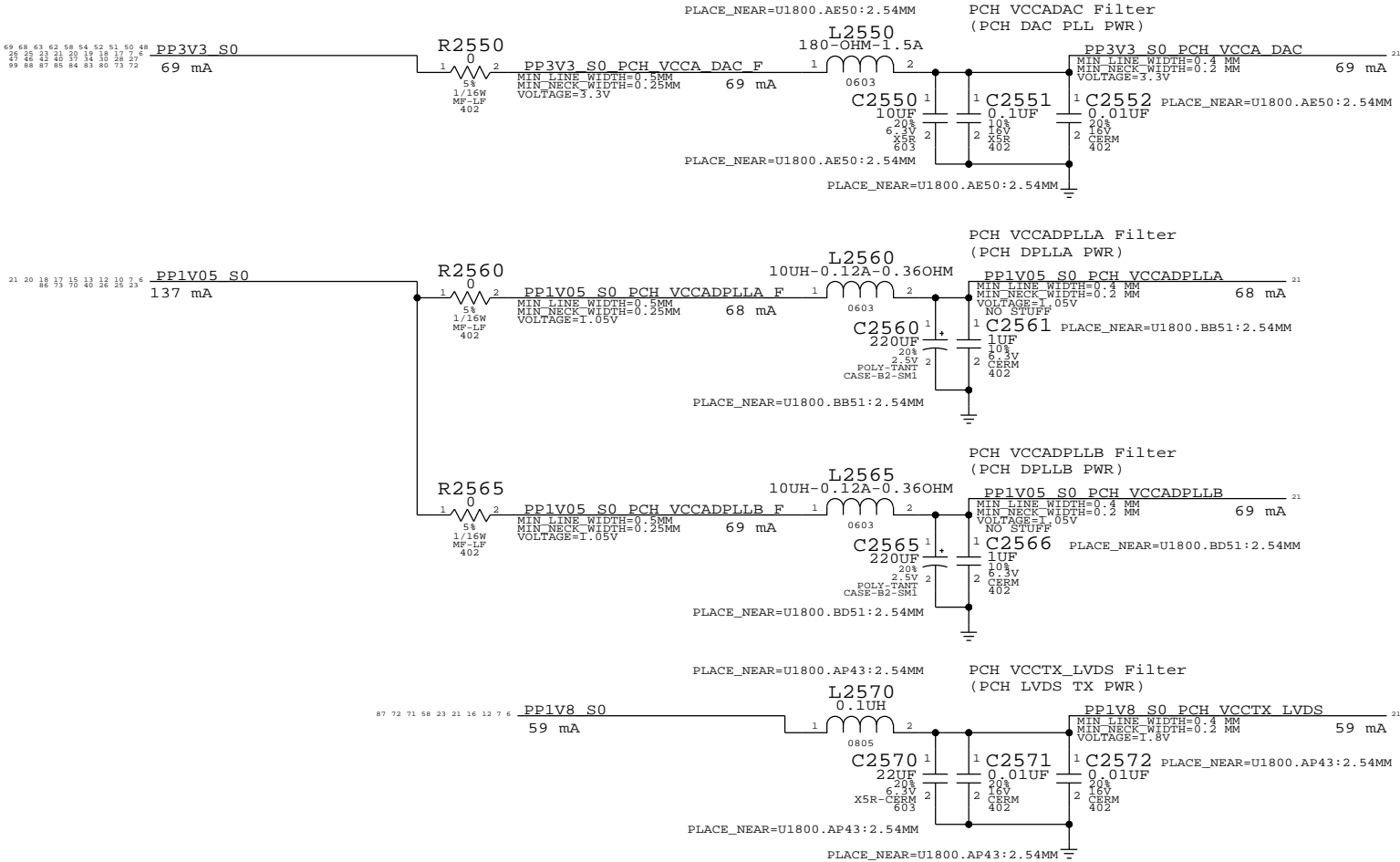
5x 1uF 0402

PLACEMENT_NOTE (C2510-C2514):

Place on bottom side of U1000.




Design recommendations from Calpella Small Form Factor Design Guide Rev 1.5 (doc #407364) table 2-34 and Calpella Small Form F actor Schematic Check List Rev 1.1 (doc #395914) table 3.26.

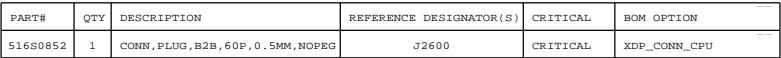


Design recommendations from Calpella Design Guide Rev 1.5 (doc #398905) Section 3.25.3 tables 161 and 162.

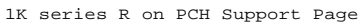
Current numbers from Ibox Peak EDS Spec Update rev 0.71, doc #386904 (Table 8-3). Pre-Silicon Mobile Estimates.


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Calpella Processor mini XDP



Calpella PCH mini XDP



SYNC MASTER=K1-7 REF		SYNC DATE=06/15/2009	
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eXtended Debug Port (XDP)		D	
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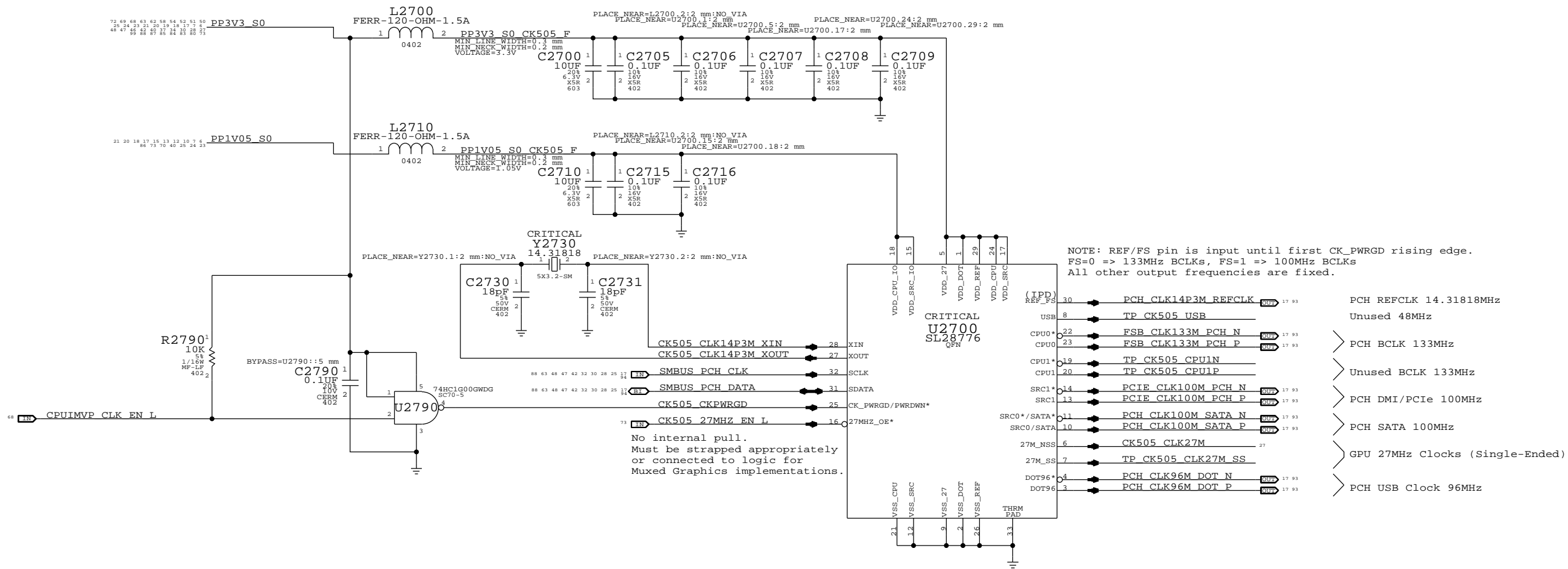
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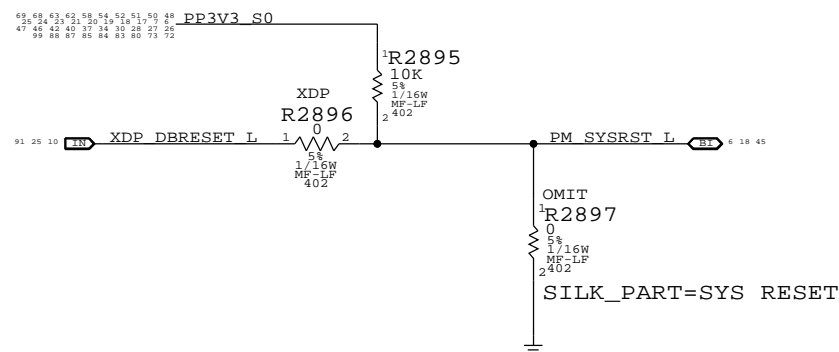
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SYNCH MASTER=K17 REF

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Chipset Support



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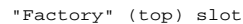
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DDR3 SO-DIMM Connector A			
 Apple Inc.		DRAWING NUMBER <SCH_NUM>	
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8	7	6	5	4	3	2	1
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The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.

WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.

WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

$P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L$

$MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L$

$MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L$

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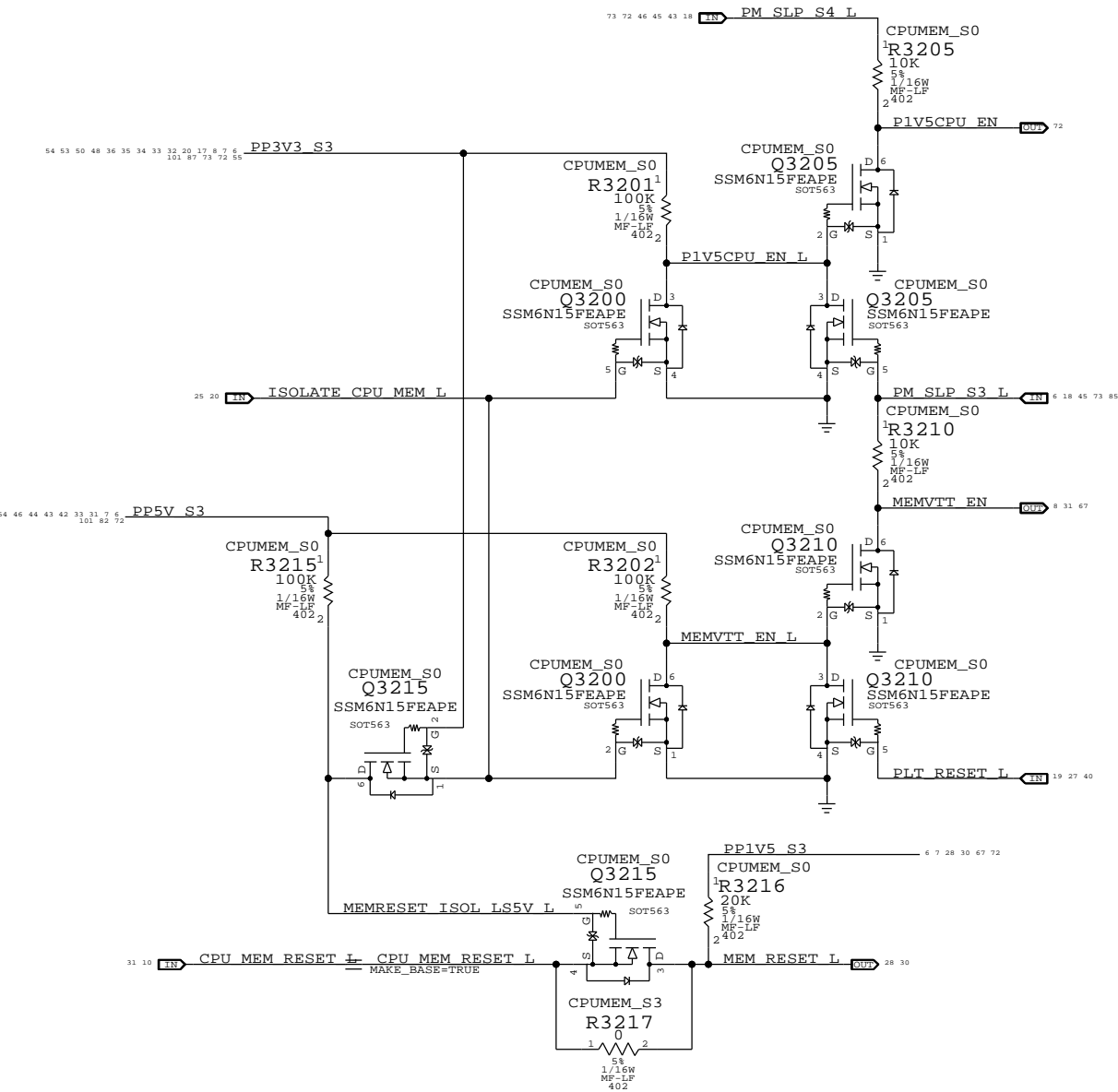
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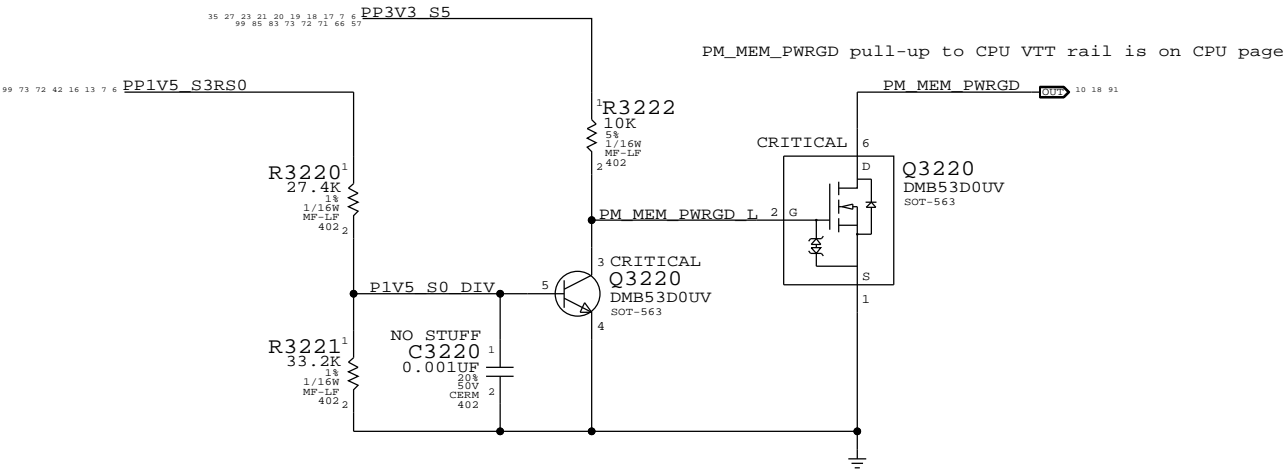
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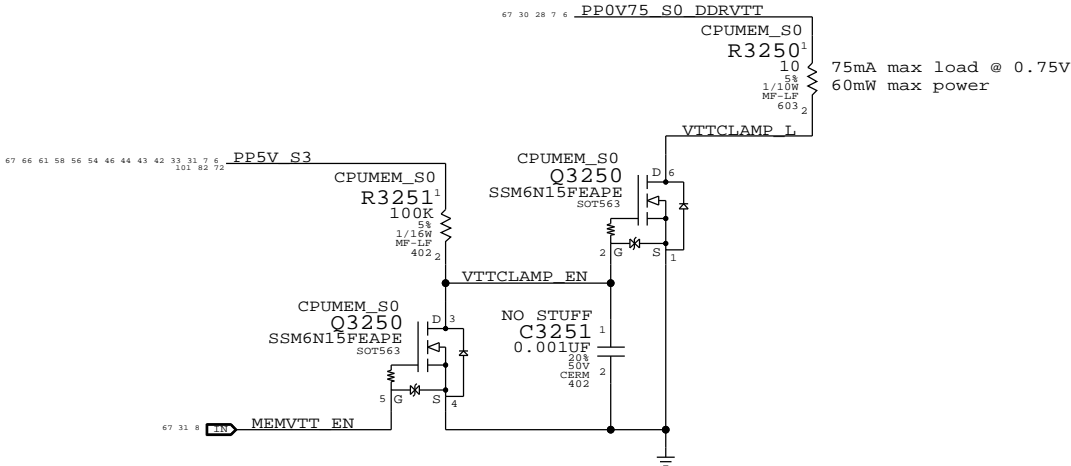


1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1
2	0	0	1	1	1	1	0	1
3	0	0	0	1	X	1	0	0
4	0	0	1	1	X	1	0	1
5	0	1	1	1	0 (*)	1	1	1
6	0	1	1	1	1	1	1	1
to	1	1	1	1	1	CPU_MEM_RESET_L	1	1
S0	7							

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC MASTER=K17 REF

SYNC DATE=06/15/2009

CPU Memory S3 Support

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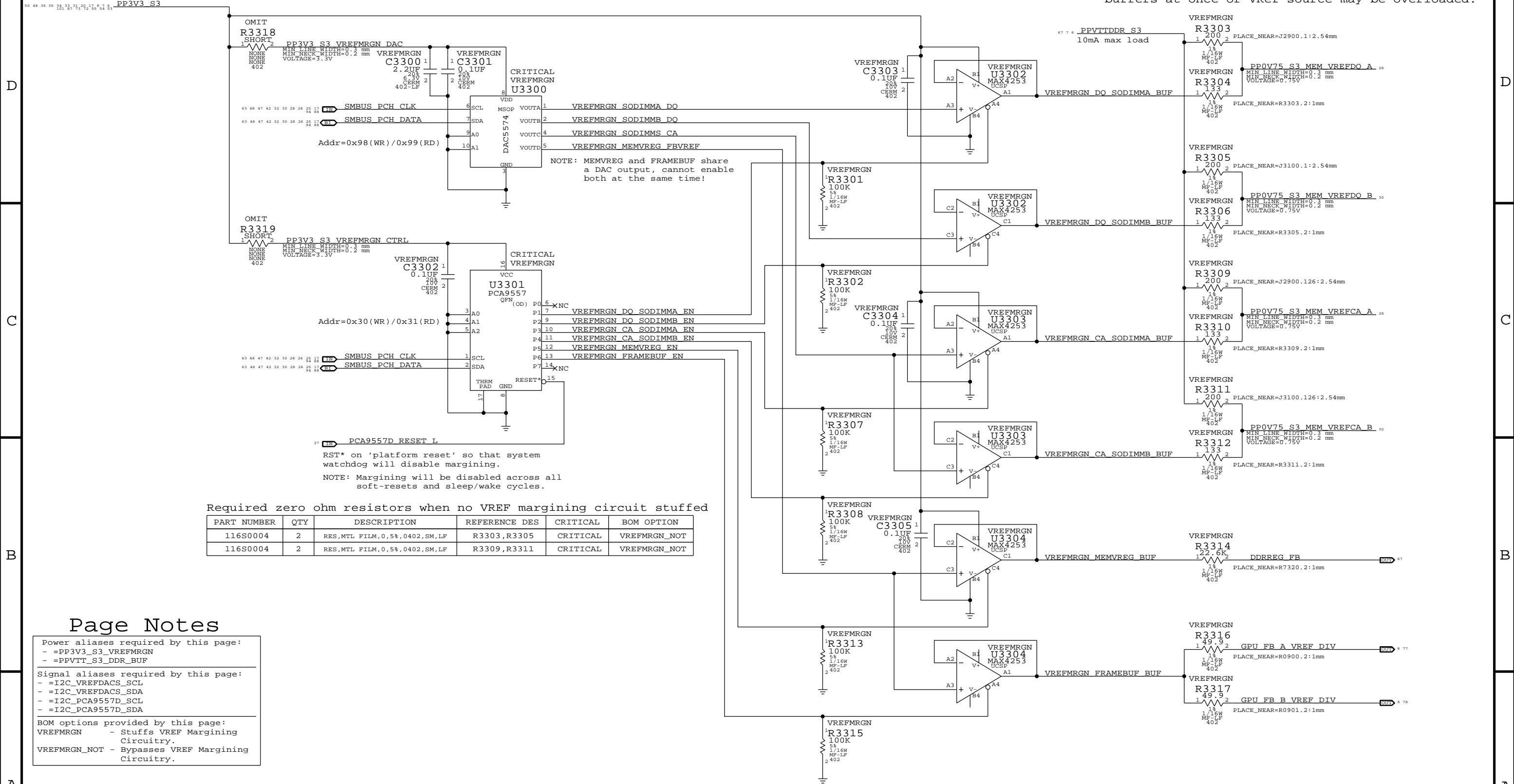
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NOTE: Must not enable more than two SO-DIMM margining buffers at once or Vref source may be overloaded.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3303,R3305	CRITICAL	VREFMRGN_NOT
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3309,R3311	CRITICAL	VREFMRGN_NOT

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN - Stuffs VREF Margining Circuitry.
VREFMRGN_NOT - Bypasses VREF Margining Circuitry.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% Vref)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value			0.75V (DAC: 0x3A)		1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:			0.300V - 1.200V (+/- 450mV)		1.998V - 1.002V (+/- 498mV)	1.056V - 1.442V (+/- 180mV)
DAC range:			0.000V - 1.501V (0x00 - 0x74)		0.000V - 1.501V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
Vref current:			+3.4mA - -3.4mA (- = sourced)		+33uA - -33uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:			7.69mV / step @ output		8.59mV / step @ output	1.51mV / step @ output

SYNC MASTER=K17 REF

SYNC DATE=06/15/2009

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FSB/DDR3/FRAMEBUF Vref Margining


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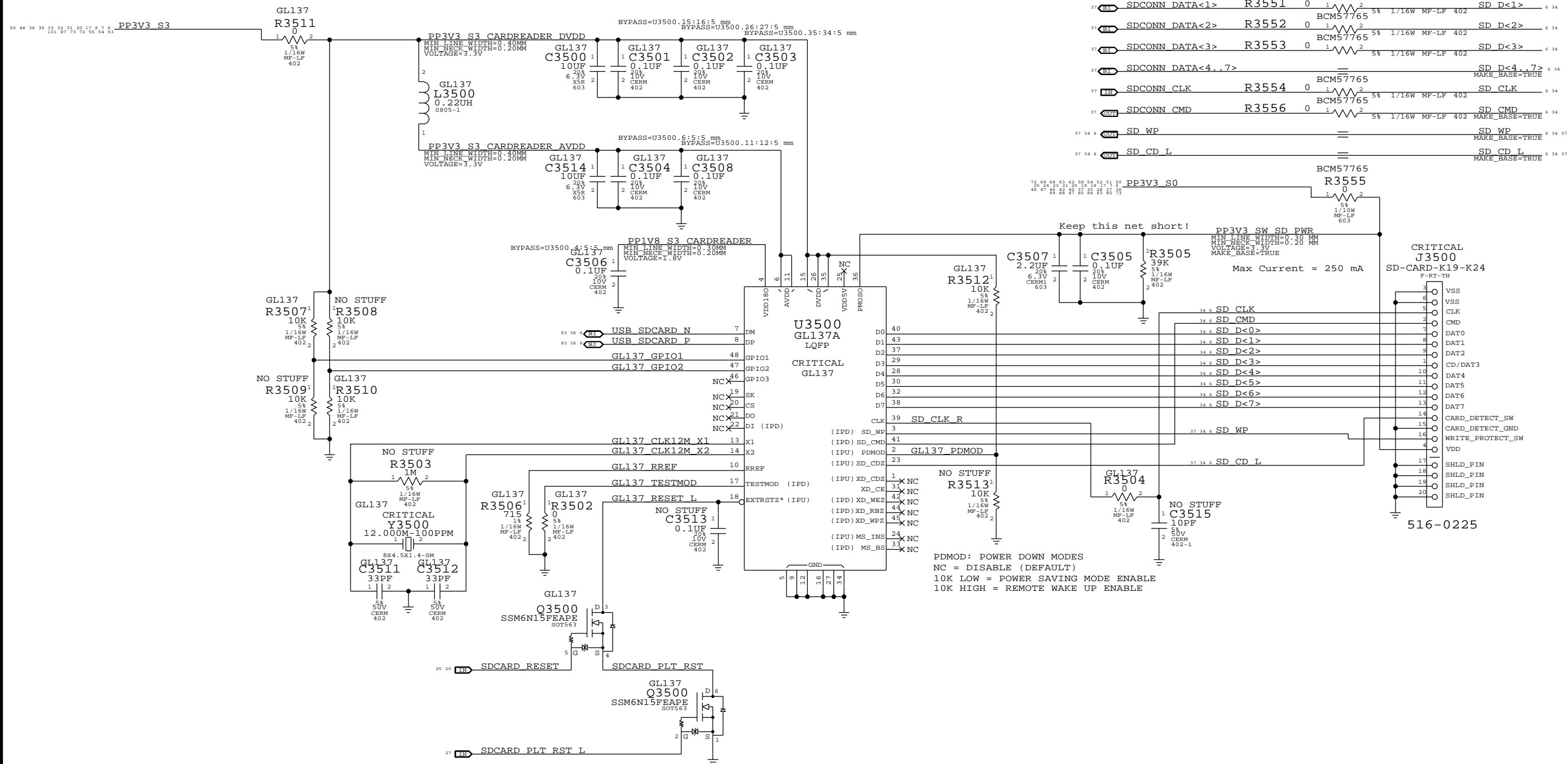
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Caesar IV Support



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PRG# 1111			
SecureDigital Card Reader			
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USB HUB-1

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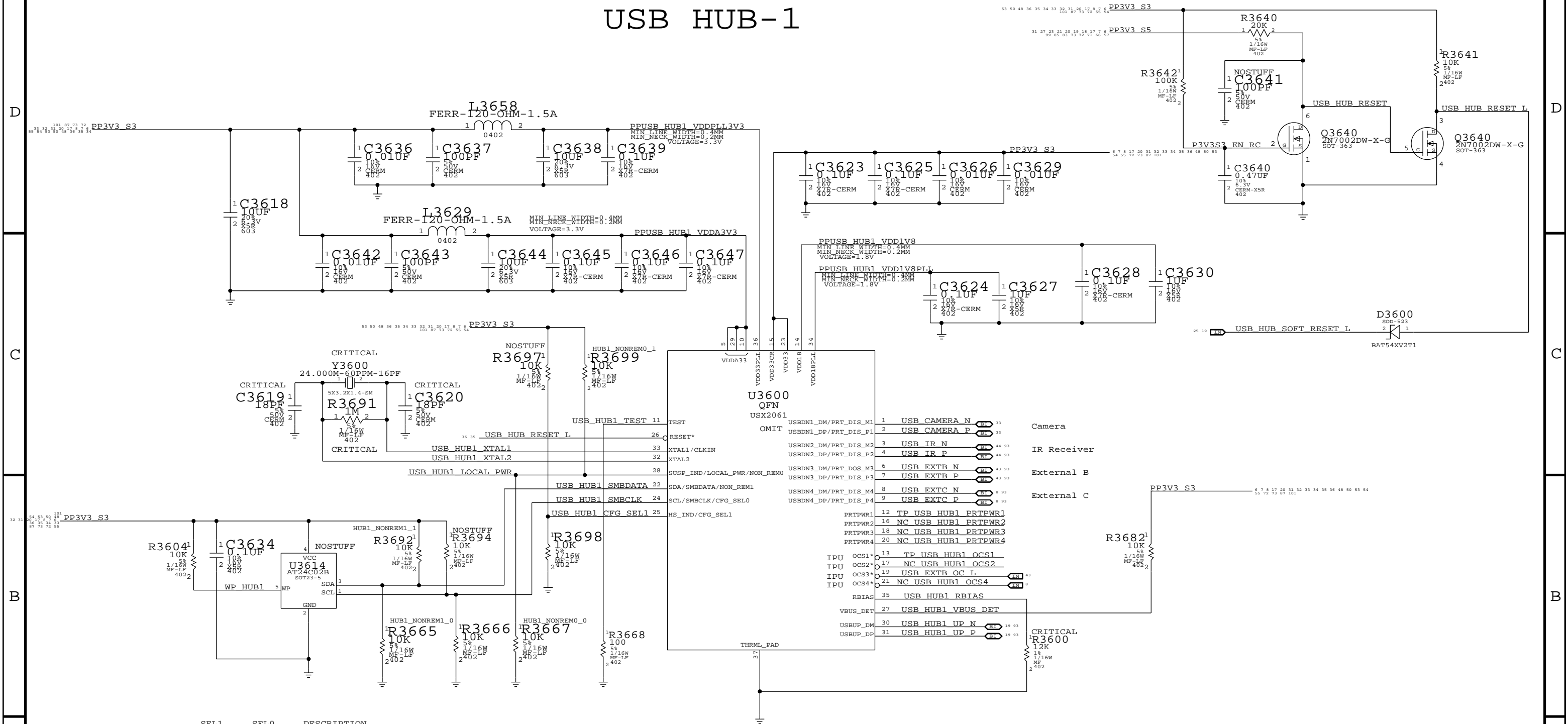
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SEL1	SEL0	DESCRIPTION
0	0	Internal Default with Self powered Operation
0	1	SMBUS Slave Config
1	0	Internal Default with Bus powered Operation
1	1	EEPROM Supported

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0720	2	SMSC USB2514	U3600,U3700	CRITICAL	USBHUB_2514
338S0824	2	SMSC USB2514B	U3600,U3700	CRITICAL	USBHUB_2514B
338S0721	2	SMSC USX2061	U3600,U3700	CRITICAL	USBHUB_2061

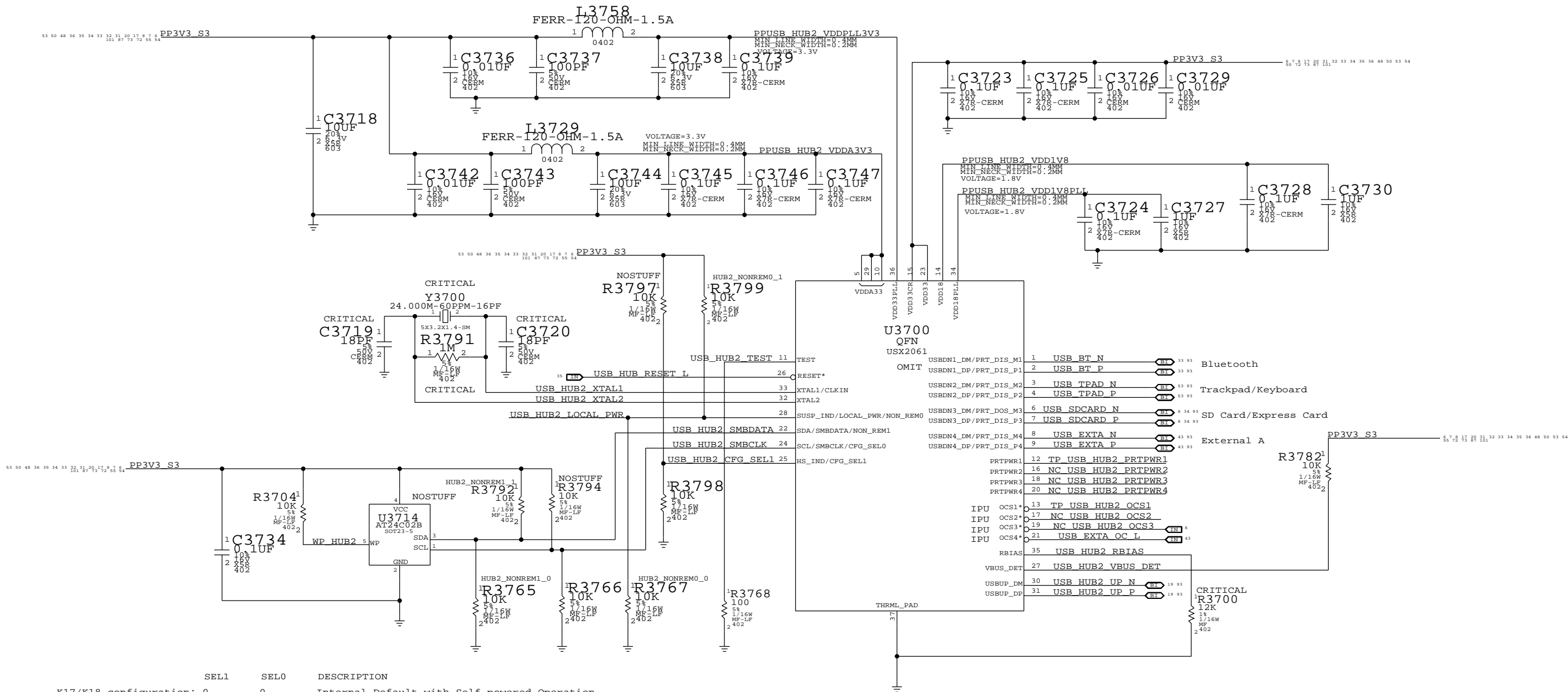
NON_REM1	NON_REMO	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

BOM GROUP	BOM OPTIONS
HUB1_ALLREM	HUB1_NONREM1_0,HUB1_NONREM0_0
HUB1_1NONREM	HUB1_NONREM1_0,HUB1_NONREM0_1
HUB1_2NONREM	HUB1_NONREM1_1,HUB1_NONREM0_0
HUB1_3NONREM	HUB1_NONREM1_1,HUB1_NONREM0_1

SYNC MASTER=K18 MLB SYNC DATE=10/07/2009

PAGE TITLE	
USB HUB 1	
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REVISION <E4LABEL>	SIZE D
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USB HUB-2



	SEL1	SEL0	DESCRIPTION
K17/K18 configuration:	0	0	Internal Default with Self powered Operation
	0	1	SMBUS Slave Config
	1	0	Internal Default with Bus powered Operation
	1	1	EEPROM Supported

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

BOM GROUP	BOM OPTIONS
HUB2_ALLREM	HUB2_NONREM1_0, HUB2_NONREM0_0
HUB2_1NONREM	HUB2_NONREM1_0, HUB2_NONREM0_1
HUB2_2NONREM	HUB2_NONREM1_1, HUB2_NONREM0_0
HUB2_3NONREM	HUB2_NONREM1_1, HUB2_NONREM0_1

SYNC MASTER=K23F

SYNC DATE=10/06/2009

USB HUB 2

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BCM57765 SR LX	3
BCM57765 SR VFB	3

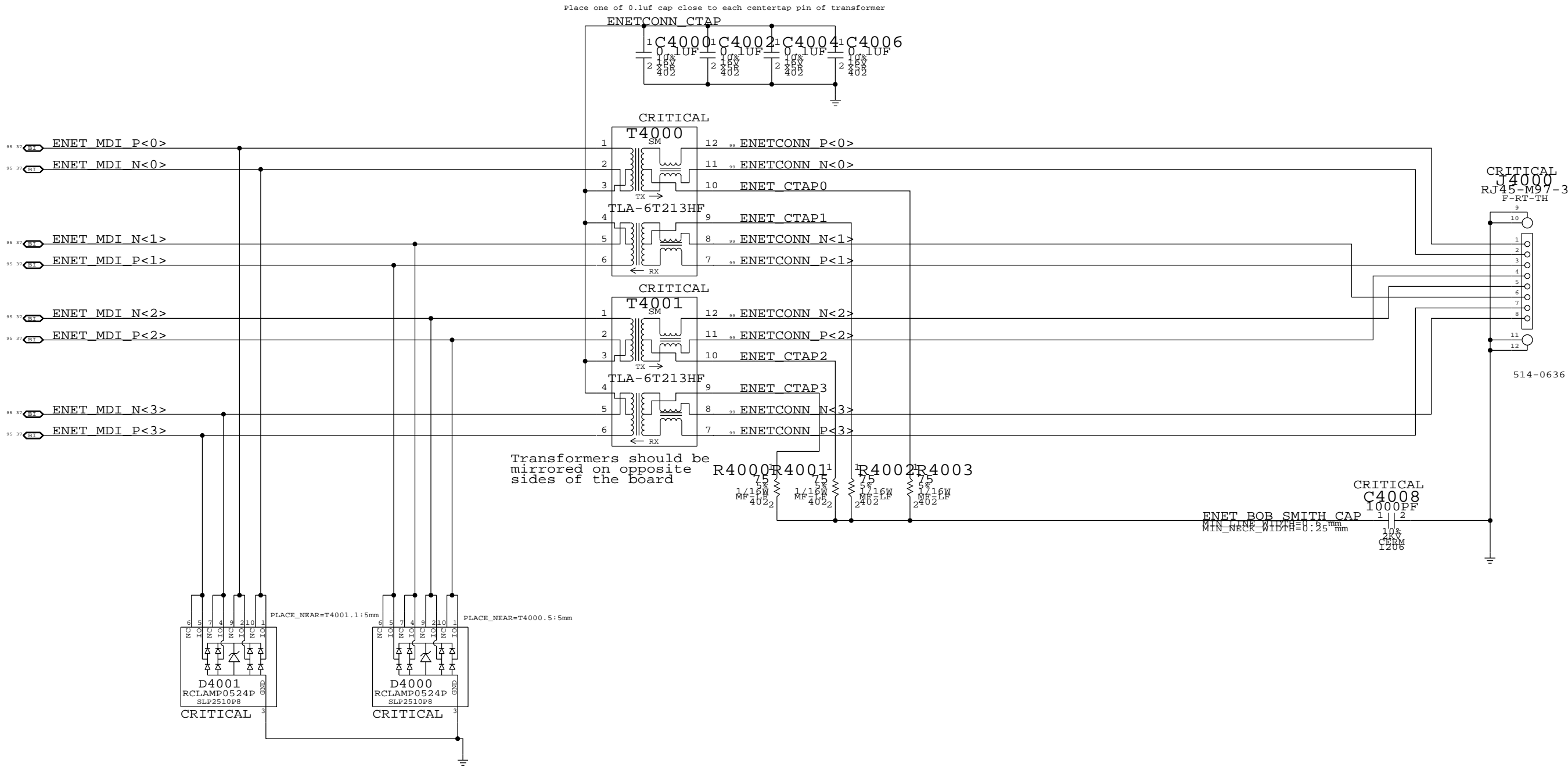



Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



SYNC MASTER=K17 REF		SYNC DATE=06/15/2009		
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Ethernet Connector				
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PAGE		40 OF 132		
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B1

Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMODE (power passthru summation mode)
Signal aliases required by this page:
(NONE)
BOM options provided by this page:

3.3V FW FET

I(max) = 1.7A (85C)

1.05V FW FET

FireWire Port Power Switch

Late-VG Protection

PAGE TITLE		PAGE TITLE	
SYNC MASTER=K19 MLB		SYNC DATE=05/29/2009	
FireWire Port Power		DRAWING NUMBER	
Apple Inc.		<SCH_NUM> D	
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		BRANCH	
		<BRANCH>	
		PAGE	
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		SHEET	
		40 OF 101	

D

```
- =PPVP_FW_PORT1
- =PP3V3_FW_LATEVG
```

```
- =GND_CHASSIS_FW_PORT1
- =GND_CHASSIS_FW_EMI_R
```

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple
FireWire Design Guide (FWDG 0.6, 5/14/03)

Configures PHY for:

- C

Place close to FireWire PHY

B



1 C4314 SM

Note: Trace PPVP_FW_PORT1 must handle up to 5A

```

PPVP FW PORT1 F
MIN LINE WIDTH=0.5 mm
MIN NECK WIDTH=0.25 mm
VOLTAGE=33V

```

C



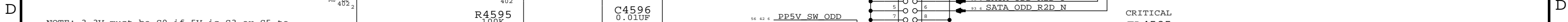
AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

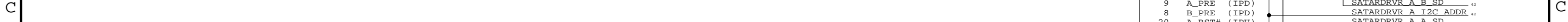
BREF should be hard-connected to logic ground for speed signaling and connection

8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---

SATA ODD Connector




PS8511A / PS8515A Straps



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0769	1	SATA 3GB/S REDRIVER, LOW POWER	U4510	CRITICAL	RDRV:8511
338S0778	1	SATA 3GB/S REDRIVER, LOW POWER	U4510	CRITICAL	RDRV:8515A1

(All 4 C's)



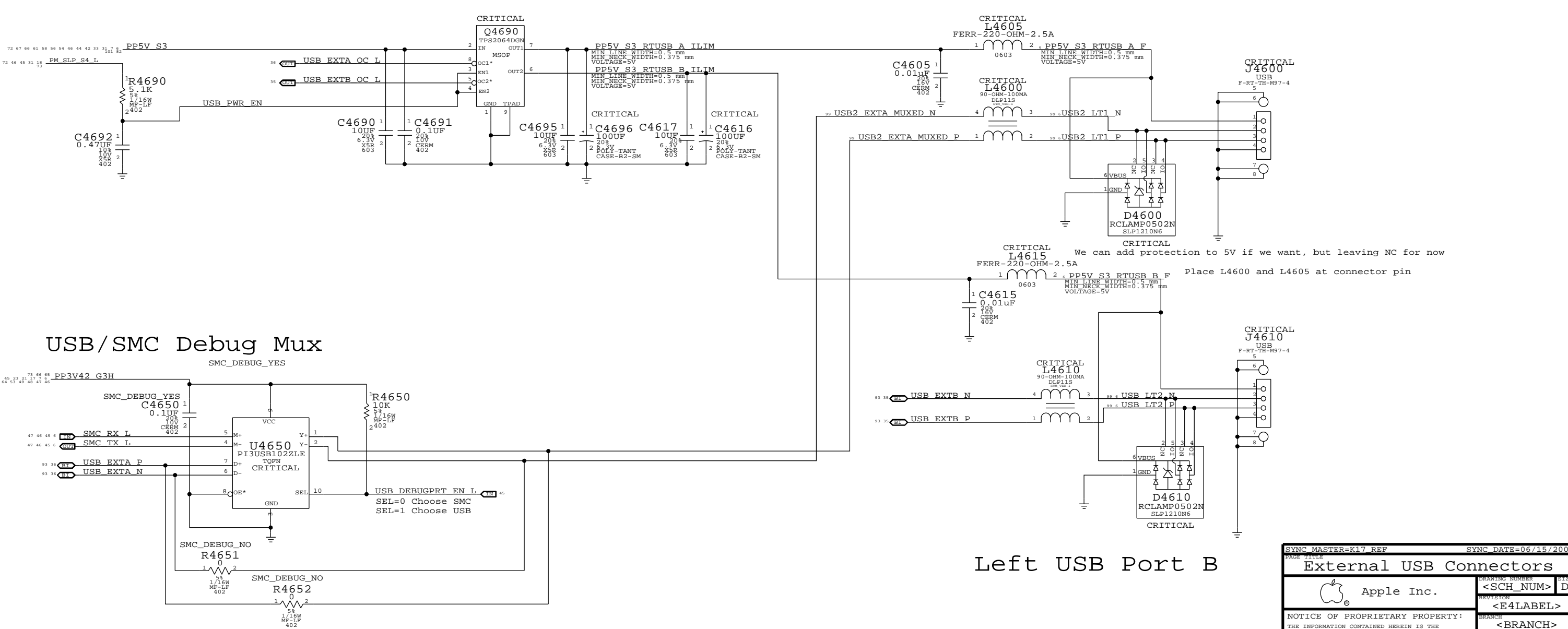
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Port Power Switch

Left USB Port A

USB/SMC Debug Mux

Left USB Port B



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PAGE TITLE			
External USB Connectors			
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		PAGE	46 OF 132
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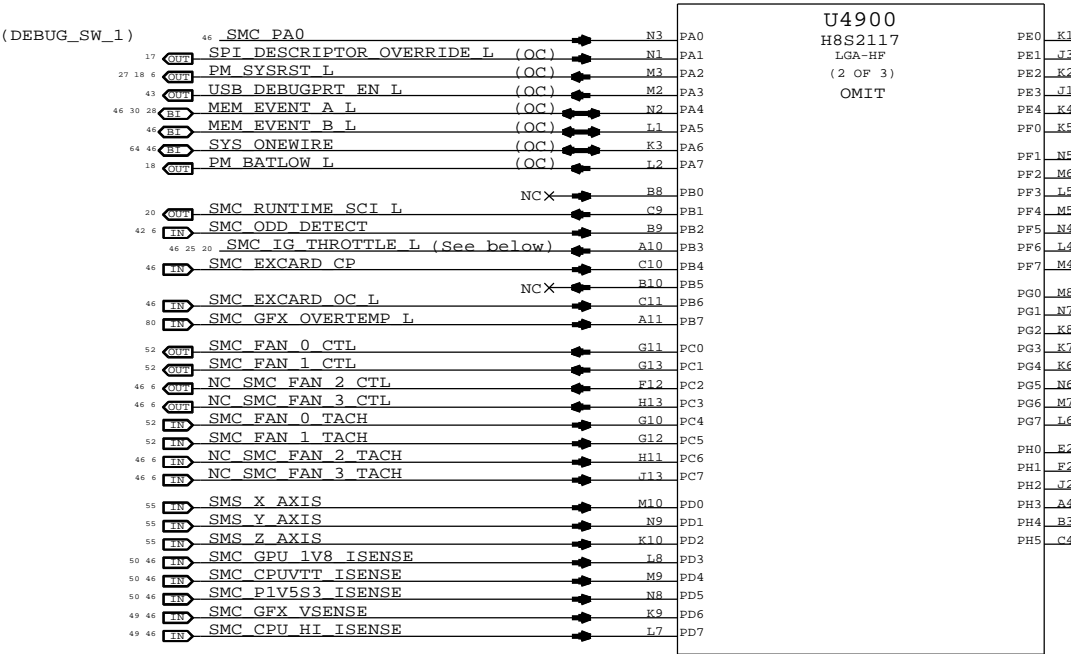
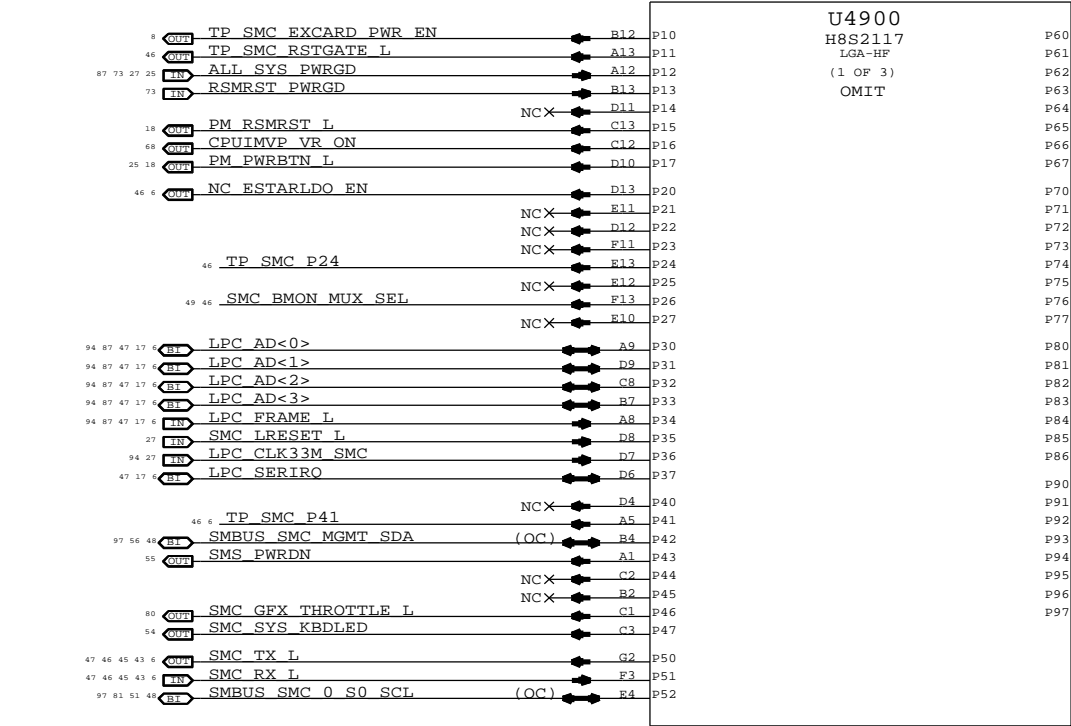
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

D

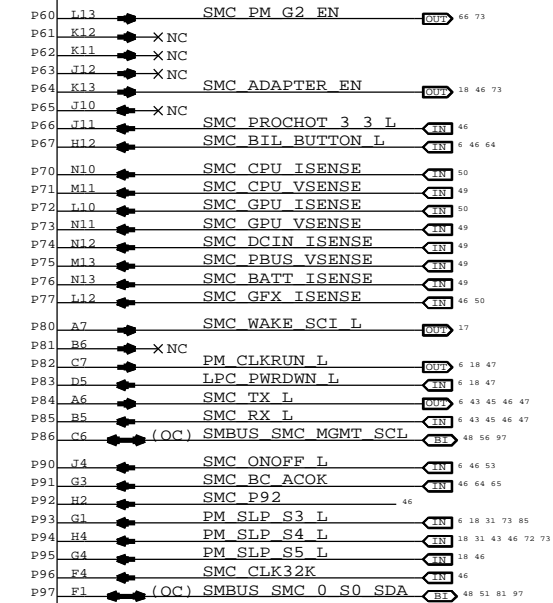
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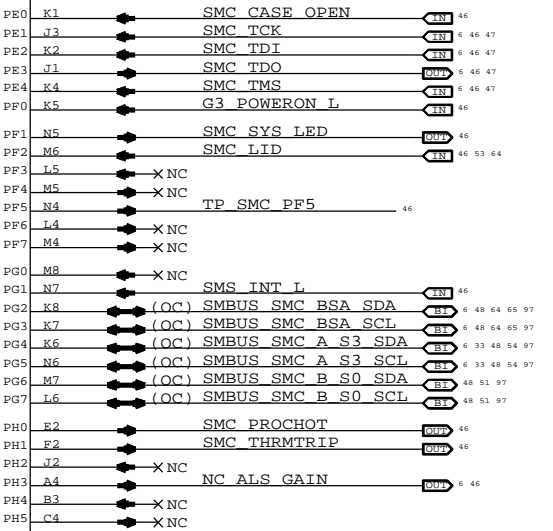
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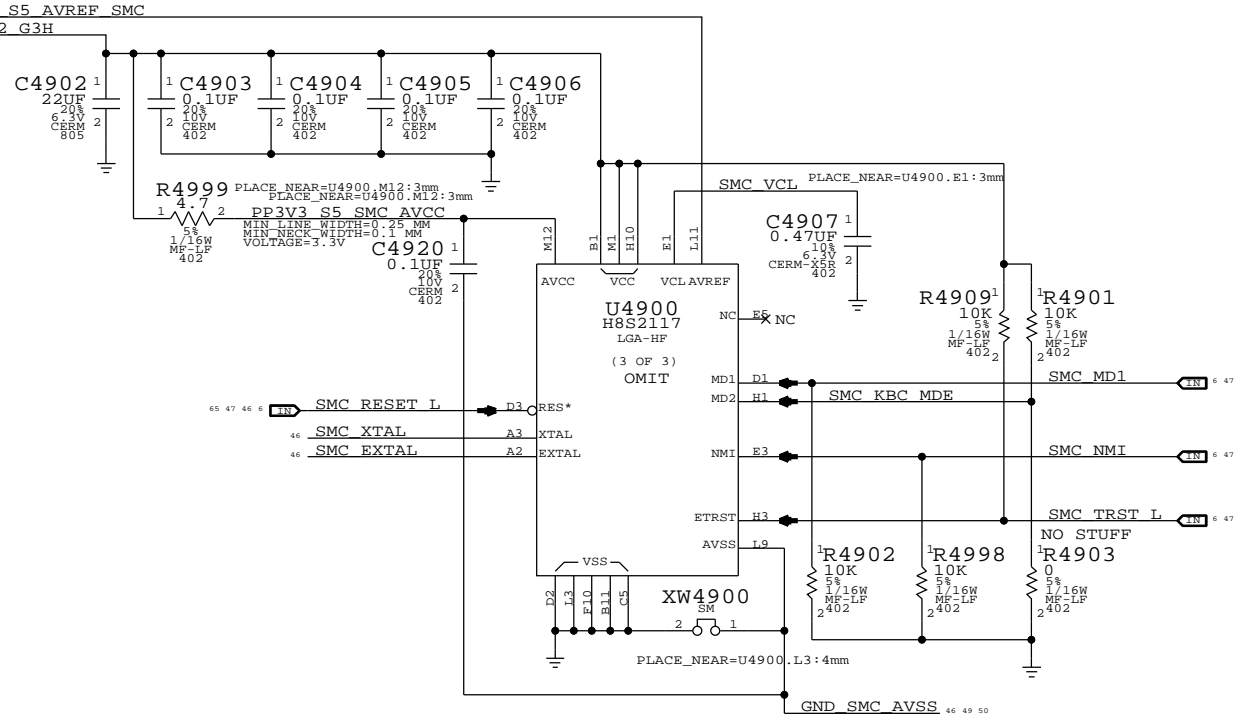
SMC_PB3:
SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)




NOTE: P94 and P95 are shorted, P95 could be spare.

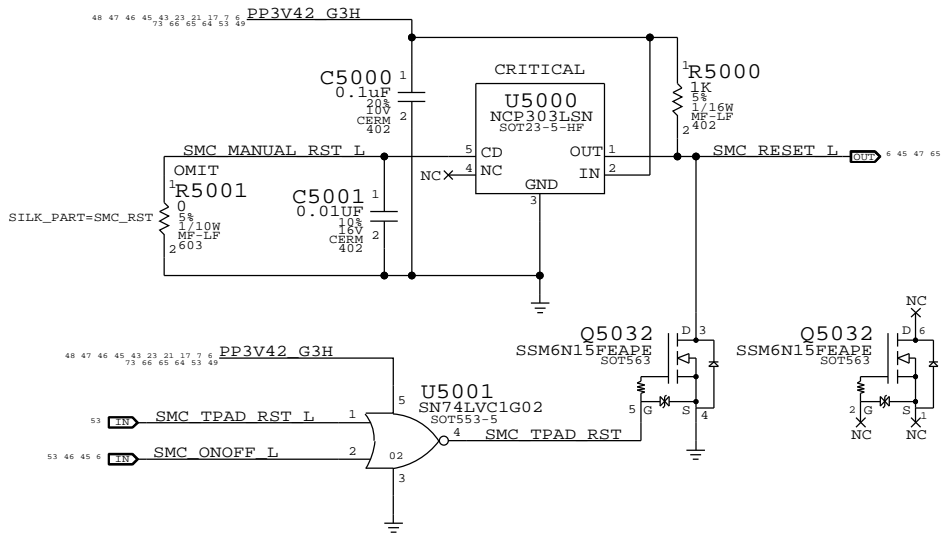


NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

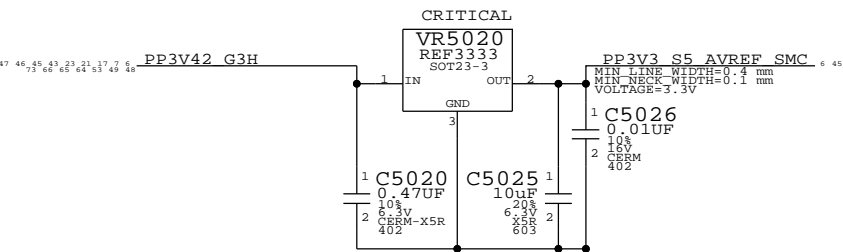


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SMC			
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SMC Reset "Button" / Brownout Detect

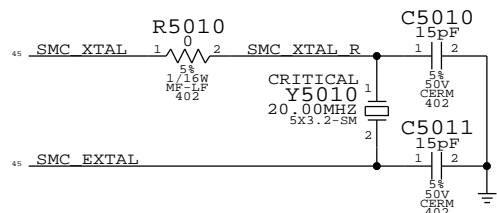


SMC AVREF Supply



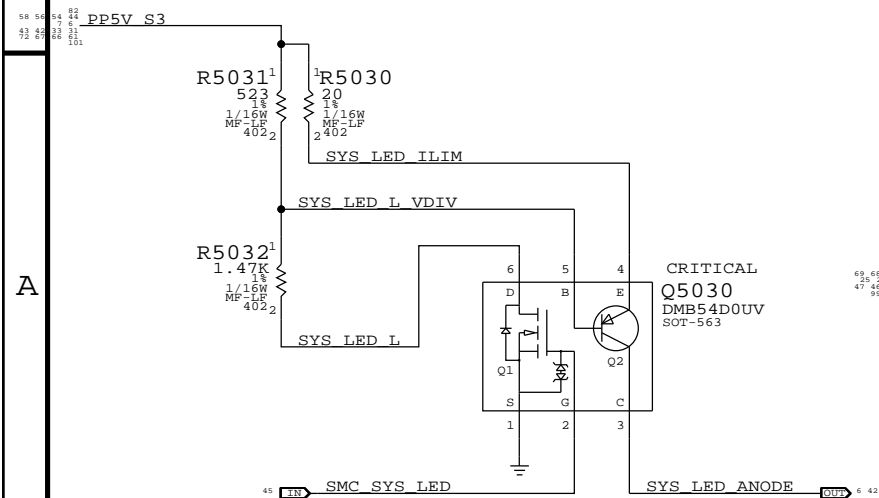
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1912		ALL	Interall ISL60002-33

SMC Crystal Circuit

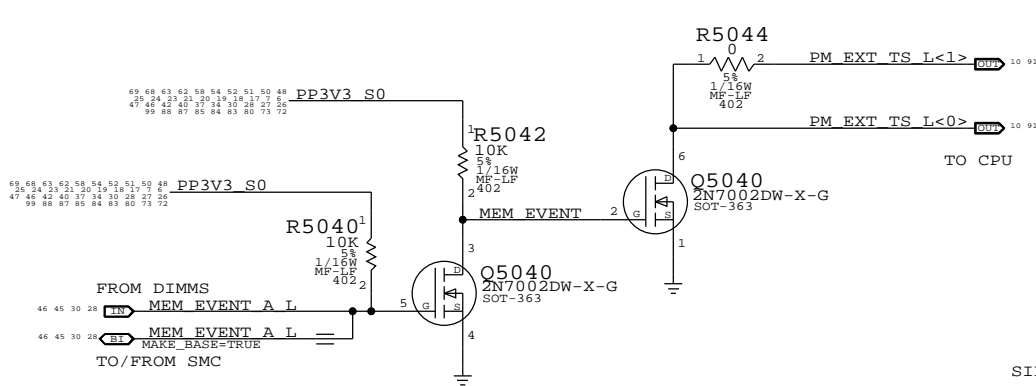


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0350	1	OSC, XTAL, 32.768KHZ, LF, HF	U5010	CRITICAL	SMC_OSC_YES

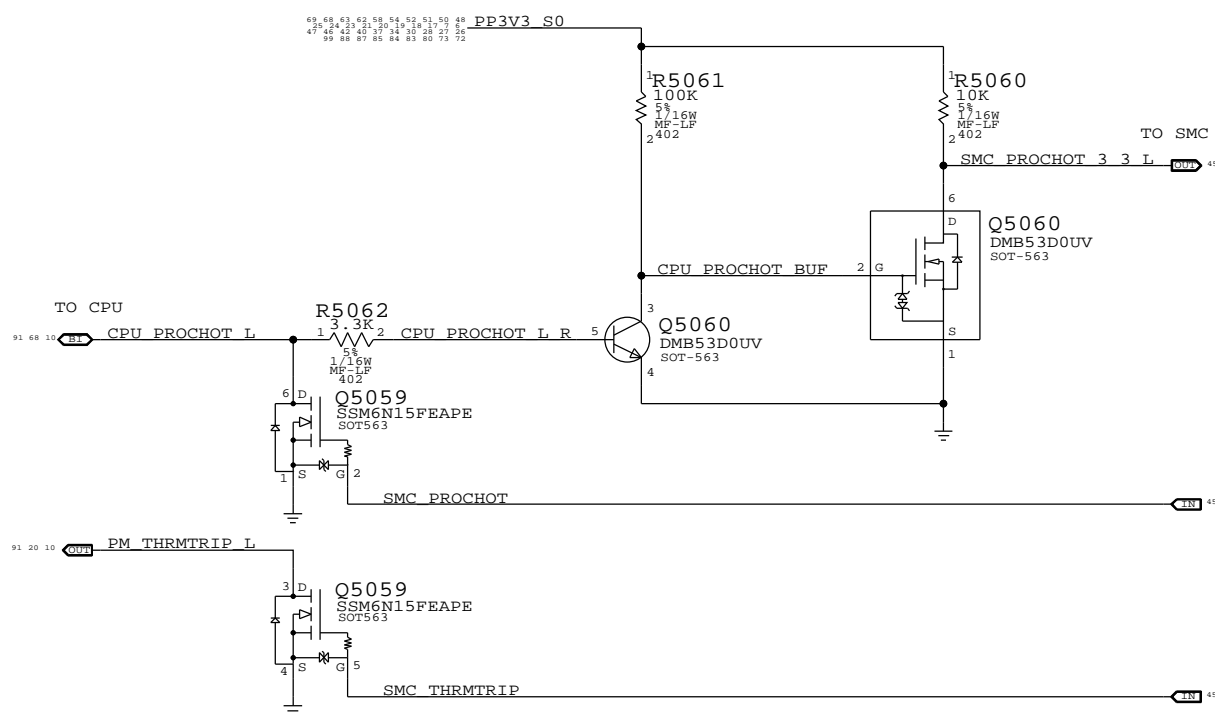
System (Sleep) LED Circuit



CPU PM_EXTTS_L / MEM_EVENT_L Level Shifting

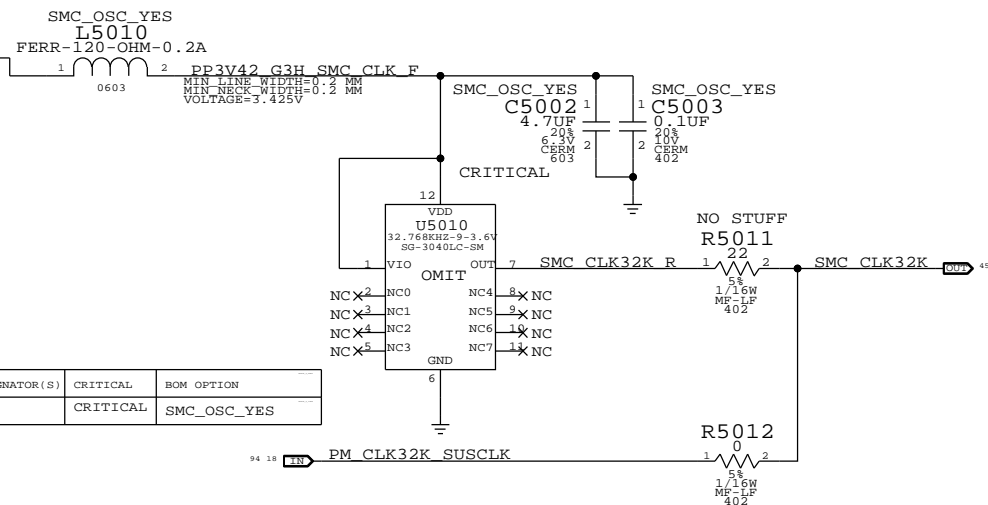


SMC FSB to 3.3V Level Shifting



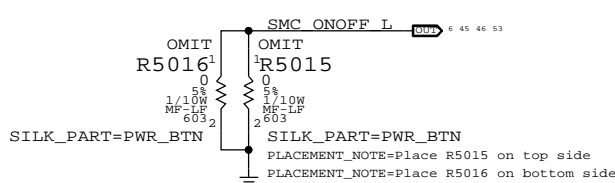
SMC G3Hot 32kHz Oscillator

To support timed wake-up events in G3Hot



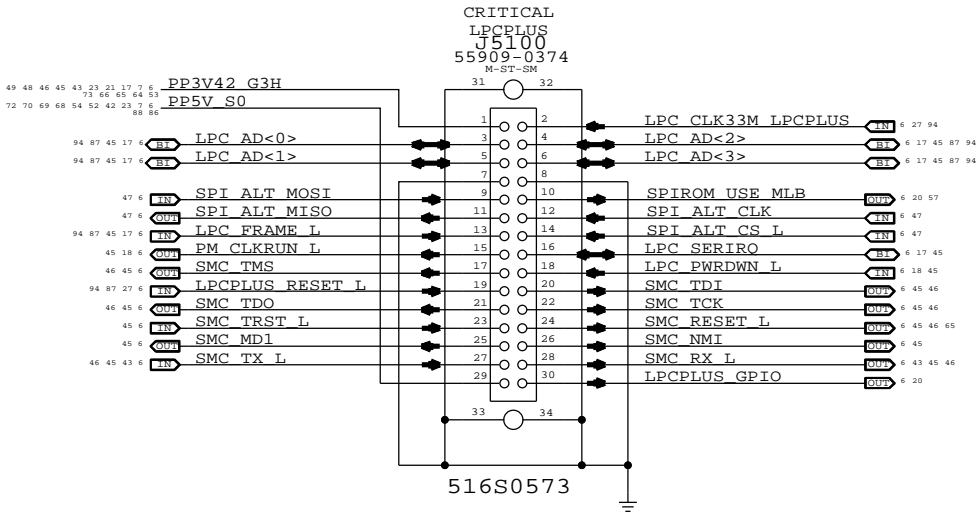
SMC ONOFF L	R5070	10K	1	2	5% 1/16W MF-LF 402
G3 POWERON L	R5072	10K	1	2	5% 1/16W MF-LF 402
SMC LID	R5071	100K	1	2	5% 1/16W MF-LF 402
SMC TX L	R5073	10K	1	2	5% 1/16W MF-LF 402
SMC RX L	R5074	100K	1	2	5% 1/16W MF-LF 402
SYS ONEWIRE NO STUFF	R5075	2.0K	1	2	5% 1/16W MF-LF 402
SMC TMS	R5077	10K	1	2	5% 1/16W MF-LF 402
SMC TDO	R5078	10K	1	2	5% 1/16W MF-LF 402
SMC TDI	R5079	10K	1	2	5% 1/16W MF-LF 402
SMC TCK	R5080	10K	1	2	5% 1/16W MF-LF 402
SMC BIL BUTTON L	R5081	10K	1	2	5% 1/16W MF-LF 402
SMC BC ACOK	R5087	470K	1	2	5% 1/16W MF-LF 402
SMS INT L	R5093	10K	1	2	5% 1/16W MF-LF 402
SMC P92	R5076	100K	1	2	5% 1/16W MF-LF 402
SMC PA0	R5091	100K	1	2	5% 1/16W MF-LF 402
SMC EXCARD OC L	R5092	100K	1	2	5% 1/16W MF-LF 402
SMC ADAPTER EN	R5085	10K	1	2	5% 1/16W MF-LF 402
SMC CASE OPEN	R5086	10K	1	2	5% 1/16W MF-LF 402
SMC EXCARD CP	R5088	10K	1	2	5% 1/16W MF-LF 402
PM SLP S5 L	R5090	100K	1	2	5% 1/16W MF-LF 402
PM SLP S4 L	R5094	100K	1	2	5% 1/16W MF-LF 402

Debug Power "Buttons"

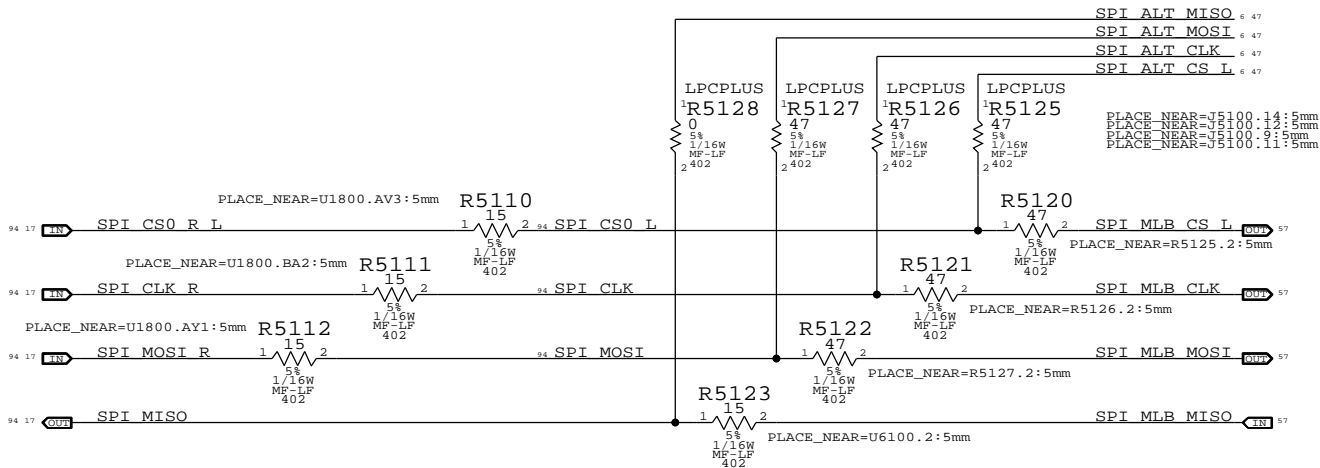


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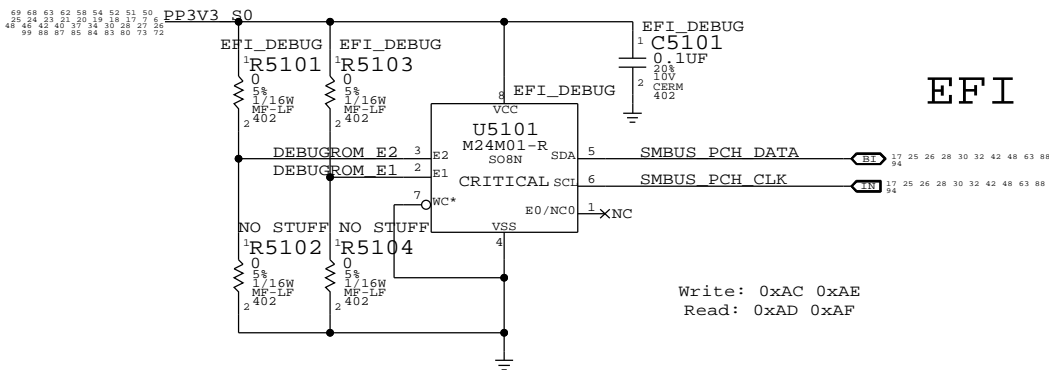
LPC+SPI Connector




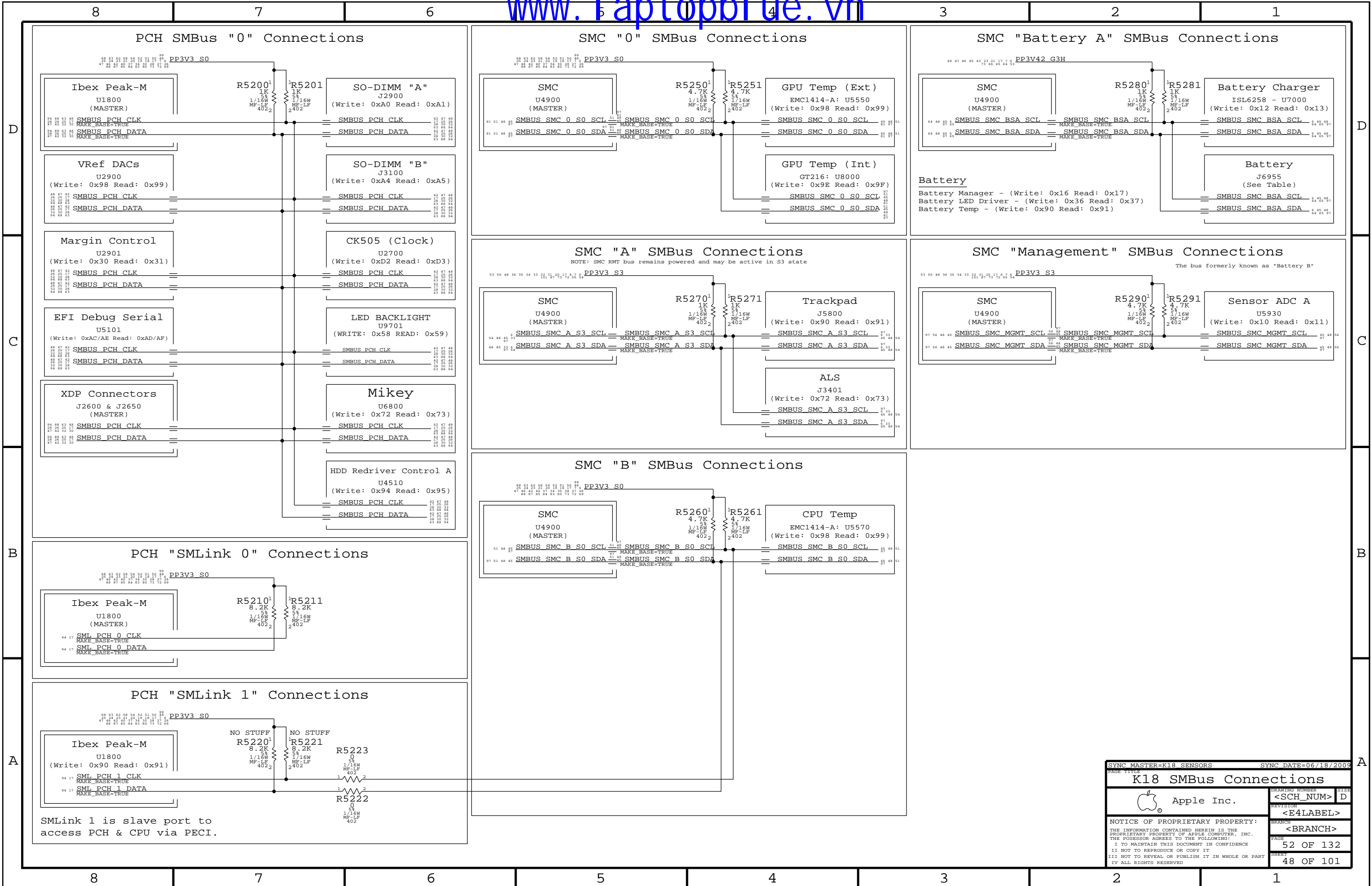
SPI Bus Series Termination



EFI Debug ROM



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LPC+SPI Debug Connector			
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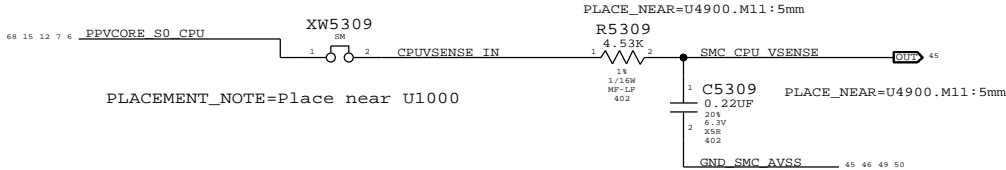
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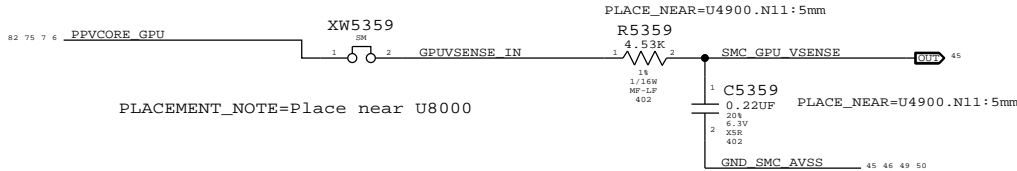
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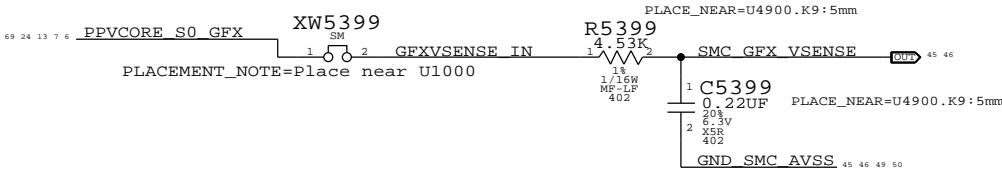
CPU Voltage Sense / Filter



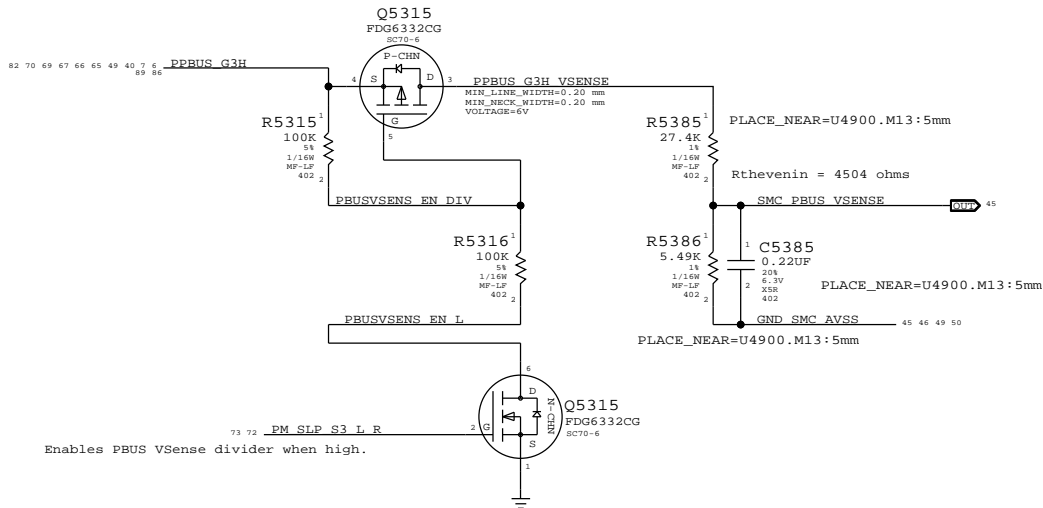
GPU Voltage Sense / Filter



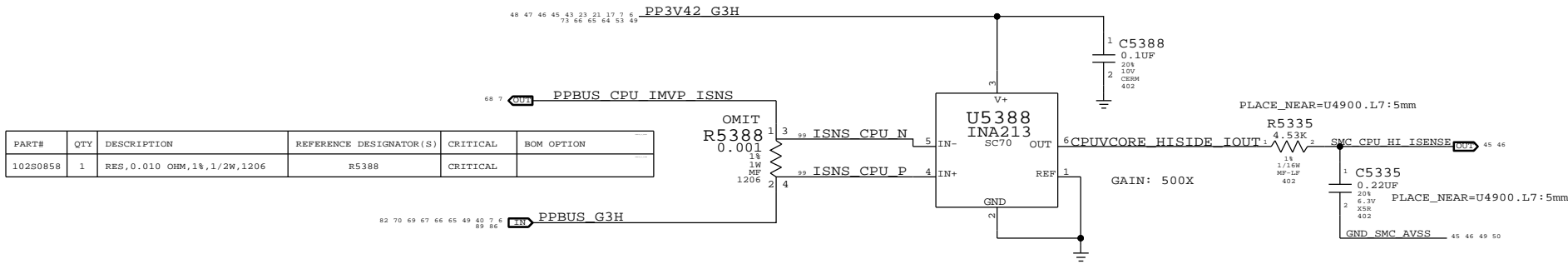
GFX Voltage Sense / Filter



PBUS Voltage Sense & Filter

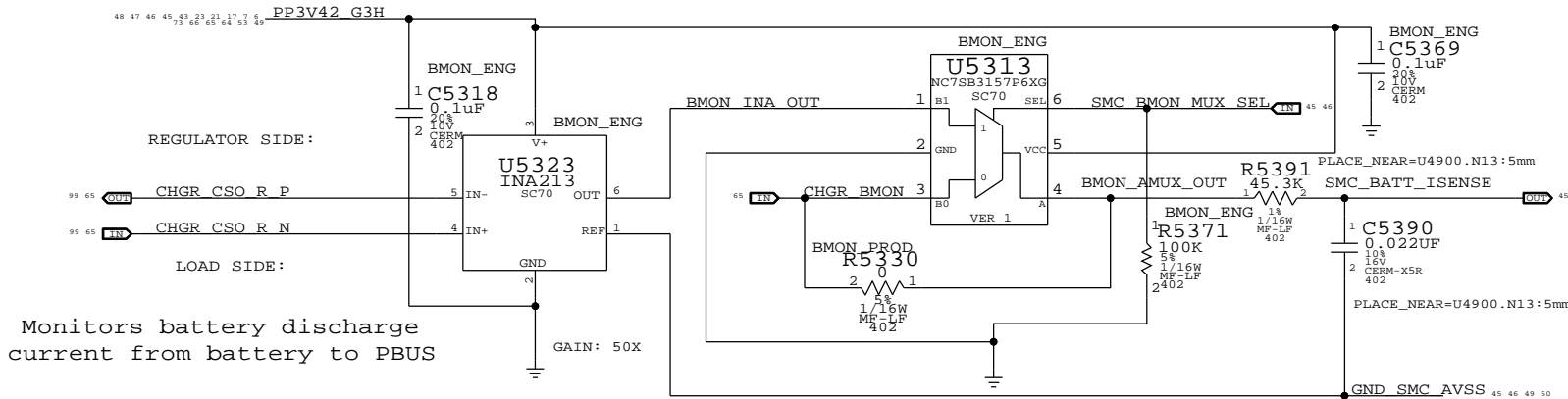


CPU VCore High Side Current Sensor



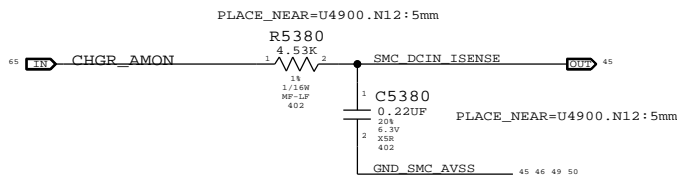
EDP for PPVIN_S5_CPU_IMVP_ISNS_R = 5.867 amps for K18.

BMON Current Sense - Entire circuit must be near SMC (U4900)




Monitors battery discharge current from battery to PBUS

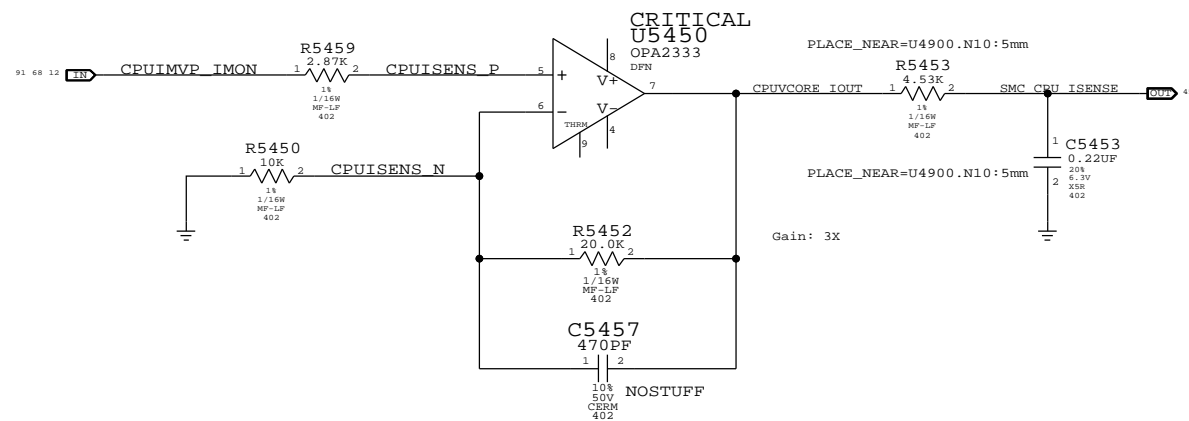
DCIN Current Sense Filter



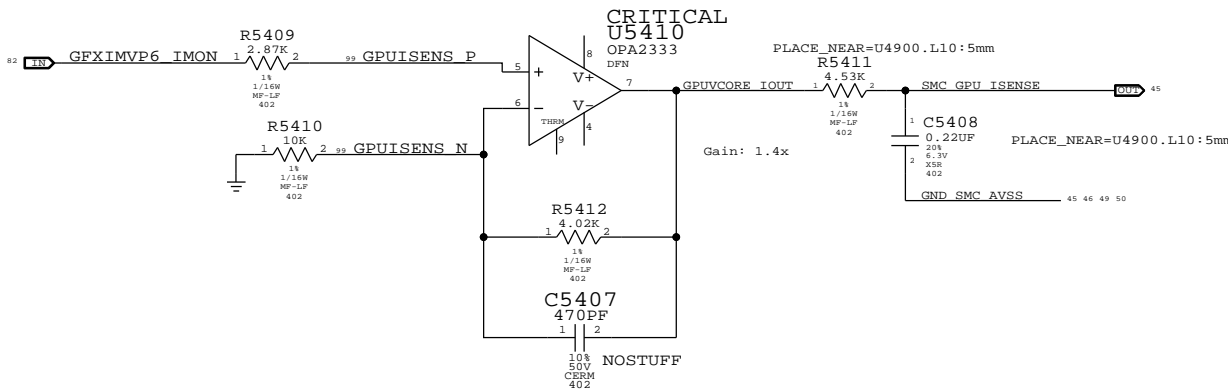
U5303 only senses current up to 6.6A

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PAGE TITLE			
Current & Voltage Sensing			
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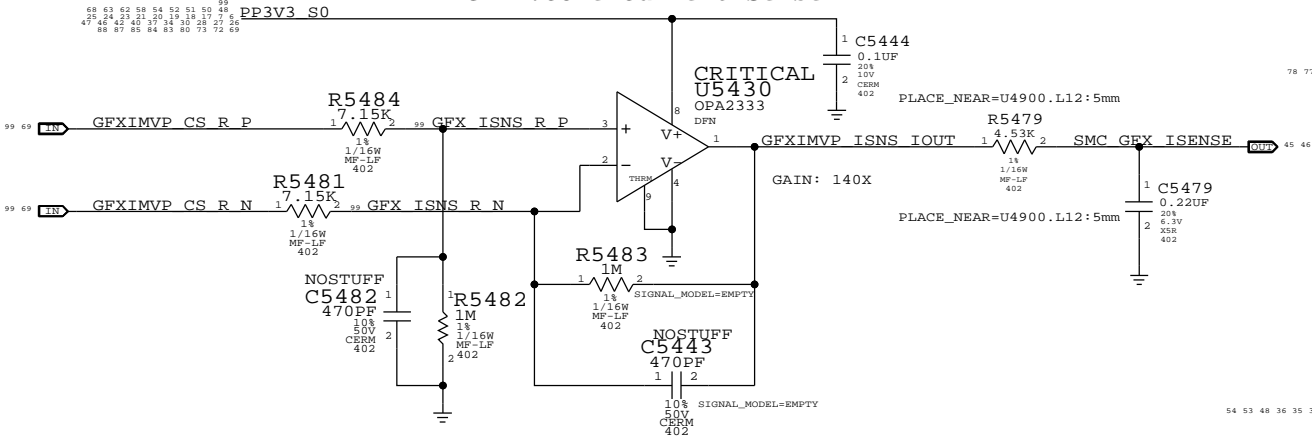
CPU VCore Load Side Current Sense / Filter



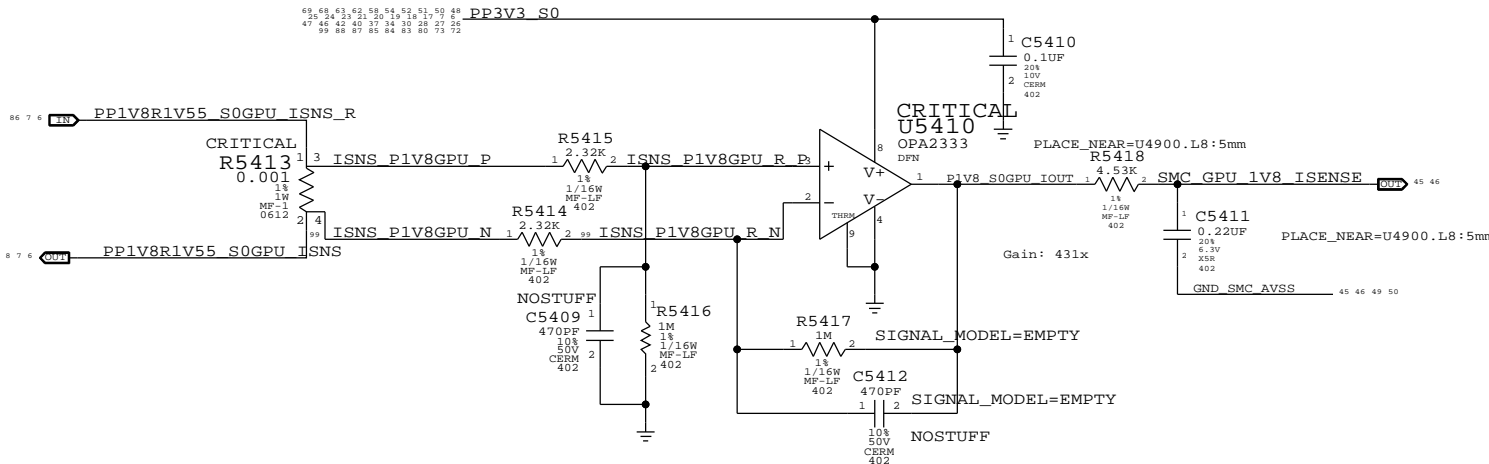
GPU VCore Current Sense



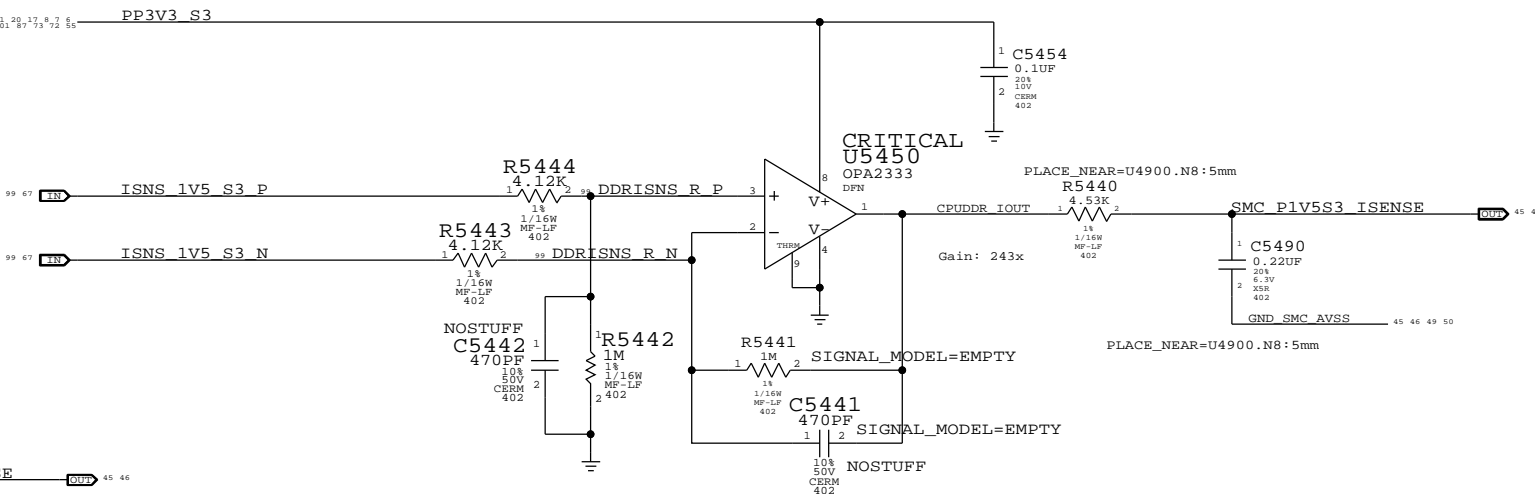
GFX VCore Current Sense



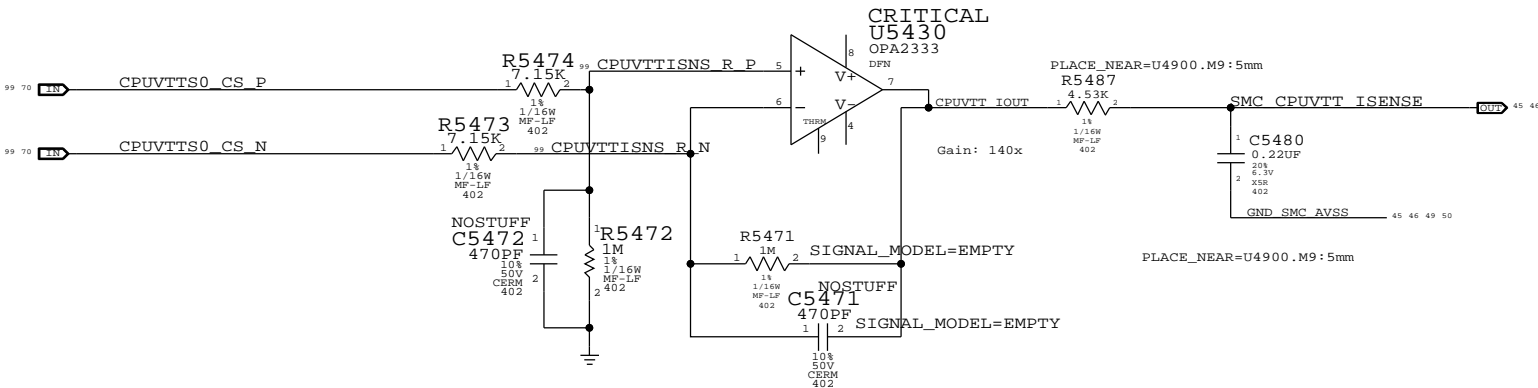
1.8V FB Current Sense



CPU & MEM 1.5V S3 (DDR) Current Sense

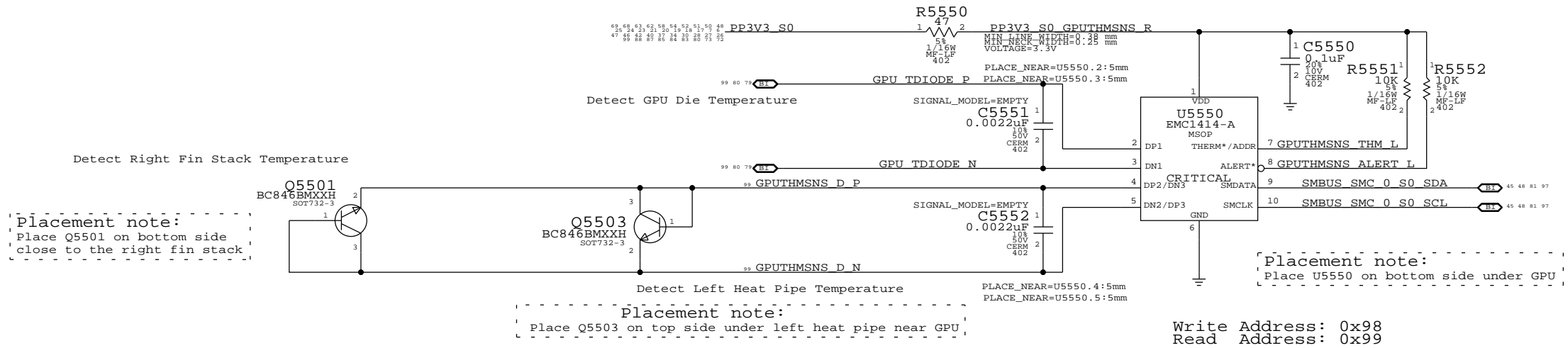


CPUVTT 1.05V Current Sense

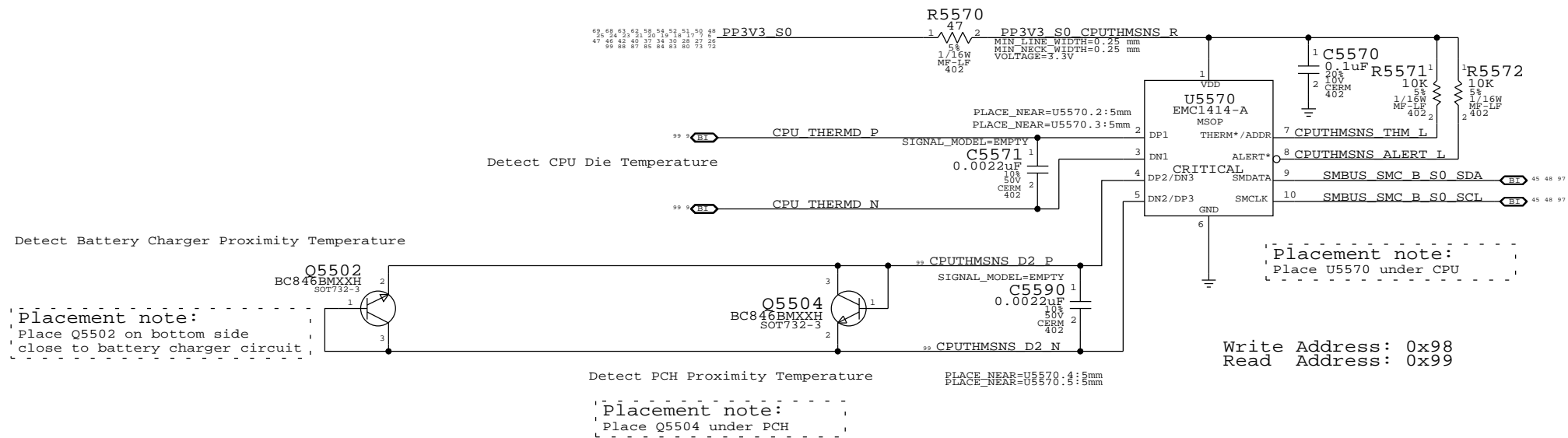


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		PAGE	54 OF 132
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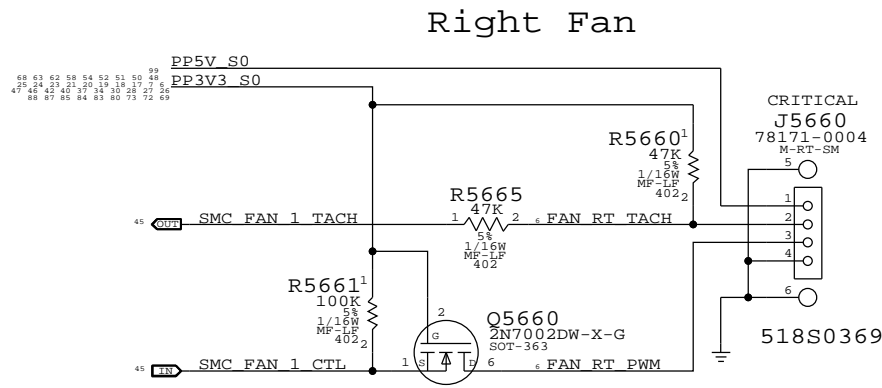
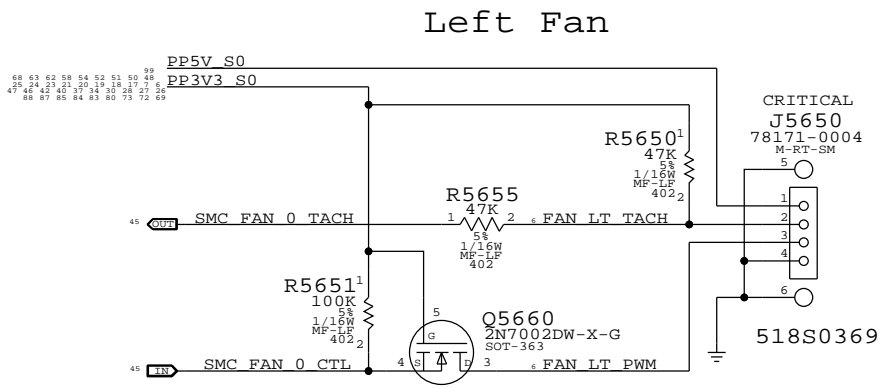
GPU Proximity/GPU Die/Left Heat Pipe/Right Fin Stack



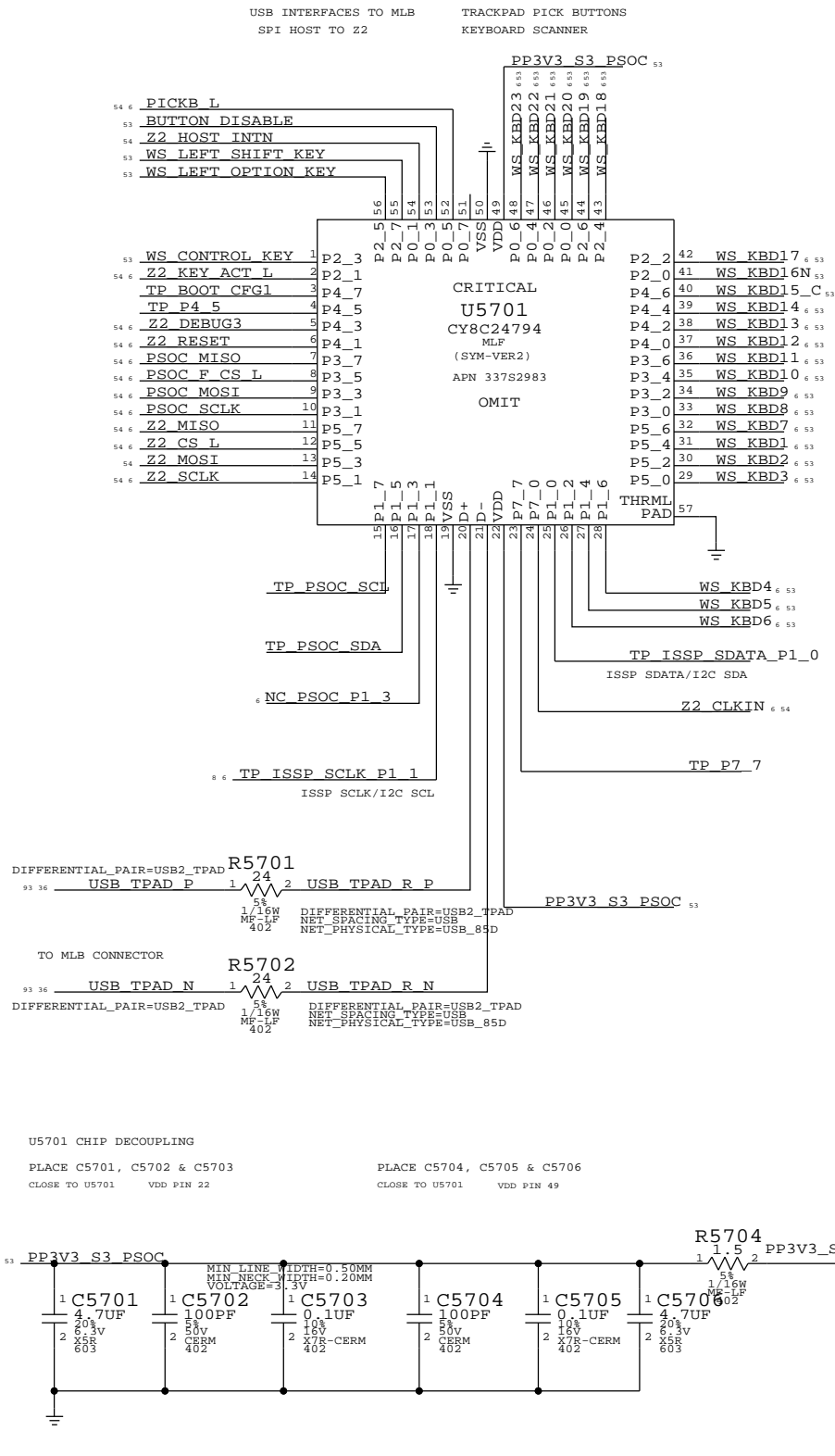
CPU Proximity/CPU Die/PCH Proximity/Battery Charger Proximity



Note: EMC1414 can perform Beta Compensation for External Diode 1 only

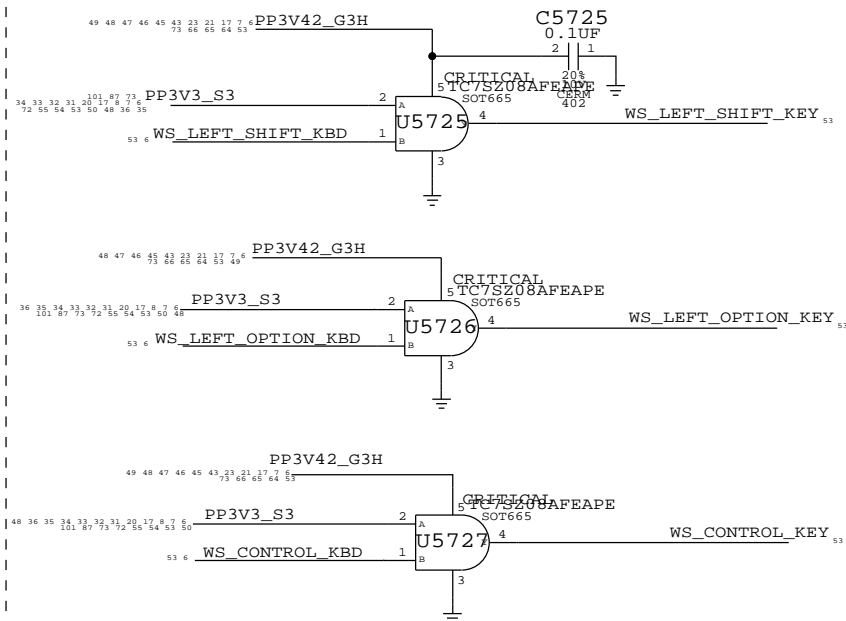


PSOC USB CONTROLLER

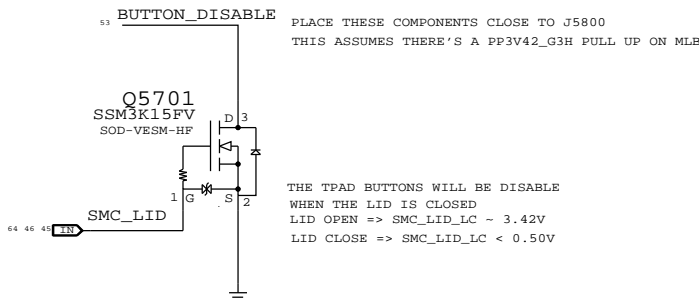


IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	100A	2.55 KOHM	0.0255 V	0.255E-6 W
3V3 LDO	VDD	800A	10 OHM	0.204 V	16.32E-6 W
	VOUT	60MA MAX	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TVP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
1.8V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

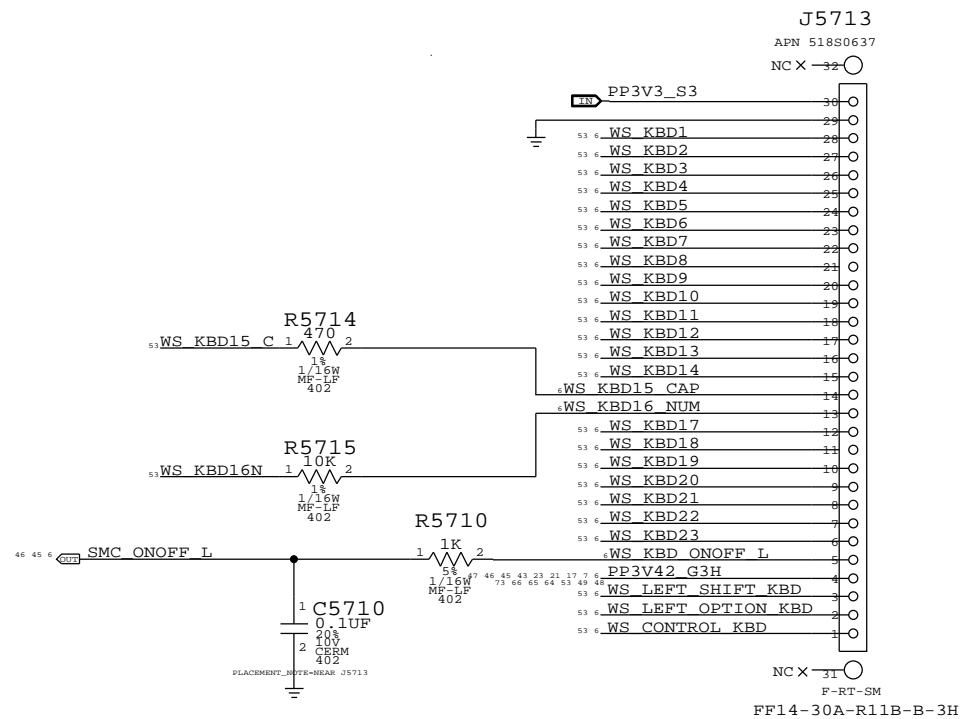
ISOLATION CIRCUIT



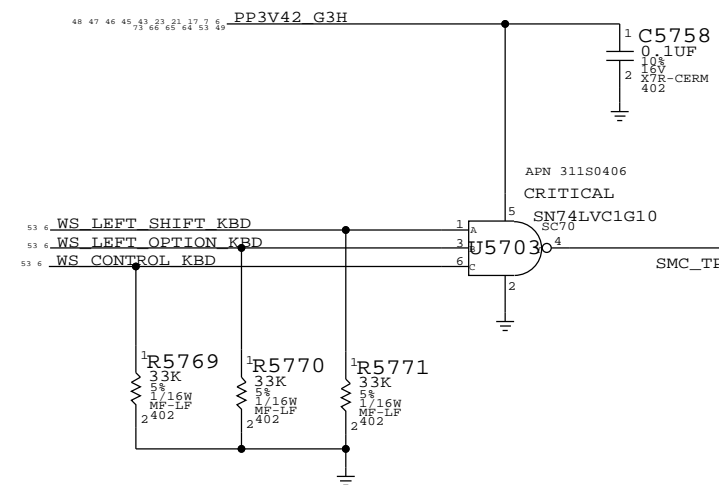
TPAD BUTTONS DISABLE




KEYBOARD CONNECTOR

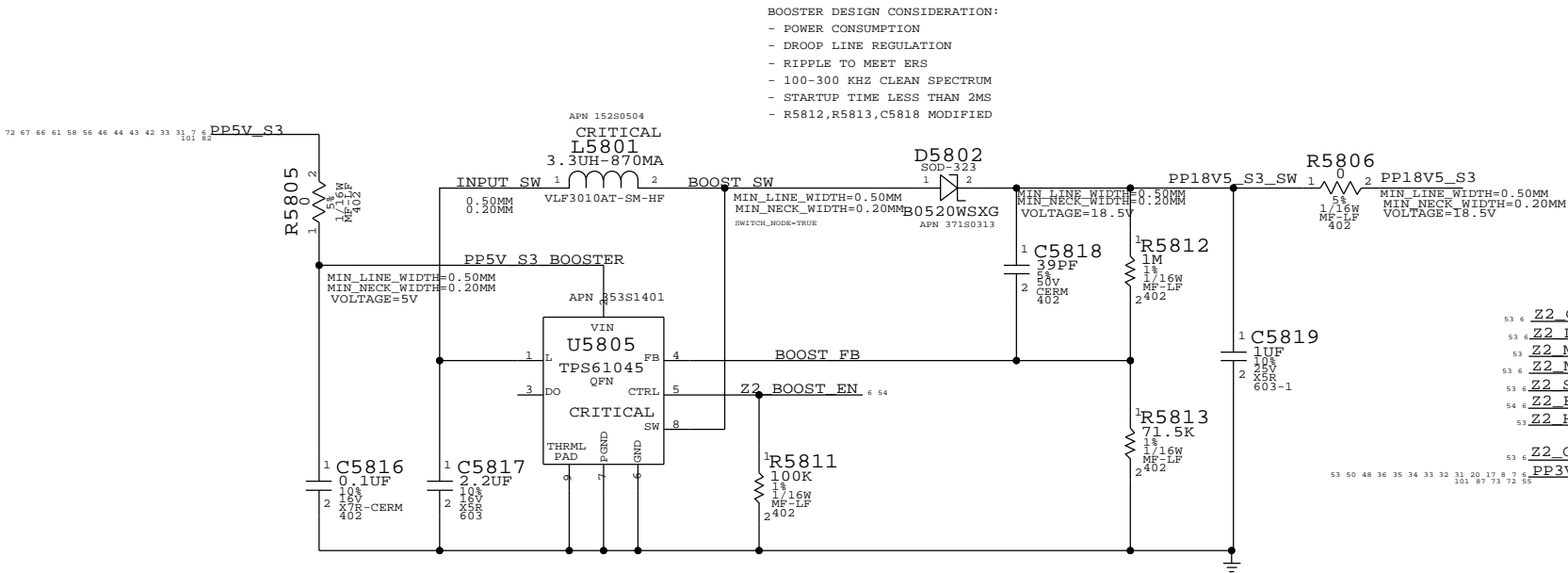


SMC_MANUAL_RESET LOGIC

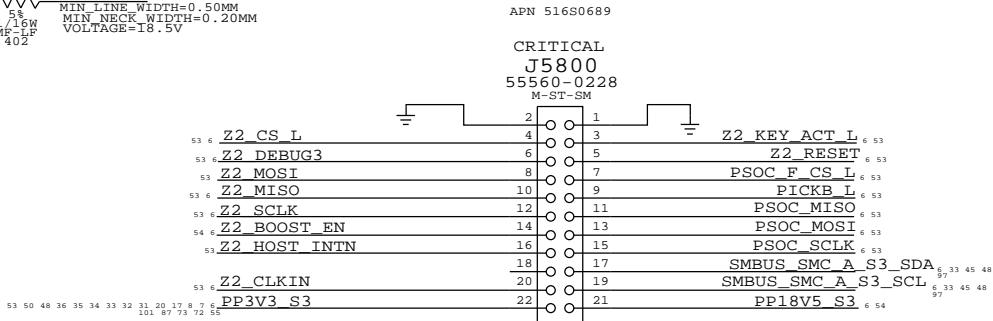


SYNC MASTER=K19 MLB		SYNC DATE=05/29/2009	
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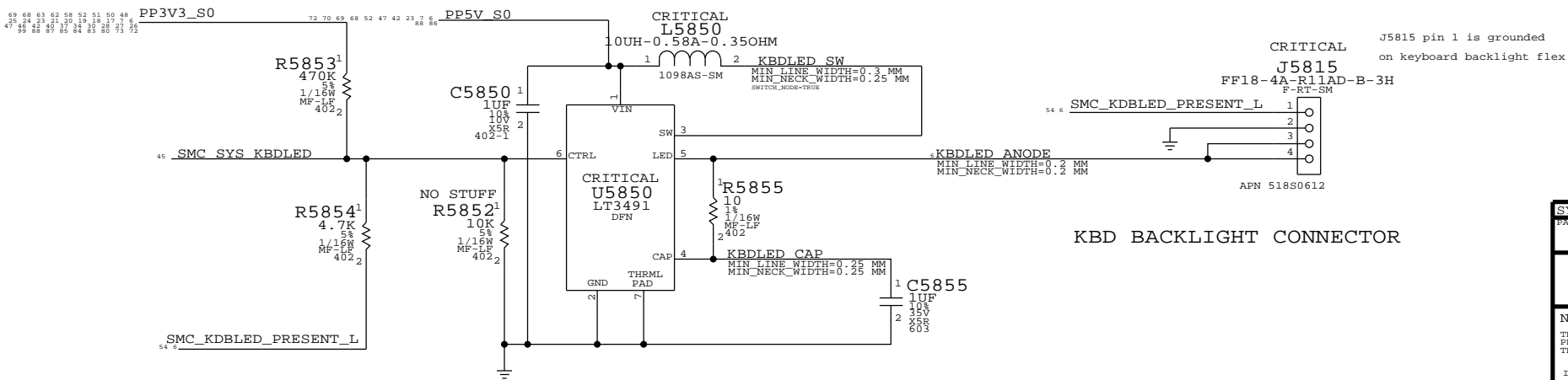
BOOSTER +18.5VDC FOR SENSORS




IPD FLEX CONNECTOR

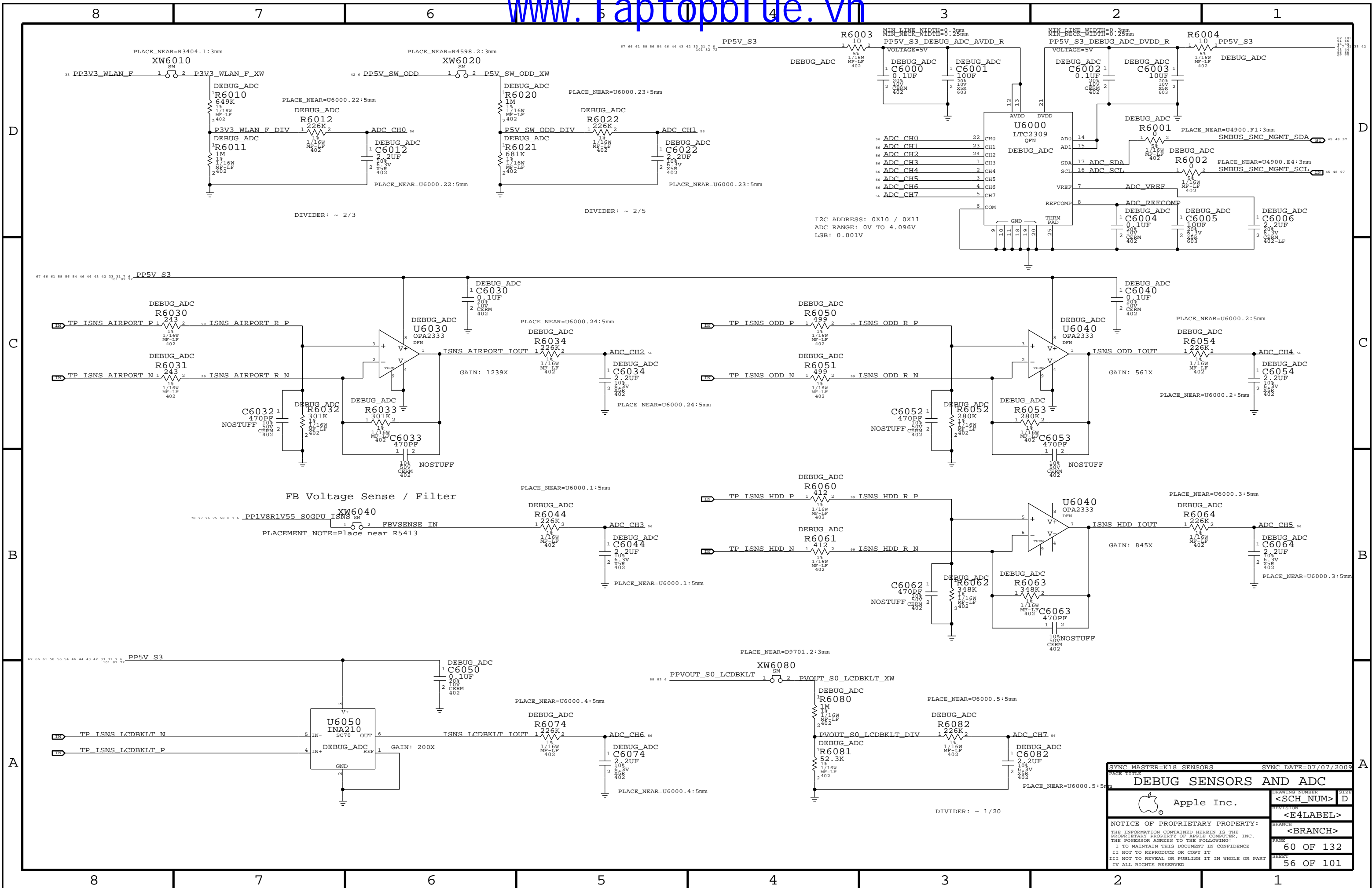



Keyboard LED Driver

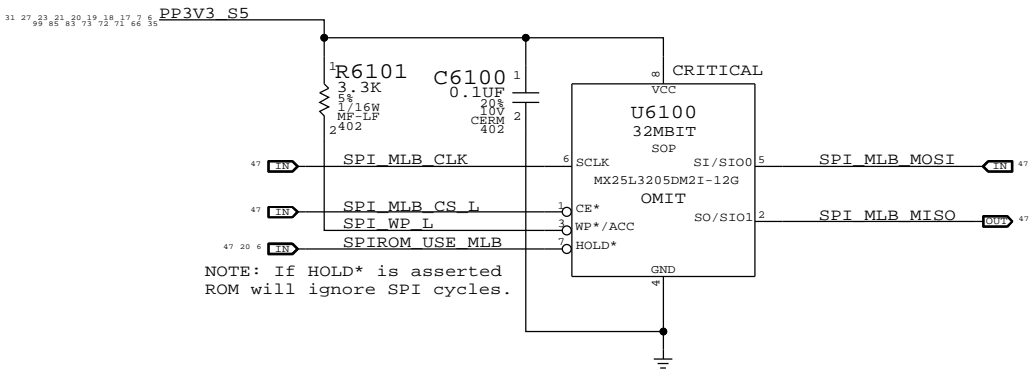


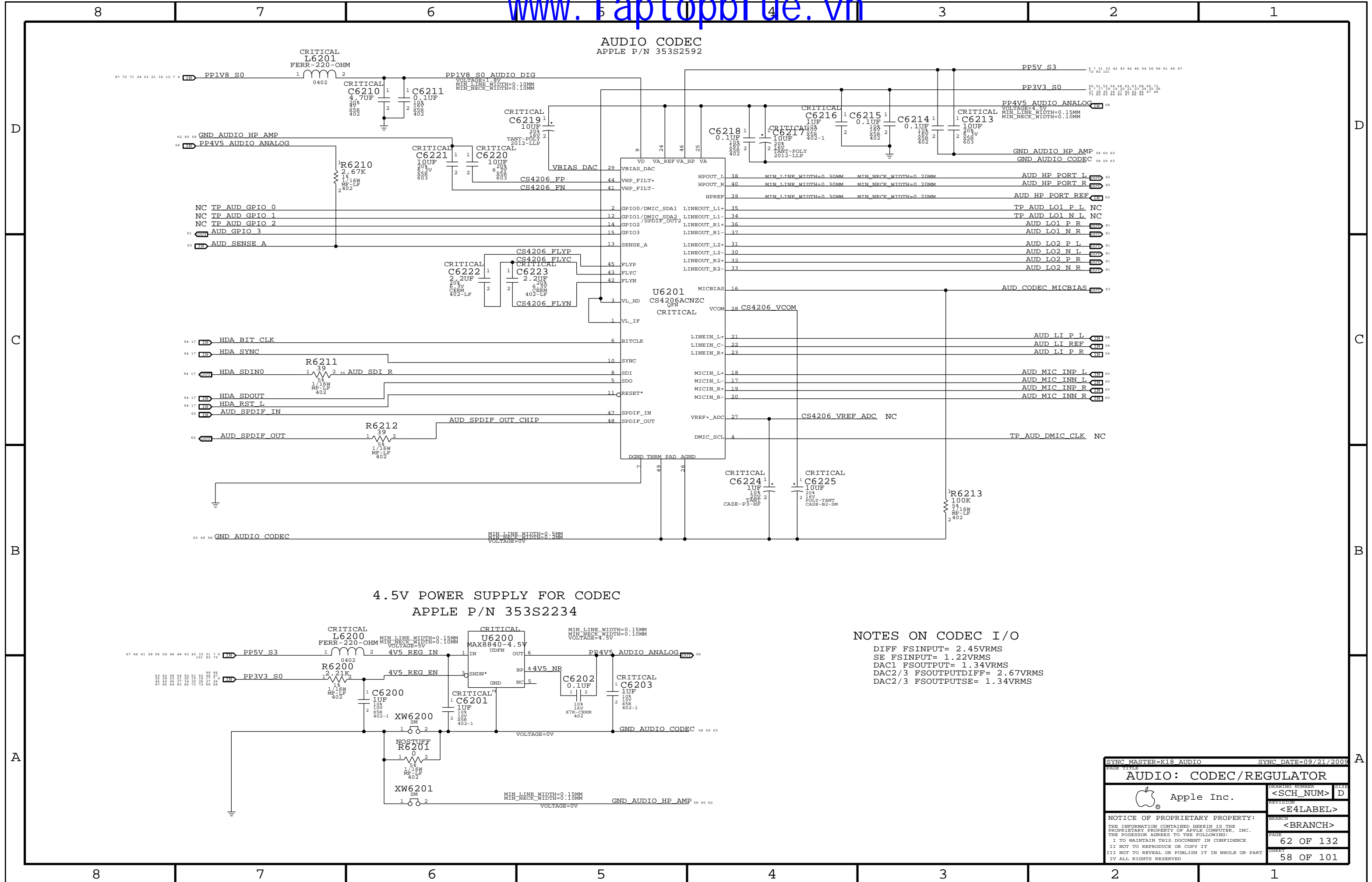
KBD BACKLIGHT CONNECTOR


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WELLSPRING 2			
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		PAGE	58 OF 132
		SHEET	54 OF 101



SYNC MASTER=K18_SENSORS		SYNC DATE=07/07/2009	
PAGE TITLE			
DEBUG SENSORS AND ADC			
 Apple Inc.		DRAWING NUMBER	SIZE
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		PAGE	60 OF 132
		SHEET	56 OF 101

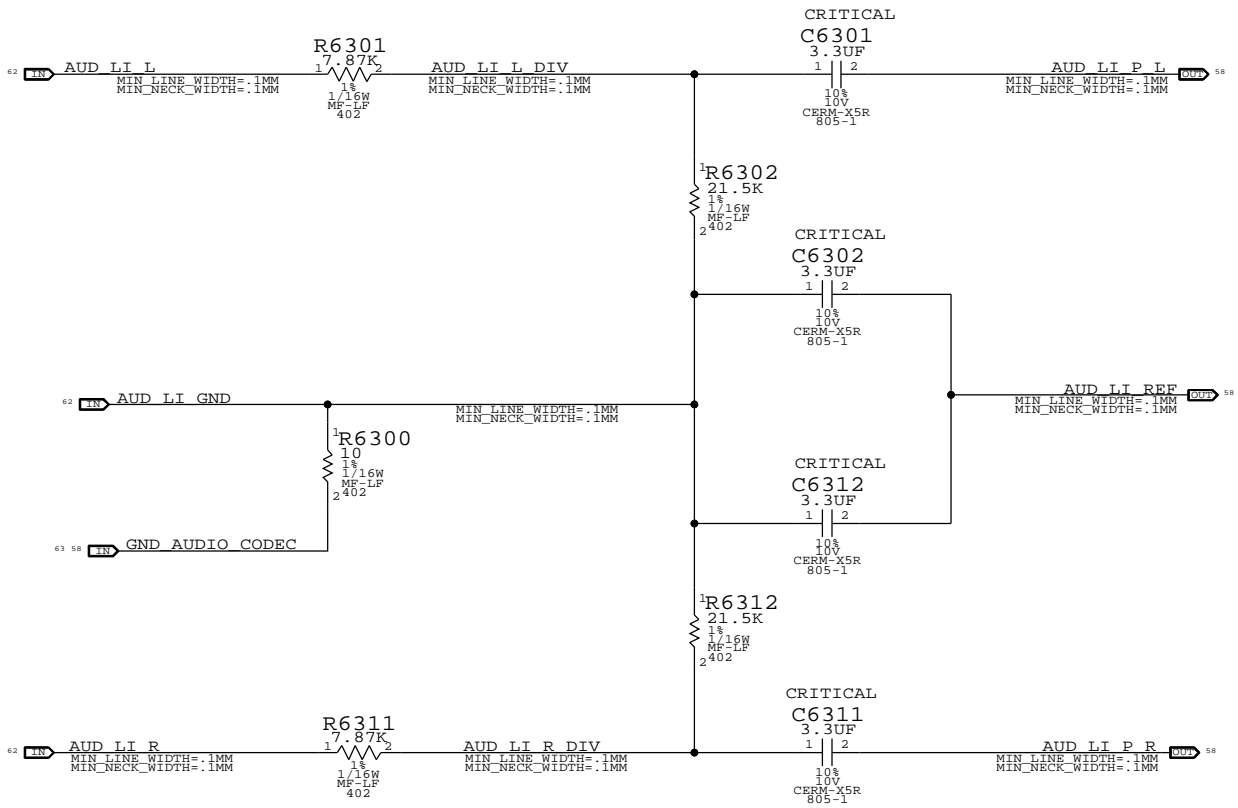




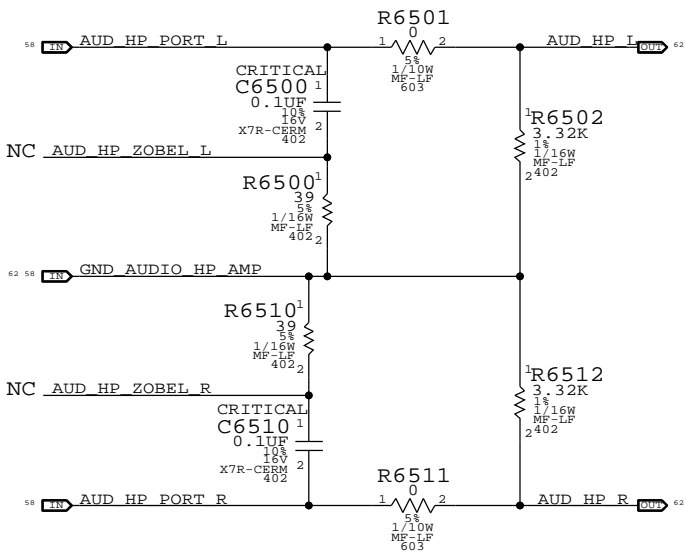
SYNC MASTER=K18_AUDIO		SYNC DATE=09/21/2009	
PAGE TITLE			
AUDIO: CODEC/REGULATOR			
 Apple Inc.		DRAWING NUMBER	SIZE
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		REVISION	
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		PAGE	62 OF 132
		SHEET	58 OF 101

LINE INPUT VOLTAGE DIVIDER

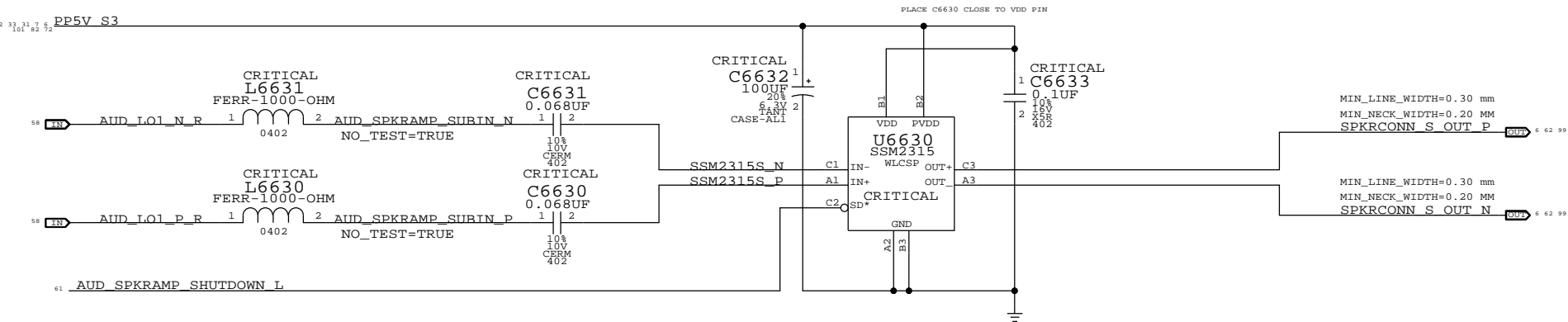
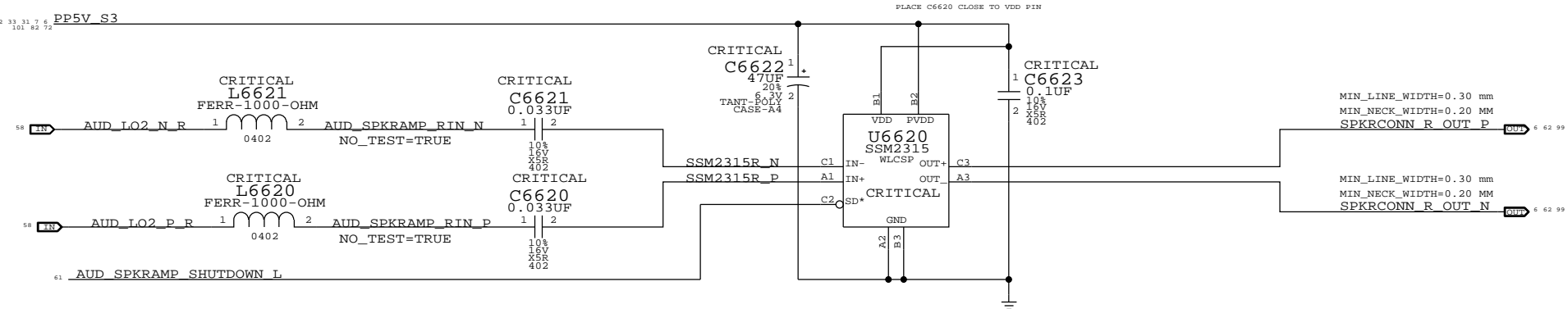
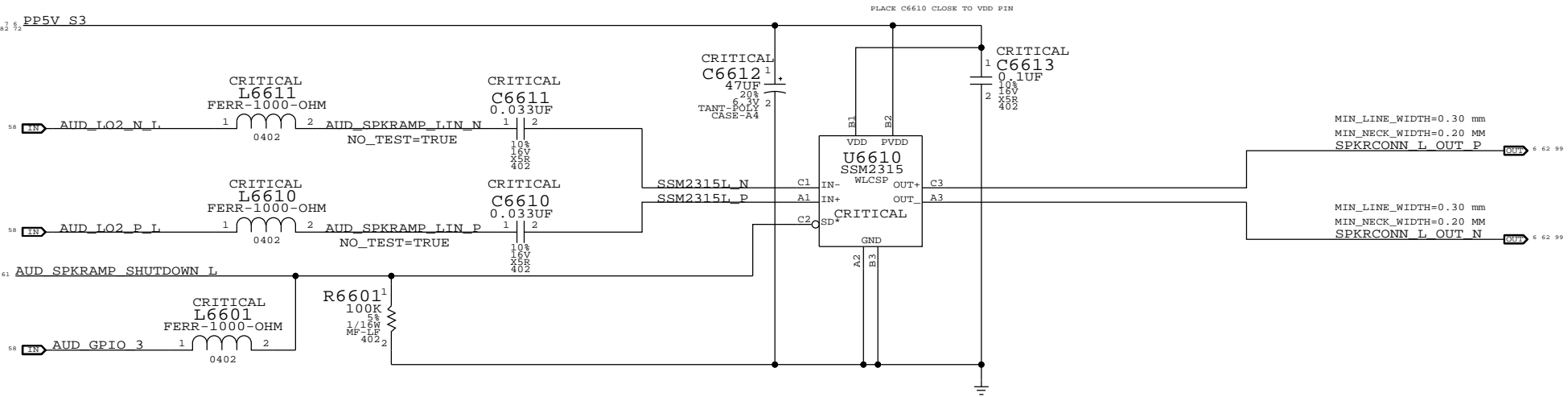
CODEC RIN = 20K OHMS
NET RIN = 18K OHMS
FC = 8 HZ
VIN = 2VRMS, CODEC VIN = 1.14 VRMS




ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER

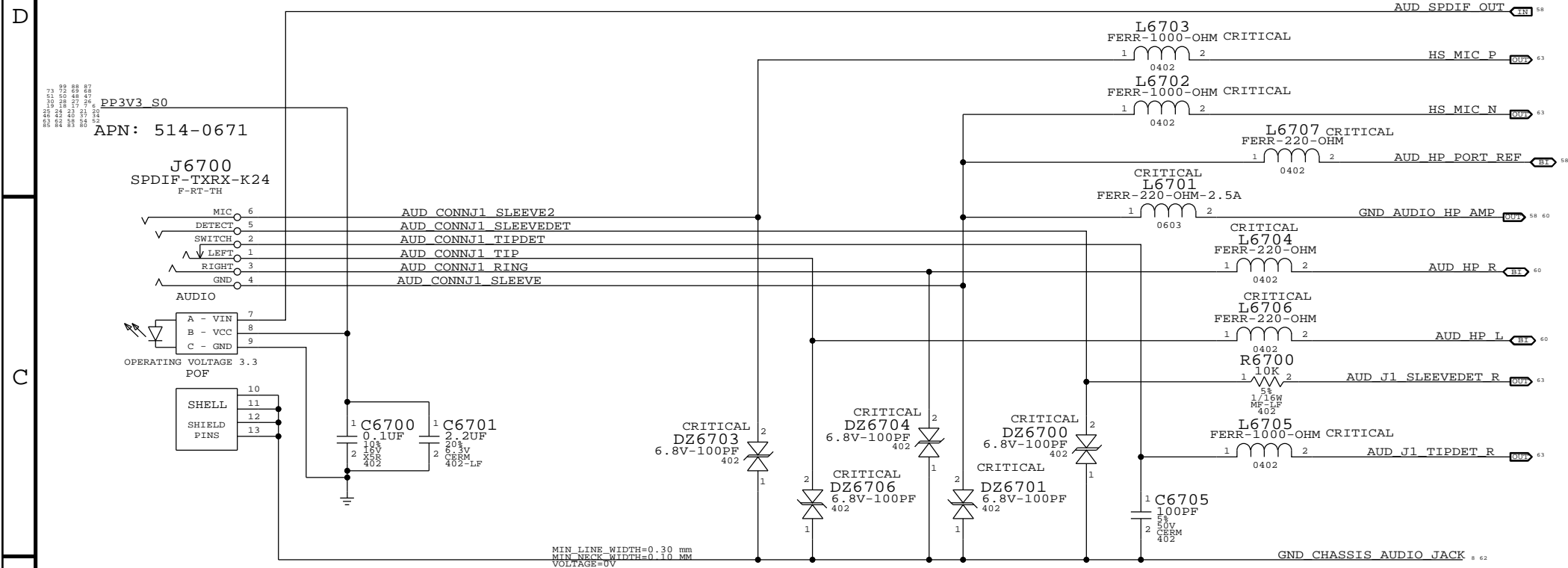


3X MONO SPEAKER AMPLIFIERS (SSM2315)
APN: 353S2500
GAIN = 6DB
1ST ORDER FC (L&R) = 120 HZ +/- 30%
1ST ORDER FC (SUB) = 58HZ +/- 30%

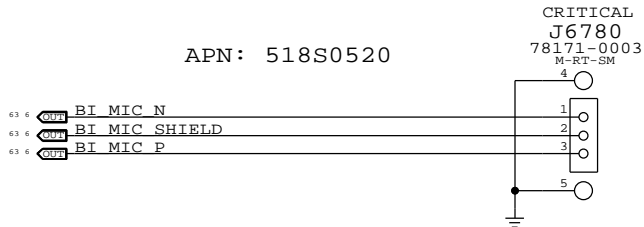


SYNC MASTER=K18 AUDIO		SYNC DATE=07/29/2009	
PAGE TITLE			
AUDIO: SPEAKER AMP			
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NOTICE OF PROPRIETARY PROPERTY:			
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PAGE		66 OF 132	
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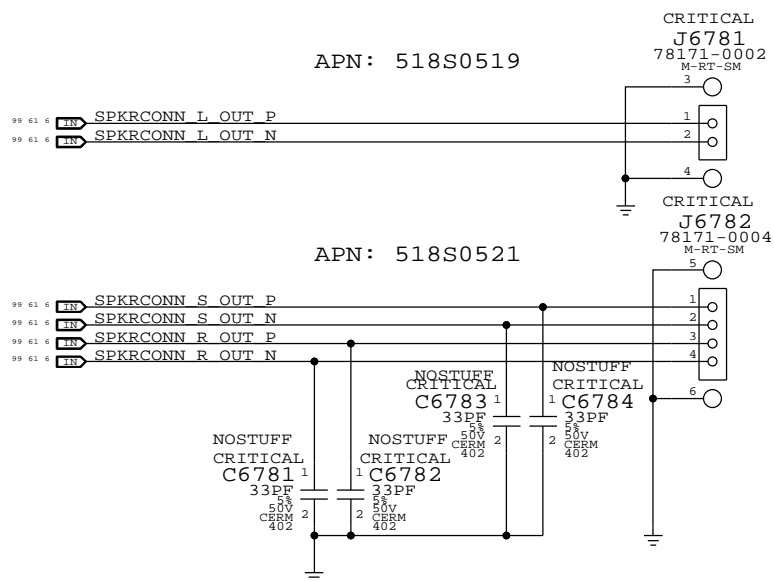
AUDIO JACK 1 LO/HP JACK, SPDIF TX



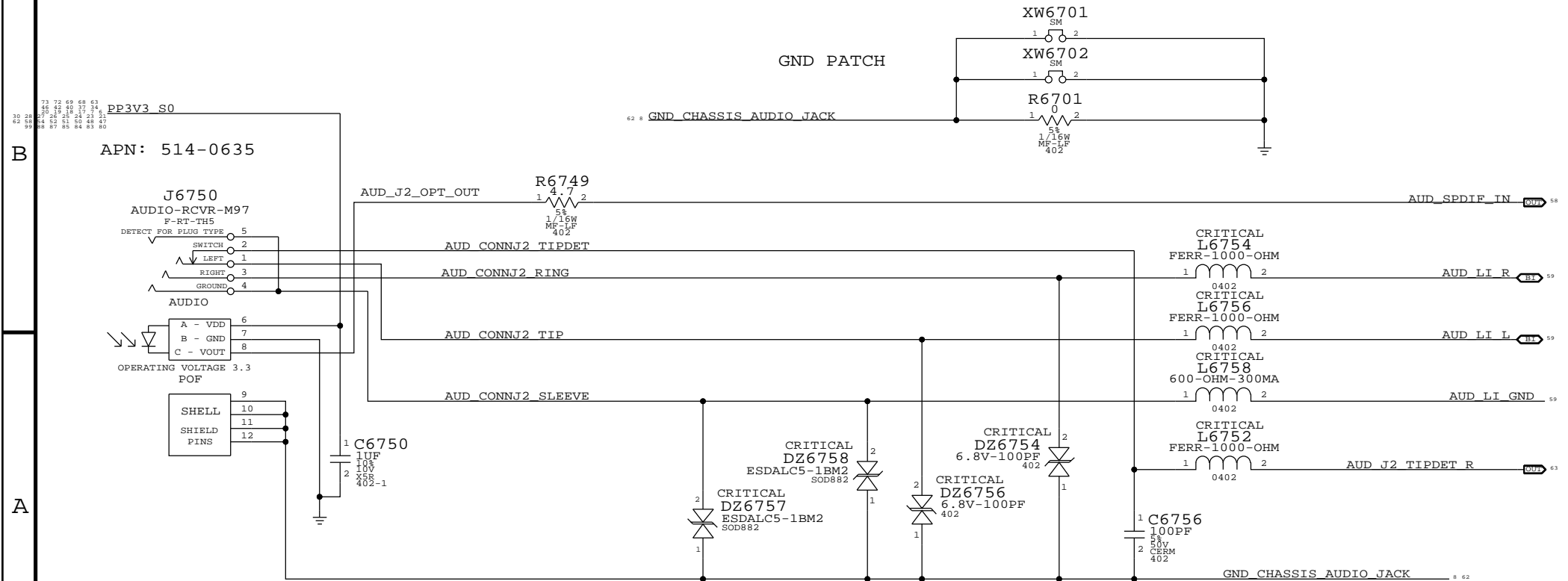
MIC CONNECTOR




SPEAKER CONNECTOR



AUDIO JACK 2 LINE IN JACK, SPDIF RX



SYNC MASTER=K18 AUDIO		SYNC DATE=07/29/2009	
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AUDIO: JACKS			
 Apple Inc.		DRAWING NUMBER	SIZE
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		BRANCH	
		<BRANCH>	
		PAGE	67 OF 132
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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	N/A	0X09 (A)
SATELLITES	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0C (B)

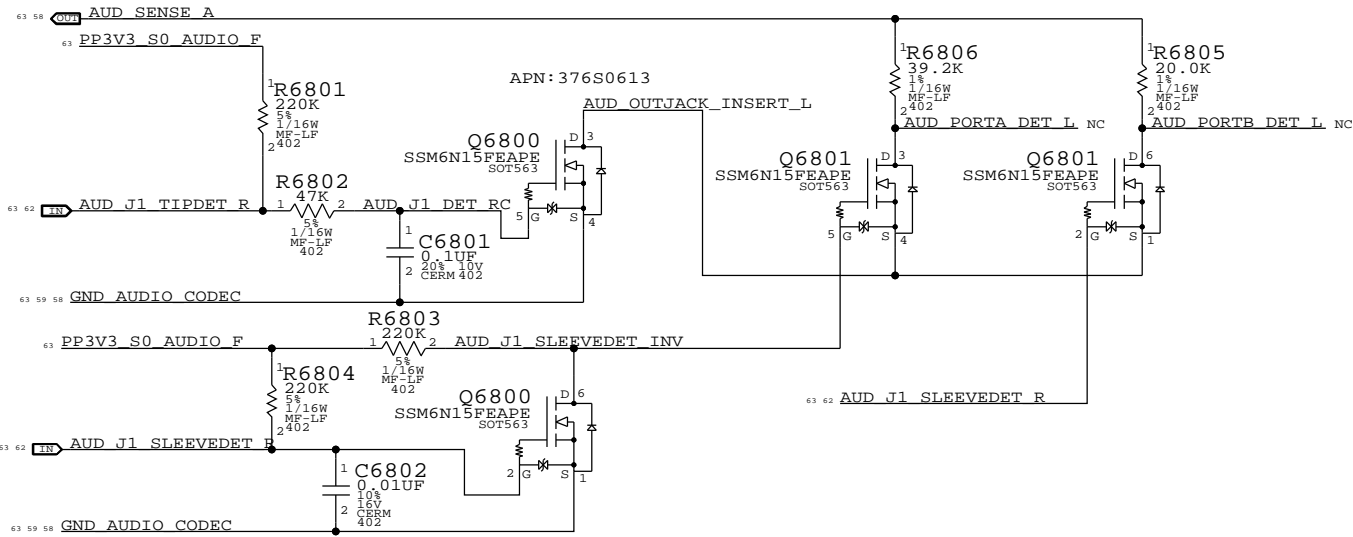
CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X05 (5)	0X0C (12,C)	N/A	0X0C (12,C)
SPDIF IN	0X07 (7)	0X0F (15)	N/A	N/A
BUILT-IN MIC	0X06 (6)	0X0D (13,B,RIGHT)	MIC_BIAS (80%)	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

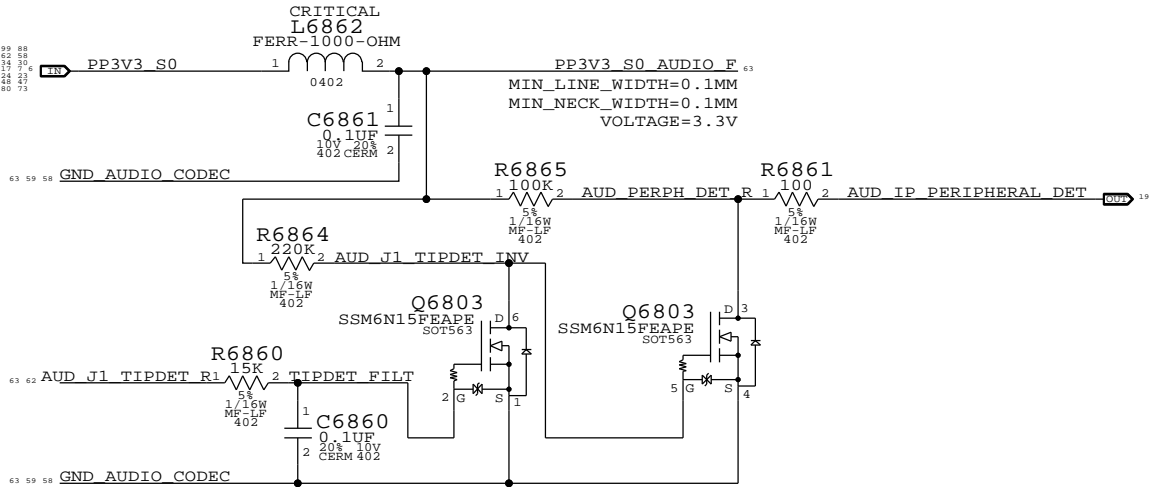
SYSTEM INT AND GPIO LINES

FUNCTION	INT	GPIO
MIKEY ENABLE		SATA4GP/GPIO 16
MIKEY INTERRUPT	PIRQ H	GPIO 5
PERIPHERAL DETECT	PIRQ F	GPIO 3

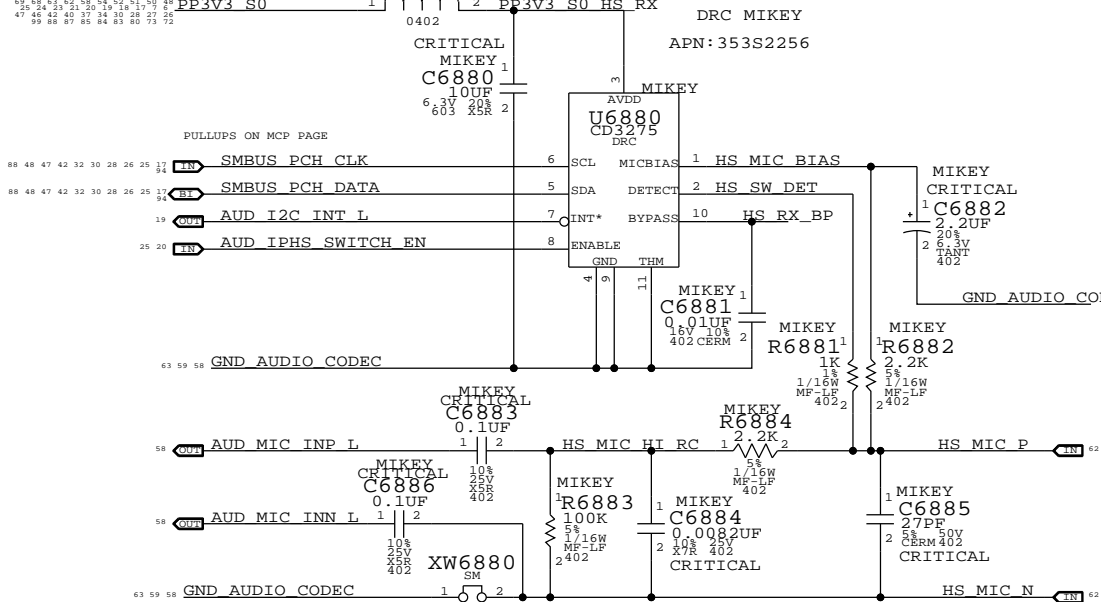
PORT A DETECT (HEADPHONES) PORT B DETECT (SPDIF DELEGATE)



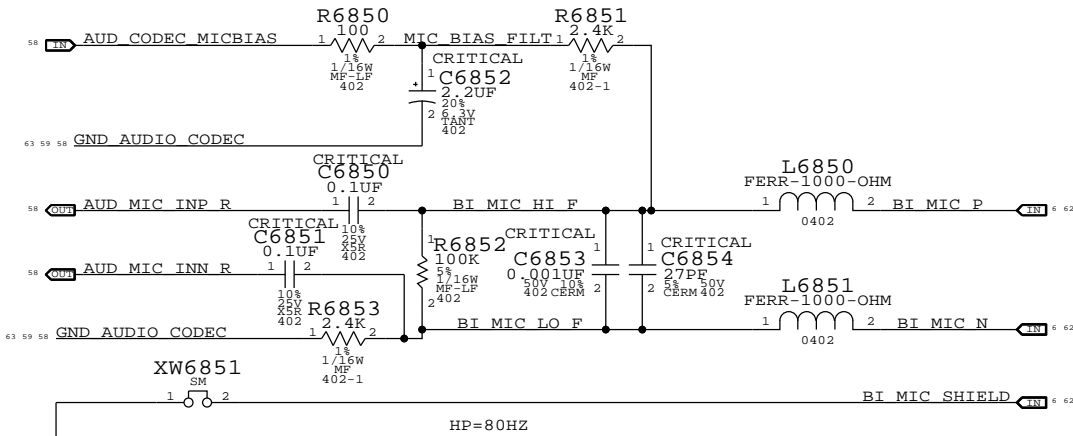
EXTRACTION NOTIFICATION



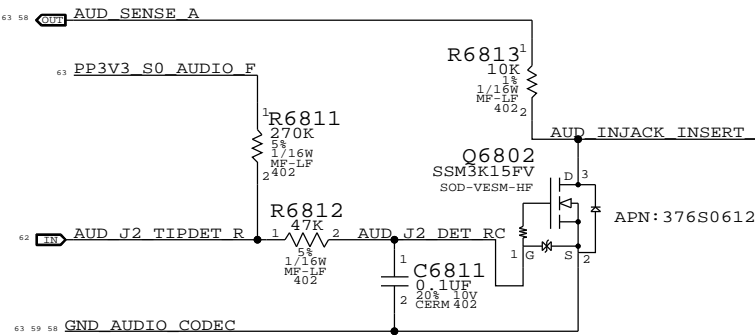
PORT B LEFT(HEADSET MIC)
CRITICAL HP=80HZ, LP=8.82KHZ
MIKEY MIN_LINE_WIDTH=0.1MM
L6880 MIN_NECK_WIDTH=0.1MM
FERR-1000-OHM VOLTAGE=3.3V



PORT B RIGHT(BUILT-IN MIC)



PORT C DETECT (LINE-IN)

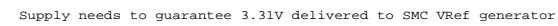


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D



BIL CONNECTOR




PPVBAT_G3H_CONN



1



SYNCH MASTER=K18 POWER		SYNCH DATE=06/30/2009	
PAGE TITLE			
PBus Supply & Battery Charger			
 Apple Inc.		DRAWING NUMBER <SCH NUM>	
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		REVISION <E4LABEL>	
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		PAGE 70 OF 132	
		SHEET 65 OF 101	

D

D

C

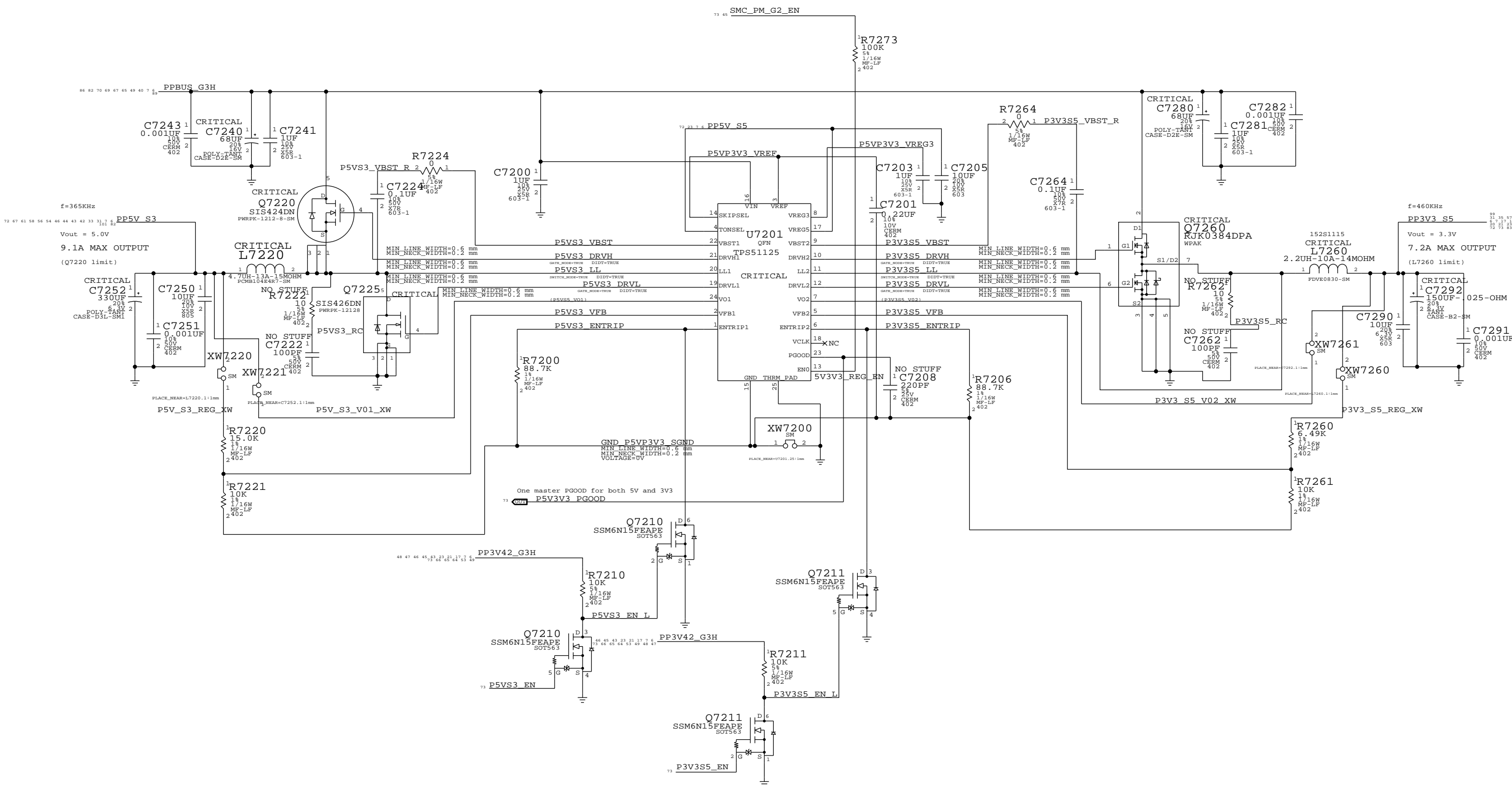
C


B

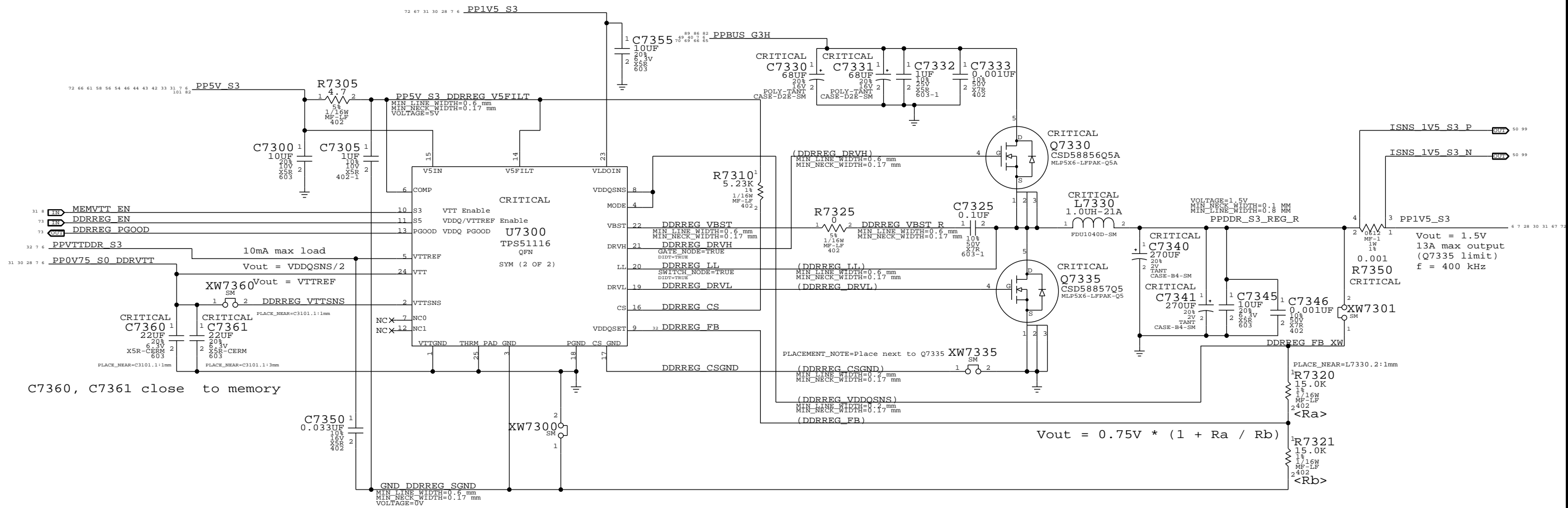
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A

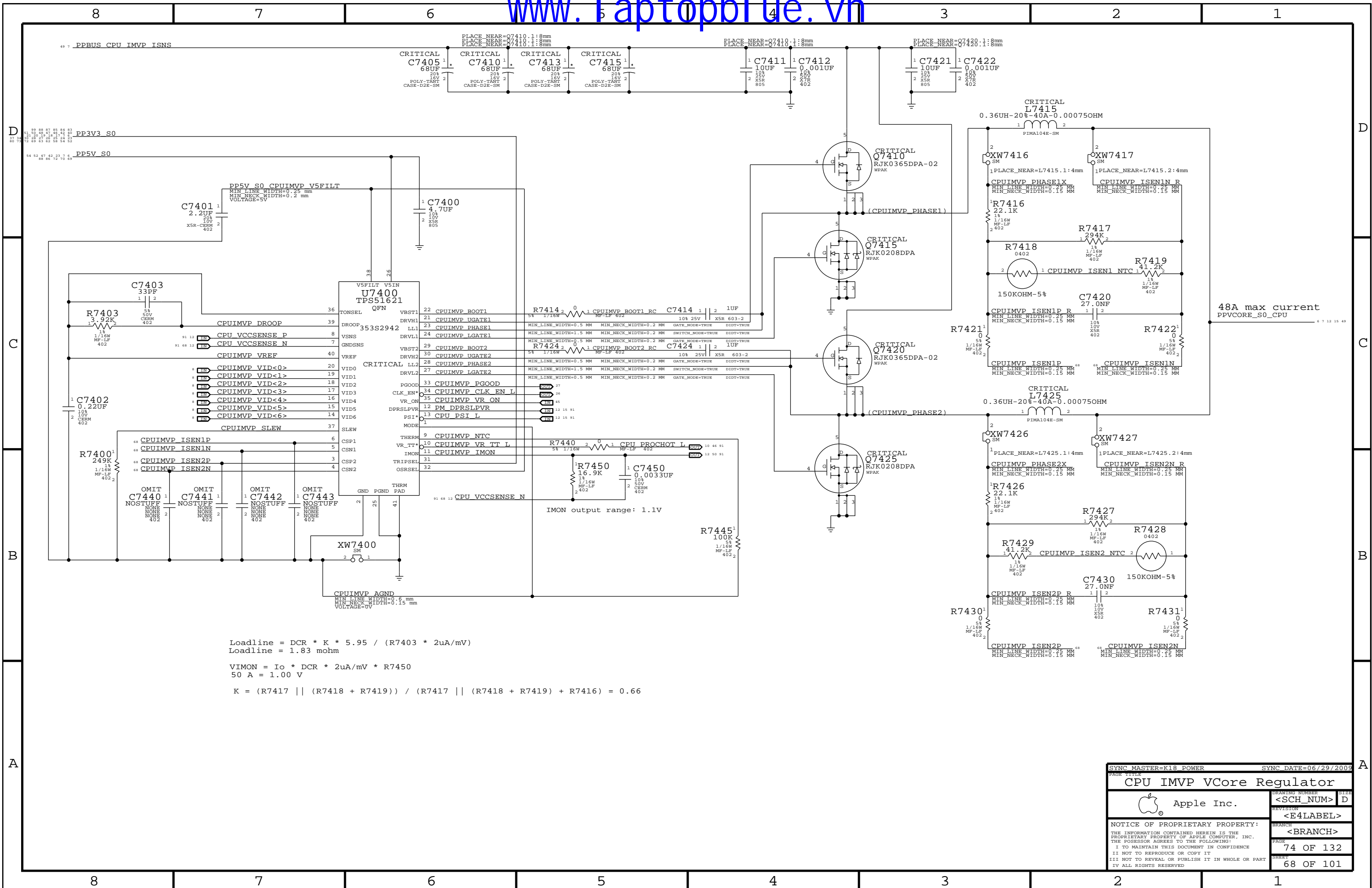
A



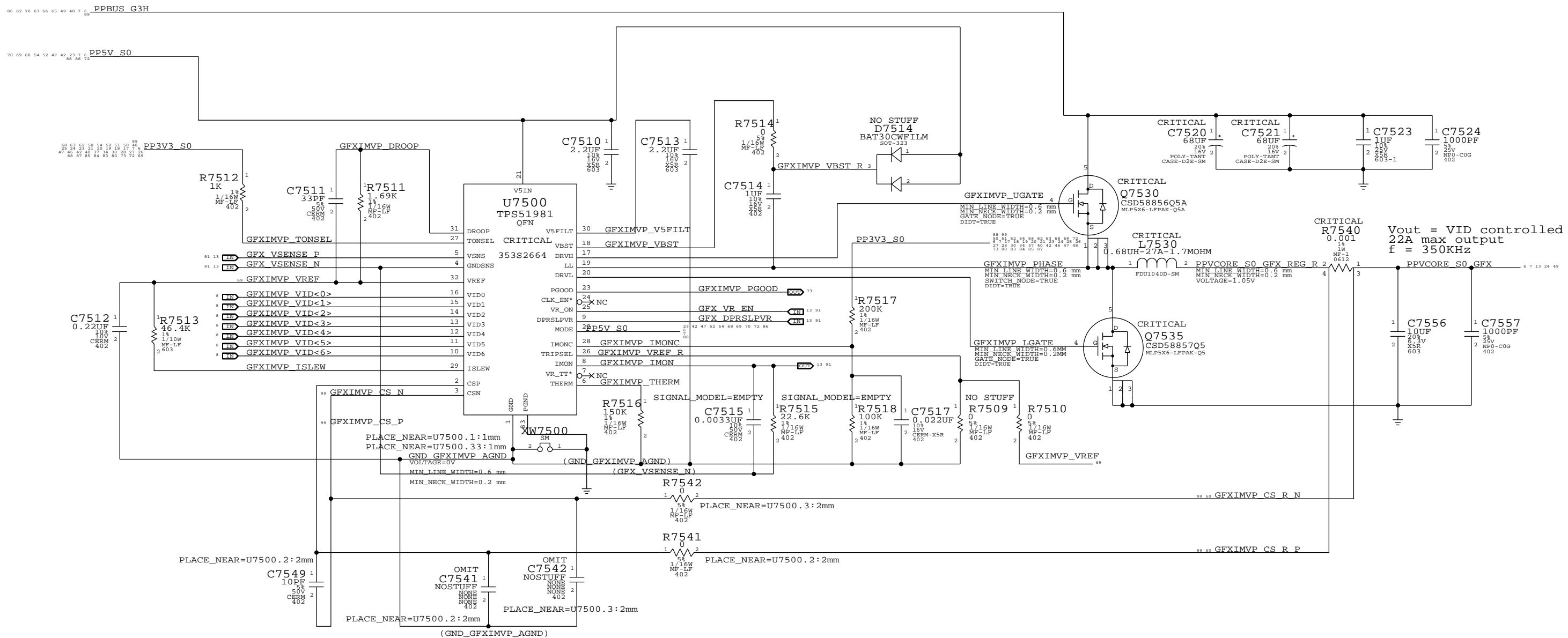
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PAGE TITLE			
5V / 3.3V Power Supply			
 Apple Inc.		DRAWING NUMBER	SIZE
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SYNC MASTER=K18 POWER		SYNC DATE=07/14/2009	
PAGE TITLE			
1.5V DDR3 Supply			
 Apple Inc.	DRAWING NUMBER		SIZE
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GFX IMVP VCore

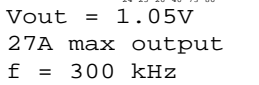



$$I_{mon} = I_o \times R7540 \times 2\mu A/mV \times R7515$$

$$I_{mon} = I_o \times 45.2mV/A$$

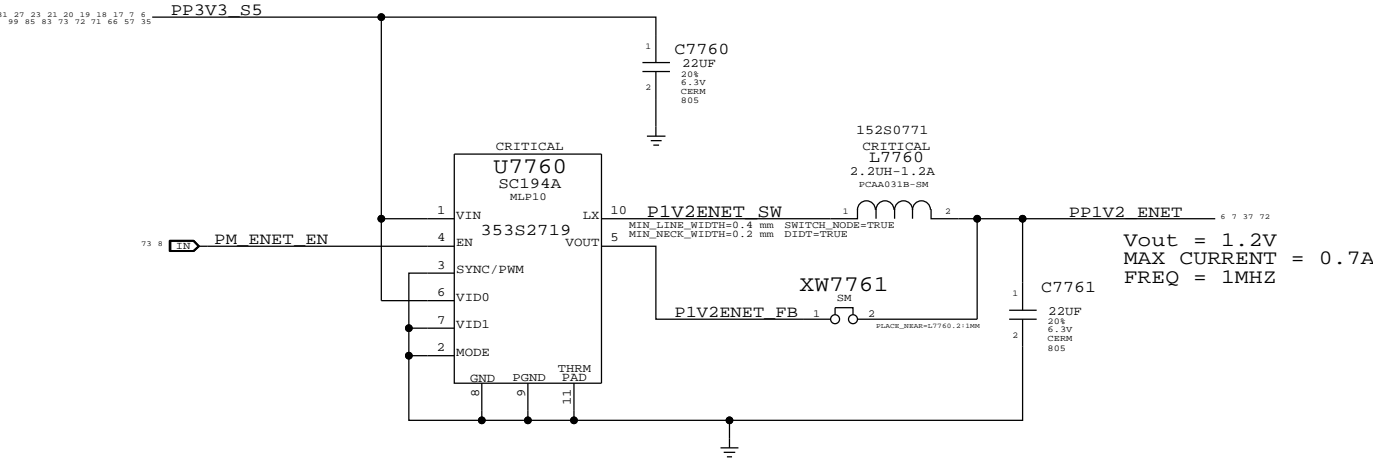
$$22A \Rightarrow 1V$$

SYNC MASTER=K18 POWER		SYNC DATE=07/08/2009	
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GFX IMVP VCore Regulator			
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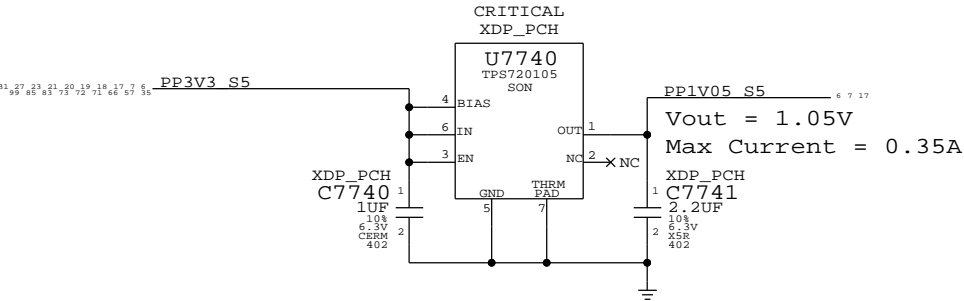
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PAGE TITLE			
CPUVTTT (1.05V) Power Supply			
		DRAWING NUMBER <SCH_NUM>	
Apple Inc.		SIZE D	
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1.2V S3 Regulator

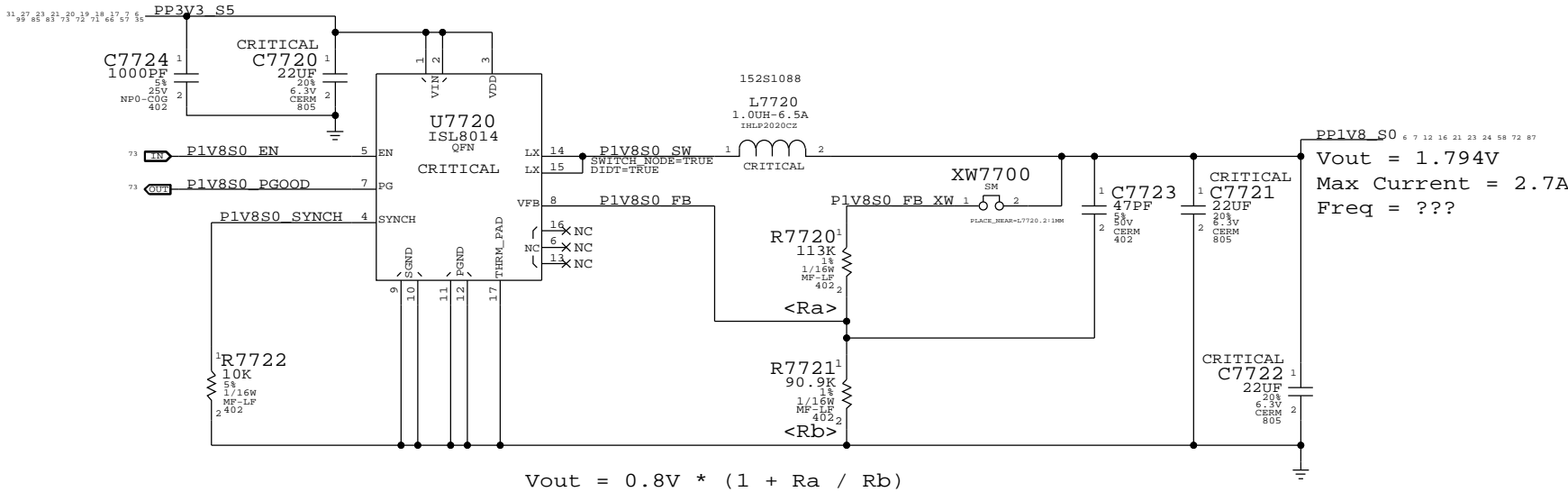


1.05V S5 LDO

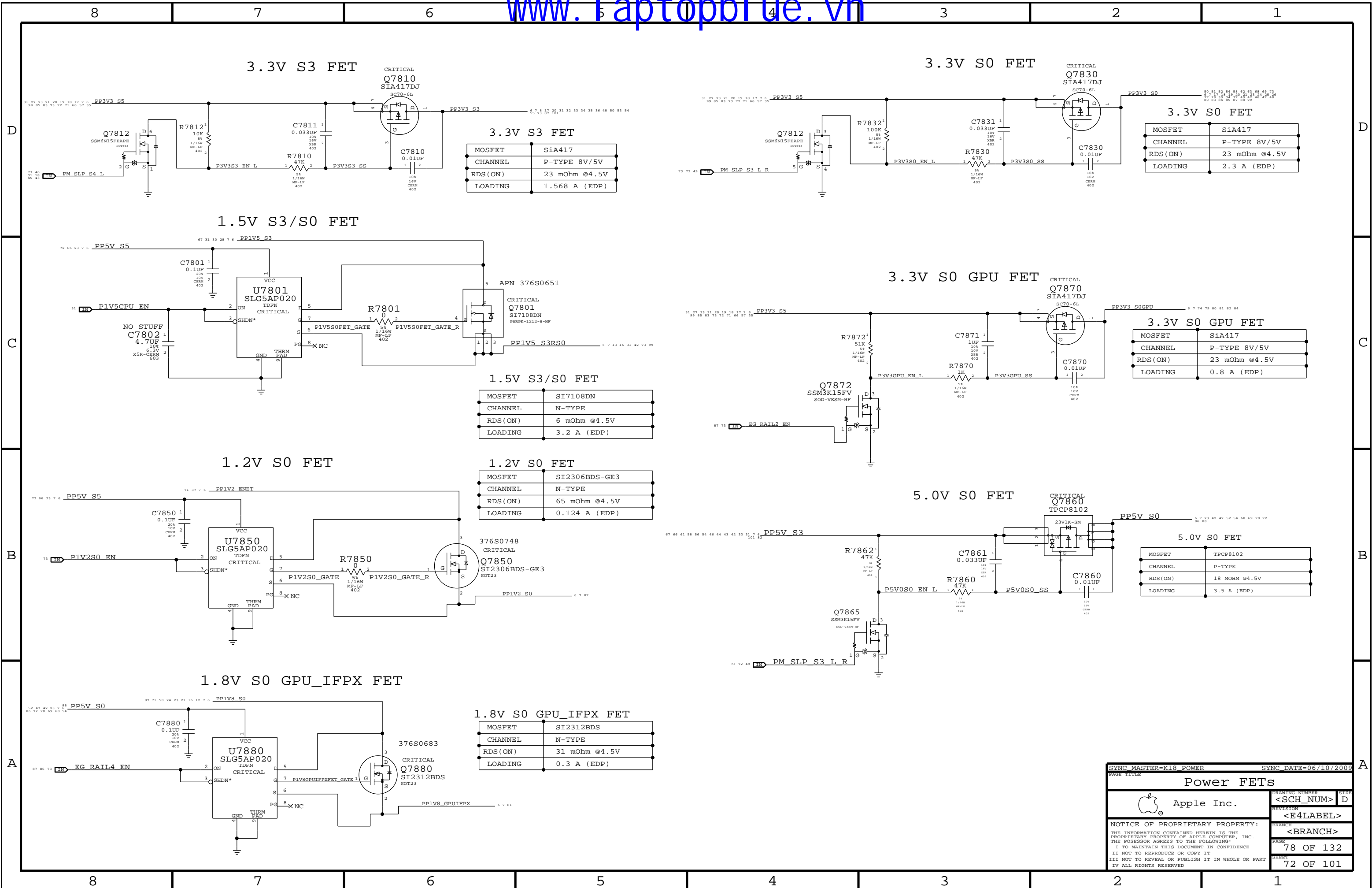
Ibex Peak-M requires JTAG pull-ups to be powered at 1.05V in S5. Pull-ups (3) must be 51 ohms to support XDP (not required in production). 70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



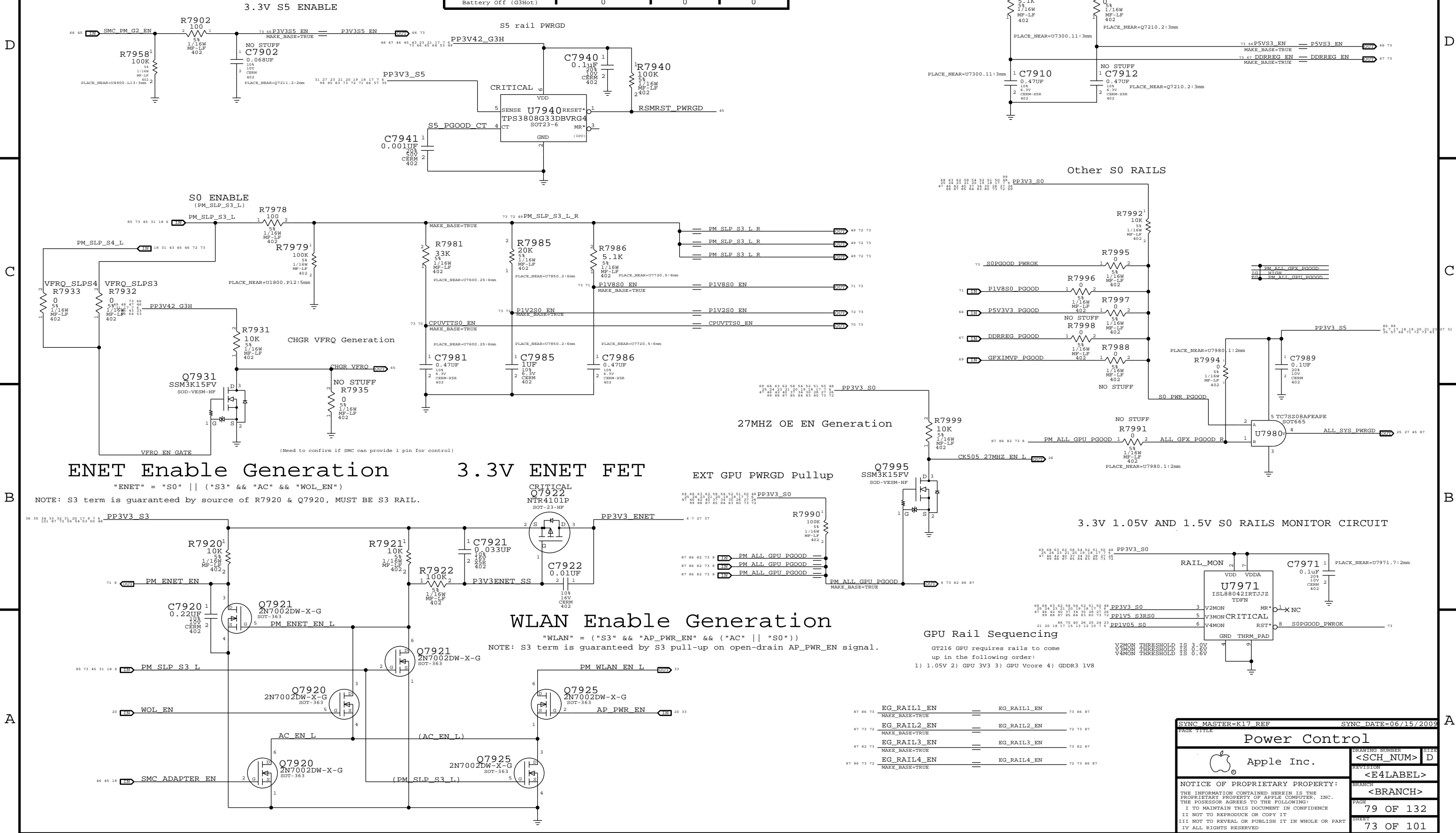
1.8V S0 Regulator



$$V_{out} = 0.8V * (1 + R_a / R_b)$$



State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0



Page Notes

Power aliases required by this page:

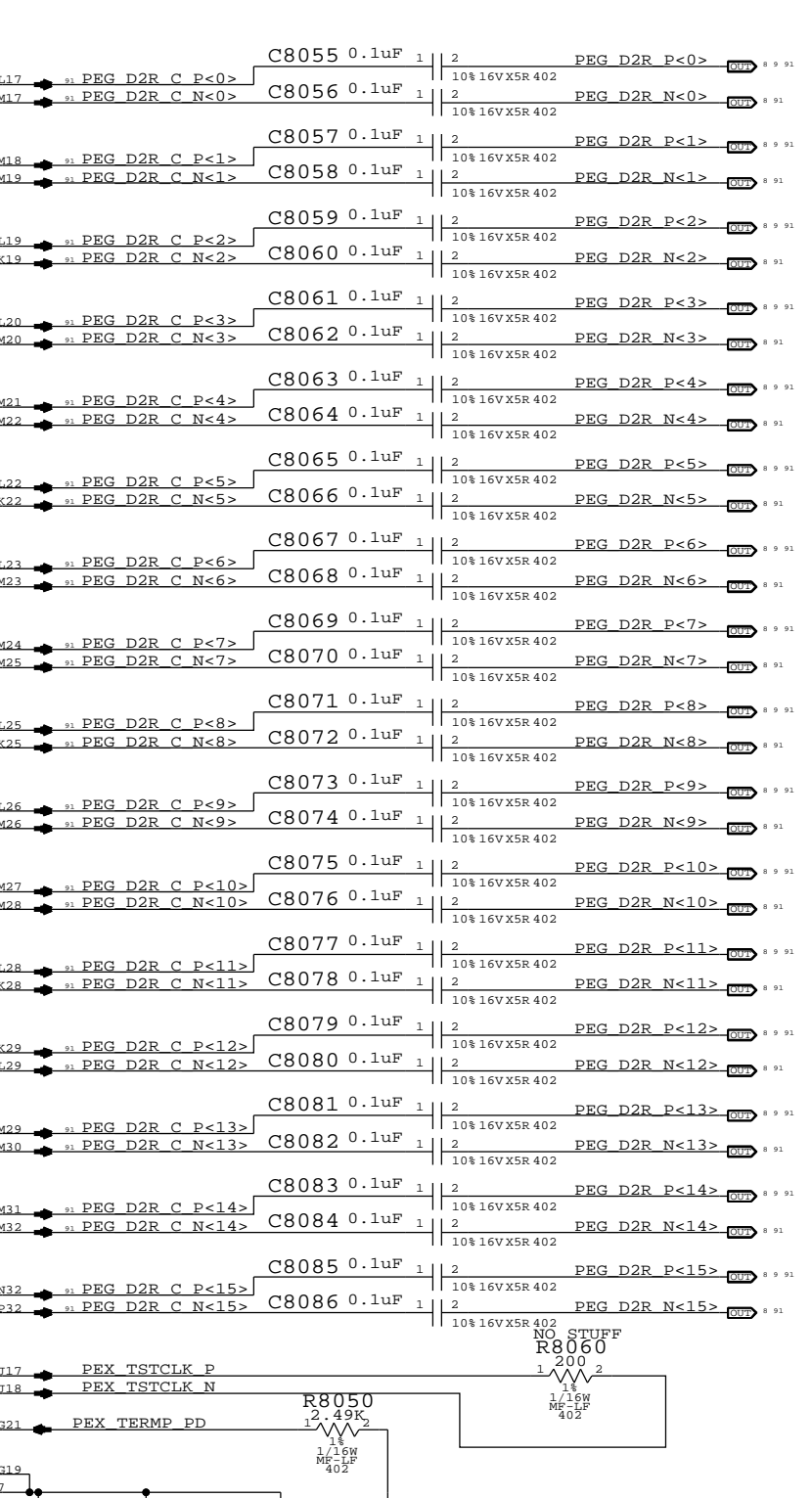
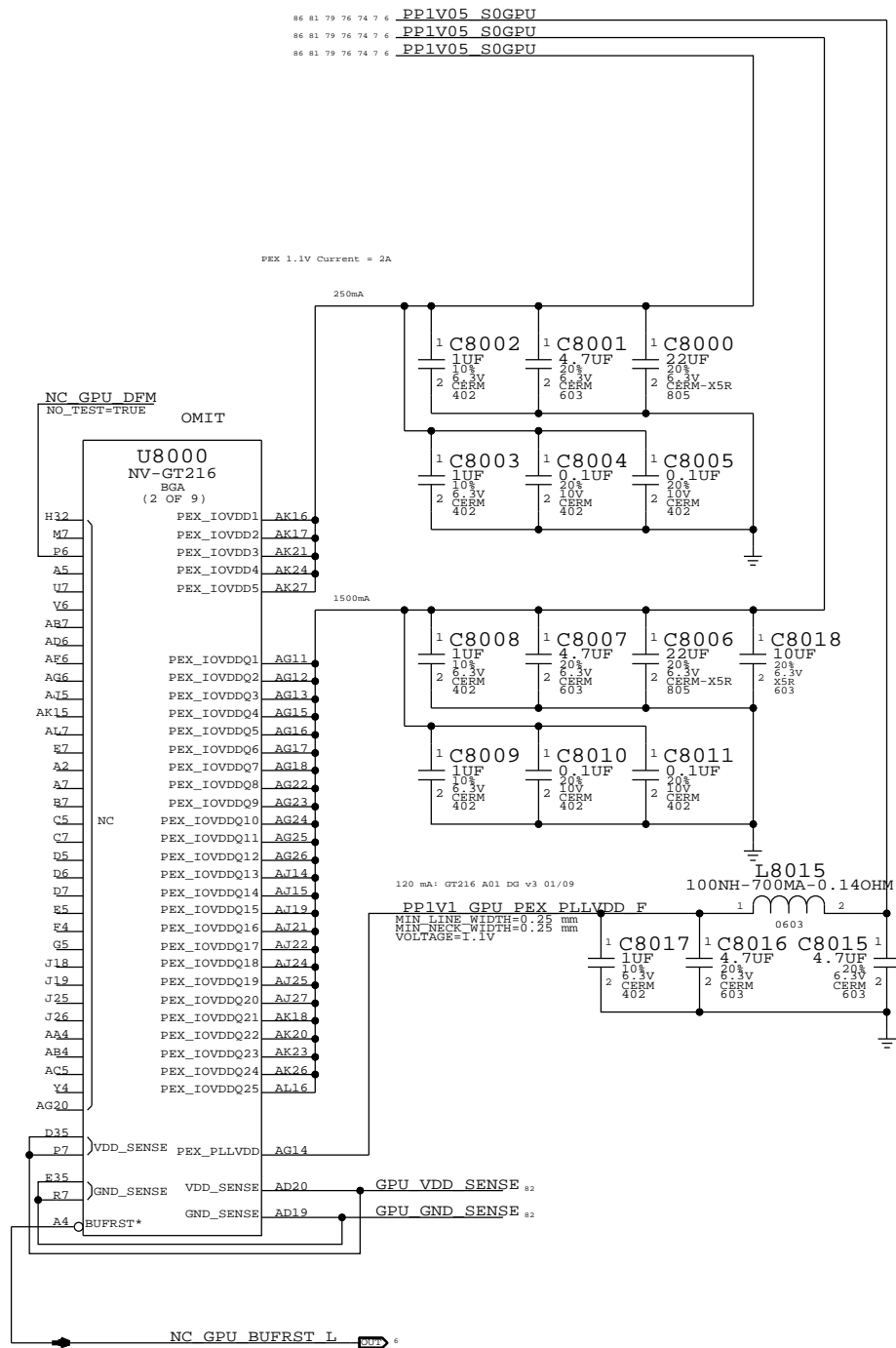
- =PP1V2_GPU_PEX_PL1XVDD
- =PP1V2_GPU_PEX_I0VDDQ
- =PP1V2_GPU_PEX_I0VDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)



SYNC MASTER=K17 REF		SYNC DATE=06/15/2009	
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Apple Inc.		DRAWING NUMBER	<SCH_NUM> D
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Page Notes

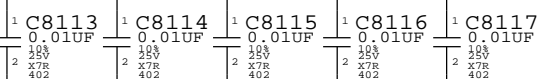
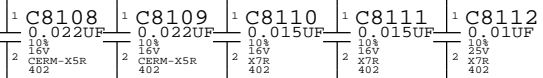
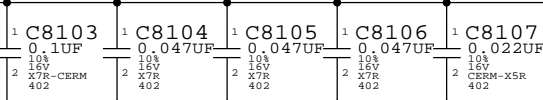
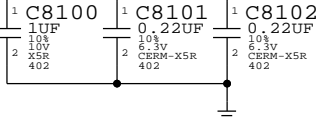
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- =PPVCORE_GPU
- =PPIV8_GPU_FBVDDQ

Signal aliases required by this page:
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BOM options provided by this page:
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PPVCORE_GPU

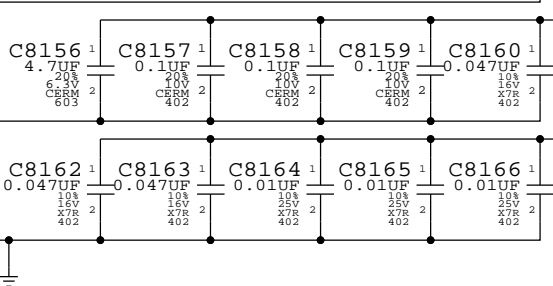
???A @ ???MHz Core/Mem Clk for VDD



PPIV8R1V55_S0GPU_ISNS

Nvidia PRD for GB-128 uses 4x4.7uF, 8x0.47uF, 16x0.1uF

???A @ ???MHz 1.8V GDDR3



U8000
NV-GT216
BGA
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OMIT

L11
L12
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L14
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L17
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L21
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M12
M14
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T12
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T22
T24
V11
V13
V15
V17

VDD

VDD

OMIT

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NV-GT216
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AC27
AD27
AE27
AT28
E21
G8
G9
G17
G18
G22
H29
J14
J15
J16

FBVDDQ

FBVDDQ

J20
J21
J22
J23
J24
J29
N27
P27
R27
T27
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U8000
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BGA
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OMIT

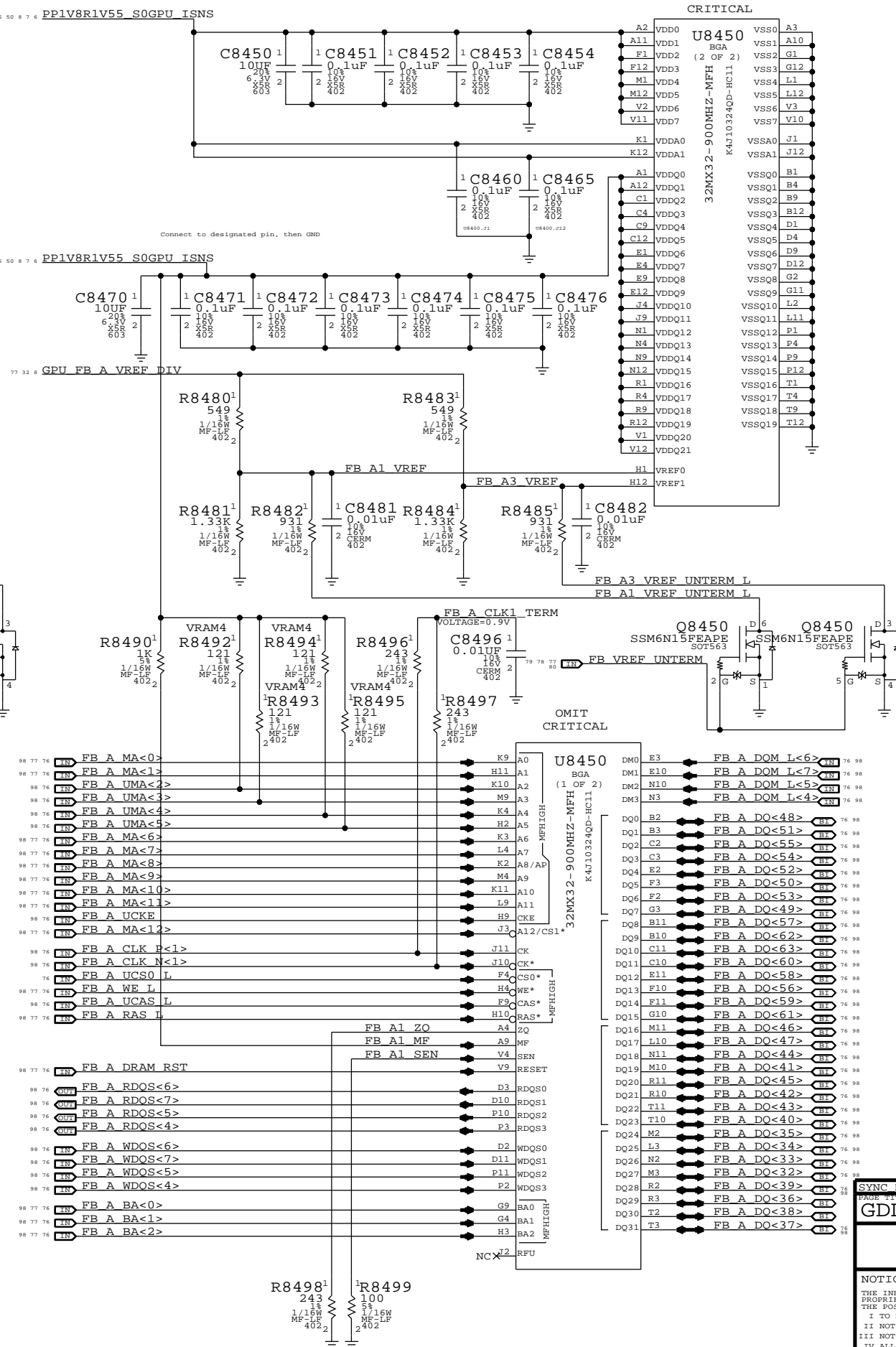
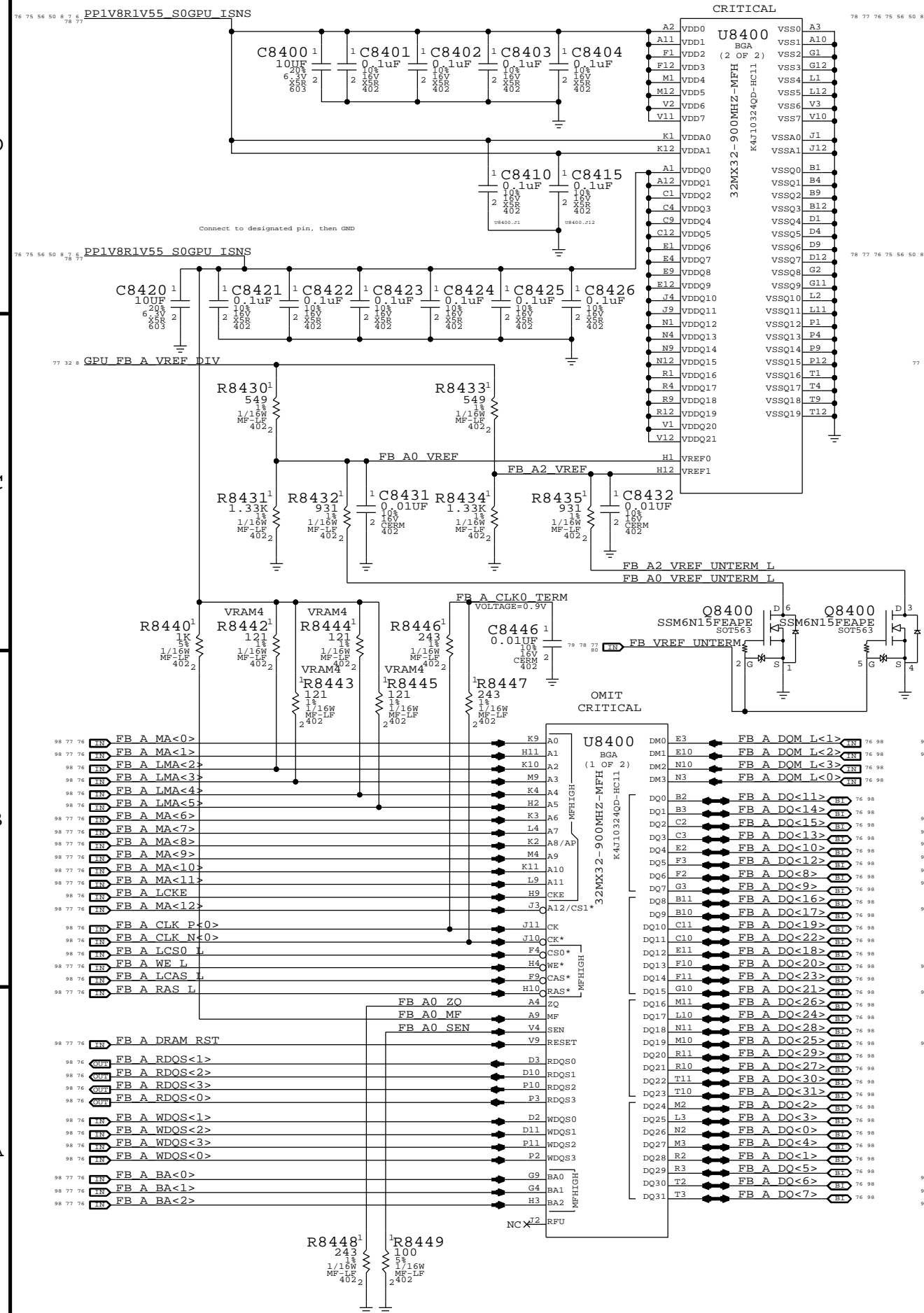
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U21
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U23
U24
U25
V2
V5
V9
V12
V14
V16


GND

GND

V18
V20
V22
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V31
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AL6
AL9
AL12
AL15
AL18
AL21
AL24
AL27
AL30
AN2
AN34
AP3
AP6
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AP15
AP18
AP21
AP24
AP27
AP30
K9
AK14

SYNC MASTER=K17 REF		SYNC DATE=06/15/2009	
PAGE TITLE			
NV GT216 CORE/FB POWER			
 Apple Inc.		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
		REVISION	
		<E4LABEL>	
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SYNCH MASTER-K17 REF		SYNCH DATE=06/15/2009	
PART TITLE		DRAWING NUMBER	
GDDR3 Frame Buffer A (Top)		<SCH_NUM>	
 Apple Inc.		SIZE	
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Power aliases required by this page:
- PPIV8_S0_FB_VDD
- PPIV8_S0_FB_VREF_B
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
VRAM4

PP1V8R1V55 S0GPU ISNS

PP1V8R1V55 S0GPU ISNS

PP1V8R1V55 S0GPU ISNS

PP1V8R1V55 S0GPU ISNS

PP1V8R1V55 S0GPU ISNS

PP1V8R1V55 S0GPU ISNS

GPU FB B VREF DIV

GPU FB B VREF DIV

GPU FB B VREF DIV

FB B MA<0>

FB B MA<0>

FB B MA<0>

FB B MA<1>

FB B MA<1>

FB B MA<1>

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FB B LMA<2>

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FB B MA<11>

FB B LCKE

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FB B WE L

FB B WE L

FB B WE L

FB B LCAS L

FB B LCAS L

FB B LCAS L

FB B RAS L

FB B RAS L

FB B RAS L

FB B DRAM RST

FB B DRAM RST

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FB B BA<0>

FB B BA<0>

FB B BA<1>

FB B BA<1>

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FB B BA<2>

FB B BA<2>

FB B BA<2>

Page Notes

Power aliases required by this page:

- =PP3V3_GPU_VDD33
- =PP3V3_GPU_MIO
- =PP1V2_GPU_PLLVDD
- =PP1V2_GPU_M_PLLVDD
- =PP1V2_GPU_VID_PLLVDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

110mA

OMIT

U8000
NV-GT216
BGA
(6 OF 9)

GPIO0	K1	GPU VCORE VID3	80 82
GPIO1	K2	DP EG HPD	80 84
GPIO2	K3	GPU VCORE VID4	80 82
GPIO3	H3	EG LCD PWR EN	80 87
GPIO4	H2	EG BKLT EN	80 87
GPIO5	H1	GPU VCORE VID0	80 82
GPIO6	H4	GPU VCORE VID1	80 82
GPIO7	H5	GPU VCORE VID2	80 82
GPIO8	H6	SMC GFX OVERTEMP R	80 80
GPIO9	J7	TP GPU GSTATE<0>	77 78 80
GPIO10	K4	FB VREF UNTERM	80 80
GPIO11	K5	GPU GPIO 11	80 80
GPIO12	H7	SMC GFX THROTTLE P	80 80
GPIO13	J4	FBVDD ALTVO	80 86
GPIO14	J6	NC GPU GPIO 14	80 80
GPIO15	L1	NC GPU GPIO 15	80 80
GPIO16	L2	GPU GPIO 16	80 80
GPIO17	L4	NC GPU GPIO 17	80 80
GPIO18	M4	NC GPU GPIO 18	80 80
GPIO19	L7	NC GPU GPIO 19	80 80
GPIO20	L5	NC GPU GPIO 20	80 80
GPIO21	K6	NC GPU GPIO 21	80 80
GPIO22	L6	NC GPU GPIO 22	80 80
GPIO23	M6	NC GPU GPIO 23	80 80

JTAG_TCK	AP14	TP GPU JTAG TCK	80 80
JTAG_TDI	AN14	TP GPU JTAG TDI	80 80
JTAG_TDO	AN16	TP GPU JTAG TDO	80 80
JTAG_TMS	AR14	TP GPU JTAG TMS	80 80
JTAG_TRST*	AP16	TP GPU JTAG TRST	80 80
MIOA_CLKIN	N4	NC GPU MIOA CLKIN	80 80
MIOA_CLKOUT	R4	NC GPU MIOA CLKOUT	80 80
MIOA_CLKOUT*	T4	NC GPU MIOA CLKOUT	80 80
MIOA_CTL3	P5	NC GPU MIOA CTL3	80 80
MIOA_DE	N2	TP GPU MIOA DE	80 80
MIOA_D0	N1	TP GPU MIOA D<0>	80 80
MIOA_D1	P4	TP GPU MIOA D<1>	80 80
MIOA_D2	P1	TP GPU MIOA D<2>	80 80
MIOA_D3	P2	TP GPU MIOA D<3>	80 80
MIOA_D4	P3	TP GPU MIOA D<4>	80 80
MIOA_D5	T3	TP GPU MIOA D<5>	80 80
MIOA_D6	T2	TP GPU MIOA D<6>	80 80
MIOA_D7	T1	TP GPU MIOA D<7>	80 80
MIOA_D8	U4	TP GPU MIOA D<8>	80 80
MIOA_D9	U1	TP GPU MIOA D<9>	80 80
MIOA_D10	U2	GPU MIOA D<10>	80 80
MIOA_D11	U3	GPU MIOA D<11>	80 80
MIOA_D12	R6	GPU MIOA D<12>	80 80
MIOA_D13	T6	GPU MIOA D<13>	80 80
MIOA_D14	N6	GPU MIOA D<14>	80 80
MIOA_HSYNC	N3	NC GPU MIOA HSYNC	80 80
MIOA_VSYNC	L3	NC GPU MIOA VSYNC	80 80
MIOB_CLKIN	AE1	NC GPU MIOB CLKIN	80 80
MIOB_CLKOUT	V4	NC GPU MIOB CLKOUT	80 80
MIOB_CLKOUT*	M4	NC GPU MIOB CLKOUT	80 80
MIOB_CTL3	W3	NC GPU MIOB CTL3	80 80
MIOB_DE	Y5	NC GPU MIOB DE	80 80
MIOB_D0	Y1	NC GPU MIOB D<0>	80 80
MIOB_D1	Y2	NC GPU MIOB D<1>	80 80
MIOB_D2	Y3	NC GPU MIOB D<2>	80 80
MIOB_D3	AB3	NC GPU MIOB D<3>	80 80
MIOB_D4	AB2	NC GPU MIOB D<4>	80 80
MIOB_D5	AB1	NC GPU MIOB D<5>	80 80
MIOB_D6	AC4	NC GPU MIOB D<6>	80 80
MIOB_D7	AC1	NC GPU MIOB D<7>	80 80
MIOB_D8	AC2	NC GPU MIOB D<8>	80 80
MIOB_D9	AC3	NC GPU MIOB D<9>	80 80
MIOB_D10	AE3	NC GPU MIOB D<10>	80 80
MIOB_D11	AE2	NC GPU MIOB D<11>	80 80
MIOB_D12	U6	NC GPU MIOB D<12>	80 80
MIOB_D13	W6	NC GPU MIOB D<13>	80 80
MIOB_D14	Y6	NC GPU MIOB D<14>	80 80

MIOB_HSYNC	W1	NC GPU MIOB HSYNC	80 80
MIOB_VSYNC	W2	NC GPU MIOB VSYNC	80 80
THERMDP	B5	GPU TDIODE P	81 80 99
THERMDN	B4	GPU TDIODE N	80 81 99

SYNC MASTER=K17 REF SYNC DATE=06/15/2009

PAGE TITLE NV GT216 GPIO/MIO/MISC



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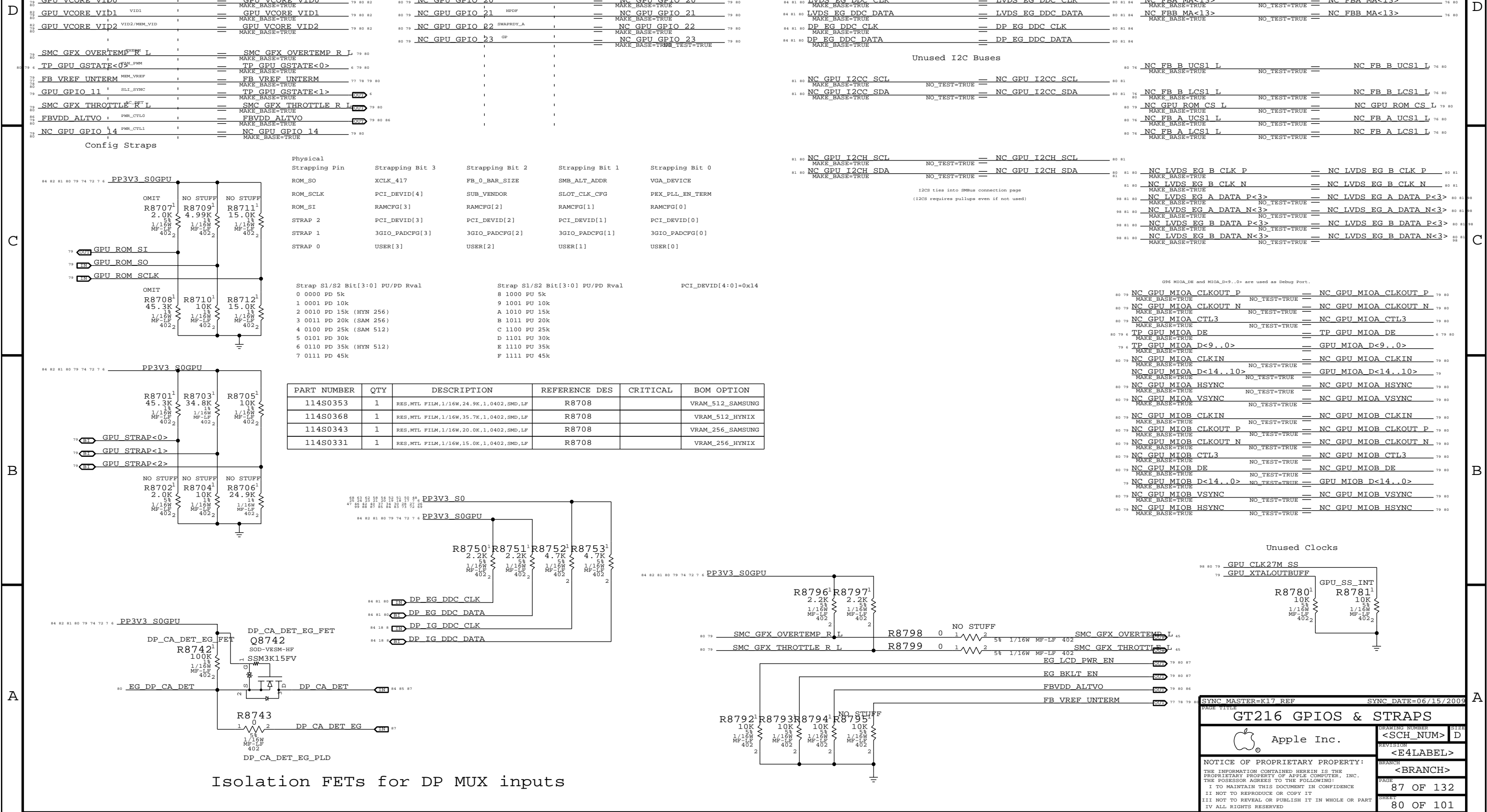
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Page Notes

Power aliases required by this page:

- =PP1V8_GPU_IFPX

- =PP3V3_GPU_IFPCD_IOVDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

Sum of peak currents: 240mA

72 7 6 PP1V8_GPUIFPX

CRITICAL

L8800

300-OHM-0.5A

7mA peak per diff pair

7mA peak for all pairs

0603-1

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L8805

180-OHM-1.5A

80mA peak

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L8810

180-OHM-1.5A

7mA peak per diff pair

7mA peak for all pairs

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L8815

300-OHM-0.5A

160mA peak

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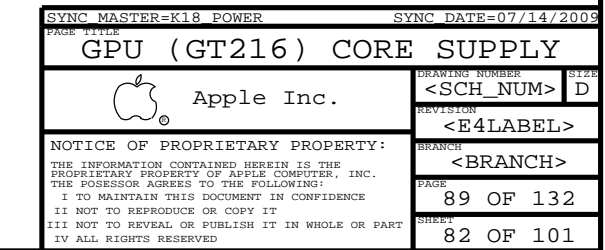
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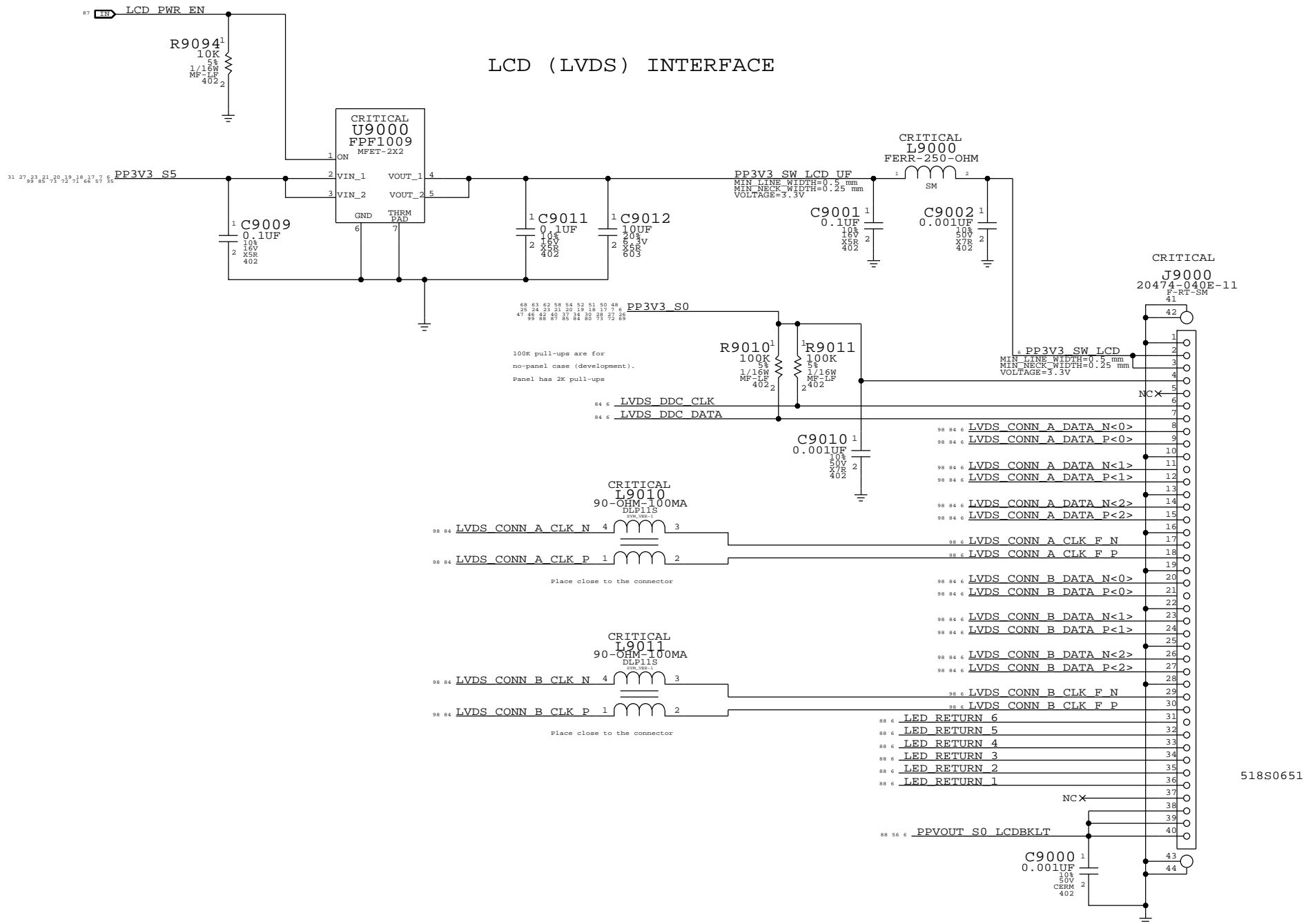
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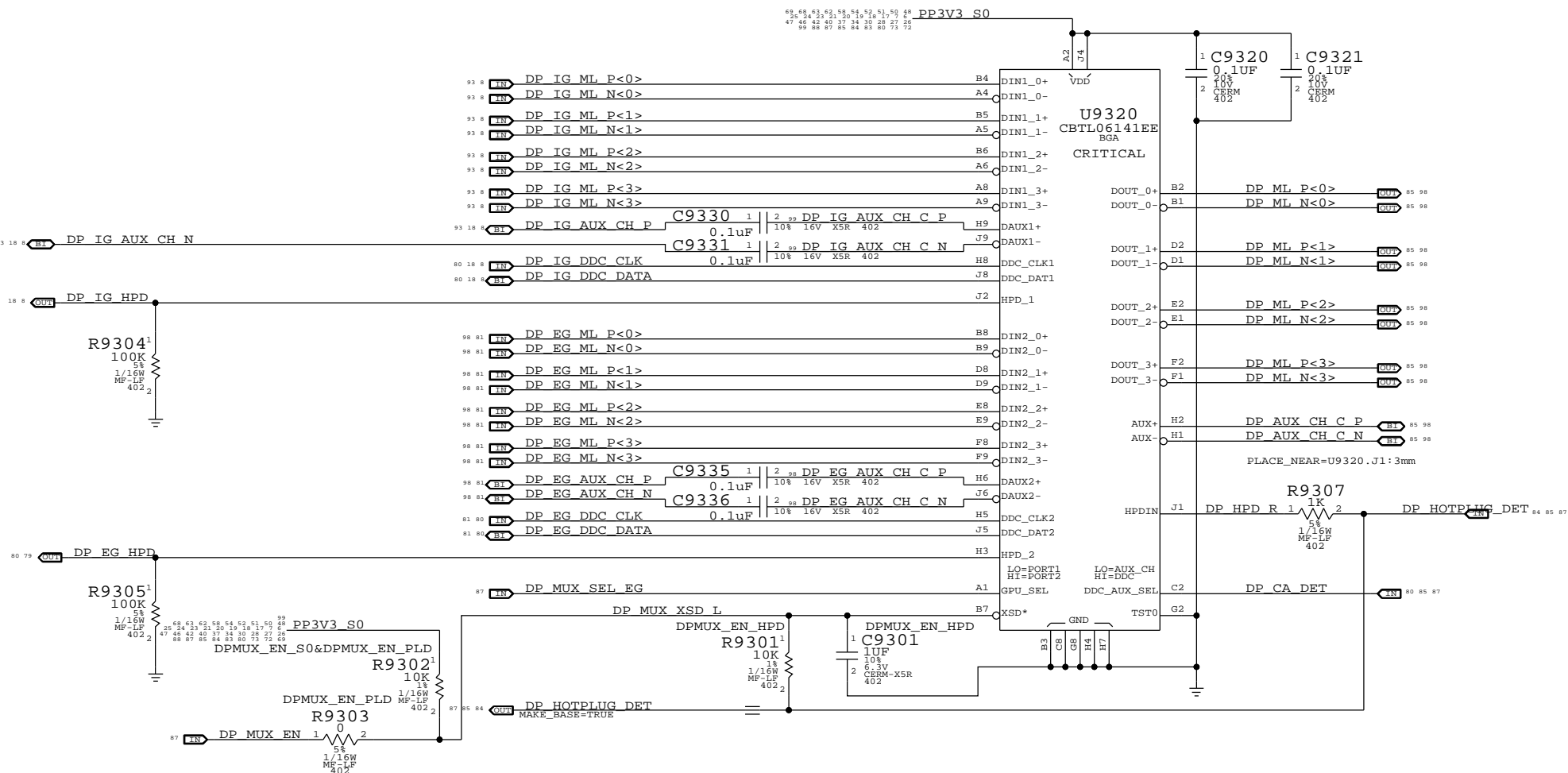


LVDS Transmitter Termination

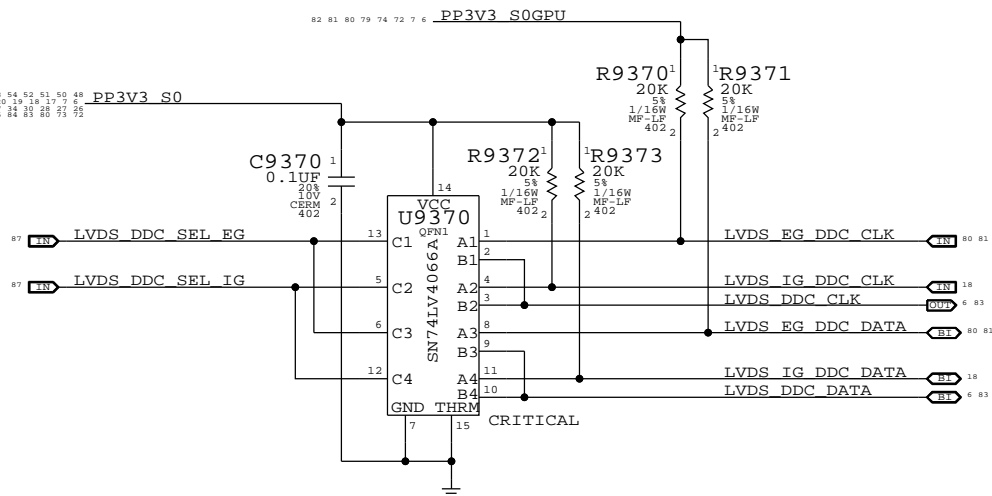
All emulated LVDS outputs require this termination




DisplayPort Mux

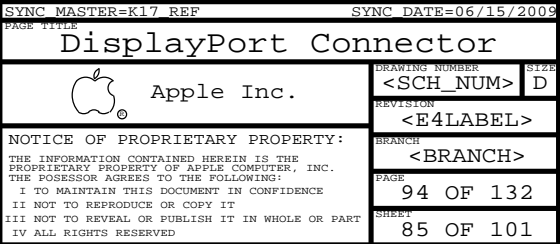


LVDS DDC MUX

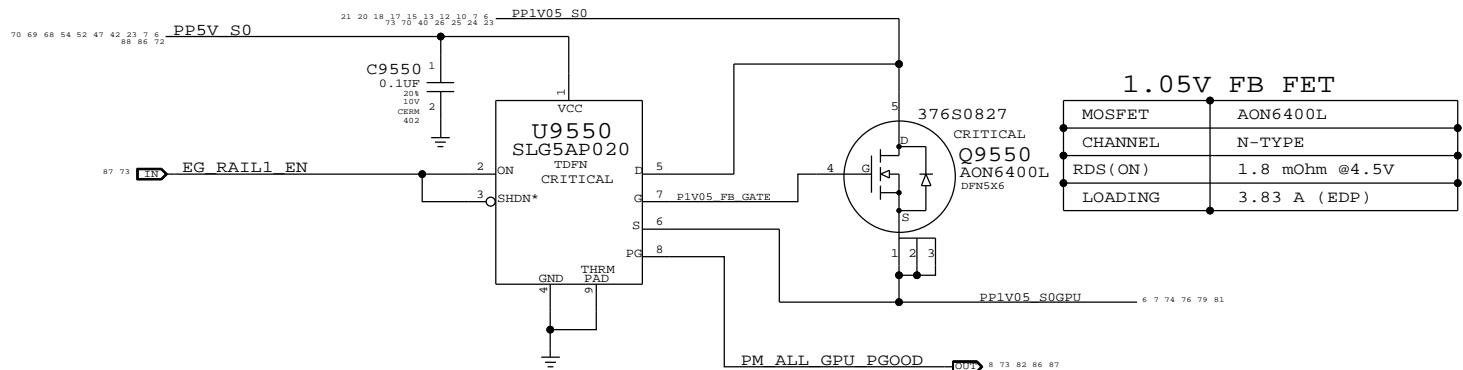


SYNC MASTER=K17 REF		SYNC DATE=06/15/2009	
PAGE TITLE			
Muxed Graphics		Support	
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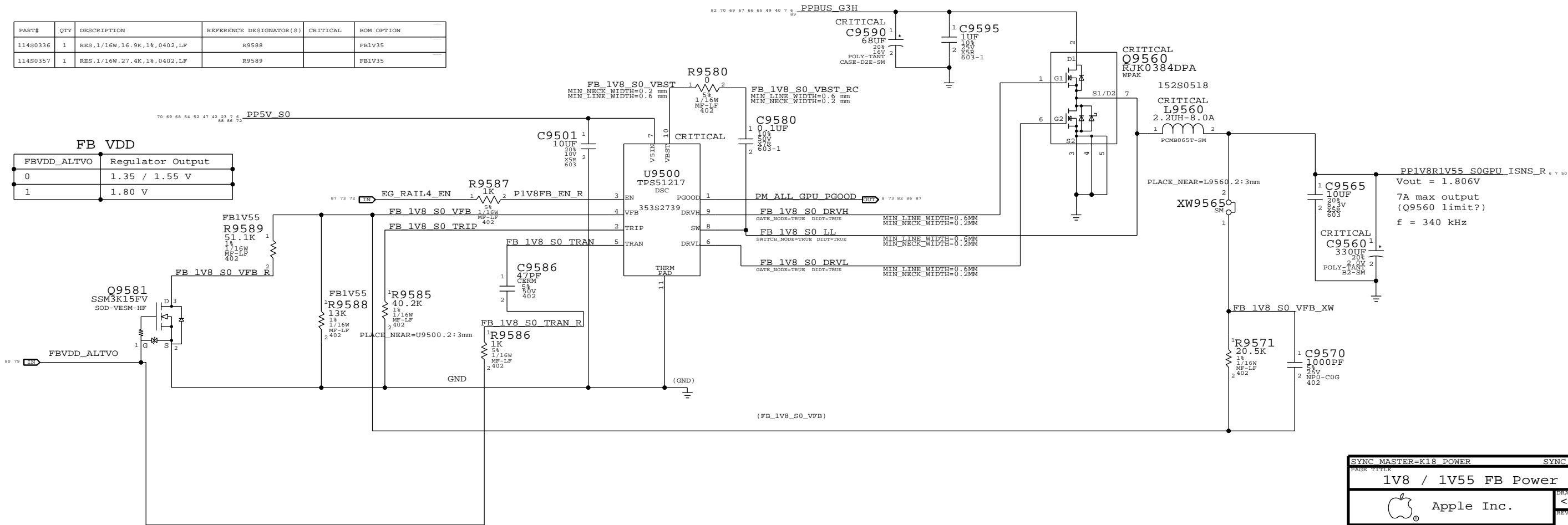
1V05 S0 GPU FET




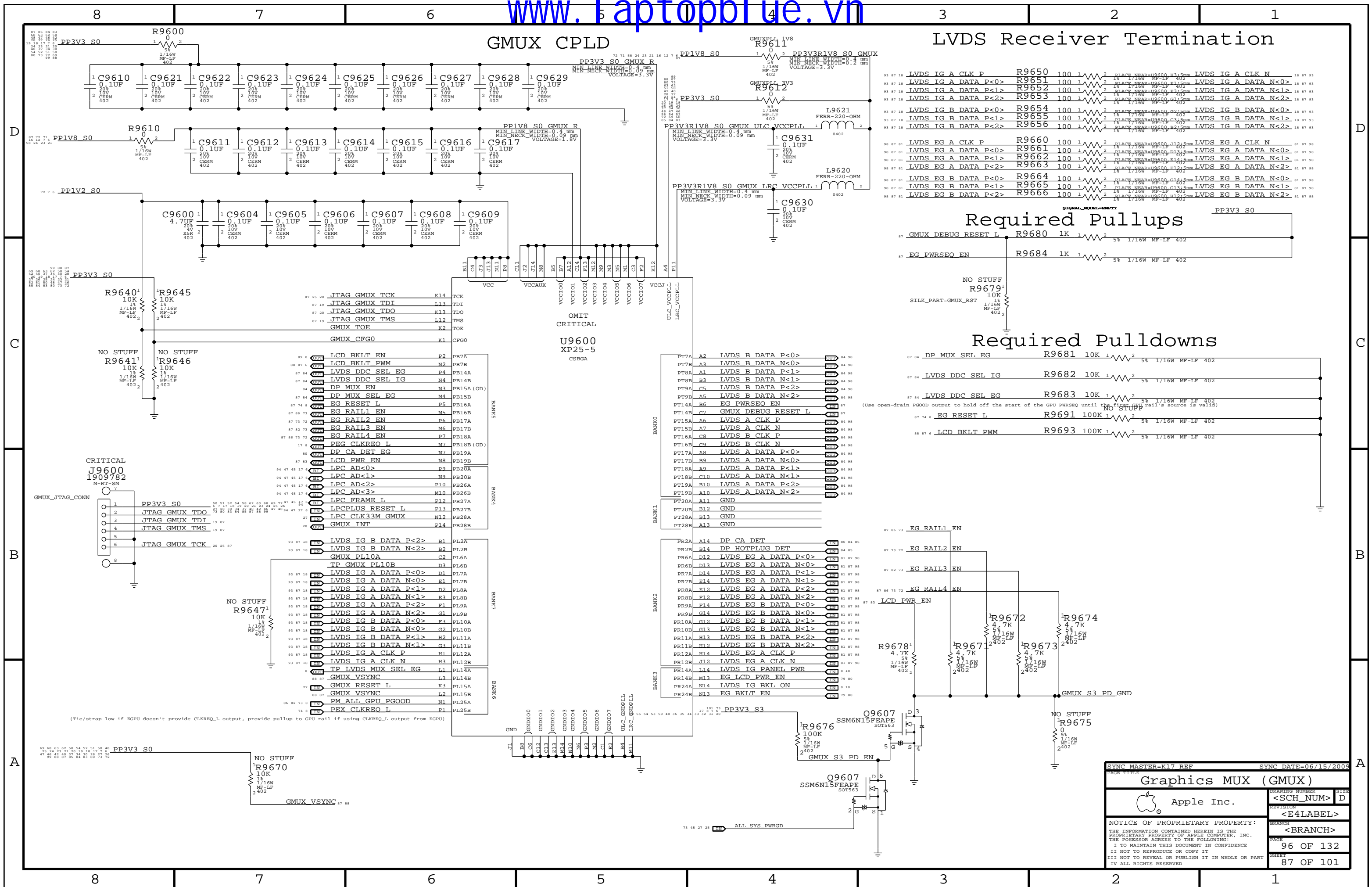
1V8 / 1V55 / 1V35 S0 FRAMEBUFFER REGULATOR

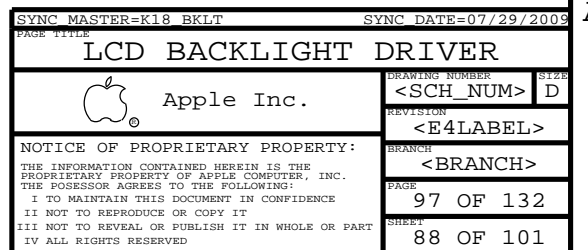
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
11480336	1	RES,1/16W,16.9K,1%,0402,LF	R9588		FB1V35
11480357	1	RES,1/16W,27.4K,1%,0402,LF	R9589		FB1V35

FB VDD	
FBVDD_ALTVO	Regulator Output
0	1.35 / 1.55 V
1	1.80 V



SYNC MASTER=K18 POWER		SYNC DATE=06/26/2009	
PAGE TITLE			
1V8 / 1V55 FB Power Supply			
 Apple Inc.		DRAWING NUMBER	SIZE
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		BRANCH	<BRANCH>
		PAGE	95 OF 132
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D

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C

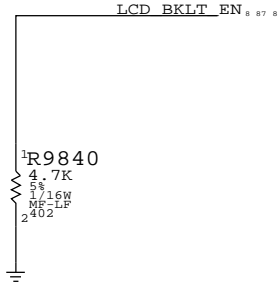
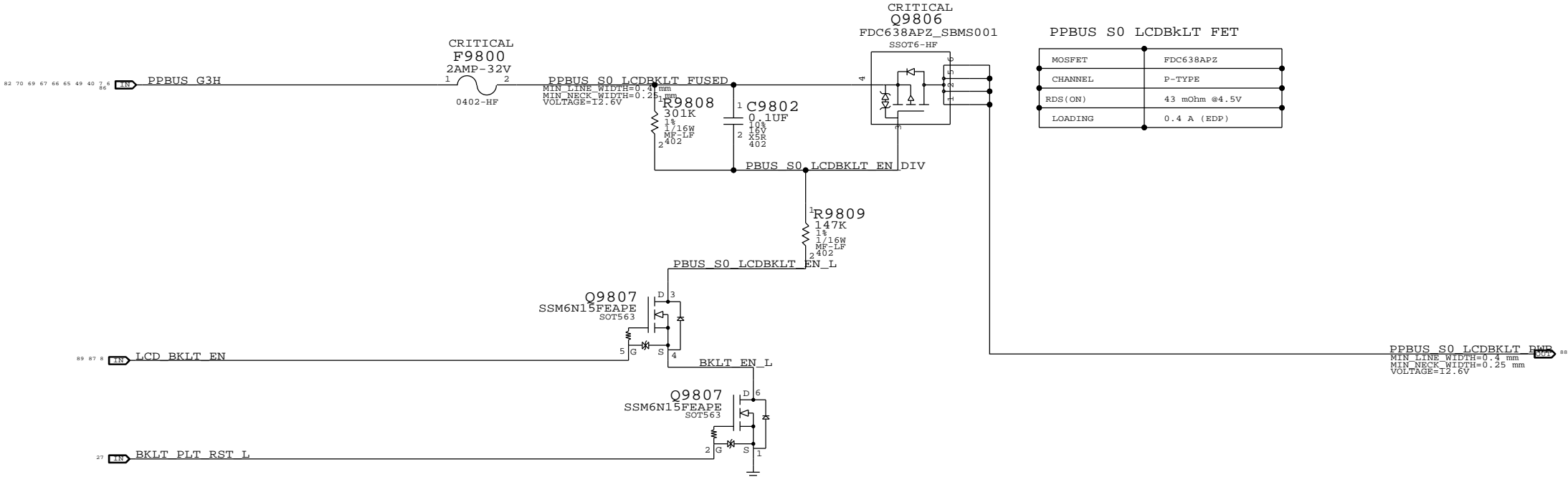
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
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Blank Page, was 1.2V/1.8V in K19

SYNC MASTER=K18 POWER		SYNC DATE=06/10/2009	
PAGE TITLE			
Misc Power Supplies		DRAWING NUMBER	
 Apple Inc.		<SCH_NUM>	
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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

Most CPU signals with impedance requirements are 50-ohm single-ended. Some signals require 27.4-ohm single-ended impedance.

SOURCE: Calpella SFF DG (DG-407364_v1.5), Section 2.8

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?

SOURCE: Calpella SFF DG (DG-407364_v1.5), Section 2.1 and Table 4-184.

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
DMI_S2N	PCIE_85D	PCIE	DMI_S2N P<3:0>	9 18
DMI_S2N	PCIE_85D	PCIE	DMI_S2N N<3:0>	9 18
DMI_N2S	PCIE_85D	PCIE	DMI_N2S P<3:0>	9 18
DMI_N2S	PCIE_85D	PCIE	DMI_N2S N<3:0>	9 18
FDI_DATA	PCIE_85D	PCIE	FDI_DATA P<7:0>	9 18
FDI_DATA	PCIE_85D	PCIE	FDI_DATA N<7:0>	9 18
	CPU_50S	CPU_AGTL	FDI_FSYNC<1..0>	9 18
	CPU_50S	CPU_AGTL	FDI_LSYNC<1..0>	9 18
	CPU_50S	CPU_AGTL	FDI_INT	9 18
CPU_PECT	CPU_50S	PCIE	CPU_PECT	10 20
FSB_CPURST_L	CPU_50S	CPU_AGTL	FSB_CPURST_L	10 25
PM_SYNC	CPU_50S	CPU_AGTL	PM_SYNC	10 18
PM_MEM_PWRGD	CPU_50S	CPU_AGTL	PM_MEM_PWRGD	10 18 31
CPU_VTT_S0_PGOOD	CPU_50S	CPU_AGTL	CPUVTT_S0_PGOOD	10 70
XDP_XPU_PWROOD	CPU_50S	CPU_ITP	XDP_CPUPWRGD	10 25
XDP_DBRESET_L	CPU_50S	CPU_ITP	XDP_DBRESET_L	10 25 27
XDP_PRDY_L	CPU_50S	CPU_ITP	XDP_PRDY_L	10 25
XDP_PREQ_L	CPU_50S	CPU_ITP	XDP_PREQ_L	10 25
	CPU_50S	CPU_AGTL	PM_EXT_TS_L<0>	10 46
	CPU_50S	CPU_AGTL	PM_EXT_TS_L<1>	10 46
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP0	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP1	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP2	10
CPU_CFG	CPU_50S	CPU_ITP	CPU_CFG<17..0>	8 9 25
CPU_CATERR_L	CPU_50S	CPU_AGTL	CPU_CATERR_L	10
	CPU_50S	CPU_AGTL	TP_CPU_VTT_SELECT	8 12
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	10 46 68
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	10 20 25
PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	10 20 46
FSB_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_CPU_P	10 20
FSB_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_CPU_N	10 20
FSB_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_ITP_P	10 25
FSB_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_ITP_N	10 25
PCIE_CLK100M_CPU	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_CPU_P	10 17
PCIE_CLK100M_CPU	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_CPU_N	10 17
	CPU_55S	CPU_8MIL	CPU_PSI_L	12 15 68
PM_DPRSIPVR	CPU_50S	CPU_AGTL	PM_DPRSIPVR	12 15 68
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	9
	CPU_27P4S	CPU_COMP	CPU_PEG_RBIA	9
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP3	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP2	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP1	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP0	10
XDP_TDI	CPU_50S	CPU_ITP	XDP_TDI	25
XDP_TDO	CPU_50S	CPU_ITP	XDP_TDO	25
XDP_TMS	CPU_50S	CPU_ITP	XDP_TMS	10 25
XDP_TCK	CPU_50S	CPU_ITP	XDP_TCK	10 25
XDP_TEST_L	CPU_50S	CPU_ITP	XDP_TRST_L	10 25
XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<6..0>	10 25
XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<7>	10 25
(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	25
	CPU_55S	CPU_8MIL	CPU_VID<6..0>	4 12 15
	CPU_50S	CPU_AGTL	CPUIMVP_IMON	12 50 68
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	12 68
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	12 68
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VTTSENSE_P	12 70
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VTTSENSE_N	12 70
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	GFX_VSENSE_P	13 69
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	GFX_VSENSE_N	13 69
PM_DPRSIPVR	CPU_55S	CPU_8MIL	GFX_VID<6..0>	8 13
	CPU_50S	CPU_AGTL	GFX_DPRSIPVR	13 69
	CPU_50S	CPU_AGTL	GFX_VR_EN	13 69
	CPU_50S	CPU_AGTL	GFXIMVP_IMON	13 69
	PCIE_85D	PCIE	PEG_R2D_P<15..0>	74
	PCIE_85D	PCIE	PEG_R2D_N<15..0>	74
PEG_R2D	PCIE_85D	PCIE	PEG_R2D_C_P<15..0>	8 9 74
	PCIE_85D	PCIE	PEG_R2D_C_N<15..0>	8 74
PEG_D2R	PCIE_85D	PCIE	PEG_D2R_P<15..0>	8 9 74
	PCIE_85D	PCIE	PEG_D2R_N<15..0>	8 74
	PCIE_85D	PCIE	PEG_D2R_C_P<15..0>	74
	PCIE_85D	PCIE	PEG_D2R_C_N<15..0>	74

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=3:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_QS2MEM	*	=3:1_SPACING	?
MEM_20OTHER	*	25 MILS	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_QS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_QS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_QS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_QS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_QS	MEM_CLK	*	MEM_QS2MEM
MEM_QS	MEM_CTRL	*	MEM_QS2MEM
MEM_QS	MEM_CMD	*	MEM_QS2MEM
MEM_QS	MEM_DATA	*	MEM_QS2MEM
MEM_QS	MEM_QS	*	MEM_QS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_20OTHER
MEM_CTRL	*	*	MEM_20OTHER
MEM_CMD	*	*	MEM_20OTHER
MEM_DATA	*	*	MEM_20OTHER
MEM_QS	*	*	MEM_20OTHER

DDR3:

DQ/DM signals should be matched within 0.508mm of associated DQS pair.

DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.

DQS to clock matching should be within [CLK-12.7mm] and [CLK+25.4mm].

CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.

CONTROL signals should be matched within [CLK-12.7mm] to [CLK+0.0mm] of CLK pairs.

A/BA/CMD signals should be matched within [CLK-12.7mm] to [CLK+12.7mm] of CLK pairs.


DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.

Maximum length of any signal from die pad to SODIMM pad is 139.7mm, from procesor ball to SODIMM pad is 114.3mm.

SOURCE: Calpella SFF Platform DG, Rev 1.5 (#407364), Section 2.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
MEM_A_CLK	MEM_72D	MEM_CLK	MEM A CLK P<5..0>	11 28
MEM_A_CLK	MEM_72D	MEM_CLK	MEM A CLK N<5..0>	11 28
MEM_A_CNTRL	MEM_37S	MEM_CTRL	MEM A CKE<3..0>	11 28
MEM_A_CNTRL	MEM_37S	MEM_CTRL	MEM A CS_L<3..0>	11 28
MEM_A_CNTRL	MEM_37S	MEM_CTRL	MEM A ODT<3..0>	11 28
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A A<15..0>	11 28
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A BA<2..0>	11 28
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A RAS_L	11 28
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A CAS_L	11 28
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A WE_L	11 28
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM A DQ<7..0>	11 29
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM A DQ<15..8>	11 29
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM A DQ<23..16>	11 29
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM A DQ<31..24>	11 29
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM A DQ<39..32>	11 28 29
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM A DQ<47..40>	11 29
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM A DQ<55..48>	11 29
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM A DQ<63..56>	11 29
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM A DM<0>	11 28 29
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM A DM<1>	11 29
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM A DM<2>	11 29
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM A DM<3>	11 29
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM A DM<4>	11 29
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM A DM<5>	11 29
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM A DM<6>	11 29
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM A DM<7>	11 29
MEM_A_DQS0	MEM_85D	MEM_QS	MEM A DQS P<0>	11 28 29
MEM_A_DQS0	MEM_85D	MEM_QS	MEM A DQS N<0>	11 28 29
MEM_A_DQS1	MEM_85D	MEM_QS	MEM A DQS P<1>	11 29
MEM_A_DQS1	MEM_85D	MEM_QS	MEM A DQS N<1>	11 29
MEM_A_DQS2	MEM_85D	MEM_QS	MEM A DQS P<2>	11 29
MEM_A_DQS2	MEM_85D	MEM_QS	MEM A DQS N<2>	11 29
MEM_A_DQS3	MEM_85D	MEM_QS	MEM A DQS P<3>	11 29
MEM_A_DQS3	MEM_85D	MEM_QS	MEM A DQS N<3>	11 29
MEM_A_DQS4	MEM_85D	MEM_QS	MEM A DQS P<4>	11 29
MEM_A_DQS4	MEM_85D	MEM_QS	MEM A DQS N<4>	11 29
MEM_A_DQS5	MEM_85D	MEM_QS	MEM A DQS P<5>	11 29
MEM_A_DQS5	MEM_85D	MEM_QS	MEM A DQS N<5>	11 29
MEM_A_DQS6	MEM_85D	MEM_QS	MEM A DQS P<6>	11 29
MEM_A_DQS6	MEM_85D	MEM_QS	MEM A DQS N<6>	11 29
MEM_A_DQS7	MEM_85D	MEM_QS	MEM A DQS P<7>	11 29
MEM_A_DQS7	MEM_85D	MEM_QS	MEM A DQS N<7>	11 29
MEM_B_CLK	MEM_72D	MEM_CLK	MEM B CLK P<5..0>	11 30
MEM_B_CLK	MEM_72D	MEM_CLK	MEM B CLK N<5..0>	11 30
MEM_B_CNTRL	MEM_37S	MEM_CTRL	MEM B CKE<3..0>	11 30
MEM_B_CNTRL	MEM_37S	MEM_CTRL	MEM B CS_L<3..0>	11 30
MEM_B_CNTRL	MEM_37S	MEM_CTRL	MEM B ODT<3..0>	11 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B A<15..0>	11 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B BA<2..0>	11 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B RAS_L	11 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B CAS_L	11 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B WE_L	11 30
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM B DQ<7..0>	11 29
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM B DQ<15..8>	11 29
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM B DQ<23..16>	11 29
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM B DQ<31..24>	11 29
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM B DQ<39..32>	11 28 30
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM B DQ<47..40>	11 29
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM B DQ<55..48>	11 29
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM B DQ<63..56>	11 29
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM B DM<0>	11 29 30
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM B DM<1>	11 29
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM B DM<2>	11 29
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM B DM<3>	11 29
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM B DM<4>	11 29
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM B DM<5>	11 29
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM B DM<6>	11 29
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM B DM<7>	11 29
MEM_B_DQS0	MEM_85D	MEM_QS	MEM B DQS P<0>	11 29 30
MEM_B_DQS0	MEM_85D	MEM_QS	MEM B DQS N<0>	11 29 30
MEM_B_DQS1	MEM_85D	MEM_QS	MEM B DQS P<1>	11 29
MEM_B_DQS1	MEM_85D	MEM_QS	MEM B DQS N<1>	11 29
MEM_B_DQS2	MEM_85D	MEM_QS	MEM B DQS P<2>	11 29
MEM_B_DQS2	MEM_85D	MEM_QS	MEM B DQS N<2>	11 29
MEM_B_DQS3	MEM_85D	MEM_QS	MEM B DQS P<3>	11 29
MEM_B_DQS3	MEM_85D	MEM_QS	MEM B DQS N<3>	11 29
MEM_B_DQS4	MEM_85D	MEM_QS	MEM B DQS P<4>	11 29
MEM_B_DQS4	MEM_85D	MEM_QS	MEM B DQS N<4>	11 29
MEM_B_DQS5	MEM_85D	MEM_QS	MEM B DQS P<5>	11 29
MEM_B_DQS5	MEM_85D	MEM_QS	MEM B DQS N<5>	11 29
MEM_B_DQS6	MEM_85D	MEM_QS	MEM B DQS P<6>	11 29
MEM_B_DQS6	MEM_85D	MEM_QS	MEM B DQS N<6>	11 29
MEM_B_DQS7	MEM_85D	MEM_QS	MEM B DQS P<7>	11 29
MEM_B_DQS7	MEM_85D	MEM_QS	MEM B DQS N<7>	11 29

SYNC MASTER=K17_REF		SYNC DATE=06/15/2009		
PAGE TITLE				
Memory Constraints				
	Apple Inc.		DRAWING NUMBER	SIZE
			<SCH_NUM>	D
		REVISION		
		<E4LABEL>		
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Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
LVDS_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?	DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?	LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length. DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps. DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals. Max length of LVDS/DisplayPort/TMDS traces: 12 inches. SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?	SATA	TOP,BOTTOM	=3x_DIELECTRIC	?
SATA_ICOMP	*	8 MIL	?				

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

USB 2.0 Interface Constraints


PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?	USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.8

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
	PHYSICAL	SPACING		
DP_ML	DP_85D	DISPLAYPORT	DP IG ML P<3..0>	8 84
DP_ML	DP_85D	DISPLAYPORT	DP IG ML N<3..0>	8 84
DP_AUX_CH	DP_85D	DISPLAYPORT	DP IG AUX_CH P	8 18 84
DP_AUX_CH	DP_85D	DISPLAYPORT	DP IG AUX_CH N	8 18 84
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS IG A_CLK P	18 87
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS IG A_CLK N	18 87
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS IG A_DATA P<2..0>	18 87
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS IG A_DATA N<2..0>	18 87
LVDS_IG_A_DATA3	LVDS_85D	LVDS	NC LVDS IG A_DATAP<3>	8 18
LVDS_IG_A_DATA3	LVDS_85D	LVDS	NC LVDS IG A_DATAN<3>	8 18
LVDS_IG_B_CLK	LVDS_85D	LVDS	TP LVDS IG B_CLKP	6 8 18
LVDS_IG_B_CLK	LVDS_85D	LVDS	TP LVDS IG B_CLKN	6 8 18
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS IG B_DATA P<2..0>	18 87
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS IG B_DATA N<2..0>	18 87
LVDS_IG_B_DATA3	LVDS_85D	LVDS	NC LVDS IG B_DATAP<3>	8 18
LVDS_IG_B_DATA3	LVDS_85D	LVDS	NC LVDS IG B_DATAN<3>	8 18
SATA_HDD_R2D	SATA_90D	SATA	SATA HDD R2D C P	17 42
SATA_90D	SATA	SATA	SATA HDD R2D C N	17 42
SATA_90D	SATA	SATA	SATA HDD R2D P	6 42
SATA_90D	SATA	SATA	SATA HDD R2D N	6 42
SATA_HDD_D2R	SATA_90D	SATA	SATA HDD D2R P	17 42
SATA_90D	SATA	SATA	SATA HDD D2R N	17 42
SATA_90D	SATA	SATA	SATA HDD D2R C P	6 42
SATA_90D	SATA	SATA	SATA HDD D2R C N	6 42
SATA_ODD_R2D	SATA_90D	SATA	SATA ODD R2D C P	17 42
SATA_90D	SATA	SATA	SATA ODD R2D C N	17 42
SATA_90D	SATA	SATA	SATA ODD R2D P	6 42
SATA_90D	SATA	SATA	SATA ODD R2D N	6 42
SATA_ODD_D2R	SATA_90D	SATA	SATA ODD D2R P	17 42
SATA_90D	SATA	SATA	SATA ODD D2R N	17 42
SATA_90D	SATA	SATA	SATA ODD D2R C P	6 42
SATA_90D	SATA	SATA	SATA ODD D2R C N	6 42
SATA_HDD_R2D	SATA_90D	SATA	SATA HDD R2D RDRV IN P	42
SATA_90D	SATA	SATA	SATA HDD R2D RDRV IN N	42
SATA_90D	SATA	SATA	SATA HDD R2D RDRV OUT P	42
SATA_90D	SATA	SATA	SATA HDD R2D RDRV OUT N	42
SATA_HDD_D2R	SATA_90D	SATA	SATA HDD D2R RDRV IN P	42
SATA_90D	SATA	SATA	SATA HDD D2R RDRV IN N	42
SATA_90D	SATA	SATA	SATA HDD D2R RDRV OUT P	42
SATA_90D	SATA	SATA	SATA HDD D2R RDRV OUT N	42
PCH_SATA_ICOMP		SATA_ICOMP	PCH SATAICOMP	17
USB_HUB1_UP	USB_85D	USB	USB HUB1 UP P	19 35
USB_85D	USB	USB	USB HUB1 UP N	19 35
USB_HUB2_UP	USB_85D	USB	USB HUB2 UP P	19 36
USB_85D	USB	USB	USB HUB2 UP N	19 36
USB_EXT_A	USB_85D	USB	USB EXT_A P	36 43
USB_85D	USB	USB	USB EXT_A N	36 43
USB_EXT_B	USB_85D	USB	USB EXT_B P	36 43
USB_85D	USB	USB	USB EXT_B N	36 43
USB_EXT_C	USB_85D	USB	USB EXT_C P	8 35
USB_85D	USB	USB	USB EXT_C N	8 35
USB_EXT_D	USB_85D	USB	USB EXT_D P	
USB_85D	USB	USB	USB EXT_D N	
USB_MINI	USB_85D	USB	USB MINI P	
USB_85D	USB	USB	USB MINI N	
USB_WM	USB_85D	USB	USB WM P	
USB_85D	USB	USB	USB WM N	
USB_CAMERA	USB_85D	USB	USB CAMERA CONN P	6 33
USB_85D	USB	USB	USB CAMERA CONN N	6 33
USB_BT	USB_85D	USB	USB BT P	33 36
USB_85D	USB	USB	USB BT N	33 36
USB_TP_A	USB_85D	USB	USB TPAD P	36 53
USB_85D	USB	USB	USB TPAD N	36 53
USB_IR	USB_85D	USB	USB IR P	35 44
USB_85D	USB	USB	USB IR N	35 44
USB_SDCARD	USB_85D	USB	USB SDCARD P	8 34 36
USB_85D	USB	USB	USB SDCARD N	8 34 36
USB_BRCRYPT	USB_85D	USB	USB BRCRYPT P	19 101
USB_85D	USB	USB	USB BRCRYPT N	19 101
PCH_USB_RBIAS	PCH_USB_RBIAS		PCH USB RBIAS	19
PCH_CLK100M_PCH	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M_PCH P	17 26
CLK_PCIE_90D	CLK_PCIE	CLK_PCIE	PCIE CLK100M_PCH N	17 26
CLK_PCIE_90D	CLK_PCIE	CLK_PCIE	FSB CLK133M_PCH P	17 26
CLK_PCIE_90D	CLK_PCIE	CLK_PCIE	FSB CLK133M_PCH N	17 26
CLK_PCIE_90D	CLK_PCIE	CLK_PCIE	PCH CLK96M_DOT P	17 26
CLK_PCIE_90D	CLK_PCIE	CLK_PCIE	PCH CLK96M_DOT N	17 26
PCH_CLK100M_SATA	CLK_PCIE_90D	CLK_PCIE	PCH CLK100M_SATA P	17 26
PCH_CLK100M_SATA	CLK_PCIE_90D	CLK_PCIE	PCH CLK100M_SATA N	17 26
CPU_50S	CLK_PCIE	CLK_PCIE	PCH CLK14P3M_REFCLK	17 26
CPU_50S	CLK_PCIE	CLK_PCIE	PCH CLK33M_PCIIN	17 27
GFX_CLK_DPLLSS	CLK_PCIE_90D	CLK_PCIE	GFX CLK120M_DPLLSS P	10 17
GFX_CLK_DPLLSS	CLK_PCIE_90D	CLK_PCIE	GFX CLK120M_DPLLSS N	10 17

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD



















































































SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?


SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE				
	PHYSICAL	SPACING			
 LPC_AD	LPC_50S	LPC	LPC_AD<3..0>	6 17 45	
 LPC_FRAME_L	LPC_50S	LPC	LPC_FRAME_L	6 17 45	
 LPC_RESET_L	LPC_50S	LPC	LPCPLUS_RESET_L	6 27 47	
 MCP_LPC_CLK0	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC_R	19 27	
	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC	27 45	
	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_LPCPLUS	6 27 47	
	SMBUS_PCH_CLK	SMB	SMBUS_PCH_CLK	17 26 28	
	SMBUS_PCH_DATA	SMB	SMBUS_PCH_DATA	88 26 28	
	SMBUS_PCH_0_CLK	SMB	SML_PCH_0_CLK	17 48	
	SMBUS_PCH_0_DATA	SMB	SML_PCH_0_DATA	17 48	
	SMBUS_PCH_1_CLK	SMB	SML_PCH_1_CLK	17 48	
	SMBUS_PCH_1_DATA	SMB	SML_PCH_1_DATA	17 48	
	HDA_BIT_CLK	HDA	HDA_BIT_CLK	17 58	
	HDA_50S	HDA	HDA_BIT_CLK_R	17	
	HDA_SYNC	HDA	HDA_SYNC	17 58	
	HDA_50S	HDA	HDA_SYNC_R	17	
	HDA_RST_L	HDA	HDA_RST_R_L	17	
	HDA_50S	HDA	HDA_RST_L	17 58	
	HDA_SDIN0	HDA	HDA_SDIN0	17 58	
	HDA_50S	HDA	AUD_SDI_R	58	
	HDA_SDOINT	HDA	HDA_SDOUT	17 58	
	HDA_50S	HDA	HDA_SDOUT_R	17	
	PM_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK	18 46
	SPI_CLK	SPI_55S	SPI	SPI_CLK_R	17 47
	SPI_55S	SPI	SPI_CLK	47	
	SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	17 47
	SPI_55S	SPI	SPI_MOSI	47	
	SPI_MISO	SPI_55S	SPI	SPI_MISO	17 47
	SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	17 47
	SPI_55S	SPI	SPI_CS0_L	47	
	PCIE_85D	PCIE	PCIE_ENET_R2D_P	37	
	PCIE_85D	PCIE	PCIE_ENET_R2D_N	37	
	PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_P	17 37
	PCIE_85D	PCIE	PCIE_ENET_R2D_C_N	17 37	
	PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_P	17 37
	PCIE_85D	PCIE	PCIE_ENET_D2R_N	17 37	
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_P	37	
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_N	37	
	PCIE_85D	PCIE	PCIE_AP_R2D_P	6 33	
	PCIE_85D	PCIE	PCIE_AP_R2D_N	6 33	
	PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_C_P	17 33
	PCIE_85D	PCIE	PCIE_AP_R2D_C_N	17 33	
	PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_P	6 17 33
	PCIE_85D	PCIE	PCIE_AP_D2R_N	6 17 33	
	PCIE_85D	PCIE	PCIE_FW_R2D_P	39	
	PCIE_85D	PCIE	PCIE_FW_R2D_N	39	
	PCIE_FW_R2D	PCIE_85D	PCIE	PCIE_FW_R2D_C_P	17 39
	PCIE_85D	PCIE	PCIE_FW_R2D_C_N	17 39	
	PCIE_FW_D2R	PCIE_85D	PCIE	PCIE_FW_D2R_P	17 39
	PCIE_85D	PCIE	PCIE_FW_D2R_N	17 39	
	PCIE_85D	PCIE	PCIE_FW_D2R_C_P	39	
	PCIE_85D	PCIE	PCIE_FW_D2R_C_N	39	
	PCIE_AP_D2R	PCIE_85D	PCIE	CONN_PCIE_AP_D2R_P	
	PCIE_85D	PCIE	CONN_PCIE_AP_D2R_N		
	PCIE_AP_R2D	PCIE_85D	PCIE	CONN_PCIE_AP_R2D_P	
	PCIE_85D	PCIE	CONN_PCIE_AP_R2D_N		
	MCP_PE0_REECLK	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_P	17 74
	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_N	17 74	
	PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_P	17 37
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_N	17 37	
	MCP_PE1_REECLK	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_P	17 33
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_N	17 33	
	MCP_PE2_REECLK	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_P	17 39
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_N	17 39	
	MCP_PE3_REECLK	CLK_PCIE_90D	CLK_PCIE	NC_PCIE_CLK100M_EXCARD_P	8 17
	CLK_PCIE_90D	CLK_PCIE	NC_PCIE_CLK100M_EXCARD_N	8 17	
	CPU_27B4S	CPU_COMP	PCH_VSS_NCTF<1>	6 20	
	CPU_27B4S	CPU_COMP	PCH_VSS_NCTF<2>	6 20	
	CPU_27B4S	CPU_COMP	PCH_VSS_NCTF<5>	6 20	
	CPU_27B4S	CPU_COMP	TP_PCH_VSS_NCTF<7>	20	
	CPU_27B4S	CPU_COMP	PCH_VSS_NCTF<9>	6 20 94	
	CPU_27B4S	CPU_COMP	PCH_VSS_NCTF<9>	6 20 94	
	CPU_27B4S	CPU_COMP	PCH_VSS_NCTF<11>	6 20	
	CPU_27B4S	CPU_COMP	PCH_VSS_NCTF<12>	6 20	
	CPU_27B4S	CPU_COMP	PCH_VSS_NCTF<15>	6 20	
	CPU_27B4S	CPU_COMP	PCH_VSS_NCTF<17>	6 20	
	CPU_27B4S	CPU_COMP	PCH_VSS_NCTF<19>	6 20	
	CPU_27B4S	CPU_COMP	PCH_VSS_NCTF<21>	6 20	
	CPU_27B4S	CPU_COMP	PCH_VSS_NCTF<22>	20	
	CPU_27B4S	CPU_COMP	PCH_VSS_NCTF<25>	6 20	
	CPU_27B4S	CPU_COMP	PCH_VSS_NCTF<27>	6 20	
	CPU_27B4S	CPU_COMP	PCH_VSS_NCTF<29>	6 20	

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CAESAR II (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_3X	*	=3:1_SPACING	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

CAESAR II (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	0.6 MM	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

Ethernet Net Properties

NET_TYPE		
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING
	ENET_50S	ENET_3X
	ENET_50S	ENET_3X
	ENET_50S	ENET_3X
	ENET_100D	ENET_MDI
	ENET_100D	ENET_MDI

BCM5764_CLK25M_XTALI

2737

BCM5764_CLK25M_XTALO

2737

ENET_RESET_L

2737

ENET_MDI_P<3..0>

3738

ENET_MDI_N<3..0>

3738

D

C

B

A

D

C

B









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FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
 FW_P0_TPA	FW_110D	FW_TP	NC FW0 TPAP 6 39 41
 FW_P0_TPA	FW_110D	FW_TP	NC FW0 TPAN 39 41
 FW_P0_TPB	FW_110D	FW_TP	NC FW0 TPBP 6 39 41
 FW_P0_TPB	FW_110D	FW_TP	NC FW0 TPBN 6 39 41
 FW_P1_TPA	FW_110D	FW_TP	FW PORT1 TPA P 39 40 41
 FW_P1_TPA	FW_110D	FW_TP	FW PORT1 TPA N 39 40 41
 FW_P1_TPB	FW_110D	FW_TP	FW PORT1 TPB P 39 40 41
 FW_P1_TPB	FW_110D	FW_TP	FW PORT1 TPB N 39 40 41
Port 2 Not Used			

D











C

B





A

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
 SMBUS_SMC_A_S3_SCL	SMB_50S	SMB	SMBUS_SMC_A_S3_SCL 6 33 45 48 54
 SMBUS_SMC_A_S3_SDA	SMB_50S	SMB	SMBUS_SMC_A_S3_SDA 6 33 45 48 54
 SMBUS_SMC_B_S0_SCL	SMB_50S	SMB	SMBUS_SMC_B_S0_SCL 45 48 51
 SMBUS_SMC_B_S0_SDA	SMB_50S	SMB	SMBUS_SMC_B_S0_SDA 45 48 51
 SMBUS_SMC_0_S0_SCL	SMB_50S	SMB	SMBUS_SMC_0_S0_SCL 45 48 51 81
 SMBUS_SMC_0_S0_SDA	SMB_50S	SMB	SMBUS_SMC_0_S0_SDA 45 48 51 81
 SMBUS_SMC_BSA_SCL	SMB_50S	SMB	SMBUS_SMC_BSA_SCL 6 45 48 64 65
 SMBUS_SMC_BSA_SDA	SMB_50S	SMB	SMBUS_SMC_BSA_SDA 6 45 48 64 65
 SMBUS_SMC_MGMT_SCL	SMB_50S	SMB	SMBUS_SMC_MGMT_SCL 45 48 56
 SMBUS_SMC_MGMT_SDA	SMB_50S	SMB	SMBUS_SMC_MGMT_SDA 45 48 56

SMBus Charger Net Properties

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
 CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P 65
 CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_N 65
 CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P 65
 CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_N 65

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GDDR3 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR3_40R55SE	*	=55_OHM_SE	=40_OHM_SE	0.095 MM	12.7 MM	=STANDARD	=STANDARD
GDDR3_40SE	*	=40_OHM_SE	=40_OHM_SE	0.095 MM	=40_OHM_SE	=STANDARD	=STANDARD
GDDR3_80D	*	=85_OHM_DIFF	=85_OHM_DIFF	0.095 MM	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR3_CLK	*	=2.5:1_SPACING	?
GDDR3_CMD	*	=2.5:1_SPACING	?
GDDR3_DATA	*	=2.5:1_SPACING	?
GDDR3_DQS	*	=2.5:1_SPACING	?

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
LVDS_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?	DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?	LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 0.127 mm. Pairs should be within 0.508mm of entire channel.
DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.
DisplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.
Max length of LVDS/DisplayPort/TMDS traces: 13 inches.
SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.

GDDR3 FB A/B Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
FB_A_CLK	GDDR3_80D	GDDR3_CLK	FB A CLK P<0>	76 77
	GDDR3_80D	GDDR3_CLK	FB A CLK N<0>	76 77
FB_B_CLK	GDDR3_80D	GDDR3_CLK	FB A CLK P<1>	76 77
	GDDR3_80D	GDDR3_CLK	FB A CLK N<1>	76 77
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB A MA<1..0>	76 77
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB A MA<12..6>	76 77
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB A BA<2..0>	76 77
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB A RAS L	76 77
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB A UCAS L	76 77
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB A WE L	76 77
FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB A UCKE	76 77
FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB A LCKE	76 77
FB_AB_CS0	GDDR3_40R55SE	GDDR3_CMD	FB A LCS0 L	76 77
FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB A DRAM RST	76 77
FB_A_CMD	GDDR3_40SE	GDDR3_CMD	FB A LMA<5..2>	76 77
FB_B_CMD	GDDR3_40SE	GDDR3_CMD	FB A UMA<5..2>	76 77
FB_A_WDQS0	GDDR3_40SE	GDDR3_DQS	FB A WDQS<0>	76 77
FB_A_WDQS1	GDDR3_40SE	GDDR3_DQS	FB A WDQS<1>	76 77
FB_A_WDQS2	GDDR3_40SE	GDDR3_DQS	FB A WDQS<2>	76 77
FB_A_WDQS3	GDDR3_40SE	GDDR3_DQS	FB A WDQS<3>	76 77
FB_A_RDQS0	GDDR3_40SE	GDDR3_DQS	FB A RDQS<0>	76 77
FB_A_RDQS1	GDDR3_40SE	GDDR3_DQS	FB A RDQS<1>	76 77
FB_A_RDQS2	GDDR3_40SE	GDDR3_DQS	FB A RDQS<2>	76 77
FB_A_RDQS3	GDDR3_40SE	GDDR3_DQS	FB A RDQS<3>	76 77
FB_A_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB A DQ<7..0>	76 77
FB_A_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB A DQ<15..8>	76 77
FB_A_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB A DQ<23..16>	76 77
FB_A_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB A DQ<31..24>	76 77
FB_A_DQM0	GDDR3_40SE	GDDR3_DATA	FB A DOM L<0>	76 77
FB_A_DQM1	GDDR3_40SE	GDDR3_DATA	FB A DOM L<1>	76 77
FB_A_DQM2	GDDR3_40SE	GDDR3_DATA	FB A DOM L<2>	76 77
FB_A_DQM3	GDDR3_40SE	GDDR3_DATA	FB A DOM L<3>	76 77
FB_B_WDQS0	GDDR3_40SE	GDDR3_DQS	FB A WDQS<4>	76 77
FB_B_WDQS1	GDDR3_40SE	GDDR3_DQS	FB A WDQS<5>	76 77
FB_B_WDQS2	GDDR3_40SE	GDDR3_DQS	FB A WDQS<6>	76 77
FB_B_WDQS3	GDDR3_40SE	GDDR3_DQS	FB A WDQS<7>	76 77
FB_B_RDQS0	GDDR3_40SE	GDDR3_DQS	FB A RDQS<4>	76 77
FB_B_RDQS1	GDDR3_40SE	GDDR3_DQS	FB A RDQS<5>	76 77
FB_B_RDQS2	GDDR3_40SE	GDDR3_DQS	FB A RDQS<6>	76 77
FB_B_RDQS3	GDDR3_40SE	GDDR3_DQS	FB A RDQS<7>	76 77
FB_B_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB A DQ<39..32>	76 77
FB_B_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB A DQ<47..40>	76 77
FB_B_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB A DQ<55..48>	76 77
FB_B_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB A DQ<63..56>	76 77
FB_B_DQM0	GDDR3_40SE	GDDR3_DATA	FB A DOM L<4>	76 77
FB_B_DQM1	GDDR3_40SE	GDDR3_DATA	FB A DOM L<5>	76 77
FB_B_DQM2	GDDR3_40SE	GDDR3_DATA	FB A DOM L<6>	76 77
FB_B_DQM3	GDDR3_40SE	GDDR3_DATA	FB A DOM L<7>	76 77

G96 Net Properties


ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
GPU_CLK27M	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M	27 79 80
GPU_CLK27M_SS	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M_SS	79 80
LVDS_EG_A_CLK	LVDS_85D	LVDS	LVDS EG A CLK P	81 87
LVDS_EG_A_CLK	LVDS_85D	LVDS	LVDS EG A CLK N	81 87
LVDS_EG_A_DATA	LVDS_85D	LVDS	LVDS EG A DATA P<2..0>	81 87
LVDS_EG_A_DATA	LVDS_85D	LVDS	LVDS EG A DATA N<2..0>	81 87
LVDS_EG_A_DATA3	LVDS_85D	LVDS	NC LVDS EG A DATA P<3>	80 81
LVDS_EG_A_DATA3	LVDS_85D	LVDS	NC LVDS EG A DATA N<3>	80 81
LVDS_EG_B_DATA	LVDS_85D	LVDS	LVDS EG B DATA P<2..0>	81 87
LVDS_EG_B_DATA	LVDS_85D	LVDS	LVDS EG B DATA N<2..0>	81 87
LVDS_EG_B_DATA3	LVDS_85D	LVDS	NC LVDS EG B DATA P<3>	80 81
LVDS_EG_B_DATA3	LVDS_85D	LVDS	NC LVDS EG B DATA N<3>	80 81
DP_ML	DP_85D	DISPLAYPORT	DP EG ML P<3..0>	81 84
DP_ML	DP_85D	DISPLAYPORT	DP EG ML N<3..0>	81 84
DP_AUX_CH	DP_85D	DISPLAYPORT	DP EG AUX CH P	81 84
DP_AUX_CH	DP_85D	DISPLAYPORT	DP EG AUX CH N	81 84
DP_AUX_CH	DP_85D	DISPLAYPORT	DP EG AUX CH C P	84
DP_AUX_CH	DP_85D	DISPLAYPORT	DP EG AUX CH C N	84

GDDR3 FB C/D Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
FB_C_CLK	GDDR3_80D	GDDR3_CLK	FB B CLK P<0>	76 78
	GDDR3_80D	GDDR3_CLK	FB B CLK N<0>	76 78
FB_D_CLK	GDDR3_80D	GDDR3_CLK	FB B CLK P<1>	76 78
	GDDR3_80D	GDDR3_CLK	FB B CLK N<1>	76 78
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB B MA<1..0>	76 78
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB B MA<12..6>	76 78
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB B BA<2..0>	76 78
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB B RAS L	76 78
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB B UCAS L	76 78
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB B WE L	76 78
FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB B UCKE	76 78
FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB B LCKE	76 78
FB_CD_CS0	GDDR3_40R55SE	GDDR3_CMD	FB B LCS0 L	76 78
FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB B DRAM RST	76 78
FB_C_CMD	GDDR3_40SE	GDDR3_CMD	FB B LMA<5..2>	76 78
FB_D_CMD	GDDR3_40SE	GDDR3_CMD	FB B UMA<5..2>	76 78
FB_C_WDQS0	GDDR3_40SE	GDDR3_DQS	FB B WDQS<0>	76 78
FB_C_WDQS1	GDDR3_40SE	GDDR3_DQS	FB B WDQS<1>	76 78
FB_C_WDQS2	GDDR3_40SE	GDDR3_DQS	FB B WDQS<2>	76 78
FB_C_WDQS3	GDDR3_40SE	GDDR3_DQS	FB B WDQS<3>	76 78
FB_C_RDQS0	GDDR3_40SE	GDDR3_DQS	FB B RDQS<0>	76 78
FB_C_RDQS1	GDDR3_40SE	GDDR3_DQS	FB B RDQS<1>	76 78
FB_C_RDQS2	GDDR3_40SE	GDDR3_DQS	FB B RDQS<2>	76 78
FB_C_RDQS3	GDDR3_40SE	GDDR3_DQS	FB B RDQS<3>	76 78
FB_C_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB B DQ<7..0>	76 78
FB_C_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB B DQ<15..8>	76 78
FB_C_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB B DQ<23..16>	76 78
FB_C_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB B DQ<31..24>	76 78
FB_C_DQM0	GDDR3_40SE	GDDR3_DATA	FB B DOM L<0>	76 78
FB_C_DQM1	GDDR3_40SE	GDDR3_DATA	FB B DOM L<1>	76 78
FB_C_DQM2	GDDR3_40SE	GDDR3_DATA	FB B DOM L<2>	76 78
FB_C_DQM3	GDDR3_40SE	GDDR3_DATA	FB B DOM L<3>	76 78
FB_D_WDQS0	GDDR3_40SE	GDDR3_DQS	FB B WDQS<4>	76 78
FB_D_WDQS1	GDDR3_40SE	GDDR3_DQS	FB B WDQS<5>	76 78
FB_D_WDQS2	GDDR3_40SE	GDDR3_DQS	FB B WDQS<6>	76 78
FB_D_WDQS3	GDDR3_40SE	GDDR3_DQS	FB B WDQS<7>	76 78
FB_D_RDQS0	GDDR3_40SE	GDDR3_DQS	FB B RDQS<4>	76 78
FB_D_RDQS1	GDDR3_40SE	GDDR3_DQS	FB B RDQS<5>	76 78
FB_D_RDQS2	GDDR3_40SE	GDDR3_DQS	FB B RDQS<6>	76 78
FB_D_RDQS3	GDDR3_40SE	GDDR3_DQS	FB B RDQS<7>	76 78
FB_D_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB B DQ<39..32>	76 78
FB_D_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB B DQ<47..40>	76 78
FB_D_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB B DQ<55..48>	76 78
FB_D_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB B DQ<63..56>	76 78
FB_D_DQM0	GDDR3_40SE	GDDR3_DATA	FB B DOM L<4>	76 78
FB_D_DQM1	GDDR3_40SE	GDDR3_DATA	FB B DOM L<5>	76 78
FB_D_DQM2	GDDR3_40SE	GDDR3_DATA	FB B DOM L<6>	76 78
FB_D_DQM3	GDDR3_40SE	GDDR3_DATA	FB B DOM L<7>	76 78
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB A LCAS L	76 77
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB B LCAS L	76 78

MUXGFX Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
LVDS_A_CLK	LVDS_85D	LVDS	LVDS A CLK P	84 87
LVDS_A_CLK	LVDS_85D	LVDS	LVDS A CLK N	84 87
LVDS_A_DATA	LVDS_85D	LVDS	LVDS A DATA P<2..0>	84 87
LVDS_A_DATA	LVDS_85D	LVDS	LVDS A DATA N<2..0>	84 87
LVDS_B_CLK	LVDS_85D	LVDS	LVDS B CLK P	84 87
LVDS_B_CLK	LVDS_85D	LVDS	LVDS B CLK N	84 87
LVDS_B_DATA	LVDS_85D	LVDS	LVDS B DATA P<2..0>	84 87
LVDS_B_DATA	LVDS_85D	LVDS	LVDS B DATA N<2..0>	84 87
LVDS_CONN_A_CLK_F_P	LVDS_85D	LVDS	LVDS CONN A CLK F P	6 83
LVDS_CONN_A_CLK_F_N	LVDS_85D	LVDS	LVDS CONN A CLK F N	6 83
LVDS_CONN_B_CLK_F_P	LVDS_85D	LVDS	LVDS CONN B CLK F P	6 83
LVDS_CONN_B_CLK_F_N	LVDS_85D	LVDS	LVDS CONN B CLK F N	6 83
LVDS_CONN_A_CLK_P	LVDS_85D	LVDS	LVDS CONN A CLK P	83 84
LVDS_CONN_A_CLK_N	LVDS_85D	LVDS	LVDS CONN A CLK N	83 84
LVDS_CONN_A_DATA_P<2..0>	LVDS_85D	LVDS	LVDS CONN A DATA P<2..0>	6 83 84
LVDS_CONN_A_DATA_N<2..0>	LVDS_85D	LVDS	LVDS CONN A DATA N<2..0>	6 83 84
LVDS_CONN_B_CLK_P	LVDS_85D	LVDS	LVDS CONN B CLK P	83 84
LVDS_CONN_B_CLK_N	LVDS_85D	LVDS	LVDS CONN B CLK N	83 84
LVDS_CONN_B_DATA_P<2..0>	LVDS_85D	LVDS	LVDS CONN B DATA P<2..0>	6 83 84
LVDS_CONN_B_DATA_N<2..0>	LVDS_85D	LVDS	LVDS CONN B DATA N<2..0>	6 83 84
DP_ML	DP_85D	DISPLAYPORT	DP ML C P<3..0>	85
DP_ML	DP_85D	DISPLAYPORT	DP ML C N<3..0>	85
DP_ML	DP_85D	DISPLAYPORT	DP ML P<3..0>	84 85
DP_ML	DP_85D	DISPLAYPORT	DP ML N<3..0>	84 85
DP_ML	DP_85D	DISPLAYPORT	DP ML CONN P<3..0>	85
DP_ML	DP_85D	DISPLAYPORT	DP ML CONN N<3..0>	85
DP_AUX_CH	DP_85D	DISPLAYPORT	DP AUX CH C P	84 85
DP_AUX_CH	DP_85D	DISPLAYPORT	DP AUX CH C N	84 85

SYNC MASTER=K17 REF		SYNC DATE=06/15/2009			
PAGE TITLE					
GPU (GT216) CONSTRAINTS					
 Apple Inc.		DRAWING NUMBER	SIZE		
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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1T01_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1T01_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	10 MM OVERRIDE	OVERRIDE	OVERRIDE
USB_85D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	BOTTOM OVERRIDE	OVERRIDE	OVERRIDE	0.23 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE

Graphics ,SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_85D	BGA	LVDS_85D
DP_85D	BGA	100_DIFF_BGA
SATA_90D	BGA	100_DIFF_BGA
CLK_PCIE_90D	BGA	100_DIFF_BGA

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.


PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

K18 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
	ENET_100D	ENETCONN	ENETCONN P<3..0>
	ENET_100D	ENETCONN	ENETCONN N<3..0>
	SATA_90D	SATA	SATA_ODD_R2D_UF_P
	SATA_90D	SATA	SATA_ODD_R2D_UF_N
	SATA_90D	SATA	SATA_ODD_D2R_UF_P
	SATA_90D	SATA	SATA_ODD_D2R_UF_N
	SATA_90D	SATA	SATA_HDD_D2R_UF_P
	SATA_90D	SATA	SATA_HDD_D2R_UF_N
	SATA_90D	SATA	SATA_HDD_R2D_UF_P
	SATA_90D	SATA	SATA_HDD_R2D_UF_N
	SENSE_DIFFPAIR	THERM_1T01_55S	CPU THMSNS D2 P
	SENSE_DIFFPAIR	THERM_1T01_55S	CPU THMSNS D2 N
	SENSE_DIFFPAIR	THERM_1T01_55S	CPU THERMD P
	SENSE_DIFFPAIR	THERM_1T01_55S	CPU THERMD N
	SENSE_DIFFPAIR	THERM_1T01_55S	GPU THMSNS D P
	SENSE_DIFFPAIR	THERM_1T01_55S	GPU THMSNS D N
	SENSE_DIFFPAIR	THERM_1T01_55S	GPU TDIODE P
	SENSE_DIFFPAIR	THERM_1T01_55S	GPU TDIODE N
	SENSE_DIFFPAIR	SENSE_1T01_55S	CPUVTTISNS R N
	SENSE_DIFFPAIR	SENSE_1T01_55S	CPUVTTISNS R P
	SENSE_DIFFPAIR	SENSE_1T01_55S	CPUVTTIS0 CS N
	SENSE_DIFFPAIR	SENSE_1T01_55S	CPUVTTIS0 CS P
	SENSE_DIFFPAIR	SENSE_1T01_55S	DDRISNS R N
	SENSE_DIFFPAIR	SENSE_1T01_55S	DDRISNS R P
	SENSE_DIFFPAIR	SENSE_1T01_55S	GFXIMVP CS N
	SENSE_DIFFPAIR	SENSE_1T01_55S	GFXIMVP CS P
	SENSE_DIFFPAIR	SENSE_1T01_55S	GFXIMVP CS R N
	SENSE_DIFFPAIR	SENSE_1T01_55S	GFXIMVP CS R P
	SENSE_DIFFPAIR	SENSE_1T01_55S	GFX ISNS R N
	SENSE_DIFFPAIR	SENSE_1T01_55S	GFX ISNS R P
	SENSE_DIFFPAIR	SENSE_1T01_55S	GPUISENS N
	SENSE_DIFFPAIR	SENSE_1T01_55S	GPUISENS P
	SENSE_DIFFPAIR	SENSE_1T01_55S	ISNS_1V5_S3 N
	SENSE_DIFFPAIR	SENSE_1T01_55S	ISNS_1V5_S3 P
	SENSE_DIFFPAIR	SENSE_1T01_55S	ISNS AIRPORT N
	SENSE_DIFFPAIR	SENSE_1T01_55S	ISNS AIRPORT N
	SENSE_DIFFPAIR	SENSE_1T01_55S	ISNS AIRPORT P
	SENSE_DIFFPAIR	SENSE_1T01_55S	ISNS AIRPORT P
	SENSE_DIFFPAIR	SENSE_1T01_55S	ISNS AIRPORT R N
	SENSE_DIFFPAIR	SENSE_1T01_55S	ISNS AIRPORT R P
	SENSE_DIFFPAIR	SENSE_1T01_55S	ISNS CPU N
	SENSE_DIFFPAIR	SENSE_1T01_55S	ISNS CPU P
	SENSE_DIFFPAIR	SENSE_1T01_55S	ISNS HDD N
	SENSE_DIFFPAIR	SENSE_1T01_55S	ISNS HDD P
	SENSE_DIFFPAIR	SENSE_1T01_55S	ISNS HDD R N
	SENSE_DIFFPAIR	SENSE_1T01_55S	ISNS HDD R P
	SENSE_DIFFPAIR	SENSE_1T01_55S	ISNS LCDBKLT N
	SENSE_DIFFPAIR	SENSE_1T01_55S	ISNS LCDBKLT P
	SENSE_DIFFPAIR	SENSE_1T01_55S	ISNS ODD N
	SENSE_DIFFPAIR	SENSE_1T01_55S	ISNS ODD P
	SENSE_DIFFPAIR	SENSE_1T01_55S	ISNS ODD R N
	SENSE_DIFFPAIR	SENSE_1T01_55S	ISNS ODD R P
	SENSE_DIFFPAIR	SENSE_1T01_55S	ISNS P1V8GPU N
	SENSE_DIFFPAIR	SENSE_1T01_55S	ISNS P1V8GPU P
	SENSE_DIFFPAIR	SENSE_1T01_55S	ISNS P1V8GPU R N
	SENSE_DIFFPAIR	SENSE_1T01_55S	ISNS P1V8GPU R P

K18 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
	PCIE_CLK100M_AP	CLK_PCIE_90D	PCIE_CLK100M_AP_CONN_P
		CLK_PCIE_90D	PCIE_CLK100M_AP_CONN_N
		1T01_DIFFPAIR	CHGR_CSI_R_P
		1T01_DIFFPAIR	CHGR_CSI_R_N
		1T01_DIFFPAIR	CHGR_CSO_R_P
		1T01_DIFFPAIR	CHGR_CSO_R_N
	(USB_EXTN)	USB_85D	USB2_EXTN_MUXED_P
	(USB_EXTN)	USB_85D	USB2_EXTN_MUXED_N
	(USB_EXTN)	USB_85D	USB2_LT1_P
	(USB_EXTN)	USB_85D	USB2_LT1_N
		USB_85D	CONN_USB2_BT_P
		USB_85D	CONN_USB2_BT_N
		USB_85D	USB_LT2_P
		USB_85D	USB_LT2_N
	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_C_P
	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_C_N
	SPK_OUT	DIFFPAIR	SPKRCONN_L_OUT_P
	SPK_OUT	DIFFPAIR	SPKRCONN_L_OUT_N
	SPK_OUT	DIFFPAIR	SPKRCONN_R_OUT_P
	SPK_OUT	DIFFPAIR	SPKRCONN_R_OUT_N
	SPK_OUT	DIFFPAIR	SPKRCONN_S_OUT_P
	SPK_OUT	DIFFPAIR	SPKRCONN_S_OUT_N
		USB_85D	USB_TPAD_R_P
		USB_85D	USB_TPAD_R_N
		SB_POWER	PP3V3_S5
		SB_POWER	PP3V3_S0
		SB_POWER	PP1V5_S3RS0
		GND	GND

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Project Specific Constraints			
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K18 Board-Specific Spacing & Physical Constraints

BOARD LAYERS				BOARD AREAS			BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM				NO_TYPE, BGA			MM	15.5.1
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM	
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
55_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM				
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
50_OHM_SE	TOP, BOTTOM	Y	0.110 MM	0.095 MM				
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
40_OHM_SE	TOP, BOTTOM	Y	0.165 MM	0.095 MM				
40_OHM_SE	*	Y	0.135 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
37_OHM_SE	TOP, BOTTOM	Y	0.185 MM	0.095 MM				
37_OHM_SE	*	Y	0.155 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
27P4_OHM_SE	TOP, BOTTOM	Y	0.310 MM	0.095 MM				
27P4_OHM_SE	*	Y	0.250 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD	

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	
72_OHM_DIFF	ISL3, ISL4	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM	
72_OHM_DIFF	ISL9, ISL10	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM	
72_OHM_DIFF	TOP, BOTTOM	Y	0.175 MM	0.175 MM		0.200 MM	0.200 MM	

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	
85_OHM_DIFF	ISL3, ISL4	Y	0.110 MM	0.090 MM		0.180 MM	0.180 MM	
85_OHM_DIFF	ISL9, ISL10	Y	0.110 MM	0.090 MM		0.180 MM	0.180 MM	
85_OHM_DIFF	TOP, BOTTOM	Y	0.125 MM	0.090 MM		0.190 MM	0.190 MM	

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	
90_OHM_DIFF	ISL3, ISL4	Y	0.102 MM	0.090 MM		0.220 MM	0.220 MM	
90_OHM_DIFF	ISL9, ISL10	Y	0.102 MM	0.090 MM		0.220 MM	0.220 MM	
90_OHM_DIFF	TOP, BOTTOM	Y	0.115 MM	0.090 MM		0.230 MM	0.230 MM	

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	
100_OHM_DIFF	ISL3, ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM	
100_OHM_DIFF	ISL9, ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM	
100_OHM_DIFF	TOP, BOTTOM	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM	

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	
110_OHM_DIFF	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM	
110_OHM_DIFF	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM	
110_OHM_DIFF	TOP, BOTTOM	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM	

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	
DEFAULT	*	0.1 MM	?	
STANDARD	*	=DEFAULT	?	
BGA_P1MM	*	=DEFAULT	?	
BGA_P2MM	*	=DEFAULT	?	

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	
1.5:1_SPACING	*	0.15 MM	?	
2:1_SPACING	*	0.2 MM	?	
2.5:1_SPACING	*	0.25 MM	?	
3:1_SPACING	*	0.3 MM	?	
4:1_SPACING	*	0.4 MM	?	

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	
*	*	BGA	BGA_P1MM	
MEM_CLK	*	BGA	BGA_P2MM	
CLK_PCIE	*	BGA	BGA_P2MM	
CLK_SLOW	*	BGA	BGA_P2MM	


SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	
2X_DIELECTRIC	*	0.140 MM	?	
3X_DIELECTRIC	*	0.210 MM	?	
4X_DIELECTRIC	*	0.280 MM	?	

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM	

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	
100_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM	
100_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM	

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

NOTE: 110_DIFF is 110-ohms differential impedance on outer layers and 105-ohms on inner layers.

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