

SCHEM, CORNHOLE, K19

PVT 04/24/2009

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
?		?	?	?	?

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

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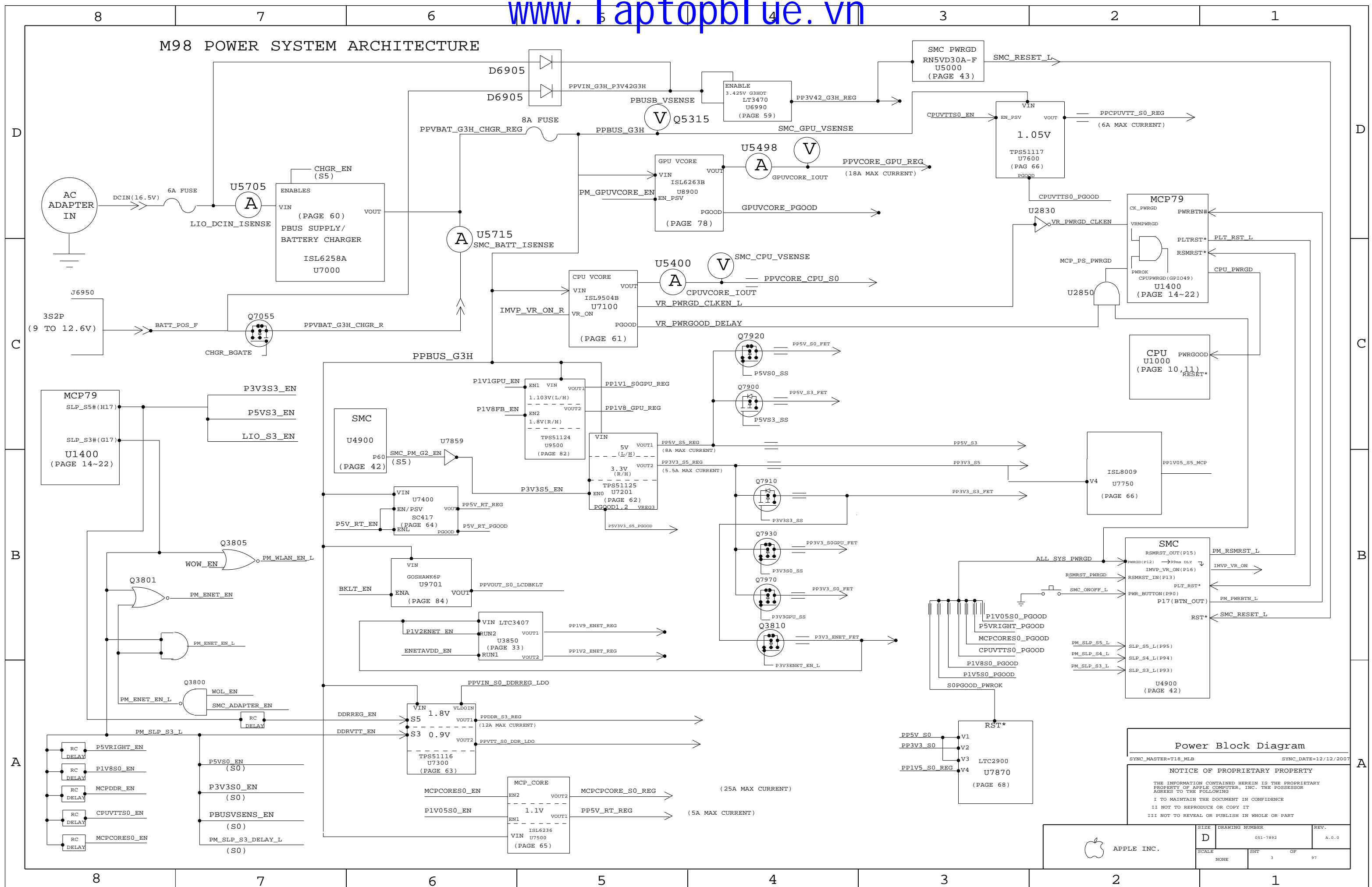
ALIASES RESOLVED

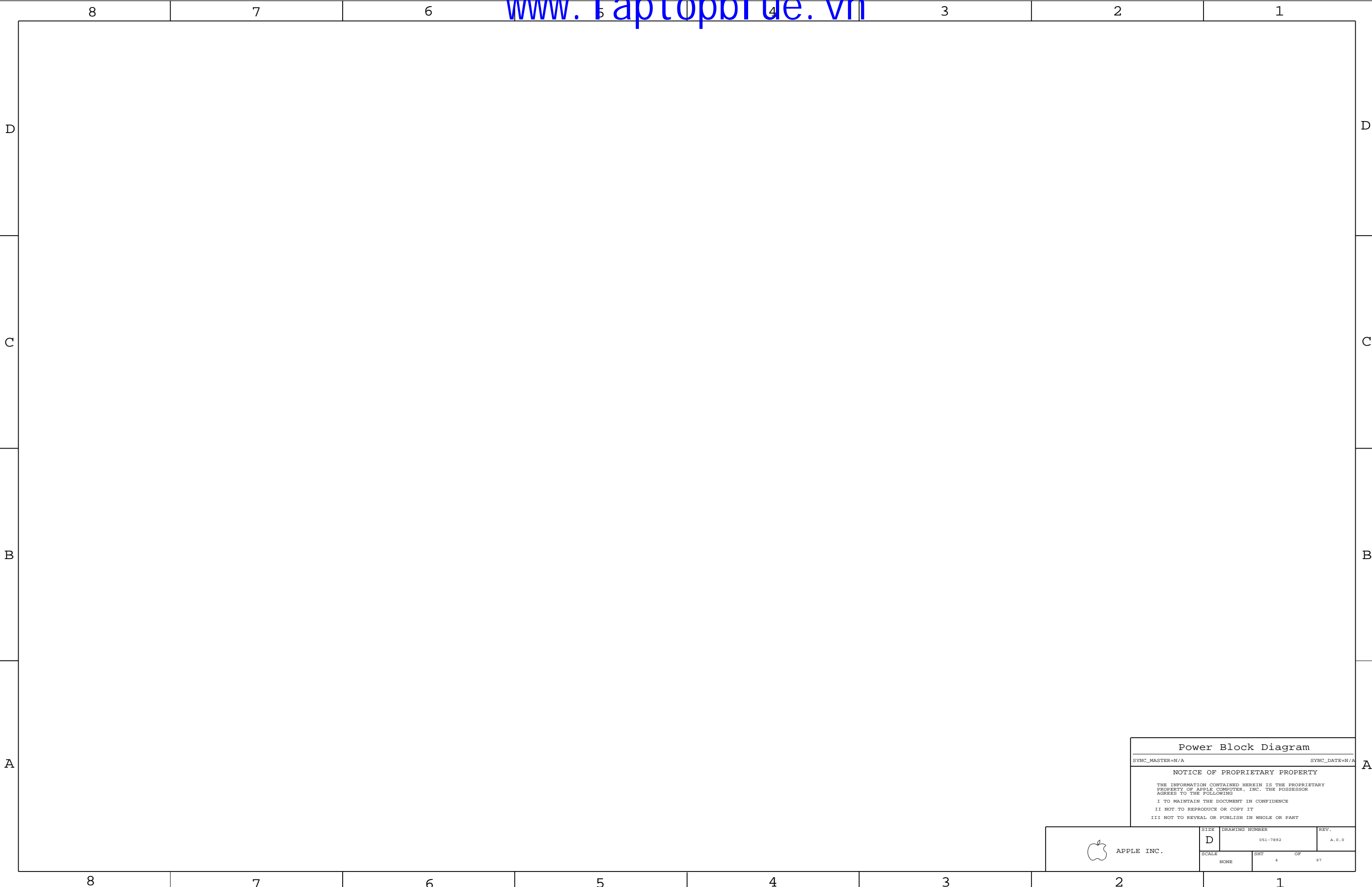
Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7892	1	SCHEM,CORNHOLE,K19	SCH	CRITICAL	
820-2523	1	PCBF,CORNHOLE,K19	PCB	CRITICAL	


DRAWING
TITLE:MLB
LAST_MODIFIED=Fri Apr 24 15:23:24 2009

DIMENSIONS ARE IN MILLIMETERS XX ± _____ X.XX ± _____ X.XXX ± _____ ANGLES ± _____ DO NOT SCALE DRAWING  THIRD ANGLE PROJECTION	METRIC		 APPLE INC.	
	DRAFTER	DESIGN CK	NOTICE OF PROPRIETARY PROPERTY THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING I. TO MAINTAIN THE DOCUMENT IN CONFIDENCE II. NOT TO REPRODUCE OR COPY IT III. NOT TO REVEAL OR PUBLISH IN WHOLE OR PART	
	ENG APPD	MFG APPD	TITLE	
	QA APPD	DESIGNER	SCHEM,MBP 15MLB	
	RELEASE	SCALE NONE	DRAWING NUMBER	REV.
MATERIAL/FINISH NOTED AS APPLICABLE		SIZE D	051-7892	A.0.0
SHT 1 OF 97				





Power Block Diagram			
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	SCALE NONE	SHT 4 OF 97	

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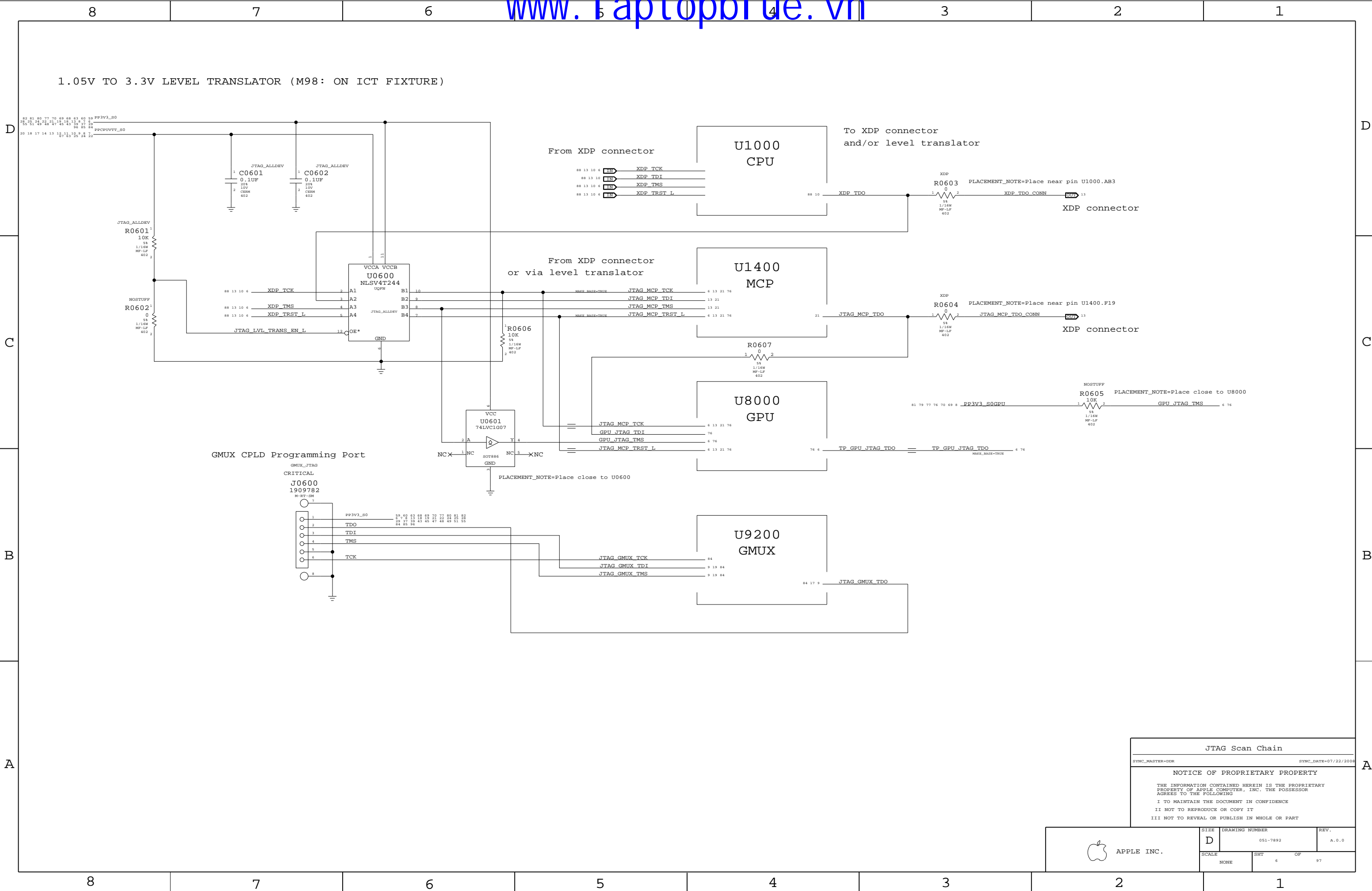
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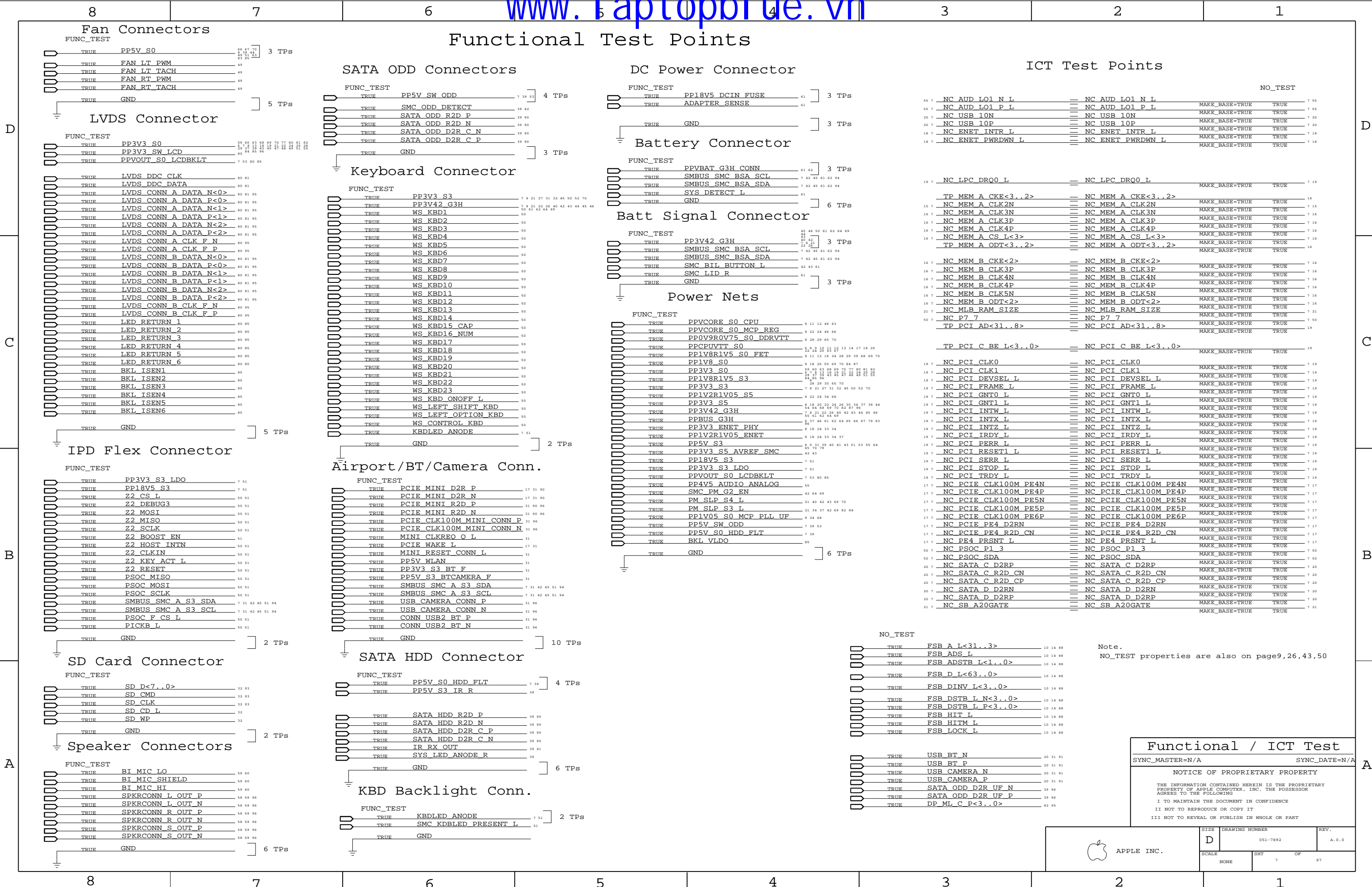
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Functional Test Points



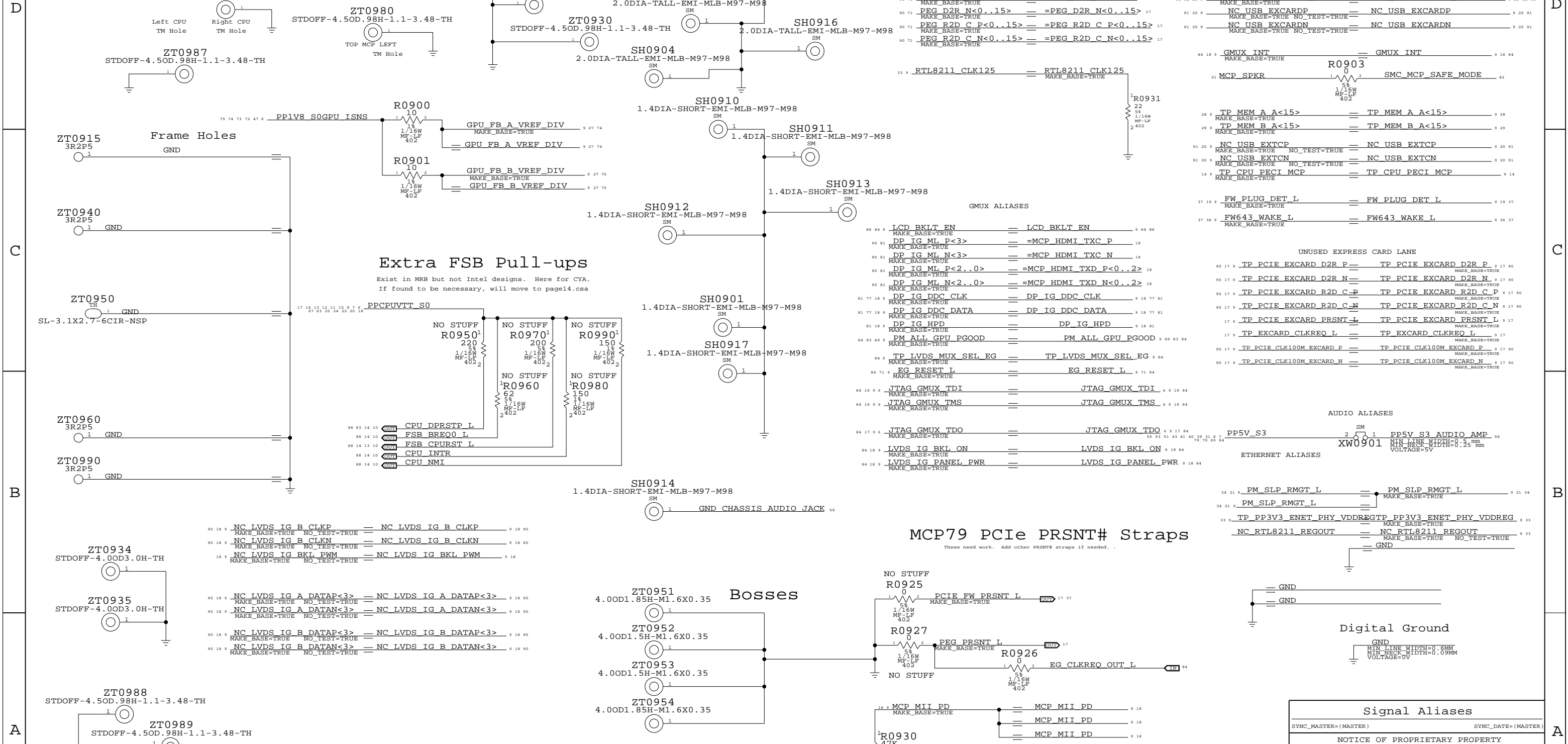
Note.
NO_TEST properties are also on page9,26,43,50

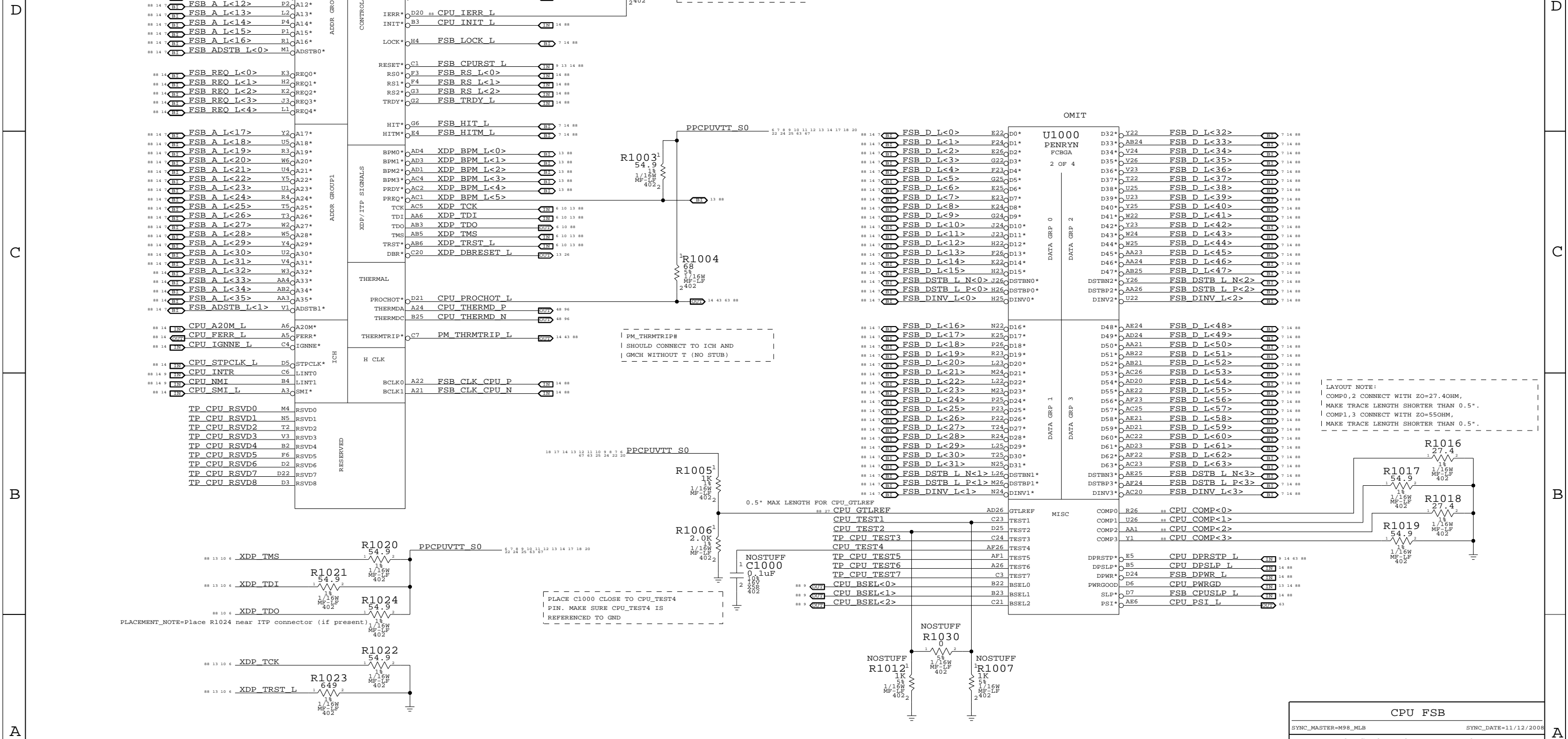
Functional / ICT Test

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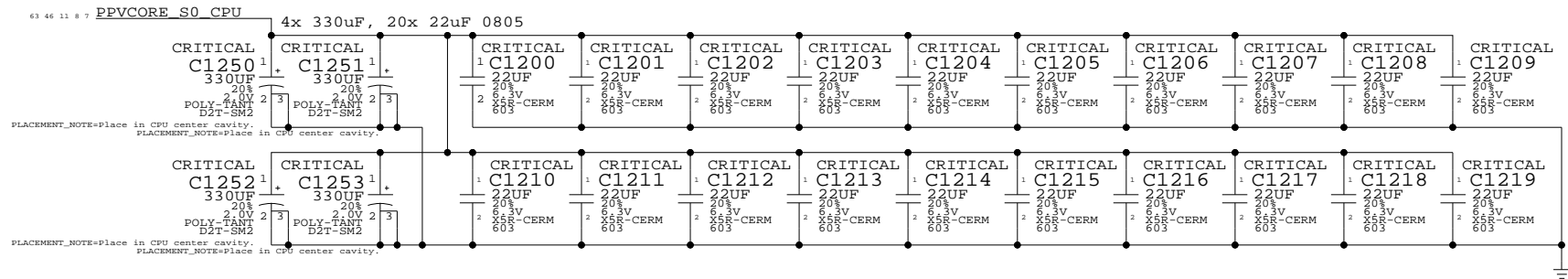
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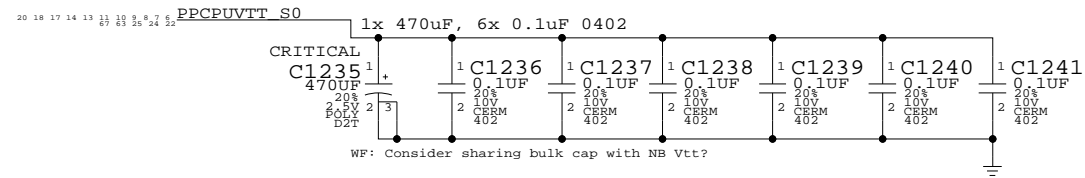




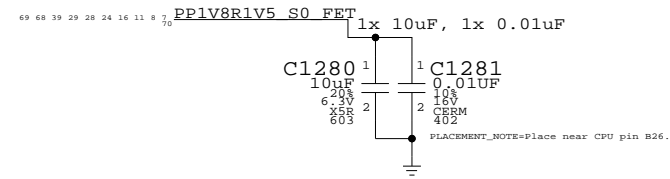
CPU VCORE HF AND BULK DECOUPLING



VCCP (CPU I/O) DECOUPLING



VCCA (CPU AVdd) DECOUPLING



CPU Decoupling & VID

SYNC_MASTER=M87_MLB SYNC_DATE=10/17/2007

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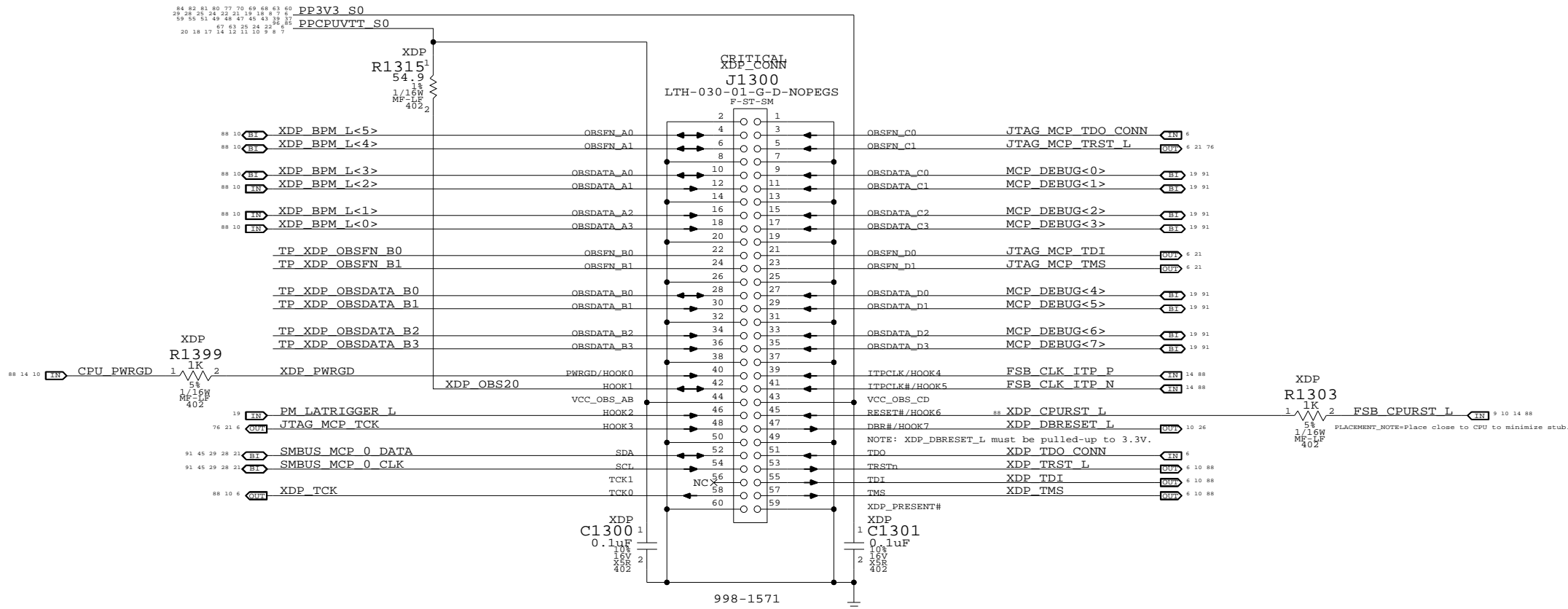
OF

97

Mini-XDP Connector

NOTE: This is not the standard XDP pinout.
Use with 920-0620 adapter board to support CPU, MCP debugging.

MCP79-specific pinout



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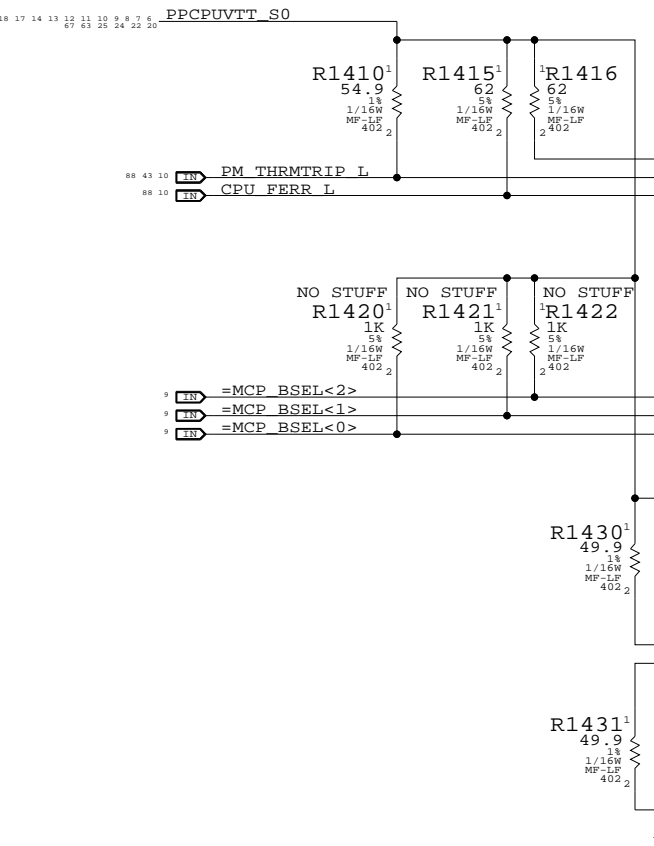
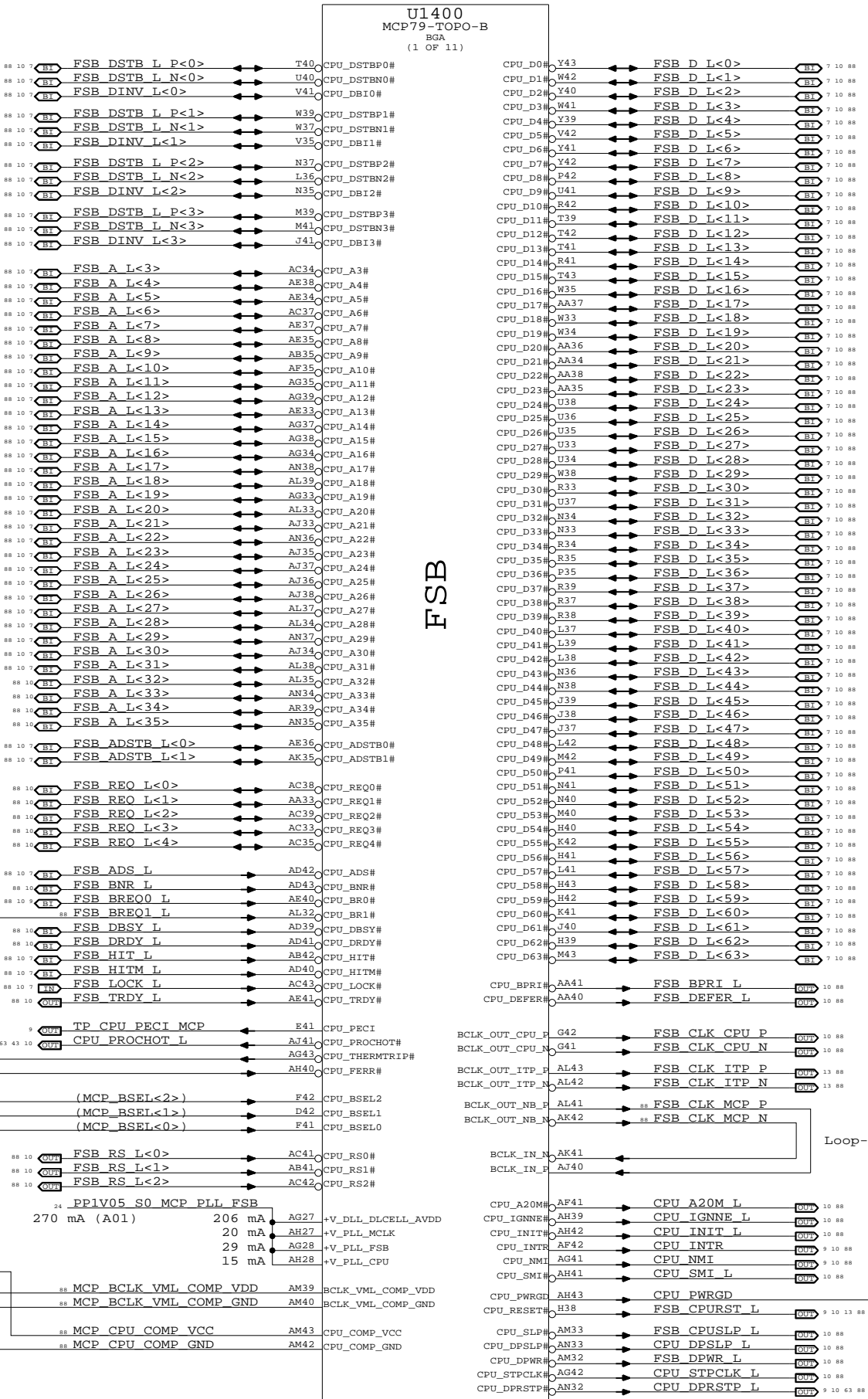
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Loop-back clock for delay matching.

MCP CPU Interface

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2008

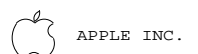
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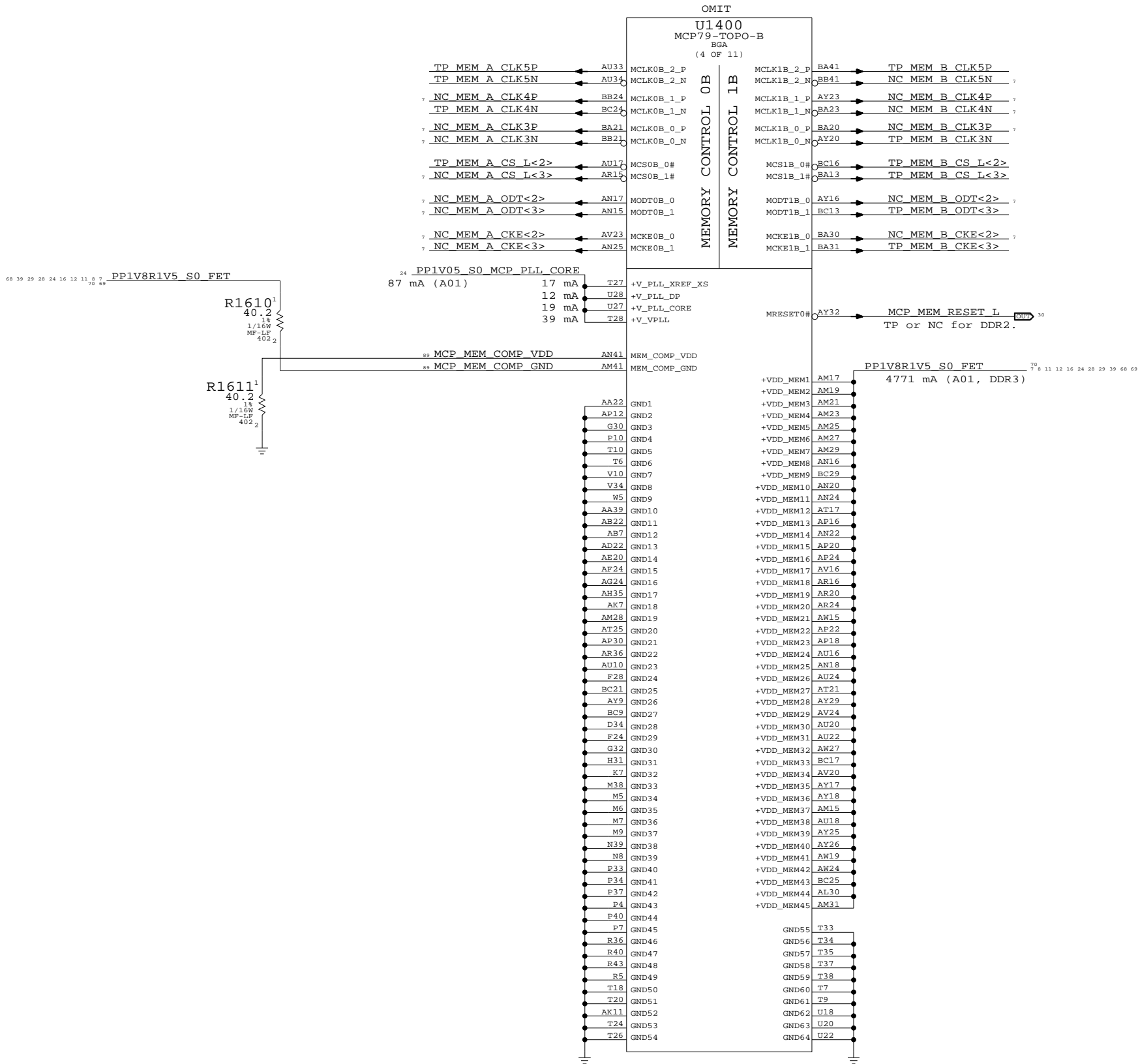
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MCP Memory Misc

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2008

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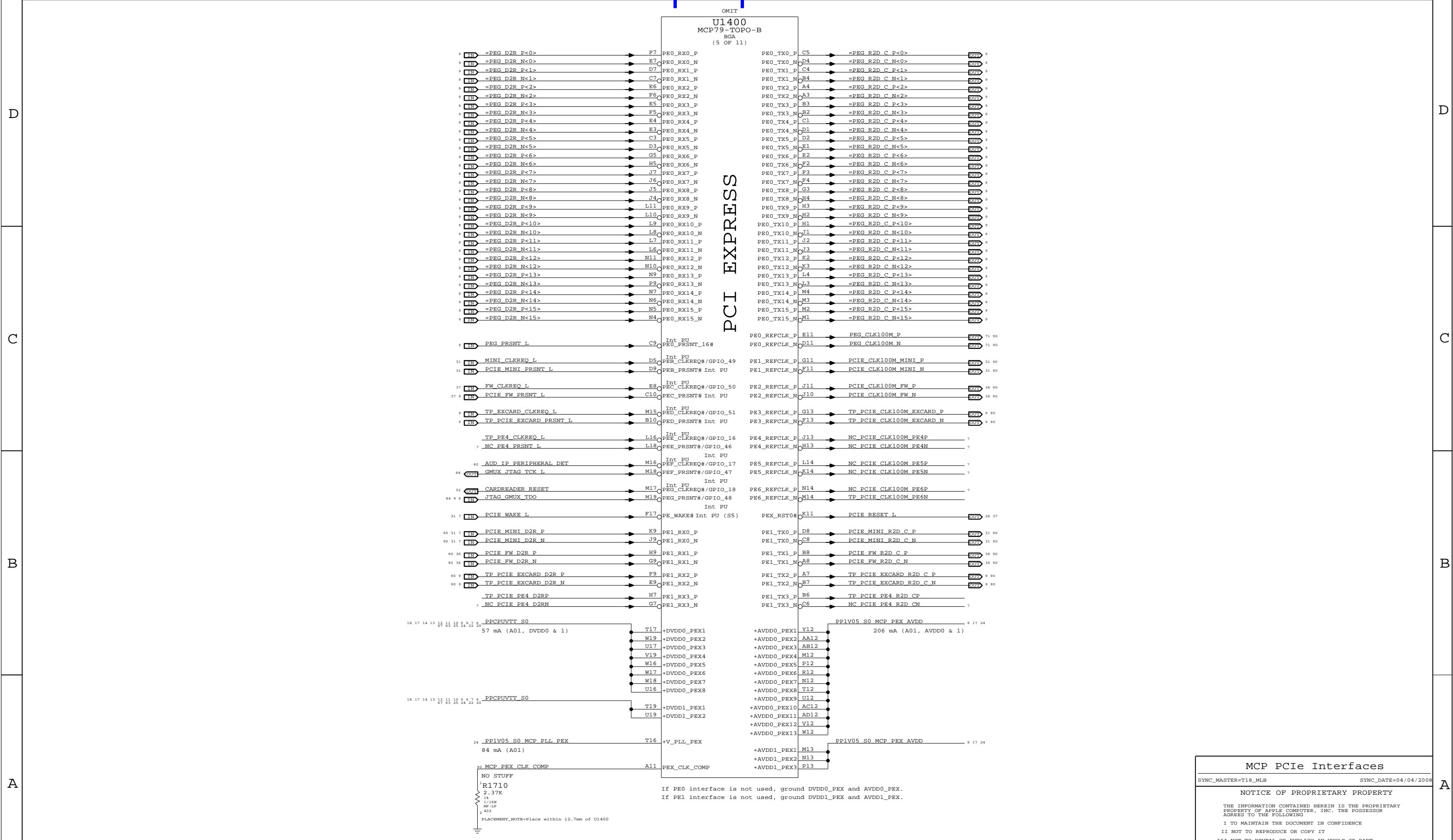
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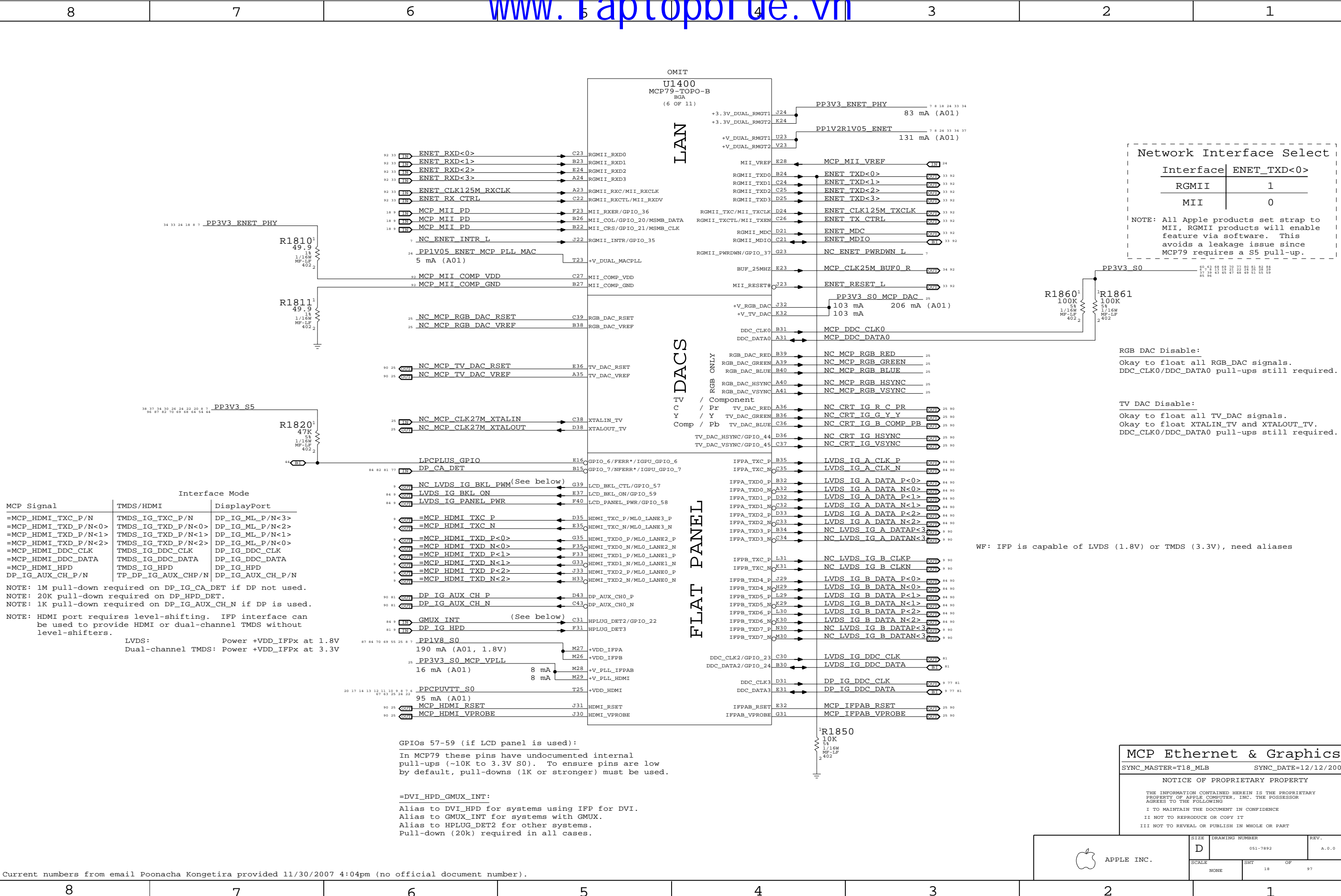
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Network Interface Select	
Interface	ENET_TXD<0>
RGMII	1
MII	0

NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

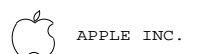
RGB DAC Disable:
Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required.

TV DAC Disable:
Okay to float all TV_DAC signals.
Okay to float XTALIN_TV and XTALOUT_TV.
DDC_CLK0/DDC_DATA0 pull-ups still required.

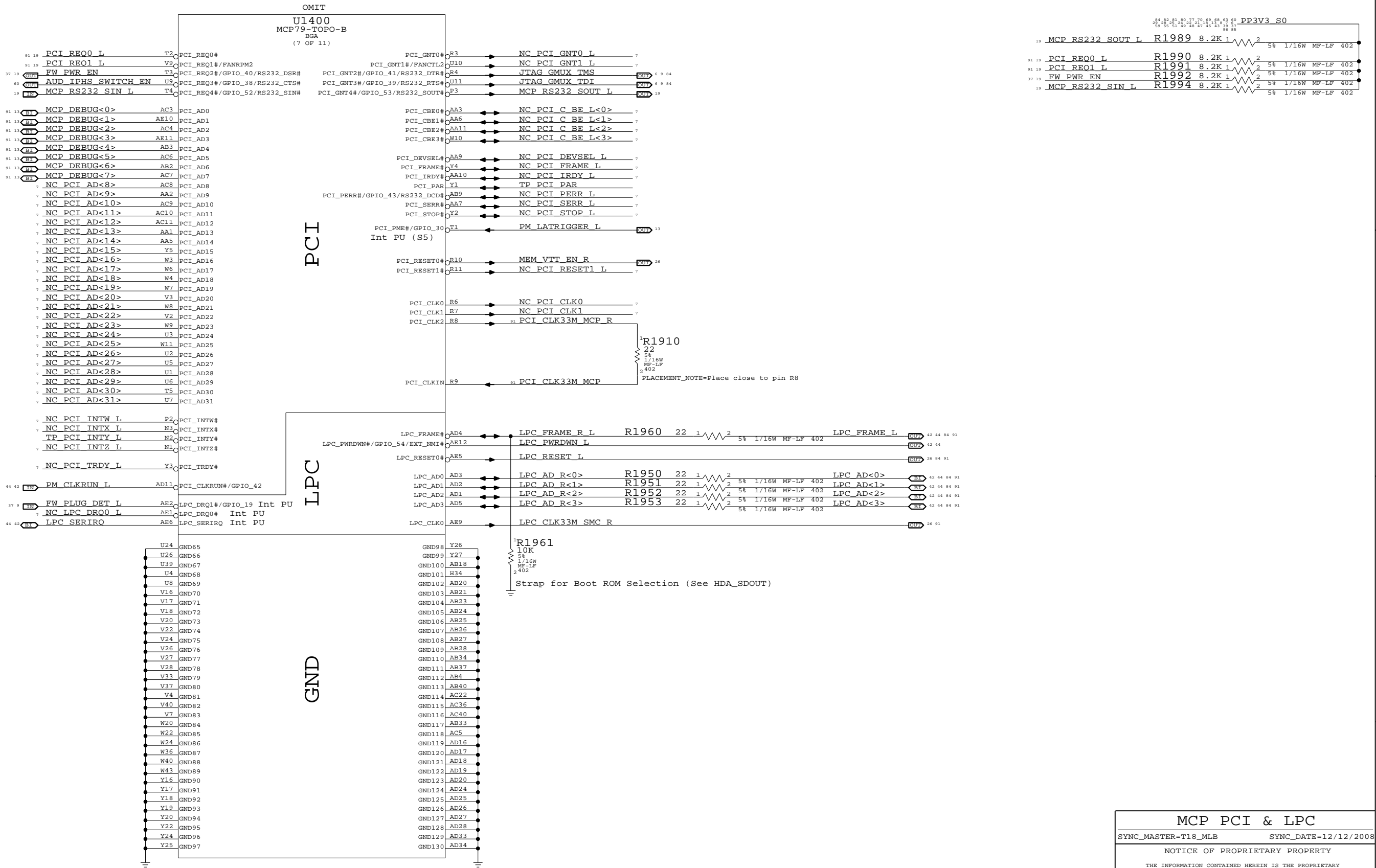
WF: IFP is capable of LVDS (1.8V) or TMDS (3.3V), need aliases

MCP Ethernet & Graphics	
SYNC_MASTER=T18_MLB	SYNC_DATE=12/12/2008
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MCP PCI & LPC

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2008

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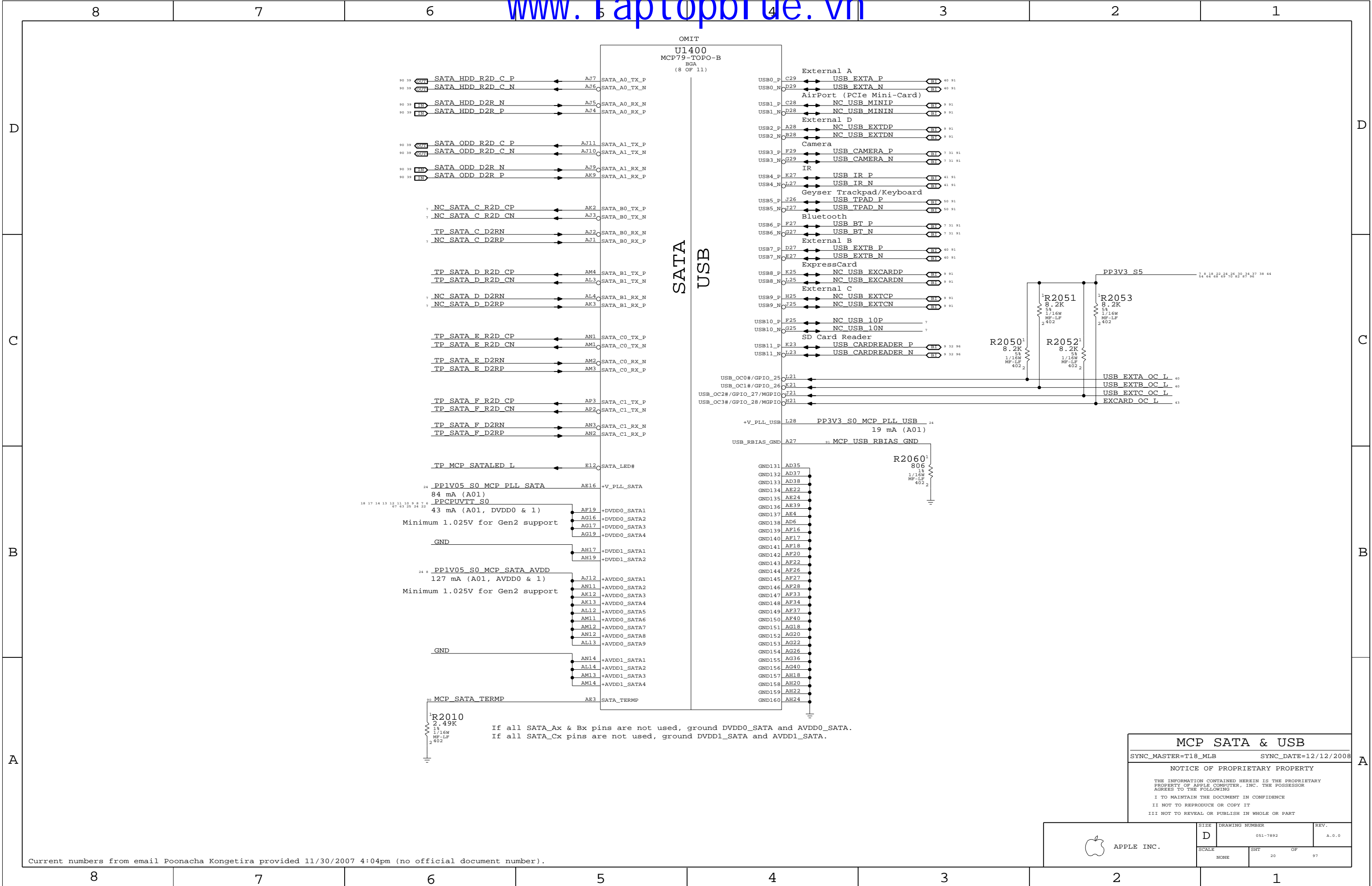
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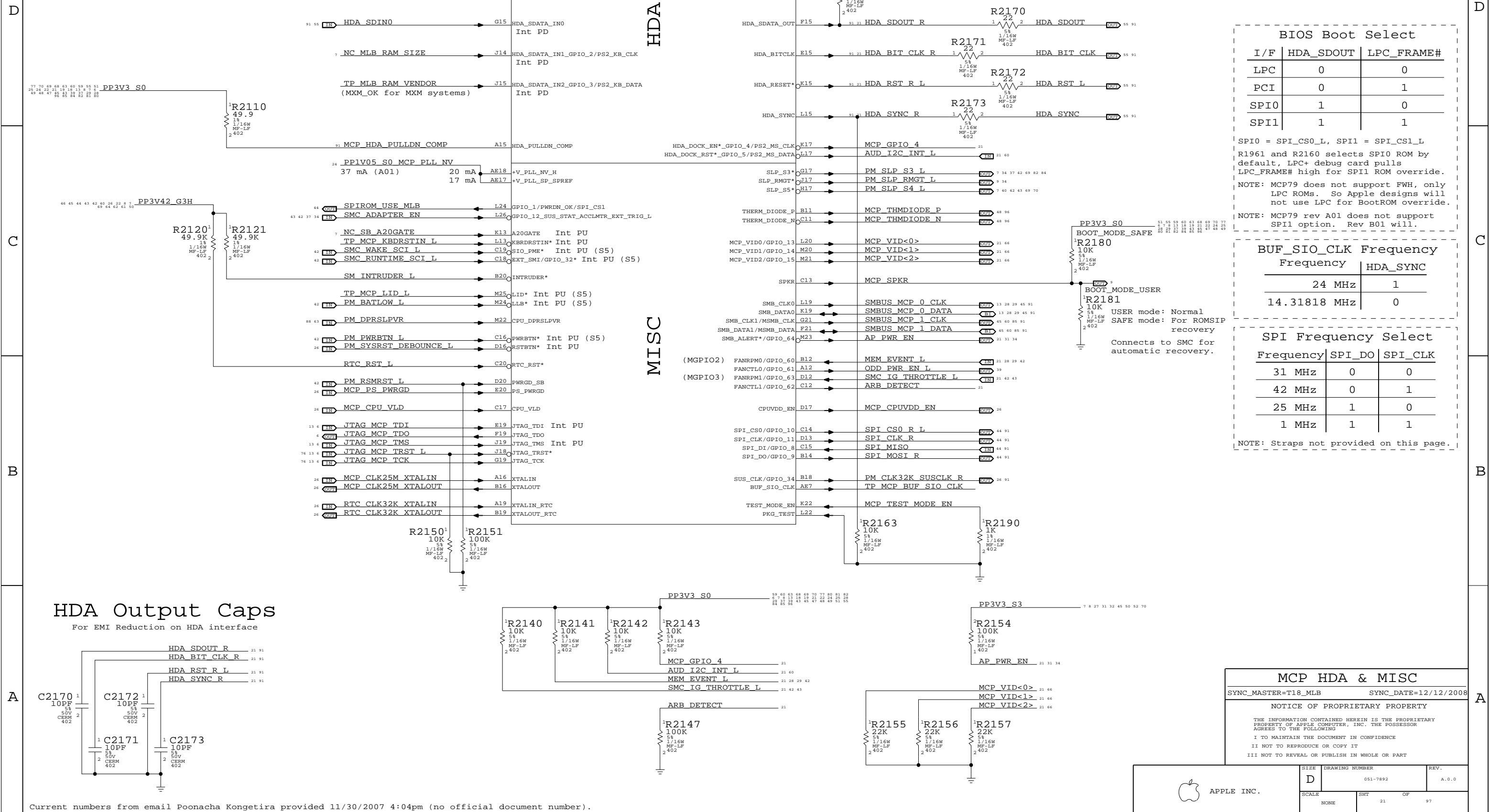
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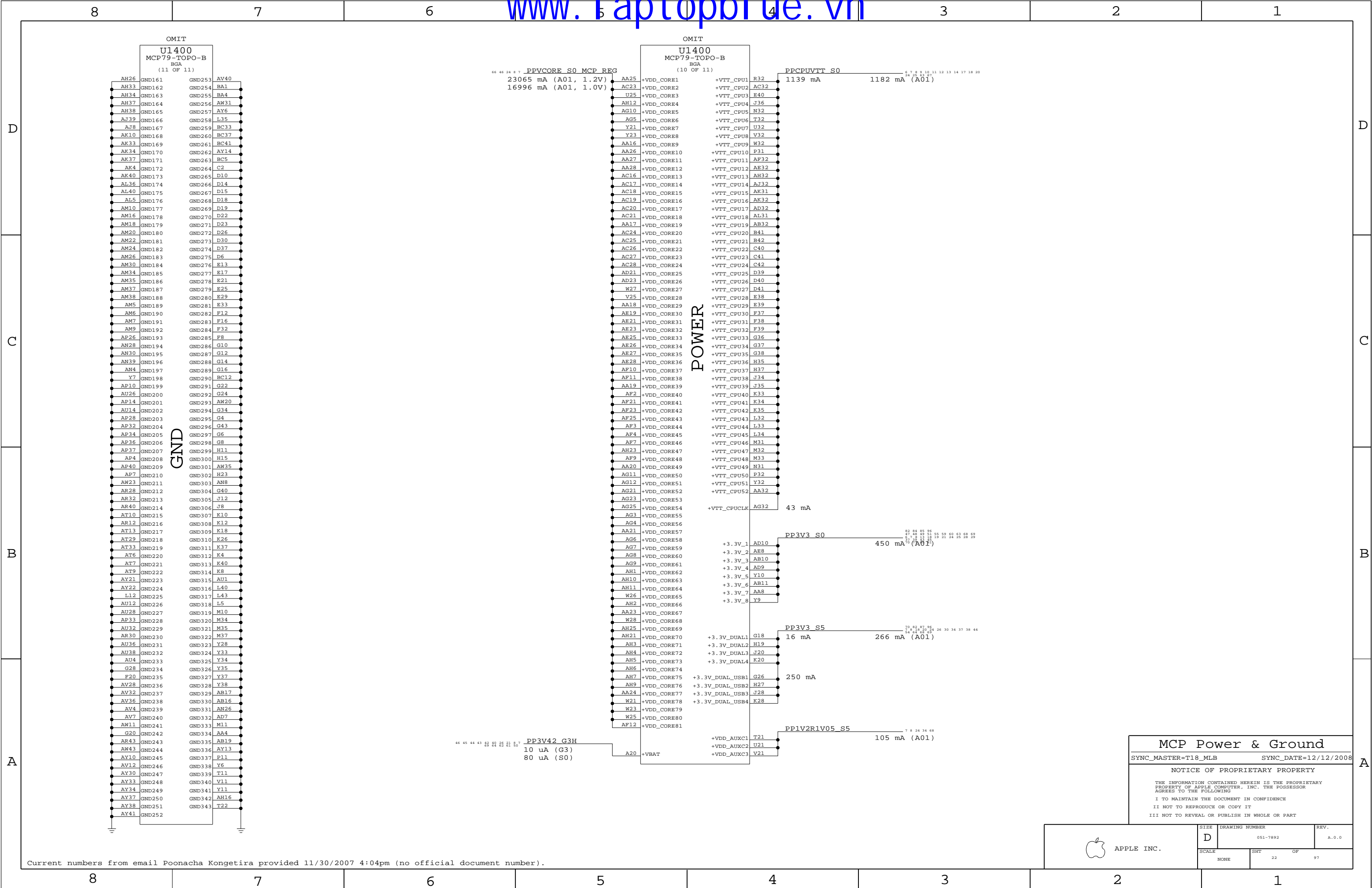
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	NONE	19	97







MCP Power & Ground

SYNC_MASTER=T18_MLB

SYNC_DATE=12/12/2008

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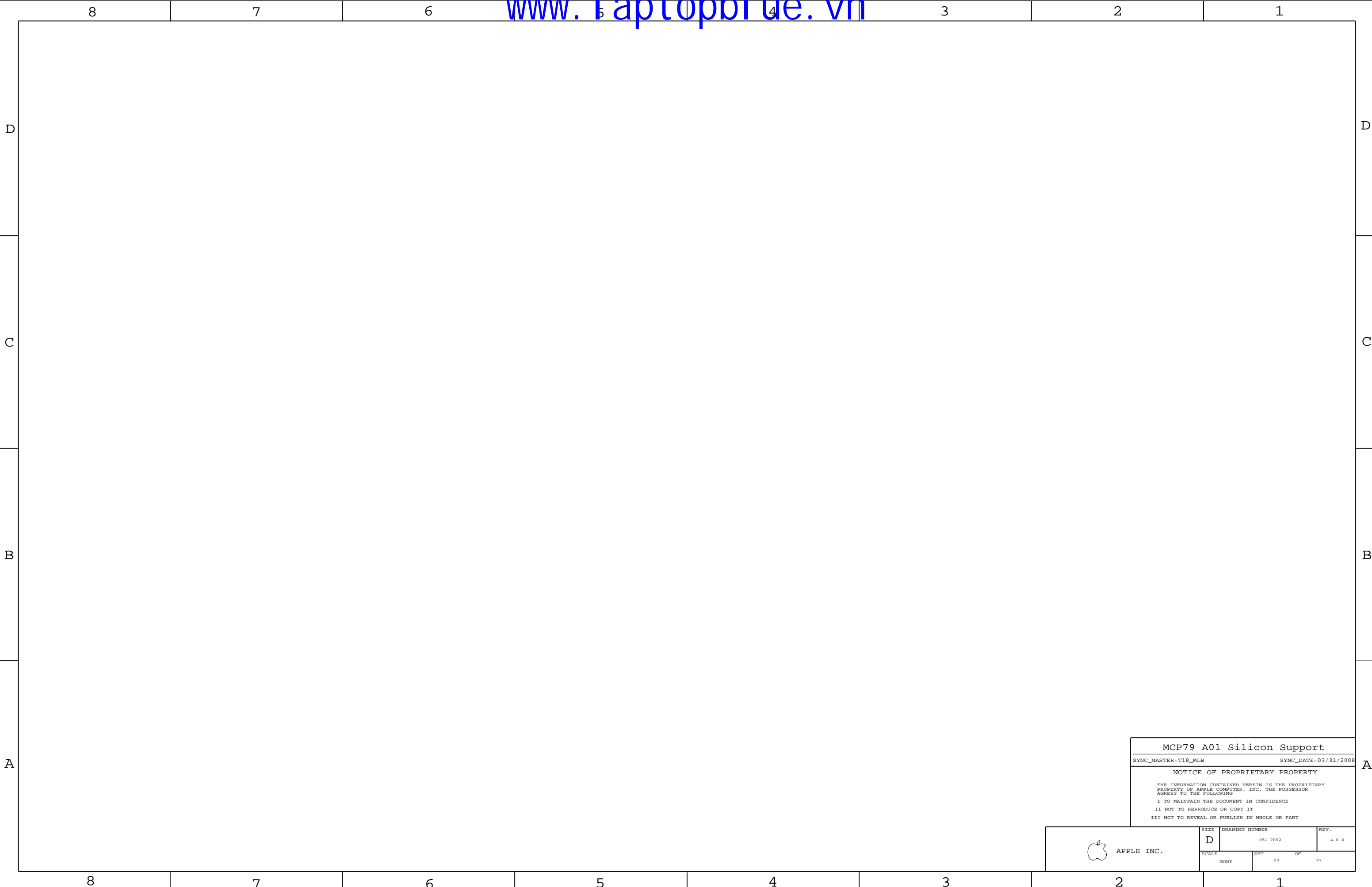
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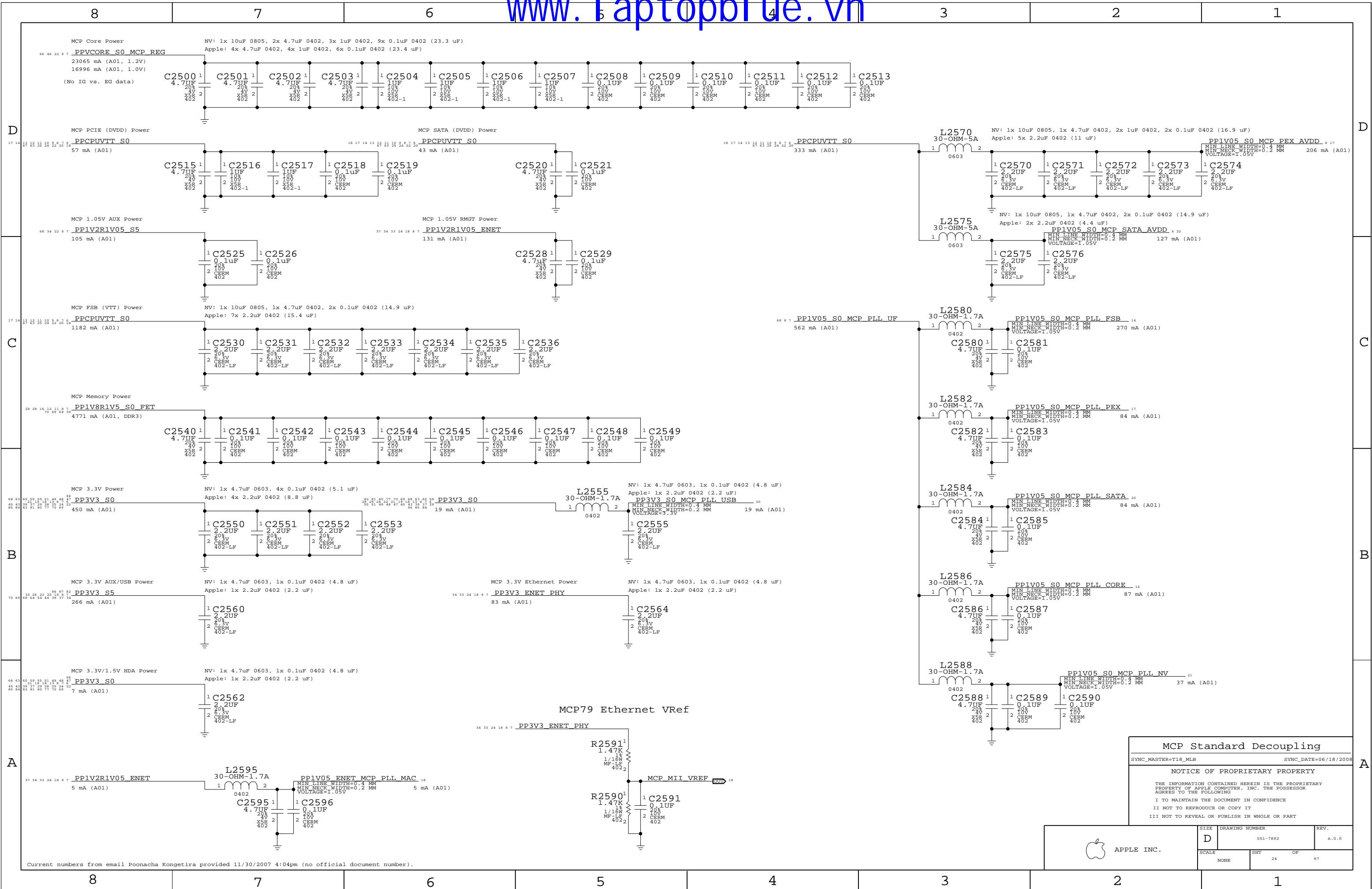
SCALE
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MCP79 A01 Silicon Support			
SYNC_MASTER=T18_MLB		SYNC_DATE=03/31/2008	
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	SCALE NONE	SHT 23 OF 97	



Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP Standard Decoupling

SYNC_MASTER=T18_MLB

SYNC_DATE=06/18/2008

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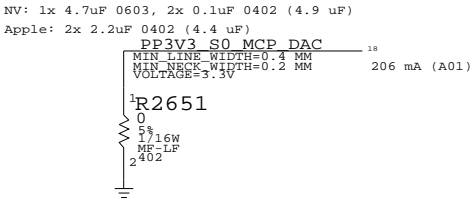
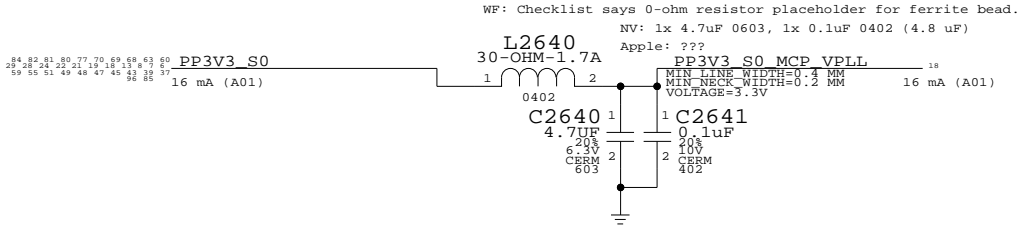
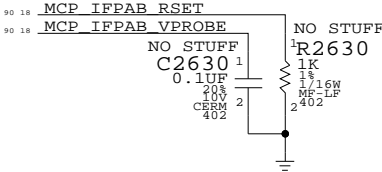
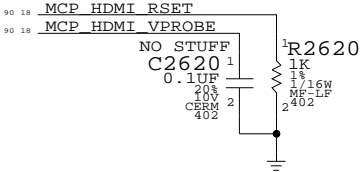
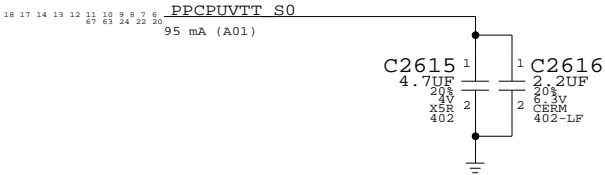
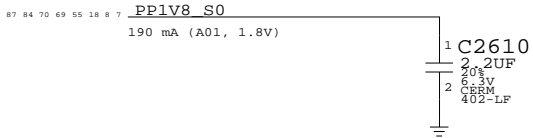
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WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)



25 18	NC MCP RGB RED	==	NC MCP RGB RED	18 25
25 18	NC MCP RGB GREEN	==	MAKE_BASE=TRUE NO_TEST=TRUE	18 25
25 18	NC MCP RGB BLUE	==	MAKE_BASE=TRUE NO_TEST=TRUE	18 25
25 18	NC MCP RGB HSYNC	==	MAKE_BASE=TRUE NO_TEST=TRUE	18 25
25 18	NC MCP RGB VSYNC	==	MAKE_BASE=TRUE NO_TEST=TRUE	18 25
90 25 18	NC CRT IG R C PR	==	NC CRT IG R C PR	18 25 90
90 25 18	NC CRT IG G Y Y	==	MAKE_BASE=TRUE NO_TEST=TRUE	18 25 90
90 25 18	NC CRT IG B COMP PB	==	MAKE_BASE=TRUE NO_TEST=TRUE	18 25 90
90 25 18	NC CRT IG HSYNC	==	MAKE_BASE=TRUE NO_TEST=TRUE	18 25 90
90 25 18	NC CRT IG VSYNC	==	MAKE_BASE=TRUE NO_TEST=TRUE	18 25 90
25 18	NC MCP RGB DAC RSET	==	NC MCP RGB DAC RSET	18 25
25 18	NC MCP RGB DAC VREF	==	MAKE_BASE=TRUE NO_TEST=TRUE	18 25
90 25 18	NC MCP TV DAC RSET	==	MAKE_BASE=TRUE NO_TEST=TRUE	18 25 90
90 25 18	NC MCP TV DAC VREF	==	MAKE_BASE=TRUE NO_TEST=TRUE	18 25 90
25 18	NC MCP CLK27M XTALIN	==	NC MCP CLK27M XTALIN	18 25
25 18	NC MCP CLK27M XTALOUT	==	MAKE_BASE=TRUE NO_TEST=TRUE	18 25

MCP Graphics Support

SYNC_MASTER=AMASON_M98_MLB SYNC_DATE=06/18/2008

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APPLE INC.

SIZE

D

DRAWING NUMBER

051-7892

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A.0.0

SCALE

NONE

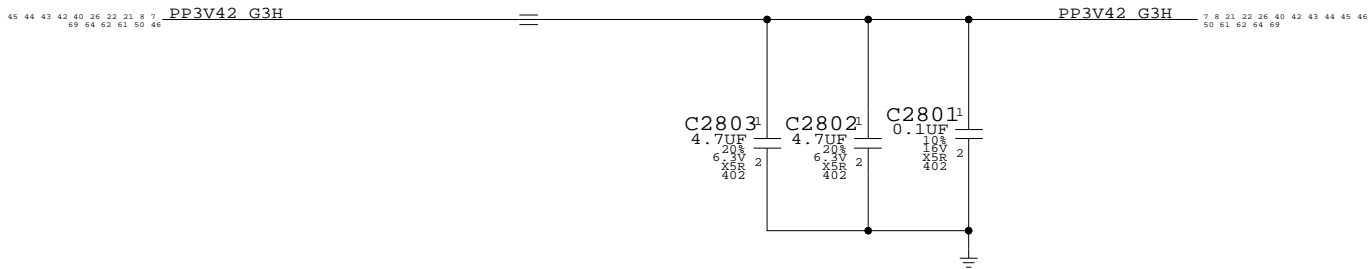
SHT

25

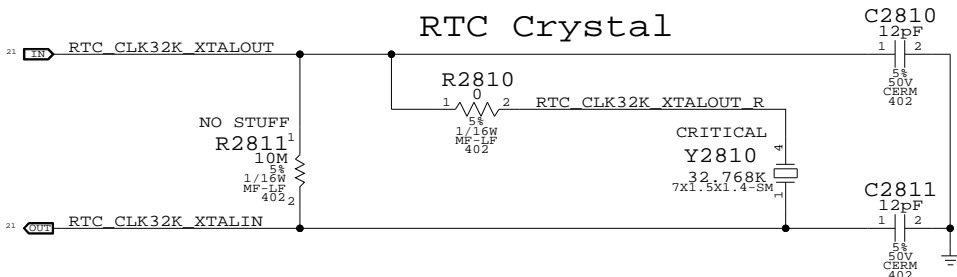
OF

97

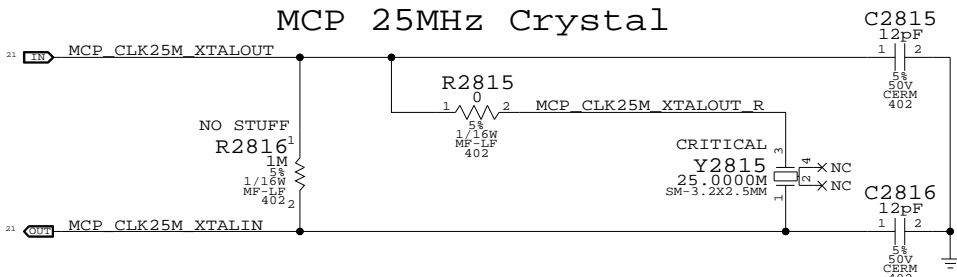
RTC Power Sources



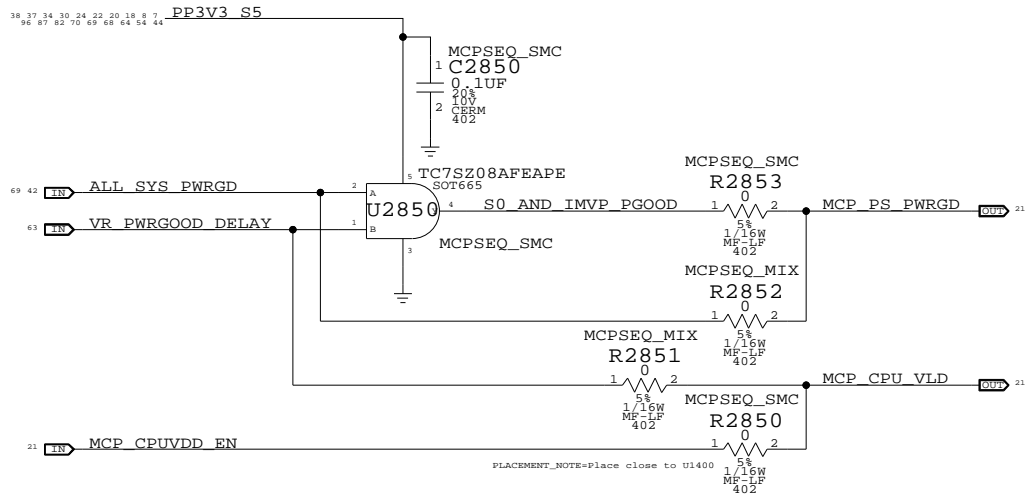
RTC Crystal



MCP 25MHz Crystal



MCP S0 PWRGD & CPU_VLD



MCPSEQ_SMC represents MCP79 'MLB' power sequencing connections, but results in MCP79 ROMSIP sequence happening after CPU powers up.

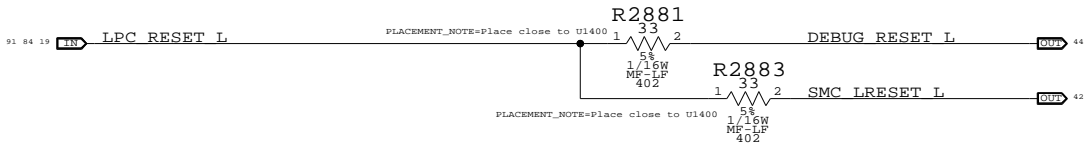
MCPSEQ_MIX is cross between MLB and internal power sequencing, which results in earlier ROMSIP and MCP FSB I/O interface initialization.

SMC 99ms delay from ALL_SYS_PWRGD to IMVP_VR_ON plus IMVP6 delay for VR_PWRGOOD_DELAY should guarantee CPU_VLD does not go high before CPUVDD_EN (which is 40-100ms after PS_PWRGD assertion).

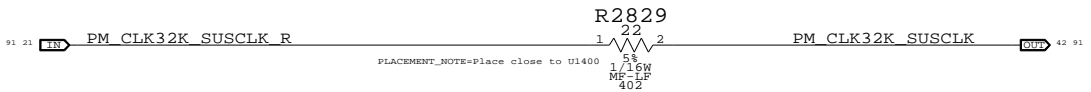
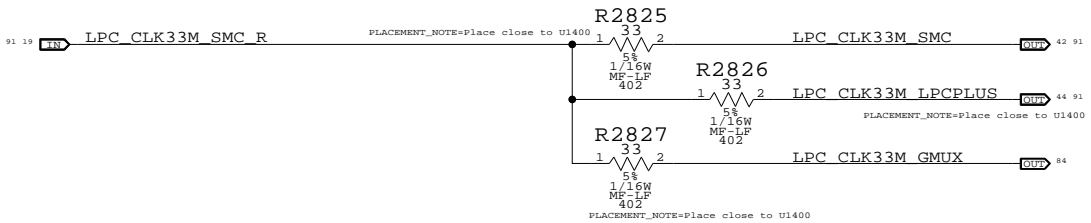
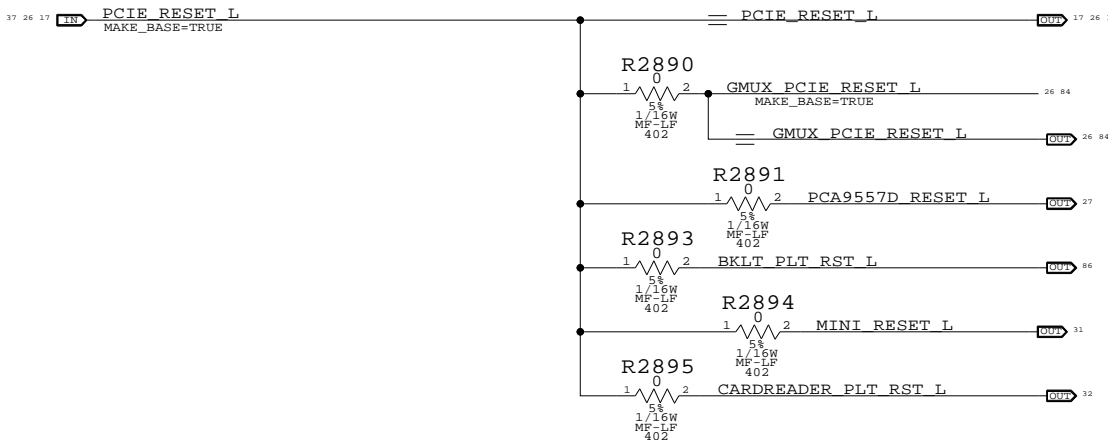
NOTE: If CPU_VLD deasserts during S0 MCP79 will take system to S5 immediately.

Platform Reset Connections

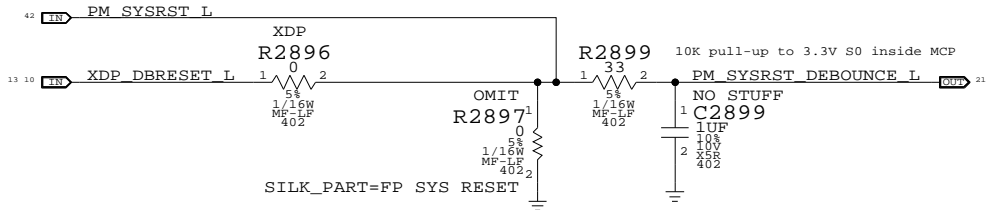
LPC Reset (Unbuffered)



PCIE Reset (Unbuffered)



Reset Button



SB Misc

SYNC_MASTER=DDR SYNC_DATE=12/15/2008

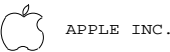
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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE	SHT	OF
NONE	26	97

D

```
- =PP3V3_S3_VREFMRGN
- =PP3V3_S5_VREFMRGN
- =PPVTT_S3_DDR_BUF
```

```
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA
```

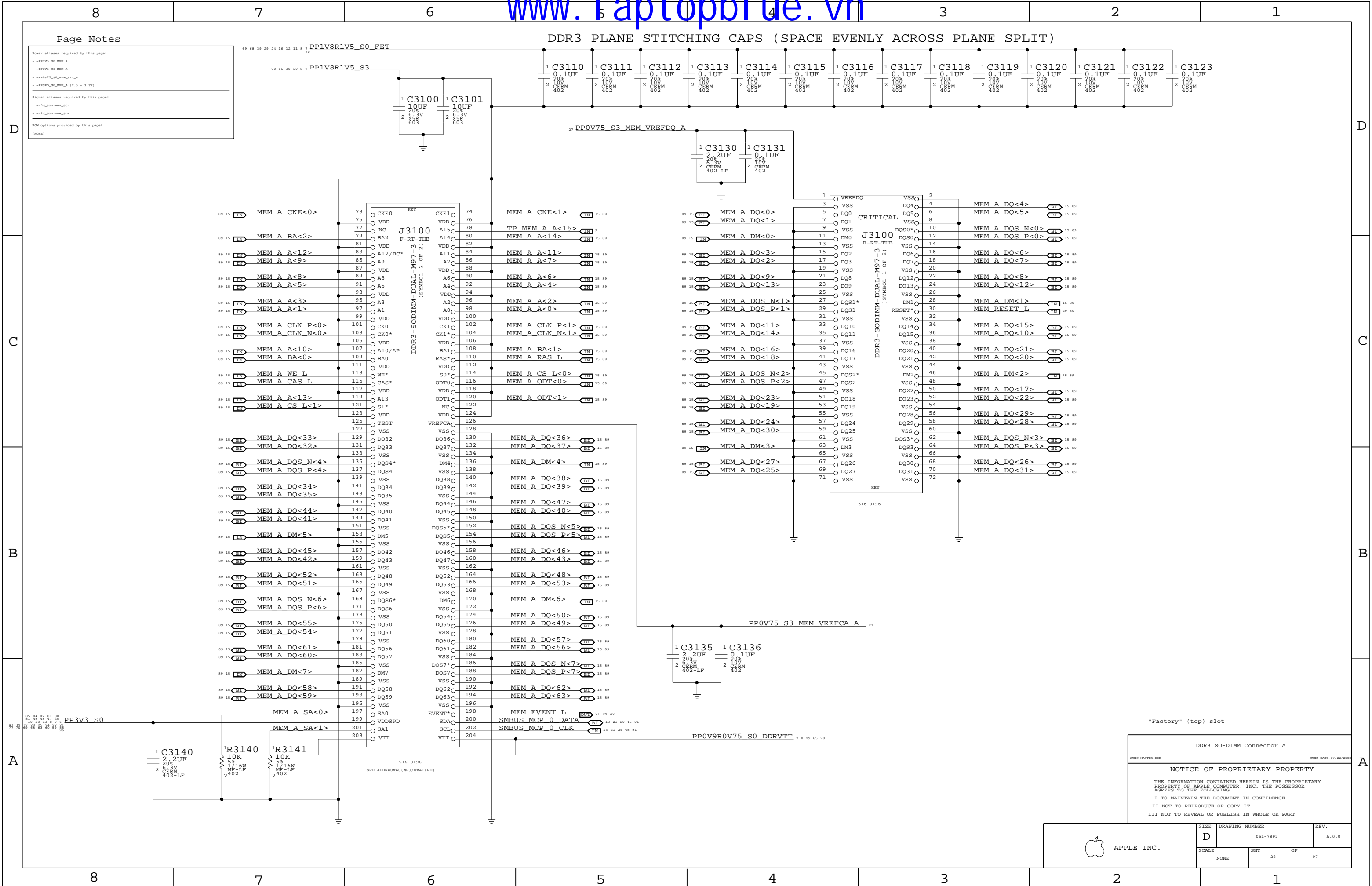
VREFMRGN
NO_VREFMRGN

C

A

FSB/DDR3/FRAMEBUF Vref Margining	
SYNC_MASTER=DDR	SYNC_DATE=12/05/2008
NOTICE OF PROPRIETARY PROPERTY	
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8	7	6	5	4	3	2	1
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Page Notes

Power aliases required by this page:

- PP1V5_S0_MEM_A
- PP1V5_S3_MEM_A
- PP0V75_S0_MEM_VTT_A
- PP0V75_S0_MEM_VTT_A
- PP0V75_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:

- I2C_S0DIMA_SCL
- I2C_S0DIMA_SDA

ROM options provided by this page:

(NONE)

"Factory" (top) slot

DDR3 SO-DIMM Connector A		
SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
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D

C

B

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D

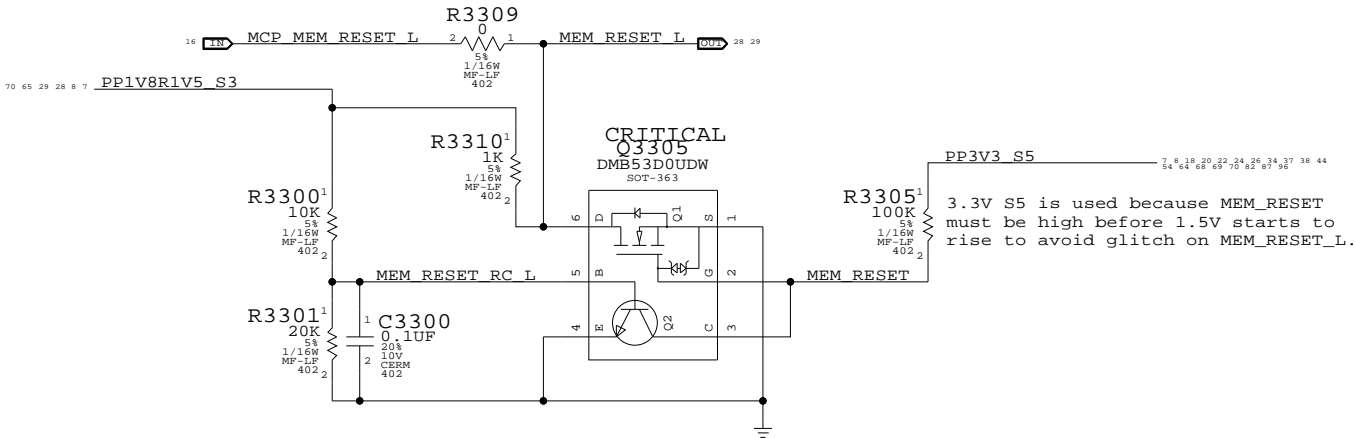
C

B

A

DDR3 RESET Support

Required becaues MCP79 does not meet DDR3 spec power-up reset timing requirement.



DDR3 Support

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2008

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APPLE INC.

SIZE

D

DRAWING NUMBER

051-7892

REV.

A.0.0

SCALE

NONE

SHT

30

OF

97

D

D

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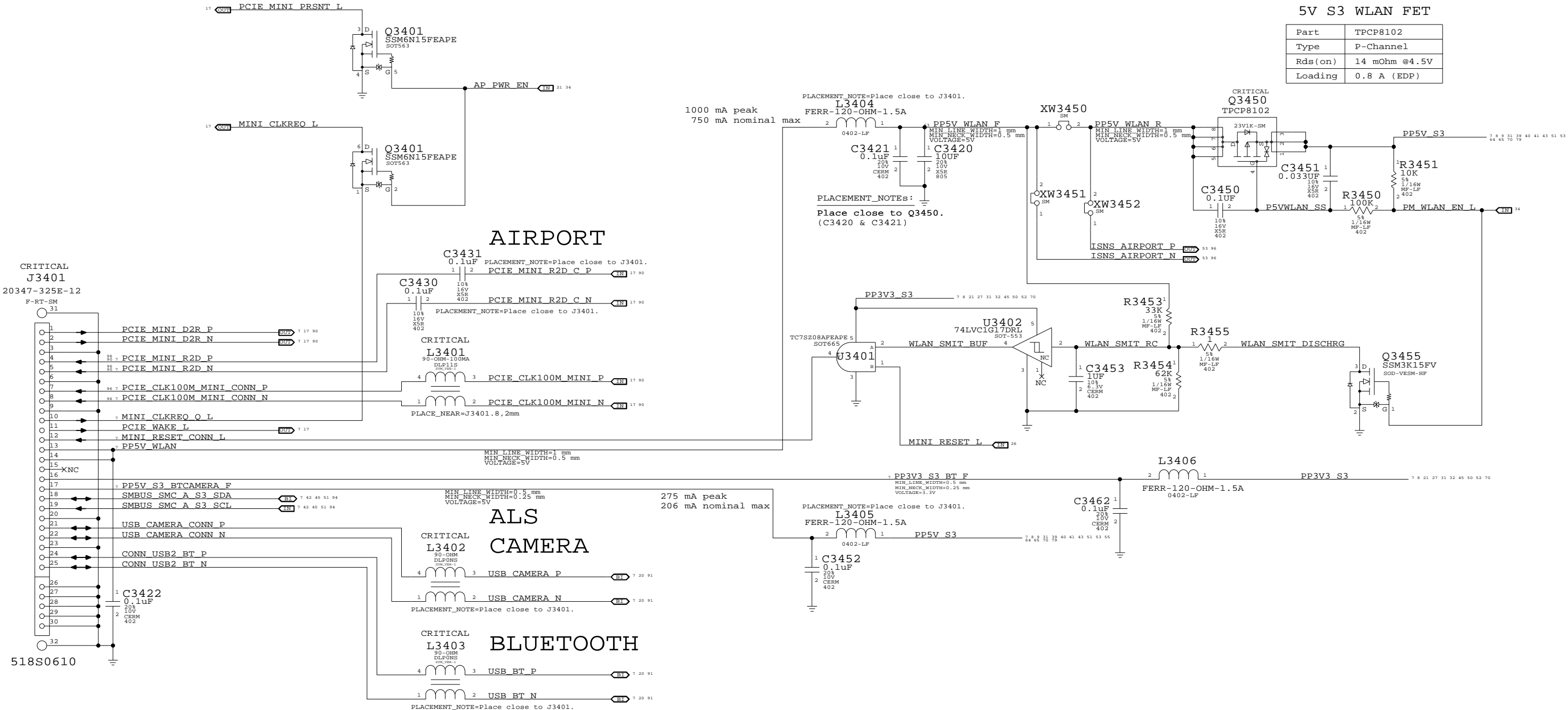
C

B

B

A

A



Right Clutch Connector

SYNC_MASTER=MUXGFX SYNC_DATE=12/08/2008

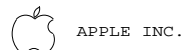
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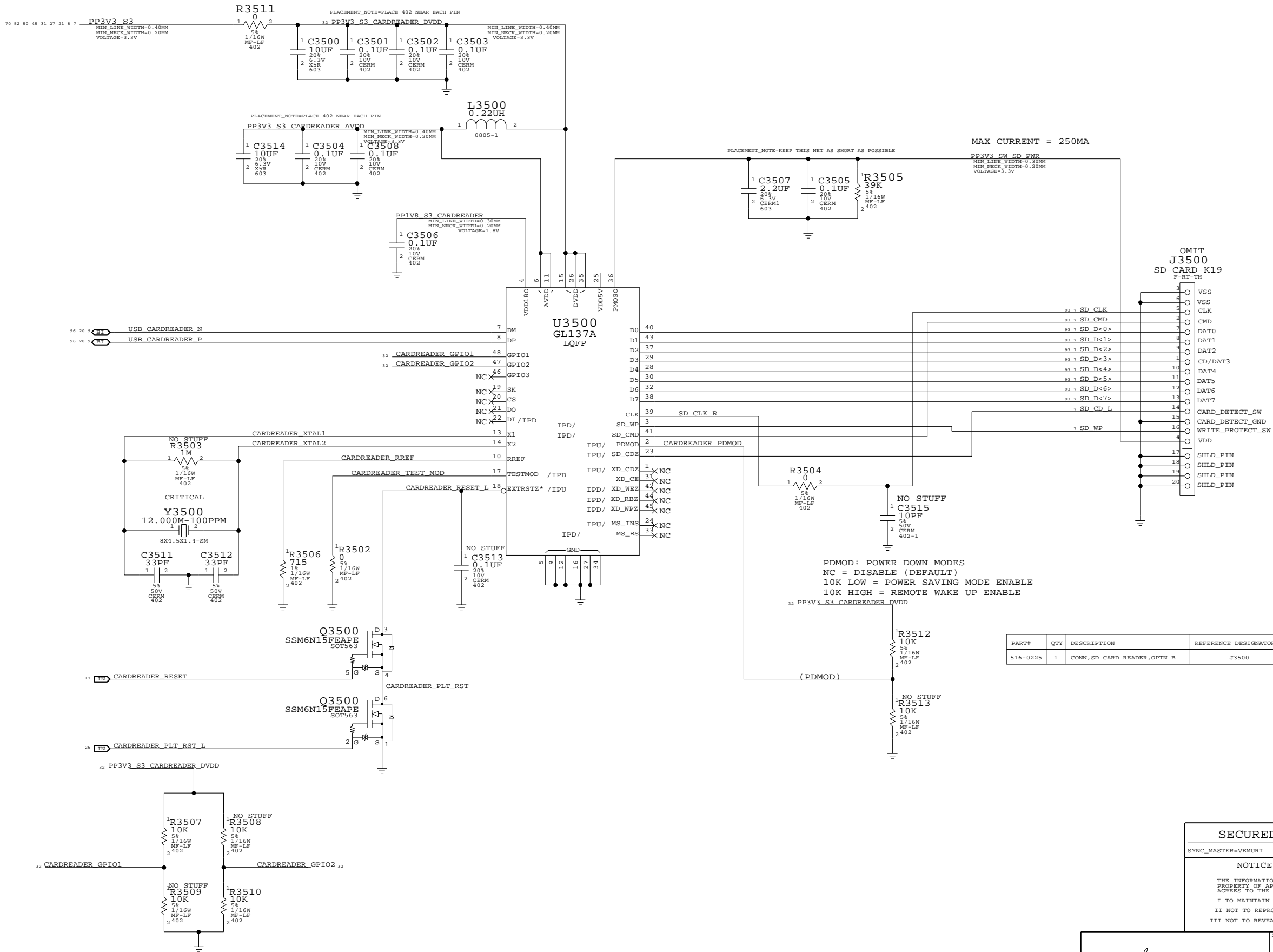
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE INC.

SIZE D DRAWING NUMBER 051-7892 REV. A.0.0

SCALE NONE SHT 31 OF 97



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516-0225	1	CONN,SD CARD READER,OPTN B	J3500	CRITICAL	

SECUREDIGITAL CARD READER

SYNC_MASTER=VEMURI SYNC_DATE=01/30/2009

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7892	A.0.0
SCALE		SHT	OF
NONE		32	97

D

C

B

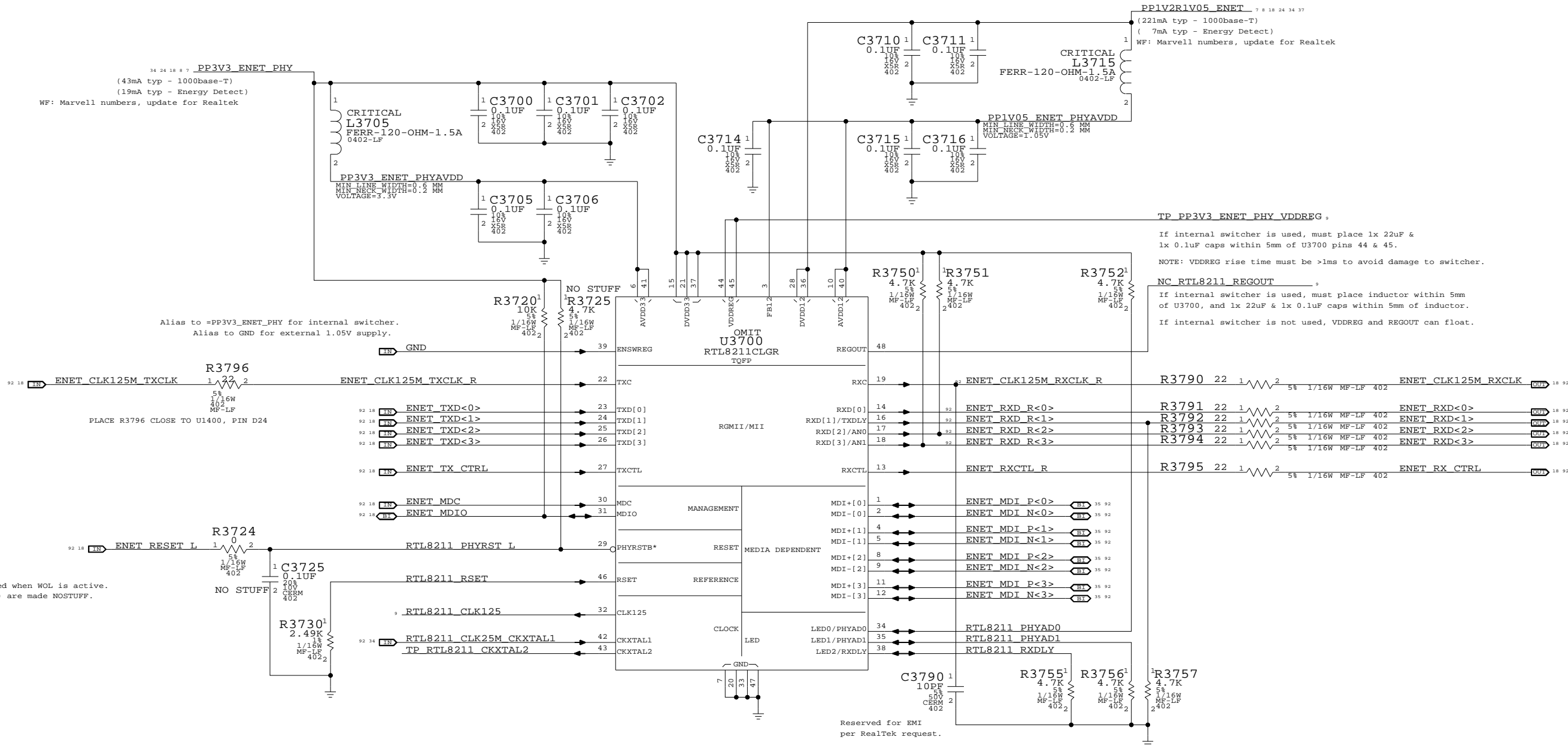
A

D

C

B


A



Configuration Settings:

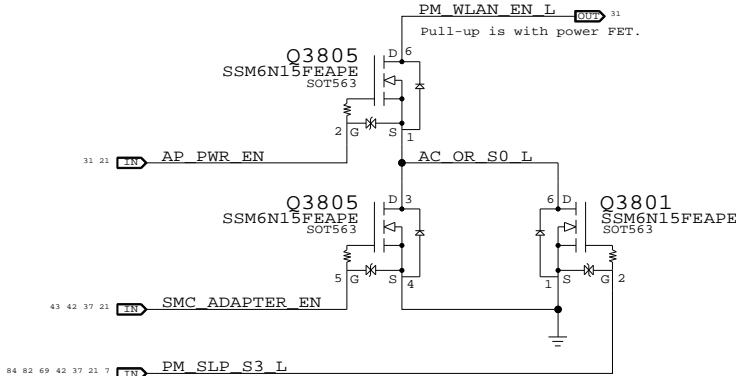
PHYAD = 01 (PHY Address 00001)
AN[1:0] = 11 (Full auto-negotiation)
RXDLY = 0 (RXCLK transitions with data)
TXDLY = 0 (No TXCLK Delay)

Ethernet PHY (RTL8211CL)		
SYNC_MASTER=SUMA_M98_MLB		SYNC_DATE=07/01/2008
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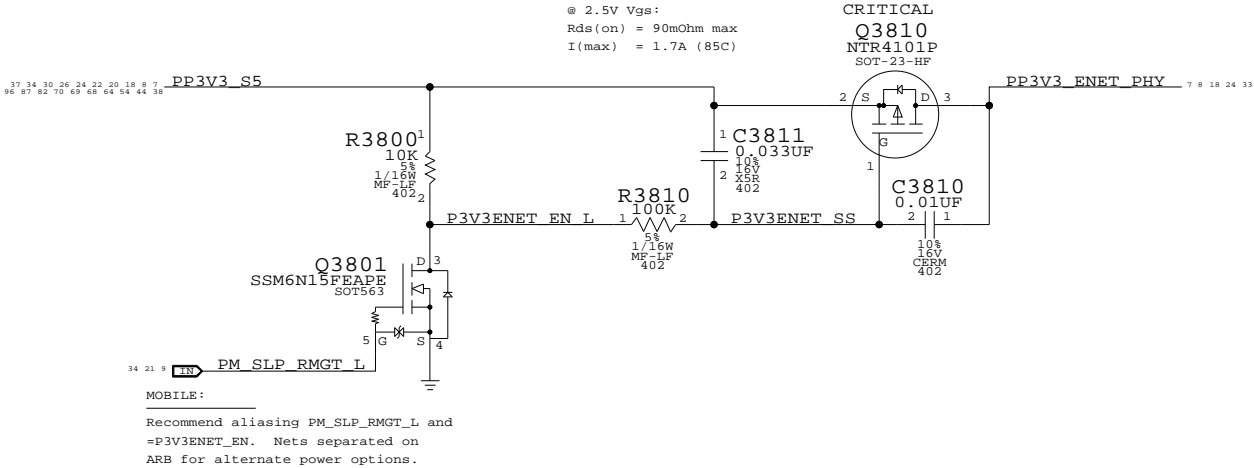
 APPLE INC.	SIZE D	DRAWING NUMBER 051-7892	REV. A.0.0
	SCALE NONE	SHT 33	OF 97

WLAN Enable Generation

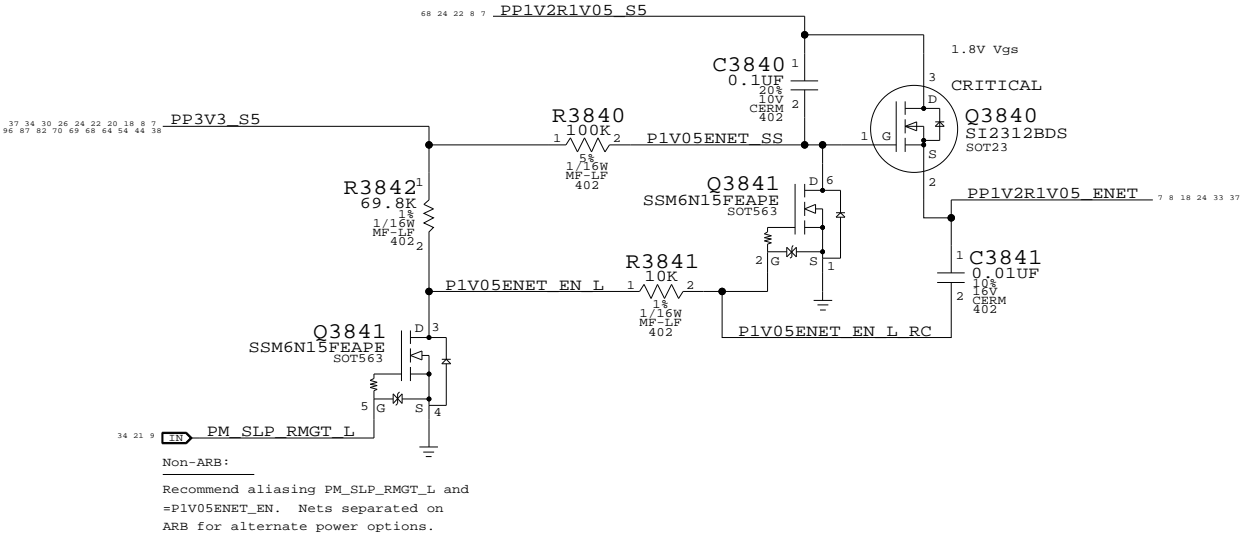
"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))
NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.



3.3V ENET FET

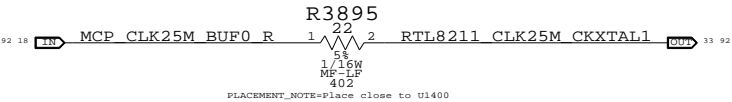


1.05V ENET FET



RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.
Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.



Ethernet & AirPort Support

SYNC_MASTER=SUMA_M98_MLB SYNC_DATE=07/01/2008

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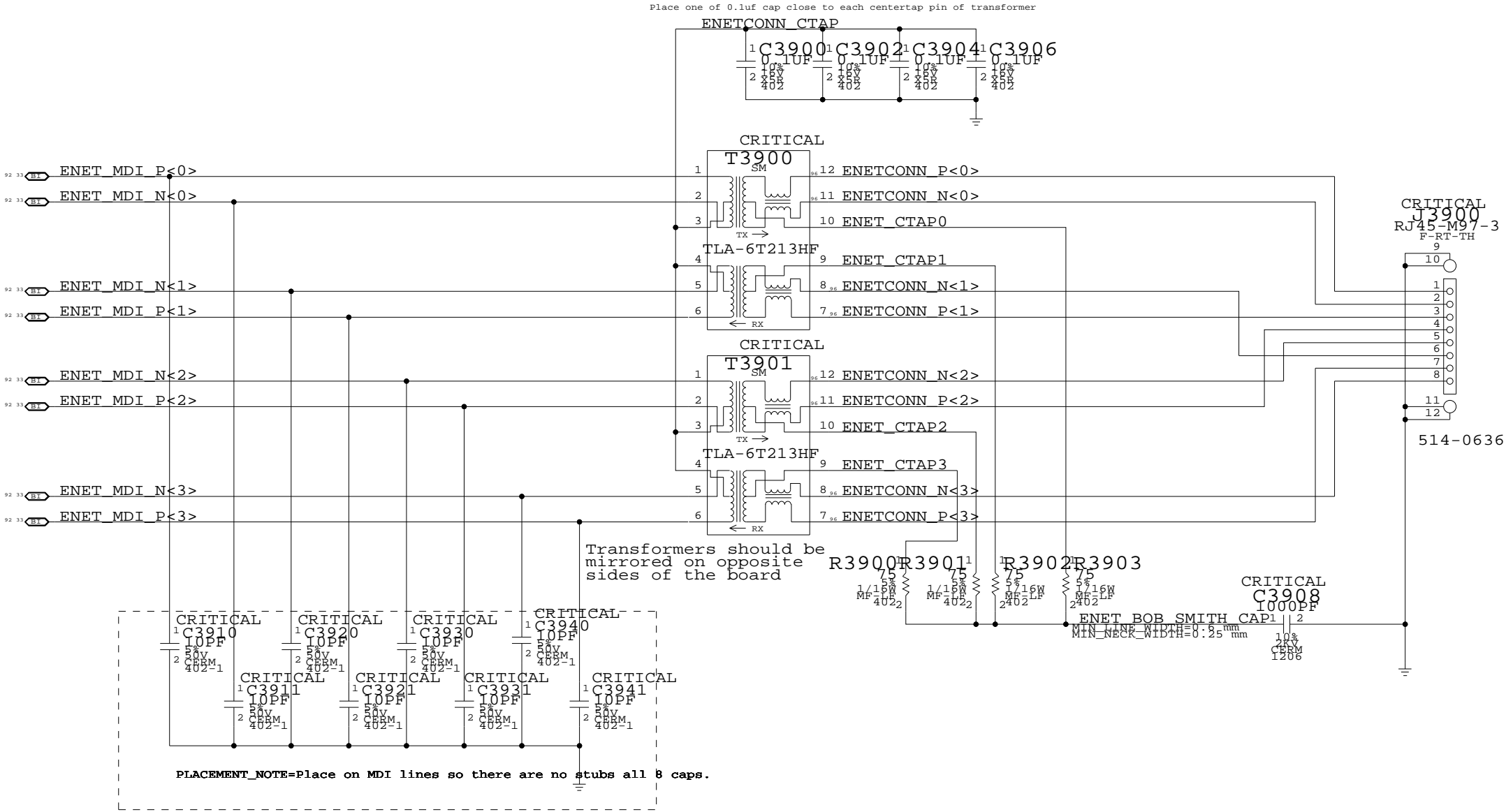


APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE	SHT	OF
NONE	34	97

Page Notes

Power aliases required by this page:
(NONE)
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)



Ethernet Connector

SYNC_MASTER=AMASON_M98_MLB SYNC_DATE=12/16/2008

NOTICE OF PROPRIETARY PROPERTY

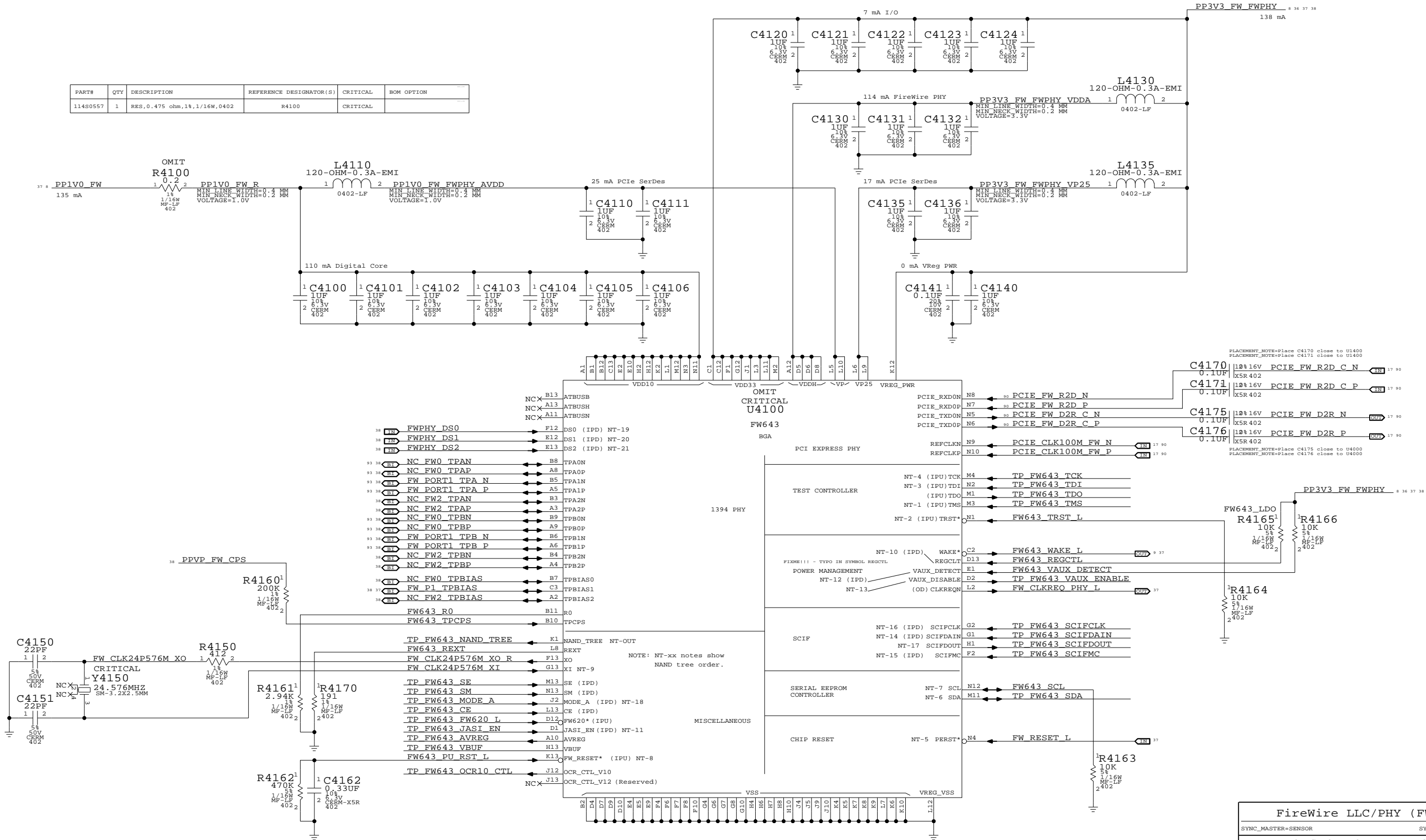
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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE	SHT	OF
NONE	35	97

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
11480557	1	RES,0.475 ohm,1%,1/16W,0402	R4100	CRITICAL	



FireWire LLC/PHY (FW643)

SYNC_MASTER=SENSOR SYNC_DATE=08/14/2008

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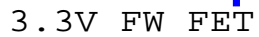
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	4.12.0
SCALE	SHT	OF
NONE	36	97


```
Power aliases required by this page:
- =PPRUS_RS_FW_FWRSEN (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)

Signal aliases required by this page:
(NONE)

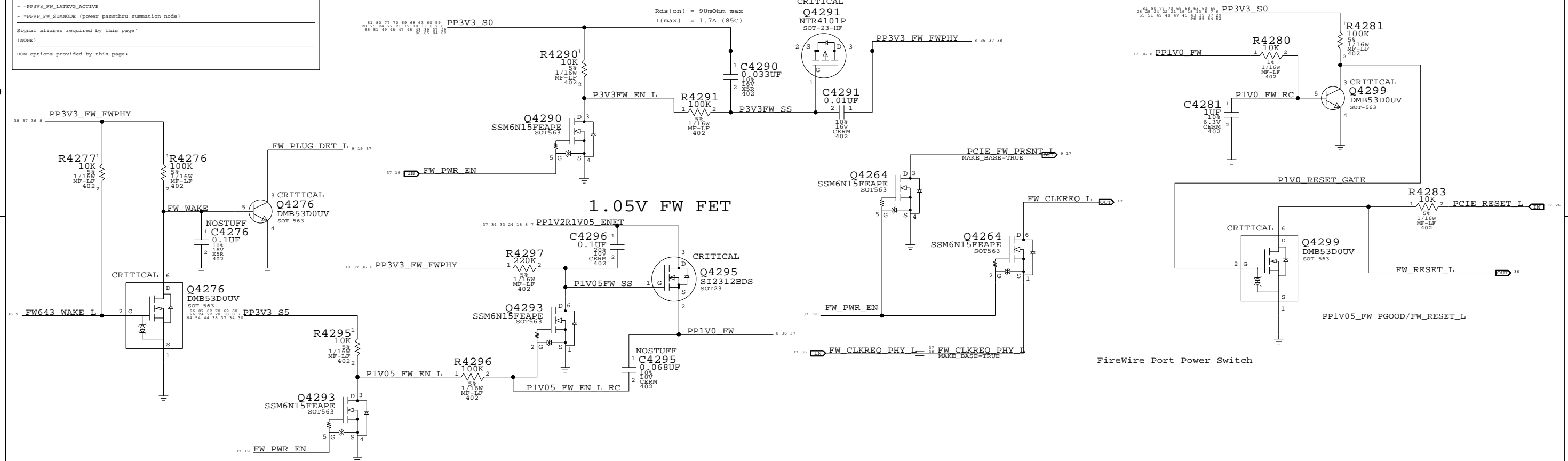
BCM options provided by this page:
```



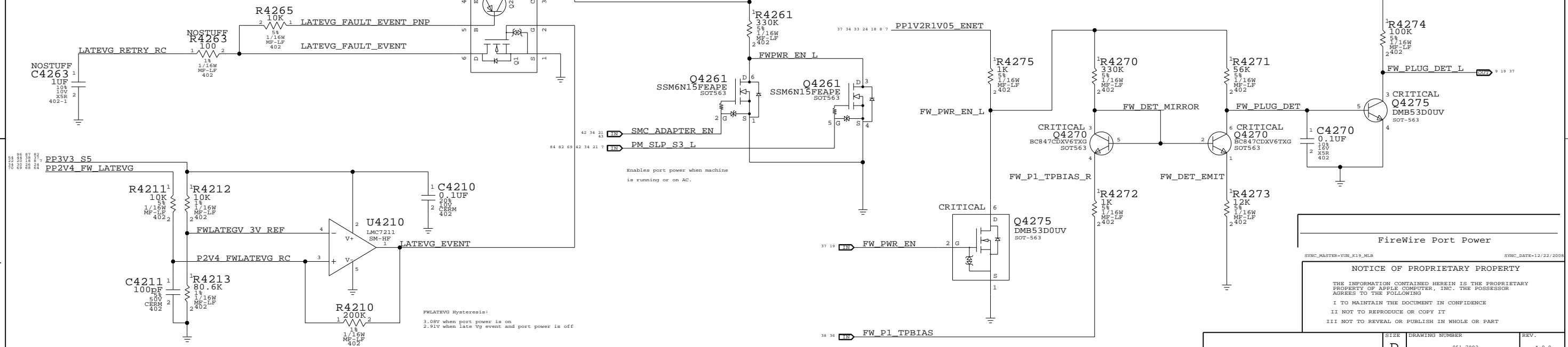
@ 2.5V V_{gs} :

R_{ds(on)} = 90mOhm max
I(max) = 1.7A (85C)

CRITICAL
Q4291
NTR4101P
SOT-23-HF



Late-VG Event Detection



FireWire Port Power

SYNC_MASTER=YUN_K19_MLB SYNC_DATE=12/22/2008

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SIZE D	DRAWING NUMBER 051-7892	REV. A.0.0
SCALE NONE	SHT 37	OF 97

 APPLE INC.

D

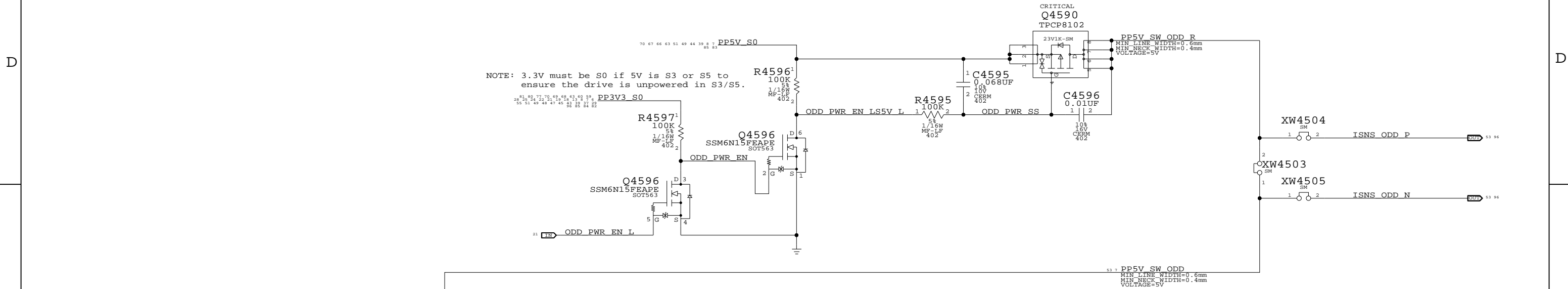
B

A

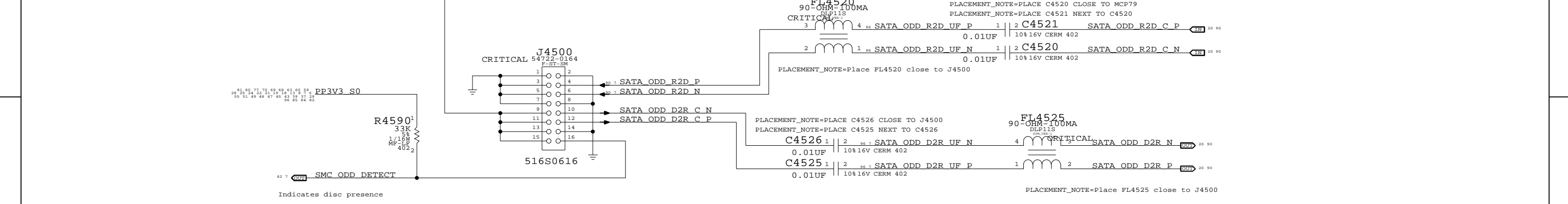
8	7	6	5	4	3	2	1
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FireWire Ports	
SYNC_MASTER=SENSOR	SYNC_DATE=08/14/2008
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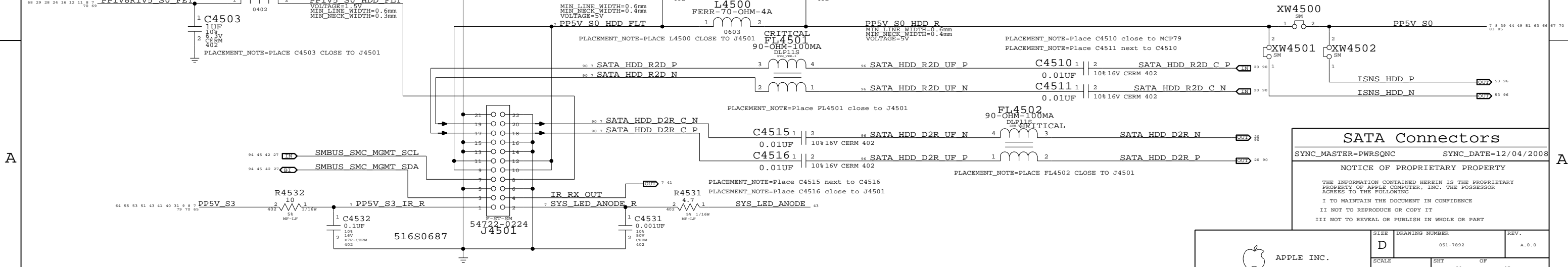
ODD Power Control



SATA ODD Port



SATA HDD Port



SATA Connectors

SYNC_MASTER=PWRSQNC SYNC_DATE=12/04/2008

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7892	A.0.0
SCALE	NONE	SHT	39 OF 97

D

D

C

C

B

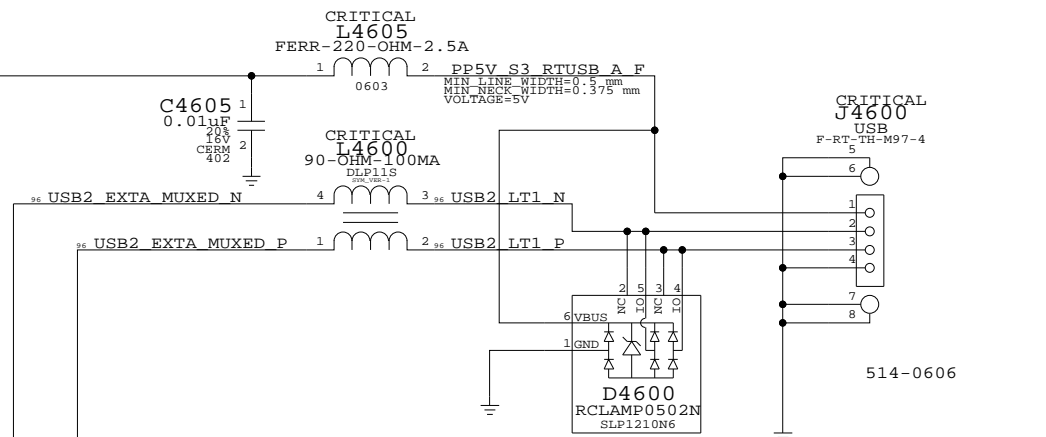
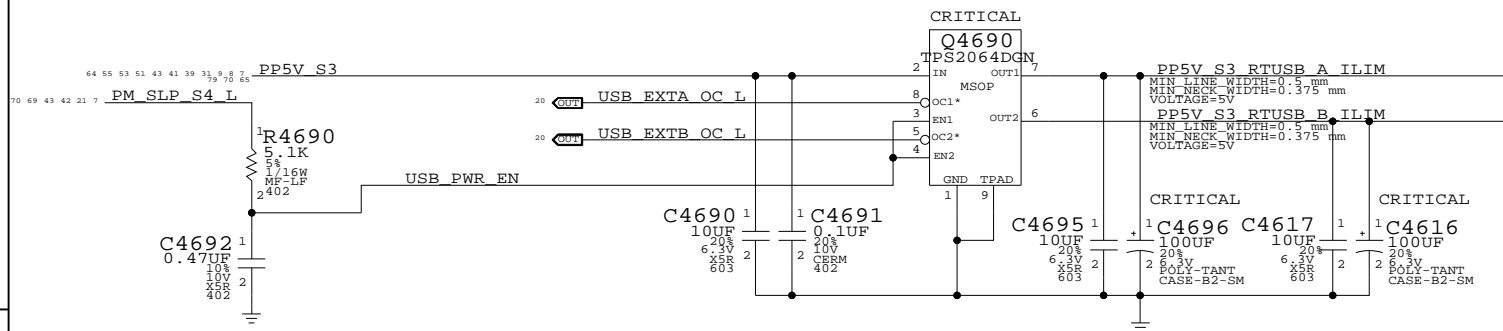
B

A

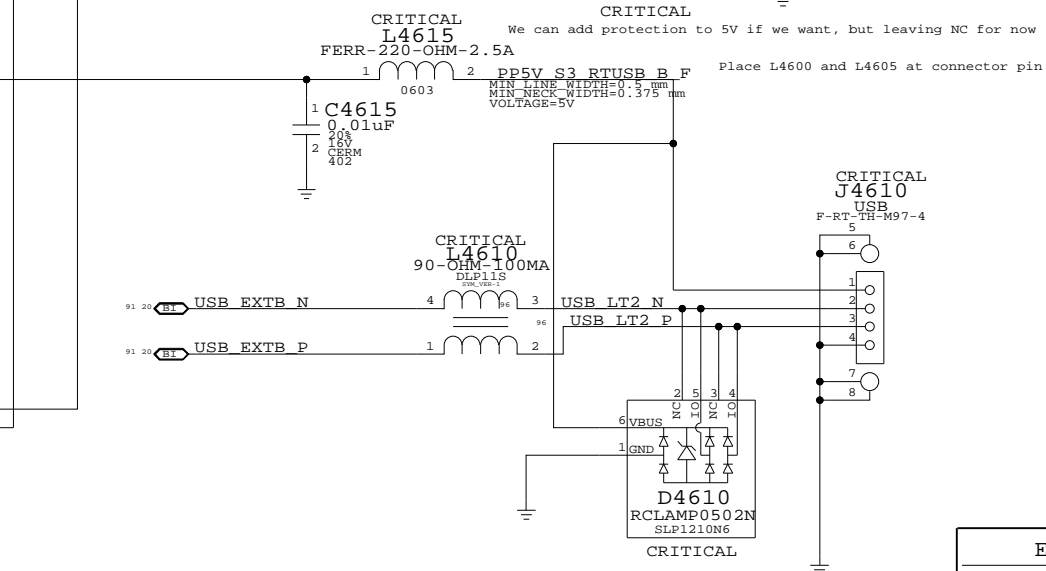
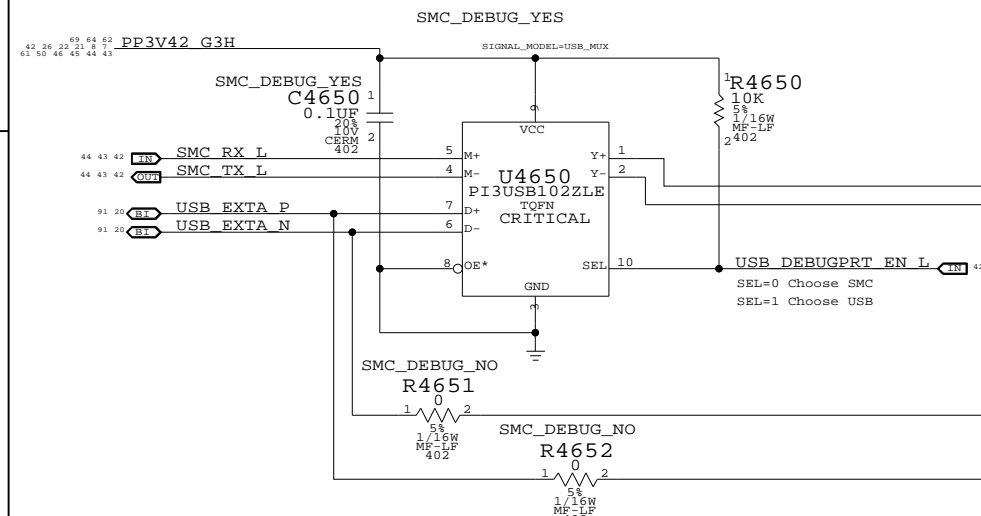
A

Port Power Switch

Left USB Port A



USB/SMC Debug Mux

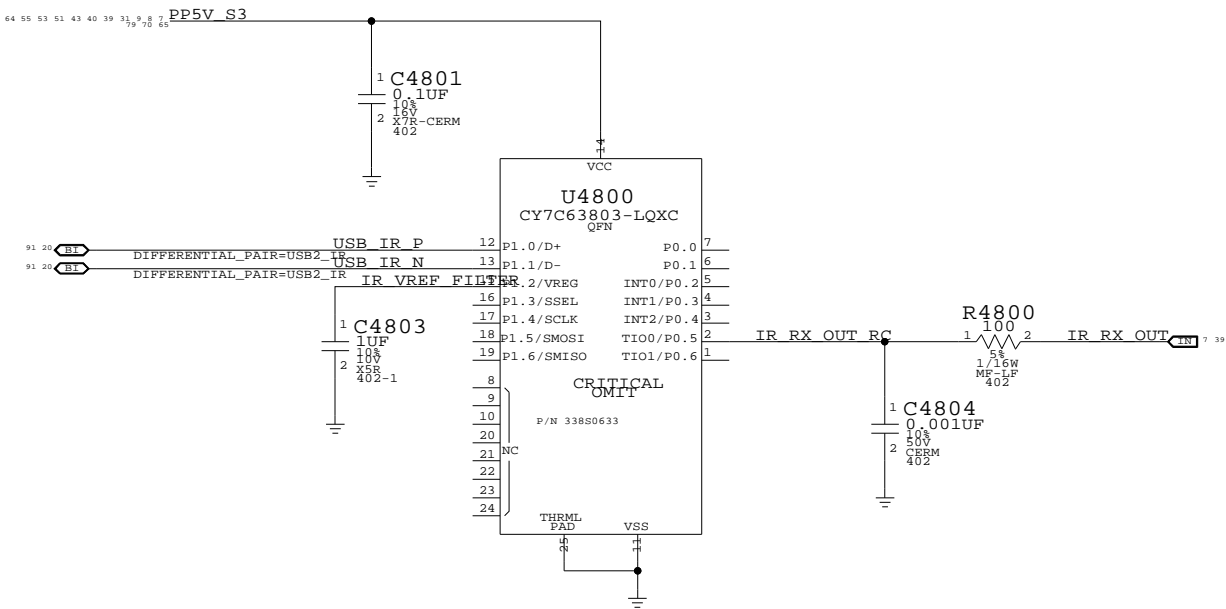


Left USB Port B

External USB Connectors		
SYNC_MASTER=M98_MLB		SYNC_DATE=11/14/2008
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7892	A.0.0
SCALE		SHT	OF
NONE		40	97

IR SUPPORT



Front Flex Support

SYNC_MASTER=PWRSONC SYNC_DATE=12/04/2008

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APPLE INC.

SIZE
D

DRAWING NUMBER

051-7892

REV.

A.0.0

SCALE

NONE

SHT

41

OF

97

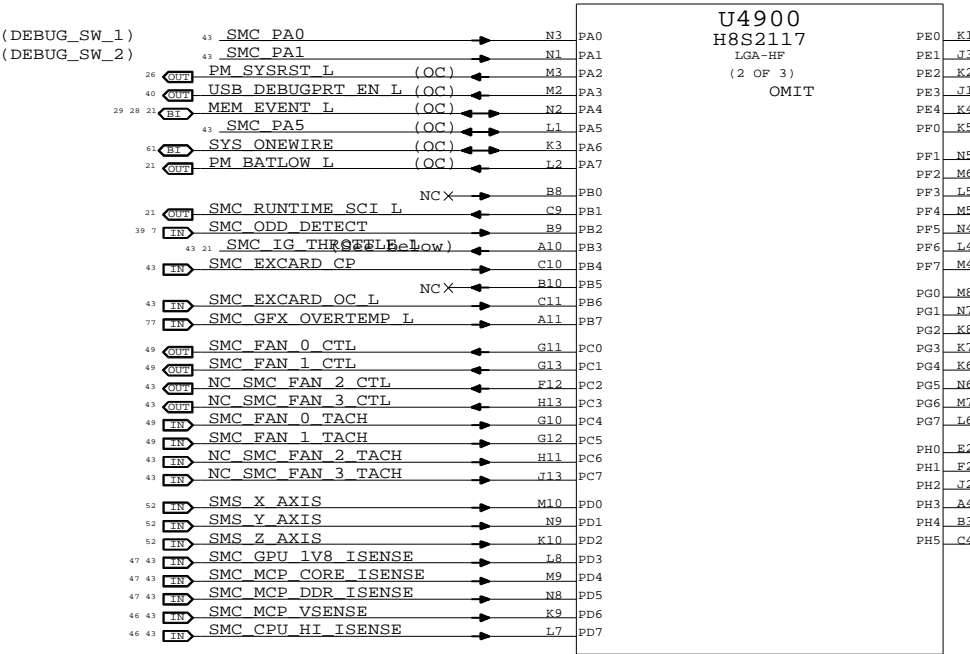
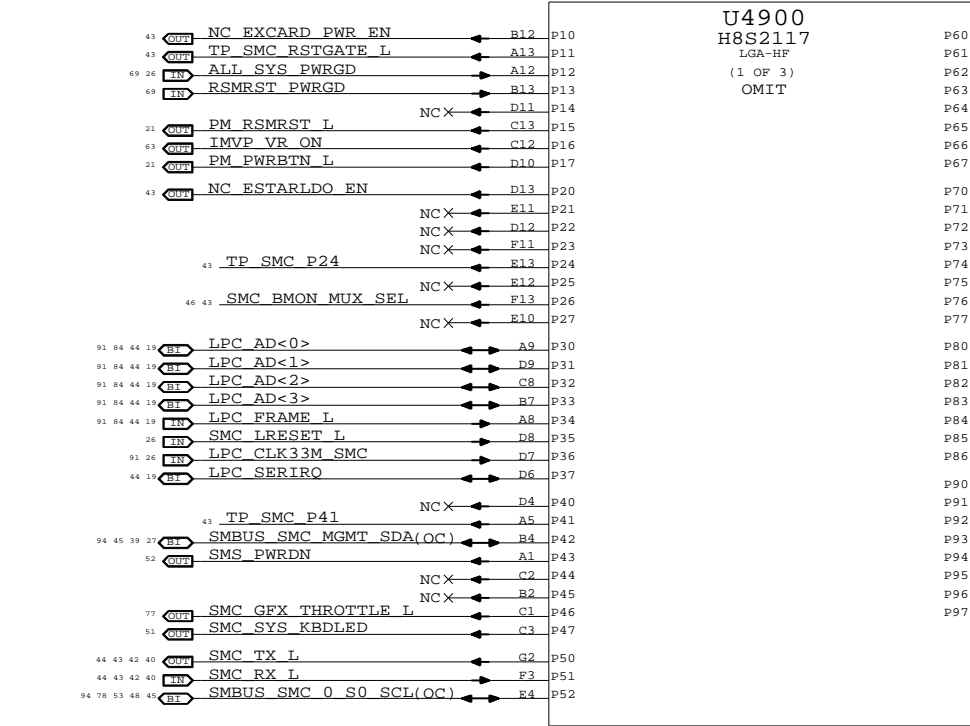
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

D

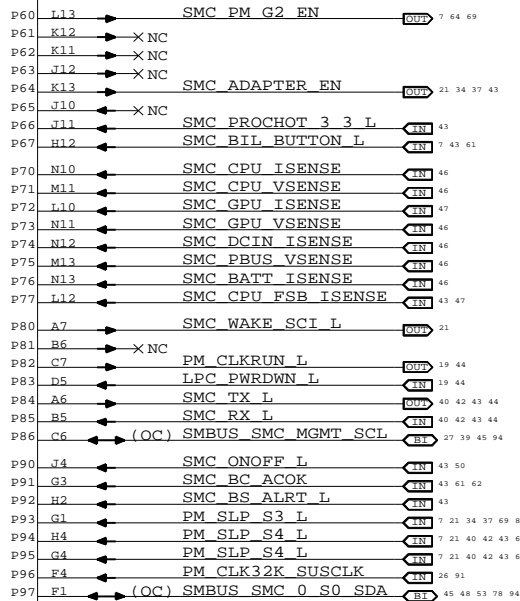
C

B

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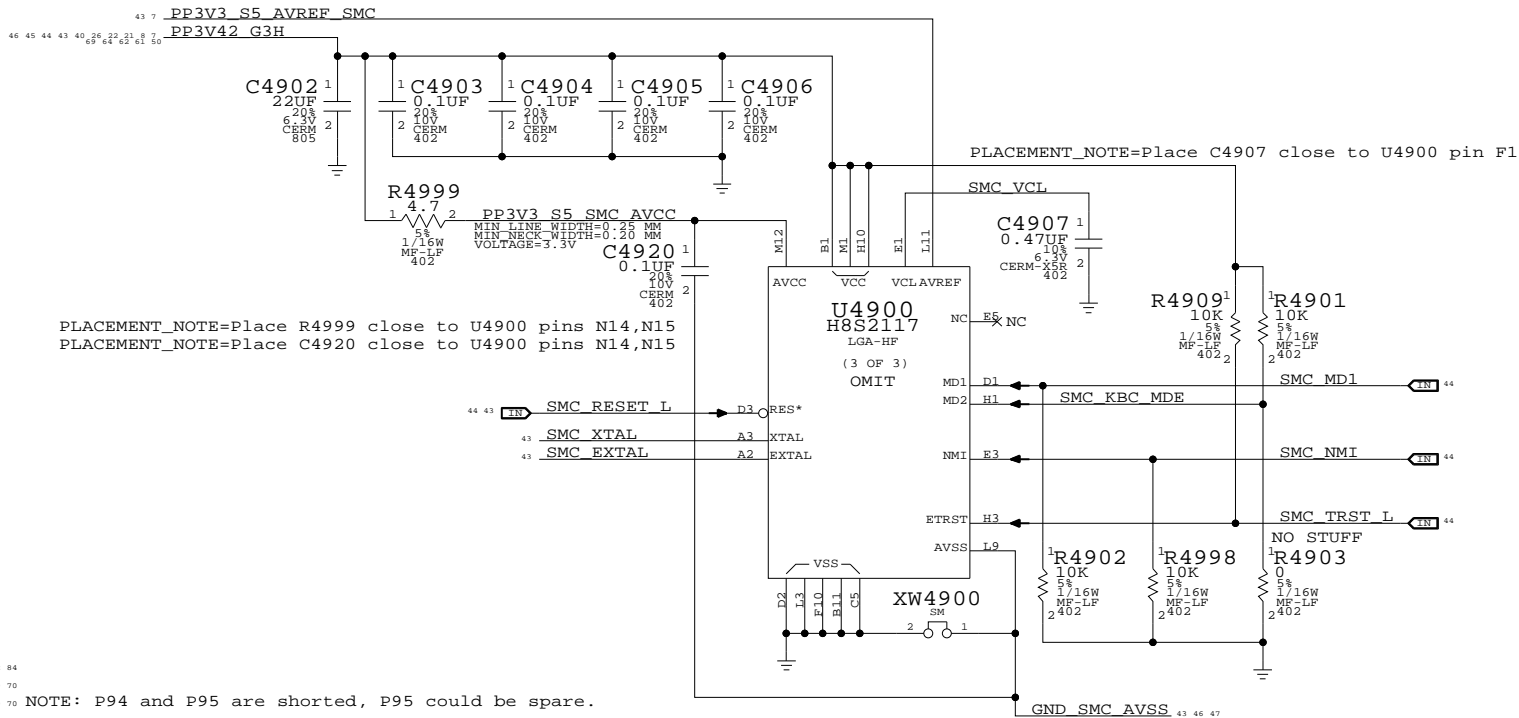


SMC_PB3:
SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)



PLACEMENT_NOTE=Place R4999 close to U4900 pins N14,N15
PLACEMENT_NOTE=Place C4920 close to U4900 pins N14,N15

NOTE: P94 and P95 are shorted, P95 could be spare.



NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SMC

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2008

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APPLE INC.

SIZE D

DRAWING NUMBER 051-7892

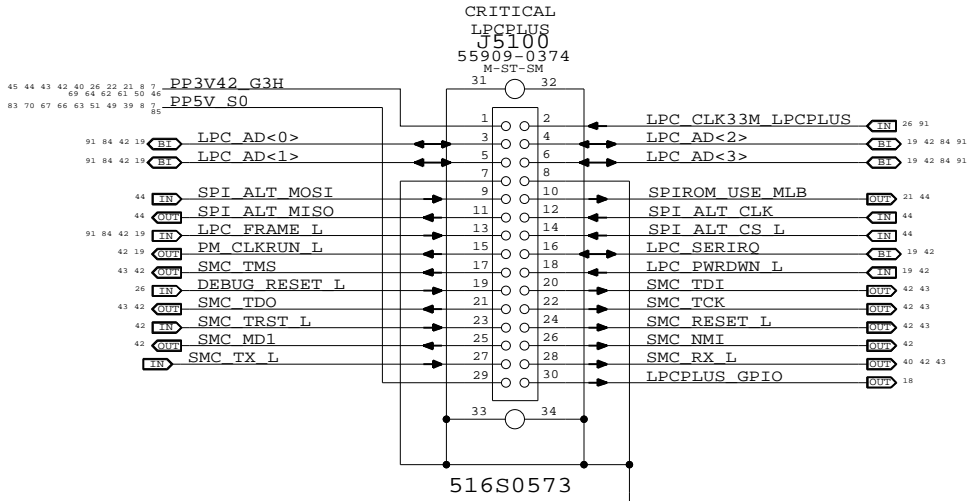
REV. A.0.0

SCALE NONE

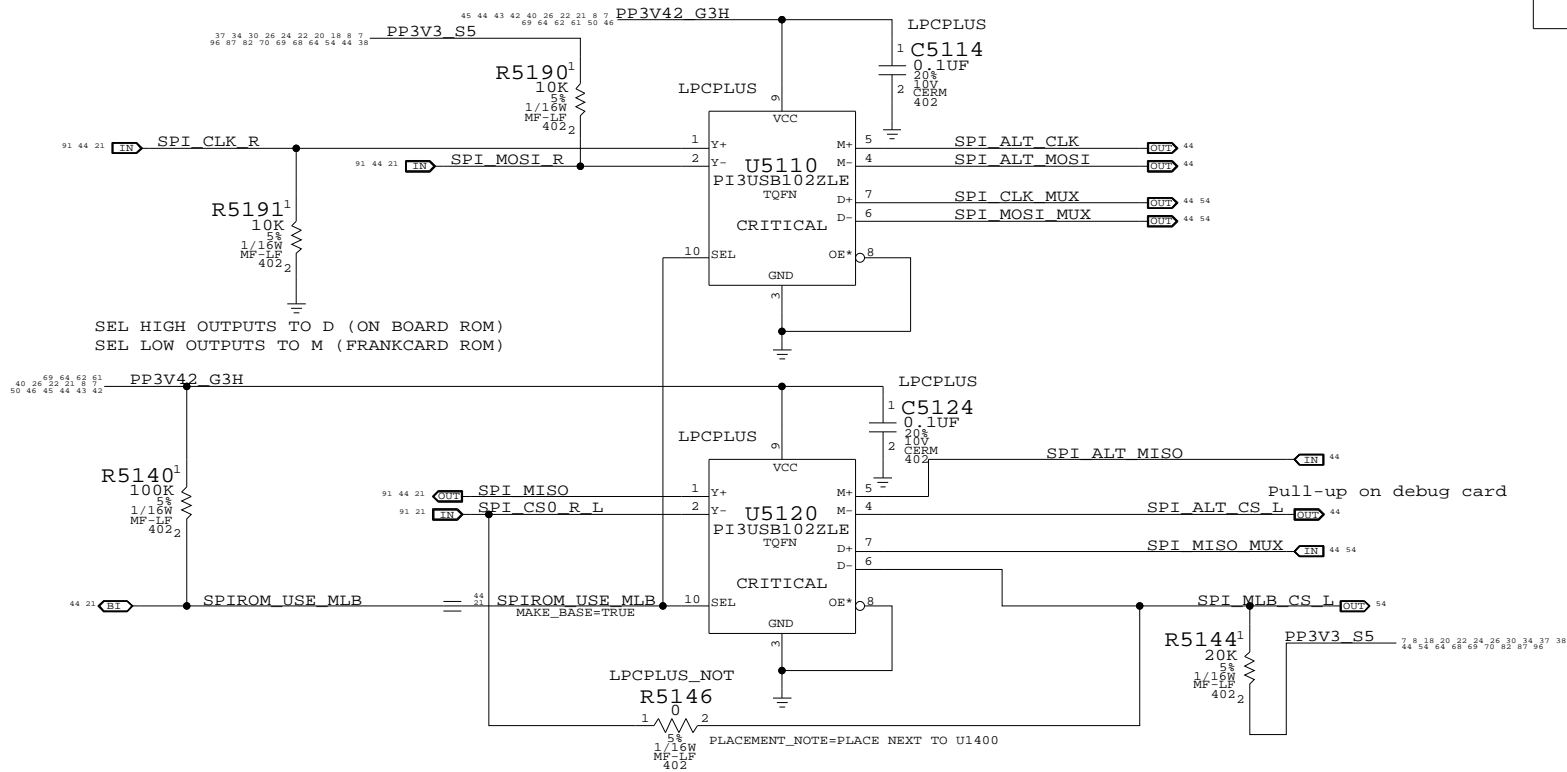
SHT 42

OF 97

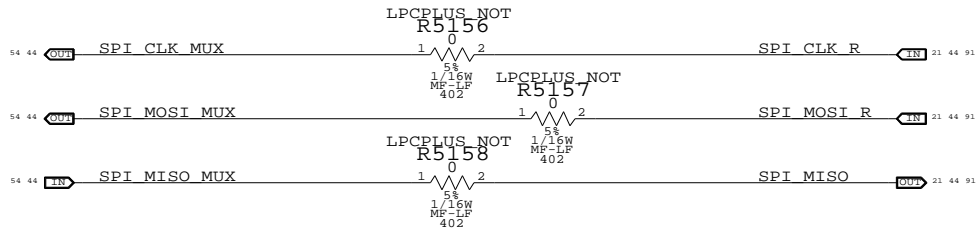
LPC+SPI Connector



Alternate SPI ROM Support



SPI MUX BYPASS



LPC+SPI Debug Connector

SYNC_MASTER=CHANGZHANG SYNC_DATE=05/09/2008

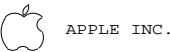
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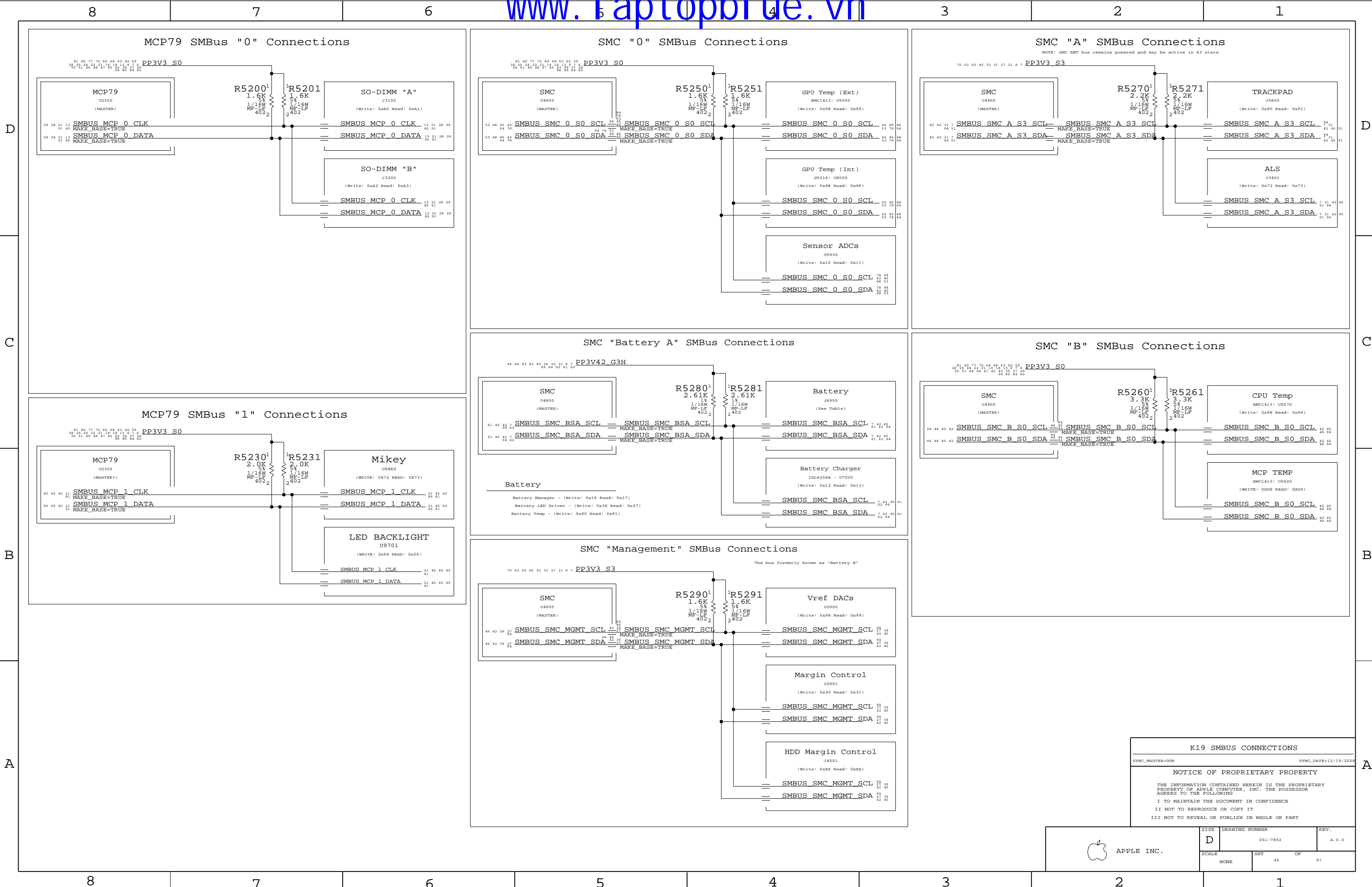
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART




APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE	SHT	OF
NONE	44	97



K19 SMBUS CONNECTIONS		
SYNC_MASTER=DOR		SYNC_DATE=12/19/2008
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 APPLE INC.	SIZE D	DRAWING NUMBER 051-7892	REV. A.0.0
	SCALE NONE	SHT 45	OF 97

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C

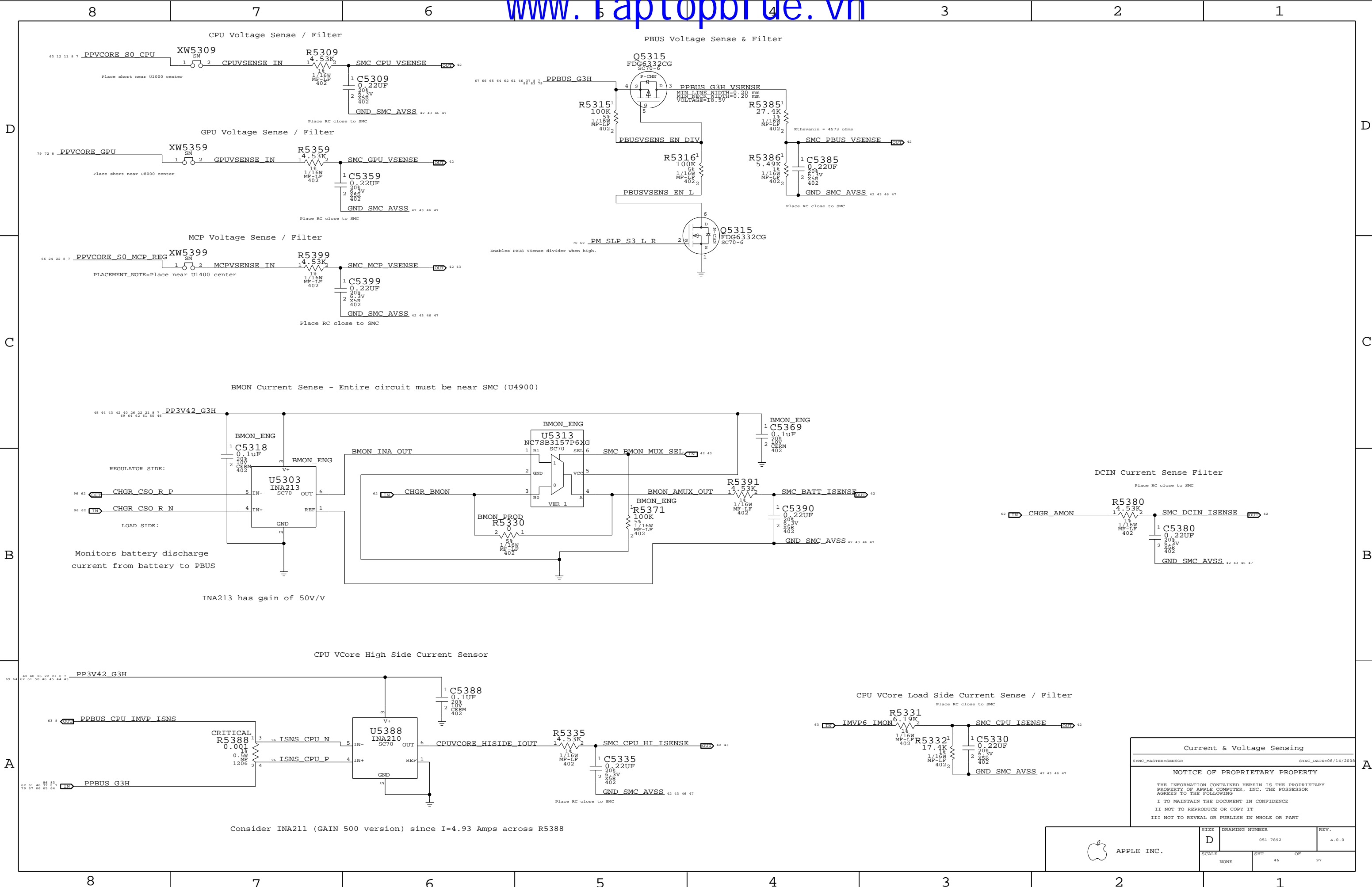
C

B

B

A

A



Current & Voltage Sensing

SYNC_MASTER=SENSOR SYNC_DATE=08/14/2008

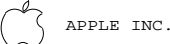
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SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE	SHT	OF
NONE	46	97

D

D

C

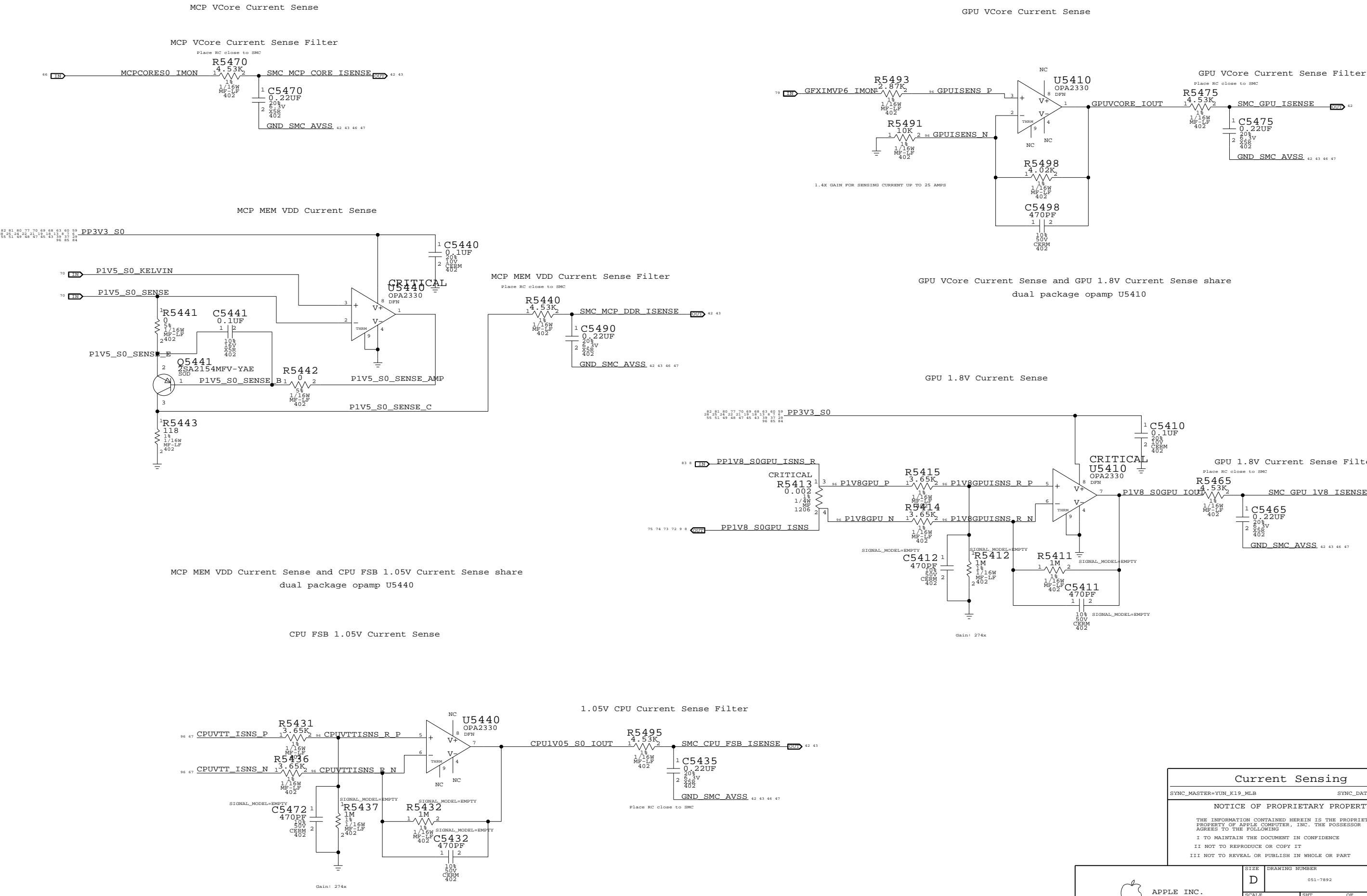
C

B

B

A

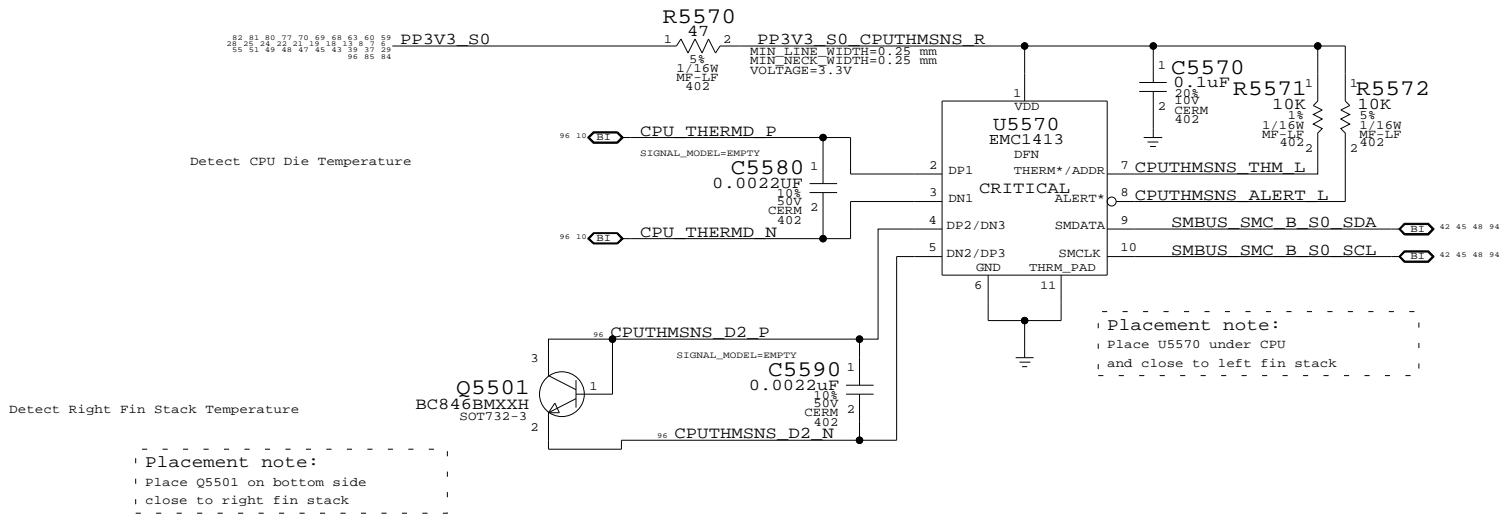
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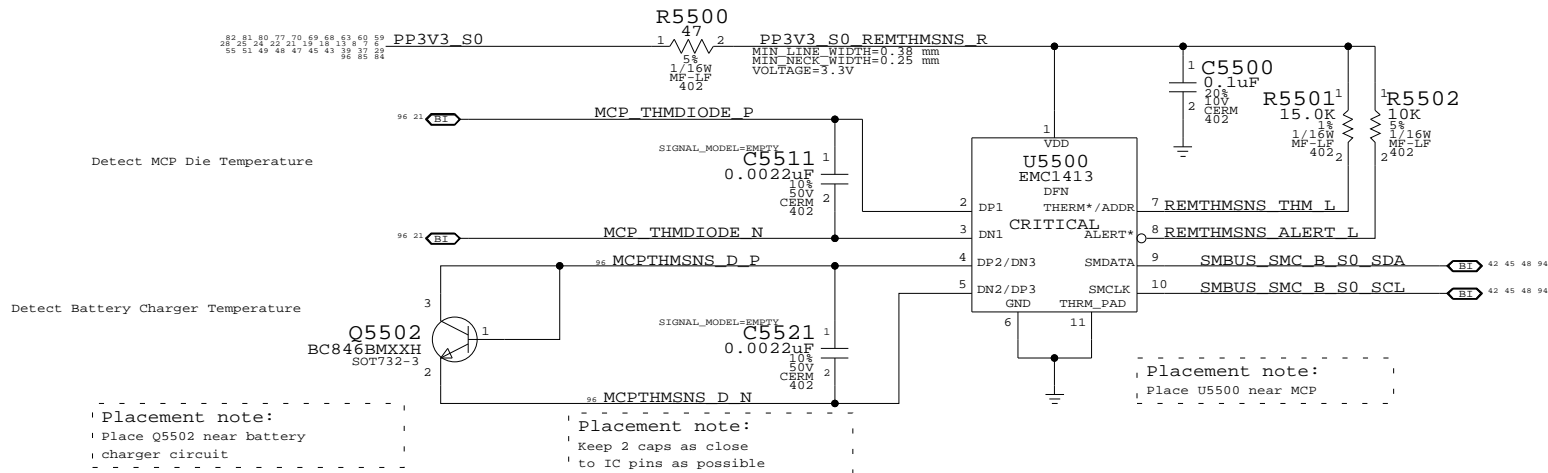
Current Sensing		
SYNC_MASTER=YUN_K19_MLB		SYNC_DATE=12/10/2008
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	D	051-7892	A.0.0
SCALE	NONE	SHT	OF
		47	97

CPU Proximity/CPU Die/Right Fin Stack

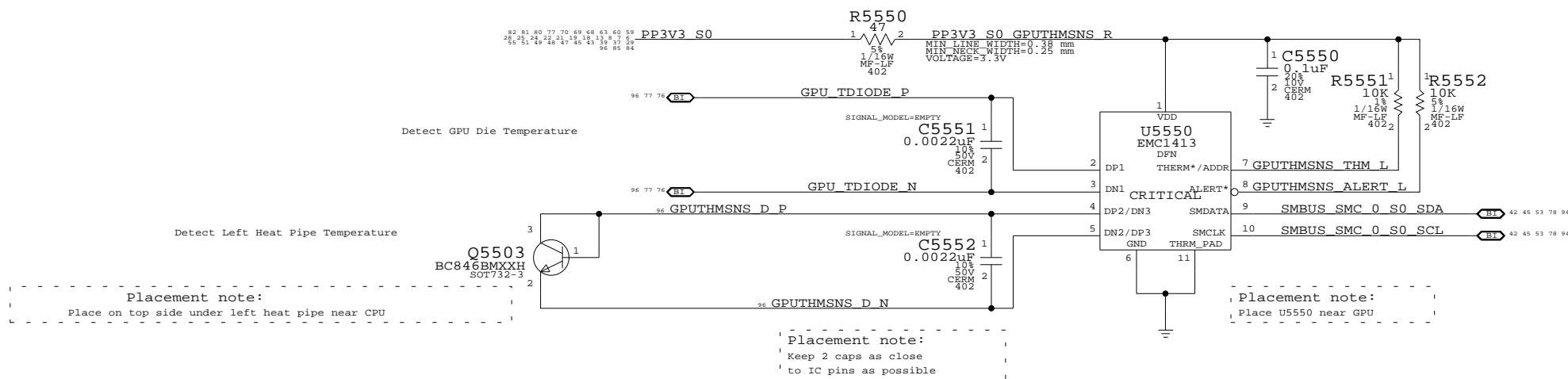


MCP Proximity/MCP Die/Battery Charger Proximity



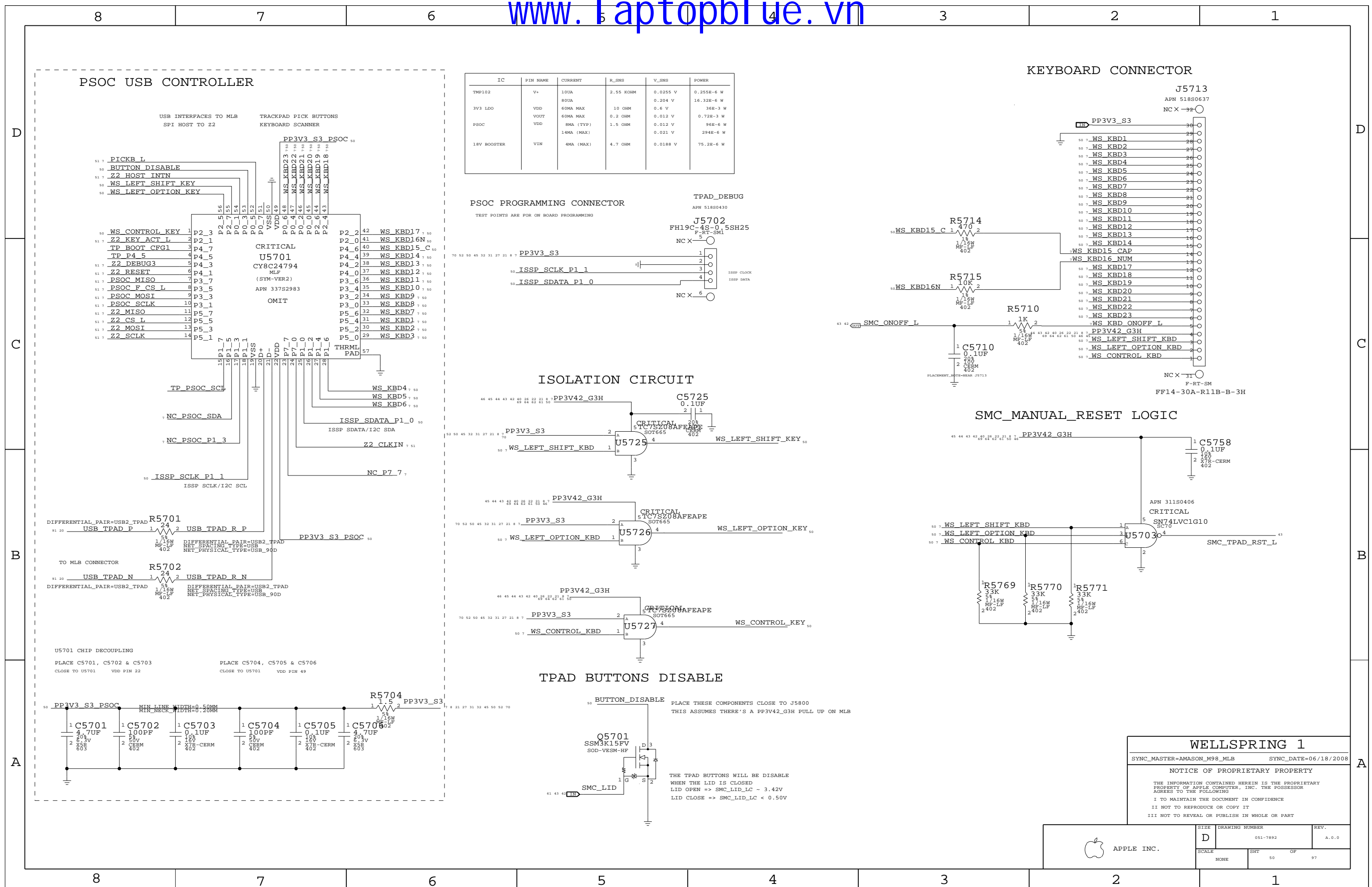
Note: EMC1413 can perform Beta Compensation for External Diode 1 only

GPU Proximity/GPU Die/Left Heat Pipe

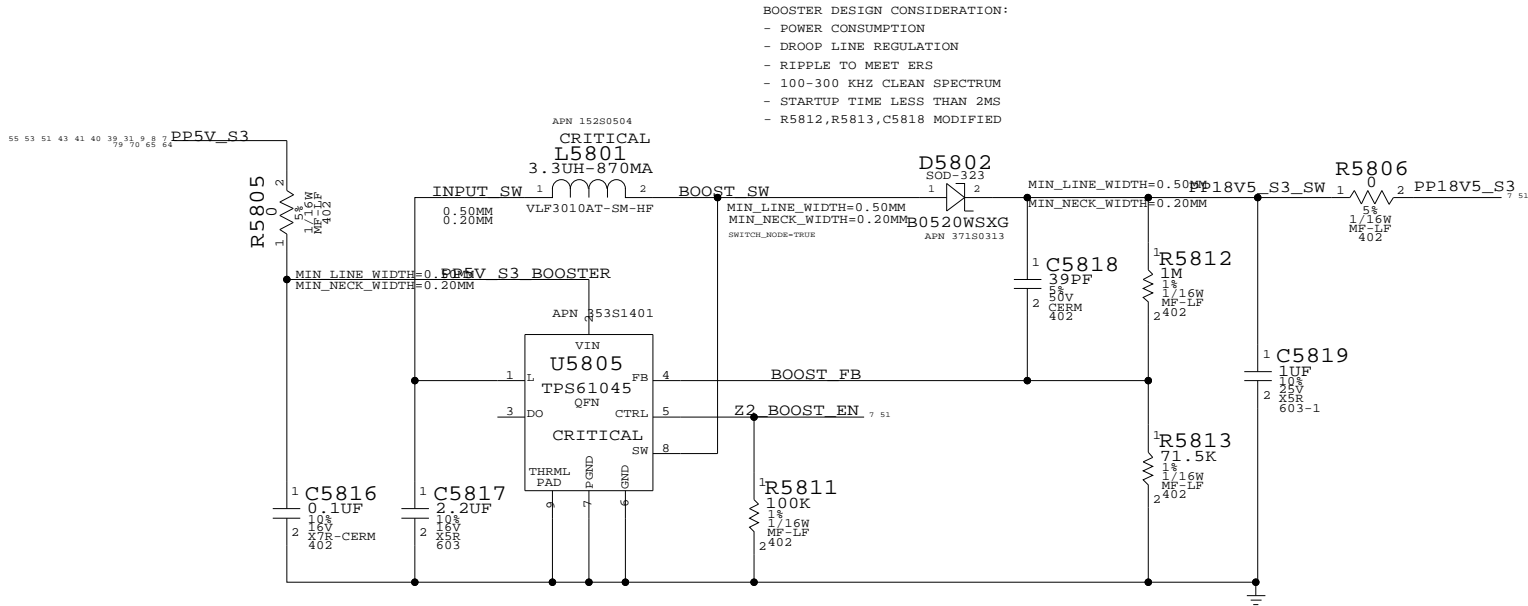


Thermal Sensors		
SYNC_MASTER=YUN_K19_MLB		SYNC_DATE=12/22/2008
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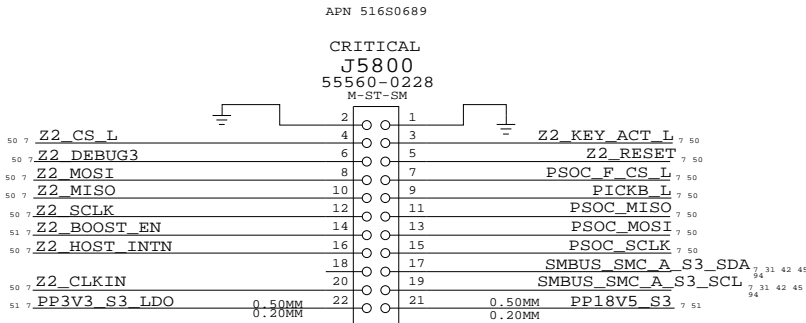
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7892	A.0.0
SCALE		SHT	OF
NONE		48	97



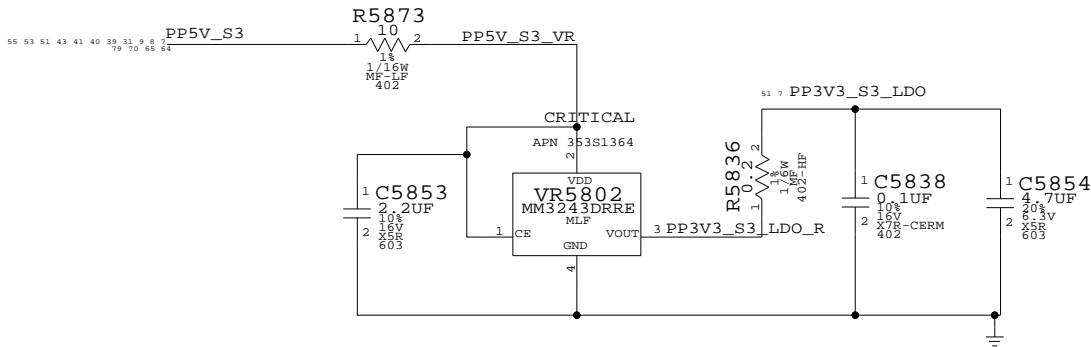
BOOSTER +18.5VDC FOR SENSORS



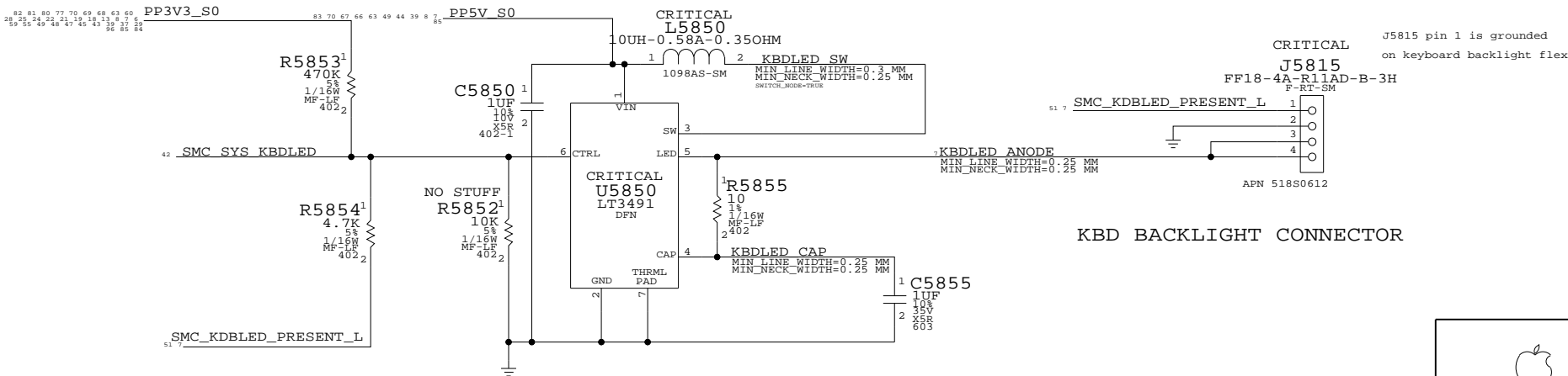
IPD FLEX CONNECTOR



3V3 LDO FOR IPD

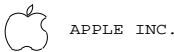


Keyboard LED Driver



KBD BACKLIGHT CONNECTOR

WELLSPRING 2	
SYNC_MASTER=PWRSONC	SYNC_DATE=01/05/2009
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SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE	SHT	OF
NONE	51	97

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D

C

B

A

Analog SMS

R5921 PULLS UP SMS_PWRDN TO TURN OFF SMS WHEN PIN IS NOT BEING DRIVEN BY SMC

The circuit diagram shows the following connections:

- VDD (pin 14) connected to PP3V3_S3.
- GND (pin 7) connected to ground.
- SMS_SELFTEST (pin 15) connected to GND through resistor R5922 (10K).
- SMS_PWRDN (pin 52) pulled up by resistor R5921 (10K) to PP3V3_S3.
- Output pins: VOUTX (pin 12), VOUTY (pin 10), and VOUTZ (pin 8) are connected to test points 402.
- Capacitors C5922, C5923, C5924, C5925, and C5926 provide decoupling at various nodes.

Desired orientation when placed on board top-side:

+Z (up)

Circle indicates pin 1 location when placed in correct orientation

Sudden Motion Sensor (SMS)		
SYNC_MASTER=SENSOR		SYNC_DATE=08/14/2008
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SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0

SCALE	SHT	OF
NONE	52	97

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A

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+Z (up)

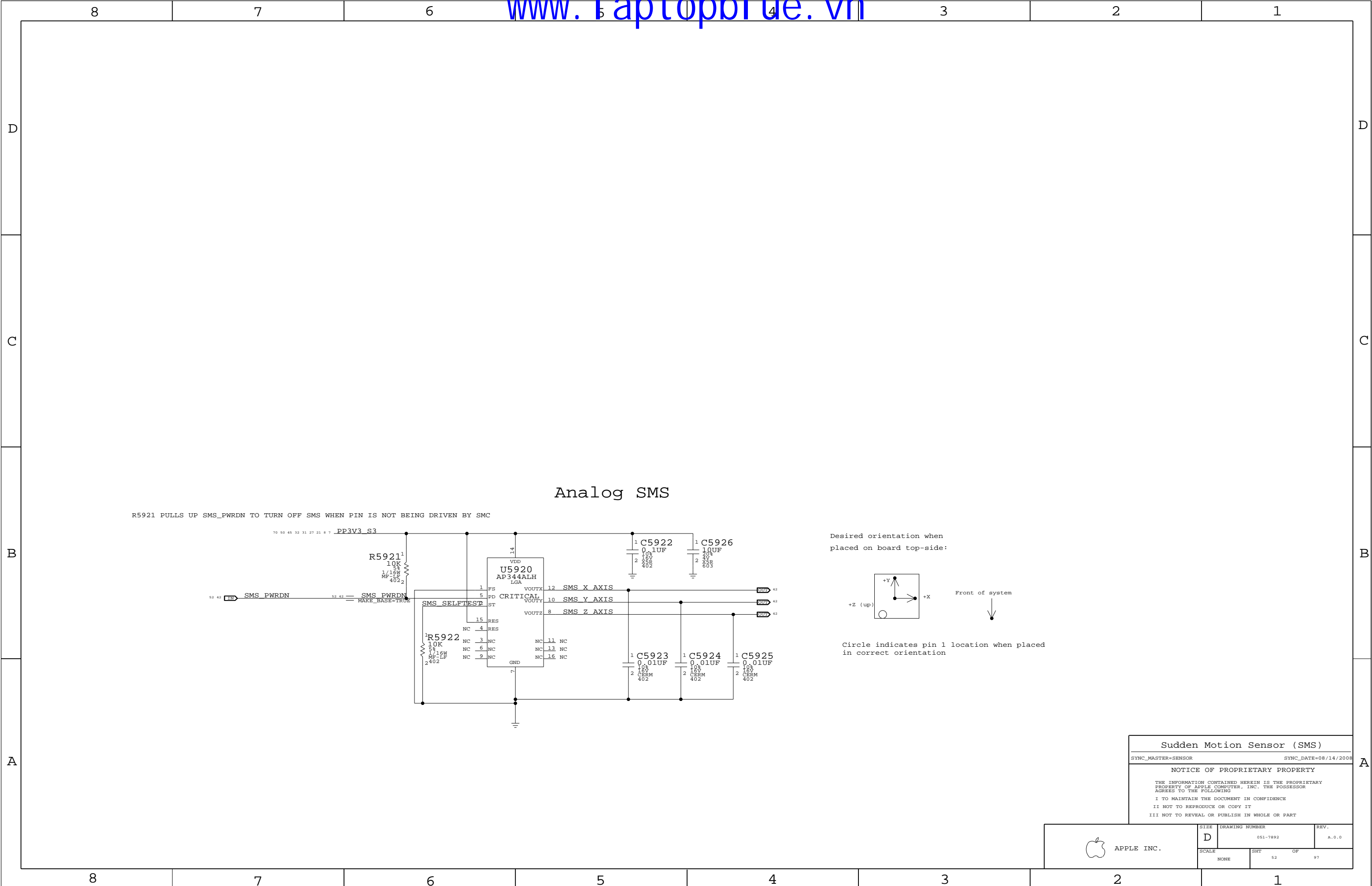
Circle indicates pin 1 location when placed in correct orientation

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SYNC_MASTER=SENSOR		SYNC_DATE=08/14/2008
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D	051-7892	A.0.0

SCALE	SHT	OF
NONE	52	97

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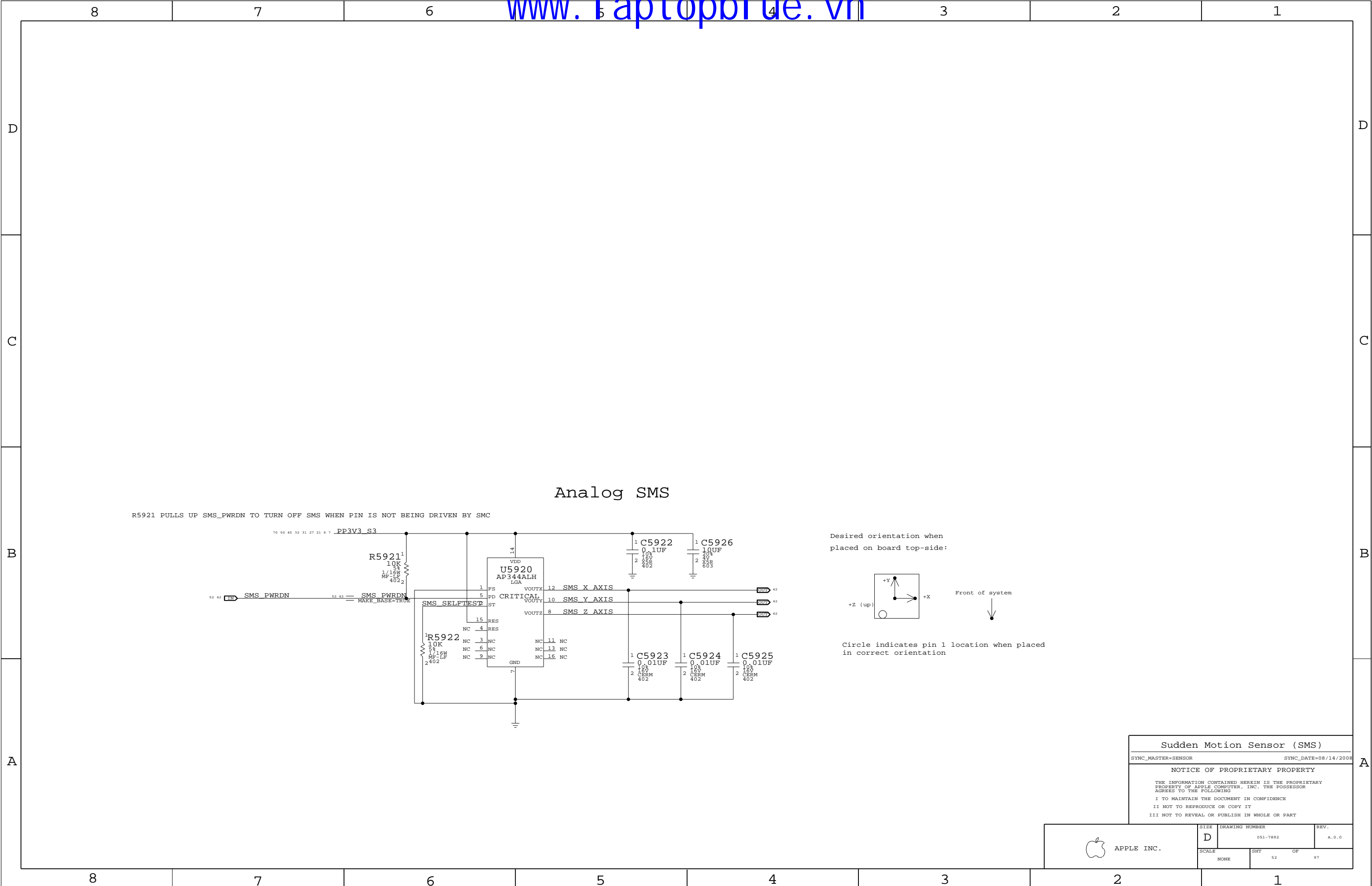
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D	051-7892	A.0.0

SCALE	SHT	OF
NONE	52	97

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NONE	52	97

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Desired orientation when placed on board top-side:

+Z (up)

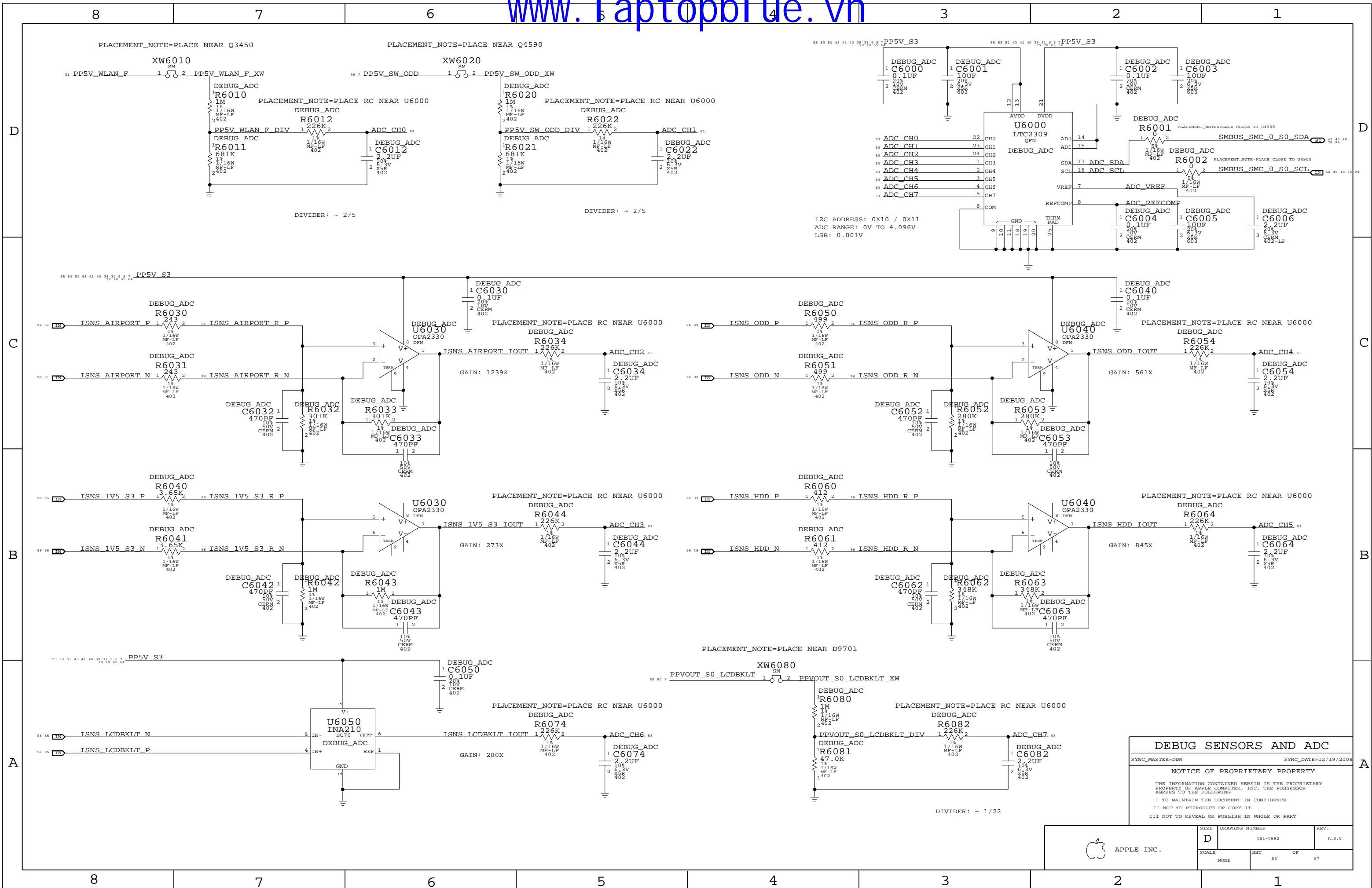
Circle indicates pin 1 location when placed in correct orientation

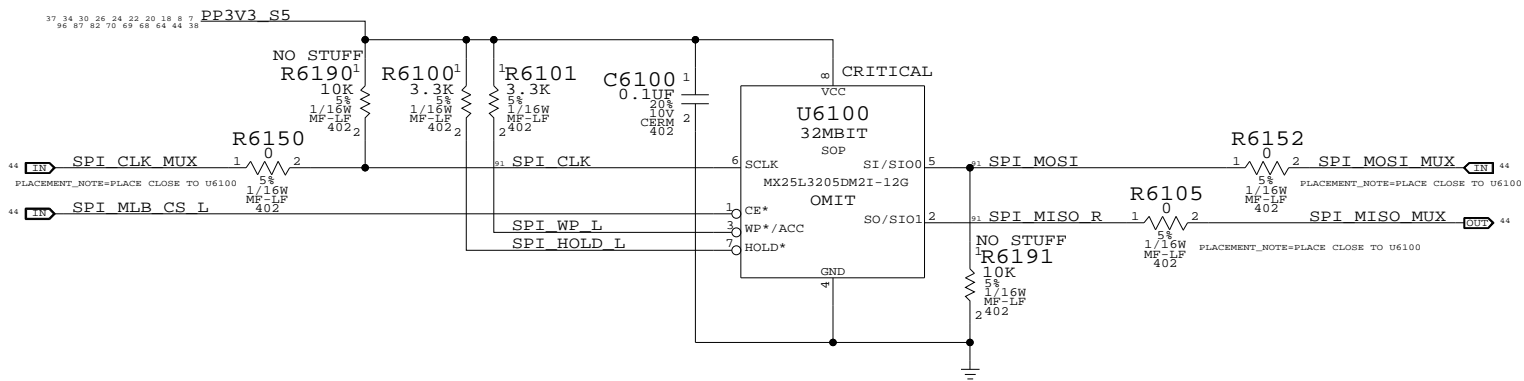
Sudden Motion Sensor (SMS)		
SYNC_MASTER=SENSOR		SYNC_DATE=08/14/2008
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SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0

SCALE	SHT	OF
NONE	52	97

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MCP79 SPI Frequency Select		
Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

25MHz is selected with R5190 and R5191
Any of the 4 frequencies can be selected
with R6190, R6191, R5190 and R5191

SPI ROM

SYNC_MASTER=CHANG_M98_MLBSYNC_DATE=07/01/2008

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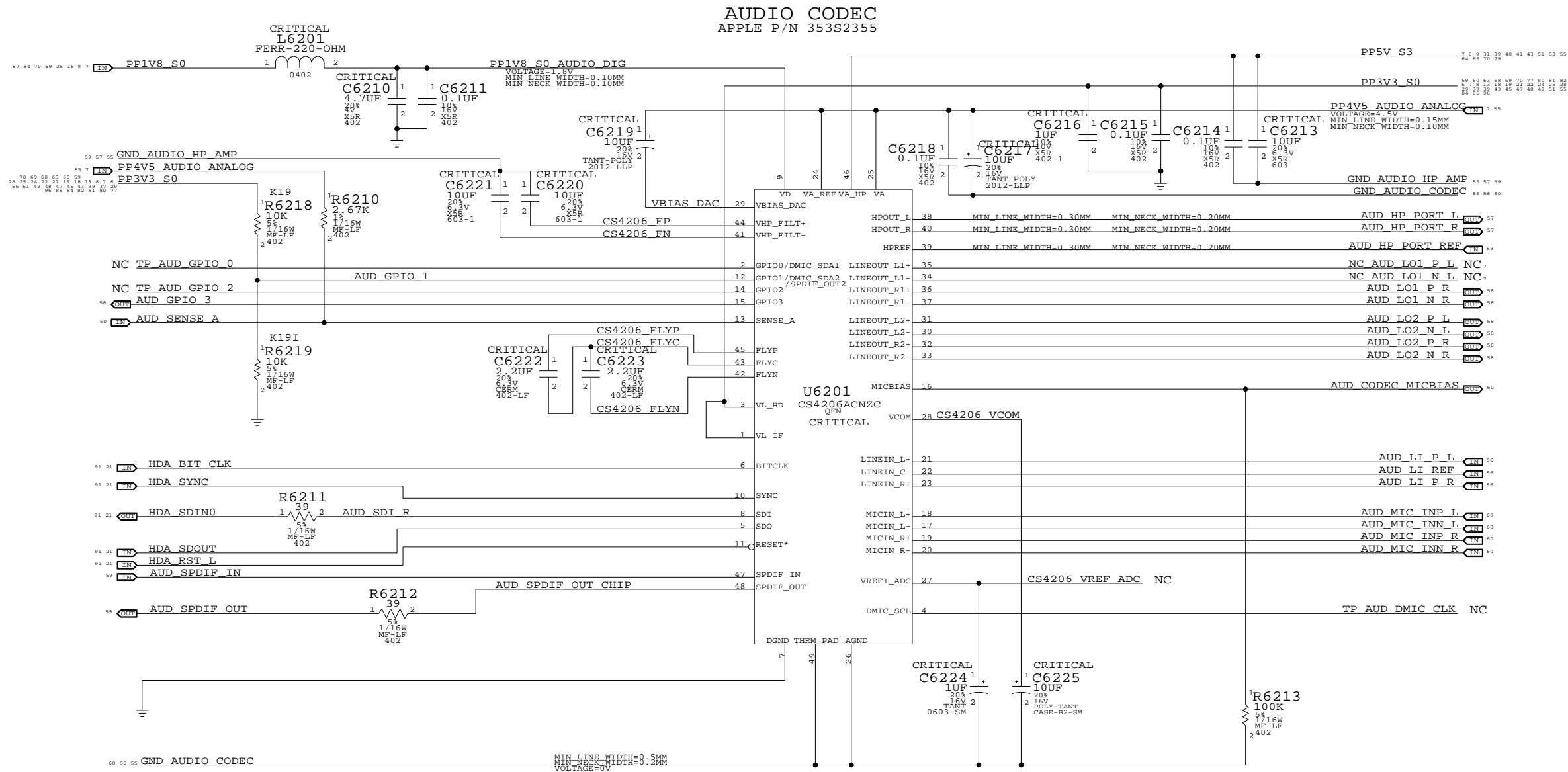
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II NOT TO REPRODUCE OR COPY IT

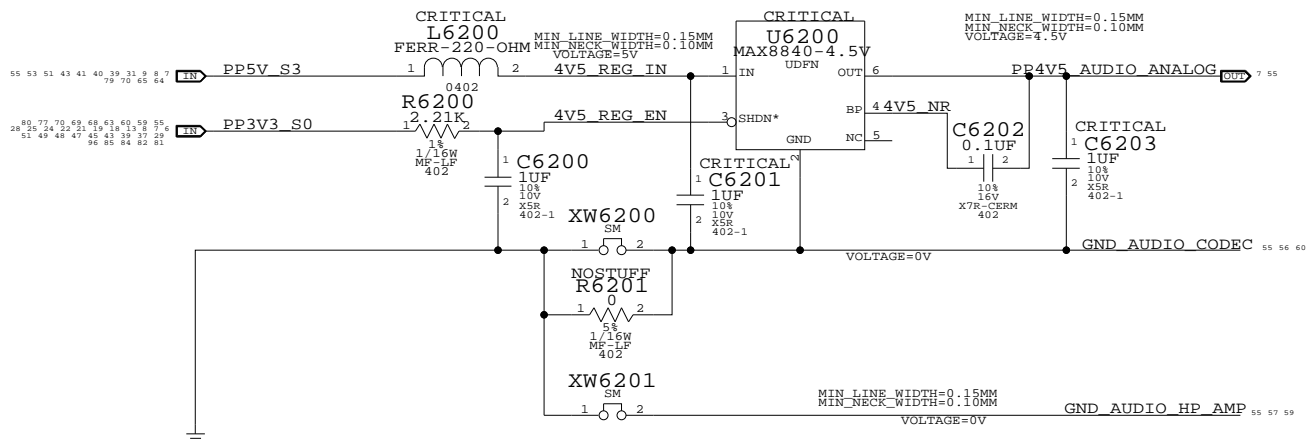
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

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SIZE D	DRAWING NUMBER 051-7892	REV. A.0.0
SCALE NONE	SHT 54	OF 97



4.5V POWER SUPPLY FOR CODEC
APPLE P/N 353S2234



NOTES ON CODEC I/O

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

AUDIO: CODEC/REGULATOR

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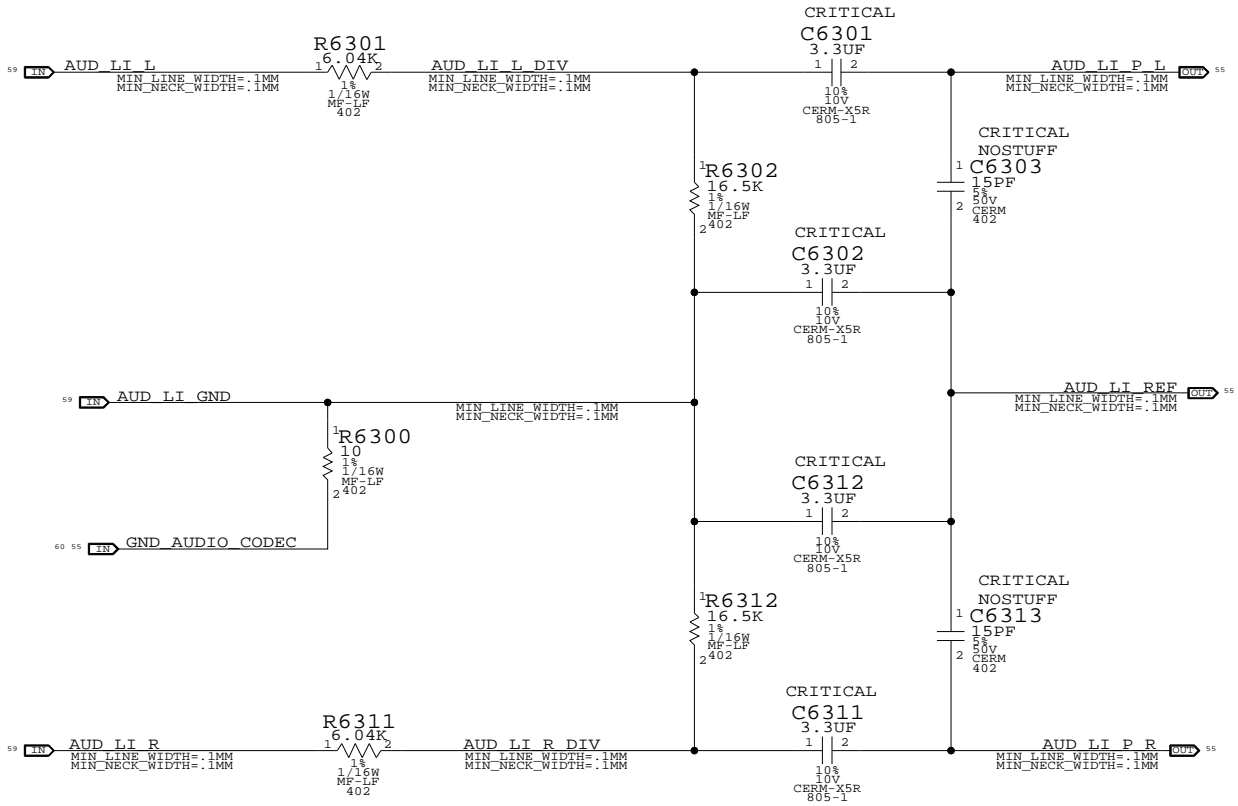


APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE	SHT	OF
NONE	55	97

LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS
NET RIN = 20K OHMS
FC = 8 HZ
VIN = 2VRMS, CODEC VIN = 1.21 VRMS



AUDIO: LINE INPUT FILTER

NOTICE OF PROPRIETARY PROPERTY

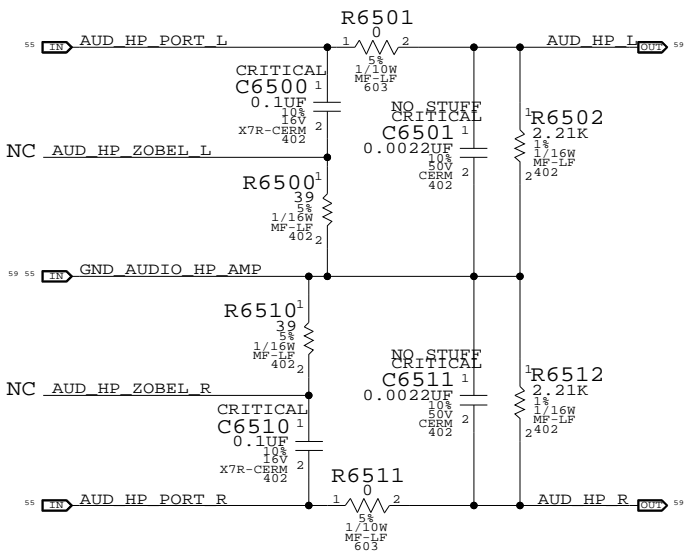
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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE	SHT	OF
NONE	56	97

ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER



AUDIO: HEADPHONE FILTER

SYNC_MASTER=AUDIO SYNC_DATE=03/16/2009

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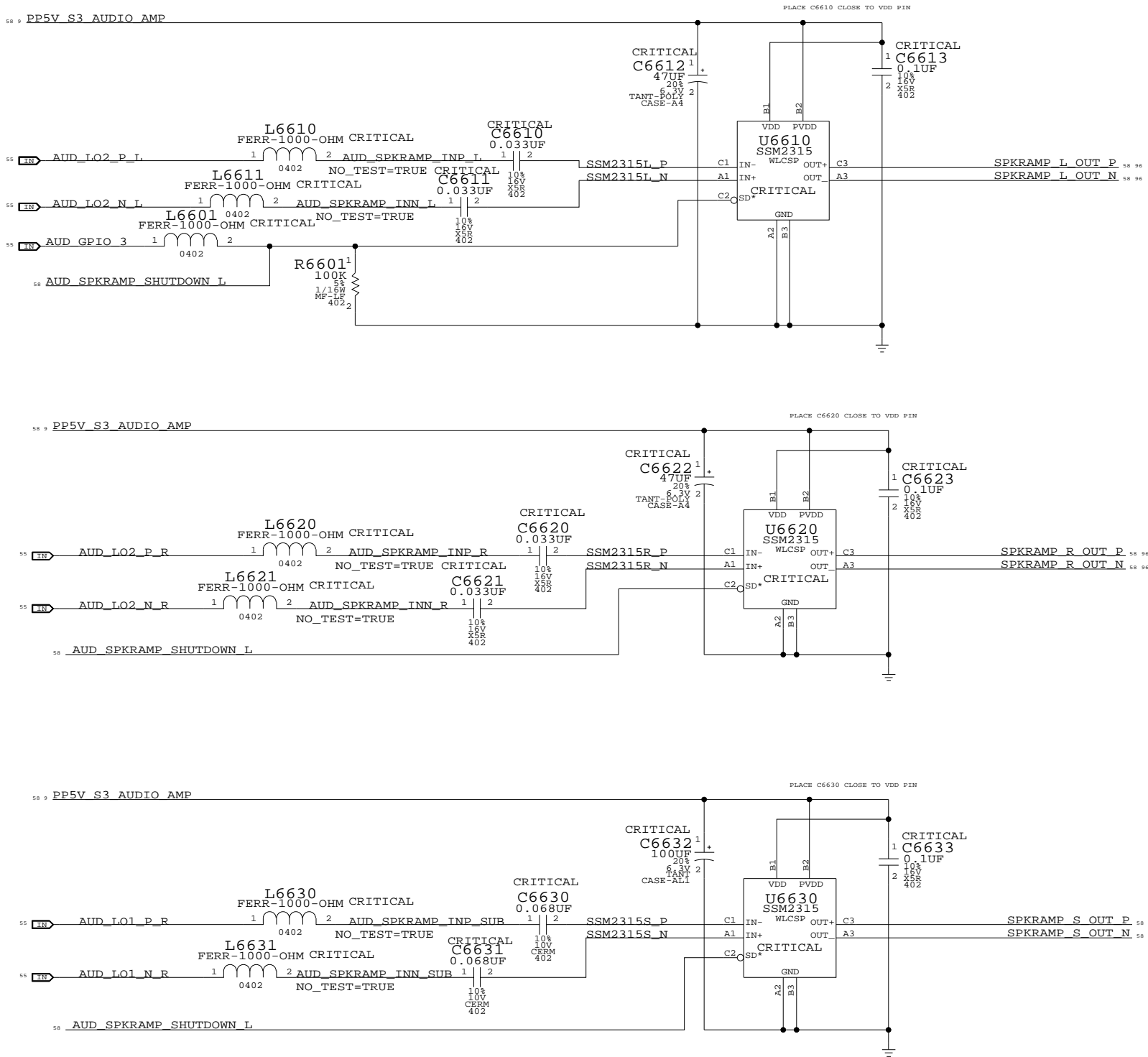
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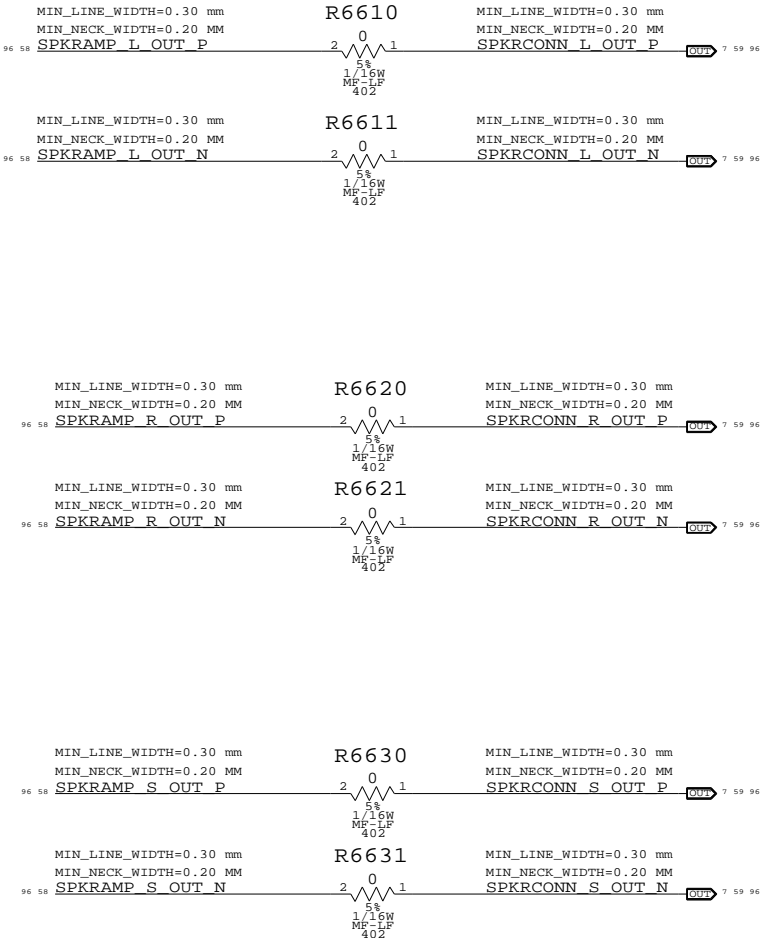
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE	SHT	OF
NONE	57	97

3X MONO SPEAKER AMPLIFIERS (SSM2315)
APN: 353S2500
GAIN = 6DB
1ST ORDER FC (L&R) = 120 HZ +/- 30%
1ST ORDER FC (SUB) = 58HZ +/- 30%



SPEAKER CHECKPOINTS



AUDIO: SPEAKER AMP

SYNC_MASTER=AUDIO SYNC_DATE=03/16/2009

NOTICE OF PROPRIETARY PROPERTY

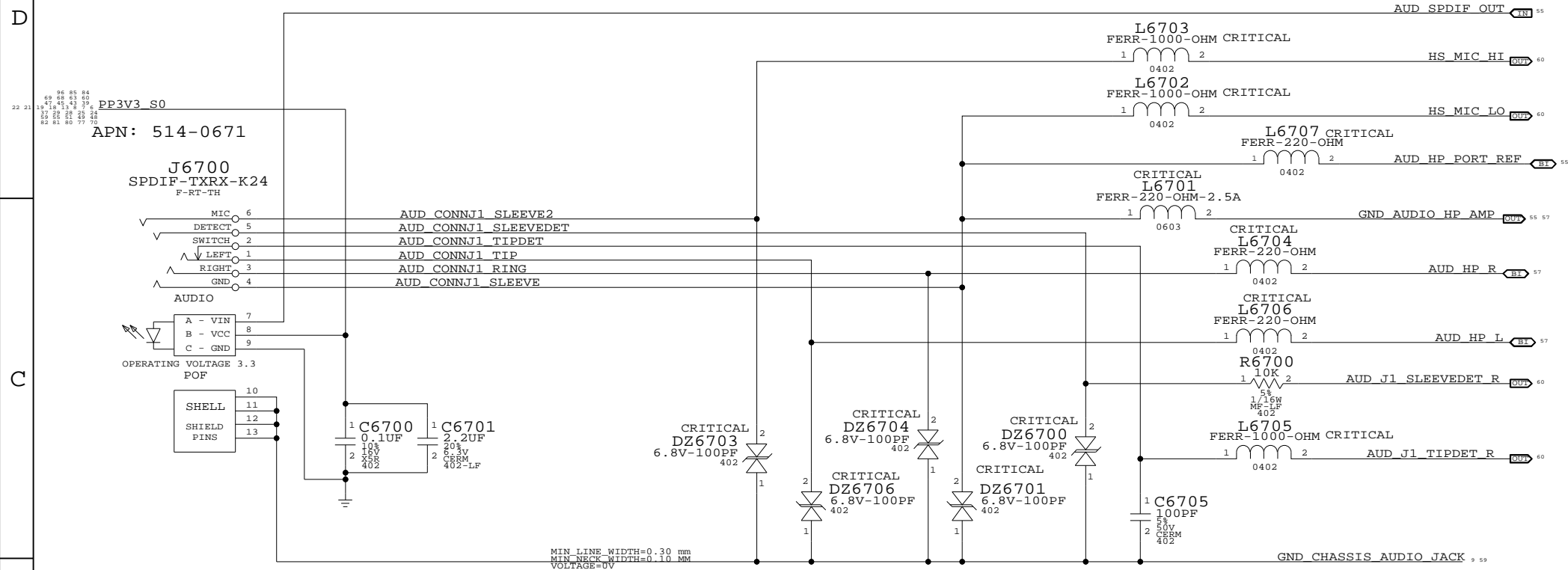
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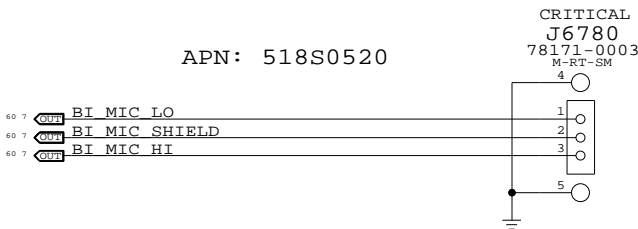
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE	SHT	OF
NONE	58	97

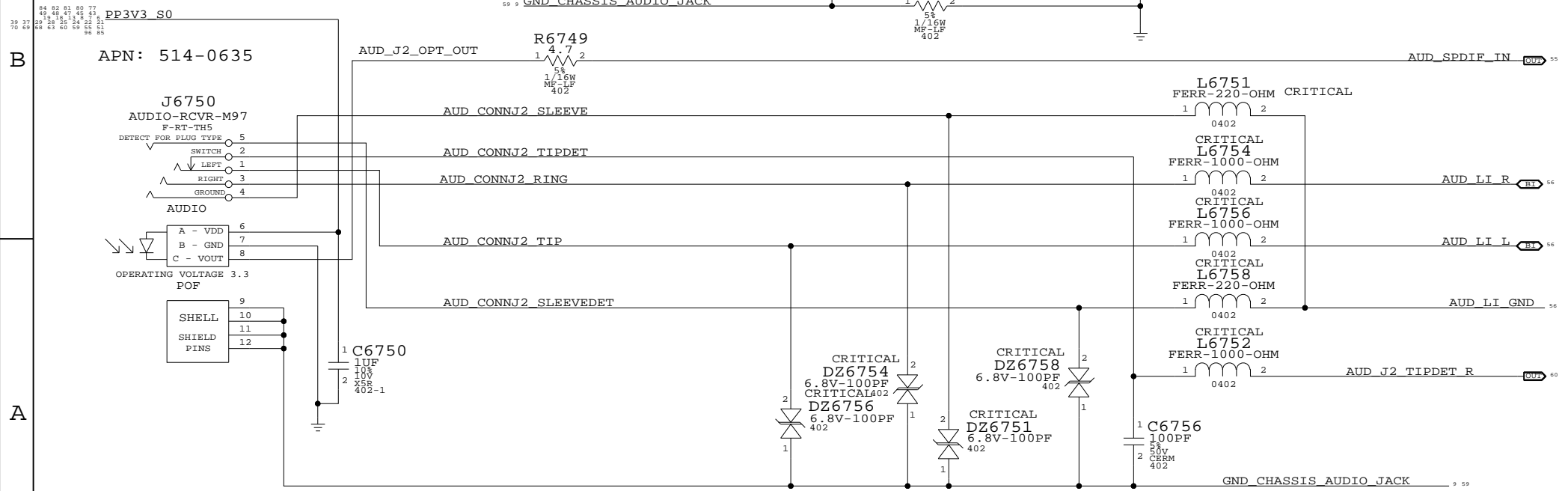
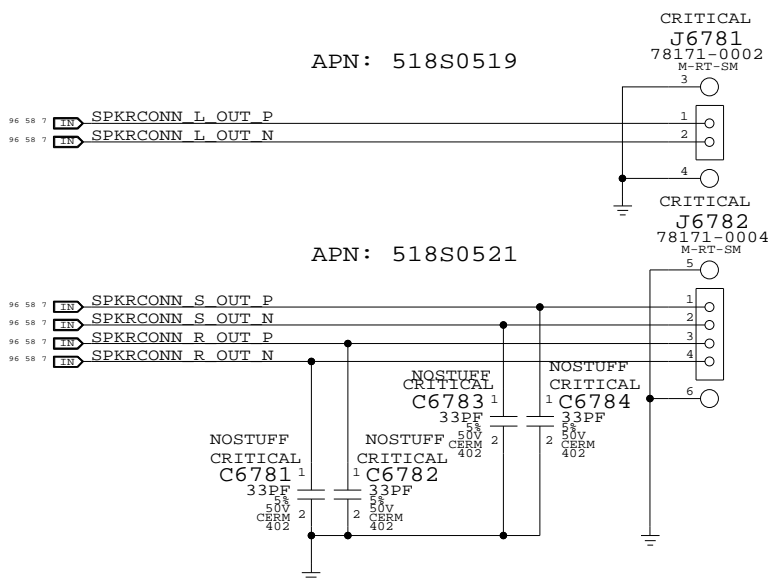
AUDIO JACK 1 LO/HP JACK, SPDIF TX



MIC CONNECTOR



SPEAKER CONNECTOR

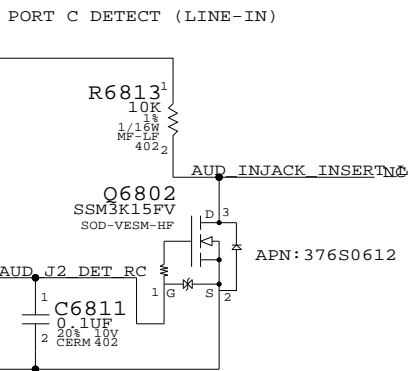
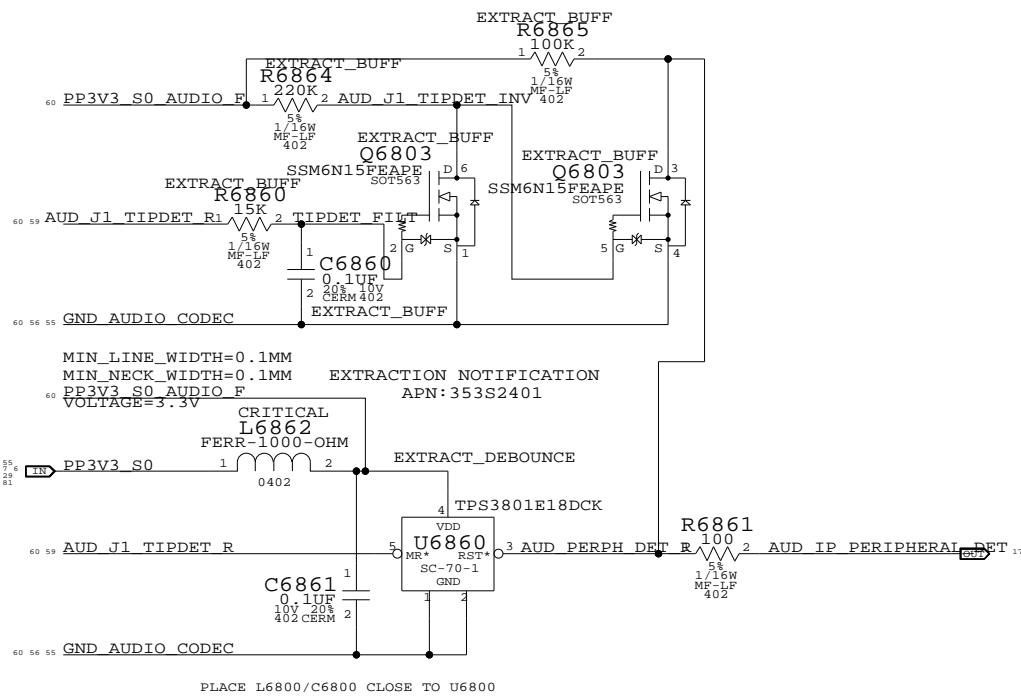



AUDIO JACK 2 LINE IN JACK, SPDIF RX

AUDIO: JACKS		
SYNC_MASTER=AUDIO		SYNC_DATE=03/16/2009
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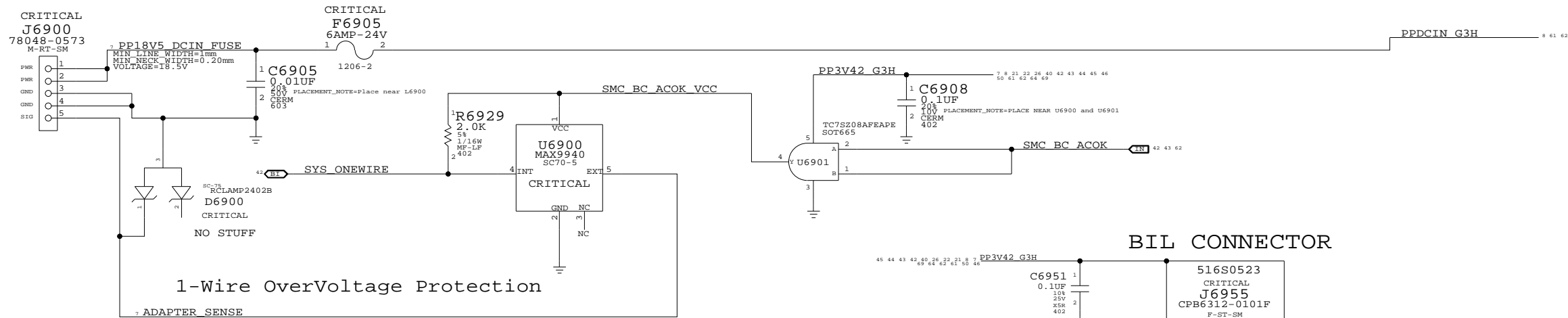
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7892	A.0.0
SCALE		SHT	OF
NONE		59	97

FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X05 (5)	0X0C (12,C)	N/A	0X0C (12,C)
SPDIF IN	0X07 (7)	0X0F (15)	N/A	N/A
BUILT-IN MIC	0X06 (6)	0X0D (13,B,RIGHT)	MIC_BIAS (80%)	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY



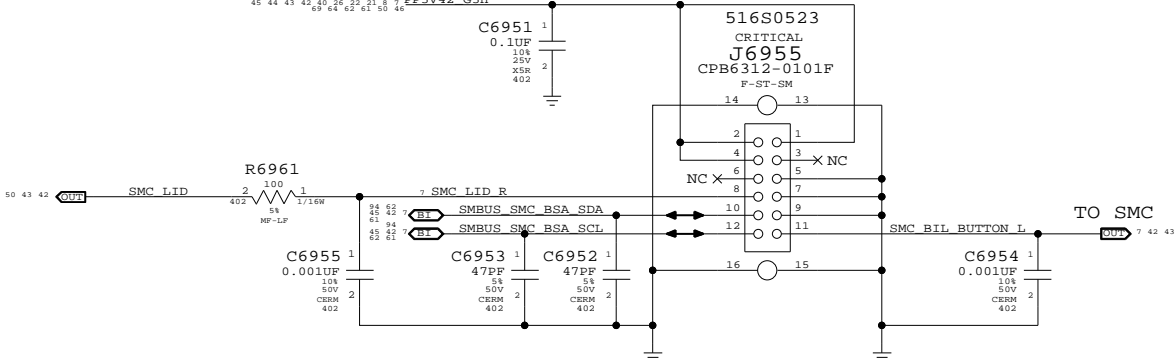
 APPLE INC.	SIZE D	DRAWING NUMBER 051-7892		REV. A. 0. 0
	SCALE NONE	SHT 60	OF 97	

MagSafe DC Power Jack



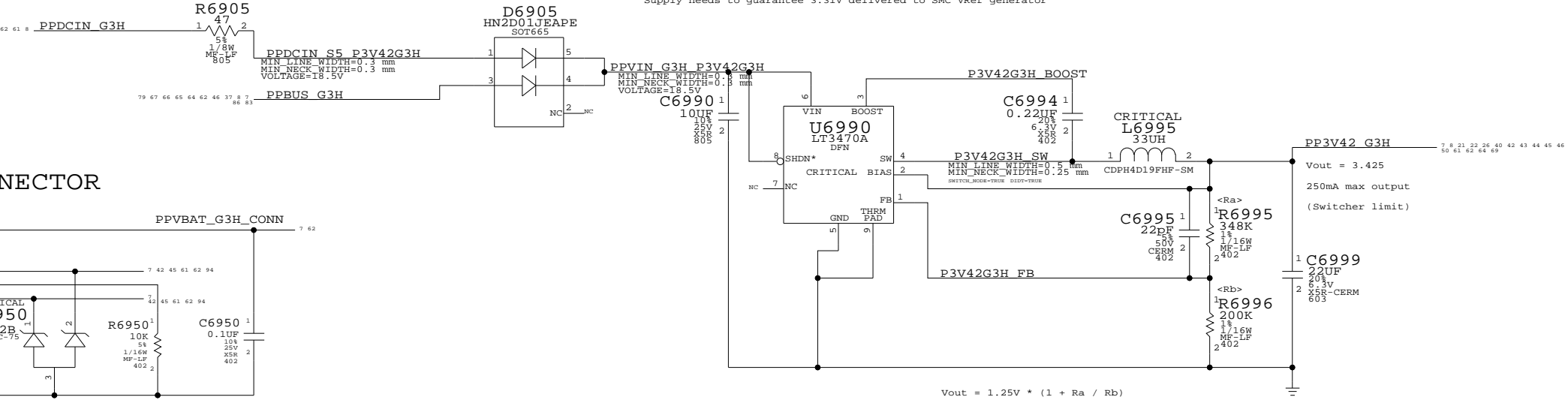
The chassis ground will otherwise float and can send transients onto ADAPTER_SENSE when AC is connected.

BIL CONNECTOR

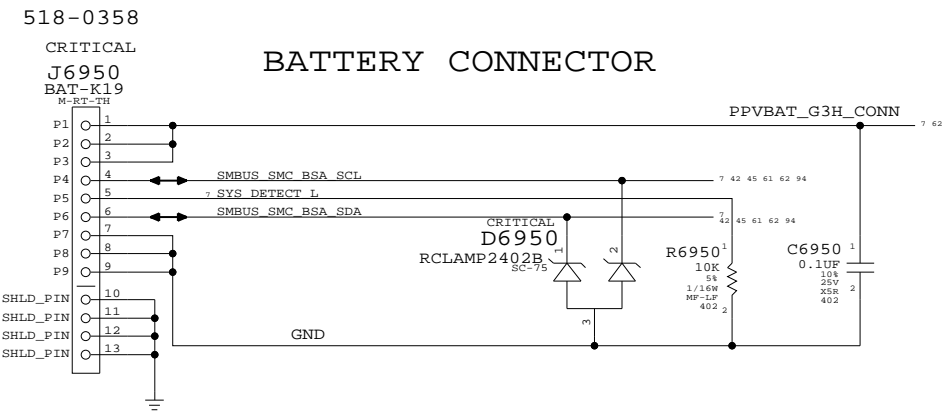


3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



BATTERY CONNECTOR



DC-In & Battery Connectors

SYNC_MASTER=YUN_K19_MLB SYNC_DATE=12/16/2008

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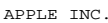
APPLE INC.

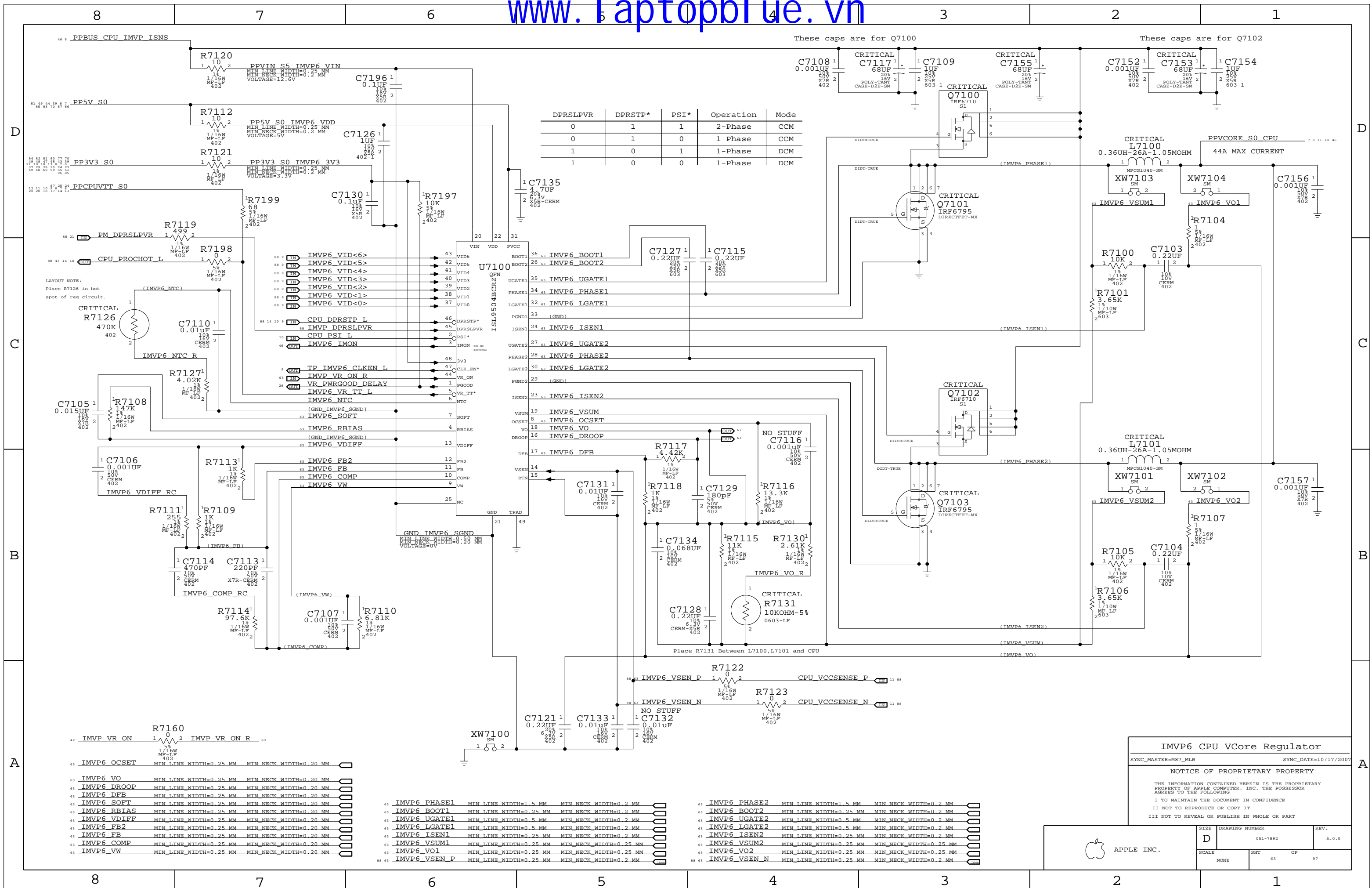
SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE	SHT	OF
NONE	61	97



```
2S Battery Default
3S Battery Default
```

SIZE D	DRAWING NUMBER 051-7892	REV. .
SCALE NONE	SHT 62	OF 97





IMVP6 CPU VCore Regulator

SYNC_MASTER=M87_MLB SYNC_DATE=10/17/2007

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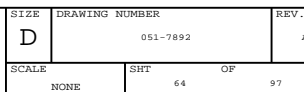
II NOT TO REPRODUCE OR COPY IT

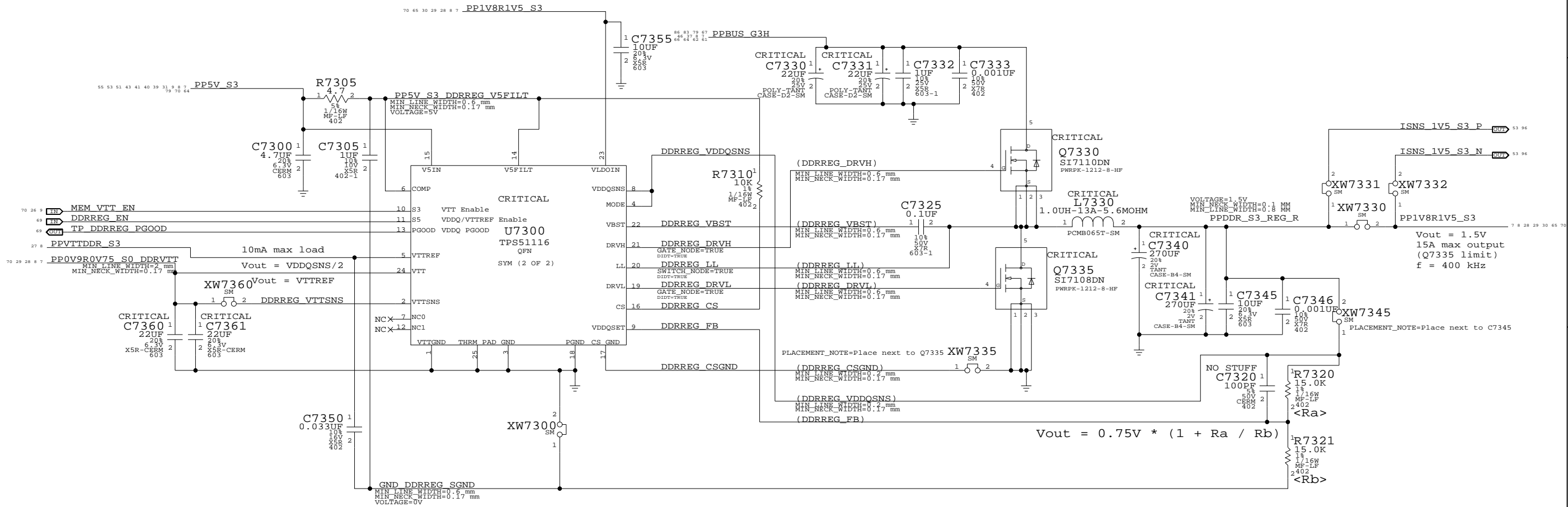
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE	SHT	OF
NONE	63	97

AA



1.5V DDR3 Supply

SYNC_MASTER=DDR SYNC_DATE=12/05/2008

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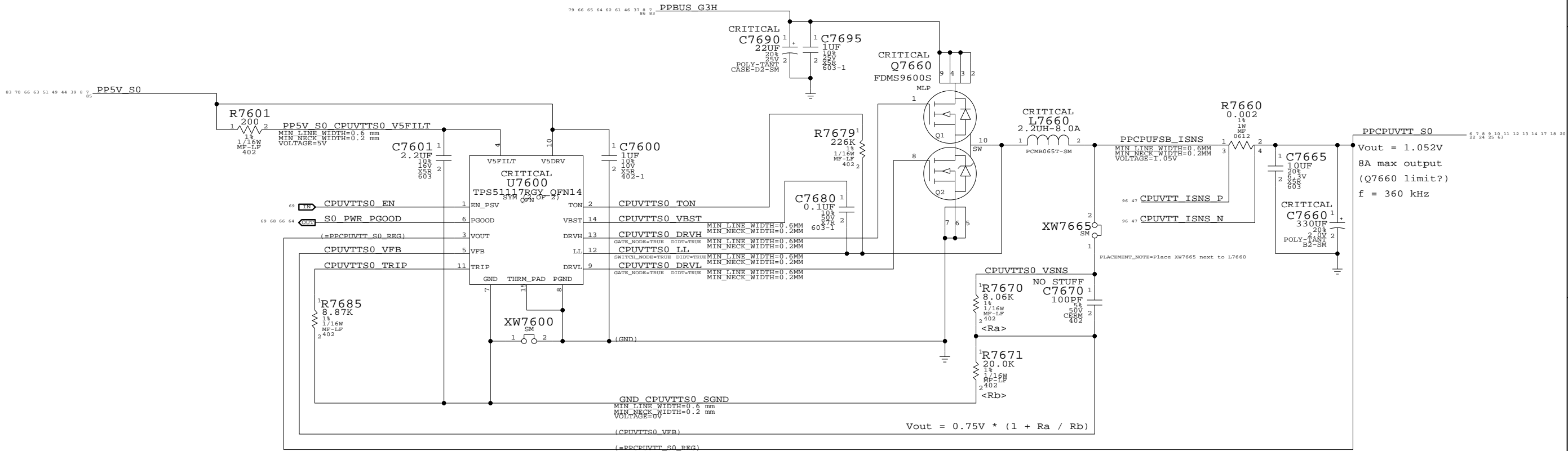
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE INC.



MCP CORE REGULATOR	
SYNC_MASTER=M98_MLB	SYNC_DATE=11/14/2008
NOTICE OF PROPRIETARY PROPERTY	
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III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART	



M99 differences from last sync on 12/03/07 to T18 MLB:
1. Tied THERMAL_PAD to PGND. GND and THERMAL_PAD disconnected.

CPU VTT / 1V05 S0 Power Supply

SYNC_MASTER=M99_MLB

SYNC_DATE=12/14/2007

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APPLE INC.	SIZE	DRAWING NUMBER		REV.
	D	051-7892		A.0.0
SCALE		SHT	OF	REV.
NONE		67	97	

D

C

B

A

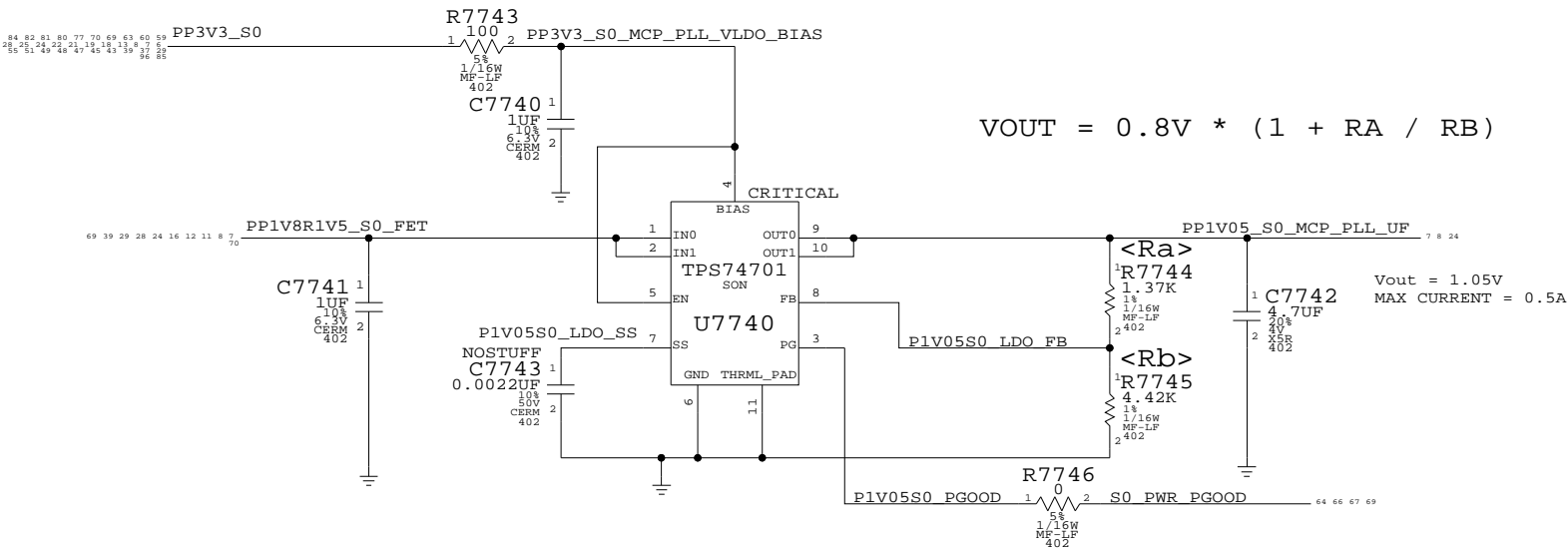
D

C

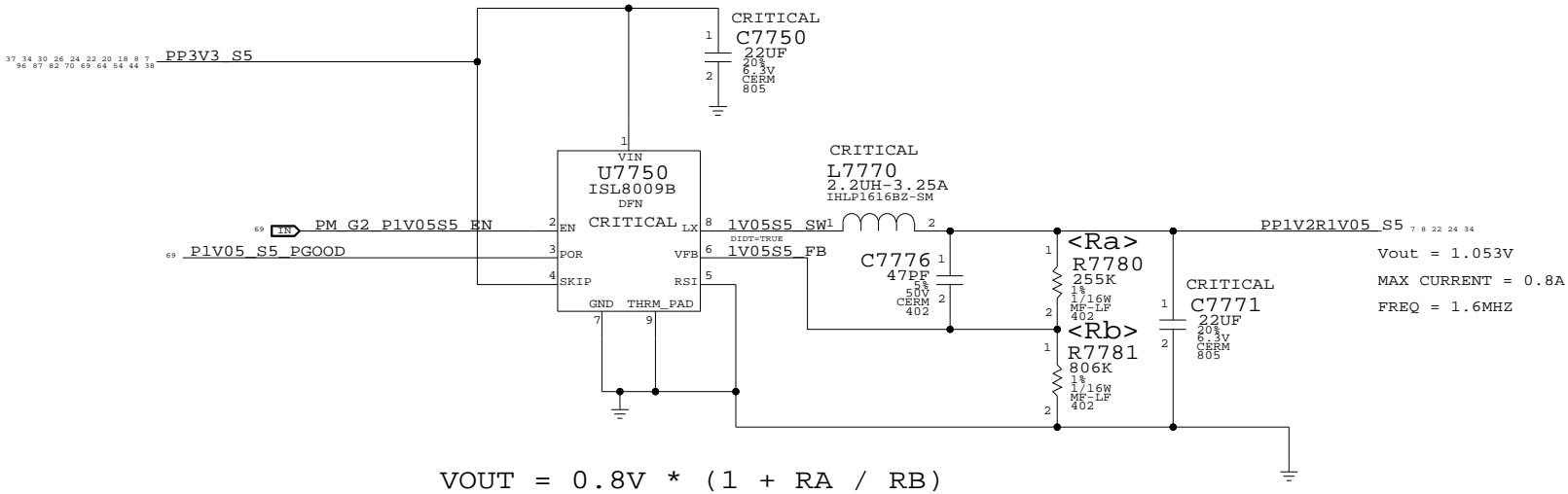
B

A

1.05V S0 PLL LDO



MCP 1.05V S5 (AUXC) SUPPLY



Misc Power Supplies

SYNC_MASTER=M99_MLS SYNC_DATE=12/14/2007

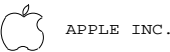
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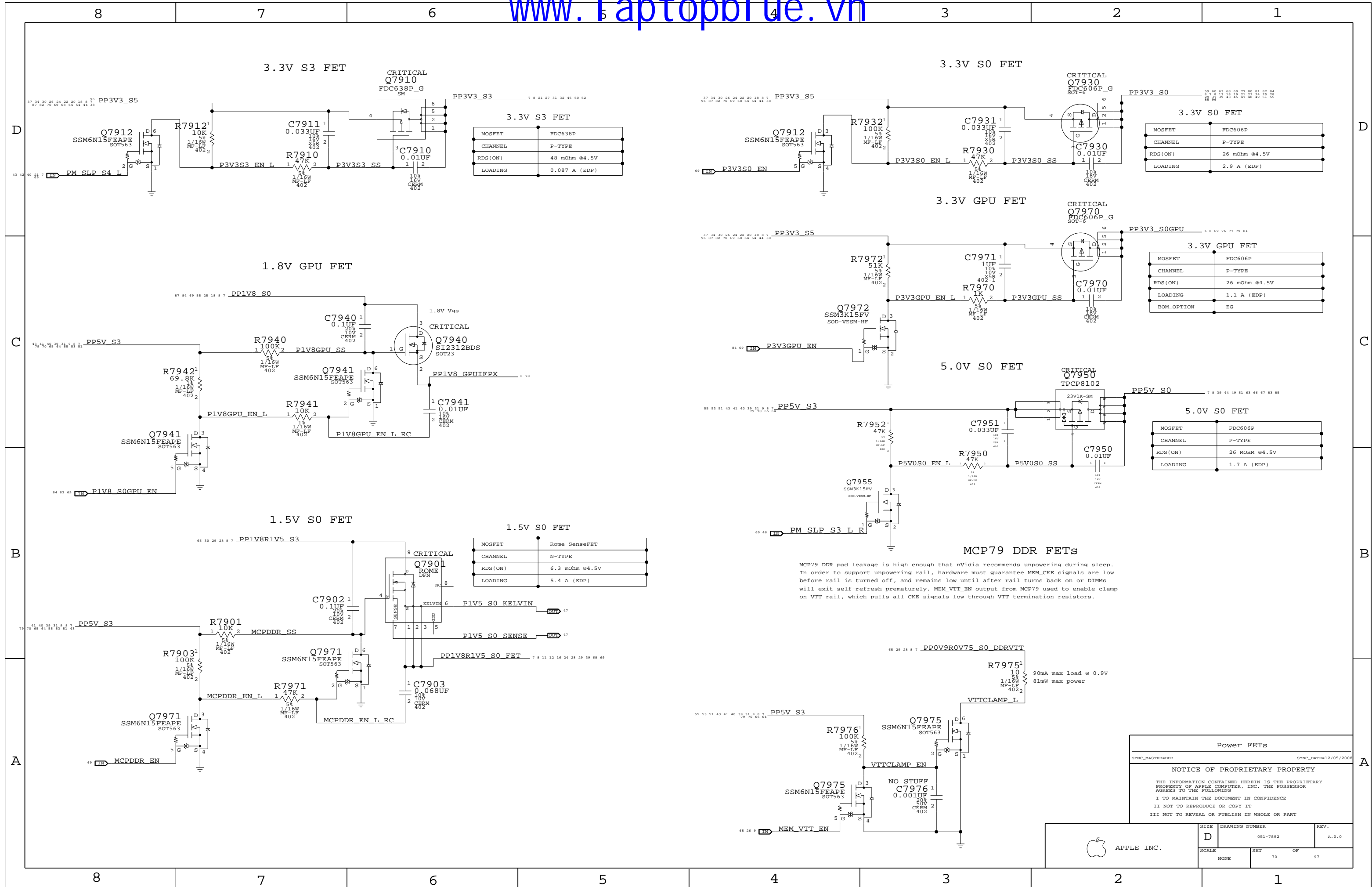
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE INC.

SIZE D DRAWING NUMBER 051-7892 REV. A.0.0

SCALE NONE SHT 68 OF 97



Page Notes

Power aliases required by this page:
- =PPIV2_GPU_PEX_PLLXVDD
- =PPIV2_GPU_PEX_IOVDDQ
- =PPIV2_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

PPIV1 SOGPU REG
PPIV1 SOGPU REG
PPIV1 SOGPU REG

PEX 1.1V Current = 2A

250mA

1500mA

180mA

PPIV1 GPU PEX PLLVDD F
MIN LINE WIDTH=0.25 mm
MIN DRILL WIDTH=0.25 mm
VOLTAGE=1.2V

L8015
10NH-600MA

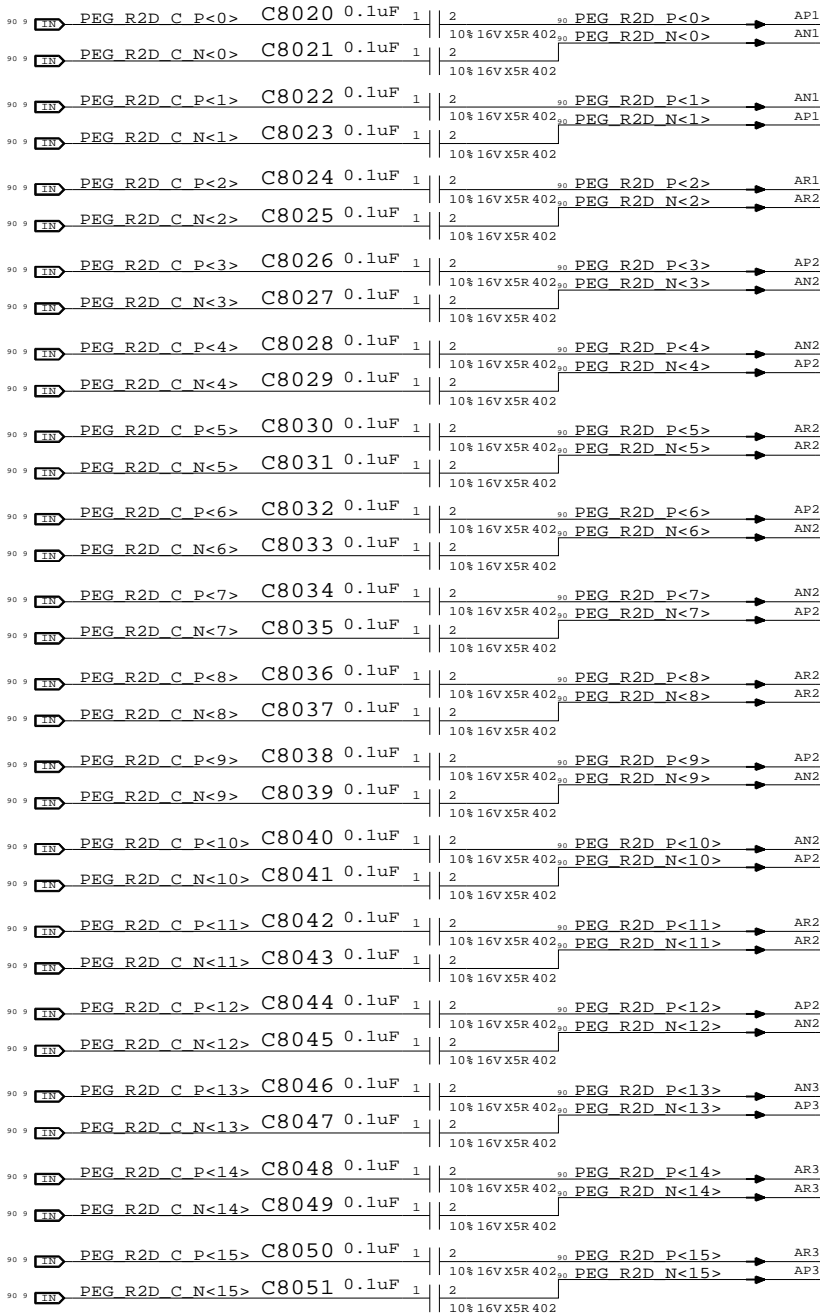
PEX_PLLVDD

VDD_SENSE

GND_SENSE

GPU VDD SENSE

GPU GND SENSE



OMIT

U8000

NB9P-GS

BGA

SYMBOL 1 OF 9

PEX_RX0

PEX_RX0*

PEX_RX1

PEX_RX1*

PEX_RX2

PEX_RX2*

PEX_RX3

PEX_RX3*

PEX_RX4

PEX_RX4*

PEX_RX5

PEX_RX5*

PEX_RX6

PEX_RX6*

PEX_RX7

PEX_RX7*

PEX_RX8

PEX_RX8*

PEX_RX9

PEX_RX9*

PEX_RX10

PEX_RX10*

PEX_RX11

PEX_RX11*

PEX_RX12

PEX_RX12*

PEX_RX13

PEX_RX13*

PEX_RX14

PEX_RX14*

PEX_RX15

PEX_RX15*

PEX_CLK100M P

PEX_CLK100M N

EG RESET L

GPU RESET R L

TP PEX CLKREO L

PEX_RST*

PEX_CLKREQ*

PEX_TSTCLK_OUT

PEX_TSTCLK_OUT*

PEX_TERM

PEX_TERM PD

PEX_RFU1

PEX_RFU2

PEX_TSTCLK P

PEX_TSTCLK N

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Page Notes

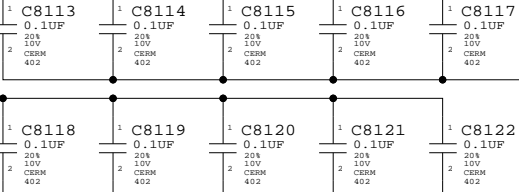
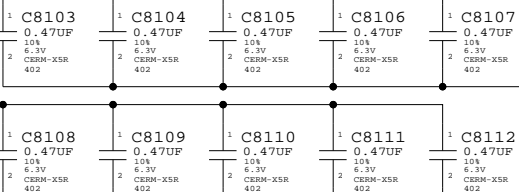
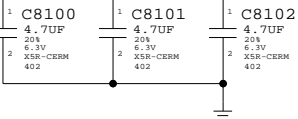
Power aliases required by this page:
- =PPVCORE_GPU
- =PP1V8_GPU_FBVDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

79 PPVCORE_GPU

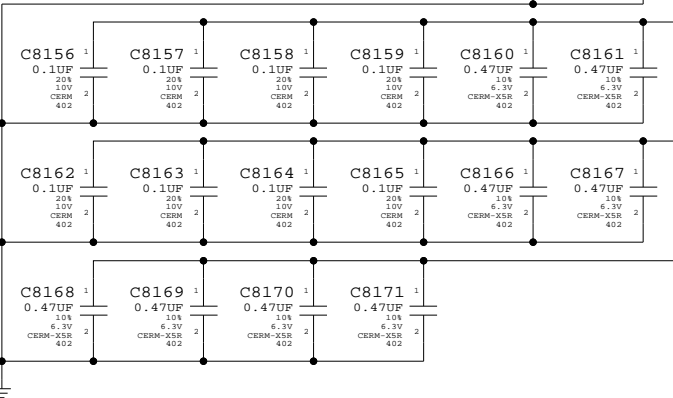
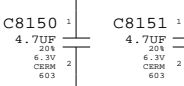
???A @ ???MHz Core/Mem Clk for VDD



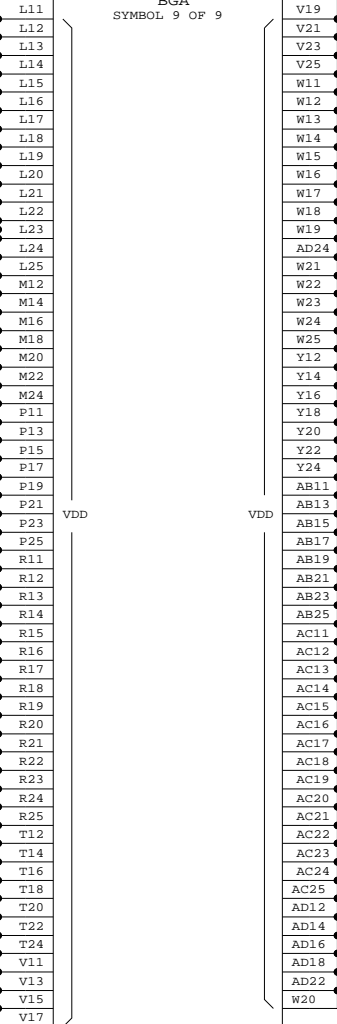
75 74 73 47 9 8 PP1V8_S0GPU_ISNS

Nvidia PRD for GB-128 uses 4x4.7uF, 8x0.47uF, 16x0.1uF

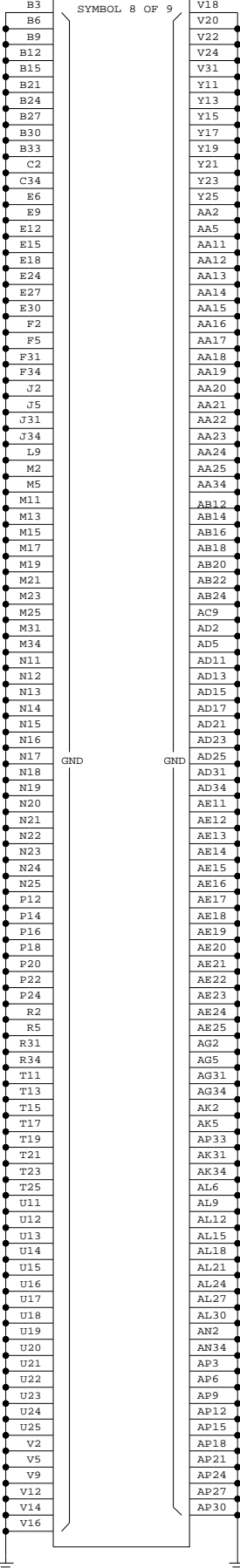
???A @ ???MHz 1.8V GDDR3



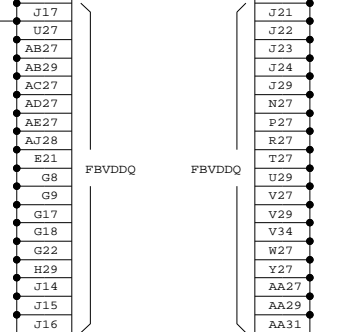
U8000
NB9P-GS
BGA
SYMBOL 9 OF 9



U8000
NB9P-GS
BGA
SYMBOL 8 OF 9



U8000
NB9P-GS
BGA
SYMBOL 7 OF 9



NV G96 Core/FB Power

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

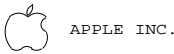
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SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE	SHT	OF
NONE	72	97

Page Notes

Power aliases required by this page:

- =PP1V2_GPU_FBPLLAVDD
- =PP1V8_GPU_FBIO

Signal aliases required by this page:

(NONE)

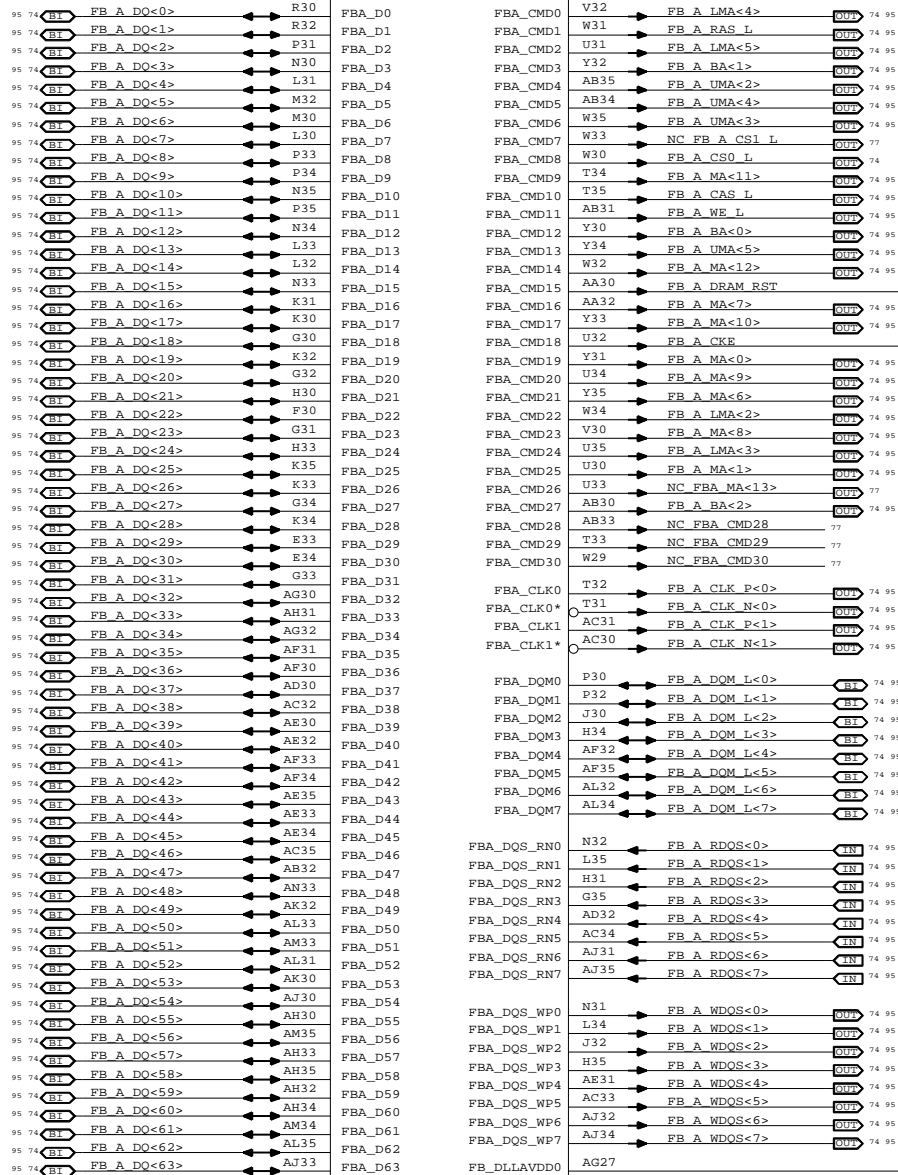
BOM options provided by this page:

(NONE)

OMIT

U8000
NB9P-GS
BGA

SYMBOL 3 OF 9



FBA_CMD0

FBA_CMD1

FBA_CMD2

FBA_CMD3

FBA_CMD4

FBA_CMD5

FBA_CMD6

FBA_CMD7

FBA_CMD8

FBA_CMD9

FBA_CMD10

FBA_CMD11

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FBA_CMD295

FBA_CMD296

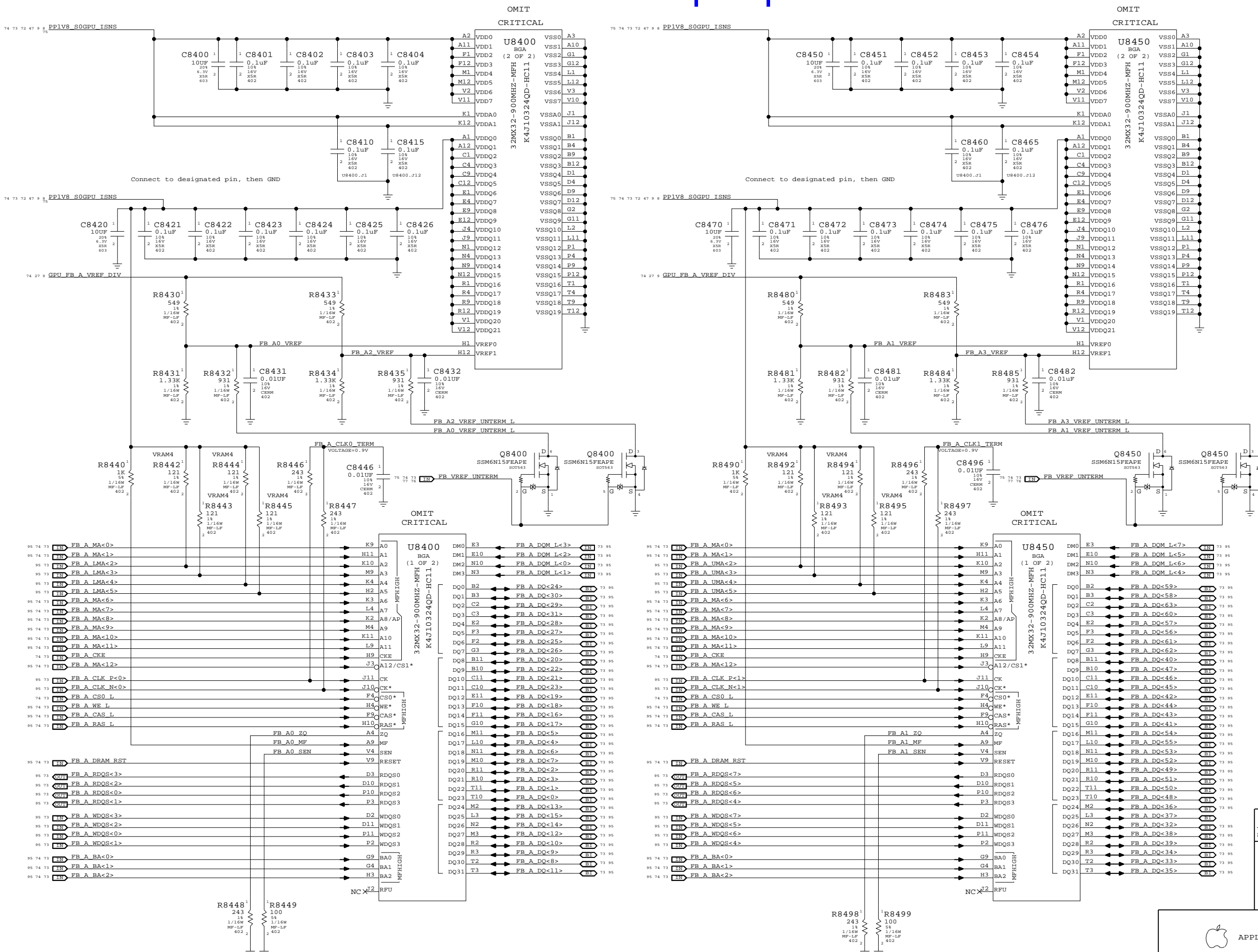
FBA_CMD297

FBA_CMD298

Power aliases required by this page:
- =PPIV8_S0_FB_VDD
- =PPIV8_S0_FB_VREFA

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
VRAM4



GDDR3 Frame Buffer A (Top)

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

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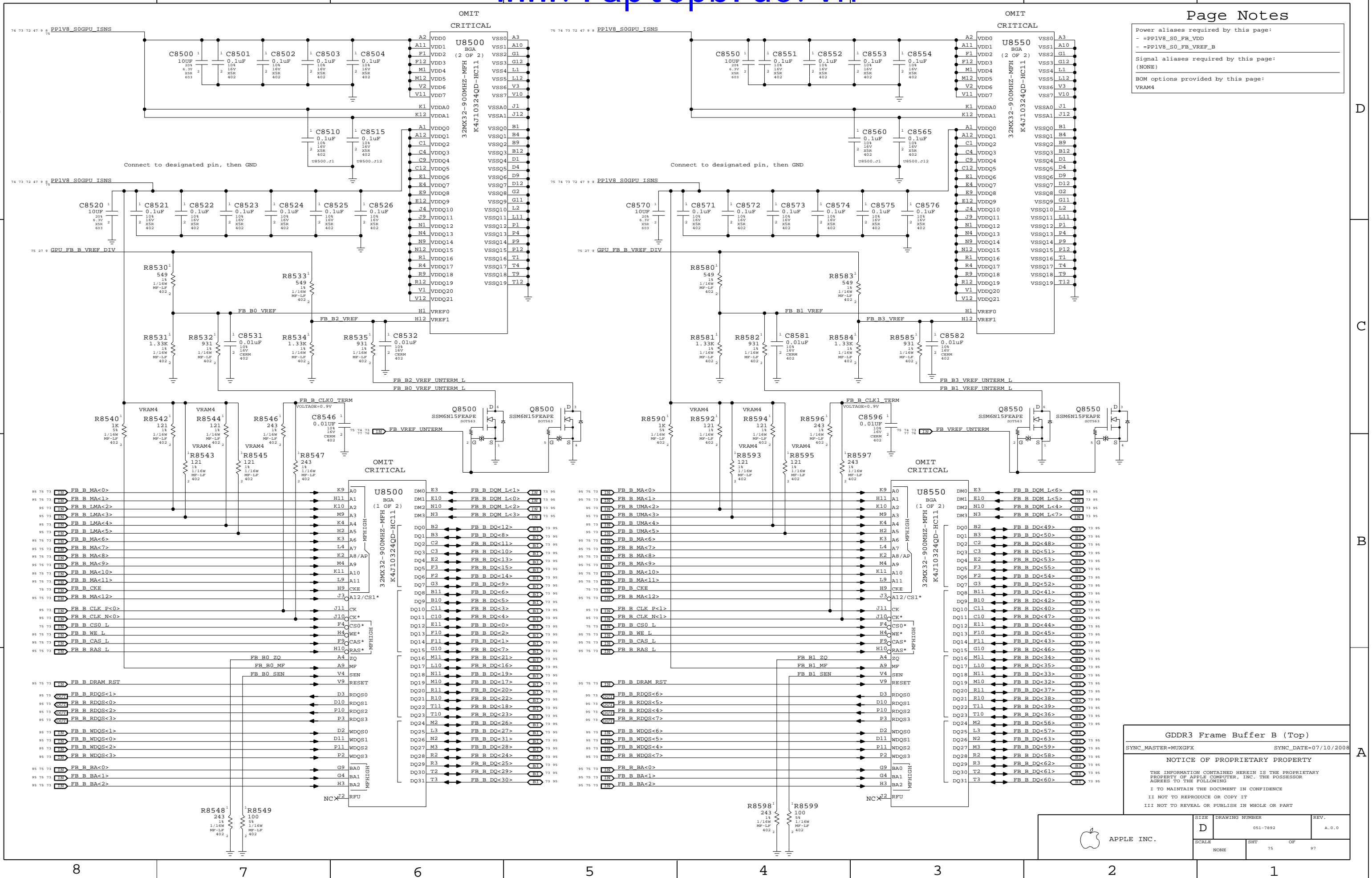
SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE	SIT	OF
NONE	74	97

Power aliases required by this page:

```
- =PP1V8_S0_FB_VDD
```

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
VRAM4



Page Notes

Power aliases required by this page:

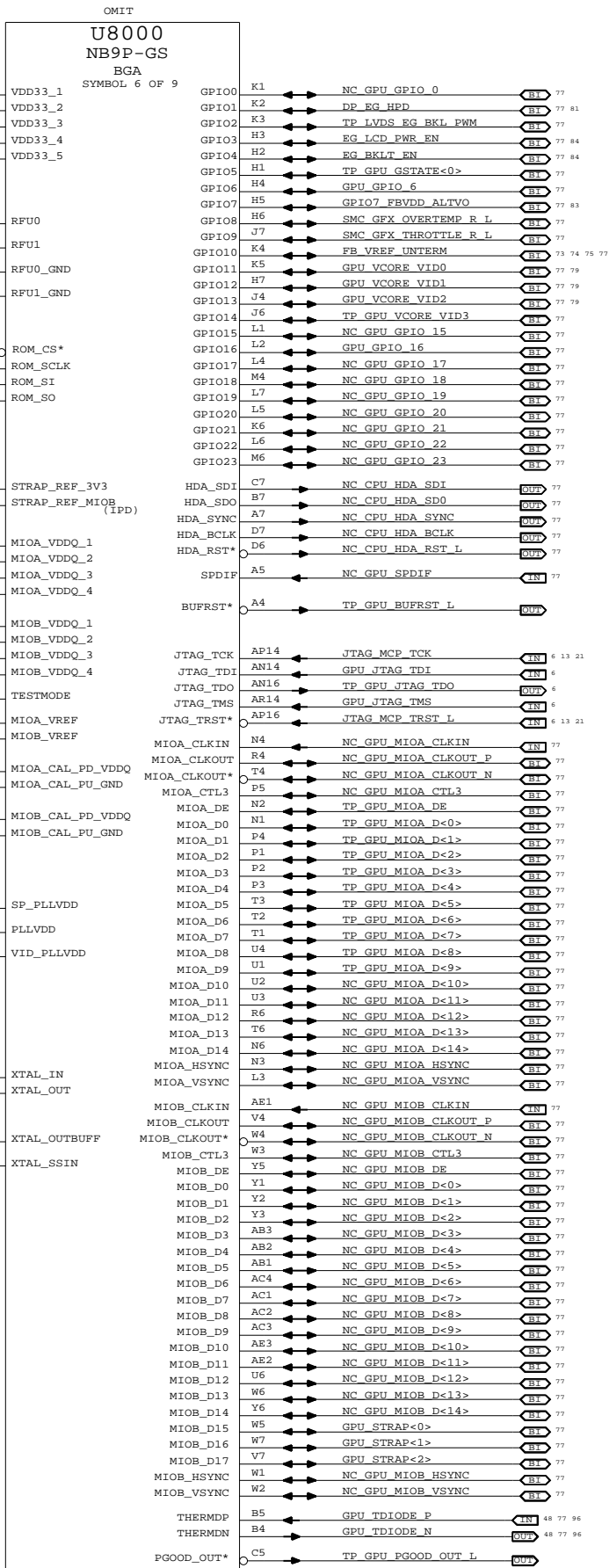
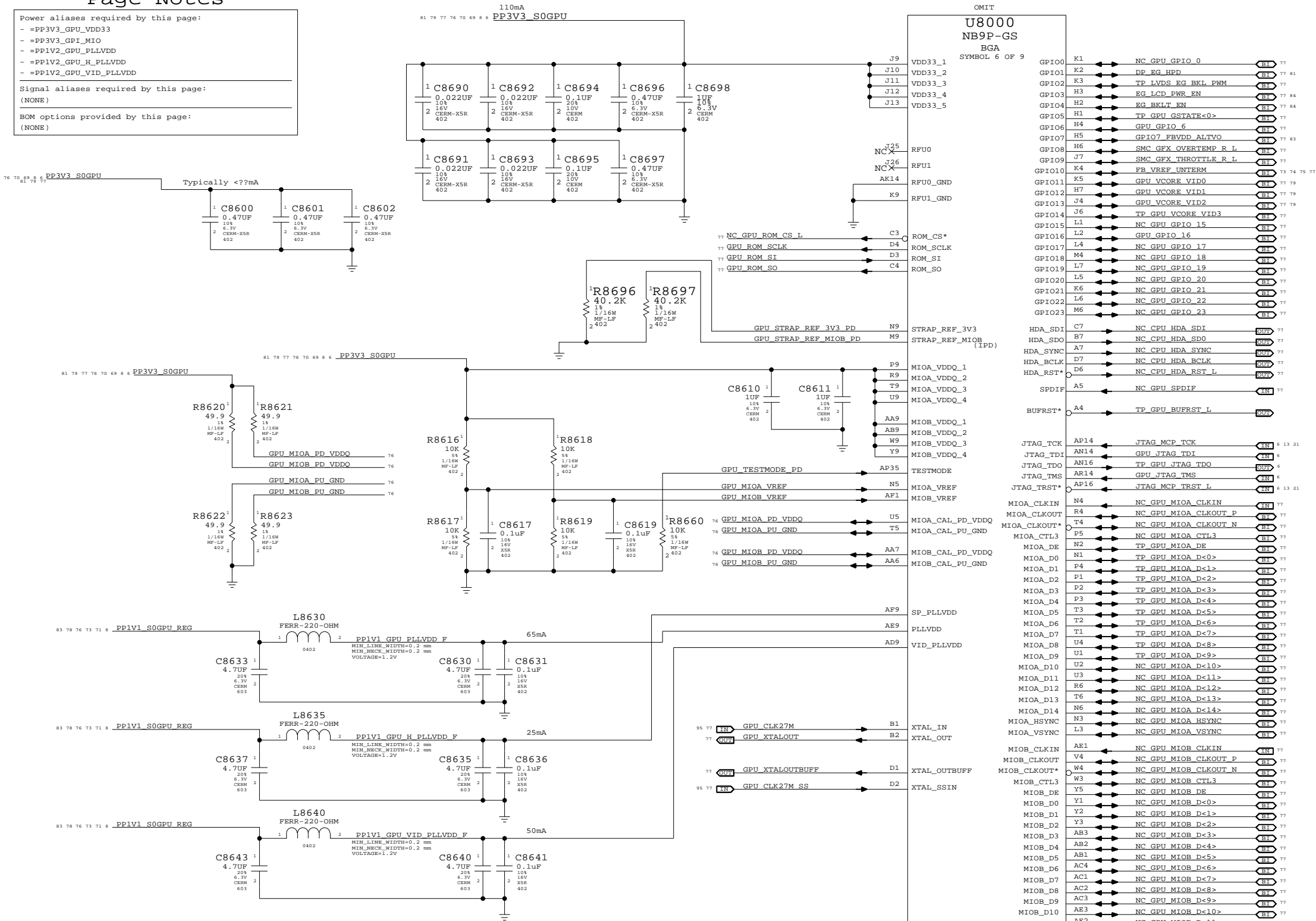
- =PP3V3_GPU_VDD33
- =PP3V3_GPU_MIO
- =PP1V2_GPU_PLLVDD
- =PP1V2_GPU_H_PLLVDD
- =PP1V2_GPU_VID_PLLVDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)



Page Notes

Power aliases required by this page:
- =PP1V8_GPU_IPFX
- =PP3V3_GPU_IFPCD_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Sum of peak currents: 240mA

70 8 PP1V8_GPU_IPFX

L8800

FERR-220-OHM

0402

?mA peak per diff pair

?mA peak for all pairs

C8800

4.7UF

20% 6.3V CERM 603

C8801

0.1UF

20% 10V CERM 402

C8803

0.1UF

20% 10V CERM 402

Place at AG9

Place at AG10

PP1V8_GPU_IPFAB_IOVDD_F

MIN_LINE_WIDTH=0.4 mm

MIN_NECK_WIDTH=0.2 mm

VOLTAGE=1.8V

OMIT

U8000

NB9P-GS

BGA

SYMBOL 5 OF 9

IFPA_TXC

IFPA_TXC*

IFPA_TXD0

IFPA_TXD0*

IFPA_TXD1

IFPA_TXD1*

IFPA_TXD2

IFPA_TXD2*

IFPA_TXD3

IFPB_TXC

IFPB_TXC*

IFPB_TXD4

IFPB_TXD4*

IFPB_TXD5

IFPB_TXD5*

IFPB_TXD6

IFPB_TXD6*

IFPB_TXD7

IFPC_AUX

IFPC_AUX*

IFPC_L0

IFPC_L0*

IFPC_L1

IFPC_L1*

IFPC_L2

IFPC_L2*

IFPC_L3

IFPC_L3*

IFPD_AUX

IFPD_AUX*

IFPD_L0

IFPD_L0*

IFPD_L1

IFPD_L1*

IFPD_L2

IFPD_L2*

IFPD_L3

IFPD_L3*

IFPE_AUX

IFPE_AUX*

IFPE_L0

IFPE_L0*

IFPE_L1

IFPE_L1*

IFPE_L2

IFPE_L2*

IFPE_L3

IFPE_L3*

IFPF_AUX

IFPF_AUX*

IFPF_L0

IFPF_L0*

IFPF_L1

IFPF_L1*

IFPF_L2

IFPF_L2*

IFPF_L3

IFPF_L3*

DACA_RED

DACA_GREEN

DACA_BLUE

DACA_HSYNC

DACA_VSYNC

DACB_RED

DACB_GREEN

DACB_BLUE

DACB_CSNC

DACC_RED

DACC_GREEN

DACC_BLUE

DACC_HSYNC

DACC_VSYNC

AM11

AM12

AM8

AL8

AM10

AM9

AK10

AL10

AK11

AL11

AP13

AN13

AN8

AP8

AP10

AN10

AR11

AR10

AN11

AP11

AP2

AN3

AM7

AL5

AM5

AM3

AM4

AP1

AR2

AP4

AN1

AR8

AL6

AM6

AL5

AM5

AM3

AM4

AP1

AR2

AP4

AN1

AR8

AL6

AM6

AL5

AM5

AM3

AM4

AP1

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AM6

AL5

AM5

AM3

AM4

AP1

AR2

AP4

AN1

AR8

AL6

AM6

AL5

AM5

AM3

AM4

LVDS EG A CLK P

LVDS EG A CLK N

LVDS EG A DATA P<0>

LVDS EG A DATA N<0>

LVDS EG A DATA P<1>

LVDS EG A DATA N<1>

LVDS EG A DATA P<2>

LVDS EG A DATA N<2>

NC LVDS EG A DATA P<3>

NC LVDS EG A DATA N<3>

TP LVDS EG B CLK P

TP LVDS EG B CLK N

LVDS EG B DATA P<0>

LVDS EG B DATA N<0>

LVDS EG B DATA P<1>

LVDS EG B DATA N<1>

LVDS EG B DATA P<2>

LVDS EG B DATA N<2>

NC LVDS EG B DATA P<3>

NC LVDS EG B DATA N<3>

DP EG AUX CH P

DP EG AUX CH N

DP EG ML P<0>

DP EG ML N<0>

DP EG ML P<1>

DP EG ML N<1>

DP EG ML P<2>

DP EG ML N<2>

DP EG ML P<3>

DP EG ML N<3>

DP EG ML P<0>

DP EG ML N<0>

DP EG ML P<1>

DP EG ML N<1>

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DP EG ML N<2>

DP EG ML P<3>

DP EG ML N<3>

DP EG ML P<0>

DP EG ML N<0>

DP EG ML P<1>

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DP EG ML P<3>

DP EG ML N<3>

DP EG ML P<0>

DP EG ML N<0>

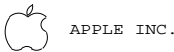
DP EG ML P<1>

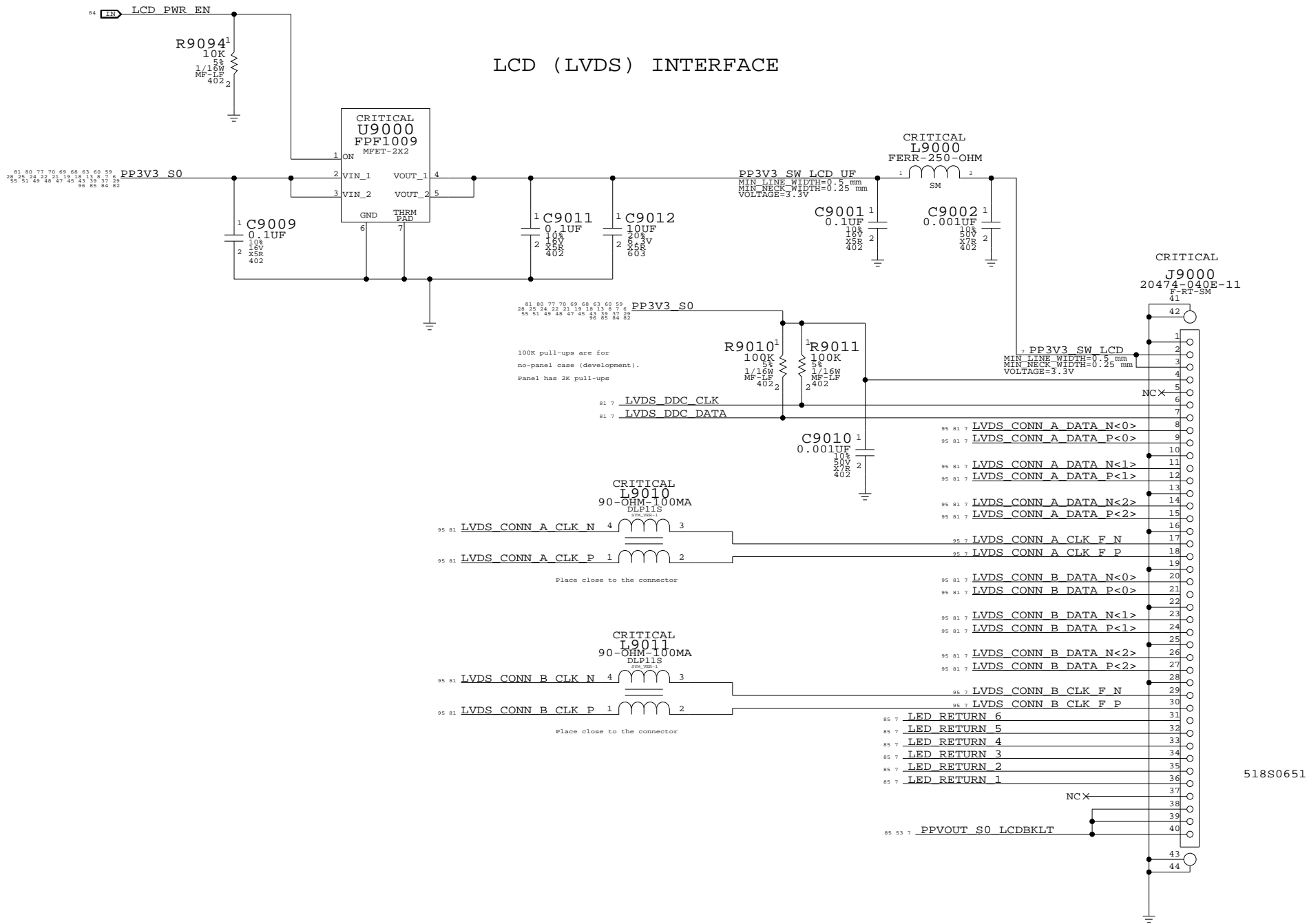
DP EG ML N<1>

DP EG ML P<2>

DP EG ML N<2>

DP EG ML P<3>





LVDS Display Connector

SYNC_MASTER=D0R SYNC_DATE=12/19/2008


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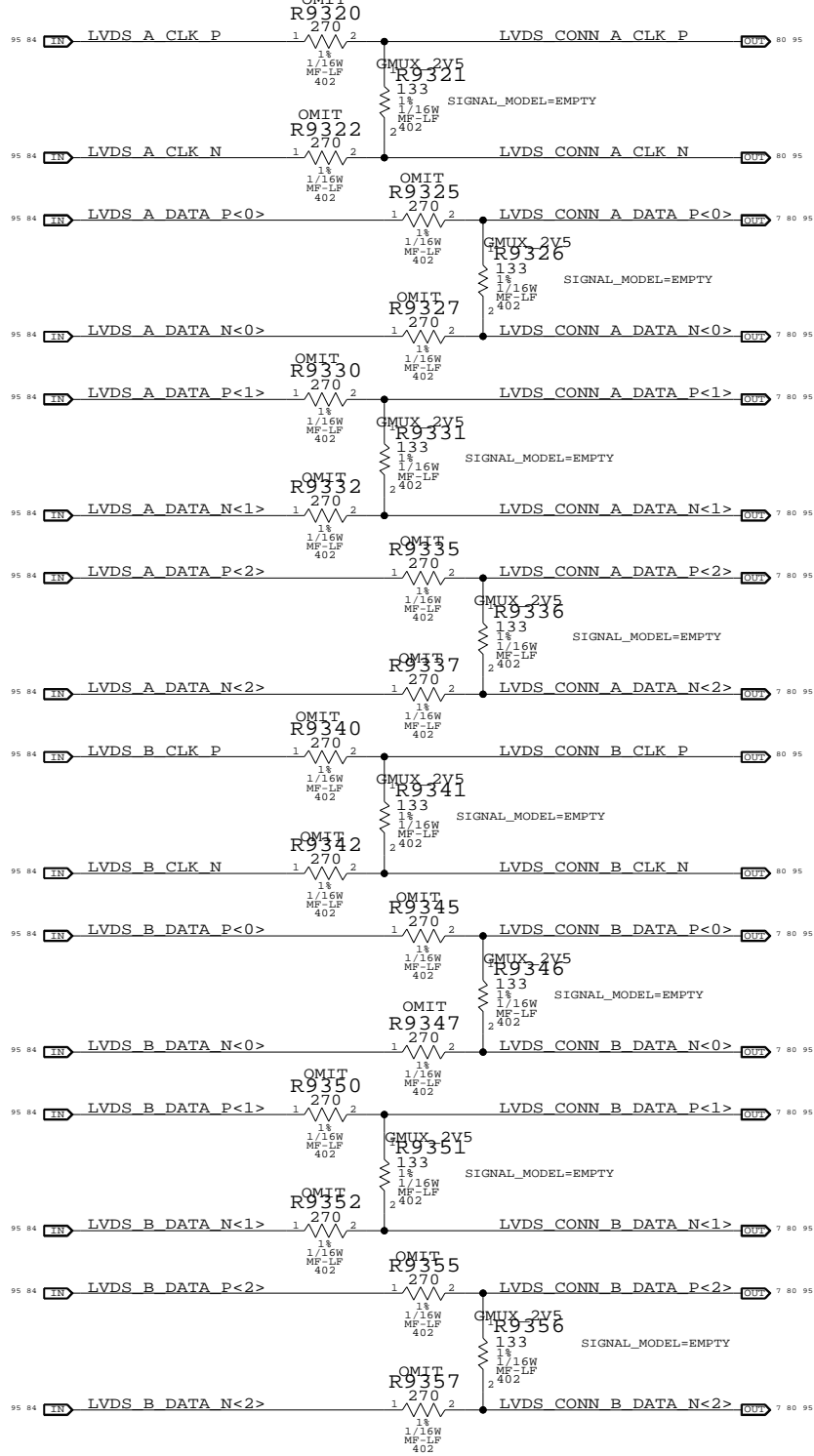
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 APPLE INC.	SIZE D	DRAWING NUMBER 051-7892	REV. A.0.0
	SCALE NONE	SHT 80	OF 97

LVDS Transmitter Termination

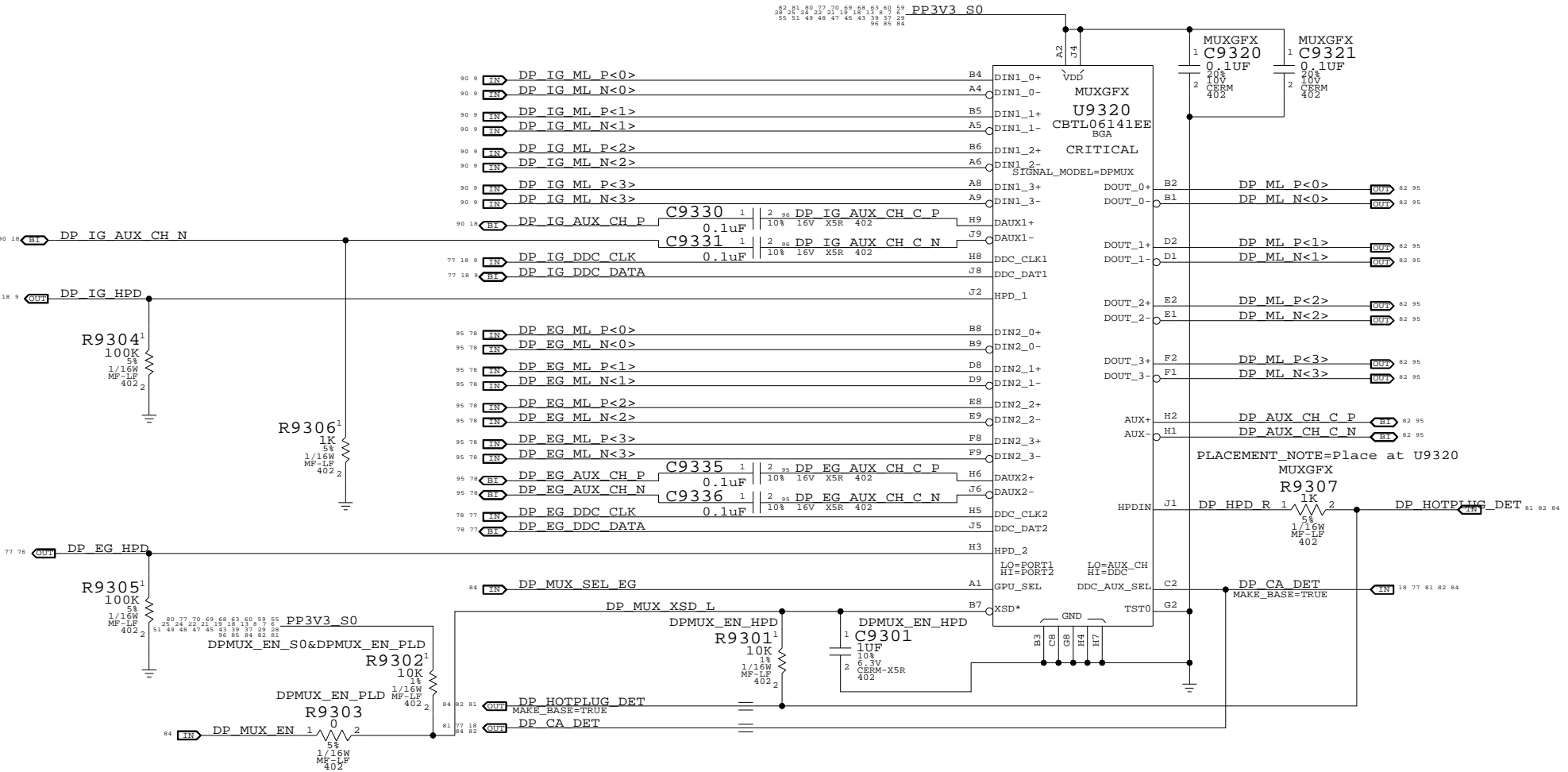
All emulated LVDS outputs require this termination

PLACEMENT NOTE=Place at U9600 (All 24 resistors)

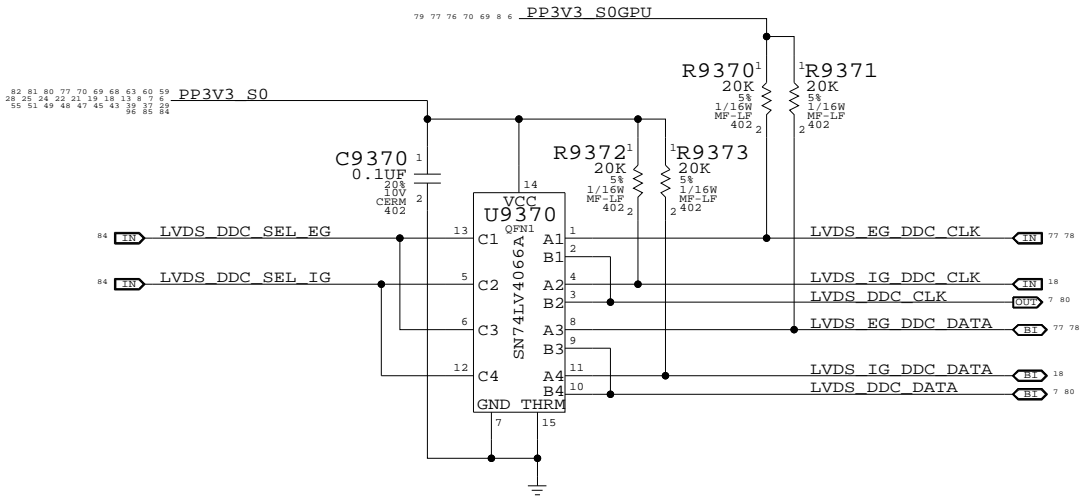


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0517	16	RES,MTL FILM,270 OHM,1%,1/16W,0402,500,LF	R9320,R9321,R9322,R9325,R9326,R9327,R9330,R9331,R9332,R9335,R9336,R9337,R9340,R9341,R9342,R9345,R9346,R9347,R9350,R9351,R9352,R9355,R9356,R9357		GMUX_2V5
114S0174	16	RES,MTL FILM,1/16W,357 OHM,1%,0402,500,LF	R9320,R9321,R9322,R9325,R9326,R9327,R9330,R9331,R9332,R9335,R9336,R9337,R9340,R9341,R9342,R9345,R9346,R9347,R9350,R9351,R9352,R9355,R9356,R9357		GMUX_1V8

DisplayPort Mux



LVDS DDC MUX

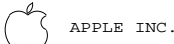


Muxed Graphics Support

SYNC_MASTER=AMASON_M98_MLB SYNC_DATE=12/05/2008

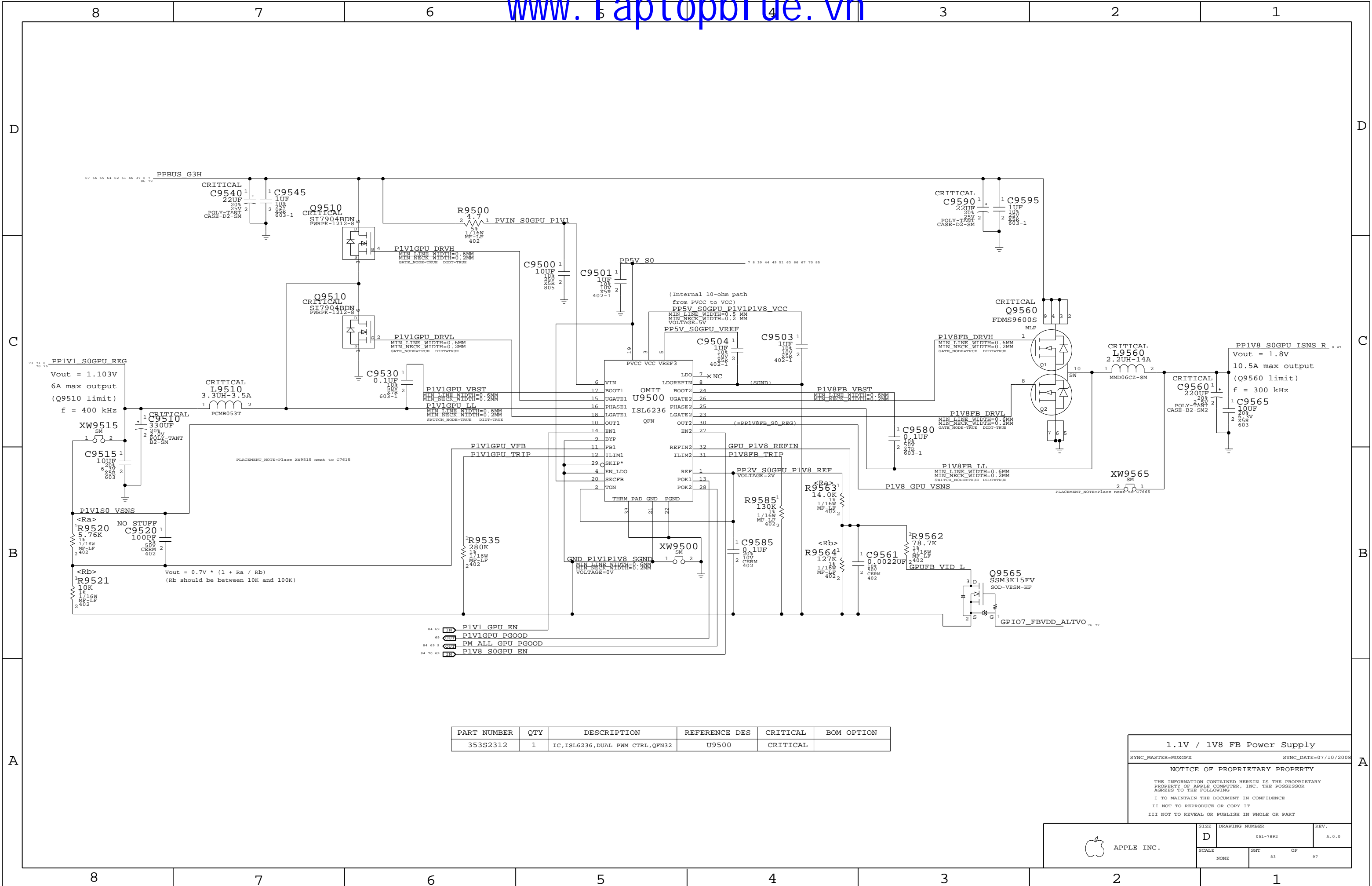
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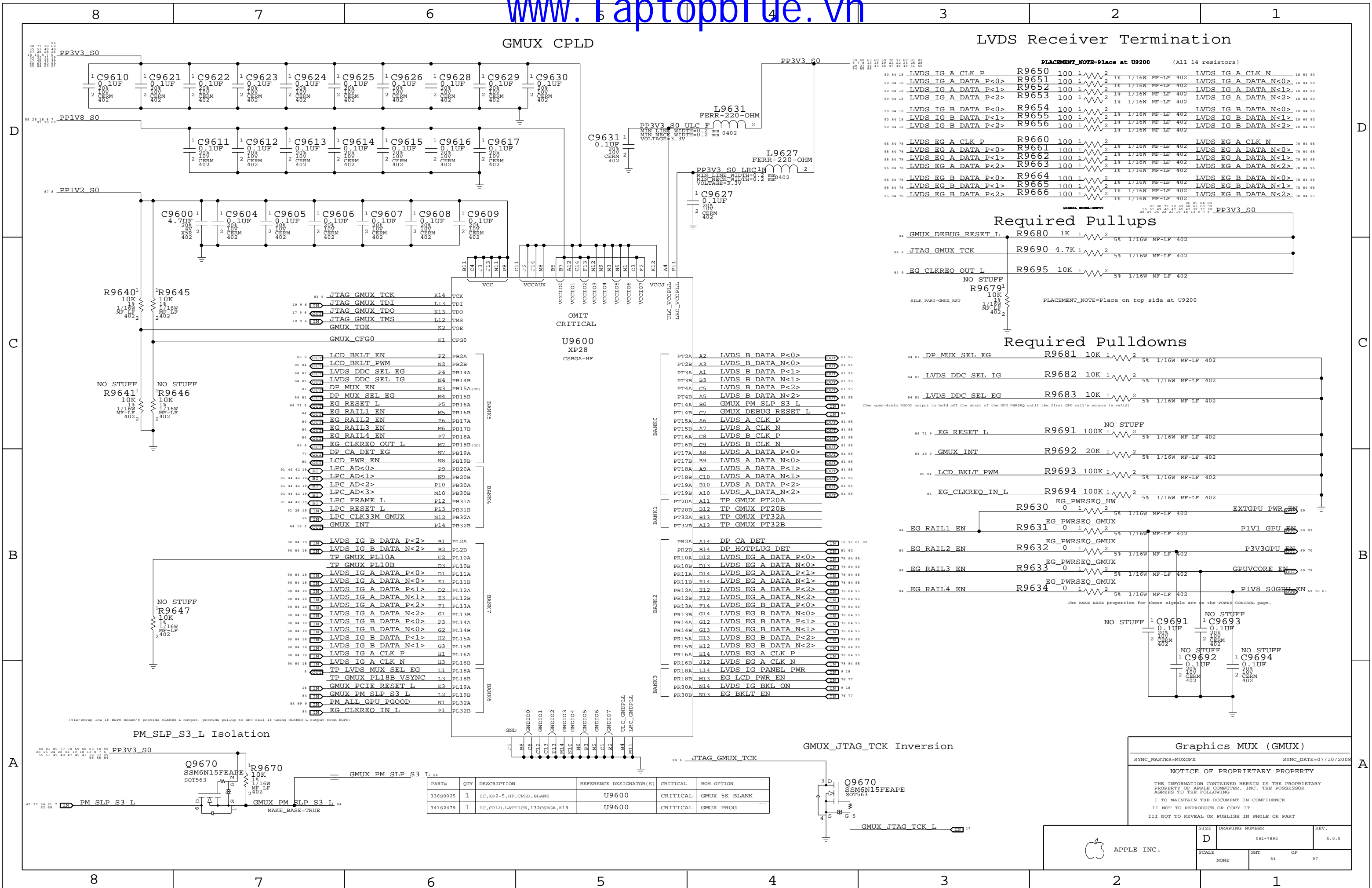
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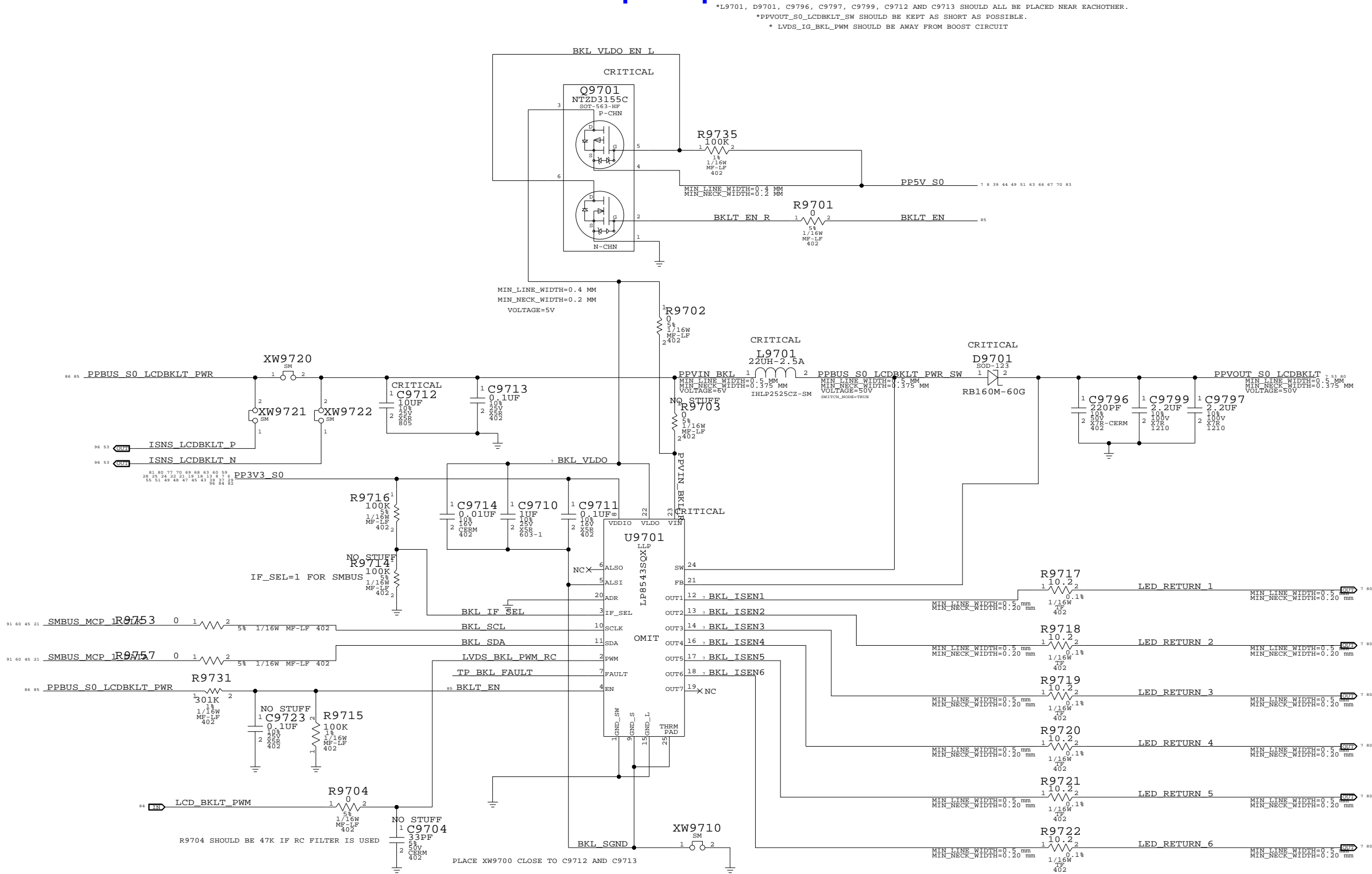


APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE	SHT	OF
NONE	81	97







PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S2670	1	IC,LP8543,WHT LED BKLT,PROD	U9701	CRITICAL	

LCD BACKLIGHT DRIVER

SYNC_MASTER=DDR

SYNC_DATE=12/12/2008

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APPLE INC.

SIZE

D

DRAWING NUMBER

051-7892

REV.

A.0.0

SCALE

NONE

SHT

85

OF

97

D

C

B

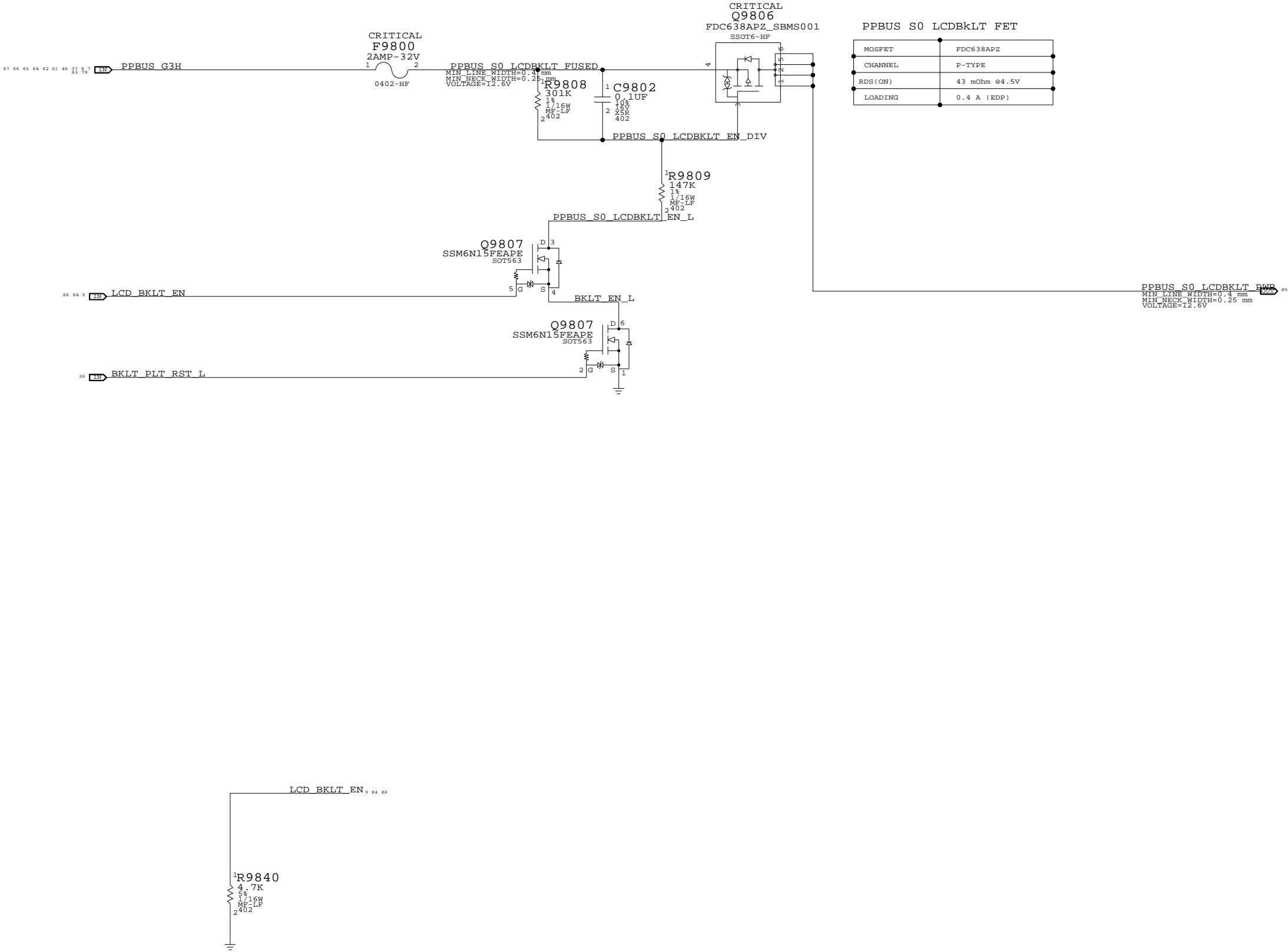
A

D

C

B

A



LCD Backlight Support

SYNC_MASTER=VITE_M98_MLSSYNC_DATE=07/02/2008

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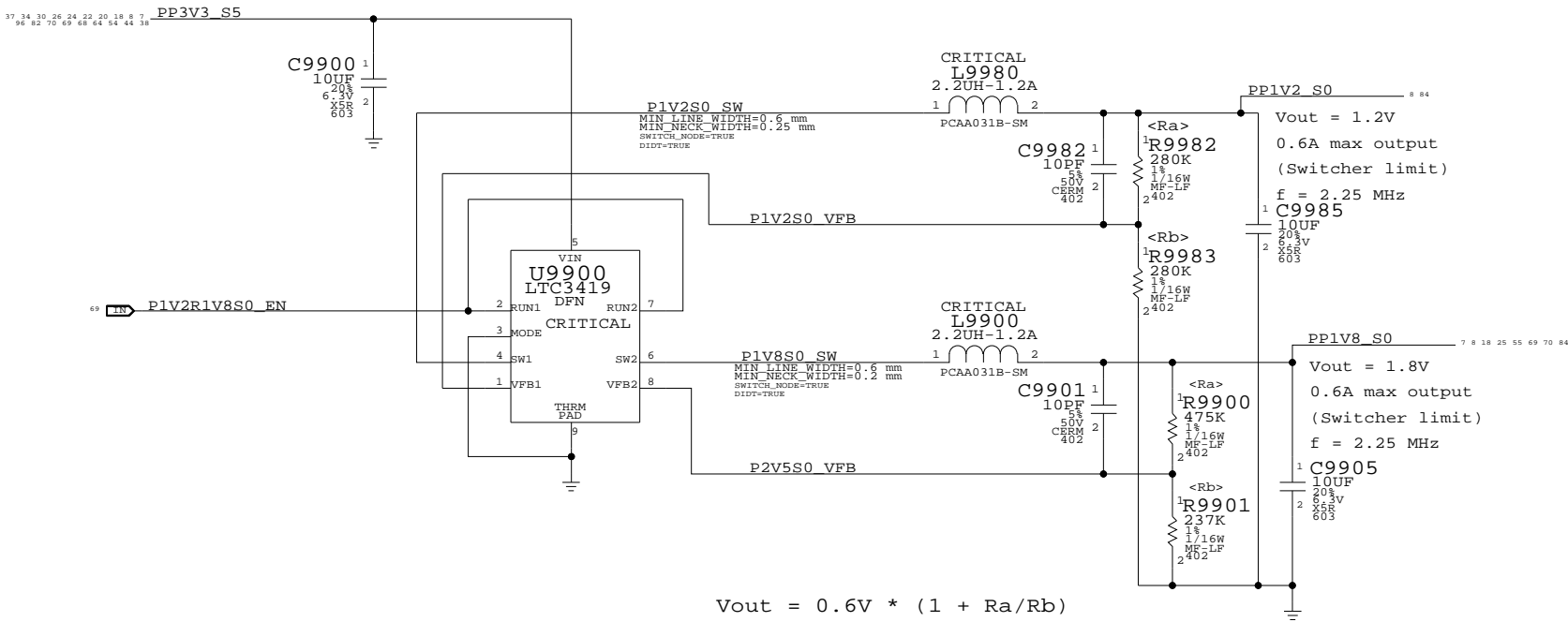
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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE	SHT	OF
NONE	86	97

1.8V/1.2V S0 SWITCHER



Misc Power Supplies

SYNC_MASTER=MUXGFX SYNC_DATE=02/01/2008

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7892	A.0.0
SCALE		SHT	OF
NONE		87	97

87654321

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR2:

DQ signals should be matched within 20 ps of associated DQS pair.

DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.

All DQS pairs should be matched within 100 ps of clocks.

CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.

A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.

All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).

DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:

DQ signals should be matched within 5 ps of associated DQS pair.

DQS intra-pair matching should be within 1 ps, inter-pair matching should be within 180 ps

No DQS to clock matching requirement.

CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.

A/BA/cmd signals should be matched within 5 ps of CLK pairs.

All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).

DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	7 MIL	7 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM A CLK P<5..0>	15 28
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM A CLK N<5..0>	15 28
MEM_A_CNTRL	MEM_40S_VDD	MEM_CTRL	MEM A CKE<3..0>	15 28
MEM_A_CNTRL	MEM_40S_VDD	MEM_CTRL	MEM A CS_L<3..0>	15 28
MEM_A_CNTRL	MEM_40S_VDD	MEM_CTRL	MEM A ODT<3..0>	15 28
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A A<14..0>	15 28
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A BA<2..0>	15 28
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A RAS_L	15 28
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A CAS_L	15 28
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A WE_L	15 28
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM A DQ<7..0>	15 28
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM A DQ<15..8>	15 28
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM A DQ<23..16>	15 28
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM A DQ<31..24>	15 28
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM A DQ<39..32>	15 28
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM A DQ<47..40>	15 28
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM A DQ<55..48>	15 28
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM A DQ<63..56>	15 28
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM A DM<0>	15 28
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM A DM<1>	15 28
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM A DM<2>	15 28
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM A DM<3>	15 28
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM A DM<4>	15 28
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM A DM<5>	15 28
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM A DM<6>	15 28
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM A DM<7>	15 28
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM A DQS P<0>	15 28
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM A DQS N<0>	15 28
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM A DQS P<1>	15 28
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM A DQS N<1>	15 28
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM A DQS P<2>	15 28
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM A DQS N<2>	15 28
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM A DQS P<3>	15 28
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM A DQS N<3>	15 28
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM A DQS P<4>	15 28
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM A DQS N<4>	15 28
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM A DQS P<5>	15 28
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM A DQS N<5>	15 28
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM A DQS P<6>	15 28
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM A DQS N<6>	15 28
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM A DQS P<7>	15 28
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM A DQS N<7>	15 28
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM B CLK P<5..0>	15 29
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM B CLK N<5..0>	15 29
MEM_B_CNTRL	MEM_40S_VDD	MEM_CTRL	MEM B CKE<3..0>	15 29
MEM_B_CNTRL	MEM_40S_VDD	MEM_CTRL	MEM B CS_L<3..0>	15 29
MEM_B_CNTRL	MEM_40S_VDD	MEM_CTRL	MEM B ODT<3..0>	15 29
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B A<14..0>	15 29
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B BA<2..0>	15 29
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B RAS_L	15 29
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B CAS_L	15 29
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B WE_L	15 29
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM B DQ<7..0>	15 29
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM B DQ<15..8>	15 29
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM B DQ<23..16>	15 29
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM B DQ<31..24>	15 29
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM B DQ<39..32>	15 29
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM B DQ<47..40>	15 29
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM B DQ<55..48>	15 29
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM B DQ<63..56>	15 29
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM B DM<0>	15 29
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM B DM<1>	15 29
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM B DM<2>	15 29
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM B DM<3>	15 29
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM B DM<4>	15 29
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM B DM<5>	15 29
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM B DM<6>	15 29
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM B DM<7>	15 29
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM B DQS P<0>	15 29
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM B DQS N<0>	15 29
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM B DQS P<1>	15 29
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM B DQS N<1>	15 29
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM B DQS P<2>	15 29
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM B DQS N<2>	15 29
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM B DQS P<3>	15 29
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM B DQS N<3>	15 29
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM B DQS P<4>	15 29
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM B DQS N<4>	15 29
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM B DQS P<5>	15 29
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM B DQS N<5>	15 29
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM B DQS P<6>	15 29
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM B DQS N<6>	15 29
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM B DQS P<7>	15 29
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM B DQS N<7>	15 29
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP VDD	16
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP GND	16

Memory Constraints

SYNC_MASTER=MUXGFX

SYNC_DATE=02/18/2008

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PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?	USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

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ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
MCP_DEBUG	PCI_55S	PCI	MCP_DEBUG<7..0> 13 19
PCI_AD	PCI_55S	PCI	PCI_AD<23..8>
PCI_AD24	PCI_55S	PCI	PCI_AD<24>
PCI_AD	PCI_55S	PCI	PCI_AD<31..25>
PCI_AD	PCI_55S	PCI	PCI_PAR
PCI_C_BE_L	PCI_55S	PCI	PCI_C_BE_L<3..0>
PCI_CNTL	PCI_55S	PCI	PCI_IRDY_L
PCI_CNTL	PCI_55S	PCI	PCI_DEVSEL_L
PCI_CNTL	PCI_55S	PCI	PCI_PERR_L
PCI_CNTL	PCI_55S	PCI	PCI_SERR_L
PCI_CNTL	PCI_55S	PCI	PCI_STOP_L
PCI_CNTL	PCI_55S	PCI	PCI_TRDY_L
PCI_CNTL	PCI_55S	PCI	PCI_FRAME_L
PCI_REQ0_L	PCI_55S	PCI	PCI_REQ0_L 19
PCI_GNT0_L	PCI_55S	PCI	PCI_GNT0_L
PCI_REQ1_L	PCI_55S	PCI	PCI_REQ1_L 19
PCI_GNT1_L	PCI_55S	PCI	PCI_GNT1_L
PCI_INTW_L	PCI_55S	PCI	PCI_INTW_L
PCI_INTX_L	PCI_55S	PCI	PCI_INTX_L
PCI_INTY_L	PCI_55S	PCI	PCI_INTY_L
PCI_INTZ_L	PCI_55S	PCI	PCI_INTZ_L
MCP_PCI_CLK2	CLK_PCI_55S	CLK_PCI	PCI_CLK33M MCP_R 19
	CLK_PCI_55S	CLK_PCI	PCI_CLK33M MCP 19
LPC_AD	LPC_55S	LPC	LPC_AD<3..0> 19 42 44 84
LPC_FRAME_L	LPC_55S	LPC	LPC_FRAME_L 19 42 44 84
LPC_RESET_L	LPC_55S	LPC	LPC_RESET_L 19 26 84
MCP_LPC_CLK0	CLK_LPC_55S	CLK_LPC	LPC_CLK33M SMC_R 19 26
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M SMC 26 42
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M LPCPLUS 26 44
USB_EXTN_P	USB_90D	USB	USB_EXTN_P 20 40
USB_EXTN_N	USB_90D	USB	USB_EXTN_N 20 40
USB_EXTN_MUXED_P	USB_90D	USB	USB_EXTN_MUXED_P
USB_EXTN_MUXED_N	USB_90D	USB	USB_EXTN_MUXED_N
NC_USB_MINIP	USB_90D	USB	NC_USB_MINIP 9 20
NC_USB_MININ	USB_90D	USB	NC_USB_MININ 9 20
NC_USB_EXTDP	USB_90D	USB	NC_USB_EXTDP 9 20
NC_USB_EXTDN	USB_90D	USB	NC_USB_EXTDN 9 20
USB_CAMERA_P	USB_90D	USB	USB_CAMERA_P 7 20 31
USB_CAMERA_N	USB_90D	USB	USB_CAMERA_N 7 20 31
USB_BT_P	USB_90D	USB	USB_BT_P 7 20 31
USB_BT_N	USB_90D	USB	USB_BT_N 7 20 31
USB_TPAD_P	USB_90D	USB	USB_TPAD_P 20 50
USB_TPAD_N	USB_90D	USB	USB_TPAD_N 20 50
USB_IR_P	USB_90D	USB	USB_IR_P 20 41
USB_IR_N	USB_90D	USB	USB_IR_N 20 41
USB_EXTB_P	USB_90D	USB	USB_EXTB_P 20 40
USB_EXTB_N	USB_90D	USB	USB_EXTB_N 20 40
NC_USB_EXCARDP	USB_90D	USB	NC_USB_EXCARDP 9 20
NC_USB_EXCARDN	USB_90D	USB	NC_USB_EXCARDN 9 20
NC_USB_EXTCP	USB_90D	USB	NC_USB_EXTCP 9 20
NC_USB_EXTCN	USB_90D	USB	NC_USB_EXTCN 9 20
MCP_USB_RBIAS	MCP_USB_RBIAS		MCP_USB_RBIAS_GND 20
SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS_MCP_0_CLK 13 21 28 29 45
SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS_MCP_0_DATA 13 21 28 29 45
SMBUS_MCP_1_CLK	SMB_55S	SMB	SMBUS_MCP_1_CLK 21 45 60 85
SMBUS_MCP_1_DATA	SMB_55S	SMB	SMBUS_MCP_1_DATA 21 45 60 85
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK 21 55
HDA_BIT_CLK_R	HDA_55S	HDA	HDA_BIT_CLK_R 21
HDA_SYNC	HDA_55S	HDA	HDA_SYNC 21 55
HDA_RST_L	HDA_55S	HDA	HDA_RST_R_L 21
HDA_RST_L	HDA_55S	HDA	HDA_RST_L 21 55
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0 21 55
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN_CODEC 21 55
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT 21 55
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT_R 21
MCP_HDA_PULLDN_COMP	MCP_HDA_COMP		MCP_HDA_PULLDN_COMP 21
PM_CLK32K_SUSCLK_R	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK_R 21 26
PM_CLK32K_SUSCLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK 26 42
SPI_CLK_R	SPI_55S	SPI	SPI_CLK_R 21 44
SPI_CLK	SPI_55S	SPI	SPI_CLK 54
SPI_MOSI_R	SPI_55S	SPI	SPI_MOSI_R 21 44
SPI_MOSI	SPI_55S	SPI	SPI_MOSI 54
SPI_MISO	SPI_55S	SPI	SPI_MISO 21 44
SPI_MISO_R	SPI_55S	SPI	SPI_MISO_R 54
SPI_CS0_R_L	SPI_55S	SPI	SPI_CS0_R_L 21 44
SPI_CS0_L	SPI_55S	SPI	SPI_CS0_L

MCP Constraints 2

SYNC_MASTER=MUXGFX SYNC_DATE=02/18/2008

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MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?






















SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
 MCP_MII_COMP	MCP_MII_COMP		MCP MII COMP VDD	16
 MCP_MII_COMP	MCP_MII_COMP		MCP MII COMP GND	16
 MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0_R	16 34
 MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	RTL8211 CLK25M CKXTAL1	33 34
 ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET_INTR_L	
 ENET_MDIO	ENET_MII_55S	ENET_MII	ENET MDIO	16 33
 ENET_MDC	ENET_MII_55S	ENET_MII	ENET MDC	16 33
 ENET_PWRDWN_L	ENET_MII_55S	ENET_MII	ENET_PWRDWN_L	
 ENET_CLK125M_RXCLK_R	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R	33
 ENET_CLK125M_RXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK	16 33
 ENET_RXD<3..0>	ENET_MII_55S	ENET_MII	ENET_RXD R<3..0>	33
 ENET_RXD<0>	ENET_MII_55S	ENET_MII	ENET_RXD<0>	16 33
 ENET_RXD<3..1>	ENET_MII_55S	ENET_MII	ENET_RXD<3..1>	16 33
 ENET_RX_CTRL	ENET_MII_55S	ENET_MII	ENET_RX_CTRL	16 33
 ENET_CLK125M_TXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK	16 33
 ENET_TXD<0>	ENET_MII_55S	ENET_MII	ENET_TXD<0>	16 33
 ENET_TXD<3..1>	ENET_MII_55S	ENET_MII	ENET_TXD<3..1>	16 33
 ENET_TX_CTRL	ENET_MII_55S	ENET_MII	ENET_TX_CTRL	16 33
 ENET_RESET_L	ENET_MII_55S	ENET_MII	ENET_RESET_L	16 33
 ENET_MDI P<3..0>	ENET_MDI_100D	ENET_MDI	ENET MDI P<3..0>	33 36
 ENET_MDI N<3..0>	ENET_MDI_100D	ENET_MDI	ENET MDI N<3..0>	33 36

Ethernet Constraints

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FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF









SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

SD CARD INTERFACE CONSTRAINTS











PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD_INTERFACE	*	=3X_DIELECTRIC	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
 FW_P0_TPA	FW_110D	FW_TP	NC FW0 TPAP	36 38
 FW_P0_TPB	FW_110D	FW_TP	NC FW0 TPAN	36 38
 FW_P0_TPB	FW_110D	FW_TP	NC FW0 TPBP	36 38
 FW_P1_TPA	FW_110D	FW_TP	NC FW0 TPBN	36 38
 FW_P1_TPB	FW_110D	FW_TP	FW PORT1 TPA P	36 38
 FW_P1_TPB	FW_110D	FW_TP	FW PORT1 TPA N	36 38
 FW_P1_TPB	FW_110D	FW_TP	FW PORT1 TPB P	36 38
 FW_P1_TPB	FW_110D	FW_TP	FW PORT1 TPB N	36 38
Port 2 Not Used				

SD CARD NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
 SD_DATA	SD_55S	SD_INTERFACE	SD_D<0>	7 32
 SD_DATA	SD_55S	SD_INTERFACE	SD_D<1>	7 32
 SD_DATA	SD_55S	SD_INTERFACE	SD_D<2>	7 32
 SD_DATA	SD_55S	SD_INTERFACE	SD_D<3>	7 32
 SD_DATA	SD_55S	SD_INTERFACE	SD_D<4>	7 32
 SD_DATA	SD_55S	SD_INTERFACE	SD_D<5>	7 32
 SD_DATA	SD_55S	SD_INTERFACE	SD_D<6>	7 32
 SD_DATA	SD_55S	SD_INTERFACE	SD_D<7>	7 32
 SD_CLK	SD_55S	SD_INTERFACE	SD_CLK	7 32
 SD_CMD	SD_55S	SD_INTERFACE	SD_CMD	7 32

FireWire Constraints

SYNC_MASTER=MUXGFX SYNC_DATE=02/18/2008

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APPLE INC.

SIZE
D

DRAWING NUMBER
051-7892

REV.

A.0.0

SCALE

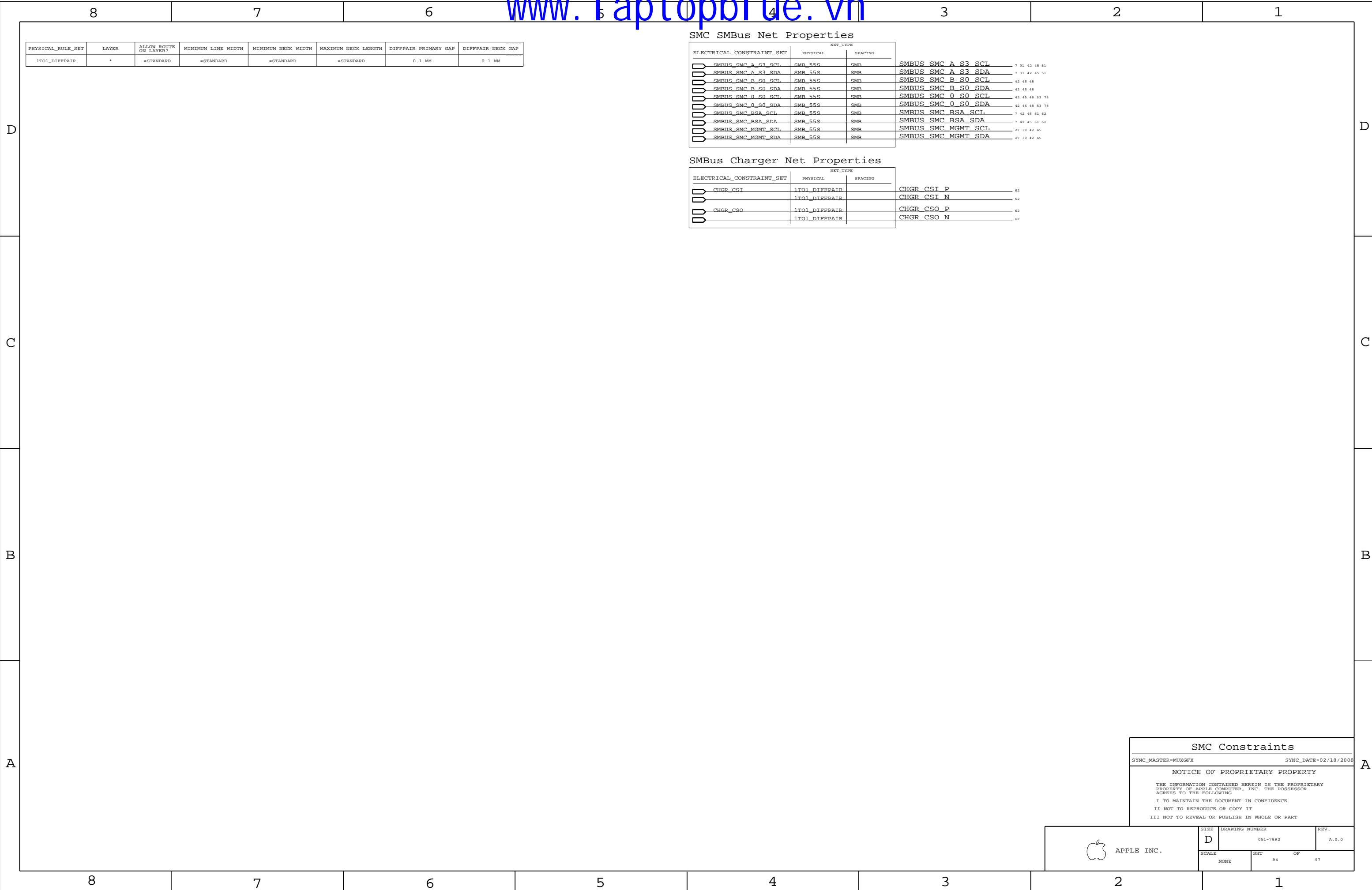
NONE

SHT

93

OF

97



8

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1



APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE	SHT	OF
NONE	94	97

GDDR3 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR3_40R55SE	*	=45_OHM_SE	=40_OHM_SE	0.095 MM	12.7 MM	=STANDARD	=STANDARD
GDDR3_40SE	*	=45_OHM_SE	=40_OHM_SE	0.095 MM	=40_OHM_SE	=STANDARD	=STANDARD
GDDR3_80D	*	=40_OHM_DIFF	=40_OHM_DIFF	0.095 MM	=40_OHM_DIFF	=40_OHM_DIFF	=40_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR3_CLK	*	=2.5:1:1_SPACING	?
GDDR3_CMD	*	=2.5:1:1_SPACING	?
GDDR3_DATA	*	=2.5:1:1_SPACING	?
GDDR3_DQS	*	=2.5:1:1_SPACING	?

From T18 MXM:

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?	DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?	LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDs intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDs traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

MUXGFX Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_P
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_N
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_P<2..0>
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_N<2..0>
LVDS_B_CLK	LVDS_100D	LVDS	LVDS_B_CLK_P
LVDS_B_CLK	LVDS_100D	LVDS	LVDS_B_CLK_N
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_P<2..0>
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_N<2..0>
LVDS_CONN_A_CLK_F_P	LVDS_100D	LVDS	LVDS_CONN_A_CLK_F_P
LVDS_CONN_A_CLK_F_N	LVDS_100D	LVDS	LVDS_CONN_A_CLK_F_N
LVDS_CONN_B_CLK_F_P	LVDS_100D	LVDS	LVDS_CONN_B_CLK_F_P
LVDS_CONN_B_CLK_F_N	LVDS_100D	LVDS	LVDS_CONN_B_CLK_F_N
LVDS_CONN_A_CLK_P	LVDS_100D	LVDS	LVDS_CONN_A_CLK_P
LVDS_CONN_A_CLK_N	LVDS_100D	LVDS	LVDS_CONN_A_CLK_N
LVDS_CONN_A_DATA_P<2..0>	LVDS_100D	LVDS	LVDS_CONN_A_DATA_P<2..0>
LVDS_CONN_A_DATA_N<2..0>	LVDS_100D	LVDS	LVDS_CONN_A_DATA_N<2..0>
LVDS_CONN_B_CLK_P	LVDS_100D	LVDS	LVDS_CONN_B_CLK_P
LVDS_CONN_B_CLK_N	LVDS_100D	LVDS	LVDS_CONN_B_CLK_N
LVDS_CONN_B_DATA_P<2..0>	LVDS_100D	LVDS	LVDS_CONN_B_DATA_P<2..0>
LVDS_CONN_B_DATA_N<2..0>	LVDS_100D	LVDS	LVDS_CONN_B_DATA_N<2..0>
DP_ML	DP_100D	DISPLAYPORT	DP_ML_C_P<3..0>
DP_ML	DP_100D	DISPLAYPORT	DP_ML_C_N<3..0>
DP_ML	DP_100D	DISPLAYPORT	DP_ML_CONN_P<3..0>
DP_ML	DP_100D	DISPLAYPORT	DP_ML_CONN_N<3..0>
DP_ML	DP_100D	DISPLAYPORT	DP_ML_CONN_P<3..0>
DP_ML	DP_100D	DISPLAYPORT	DP_ML_CONN_N<3..0>
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_AUX_CH_C_P
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_AUX_CH_C_N

GDDR3 FB A/B Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
FB_A_CLK_P	GDDR3_80D	GDDR3_CLK	FB A CLK_P<0>
FB_A_CLK_P	GDDR3_80D	GDDR3_CLK	FB A CLK_N<0>
FB_B_CLK_P	GDDR3_80D	GDDR3_CLK	FB A CLK_P<1>
FB_B_CLK_P	GDDR3_80D	GDDR3_CLK	FB A CLK_N<1>
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB A MA<1..0>
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB A MA<12..6>
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB A BA<2..0>
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB A RAS_L
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB A CAS_L
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB A WE_L
FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB A UCKE
FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB A LCKE
FB_AB_CS0	GDDR3_40R55SE	GDDR3_CMD	FB A LCS0_L
FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB A DRAM_RST
FB_A_CMD	GDDR3_40SE	GDDR3_CMD	FB A LMA<5..2>
FB_B_CMD	GDDR3_40SE	GDDR3_CMD	FB A UMA<5..2>
FB_A_WDQS0	GDDR3_40SE	GDDR3_DQS	FB A WDQS<0>
FB_A_WDQS1	GDDR3_40SE	GDDR3_DQS	FB A WDQS<1>
FB_A_WDQS2	GDDR3_40SE	GDDR3_DQS	FB A WDQS<2>
FB_A_WDQS3	GDDR3_40SE	GDDR3_DQS	FB A WDQS<3>
FB_A_RDQS0	GDDR3_40SE	GDDR3_DQS	FB A RDQS<0>
FB_A_RDQS1	GDDR3_40SE	GDDR3_DQS	FB A RDQS<1>
FB_A_RDQS2	GDDR3_40SE	GDDR3_DQS	FB A RDQS<2>
FB_A_RDQS3	GDDR3_40SE	GDDR3_DQS	FB A RDQS<3>
FB_A_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB A DQ<7..0>
FB_A_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB A DQ<15..8>
FB_A_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB A DQ<23..16>
FB_A_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB A DQ<31..24>
FB_A_DQM0	GDDR3_40SE	GDDR3_DATA	FB A DQM_L<0>
FB_A_DQM1	GDDR3_40SE	GDDR3_DATA	FB A DQM_L<1>
FB_A_DQM2	GDDR3_40SE	GDDR3_DATA	FB A DQM_L<2>
FB_A_DQM3	GDDR3_40SE	GDDR3_DATA	FB A DQM_L<3>
FB_B_WDQS0	GDDR3_40SE	GDDR3_DQS	FB A WDQS<4>
FB_B_WDQS1	GDDR3_40SE	GDDR3_DQS	FB A WDQS<5>
FB_B_WDQS2	GDDR3_40SE	GDDR3_DQS	FB A WDQS<6>
FB_B_WDQS3	GDDR3_40SE	GDDR3_DQS	FB A WDQS<7>
FB_B_RDQS0	GDDR3_40SE	GDDR3_DQS	FB A RDQS<4>
FB_B_RDQS1	GDDR3_40SE	GDDR3_DQS	FB A RDQS<5>
FB_B_RDQS2	GDDR3_40SE	GDDR3_DQS	FB A RDQS<6>
FB_B_RDQS3	GDDR3_40SE	GDDR3_DQS	FB A RDQS<7>
FB_B_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB A DQ<39..32>
FB_B_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB A DQ<47..40>
FB_B_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB A DQ<55..48>
FB_B_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB A DQ<63..56>
FB_B_DQM0	GDDR3_40SE	GDDR3_DATA	FB A DOM_L<4>
FB_B_DQM1	GDDR3_40SE	GDDR3_DATA	FB A DOM_L<5>
FB_B_DQM2	GDDR3_40SE	GDDR3_DATA	FB A DOM_L<6>
FB_B_DQM3	GDDR3_40SE	GDDR3_DATA	FB A DOM_L<7>

G96 Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
GPU_CLK27M	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M
GPU_CLK27M_SS	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M_SS
LVDS_EG_A_CLK_P	LVDS_100D	LVDS	LVDS_EG_A_CLK_P
LVDS_EG_A_CLK_N	LVDS_100D	LVDS	LVDS_EG_A_CLK_N
LVDS_EG_A_DATA_P<2..0>	LVDS_100D	LVDS	LVDS_EG_A_DATA_P<2..0>
LVDS_EG_A_DATA_N<2..0>	LVDS_100D	LVDS	LVDS_EG_A_DATA_N<2..0>
LVDS_EG_B_DATA_P<2..0>	LVDS_100D	LVDS	LVDS_EG_B_DATA_P<2..0>
LVDS_EG_B_DATA_N<2..0>	LVDS_100D	LVDS	LVDS_EG_B_DATA_N<2..0>
DP_ML	DP_100D	DISPLAYPORT	DP_EG_ML_P<3..0>
DP_ML	DP_100D	DISPLAYPORT	DP_EG_ML_N<3..0>
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_EG_AUX_CH_P
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_EG_AUX_CH_N
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_EG_AUX_CH_C_P
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_EG_AUX_CH_C_N

GDDR3 FB C/D Net Properties

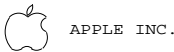
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
FB_C_CLK_P	GDDR3_80D	GDDR3_CLK	FB B CLK_P<0>
FB_C_CLK_P	GDDR3_80D	GDDR3_CLK	FB B CLK_N<0>
FB_D_CLK_P	GDDR3_80D	GDDR3_CLK	FB B CLK_P<1>
FB_D_CLK_P	GDDR3_80D	GDDR3_CLK	FB B CLK_N<1>
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB B MA<1..0>
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB B MA<12..6>
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB B BA<2..0>
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB B RAS_L
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB B CAS_L
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB B WE_L
FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB B UCKE
FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB B LCKE
FB_CD_CS0	GDDR3_40R55SE	GDDR3_CMD	FB B LCS0_L
FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB B DRAM_RST
FB_C_CMD	GDDR3_40SE	GDDR3_CMD	FB B LMA<5..2>
FB_D_CMD	GDDR3_40SE	GDDR3_CMD	FB B UMA<5..2>
FB_C_WDQS0	GDDR3_40SE	GDDR3_DQS	FB B WDQS<0>
FB_C_WDQS1	GDDR3_40SE	GDDR3_DQS	FB B WDQS<1>
FB_C_WDQS2	GDDR3_40SE	GDDR3_DQS	FB B WDQS<2>
FB_C_WDQS3	GDDR3_40SE	GDDR3_DQS	FB B WDQS<3>
FB_C_RDQS0	GDDR3_40SE	GDDR3_DQS	FB B RDQS<0>
FB_C_RDQS1	GDDR3_40SE	GDDR3_DQS	FB B RDQS<1>
FB_C_RDQS2	GDDR3_40SE	GDDR3_DQS	FB B RDQS<2>
FB_C_RDQS3	GDDR3_40SE	GDDR3_DQS	FB B RDQS<3>
FB_C_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB B DQ<7..0>
FB_C_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB B DQ<15..8>
FB_C_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB B DQ<23..16>
FB_C_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB B DQ<31..24>
FB_C_DQM0	GDDR3_40SE	GDDR3_DATA	FB B DQM_L<0>
FB_C_DQM1	GDDR3_40SE	GDDR3_DATA	FB B DQM_L<1>
FB_C_DQM2	GDDR3_40SE	GDDR3_DATA	FB B DQM_L<2>
FB_C_DQM3	GDDR3_40SE	GDDR3_DATA	FB B DQM_L<3>
FB_D_WDQS0	GDDR3_40SE	GDDR3_DQS	FB B WDQS<4>
FB_D_WDQS1	GDDR3_40SE	GDDR3_DQS	FB B WDQS<5>
FB_D_WDQS2	GDDR3_40SE	GDDR3_DQS	FB B WDQS<6>
FB_D_WDQS3	GDDR3_40SE	GDDR3_DQS	FB B WDQS<7>
FB_D_RDQS0	GDDR3_40SE	GDDR3_DQS	FB B RDQS<4>
FB_D_RDQS1	GDDR3_40SE	GDDR3_DQS	FB B RDQS<5>
FB_D_RDQS2	GDDR3_40SE	GDDR3_DQS	FB B RDQS<6>
FB_D_RDQS3	GDDR3_40SE	GDDR3_DQS	FB B RDQS<7>
FB_D_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB B DQ<39..32>
FB_D_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB B DQ<47..40>
FB_D_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB B DQ<55..48>
FB_D_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB B DQ<63..56>
FB_D_DQM0	GDDR3_40SE	GDDR3_DATA	FB B DOM_L<4>
FB_D_DQM1	GDDR3_40SE	GDDR3_DATA	FB B DOM_L<5>
FB_D_DQM2	GDDR3_40SE	GDDR3_DATA	FB B DOM_L<6>
FB_D_DQM3	GDDR3_40SE	GDDR3_DATA	FB B DOM_L<7>

GPU (G96) CONSTRAINTS

SYNC_MASTER=MUXGFX SYNC_DATE=02/18/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE	SHT	OF
NONE	95	97

DCB

A

5D

8		7		6		5		4		3		2		1	
K19 Board-Specific Spacing & Physical Constraints															
BOARD LAYERS						BOARD AREAS			BOARD UNITS (MIL OR MM)		ALLEGRO VERSION				
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM						NO_TYPE, BGA, PGA			MM		15.5.1				
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH		MINIMUM NECK WIDTH		MAXIMUM NECK LENGTH		DIFFPAIR PRIMARY GAP		DIFFPAIR NECK GAP			
DEFAULT		*	Y	~50_OHM_SE		~50_OHM_SE		33.6 MM		0 MM		0 MM			
STANDARD		*	Y	~DEFAULT		~DEFAULT		10 MM		~DEFAULT		~DEFAULT			
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH		MINIMUM NECK WIDTH		MAXIMUM NECK LENGTH		DIFFPAIR PRIMARY GAP		DIFFPAIR NECK GAP			
55_OHM_SE		TOP, BOTTOM	Y	0.090 MM		0.090 MM									
55_OHM_SE		*	Y	0.076 MM		0.076 MM		~STANDARD		~STANDARD		~STANDARD			
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH		MINIMUM NECK WIDTH		MAXIMUM NECK LENGTH		DIFFPAIR PRIMARY GAP		DIFFPAIR NECK GAP			
50_OHM_SE		TOP, BOTTOM	Y	0.110 MM		0.095 MM									
50_OHM_SE		*	Y	0.090 MM		0.090 MM		~STANDARD		~STANDARD		~STANDARD			
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH		MINIMUM NECK WIDTH		MAXIMUM NECK LENGTH		DIFFPAIR PRIMARY GAP		DIFFPAIR NECK GAP			
40_OHM_SE		TOP, BOTTOM	Y	0.165 MM		0.095 MM									
40_OHM_SE		*	Y	0.135 MM		0.135 MM		~STANDARD		~STANDARD		~STANDARD			
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH		MINIMUM NECK WIDTH		MAXIMUM NECK LENGTH		DIFFPAIR PRIMARY GAP		DIFFPAIR NECK GAP			
27P4_OHM_SE		TOP, BOTTOM	Y	0.310 MM		0.095 MM									
27P4_OHM_SE		*	Y	0.250 MM		0.250 MM		~STANDARD		~STANDARD		~STANDARD			
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH		MINIMUM NECK WIDTH		MAXIMUM NECK LENGTH		DIFFPAIR PRIMARY GAP		DIFFPAIR NECK GAP			
70_OHM_DIFF		*	N	~STANDARD		~STANDARD		~STANDARD		~STANDARD		~STANDARD			
70_OHM_DIFF		ISL3, ISL4	Y	0.160 MM		0.160 MM				0.175 MM		0.175 MM			
70_OHM_DIFF		ISL9, ISL10	Y	0.160 MM		0.160 MM				0.175 MM		0.175 MM			
70_OHM_DIFF		ISL2, ISL11	Y	0.170 MM		0.170 MM				0.150 MM		0.150 MM			
70_OHM_DIFF		TOP, BOTTOM	Y	0.170 MM		0.095 MM				0.150 MM		0.150 MM			
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH		MINIMUM NECK WIDTH		MAXIMUM NECK LENGTH		DIFFPAIR PRIMARY GAP		DIFFPAIR NECK GAP			
80_OHM_DIFF		*	N	~STANDARD		~STANDARD		~STANDARD		~STANDARD		~STANDARD			
80_OHM_DIFF		ISL3, ISL4	Y	0.125 MM		0.125 MM				0.180 MM		0.180 MM			
80_OHM_DIFF		ISL9, ISL10	Y	0.125 MM		0.125 MM				0.180 MM		0.180 MM			
80_OHM_DIFF		ISL2, ISL11	Y	0.140 MM		0.140 MM				0.190 MM		0.190 MM			
80_OHM_DIFF		TOP, BOTTOM	Y	0.140 MM		0.095 MM				0.190 MM		0.190 MM			
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH		MINIMUM NECK WIDTH		MAXIMUM NECK LENGTH		DIFFPAIR PRIMARY GAP		DIFFPAIR NECK GAP			
90_OHM_DIFF		*	N	~STANDARD		~STANDARD		~STANDARD		~STANDARD		~STANDARD			
90_OHM_DIFF		ISL3, ISL4	Y	0.102 MM		0.102 MM				0.220 MM		0.220 MM			
90_OHM_DIFF		ISL9, ISL10	Y	0.102 MM		0.102 MM				0.220 MM		0.220 MM			
90_OHM_DIFF		ISL2, ISL11	Y	0.115 MM		0.115 MM				0.230 MM		0.230 MM			
90_OHM_DIFF		TOP, BOTTOM	Y	0.115 MM		0.095 MM				0.230 MM		0.230 MM			
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH		MINIMUM NECK WIDTH		MAXIMUM NECK LENGTH		DIFFPAIR PRIMARY GAP		DIFFPAIR NECK GAP			
100_OHM_DIFF		*	N	~STANDARD		~STANDARD		~STANDARD		~STANDARD		~STANDARD			
100_OHM_DIFF		ISL3, ISL4	Y	0.080 MM		0.080 MM				0.200 MM		0.200 MM			
100_OHM_DIFF		ISL9, ISL10	Y	0.080 MM		0.080 MM				0.200 MM		0.200 MM			
100_OHM_DIFF		ISL2, ISL11	Y	0.089 MM		0.089 MM				0.220 MM		0.220 MM			
100_OHM_DIFF		TOP, BOTTOM	Y	0.089 MM		0.089 MM				0.220 MM		0.220 MM			
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH		MINIMUM NECK WIDTH		MAXIMUM NECK LENGTH		DIFFPAIR PRIMARY GAP		DIFFPAIR NECK GAP			
110_OHM_DIFF		*	N	~STANDARD		~STANDARD		~STANDARD		~STANDARD		~STANDARD			
110_OHM_DIFF		ISL3, ISL4	Y	0.077 MM		0.077 MM				0.330 MM		0.330 MM			
110_OHM_DIFF		ISL9, ISL10	Y	0.077 MM		0.077 MM				0.330 MM		0.330 MM			
110_OHM_DIFF		ISL2, ISL11	Y	0.077 MM		0.077 MM				0.330 MM		0.330 MM			
110_OHM_DIFF		TOP, BOTTOM	Y	0.077 MM		0.077 MM				0.330 MM		0.330 MM			
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH		MINIMUM NECK WIDTH		MAXIMUM NECK LENGTH		DIFFPAIR PRIMARY GAP		DIFFPAIR NECK GAP			
100_DIFF_BGA		*	~100_OHM_DIFF	~100_OHM_DIFF		~100_OHM_DIFF		~100_OHM_DIFF		~100_OHM_DIFF		~100_OHM_DIFF			
100_DIFF_BGA		ISL3, ISL4	Y	0.075 MM		0.075 MM				0.125 MM		0.125 MM			
100_DIFF_BGA		ISL9, ISL10	Y	0.075 MM		0.075 MM				0.125 MM		0.125 MM			
NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.															
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH		MINIMUM NECK WIDTH		MAXIMUM NECK LENGTH		DIFFPAIR PRIMARY GAP		DIFFPAIR NECK GAP			
100_OHM_DIFF		*	N	~STANDARD		~STANDARD		~STANDARD		~STANDARD		~STANDARD			
100_OHM_DIFF		ISL3, ISL4	Y	0.080 MM		0.080 MM				0.200 MM		0.200 MM			
100_OHM_DIFF		ISL9, ISL10	Y	0.080 MM		0.080 MM				0.200 MM		0.200 MM			
100_OHM_DIFF		ISL2, ISL11	Y	0.089 MM		0.089 MM				0.220 MM		0.220 MM			
100_OHM_DIFF		TOP, BOTTOM	Y	0.089 MM		0.089 MM				0.220 MM		0.220 MM			
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH		MINIMUM NECK WIDTH		MAXIMUM NECK LENGTH		DIFFPAIR PRIMARY GAP		DIFFPAIR NECK GAP			
110_OHM_DIFF		*	N	~STANDARD		~STANDARD		~STANDARD		~STANDARD		~STANDARD			
110_OHM_DIFF		ISL3, ISL4	Y	0.077 MM		0.077 MM				0.330 MM		0.330 MM			
110_OHM_DIFF		ISL9, ISL10	Y	0.077 MM		0.077 MM				0.330 MM		0.330 MM			
110_OHM_DIFF		ISL2, ISL11	Y	0.077 MM		0.077 MM				0.330 MM		0.330 MM			
110_OHM_DIFF		TOP, BOTTOM	Y	0.077 MM		0.077 MM				0.330 MM		0.330 MM			
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH		MINIMUM NECK WIDTH		MAXIMUM NECK LENGTH		DIFFPAIR PRIMARY GAP		DIFFPAIR NECK GAP			
100_OHM_DIFF		*	N	~STANDARD		~STANDARD		~STANDARD		~STANDARD		~STANDARD			
100_OHM_DIFF		ISL3, ISL4	Y	0.080 MM		0.080 MM				0.200 MM		0.200 MM			
100_OHM_DIFF		ISL9, ISL10	Y	0.080 MM		0.080 MM				0.200 MM		0.200 MM			
100_OHM_DIFF		ISL2, ISL11	Y	0.089 MM		0.089 MM				0.220 MM		0.220 MM			
100_OHM_DIFF		TOP, BOTTOM	Y	0.089 MM		0.089 MM				0.220 MM		0.220 MM			
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH		MINIMUM NECK WIDTH		MAXIMUM NECK LENGTH		DIFFPAIR PRIMARY GAP		DIFFPAIR NECK GAP			
110_OHM_DIFF		*	N	~STANDARD		~STANDARD		~STANDARD		~STANDARD		~STANDARD			
110_OHM_DIFF		ISL3, ISL4	Y	0.077 MM		0.077 MM				0.330 MM		0.330 MM			
110_OHM_DIFF		ISL9, ISL10	Y	0.077 MM		0.077 MM				0.330 MM		0.330 MM			
110_OHM_DIFF		ISL2, ISL11	Y	0.077 MM		0.077 MM				0.330 MM		0.330 MM			
110_OHM_DIFF		TOP, BOTTOM	Y	0.077 MM		0.077 MM				0.330 MM		0.330 MM			
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH		MINIMUM NECK WIDTH		MAXIMUM NECK LENGTH		DIFFPAIR PRIMARY GAP		DIFFPAIR NECK GAP			
100_OHM_DIFF		*	N	~STANDARD		~STANDARD		~STANDARD		~STANDARD		~STANDARD			
100_OHM_DIFF		ISL3, ISL4	Y	0.080 MM		0.080 MM				0.200 MM		0.200 MM			
100_OHM_DIFF		ISL9, ISL10	Y	0.080 MM		0.080 MM				0.200 MM		0.200 MM			
100_OHM_DIFF		ISL2, ISL11	Y	0.089 MM		0.089 MM				0.220 MM		0.220 MM			
100_OHM_DIFF		TOP, BOTTOM	Y	0.089 MM		0.089 MM				0.220 MM		0.220 MM			
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH		MINIMUM NECK WIDTH		MAXIMUM NECK LENGTH		DIFFPAIR PRIMARY GAP		DIFFPAIR NECK GAP			
110_OHM_DIFF		*	N	~STANDARD		~STANDARD		~STANDARD		~STANDARD		~STANDARD			
110_OHM_DIFF		ISL3, ISL4	Y	0.077 MM		0.077 MM				0.330 MM		0.330 MM			
110_OHM_DIFF		ISL9, ISL10	Y	0.077 MM		0.077 MM				0.330 MM		0.330 MM			
110_OHM_DIFF		ISL2, ISL11	Y	0.077 MM		0.077 MM				0.330 MM		0.330 MM			
110_OHM_DIFF		TOP, BOTTOM	Y	0.077 MM		0.077 MM				0.330 MM		0.330 MM			
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH		MINIMUM NECK WIDTH		MAXIMUM NECK LENGTH		DIFFPAIR PRIMARY GAP		DIFFPAIR NECK GAP			
100_OHM_DIFF		*	N	~STANDARD		~STANDARD		~STANDARD		~STANDARD		~STANDARD			
100_OHM_DIFF		ISL3, ISL4	Y	0.080 MM		0.080 MM				0.200 MM		0.200 MM			
100_OHM_DIFF		ISL9, ISL10	Y	0.080 MM		0.080 MM				0.200 MM		0.200 MM			
100_OHM_DIFF		ISL2, ISL11	Y	0.089 MM		0.089 MM				0.220 MM		0.220 MM			
100_OHM_DIFF		TOP, BOTTOM	Y	0.089 MM		0.089 MM				0.220 MM		0.220 MM			
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH		MINIMUM NECK WIDTH		MAXIMUM NECK LENGTH		DIFFPAIR PRIMARY GAP		DIFFPAIR NECK GAP			
110_OHM_DIFF		*	N	~STANDARD		~STANDARD		~STANDARD		~STANDARD		~STANDARD			
110_OHM_DIFF		ISL3, ISL4	Y	0.077 MM		0.077 MM				0.330 MM		0.330 MM			
110_OHM_DIFF		ISL9, ISL10	Y	0.077 MM		0.077 MM				0.330 MM		0.330 MM			
110_OHM_DIFF		ISL2, ISL11	Y	0.077 MM		0.077 MM				0.330 MM		0.330 MM			
110_OHM_DIFF		TOP, BOTTOM	Y	0.077 MM		0.077 MM				0.330 MM		0.330 MM			
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH		MINIMUM NECK WIDTH		MAXIMUM NECK LENGTH		DIFFPAIR PRIMARY GAP		DIFFPAIR NECK GAP			
100_OHM_DIFF		*	N	~STANDARD		~STANDARD		~STANDARD		~STANDARD		~STANDARD			
100_OHM_DIFF		ISL3, ISL4	Y	0.080 MM		0.080 MM				0.200 MM		0.200 MM			
100_OHM_DIFF		ISL9, ISL10	Y	0.080 MM		0.080 MM				0.200 MM		0.200 MM			
100_OHM_DIFF		ISL2, ISL11	Y	0.089 MM		0.089 MM				0.220 MM		0.220 MM			
100_OHM_DIFF		TOP, BOTTOM	Y	0.089 MM		0.089 MM				0.220 MM		0.220 MM			
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH		MINIMUM NECK WIDTH		MAXIMUM NECK LENGTH		DIFFPAIR PRIMARY GAP		DIFFPAIR NECK GAP			
110_OHM_DIFF		*	N	~STANDARD		~STANDARD		~STANDARD		~STANDARD		~STANDARD			
110_OHM_DIFF		ISL3, ISL4	Y	0.077 MM		0.077 MM				0.330 MM		0.330 MM			
110_OHM_DIFF		ISL9, ISL10	Y	0.077 MM		0.077 MM				0.330 MM		0.330 MM			
110_OHM_DIFF		ISL2, ISL11	Y	0.077 MM		0.077 MM				0.330 MM		0.330 MM			
110_OHM_DIFF		TOP, BOTTOM	Y	0.077 MM		0.077 MM				0.330 MM		0.330 MM			
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH		MINIMUM NECK WIDTH		MAXIMUM NECK LENGTH		DIFFPAIR PRIMARY GAP		DIFFPAIR NECK GAP			
100_OHM_DIFF		*	N	~STANDARD		~STANDARD		~STANDARD		~STANDARD		~STANDARD			
100_OHM_DIFF		ISL3, ISL4	Y	0.080 MM		0.080 MM				0.200 MM		0.200 MM			
100_OHM_DIFF		ISL9, ISL10	Y	0.080 MM		0.080 MM				0.200 MM		0.200 MM			
100_OHM_DIFF		ISL2, ISL11	Y	0.089 MM		0.089 MM				0.220 MM		0.220 MM			
100_OHM_DIFF		TOP, BOTTOM	Y	0.089 MM		0.089 MM				0.220 MM		0.220 MM			
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH		MINIMUM NECK WIDTH		MAXIMUM NECK LENGTH		DIFFPAIR PRIMARY GAP		DIFFPAIR NECK GAP			
110_OHM_DIFF		*	N	~STANDARD		~STANDARD		~STANDARD		~STANDARD		~STANDARD			
110_OHM_DIFF		ISL3, ISL4	Y	0.077 MM		0.077 MM				0.330 MM		0.330 MM			
110_OHM_DIFF		ISL9, ISL10	Y	0.077 MM		0.077 MM				0.330 MM		0.330 MM			
110_OHM_DIFF		ISL2, IS													

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	~DEFAULT	?
BGA_P1MM	*	~DEFAULT	?
BGA_P2MM	*	~DEFAULT	?
BGA_P3MM	*	~DEFAULT	?
PGA_CPU	*	0.073 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P3MM
CLK_PCTE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

NOTE: From T18 MLB, changed to reflect M99 stackup.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	~STANDARD	~STANDARD	~STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	~100_OHM_DIFF	~100_OHM_DIFF	~100_OHM_DIFF	~100_OHM_DIFF	~100_OHM_DIFF	~100_OHM_DIFF
100_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

PCB Rule Definitions

SYNC_MASTER=M99_MLB

SYNC_DATE=01/22/2008


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