

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD DATE
			2011-04-08

K78 MLB SCHEMATIC

04/08/11

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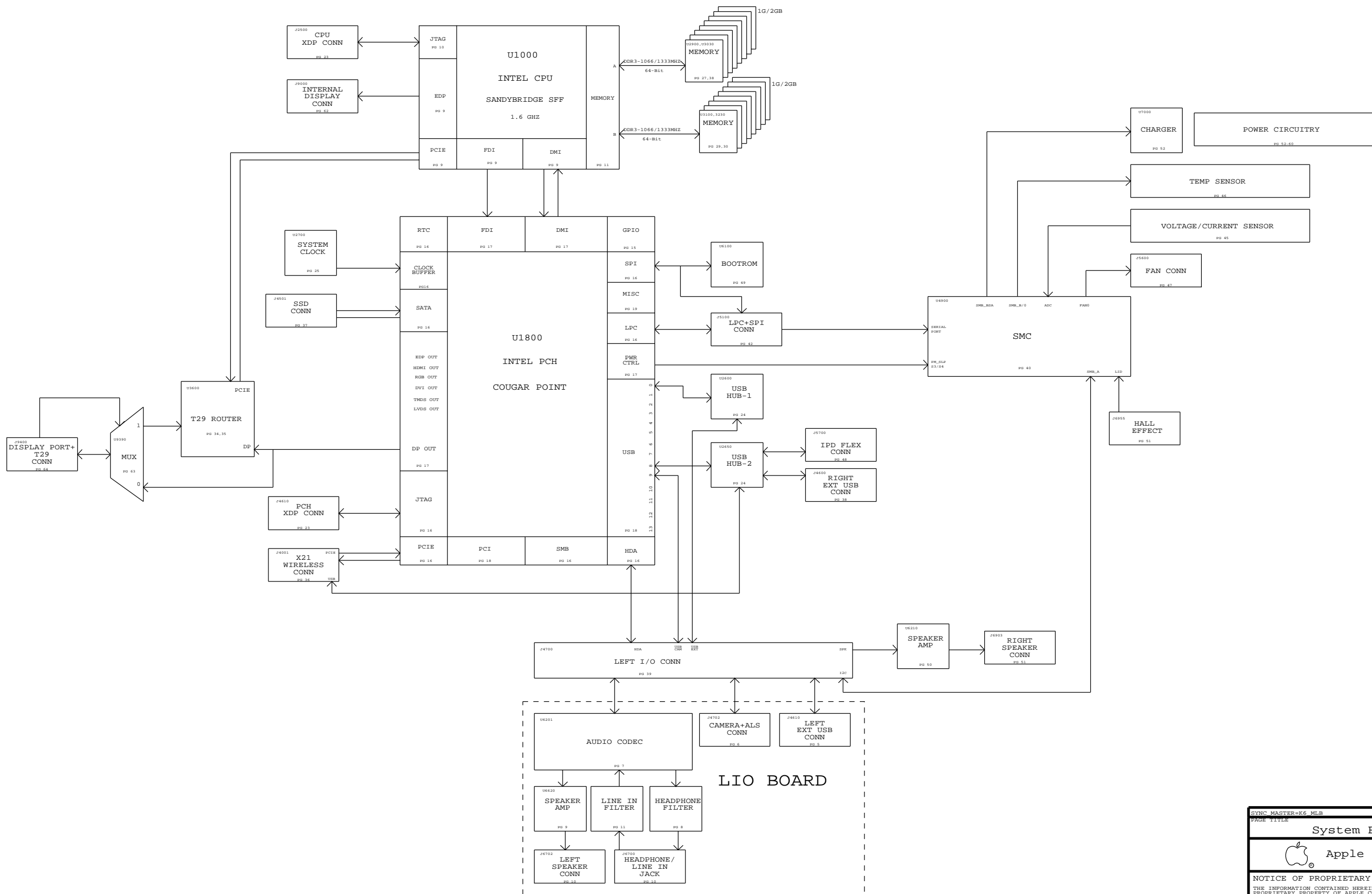
Schematic / PCB #'s

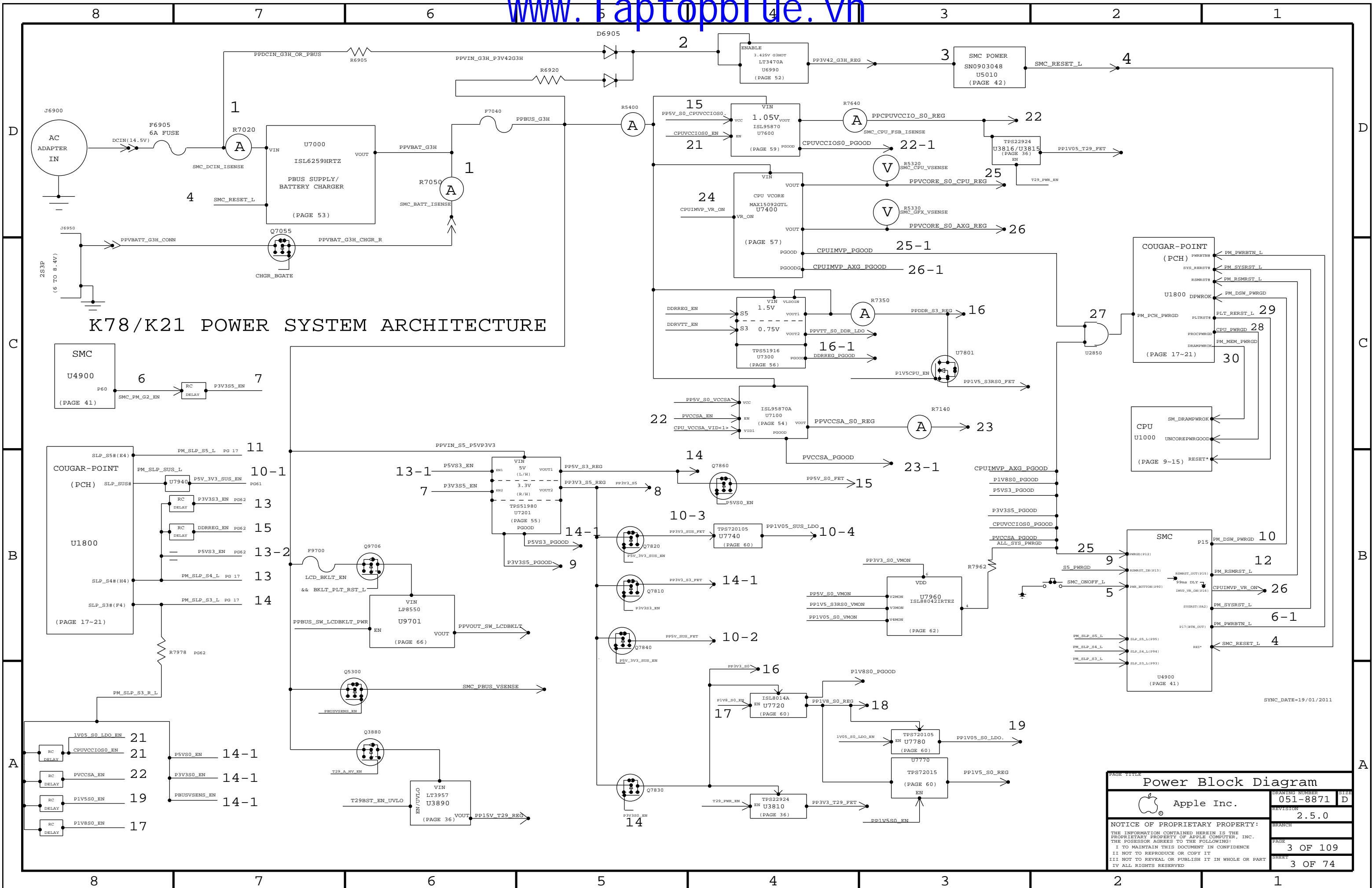
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8871	1	SCREEN_MLB,K78	SCH	CRITICAL	
820-3024	1	PCBP_MLB,K78	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST MODIFIED=11 MAY '08 10:02:01 2011

PRODUCT SAFETY REQUIREMENTS:
PCB, UL RECOGNIZED, MIN. 130-C TEMP. RATING AND V-0 FLAME RATING PER UL 796 & UL 94.
PCB TO BE SILK-SCREENED WITH UL/CUL RECOGNITION MARK, MANUFACTURER'S UL FILE
NUMBER, UL PCB MATERIAL DESIGNATION, 130-C TEMP. RATING AND V-0 FLAME RATING.

DRAWING TITLE		
SCHEM,MLB,K78		
 Apple Inc.	DRAWING NUMBER	051-8871
	REVISION	2.5.0
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K78 BOM GROUPS

BOM GROUP	BOM OPTIONS
K78_COMMON	ALTERNATE,COMMON,K78_MISC,K78_DEBUG:ENG,K78_PROGPARTS,USBHUB_2513B,T29BST:Y,EDP
K78_MISC	PCH:B3,CPUMEM_S0,HUB1_2NONREM,HUB2_2NONREM,T29:YES,SDRVI2C:MCU,SDRV_PD,KB_BL
K78_PROGPARTS	BOOTROM_PROG,SMC_PROG,T29ROM:PROG,T29MCU:PROG
K78_DEVEL:ENG	BELT:ENG,BMON:ENG,XDP_CONN,XDP_CPU:BPW,XDP_PCH,LPCLPLUS,VREFPMGN,S0PGOOD_ISL,S3_S0_LED,VCCIOISNS_BMG,AIRPORTISNS_BMG,REDISNS_BMG,LCDCLKTISNS_BMG
K78_DEVEL:PVT	LPCLPLUS,XDP_CONN,XDP_PCH
K78_DEBUG:ENG	DEVEL_BOM,SMC_DEBUG_YES,XDP
K78_DEBUG:PVT	DEVEL_BOM,BKLT:PROD,BMON:PROD,SMC_DEBUG_YES,XDP,VREFPMGN_NOT
K78_DEBUG:PROD	BKLT:PROD,BMON:PROD,SMC_DEBUG_YES,XDP,VREFPMGN_NOT,LPCLPLUS,VCCIOISNS_PROD,AIRPORTISNS_PROD,HDDISNS_PROD,LCDCLKTISNS_PROD
DDR3:HYNIX_2GB	DRAM_CFG0:L,DRAM_CFG1:L,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:HYNIX_2GB
DDR3:HYNIX_4GB	DRAM_CFG0:L,DRAM_CFG1:L,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:HYNIX_4GB
DDR3:SAMSUNG_2GB	DRAM_CFG0:L,DRAM_CFG1:H,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:SAMSUNG_2GB
DDR3:SAMSUNG_4GB	DRAM_CFG0:L,DRAM_CFG1:H,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:SAMSUNG_4GB
DDR3:MICRON_2GB	DRAM_CFG0:H,DRAM_CFG1:L,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:MICRON_2GB
DDR3:ELPIDA_4GB	DRAM_CFG0:H,DRAM_CFG1:H,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:ELPIDA_4GB

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
33580550	1	EEPROM,32KB:IT,2X3QFN	U3690	CRITICAL	T29ROM:BLANK
341T0354	1	IC,T29-ROM,K78	U3690	CRITICAL	T29ROM:PROG
33783997	1	IC,MCU,32B,LPQ112A,16KB/2KB,WQFN25	U9330	CRITICAL	T29MCU:BLANK
341T0355	1	IC,T29-MCU,K78	U9330	CRITICAL	T29MCU:PROG
33880895	1	IC,SMC,RENESAS,H8S/2117BP,99M,TLP,HF	U4900	CRITICAL	SMC_BLANK
341T0350	1	IC,SMC,K78	U4900	CRITICAL	SMC_PROG
33580809	1	64 MBIT SPI SERIAL DUAL 1/0 FLASH,BAES2_8	U6100	CRITICAL	BOOTROM:BLANK
33580803	1	64 MBIT SPI SERIAL DUAL 1/0 FLASH,BAES2_8	U6100	CRITICAL	BOOTROM:BLANK
341T0349	1	IC,SPI ROM,K21 K78	U6100	CRITICAL	BOOTROM:PROG

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
37680855	37680613		ALL	Diodes alt to Toshiba
37680977	37680859		ALL	Diodes alt to Toshiba
37680972	37680612		ALL	Bohm alt to Toshiba
37780107	37780066		ALL	Omami alt to Semtech
13880676	13880691		ALL	Murata alt to Samsung
37180679	37180652		ALL	NXP alt to NXP
13880671	13880673		ALL	Taiyo alt to Murata
13880679	13880678		ALL	Murata/Samsung alt to Taiyo
35183312	35183055		ALL	NXP ALT TO PERICOM
10480035	10480011		ALL	Panasonic alt to Cytotec
15281085	15281307		ALL	Toko alt to Cytotec
15281462	15281295		ALL	Toko alt to NMC Inductor
12880333	12880294		ALL	Sanyo alt to Sanyo/Fredrick
33784092	33784100		ALL	EARLY 1.5GHZ CPU SAMPLES
33784093	33784101		ALL	EARLY 1.4GHZ CPU SAMPLES
37680874	37680895		ALL	FMG02028 alt to RJX03802NS
37681018	37680617		ALL	FMG0349 alt to RJX03050DB
37680826	37680917		ALL	RJX0320DB alt to FMG0355
514-0744	998-3941		ALL	SDP connector alt

DRAM CFG CHART

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

SIZE	CFG 2
2GB	0
4GB	1

DIE REV	CFG 3
A	0
B	1

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
33784101	1	SNB,QAM1,QS,J1,1.6,17W,2+2,1.1,4M,BGA	U1000	CRITICAL	CPU:1.6GHZ
33784100	1	SNB,QAM2,QS,J1,1.5,17W,2+2,1.1,4M,BGA	U1000	CRITICAL	CPU:1.5GHZ
33784099	1	SNB,QAM3,QS,J1,1.4,17W,2+2,1.05,3M,BGA	U1000	CRITICAL	CPU:1.4GHZ
33784098	1	SNB,QAM4,QS,J1,1.3,17W,2+2,1.05,3M,BGA	U1000	CRITICAL	CPU:1.3GHZ
33784080	1	COUGAR POINT,SLHAG,PRQ,BDR2Q567	U1800	CRITICAL	PCH:B2
33784091	1	COUGAR POINT,B3,SLJ4K,PRQ,BDR2Q567	U1800	CRITICAL	PCH:B3
338S0976	1	IC,T29,FCBGA,PRQ 8x9MM	U3600	CRITICAL	T29:YES


333S0585	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,T-DIE,HYNIX	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0585	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,T-DIE,HYNIX	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0585	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,T-DIE,HYNIX	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0585	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,T-DIE,HYNIX	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0586	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,B-DIE,HYNIX	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0586	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,B-DIE,HYNIX	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0586	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,B-DIE,HYNIX	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0586	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,B-DIE,HYNIX	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0587	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,G-DIE,SAMSUNG	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0587	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,G-DIE,SAMSUNG	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0587	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,G-DIE,SAMSUNG	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0587	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,G-DIE,SAMSUNG	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0588	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,D-DIE,SAMSUNG	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0588	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,D-DIE,SAMSUNG	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0588	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,D-DIE,SAMSUNG	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0588	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,D-DIE,SAMSUNG	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0590	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,V68A-D,MICRON	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0590	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,V68A-D,MICRON	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0590	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,V68A-D,MICRON	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0590	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,V68A-D,MICRON	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0589	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,C-DIE,ELPIDA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0589	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,C-DIE,ELPIDA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0589	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,C-DIE,ELPIDA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0589	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,C-DIE,ELPIDA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:ELPIDA_4GB
607-6811	1	ASSEMBLY,SUBASSY,PCBA,HALL EFFECT,K99	J6955	CRITICAL	
35382929	1	IC,1SL6259,BATCHCHARGE,3%,4C4MM,QFN28	U7000	CRITICAL	

SYDC PARTNO:K11_MCB

SYDC DATE:11/16/2015

PAGE TITLE

BOM Configuration

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DRAWING NUMBER

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SIZE

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
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MAKE_BASE=TRUE				
<u>NC PEG R2D CN<15..4></u>	TRUE	==	=PEG R2D C N<15..4>	9
MAKE_BASE=TRUE				
<u>NC PEG D2RP<15..4></u>		==	=PEG D2R P<15..4>	9
MAKE_BASE=TRUE				
<u>NC PEG D2RN<15..4></u>	TRUE	==	=PEG D2R N<15..4>	9
MAKE_BASE=TRUE				

TP_PCIE_CLK100M_P64N	TRUE	NC_PCIE_CLK100M_P64N
TP_PCIE_CLK100M_P64P	MAKE_RASB=TRUE	NC_PCIE_CLK100M_P64P
TP_PCIE_CLK100M_P65N	TRUE	NC_PCIE_CLK100M_P65N
TP_PCIE_CLK100M_P65P	MAKE_RASB=TRUE	NC_PCIE_CLK100M_P65P
TP_PCIE_CLK100M_P66N	MAKE_RASB=TRUE	NC_PCIE_CLK100M_P66N
TP_PCIE_CLK100M_P66P	MAKE_RASB=TRUE	NC_PCIE_CLK100M_P66P
TP_PCIE_CLK100M_P67N	MAKE_RASB=TRUE	NC_PCIE_CLK100M_P67N
TP_PCIE_CLK100M_P67P	MAKE_RASB=TRUE	NC_PCIE_CLK100M_P67P
TP_PROC_P1_3	MAKE_RASB=TRUE	NC_PROC_P1_3
TP_SATA_B_D28N	MAKE_RASB=TRUE	NC_SATA_B_D28N
TP_SATA_B_D28P	MAKE_RASB=TRUE	NC_SATA_B_D28P
TP_SATA_B_R2D_CN	MAKE_RASB=TRUE	NC_SATA_B_R2D_CN
TP_SATA_B_R2D_CP	MAKE_RASB=TRUE	NC_SATA_B_R2D_CP
TP_SATA_D_D28N	MAKE_RASB=TRUE	NC_SATA_D_D28N
TP_SATA_D_D28P	MAKE_RASB=TRUE	NC_SATA_D_D28P
TP_SATA_D_R2D_CN	MAKE_RASB=TRUE	NC_SATA_D_R2D_CN
TP_SATA_D_R2D_CP	MAKE_RASB=TRUE	NC_SATA_D_R2D_CP
TP_SATA_E_D28N	MAKE_RASB=TRUE	NC_SATA_E_D28N
TP_SATA_E_D28P	MAKE_RASB=TRUE	NC_SATA_E_D28P
TP_SATA_E_R2D_CN	MAKE_RASB=TRUE	NC_SATA_E_R2D_CN
TP_SATA_E_R2D_CP	MAKE_RASB=TRUE	NC_SATA_E_R2D_CP
TP_SATA_F_D28N	MAKE_RASB=TRUE	NC_SATA_F_D28N
TP_SATA_F_D28P	MAKE_RASB=TRUE	NC_SATA_F_D28P
TP_SATA_F_R2D_CN	MAKE_RASB=TRUE	NC_SATA_F_R2D_CN
TP_SATA_F_R2D_CP	MAKE_RASB=TRUE	NC_SATA_F_R2D_CP

TP_ECM_TP18	TRUE	NC_ECM_TP18
TP_ECM_TP17	FALSE	NC_ECM_TP17
TP_ECM_TP16	TRUE	NC_ECM_TP16
TP_ECM_TP15	FALSE	NC_ECM_TP15
TP_ECM_TP14	FALSE	NC_ECM_TP14
TP_ECM_TP13	TRUE	NC_ECM_TP13
TP_ECM_TP12	FALSE	NC_ECM_TP12
TP_ECM_TP10	TRUE	NC_ECM_TP10
TP_ECM_TP9	TRUE	NC_ECM_TP9
TP_ECM_TP8	FALSE	NC_ECM_TP8
TP_ECM_TP7	TRUE	NC_ECM_TP7
TP_ECM_TP6	FALSE	NC_ECM_TP6
TP_ECM_TP5	FALSE	NC_ECM_TP5
TP_ECM_TP4	FALSE	NC_ECM_TP4
TP_ECM_TP3	TRUE	NC_ECM_TP3
TP_ECM_TP2	FALSE	NC_ECM_TP2
TP_ECM_TP1	FALSE	NC_ECM_TP1

1550	5000	PCH_VSS_NCTF7:1	69	1550	5000	PCH_VSS_NCTF7:15	69
1550	5000	PCH_VSS_NCTF7:2	69	1550	5000	PCH_VSS_NCTF7:17	69
1550	5000	PCH_VSS_NCTF7:3	69	1550	5000	PCH_VSS_NCTF7:19	6
1550	5000	PCH_VSS_NCTF7:5	69	1550	5000	PCH_VSS_NCTF7:19	6
1550	5000	PCH_VSS_NCTF7:9	69	1550	5000	PCH_VSS_NCTF7:19	6
1550	5000	PCH_VSS_NCTF7:11	69	1550	5000	PCH_VSS_NCTF7:21	69
1550	5000	PCH_VSS_NCTF7:11	69	1550	5000	PCH_VSS_NCTF7:25	69
1550	5000	PCH_VSS_NCTF7:12	69	1550	5000	PCH_VSS_NCTF7:27	69
1550	5000	PCH_VSS_NCTF7:12	69	1550	5000	PCH_VSS_NCTF7:29	69

8	TP LVDS IG B CLKN	TRUE	NC LVDS IG B CLKN
8	TP LVDS IG B CLKP	MAX9_BASE=TRUE TRUE	NC LVDS IG B CLKP
	TP LVDS IG BKL PWM	MAX9_BASE=TRUE TRUE	NC LVDS IG BKL PWM

SYNC MASTER=(K99 MLB)		SYNC DATE=(02/16/2010)	
PAGE TITLE			
Functional Test / No Test			
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	REVISION		
		2.5.0	
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		7 OF 109	
SHEET		6 OF 74	

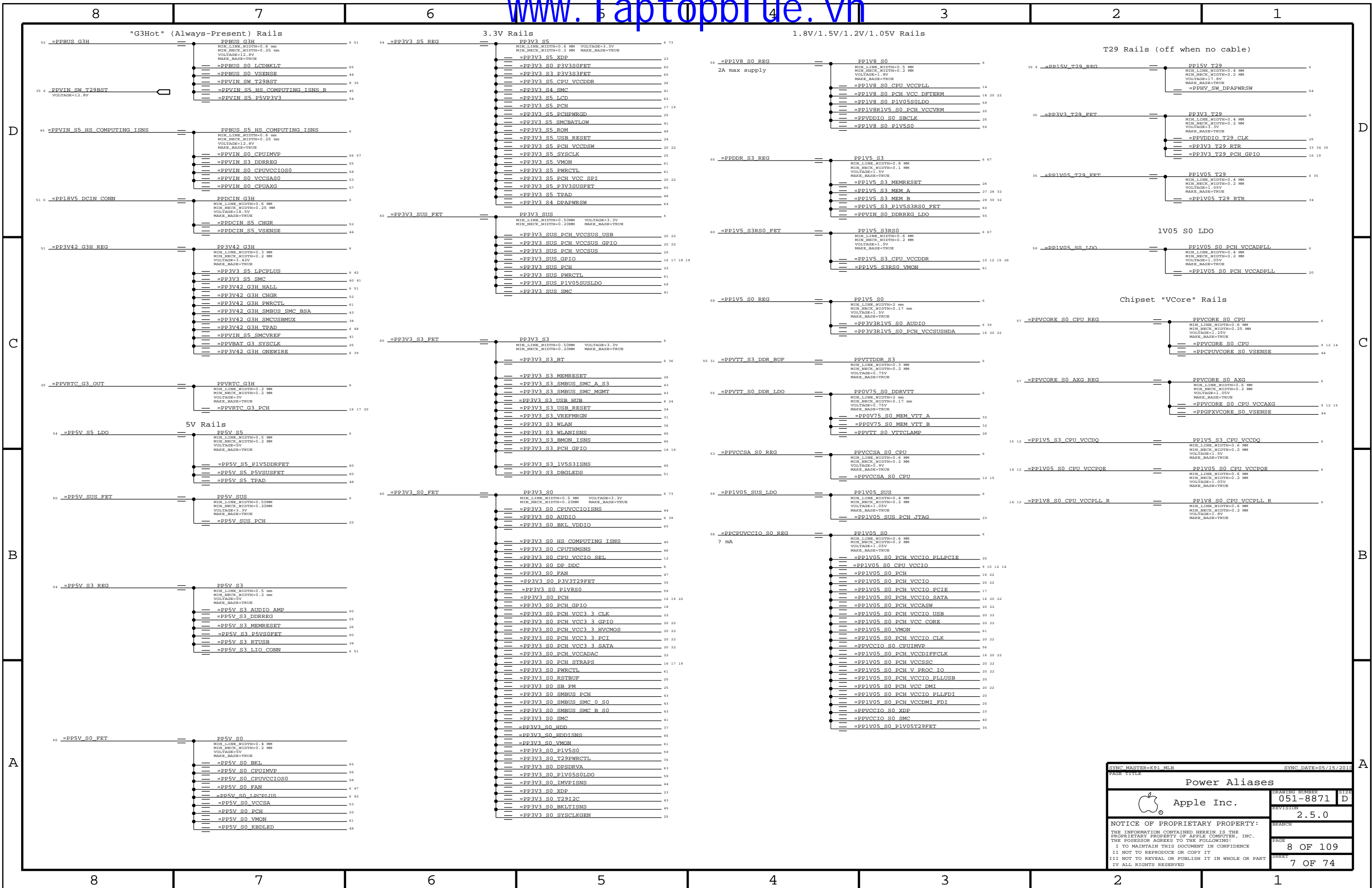
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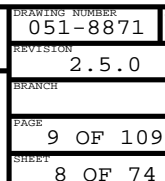
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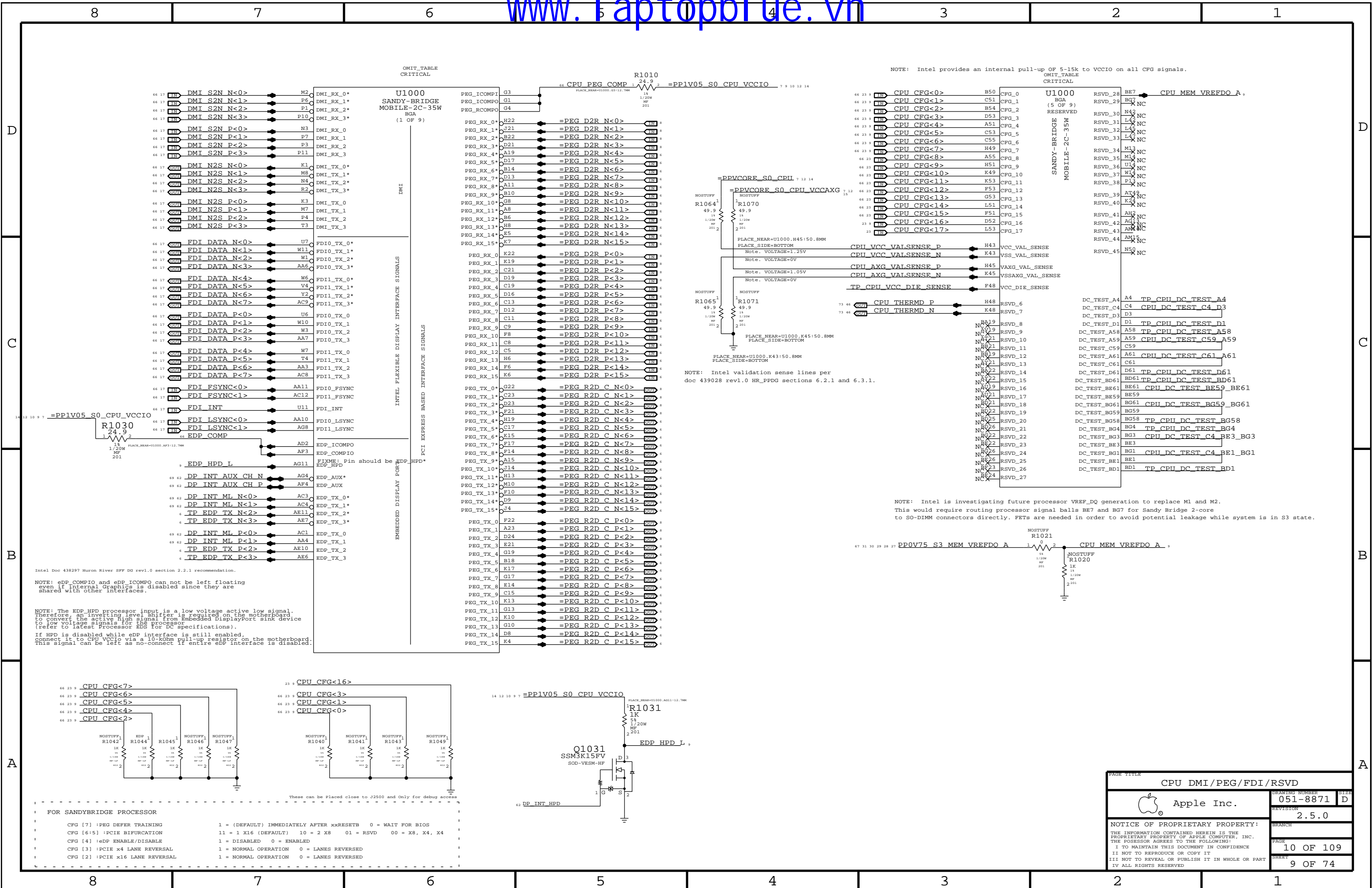
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(Need to add 27 GND TPs)

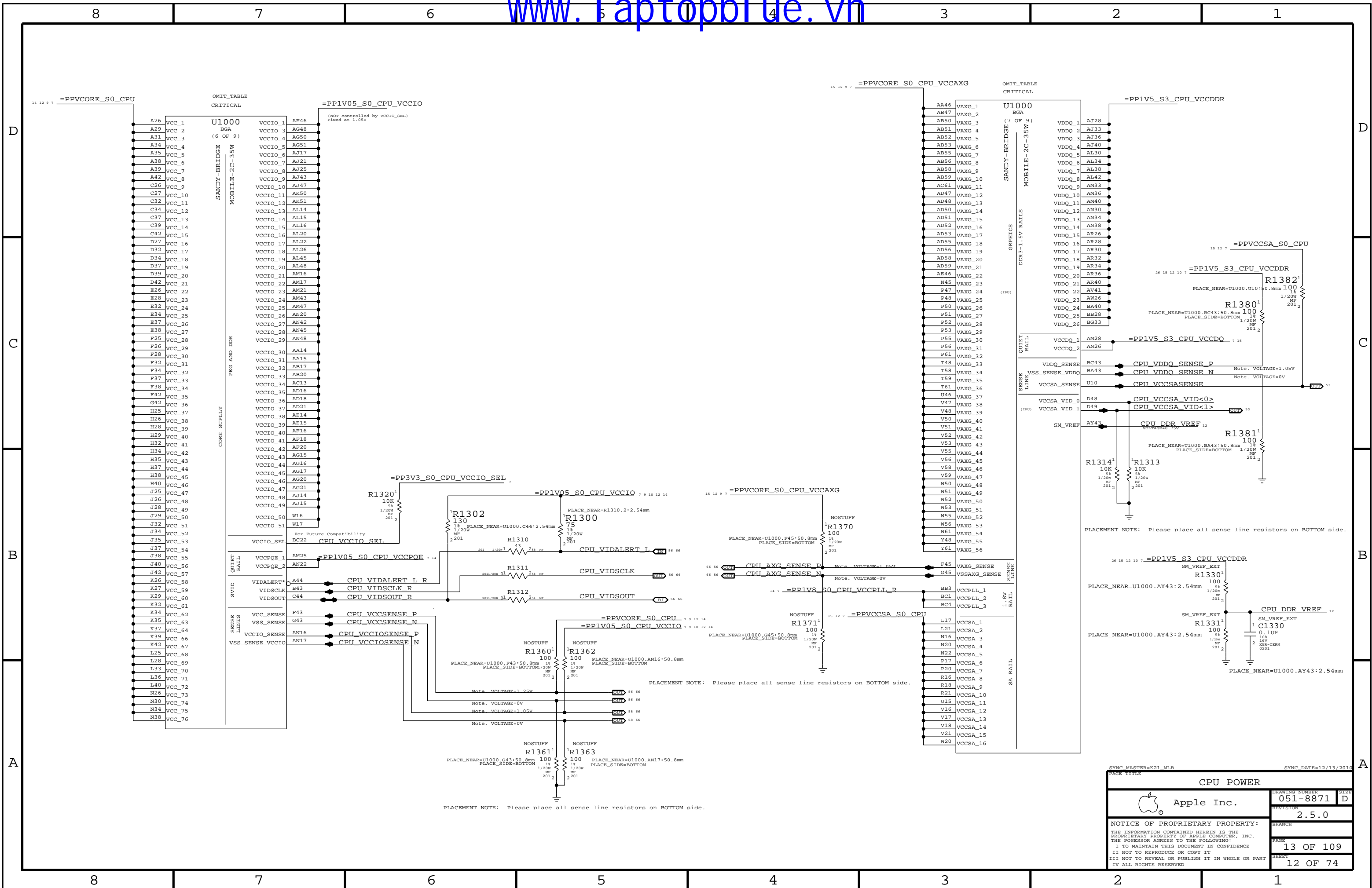








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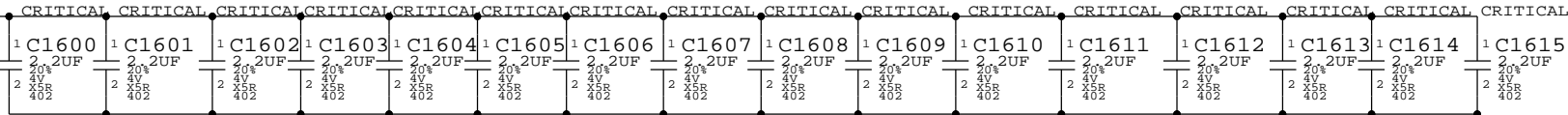
All INTEL recommendations from Intel doc #4439028 Huron River Platform Power Design Guide

Processor Load Line : -2.9 mOhms

CPU VCORE DECOUPLING

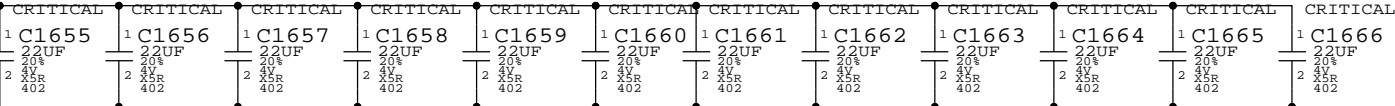
Intel recommendation (Table 7-1): 16x 2.2uF, 12x 22uF, 3x 330uF

12 9 7 =PPVCORE_S0_CPU



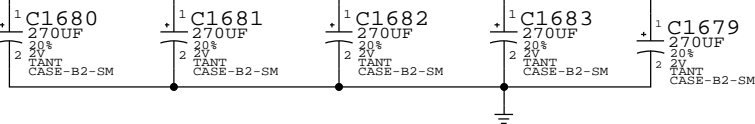
PLACEMENT_NOTE (C1655-C1666):

Place close to U1000 on top side.



PLACEMENT_NOTE (C1667-C1679):

PLACEMENT_NOTE (C1640-C1645):



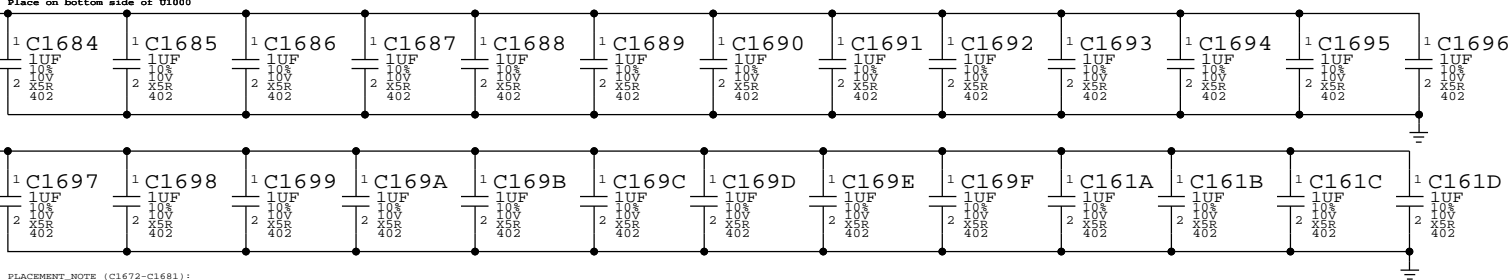
CPU VCCIO/VCCPQ DECOUPLING

Intel recommendation (Section 6.5): 26x 1uF, 10x 10uF, 2x 330uF

PLACEMENT_NOTE (C1684-C1697):

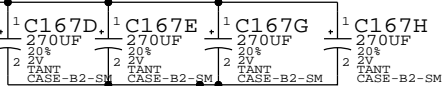
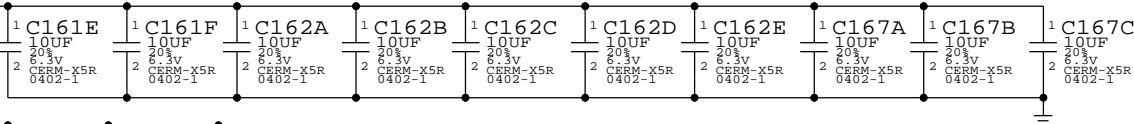
Place on bottom side of U1000

12 10 9 7 =PP1V05_S0_CPU_VCCIO

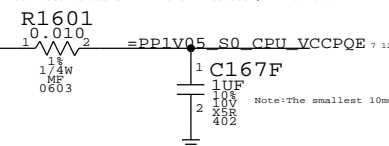


PLACEMENT_NOTE (C1672-C1681):

Place near U1000 on bottom side



Intel recommendation: 1x 10mOhm resistor, 1x 1uF 0402



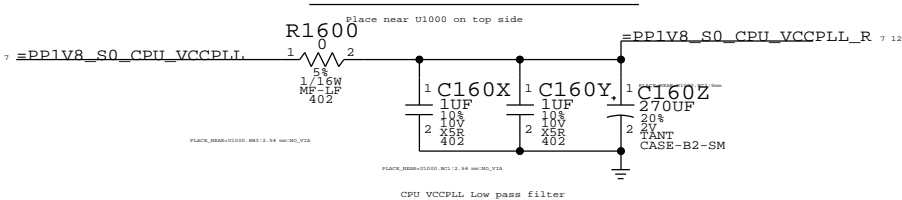
Note: The smallest 10mOhm available in the library are 0805s

CPU VCCPLL DECOUPLING


Intel recommendation (section 6.4): 2x 1uF, 1x 330uF

PLACEMENT_NOTE (C1646-C1671):

Place near U1000 on top side



CPU VCCPLL Low pass filter

PAGE TITLE		
CPU DECOUPLING-I		
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VAXG DECOUPLING

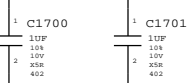
Graphics Load Line : -3.9 mOhms

Intel recommendation (section 6.3): 18x 1uF(9 no-stuff), 10x 104F(2 no-stuff), 8x 22uF(2 no stuff), 4x 470uF(2 no-stuff)

PLACEMENT_NOTE (C1700-C1710):

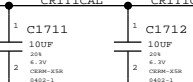
Place on bottom side of U1000

CRITICAL CRITICAL CRITICAL CRITICAL CRITICAL CRITICAL CRITICAL CRITICAL CRITICAL CRITICAL CRITICAL



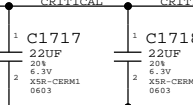
PLACEMENT_NOTE (C1711-C1716):

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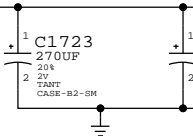
PLACEMENT_NOTE (C1717-C1722):

CRITICAL CRITICAL CRITICAL CRITICAL CRITICAL CRITICAL



PLACEMENT_NOTE (C1723-C1724):

CRITICAL CRITICAL CRITICAL



CPU VDDQ/VCCDQ DECOUPLING

Intel recommendation (Section 6.13): 10x 1uF, 8x 10uF, 1x 330uF

PLACEMENT_NOTE (C1738-C1747):

Place on bottom side of U1000

CRITICAL CRITICAL CRITICAL CRITICAL CRITICAL CRITICAL CRITICAL CRITICAL CRITICAL CRITICAL



Place close to U1000 on bottom side

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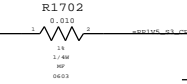


CRITICAL CRITICAL CRITICAL



Intel recommendation: 1x 10mOhm resistor, 1x 1uF 0402

R1702



CPU VCCSA DECOUPLING

Intel recommendation (Section 6.6): 3x 1uF, 3x 10uF, 1x 330uF

PLACEMENT_NOTE (C1758-C1762):

Place on bottom side of U1000

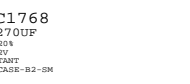
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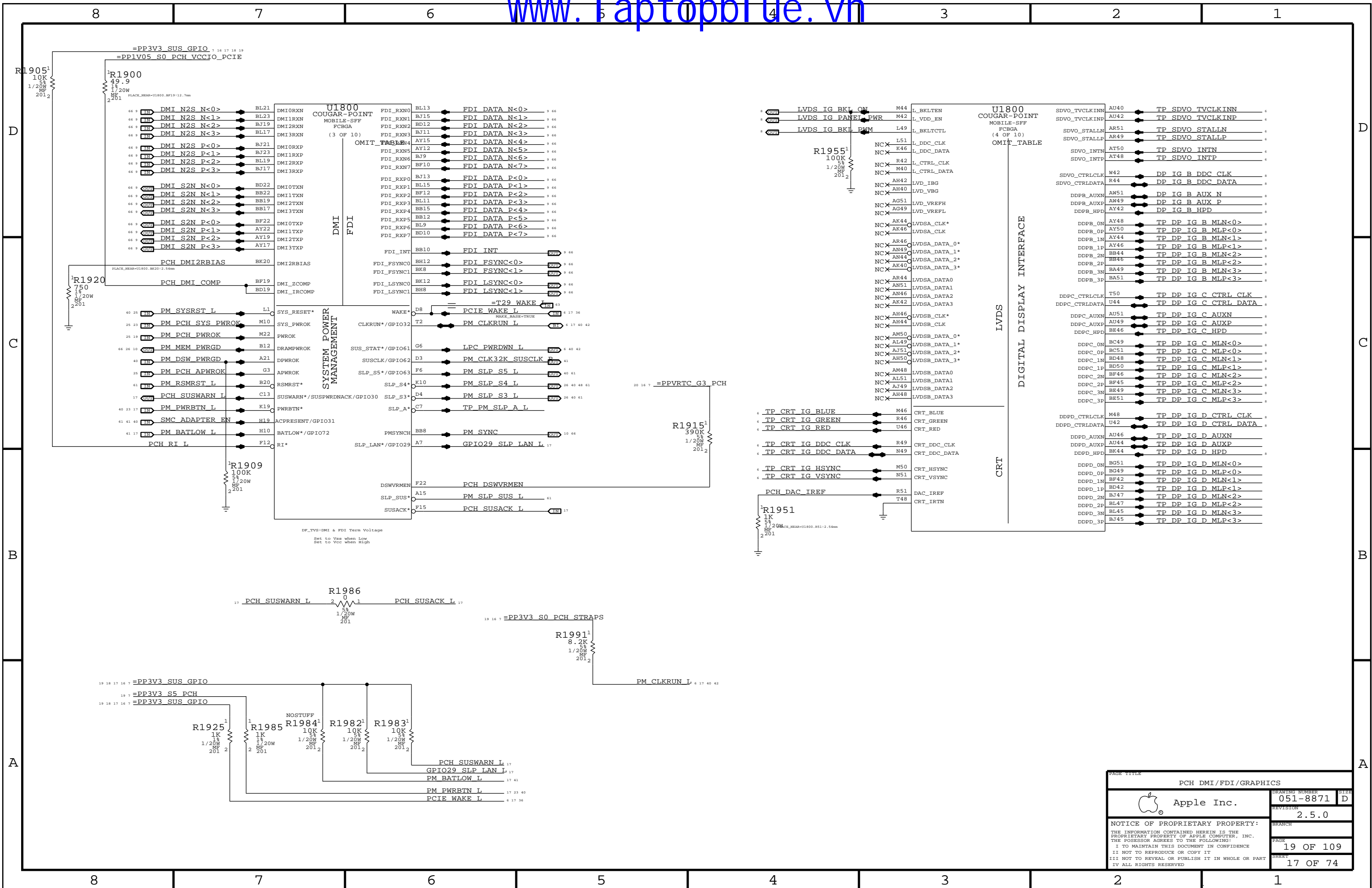


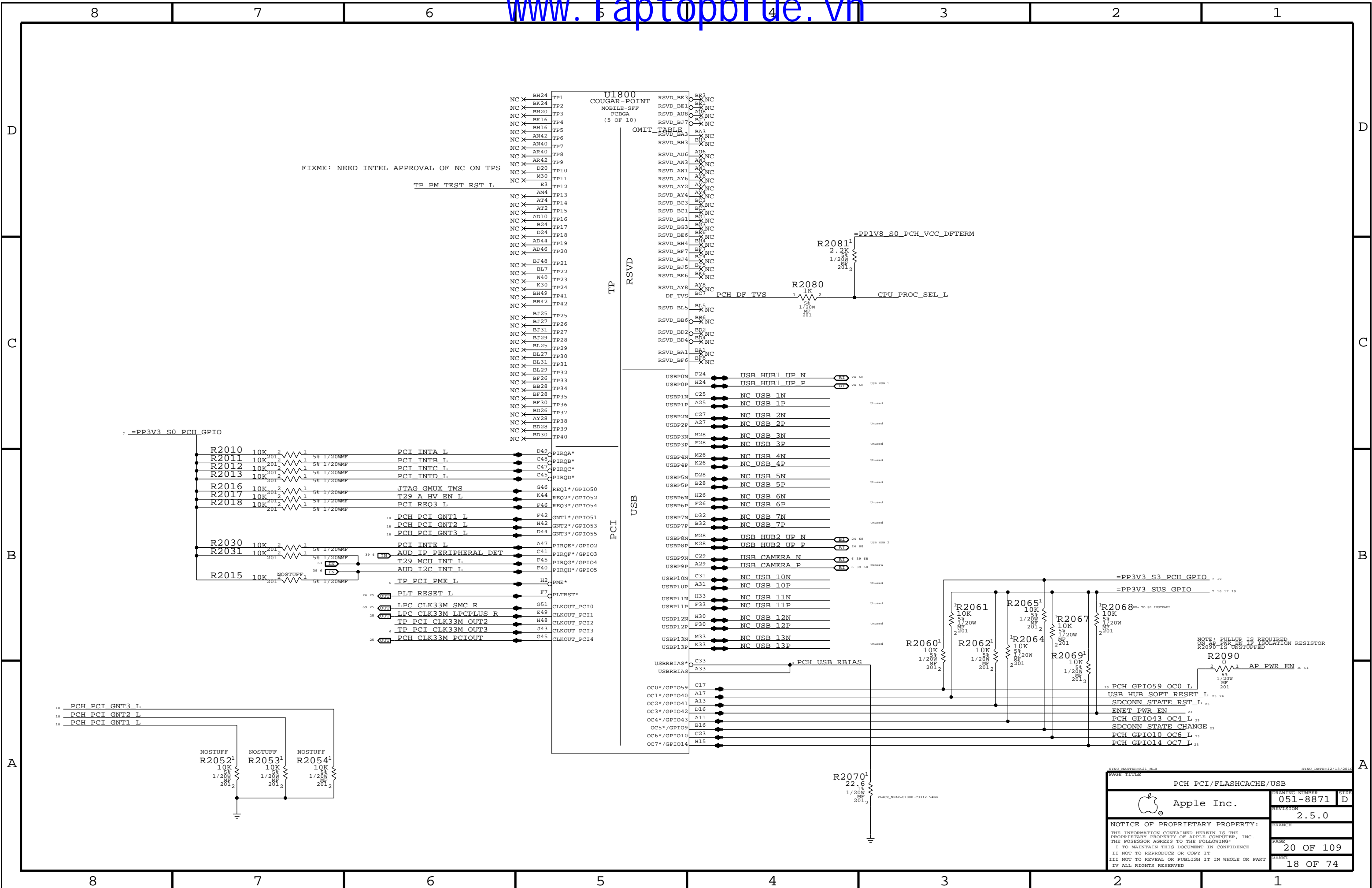
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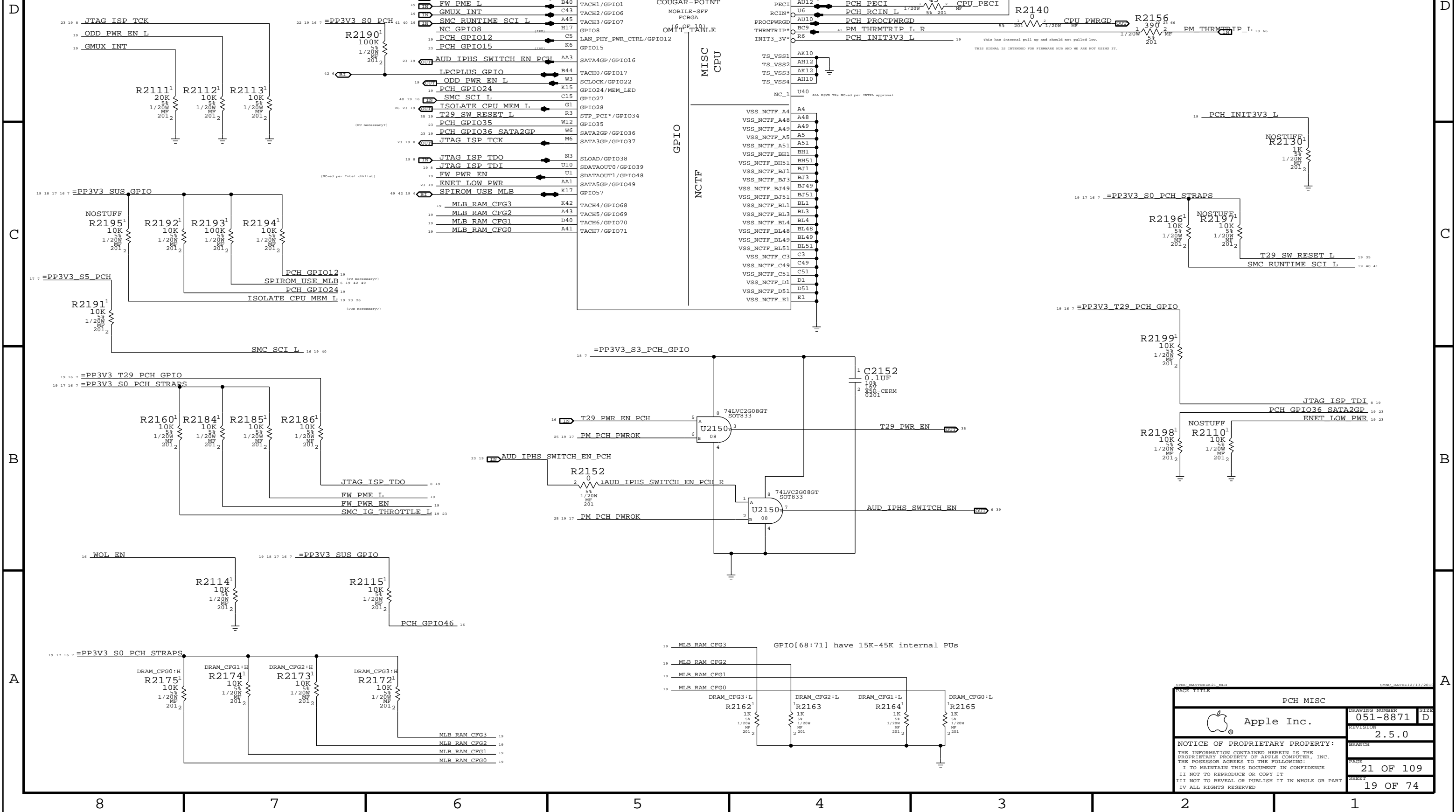


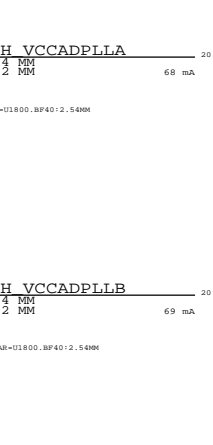
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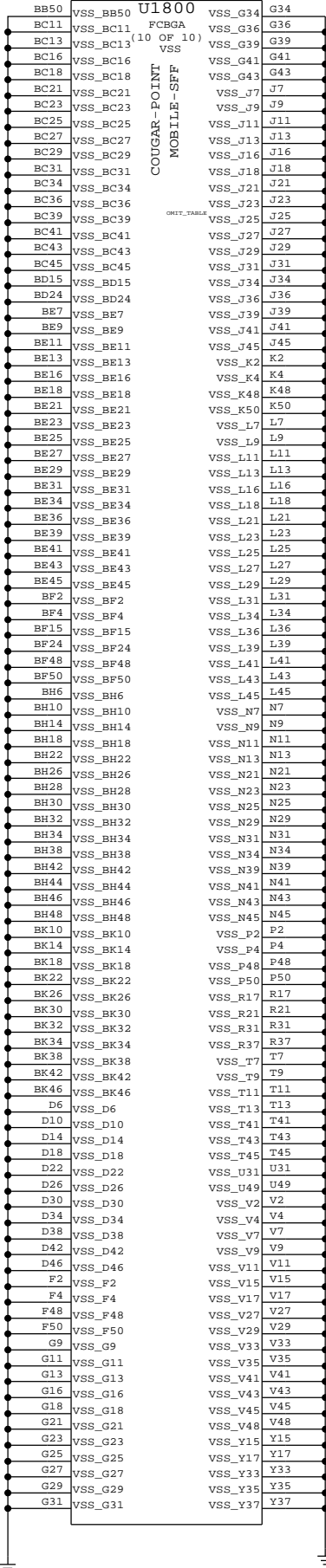
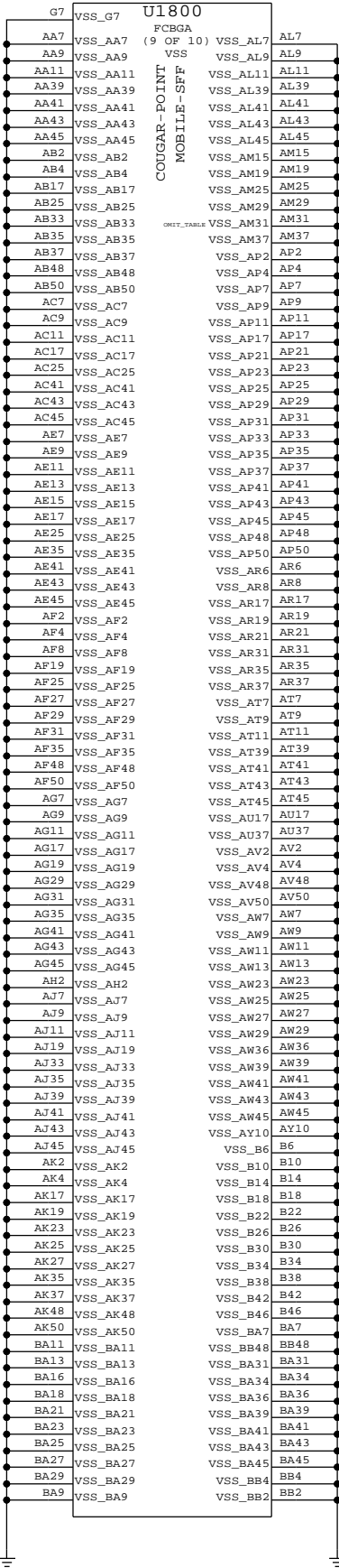
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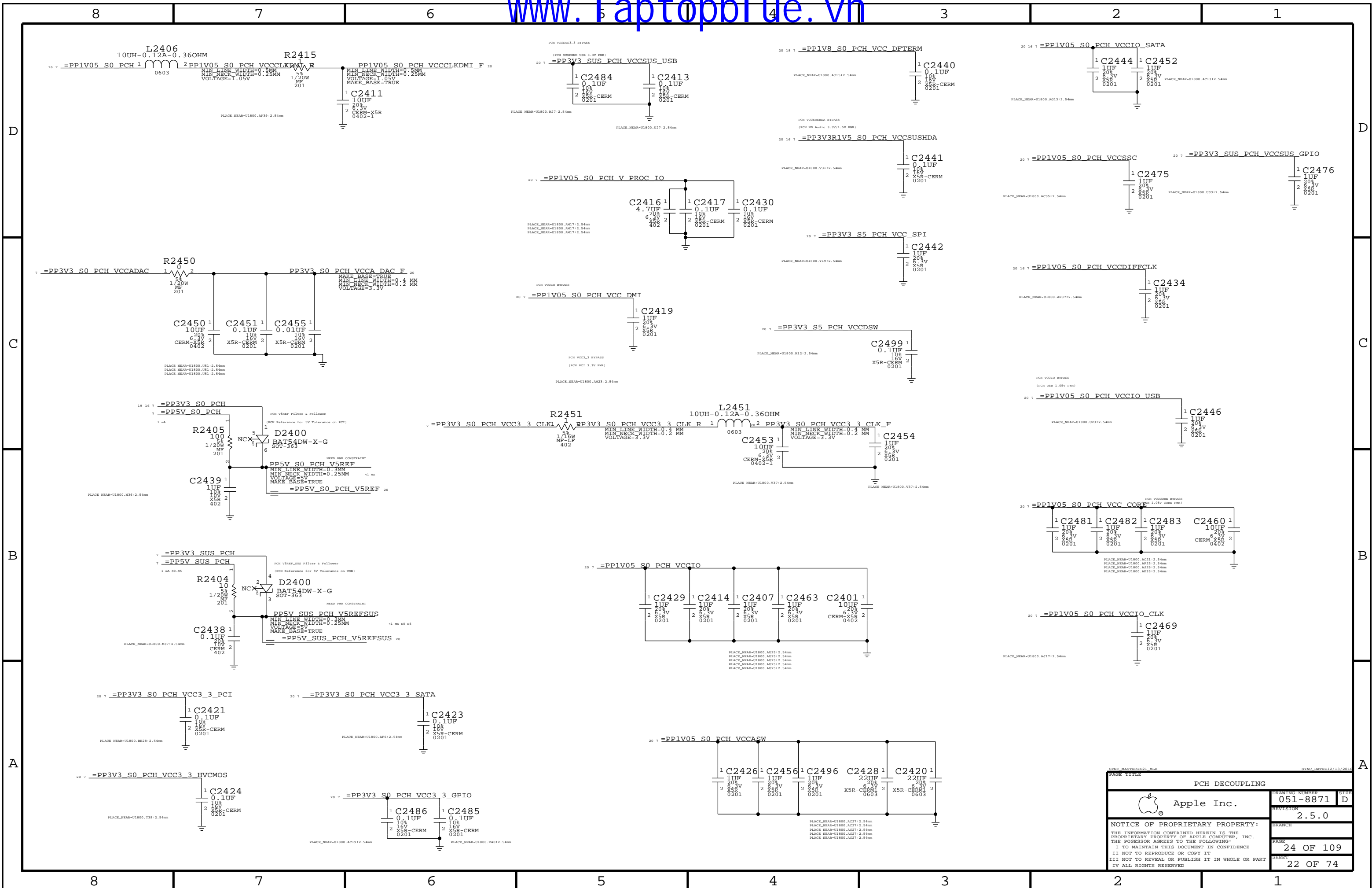
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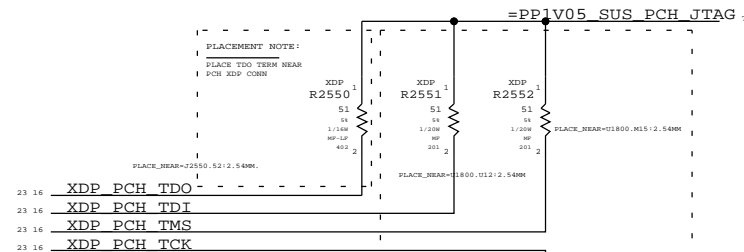
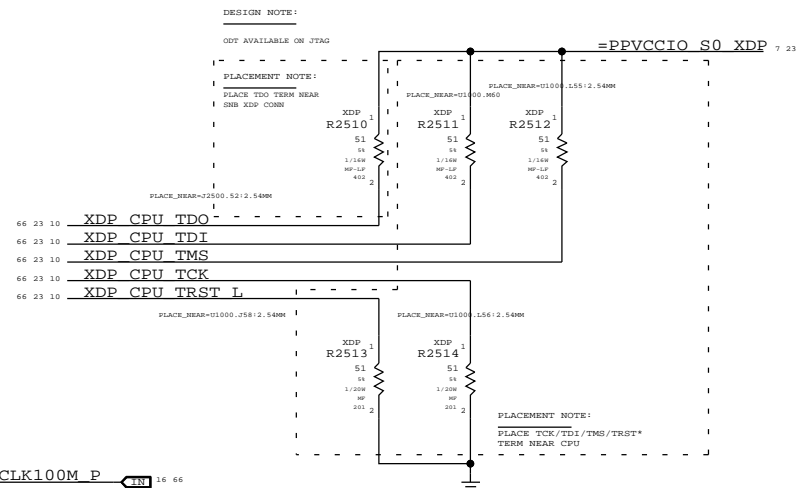
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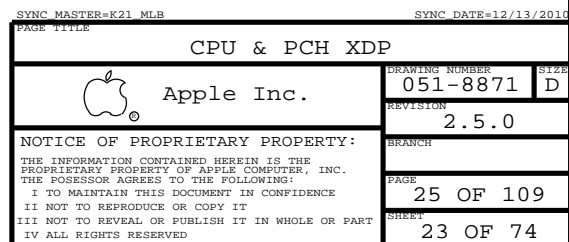
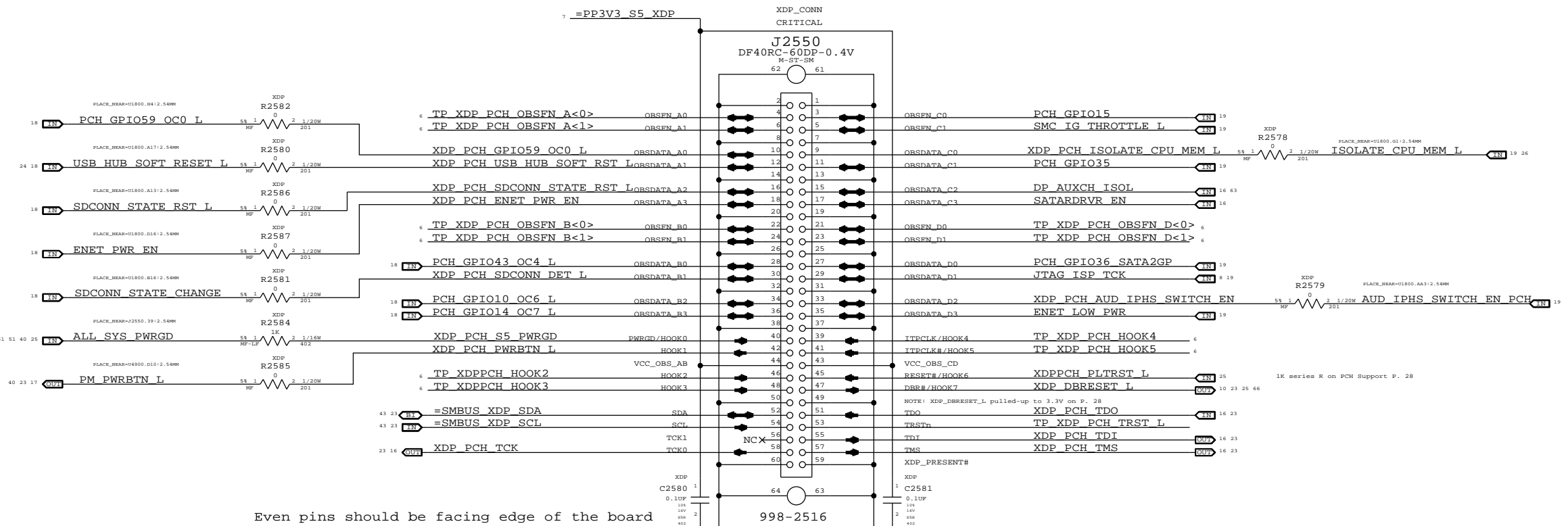
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				21 OF 74			

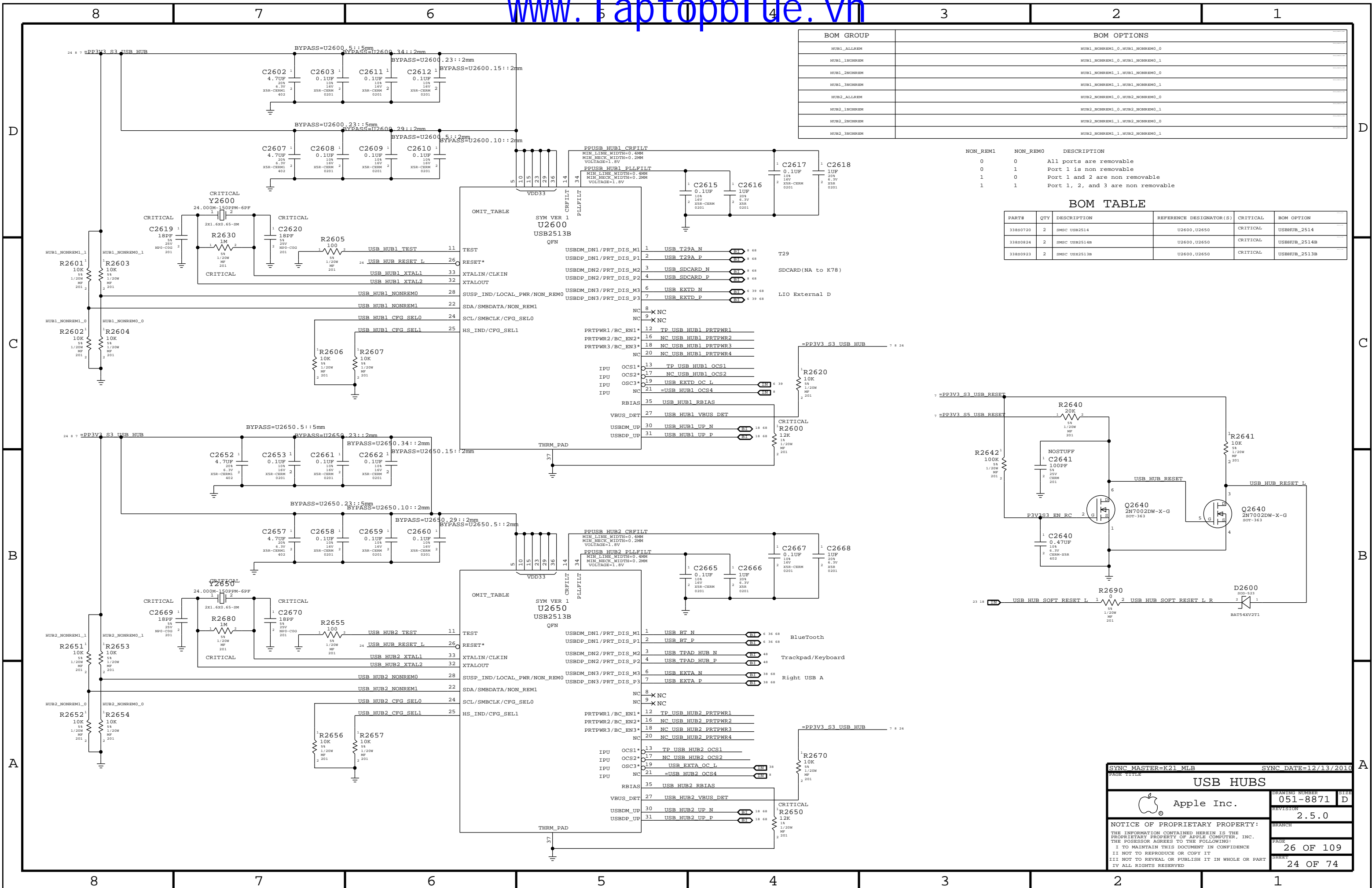


PAGE 11111		PCH DECOUPLING		BYNC-DATE=12/11/2010	
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NOTE: This is not the standard XDP pinout
Use with 920-0782 Adapter Flex to support chipset debug





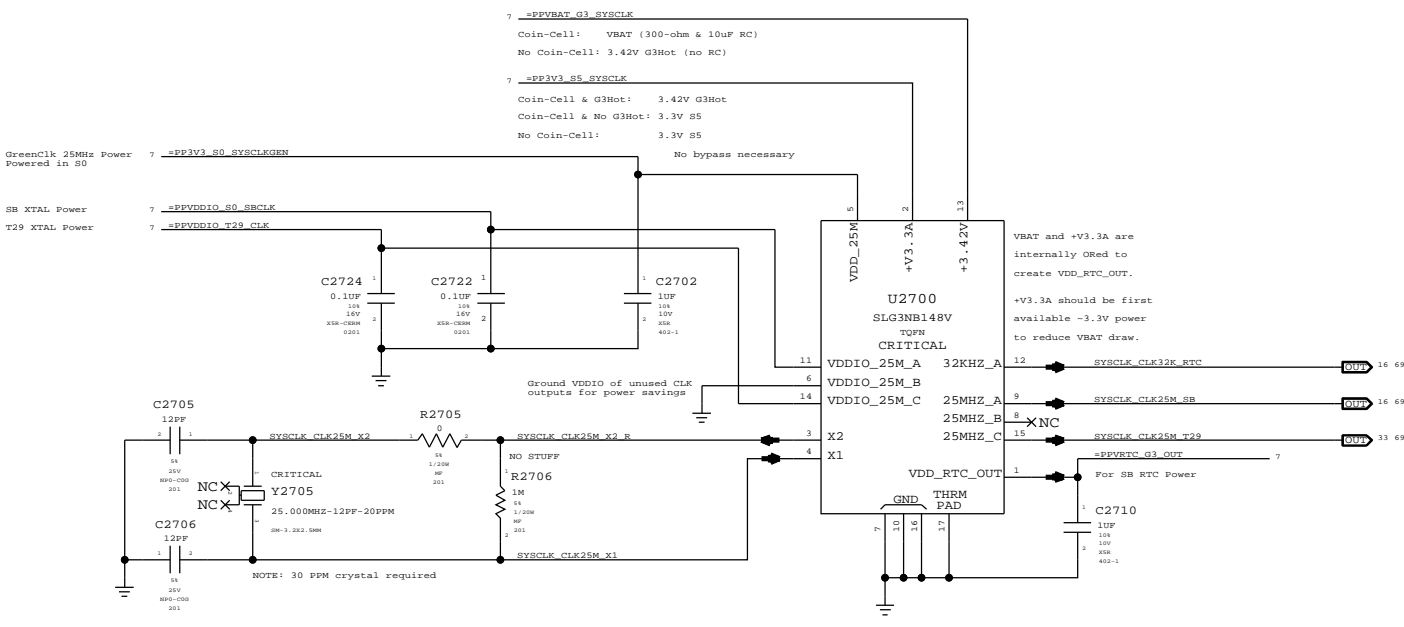
System RTC Power Source & 32kHz / 25MHz Clock Generator

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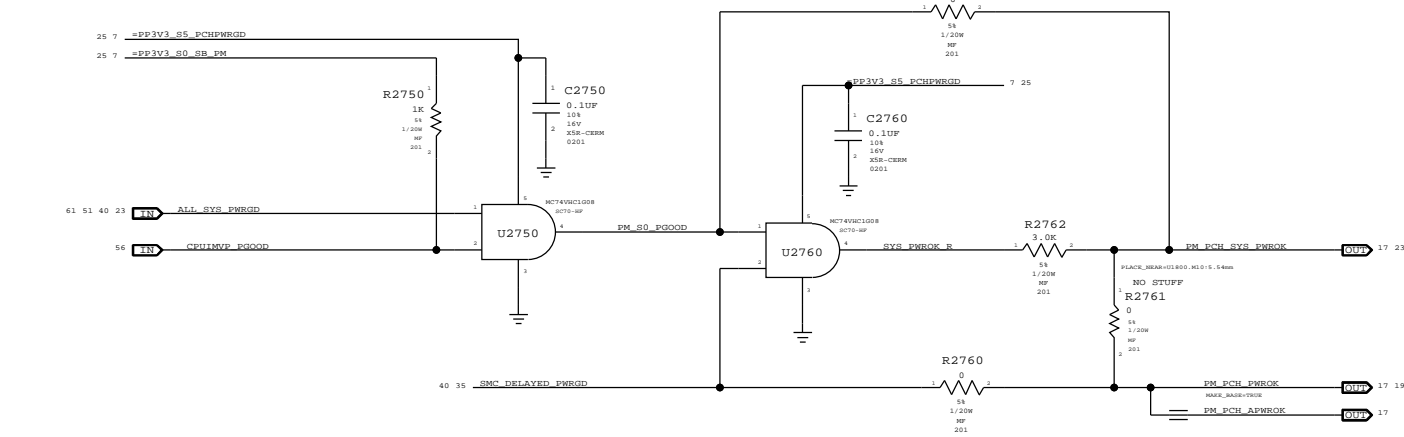
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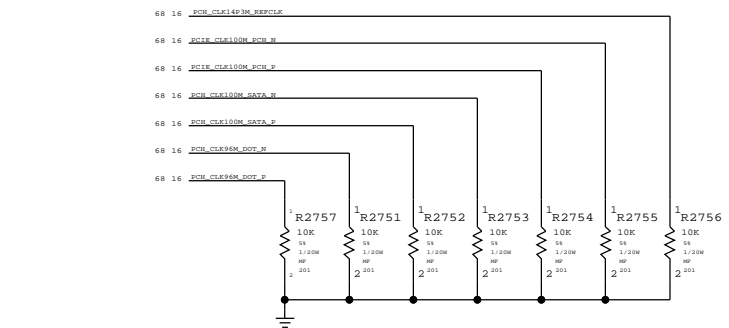


PCH S0 PWRGD

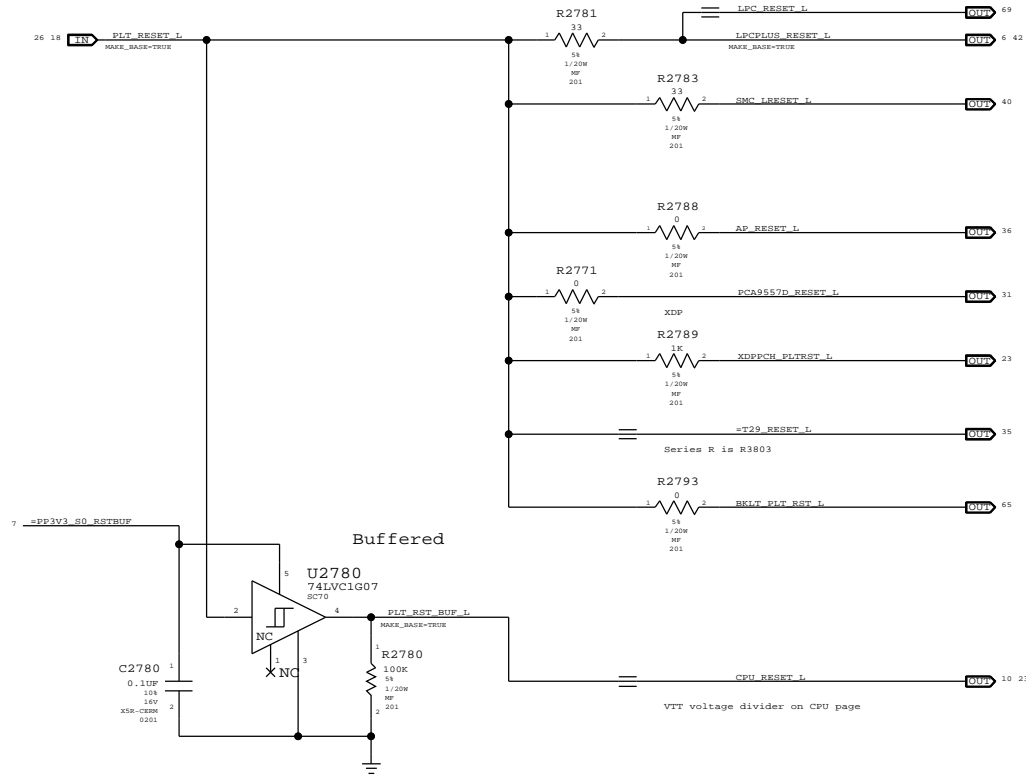


CLOCK (CK505)

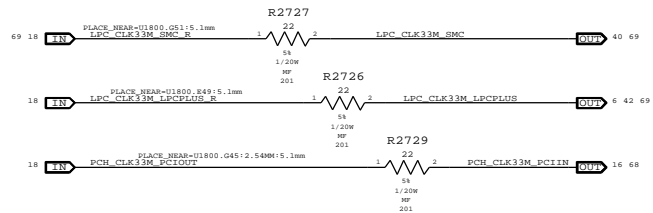
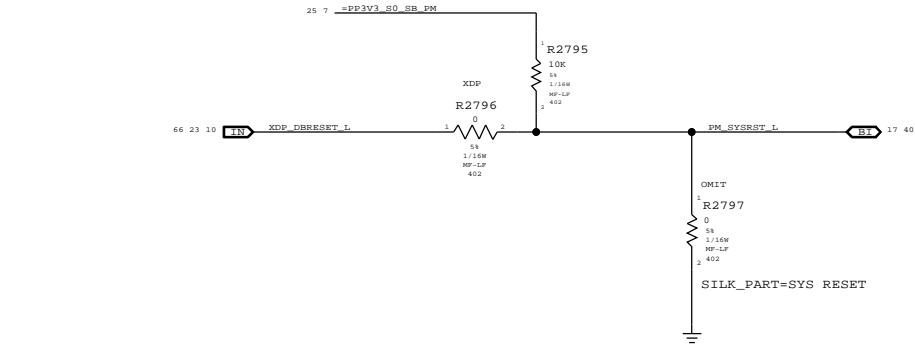
UNUSED clock terminations for PCIM MODE



Platform Reset Connections
Unbuffered



PCH Reset Button



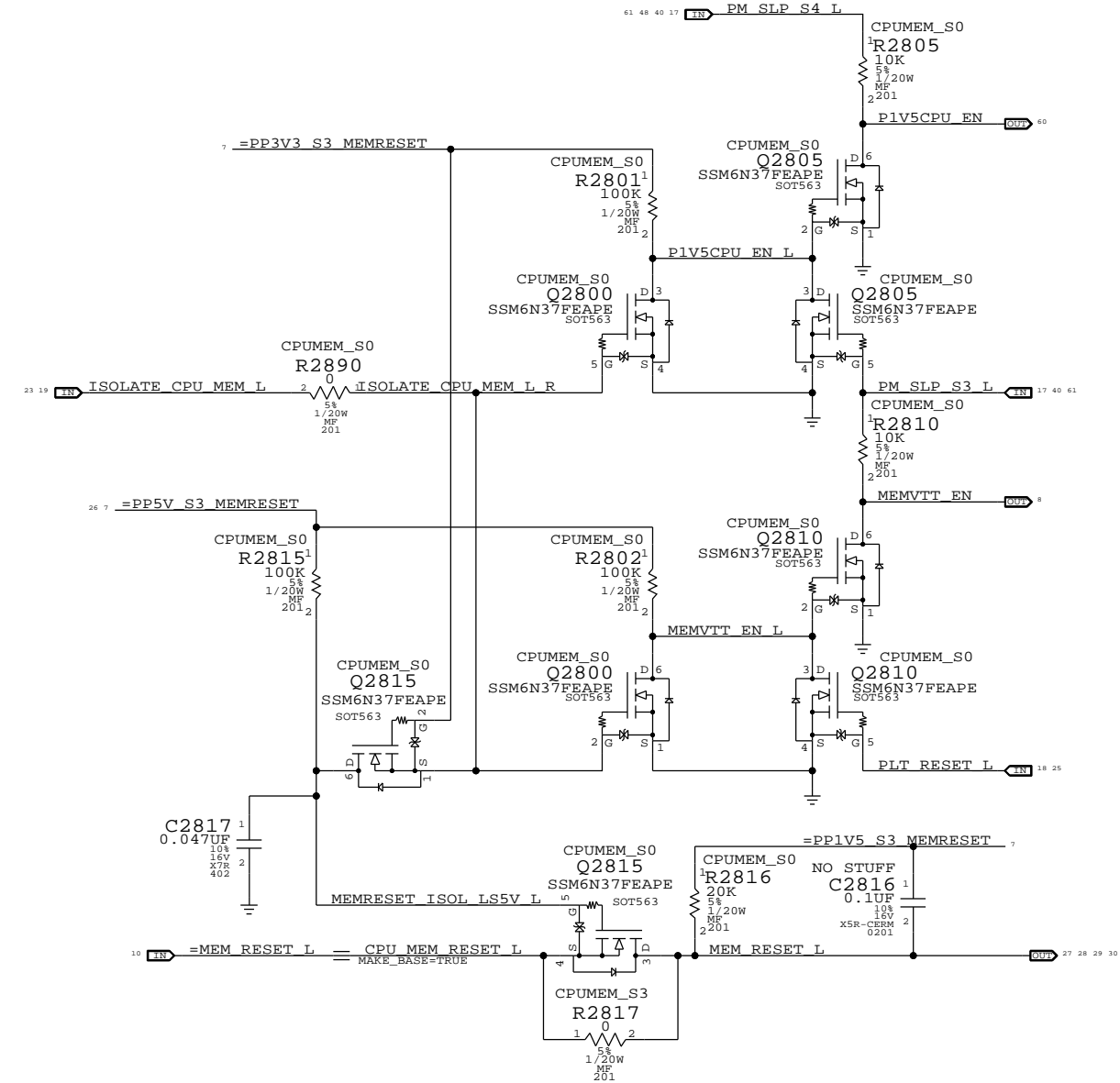
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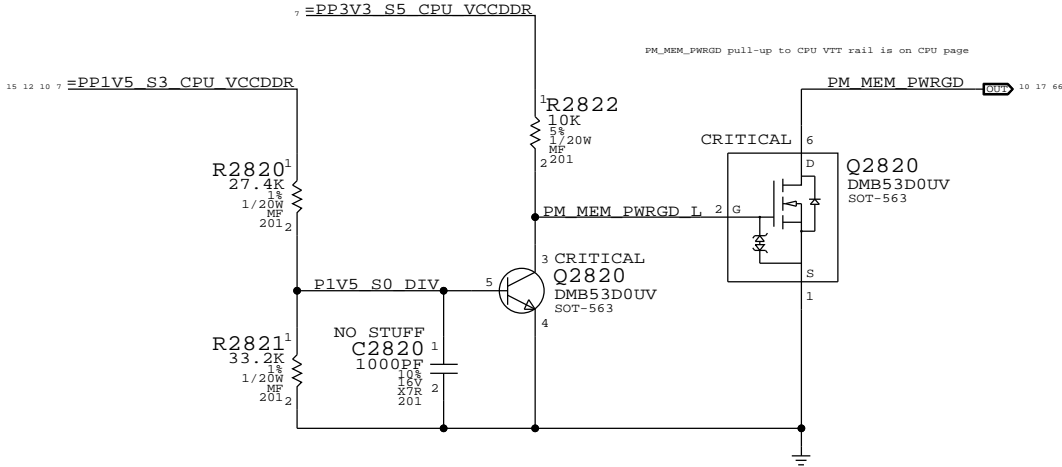
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the S0-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

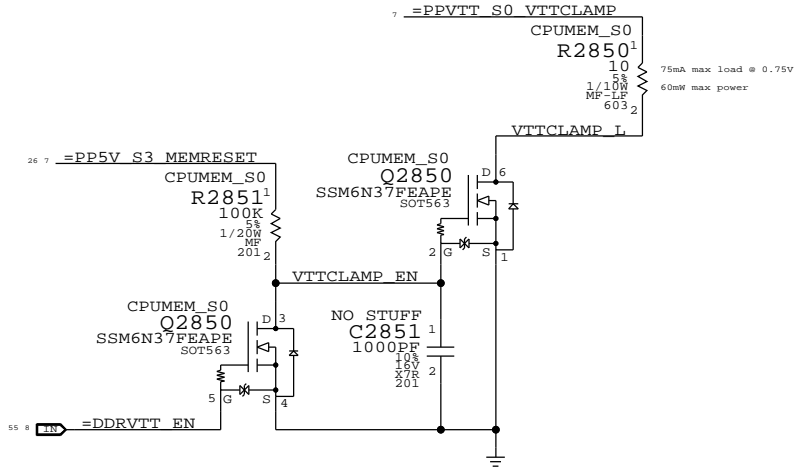


1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

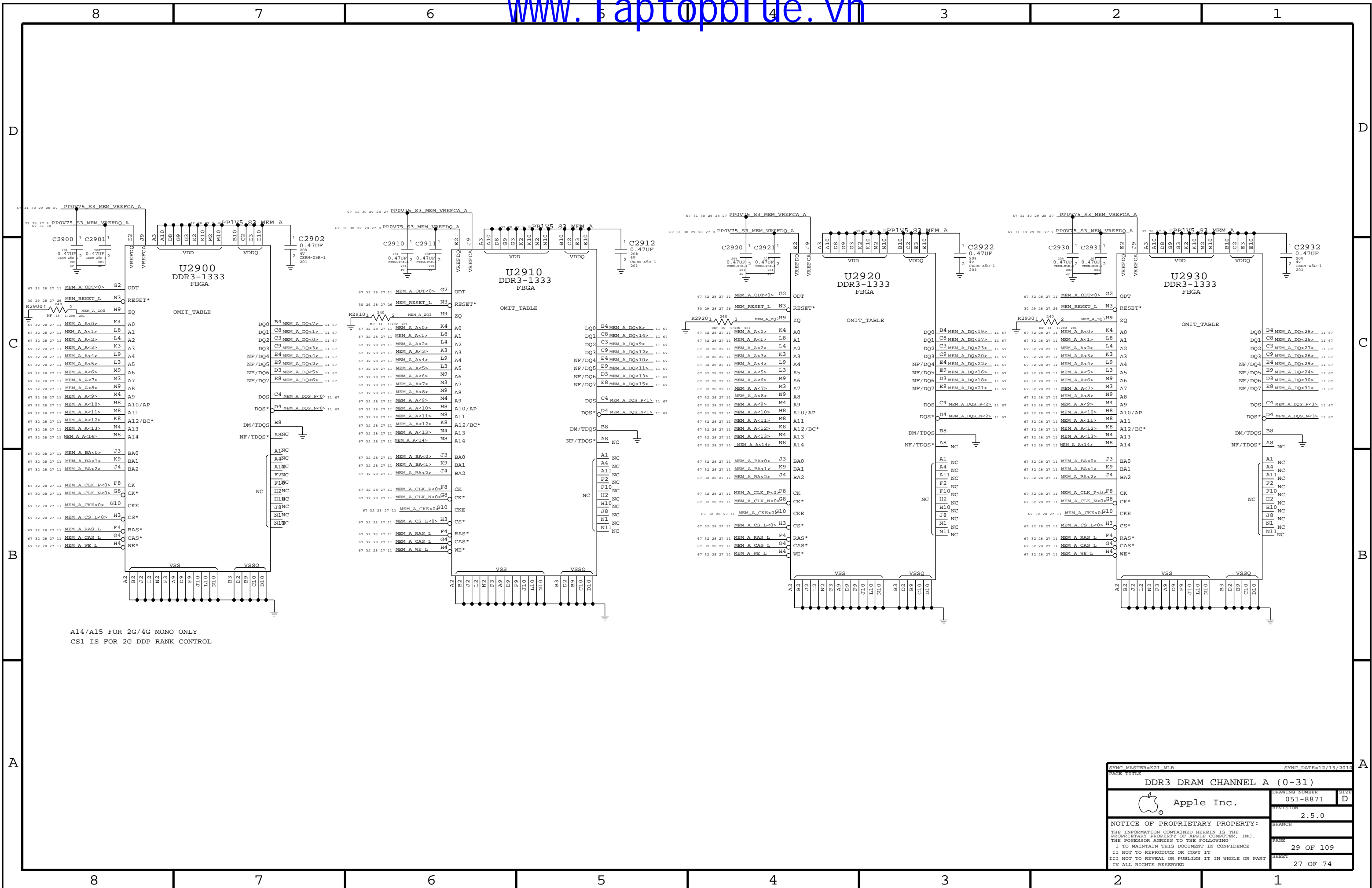
Ensures CKE signals are held low in S3



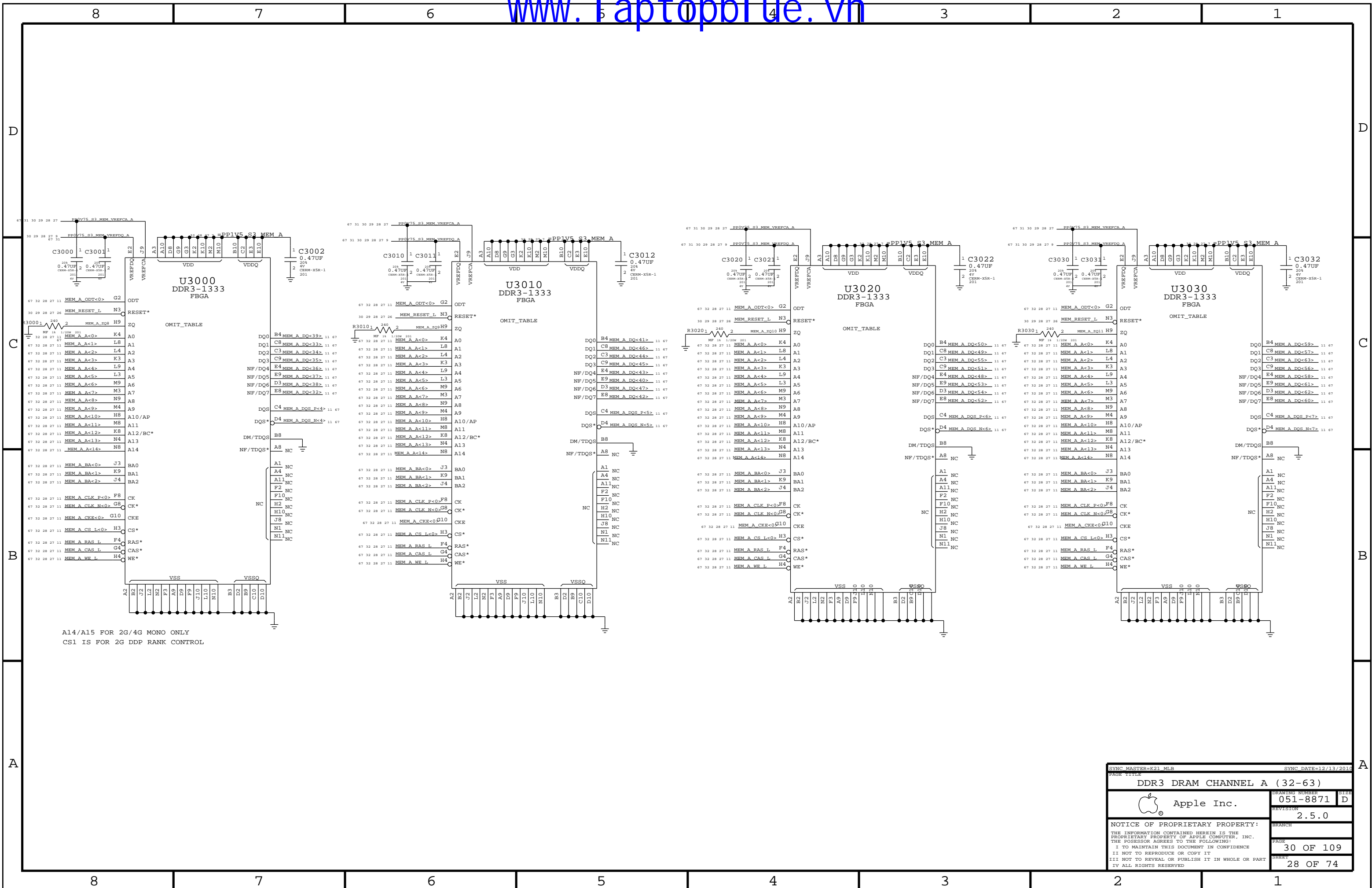
Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1
S3	2	0	0	1	1	0	0	1
to	3	0	0	1	X	0	0	0
S0	4	0	0	1	X	0	0	1
to	5	0	1	1	0 (*)	1	1	1
S0	6	0	1	1	1	1	1	1
	7	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.


NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.



A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL

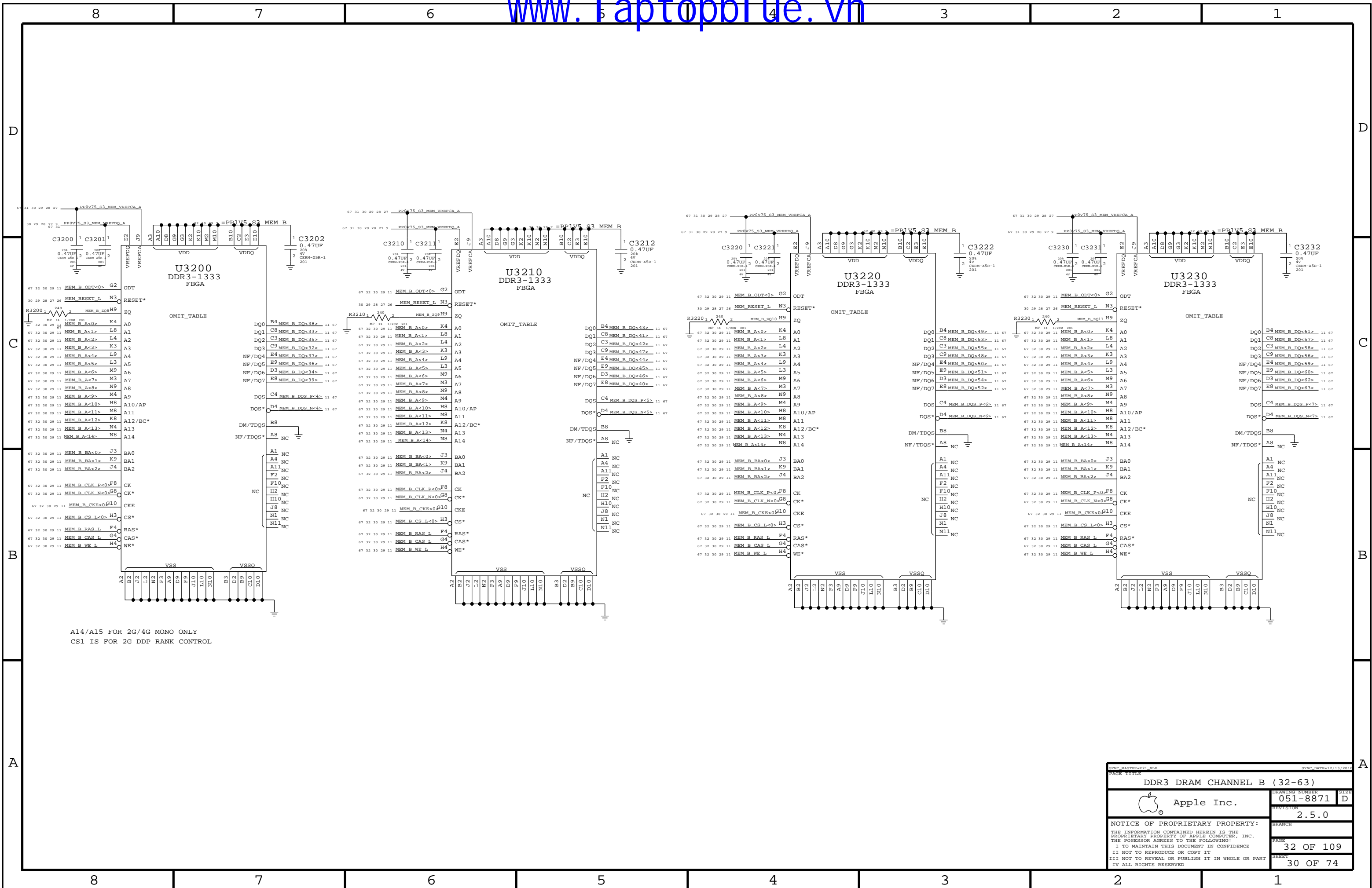


A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL

SYNC MASTER=K21 MLB		SYNC DATE=12/13/2010	
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DDR3 DRAM CHANNEL A (32-63)			
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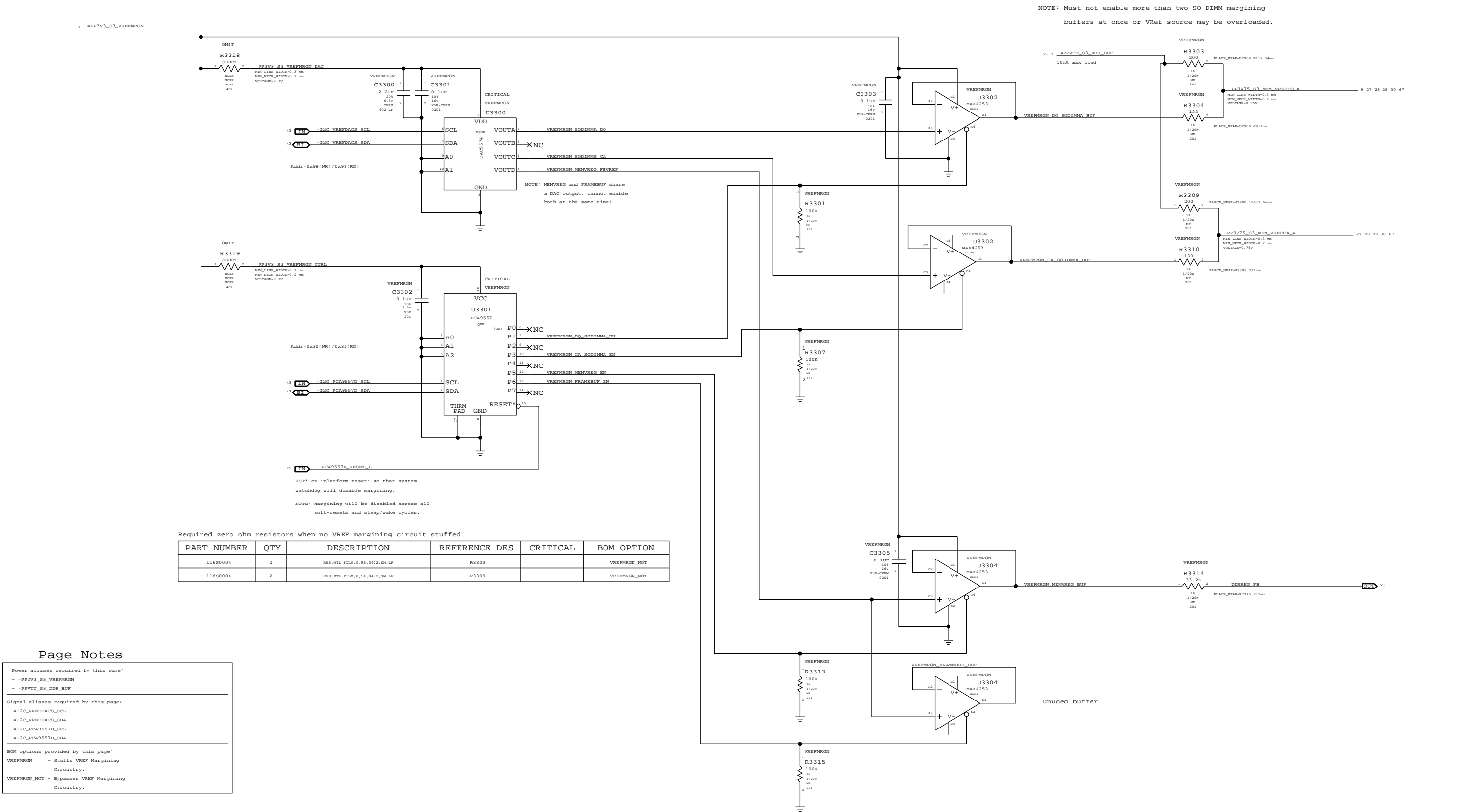
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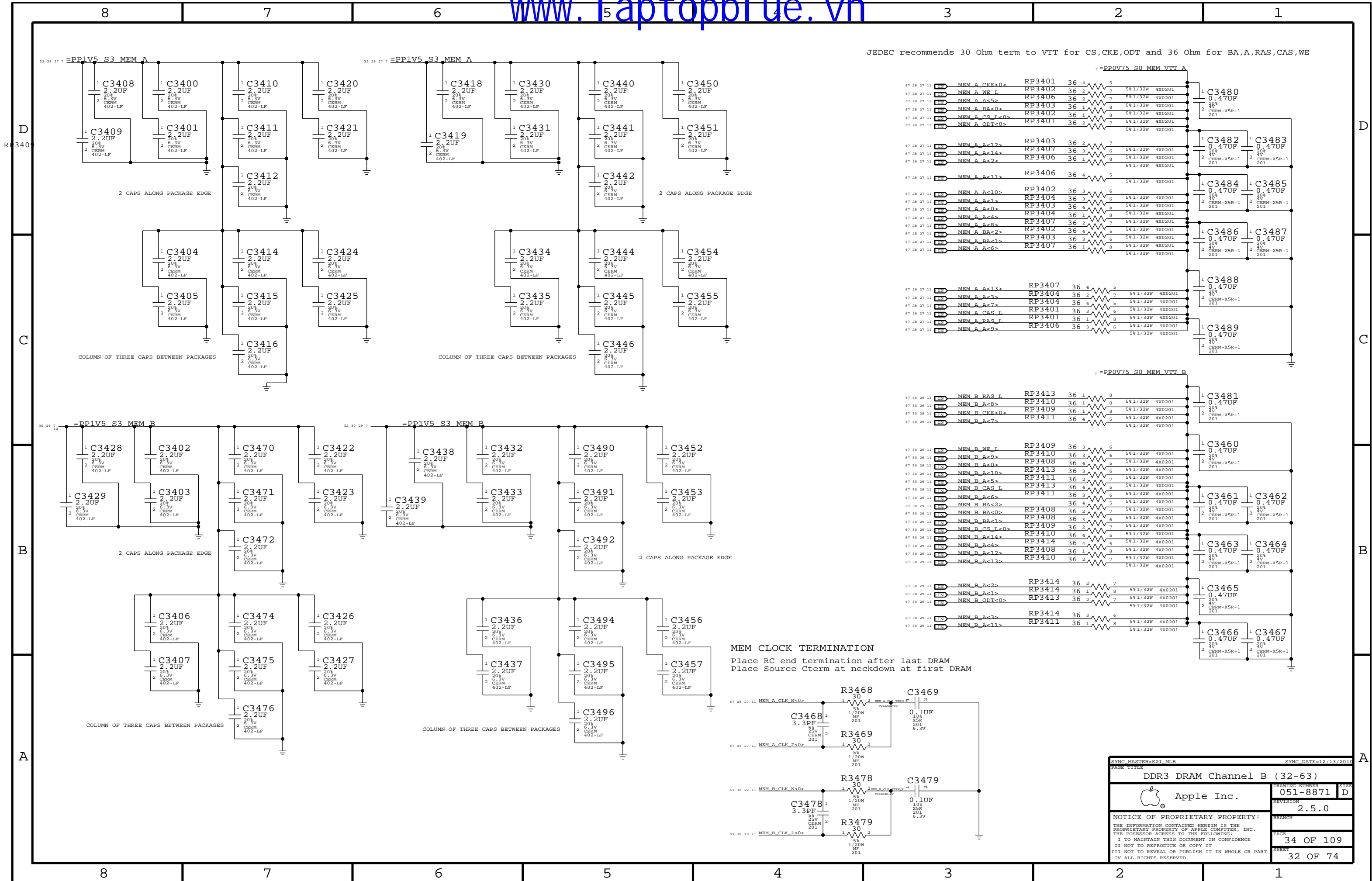
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- =PPVTT_S3_DDR_BUF

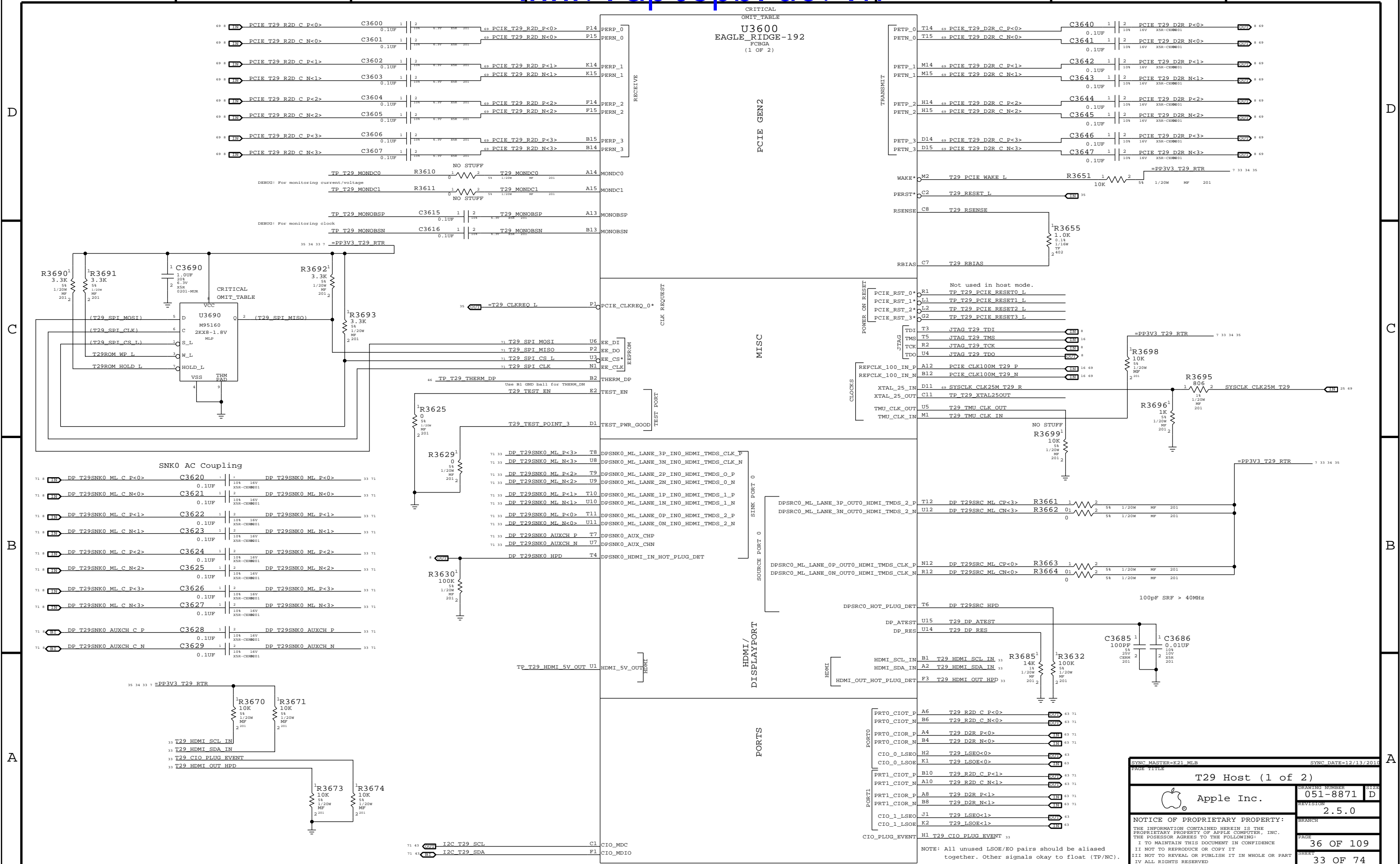
Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

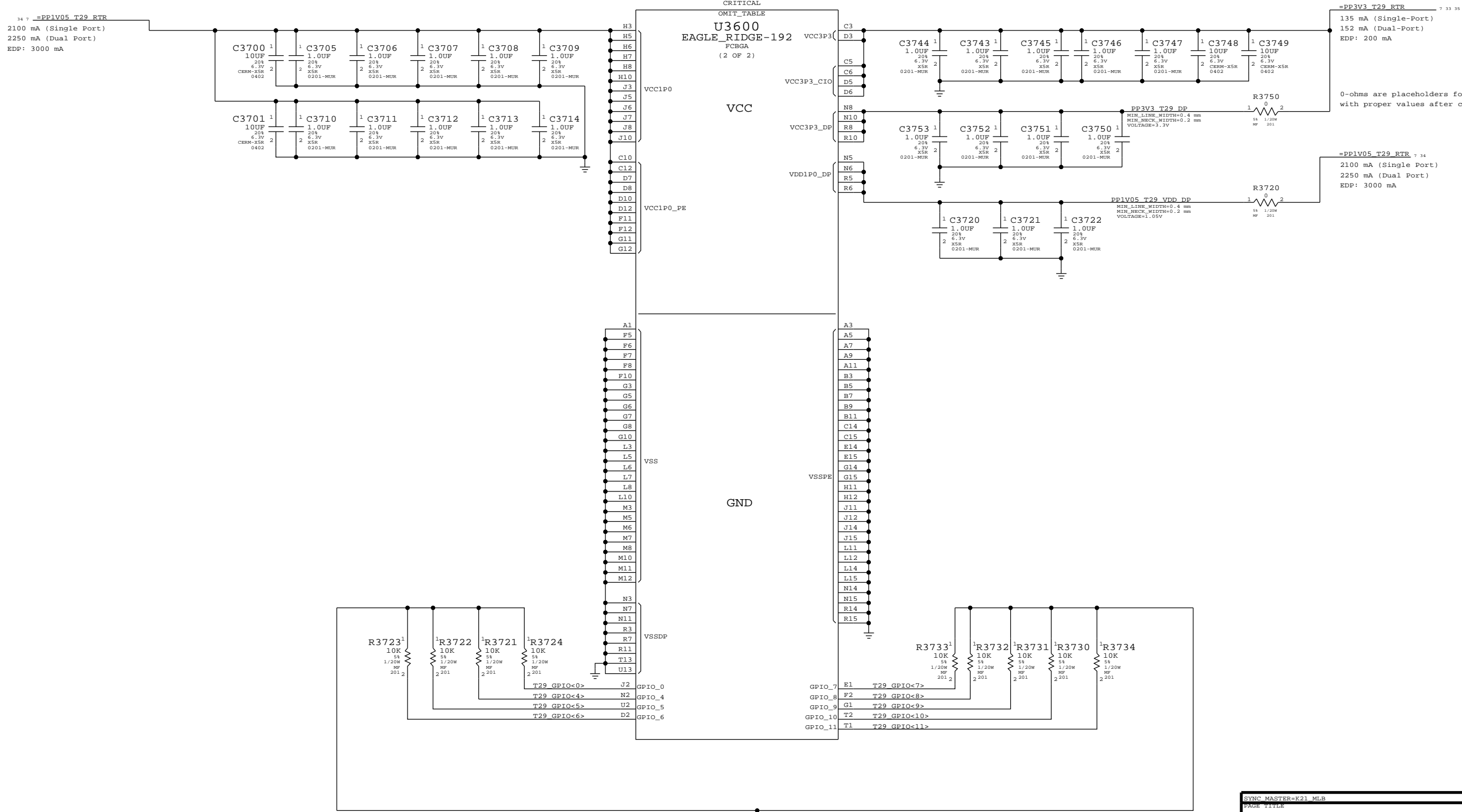
BOM options provided by this page:
VREFMGN - Stuffs VREF Margining Circuitry.
VREFMGN_NOT - Bypasses VREF Margining Circuitry.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% Vref)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value		0.75V (DAC: 0x3A)			1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:		0.300V - 1.200V (+/- 450mV)			1.998V - 1.002V (+/- 498mV)	1.056V - 1.442V (+/- 180mV)
DAC range:		0.000V - 1.501V (0x00 - 0x74)			0.000V - 1.501V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:		+3.4mA - -3.4mA (- = sourced)			+33uA - -33uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:		7.69mV / step @ output			8.59mV / step @ output	1.51mV / step @ output

SYMC MASTER-#21 MCB		SYMC DATE=12/13/2015	
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FSB/DDR3/FRAMEBUF Vref Margining			
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BOM options provided by this page:
T29BST:Y - Stuffs 18V boost circuitry.



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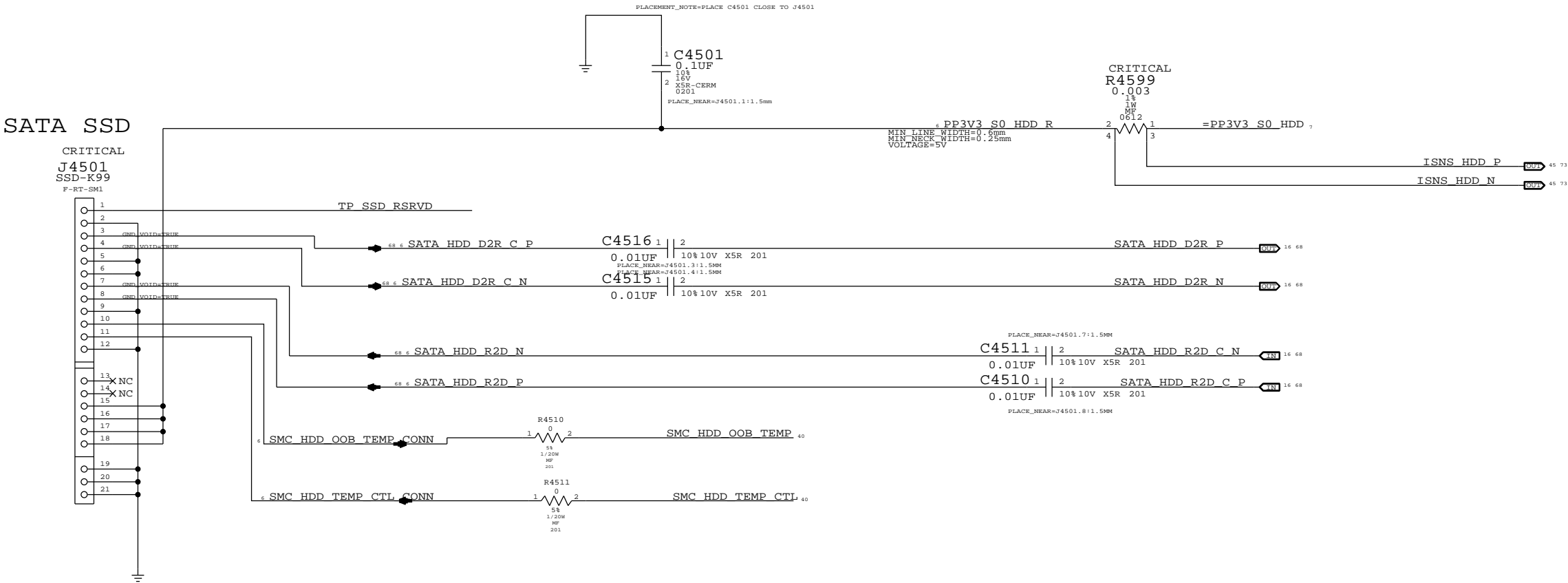


Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

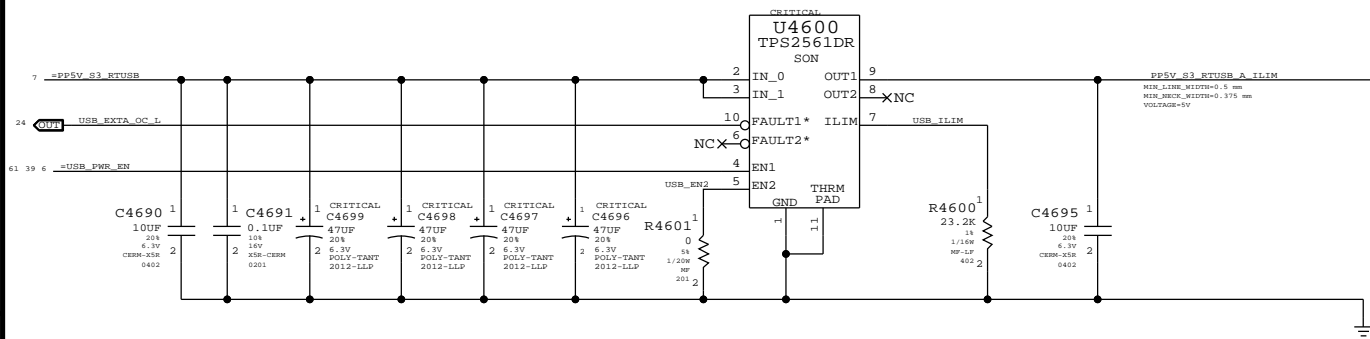
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PAGE 1411LE			
T29 Power Support			
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X21 WIRELESS CONNECTOR			
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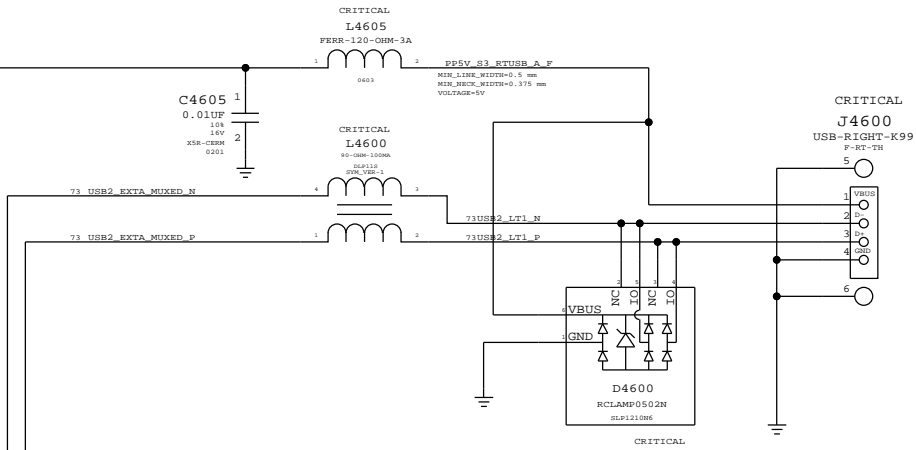


USB Port Power Switch



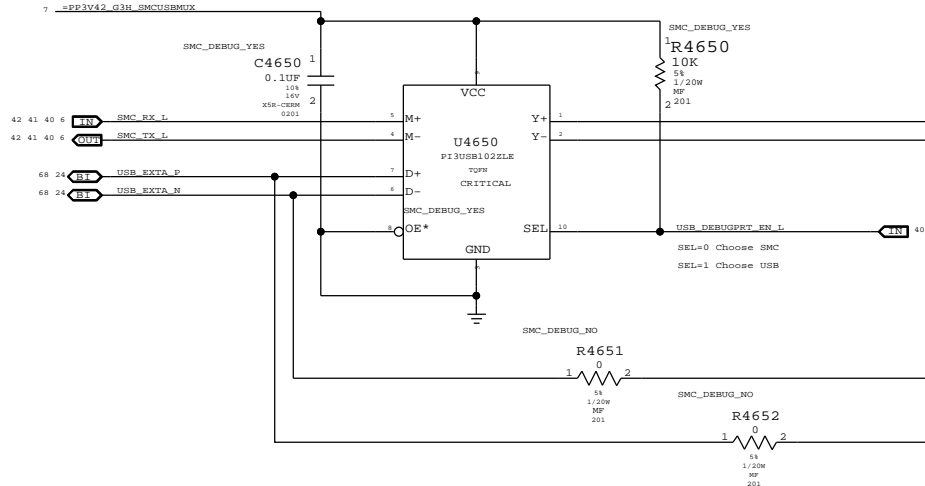
Current limit (R4600): 2.17-2.59A

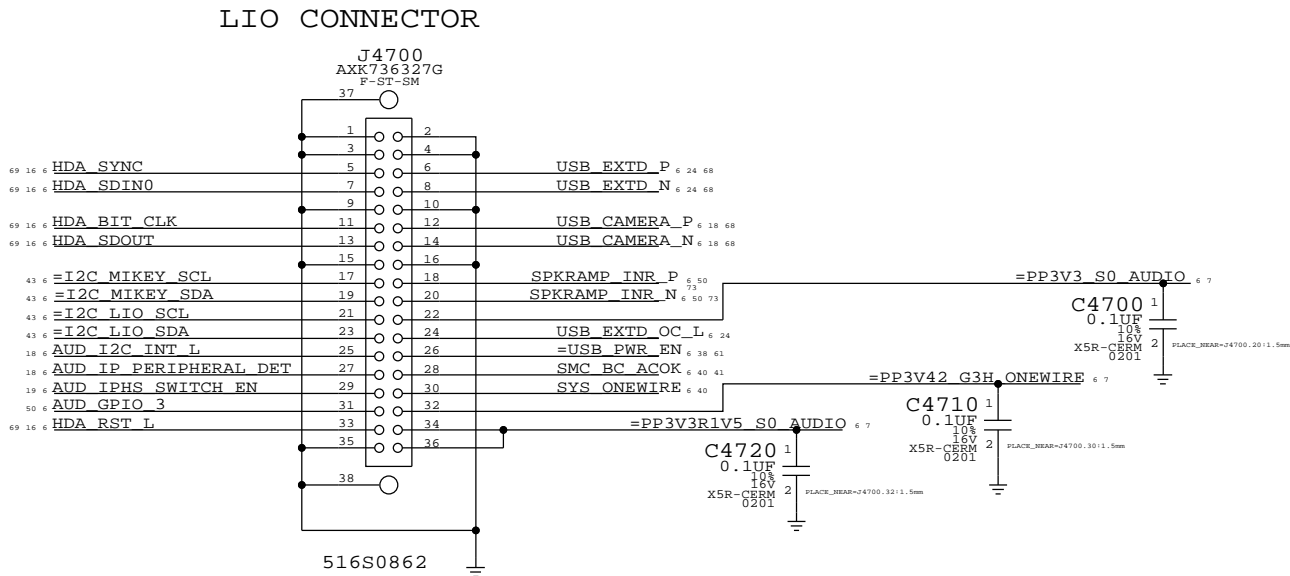
Right USB Port A



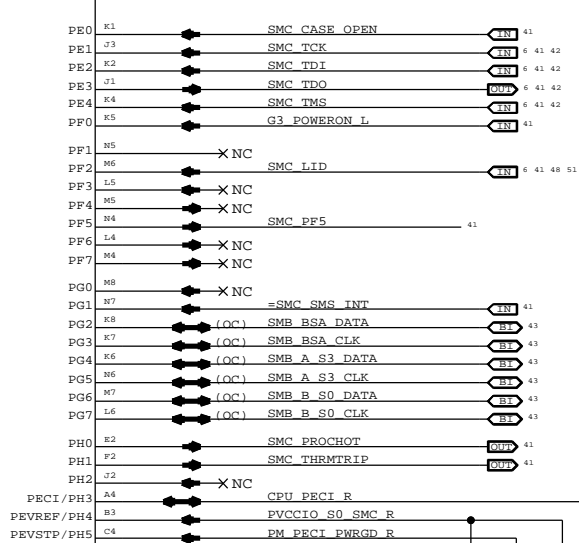
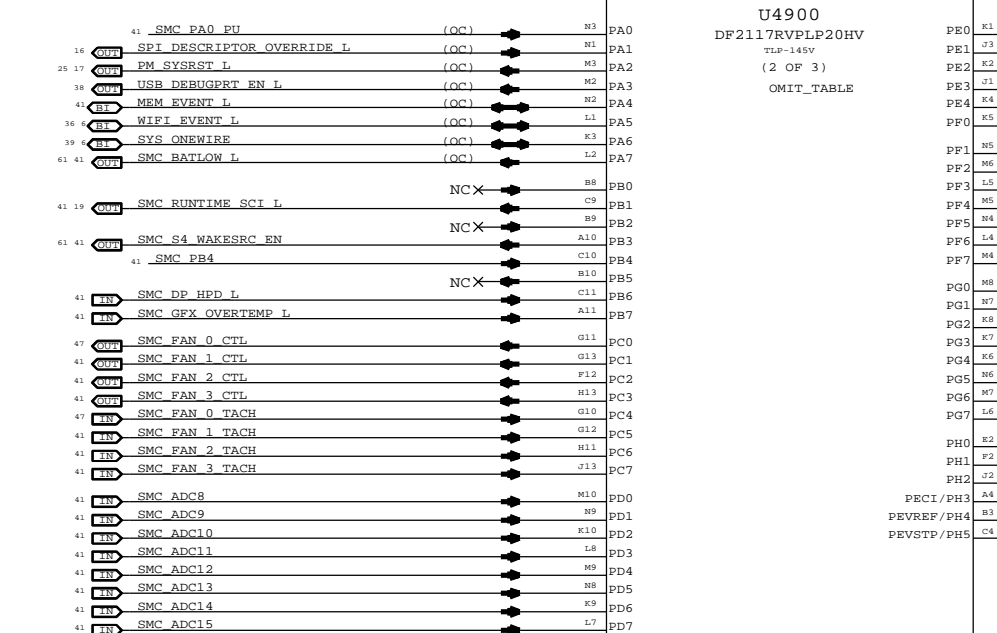
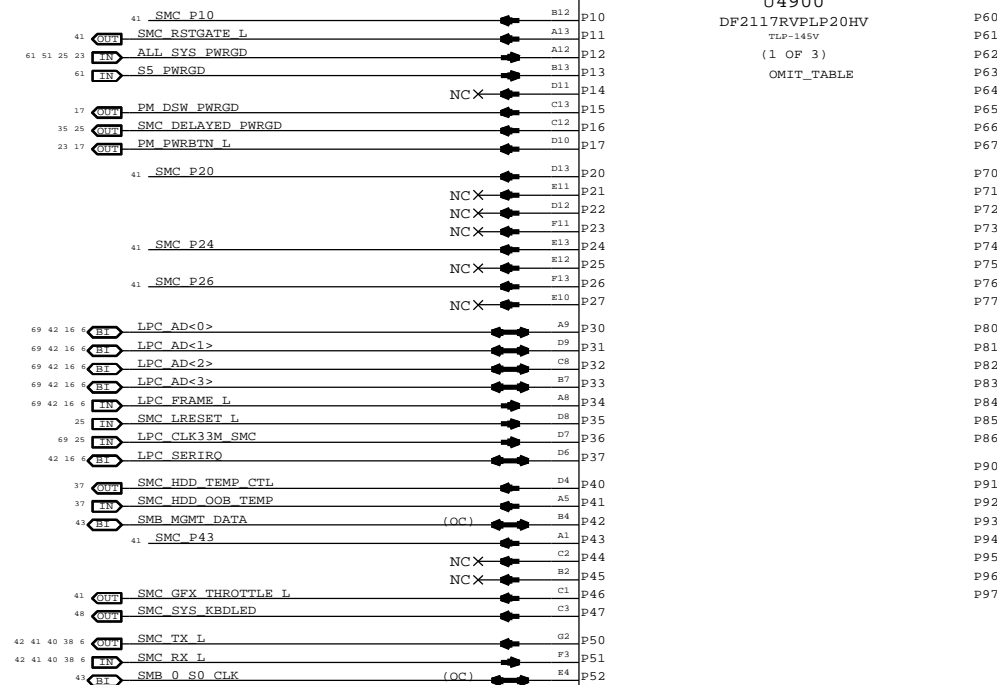
We can add protection to 5V if we want, but leaving NC for now
Place L4605 at connector pin

USB/SMC Debug Mux

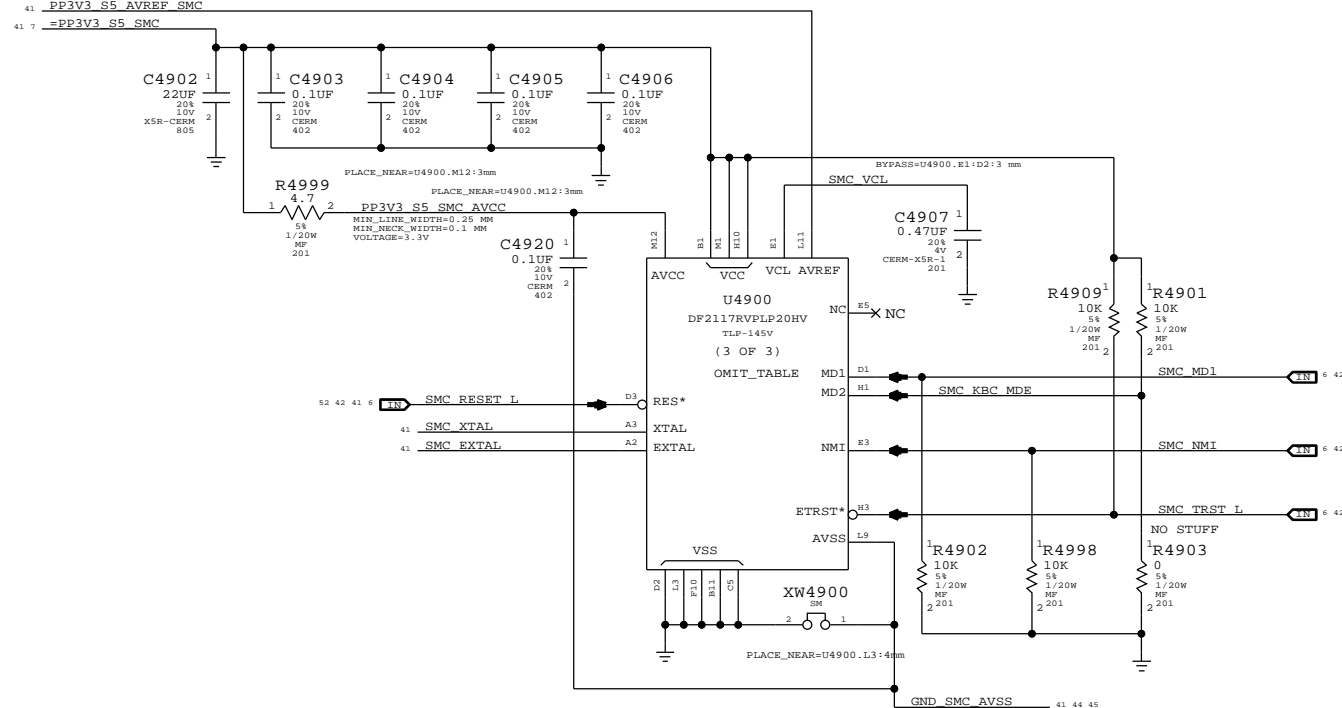
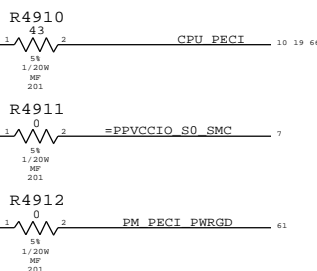
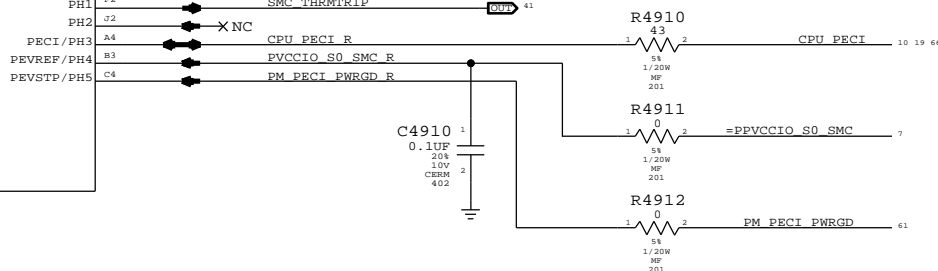




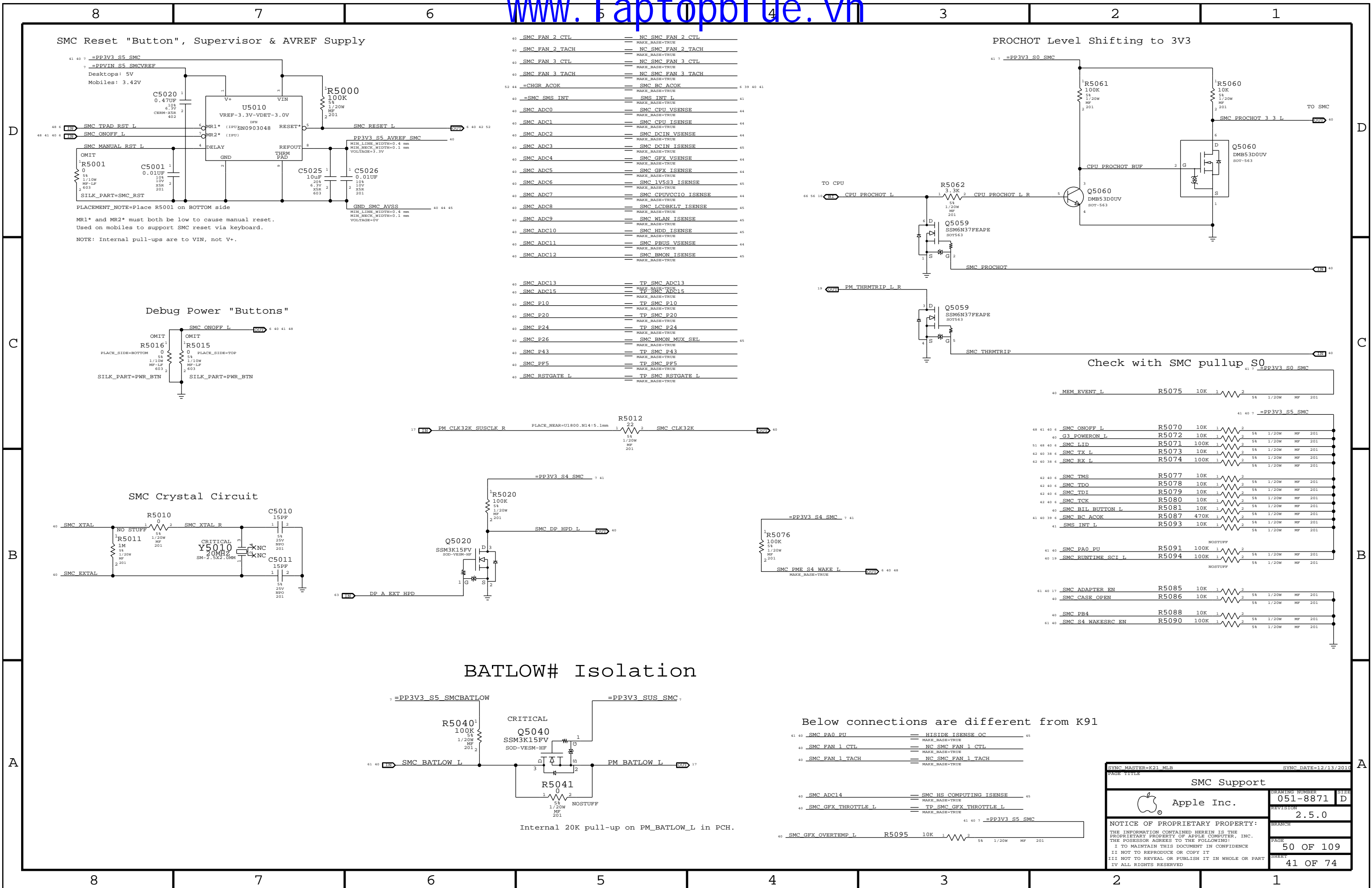
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.



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PAGE TITLE			
SMC		DRAWING NUMBER	SIZE
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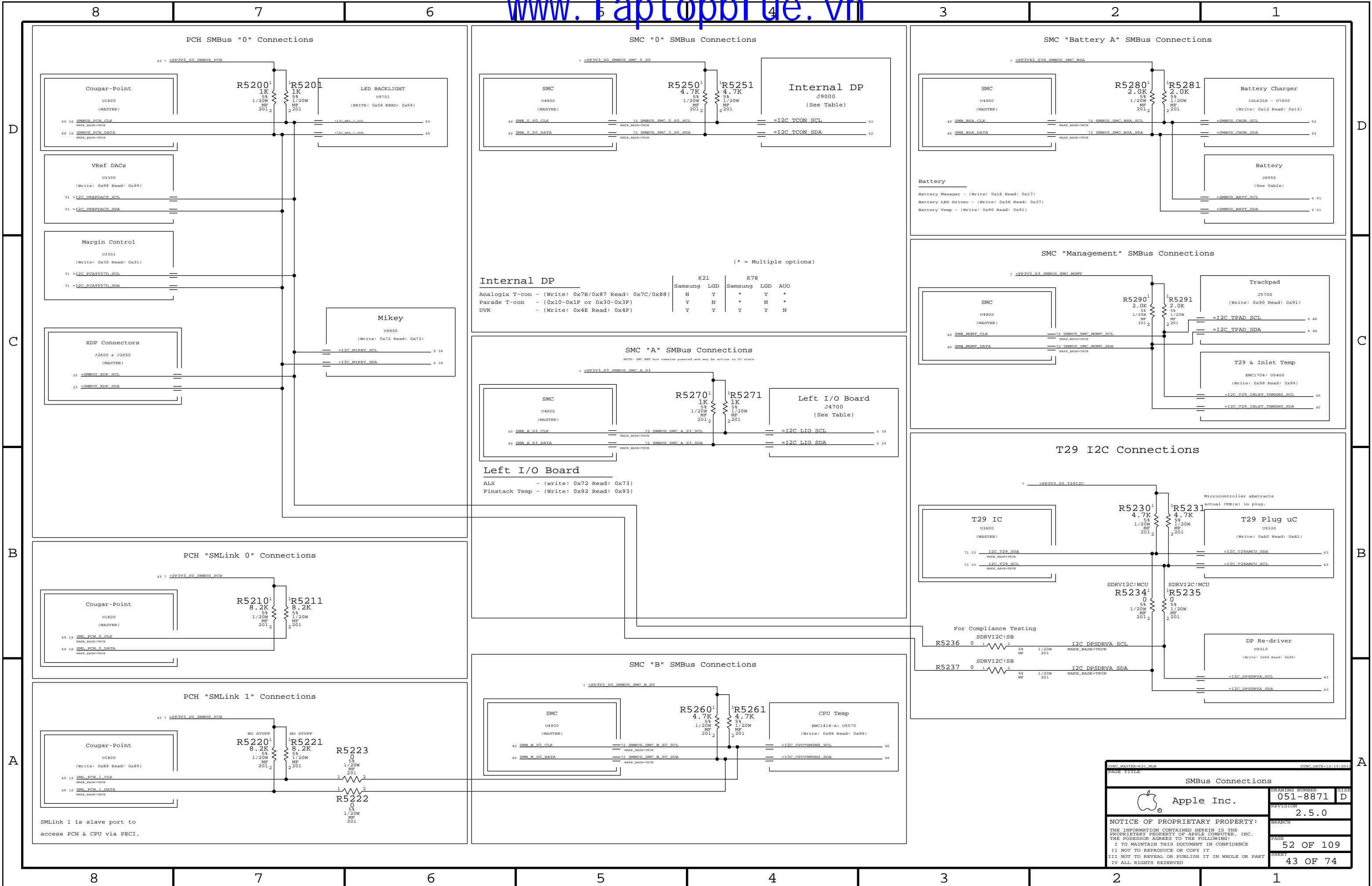


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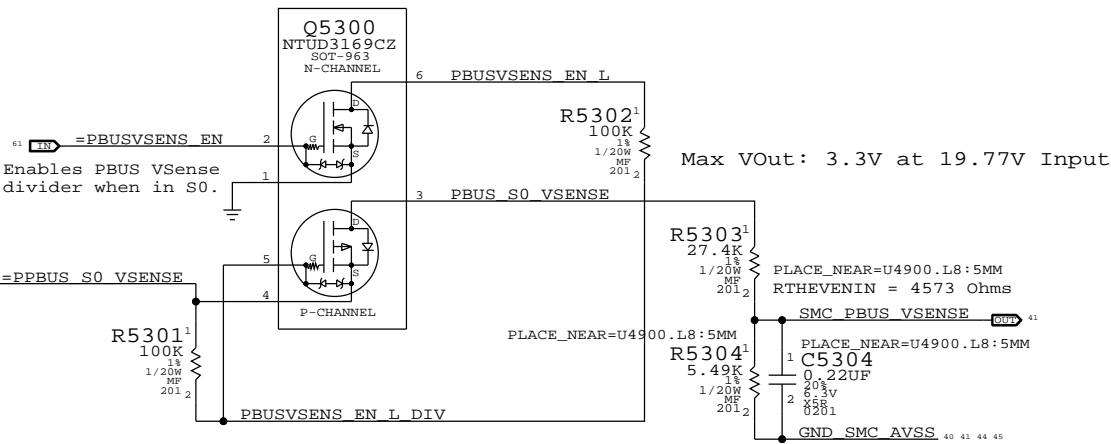


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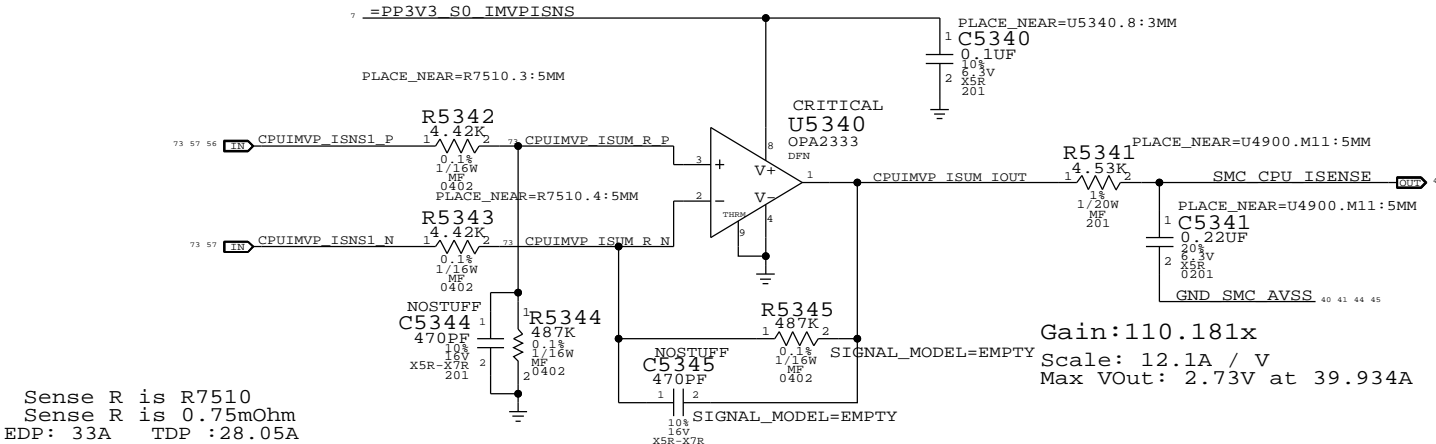




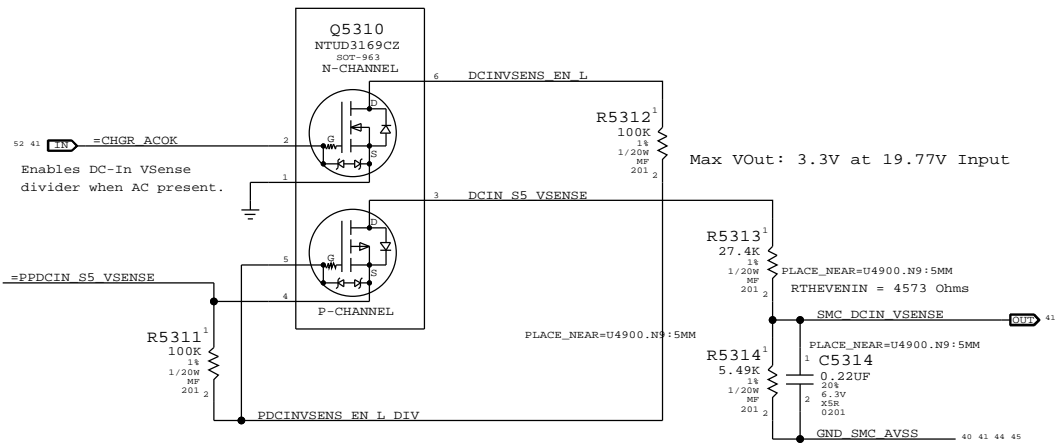
PBUS Voltage Sense Enable & Filter



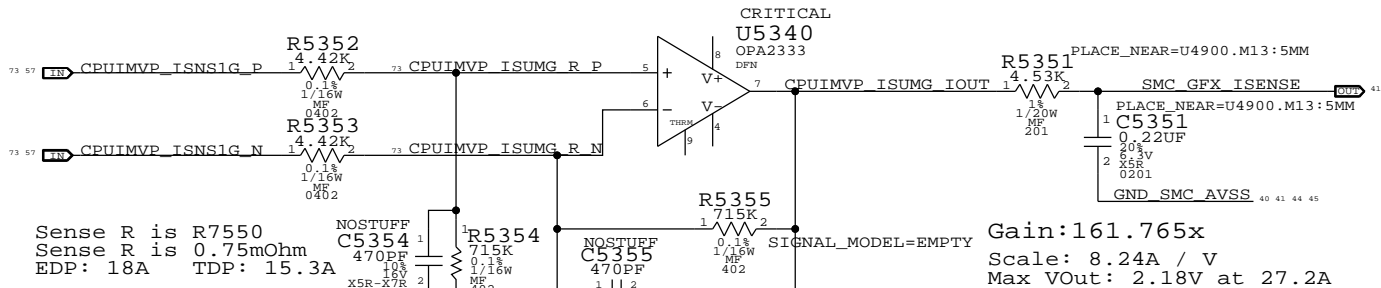
CPU VCore Load Side Current Sense / Filter



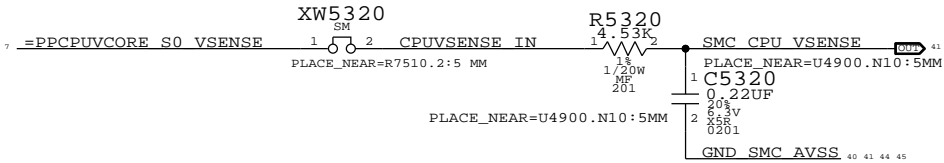
DC-In Voltage Sense Enable & Filter



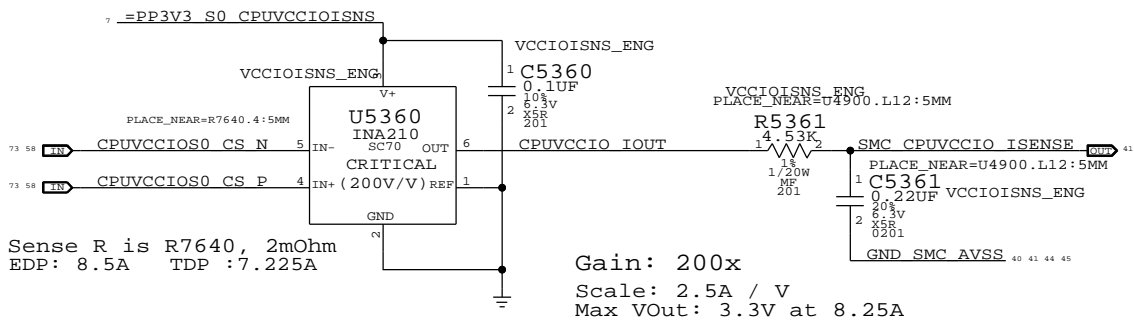
GFX/IG VCore Load Side Current Sense / Filter



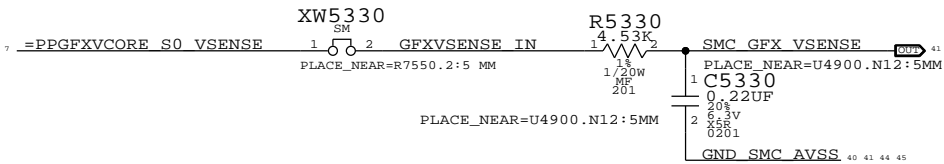
CPU Vcore Voltage Sense / Filter



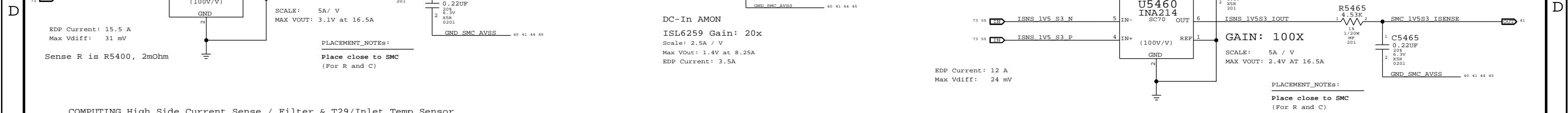
CPU 1.05V VCCIO Current Sense / Filter




GFX/IG Vcore Voltage Sense / Filter



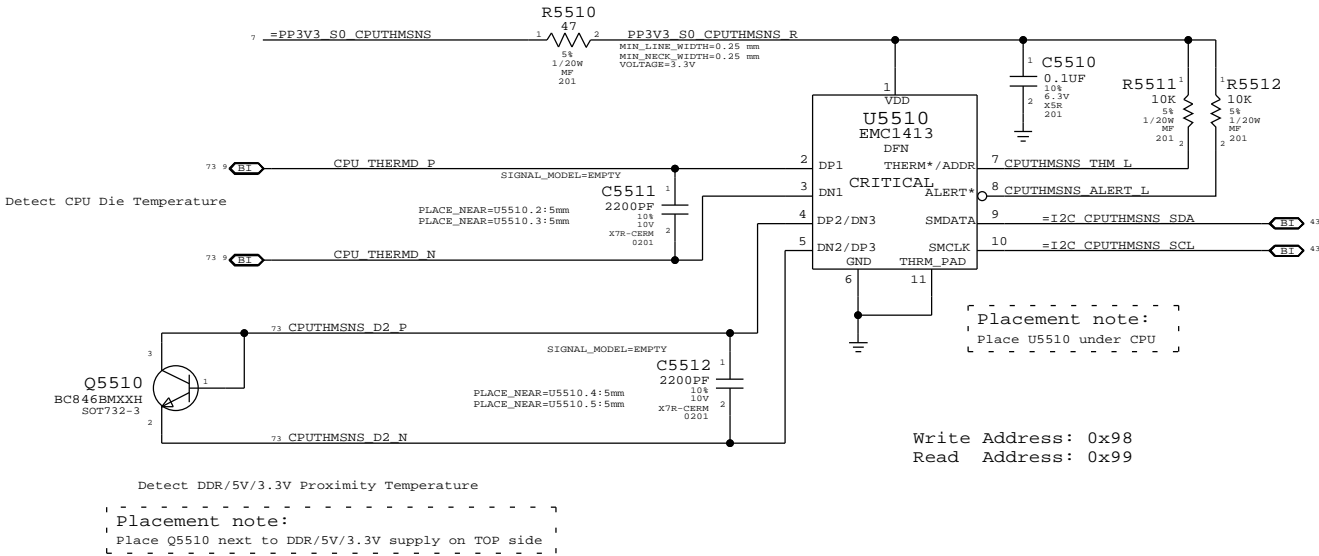
SYNC MASTER=K21 MLB		SYNC DATE=12/13/2010	
Voltage & Load Side Current Sensing		DRAWING NUMBER	051-8871
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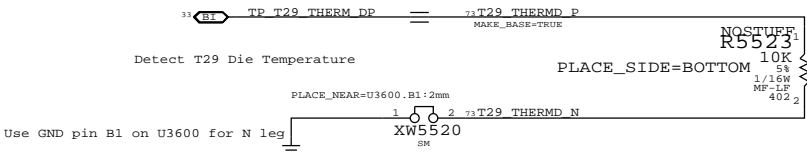
Charger BMON (Production) Solution
ISL6259 Gain: 36x
Scale: 2.78A / V
Max VOut: 3.3V at 9.167A
EDP Current: 310A

SYNCH MASTER-#211 MCB		SYNCH DATE-12/11/2014	
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High Side Current Sensing			
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CPU Proximity Sensor



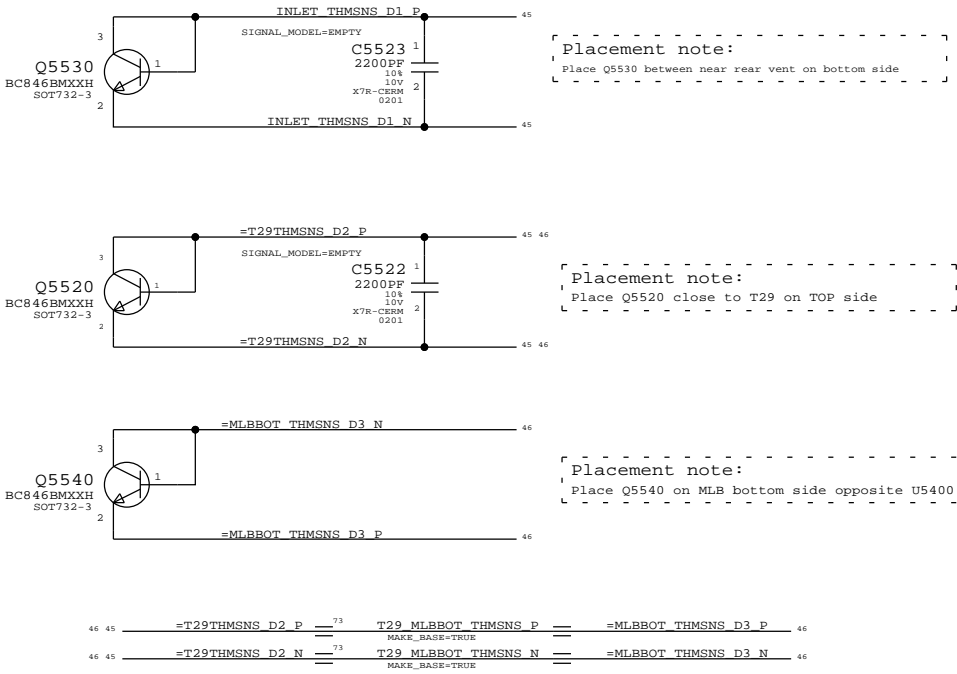
T29 Die




PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MP,1/20W,100K OHM,5,0201,0ND	C5361		VCCIOISNS_PROD
117S0008	1	RES,MP,1/20W,100K OHM,5,0201,0ND	C5475		AIRPORTISNS_PROD
117S0008	1	RES,MP,1/20W,100K OHM,5,0201,0ND	C5485		HDDISNS_PROD
117S0008	1	RES,MP,1/20W,100K OHM,5,0201,0ND	C5495		LCDBKLTISNS_PROD

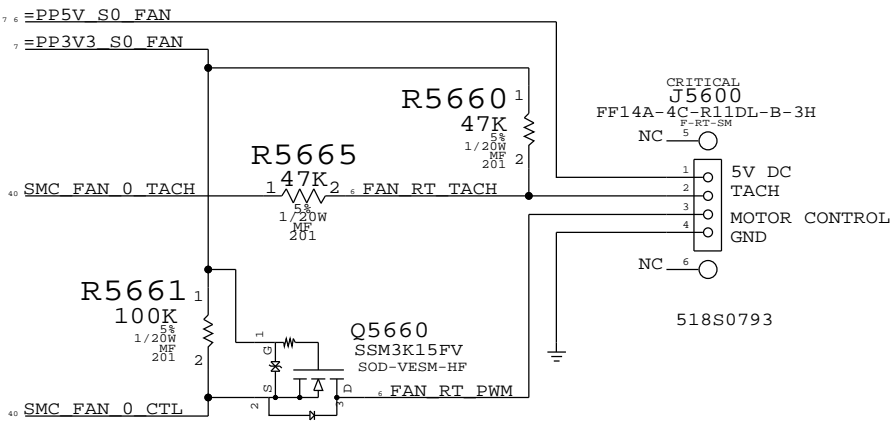
Replacing caps with 100K PD on ISENSE SMC inputs

T29,MLB Bottom & Inlet Proximity Sensors

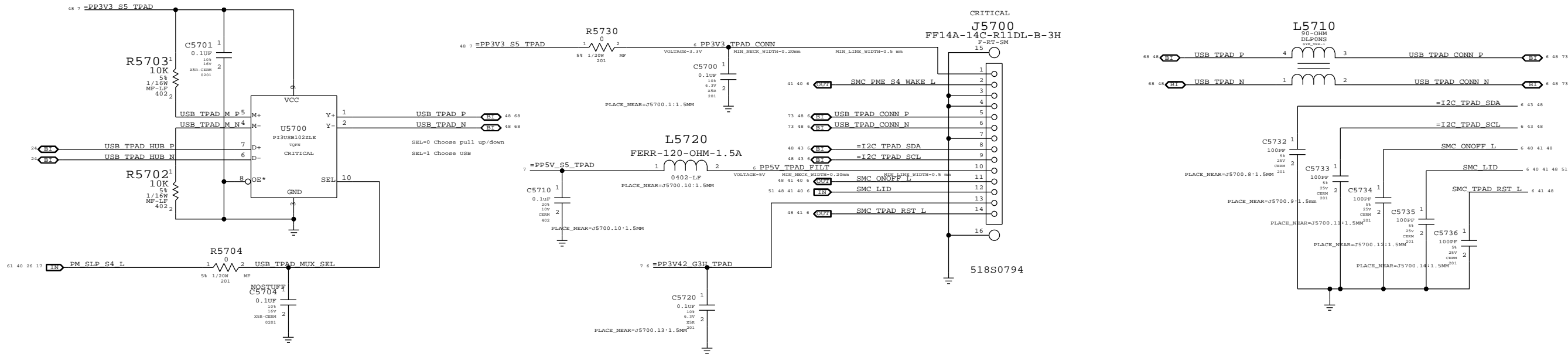


SYNC MASTER=K21_MLB		SYNC DATE=12/13/2010	
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Thermal Sensors			
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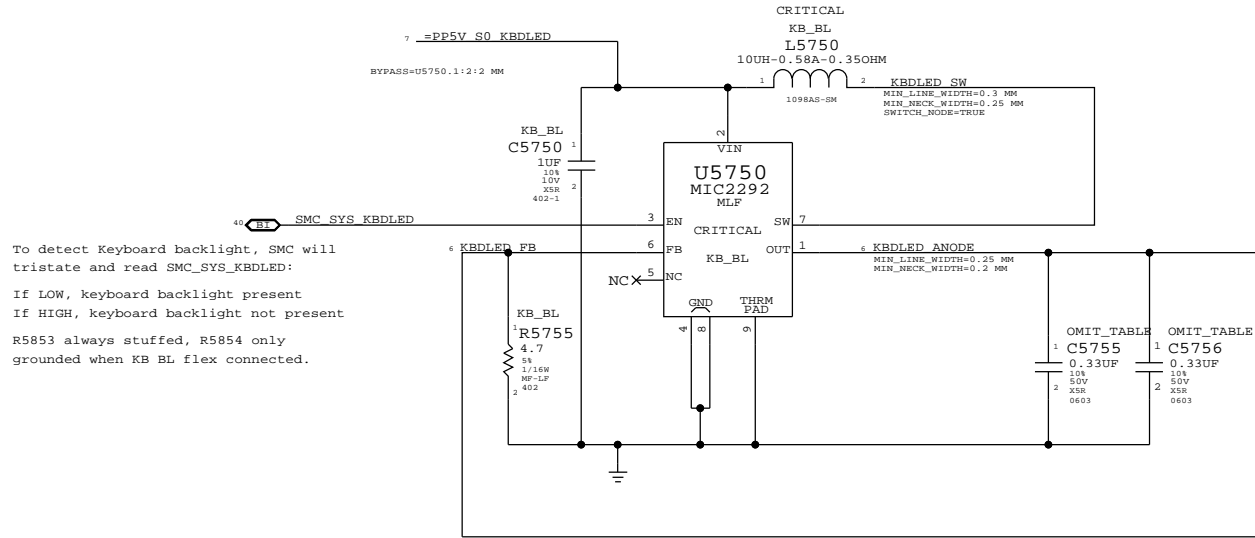
FAN CONNECTOR



IPD Flex Connector

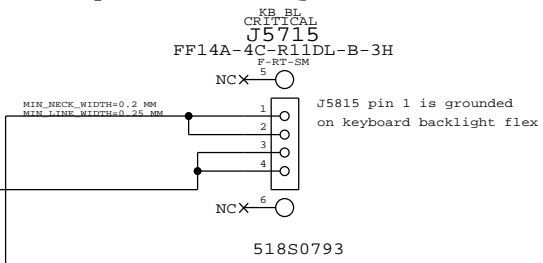


Keyboard Backlight Driver & Detection



To detect Keyboard backlight, SMC will tristate and read SMC_SYS_KBDLED:
If LOW, keyboard backlight present
If HIGH, keyboard backlight not present
R5853 always stuffed, R5854 only grounded when KB BL flex connected.

Keyboard Backlight Connector



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0704	2	CAP, CER, 0.22UF, 10V, 50V, X5R, 0603	C5756, C5755		KB_BL

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SYNC DATE=12/13/2010

IPD / KBD Backlight

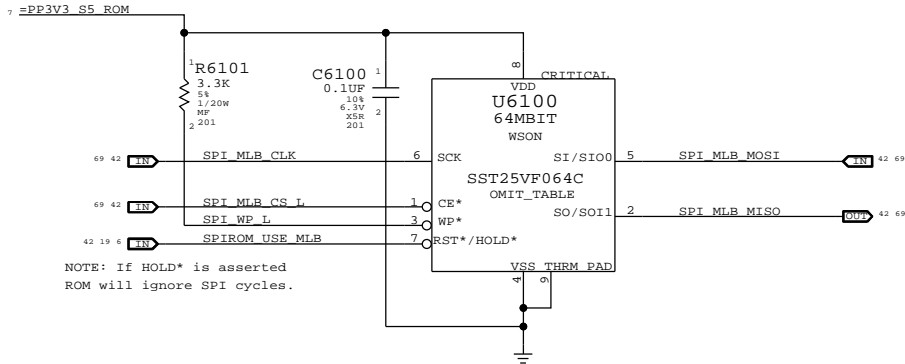
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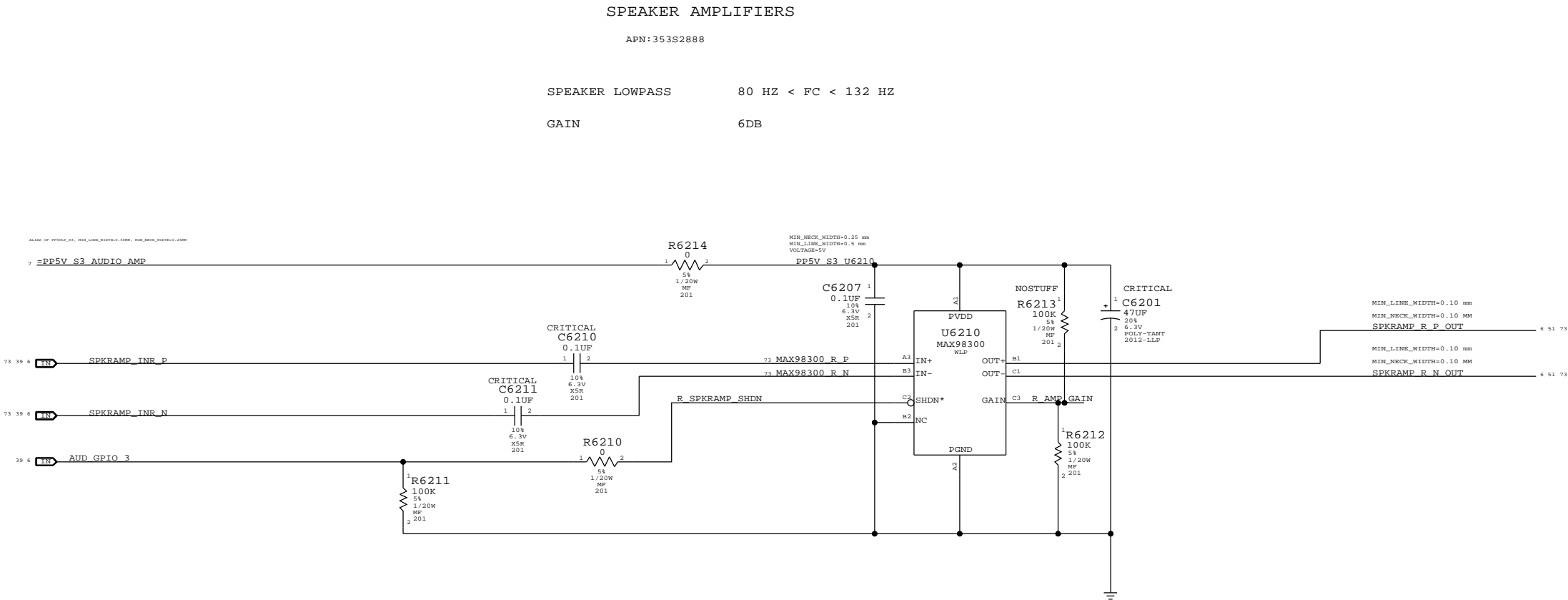
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B

B

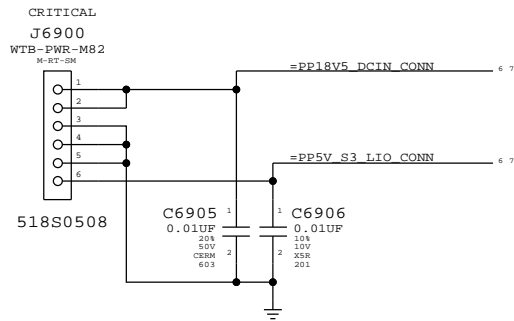
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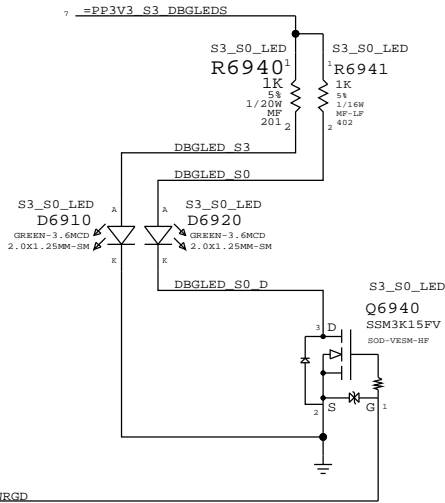
SYNC MASTER=K21 MLB		SYNC DATE=12/13/2010	
PAGE TITLE			
AUDIO0: SPEAKER AMP			
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MLB to LIO Power Cable Connector



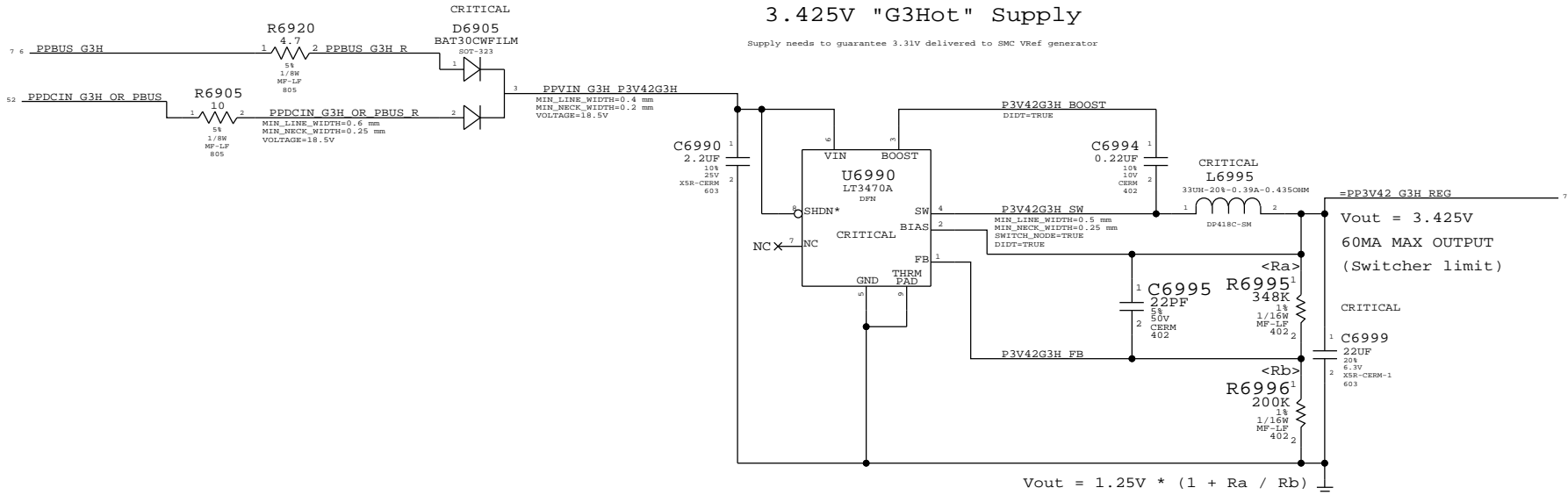
Debug LEDs

(For development only)

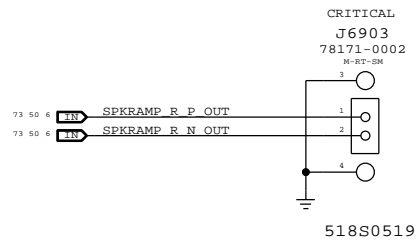


3.425V "G3Hot" Supply

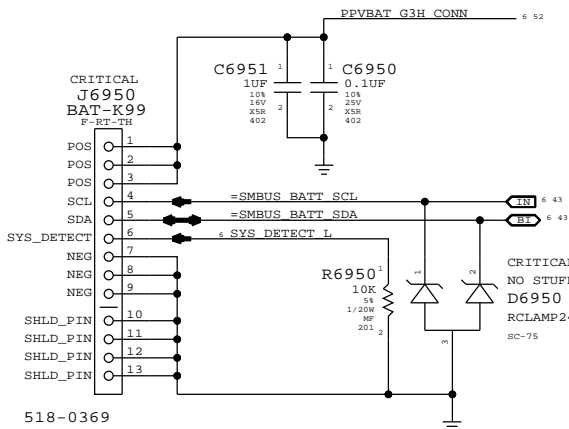
Supply needs to guarantee 3.31V delivered to SMC VRef generator



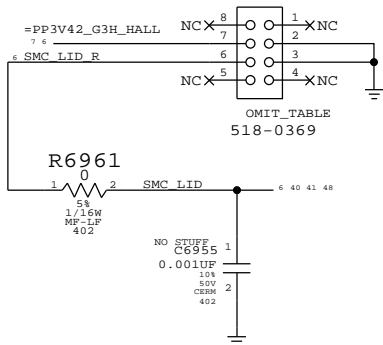
Right Speaker Connector




K99-Specific Battery Connector

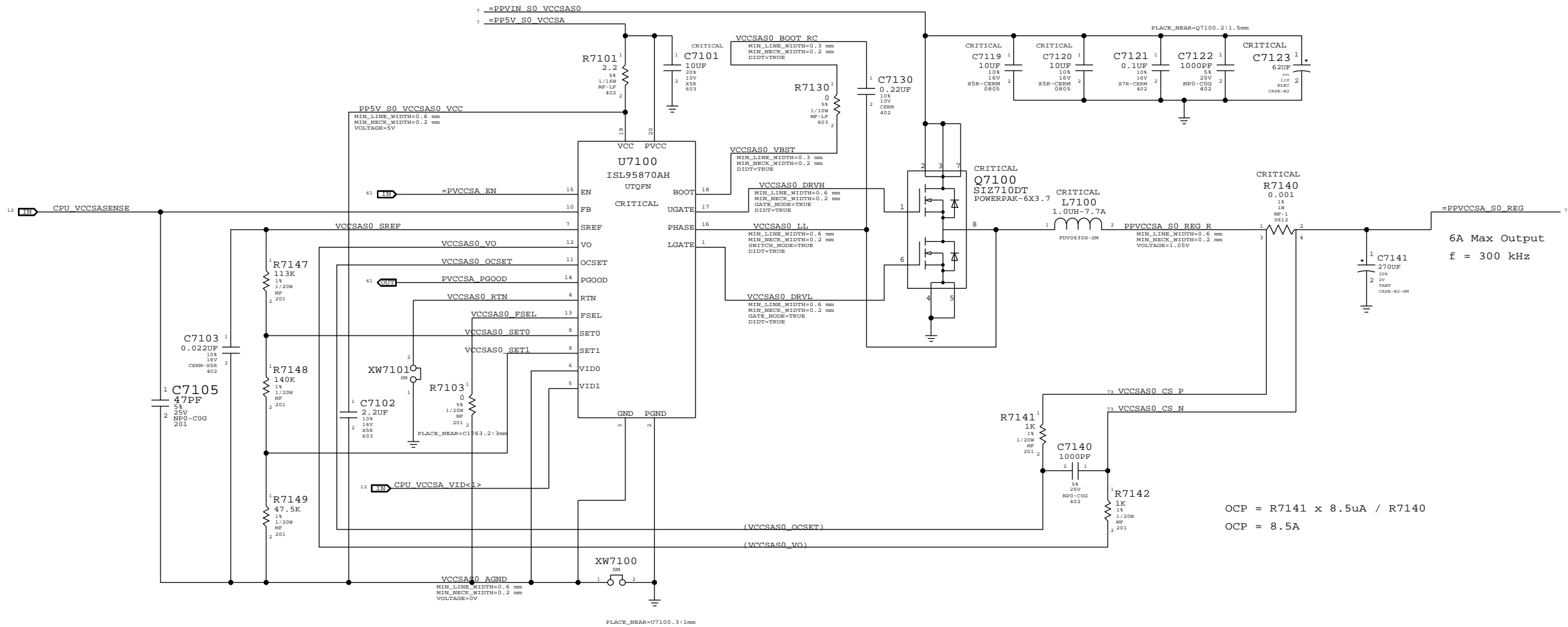


J6955 HALL-SENSOR-MLB-PADS-K99



SYM PART#K99 MLB		SYMC DATE=11/11/2011	
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DC-In & Battery Connectors			
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VID1	VID0	Voltage
0	0	0.9V
1	0	0.8V

$$OCP = R7141 \times 8.5\mu A / R7140$$
$$OCP = 8.5A$$

A

8

7

6

5

4

3

2

1

D

D

C

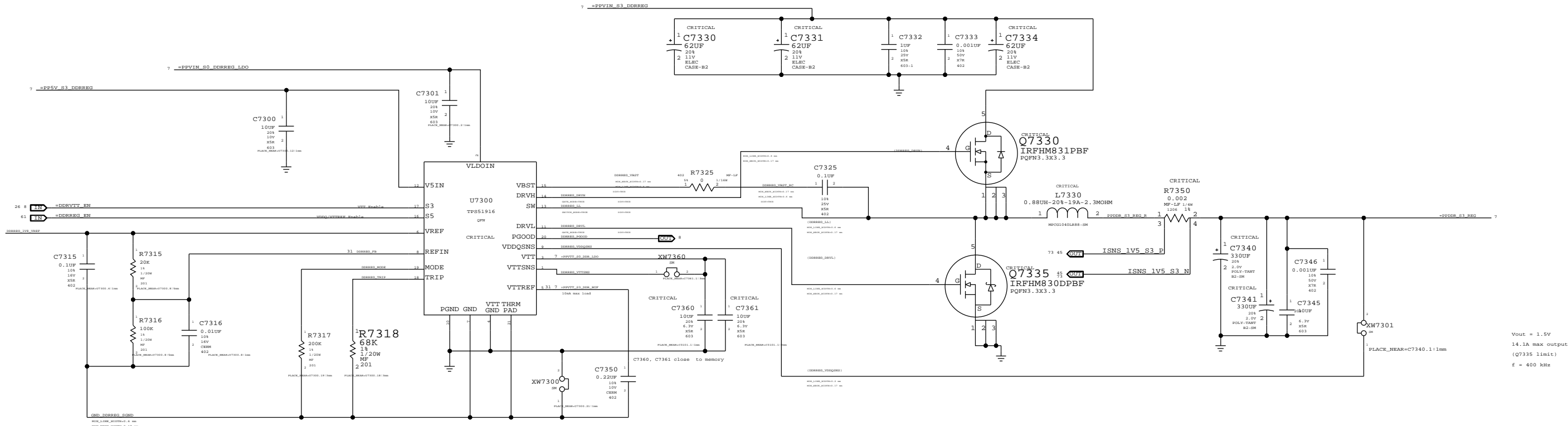
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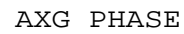
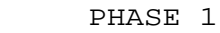
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1.5V DDR3 Supply			
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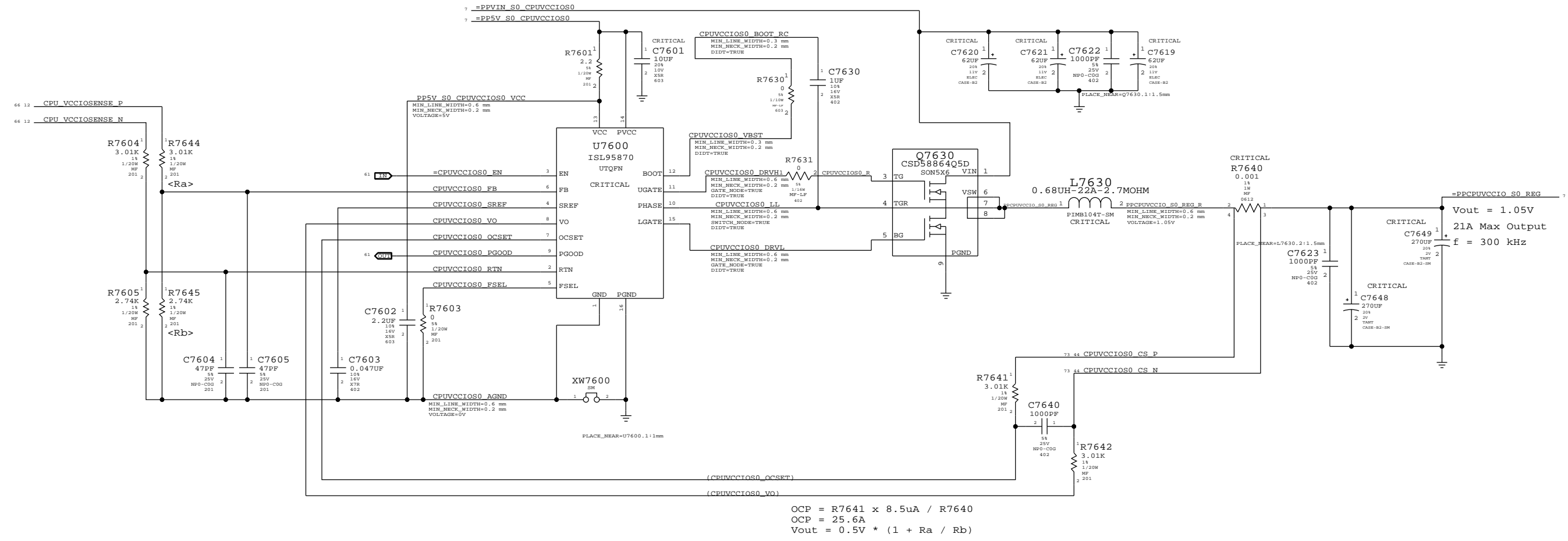
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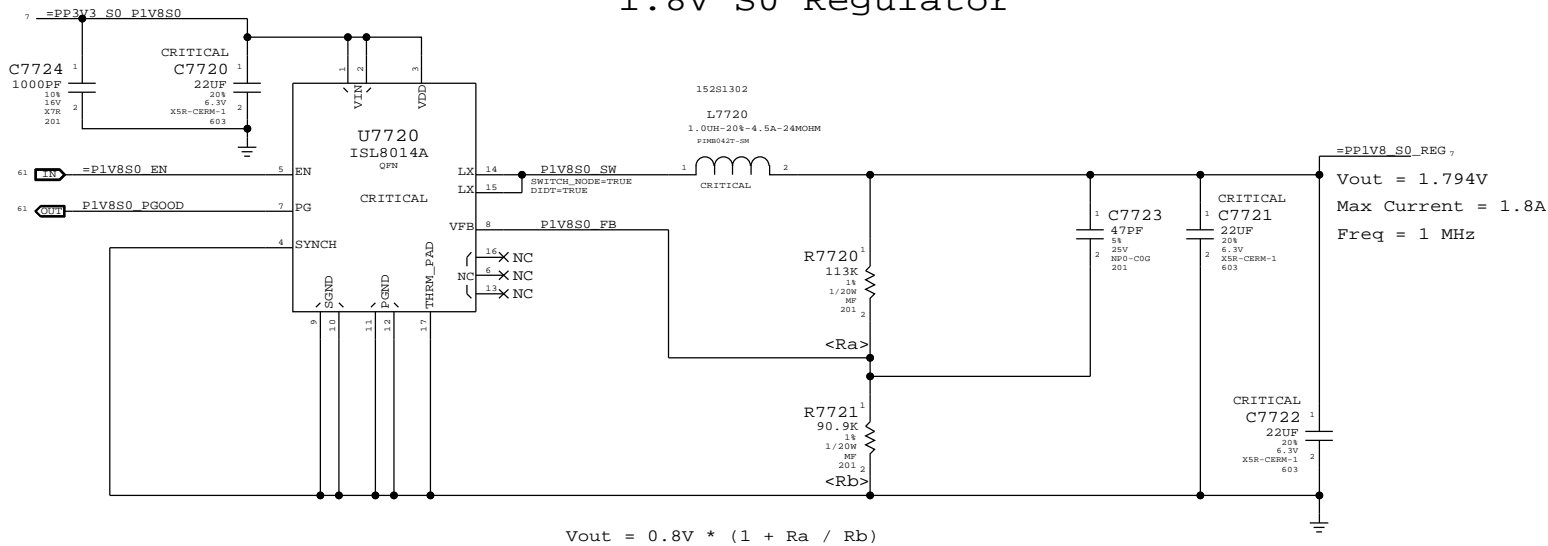
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CPU VCCIO (1.05V S0) Regulator

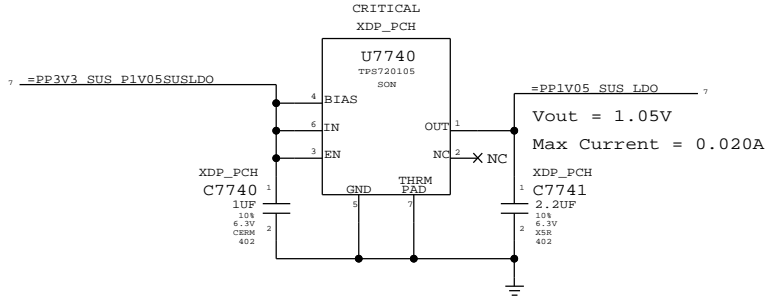


1.8V S0 Regulator

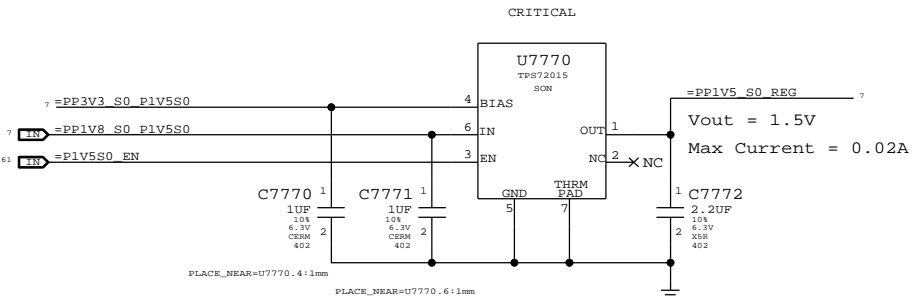


1.05V SUS LDO

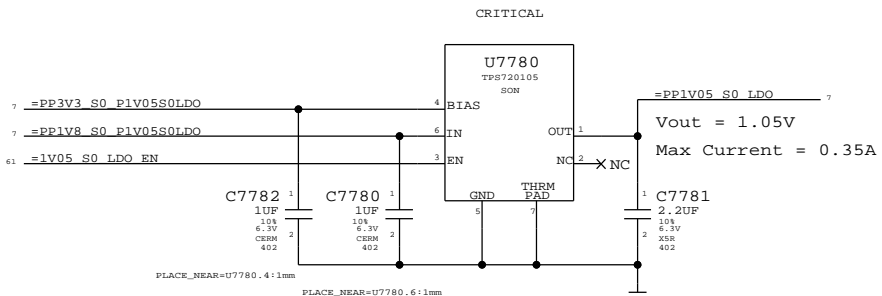
Cougar Point requires JTAG pull-ups to be powered at 1.05V when SUS suspend well is active. Pull-ups (3) must be 51 ohms to support XDP (not required in production). 70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.

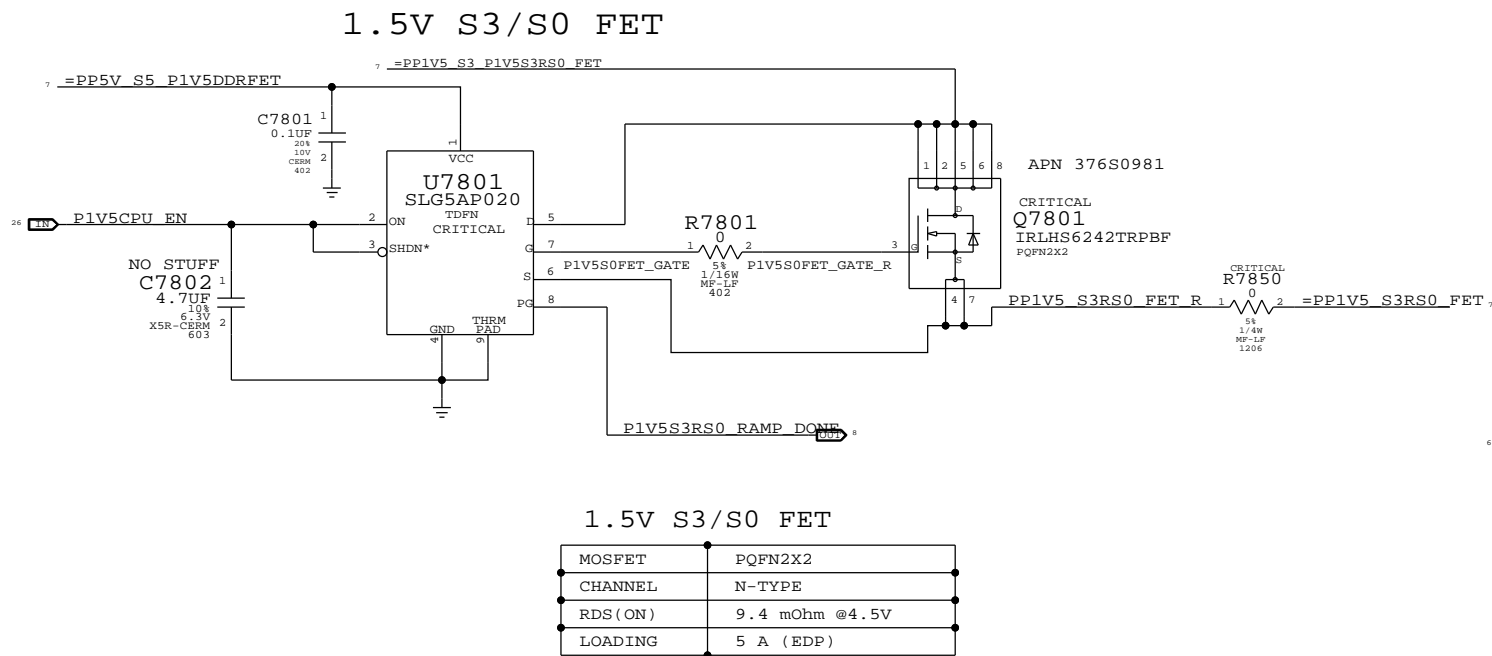
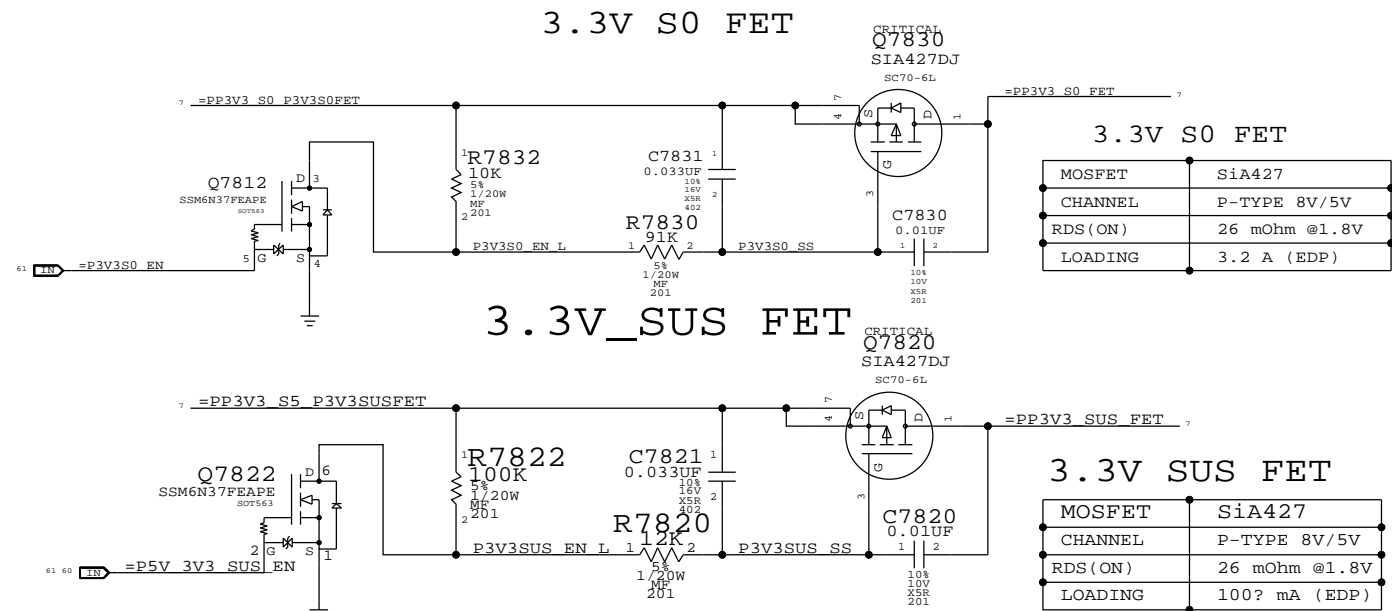
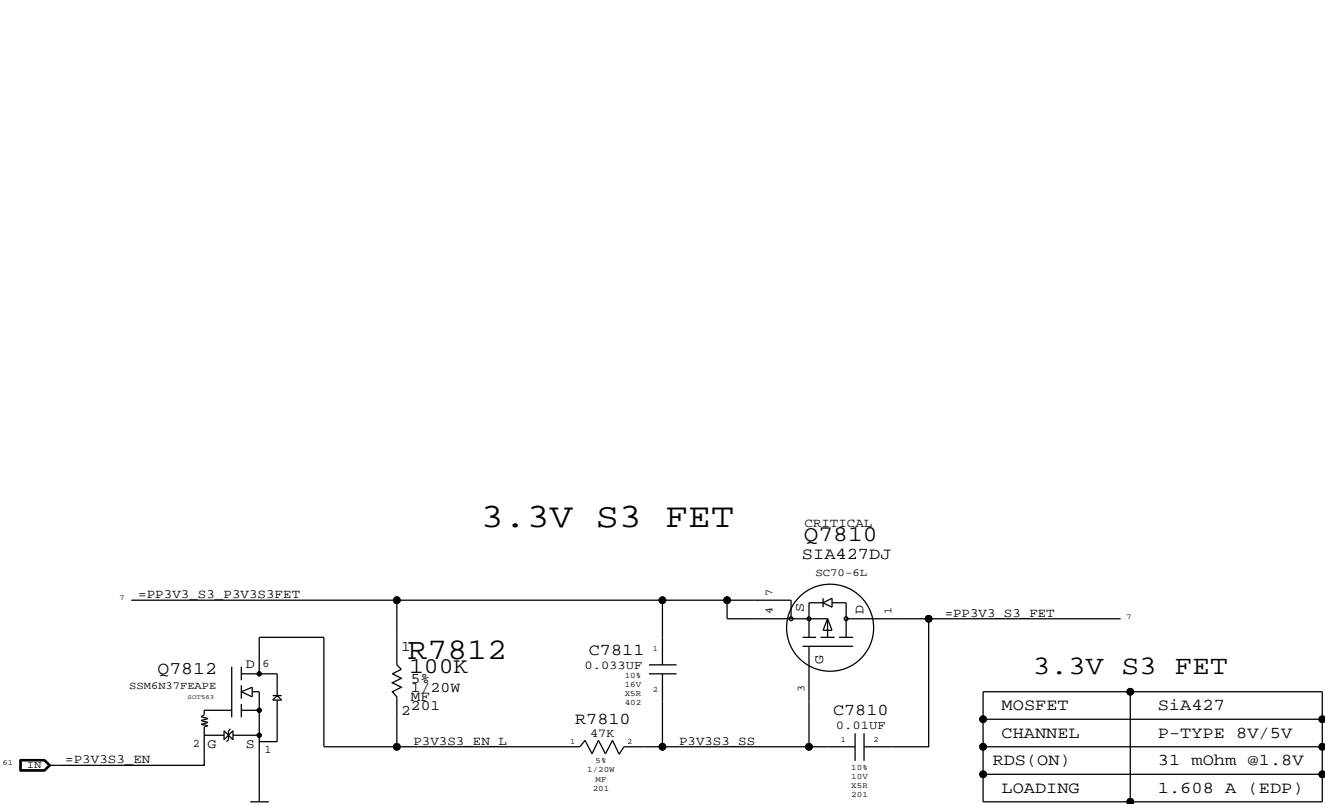


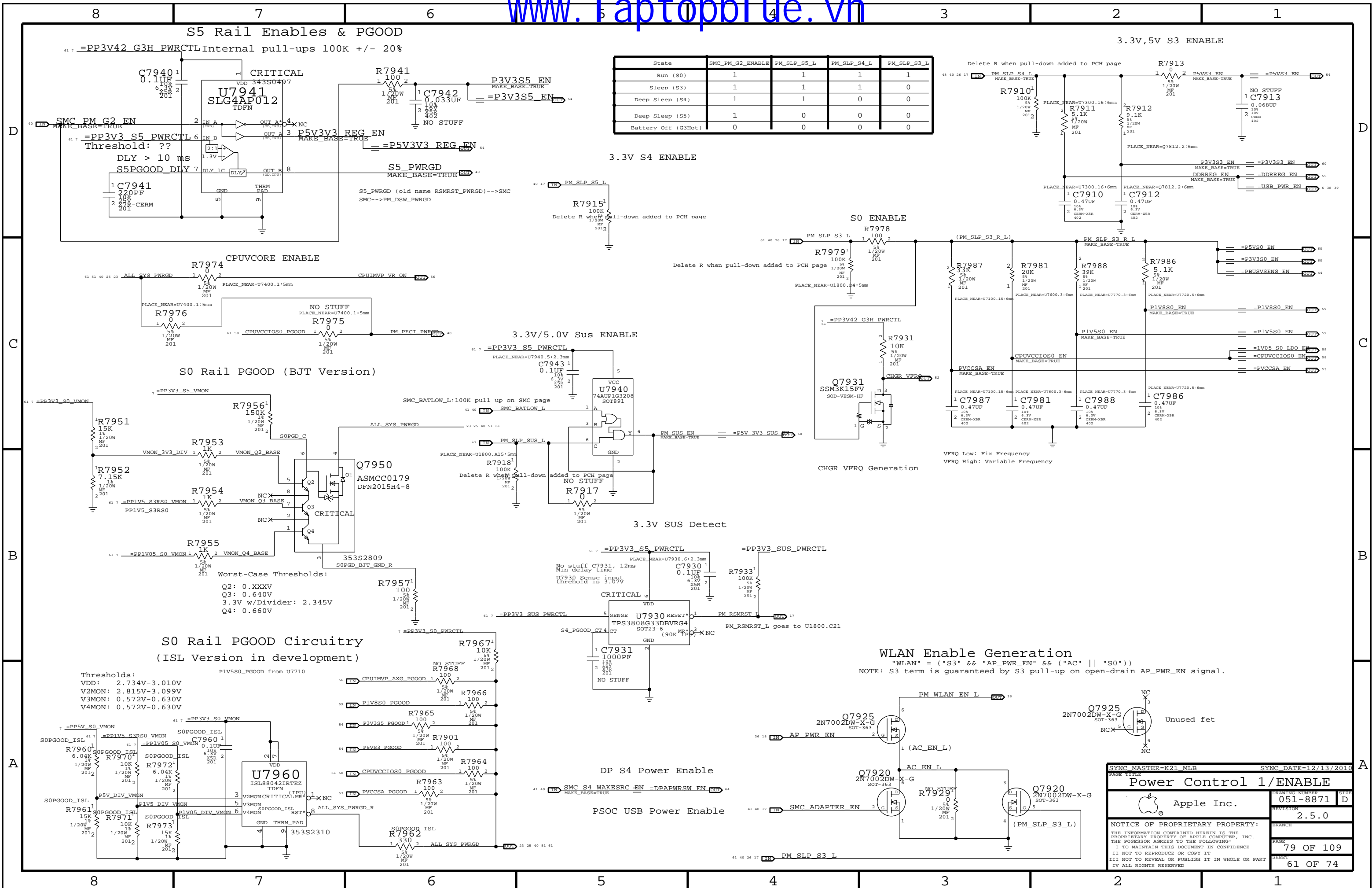
1.5V S0 LDO



1.05V S0 LDO

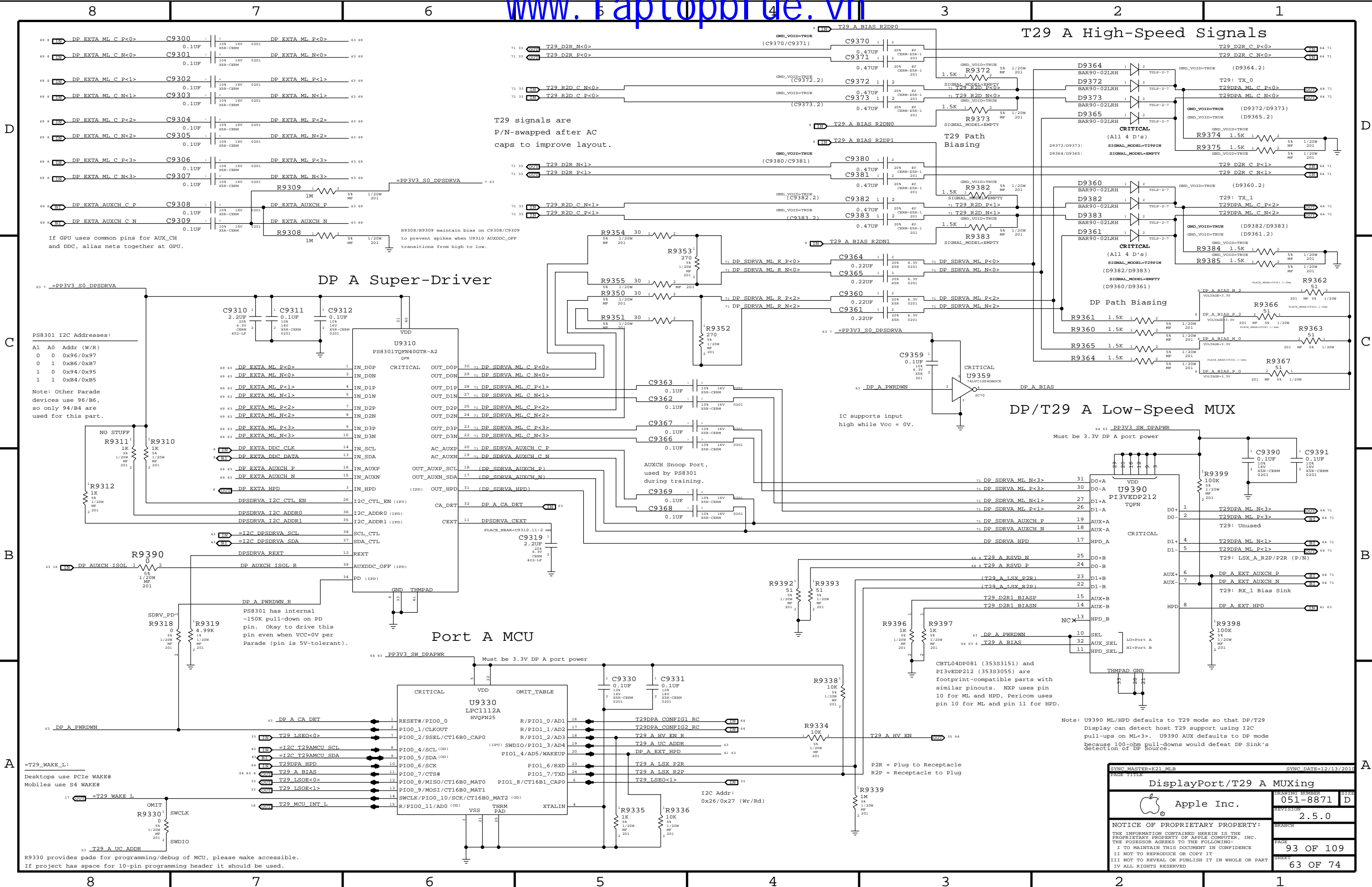








8	7	6	5	4	3	2	1
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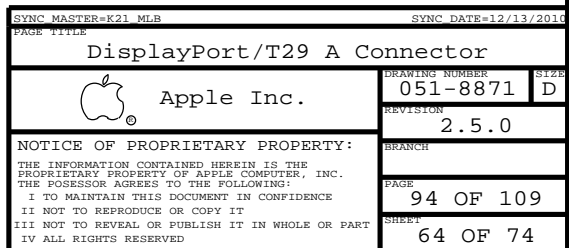


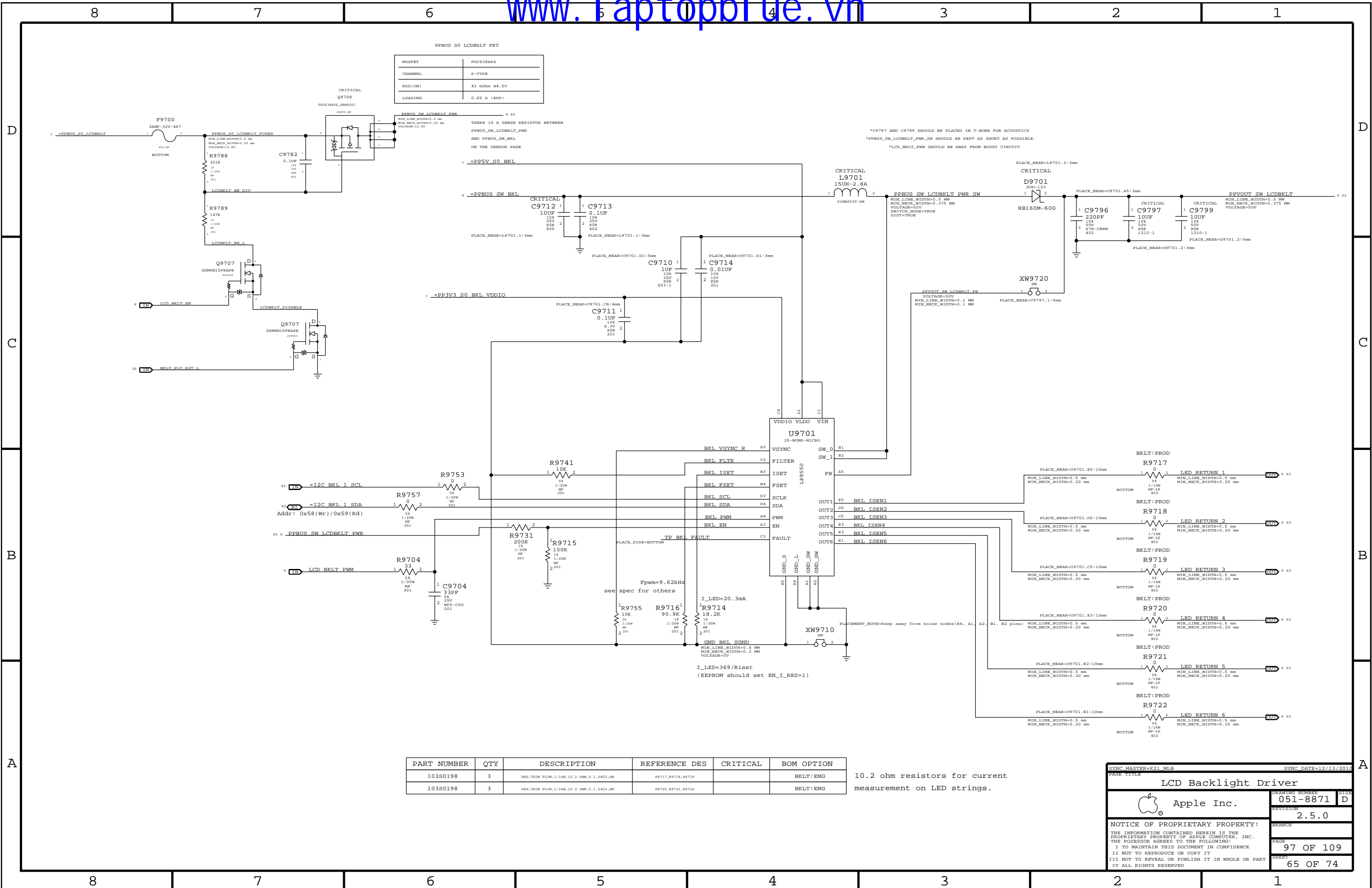
T29 signals are P/N-swapped after AC caps to improve layout.

IC supports input high while Vcc = 0V.

Note: U9390 ML/HPD defaults to T29 mode so that DP/T29 Display can detect host T29 support using I2C pull-ups on ML<3>. U9390 AUX defaults to DP mode because 100-ohm pull-downs would defeat DP Sink's detection of DP Source.

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DisplayPort/T29 A MUXing		051-8871	
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES, THIN FILM, 1/16W, 10.2 OHM, 0.1, 0402, 0H	R9717, R9718, R9719		BKLT:ENG
103S0198	3	RES, THIN FILM, 1/16W, 10.2 OHM, 0.1, 0402, 0H	R9720, R9721, R9722		BKLT:ENG

10.2 ohm resistors for current measurement on LED strings.

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SYNC DATE=12/13/2010

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LCD Backlight Driver

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	~37_OBM_SE	+37_OBM_SE	~37_OBM_SE	~37_OBM_SE	~STANDARD	~STANDARD
MEM_40S	*	~40_OBM_SE	+40_OBM_SE	~40_OBM_SE	~40_OBM_SE	~STANDARD	~STANDARD
MEM_55S	*	~55_OBM_SE	+55_OBM_SE	~55_OBM_SE	~55_OBM_SE	~STANDARD	~STANDARD
MEM_72S	*	~72_OBM_DIFF	+72_OBM_DIFF	~72_OBM_DIFF	~72_OBM_DIFF	~72_OBM_DIFF	~72_OBM_DIFF
MEM_50S	TOP_BOTTOM	Y	+50_OBM_SE	~50_OBM_SE	~50_OBM_SE	~STANDARD	~STANDARD
MEM_85D	TOP_BOTTOM	Y	+85_OBM_DIFF	+85_OBM_DIFF	+85_OBM_DIFF	+85_OBM_DIFF	+85_OBM_DIFF
MEM_50S	ISL3, ISL4, ISL9, ISL10	Y	+50_OBM_SE	~50_OBM_SE	~50_OBM_SE	~STANDARD	~STANDARD
MEM_85D	ISL3, ISL4, ISL9, ISL10	Y	+85_OBM_DIFF	+85_OBM_DIFF	+85_OBM_DIFF	+85_OBM_DIFF	+85_OBM_DIFF

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
MEM_A_CLK	MEM_72D	MEM_CLK	MEM A CLK P<5..0>	8 11 27 28 32
MEM_A_CLK	MEM_72D	MEM_CLK	MEM A CLK N<5..0>	8 11 27 28 32
MEM_A_CTRL	MEM_55S	MEM_CTRL	MEM A CKE<3..0>	8 11 27 28 32
MEM_A_CTRL	MEM_55S	MEM_CTRL	MEM A CS L<3..0>	8 11 27 28 32
MEM_A_CTRL	MEM_55S	MEM_CTRL	MEM A ODT<3..0>	8 11 27 28 32
MEM_A_CMD	MEM_55S	MEM_CMD	MEM A A<15..0>	8 11 27 28 32
MEM_A_CMD	MEM_55S	MEM_CMD	MEM A BA<2..0>	11 27 28 32
MEM_A_CMD	MEM_55S	MEM_CMD	MEM A RAS L	11 27 28 32
MEM_A_CMD	MEM_55S	MEM_CMD	MEM A CAS L	11 27 28 32
MEM_A_CMD	MEM_55S	MEM_CMD	MEM A WE L	11 27 28 32
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM A DQ<7..0>	11 27
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM A DQ<15..8>	11 27
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM A DQ<23..16>	11 27
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM A DQ<31..24>	11 27
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM A DQ<39..32>	11 28
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM A DQ<47..40>	11 28
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM A DQ<55..48>	11 28
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM A DQ<63..56>	11 28
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM A DQS P<0>	11 27
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM A DQS N<0>	11 27
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM A DQS P<1>	11 27
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM A DQS N<1>	11 27
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM A DQS P<2>	11 27
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM A DQS N<2>	11 27
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM A DQS P<3>	11 27
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM A DQS N<3>	11 27
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM A DQS P<4>	11 28
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM A DQS N<4>	11 28
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM A DQS P<5>	11 28
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM A DQS N<5>	11 28
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM A DQS P<6>	11 28
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM A DQS N<6>	11 28
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM A DQS P<7>	11 28
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM A DQS N<7>	11 28
MEM_B_CLK	MEM_72D	MEM_CLK	MEM B CLK P<5..0>	8 11 29 30 32
MEM_B_CLK	MEM_72D	MEM_CLK	MEM B CLK N<5..0>	8 11 29 30 32
MEM_B_CTRL	MEM_55S	MEM_CTRL	MEM B CKE<3..0>	8 11 29 30 32
MEM_B_CTRL	MEM_55S	MEM_CTRL	MEM B CS L<3..0>	8 11 29 30 32
MEM_B_CTRL	MEM_55S	MEM_CTRL	MEM B ODT<3..0>	8 11 29 30 32
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B A<15..0>	8 11 29 30 32
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B BA<2..0>	11 29 30 32
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B RAS L	11 29 30 32
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B CAS L	11 29 30 32
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B WE L	11 29 30 32
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM B DQ<7..0>	11 29
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM B DQ<15..8>	11 29
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM B DQ<23..16>	11 29
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM B DQ<31..24>	11 29
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM B DQ<39..32>	11 30
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM B DQ<47..40>	11 30
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM B DQ<55..48>	11 30
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM B DQ<63..56>	11 30
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM B DQS P<0>	11 29
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM B DQS N<0>	11 29
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM B DQS P<1>	11 29
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM B DQS N<1>	11 29
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM B DQS P<2>	11 29
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM B DQS N<2>	11 29
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM B DQS P<3>	11 29
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM B DQS N<3>	11 29
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM B DQS P<4>	11 30
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM B DQS N<4>	11 30
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM B DQS P<5>	11 30
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM B DQS N<5>	11 30
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM B DQS P<6>	11 30
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM B DQS N<6>	11 30
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM B DQS P<7>	11 30
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM B DQS N<7>	11 30
		MEM_PWR	PP1V5 S3RS0	6 7
		MEM_PWR	PP1V5 S3	6 7
		MEM_PWR	PP0V75 S3 MEM VREFCA A	27 28 29 30 31
		MEM_PWR	PP0V75 S3 MEM VREFDQ A	9 27 28 29 30 31

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2CLK	*	0.6 MM	?
MEM_CTRL2CTRL	*	0.2 MM	?
MEM_CMD2CTRL	*	0.2 MM	?
MEM_CMD2CMD	*	0.2 MM	?
MEM_DATA2DATA	*	0.14 MM	?
MEM_DQS2DQS	*	0.4 MM	?
MEM_MEM2OTHERMEM	*	0.4 MM	?
MEM_PWR	*	+DNR_P2MM	?
MEM_20RD	*	+GND_P2MM	?
MEM_20THER	*	0.6 MM	?

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_PWR	*	MEM_P2WR
MEM_CTRL	MEM_PWR	*	MEM_P2WR
MEM_CMD	MEM_PWR	*	MEM_P2WR
MEM_DATA	MEM_PWR	*	MEM_P2WR
MEM_DQS	MEM_PWR	*	MEM_P2WR

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	MEM_20RD
MEM_CTRL	GND	*	MEM_20RD
MEM_CMD	GND	*	MEM_20RD
MEM_DATA	GND	*	MEM_20RD
MEM_DQS	GND	*	MEM_20RD

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK
MEM_CLK	MEM_CTRL	*	MEM_MEM2OTHERMEM
MEM_CLK	MEM_CMD	*	MEM_MEM2OTHERMEM
MEM_CLK	MEM_DATA	*	MEM_MEM2OTHERMEM
MEM_CLK	MEM_DQS	*	MEM_MEM2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_MEM2OTHERMEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_MEM2OTHERMEM
MEM_CMD	MEM_DQS	*	MEM_MEM2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_MEM2OTHERMEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CMD	MEM_CMD	*	MEM_CMD2CTRL
MEM_CTRL	MEM_DATA	*	MEM_MEM2OTHERMEM
MEM_CTRL	MEM_DQS	*	MEM_MEM2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_MEM2OTHERMEM
MEM_DATA	MEM_CTRL	*	MEM_MEM2OTHERMEM
MEM_DATA	MEM_CMD	*	MEM_MEM2OTHERMEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_MEM2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_MEM2OTHERMEM
MEM_DQS	MEM_CTRL	*	MEM_MEM2OTHERMEM
MEM_DQS	MEM_CMD	*	MEM_MEM2OTHERMEM
MEM_DQS	MEM_DATA	*	MEM_MEM2OTHERMEM
MEM_DQS	MEM_DQS	*	MEM_DQS2DQS

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_20THER
MEM_CTRL	*	*	MEM_20THER
MEM_CMD	*	*	MEM_20THER
MEM_DATA	*	*	MEM_20THER
MEM_DQS	*	*	MEM_20THER

Need to support MEM_*-style wildcards!

DDR3: Sandybridge SFF 2C when routed on Type-3 (Through hole) should follow +PGA guidelines per Huron River SFF DG rev1.0 (#438297).

DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.

DQ to DQS matching per byte lane should be within 0.127mm.

DQS to clock matching should be within [CLK-63.5mm] and [CLK+38.1mm].

CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.0508mm.

CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0.0mm] of CLK pairs.

A/BA/CMD signals should be matched within [CLK-12.7mm] to [CLK+12.7mm] of CLK pairs A/BA/CMD signals to each other should match within 5.08mm.

DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.


Maximum length of any signal from die pad to SODIMM pad is 119.83mm, from processor ball to SODIMM pad is 88.9mm.

SOURCE: Huron River Platform DG, Rev 1.01 (#436735), Section 2.5

SYMC PARTS-CONSTRAINTS

SYMC DATE=01/06/2011

Memory Constraints

 Apple Inc.

DRAWING NUMBER051-8871SIZE D

REVISION2.5.0

BRANCH

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Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	+85_OBM_DIFF	+85_OBM_DIFF	+85_OBM_DIFF	+85_OBM_DIFF	+85_OBM_DIFF	+85_OBM_DIFF
LVDS_90D	*	+90_OBM_DIFF	+90_OBM_DIFF	+90_OBM_DIFF	+90_OBM_DIFF	+90_OBM_DIFF	+90_OBM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	+3x_DIELECTRIC	?	DISPLAYPORT	TOP,BOTTOM	+4x_DIELECTRIC	?
LVDS	*	+3x_DIELECTRIC	?	LVDS	TOP,BOTTOM	+4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	+90_OBM_DIFF	+90_OBM_DIFF	+90_OBM_DIFF	+90_OBM_DIFF	+90_OBM_DIFF	+90_OBM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	+4x_DIELECTRIC	?	SATA	TOP,BOTTOM	+3x_DIELECTRIC	?
SATA_ICOMP	*	8 MIL	?				

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	+STANDARD	8 MIL	8 MIL	+STANDARD	+STANDARD	+STANDARD
USB_85D	*	+85_OBM_DIFF	+85_OBM_DIFF	+85_OBM_DIFF	+85_OBM_DIFF	+85_OBM_DIFF	+85_OBM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	+2x_DIELECTRIC	?	USB	TOP,BOTTOM	+4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ixex Peak M (DG-398905-398905_v1.5), Section 3.8

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
DP_ML	DP_85D	DISPLAYPORT	DP IG ML P<3..0>	8
DP_ML	DP_85D	DISPLAYPORT	DP IG ML N<3..0>	8
DP_EXT_AUXCH	DP_85D	DISPLAYPORT	DP IG AUX_CH P	8
DP_EXT_AUXCH	DP_85D	DISPLAYPORT	DP IG AUX_CH N	8
LVDS_IG_A_CLK	LVDS_90D	LVDS	LVDS IG A_CLK P	
LVDS_IG_A_CLK	LVDS_90D	LVDS	LVDS IG A_CLK N	
LVDS_IG_A_DATA	LVDS_90D	LVDS	LVDS IG A_DATA P<2..0>	
LVDS_IG_A_DATA	LVDS_90D	LVDS	LVDS IG A_DATA N<2..0>	
	LVDS_90D	LVDS	LVDS IG A_DATA P<3>	8
	LVDS_90D	LVDS	LVDS IG A_DATA N<3>	8
	LVDS_90D	LVDS	LVDS IG B_DATA P<3..0>	8
	LVDS_90D	LVDS	LVDS IG B_DATA N<3..0>	8
	LVDS_90D	LVDS	LVDS IG B_CLK P	8
	LVDS_90D	LVDS	LVDS IG B_CLK N	8
	SATA_90D	SATA	SATA HDD R2D_C_P	16 37
	SATA_90D	SATA	SATA HDD R2D_C_N	16 37
SATA_HDD_R2D	SATA_90D	SATA	SATA HDD R2D_P	6 37
SATA_HDD_R2D	SATA_90D	SATA	SATA HDD R2D_N	6 37
SATA_HDD_D2R	SATA_90D	SATA	SATA HDD D2R_P	16 37
SATA_HDD_D2R	SATA_90D	SATA	SATA HDD D2R_N	16 37
	SATA_90D	SATA	SATA HDD D2R_C_P	6 37
	SATA_90D	SATA	SATA HDD D2R_C_N	6 37
	SATA_90D	SATA	SATA ODD R2D_C_P	8 16
	SATA_90D	SATA	SATA ODD R2D_C_N	8 16
SATA_ODD_R2D	SATA_90D	SATA	SATA ODD R2D_P	
SATA_ODD_R2D	SATA_90D	SATA	SATA ODD R2D_N	
SATA_ODD_D2R	SATA_90D	SATA	SATA ODD D2R_P	8 16
SATA_ODD_D2R	SATA_90D	SATA	SATA ODD D2R_N	8 16
	SATA_90D	SATA	SATA HDD R2D_RC_P	
	SATA_90D	SATA	SATA HDD R2D_RC_N	
	SATA_90D	SATA	SATA HDD D2R_RC_P	
	SATA_90D	SATA	SATA HDD D2R_RC_N	
PCH_SATA_ICOMP		SATA_ICOMP	PCH_SATAICOMP	16
USB_HUB1_UP	USB_85D	USB	USB HUB1_UP_P	18 24
	USB_85D	USB	USB HUB1_UP_N	18 24
USB_HUB2_UP	USB_85D	USB	USB HUB2_UP_P	18 24
	USB_85D	USB	USB HUB2_UP_N	18 24
USB_EXT_A	USB_85D	USB	USB_EXT_A_P	24 38
USB_EXT_A	USB_85D	USB	USB_EXT_A_N	24 38
USB_EXT_B	USB_85D	USB	USB_EXT_B_P	
	USB_85D	USB	USB_EXT_B_N	
USB_EXT_C	USB_85D	USB	USB_EXT_C_P	
	USB_85D	USB	USB_EXT_C_N	
USB_EXT_D	USB_85D	USB	USB_EXT_D_P	6 24 39
	USB_85D	USB	USB_EXT_D_N	6 24 39
USB_EXT_D	USB_85D	USB	USB_T29A_P	8 24
	USB_85D	USB	USB_T29A_N	8 24
	USB_85D	USB	T29_A_RSVD_P	8 63
	USB_85D	USB	T29_A_RSVD_N	8 63
USB_CAMERA	USB_85D	USB	USB_CAMERA_P	6 18 39
	USB_85D	USB	USB_CAMERA_N	6 18 39
USB_CAMERA	USB_85D	USB	USB_CAMERA_CONN_P	
	USB_85D	USB	USB_CAMERA_CONN_N	
USB_BT	USB_85D	USB	USB_BT_P	6 24 36
USB_BT	USB_85D	USB	USB_BT_N	6 24 36
USB_TPAD	USB_85D	USB	USB_TPAD_P	
	USB_85D	USB	USB_TPAD_N	
USB_IR	USB_85D	USB	USB_IR_P	
	USB_85D	USB	USB_IR_N	
USB_SDCARD	USB_85D	USB	USB_SDCARD_P	8 24
	USB_85D	USB	USB_SDCARD_N	8 24
USB_BRCRYPT	USB_85D	USB	USB_BRCRYPT_P	
	USB_85D	USB	USB_BRCRYPT_N	
PCH_USB_RBIAS	PCH_USB_RBIAS		PCH_USB_RBIAS	18
PCH_DIFECCLK_UNUSED	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_P	16 25
PCH_DIFECCLK_UNUSED	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_N	16 25
	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_PCH_P	
	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_PCH_N	
PCH_DIFECCLK_UNUSED	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_P	16 25
PCH_DIFECCLK_UNUSED	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_N	16 25
PCH_DIFECCLK_UNUSED	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_P	16 25
PCH_DIFECCLK_UNUSED	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_N	16 25
	CPH_50S	CLK_PCIE	PCH_CLK14P3M_REFCLK	16 25
LPC_CLK33M	CPH_50S	CLK_PCIE	PCH_CLK33M_PCIIN	16 25
GFX_CLK_DPLLSS	CLK_PCIE_90D	CLK_PCIE	GFX_CLK120M_DPLLSS_P	
GFX_CLK_DPLLSS	CLK_PCIE_90D	CLK_PCIE	GFX_CLK120M_DPLLSS_N	

D

C

B

A

D

C

B

A

CAESAR IV (Ethernet) Constraints							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_3X	*	=3:1_SPACING	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_CR_DATA	*	8MIL	?












CAESAR IV (Ethernet PHY) Constraints							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF









SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	8.6 MM	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

FireWire Interface Constraints							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

Ethernet Net Properties			
ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALI
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALO
	ENET_50S	ENET_3X	ENET_RESET_L
	ENET_MDI	ENET_MDI	ENET_MDI_P<3..0>
	ENET_100D	ENET_MDI	ENET_MDI_N<3..0>
	ENET_50S	ENET_CR_DATA	ENET_CR_DATA<7..0>
	ENET_50S	ENET_CR_DATA	ENET_CR_CMD
	ENET_50S	ENET_CR_DATA	ENET_CR_CLK
	ENET_50S	ENET_CR_DATA	SDCONN_DATA<7..0>
	ENET_50S	ENET_CR_DATA	SDCONN_CMD
	ENET_50S	ENET_CR_DATA	SDCONN_CLK

FireWire Net Properties			
ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
	FW_110D	FW_TP	FW_P0_TPA_P
	FW_110D	FW_TP	FW_P0_TPA_N
	FW_110D	FW_TP	FW_P0_TPB_P
	FW_110D	FW_TP	FW_P0_TPB_N
	FW_110D	FW_TP	FW_P1_TPA_P
	FW_110D	FW_TP	FW_P1_TPA_N
	FW_110D	FW_TP	FW_P1_TPB_P
	FW_110D	FW_TP	FW_P1_TPB_N
Part 2 Not Used			

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

T29 I2C Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_I2C_55S	*	+55_OHM_SR	+55_OHM_SR	+55_OHM_SR	+55_OHM_SR	-STANDARD	-STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_I2C	*	+2x_DIELECTRIC	?

T29 SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SPI_55S	*	+55_OHM_SR	+55_OHM_SR	+55_OHM_SR	+55_OHM_SR	-STANDARD	-STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SPI	*	+2x_DIELECTRIC	?

DP/T29 Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29DP_80D	*	+80_OHM_DIFF	+80_OHM_DIFF	+80_OHM_DIFF	+80_OHM_DIFF	+80_OHM_DIFF	+80_OHM_DIFF
T29DP_100D	*	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	*	+5x_DIELECTRIC	?	T29DP	TOP,BOTTOM	+7x_DIELECTRIC	?

SOURCE: Bill Cornelius's T29 Routing Notes

T29 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
DP_85D	DP_85D	DISPLAYPORT	DP T29SNK0 ML C P<3..0> 8 33
DP_85D	DP_85D	DISPLAYPORT	DP T29SNK0 ML C N<3..0> 8 33
DP_T29SNK0_ML	DP_85D	DISPLAYPORT	DP T29SNK0 ML P<3..0> 33
DP_T29SNK0_ML	DP_85D	DISPLAYPORT	DP T29SNK0 ML N<3..0> 33
DP_85D	DP_85D	DISPLAYPORT	DP T29SNK0 AUXCH C P 8 33
DP_85D	DP_85D	DISPLAYPORT	DP T29SNK0 AUXCH C N 8 33
DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP T29SNK0 AUXCH P 33
DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP T29SNK0 AUXCH N 33
DP_85D	DP_85D	DISPLAYPORT	DP T29SNK1 ML C P<3..0> 33
DP_85D	DP_85D	DISPLAYPORT	DP T29SNK1 ML C N<3..0> 33
DP_T29SNK1_ML	DP_85D	DISPLAYPORT	DP T29SNK1 ML P<3..0> 33
DP_T29SNK1_ML	DP_85D	DISPLAYPORT	DP T29SNK1 ML N<3..0> 33
DP_85D	DP_85D	DISPLAYPORT	DP T29SNK1 AUXCH C P 33
DP_85D	DP_85D	DISPLAYPORT	DP T29SNK1 AUXCH C N 33
DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP T29SNK1 AUXCH P 33
DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP T29SNK1 AUXCH N 33
T29_I2C_55S	T29_I2C	I2C T29_SCL	33 43
T29_I2C_55S	T29_I2C	I2C T29_SDA	33 43
T29_SPI_CLK	T29_SPI_55S	T29_SPI	T29_SPI_CLK 33
T29_SPI_MOSI	T29_SPI_55S	T29_SPI	T29_SPI MOSI 33
T29_SPI_MISO	T29_SPI_55S	T29_SPI	T29_SPI MISO 33
T29_SPI_CS_L	T29_SPI_55S	T29_SPI	T29_SPI CS L 33
T29DP_80D	T29DP	T29DP	T29 R2D C P<3..0> 33 63
T29DP_80D	T29DP	T29DP	T29 R2D C N<3..0> 33 63
T29DP_80D	T29DP	T29DP	T29 D2R P<3..0> 33 63
T29DP_80D	T29DP	T29DP	T29 D2R N<3..0> 33 63
T29_R2D0	T29DP_80D	T29DP	T29 R2D P<0> 63
T29_R2D0	T29DP_80D	T29DP	T29 R2D N<0> 63
T29_R2D1	T29DP_80D	T29DP	T29 R2D P<1> 63
T29_R2D1	T29DP_80D	T29DP	T29 R2D N<1> 63
T29DP_80D	T29DP	T29DP	T29 R2D C F P<1..0> 63
T29DP_80D	T29DP	T29DP	T29 R2D C F N<1..0> 63
T29_D2R0	T29DP_80D	T29DP	T29 D2R C P<0> 63 64
T29_D2R0	T29DP_80D	T29DP	T29 D2R C N<0> 63 64
T29_D2R1	T29DP_80D	T29DP	T29 D2R C P<1> 63 64
T29_D2R1	T29DP_80D	T29DP	T29 D2R C N<1> 63 64
T29DP_80D	T29DP	T29DP	T29DPA D2R1 AUXCH P 64
T29DP_80D	T29DP	T29DP	T29DPA D2R1 AUXCH N 64
T29DP_80D	T29DP	T29DP	DP SDRVA ML C P<3..0> 63
T29DP_80D	T29DP	T29DP	DP SDRVA ML C N<3..0> 63
T29DP_80D	T29DP	T29DP	DP SDRVA ML R P<3..0> 63
T29DP_80D	T29DP	T29DP	DP SDRVA ML R N<3..0> 63
DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP SDRVA ML P<0> 63
DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP SDRVA ML N<0> 63
DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP SDRVA ML P<1> 63
DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP SDRVA ML N<1> 63
DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP SDRVA ML P<2> 63
DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP SDRVA ML N<2> 63
DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP SDRVA ML P<3> 63
DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP SDRVA ML N<3> 63
DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP SDRVA AUXCH P 63
DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP SDRVA AUXCH N 63
T29DP_80D	T29DP	T29DP	DP SDRVA AUXCH C P 63
T29DP_80D	T29DP	T29DP	DP SDRVA AUXCH C N 63
T29DPA_ML_ODD			T29DPA ML P<1> 63 64 71
T29DPA_ML_ODD			T29DPA ML N<1> 63 64 71
T29DPA_ML_ODD			T29DPA ML P<3> 63 64 71
T29DPA_ML_ODD			T29DPA ML N<3> 63 64 71
T29DP_80D	T29DP_80D	T29DP	T29DPA ML P<3..0> 63 64 71
T29DP_80D	T29DP_80D	T29DP	T29DPA ML N<3..0> 63 64 71
T29DP_80D	T29DP_80D	T29DP	T29DPA ML C P<3..0> 63 64
T29DP_80D	T29DP_80D	T29DP	T29DPA ML C N<3..0> 63 64
DP_A_EXT_AUXCH	T29DP_80D	T29DP	DP A EXT AUXCH P 63 64
DP_A_EXT_AUXCH	T29DP_80D	T29DP	DP A EXT AUXCH N 63 64

T29/DP Net Properties

T29 IC Net Properties

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








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PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
1T01_DIFFPAIR	*	~STANDARD	~STANDARD	~STANDARD	~STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
 SMBUS_SMC_A_S3_SCL	SMB_50S	SMB	SMBUS_SMC_A_S3_SCL	43
 SMBUS_SMC_A_S3_SDA	SMB_50S	SMB	SMBUS_SMC_A_S3_SDA	43
 SMBUS_SMC_B_S0_SCL	SMB_50S	SMB	SMBUS_SMC_B_S0_SCL	43
 SMBUS_SMC_B_S0_SDA	SMB_50S	SMB	SMBUS_SMC_B_S0_SDA	43
 SMBUS_SMC_0_S0_SCL	SMB_50S	SMB	SMBUS_SMC_0_S0_SCL	43
 SMBUS_SMC_0_S0_SDA	SMB_50S	SMB	SMBUS_SMC_0_S0_SDA	43
 SMBUS_SMC_BSA_SCL	SMB_50S	SMB	SMBUS_SMC_BSA_SCL	43
 SMBUS_SMC_BSA_SDA	SMB_50S	SMB	SMBUS_SMC_BSA_SDA	43
 SMBUS_SMC_MGMT_SCL	SMB_50S	SMB	SMBUS_SMC_MGMT_SCL	43
 SMBUS_SMC_MGMT_SDA	SMB_50S	SMB	SMBUS_SMC_MGMT_SDA	43

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
 CHGR_CSI	1T01_DIFFPAIR		CHGR_CSI_P	52
 CHGR_CSI	1T01_DIFFPAIR		CHGR_CSI_N	52
 CHGR_CSO	1T01_DIFFPAIR		CHGR_CSO_P	52
 CHGR_CSO	1T01_DIFFPAIR		CHGR_CSO_N	52

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SYMC MASTER-CONSTRAINTS

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SMC Constraints

 Apple Inc.

DRAWING NUMBER

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SIZE

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Project Specific Constraints			
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K901 Board-Specific Spacing & Physical Constraints							
BOARD LAYERS				BOARD AREAS		BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM				NO_TYPE, BGA		MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.110 MM	0.090 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.170 MM	0.170 MM			
40_OHM_SE	ISL3, ISL4, ISL9, ISL10	Y	0.140 MM	0.140 MM	=STANDARD	=STANDARD	=STANDARD
40_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP, BOTTOM	Y	0.195 MM	0.1 MM			
37_OHM_SE	ISL3, ISL4, ISL9, ISL10	Y	0.160 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD
37_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP, BOTTOM	Y	0.310 MM	0.2 MM			
27P4_OHM_SE	*	Y	0.250 MM	0.2 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3, ISL10	Y	0.135 MM	0.135 MM		0.130 MM	0.130 MM
72_OHM_DIFF	ISL4, ISL9	Y	0.155MM	0.155 MM		0.130 MM	0.130 MM
72_OHM_DIFF	TOP, BOTTOM	Y	0.165 MM	0.165 MM		0.130 MM	0.130 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3, ISL10	Y	0.095 MM	0.1 MM		0.170 MM	0.170 MM
85_OHM_DIFF	ISL4, ISL9	Y	0.115 MM	0.115 MM		0.170 MM	0.170 MM
85_OHM_DIFF	TOP, BOTTOM	Y	0.130 MM	0.130 MM		0.195 MM	0.195 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3, ISL10	Y	0.089 MM	0.089 MM		0.210 MM	0.210 MM
90_OHM_DIFF	ISL4, ISL9	Y	0.105 MM	0.105 MM		0.210 MM	0.210 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.115 MM	0.115 MM		0.210 MM	0.210 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3, ISL10	Y	0.074 MM	0.074 MM		0.250 MM	0.250 MM
100_OHM_DIFF	ISL4, ISL9	Y	0.085 MM	0.085 MM		0.250 MM	0.250 MM
100_OHM_DIFF	TOP, BOTTOM	Y	0.091 MM	0.091 MM		0.200 MM	0.200 MM

NOTE: 110_DIFF is 110-ohms differential impedance on outer layers and 105-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3, ISL10	N	0.070 MM	0.070 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL4, ISL9	Y	0.071 MM	0.071 MM		0.300 MM	0.300 MM
110_OHM_DIFF	TOP, BOTTOM	Y	0.077 MM	0.077 MM		0.280 MM	0.280 MM

NOTE: These are Intel recommended impedances for PEG, unused on K901.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
48_OHM_SE	TOP, BOTTOM	Y	0.120 MM	0.165 MM			
48_OHM_SE	*	Y	0.097 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3, ISL10	Y	0.110 MM	0.110 MM		0.170 MM	0.170 MM
80_OHM_DIFF	ISL4, ISL9	Y	0.129 MM	0.129 MM		0.170 MM	0.170 MM
80_OHM_DIFF	TOP, BOTTOM	Y	0.145 MM	0.145 MM		0.180 MM	0.180 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?
7X_DIELECTRIC	*	0.490 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_DIFF_BGA	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
85_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
85_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM


NOTE: 85_DIFF_BGA is 85-ohms differential impedance on outer layers and 80-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_DIFF_BGA	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
90_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
90_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 90_DIFF_BGA is 90-ohms differential impedance on outer layers and 85-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

SYMC MASTER-CONSTRAINTS		SYMC DATE=04/06/2011	
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