

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
			2010-07-22

# SCHEM, MLB DVT, K99


07/22/10

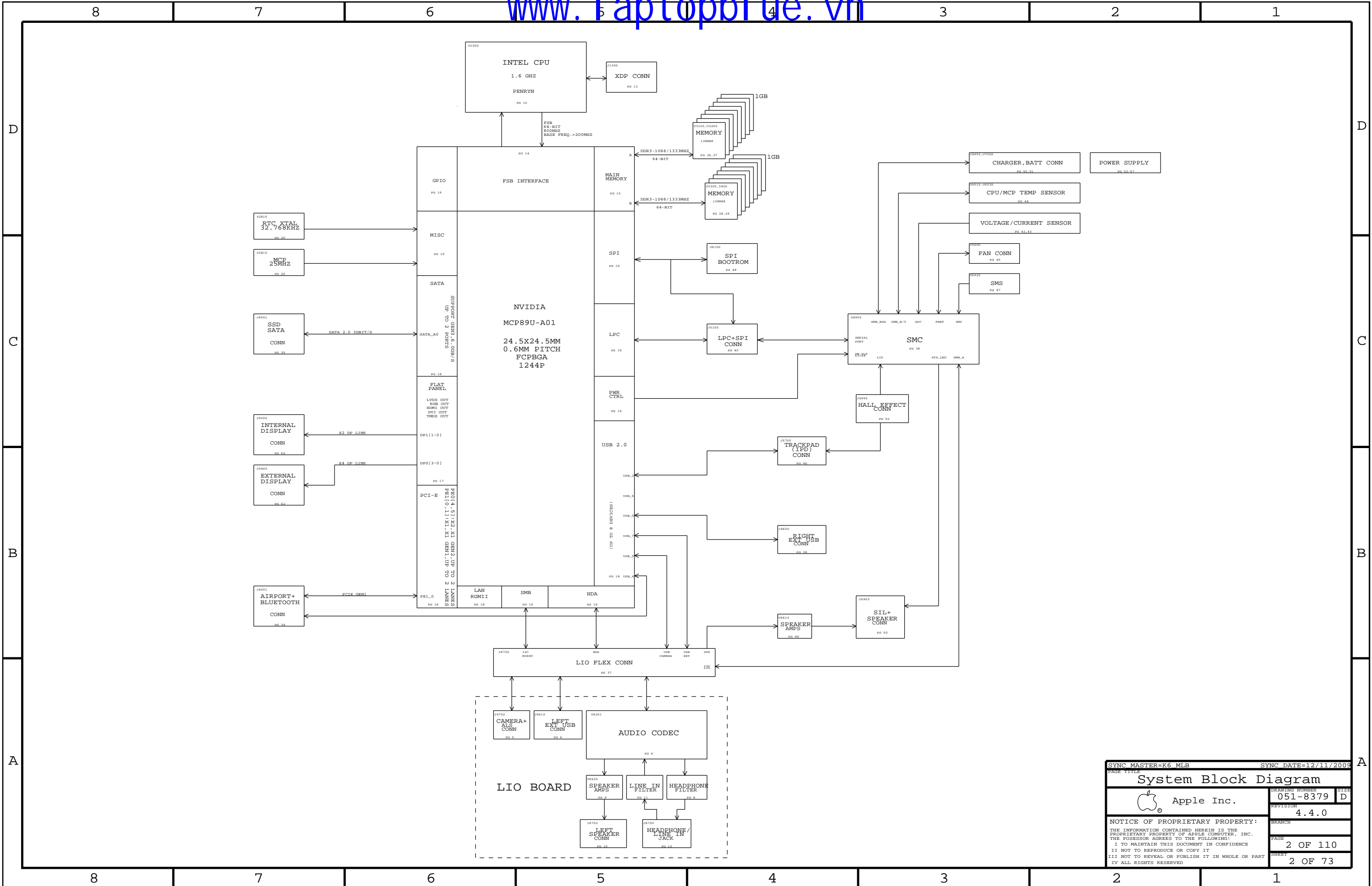
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Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8379	1	SCHEM, MLB, K99	SCH	CRITICAL	
820-2796	1	PCBF, MLB, K99	PCB	CRITICAL	

DRAWING TITLE			
SCHEM, MLB, K99			
 Apple Inc.	DRAWING NUMBER	051-8379	SIZE D
	REVISION	4.4.0	
	BRANCH		
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K99 POWER SYSTEM ARCHITECTURE

Need to update!!!

D

D

C

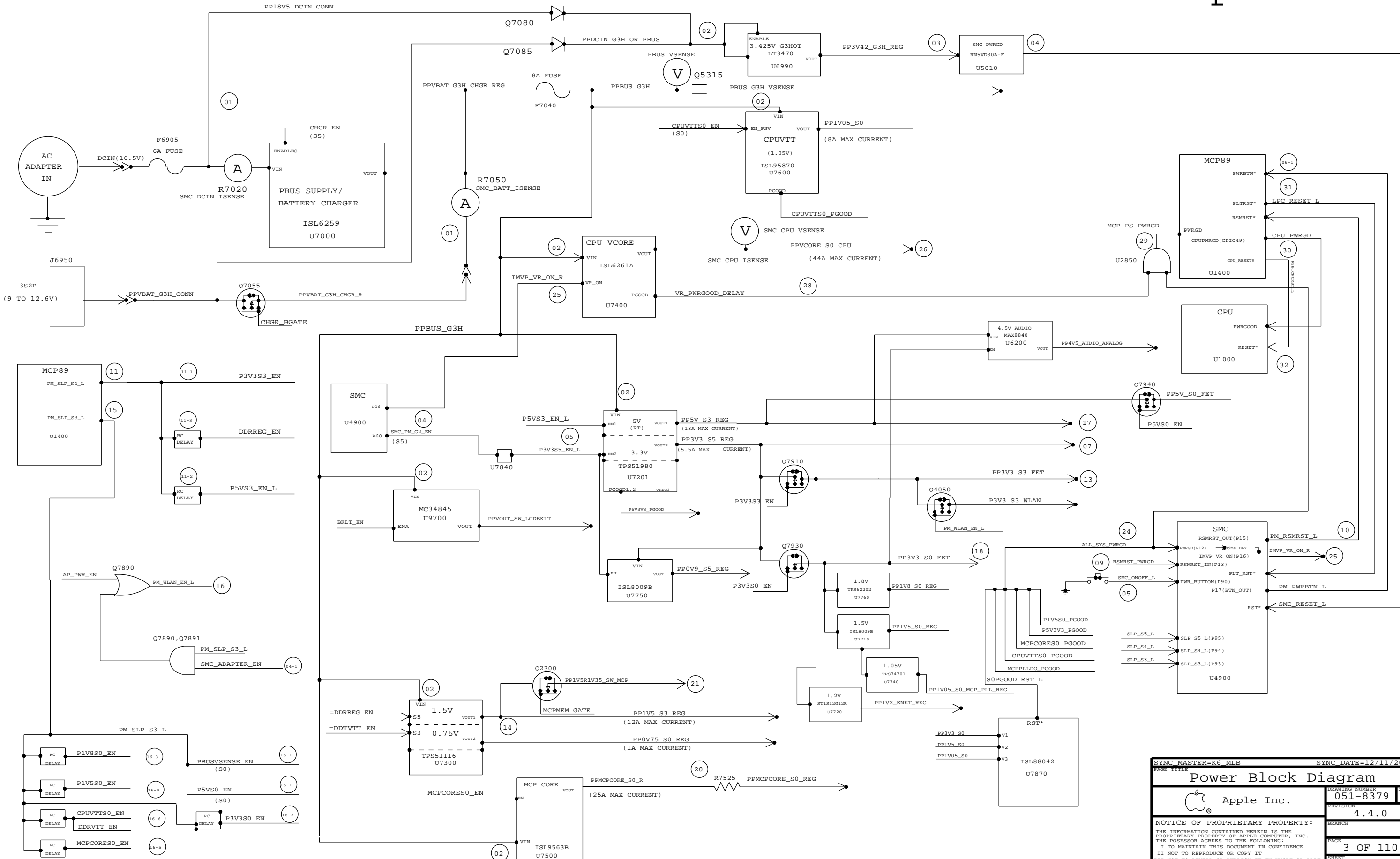
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SYNC MASTER=K6_MLB		SYNC DATE=12/11/2009	
PAGE TITLE			
Power Block Diagram			
	Apple Inc.	DRAWING NUMBER	051-8379
		SIZE	D
		REVISION	4.4.0
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8		7		6		5		4		3		2		1			
BOM Variants						Bar Code Labels / EEE #'						DRAM CFG CHART					
BOM NUMBER		BOM NAME		BOM OPTIONS		PART NUMBER		QTY		DESCRIPTION		REFERENCE DES		CRITICAL		BOM OPTION	
639-0651		PCBA,MLB,HY 2GB,SS CAP,K99		K99_CMNPTS,CPU:1.6GHZ,EEE:DX7,DDR3:HYNIX_2GB,CAPS:SS		825-7557		1		LABEL,MLB,K16/K99		[EEE_DX7]		CRITICAL		EEE:DX7	
639-1055		PCBA,MLB,HY 2GB,MU CAP,K99		K99_CMNPTS,CPU:1.6GHZ,EEE:DD15,DDR3:HYNIX_2GB,CAPS:MU		825-7557		1		LABEL,MLB,K16/K99		[EEE_DD0L]		CRITICAL		EEE:DD0L	
639-1048		PCBA,MLB,HY 2GB,TY CAP,K99		K99_CMNPTS,CPU:1.6GHZ,EEE:DD0X,DDR3:HYNIX_2GB,CAPS:TY		825-7557		1		LABEL,MLB,K16/K99		[EEE_DD0M]		CRITICAL		EEE:DD0M	
639-1043		PCBA,MLB,HY 4GB,SS CAP,K99		K99_CMNPTS,CPU:1.6GHZ,EEE:DD0Q,DDR3:HYNIX_4GB,CAPS:SS		825-7557		1		LABEL,MLB,K16/K99		[EEE_DD0N]		CRITICAL		EEE:DD0N	
639-1044		PCBA,MLB,HY 4GB,MU CAP,K99		K99_CMNPTS,CPU:1.6GHZ,EEE:DD0R,DDR3:HYNIX_4GB,CAPS:MU		825-7557		1		LABEL,MLB,K16/K99		[EEE_DD0P]		CRITICAL		EEE:DD0P	
639-1039		PCBA,MLB,HY 4GB,TY CAP,K99		K99_CMNPTS,CPU:1.6GHZ,EEE:DD0L,DDR3:HYNIX_4GB,CAPS:TY		825-7557		1		LABEL,MLB,K16/K99		[EEE_DD0Q]		CRITICAL		EEE:DD0Q	
639-1045		PCBA,MLB,SA 2GB,SS CAP,K99		K99_CMNPTS,CPU:1.6GHZ,EEE:DD0T,DDR3:SAMSUNG_2GB,CAPS:SS		825-7557		1		LABEL,MLB,K16/K99		[EEE_DD0R]		CRITICAL		EEE:DD0R	
639-1054		PCBA,MLB,SA 2GB,MU CAP,K99		K99_CMNPTS,CPU:1.6GHZ,EEE:DD14,DDR3:SAMSUNG_2GB,CAPS:MU		825-7557		1		LABEL,MLB,K16/K99		[EEE_DD0T]		CRITICAL		EEE:DD0T	
639-1049		PCBA,MLB,SA 2GB,TY CAP,K99		K99_CMNPTS,CPU:1.6GHZ,EEE:DD0Y,DDR3:SAMSUNG_2GB,CAPS:TY		825-7557		1		LABEL,MLB,K16/K99		[EEE_DD0V]		CRITICAL		EEE:DD0V	
639-1052		PCBA,MLB,SA 4GB,SS CAP,K99		K99_CMNPTS,CPU:1.6GHZ,EEE:DD12,DDR3:SAMSUNG_4GB,CAPS:SS		825-7557		1		LABEL,MLB,K16/K99		[EEE_DD0W]		CRITICAL		EEE:DD0W	
639-1046		PCBA,MLB,SA 4GB,MU CAP,K99		K99_CMNPTS,CPU:1.6GHZ,EEE:DD0V,DDR3:SAMSUNG_4GB,CAPS:MU		825-7557		1		LABEL,MLB,K16/K99		[EEE_DD0X]		CRITICAL		EEE:DD0X	
639-1040		PCBA,MLB,SA 4GB,TY CAP,K99		K99_CMNPTS,CPU:1.6GHZ,EEE:DD0M,DDR3:SAMSUNG_4GB,CAPS:TY		825-7557		1		LABEL,MLB,K16/K99		[EEE_DD0Y]		CRITICAL		EEE:DD0Y	
639-1042		PCBA,MLB,MI 2GB,SS CAP,K99		K99_CMNPTS,CPU:1.6GHZ,EEE:DD0P,DDR3:MICRON_2GB,CAPS:SS		825-7557		1		LABEL,MLB,K16/K99		[EEE_DD10]		CRITICAL		EEE:DD10	
639-1053		PCBA,MLB,MI 2GB,MU CAP,K99		K99_CMNPTS,CPU:1.6GHZ,EEE:DD13,DDR3:MICRON_2GB,CAPS:MU		825-7557		1		LABEL,MLB,K16/K99		[EEE_DD11]		CRITICAL		EEE:DD11	
639-1047		PCBA,MLB,MI 2GB,TY CAP,K99		K99_CMNPTS,CPU:1.6GHZ,EEE:DD0W,DDR3:MICRON_2GB,CAPS:TY		825-7557		1		LABEL,MLB,K16/K99		[EEE_DD12]		CRITICAL		EEE:DD12	
639-1051		PCBA,MLB,MI 4GB,SS CAP,K99		K99_CMNPTS,CPU:1.6GHZ,EEE:DD11,DDR3:MICRON_4GB,CAPS:SS		825-7557		1		LABEL,MLB,K16/K99		[EEE_DD13]		CRITICAL		EEE:DD13	
639-1041		PCBA,MLB,MI 4GB,MU CAP,K99		K99_CMNPTS,CPU:1.6GHZ,EEE:DD0N,DDR3:MICRON_4GB,CAPS:MU		825-7557		1		LABEL,MLB,K16/K99		[EEE_DD14]		CRITICAL		EEE:DD14	
639-1050		PCBA,MLB,MI 4GB,TY CAP,K99		K99_CMNPTS,CPU:1.6GHZ,EEE:DD10,DDR3:MICRON_4GB,CAPS:TY		825-7557		1		LABEL,MLB,K16/K99		[EEE_DD15]		CRITICAL		EEE:DD15	
639-1446		PCBA,MLB,1.6GHZ,EL 2GB,SS CAP,K99		K99_CMNPTS,CPU:1.6GHZ,EEE:DG4Q,DDR3:ELPIDA_2GB,CAPS:SS		825-7557		1		LABEL,MLB,K16/K99		[EEE_DF82]		CRITICAL		EEE:DF82	
639-1438		PCBA,MLB,1.6GHZ,EL 2GB,MU CAP,K99		K99_CMNPTS,CPU:1.6GHZ,EEE:DG4G,DDR3:ELPIDA_2GB,CAPS:MU		825-7557		1		LABEL,MLB,K16/K99		[EEE_DF83]		CRITICAL		EEE:DF83	
639-1444		PCBA,MLB,1.6GHZ,EL 2GB,TY CAP,K99		K99_CMNPTS,CPU:1.6GHZ,EEE:DG4N,DDR3:ELPIDA_2GB,CAPS:TY		825-7557		1		LABEL,MLB,K16/K99		[EEE_DF84]		CRITICAL		EEE:DF84	
639-1449		PCBA,MLB,1.6GHZ,EL 4GB,SS CAP,K99		K99_CMNPTS,CPU:1.6GHZ,EEE:DG4V,DDR3:ELPIDA_4GB,CAPS:SS		825-7557		1		LABEL,MLB,K16/K99		[EEE_DF85]		CRITICAL		EEE:DF85	
639-1448		PCBA,MLB,1.6GHZ,EL 4GB,MU CAP,K99		K99_CMNPTS,CPU:1.6GHZ,EEE:DG4T,DDR3:ELPIDA_4GB,CAPS:MU		825-7557		1		LABEL,MLB,K16/K99		[EEE_DF86]		CRITICAL		EEE:DF86	
639-1445		PCBA,MLB,1.6GHZ,EL 4GB,TY CAP,K99		K99_CMNPTS,CPU:1.6GHZ,EEE:DG4P,DDR3:ELPIDA_4GB,CAPS:TY		825-7557		1		LABEL,MLB,K16/K99		[EEE_DF87]		CRITICAL		EEE:DF87	
607-6999		CMN PTS,PCBA,MLB,K99		K99_COMMON		825-7557		1		LABEL,MLB,K16/K99		[EEE_DF88]		CRITICAL		EEE:DF88	
085-1121		K99 MLB DEVELOPMENT BOM		K99_DEVEL:ENG		825-7557		1		LABEL,MLB,K16/K99		[EEE_DF89]		CRITICAL		EEE:DF89	
639-1355		PCBA,MLB,1.4GHZ,HY 2GB,SS CAP,K99		K99_CMNPTS,CPU:1.4GHZ,EEE:DF8L,DDR3:HYNIX_2GB,CAPS:SS		825-7557		1		LABEL,MLB,K16/K99		[EEE_DF8C]		CRITICAL		EEE:DF8C	
639-1341		PCBA,MLB,1.4GHZ,HY 2GB,MU CAP,K99		K99_CMNPTS,CPU:1.4GHZ,EEE:DF83,DDR3:HYNIX_2GB,CAPS:MU		825-7557		1		LABEL,MLB,K16/K99		[EEE_DF8D]		CRITICAL		EEE:DF8D	
639-1353		PCBA,MLB,1.4GHZ,HY 2GB,TY CAP,K99		K99_CMNPTS,CPU:1.4GHZ,EEE:DF8J,DDR3:HYNIX_2GB,CAPS:TY		825-7557		1		LABEL,MLB,K16/K99		[EEE_DF8F]		CRITICAL		EEE:DF8F	
639-1350		PCBA,MLB,1.4GHZ,HY 4GB,SS CAP,K99		K99_CMNPTS,CPU:1.4GHZ,EEE:DF8F,DDR3:HYNIX_4GB,CAPS:SS		825-7557		1		LABEL,MLB,K16/K99		[EEE_DF8G]		CRITICAL		EEE:DF8G	
639-1356		PCBA,MLB,1.4GHZ,HY 4GB,MU CAP,K99		K99_CMNPTS,CPU:1.4GHZ,EEE:DF8M,DDR3:HYNIX_4GB,CAPS:MU		825-7557		1		LABEL,MLB,K16/K99		[EEE_DF8H]		CRITICAL		EEE:DF8H	
639-1348		PCBA,MLB,1.4GHZ,HY 4GB,TY CAP,K99		K99_CMNPTS,CPU:1.4GHZ,EEE:DF8C,DDR3:HYNIX_4GB,CAPS:TY		825-7557		1		LABEL,MLB,K16/K99		[EEE_DF8J]		CRITICAL		EEE:DF8J	
639-1349		PCBA,MLB,1.4GHZ,SA 2GB,SS CAP,K99		K99_CMNPTS,CPU:1.4GHZ,EEE:DF8D,DDR3:SAMSUNG_2GB,CAPS:SS		825-7557		1		LABEL,MLB,K16/K99		[EEE_DF8K]		CRITICAL		EEE:DF8K	
639-1351		PCBA,MLB,1.4GHZ,SA 2GB,MU CAP,K99		K99_CMNPTS,CPU:1.4GHZ,EEE:DF8G,DDR3:SAMSUNG_2GB,CAPS:MU		825-7557		1		LABEL,MLB,K16/K99		[EEE_DF8L]		CRITICAL		EEE:DF8L	
639-1357		PCBA,MLB,1.4GHZ,SA 2GB,TY CAP,K99		K99_CMNPTS,CPU:1.4GHZ,EEE:DF8N,DDR3:SAMSUNG_2GB,CAPS:TY		825-7557		1		LABEL,MLB,K16/K99		[EEE_DF8M]		CRITICAL		EEE:DF8M	
639-1344		PCBA,MLB,1.4GHZ,SA 4GB,SS CAP,K99		K99_CMNPTS,CPU:1.4GHZ,EEE:DF86,DDR3:SAMSUNG_4GB,CAPS:SS		825-7557		1		LABEL,MLB,K16/K99		[EEE_DF8N]		CRITICAL		EEE:DF8N	
639-1352		PCBA,MLB,1.4GHZ,SA 4GB,MU CAP,K99		K99_CMNPTS,CPU:1.4GHZ,EEE:DF8H,DDR3:SAMSUNG_4GB,CAPS:MU		825-7557		1		LABEL,MLB,K16/K99		[EEE_DG4G]		CRITICAL		EEE:DG4G	
639-1354		PCBA,MLB,1.4GHZ,SA 4GB,TY CAP,K99		K99_CMNPTS,CPU:1.4GHZ,EEE:DF8K,DDR3:SAMSUNG_4GB,CAPS:TY		825-7557		1		LABEL,MLB,K16/K99		[EEE_DG4H]		CRITICAL		EEE:DG4H	
639-1342		PCBA,MLB,1.4GHZ,MI 2GB,SS CAP,K99		K99_CMNPTS,CPU:1.4GHZ,EEE:DF84,DDR3:MICRON_2GB,CAPS:SS		825-7557		1		LABEL,MLB,K16/K99		[EEE_DG4J]		CRITICAL		EEE:DG4J	
639-1346		PCBA,MLB,1.4GHZ,MI 2GB,MU CAP,K99		K99_CMNPTS,CPU:1.4GHZ,EEE:DF88,DDR3:MICRON_2GB,CAPS:MU		825-7557		1		LABEL,MLB,K16/K99		[EEE_DG4K]		CRITICAL		EEE:DG4K	
639-1343		PCBA,MLB,1.4GHZ,MI 2GB,TY CAP,K99		K99_CMNPTS,CPU:1.4GHZ,EEE:DF85,DDR3:MICRON_2GB,CAPS:TY		825-7557		1		LABEL,MLB,K16/K99		[EEE_DG4M]		CRITICAL		EEE:DG4M	
639-1347		PCBA,MLB,1.4GHZ,MI 4GB,SS CAP,K99		K99_CMNPTS,CPU:1.4GHZ,EEE:DF89,DDR3:MICRON_4GB,CAPS:SS		825-7557		1		LABEL,MLB,K16/K99		[EEE_DG4N]		CRITICAL		EEE:DG4N	
639-1345		PCBA,MLB,1.4GHZ,MI 4GB,MU CAP,K99		K99_CMNPTS,CPU:1.4GHZ,EEE:DF87,DDR3:MICRON_4GB,CAPS:MU		825-7557		1		LABEL,MLB,K16/K99		[EEE_DG4P]		CRITICAL		EEE:DG4P	
639-1340		PCBA,MLB,1.4GHZ,MI 4GB,TY CAP,K99		K99_CMNPTS,CPU:1.4GHZ,EEE:DF82,DDR3:MICRON_4GB,CAPS:TY		825-7557		1		LABEL,MLB,K16/K99		[EEE_DG4Q]		CRITICAL		EEE:DG4Q	
639-1442		PCBA,MLB,1.4GHZ,EL 2GB,SS CAP,K99		K99_CMNPTS,CPU:1.4GHZ,EEE:DG4L,DDR3:ELPIDA_2GB,CAPS:SS		825-7557		1		LABEL,MLB,K16/K99		[EEE_DG4R]		CRITICAL		EEE:DG4R	
639-1443		PCBA,MLB,1.4GHZ,EL 2GB,MU CAP,K99		K99_CMNPTS,CPU:1.4GHZ,EEE:DG4M,DDR3:ELPIDA_2GB,CAPS:MU		825-7557		1		LABEL,MLB,K16/K99		[EEE_DG4L]		CRITICAL		EEE:DG4L	
639-1447		PCBA,MLB,1.4GHZ,EL 2GB,TY CAP,K99		K99_CMNPTS,CPU:1.4GHZ,EEE:DG4R,DDR3:ELPIDA_2GB,CAPS:TY		825-7557		1		LABEL,MLB,K16/K99		[EEE_DG4T]		CRITICAL		EEE:DG4T	
639-1441		PCBA,MLB,1.4GHZ,EL 4GB,SS CAP,K99		K99_CMNPTS,CPU:1.4GHZ,EEE:DG4K,DDR3:ELPIDA_4GB,CAPS:SS		825-7557		1		LABEL,MLB,K16/K99		[EEE_DG4V]		CRITICAL		EEE:DG4V	
639-1439		PCBA,MLB,1.4GHZ,EL 4GB,MU CAP,K99		K99_CMNPTS,CPU:1.4GHZ,EEE:DG4H,DDR3:ELPIDA_4GB,CAPS:MU		825-7557		1		LABEL,MLB,K16/K99		[EEE_DG4V]		CRITICAL		EEE:DG4V	
639-1440		PCBA,MLB,1.4GHZ,EL 4GB,TY CAP,K99		K99_CMNPTS,CPU:1.4GHZ,EEE:DG4J,DDR3:ELPIDA_4GB,CAPS:TY		825-7557		1		LABEL,MLB,K16/K99		[EEE_DG4V]		CRITICAL		EEE:DG4V	
Sub-BOMs																	
PART NUMBER		QTY		DESCRIPTION		REFERENCE DES		CRITICAL		BOM OPTION							
085-1121		1		K99 MLB DEVELOPMENT BOM		DEVEL		CRITICAL		DEVEL_BOM							
607-6999		1		CMN PTS,PCBA,MLB,K99		CMNPTS		CRITICAL		K99_CMNPTS							
SYNC MASTER=K6 MLB						SYNC DATE=12/11/2009											
PAGE TITLE						K99 BOM Variants											
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[illegible]

Functional Test Points

Fan Connectors

PP5V	TRUE	PP5V_S0	7 8 57
FAN	TRUE	FAN_RT_PWM	45
FAN	TRUE	FAN_RT_TACH	45

(NEED TO ADD 1 GND TP)

SPEAKER FUNC\_TEST

SPKR	TRUE	SPKRAMP_R_N_OUT	48 49
SPKR	TRUE	SPKRAMP_R_P_OUT	48 49

INT DP FUNC\_TEST

PP3V3	TRUE	PP3V3_SW_LCD	7 59 (NEED 2 TP)
-------	------	--------------	------------------

PPVOUT	TRUE	PPVOUT_SW_LCDBKLT	2, 42 59 (NEED 2 TP)
DP	TRUE	DP_INT_ML_F_N<0>	59 71
DP	TRUE	DP_INT_ML_F_P<0>	59 71
DP	TRUE	DP_INT_ML_F_N<1>	59 71
DP	TRUE	DP_INT_ML_F_P<1>	59 71
DP	TRUE	DP_INT_AUX_CH_C_N	59 71
DP	TRUE	DP_INT_AUX_CH_C_P	59 71
DP	TRUE	DP_INT_HPD_CONN	59
LED	TRUE	LED_RETURN_1	59 62
LED	TRUE	LED_RETURN_2	59 62
LED	TRUE	LED_RETURN_3	59 62
LED	TRUE	LED_RETURN_4	59 62
LED	TRUE	LED_RETURN_5	59 62
LED	TRUE	LED_RETURN_6	59 62
I2C	TRUE	=I2C_TCON_SCL	41 59
I2C	TRUE	=I2C_TCON_SDA	41 59

(NEED TO ADD 5 GND TP)

HALL EFFECT CONN (PLACEHOLDER)

SMC	TRUE	SMC_LID_R	49
PP3V42	TRUE	=PP3V42_G3H_HALL	8 49

SATA HDD

PP3V3	TRUE	PP3V3_S0_HDD_R	(NEED 5 TP) 7 35
SATA	TRUE	SATA_HDD_R2D_P	35 67
SATA	TRUE	SATA_HDD_R2D_N	35 67
SATA	TRUE	SATA_HDD_D2R_C_P	35 67
SATA	TRUE	SATA_HDD_D2R_C_N	35 67
SMC	TRUE	SMC_HDD_OOB_TEMP	35 38
SMC	TRUE	SMC_HDD_TEMP_CTL	35 38

(NEED TO ADD 6 GND TP)

BATT POWER CONN

SMBUS	TRUE	SMBUS_SMC_BSA_SCL	41 70
SMBUS	TRUE	SMBUS_SMC_BSA_SDA	41 70
SYS	TRUE	SYS_DETECT_L	49
PPVBAT	TRUE	PPVBAT_G3H_CONN	49 (NEED 4 TP) 50

(NEED TO ADD 4 GND TP NEAR J6950 AND 1 FOR SHIELD)

LIO CONNECTOR

=PP3V3	TRUE	=PP3V3_S0_AUDIO	37 (NEED 2 TP)
=PP3V42	TRUE	=PP3V42_G3H_ONEWIRE	8 37
SMC	TRUE	SMC_BC_ACOK	9 37 38 39
SYS	TRUE	SYS_ONEWIRE	37 38
=USB	TRUE	=USB_PWR_EN	36 37 57
USB	TRUE	USB_EXTD_OC_L	18 37
USB	TRUE	USB_CAMERA_P	18 37 68
USB	TRUE	USB_CAMERA_N	18 37 68
USB	TRUE	USB_EXTD_P	18 37 68
USB	TRUE	USB_EXTD_N	18 37 68
=PPIV8R1V5	TRUE	=PPIV8R1V5_S0_AUDIO	8 37
=I2C	TRUE	=I2C_LIO_SDA	37 41
=I2C	TRUE	=I2C_LIO_SCL	37 41
AUD	TRUE	AUD_GPIO_3	37 48
AUD	TRUE	AUD_I2C_INT_L	19 37
=I2C	TRUE	=I2C_MIKEY_SDA	37 41
=I2C	TRUE	=I2C_MIKEY_SCL	37 41
AUD	TRUE	AUD_IP_PERIPHERAL_DET	17 37
SPKRAMP	TRUE	SPKRAMP_INR_P	37 48 71
SPKRAMP	TRUE	SPKRAMP_INR_N	37 48 71
HDA	TRUE	HDA_SDIN0	19 37 68
HDA	TRUE	HDA_SDOUT	19 37 68
HDA	TRUE	HDA_BIT_CLK	19 37 68
HDA	TRUE	HDA_SYNC	19 37 68
HDA	TRUE	HDA_RST_L	19 37 68
AUD	TRUE	AUD_IPHS_SWITCH_EN	19 37

(NEED TO ADD 5 GND TP)

AIRPORT / BT

PCIE	TRUE	PCIE_AP_R2D_P	34 67
PCIE	TRUE	PCIE_AP_R2D_N	34 67
PCIE	TRUE	PCIE_AP_D2R_P	16 34 67
PCIE	TRUE	PCIE_AP_D2R_N	16 34 67
PCIE	TRUE	PCIE_CLK100M_AP_P	16 34 67
PCIE	TRUE	PCIE_CLK100M_AP_N	16 34 67
USB	TRUE	USB_BT_P	18 34 68
USB	TRUE	USB_BT_N	18 34 68
WIFI	TRUE	WIFI_EVENT_L	34 38 39
=PP3V3	TRUE	=PP3V3_S3_BT	8 34
PP3V3	TRUE	PP3V3_WLAN_F	(NEED 6 TP) 7 34 39
PCIE	TRUE	PCIE_WAKE_L	16 34
AP	TRUE	AP_RESET_CONN_L	34
AP	TRUE	AP_CLKREQ_O_L	34

(NEED TO ADD 8 GND TP)

IPD\_FLEX\_CONN

SMC	TRUE	SMC_TPAD_RST_L	39 46
SMC	TRUE	SMC_LID	38 39 46 49
SMC	TRUE	SMC_ONOFF_L	38 39 46
=I2C	TRUE	=I2C_TPAD_SCL	41 46
=I2C	TRUE	=I2C_TPAD_SDA	41 46
=PP3V42	TRUE	=PP3V42_G3H_TPAD	8 46
PP3V3	TRUE	PP3V3_TPAD_CONN	46
PP5V	TRUE	PP5V_TPAD_FILT	46
USB	TRUE	USB_TPAD_CONN_N	46 71
USB	TRUE	USB_TPAD_CONN_P	46 71

(NEED TO ADD 5 GND TP)

LCP + SPI CONN

=PP3V3	TRUE	=PP3V3_S5_LPCPLUS	8 40
=PP5V	TRUE	=PP5V_S0_LPCPLUS	8 40
LPC	TRUE	LPC_AD<3..0>	19 38 40 68
SPI	TRUE	SPI_ALT_MOSI	40 68
SPI	TRUE	SPI_ALT_MISO	40 68
LPC	TRUE	LPC_FRAME_L	19 38 40 68
PM	TRUE	PM_CLKRUN_L	19 38 40
SMC	TRUE	SMC_TMS	38 39 40
LPCPLUS	TRUE	LPCPLUS_RESET_L	25 40
SMC	TRUE	SMC_TDO	38 39 40
SMC	TRUE	SMC_TRST_L	38 40
SMC	TRUE	SMC_MD1	38 40
SMC	TRUE	SMC_TX_L	36 38 39 40
LPC	TRUE	LPC_CLK33M_LPCPLUS	25 40 68
SPIROM	TRUE	SPIROM_USE_MLB	19 40 47
SPI	TRUE	SPI_ALT_CLK	40 68
SPI	TRUE	SPI_ALT_CS_L	40 68
LPC	TRUE	LPC_SERIRO	19 38 40
LPC	TRUE	LPC_PWRDWN_L	19 38 40
SMC	TRUE	SMC_TDI	38 39 40
SMC	TRUE	SMC_TCK	38 39 40
SMC	TRUE	SMC_RESET_L	38 39 40 50
SMC	TRUE	SMC_NMI	38 40
SMC	TRUE	SMC_RX_L	36 38 39 40
LPCPLUS	TRUE	LPCPLUS_GPIO	19 40

(NEED TO ADD 6 GND TP)

DC POWER CONN

=PP18V5	TRUE	=PP18V5_DCIN_CONN	(NEED 6 TP) 8 49
=PP5V	TRUE	=PP5V_S3_LIO_CONN	8 49

(NEED TO ADD 6 GND TP)


DEBUG VOLTAGE

PPVCORE	TRUE	PPVCORE_S0_CPU	8 42
PPVCORE	TRUE	PPVCORE_S0_MCP	8 42
PP1V05	TRUE	PP1V05_S0	8 57
PP1V5	TRUE	PP1V5_S0	8 57 71
PP3V3	TRUE	PP3V3_S0	8 57 71
PP5V	TRUE	PP5V_S0	7 8 57
PP3V3	TRUE	PP3V3_S3	8
PP5V	TRUE	PP5V_S3	8
PP0V9	TRUE	PP0V9_S5	8
PP3V3	TRUE	PP3V3_S5	8 57 71
PP3V42	TRUE	PP3V42_G3H	8
PPBUS	TRUE	PPBUS_G3H	8 42 49
PP3V3	TRUE	PP3V3_WLAN_F	7 34 39
PP3V3	TRUE	PP3V3_S0_HDD_R	7 35
PPDCIN	TRUE	PPDCIN_S5_S5	8
PPVOUT	TRUE	PPVOUT_SW_LCDBKLT	7 42 59 62
PP3V3	TRUE	PP3V3_SW_LCD	7 59
PP1V5R1V35	TRUE	PP1V5R1V35_S3	8 71
SMC	TRUE	SMC_PM_G2_EN	38 57
PM	TRUE	PM_SLP_S4_L	19 38 57
PM	TRUE	PM_SLP_S3_L	19 38 39 57
PP0V9	TRUE	PP0V9_ENET	8
PP1V05	TRUE	PP1V05_S0_MCP_PLL_UF	8
PP3V3	TRUE	PP3V3_ENET	8
PP3V3	TRUE	PP3V3_SW_DPPWR	61
PP5V	TRUE	PP5V_S3_RTUSB_A_F	36
PPBUS	TRUE	PPBUS_G3H_ISNS	8

(NEED TO ADD 27 GND TP)

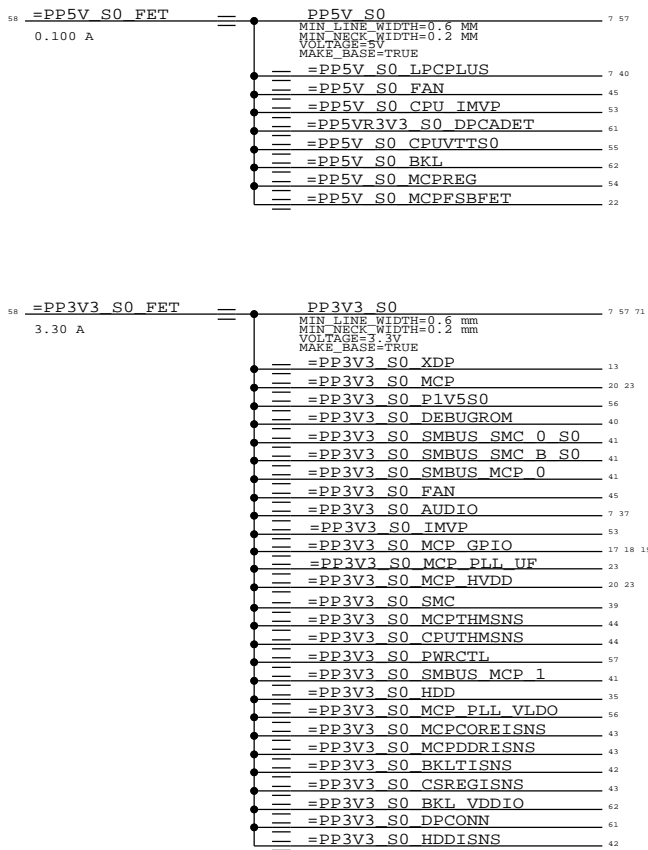
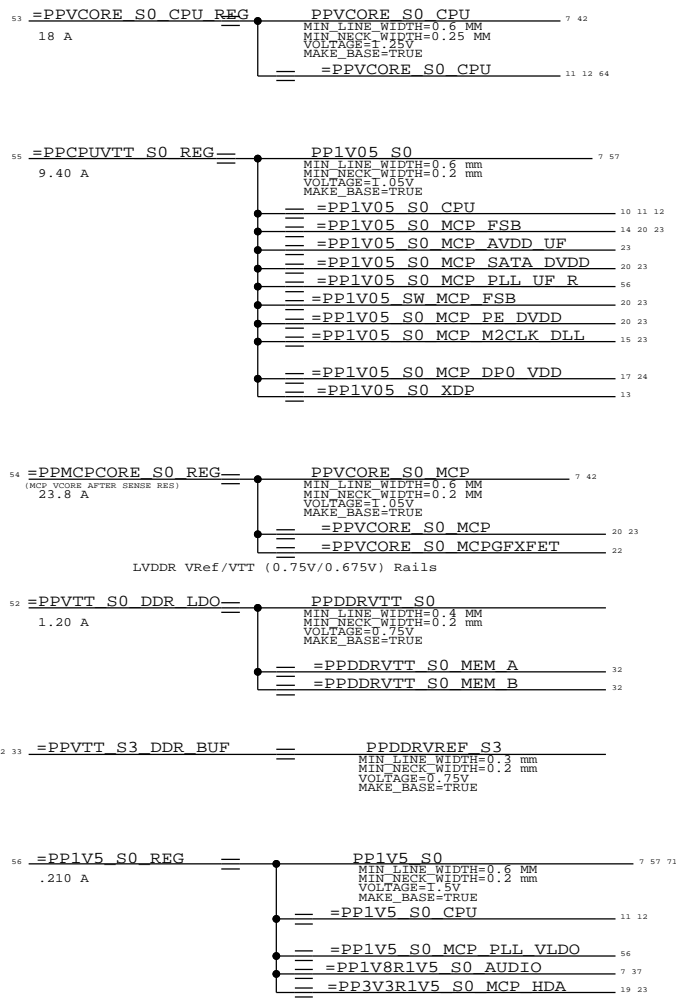
FSB SIGNALS WITH NOTEST

NO_TEST=TRUE	FSB_A_L<35..3>	10 14 65
NO_TEST=TRUE	FSB_ADS_L	10 14 65
NO_TEST=TRUE	FSB_ADSTB_L<1..0>	10 14 65
NO_TEST=TRUE	FSB_D_L<63..0>	10 14 65
NO_TEST=TRUE	FSB_DINV_L<3..0>	10 14 65
NO_TEST=TRUE	FSB_DSTB_L_N<3..0>	10 14 65
NO_TEST=TRUE	FSB_DSTB_L_P<3..0>	10 14 65
NO_TEST=TRUE	FSB_HIT_L	10 14 65
NO_TEST=TRUE	FSB_HITM_L	10 14 65
NO_TEST=TRUE	FSB_LOCK_L	10 14 65
NO_TEST=TRUE	FSB_REO_L<4..0>	10 14 65

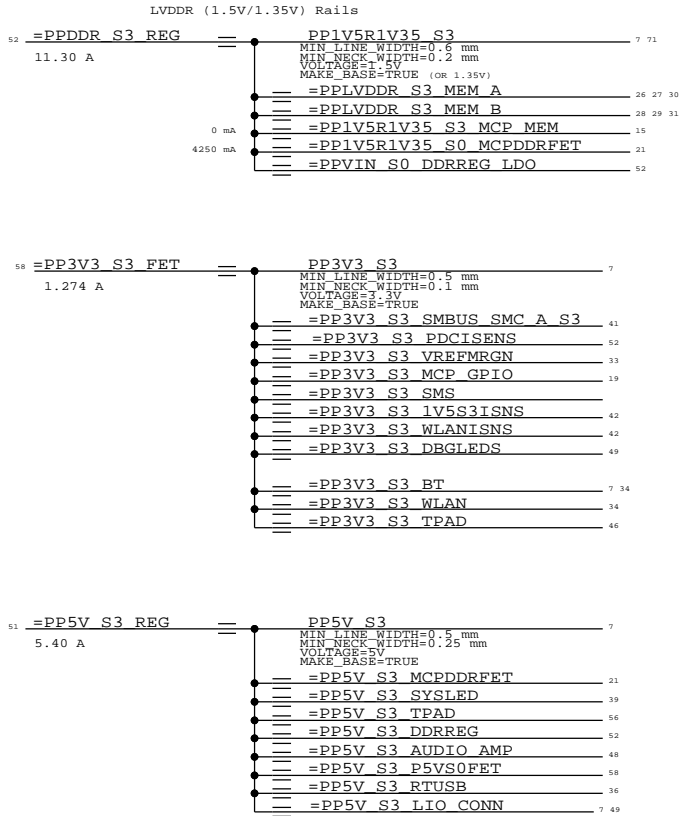
SYNC MASTER=K6_MLB		SYNC DATE=12/11/2009	
PAGE TITLE			
FUNCTIONAL TEST			
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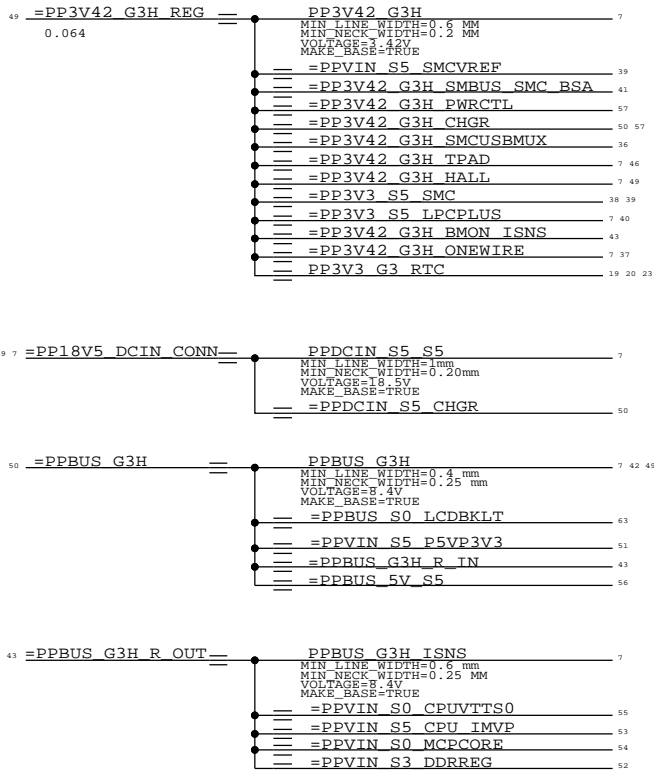
"S0,S0M" RAILS



"S3" RAILS



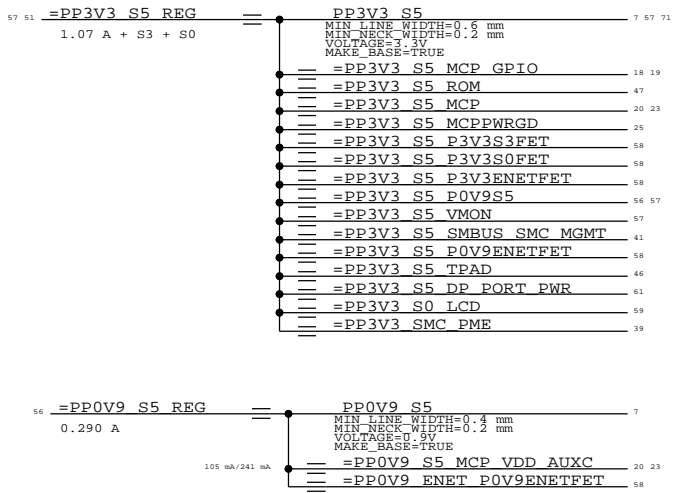
"G3H" RAILS




"ENET" RAILS

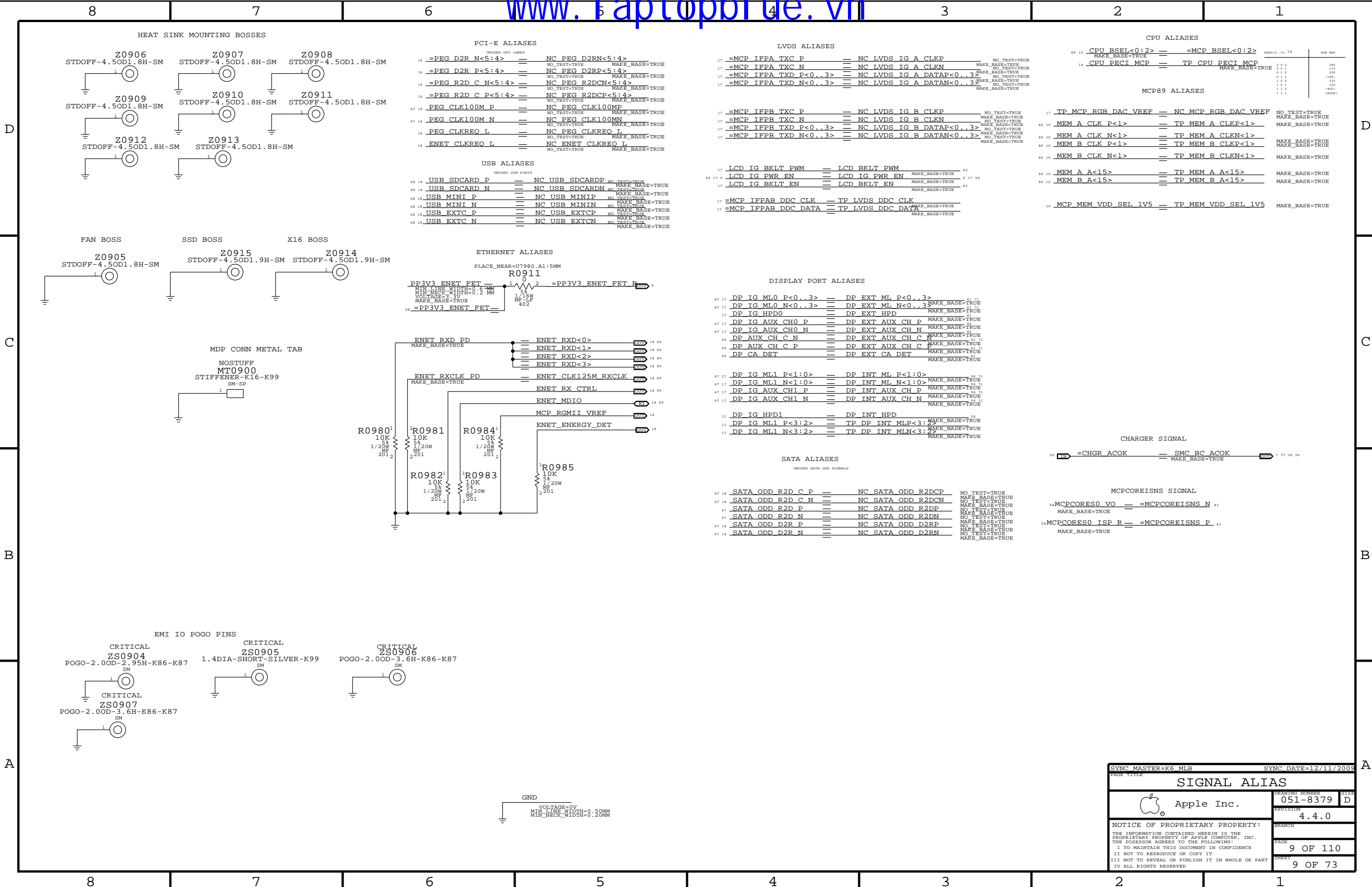


"S5" RAILS




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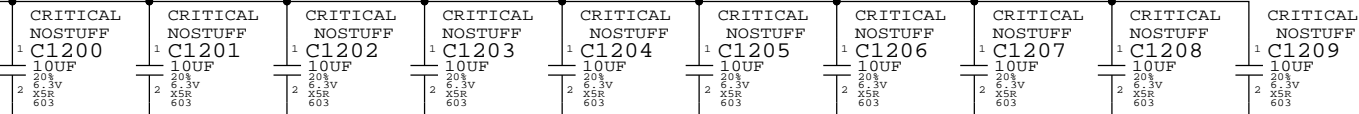




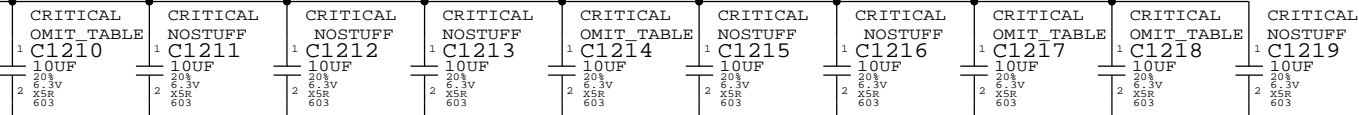
# CPU VCORE HF AND BULK DECOUPLING

4x 270uF. 32x 10uF 0603, 28x 2.2uF 0402 + 40x 2.2uF 0402

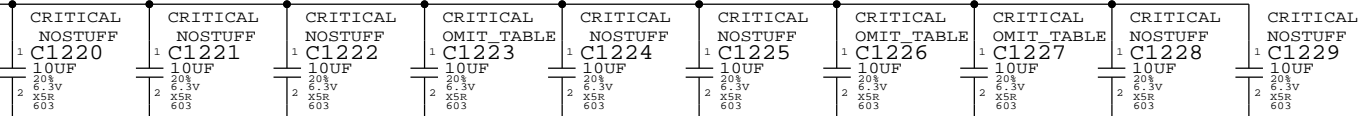
LAYOUT NOTE:  
PLACE ON OPPOSITE SIDE OF CPU



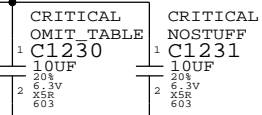
LAYOUT NOTE:  
PLACE ON OPPOSITE SIDE OF CPU



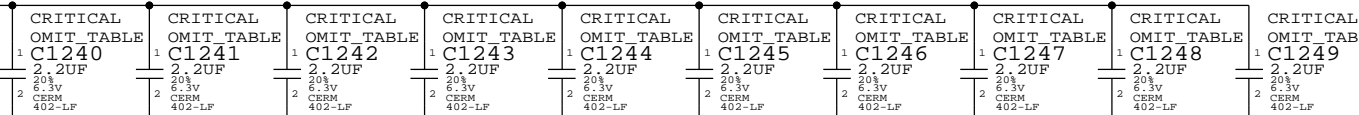
LAYOUT NOTE:  
PLACE ON OPPOSITE SIDE OF CPU



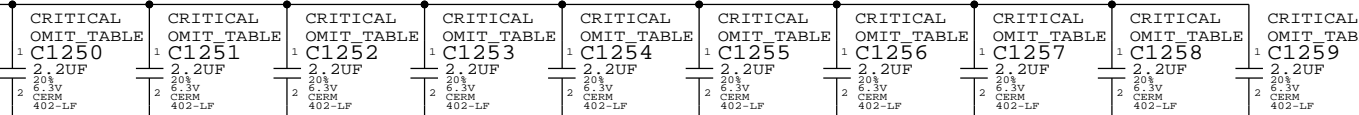
LAYOUT NOTE:  
PLACE ON OPPOSITE SIDE OF CPU



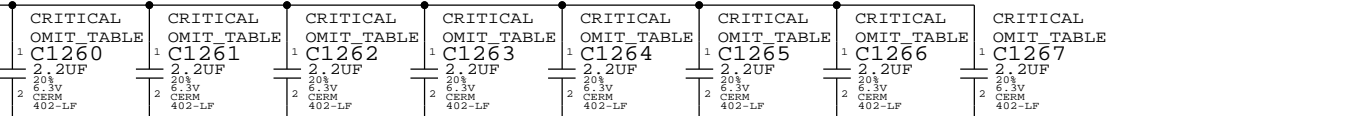
LAYOUT NOTE:  
PLACE ON OPPOSITE SIDE OF CPU



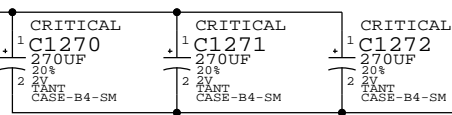
LAYOUT NOTE:  
PLACE ON OPPOSITE SIDE OF CPU



LAYOUT NOTE:  
PLACE ON OPPOSITE SIDE OF CPU



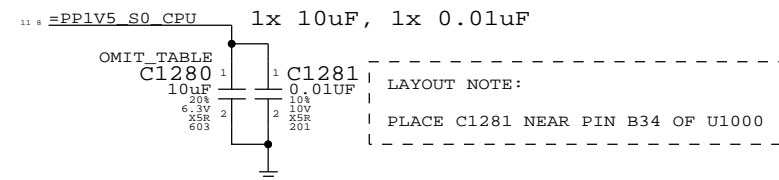
LAYOUT NOTE:  
PLACE ON SAME SIDE AS CPU



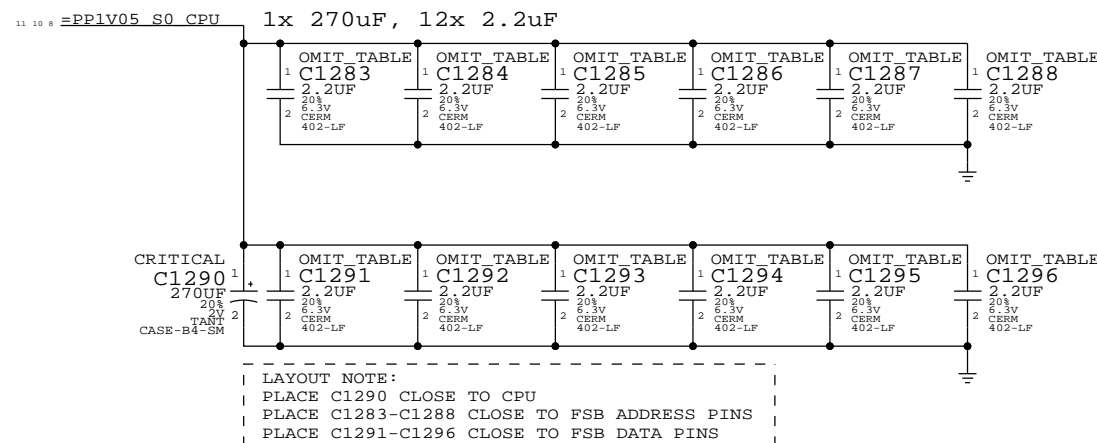
## CPU VCORE VID CONNECTIONS

CPU VID<0..6> = IMVP6\_VID<0..6>

## VCCA (CPU AVdd) DECOUPLING



## VCCP (CPU I/O) DECOUPLING

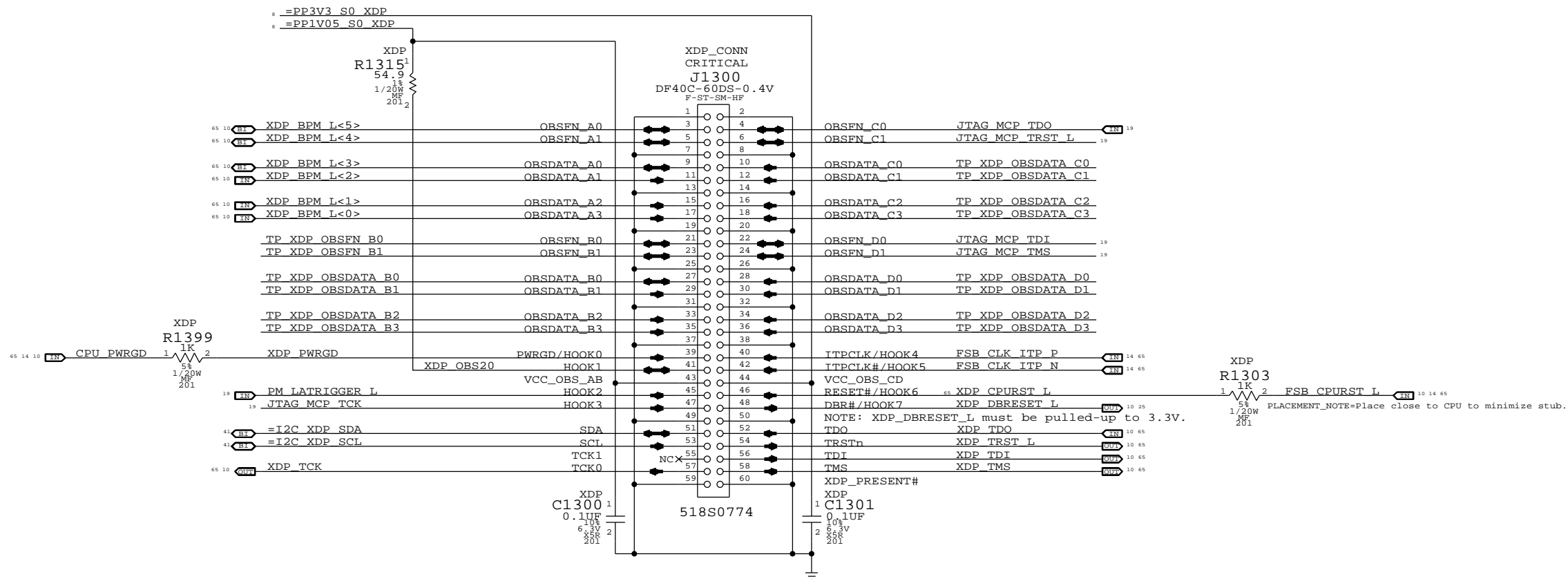




# Micro2-XDP Connector

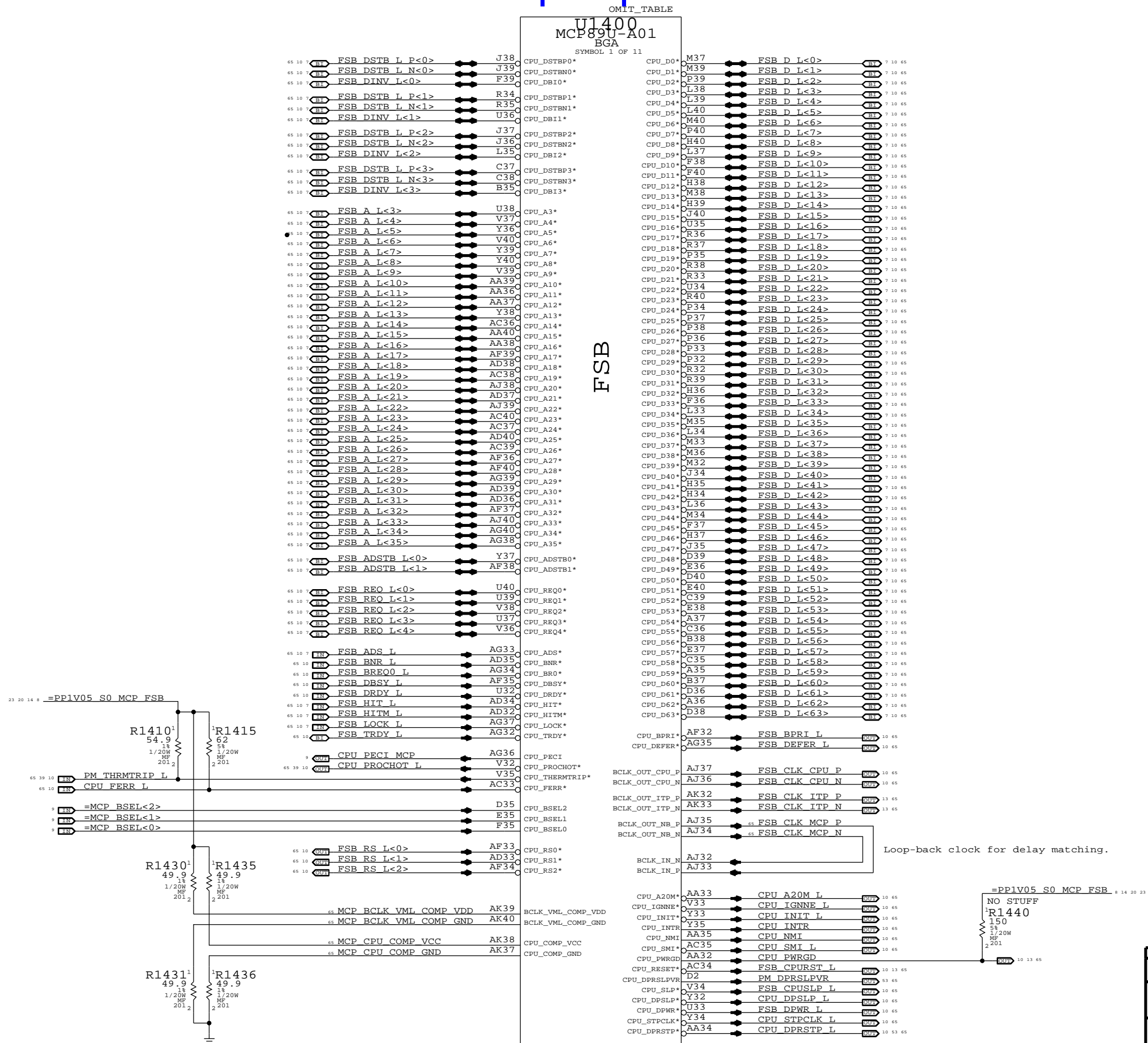
NOTE: This is not the standard XDP pinout.


Use with 920-0782 Adapter Flex to support chipset debug.



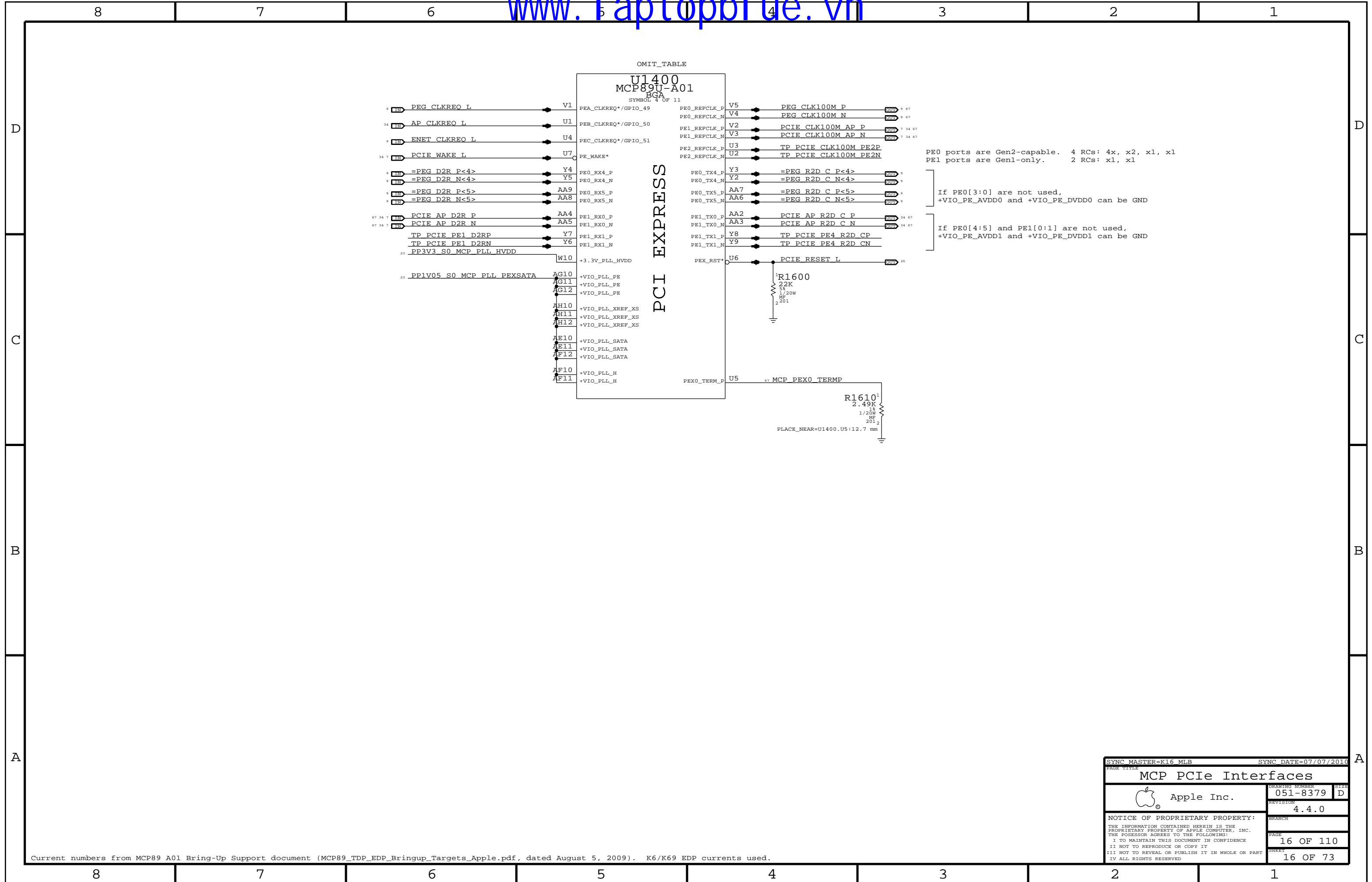
Direction of XDP adapter flex

Please place J1300 within 1" of board edge with odd-numbered pins facing edge. Avoid any tall components between J1300 and edge.



SYNC MASTER=K16 ML6		SYNC DATE=07/07/2010	
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MCP CPU Interface			
 Apple Inc.	DRAWING NUMBER	SIZE	
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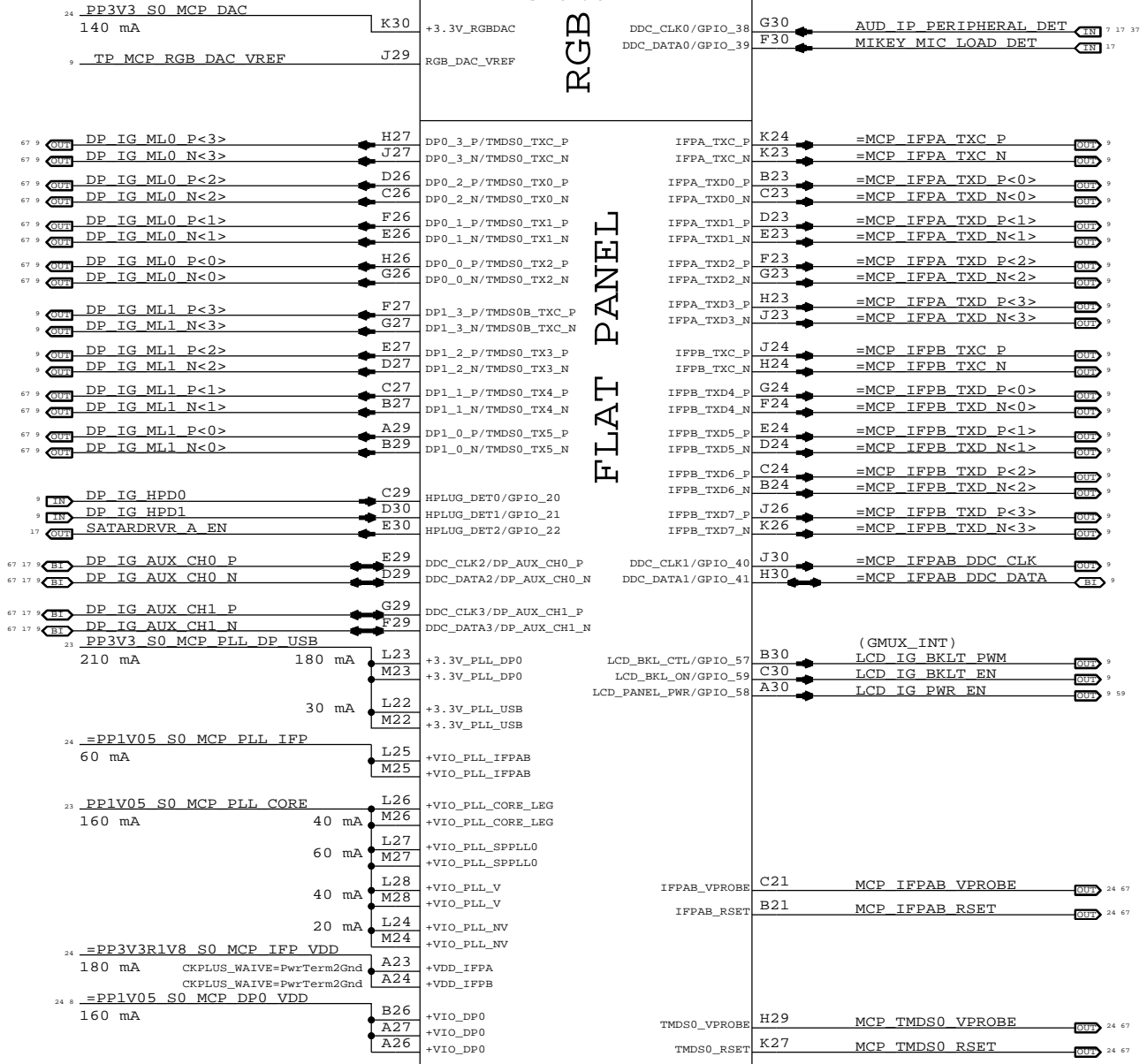
A

OMIT\_TABLE

U1400  
MCP89U-A01  
BGA  
SYMBOL 5 OF 11

RGB

FLAT PANEL



NOTE: 100K pull-downs required if HPLUG\_DET0/HPLUG\_DET1 are not used.

RGB DAC Disable:

Okay to float all RGB\_DAC signals. DDC\_CLK0/DDC\_DATA0 pull-ups still required (or use as GPIOs). Connect +3.3V\_RGBDAC pin to GND.

NOTE: No Composite/S-Video/Component Video support on MCP89

Interface Mode

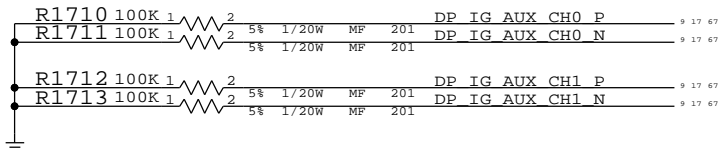
MCP Signal	TMDS/HDMI	LVDS
=MCP_IFPA_TXC_P/N	TMDS_IG_TXC_P/N	LVDS_IG_A_CLK_P/N
=MCP_IFPA_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	LVDS_IG_A_DATA_P/N<0>
=MCP_IFPA_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	LVDS_IG_A_DATA_P/N<1>
=MCP_IFPA_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	LVDS_IG_A_DATA_P/N<2>
=MCP_IFPA_TXD_P/N<3>	(UNUSED)	LVDS_IG_A_DATA_P/N<3>
=MCP_IFPB_TXC_P/N	(UNUSED)	LVDS_IG_B_CLK_P/N
=MCP_IFPB_TXD_P/N<0>	TMDS_IG_TXD_P/N<3>	LVDS_IG_B_DATA_P/N<0>
=MCP_IFPB_TXD_P/N<1>	TMDS_IG_TXD_P/N<4>	LVDS_IG_B_DATA_P/N<1>
=MCP_IFPB_TXD_P/N<2>	TMDS_IG_TXD_P/N<5>	LVDS_IG_B_DATA_P/N<2>
=MCP_IFPB_TXD_P/N<3>	(UNUSED)	LVDS_IG_B_DATA_P/N<3>
=MCP_IFPAB_DDC_CLK	TMDS_IG_DDC_CLK	LVDS_IG_DDC_CLK
=MCP_IFPAB_DDC_DATA	TMDS_IG_DDC_DATA	LVDS_IG_DDC_DATA

LVDS: Power +VDD\_IFPx at 1.8V

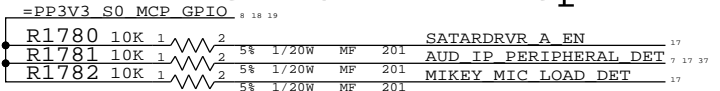
TMDS: Power +VDD\_IFPx at 3.3V

## DDC Mode Pull-downs

NOTE: DP\_AUX\_CH1 also requires pull-downs if used for dual-mode DisplayPort (DP++). If unused no pulls are necessary, if used for TMDS/HDMI only then only pull-ups are necessary.



## GPIO Pull-Ups



Current numbers from MCP89 A01 Bring-Up Support document (MCP89\_TDP\_EDP\_Bringup\_Targets\_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

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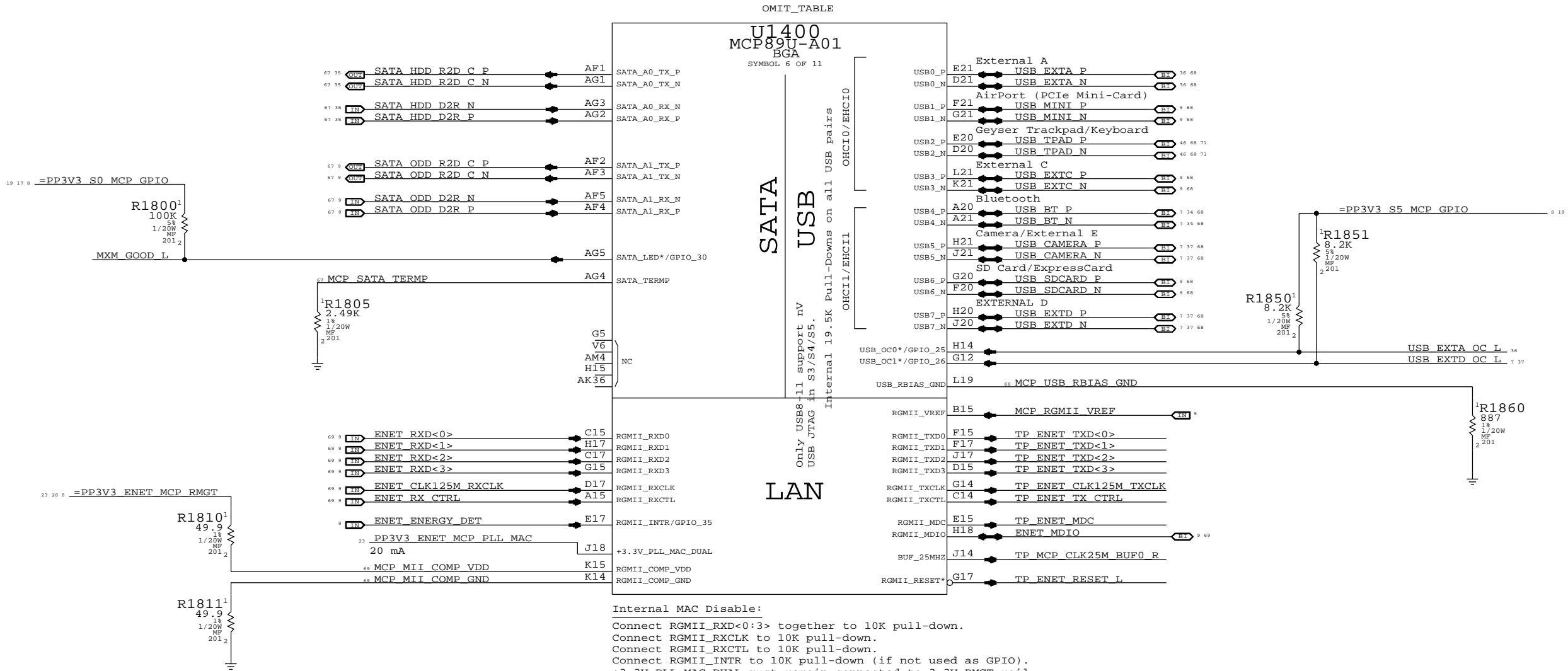
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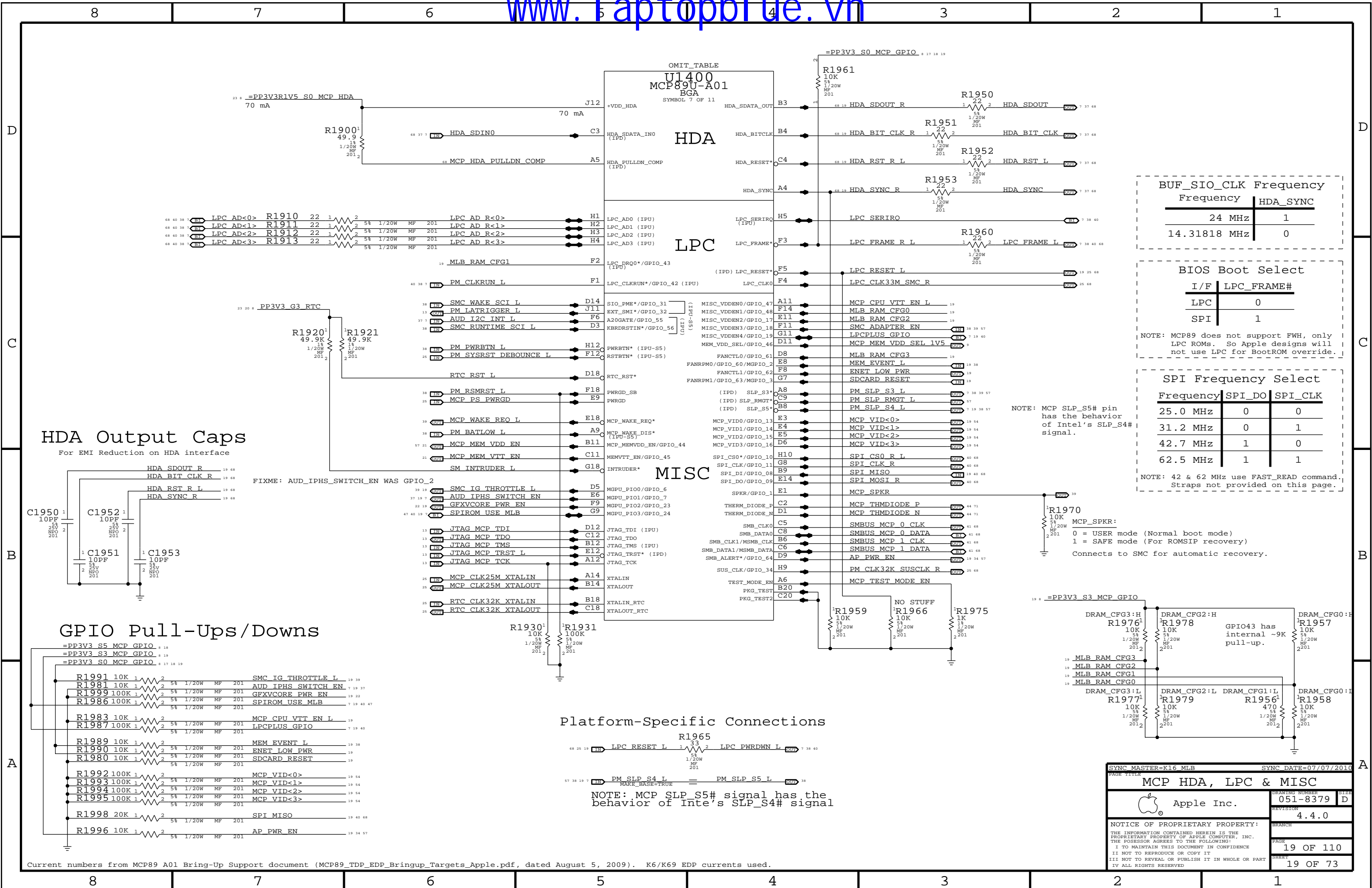
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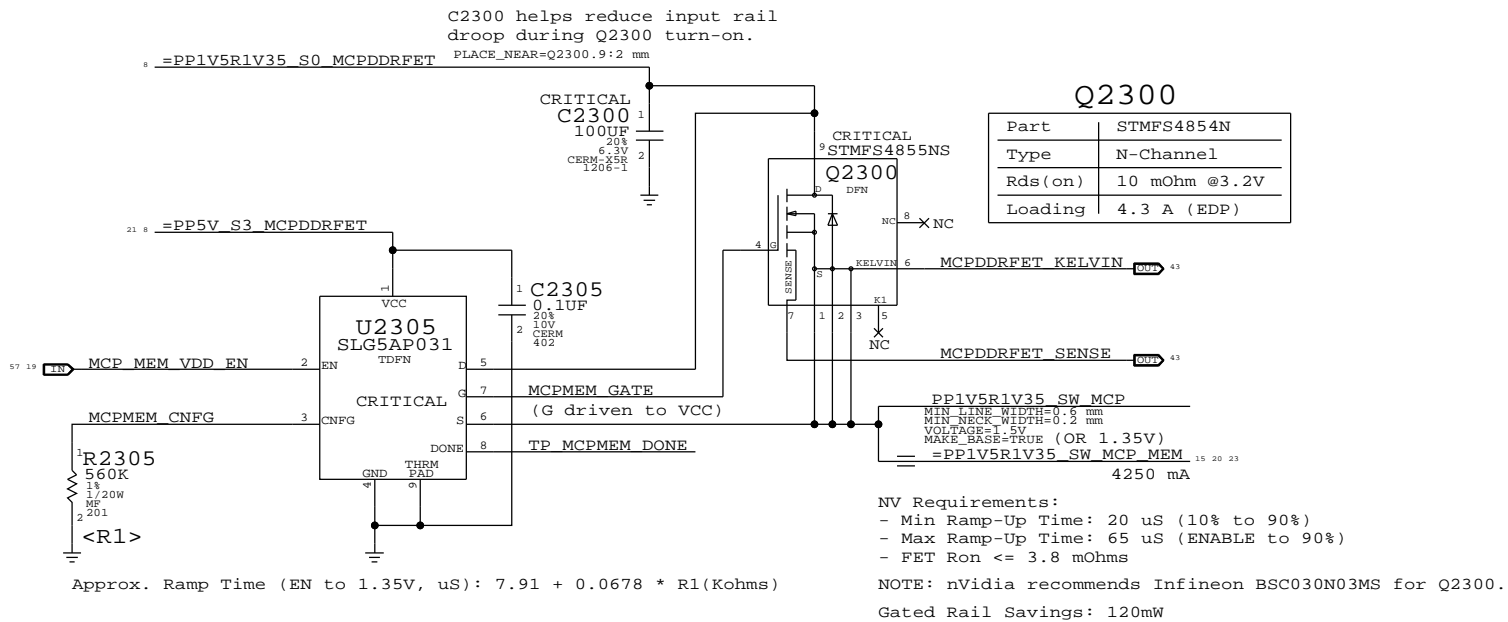
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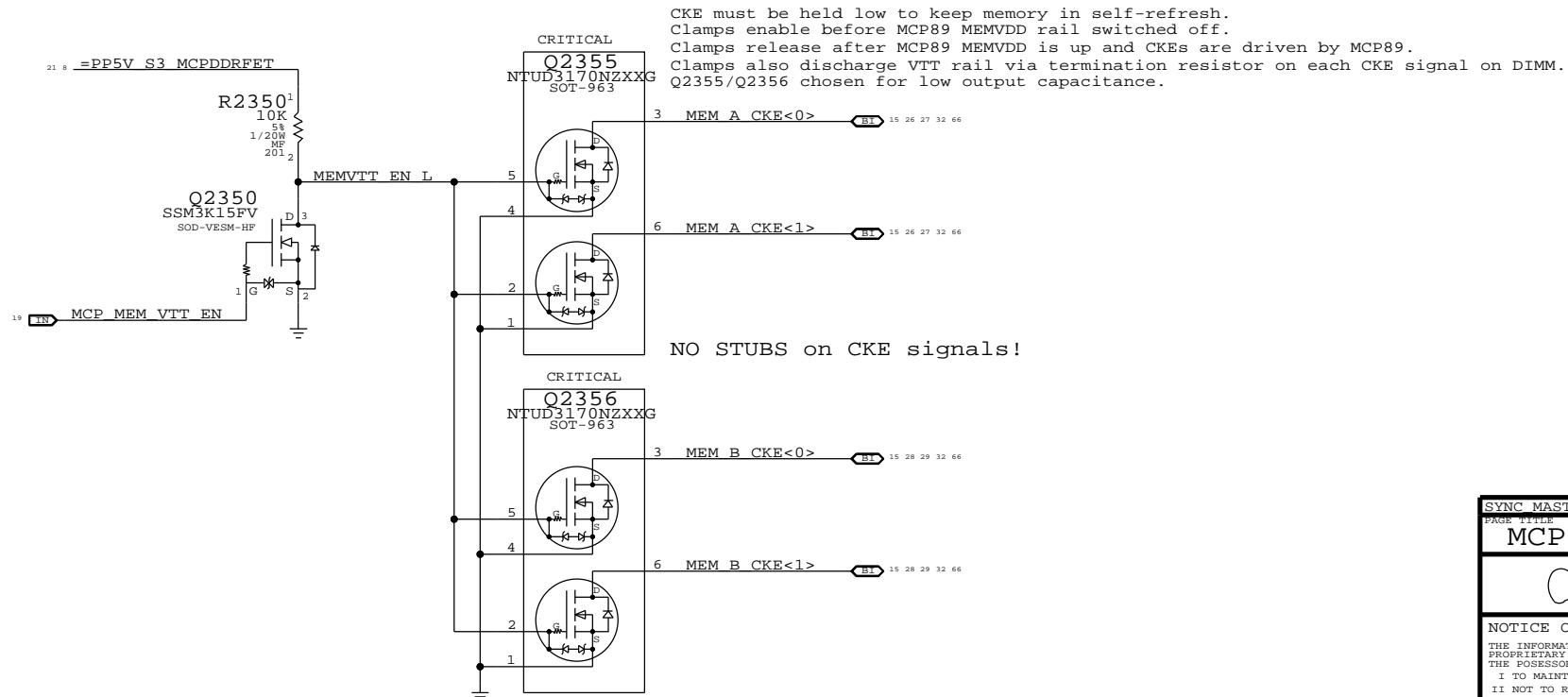








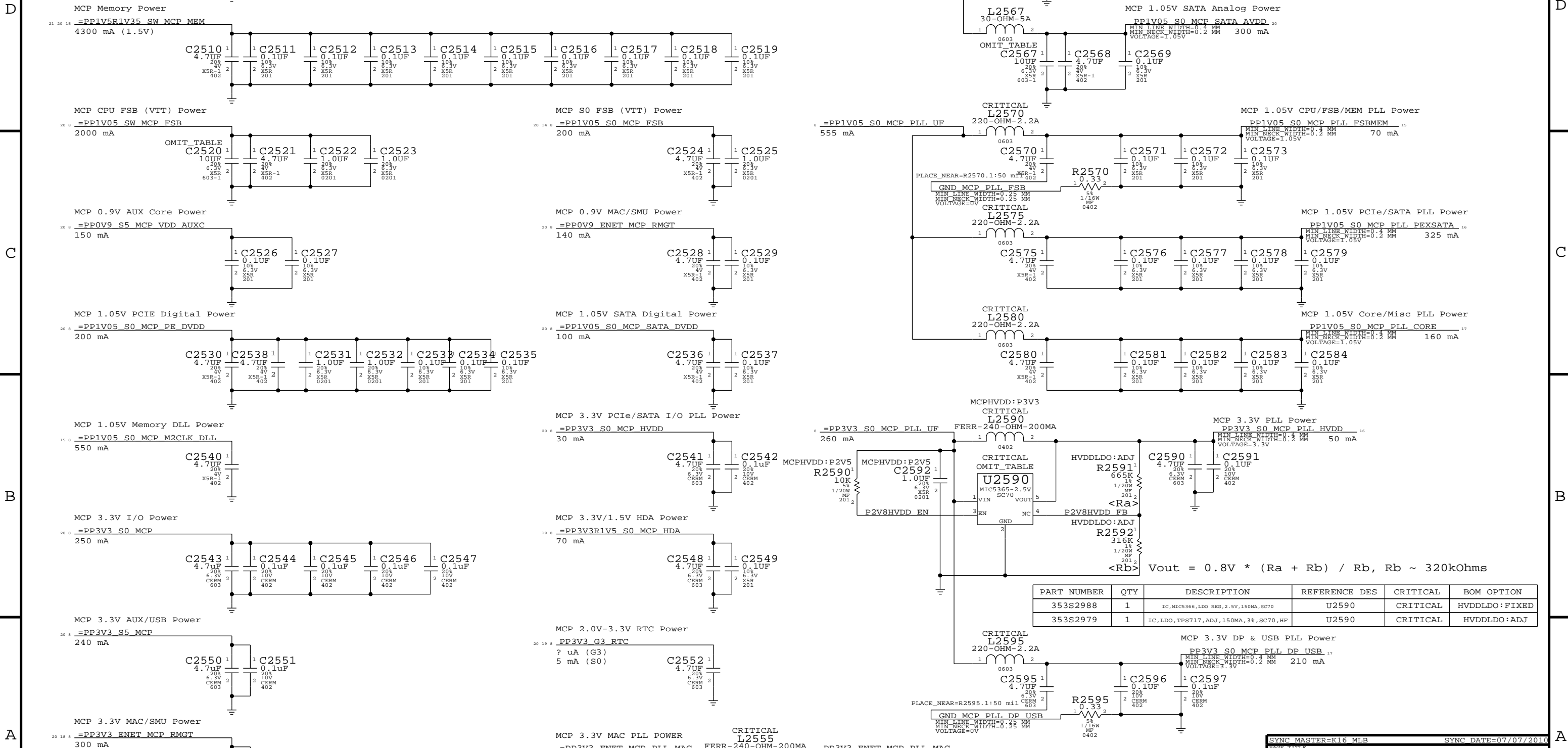
## DIMM CKE Clamps






Part	Si4838BDY
Type	N-Channel
Rds(on)	3.2 mOhm @2.5V
Loading	15.35 A (EDP)

NV Requirements:  
 - Min Ramp-Up Time: 100 uS (10% to 90%)  
 - Max Ramp-Up Time: 1500 uS (ENABLE to 90%)  
 - FET Ron <= 2.5 mOhms  
 NOTE: nvidia recommends Infineon BSC020N03MS for Q2400.  
 Gated Rail Savings: 860mW



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S2988	1	IC,MIC5366,LDO REG,2.5V,150MA,SC70	U2590	CRITICAL	HVDDLDO:FIXED
353S2979	1	IC,LDO,TPS717,ADJ,150MA,3%,SC70,HF	U2590	CRITICAL	HVDDLDO:ADJ

$$V_{out} = 0.8V * (R_a + R_b) / R_b, R_b \sim 320k\Omega$$

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MCP Standard Decoupling			
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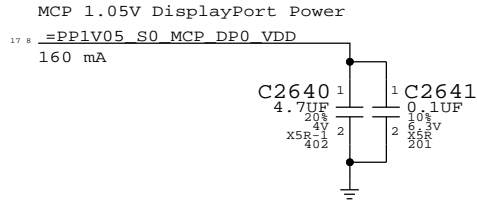
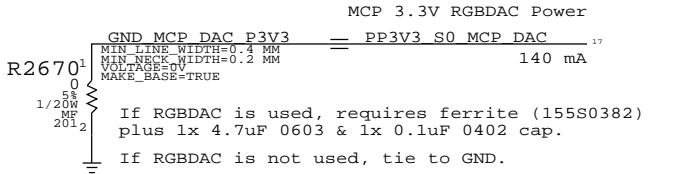
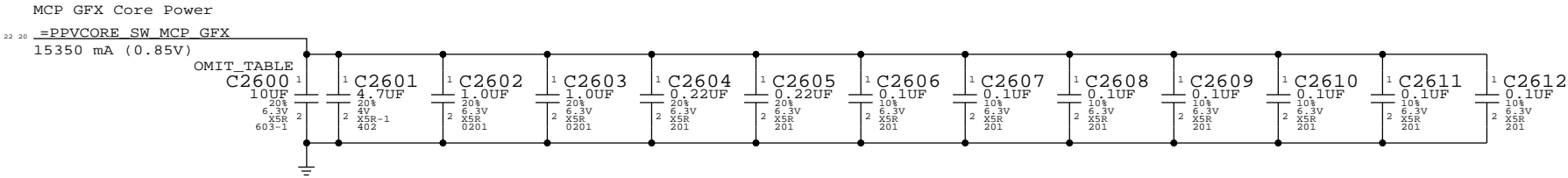
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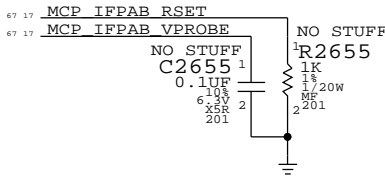
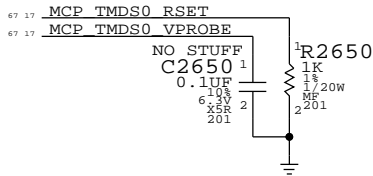
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=PP3V3R1V8 S0 MCP\_IFP\_VDD 17

=PP1V05 S0 MCP\_PLL IFP 17



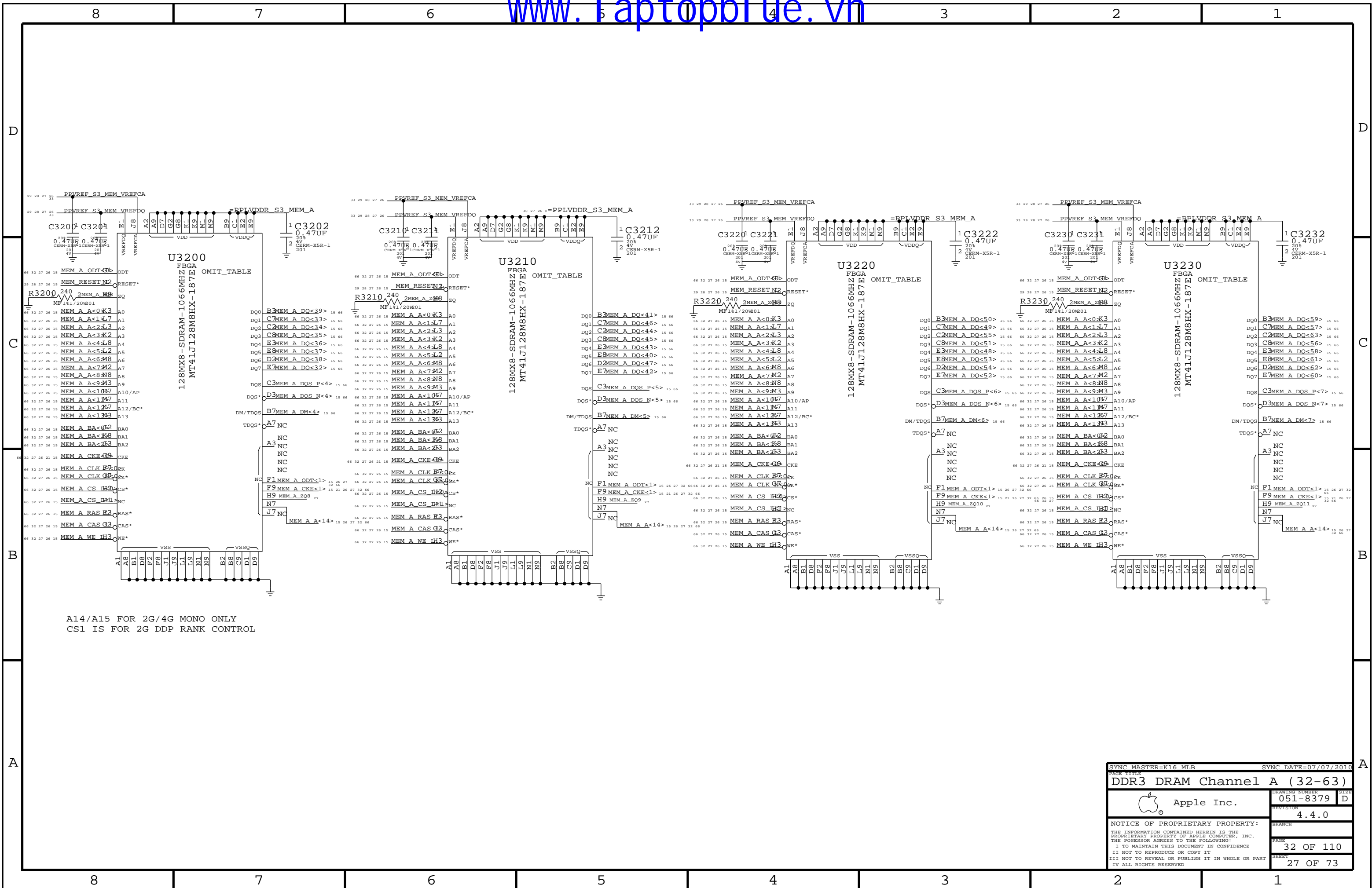
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MCP Graphics Support		Support	
 Apple Inc.	DRAWING NUMBER		051-8379
	REVISION		4.4.0
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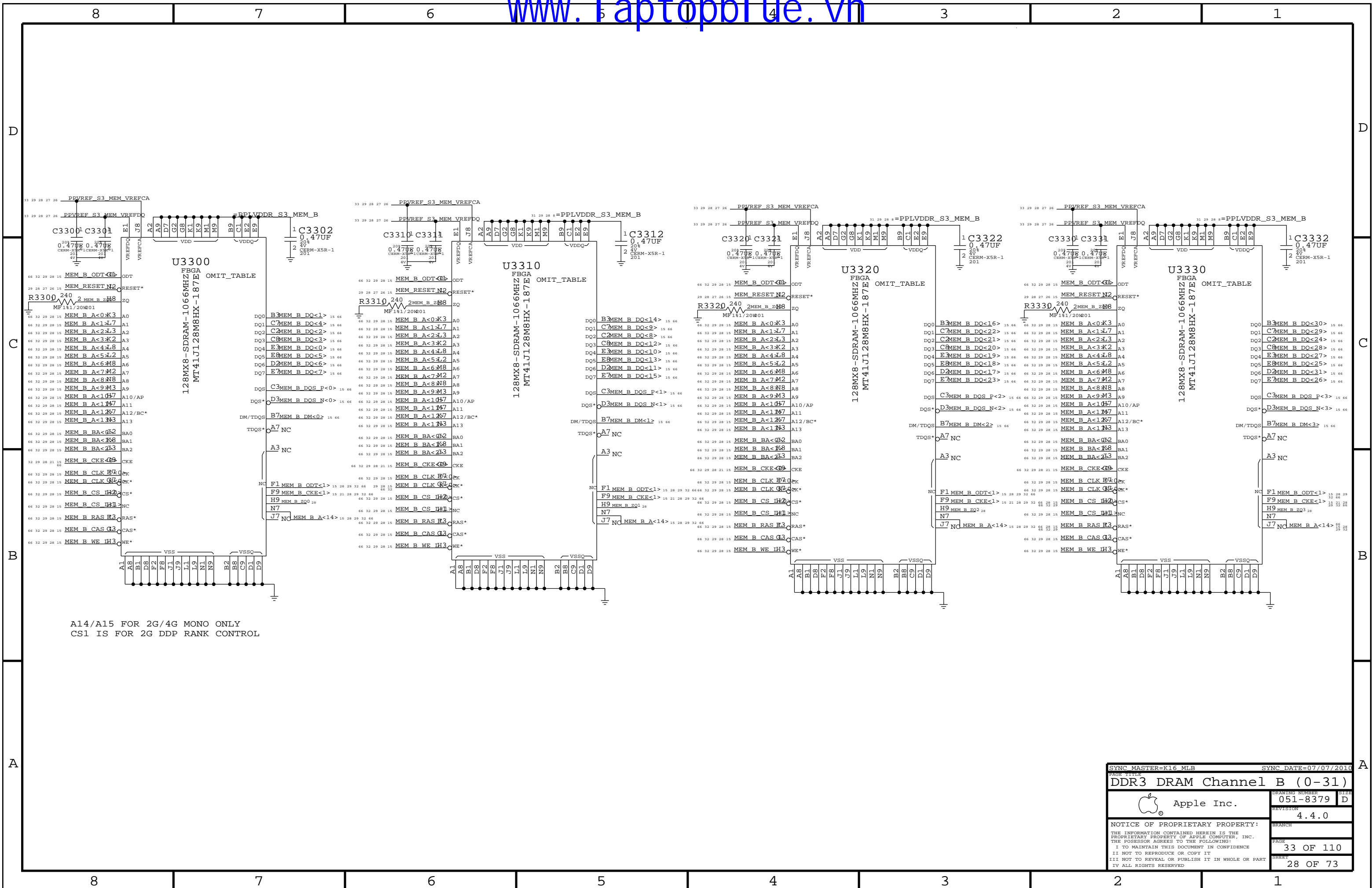


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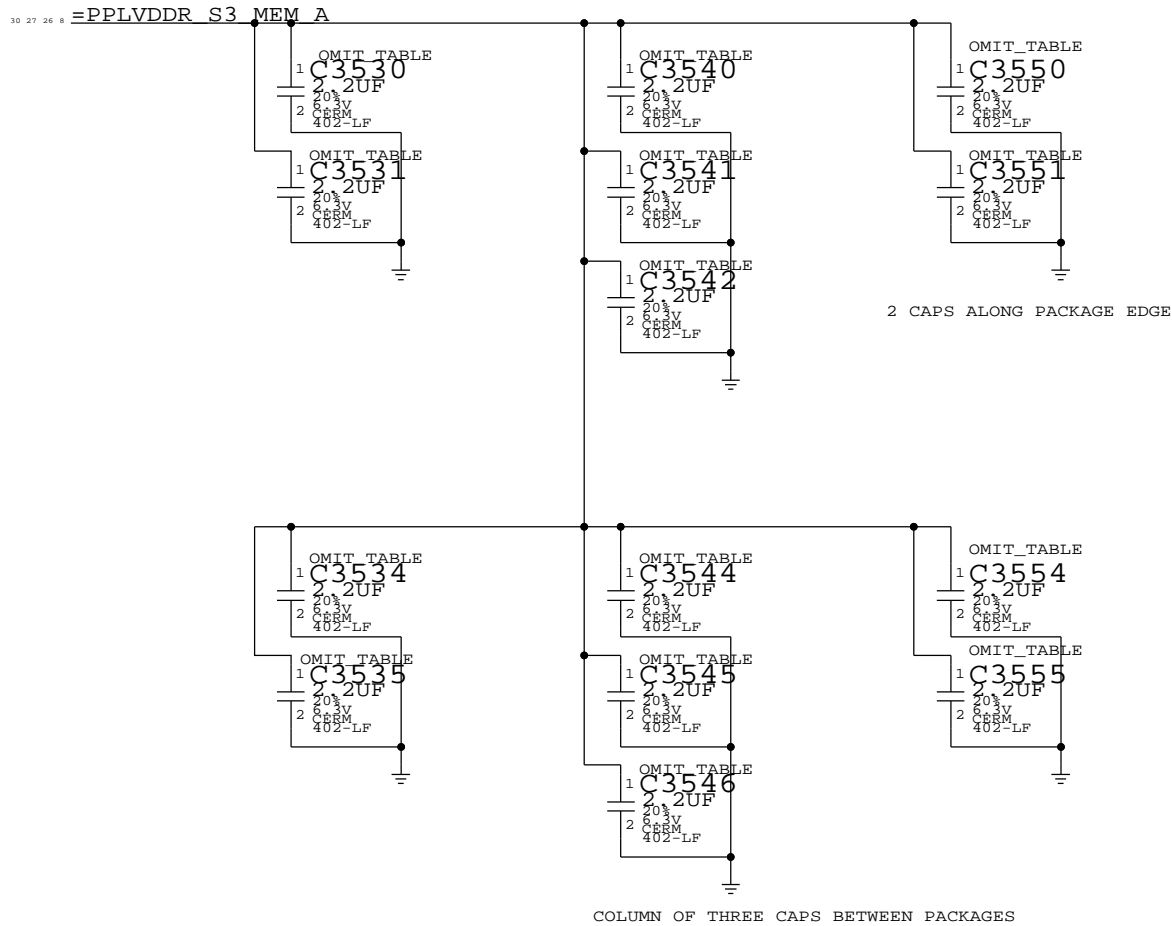





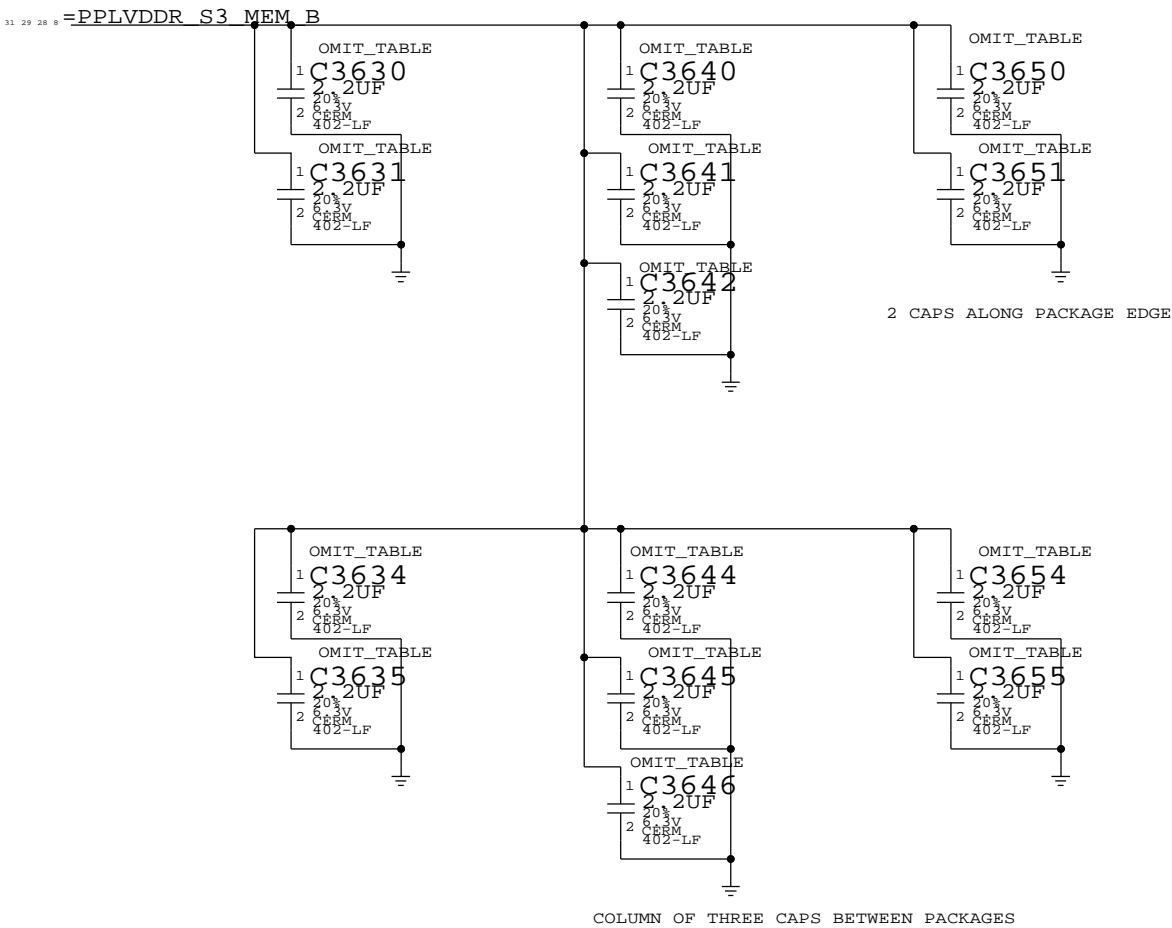




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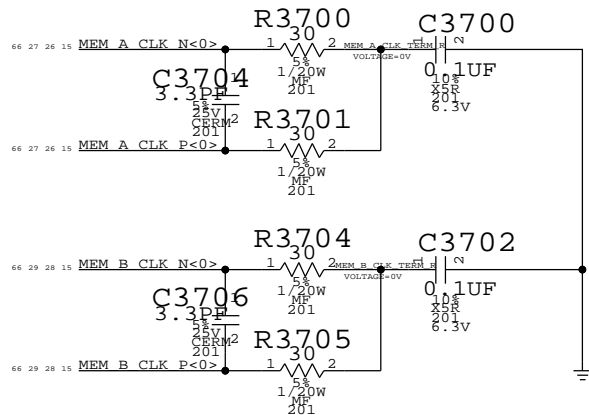


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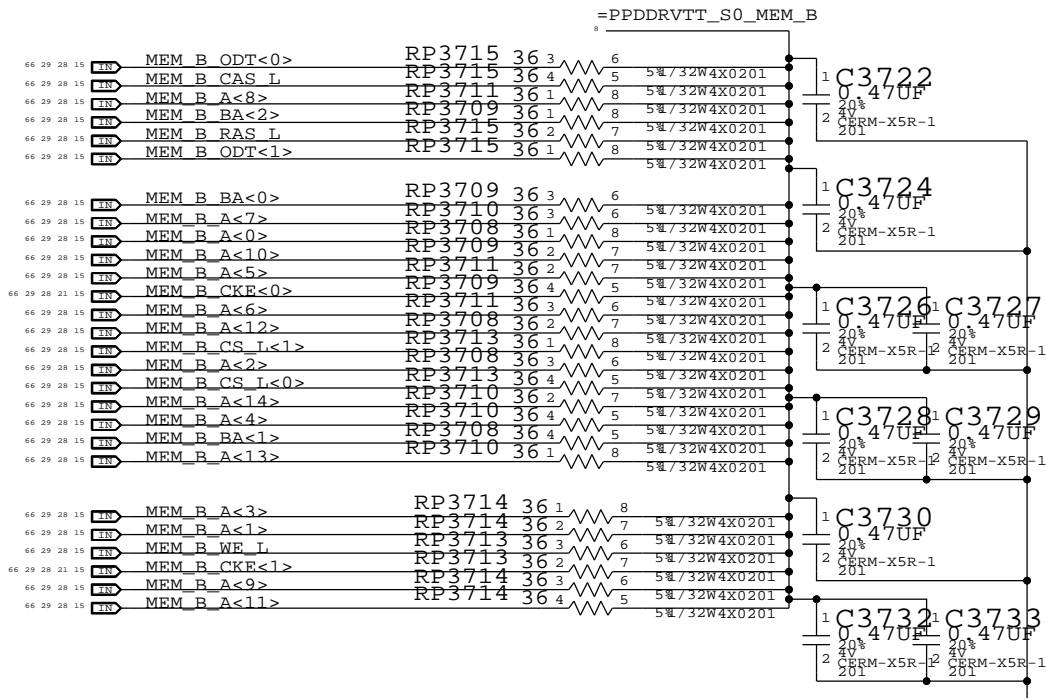
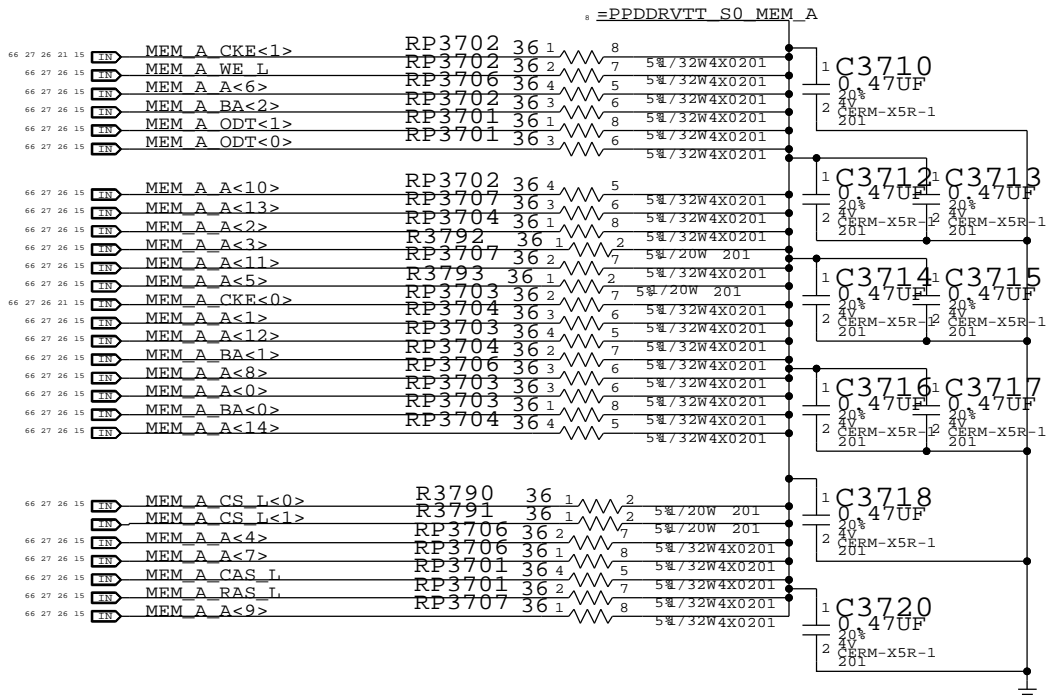


MEM CLOCK TERMINATION

Place RC end termination after last DRAM  
Place Source Cterm at neckdown at first DRAM



JEDEC recommends 30 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE





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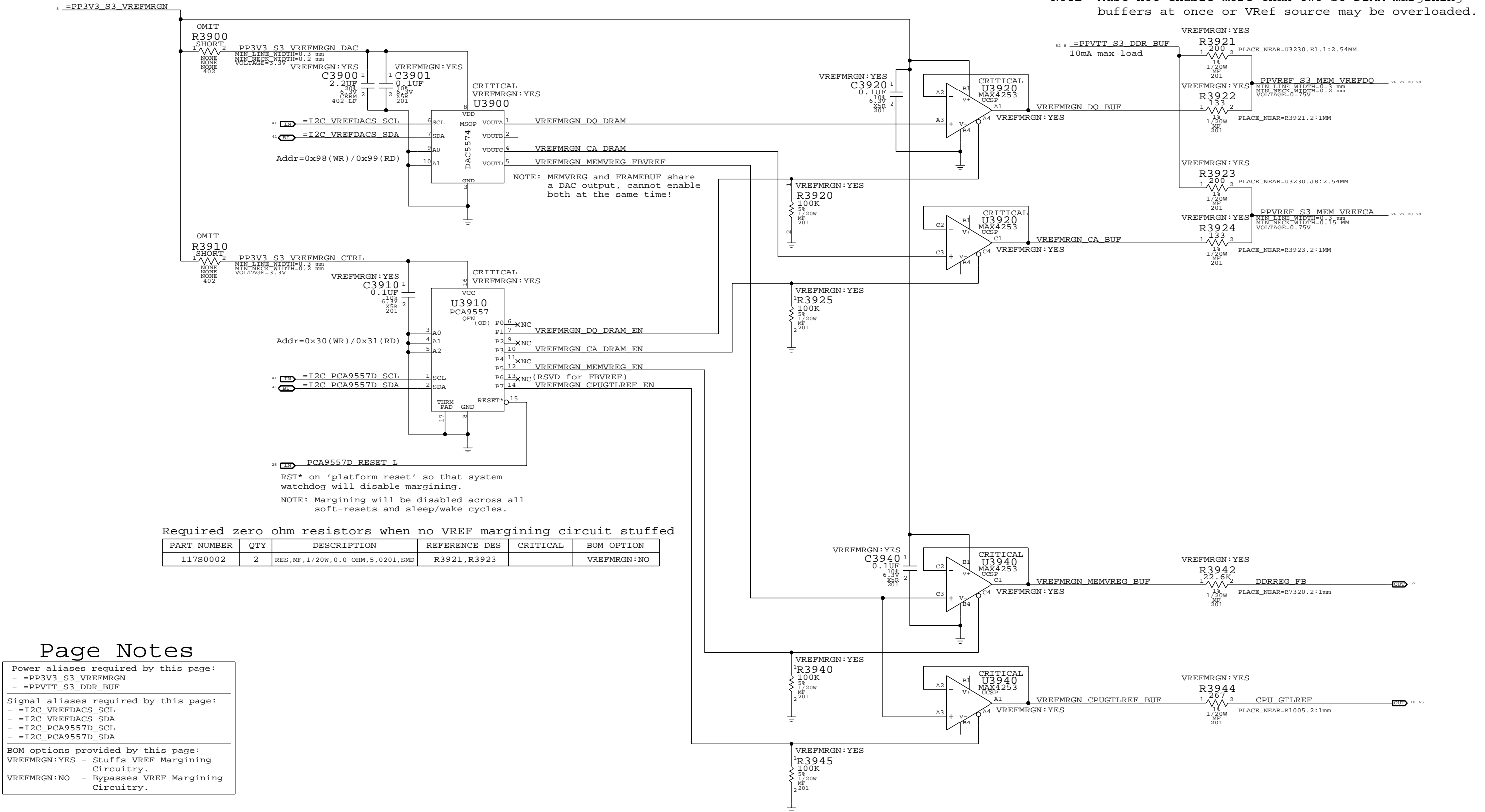
A

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### Page Notes

Power aliases required by this page:

- =PP3V3\_S3\_VREFMRGN
- =PPVTT\_S3\_DDR\_BUF

Signal aliases required by this page:

- =I2C\_VREFDACS\_SCL
- =I2C\_VREFDACS\_SDA
- =I2C\_PCA9557D\_SCL
- =I2C\_PCA9557D\_SDA

BOM options provided by this page:

- VREFMRGN:YES - Stuffs VREF Margining Circuitry.
- VREFMRGN:NO - Bypasses VREF Margining Circuitry.

	MEM VREF DQ	MEM VREF CA	MEM VREG	CPU GTLREF (FSB)
DAC Channel:	A	C	D	D
PCA9557D Pin:	1	3	5	7
Nominal value		0.75V (DAC: 0x3A)	1.5V (DAC: 0x3A)	0.7V (DAC: 0x8B)
Margined target:		0.300V - 1.200V (+/- 450mV)	1.998V - 1.002V (+/- 498mV)	0.200V - 1.050V (+/- 500mV)
DAC range:		0.000V - 1.501V (0x00 - 0x74)	0.000V - 1.501V (0x00 - 0x74)	0.000V - 1.191V (0x00 - 0x5C)
Vref current:		+3.4mA - -3.4mA (- = sourced)	+33uA - -33uA (- = sourced)	+750uA - -528uA (- = sourced)
DAC step size:		7.69mV / step @ output	8.59mV / step @ output	9.24mV / step @ output

SYNC MASTER=K16 MLB

SYNC DATE=07/07/2010

FSB/DDR3 Vref Margining

Apple Inc.

051-8379

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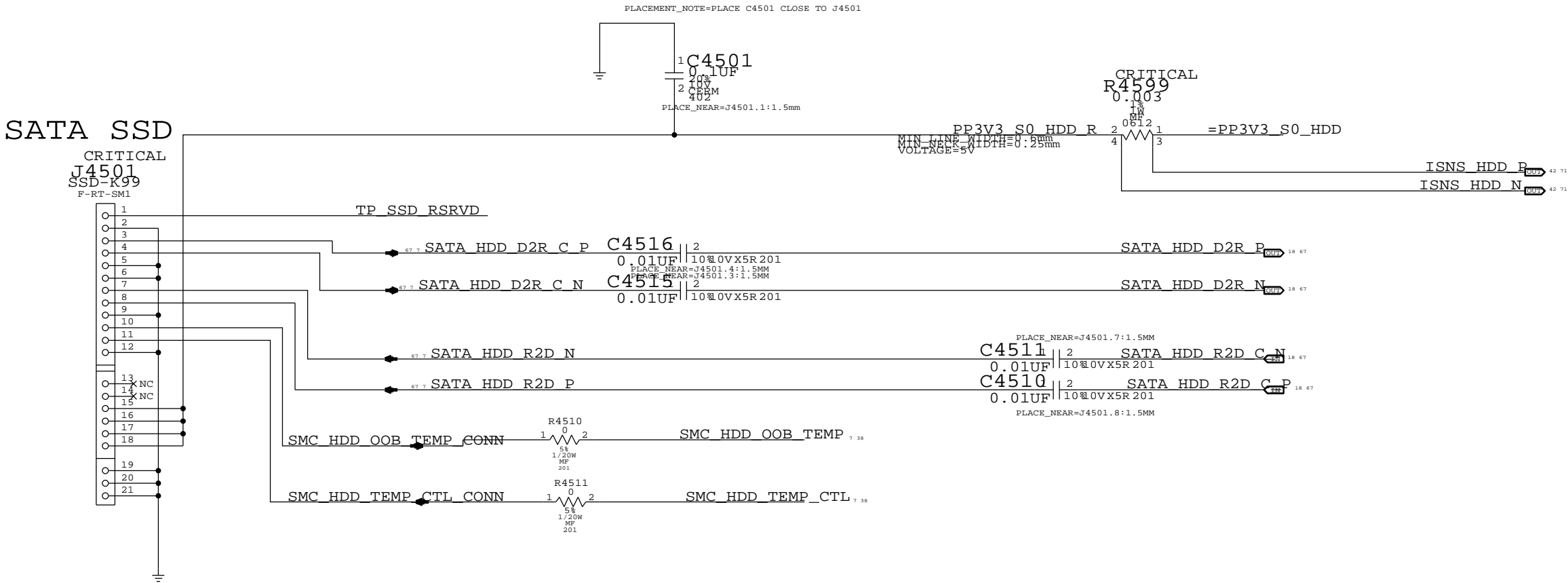
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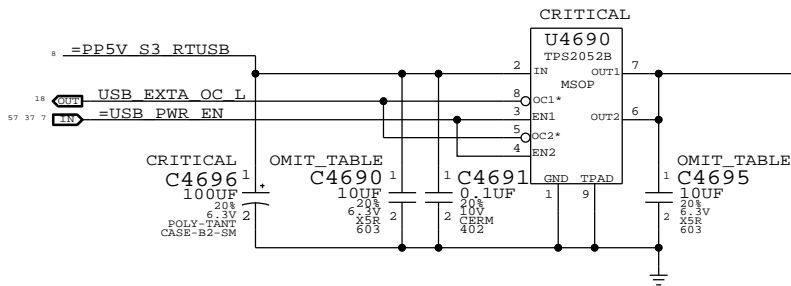


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X21 WIRELESS CONNECTOR			
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	PAGE		40 OF 110
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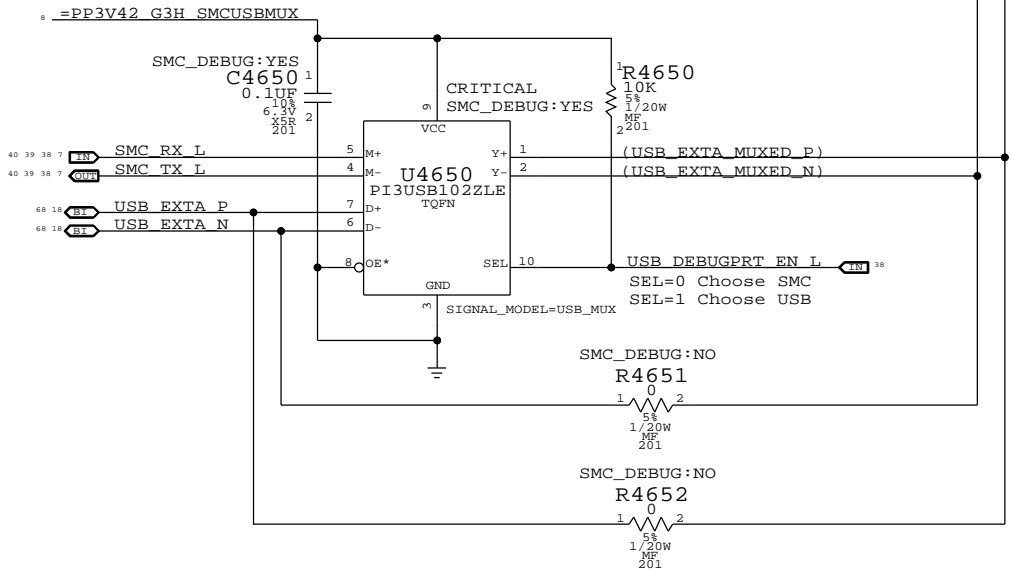


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SATA CONNECTOR			
 Apple Inc.		DRAWING NUMBER	051-8379
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		PAGE	45 OF 110
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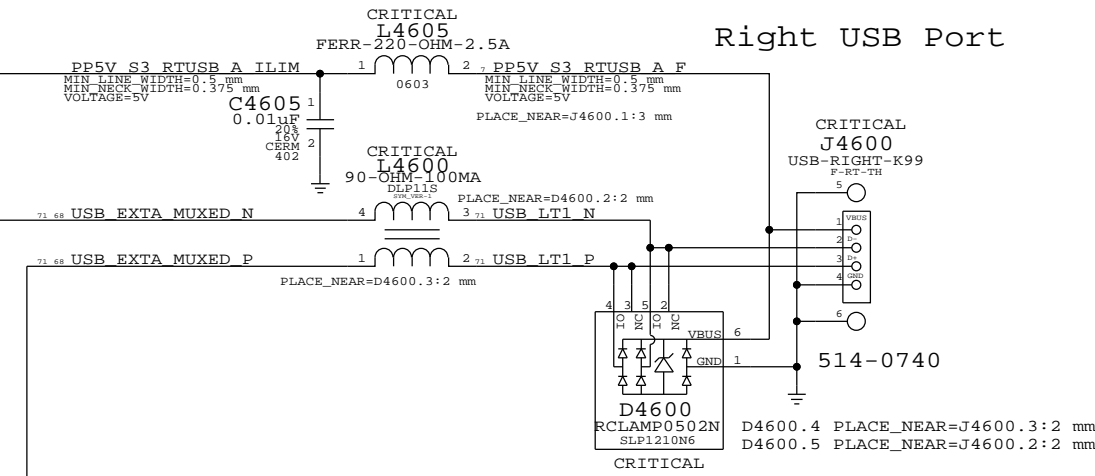
Port Power Switch



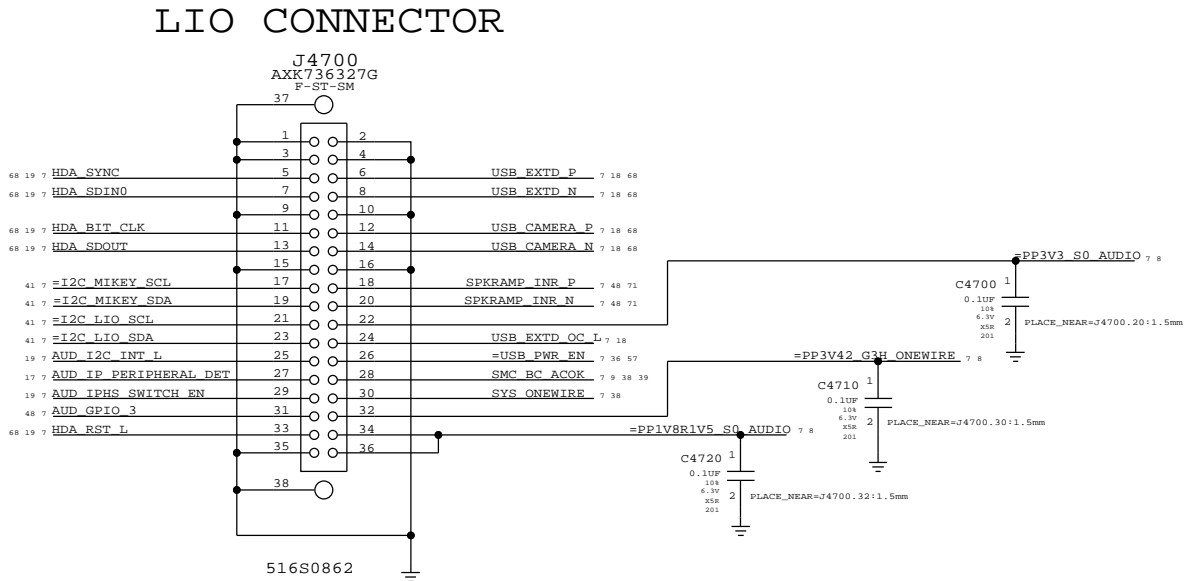
USB/SMC Debug Mux



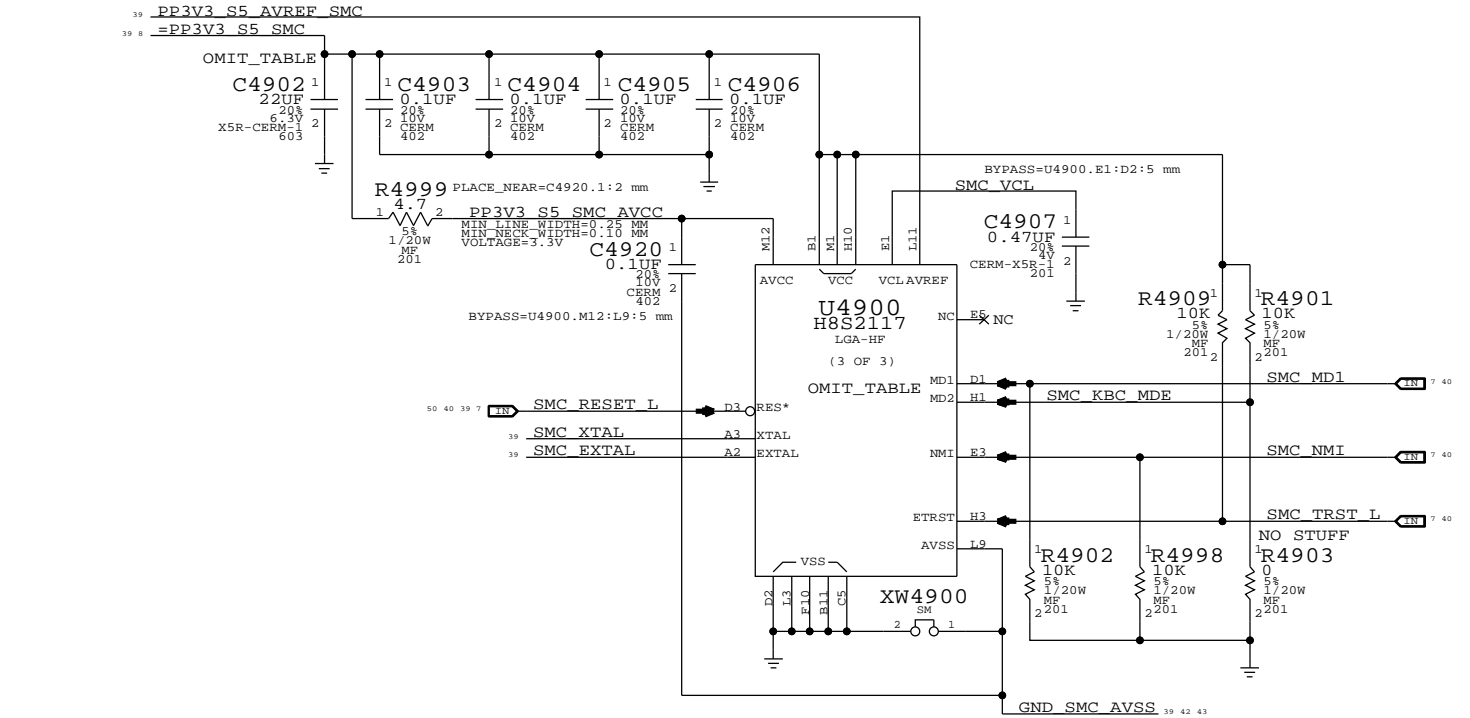
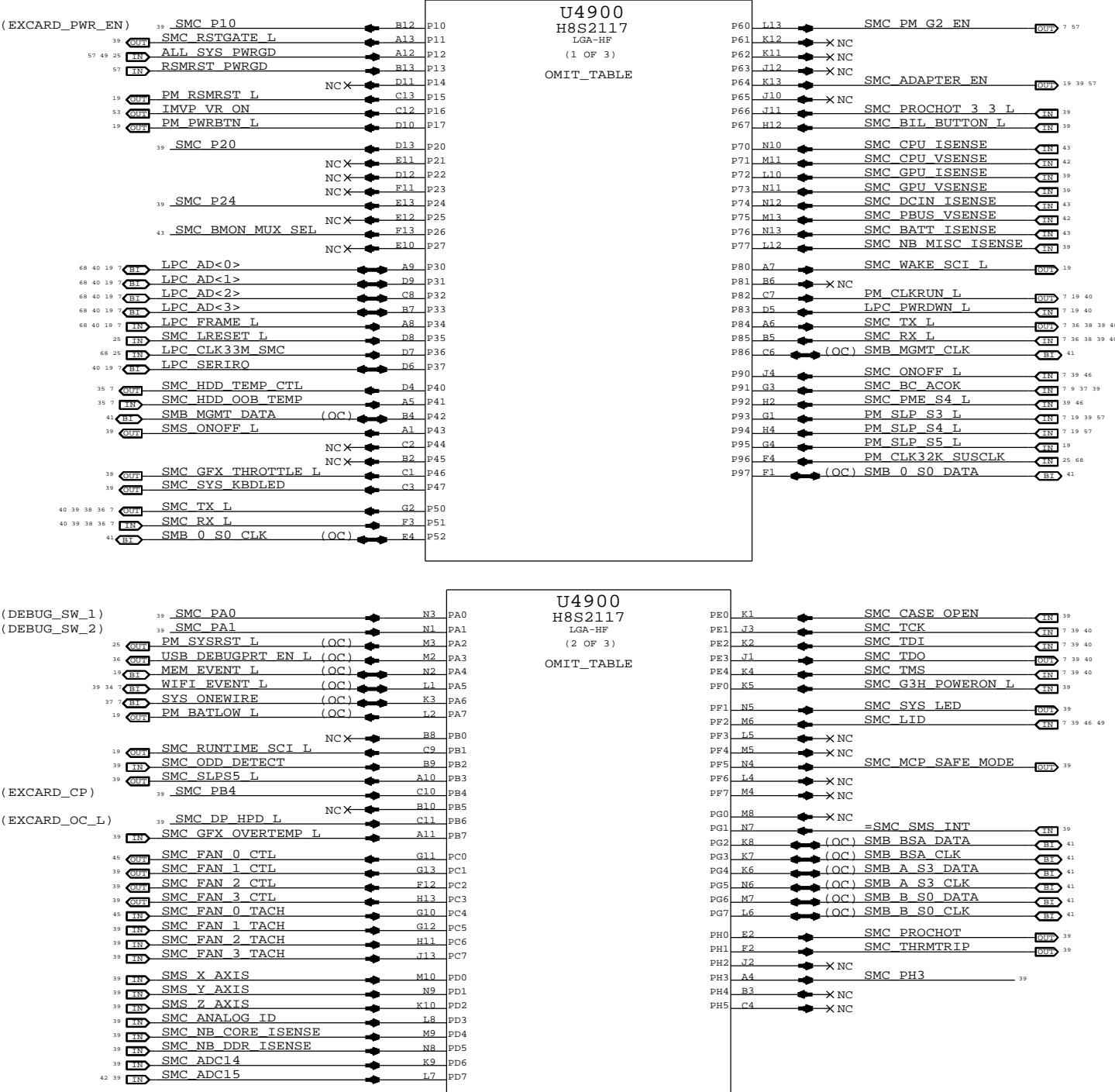
Right USB Port



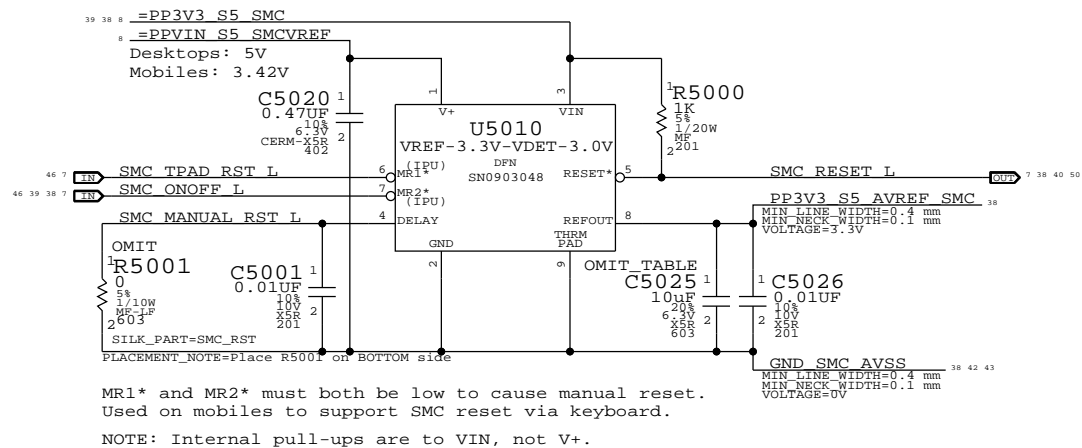




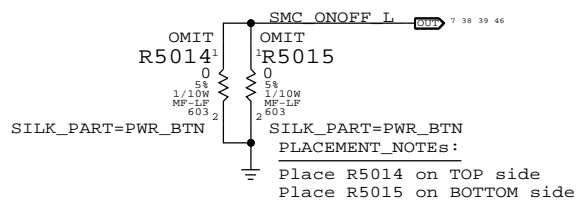
NOTE: Unused pins have "SMC\_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



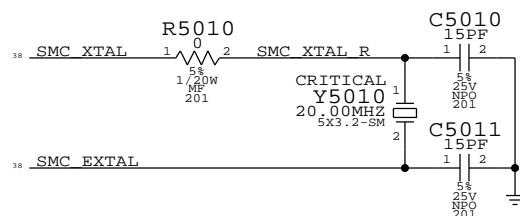
## SMC Reset "Button", Supervisor & AVREF Supply



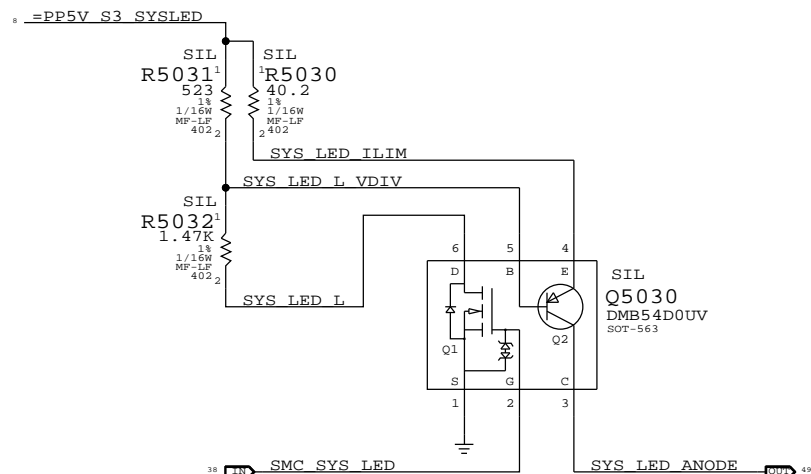
## Debug Power "Buttons"



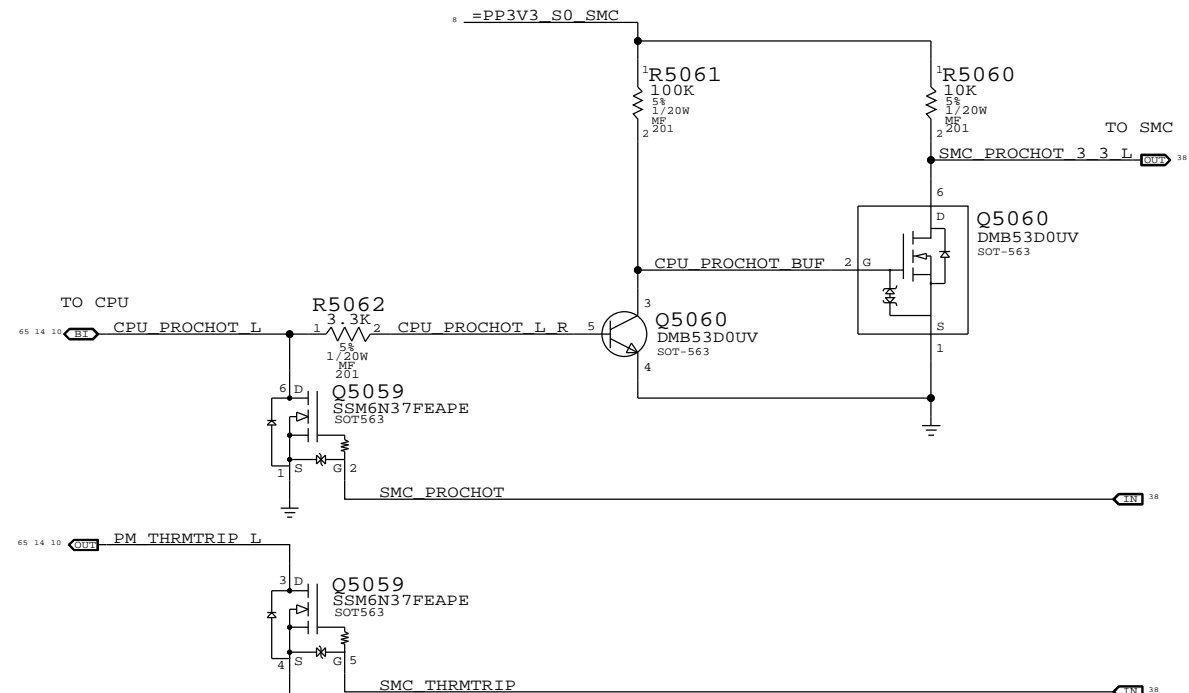
## SMC Crystal Circuit



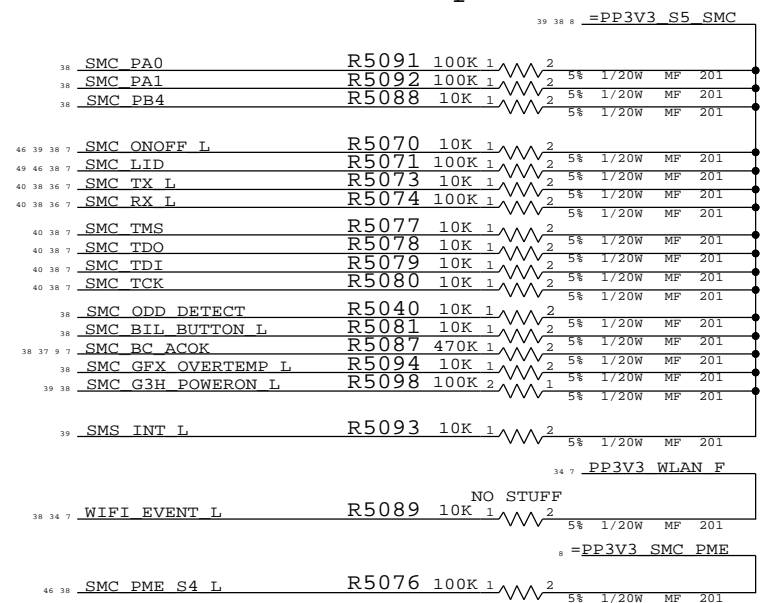
## System (Sleep) LED Circuit



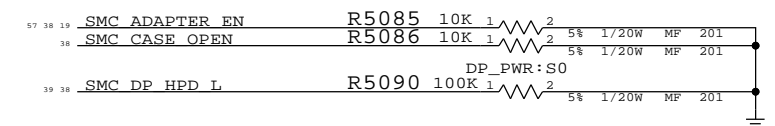
## SMC FSB to 3.3V Level Shifting




















## SMC Pull-ups

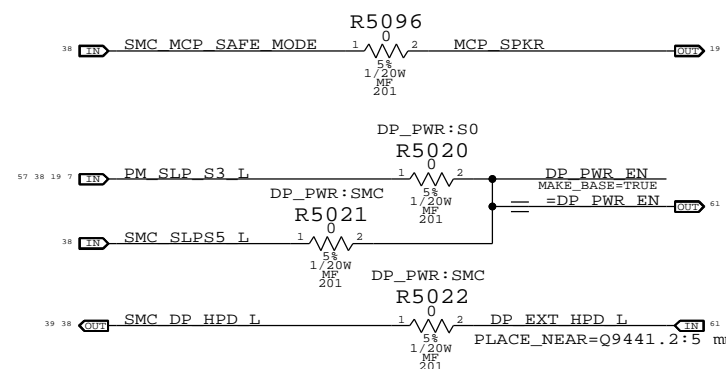


## SMC Pull-downs




## SMC Aliases

42	SMC LCDCLKT ISENSE	=	SMS X AXIS		38
	MAKE_BASE=TRUE				
42	SMC WLAN ISENSE	=	SMS Y AXIS		38
	MAKE_BASE=TRUE				
42	SMC HDD ISENSE	=	SMS Z AXIS		38
	MAKE_BASE=TRUE				
43	SMC CSREG ISENSE	=	SMC ADC14		38
	MAKE_BASE=TRUE				
43	SMC LCDCLKT VSENSE	=	SMC ADC15		38
	MAKE_BASE=TRUE				
43	SMC MCP CORE ISENSE	=	SMC NB CORE ISENSE		38
	MAKE_BASE=TRUE				
43	SMC MCP DDR ISENSE	=	SMC NB DDR ISENSE		38
	MAKE_BASE=TRUE				
42	SMC LV533 ISENSE	=	SMC NB MISC ISENSE		38
	MAKE_BASE=TRUE				
	TP SMC ANALOG ID	=	SMC ANALOG ID		38
	MAKE_BASE=TRUE				
	TP SMC GPU ISENSE	=	SMC GPU ISENSE		38
	MAKE_BASE=TRUE				
42	SMC MCP VSENSE	=	SMC GPU VSENSE		38
	MAKE_BASE=TRUE				
38	 SMC GFX THROTTLE L	=	SMC IG THROTTLE L		19
			MAKE_BASE=TRUE		
39	 SMS INT L	=	=SMC SMS INT		38
	MAKE_BASE=TRUE				
19	 MCP WAKE REO L	=	SMC G3H POWERON L		38
			MAKE_BASE=TRUE		

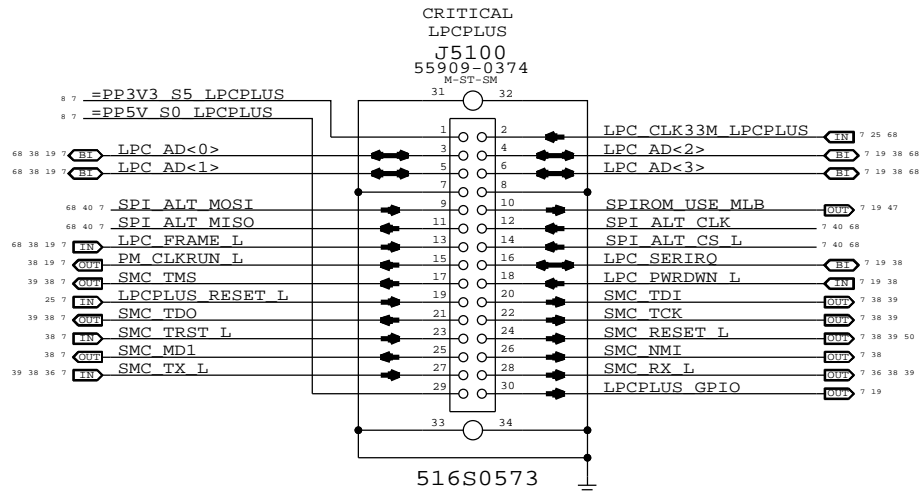


## Unused Pins

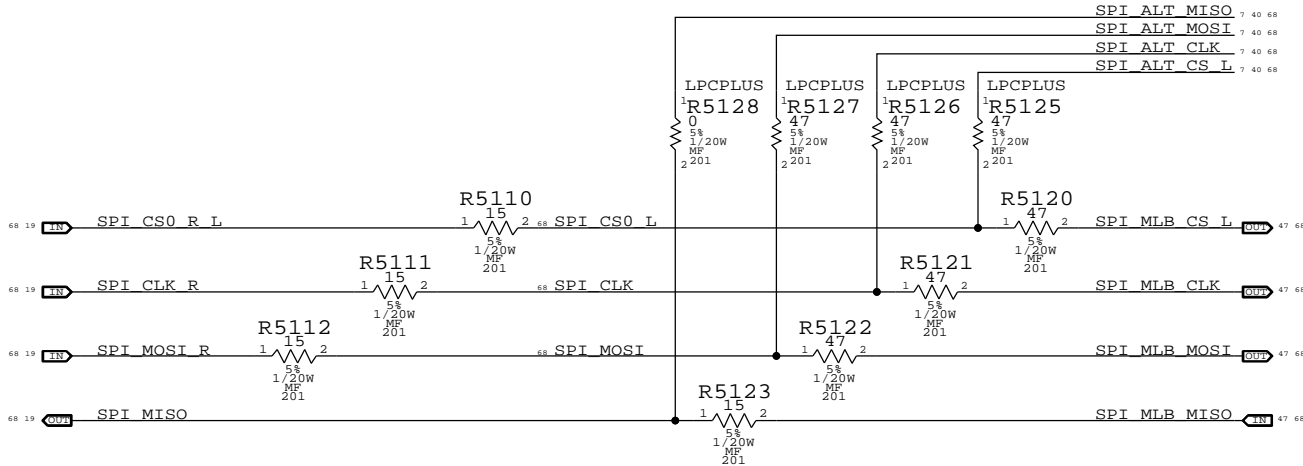
38	<b>483</b>	<b>SMS ONOFF L</b>	<b>==</b>	<b>TP SMS ONOFF L</b>	<b>MAKE_BASE=TRUE</b>	
38	<b>483</b>	<b>SMC SYS KBDLED</b>	<b>==</b>	<b>TP SMC SYS KBDLED</b>	<b>MAKE_BASE=TRUE</b>	
38	<b>483</b>	<b>SMC FAN 1 CTL</b>	<b>==</b>	<b>TP SMC FAN 1 CTL</b>	<b>MAKE_BASE=TRUE</b>	
		<b>TP SMC FAN 1 TACH</b>	<b>==</b>	<b>SMC FAN 1 TACH</b>		<b>9000</b> 38
		<b>MAKE_BASE=TRUE</b>	<b>==</b>			
38	<b>483</b>	<b>SMC FAN 2 CTL</b>	<b>==</b>	<b>NC SMC FAN 2 CTL</b>	<b>MAKE_BASE=TRUE NO_TEST=TRUE</b>	
		<b>NC SMC FAN 2 TACH</b>	<b>==</b>	<b>SMC FAN 2 TACH</b>		<b>9000</b> 38
		<b>MAKE_BASE=TRUE NO_TEST=TRUE</b>	<b>==</b>			
38	<b>483</b>	<b>SMC FAN 3 CTL</b>	<b>==</b>	<b>NC SMC FAN 3 CTL</b>	<b>MAKE_BASE=TRUE NO_TEST=TRUE</b>	
		<b>NC SMC FAN 3 TACH</b>	<b>==</b>	<b>SMC FAN 3 TACH</b>		<b>9000</b> 38
		<b>MAKE_BASE=TRUE NO_TEST=TRUE</b>	<b>==</b>			
38	<b>483</b>	<b>SMC RSTGATE L</b>	<b>==</b>	<b>TP SMC RSTGATE L</b>	<b>MAKE_BASE=TRUE</b>	
38	<b>483</b>	<b>SMC P10</b>	<b>==</b>	<b>TP SMC P10</b>	<b>MAKE_BASE=TRUE</b>	
38	<b>483</b>	<b>SMC P20</b>	<b>==</b>	<b>TP SMC P20</b>	<b>MAKE_BASE=TRUE</b>	
38	<b>483</b>	<b>SMC P24</b>	<b>==</b>	<b>TP SMC P24</b>	<b>MAKE_BASE=TRUE</b>	
38	<b>483</b>	<b>SMC PH3</b>	<b>==</b>	<b>TP SMC PH3</b>	<b>MAKE_BASE=TRUE</b>	

SYNC MASTER=K16 MLB		SYNC DATE=07/07/2010	
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SMC Support			
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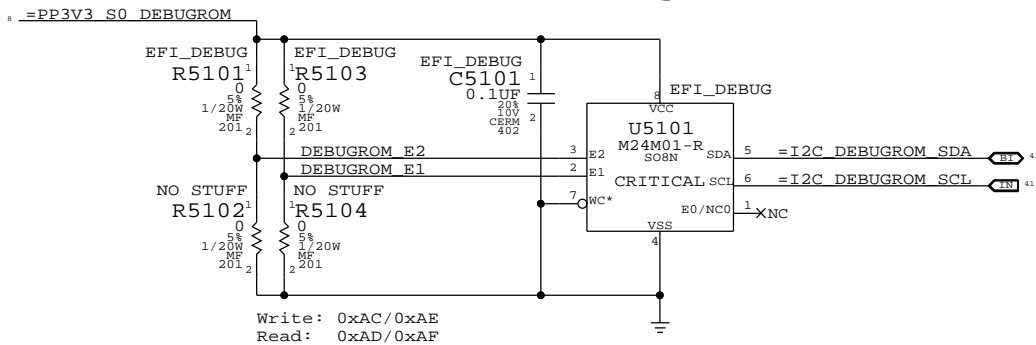
LPC+SPI Connector



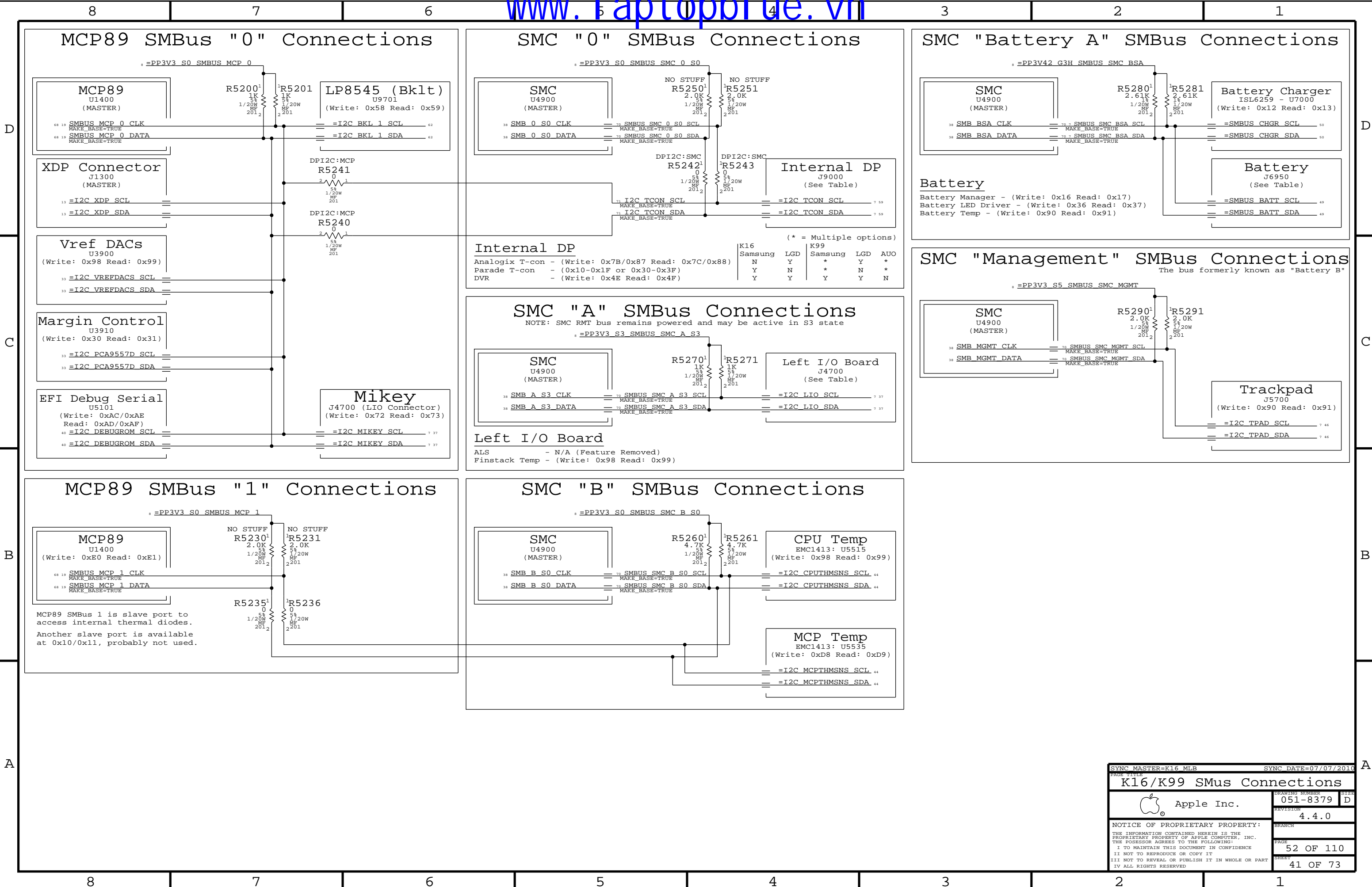
SPI Bus Series Termination



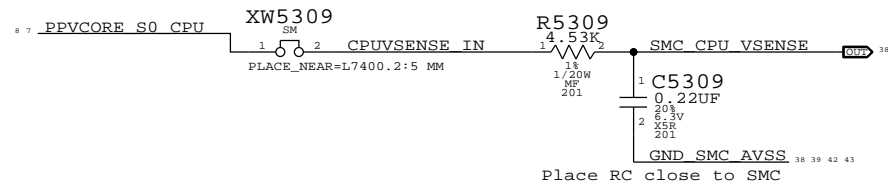
EFI Debug ROM



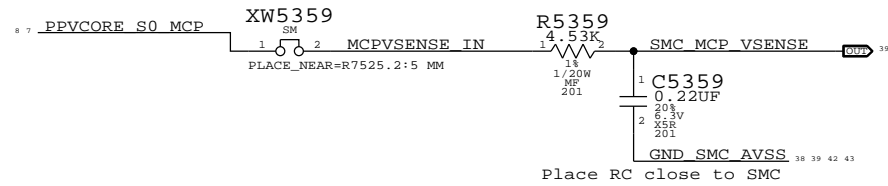




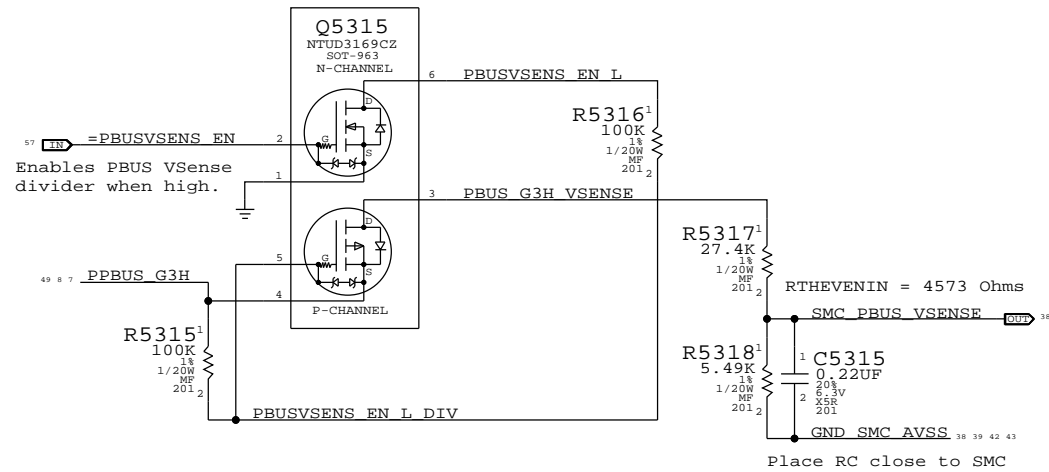
CPU Voltage Sense / Filter



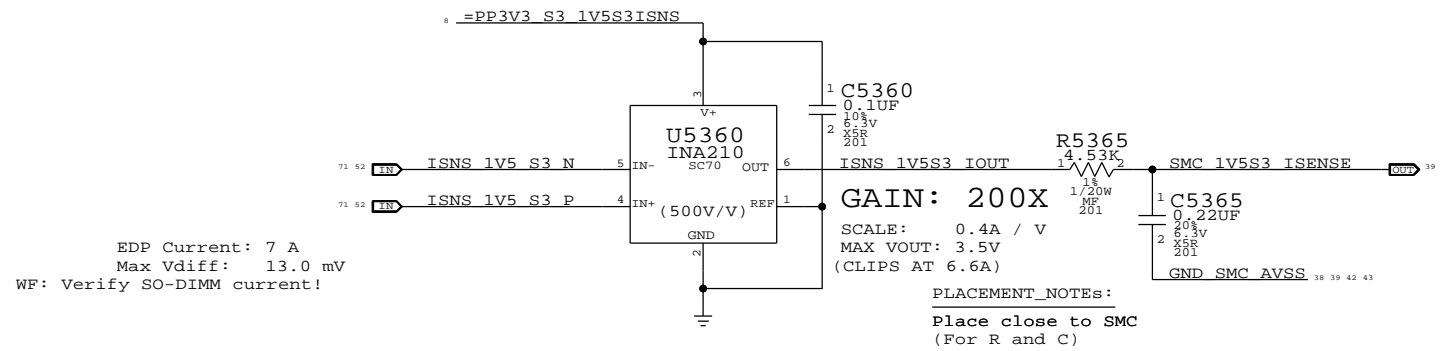
MCP Voltage Sense / Filter



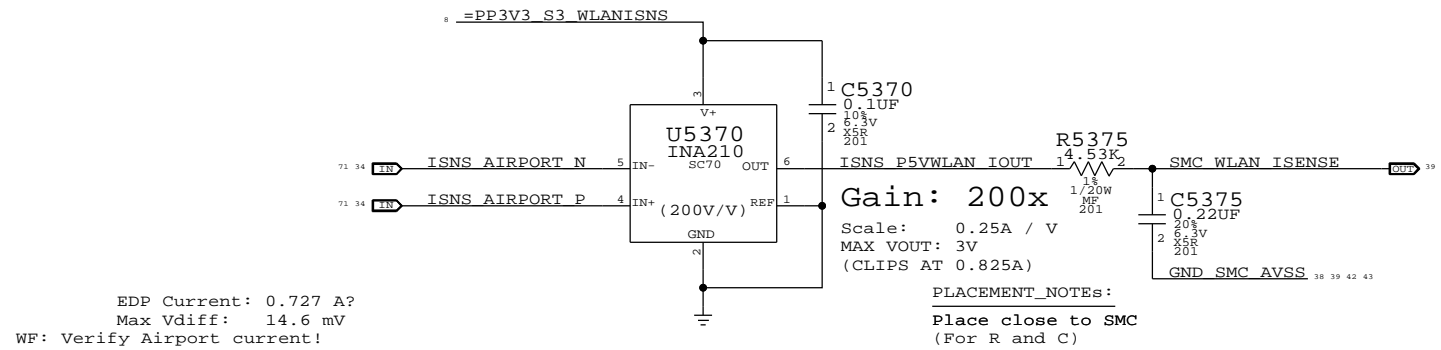
PBUS Voltage Sense Enable & Filter



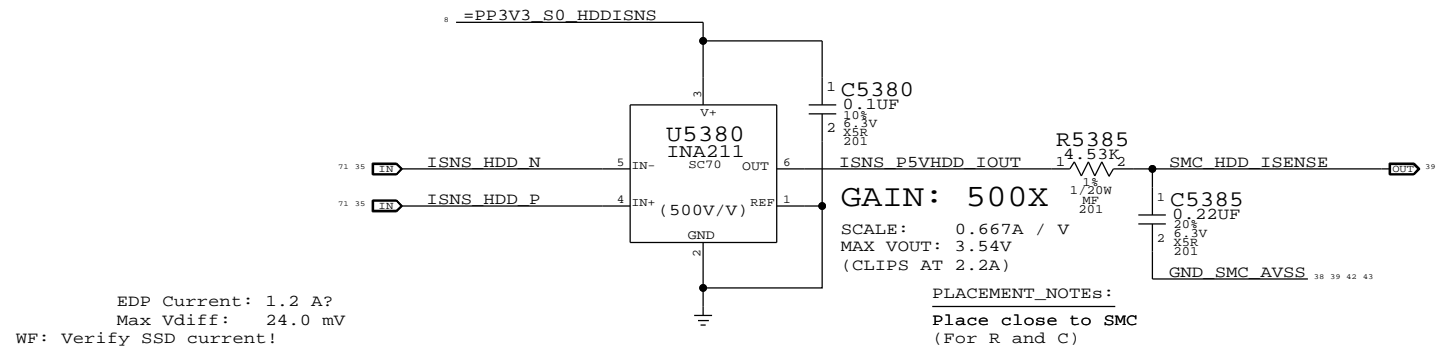
DDR3 1V5R1V35 Current Sense / Filter



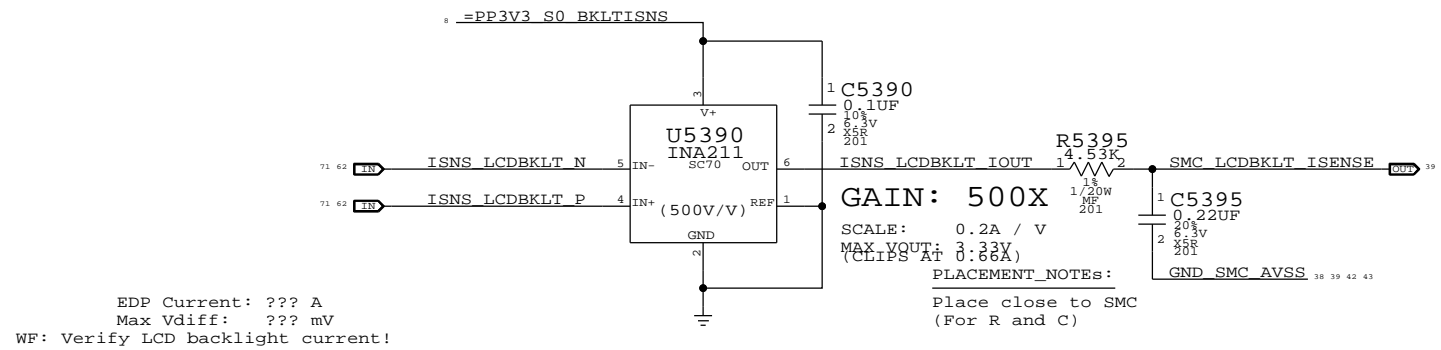
AirPort Current Sense / Filter



HDD Current Sense / Filter

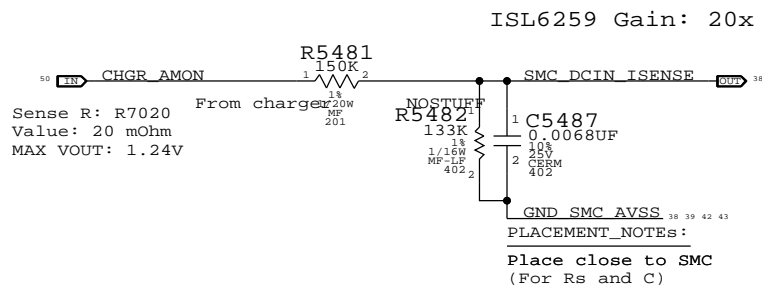


LCD Backlight Driver Input Current Sense / Filter

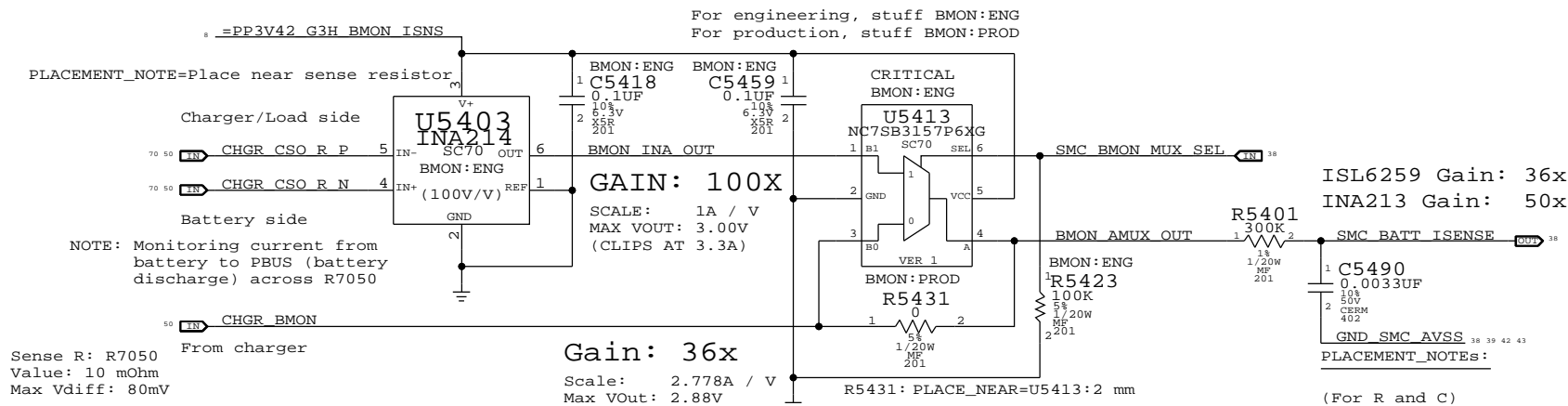


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Voltage & Current Sensing		53 OF 110	
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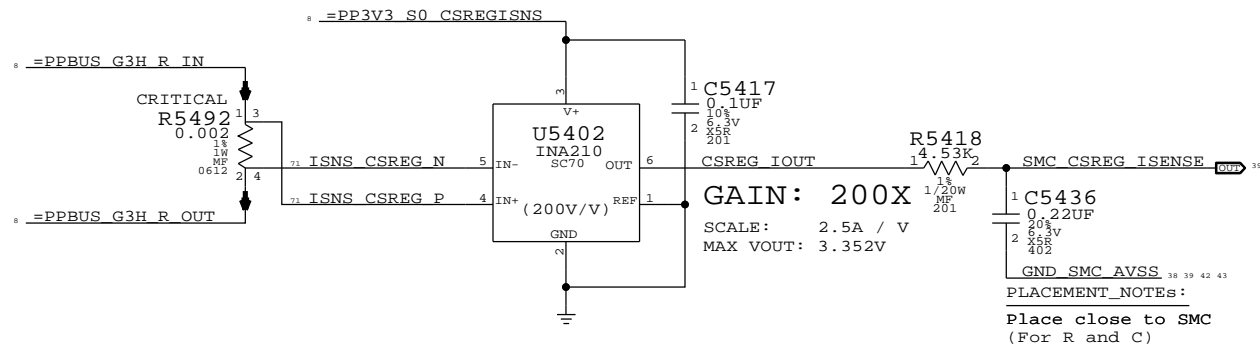
DCIN (AMON) Current Sense, RMUX & Filter



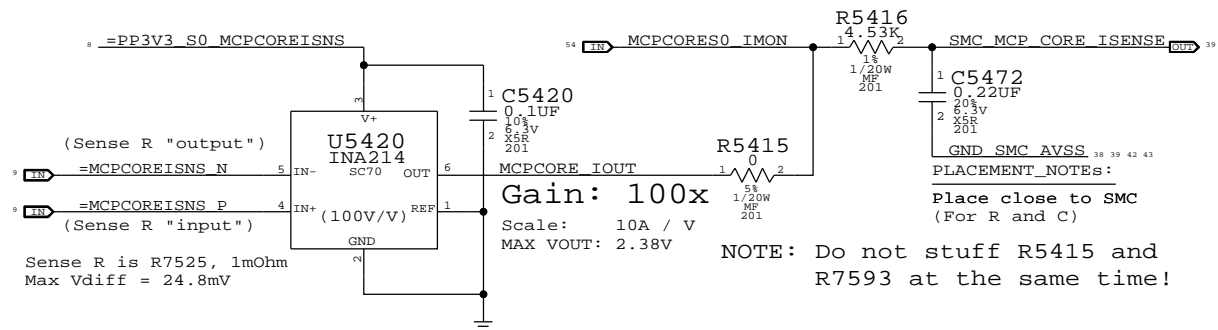
Battery (BMON) Current Sense, MUX & Filter



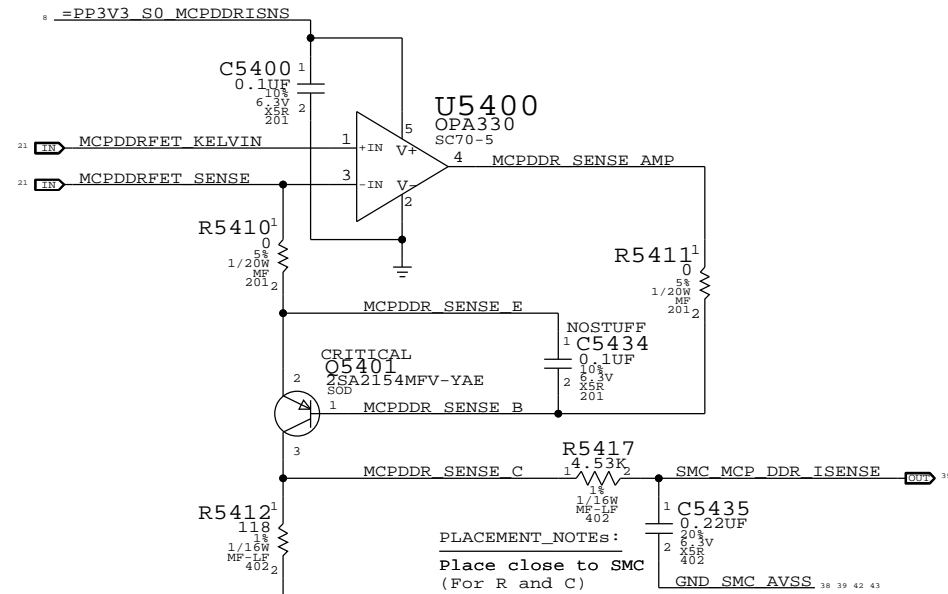
Chipset Regulators High-Side Current Sense / Filter



MCP VCore Current Sense Filter

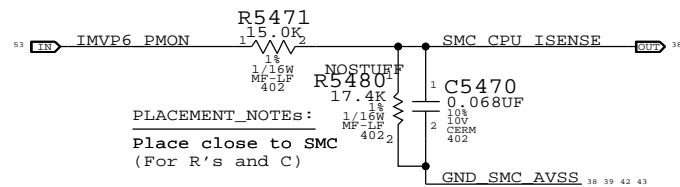



MCP MEM VDD Current Sense / Filter



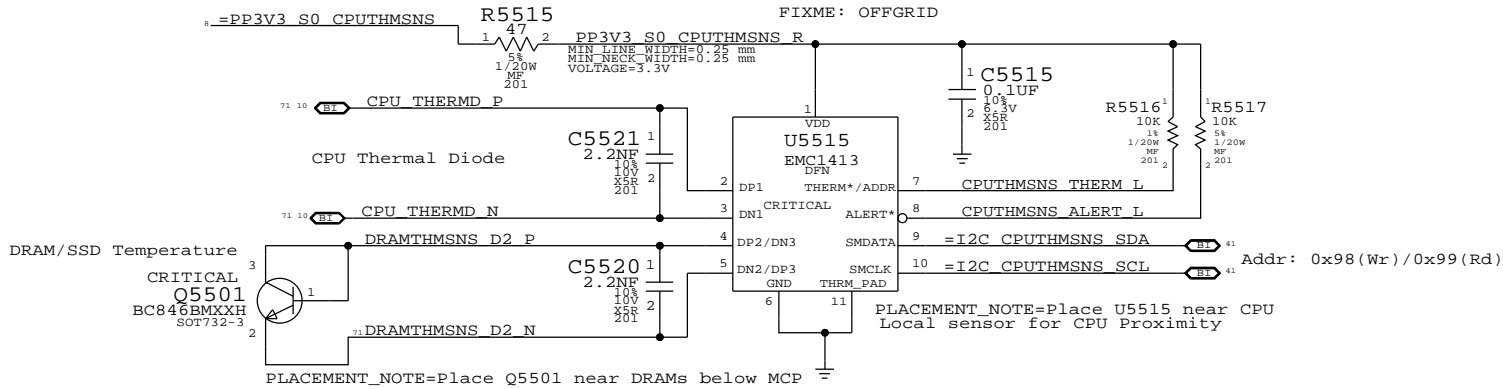
VERIFY ALL RESISTOR AND GAINS

CPU VCore Load Side Current Sense / Filter

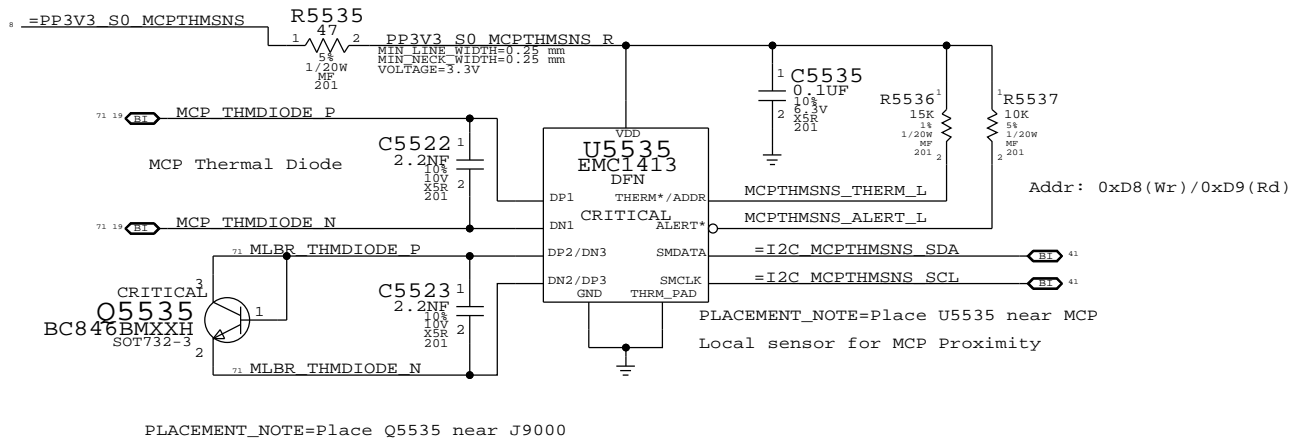


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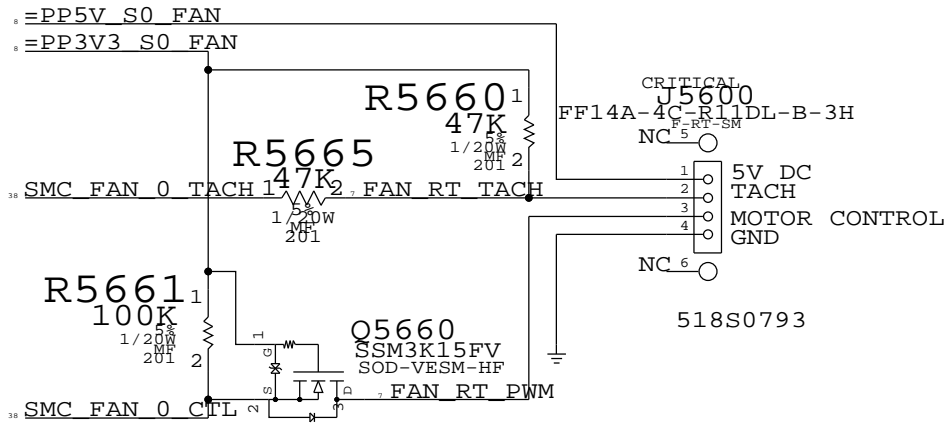
### CPU T-Diode Thermal Sensor



### MCP T-Diode Thermal Sensor

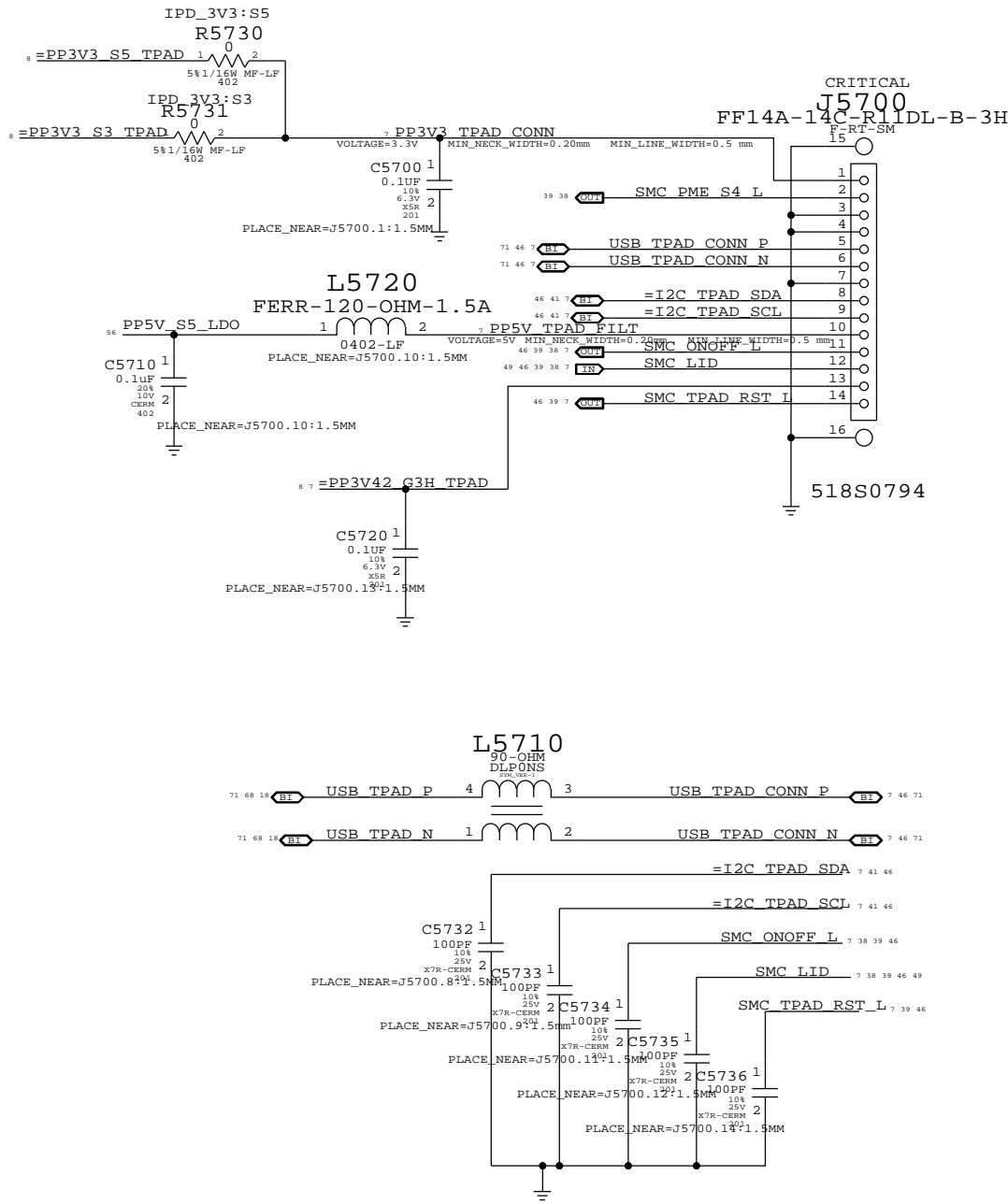


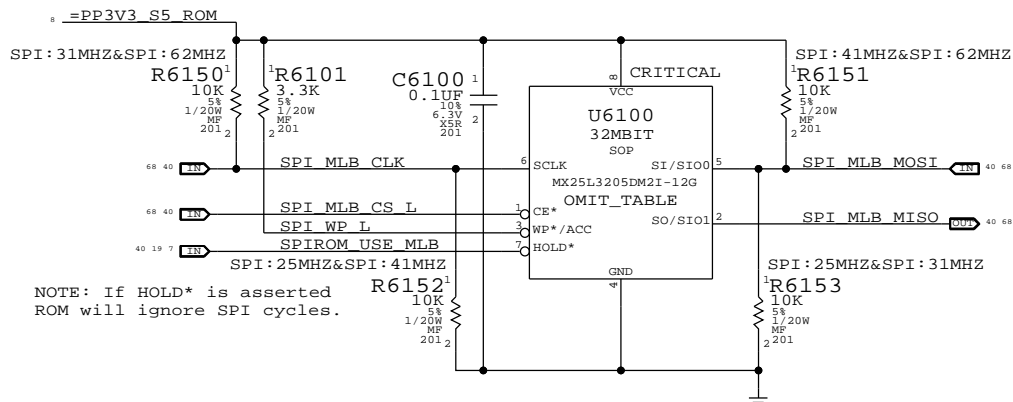
# FAN CONNECTOR





IPD Flex Connector





MCP89 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
25.0 MHz	0	0
31.2 MHz	0	1
41.7 MHz	1	0
62.5 MHz	1	1

NOTE: 42 & 62 MHz use FAST\_READ command.

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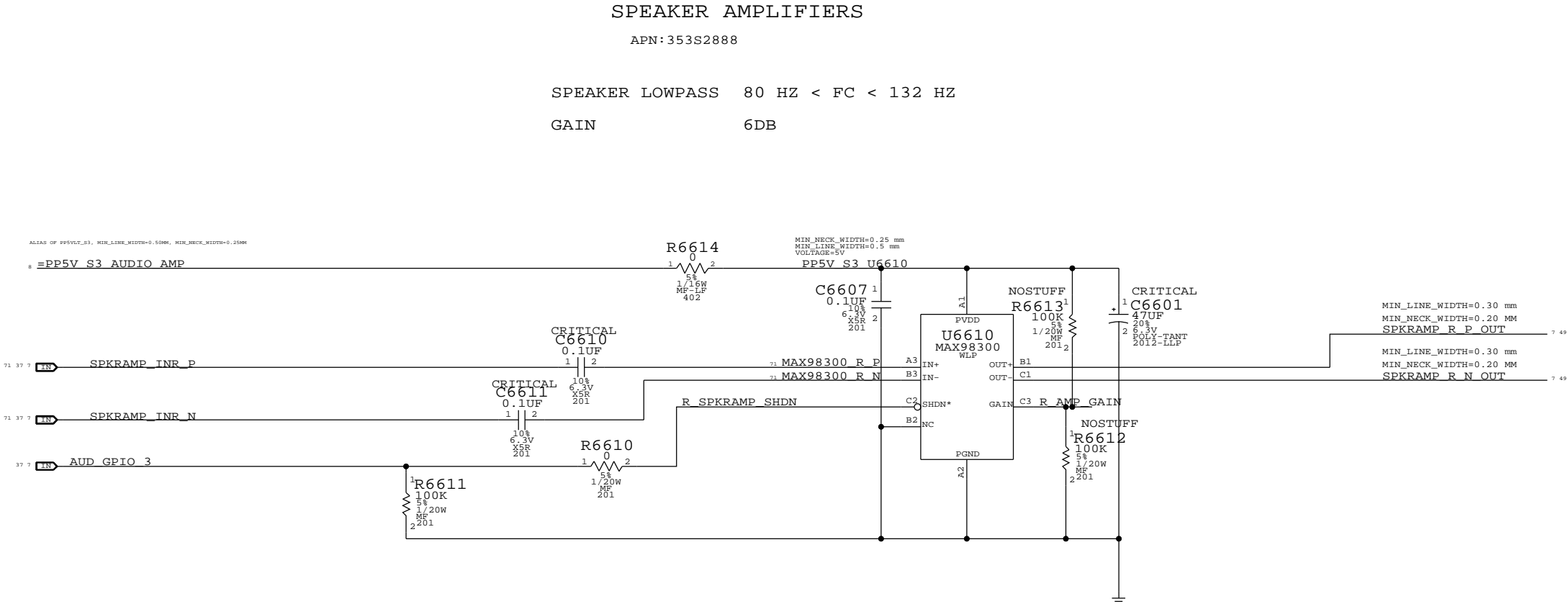
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
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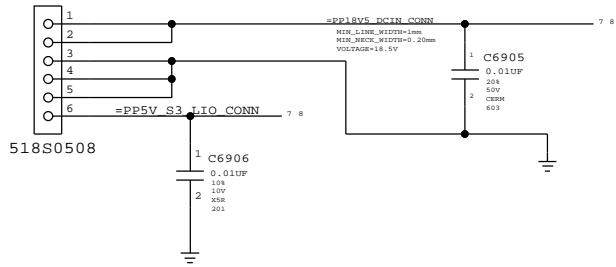
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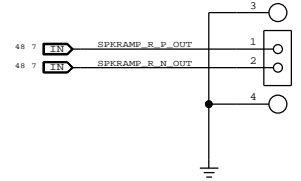
SYNC MASTER=AUDIO		SYNC DATE=02/09/2010	
PAGE TITLE			
AUDIO0: SPEAKER AMP			
 Apple Inc.	DRAWING NUMBER		SIZE
	051-8379		D
		REVISION	
		4.4.0	
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MLB TO LIO POWER CABLE CONNECTOR

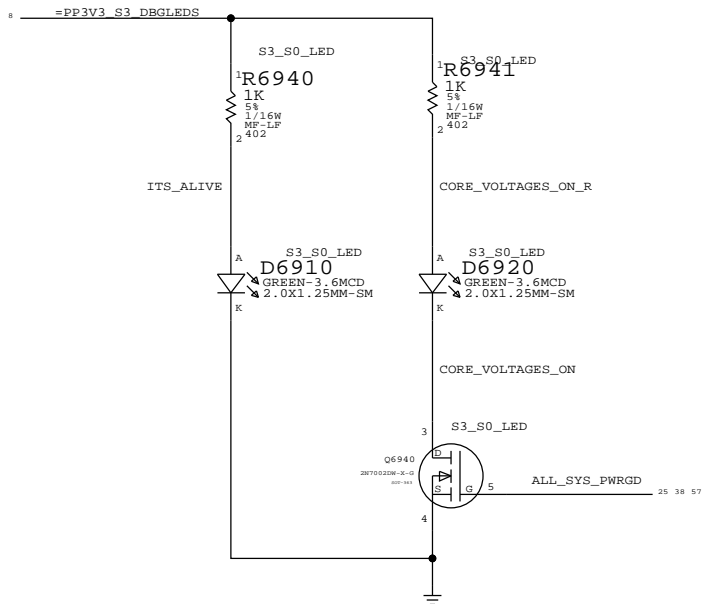
J6900  
WTB-PWR-M82  
M-RT-SM



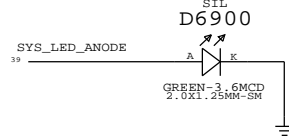
APN:518S0519  
CRITICAL  
J6903  
78171-0002  
M-RT-SM



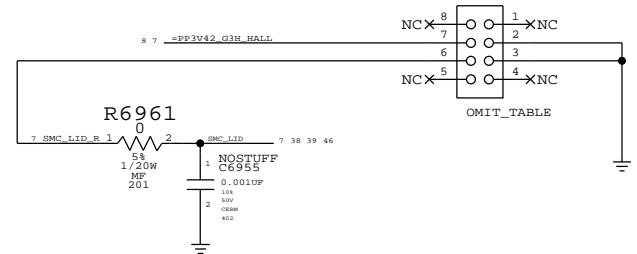
SPKR



SIL ON MLB FOR DEVELOPMENT ONLY



998-3029  
J6955  
HALL-SENSOR-MLB-PADS-K99  
SM

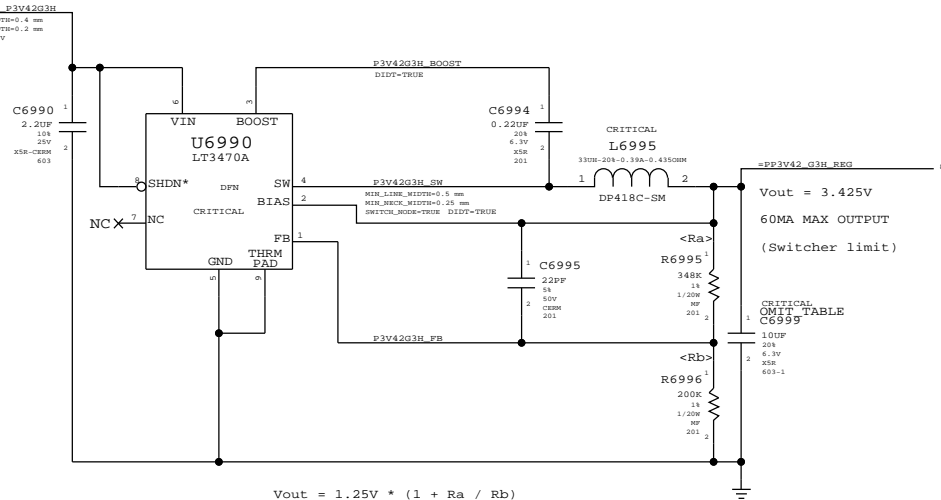


S3 AND S0 INDICATOR LEDS FOR DEVELOPMENT ONLY

HALL EFFECT PADS

3.425V "G3Hot" Supply

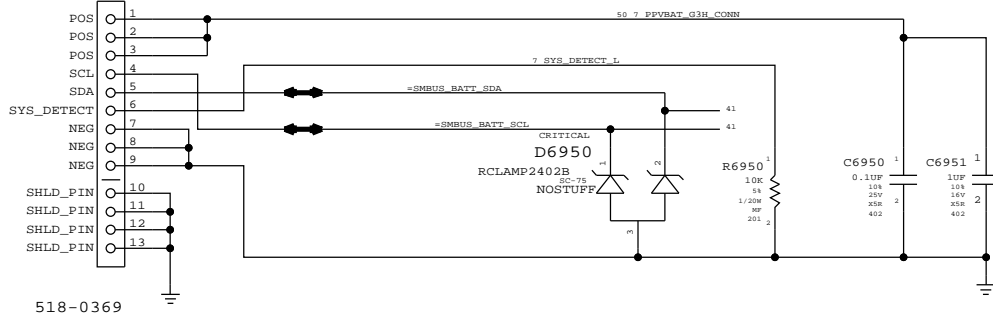
Supply needs to guarantee 3.31V delivered to SMC VRef generator




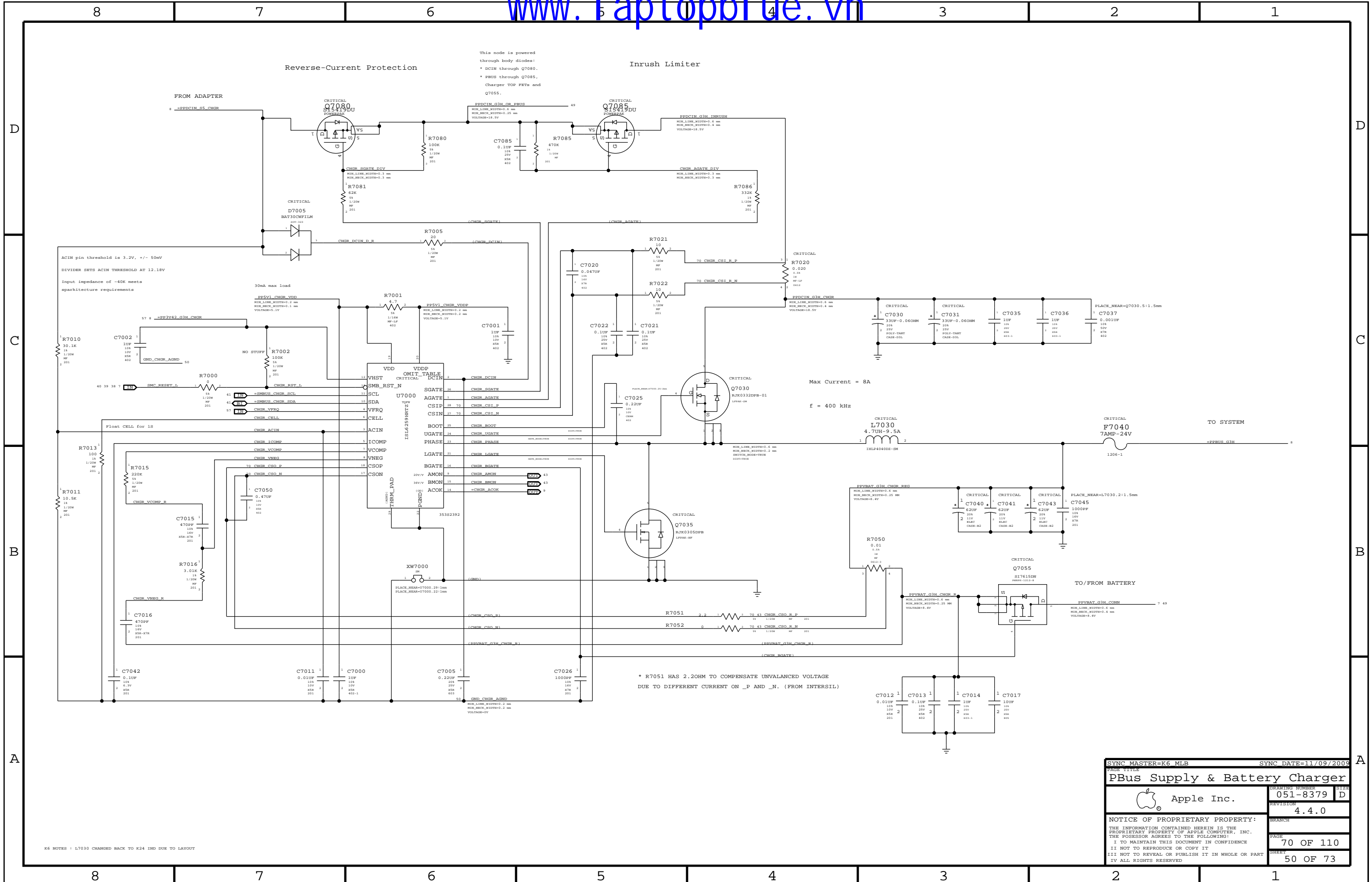
$$Vout = 1.25V * (1 + Ra / Rb)$$


BATTERY CONNECTOR

CRITICAL  
J6950  
BAT-K99  
F-RT-TH



SYNC MASTER=K84 MLB		SYNC DATE=11/09/2009	
PAGE TITLE			
DC-In & Battery Connectors			
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PAGE TITLE			
PBus Supply & Battery Charger			
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		SHEET	50 OF 73



D

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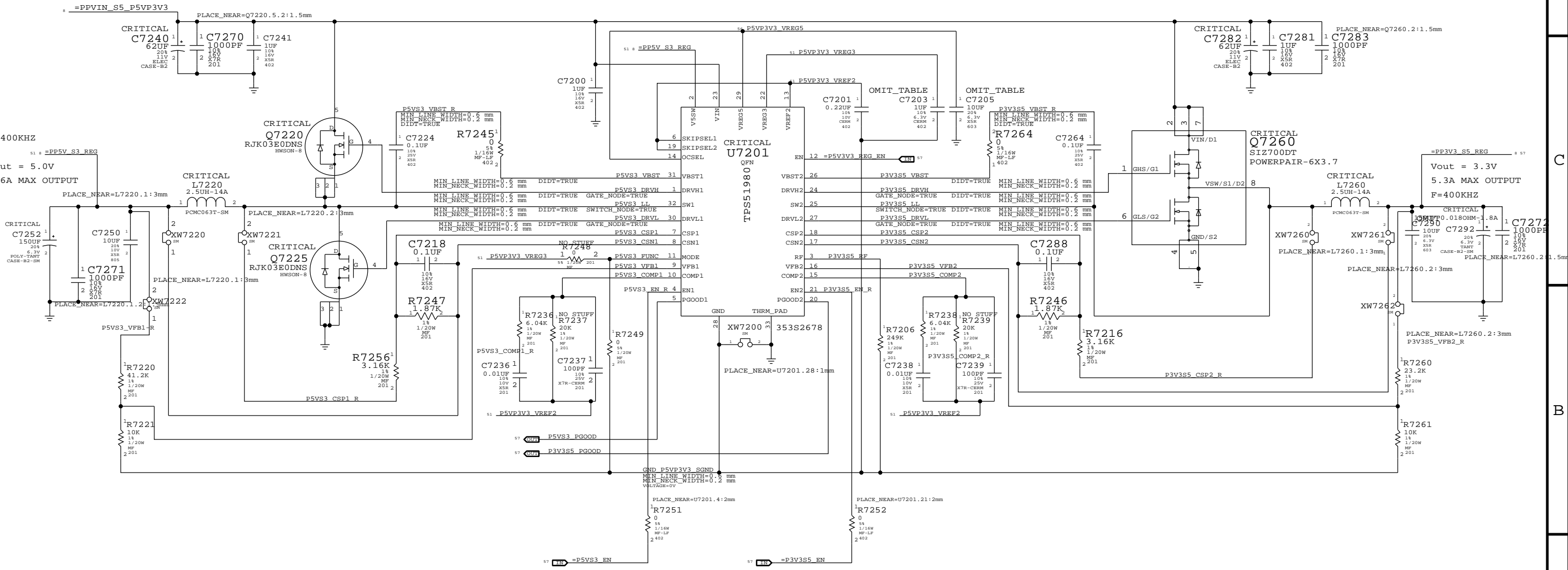
C


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SYNC MASTER=K16 MLB		SYNC DATE=07/07/2010	
PAGE TITLE			
5V / 3.3V Power Supply			
 Apple Inc.		DRAWING NUMBER	051-8379
		SIZE	D
		REVISION	4.4.0
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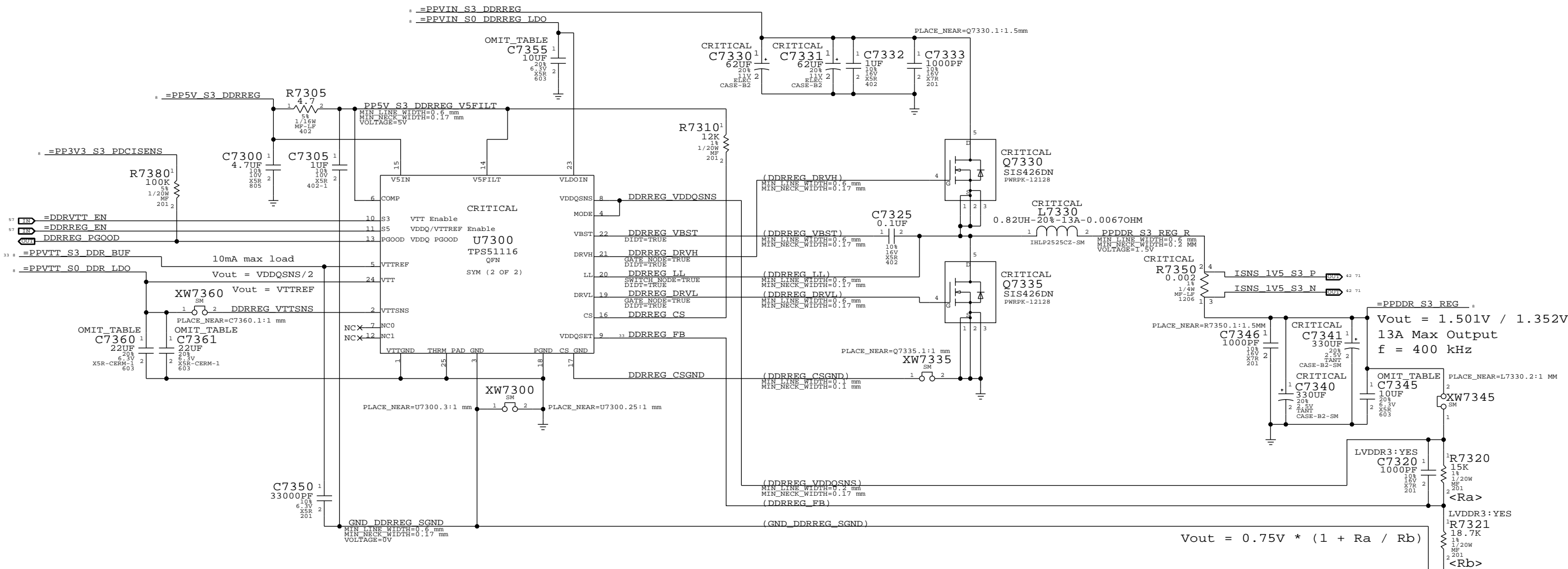
C

B

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A

A



Use LVDDR3:YES for fixed 1.35V operation or LVDDR3:NO for fixed 1.5V operation.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0331	1	RES,15K,1%,1/16W,MF-LF,0402	R7321		LVDDR3:NO

SYNC MASTER=K16_MLB		SYNC DATE=07/07/2010	
PAGE TITLE			
1.5V/1.35V LVDDR3 Supply		DRAWING NUMBER	
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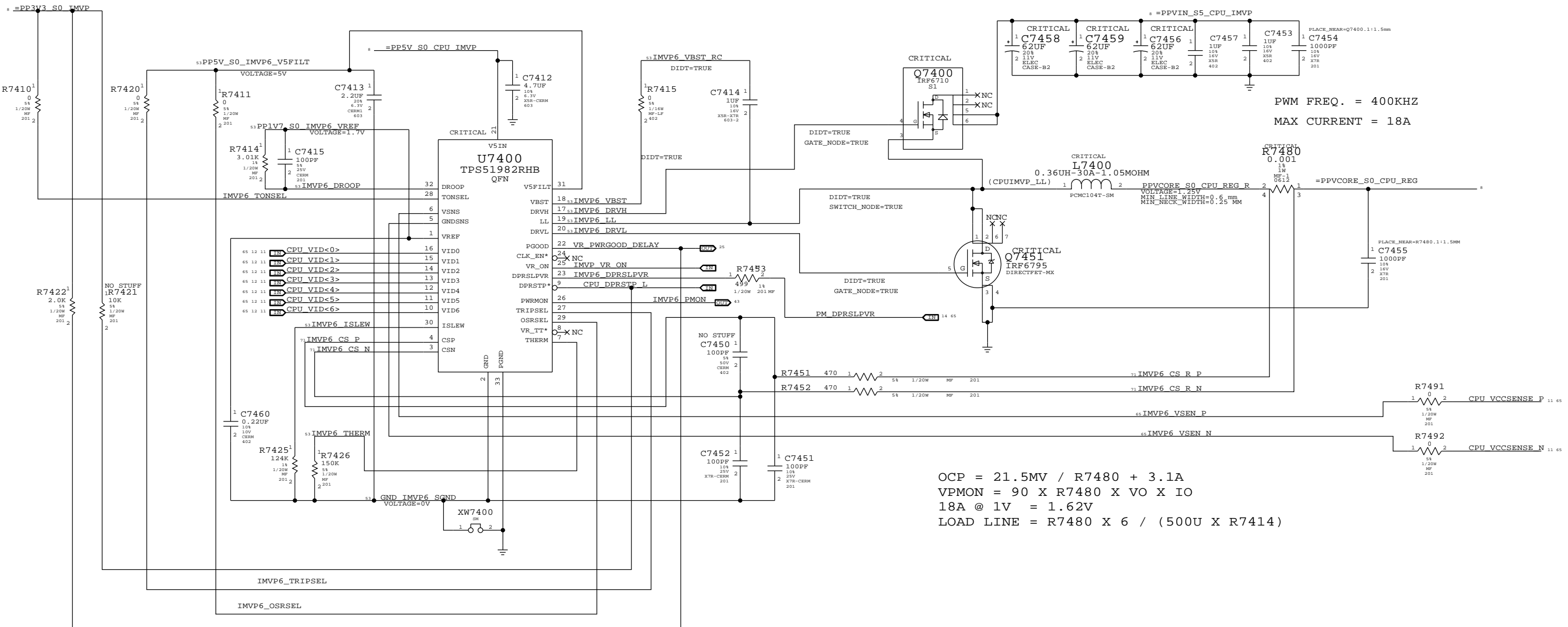
4

3

2

1

# IMVP6 CPU VCore REGULATOR



OCV = 21.5MV / R7480 + 3.1A  
VPMON = 90 X R7480 X VO X IO  
18A @ 1V = 1.62V  
LOAD LINE = R7480 X 6 / (500U X R7414)

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_LL	1.5 MM	0.20 MM
IMVP6_VBST	0.25 MM	0.20 MM
IMVP6_DRVH	1.5 MM	0.20 MM
IMVP6_DRVL	1.5 MM	0.20 MM
IMVP6_VBST_RC	1.5 MM	0.20 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_THERM	0.25 MM	0.20 MM
IMVP6_ISLEW	0.25 MM	0.20 MM
PP1V7_S0_IMVP6_VREF	0.25 MM	0.20 MM
PP5V_S0_IMVP6_V5FILT	0.25 MM	0.20 MM

SYNC\_MASTER=POWER

SYNC\_DATE=07/13/2005

IMVP6 CPU VCore Regulator

Apple Inc.

051-8379

4.4.0

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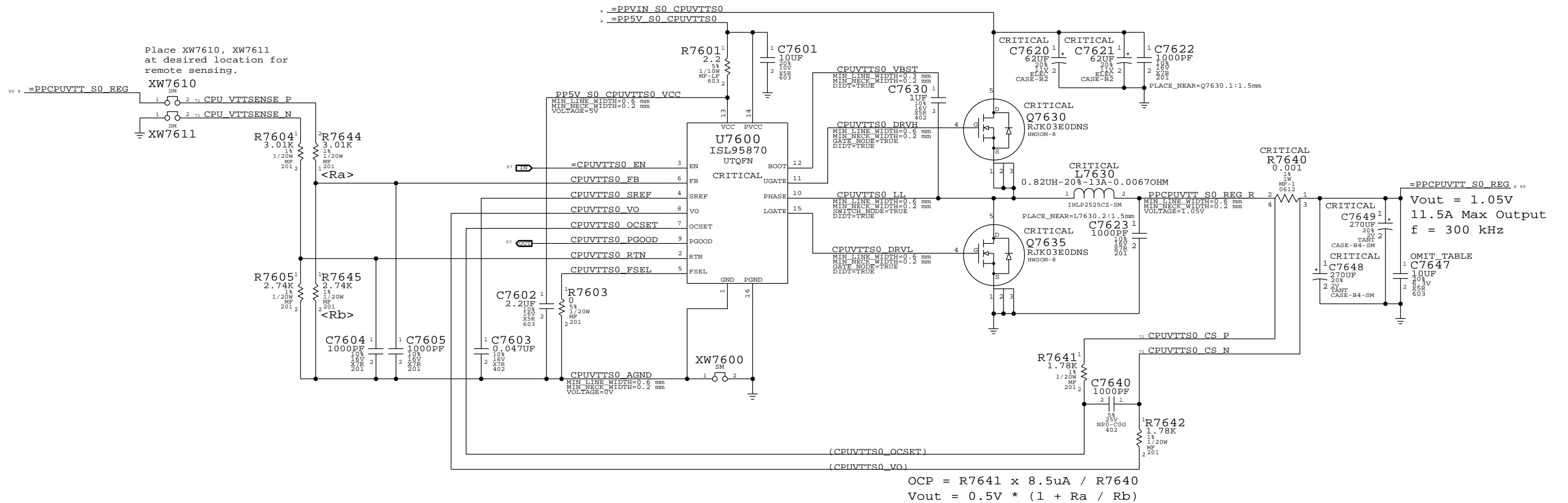
53 OF 73



B

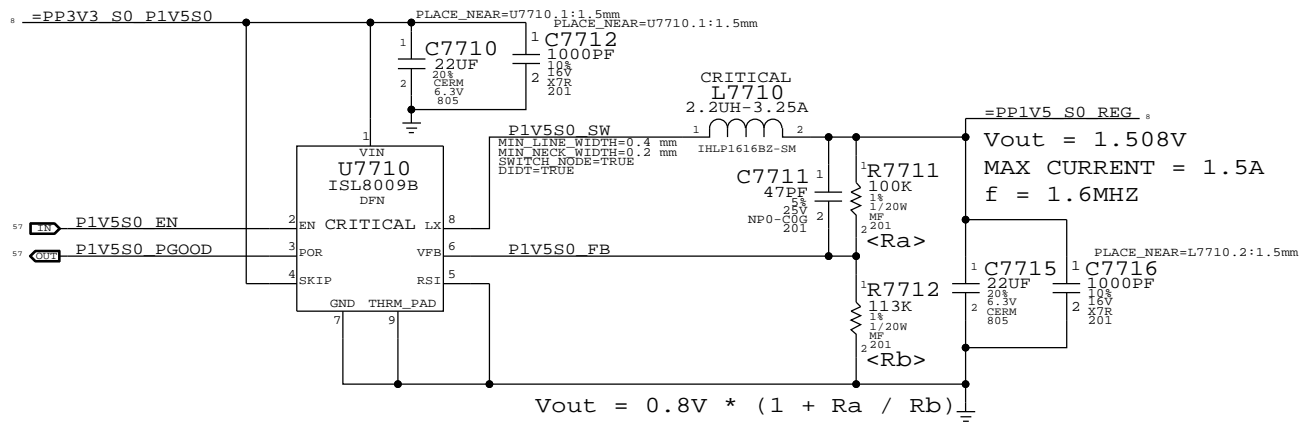
B

A

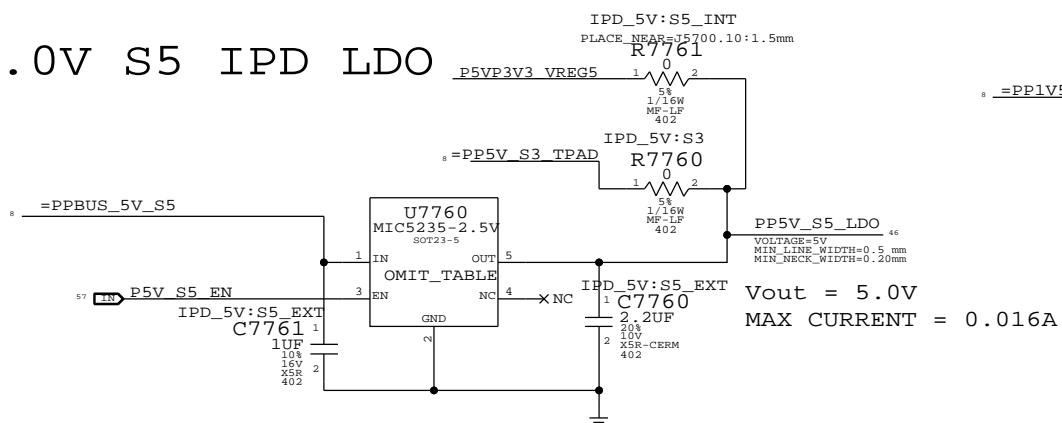




1.5V S0 Regulator

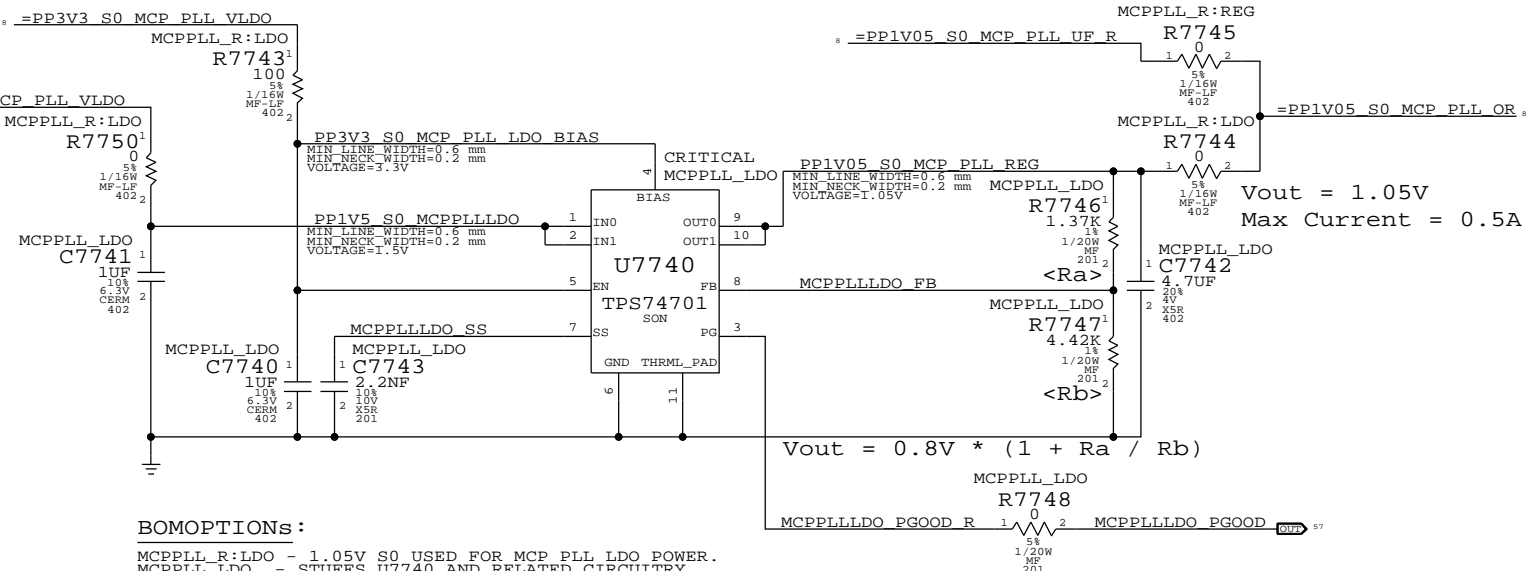


5.0V S5 IPD LDO



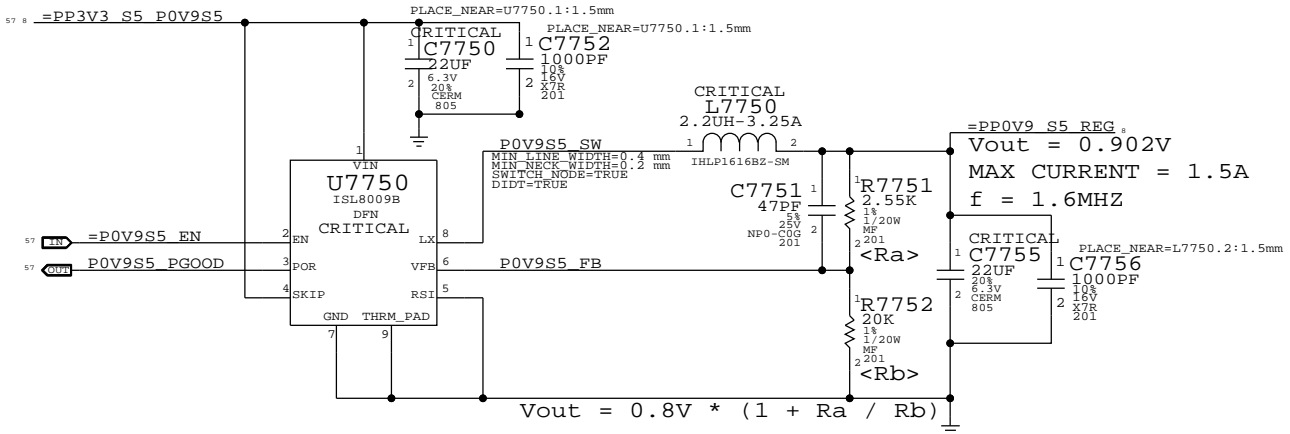
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S3034	1	IC,LDO,MIC5235,5V,1A,150MA,SOT23-5	U7760		IPD_5V:S5_EXT


1.05V S0 MCP PLL LDO



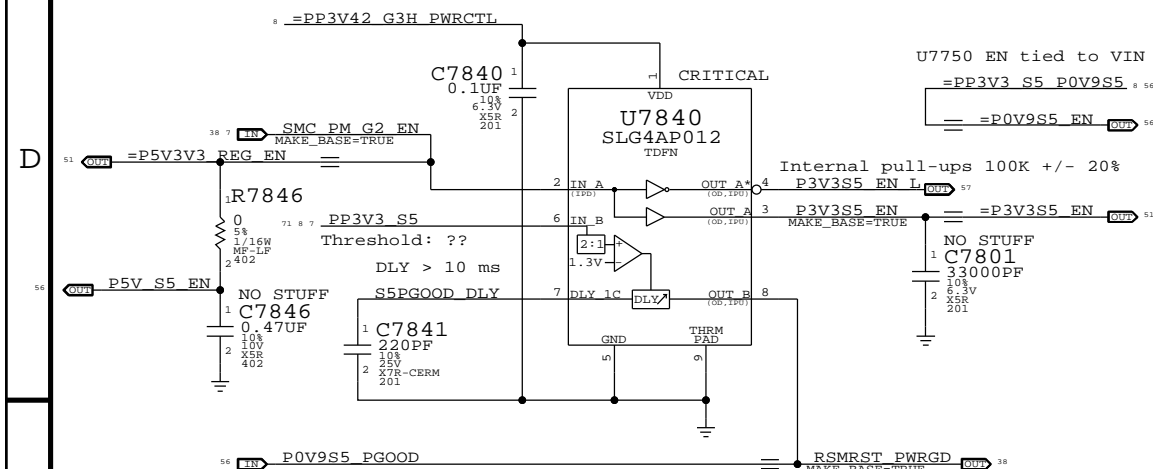
BOMOPTIONS:  
MCPPLL\_R:LDO - 1.05V S0 USED FOR MCP PLL LDO POWER.  
MCPPLL\_LDO - STUFFS U7740 AND RELATED CIRCUITRY.  
TO USE U7740, MCPPLL\_R:LDO AND MCPPLL\_LDO MUST BE ACTIVE.  
TO USE 1.05V S0, MCPPLL\_R:REG MUST BE ACTIVE, MCPPLL\_LDO CAN BE ACTIVE, MCPPLL\_R:LDO MUST BE INACTIVE.

MCP 0.9V S5 (AUXC) Switcher

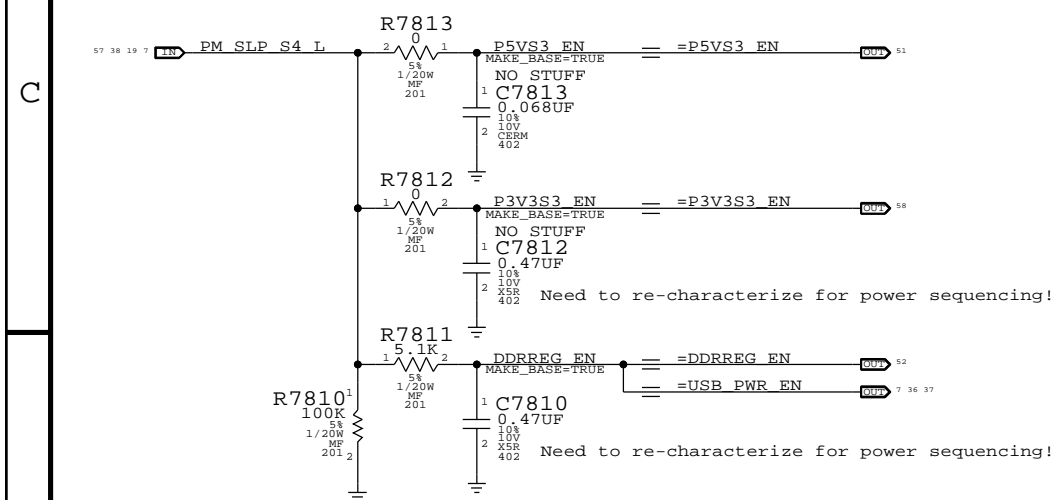


SYNC MASTER=K16 MLB		SYNC DATE=07/07/2010	
PAGE TITLE			
Misc Power Supplies			
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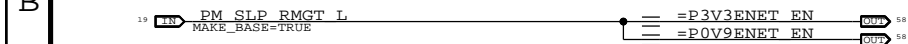
## S5 Rail Enables & PGOOD



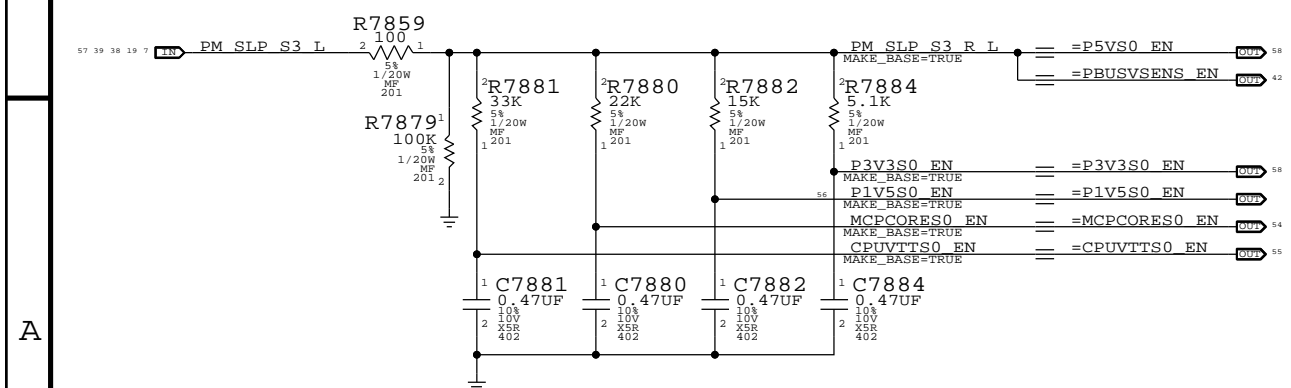
## S3 Rail Enables



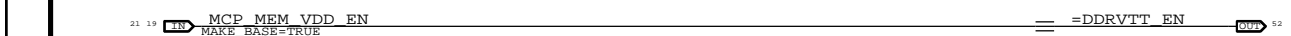
## ENET Rail Enables



## S0 Rail Enables

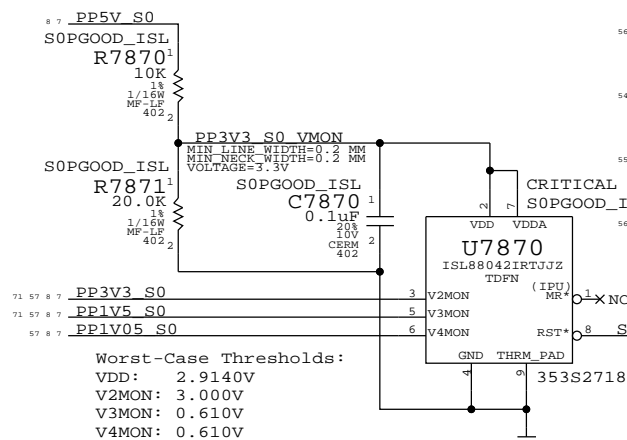


## VTT Rail Enable

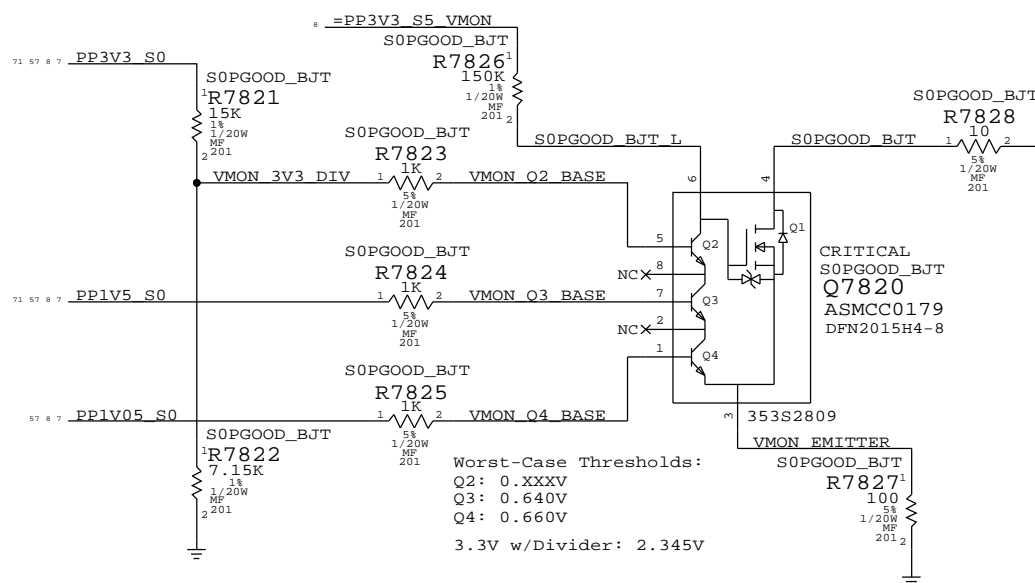


# S0 Rail PGOOD Circuitry

## S0 Rail PGOOD (ISL Version)



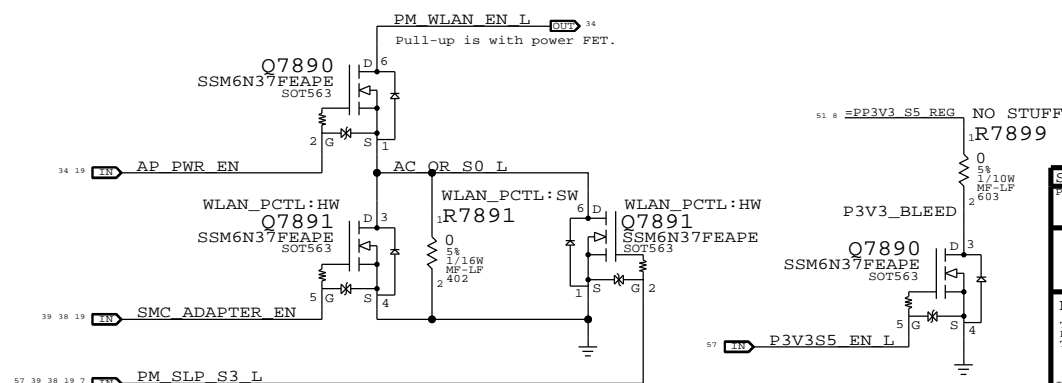
## S0 Rail PGOOD (BJT Version)



## WLAN Enable Generation

```
"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))
```

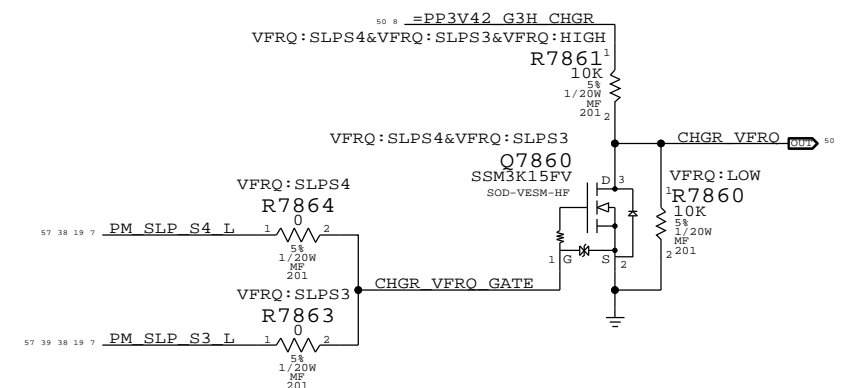
NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP\_PWR\_EN signal.  
NOTE: "AC" term valid only when Q7891 is stuffed



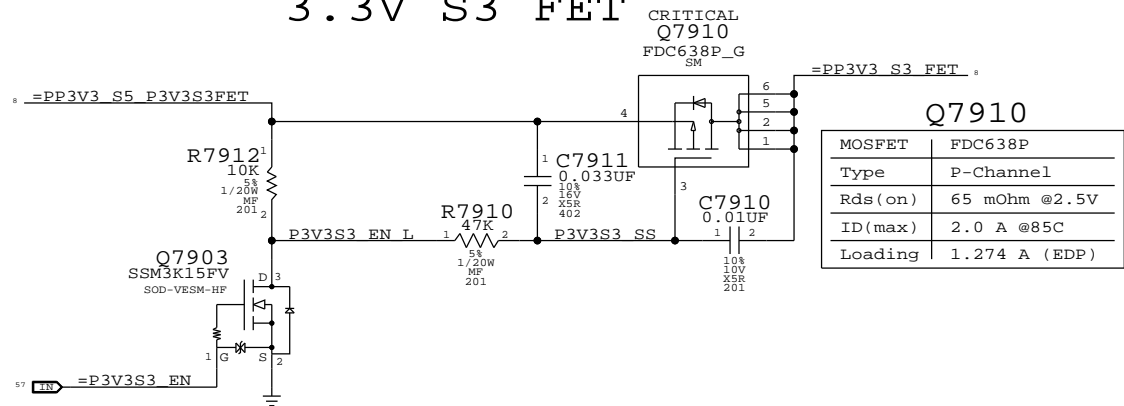
## Power Control Signals

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

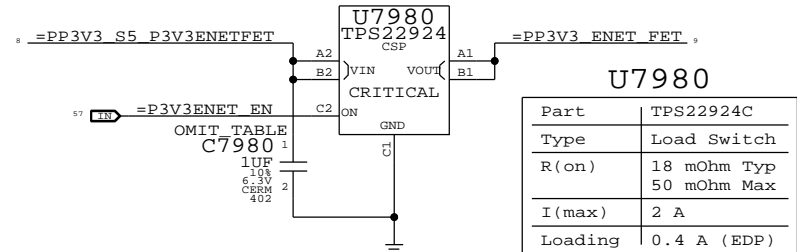
## ISL6259 Frequency Select



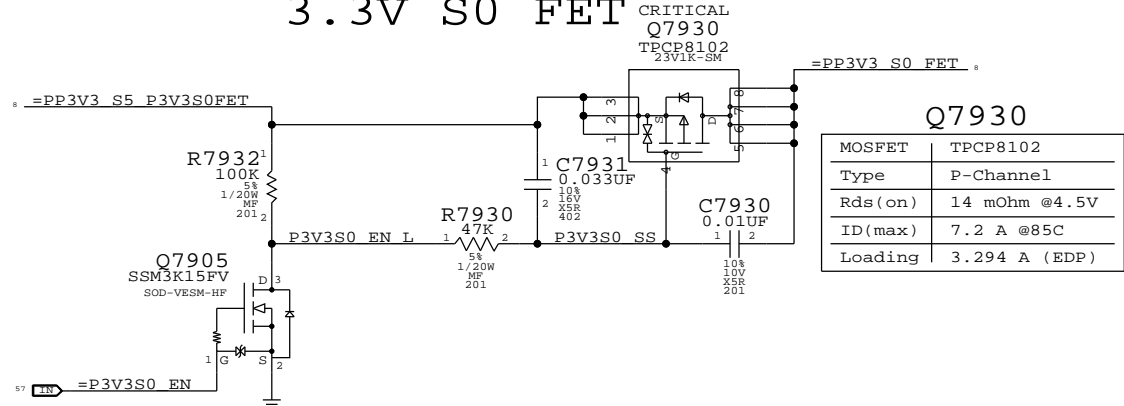
3.3V S3 FET



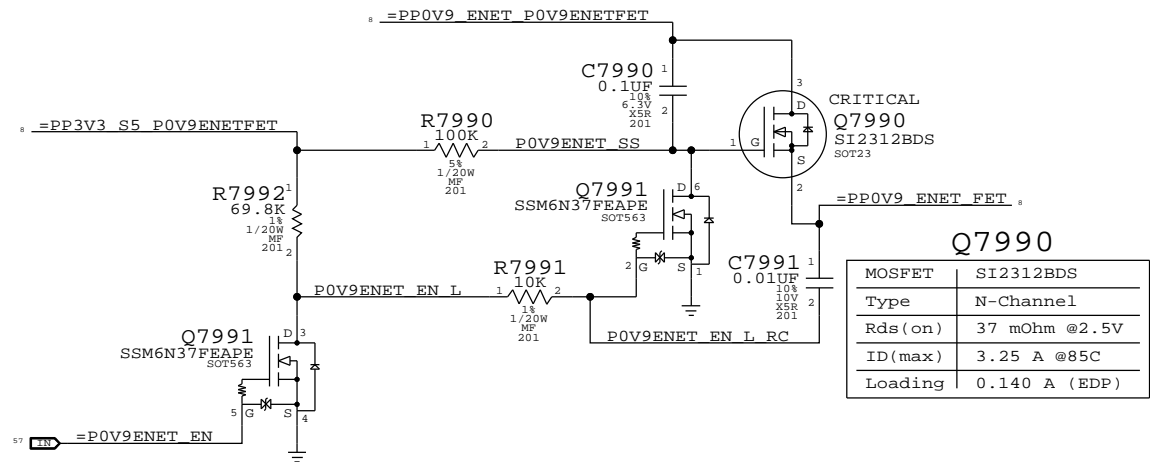
3.3V ENET Switch



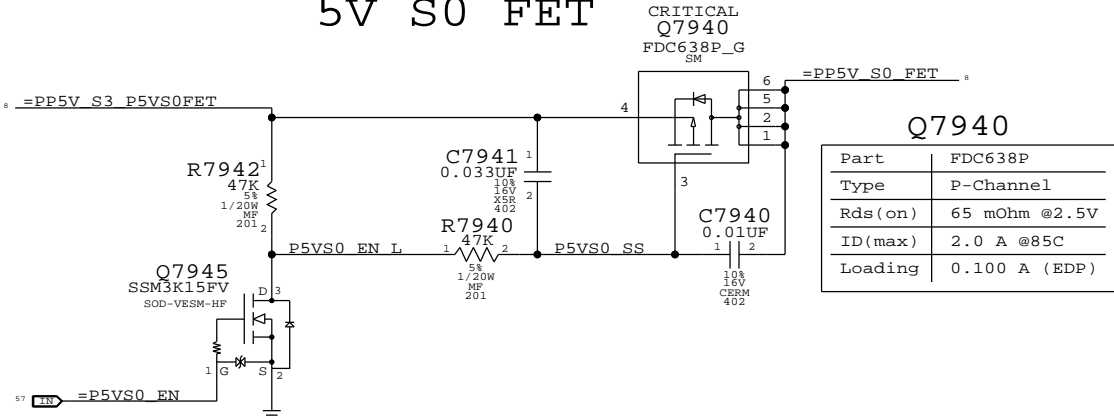
3.3V S0 FET

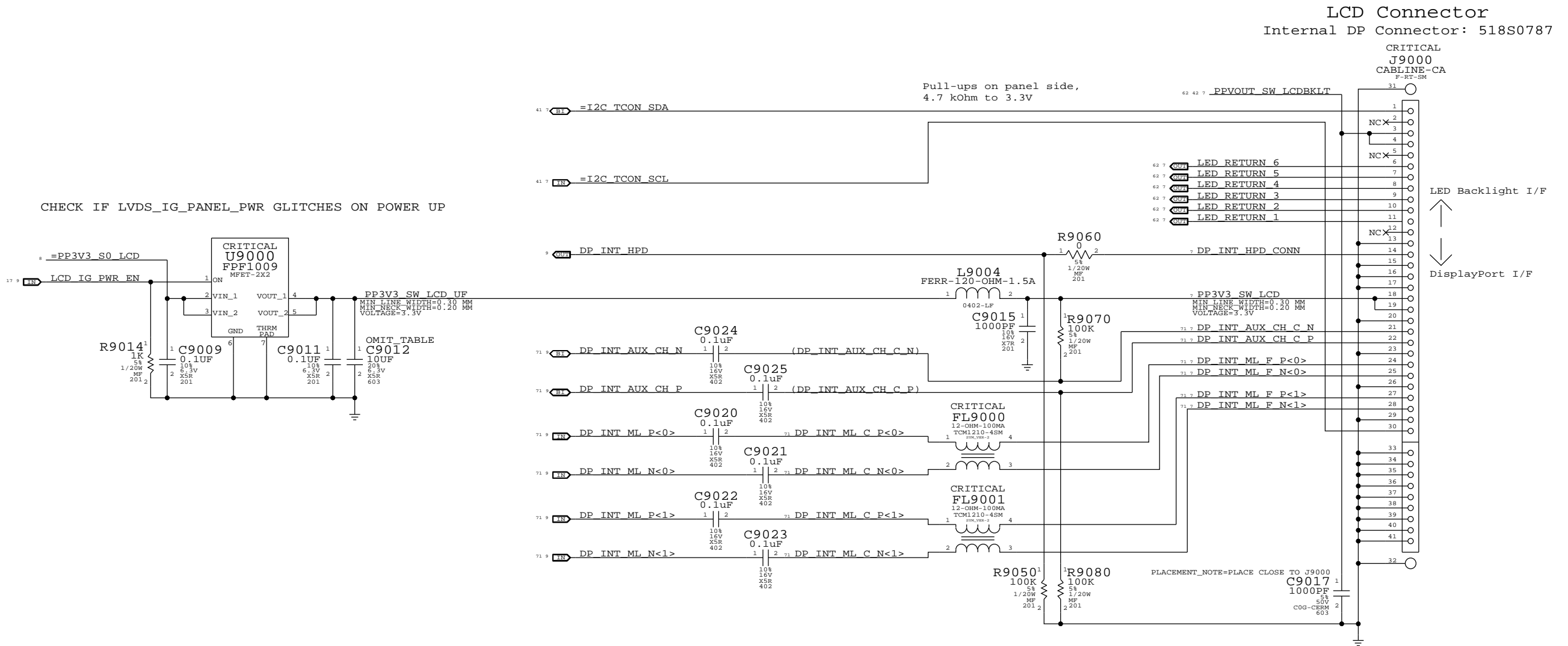


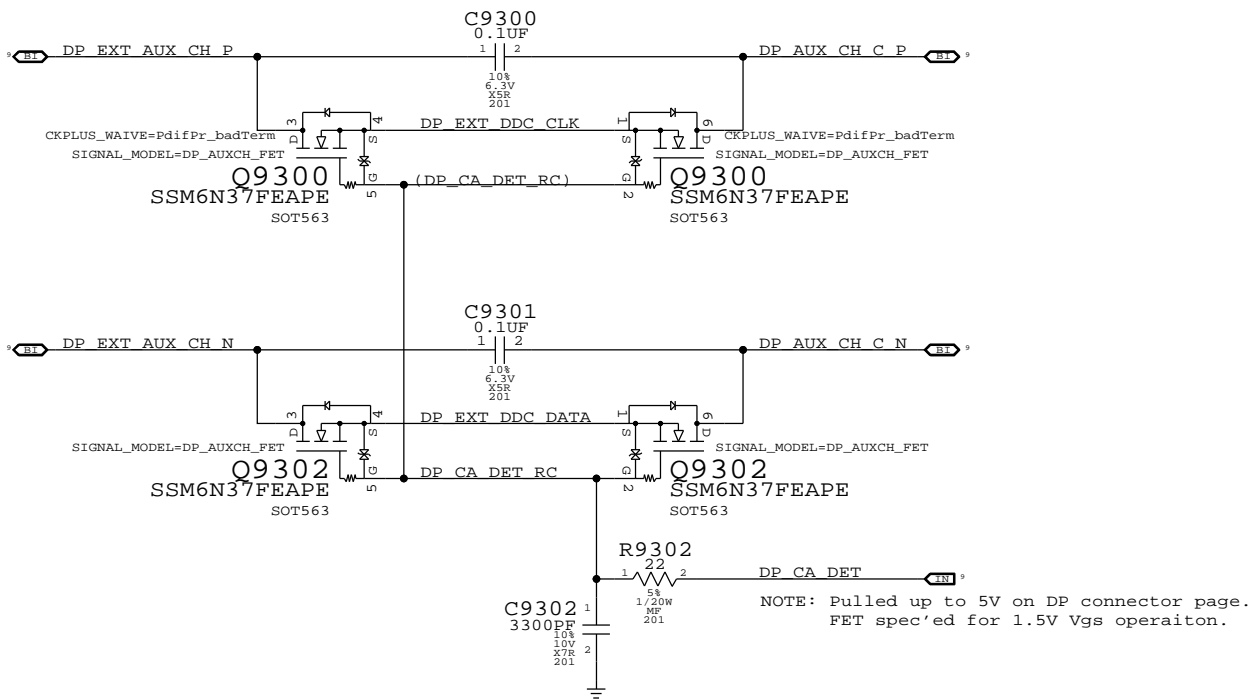
0.9V ENET FET



5V S0 FET

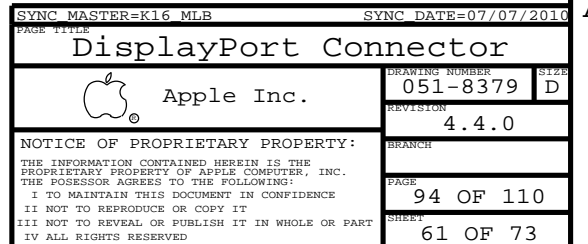


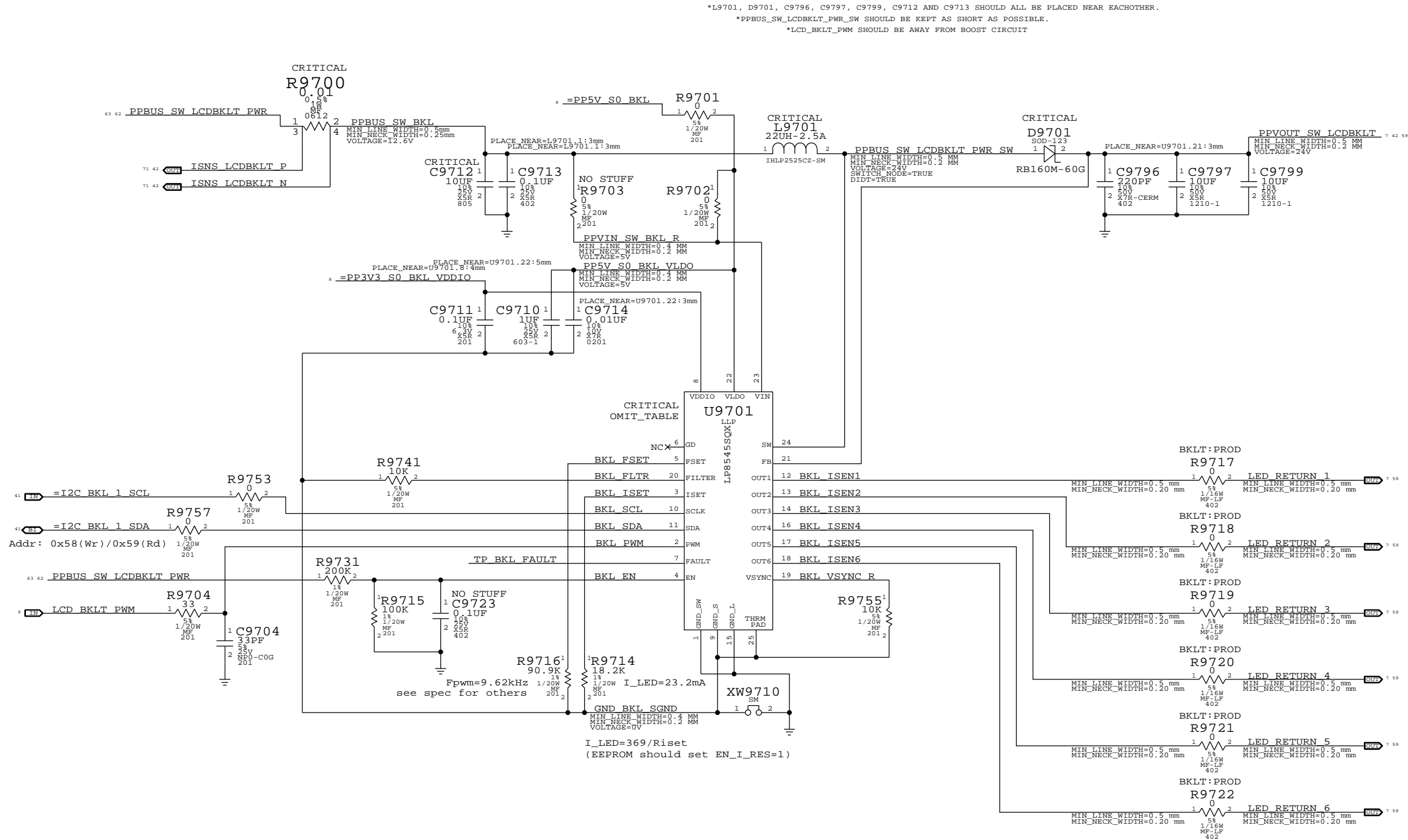






## L9400




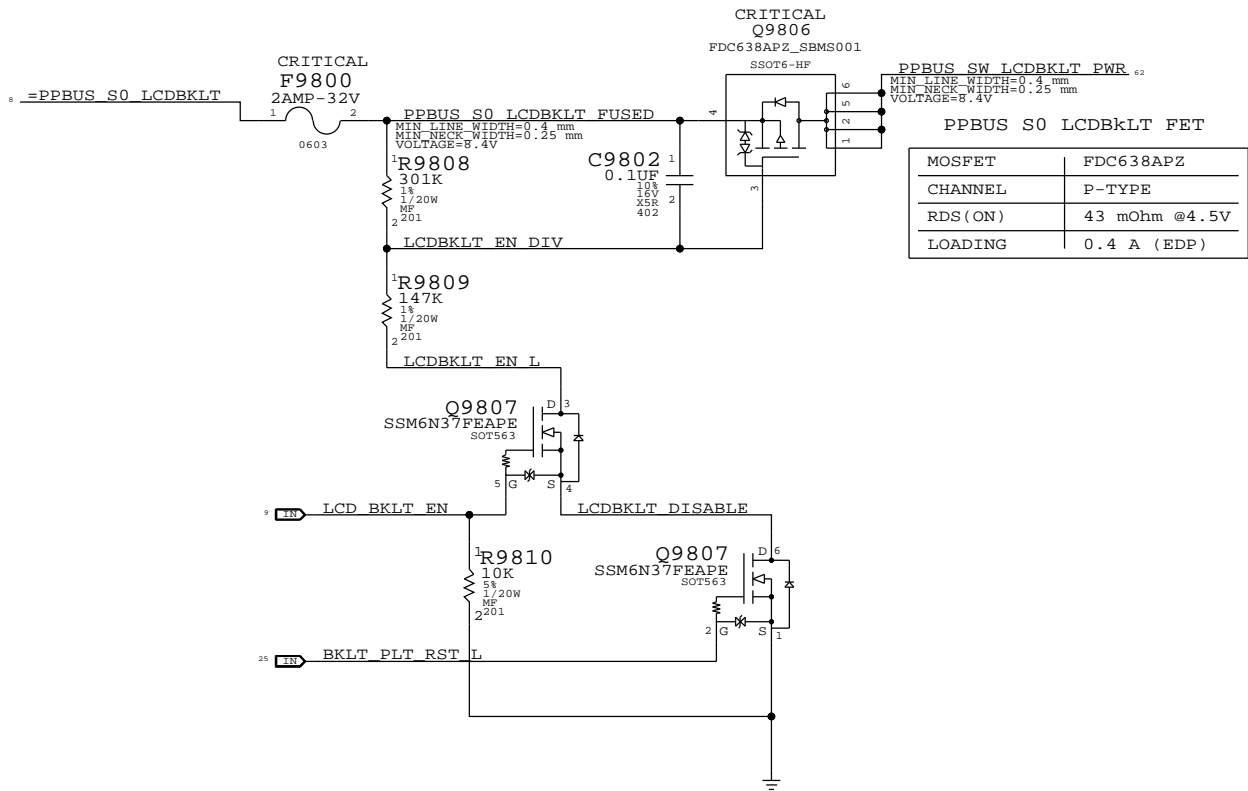


FOR LP8543:  
STUFF R9741  
NO STUFF R9740, C9740, C9741, R9754

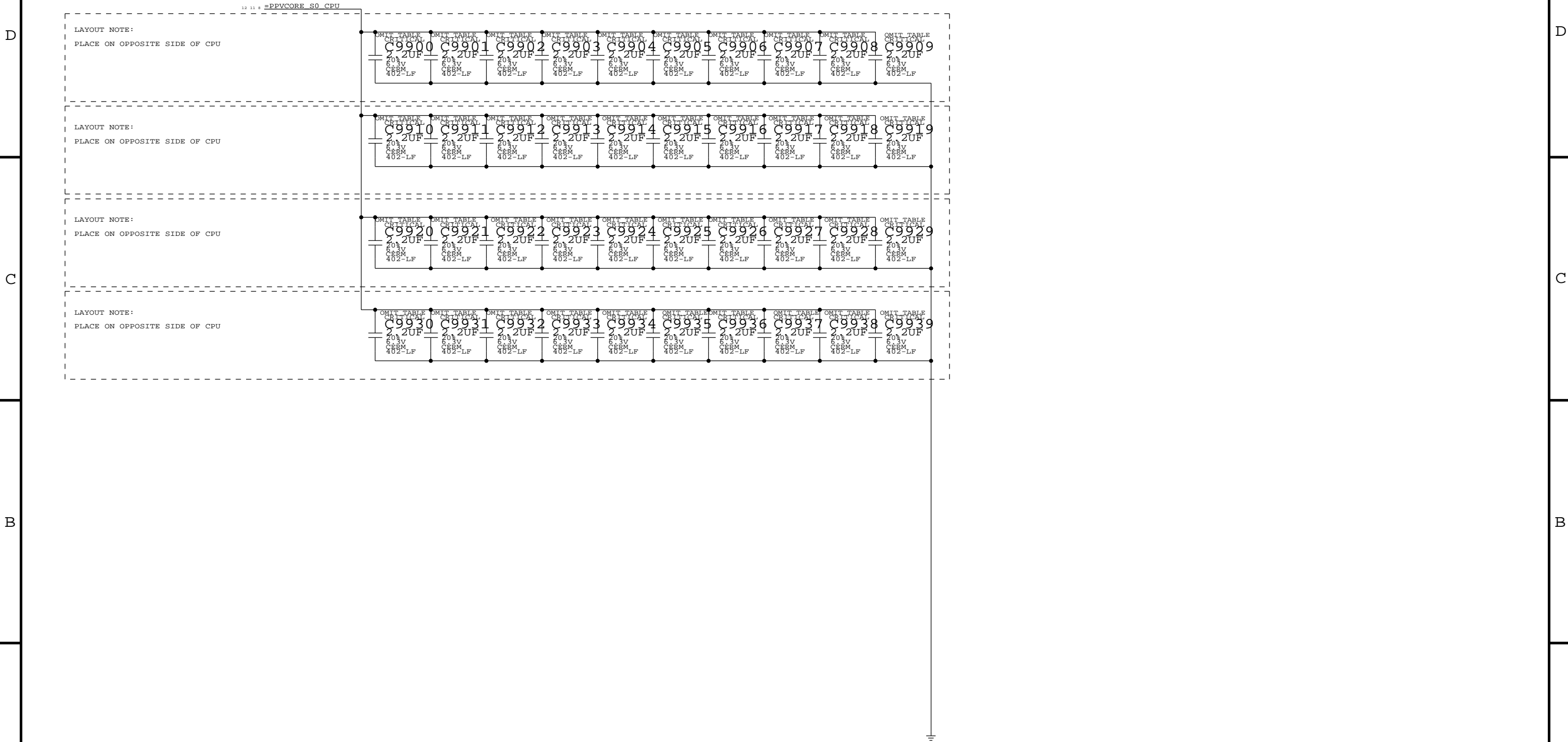
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9717,R9718,R9719		BKLT:ENG
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9720,R9721,R9722		BKLT:ENG
353S2896	1	IC,LP8545,LED BKLT CTRLR,PRODUCTIO,LLP24	U9701	CRITICAL	PROJ:K16
353S2967	1	IC,LP8545,LED BKLT CTRLR,LLP24,K99 VER	U9701	CRITICAL	PROJ:K99

10.2 ohm resistors for current measurement on LED strings.

SYNC MASTER=K16 MLB		SYNC DATE=03/31/2010		
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ADDITIONAL CPU VCORE HF DECOUPLING  
40x 1uF 0402



FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?	FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?	FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?	FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	*	=2x_DIELECTRIC	?	FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?	FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.

Signals within each 4x group should be matched within 5 ps of strobe.

DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 135 ps.

Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.

FSB 2X signals / groups shown in signal table on right.

Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 270 ps.

Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.

Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP89 Interface DG (DG-04625-001\_v0.9), Section 2.1

SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?	CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_8MIL	*	8 MIL	?				
CPU_COMP	*	25 MIL	?				
CPU_GTLREF	*	25 MIL	?				
CPU_ITP	*	=2:1_SPACING	?				
CPU_VCCSENSE	*	25 MIL	?				

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.

Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP89 Interface DG (DG-04625-001\_v0.9), Section 2.1

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP89 Interface DG (DG-04625-001\_v0.9), Section 2.1.4

FSB Clock Constraints


PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?	CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2.5

CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB D L<15..0>	7 10 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB DINV L<0>	7 10 14
FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<0>	7 10 14
FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<0>	7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB D L<31..16>	7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB DINV L<1>	7 10 14
FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<1>	7 10 14
FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<1>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB D L<47..32>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB DINV L<2>	7 10 14
FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<2>	7 10 14
FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<2>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB D L<63..48>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB DINV L<3>	7 10 14
FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<3>	7 10 14
FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<3>	7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB A L<16..3>	7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB REQ L<4..0>	7 10 14
FSB_ADSTB0	FSB_55S	FSB_ADSTB	FSB ADSTB L<0>	7 10 14
FSB_ADDR_GROUP1	FSB_55S	FSB_ADDR	FSB A L<35..17>	7 10 14
FSB_ADSTB1	FSB_55S	FSB_ADSTB	FSB ADSTB L<1>	7 10 14
FSB_1X	FSB_55S	FSB_1X	FSB ADS L	7 10 14
FSB_BREQ0_L	FSB_55S	FSB_1X	FSB_BREQ0_L	10 14
FSB_1X	FSB_55S	FSB_1X	FSB BNR L	10 14
FSB_1X	FSB_55S	FSB_1X	FSB BPRI L	10 14
FSB_1X	FSB_55S	FSB_1X	FSB DBSY L	10 14
FSB_1X	FSB_55S	FSB_1X	FSB DEFER L	10 14
FSB_1X	FSB_55S	FSB_1X	FSB DRDY L	10 14
FSB_1X	FSB_55S	FSB_1X	FSB HIT L	7 10 14
FSB_1X	FSB_55S	FSB_1X	FSB HITM L	7 10 14
FSB_1X	FSB_55S	FSB_1X	FSB LOCK L	7 10 14
FSB_CPURST_L	FSB_55S	FSB_1X	FSB_CPURST L	10 13 14
FSB_1X	FSB_55S	FSB_1X	FSB RS L<2..0>	10 14
FSB_1X	FSB_55S	FSB_1X	FSB TRDY L	10 14
CPU_ASYNC	CPU_55S	CPU_AGTL	CPU A20M L	10 14
CPU_BSEL	CPU_55S	CPU_AGTL	CPU_BSEL<2..0>	9 10
CPU_FERR_L	CPU_55S	CPU_8MITL	CPU FERR L	10 14
CPU_ASYNC	CPU_55S	CPU_AGTL	CPU IGNE L	10 14
CPU_INIT_L	CPU_55S	CPU_AGTL	CPU INIT L	10 14
CPU_ASYNC_R	CPU_55S	CPU_AGTL	CPU INTR	10 14
CPU_ASYNC_R	CPU_55S	CPU_AGTL	CPU NMI	10 14
CPU_PROCHOT_L	CPU_55S	CPU_AGTL	CPU PROCHOT L	10 14 39
CPU_PWRGD	CPU_55S	CPU_AGTL	CPU_PWRGD	10 13 14
CPU_ASYNC	CPU_55S	CPU_AGTL	CPU SMI L	10 14
CPU_ASYNC	CPU_55S	CPU_AGTL	CPU STPCLK L	10 14
PM_THERMTRIP_L	CPU_55S	CPU_8MITL	PM THERMTRIP L	10 14 39
FSB_CPUSLP_L	CPU_55S	CPU_AGTL	FSB_CPUSLP L	10 14
CPU_FROM_SR	CPU_55S	CPU_AGTL	CPU DPSLP L	10 14
CPU_DPRSTP_L	CPU_55S	CPU_AGTL	CPU_DPRSTP L	10 14 53
CPU_ASYNC	CPU_55S	CPU_AGTL	FSB DPWR L	10 14
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB CLK CPU P	10 14
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB CLK CPU N	10 14
FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB CLK ITP P	13 14
FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB CLK ITP N	13 14
FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB CLK MCP P	14
FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB CLK MCP N	14
CPU_IERR_L	CPU_55S		CPU IERR L	10
PM_DPRSLPVR	CPU_55S	CPU_AGTL	PM DPRSLPVR	14 53
(See above)	CPU_55S	CPU_AGTL	IMVP DPRSLPVR	
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP VDD	14
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP GND	14
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP VCC	14
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP GND	14
CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU GTLREF	10 33
CPU_COMP	CPU_50S	CPU_COMP	CPU COMP<3>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<2>	10
CPU_COMP	CPU_50S	CPU_COMP	CPU COMP<1>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<0>	10
XDP_TDI	CPU_55S	CPU_ITP	XDP TDI	10 13
XDP_TDO	CPU_55S	CPU_ITP	XDP TDO	10 13
XDP_TMS	CPU_55S	CPU_ITP	XDP TMS	10 13
XDP_TCK	CPU_55S	CPU_ITP	XDP TCK	10 13
XDP_TRST_L	CPU_55S	CPU_ITP	XDP TRST L	10 13
XDP_BPM_L	CPU_55S	CPU_ITP	XDP BPM L<4..0>	10 13
XDP_BPM_L5	CPU_55S	CPU_ITP	XDP BPM L<5>	10 13
(FSB_CPURST_L)	CPU_55S	CPU_ITP	XDP CPURST L	13
	CPU_55S	CPU_8MITL	CPU VID<6..0>	11 12 53
	CPU_55S	CPU_8MITL	IMVP6 VID<6..0>	12
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE P	11 53
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE N	11 53
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN P	53
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN N	53

SYNC MASTER=K16 MLB		SYNC DATE=07/07/2010	
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CPU/FSB Constraints			
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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_QS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_QS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_QS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_QS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_QS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_QS	MEM_CLK	*	MEM_QS2MEM
MEM_QS	MEM_CTRL	*	MEM_QS2MEM
MEM_QS	MEM_CMD	*	MEM_QS2MEM
MEM_QS	MEM_DATA	*	MEM_QS2MEM
MEM_QS	MEM_QS	*	MEM_QS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_QS	*	*	MEM_2OTHER

DDR3:  
DQ signals should be matched within 5 ps of associated DQS pair.  
DQS intra-pair matching should be within 1 ps, inter-pair matching should be within 360 ps  
No DQS to clock matching requirement.  
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.  
CMD/CTRL signals should be matched within 150 ps.  
All memory signals maximum length is 1.030 ps.

SOURCE: MCP89 Interface DG (DG-04625-001\_v0.9), Section 2.2.3  
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD


SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001\_v0.9), Section 2.2.2

MEM\_A/B\_CKE EC SET NAME IS CHANGED ON K6, CANNOT SYNC THIS PAGE FROM T27

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
MEM_A_CLK	MEM_70D	MEM_CLK	MEM A CLK P<5..0>	9 15 26 27 32
MEM_A_CLK	MEM_70D	MEM_CLK	MEM A CLK N<5..0>	9 15 26 27 32
MEM_A_CKE	MEM_50S	MEM_CTRL	MEM A CKE<3..0>	15 21 26 27 32
MEM_A_CNTRL	MEM_50S	MEM_CTRL	MEM A CS_L<3..0>	15 26 27 32
MEM_A_CNTRL	MEM_50S	MEM_CTRL	MEM A ODT<3..0>	15 26 27 32
MEM_A_CMD	MEM_50S	MEM_CMD	MEM A A<15..0>	9 15 26 27 32
MEM_A_CMD	MEM_50S	MEM_CMD	MEM A BA<2..0>	15 26 27 32
MEM_A_CMD	MEM_50S	MEM_CMD	MEM A RAS_L	15 26 27 32
MEM_A_CMD	MEM_50S	MEM_CMD	MEM A CAS_L	15 26 27 32
MEM_A_CMD	MEM_50S	MEM_CMD	MEM A WE_L	15 26 27 32
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM A DQ<7..0>	15 26
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM A DQ<15..8>	15 26
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM A DQ<23..16>	15 26
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM A DQ<31..24>	15 26
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM A DQ<39..32>	15 27
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM A DQ<47..40>	15 27
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM A DQ<55..48>	15 27
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM A DQ<63..56>	15 27
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM A DM<0>	15 26
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM A DM<1>	15 26
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM A DM<2>	15 26
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM A DM<3>	15 26
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM A DM<4>	15 27
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM A DM<5>	15 27
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM A DM<6>	15 27
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM A DM<7>	15 27
MEM_A_DQS0	MEM_70D	MEM_QS	MEM A DQS P<0>	15 26
MEM_A_DQS0	MEM_70D	MEM_QS	MEM A DQS N<0>	15 26
MEM_A_DQS1	MEM_70D	MEM_QS	MEM A DQS P<1>	15 26
MEM_A_DQS1	MEM_70D	MEM_QS	MEM A DQS N<1>	15 26
MEM_A_DQS2	MEM_70D	MEM_QS	MEM A DQS P<2>	15 26
MEM_A_DQS2	MEM_70D	MEM_QS	MEM A DQS N<2>	15 26
MEM_A_DQS3	MEM_70D	MEM_QS	MEM A DQS P<3>	15 26
MEM_A_DQS3	MEM_70D	MEM_QS	MEM A DQS N<3>	15 26
MEM_A_DQS4	MEM_70D	MEM_QS	MEM A DQS P<4>	15 27
MEM_A_DQS4	MEM_70D	MEM_QS	MEM A DQS N<4>	15 27
MEM_A_DQS5	MEM_70D	MEM_QS	MEM A DQS P<5>	15 27
MEM_A_DQS5	MEM_70D	MEM_QS	MEM A DQS N<5>	15 27
MEM_A_DQS6	MEM_70D	MEM_QS	MEM A DQS P<6>	15 27
MEM_A_DQS6	MEM_70D	MEM_QS	MEM A DQS N<6>	15 27
MEM_A_DQS7	MEM_70D	MEM_QS	MEM A DQS P<7>	15 27
MEM_A_DQS7	MEM_70D	MEM_QS	MEM A DQS N<7>	15 27
MEM_B_CLK	MEM_70D	MEM_CLK	MEM B CLK P<5..0>	9 15 28 29 32
MEM_B_CLK	MEM_70D	MEM_CLK	MEM B CLK N<5..0>	9 15 28 29 32
MEM_B_CKE	MEM_50S	MEM_CTRL	MEM B CKE<3..0>	15 21 28 29 32
MEM_B_CNTRL	MEM_50S	MEM_CTRL	MEM B CS_L<3..0>	15 28 29 32
MEM_B_CNTRL	MEM_50S	MEM_CTRL	MEM B ODT<3..0>	15 28 29 32
MEM_B_CMD	MEM_50S	MEM_CMD	MEM B A<15..0>	9 15 28 29 32
MEM_B_CMD	MEM_50S	MEM_CMD	MEM B BA<2..0>	15 28 29 32
MEM_B_CMD	MEM_50S	MEM_CMD	MEM B RAS_L	15 28 29 32
MEM_B_CMD	MEM_50S	MEM_CMD	MEM B CAS_L	15 28 29 32
MEM_B_CMD	MEM_50S	MEM_CMD	MEM B WE_L	15 28 29 32
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM B DQ<7..0>	15 28
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM B DQ<15..8>	15 28
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM B DQ<23..16>	15 28
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM B DQ<31..24>	15 28
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM B DQ<39..32>	15 29
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM B DQ<47..40>	15 29
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM B DQ<55..48>	15 29
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM B DQ<63..56>	15 29
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM B DM<0>	15 28
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM B DM<1>	15 28
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM B DM<2>	15 28
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM B DM<3>	15 28
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM B DM<4>	15 29
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM B DM<5>	15 29
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM B DM<6>	15 29
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM B DM<7>	15 29
MEM_B_DQS0	MEM_70D	MEM_QS	MEM B DQS P<0>	15 28
MEM_B_DQS0	MEM_70D	MEM_QS	MEM B DQS N<0>	15 28
MEM_B_DQS1	MEM_70D	MEM_QS	MEM B DQS P<1>	15 28
MEM_B_DQS1	MEM_70D	MEM_QS	MEM B DQS N<1>	15 28
MEM_B_DQS2	MEM_70D	MEM_QS	MEM B DQS P<2>	15 28
MEM_B_DQS2	MEM_70D	MEM_QS	MEM B DQS N<2>	15 28
MEM_B_DQS3	MEM_70D	MEM_QS	MEM B DQS P<3>	15 28
MEM_B_DQS3	MEM_70D	MEM_QS	MEM B DQS N<3>	15 28
MEM_B_DQS4	MEM_70D	MEM_QS	MEM B DQS P<4>	15 29
MEM_B_DQS4	MEM_70D	MEM_QS	MEM B DQS N<4>	15 29
MEM_B_DQS5	MEM_70D	MEM_QS	MEM B DQS P<5>	15 29
MEM_B_DQS5	MEM_70D	MEM_QS	MEM B DQS N<5>	15 29
MEM_B_DQS6	MEM_70D	MEM_QS	MEM B DQS P<6>	15 29
MEM_B_DQS6	MEM_70D	MEM_QS	MEM B DQS N<6>	15 29
MEM_B_DQS7	MEM_70D	MEM_QS	MEM B DQS P<7>	15 29
MEM_B_DQS7	MEM_70D	MEM_QS	MEM B DQS N<7>	15 29
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP VDD	15
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP GND	15

SYNC MASTER=K16 MLB		SYNC DATE=07/07/2010	
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Memory Constraints		DRAWING NUMBER	051-8379
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PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001\_v0.9), Section 2.3

NEED PCIe Gen1/Gen2 notes!

Analog Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CRT	*	20 MIL	?
CRT_2CRT	*	15 MIL	?
CRT_2CLK	*	50 MIL	?
CRT_2SWITCHER	*	250 MIL	?
CRT_SYNC	*	=4x_DIELECTRIC	?
MCP_DAC_COMP	*	=2x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT

CRT signal single-ended impedance varies by location:  
- 37.5-ohm from MCP to first termination resistor.  
- 50-ohm from first to second termination resistor.  
- 75-ohm from output of three-pole filter to connector (if possible).  
R/G/B signals should be matched as close as possible and < 10 inches.  
SOURCE: MCP89 Interface DG (DG-04625-001\_v0.9), Section 2.4.1.

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be matched within 100 mils.  
NOTE: NV DG recommends 90 ohm differential for LVDS, but cable/display assume 100 ohm.  
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 100 ps.  
DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.  
Max trace length: LVDS 10 inches, DP 8.5 inches.  
SOURCE: MCP89 Interface DG (DG-04625-001\_v0.9), Section 2.4.2

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF


SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=3x_DIELECTRIC	?
SATA_TERMPP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=4x_DIELECTRIC	?

SATA intra-pair matching should be 1 ps.  
Max trace length: 12 inches for SATA Gen1/Gen2, TBD for SATA Gen3.  
SOURCE: MCP89 Interface DG (DG-04625-001\_v0.9), Section 2.6

MCP89 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
	PCIE_90D	PCIE	PEG R2D P<15..0>
	PCIE_90D	PCIE	PEG R2D N<15..0>
PEG_R2D	PCIE_90D	PCIE	PEG R2D C P<15..0>
	PCIE_90D	PCIE	PEG R2D C N<15..0>
PEG_D2R	PCIE_90D	PCIE	PEG D2R P<15..0>
	PCIE_90D	PCIE	PEG D2R N<15..0>
	PCIE_90D	PCIE	PEG D2R C P<15..0>
	PCIE_90D	PCIE	PEG D2R C N<15..0>
	PCIE_90D	PCIE	PCIE AP R2D P
	PCIE_90D	PCIE	PCIE AP R2D N
PCIE_AP_R2D	PCIE_90D	PCIE	PCIE AP R2D C P
	PCIE_90D	PCIE	PCIE AP R2D C N
PCIE_AP_D2R	PCIE_90D	PCIE	PCIE AP D2R P
	PCIE_90D	PCIE	PCIE AP D2R N
	PCIE_90D	PCIE	PCIE ENET R2D P
	PCIE_90D	PCIE	PCIE ENET R2D N
PCIE_ENET_R2D	PCIE_90D	PCIE	PCIE ENET R2D C P
	PCIE_90D	PCIE	PCIE ENET R2D C N
PCIE_ENET_D2R	PCIE_90D	PCIE	PCIE ENET D2R P
	PCIE_90D	PCIE	PCIE ENET D2R N
	PCIE_90D	PCIE	PCIE ENET D2R C P
	PCIE_90D	PCIE	PCIE ENET D2R C N
	PCIE_90D	PCIE	PCIE FW R2D P
	PCIE_90D	PCIE	PCIE FW R2D N
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE FW R2D C P
	PCIE_90D	PCIE	PCIE FW R2D C N
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE FW D2R P
	PCIE_90D	PCIE	PCIE FW D2R N
	PCIE_90D	PCIE	PCIE FW D2R C P
	PCIE_90D	PCIE	PCIE FW D2R C N
MCP_PE0_BECLK	CLK_PCIE_100D	CLK_PCIE	PEG CLK100M P
	CLK_PCIE_100D	CLK_PCIE	PEG CLK100M N
MCP_PE1_BECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M AP P
	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M AP N
MCP_PE2_BECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M ENET P
	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M ENET N
MCP_PE3_BECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M FW P
	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M FW N
MCP_PEX_CLK_COMP		MCP_PEX_COMP	MCP_PEX0_TERMPP
CRT_RED	CRT_50S	CRT	CRT IG R C PR
CRT_GREEN	CRT_50S	CRT	CRT IG G Y Y
CRT_BLUE	CRT_50S	CRT	CRT IG B COMP PB
CRT_SYNC	CRT_50S	CRT_SYNC	CRT IG HSYNC
CRT_SYNC	CRT_50S	CRT_SYNC	CRT IG VSYNC
MCP_DAC_RSET		MCP_DAC_COMP	MCP_TV_DAC_RSET
MCP_DAC_VREF		MCP_DAC_COMP	MCP_TV_DAC_VREF
DP_INT_ML	DP_90D	DISPLAYPORT	DP IG ML1 P<1..0>
DP_INT_ML	DP_90D	DISPLAYPORT	DP IG ML1 N<1..0>
DP_INT_AUX_CH	DP_90D	DISPLAYPORT	DP IG AUX CH1 P
DP_INT_AUX_CH	DP_90D	DISPLAYPORT	DP IG AUX CH1 N
DP_EXT_ML	DP_90D	DISPLAYPORT	DP IG ML0 P<3..0>
DP_EXT_ML	DP_90D	DISPLAYPORT	DP IG ML0 N<3..0>
DP_EXT_AUX_CH	DP_90D	DISPLAYPORT	DP IG AUX CH0 P
DP_EXT_AUX_CH	DP_90D	DISPLAYPORT	DP IG AUX CH0 N
MCP_TMDS0_RSET	MCP_DV_COMP		MCP_TMDS0_RSET
MCP_TMDS0_VPROBE			MCP_TMDS0_VPROBE
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS IG A CLK P
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS IG A CLK N
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS IG A DATA P<2..0>
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS IG A DATA N<2..0>
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS IG A DATA P<3>
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS IG A DATA N<3>
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS IG B CLK P
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS IG B CLK N
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS IG B DATA P<2..0>
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS IG B DATA N<2..0>
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS IG B DATA P<3>
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS IG B DATA N<3>
MCP_IFPAB_RSET	MCP_DV_COMP		MCP_IFPAB_RSET
MCP_IFPAB_VPROBE			MCP_IFPAB_VPROBE
SATA_HDD_R2D	SATA_90D	SATA	SATA HDD R2D C P
	SATA_90D	SATA	SATA HDD R2D C N
	SATA_90D	SATA	SATA HDD R2D P
	SATA_90D	SATA	SATA HDD R2D N
SATA_HDD_D2R	SATA_90D	SATA	SATA HDD D2R P
	SATA_90D	SATA	SATA HDD D2R N
	SATA_90D	SATA	SATA HDD D2R C P
	SATA_90D	SATA	SATA HDD D2R C N
SATA_ODD_R2D	SATA_90D	SATA	SATA ODD R2D C P
	SATA_90D	SATA	SATA ODD R2D C N
	SATA_90D	SATA	SATA ODD R2D P
	SATA_90D	SATA	SATA ODD R2D N
SATA_ODD_D2R	SATA_90D	SATA	SATA ODD D2R P
	SATA_90D	SATA	SATA ODD D2R N
	SATA_90D	SATA	SATA ODD D2R C P
	SATA_90D	SATA	SATA ODD D2R C N
MCP_SATA_TERMPP		SATA_TERMPP	MCP_SATA_TERMPP

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MCP Constraints 1			
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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=1.5x_DIELECTRIC	?
CLK_LPC	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001\_v0.9), Section 2.7

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?	USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001\_v0.9), Section 2.8

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001\_v0.9), Section 2.9

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP89 Interface DG (DG-04625-001\_v0.9), Section 2.10

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=1.5x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001\_v0.9), Section 2.11

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=1.5x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001\_v0.9), Section 2.12

MCP89 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
LPC_AD	LPC_55S	LPC	LPC AD<3..0>	7 19 38 40
LPC_FRAME_L	LPC_55S	LPC	LPC FRAME L	7 19 38 40
LPC_RESET_L	LPC_55S	LPC	LPC RESET L	19 25
MCP_LPC_CLK0	CLK_LPC_55S	CLK_LPC	LPC CLK33M SMC R	19 25
	CLK_LPC_55S	CLK_LPC	LPC CLK33M SMC	25 38
	CLK_LPC_55S	CLK_LPC	LPC CLK33M LPCPLUS	7 25 40
USB_EXT_A	USB_90D	USB	USB EXT_A P	18 36
	USB_90D	USB	USB EXT_A N	18 36
	USB_90D	USB	USB EXT_A MUXED P	36 71
	USB_90D	USB	USB EXT_A MUXED N	36 71
USB_MINI	USB_90D	USB	USB MINI P	9 18
	USB_90D	USB	USB MINI N	9 18
USB_EXTD	USB_90D	USB	USB EXT_D P	7 18 37
	USB_90D	USB	USB EXT_D N	7 18 37
USB_CAMERA	USB_90D	USB	USB CAMERA P	7 18 37
	USB_90D	USB	USB CAMERA N	7 18 37
USB_BT	USB_90D	USB	USB BT P	7 18 34
	USB_90D	USB	USB BT N	7 18 34
USB_TPAD	USB_90D	USB	USB TPAD P	18 46 71
	USB_90D	USB	USB TPAD N	18 46 71
USB_IR	USB_90D	USB	USB IR P	
	USB_90D	USB	USB IR N	
USB_EXTR	USB_90D	USB	USB EXTB P	
	USB_90D	USB	USB EXTB N	
USB_T57	USB_90D	USB	USB T57 P	
	USB_90D	USB	USB T57 N	
USB_EXTC	USB_90D	USB	USB EXTC P	9 18
	USB_90D	USB	USB EXTC N	9 18
USB_SDCARD	USB_90D	USB	USB SDCARD P	9 18
	USB_90D	USB	USB SDCARD N	9 18
USB_WM	USB_90D	USB	USB WM P	
	USB_90D	USB	USB WM N	
MCP_USB_RBIAS	MCP_USB_RBIAS		MCP USB RBIAS GND	18
SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS MCP_0 CLK	19 41
SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS MCP_0 DATA	19 41
(SMBUS_SMC_MGMT_SCL)	SMB_55S	SMB	SMBUS MCP_1 CLK	19 41
(SMBUS_SMC_MGMT_SDA)	SMB_55S	SMB	SMBUS MCP_1 DATA	19 41
HDA_BIT_CLK	HDA_55S	HDA	HDA BIT_CLK	7 19 37
	HDA_55S	HDA	HDA BIT_CLK R	19
HDA_SYNC	HDA_55S	HDA	HDA SYNC	7 19 37
	HDA_55S	HDA	HDA SYNC R	19
HDA_RST_L	HDA_55S	HDA	HDA RST_R L	19
	HDA_55S	HDA	HDA RST_L	7 19 37
HDA_SDIN0	HDA_55S	HDA	HDA SDIN0	7 19 37
	HDA_55S	HDA	HDA SDIN CODEC	
HDA_SDOUT	HDA_55S	HDA	HDA SDOUT	7 19 37
	HDA_55S	HDA	HDA SDOUT R	19
MCP_HDA_PULLDN_COMP		MCP_HDA_COMP	MCP HDA PULLDN COMP	19
MCP_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM CLK32K SUSCLK R	19 25
	CLK_SLOW_55S	CLK_SLOW	PM CLK32K SUSCLK	25 38
SPI_CLK	SPI_55S	SPI	SPI CLK R	19 40
	SPI_55S	SPI	SPI CLK	40
SPI_MOSI	SPI_55S	SPI	SPI MOSI R	19 40
	SPI_55S	SPI	SPI MOSI	40
SPI_MISO	SPI_55S	SPI	SPI MISO	19 40
SPI_CS0	SPI_55S	SPI	SPI CS0 R L	19 40
	SPI_55S	SPI	SPI CS0 L	40
	SPI_55S	SPI	SPI MLB_CLK	40 47
	SPI_55S	SPI	SPI MLB_MOSI	40 47
	SPI_55S	SPI	SPI MLB_MISO	40 47
	SPI_55S	SPI	SPI MLB_CS_L	40 47
	SPI_55S	SPI	SPI_ALT_CLK	7 40
	SPI_55S	SPI	SPI_ALT_MOSI	7 40
	SPI_55S	SPI	SPI_ALT_MISO	7 40
	SPI_55S	SPI	SPI_ALT_CS_L	7 40

MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001\_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?




















SOURCE: MCP73 Interface DG (DG-02974-001\_v01), Section 2.7.4

SD Card Interface Constraints



PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD_INTERFACE	*	=3X_DIELECTRIC	?













RGMII Net Properties

NET TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
 MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_VDD 18
 MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_GND 18
 MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0_R
 MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	RTL8211_CLK25M_CKXTAL1
 ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET_INTR_L
 ENET_MDIO	ENET_MII_55S	ENET_MII	ENET_MDIO 9 18
 ENET_MDC	ENET_MII_55S	ENET_MII	ENET_MDC
 ENET_PWRDWN_L	ENET_MII_55S	ENET_MII	ENET_PWRDWN_L
 ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R
 ENET_MII_55S	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK 9 18
 ENET_MII_55S	ENET_MII_55S	ENET_MII	ENET_RXD_R<3..0>
 ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<0> 9 18
 ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<3..1> 9 18
 ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RX_CTRL 9 18
 ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK
 ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<0>
 ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<3..1>
 ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TX_CTRL
 ENET_TXD	ENET_MII_55S	ENET_MII	ENET_RESET_L

Ethernet Net Properties

NET TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
 ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_P<3..0>
 ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_N<3..0>











SD Card Net Properties

NET TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
 SD_DATA	SD_55S	SD_INTERFACE	SD_D<4..0>
 SD_DATA	SD_55S	SD_INTERFACE	SDCONN_DATA<4..0>
 SD_DATA	SD_55S	SD_INTERFACE	BCM57765_CR_DATA<4>
 SD_DATA_R	SD_55S	SD_INTERFACE	SD_D<7..5>
 SD_DATA_R	SD_55S	SD_INTERFACE	SDCONN_DATA<7..5>
 SD_DATA_R	SD_55S	SD_INTERFACE	BCM57765_CR_DATA<7..5>
 SD_CLK	SD_55S	SD_INTERFACE	SD_CLK
 SD_CLK	SD_55S	SD_INTERFACE	SD_CLK_R
 SD_CLK	SD_55S	SD_INTERFACE	SDCONN_CLK
 SD_CMD	SD_55S	SD_INTERFACE	SD_CMD
 SD_CMD	SD_55S	SD_INTERFACE	SDCONN_CMD
 SD_CMD	SD_55S	SD_INTERFACE	BCM57765_CR_CMD









NOTE: SD\_D<7..5> are different to support BCM5764M/BCM57765 co-layout.

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
1To1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
 SMBUS_SMC_A_S3_SCL	SMB_55G	SMB	SMBUS_SMC_A_S3_SCL 41
 SMBUS_SMC_A_S3_SDA	SMB_55G	SMB	SMBUS_SMC_A_S3_SDA 41
 SMBUS_SMC_B_S0_SCL	SMB_55G	SMB	SMBUS_SMC_B_S0_SCL 41
 SMBUS_SMC_B_S0_SDA	SMB_55G	SMB	SMBUS_SMC_B_S0_SDA 41
 SMBUS_SMC_0_S0_SCL	SMB_55G	SMB	SMBUS_SMC_0_S0_SCL 41
 SMBUS_SMC_0_S0_SDA	SMB_55G	SMB	SMBUS_SMC_0_S0_SDA 41
 SMBUS_SMC_BSA_SCL	SMB_55G	SMB	SMBUS_SMC_BSA_SCL 7 41
 SMBUS_SMC_BSA_SDA	SMB_55G	SMB	SMBUS_SMC_BSA_SDA 7 41
 SMBUS_SMC_MGMT_SCL	SMB_55G	SMB	SMBUS_SMC_MGMT_SCL 41
 SMBUS_SMC_MGMT_SDA	SMB_55G	SMB	SMBUS_SMC_MGMT_SDA 41

SMBus Charger Net Properties


NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
 CHGR_CSI_P	1To1_DIFFPAIR		CHGR_CSI_P 50
 CHGR_CSI_N	1To1_DIFFPAIR		CHGR_CSI_N 50
 CHGR_CSI_R_P	1To1_DIFFPAIR		CHGR_CSI_R_P 50
 CHGR_CSI_R_N	1To1_DIFFPAIR		CHGR_CSI_R_N 50
 CHGR_CSO_P	1To1_DIFFPAIR		CHGR_CSO_P 50
 CHGR_CSO_N	1To1_DIFFPAIR		CHGR_CSO_N 50
 CHGR_CSO_R_P	1To1_DIFFPAIR		CHGR_CSO_R_P 43 50
 CHGR_CSO_R_N	1To1_DIFFPAIR		CHGR_CSO_R_N 43 50

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SMC Constraints

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1T01_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1T01_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=1:1_SPACING	?
THERM	*	=1:1_SPACING	?
AUDIO	*	=1:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
MEM_POWER	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_POWER	*	PWR_P2MM
MEM_CMD	MEM_POWER	*	PWR_P2MM
MEM_CTRL	MEM_POWER	*	PWR_P2MM
MEM_DATA	MEM_POWER	*	PWR_P2MM
MEM_DQS	MEM_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

## SD CARD READER LAYOUT RELAXATIONS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_55S_OVERRIDE	*	OVERRIDE	=STANDARD_OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

## MCP Fanout Constraint Relaxations

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S_OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM_OVERRIDE	5.8 MM_OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP_OVERRIDE	TOP_OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM_OVERRIDE	500 MIL_OVERRIDE	OVERRIDE	OVERRIDE
MCP_MEM_COMP_OVERRIDE	TOP_OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM_OVERRIDE	500 MIL_OVERRIDE	OVERRIDE	OVERRIDE
MCP_MII_COMP_OVERRIDE	TOP_OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM_OVERRIDE	500 MIL_OVERRIDE	OVERRIDE	OVERRIDE
MCP_USB_RBIAIS_OVERRIDE	TOP_OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM_OVERRIDE	500 MIL_OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP_OVERRIDE	*	OVERRIDE	OVERRIDE	0.25 MM_OVERRIDE	250 MIL_OVERRIDE	OVERRIDE	OVERRIDE

## Misc Net Properties

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
(USB_EXT_A)	USB_90D	USB	USB EXT_A MUXED P 36 68
(USB_EXT_A)	USB_90D	USB	USB EXT_A MUXED N 36 68
(USB_EXT_A)	USB_90D	USB	USB LT1 P 36
(USB_EXT_A)	USB_90D	USB	USB LT1 N 36
(USB_TPAD)	USB_90D	USB	USB TPAD P 18 46 68
(USB_TPAD)	USB_90D	USB	USB TPAD N 18 46 68
(USB_TPAD)	USB_90D	USB	USB TPAD CONN P 7 46
(USB_TPAD)	USB_90D	USB	USB TPAD CONN N 7 46
SMBUS_SMC_MNMT_SDA	SMB_55S	SMB	I2C SMC SMS_SDA_R 41
SMBUS_SMC_MNMT_SCL	SMB_55S	SMB	I2C SMC SMS_SCL_R 41
	SMB_55S	SMB	I2C TCON_SCL 41
	SMB_55S	SMB	I2C TCON_SDA 41
	SMB_55S	SMB	I2C TCON_SCL_CONN
	SMB_55S	SMB	I2C TCON_SDA_CONN

## Graphics Net Properties


NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
	DP_90D	DISPLAYPORT	DP INT ML P<1..0> 9 59
	DP_90D	DISPLAYPORT	DP INT ML N<1..0> 9 59
	DP_90D	DISPLAYPORT	DP INT ML C P<1..0> 59
	DP_90D	DISPLAYPORT	DP INT ML C N<1..0> 59
	DP_90D	DISPLAYPORT	DP INT ML F P<1..0> 7 59
	DP_90D	DISPLAYPORT	DP INT ML F N<1..0> 7 59
	DP_90D	DISPLAYPORT	DP INT AUX CH C P 7 59
	DP_90D	DISPLAYPORT	DP INT AUX CH C N 7 59
	DP_90D	DISPLAYPORT	DP INT AUX CH P 9 59
	DP_90D	DISPLAYPORT	DP INT AUX CH N 9 59
(DP_EXT_ML)	DP_90D	DISPLAYPORT	DP EXT ML P<3..0> 9 61
	DP_90D	DISPLAYPORT	DP EXT ML N<3..0> 9 61
	DP_90D	DISPLAYPORT	DP EXT ML C P<3..0> 61
	DP_90D	DISPLAYPORT	DP EXT ML C N<3..0> 61
	DP_90D	DISPLAYPORT	DP EXT ML F P<3..0> 61
	DP_90D	DISPLAYPORT	DP EXT ML F N<3..0> 61
(DP_EXT_AUX_CH)	DP_90D	DISPLAYPORT	DP EXT AUX CH C P 9 61
	DP_90D	DISPLAYPORT	DP EXT AUX CH C N 9 61

## Power Net Properties

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
CPUTHMSNS_D2	THERM_1T01_55S	THERM	DRAMTHMSNS_D2_P 44
	THERM_1T01_55S	THERM	DRAMTHMSNS_D2_N 44
CPU_THERMD	THERM_1T01_55S	THERM	CPU_THERMD_P 10 44
	THERM_1T01_55S	THERM	CPU_THERMD_N 10 44
MCPTHMSNS_D2	THERM_1T01_55S	THERM	MLBR_THMDIODE_P 44
	THERM_1T01_55S	THERM	MLBR_THMDIODE_N 44
MCP_THMDIODE	THERM_1T01_55S	THERM	MCP_THMDIODE_P 19 44
	THERM_1T01_55S	THERM	MCP_THMDIODE_N 19 44
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS_1V5_S3_P 42 52
	SENSE_1T01_55S	SENSE	ISNS_1V5_S3_N 42 52
SENSE_DIFFPATR	SENSE_1T01_55S	SENSE	ISNS_AIRPORT_P 34 42
	SENSE_1T01_55S	SENSE	ISNS_AIRPORT_N 34 42
SENSE_DIFFPATR	SENSE_1T01_55S	SENSE	ISNS_CSREG_P 43
	SENSE_1T01_55S	SENSE	ISNS_CSREG_N 43
SENSE_DIFFPATR	SENSE_1T01_55S	SENSE	ISNS_HDD_P 35 42
	SENSE_1T01_55S	SENSE	ISNS_HDD_N 35 42
SENSE_DIFFPATR	SENSE_1T01_55S	SENSE	ISNS_LCDBKLT_P 42 62
	SENSE_1T01_55S	SENSE	ISNS_LCDBKLT_N 42 62
SENSE_DIFFPATR	SENSE_1T01_55S	SENSE	CPUVTTS0_CS_P 55
	SENSE_1T01_55S	SENSE	CPUVTTS0_CS_N 55
SENSE_DIFFPATR	SENSE_1T01_55S	SENSE	IMVP6_CS_P 53
	SENSE_1T01_55S	SENSE	IMVP6_CS_N 53
SENSE_DIFFPATR	SENSE_1T01_55S	SENSE	IMVP6_CS_R_P 53
	SENSE_1T01_55S	SENSE	IMVP6_CS_R_N 53
SENSE_DIFFPATR	SENSE_1T01_55S	SENSE	CPU_VTTSSENSE_P 55
	SENSE_1T01_55S	SENSE	CPU_VTTSSENSE_N 55
SENSE_DIFFPATR	SENSE_1T01_55S	SENSE	MCPCORES0_VSEN_P 22 54
	SENSE_1T01_55S	SENSE	MCPCORES0_VSEN_N 22 54
		MEM_POWER	PP1V5R1V35_S3 7 8
		SB_POWER	PP3V3_S5 7 8 57
		SB_POWER	PP3V3_S0 7 8 57
		SB_POWER	PP1V5_S0 7 8 57
		GND	GND

## Audio Net Properties

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
SPKRAMP_INR	DIFFPAIR	AUDIO	SPKRAMP_INR_P 7 37 48
	DIFFPAIR	AUDIO	SPKRAMP_INR_N 7 37 48
MAX98300_R	DIFFPAIR	AUDIO	MAX98300_R_P 48
	DIFFPAIR	AUDIO	MAX98300_R_N 48

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K99 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS				BOARD AREAS		BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM				NO_TYPE,BGA		MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	0.100 MM	0.076 MM	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
27P4_OHM_SE	ISL3,ISL10	Y	0.250 MM	0.250 MM			
27P4_OHM_SE	ISL4,ISL9	Y	0.250 MM	0.250 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
40_OHM_SE	TOP,BOTTOM	Y	0.170 MM	0.170 MM			
40_OHM_SE	ISL3,ISL4,ISL9,ISL10	Y	0.140 MM	0.140 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.110 MM			
50_OHM_SE	ISL3,ISL4,ISL9,ISL10	Y	0.090 MM	0.090 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	ISL3,ISL4,ISL9,ISL10	Y	0.076 MM	0.076 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	TOP,BOTTOM	Y	0.175 MM	0.175 MM		0.130 MM	0.130 MM
70_OHM_DIFF	ISL3,ISL10	Y	0.135 MM	0.135 MM		0.130 MM	0.130 MM
70_OHM_DIFF	ISL4,ISL9	Y	0.155 MM	0.155 MM		0.130 MM	0.130 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.140 MM		0.160 MM	0.160 MM
80_OHM_DIFF	ISL3,ISL10	Y	0.109 MM	0.109 MM		0.160 MM	0.160 MM
80_OHM_DIFF	ISL4,ISL9	Y	0.125 MM	0.125 MM		0.160 MM	0.160 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
75_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
75_OHM_DIFF	TOP,BOTTOM	Y	0.160 MM	0.160 MM		0.160 MM	0.160 MM
75_OHM_DIFF	ISL3,ISL10	Y	0.120 MM	0.120 MM		0.140 MM	0.140 MM
75_OHM_DIFF	ISL4,ISL9	Y	0.140 MM	0.140 MM		0.140 MM	0.140 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.115 MM		0.210 MM	0.210 MM
90_OHM_DIFF	ISL3,ISL10	Y	0.089 MM	0.089 MM		0.210 MM	0.210 MM
90_OHM_DIFF	ISL4,ISL9	Y	0.105 MM	0.105 MM		0.210 MM	0.210 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
95_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
95_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.115 MM		0.210 MM	0.210 MM
95_OHM_DIFF	ISL3,ISL10	Y	0.089 MM	0.089 MM		0.210 MM	0.210 MM
95_OHM_DIFF	ISL4,ISL9	Y	0.105 MM	0.105 MM		0.210 MM	0.210 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.091 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL3,ISL10	Y	0.075 MM	0.075 MM		0.300 MM	0.300 MM
100_OHM_DIFF	ISL4,ISL9	Y	0.085 MM	0.085 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
BGA_P3MM	*	0.3 MM	?


SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.28:1_SPACING	*	0.228 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PPIV5_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.2 MM	1000
PWR_P2MM	*	0.2 MM	1000

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
NB_STATIC	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
1.5X_DIELECTRIC	*	0.105 MM	?
5X_DIELECTRIC	*	0.350 MM	?

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1UF 0402 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

MURATA

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0629	2	CAP, 1UF, 6.3V, 10%, 0402	CT003,CT060	CRITICAL	SS_CAP_1UF	138S0628	2	CAP, 1UF, 6.3V, 10%, 0402	CT003,CT060	CRITICAL	MU_CAP_1UF	138S0630	2	CAP, 1UF, 6.3V, 10%, 0402	CT003,CT060	CRITICAL	TY_CAP_1UF

2.2UF 0402 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

MURATA

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1240,C1242,C1243,C1244,C1246,C1246,C1247,C1247	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1241,C1242,C1243,C1244,C1246,C1246,C1247,C1247	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1241,C1242,C1243,C1244,C1246,C1246,C1247,C1247	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1261,C1262,C1263,C1264,C1266,C1266,C1267,C1267	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1261,C1262,C1263,C1264,C1266,C1266,C1267,C1267	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1261,C1262,C1263,C1264,C1266,C1266,C1267,C1267	CRITICAL	TY_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1269,C1269,C1269,C1269,C1269,C1269,C1269,C1269	CRITICAL	SS_CAP_2_2UF	138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1269,C1269,C1269,C1269,C1269,C1269,C1269,C1269	CRITICAL	MU_CAP_2_2UF	138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1269,C1269,C1269,C1269,C1269,C1269,C1269,C1269	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C0901,C0902,C0903,C0904,C0905,C0906,C0907,C0907	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C0901,C0902,C0903,C0904,C0905,C0906,C0907,C0907	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C0901,C0902,C0903,C0904,C0905,C0906,C0907,C0907	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C0911,C0912,C0913,C0914,C0915,C0916,C0917,C0917	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C0911,C0912,C0913,C0914,C0915,C0916,C0917,C0917	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C0911,C0912,C0913,C0914,C0915,C0916,C0917,C0917	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C0921,C0922,C0923,C0924,C0925,C0926,C0927,C0927	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C0921,C0922,C0923,C0924,C0925,C0926,C0927,C0927	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C0921,C0922,C0923,C0924,C0925,C0926,C0927,C0927	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C0931,C0932,C0933,C0934,C0935,C0936,C0937,C0937	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C0931,C0932,C0933,C0934,C0935,C0936,C0937,C0937	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C0931,C0932,C0933,C0934,C0935,C0936,C0937,C0937	CRITICAL	TY_CAP_2_2UF
138S0632	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1285,C1286,C1287,C1288,C1291,C1292,C1293,C1293	CRITICAL	SS_CAP_2_2UF	138S0633	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1285,C1286,C1287,C1288,C1291,C1292,C1293,C1293	CRITICAL	MU_CAP_2_2UF	138S0634	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1285,C1286,C1287,C1288,C1291,C1292,C1293,C1293	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1001,C1004,C1005,C1010,C1011,C1012,C1014,C1014	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1001,C1004,C1005,C1010,C1011,C1012,C1014,C1014	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1001,C1004,C1005,C1010,C1011,C1012,C1014,C1014	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1021,C1024,C1025,C1030,C1031,C1034,C1035,C1035	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1021,C1024,C1025,C1030,C1031,C1034,C1035,C1035	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1021,C1024,C1025,C1030,C1031,C1034,C1035,C1035	CRITICAL	TY_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1041,C1044,C1045,C1046,C1050,C1051,C1054,C1054	CRITICAL	SS_CAP_2_2UF	138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1041,C1044,C1045,C1046,C1050,C1051,C1054,C1054	CRITICAL	MU_CAP_2_2UF	138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1041,C1044,C1045,C1046,C1050,C1051,C1054,C1054	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1001,C1004,C1005,C1010,C1011,C1012,C1014,C1014	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1001,C1004,C1005,C1010,C1011,C1012,C1014,C1014	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1001,C1004,C1005,C1010,C1011,C1012,C1014,C1014	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1021,C1024,C1025,C1030,C1031,C1034,C1035,C1035	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1021,C1024,C1025,C1030,C1031,C1034,C1035,C1035	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1021,C1024,C1025,C1030,C1031,C1034,C1035,C1035	CRITICAL	TY_CAP_2_2UF
138S0632	9	CAP, 2.2UF, 6.3V, 20%, 0402	C1041,C1044,C1045,C1046,C1050,C1051,C1054,C1054	CRITICAL	SS_CAP_2_2UF	138S0633	9	CAP, 2.2UF, 6.3V, 20%, 0402	C1041,C1044,C1045,C1046,C1050,C1051,C1054,C1054	CRITICAL	MU_CAP_2_2UF	138S0634	9	CAP, 2.2UF, 6.3V, 20%, 0402	C1041,C1044,C1045,C1046,C1050,C1051,C1054,C1054	CRITICAL	TY_CAP_2_2UF

10UF 0603 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

MURATA

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0626	1	CAP, 10UF, 6.3V, 20%, 0603	C1280	CRITICAL	SS_CAP_10UF	138S0625	1	CAP, 10UF, 6.3V, 20%, 0603	C1280	CRITICAL	MU_CAP_10UF	138S0627	1	CAP, 10UF, 6.3V, 20%, 0603	C1280	CRITICAL	TY_CAP_10UF
138S0626	8	CAP, 10UF, 6.3V, 20%, 0603	C0605,C0609,C0620,C7209,C7209,C7245,C7355,C7355	CRITICAL	SS_CAP_10UF	138S0625	8	CAP, 10UF, 6.3V, 20%, 0603	C0605,C0609,C0620,C7209,C7209,C7245,C7355,C7355	CRITICAL	MU_CAP_10UF	138S0627	8	CAP, 10UF, 6.3V, 20%, 0603	C0605,C0609,C0620,C7209,C7209,C7245,C7355,C7355	CRITICAL	TY_CAP_10UF
138S0626	8	CAP, 10UF, 6.3V, 20%, 0603	C0611,C0646,C0650,C0620,C0660,C0667,C0660,C0660	CRITICAL	SS_CAP_10UF	138S0625	8	CAP, 10UF, 6.3V, 20%, 0603	C0611,C0646,C0650,C0620,C0660,C0667,C0660,C0660	CRITICAL	MU_CAP_10UF	138S0627	8	CAP, 10UF, 6.3V, 20%, 0603	C0611,C0646,C0650,C0620,C0660,C0667,C0660,C0660	CRITICAL	TY_CAP_10UF

22UF 0603 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

MURATA


TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0635	4	CAP, 22UF, 6.3V, 20%, 0603	C1210,C1214,C1217,C1218	CRITICAL	SS_CAP_22UF	138S0676	4	CAP, 22UF, 6.3V, 20%, 0603	C1210,C1214,C1217,C1218	CRITICAL	MU_CAP_22UF	138S0688	4	CAP, 22UF, 6.3V, 20%, 0603	C1210,C1214,C1217,C1218	CRITICAL	TY_CAP_22UF
138S0635	3	CAP, 22UF, 6.3V, 20%, 0603	C1223,C1226,C1227	CRITICAL	SS_CAP_22UF	138S0676	3	CAP, 22UF, 6.3V, 20%, 0603	C1223,C1226,C1227	CRITICAL	MU_CAP_22UF	138S0688	3	CAP, 22UF, 6.3V, 20%, 0603	C1223,C1226,C1227	CRITICAL	TY_CAP_22UF
138S0635	5	CAP, 22UF, 6.3V, 20%, 0603	C1230,C4002,C7360,C7361,C9480	CRITICAL	SS_CAP_22UF	138S0676	5	CAP, 22UF, 6.3V, 20%, 0603	C1230,C4002,C7360,C7361,C9480	CRITICAL	MU_CAP_22UF	138S0688	5	CAP, 22UF, 6.3V, 20%, 0603	C1230,C4002,C7360,C7361,C9480	CRITICAL	TY_CAP_22UF

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