

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
			2012-02-23

SCHEM,MLB,J13

2/23/12


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27	29	DDR3 DRAM CHANNEL A (0-31)	K21_MLB	07/28/2011
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31	33	FSB/DDR3/FRAMEBUF Vref Margining	J11_MLB	08/04/2011
32	34	DDR3 Bypassing/Termination	K21_MLB	07/28/2011
33	35	SecureDigital Card Reader	J13_MLB_NON_POR	11/10/2011
34	36	Thunderbolt Host (1 of 2)	J11_MLB	09/30/2011
35	37	Thunderbolt Host (2 of 2)	J11_MLB	10/04/2011
36	38	TBT Power Support	J13_MLB_NON_POR	11/10/2011
37	40	X21 WIRELESS CONNECTOR	J11_MLB	10/11/2011
38	45	SSD CONNECTOR	J13_MLB_NON_POR	10/17/2011
39	46	External A USB3 Connector	J11_MLB	09/30/2011
40	47	Left I/O (LIO) Connector	J13_MLB_NON_POR	11/10/2011
41	49	SMC	J13_MLB_NON_POR	10/17/2011
42	50	SMC Support	J13_MLB_NON_POR	11/10/2011
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44	52	SMBus Connections	J11_MLB	10/04/2011
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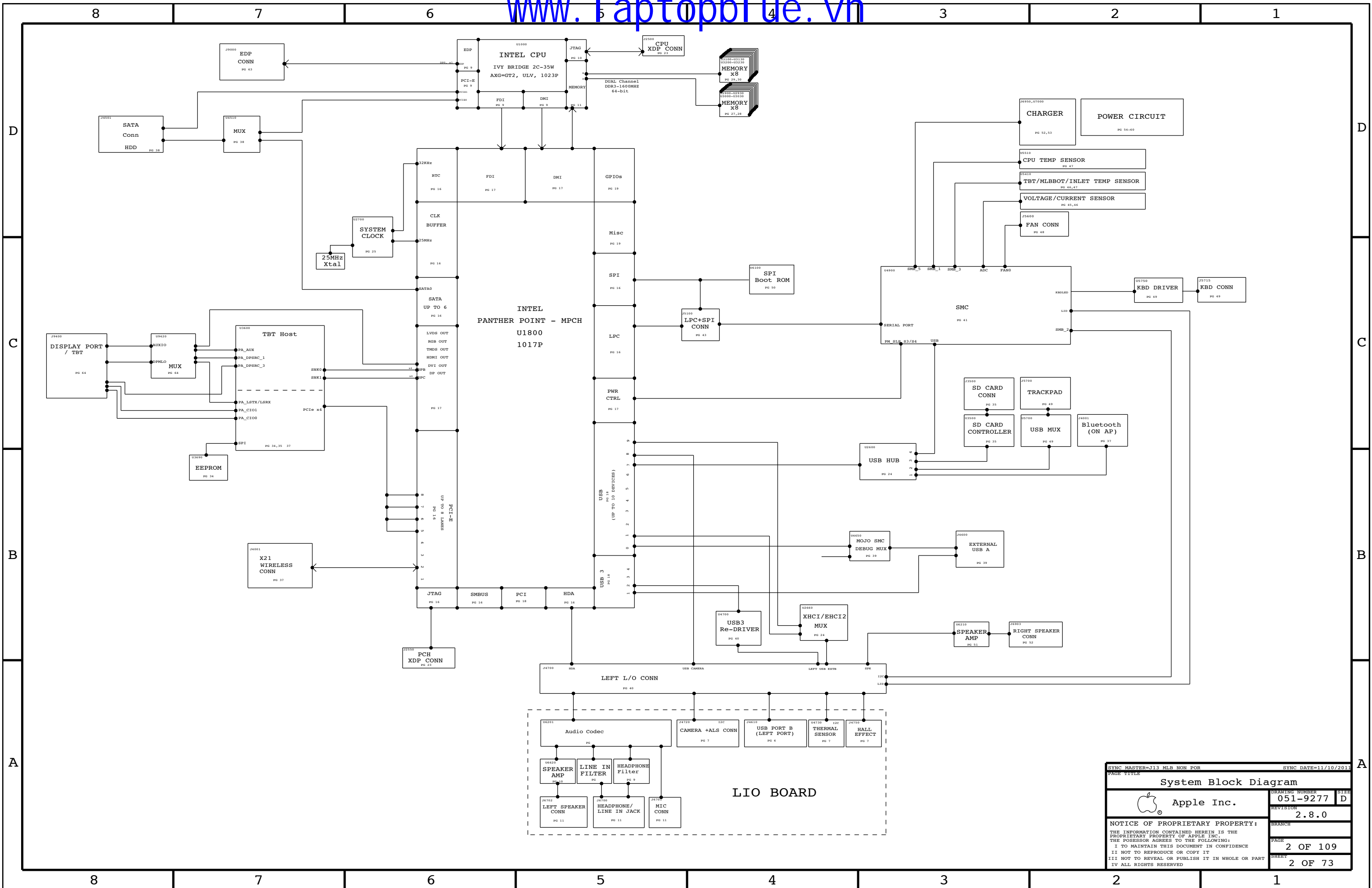
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Schematic / PCB #'s

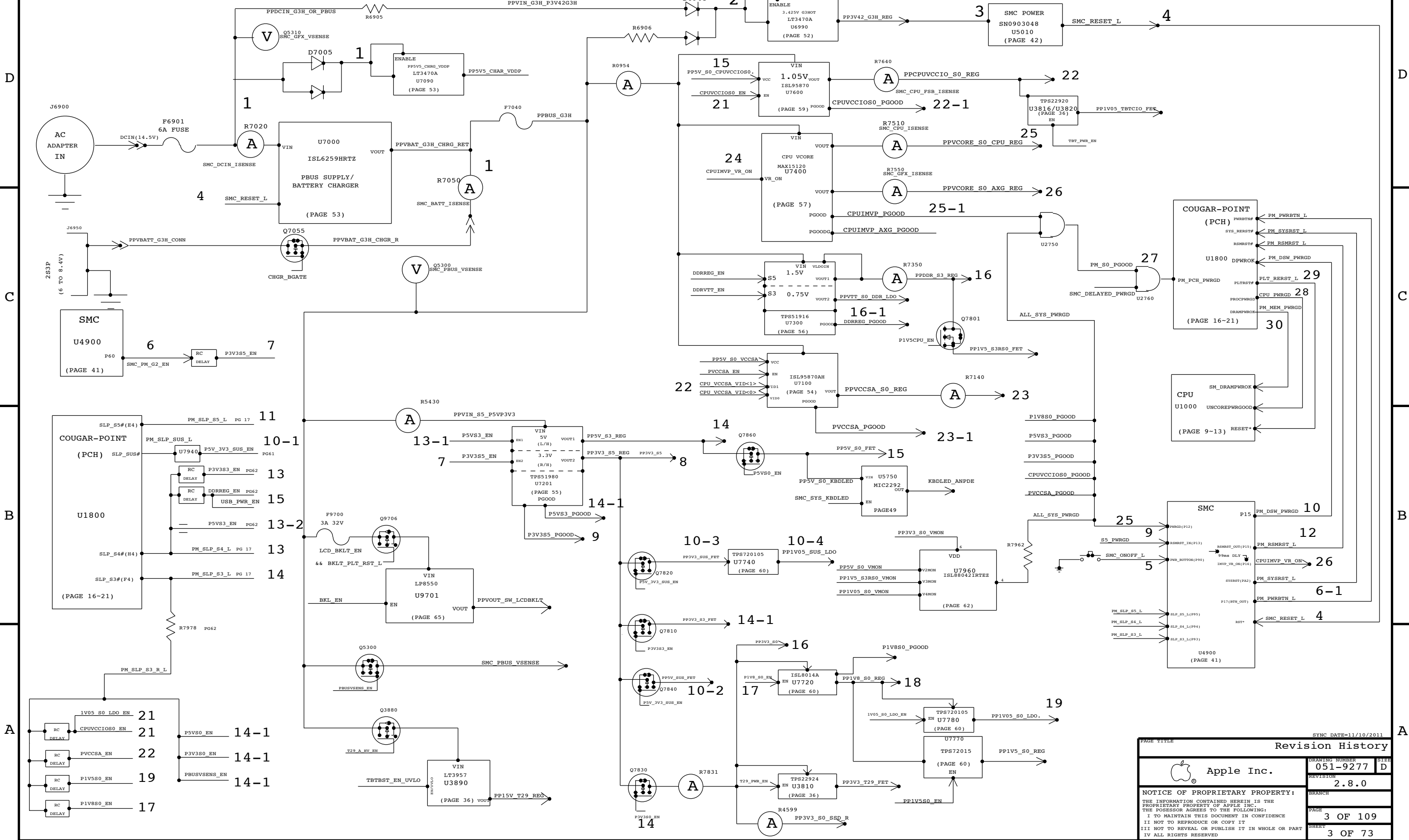
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820-3209	1	PCBF,MLB,J13	PCB	CRITICAL	


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LAST_MODIFIED=Thu Feb 23 17:52:06 2012

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SCHEM,MLB,J13			
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J13 POWER SYSTEM ARCHITECTURE



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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
085-3939	J13 MLB DEVELOPMENT BOM	J13_DEVEL_BOM
607-9090	CMN PTS,PCBA,MLB,J13	J13_CMNPTS
639-3552	PCBA,MLB,1.7GHZ,SA 4GB,J13	J13_CMNPTS,EEEE:DYRQ,CPU:1.7GHZ,DOR3:SAMSUNG_4GB
639-3553	PCBA,MLB,1.5GHZ,SA 4GB,J13	J13_CMNPTS,EEEE:DYRM,CPU:1.5GHZ,DOR3:SAMSUNG_4GB
639-3554	PCBA,MLB,1.5GHZ,HY 4GB,J13	J13_CMNPTS,EEEE:DYRN,CPU:1.5GHZ,DOR3:HYWIX_4GB
639-3555	PCBA,MLB,1.5GHZ,HY 8GB,J13	J13_CMNPTS,EEEE:DYRL,CPU:1.5GHZ,DOR3:HYWIX_8GB
639-3556	PCBA,MLB,1.7GHZ,HY 8GB,J13	J13_CMNPTS,EEEE:DYRP,CPU:1.7GHZ,DOR3:HYWIX_8GB
639-3557	PCBA,MLB,1.7GHZ,HY 4GB,J13	J13_CMNPTS,EEEE:DYRQ,CPU:1.7GHZ,DOR3:HYWIX_4GB
639-3645	PCBA,MLB,1.5GHZ,EL 8GB,J13	J13_CMNPTS,EEEE:F0TC,CPU:1.5GHZ,DOR3:ELPIDA_8GB
639-3644	PCBA,MLB,1.7GHZ,EL 8GB,J13	J13_CMNPTS,EEEE:F0TD,CPU:1.7GHZ,DOR3:ELPIDA_8GB
639-3760	PCBA,MLB,1.8GHZ,SA 4GB,J13	J13_CMNPTS,EEEE:F25Q,CPU:1.8GHZ,DOR3:SAMSUNG_4GB
639-3761	PCBA,MLB,1.8GHZ,HY 8GB,J13	J13_CMNPTS,EEEE:F25T,CPU:1.8GHZ,DOR3:HYWIX_8GB
639-3762	PCBA,MLB,1.8GHZ,HY 4GB,J13	J13_CMNPTS,EEEE:F25Y,CPU:1.8GHZ,DOR3:HYWIX_4GB
639-3763	PCBA,MLB,1.8GHZ,EL 8GB,J13	J13_CMNPTS,EEEE:F25R,CPU:1.8GHZ,DOR3:ELPIDA_8GB
639-3764	PCBA,MLB,2.0GHZ,SA 4GB,J13	J13_CMNPTS,EEEE:F25W,CPU:2.0GHZ,DOR3:SAMSUNG_4GB
639-3765	PCBA,MLB,2.0GHZ,HY 8GB,J13	J13_CMNPTS,EEEE:F25V,CPU:2.0GHZ,DOR3:HYWIX_8GB
639-3766	PCBA,MLB,2.0GHZ,HY 4GB,J13	J13_CMNPTS,EEEE:F25U,CPU:2.0GHZ,DOR3:HYWIX_4GB
639-3767	PCBA,MLB,2.0GHZ,EL 8GB,J13	J13_CMNPTS,EEEE:F25V,CPU:2.0GHZ,DOR3:ELPIDA_8GB
639-3790	PCBA,MLB,1.7GHZ,SA 8GB,J13	J13_CMNPTS,EEEE:F27V,CPU:1.7GHZ,DOR3:SAMSUNG_8GB
639-3791	PCBA,MLB,1.8GHZ,SA 8GB,J13	J13_CMNPTS,EEEE:F27Q,CPU:1.8GHZ,DOR3:SAMSUNG_8GB
639-3792	PCBA,MLB,2.0GHZ,SA 8GB,J13	J13_CMNPTS,EEEE:F27R,CPU:2.0GHZ,DOR3:SAMSUNG_8GB
639-3793	PCBA,MLB,1.7GHZ,EL 4GB,J13	J13_CMNPTS,EEEE:F27W,CPU:1.7GHZ,DOR3:ELPIDA_4GB
639-3794	PCBA,MLB,1.8GHZ,EL 4GB,J13	J13_CMNPTS,EEEE:F27Y,CPU:1.8GHZ,DOR3:ELPIDA_4GB
639-3795	PCBA,MLB,2.0GHZ,EL 4GB,J13	J13_CMNPTS,EEEE:F27Y,CPU:2.0GHZ,DOR3:ELPIDA_4GB

Bar Code Labels / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DYRK]	CRITICAL	EEEE:DYRK
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DYRL]	CRITICAL	EEEE:DYRL
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DYRM]	CRITICAL	EEEE:DYRM
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DYRN]	CRITICAL	EEEE:DYRN
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DYRP]	CRITICAL	EEEE:DYRP
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DYRQ]	CRITICAL	EEEE:DYRQ
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F0TC]	CRITICAL	EEEE:F0TC
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F0TD]	CRITICAL	EEEE:F0TD
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F25N]	CRITICAL	EEEE:F25N
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F25P]	CRITICAL	EEEE:F25P
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F25Q]	CRITICAL	EEEE:F25Q
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F25R]	CRITICAL	EEEE:F25R
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F25T]	CRITICAL	EEEE:F25T
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F25V]	CRITICAL	EEEE:F25V
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F25W]	CRITICAL	EEEE:F25W
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F25Y]	CRITICAL	EEEE:F25Y
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F27Q]	CRITICAL	EEEE:F27Q
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F27R]	CRITICAL	EEEE:F27R
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F27T]	CRITICAL	EEEE:F27T
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F27V]	CRITICAL	EEEE:F27V
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F27W]	CRITICAL	EEEE:F27W
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F27Y]	CRITICAL	EEEE:F27Y

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Sub BOM


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-3939	1	J13 MLB DEVELOPMENT	DEVEL	CRITICAL	DEVEL_BOM
607-9090	1	CMN PTS,PCBA,MLB,J13	CMNPTS	CRITICAL	J13_CMNPTS

SYNC MASTER=J130 MLB

SYNC DATE=07/27/2013

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J13 BOM GROUPS

BOM GROUP	BOM OPTIONS
J13_COMMON	ALTERNATE,COMMON,J13_MISC,J13_DEBUG:ENG,J13_PROGPARTS,USBHUB2514B,EDP:YES,PCH_C1
J13_MISC	CPUMEM_SIG:NO,HUB_NONBREM,TBT,NHMS:YES,PSPVS_DCIN:NO,TPAD_PCH:NO,SKIP_SUV3:1,NAUDIBLE,BTWPB:S4,TBTHT:P15V,LVDDR3_BH:YES,ASQ_ACOUSTIC:NO
J13_PROGPARTS	BOOTFROM_PROG,SMC_PROG,TBTFROM:PROG
J13_DEVEL:ENG	ALTERNATE,BKLT:ENG,XDP_CONN,XDP_CPU:8PM,XDP_PCH,LPCPLUS,DORVREF_DAC,VREFDQ:M1_M3,VREFCA:LDO,LDO,LPCPLUS,VCCIOISNS_PROD,AIRPORTISNS_PROD,HDDISNS_PROD,LCDKSLTISNS_PROD
J13_DEVEL:PVT	LPCPLUS,XDP_CONN
J13_DEBUG:ENG	DEVEL_BOM,M0J0:YES,XDP
J13_DEBUG:PVT	DEVEL_BOM,M0J0:PROD,M0J0:YES,XDP,XDP_CPU:8PM,VREFDQ:LDO,VREFCA:LDO,VCCIOISNS_PROD,AIRPORTISNS_PROD,HDDISNS_PROD,LCDKSLTISNS_PROD
J13_DEBUG:PROD	BKLT:PROD,M0J0:YES,XDP,XDP_CPU:8PM,VREFDQ:LDO,VREFCA:LDO,LPCPLUS,VCCIOISNS_PROD,AIRPORTISNS_PROD,HDDISNS_PROD,LCDKSLTISNS_PROD
DDR3:HYNIX_4GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:HYNIX_4GB
DDR3:HYNIX_8GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:HYNIX_8GB
DDR3:SAMSUNG_4GB	RAMCFG0:L,RAMCFG1:H,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:SAMSUNG_4GB
DDR3:SAMSUNG_8GB	RAMCFG0:L,RAMCFG1:H,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:SAMSUNG_8GB
DDR3:ELPIDA_8GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:ELPIDA_8GB
DDR3:ELPIDA_4GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:ELPIDA_4GB

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0865	1	IC,SERIAL SPI EEPROM,256KBIT,20MHZ,MLP8	U3690	CRITICAL	TBTROM:BLANK
341S3475	1	IC,EEPROM,CR,V24-1,J11/J13	U3690	CRITICAL	TBTROM:PROD
338S1098	1	IC,SMC12-A3,40MHZ/50MKIPS MCU,9X9,157BGA	U4900	CRITICAL	SMC_BLANK
338S1065	1	IC,SMC12-A3,40MHZ/50MKIPS MCU, 9X9,157BGA	U4900	CRITICAL	SMC_BLANK
341S3433	1	IC,SMC,V2-1A43,Proto18,J13	U4900	CRITICAL	SMC_PROD
335S0809	1	64 MBIT SPI SERIAL DUAL I/O FLASH,Micron14	U6100	CRITICAL	BOOTROM:BLANK
335S0803	1	64 MBIT SPI SERIAL DUAL I/O FLASH,Micron14	U6100	CRITICAL	BOOTROM:BLANK
341S3482	1	IC,EFI ROM,PROTO18,J13 J11	U6100	CRITICAL	BOOTROM_PROD

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0855	376S0613		ALL	Diodes alt to Toshiba
376S0977	376S0859		ALL	Diodes alt to Toshiba
376S0972	376S0612		ALL	Bohm alt to Toshiba
138S0676	138S0691		ALL	Murata alt to Samsung
371S0709	371S0652		ALL	NXP alt to NXP
138S0671	138S0673		ALL	Taiyo alt to Murata
376S0790	376S0928		ALL	TI alt to Fairchild
152S1462	152S1295		ALL	Toko alt for NMC inductor
152S1085	152S1307		ALL	Toko alt for Cystec
138S0703	138S0648		ALL	Murata alt to Taiyo Yuden
138S0684	138S0660		ALL	Murata alt to Taiyo Yuden
152S1493	152S1300		ALL	Colicraft alt to Murata

353S3238	353S1428		ALL	Intersil alt to OPA2333
372S0186	372S0185		ALL	NXP alt to Diodes
376S1053	376S0664		ALL	Diodes alt to Fairchild
376S0855	376S0613		ALL	Diodes alt to Toshiba
376S0903	376S0796		ALL	Fairchild alt to Siliconix
197S0431	197S0432		ALL	Epson alt to NDK
337S4198	337S4197		ALL	TDP 1.5GHE alt to Nominal
337S4236	337S4196		ALL	TDP 1.7GHE alt to Nominal
371S0713	371S0558		ALL	Diodes alt to ST Micro
128S0333	998-4435		ALL	Sanyo alt to Kemet
128S0357	998-4435		ALL	Sanyo alt to POS caps
998-4715	998-4435		ALL	Kemet_React alt to POS caps
998-4716	998-4435		ALL	Kemet_0045 Plate alt to POS caps

DRAM CFG CHART

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

SIZE	CFG 2
4GB	0
8GB	1

DIE REV	CFG 3
A	0
B	1

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4197	1	IVB,QBF8,ES2,K0,1.5,17W,2+2,0.95,4M,ULVB	U1000	CRITICAL	CPU:1.5GHZ
337S4299	1	IVB,QC55,QS,L0,1.7,17W,2+2,1.0,3M,ULVBGA	U1000	CRITICAL	CPU:1.7GHZ
337S4298	1	IVB,QC54,QS,L0,1.8,17W,2+2,1.1,3M,ULVBGA	U1000	CRITICAL	CPU:1.8GHZ
337S4296	1	IVB,QC52,QS,L0,2.0,17W,2+2,1.1,4M,ULVBGA	U1000	CRITICAL	CPU:2.0GHZ
337S4198	1	IVB,QBF8,ES2,K0,1.5,17W,2+2,0.95,4M,ULVB	U1000	CRITICAL	CPU:1.5GHZTDP
337S4236	1	IVB,QBQF,ES2,K0,1.7,17W,2+2,1.0,4M,ULV,TDP	U1000	CRITICAL	CPU:1.7GHZTDP
337S4165	1	IC,PCH,PPT-MB,SFF,ES1	U1800	CRITICAL	PCH_ES1
337S4180	1	IC,PCH,PPT-MB,SFF,ES2,B0	U1800	CRITICAL	PCH_ES2
337S4235	1	IC,PCH,PPT-MB,SFF,P-QS,C0	U1800	CRITICAL	PCH_C0
337S4275	1	IC,PCH,PPT-MB,QS77,C1,QS	U1800	CRITICAL	PCH_C1
338S1047	1	IC,TBT,CR-4C,ES1,288 FCBGA,12X12MM	U3600	CRITICAL	TBT

333S0622	4	IC,SDRAM,2GBIT,256MX8,DOR3-1600,78P FBGA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0622	4	IC,SDRAM,2GBIT,256MX8,DOR3-1600,78P FBGA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0622	4	IC,SDRAM,2GBIT,256MX8,DOR3-1600,78P FBGA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0622	4	IC,SDRAM,2GBIT,256MX8,DOR3-1600,78P FBGA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0625	4	IC,SDRAM,4GBIT,512MX8,DOR3-1600,82 FBGA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S0625	4	IC,SDRAM,4GBIT,512MX8,DOR3-1600,82 FBGA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S0625	4	IC,SDRAM,4GBIT,512MX8,DOR3-1600,82 FBGA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S0625	4	IC,SDRAM,4GBIT,512MX8,DOR3-1600,82 FBGA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S0623	4	IC,SDRAM,2GBIT,DOR3-1600,78P FBGA,D-DIE	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0623	4	IC,SDRAM,2GBIT,DOR3-1600,78P FBGA,D-DIE	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0623	4	IC,SDRAM,2GBIT,DOR3-1600,78P FBGA,D-DIE	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0623	4	IC,SDRAM,2GBIT,DOR3-1600,78P FBGA,D-DIE	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0642	4	IC,SDRAM,4GBIT,DOR3-1600,78P FBGA,C-DIE	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
333S0642	4	IC,SDRAM,4GBIT,DOR3-1600,78P FBGA,C-DIE	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
333S0642	4	IC,SDRAM,4GBIT,DOR3-1600,78P FBGA,C-DIE	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
333S0642	4	IC,SDRAM,4GBIT,DOR3-1600,78P FBGA,C-DIE	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
333S0629	4	IC,SDRAM,4GBIT,DOR3L-1600,REV B,78P FBGA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:ELPIDA_8GB
333S0629	4	IC,SDRAM,4GBIT,DOR3L-1600,REV B,78P FBGA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:ELPIDA_8GB
333S0629	4	IC,SDRAM,4GBIT,DOR3L-1600,REV B,78P FBGA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:ELPIDA_8GB
333S0629	4	IC,SDRAM,4GBIT,DOR3L-1600,REV B,78P FBGA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:ELPIDA_8GB
333S0628	4	IC,SDRAM,2GBIT,DOR3L-1600,REV C,78P FBGA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0628	4	IC,SDRAM,2GBIT,DOR3L-1600,REV D,78P FBGA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0628	4	IC,SDRAM,2GBIT,DOR3L-1600,REV D,78P FBGA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0628	4	IC,SDRAM,2GBIT,DOR3L-1600,REV D,78P FBGA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:ELPIDA_4GB

353S2929	1	IC,1S16259,BATCHNUMBER,38,4X4MM,QFN68	U7000	CRITICAL	
946-3115	1	MLB,DYMAX UV EB 0.220GRAM,R21	GLUE	CRITICAL	

PD Module Parts


806-3142	1	CAN,T29,J11/J13	TBTFENCE	CRITICAL	
806-3215	1	CAN,COVER,T29,J11/J13	TBTCOVER	CRITICAL	
806-3214	1	CAN,TOPSIDE,J11/J13	TBTTOPSIDE_1P	CRITICAL	
806-3706	1	CAN,TOPSIDE_2Ppiece_Cover,J11/J13	TBTTOPSIDE_2P_COVER	CRITICAL	
806-3705	1	CAN,TOPSIDE_2Ppiece_Fence,J11/J13	TBTTOPSIDE_2P_FENCE	CRITICAL	
806-3216	1	CAN,MDF,J11/J13	MDFCAN	CRITICAL	
806-3083	1	SRLD,USB,MLB,J11/J13	USBCAN	CRITICAL	
806-2377	1	K78, mCP Spring	MDFSPRING	CRITICAL	NOSTUFF

SYNC MASTER=J30 MLB

SYNC DATE=07/27/2013

PAGE TITLE

BOM Configuration

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Functional Test Points

J4001: AirPort / BT Connector

FUNC_TEST			
TRUE	PP3V3 WLAN_F	37	42
TRUE	WIFI_EVENT_L	37	41 42
TRUE	PCIE AP R2D_N	37	69
TRUE	PCIE AP R2D_P	37	69
TRUE	PCIE_CLK100M AP_N	16	37 69
TRUE	PCIE_CLK100M AP_P	16	37 69
TRUE	USB_BT_CONN_P	37	68
TRUE	USB_BT_CONN_N	37	68
TRUE	PCIE AP D2R_P	16	37 69
TRUE	PCIE AP D2R_N	16	37 69
TRUE	PCIE_WAKE_L	17	37
TRUE	AP_RESET_CONN_L	37	
TRUE	AP_CLKREQ_O_L	37	
TRUE	PP3V3_S3R54_BT_F	37	
(Need to add 8 GND TPs)			

J5715: KB BKLT CONNECTOR

FUNC_TEST			
TRUE	KBDLED_FB	49	
TRUE	KBDLED_ANODE	49	
(Need to add 2 GND TP)			

J4700: LIO Connector

FUNC_TEST			
TRUE	PP3V42_G3H_ONEWIRE	7	40
TRUE	PP3V3_S0_AUDIO	7	40
TRUE	PP3V3R1V5_S0_AUDIO	7	40
TRUE	SYS_ONEWIRE	40	41
TRUE	SMC_BC_ACOK	40	41 42
TRUE	USB_PWR_EN	39	40 62
TRUE	SMC_LID	6	40 41 42 49
TRUE	I2C_LIO_SDA	40	44
TRUE	I2C_LIO_SCL	40	44
TRUE	I2C_MIKEY_SCL	40	44
TRUE	I2C_MIKEY_SDA	40	44
TRUE	AUD_IPHS_SWITCH_EN	25	40
TRUE	AUD_IP_PERIPHERAL_DET	18	40
TRUE	AUD_I2C_INT_L	18	40
TRUE	AUD_GPIO_3	40	51
TRUE	SPKRAMP_INR_N	40	51 72
TRUE	SPKRAMP_INR_P	40	51 72
TRUE	USB_EXTB_N	24	40 68
TRUE	USB_EXTB_P	24	40 68
TRUE	USB3_EXTB_TX_C_N	40	68
TRUE	USB3_EXTB_TX_C_P	40	68
TRUE	USB3_EXTB_RX_RC_N	40	68
TRUE	USB3_EXTB_RX_RC_P	40	68
TRUE	USB_CAMERA_N	18	40 68
TRUE	USB_CAMERA_P	18	40 68
TRUE	HDA_SDOUT	16	40 69
TRUE	HDA_BIT_CLK	16	40 69
TRUE	HDA_SDINO	16	40 69
TRUE	USB_EXTB_OC_L	16	40 69
TRUE	HDA_RST_L	16	40 69
TRUE	HDA_SYNC	16	40 69
(Need to add 5 GND TPs)			

J4800: SD Card Connector

FUNC_TEST			
TRUE	PP3V3_SW_SD_PWR	33	
TRUE	SD_CLK	33	
TRUE	SD_CMD	33	
TRUE	SD_D<7..0>	33	
TRUE	SD_CD_L	33	
TRUE	SD_WP	33	
(Need to add 2 GND TPs)			

J5100: LPC+SPI Connector

FUNC_TEST			
TRUE	PP3V3_S5_LPCPLUS	7	43
TRUE	PP5V_S0_LPCPLUS	7	43
TRUE	LPC_AD<3..0>	16	41 43 69
TRUE	SPI_ALT_MOSI	43	
TRUE	SPI_ALT_MISO	43	
TRUE	LPC_FRAME_L	16	41 43 69
TRUE	PM_CLKRUN_L	17	41 43
TRUE	SMC_TMS	41	42 43
TRUE	LPCPLUS_RESET_L	25	43 69
TRUE	SMC_TDO	41	42 43
TRUE	TP_SMC_TRST_L	43	
TRUE	TP_SMC_MD1	43	
TRUE	SMC_TX_L	41	42 43
TRUE	LPC_CLK33M_LPCPLUS	25	43 69
TRUE	SPIROM_USE_MLB	19	43 50
TRUE	SPI_ALT_CLK	43	
TRUE	SPI_ALT_CS_L	43	
TRUE	LPC_SERIRQ	16	41 43
TRUE	LPC_PWRDWN_L	17	25 41 43
TRUE	SMC_TDI	41	42 43
TRUE	SMC_TCK	41	42 43
TRUE	SMC_RESET_L	41	42 43 53
TRUE	SMC_ROMBOOT	42	43
TRUE	SMC_RX_L	41	42 43
TRUE	LPCPLUS_GPIO	19	43
(Need to add 6 GND TPs)			

J5600: Fan Connector

FUNC_TEST			
TRUE	PP5V_S0_FAN	7	48
TRUE	FAN_RT_TACH	48	
TRUE	FAN_RT_PWM	48	
(Need to add 1 GND TP)			

J5700: IPD Flex Connector

FUNC_TEST			
TRUE	PP3V3_TPAD_CONN	49	
TRUE	PP5V_TPAD_FILT	49	
TRUE	PP3V42_G3H_TPAD	7	49
TRUE	USB_TPAD_CONN_P	68	
TRUE	USB_TPAD_CONN_N	68	
TRUE	I2C_TPAD_SDA	44	49
TRUE	I2C_TPAD_SCL	44	49
TRUE	SMC_ONOFF_L	41	42 49
TRUE	SMC_LID	6	40 41 42 49
TRUE	SMC_TPAD_RST_L	42	49
TRUE	SMC_PME_S4_WAKE_L	41	42 49
(Need to add 5 GND TPs)			

J6903: Speaker Connector

FUNC_TEST			
TRUE	SPKRAMP_ROUT_P	51	52 72
TRUE	SPKRAMP_ROUT_N	51	52 72
(Need to add 3 GND TPs)			

J6950: Battery Connector

FUNC_TEST			
TRUE	PPVBAT_G3H_CONN	52	53
TRUE	SMBUS_BATT_SCL	44	52
TRUE	SMBUS_BATT_SDA	44	52
TRUE	SYS_DETECT_L	52	
(Need to add 4 GND TPs near J6950 and 1 for shield)			

J9000: Internal DP Connector

FUNC_TEST			
TRUE	PPVOUT_SW_LCDCLK	63	65
TRUE	PP3V3_SW_LCD	63	
TRUE	I2C_TCON_SDA_R	63	
TRUE	I2C_TCON_SCL_R	63	
TRUE	LED_RETURN_6	63	65
TRUE	LED_RETURN_5	63	65
TRUE	LED_RETURN_4	63	65
TRUE	LED_RETURN_3	63	65
TRUE	LED_RETURN_2	63	65
TRUE	LED_RETURN_1	63	65
TRUE	DP_INT_HPD_CONN	63	
TRUE	DP_INT_AUX_CH_C_N	63	66
TRUE	DP_INT_AUX_CH_C_P	63	66
TRUE	DP_INT_ML_F_P<0>	63	66
TRUE	DP_INT_ML_F_N<0>	63	66
TRUE	DP_INT_ML_F_P<1>	66	
TRUE	DP_INT_ML_F_N<1>	66	
(Need to add 5 GND TPs)			

Misc Voltages & Control Signals

FUNC_TEST			
TRUE	PPBUS_G3H	7	52
TRUE	PPVIN_SW_TBTBST	7	36
TRUE	PPBUS_S5_HS_COMPUTING_ISNS	7	
TRUE	PPDCIN_G3H	7	
TRUE	PP3V42_G3H	7	
TRUE	PPVRTC_G3H	7	
TRUE	PP5V_S5	7	
TRUE	PP5V_SUS	7	
TRUE	PP3V3_S5	7	72
TRUE	PP3V3_SUS	7	
TRUE	PP3V3_S3	7	
TRUE	PP1V8_S0	7	
TRUE	PP3V3_S0	7	72
TRUE	PP1V5_S3	7	67
TRUE	PP1V5_S3R50	7	67
TRUE	PP1V5_S0	7	
TRUE	PP1V05_S0	7	
TRUE	PPVTTDDR_S3	7	
TRUE	PP0V75_S0_DDRVTT	7	
TRUE	PPVCCSA_S0_CPU	7	
TRUE	PP1V05_SUS	7	
TRUE	PP15V_TBT	7	
TRUE	PP3V3_TBTL_C	7	
TRUE	PP1V05_TBTL_C	7	36
TRUE	PP1V05_S0_PCH_VCCADPLL	7	
TRUE	PPVCORE_S0_CPU	7	
TRUE	PPVCORE_S0_AXG	7	
TRUE	PP1V5_S3_CPU_VCCDQ	7	
TRUE	PP1V05_S0_CPU_VCCPQEQ	7	
TRUE	PP1V8_S0_CPU_VCCPLL_R	7	
TRUE	PP1V05_TBTCIO	7	
TRUE	PPBUS_S5_HS_OTHER_ISNS	7	
TRUE	PPDCIN_G3H_ISOL	7	
TRUE	PP5V_S3	7	
TRUE	PP5V_S0	7	
TRUE	PP3V3_S4	7	
(Need to add 27 GND TPs)			

J4501: SATA SSD Connector

FUNC_TEST			
TRUE	PP3V3_S0_SSD_FLT	38	
TRUE	SATA_SSD_D2R_P	38	68
TRUE	SATA_SSD_D2R_N	38	68
TRUE	SMC_OOB1_RX_L	38	41
TRUE	SMC_OOB1_TX_L	38	41 42
TRUE	PCIE_CLK100M_SSD_P	16	38 66
TRUE	PCIE_CLK100M_SSD_N	16	38 66
TRUE	PCIE_SSD_R2D_P<1>	38	66
TRUE	PCIE_SSD_R2D_N<1>	38	66
TRUE	PCIE_SSD_D2R_P<1>	8	38 66
TRUE	PCIE_SSD_D2R_N<1>	8	38 66
TRUE	SATA_SSD_R2D_N	38	68
TRUE	SATA_SSD_R2D_P	38	68
TRUE	SSD_CLKREQ_L	16	38
TRUE	SATA_PCIE_SEL	38	
TRUE	SSD_P3V3S0_EN	38	
TRUE	SSD_RESET_L	25	38
(Need to add 6 GND TPs)			

J6900: DC-In Connector

FUNC_TEST			
TRUE	PP18V5_DCIN_CONN	7	52
TRUE	PP5V_S3_LIO_CONN	7	52
(Need to add 5 GND TPs)			

NO_TEST Nets

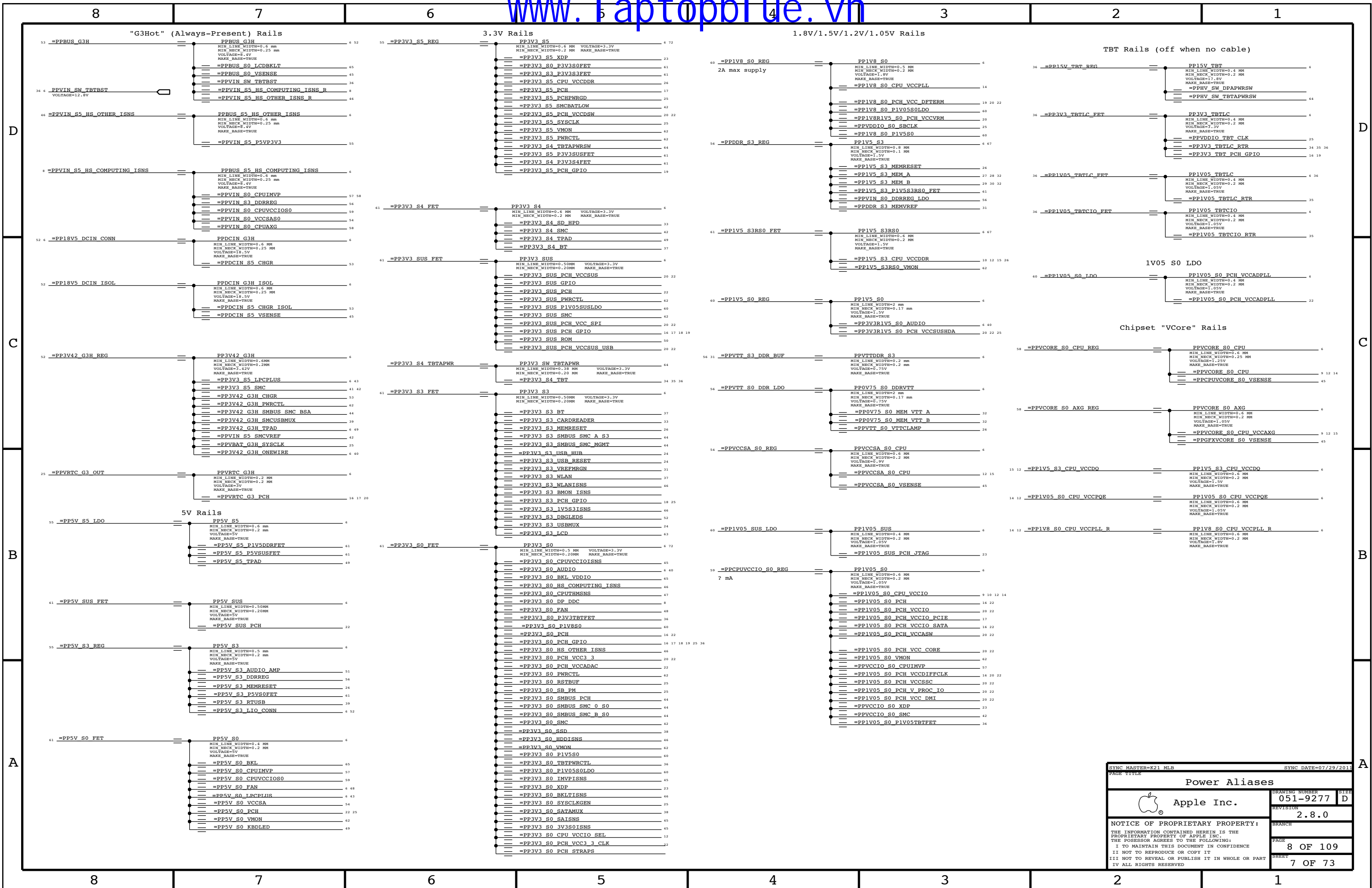
POWER SIGNALS			
TRUE	VCCSA0_SREF	54	
TRUE	VCCSA0_SET1_R	54	
TRUE	VCCSA0_SET0	54	
TRUE	VCCSA0_SET1	54	
NO_TEST			
TP_CRT_IG_BLUE	TRUE	NC_CRT_IG_BLUE	
TP_CRT_IG_GREEN	TRUE	NC_CRT_IG_GREEN	
TP_CRT_IG_RED	TRUE	NC_CRT_IG_RED	
TP_CRT_IG_DDC_CLK	TRUE	NC_CRT_IG_DDC_CLK	
TP_CRT_IG_DDC_DATA	TRUE	NC_CRT_IG_DDC_DATA	
TP_CRT_IG_HSYNC	TRUE	NC_CRT_IG_HSYNC	
TP_CRT_IG_VSYNC	TRUE	NC_CRT_IG_VSYNC	
TP_LVDS_IG_CTRL_CLK	TRUE	NC_LVDS_IG_CTRL_CLK	
TP_LVDS_IG_CTRL_DATA	TRUE	NC_LVDS_IG_CTRL_DATA	
TP_PCH_LVDS_VBG	TRUE	NC_PCH_LVDS_VBG	
TP_HDA_SDIN1	TRUE	NC_HDA_SDIN1	
TP_HDA_SDIN2	TRUE	NC_HDA_SDIN2	
TP_HDA_SDIN3	TRUE	NC_HDA_SDIN3	
TP_PCI_PME_L	TRUE	NC_PCI_PME_L	
TP_PCI_CLK13M_OUT3	TRUE	NC_PCI_CLK13M_OUT3	
TP_CLINK_CLK	TRUE	NC_CLINK_CLK	
TP_CLINK_DATA	TRUE	NC_CLINK_DATA	
TP_CLINK_RESET_L	TRUE	NC_CLINK_RESET_L	
TP_PCIE_CLK100M_PERN	TRUE	NC_PCIE_CLK100M_PERN	
TP_PCIE_CLK100M_PEPB	TRUE	NC_PCIE_CLK100M_PEPB	
XDP_PCH_AP_PWR_EN	TRUE		
XDP_PCH_USB_HUB_SOFT_RST_L	TRUE		
XDP_PCH_SDCONN_STATE_RST_L	TRUE		
XDP_PCH_ENET_PWR_EN	TRUE		
XDP_PCH_SDCONN_DET_L	TRUE		
XDP_PCH_S5_PWRGD	23		
XDP_PCH_PWRBTN_L	23		
XDP_PCH_ISOLATE_CPU_MEM_L	TRUE		
XDP_FW_CLKREQ_L	TRUE		
XDP_AP_CLKREQ_L	TRUE		
XDP_PCH_AUD_IPHS_SWITCH_EN	TRUE		

TP_SDVO_TVCCLKIN			
TRUE	NC_SDVO_TVCCLKIN		
TP_SDVO_TVCCLKINP	TRUE	NC_SDVO_TVCCLKINP	
TP_SDVO_STALLN	TRUE	NC_SDVO_STALLN	
TP_SDVO_STALLP	TRUE	NC_SDVO_STALLP	
TP_SDVO_INTN	TRUE	NC_SDVO_INTN	
TP_SDVO_INTP	TRUE	NC_SDVO_INTP	
TP_XDP_PCH_OBSPN_A<0..1>	TRUE	NC_TP_XDP_PCH_OBSPN_A<0..1>	
TP_XDP_PCH_OBSPN_B<0..1>	TRUE	NC_TP_XDP_PCH_OBSPN_B<0..1>	
TP_XDP_PCH_HOOK2	TRUE	NC_TP_XDP_PCH_HOOK2	
TP_XDP_PCH_HOOK3	TRUE	NC_TP_XDP_PCH_HOOK3	
TP_XDP_PCH_OBSPN_D<0..1>	TRUE	NC_TP_XDP_PCH_OBSPN_D<0..1>	
TP_XDP_PCH_HOOK4	TRUE	NC_TP_XDP_PCH_HOOK4	
TP_XDP_PCH_HOOK5	TRUE	NC_TP_XDP_PCH_HOOK5	
TP_PCH_GPIO64_CLKOUTFLEX0	TRUE	NC_PCH_GPIO64_CLKOUTFLEX0	
TP_PCH_GPIO65_CLKOUTFLEX1	TRUE	NC_PCH_GPIO65_CLKOUTFLEX1	
TP_PCH_GPIO66_CLKOUTFLEX2	TRUE	NC_PCH_GPIO66_CLKOUTFLEX2	
TP_PCH_GPIO67_CLKOUTFLEX3	TRUE	NC_PCH_GPIO67_CLKOUTFLEX3	

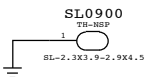
NC_EDP_TXP<0..3>	TRUE	TP_EDP_TX_P<0..3>	9
MAKE_BASE=TRUE			
NC_EDP_TXN<0..3>	TRUE	TP_EDP_TX_N<0..3>	9
MAKE_BASE=TRUE			
NC_EDP_AUXN	TRUE	TP_EDP_AUX_P	
MAKE_BASE=TRUE			
NC_EDP_AUXN	TRUE	TP_EDP_AUX_N	
MAKE_BASE=TRUE			
NC_CPU_THERMDA	TRUE	TP_CPU_THERMDA	
MAKE_BASE=TRUE			
NC_CPU_THERMDC	TRUE	TP_CPU_THERMDC	
MAKE_BASE=TRUE			
NC_CPU_RSVD<30..45>	TRUE	TP_CPU_RSVD<30..45>	
MAKE_BASE=TRUE			
NC_CPU_RSVD<8..27>	TRUE	TP_CPU_RSVD<8..27>	
MAKE_BASE=TRUE			
NC_PEG_R2D_CP<15..2>	TRUE	=PEG_R2D_C_P<15..2>	9
MAKE_BASE=TRUE			
NC_PEG_R2D_CN<15..2>	TRUE	=PEG_R2D_C_N<15..2>	9
MAKE_BASE=TRUE			
NC_PEG_D2RP<15..2>	TRUE	=PEG_D2R_P<15..2>	9
MAKE_BASE=TRUE			
NC_PEG_D2RN<15..2>	TRUE	=PEG_D2R_N<15..2>	9
MAKE_BASE=TRUE			

TP_PCIE_CLK100M_PEN	TRUE	NC_PCIE_CLK100M_PEN	
TP_PCIE_CLK100M_PENP	TRUE	NC_PCIE_CLK100M_PENP	
TP_PCIE_CLK100M_PENN	TRUE	NC_PCIE_CLK100M_PENN	
TP_PCIE_CLK100M_PEP	TRUE	NC_PCIE_CLK100M_PEP	
TP_PCIE_CLK100M_PEPN	TRUE	NC_PCIE_CLK100M_PEPN	
TP_PCIE_CLK100M_PEPN	TRUE	NC_PCIE_CLK100M_PEPN	
TP_PCIE_CLK100M_PEPN	TRUE	NC_PCIE_CLK100M_PEPN	
TP_PSDC_P1_3	TRUE	NC_PSDC_P1_3	
TP_SATA_B_D2RN	TRUE	NC_SATA_B_D2RN	
TP_SATA_B_D2RP	TRUE	NC_SATA_B_D2RP	
TP_SATA_B_R2D_CN	TRUE	NC_SATA_B_R2D_CN	
TP_SATA_B_R2D_CP	TRUE	NC_SATA_B_R2D_CP	
TP_SATA_D_D2RN	TRUE	NC_SATA_D_D2RN	
TP_SATA_D_D2RP	TRUE	NC_SATA_D_D2RP	
TP_SATA_D_R2D_CN	TRUE	NC_SATA_D_R2D_CN	
TP_SATA_D_R2D_CP	TRUE	NC_SATA_D_R2D_CP	
TP_SATA_E_D2RN	TRUE	NC_SATA_E_D2RN	
TP_SATA_E_D2RP	TRUE	NC_SATA_E_D2RP	
TP_SATA_E_R2D_CN	TRUE	NC_SATA_E_R2D_CN	
TP_SATA_E_R2D_CP	TRUE	NC_SATA_E_R2D_CP	
TP_SATA_F_D2RN	TRUE	NC_SATA_F_D2RN	
TP_SATA_F_D2RP	TRUE	NC_SATA_F_D2RP	
TP_SATA_F_R2D_CN	TRUE	NC_SATA_F_R2D_CN	
TP_SATA_F_R2D_CP	TRUE	NC_SATA_F_R2D_CP	

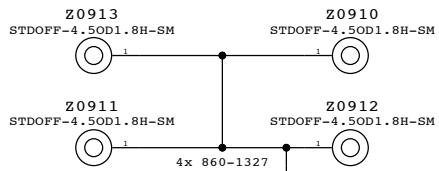
TP_PCH_TP18	TRUE	NC_PCH_TP18	
TP_PCH_TP17	TRUE	NC_PCH_TP17	
TP_PCH_TP16	TRUE	NC_PCH_TP16	
TP_PCH_TP15	TRUE	NC_PCH_TP15	
TP_PCH_TP14	TRUE	NC_PCH_TP14	
TP_PCH_TP13	TRUE	NC_PCH_TP13	



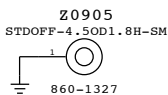
Plated Board Slot



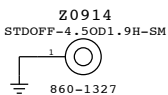
CPU Heat Sink Mounting Bosses



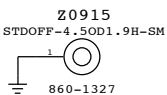
Fan Boss



X21 Boss

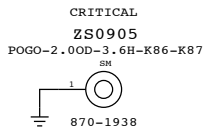


SSD Boss

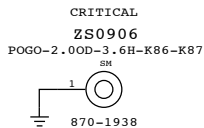


EMI I/O Pogo Pins

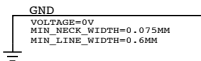
DisplayPort Pogo



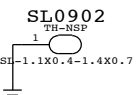
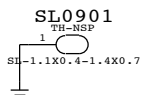
USB/SD Card Pogo



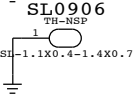
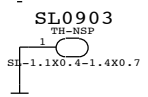
Digital Ground



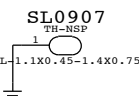
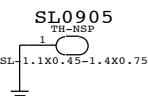
Can Slots



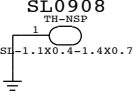
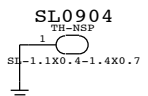
2x TBT pin diodes



2x MDP Connector



2x TBT chip



2x USB Connector

Unused PPT

16	PCIE CLK100M ENET N	==	NC PCIE CLK100M ENET N	==	MAKE_BASE=TRUE	NO_TEST=TRUE
16	PCIE CLK100M ENET P	==	NC PCIE CLK100M ENET P	==	MAKE_BASE=TRUE	NO_TEST=TRUE
16	PCIE CLK100M FW N	==	NC PCIE CLK100M FW N	==	MAKE_BASE=TRUE	NO_TEST=TRUE
16	PCIE CLK100M FW P	==	NC PCIE CLK100M FW P	==	MAKE_BASE=TRUE	NO_TEST=TRUE
16	PCIE CLK100M EXCARD N	==	NC PCIE CLK100M EXCARD N	==	MAKE_BASE=TRUE	NO_TEST=TRUE
16	PCIE CLK100M EXCARD P	==	NC PCIE CLK100M EXCARD P	==	MAKE_BASE=TRUE	NO_TEST=TRUE
16	PCIE ENET D2R N	==	NC PCIE ENET D2R N	==	MAKE_BASE=TRUE	NO_TEST=TRUE
16	PCIE ENET D2R P	==	NC PCIE ENET D2R P	==	MAKE_BASE=TRUE	NO_TEST=TRUE
16	PCIE ENET R2D C N	==	NC PCIE ENET R2D C N	==	MAKE_BASE=TRUE	NO_TEST=TRUE
16	PCIE ENET R2D C P	==	NC PCIE ENET R2D C P	==	MAKE_BASE=TRUE	NO_TEST=TRUE
16	PCIE FW D2R N	==	NC PCIE FW D2R N	==	MAKE_BASE=TRUE	NO_TEST=TRUE
16	PCIE FW D2R P	==	NC PCIE FW D2R P	==	MAKE_BASE=TRUE	NO_TEST=TRUE
16	PCIE FW R2D C N	==	NC PCIE FW R2D C N	==	MAKE_BASE=TRUE	NO_TEST=TRUE
16	PCIE FW R2D C P	==	NC PCIE FW R2D C P	==	MAKE_BASE=TRUE	NO_TEST=TRUE
16	PCIE EXCARD D2R N	==	NC PCIE EXCARD D2R N	==	MAKE_BASE=TRUE	NO_TEST=TRUE
16	PCIE EXCARD D2R P	==	NC PCIE EXCARD D2R P	==	MAKE_BASE=TRUE	NO_TEST=TRUE
16	PCIE EXCARD R2D C N	==	NC PCIE EXCARD R2D C N	==	MAKE_BASE=TRUE	NO_TEST=TRUE
16	PCIE EXCARD R2D C P	==	NC PCIE EXCARD R2D C P	==	MAKE_BASE=TRUE	NO_TEST=TRUE

67	MEM A CLK P<1>	==	TP MEM A CLKP<1>	==	MAKE_BASE=TRUE	NO_TEST=TRUE
67	MEM A CLK N<1>	==	TP MEM A CLKN<1>	==	MAKE_BASE=TRUE	NO_TEST=TRUE
67	MEM B CLK P<1>	==	TP MEM B CLKP<1>	==	MAKE_BASE=TRUE	NO_TEST=TRUE
67	MEM B CLK N<1>	==	TP MEM B CLKN<1>	==	MAKE_BASE=TRUE	NO_TEST=TRUE

19	ENET LOW PWR PCH	==	XDP D03 PCH GPIO49 ENET LOW PWR PCH	==	MAKE_BASE=TRUE	NO_TEST=TRUE
16	SATARDRVR EN	==	XDP DC3 PCH GPIO19 SATARDRVR EN	==	MAKE_BASE=TRUE	NO_TEST=TRUE
16	TP PCH CLKOUT DPW	==	DP1L REF CLK N	==	MAKE_BASE=TRUE	NO_TEST=TRUE
16	TP PCH CLKOUT DPP	==	DP1L REF CLK P	==	MAKE_BASE=TRUE	NO_TEST=TRUE

Unused USB

18	USB EXTC P	==	NC USB EXTC P	==	MAKE_BASE=TRUE	NO_TEST=TRUE
18	USB EXTC N	==	NC USB EXTC N	==	MAKE_BASE=TRUE	NO_TEST=TRUE
18	USB3 EXTC RX P	==	NC USB3 EXTC RX P	==	MAKE_BASE=TRUE	NO_TEST=TRUE
18	USB3 EXTC RX N	==	NC USB3 EXTC RX N	==	MAKE_BASE=TRUE	NO_TEST=TRUE
18	USB3 EXTC TX P	==	NC USB3 EXTC TX P	==	MAKE_BASE=TRUE	NO_TEST=TRUE
18	USB3 EXTC TX N	==	NC USB3 EXTC TX N	==	MAKE_BASE=TRUE	NO_TEST=TRUE
18	USB3 EXTD RX P	==	NC USB3 EXTD RX P	==	MAKE_BASE=TRUE	NO_TEST=TRUE
18	USB3 EXTD RX N	==	NC USB3 EXTD RX N	==	MAKE_BASE=TRUE	NO_TEST=TRUE
18	USB3 EXTD TX P	==	NC USB3 EXTD TX P	==	MAKE_BASE=TRUE	NO_TEST=TRUE
18	USB3 EXTD TX N	==	NC USB3 EXTD TX N	==	MAKE_BASE=TRUE	NO_TEST=TRUE
18	USB EXTD EHCI N	==	NC USB EXTD EHCI N	==	MAKE_BASE=TRUE	NO_TEST=TRUE
18	USB EXTD EHCI P	==	NC USB EXTD EHCI P	==	MAKE_BASE=TRUE	NO_TEST=TRUE

Unused PGOOD signal

TP P1V583RS0 RAMP DONE	==	P1V583RS0 RAMP DONE	==	MAKE_BASE=TRUE	NO_TEST=TRUE
TP DDRREG PGOOD	==	DDRREG PGOOD	==	MAKE_BASE=TRUE	NO_TEST=TRUE

SATA Aliases

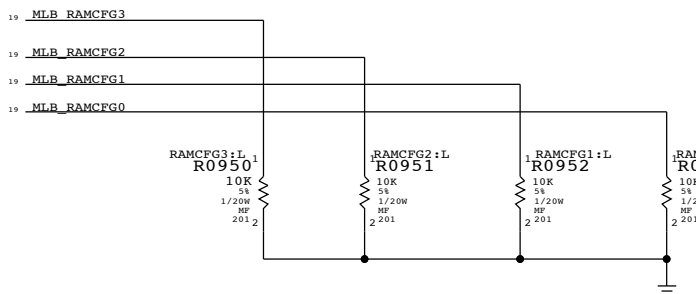
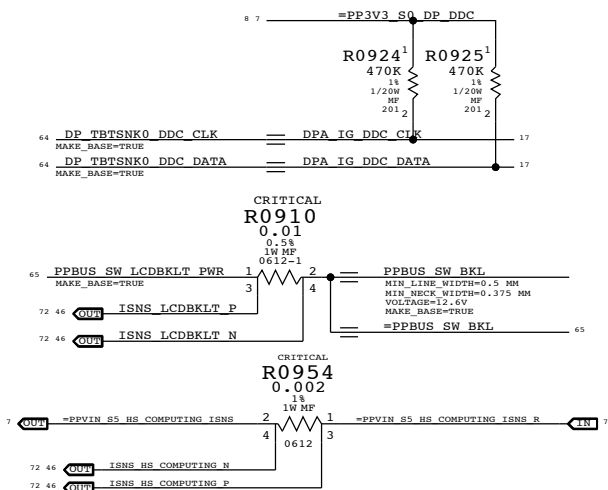
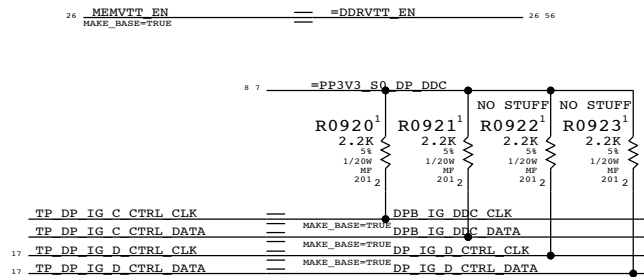
Unused SATA ODD Signals

16	SATA ODD R2D C P	==	NC SATA ODD R2DCP	==	MAKE_BASE=TRUE	NO_TEST=TRUE
16	SATA ODD R2D C N	==	NC SATA ODD R2DCN	==	MAKE_BASE=TRUE	NO_TEST=TRUE
16	SATA ODD D2R P	==	NC SATA ODD D2RP	==	MAKE_BASE=TRUE	NO_TEST=TRUE
16	SATA ODD D2R N	==	NC SATA ODD D2RN	==	MAKE_BASE=TRUE	NO_TEST=TRUE

SSD PCIE Signals

9	PEG D2R P<1..0>	==	PCIE SSD D2R P<1..0>	==	MAKE_BASE=TRUE	NO_TEST=TRUE
9	PEG D2R N<1..0>	==	PCIE SSD D2R N<1..0>	==	MAKE_BASE=TRUE	NO_TEST=TRUE
9	PEG R2D C P<1..0>	==	PCIE SSD R2D C P<1..0>	==	MAKE_BASE=TRUE	NO_TEST=TRUE
9	PEG R2D C N<1..0>	==	PCIE SSD R2D C N<1..0>	==	MAKE_BASE=TRUE	NO_TEST=TRUE

CPU signals



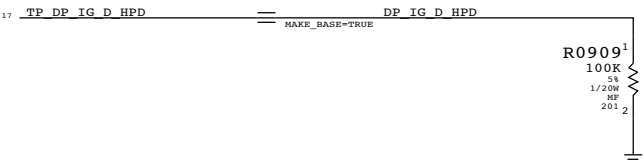
LVDS Aliases

6	TP LVDS IG B CLKP	==	LVDS IG B CLK P	==	MAKE_BASE=TRUE	NO_TEST=TRUE
6	TP LVDS IG B CLKN	==	LVDS IG B CLK N	==	MAKE_BASE=TRUE	NO_TEST=TRUE
6	NC LVDS IG B DATAP<0..3>	==	LVDS IG B DATA P<0..3>	==	MAKE_BASE=TRUE	NO_TEST=TRUE
6	NC LVDS IG B DATAN<0..3>	==	LVDS IG B DATA N<0..3>	==	MAKE_BASE=TRUE	NO_TEST=TRUE
6	NC LVDS IG A DATAP<3>	==	LVDS IG A DATA P<3>	==	MAKE_BASE=TRUE	NO_TEST=TRUE
6	NC LVDS IG A DATAN<3>	==	LVDS IG A DATA N<3>	==	MAKE_BASE=TRUE	NO_TEST=TRUE
6	LCD BKLT PWM	==	LVDS IG BKLT PWM	==	MAKE_BASE=TRUE	NO_TEST=TRUE
6	LCD IG PWR EN	==	LVDS IG PANEL PWR	==	MAKE_BASE=TRUE	NO_TEST=TRUE
6	LCD BKLT EN	==	LVDS IG BKLT ON	==	MAKE_BASE=TRUE	NO_TEST=TRUE

SMC Aliases

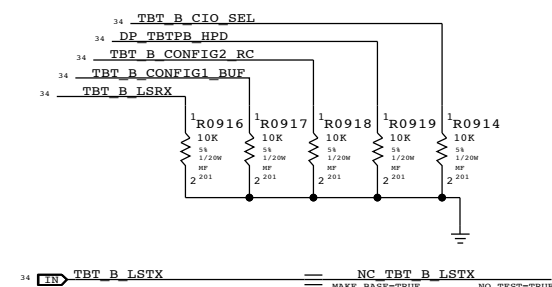
Unused SMC Signals

41	SMC SYS LED	==	NC SMC SYS LED	==	MAKE_BASE=TRUE	NO_TEST=TRUE
41	IR_RX_OUT_RC	==	NC IR_RX_OUT_RC	==	MAKE_BASE=TRUE	NO_TEST=TRUE



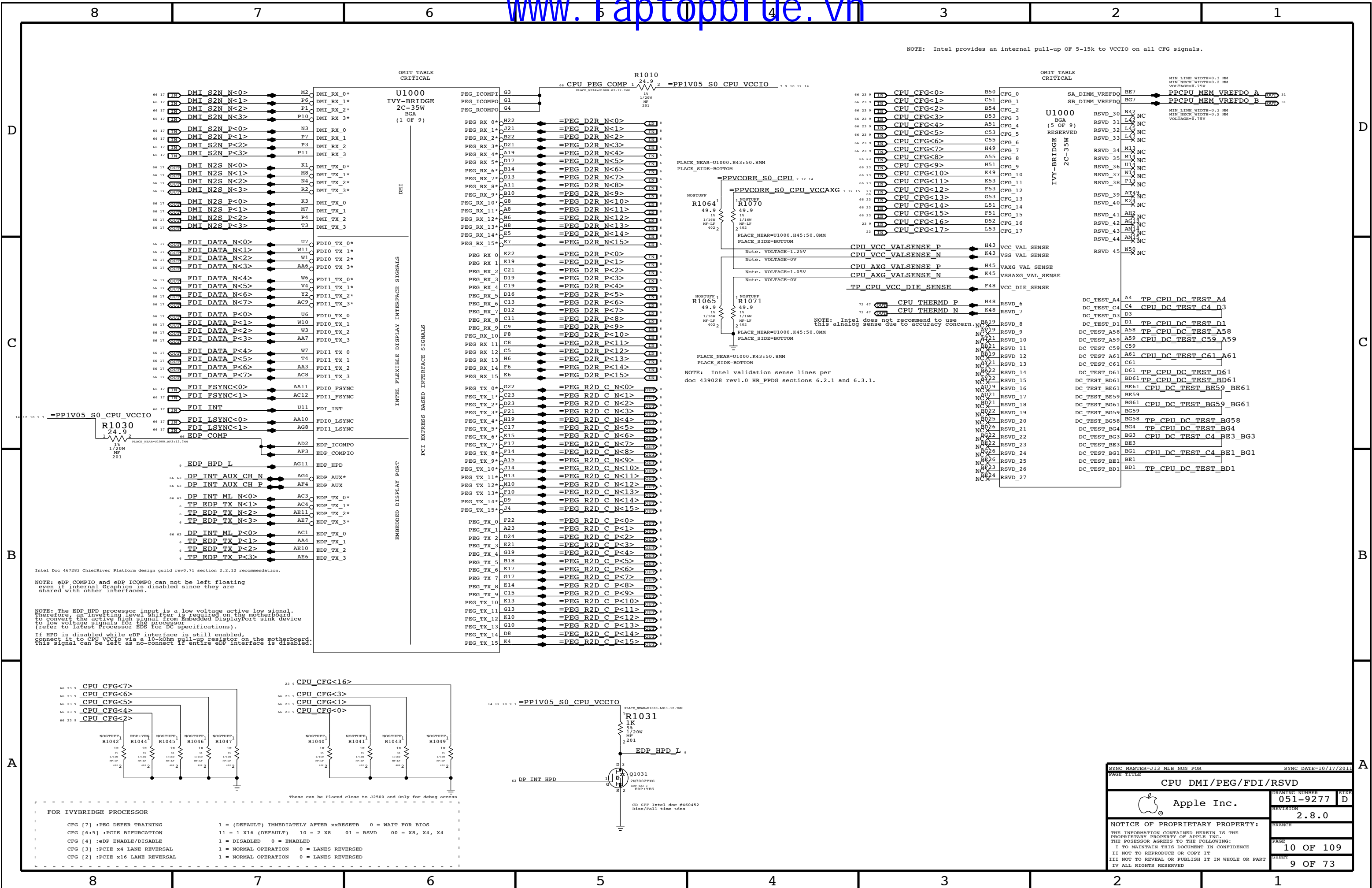
TBT DP Ports

17	DPB IG HPD	==	DP TBTSNK1 HPD	==	MAKE_BASE=TRUE	NO_TEST=TRUE
17	DPA IG HPD	==	DP TBTSNK0 HPD	==	MAKE_BASE=TRUE	NO_TEST=TRUE
69	DP TBTSNK0 AUXCH C P	==	DPA IG AUX CH P	==	MAKE_BASE=TRUE	NO_TEST=TRUE
69	DP TBTSNK0 AUXCH C N	==	DPA IG AUX CH N	==	MAKE_BASE=TRUE	NO_TEST=TRUE
69	DP TBTSNK1 AUXCH C P	==	DPB IG AUX CH P	==	MAKE_BASE=TRUE	NO_TEST=TRUE
69	DP TBTSNK1 AUXCH C N	==	DPB IG AUX CH N	==	MAKE_BASE=TRUE	NO_TEST=TRUE
69	DP TBTSNK1 ML C P<3..0>	==	TP DP IG C MLN<3..0>	==	MAKE_BASE=TRUE	NO_TEST=TRUE
69	DP TBTSNK1 ML C N<3..0>	==	TP DP IG C MLN<3..0>	==	MAKE_BASE=TRUE	NO_TEST=TRUE
69	DP TBTSNK0 ML C P<3..0>	==	TP DP IG B MLN<3..0>	==	MAKE_BASE=TRUE	NO_TEST=TRUE
69	DP TBTSNK0 ML C N<3..0>	==	TP DP IG B MLN<3..0>	==	MAKE_BASE=TRUE	NO_TEST=TRUE
70	DP TBTPB ML C P<1>	==	NC DP TBTPB ML C P<1>	==	MAKE_BASE=TRUE	NO_TEST=TRUE
70	DP TBTPB ML C N<1>	==	NC DP TBTPB ML C N<1>	==	MAKE_BASE=TRUE	NO_TEST=TRUE
70	DP TBTPB ML C P<3>	==	NC DP TBTPB ML C P<3>	==	MAKE_BASE=TRUE	NO_TEST=TRUE
70	DP TBTPB ML C N<3>	==	NC DP TBTPB ML C N<3>	==	MAKE_BASE=TRUE	NO_TEST=TRUE
70	DP TBTPB AUXCH C P	==	NC DP TBTPB AUXCH C P	==	MAKE_BASE=TRUE	NO_TEST=TRUE
70	DP TBTPB AUXCH C N	==	NC DP TBTPB AUXCH C N	==	MAKE_BASE=TRUE	NO_TEST=TRUE

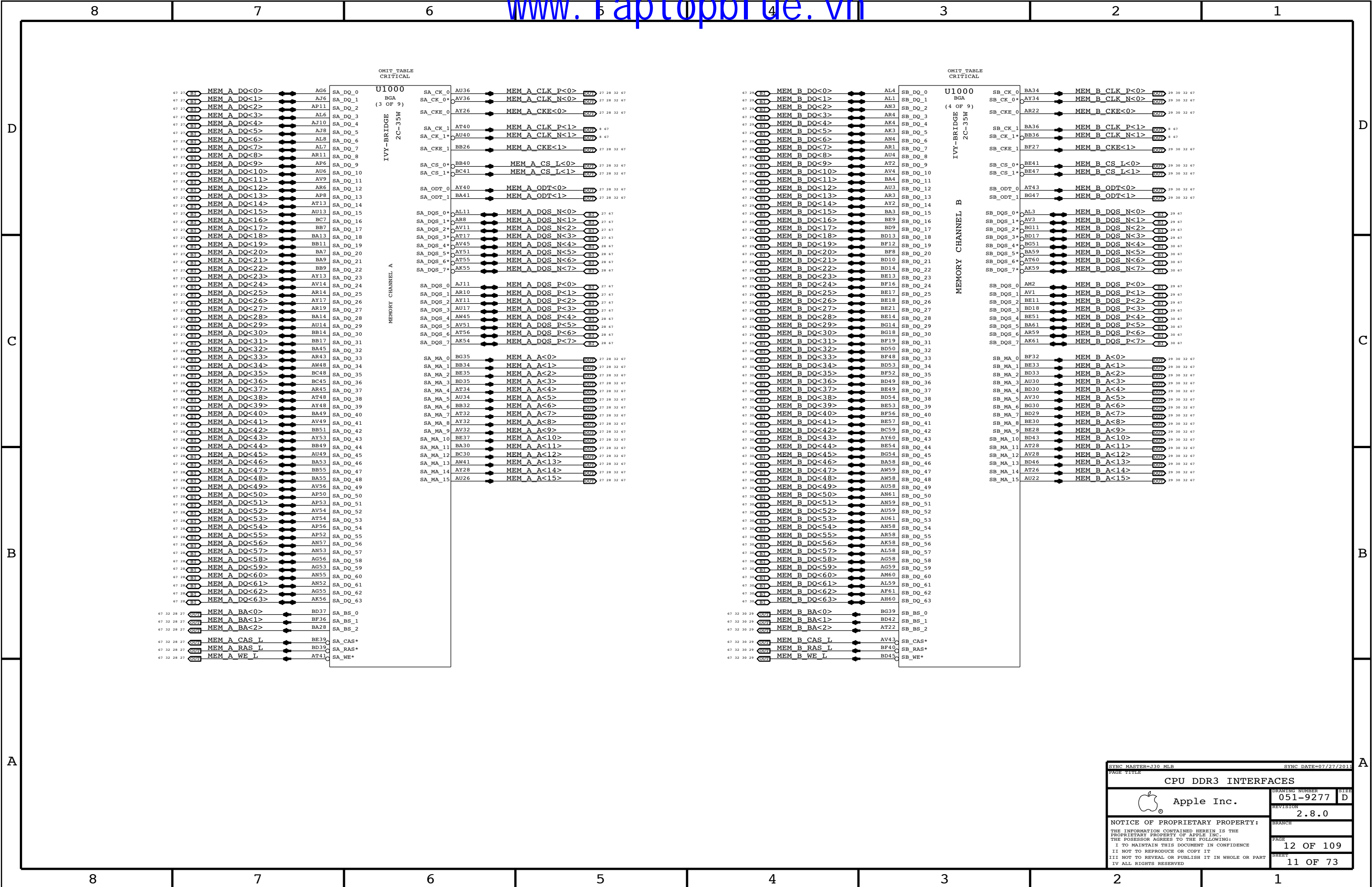


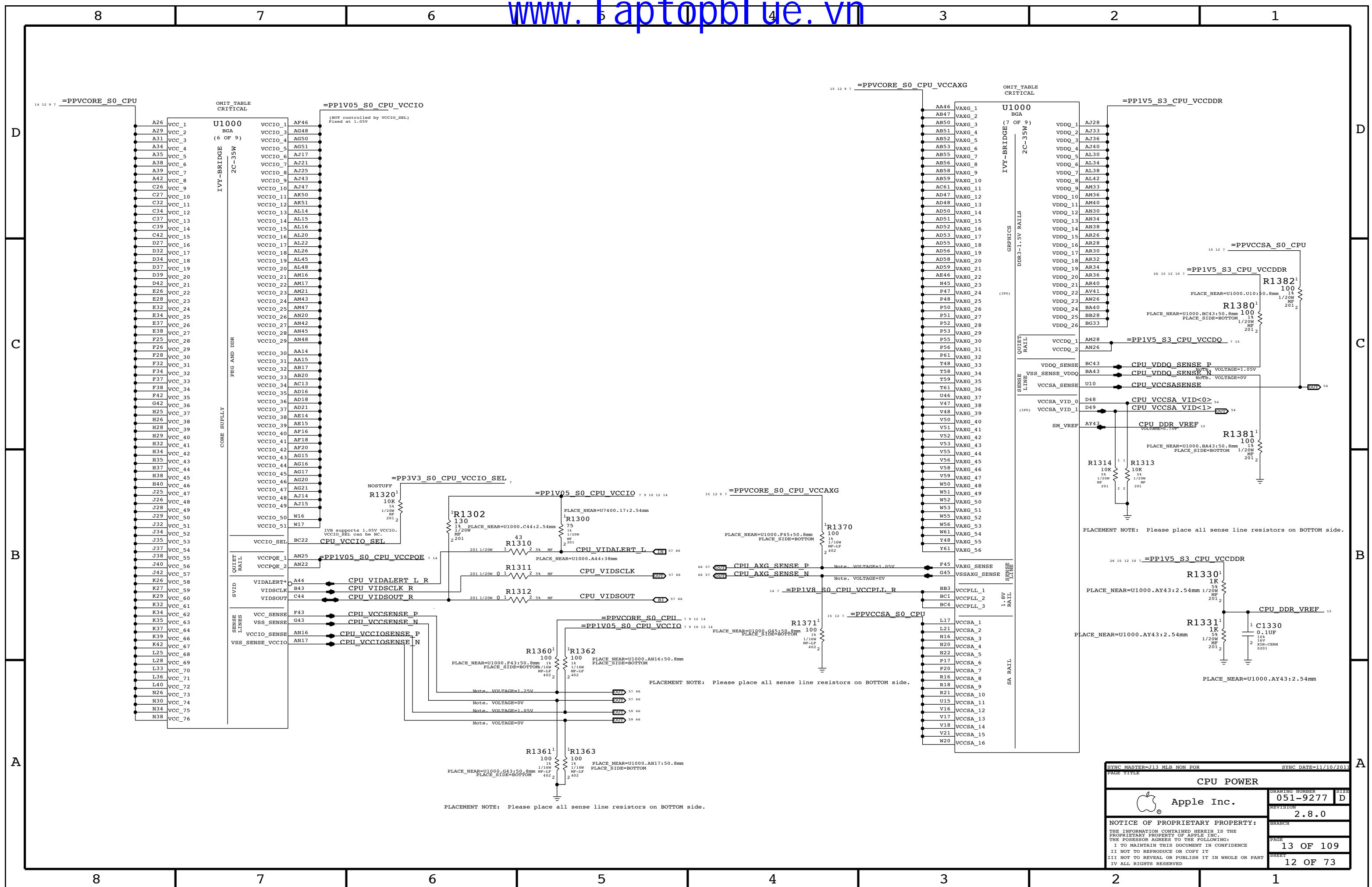
34	TBT B LSTX	==	NC TBT B LSTX	==	MAKE_BASE=TRUE	NO_TEST=TRUE
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SYNC MASTER=J13 MLB NON POR		SYNC DATE=11/10/2011	
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Apple Inc.		DRAWING NUMBER	051-9277
		REVISION	2.8.0
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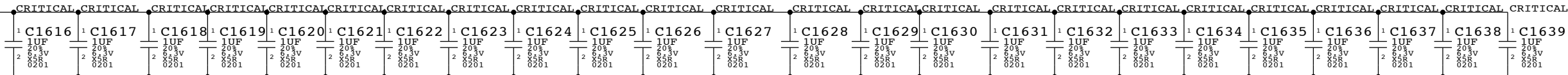
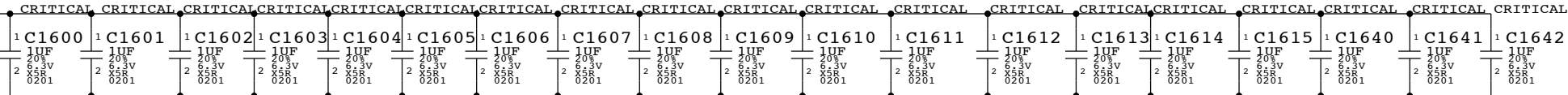
All INTEL recommendations from Intel doc #4439028 Huron River Platform Power Design Guide

CPU VCORE DECOUPLING

Processor Load Line : -2.9 mOhms

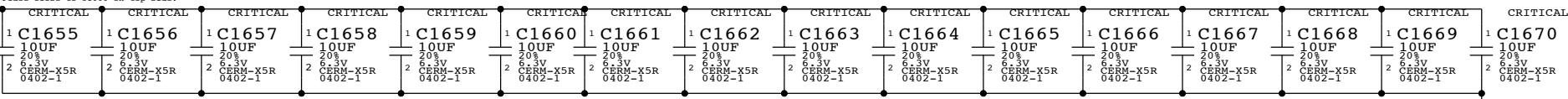
Intel recommendation (Table 7-1): 16x 2.2uF, 12x 22uF, 3x 330uF

12 9 7 =PPVCORE_S0_CPU



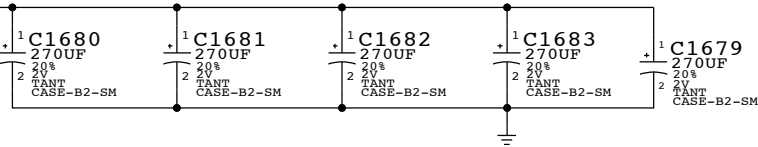
PLACEMENT_NOTE (C1655-C1666):

Place close to U1000 on top side.



PLACEMENT_NOTE (C1667-C1679):

PLACEMENT_NOTE (C1640-C1645):

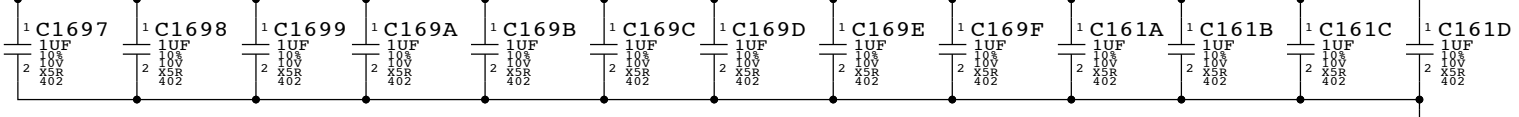
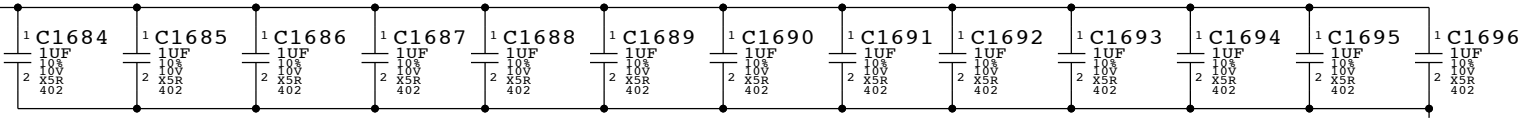


CPU VCCIO/VCCPQ DECOUPLING

Intel recommendation (Section 6.5): 26x 1uF, 10x 10uF, 2x 330uF

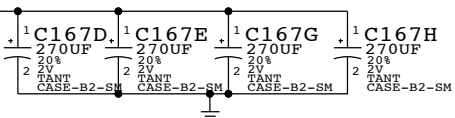
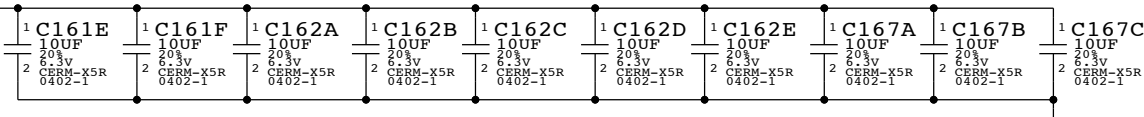
PLACEMENT_NOTE (C1684-C167F):

Place on bottom side of U1000

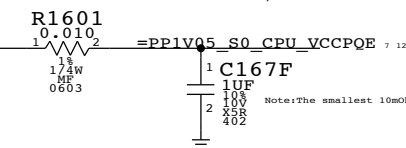


PLACEMENT_NOTE (C1672-C1681):

Place near U1000 on bottom side



Intel recommendation: 1x 10mOhm resistor, 1x 1uF 0402



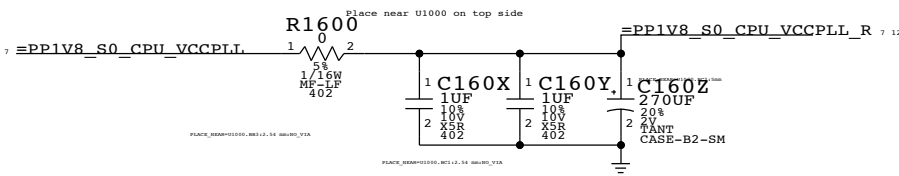
Note: The smallest 10mOhm available in the library are 0805s

CPU VCCPLL DECOUPLING

Intel recommendation (section 6.4): 2x 1uF, 1x 330uF

PLACEMENT_NOTE (C1646-C1671):

Place near U1000 on top side



CPU VCCPLL Low pass filter

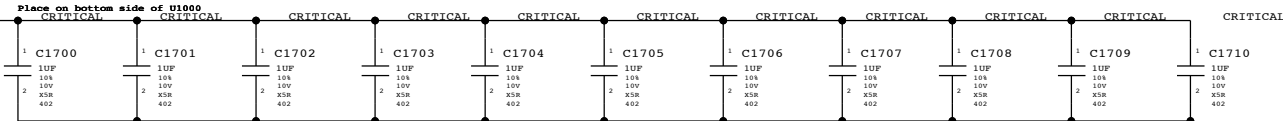
CPU DECOUPLING-I		
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	REVISION	2.8.0
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		14 OF 73

VAXG DECOUPLING

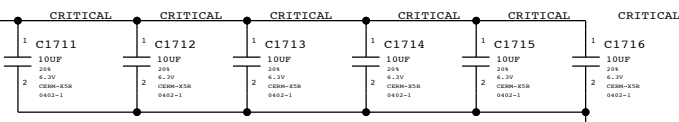
Graphics Load Line : -3.9 mOhms

Intel recommendation (section 6.3): 18x 1uF(9 no-stuff), 10x 104F(2 no-stuff), 8x 22uF(2 no stuff), 4x 470uF(2 no-stuff)

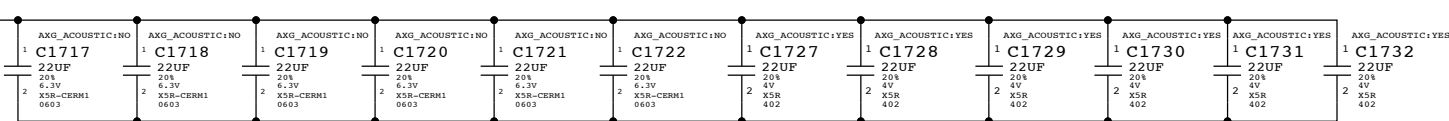
PLACEMENT_NOTE (C1700-C1710):



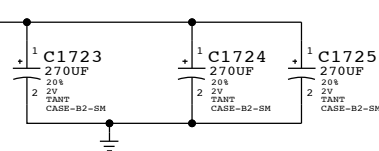
PLACEMENT_NOTE (C1711-C1716):



PLACEMENT_NOTE (C1717-C1722):



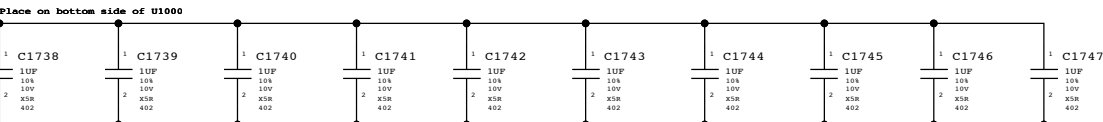
PLACEMENT_NOTE (C1723-C1724):



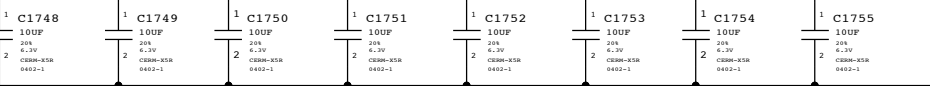
CPU VDDQ/VCCDQ DECOUPLING

Intel recommendation (Section 6.13): 10x 1uF, 8x 10uF, 1x 330uF

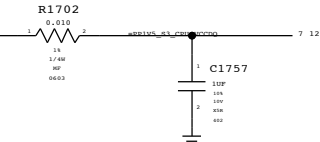
PLACEMENT_NOTE (C1738-C1747):



Place close to U1000 on bottom side



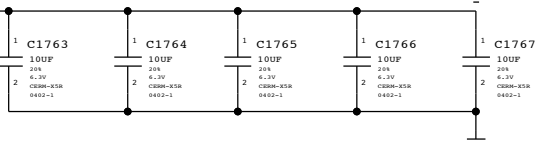
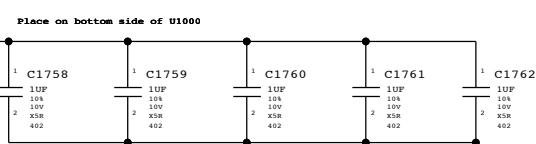
Intel recommendation: 1x 10mOhm resistor, 1x 1uF 0402



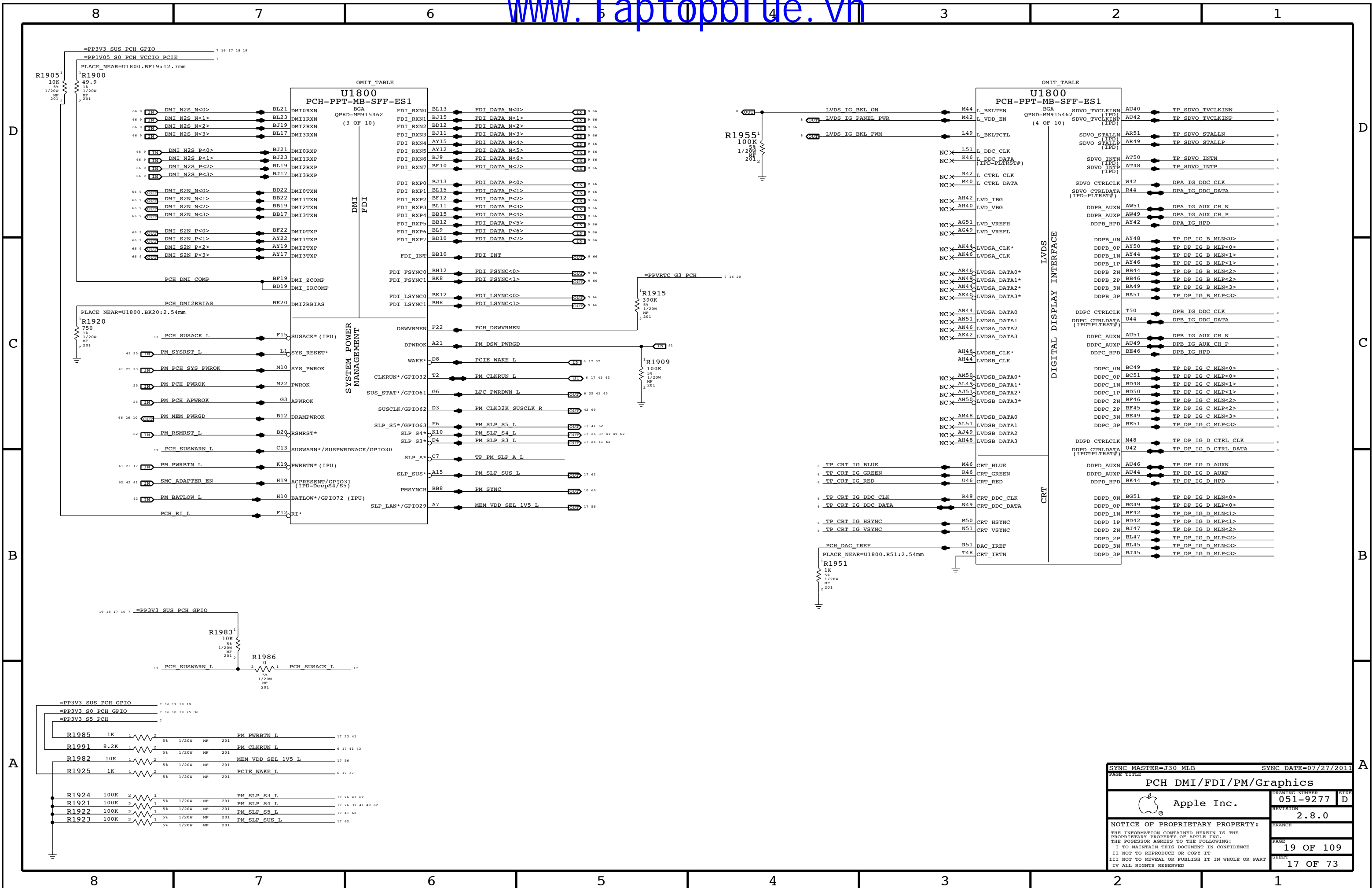
CPU VCCSA DECOUPLING

Intel recommendation (Section 6.6): 3x 1uF, 3x 10uF, 1x 330uF

PLACEMENT_NOTE (C1758-C1762):

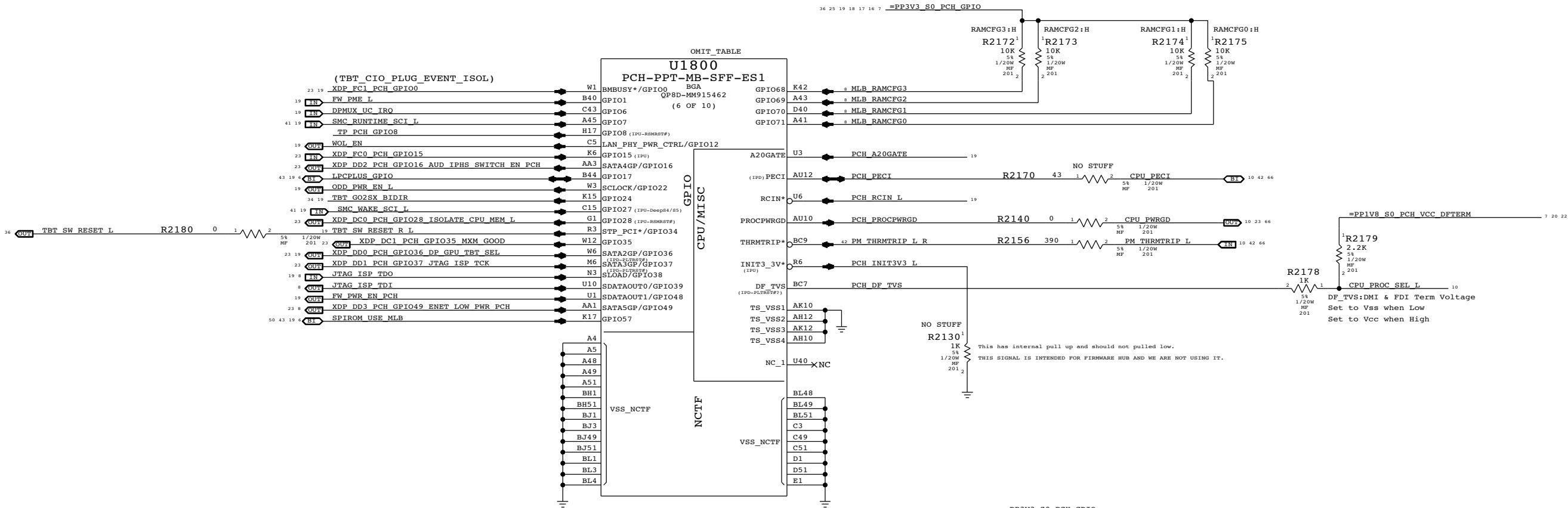




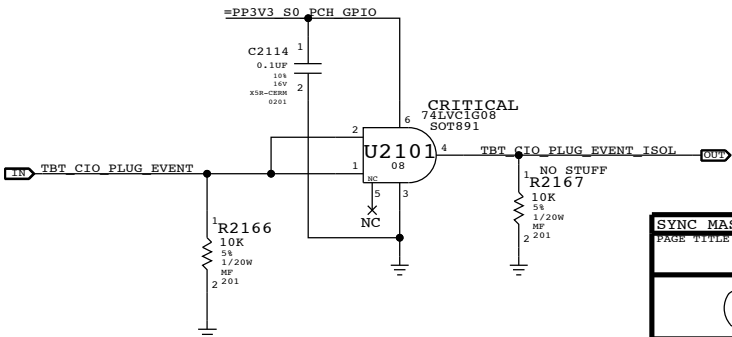
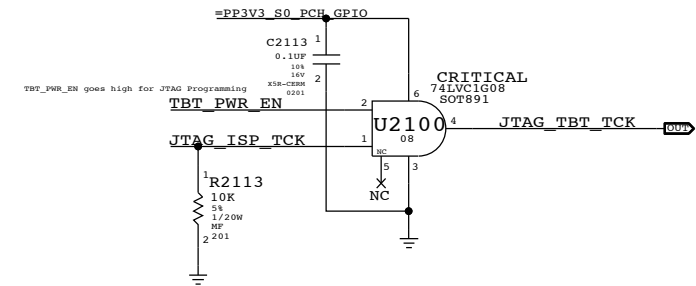
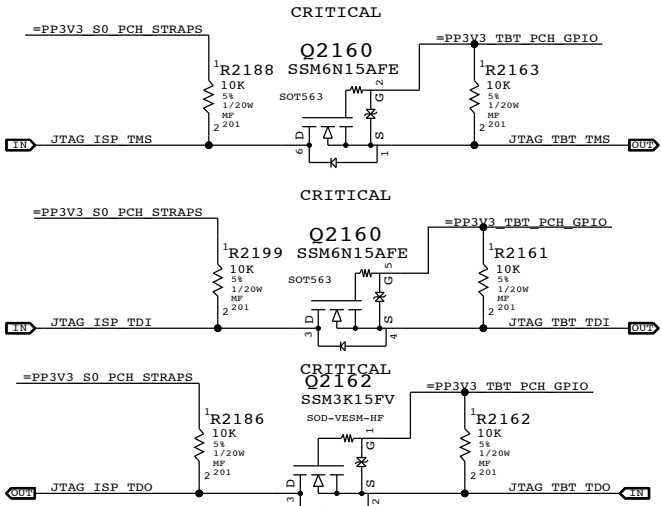
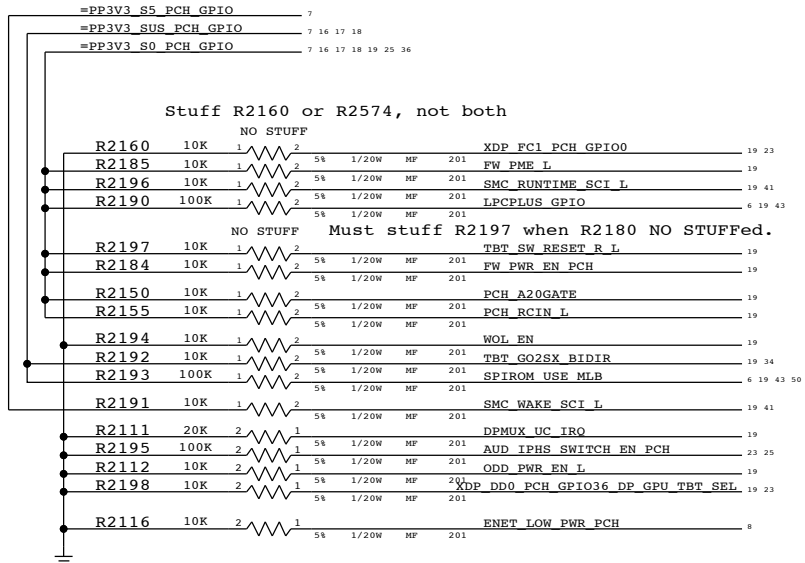


BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H, RAMCFG2:H, RAMCFG1:H, RAMCFG0:H

Systems with no chip-down memory should pull all 4 RAMCFG GPIOs high.
Systems with chip-down memory should add pull-downs on another page and set straps per software.

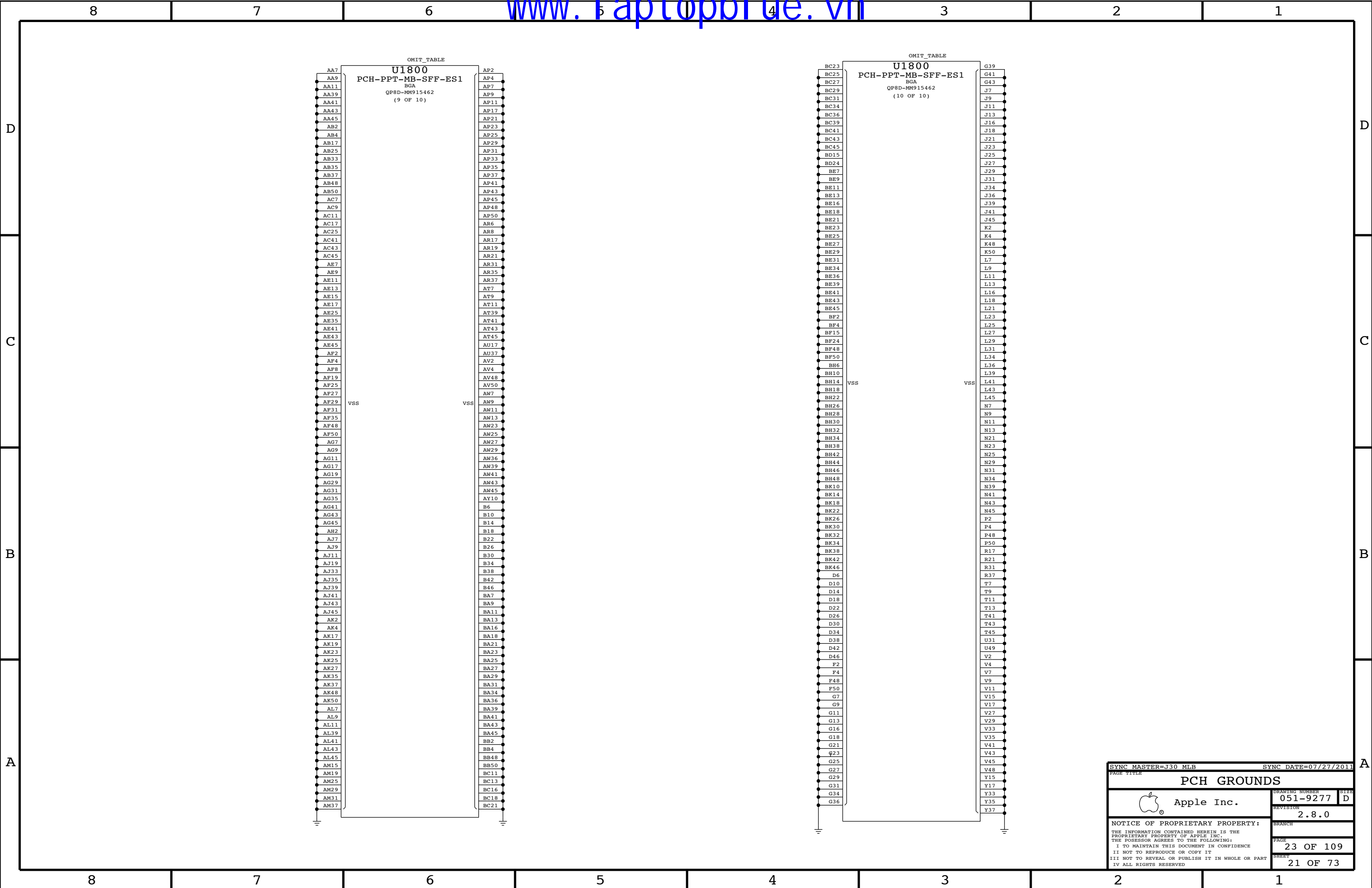


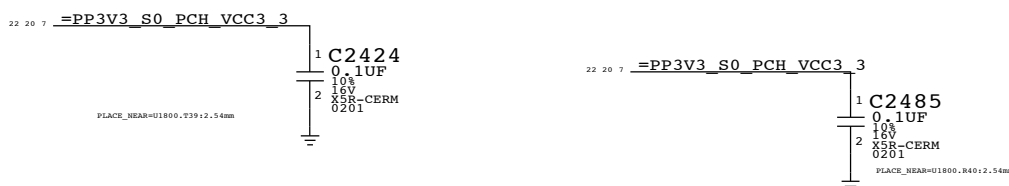
JTAG Isolation due to glitch in and out of sleep
NOTE: TCK from PCH is Push-Pull CMOS
NOTE: TMS/TDO from PCH is Open Drain
NOTE: TDO from CR is Push-Pull CMOS

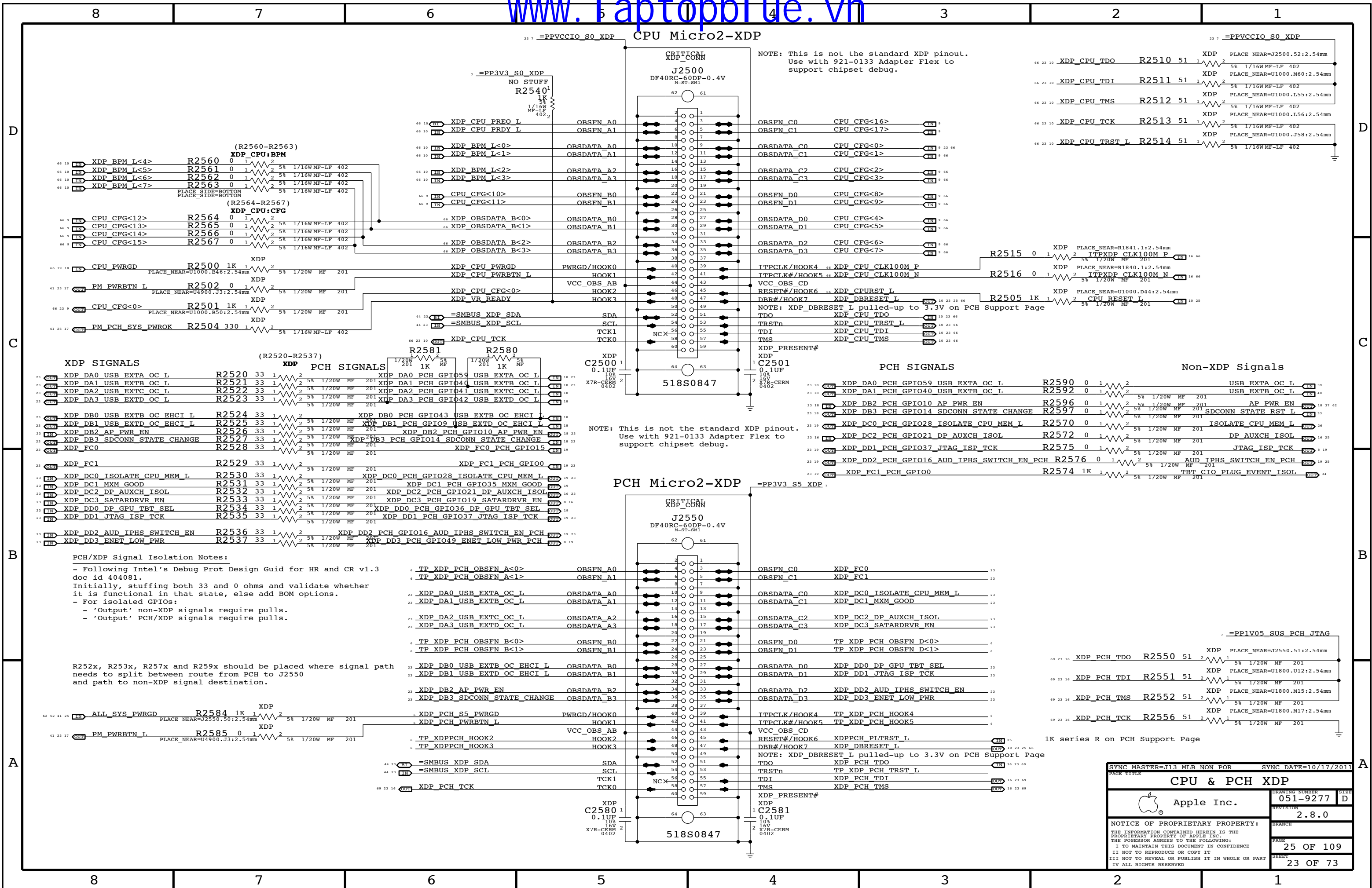


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		REVISION	2.8.0
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A



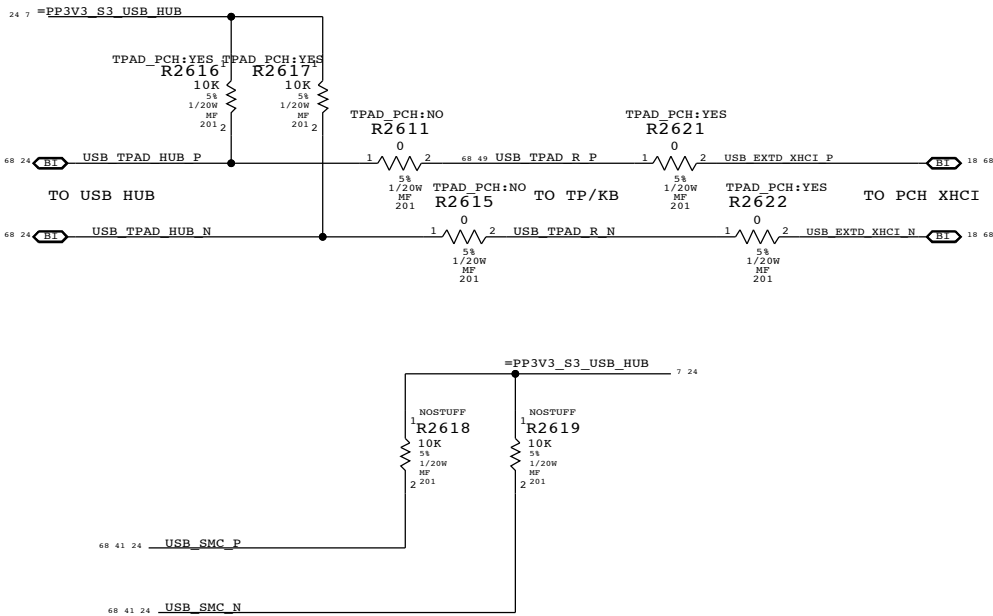
BOM GROUP	BOM OPTIONS
HUB_ALLREM	HUB_NONREM1_0,HUB_NONREMO_0
HUB_1NONREM	HUB_NONREM1_0,HUB_NONREMO_1
HUB_2NONREM	HUB_NONREM1_1,HUB_NONREMO_0
HUB_3NONREM	HUB_NONREM1_1,HUB_NONREMO_1

NON_REM1	NON_REMO	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

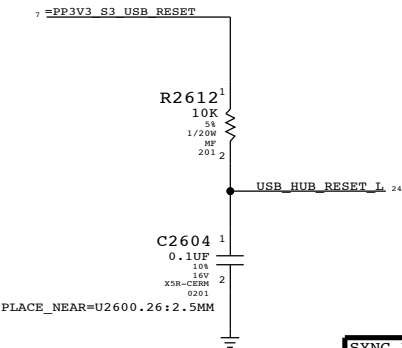
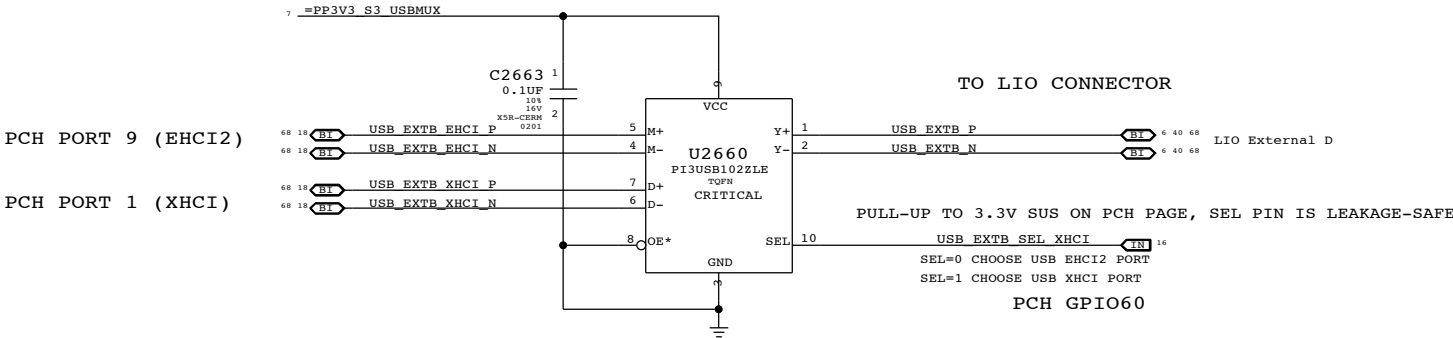
BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0983	1	IC,USB2512B,USB 2.0 HUB CNTRL,36-QFN	U2600	CRITICAL	USBHUB2512B
338S0923	1	IC,USB2513B,USB 2.0,HUB CNTRL,3PRT,46QFN	U2600	CRITICAL	USBHUB2513B
338S0824	1	IC,USB2514B,USB 2.0,HUB CNTRL,4PRT	U2600	CRITICAL	USBHUB2514B

TO CONNECT TP/KB TO PCH XHCI
NOSTUFF R2611 & R2615, STUFF R2621 & R2622,R2616 & R2617

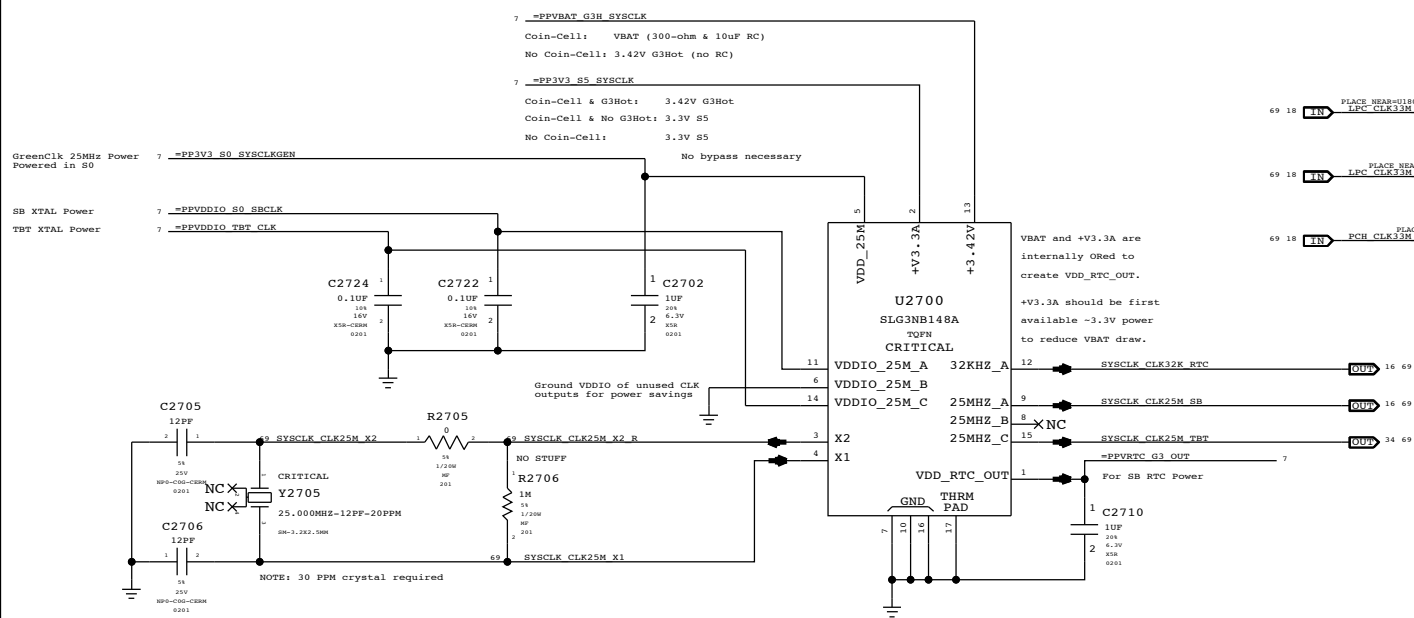


USB XHCI/EHCI2 PORT MUX FOR EXT B

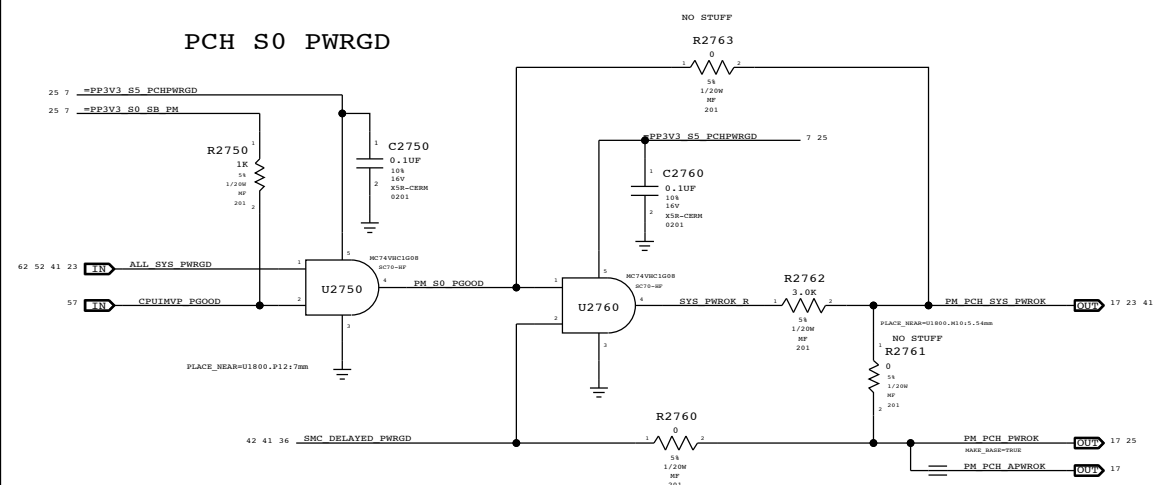


PAGE TITLE		SYNC MASTER=J13 MLB NON POR		SYNC DATE=11/10/2011	
USB HUB & MUX		DRAWING NUMBER		SIZE	
Apple Inc.		051-9277		D	
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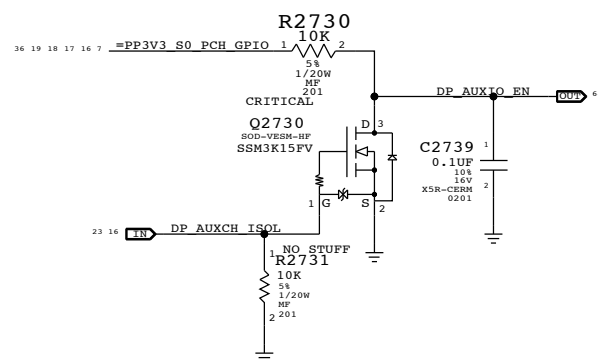
System RTC Power Source & 32kHz / 25MHz Clock Generator



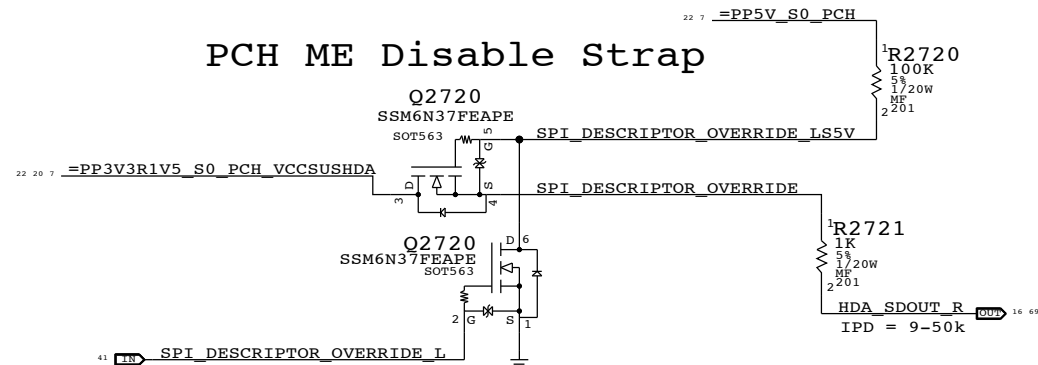
PCH S0 PWRGD



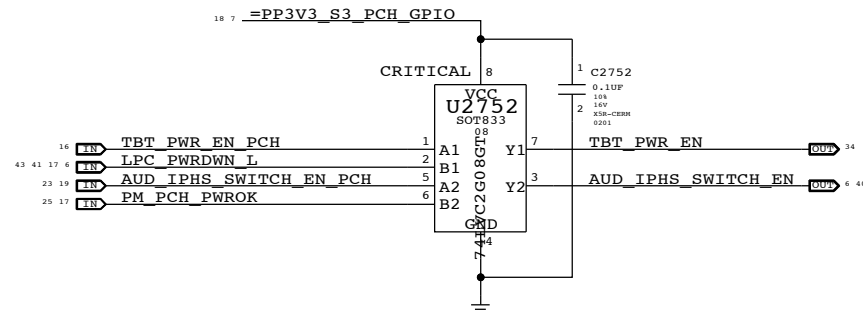
DP AUXIO EN Inversion



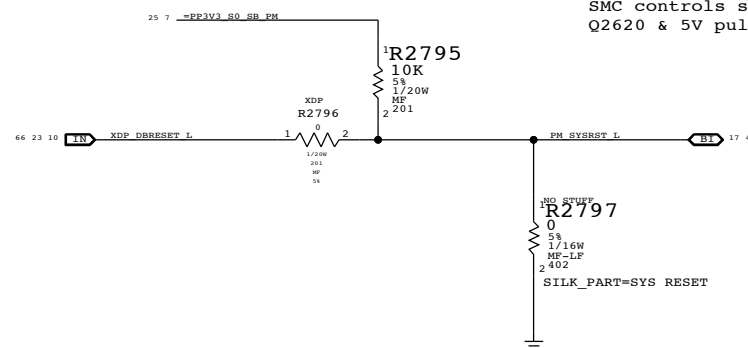
PCH ME Disable Strap




GPIO Glitch Prevention



PCH Reset Button



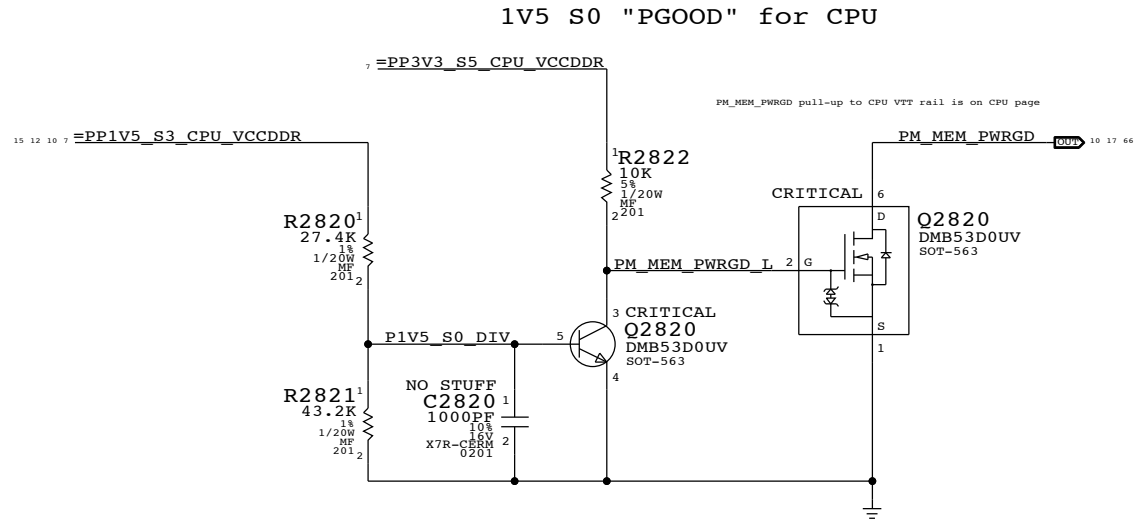
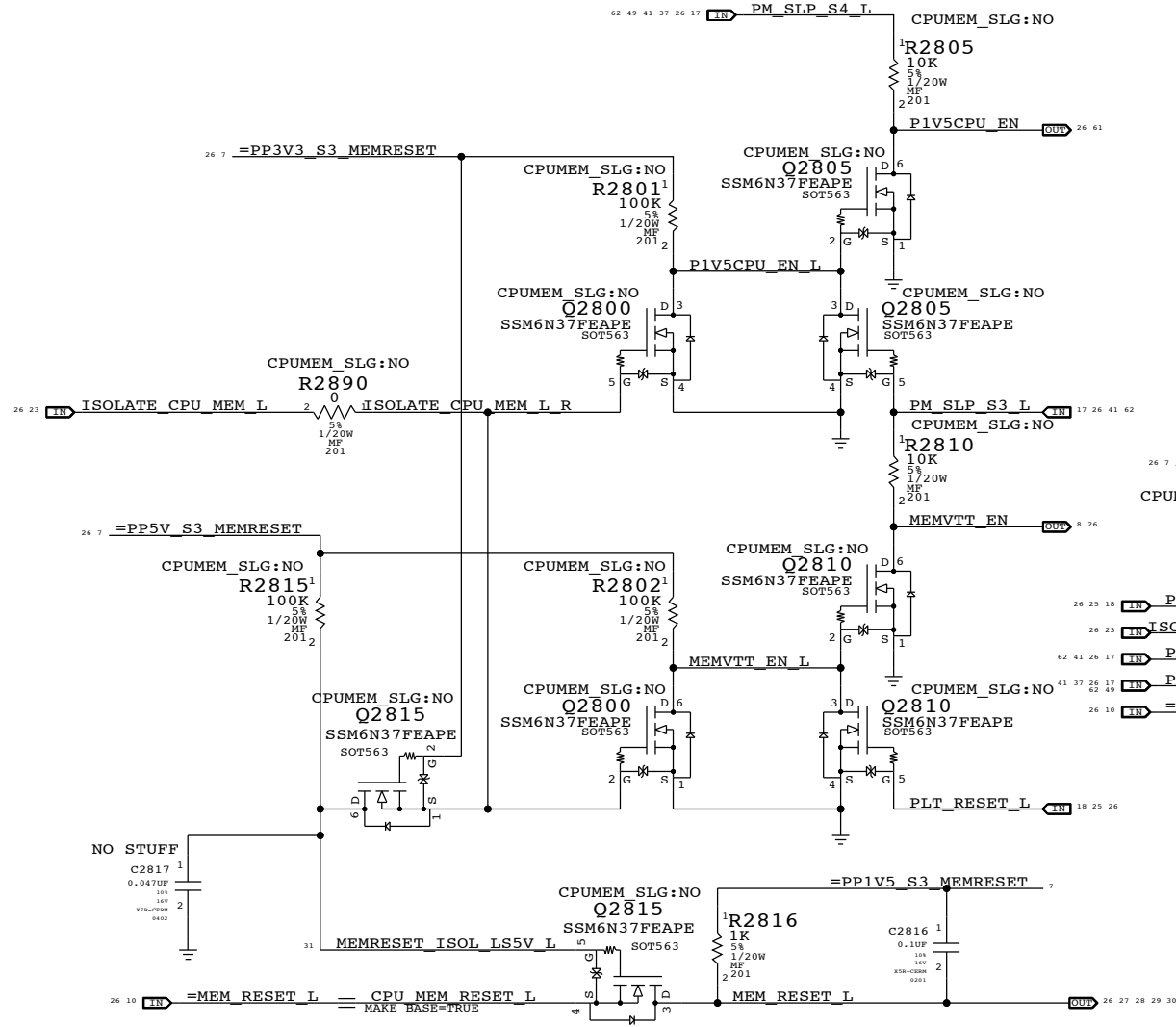
PCH uses HDA_SDO as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of strap setting. Q2620 & 5V pull-up allows circuit to work regardless of HDA voltage.

DATE: 04/27/2011 08:54 PRICE TITLE		ESTD: 04/27/2011 08:54	
Clock (CK505) and Chipset Support			
		DRAWING NUMBER 051-9277	
Apple Inc.		SIZE D	
		REVISION 2.8.0	
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The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the S0-DIMMs when necessary.

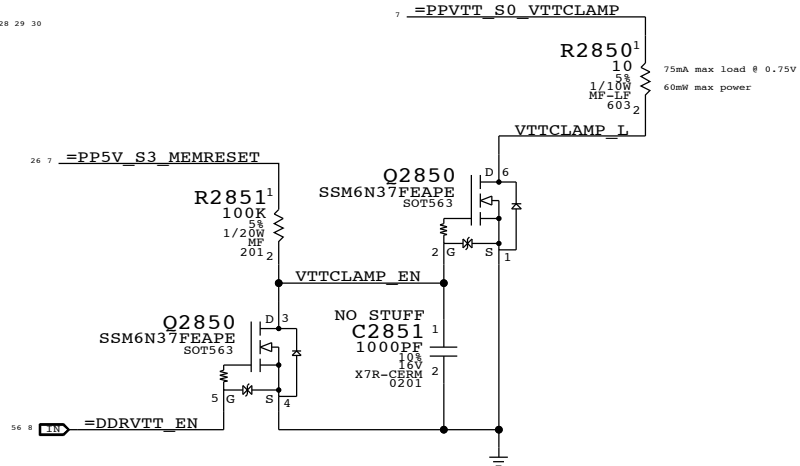
ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L



MEMVTT Clamp

Ensures CKE signals are held low in S3



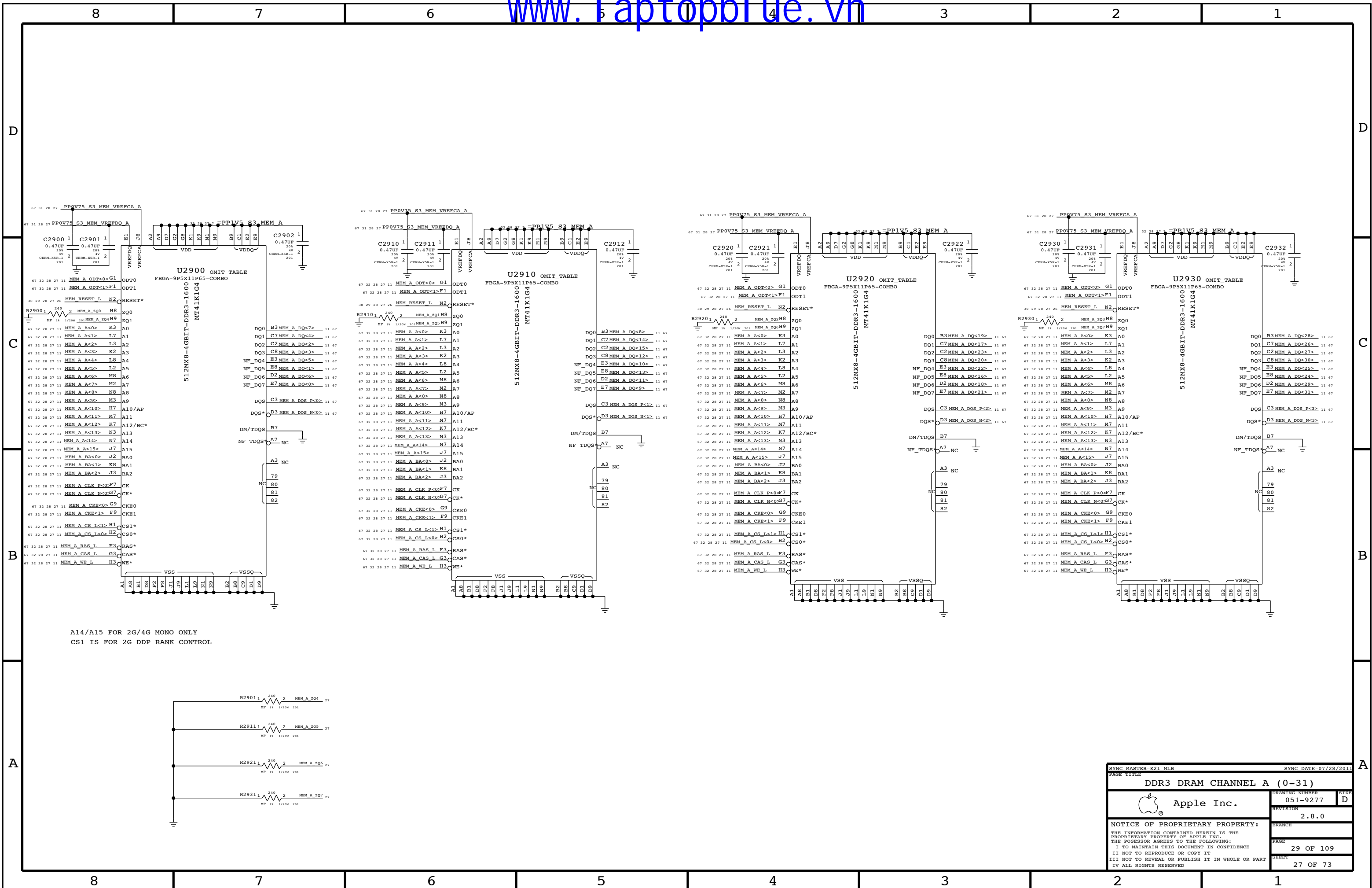
Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPUMEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	CPUMEM_RESET_L	1	1
1	0	1	1	1	1	1	1	1
to	2	0	0	1	1	0	0	1
3	0	0	0	1	X	0	0	0
S3	4	0	0	1	X	0	0	1
5	0	1	1	1	0 (*)	1	1	1
to	6	0	1	1	1	1	1	1
S0	7	1	1	1	1	CPUMEM_RESET_L	1	1

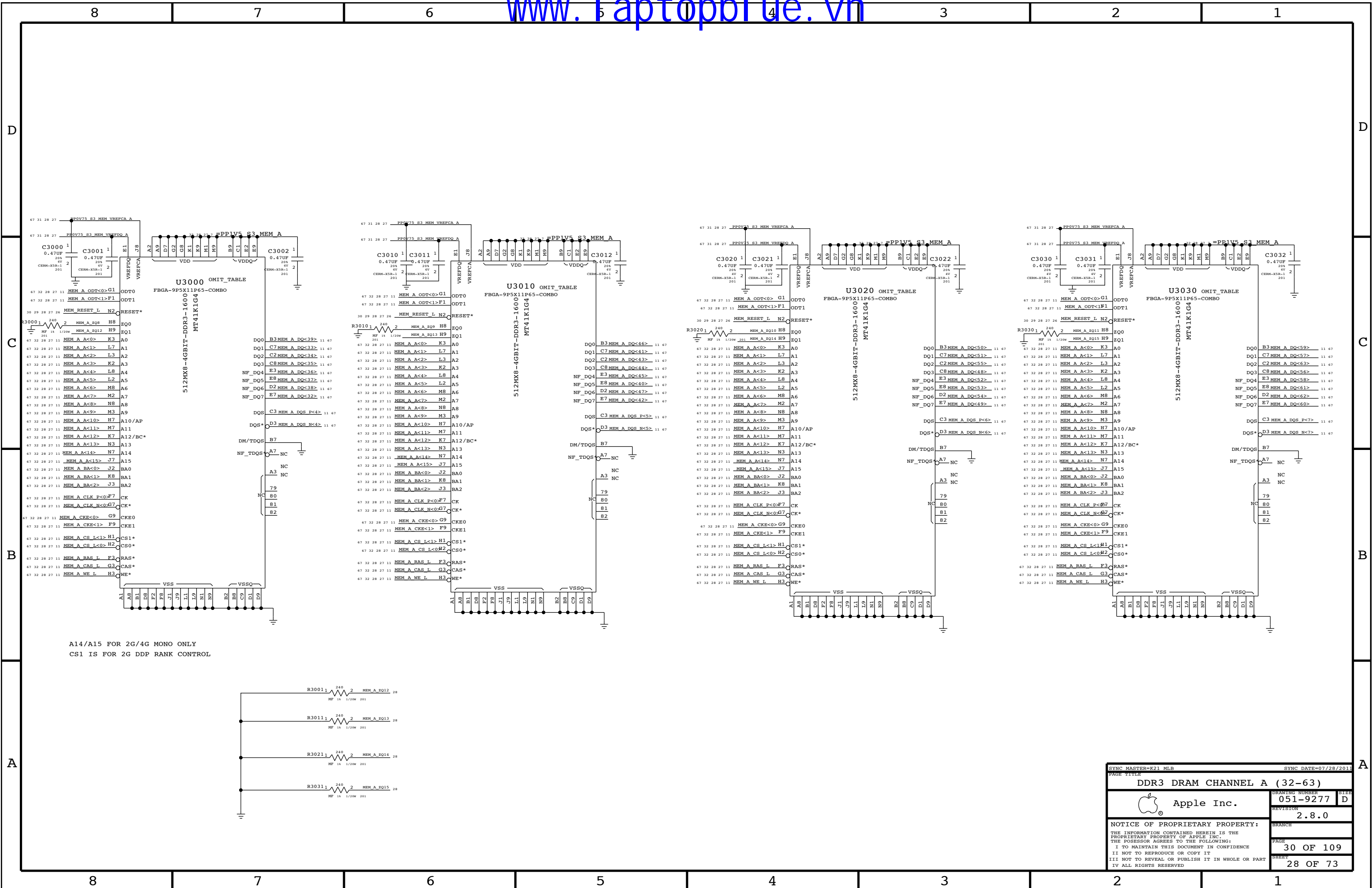
(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

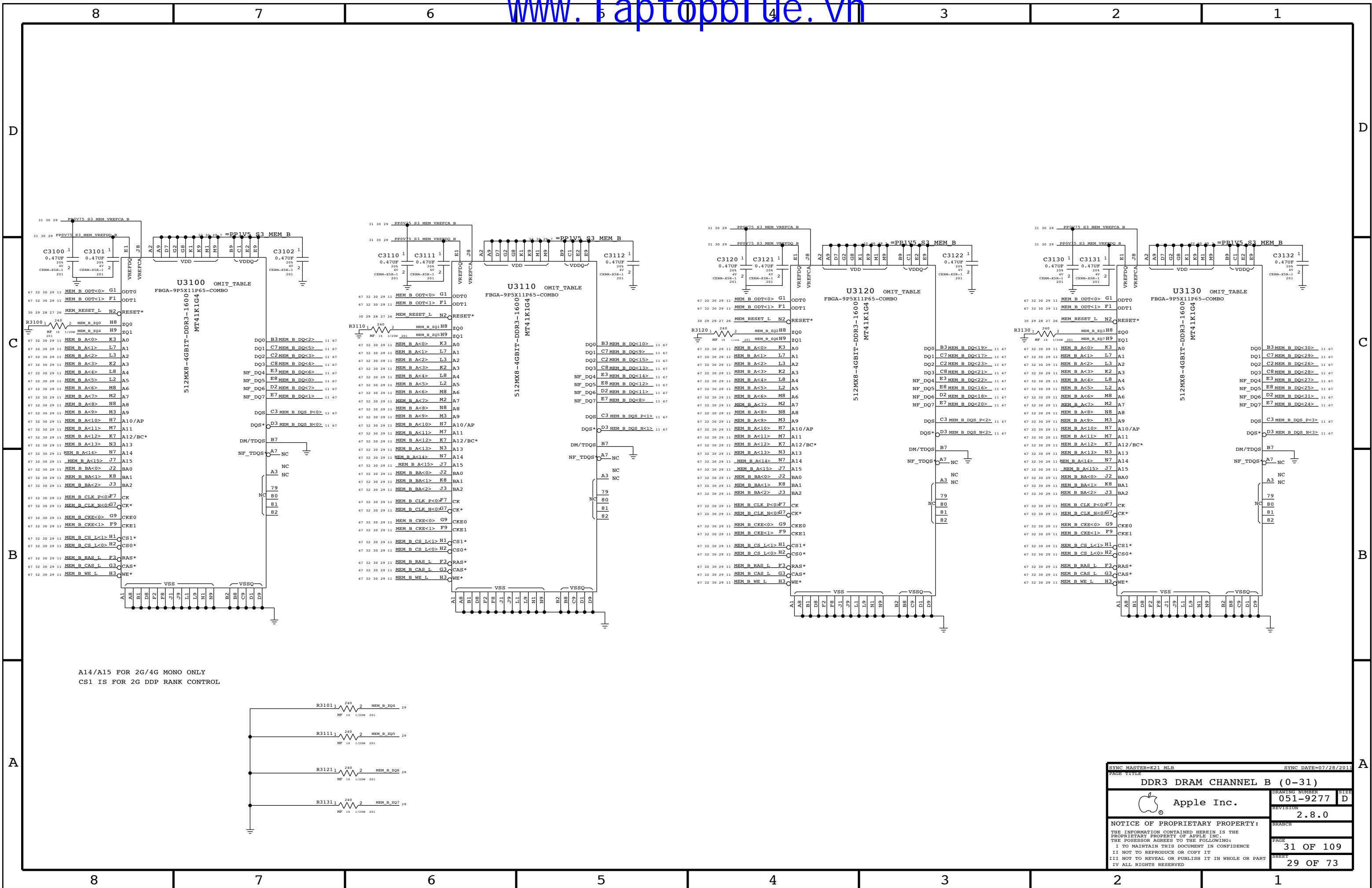
NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

CPU Memory S3 Support		DRAWING NUMBER		SIZE
Apple Inc.		051-9277		D
REVISION		2.8.0		
BRANCH				
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D

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C

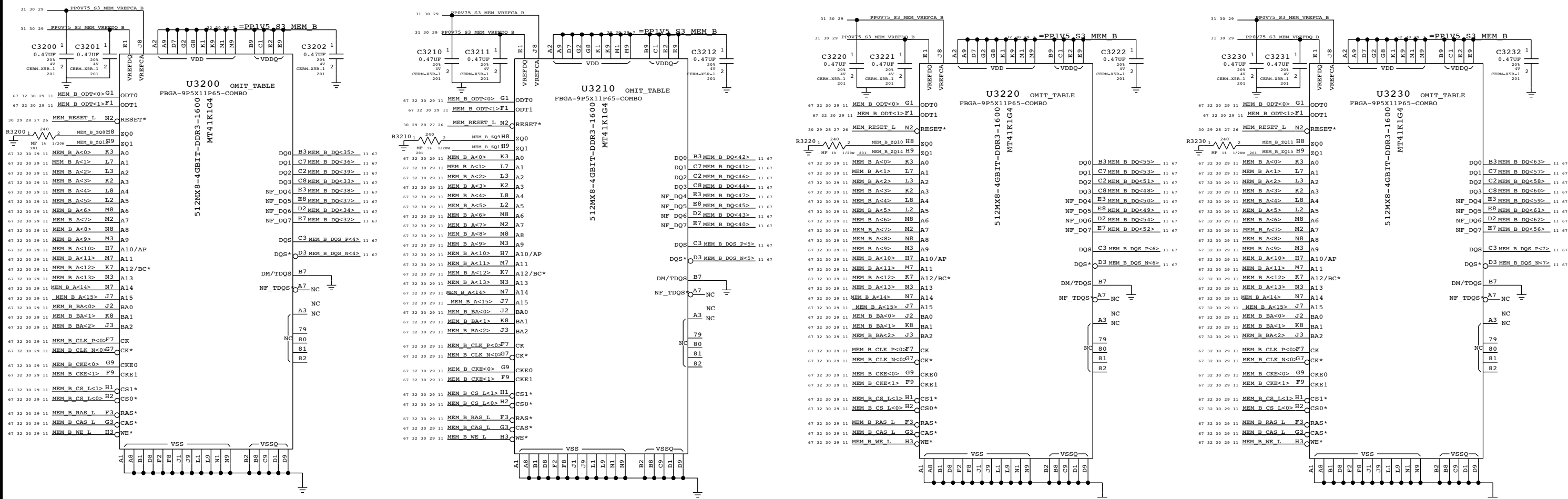
C

B

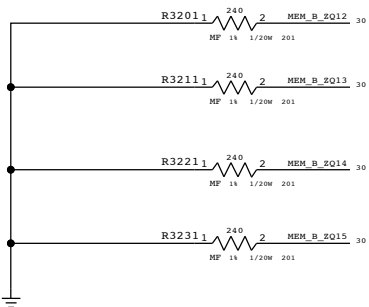
B


A

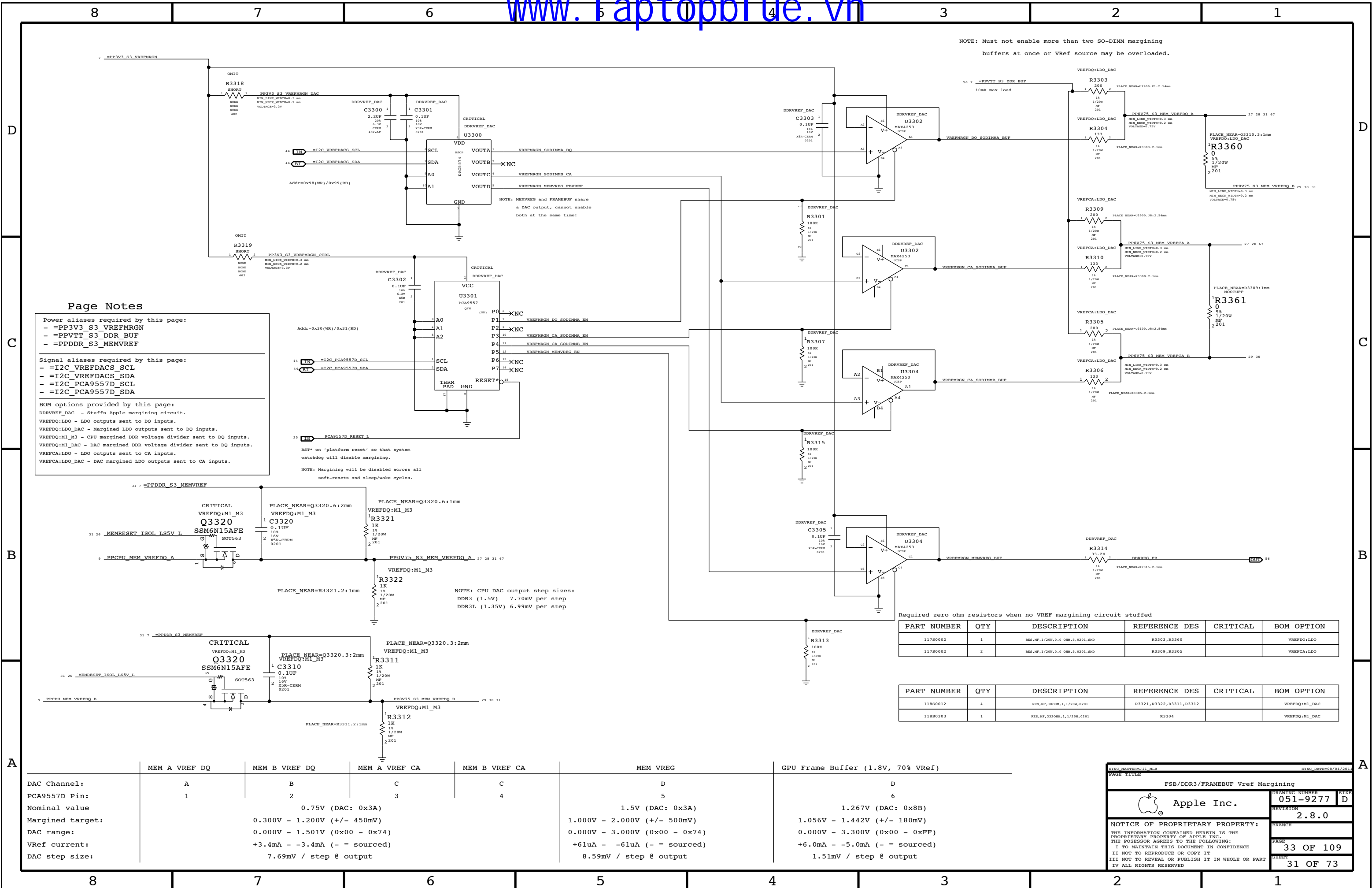
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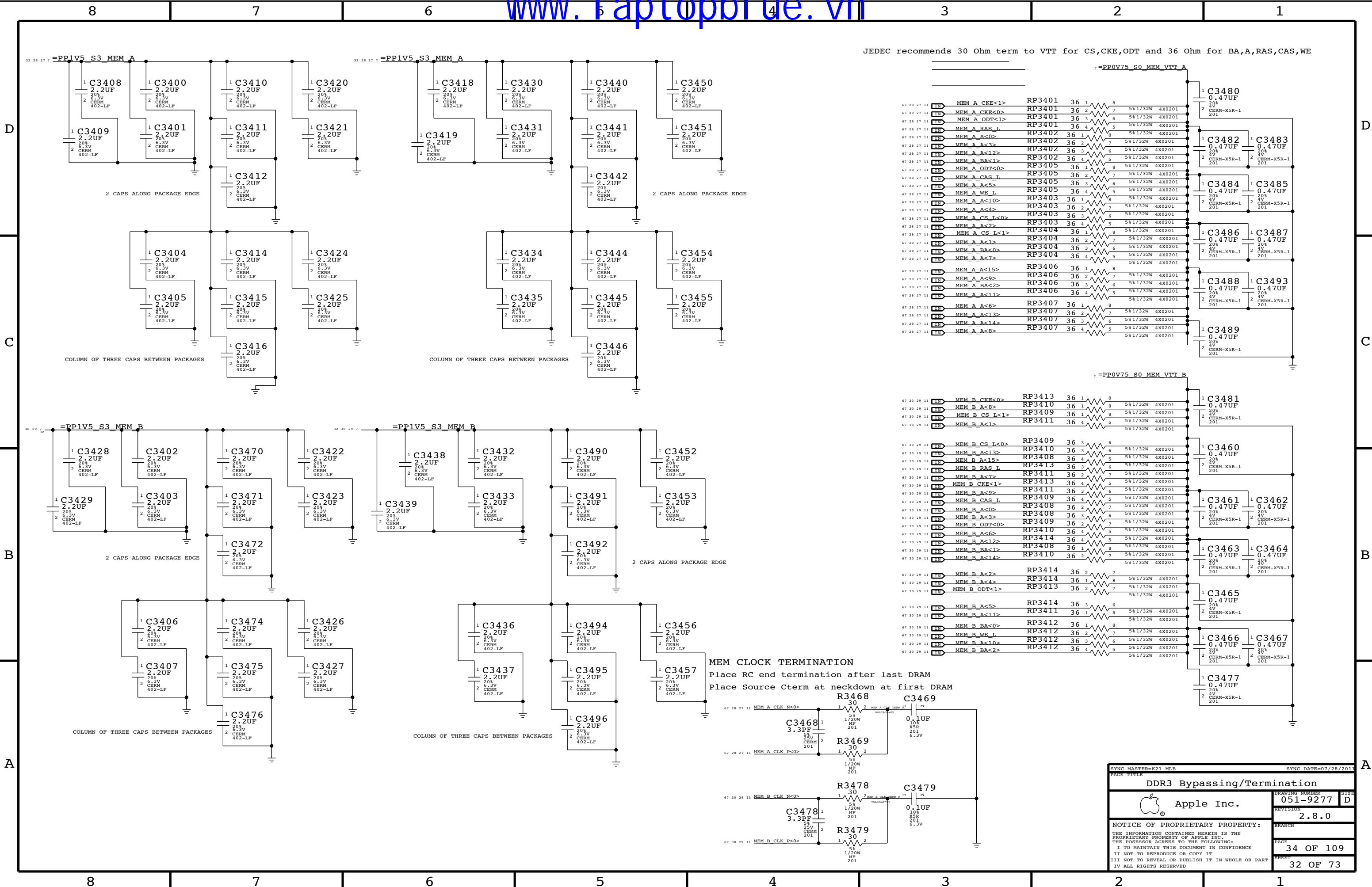


A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL



SYNC MASTER=K21 M2B		SYNC DATE=07/28/2011	
PAGE TITLE			
DDR3 DRAM CHANNEL B		(32-63)	
	Apple Inc.	DRAWING NUMBER	051-9277
		SIZE	D
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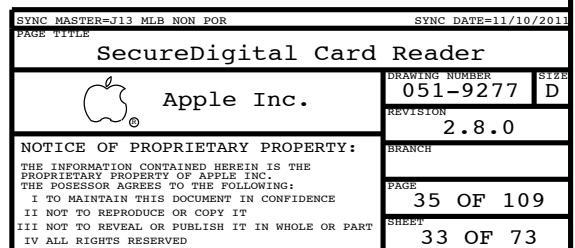


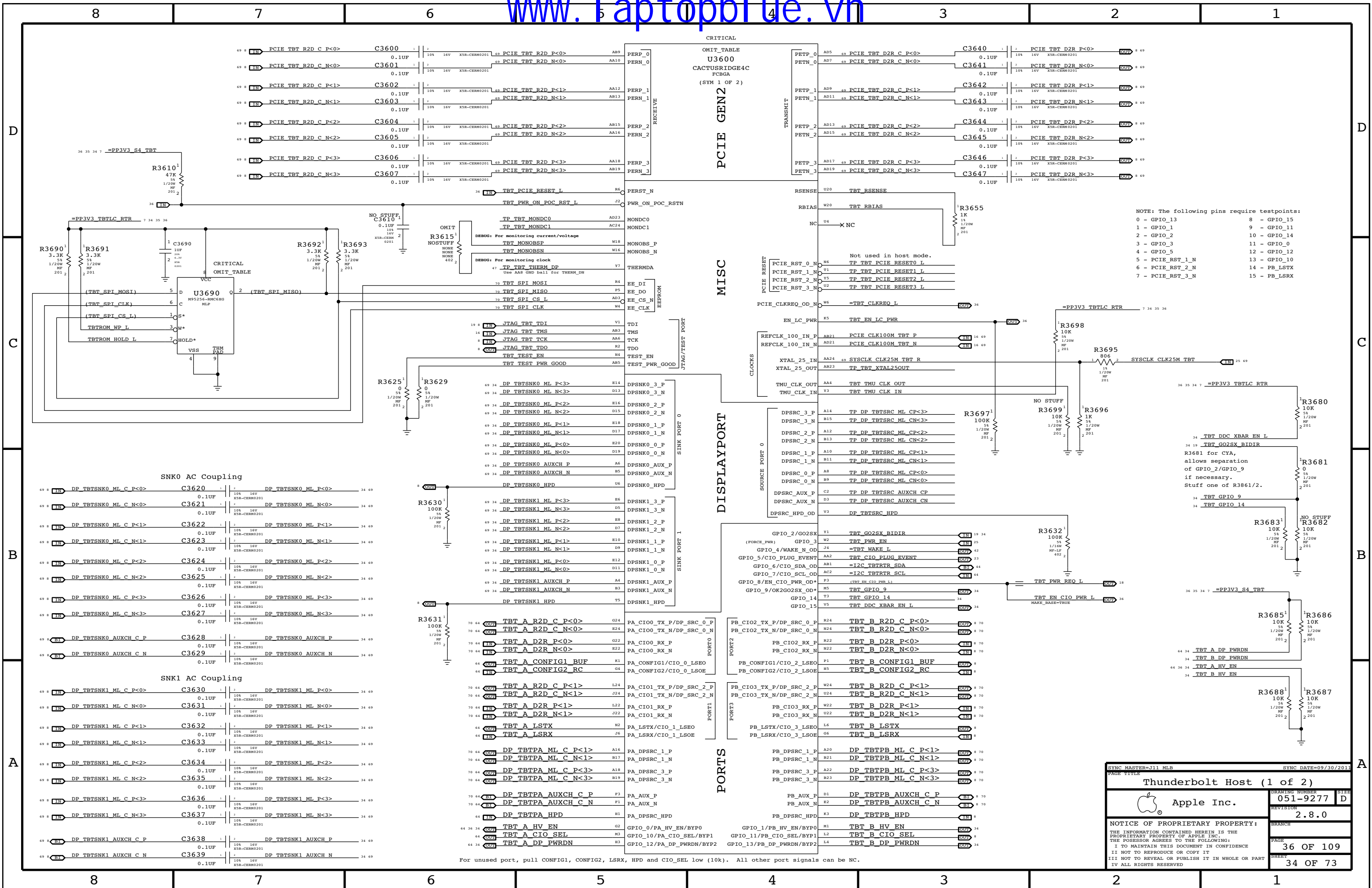




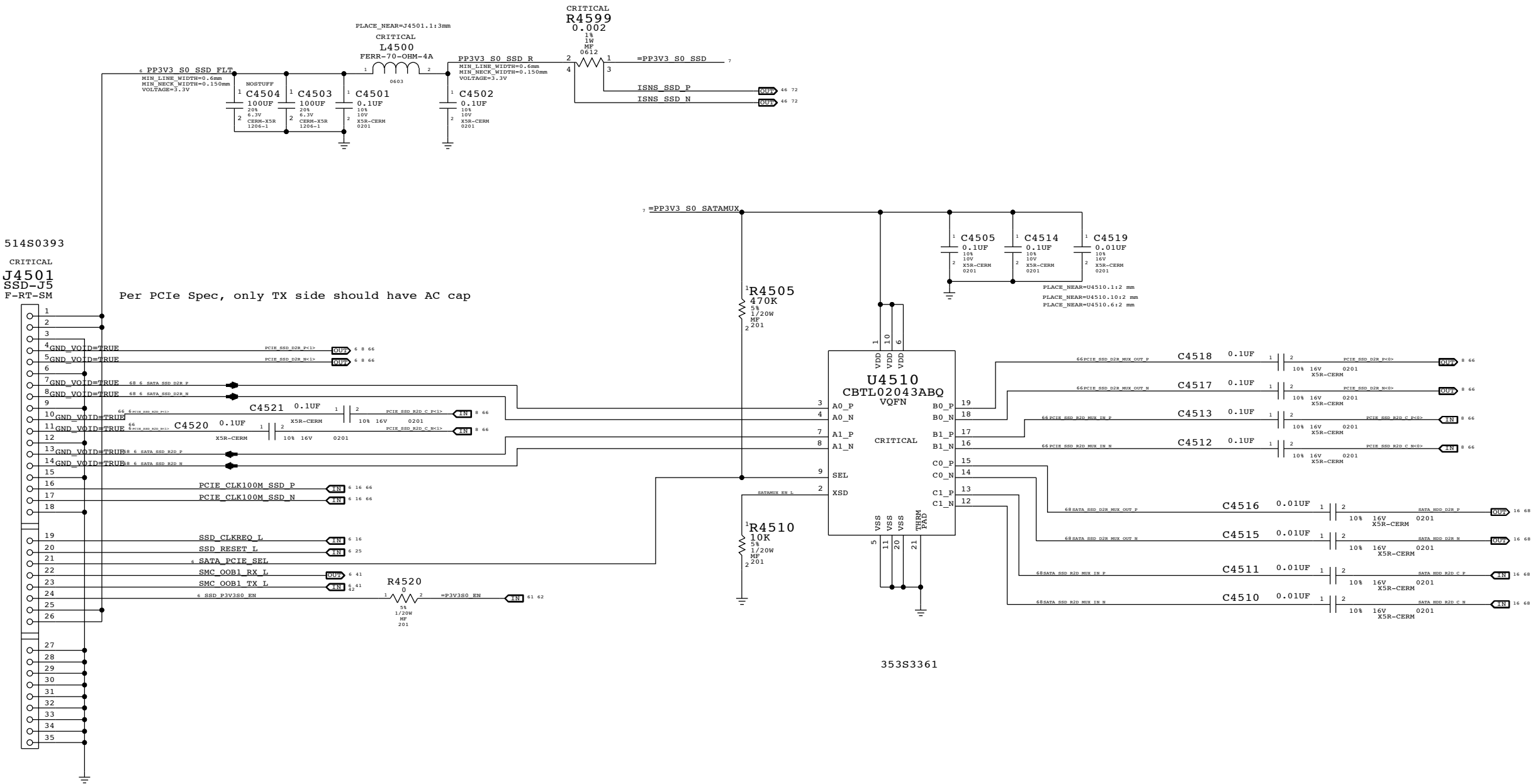
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A






A

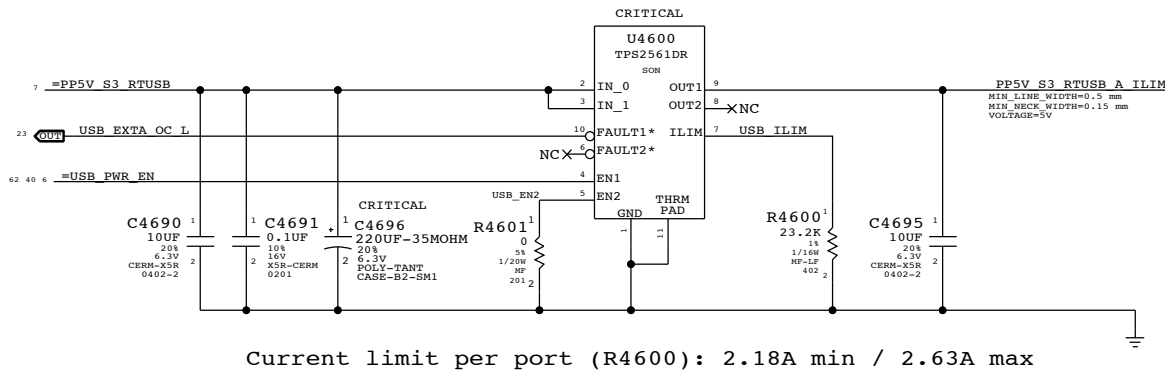


PCIE/SATA GUMSTICK2 CONNECTOR

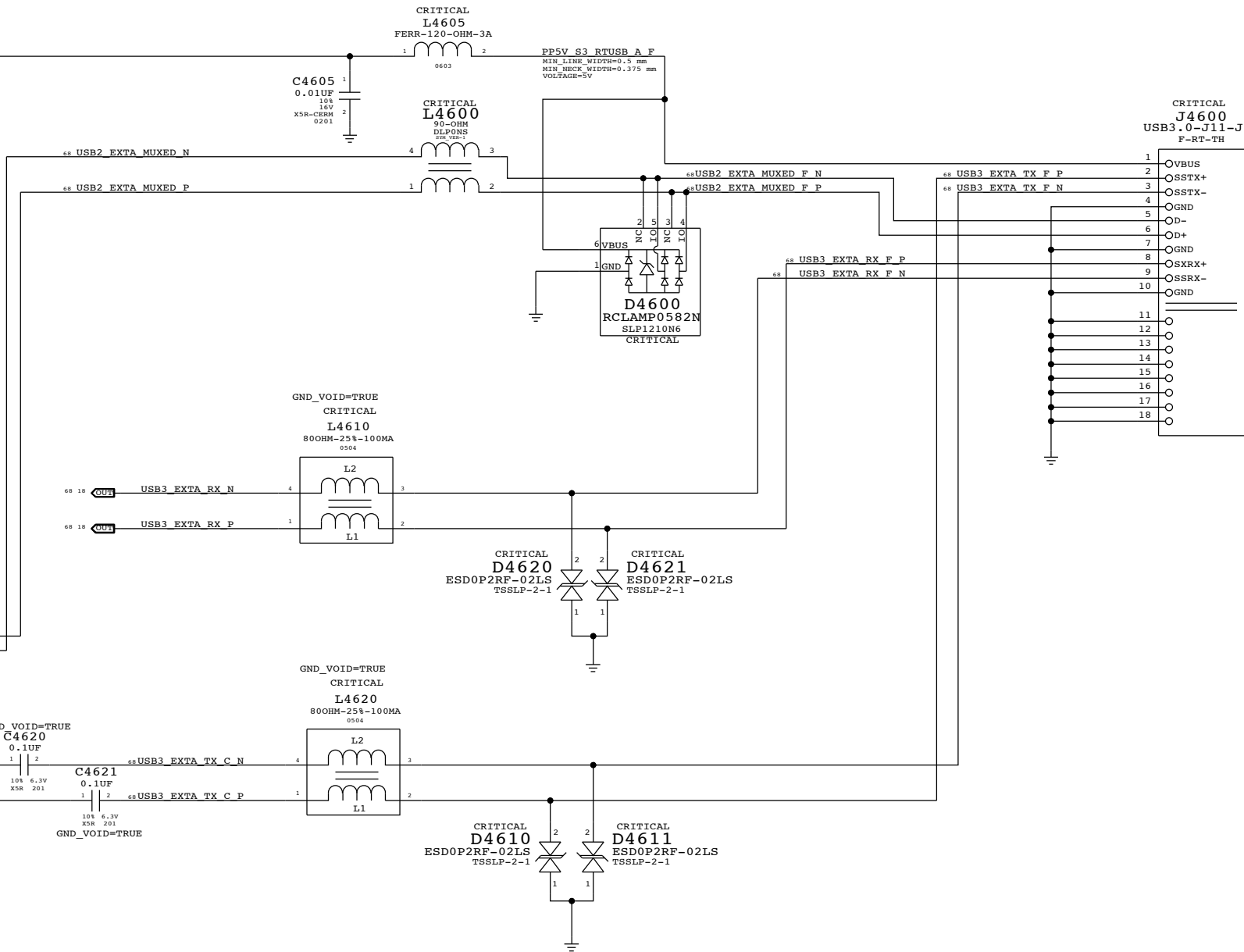
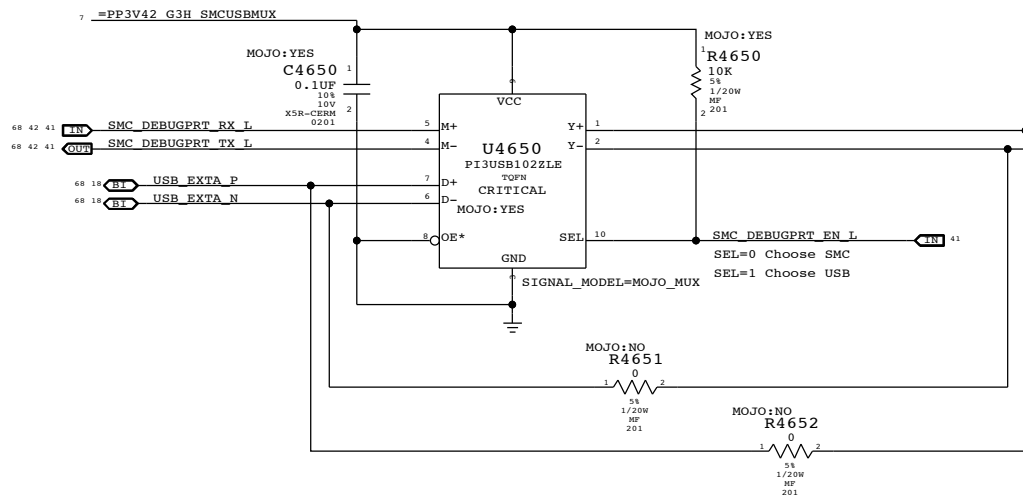
SYNC MASTER=J13 MLB NON POR		SYNC DATE=10/17/2011	
PAGE TITLE			
SSD CONNECTOR			
 Apple Inc.		DRAWING NUMBER	051-9277
		REVISION	2.8.0
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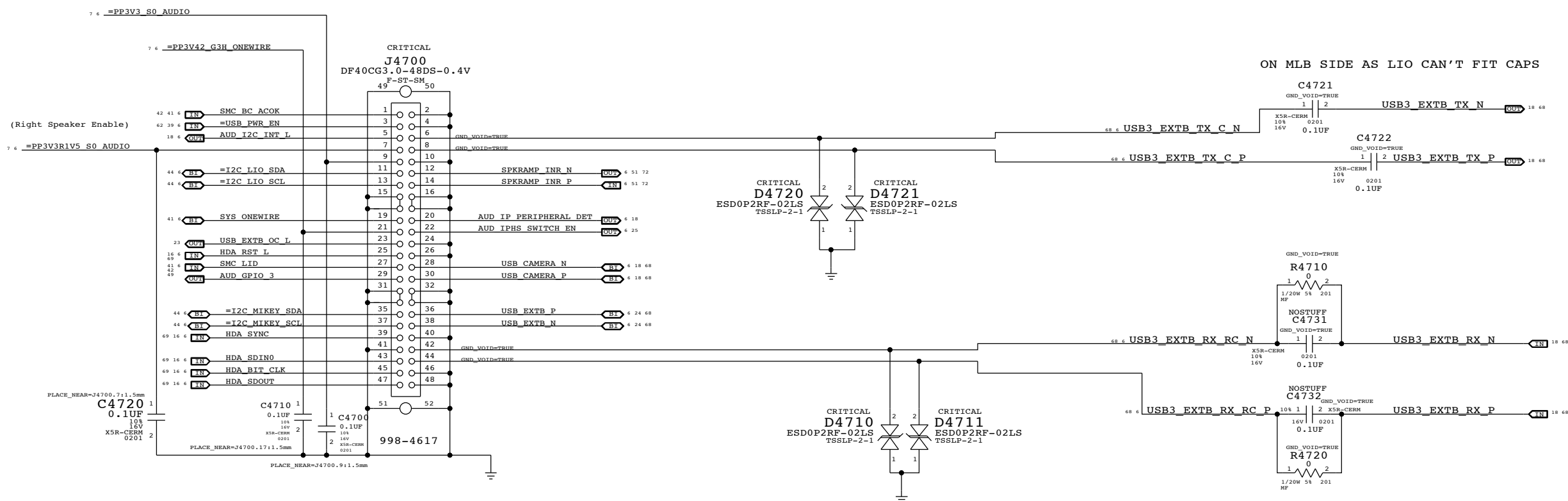
Right USB Port A

USB Port Power Switch



Mojo SMC Debug Mux





D

D

C

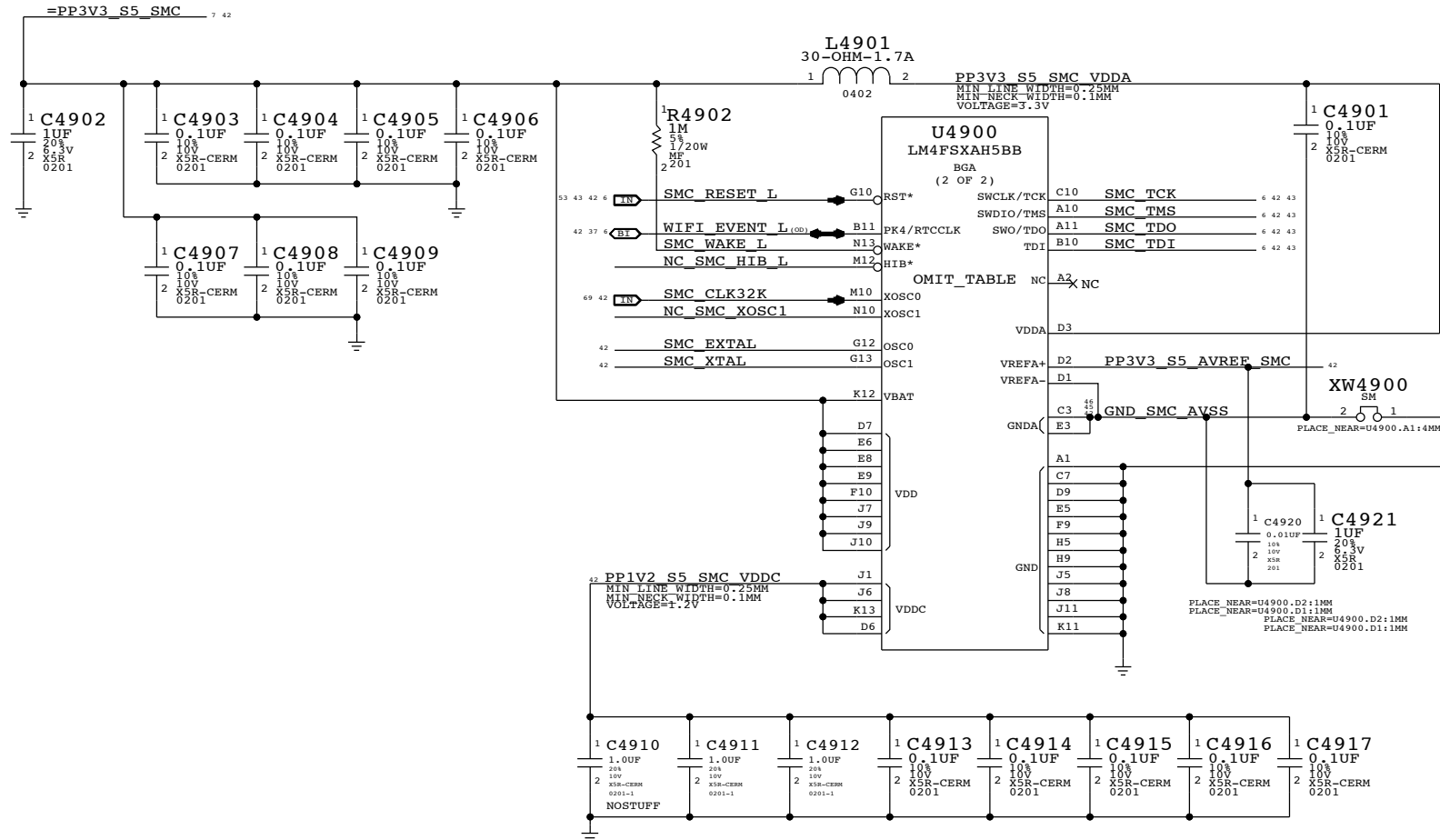
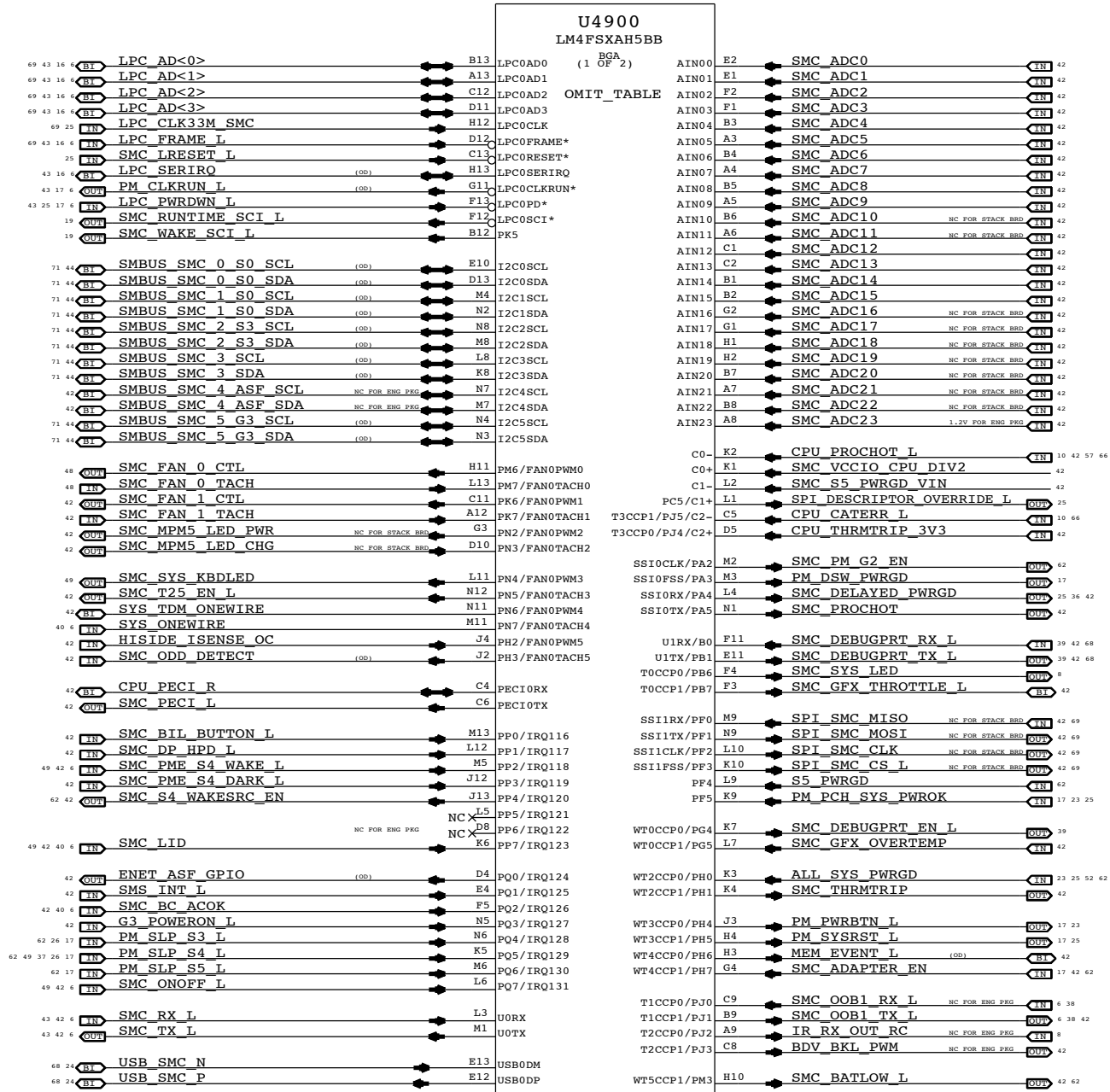
C

B

B


A

A

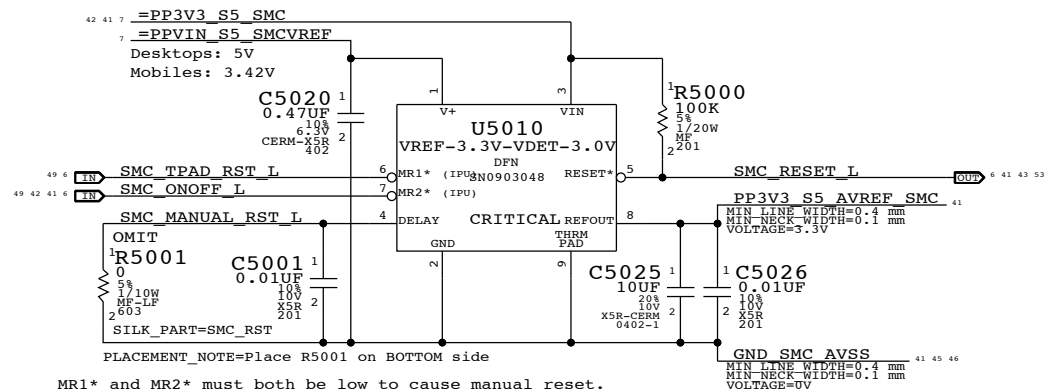


NOTE:
SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

NOTE:
Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.

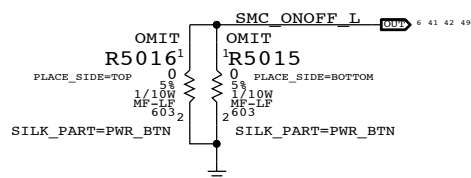
SYNC MASTER=J13 MLB NON POR		SYNC DATE=10/17/2013	
PAGE TITLE			
SMC			
 Apple Inc.		DRAWING NUMBER	051-9277
		REVISION	2.8.0
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SMC Reset "Button", Supervisor & AVREF Supply



MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.
NOTE: Internal pull-ups are to VIN, not V+.

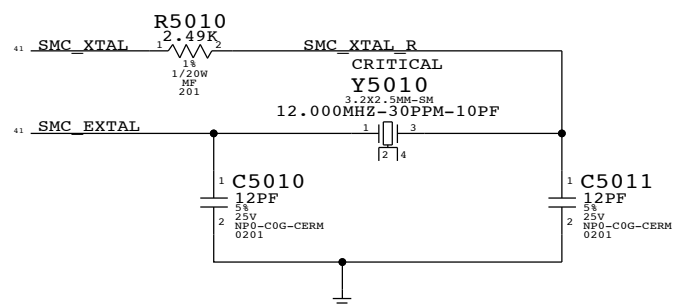
Debug Power "Buttons"



SMC Crystal Circuit

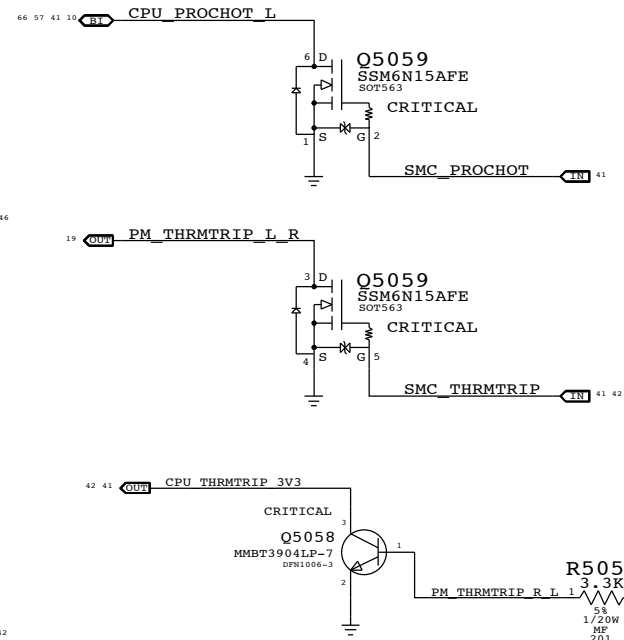
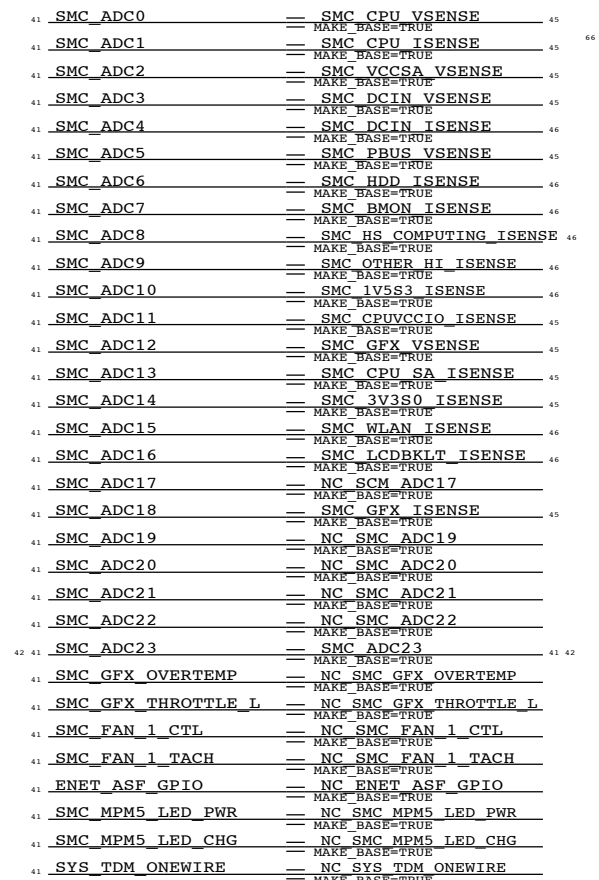
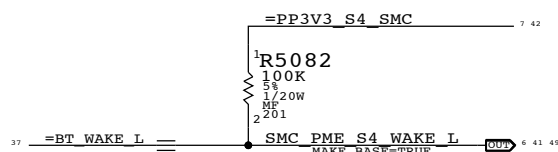
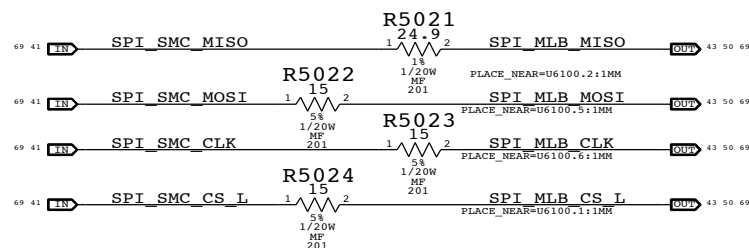
SMC USB Clock require these crystal values:5,6,8,10,12,16,18,20,24,25 MHz

Note:
ADC10 and ADC11 are shared
with comparators on Stack Board.



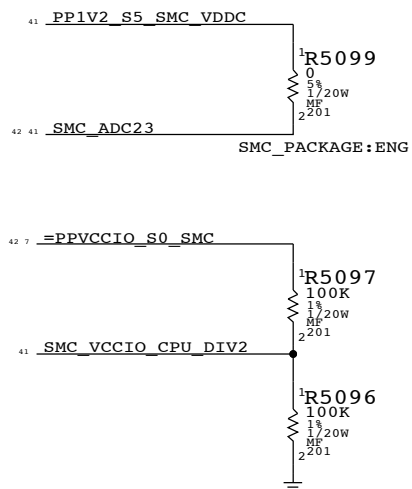
SMC12 SPI Support

Series resistors are no stuffed until the topology of 2 SPI Masters are verified.

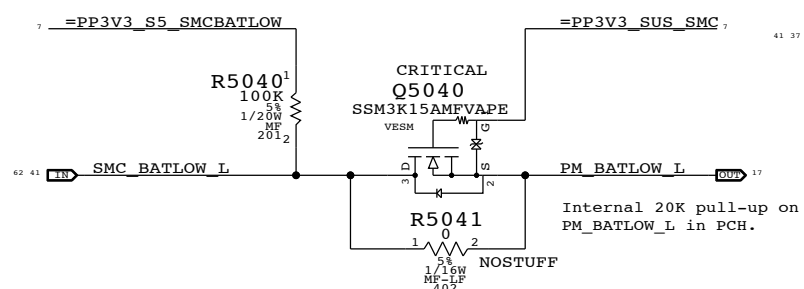


SMC12 Eng Pkg Support

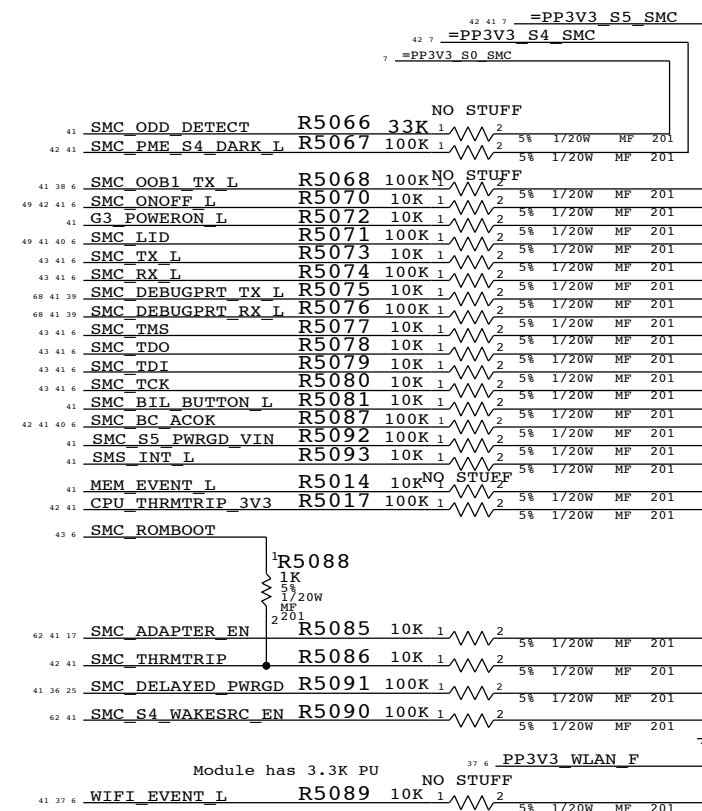
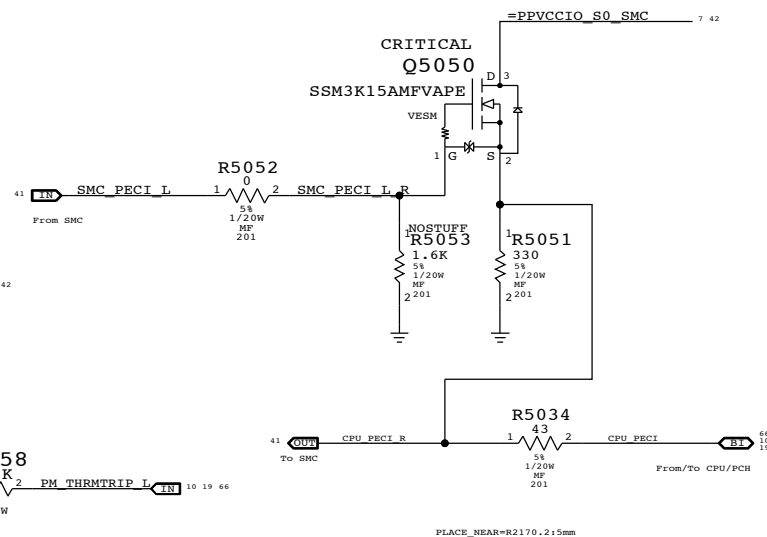
Eng Package requires 1.2V ON SMC ADC23 pin.





BATLOW# Isolation

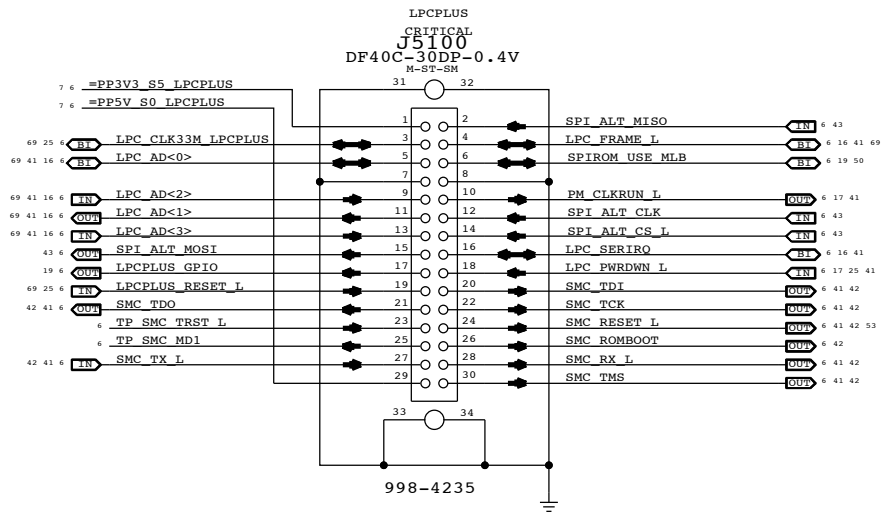


SMC12 PECE Support

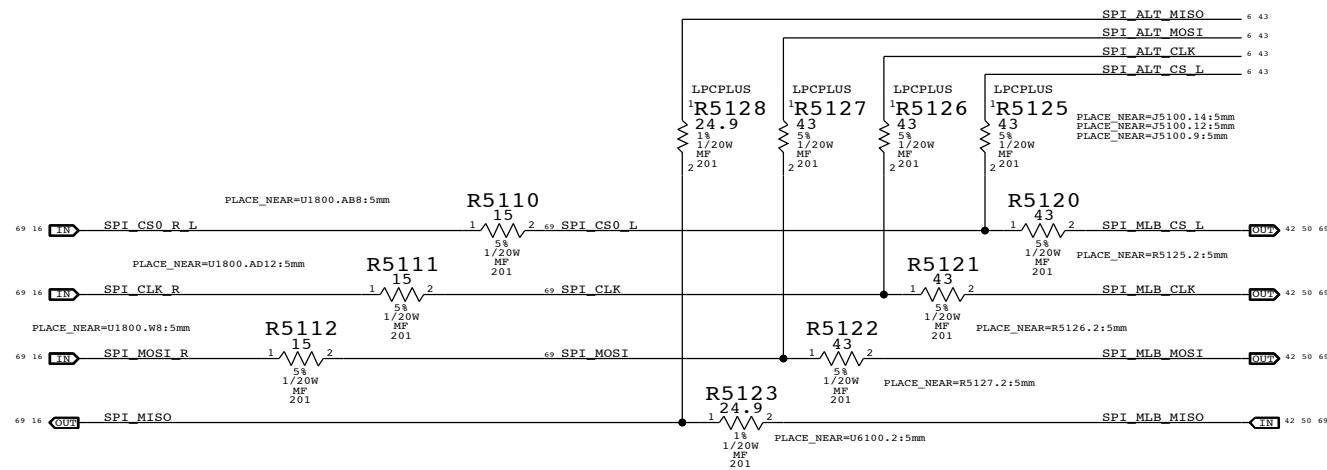


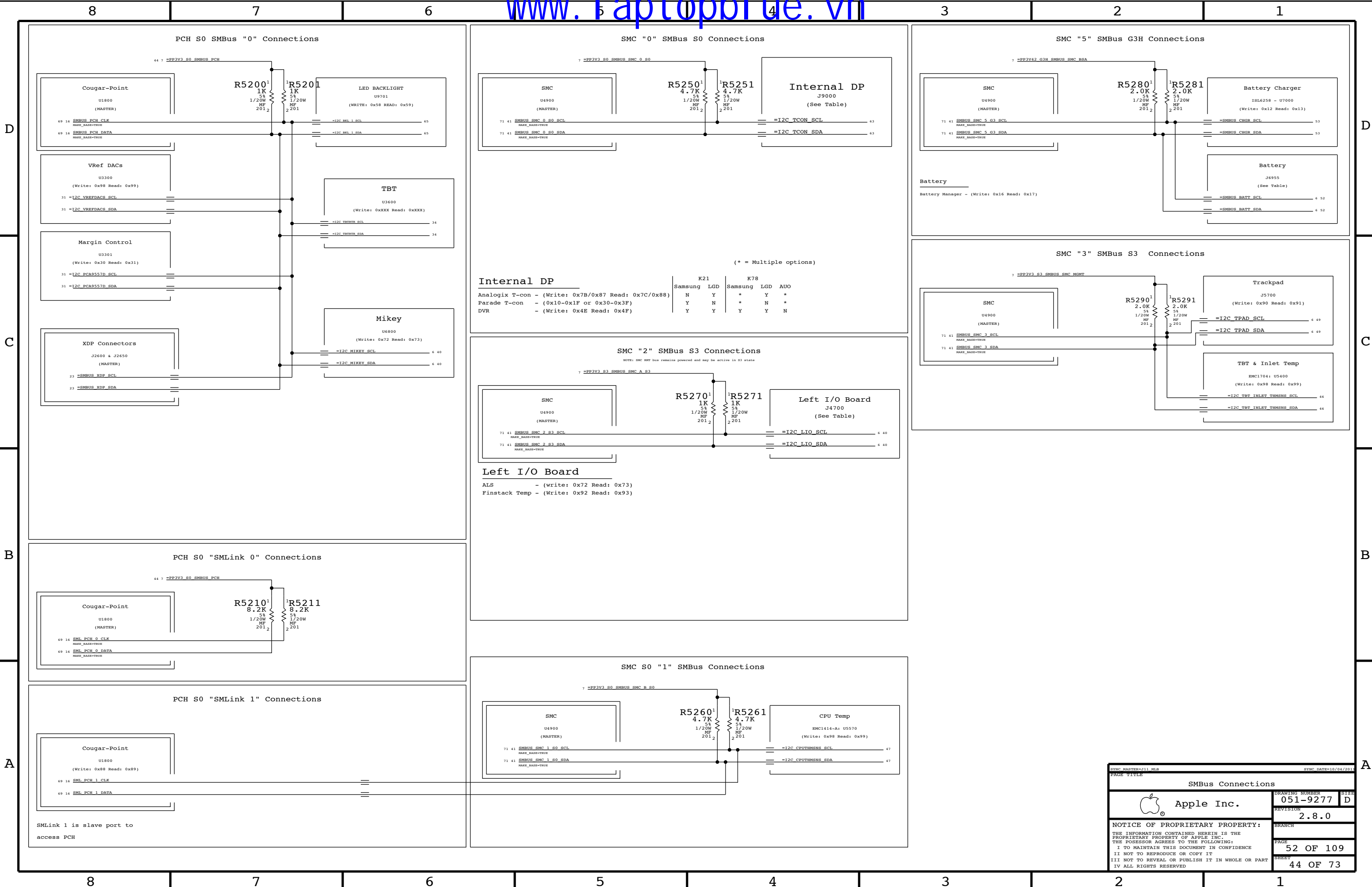
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 <h2 style="margin: 0;">Apple Inc.</h2>		DRAWING NUMBER	051-9277
		REVISION	2.8.0
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LPC+SPI Connector

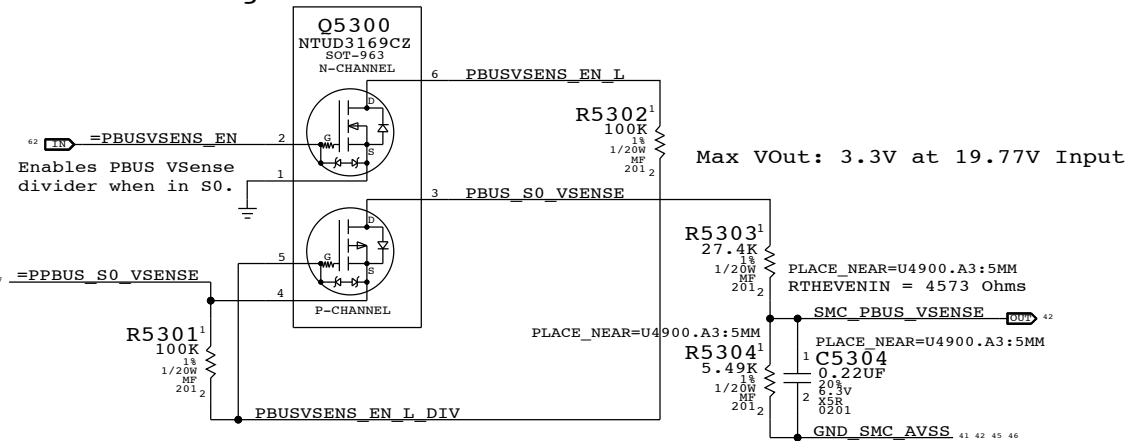


SPI Bus Series Termination

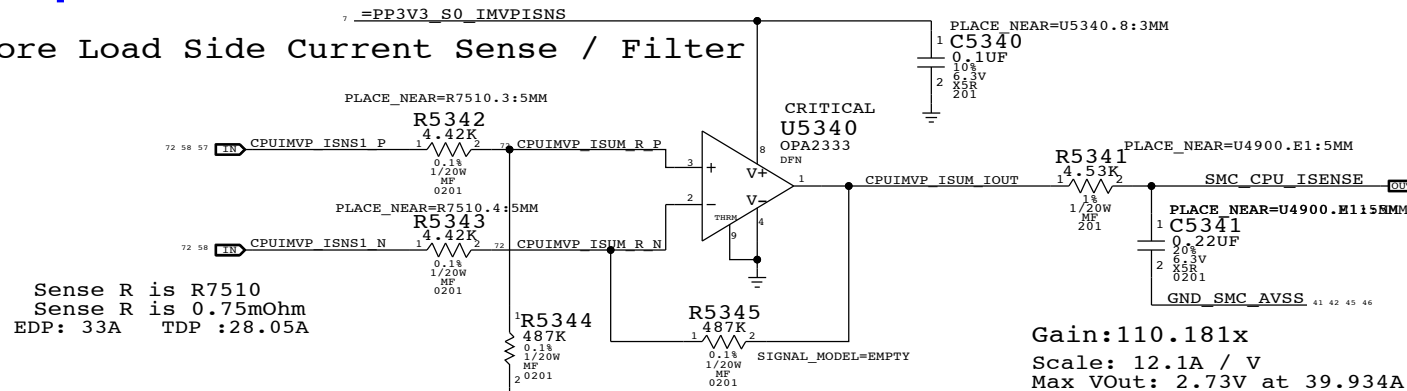




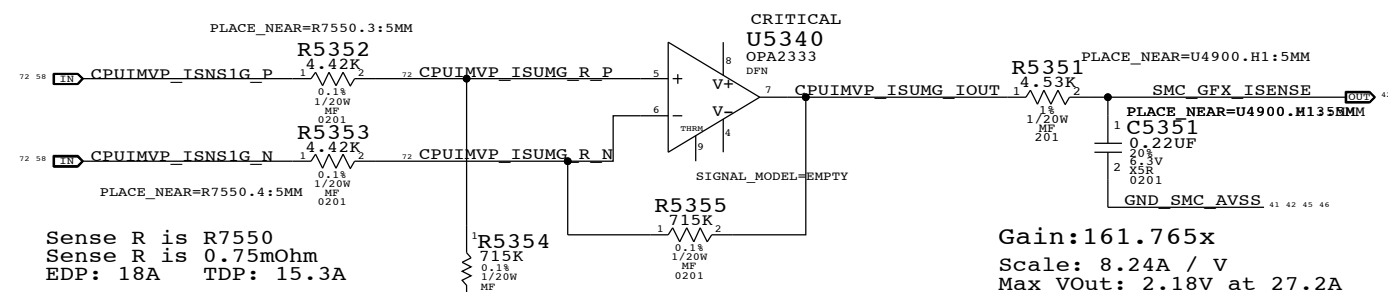
PBUS Voltage Sense Enable & Filter



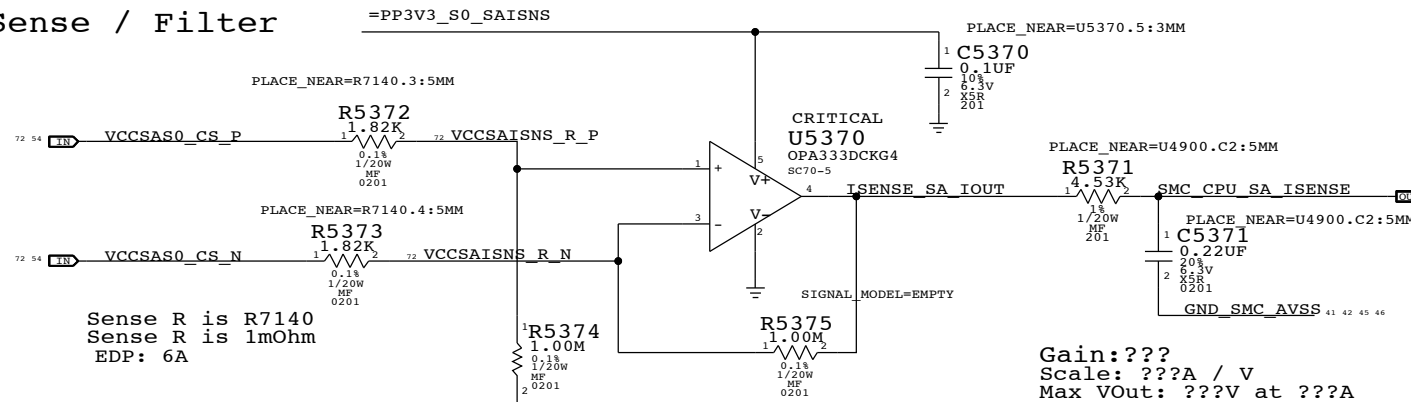
CPU VCore Load Side Current Sense / Filter



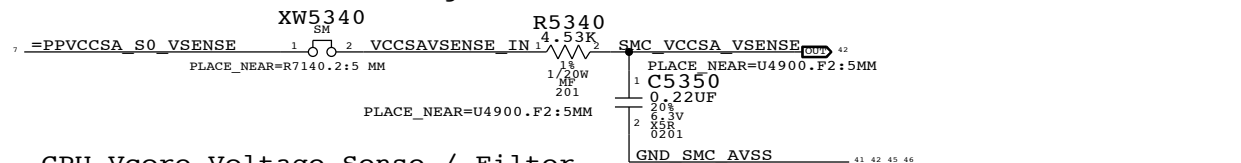
GFX/IG VCore Load Side Current Sense / Filter



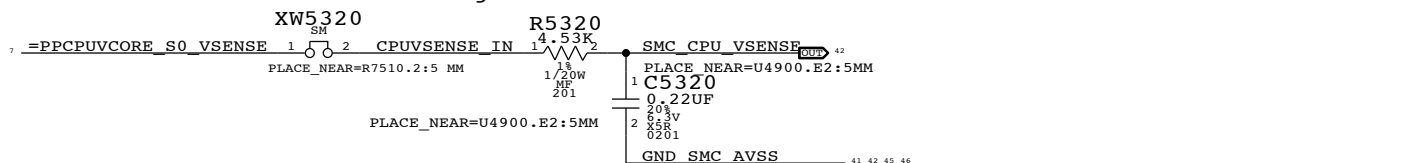
CPU SA Current Sense / Filter



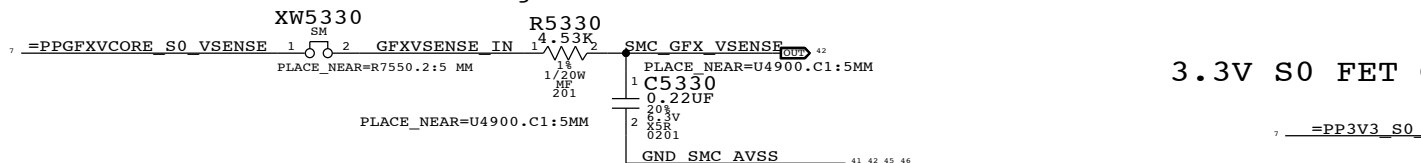
VCCSA Voltage Sense / Filter



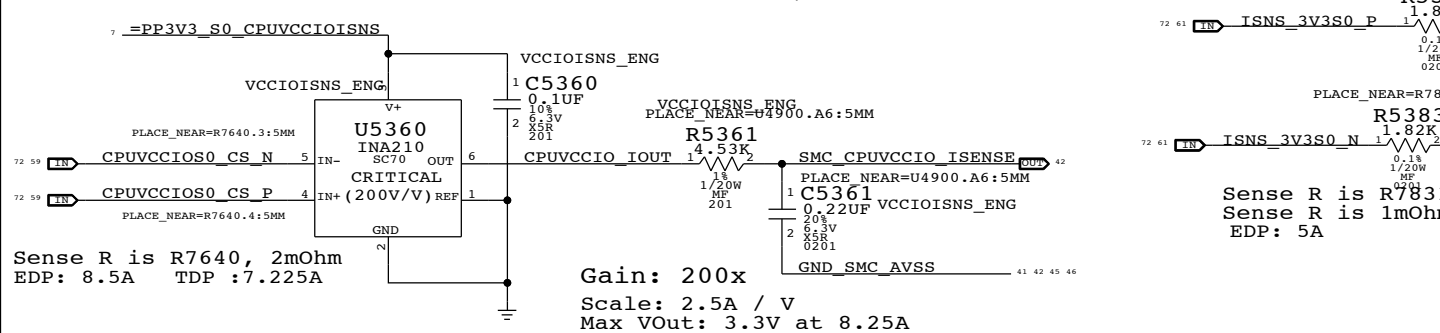
CPU Vcore Voltage Sense / Filter



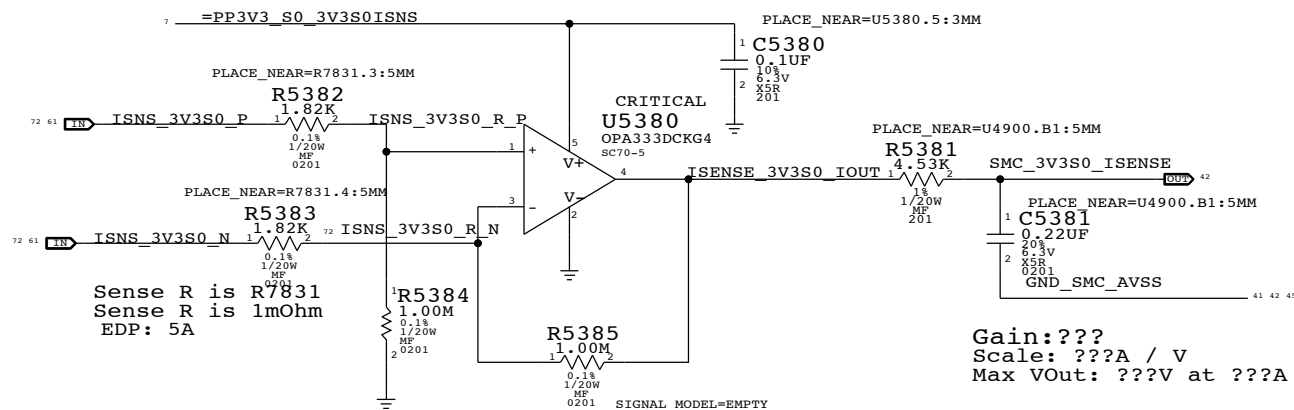
GFX/IG Vcore Voltage Sense / Filter



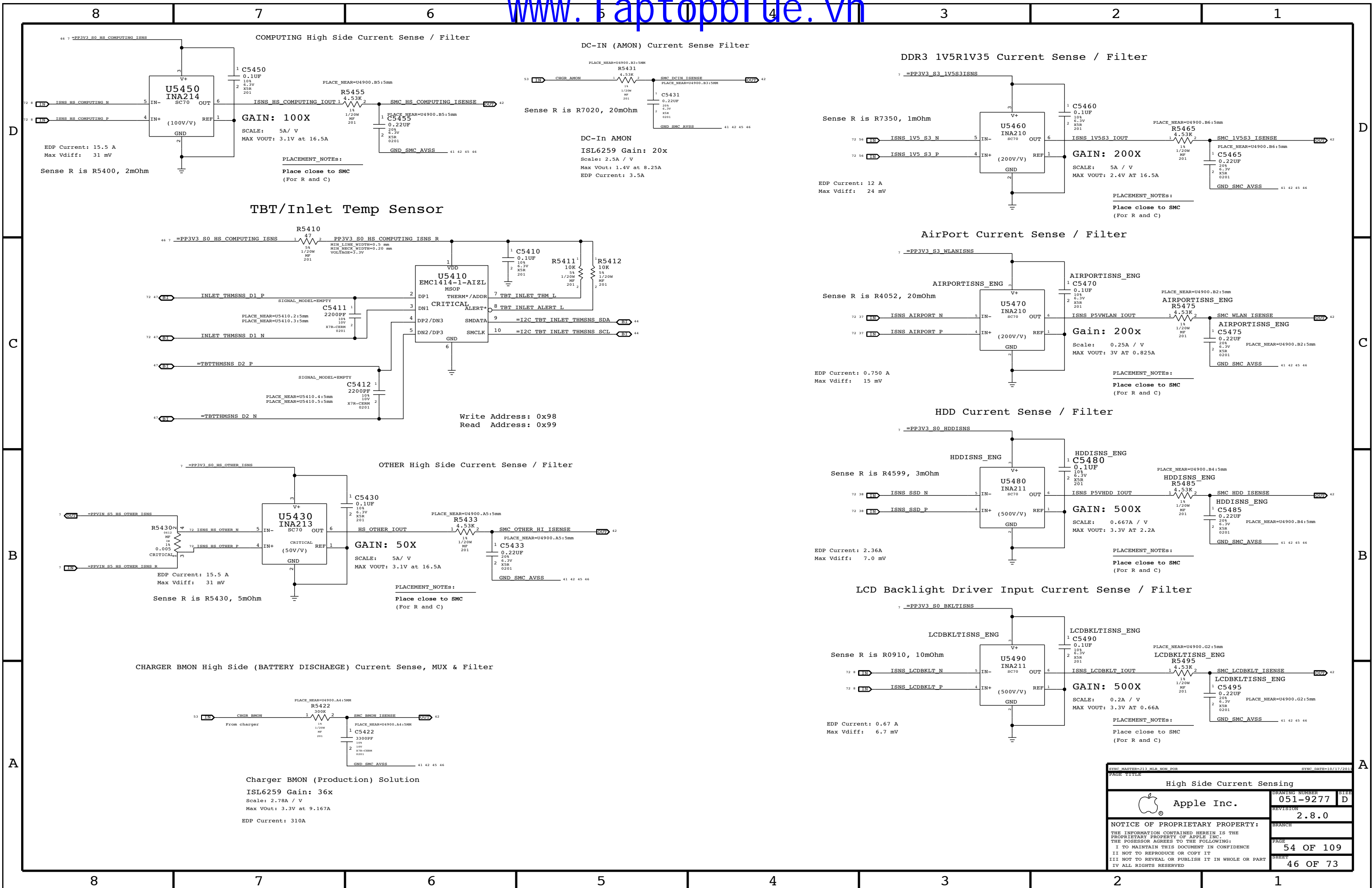
CPU 1.05V VCCIO Current Sense / Filter



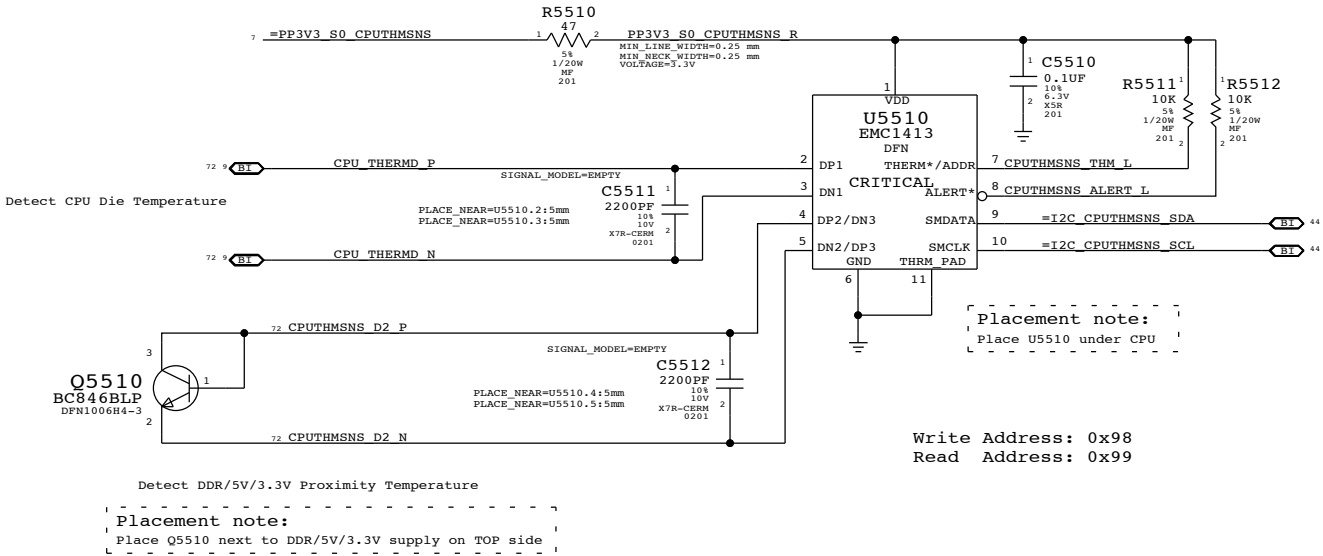
3.3V S0 FET Current Sense / Filter



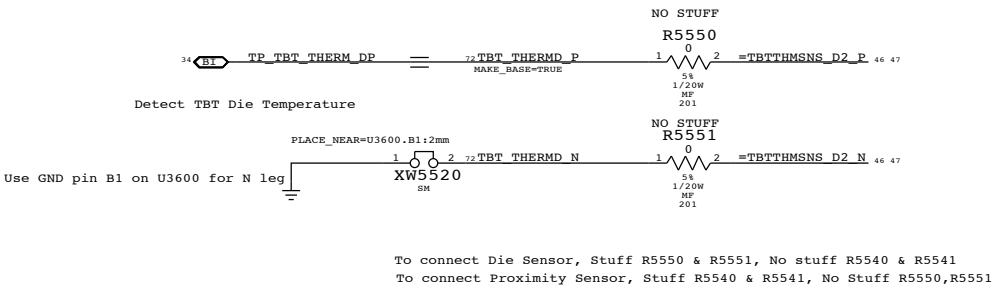
SYNC MASTER=J11 MLB		SYNC DATE=12/02/2011	
PAGE TITLE		Voltage & Load Side Current Sensing	
Apple Inc.		DRAWING NUMBER	051-9277
		REVISION	2.8.0
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CPU Proximity Sensor



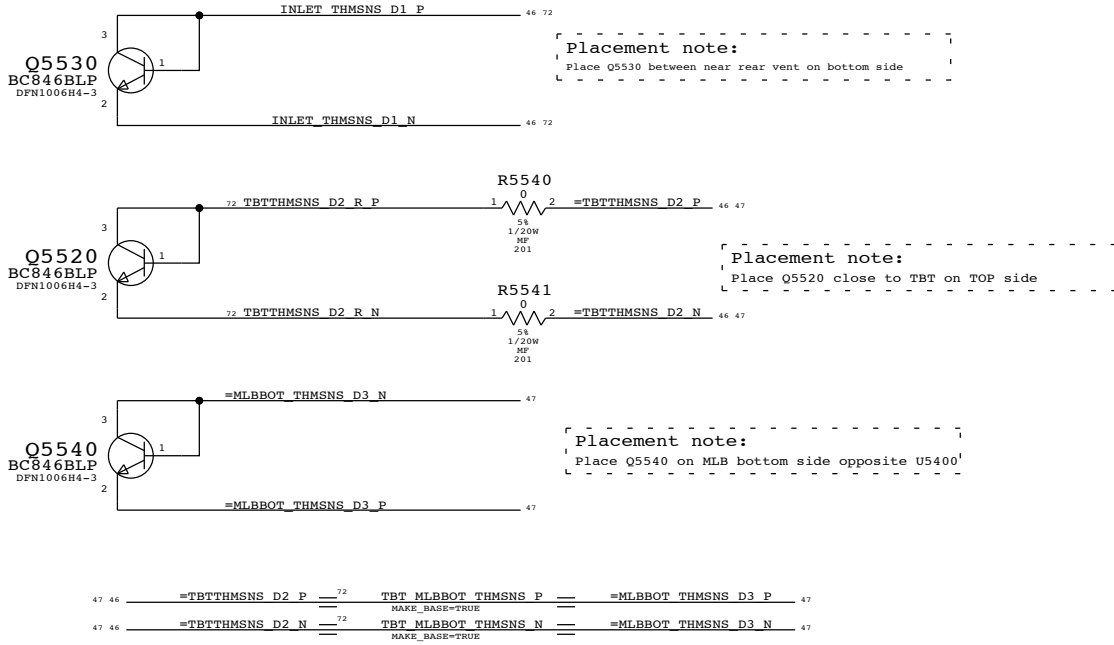
TBT Die




PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5361		VCCIOISNS_PROD
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5475		AIRPORTISNS_PROD
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5485		HDDISNS_PROD
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5495		LCDBKLTISNS_PROD

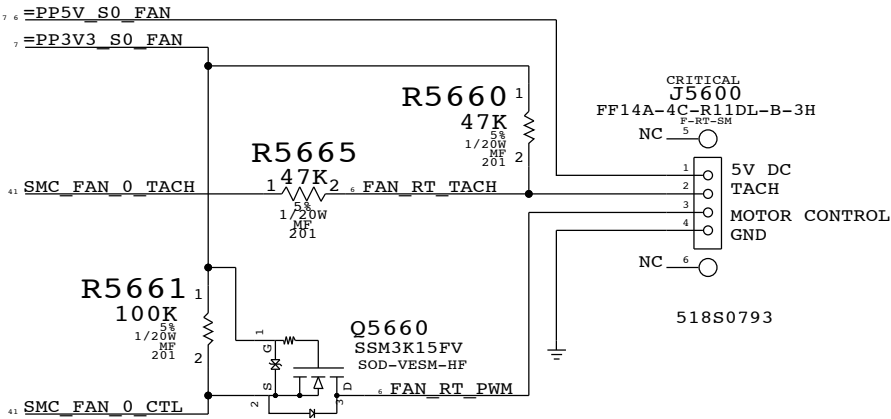
Replacing caps with 100K PD on ISENSE SMC inputs

TBT,MLB Bottom & Inlet Proximity Sensors

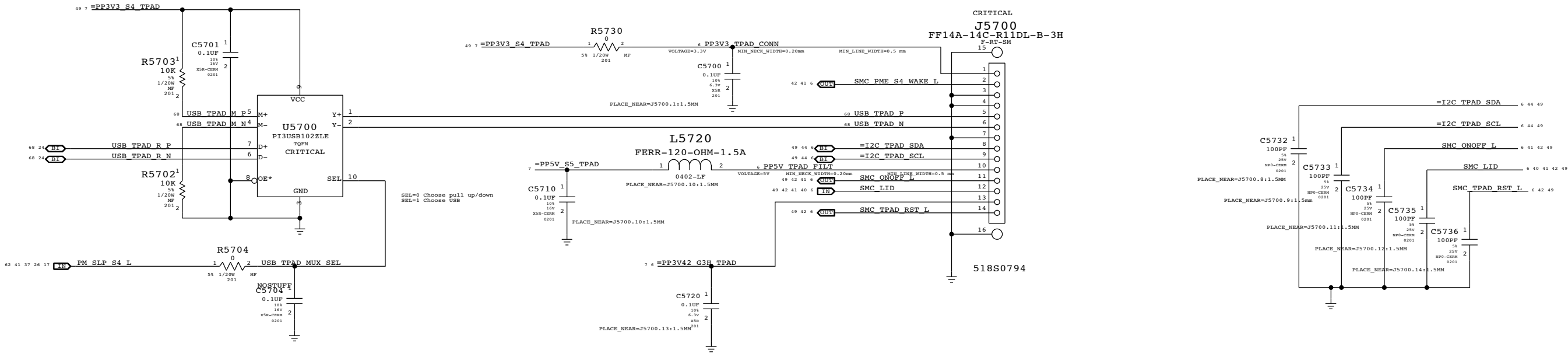


SYNC MASTER=J11 MLB		SYNC DATE=08/03/2011	
PAGE TITLE			
Thermal Sensors			
 Apple Inc.		DRAWING NUMBER	051-9277
		SIZE	D
		REVISION	2.8.0
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		PAGE	55 OF 109
		SHEET	47 OF 73

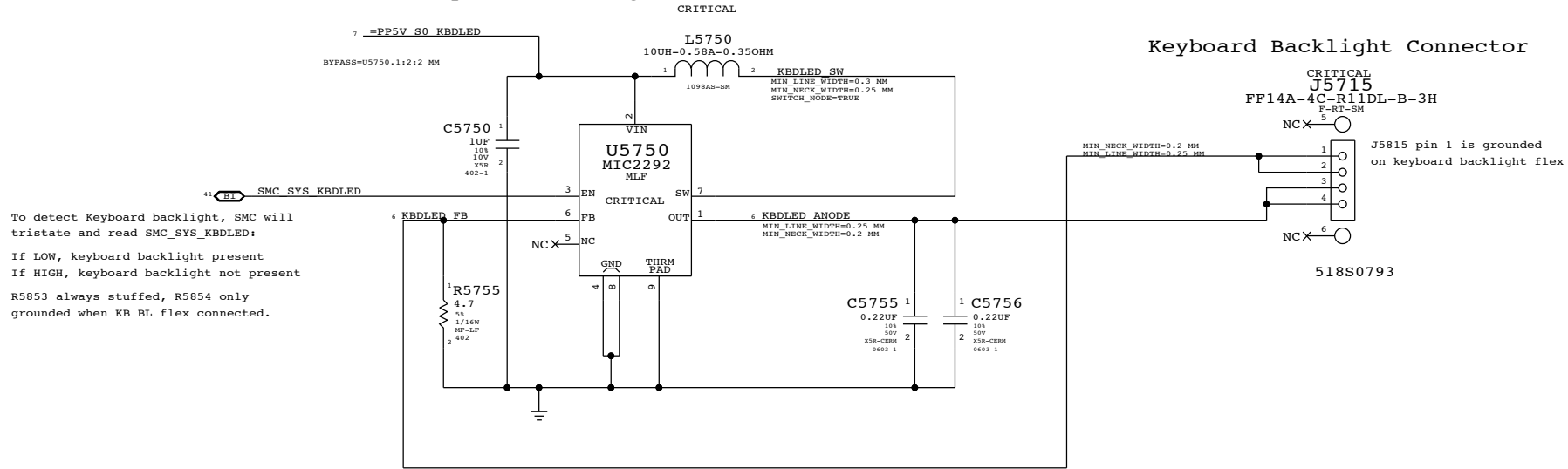
FAN CONNECTOR



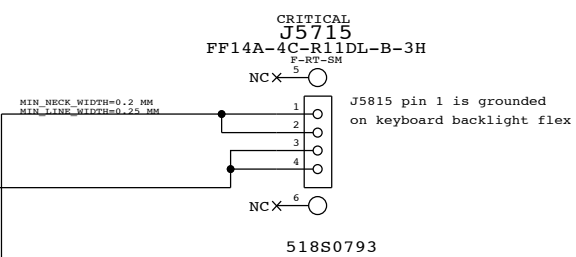
IPD Flex Connector




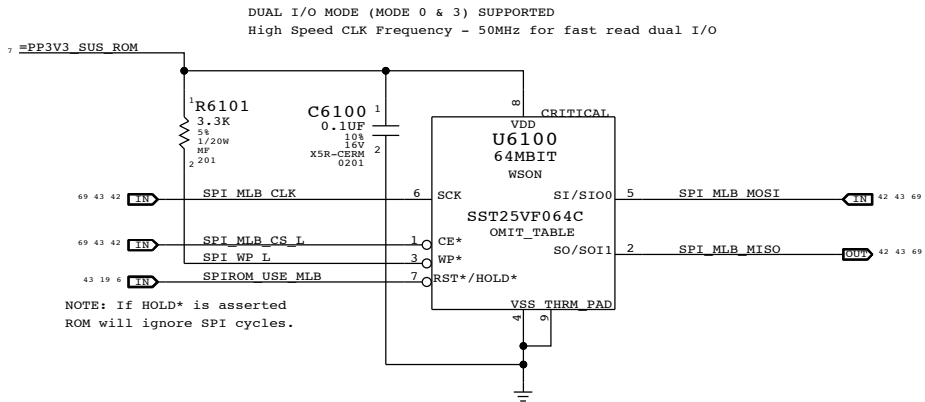
Keyboard Backlight Driver & Detection



Keyboard Backlight Connector



SYNC MASTER=J13 MLB NON POR		SYNC DATE=11/10/2011	
PAGE TITLE			
IPD / KBD Backlight			
	DRAWING NUMBER		SIZE
	051-9277		D
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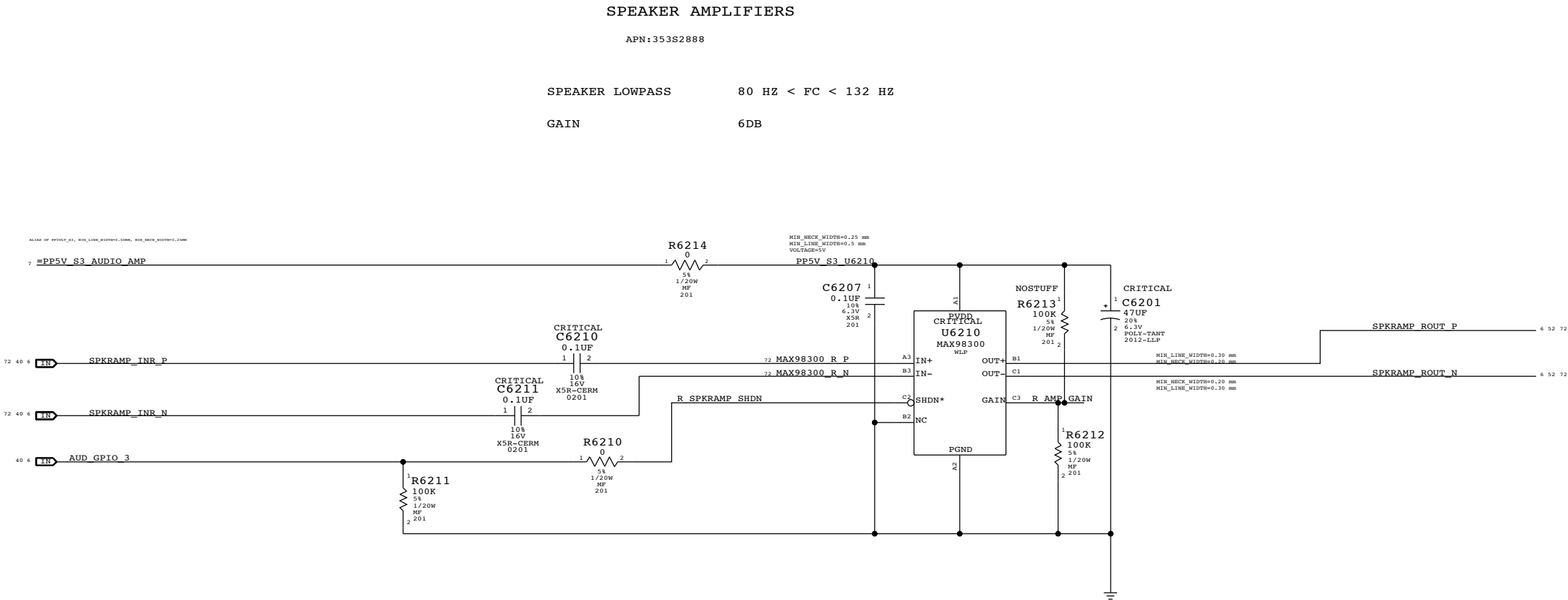
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B

B

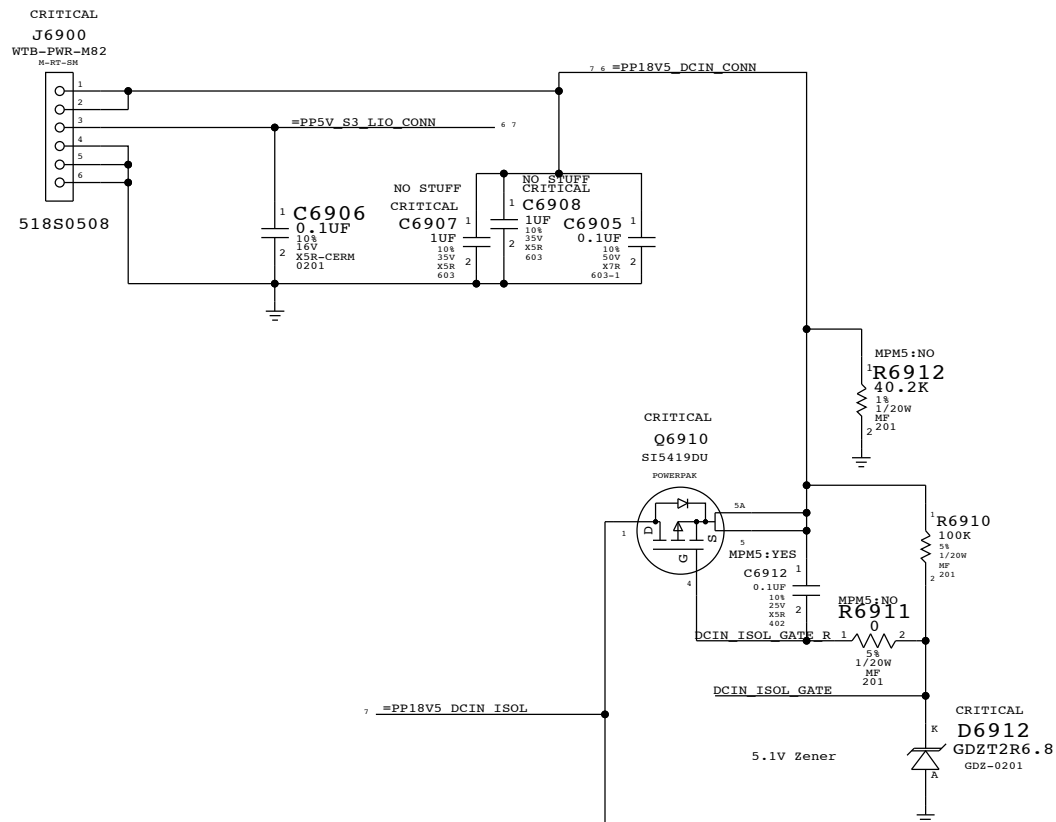
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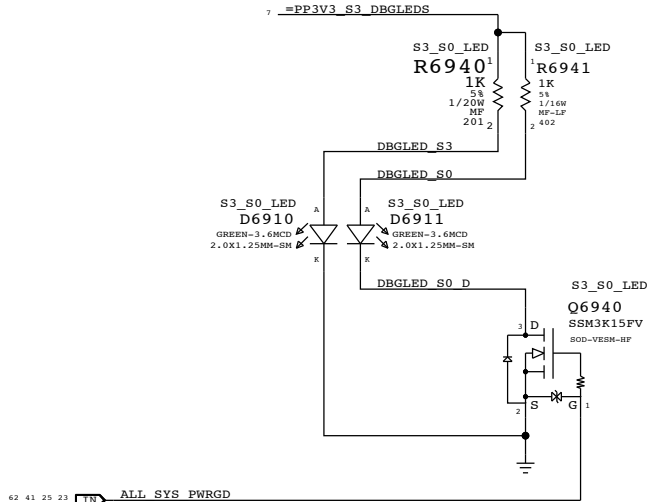
SYNC MASTER=J11 MLB		SYNC DATE=09/30/2013	
PAGE TITLE			
AUDIO0: SPEAKER AMP			
 Apple Inc.	DRAWING NUMBER		SIZE
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	REVISION		
	2.8.0		
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MLB to LIO Power Cable Connector

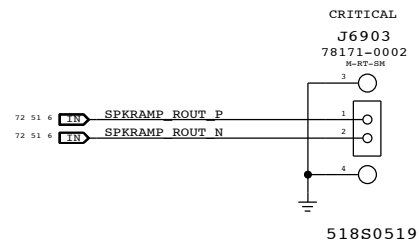


Debug LEDs

(For development only)



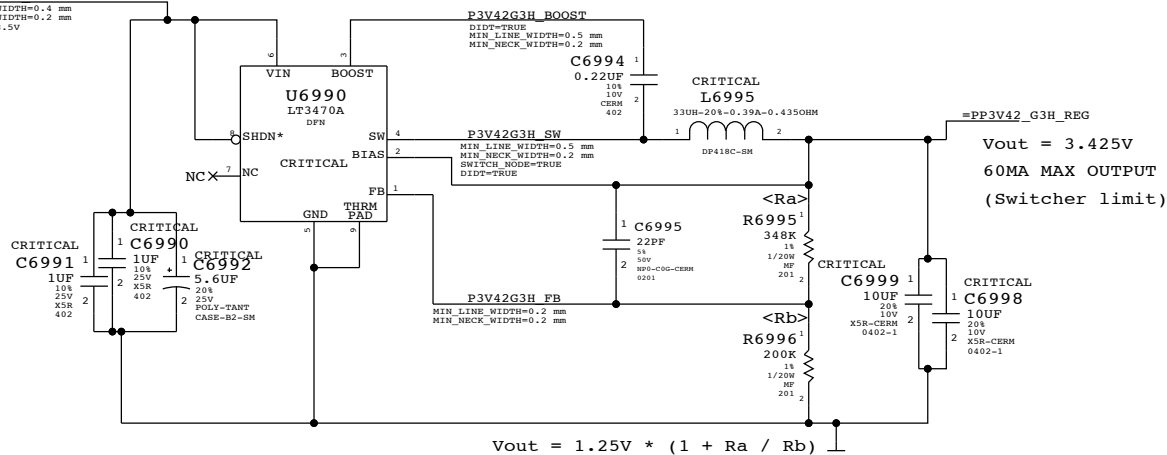
Right Speaker Connector



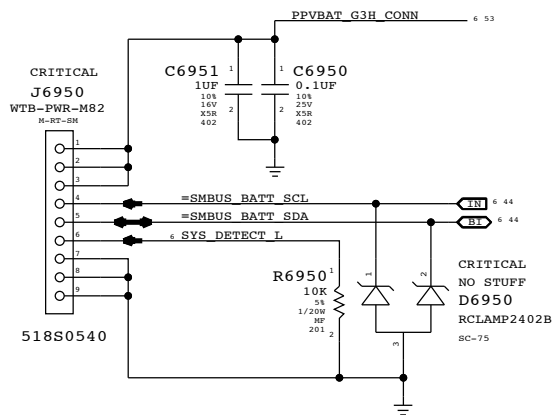
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0560	1	RES,HP,1/20W,50.9KOHM,1,0201,SMD	R6912		MPM5:YES
117S0008	1	RES,HP,1/20W,100KOHM,1,0201,SMD	R6911		MPM5:YES

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC Vref generator



K16-Specific Battery Connector

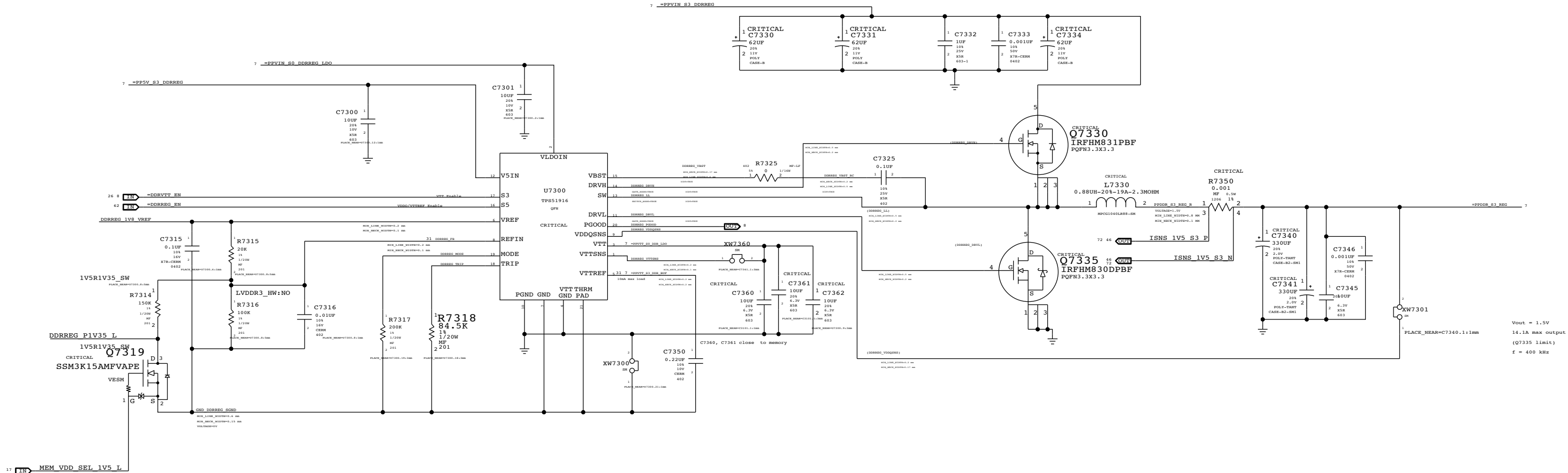


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$$\begin{aligned} \text{OCP} &= R_{7141} \times 8.5\mu\text{A} / R_{7140} \\ \text{OCP} &= 8.5\text{A} \end{aligned}$$

1

A

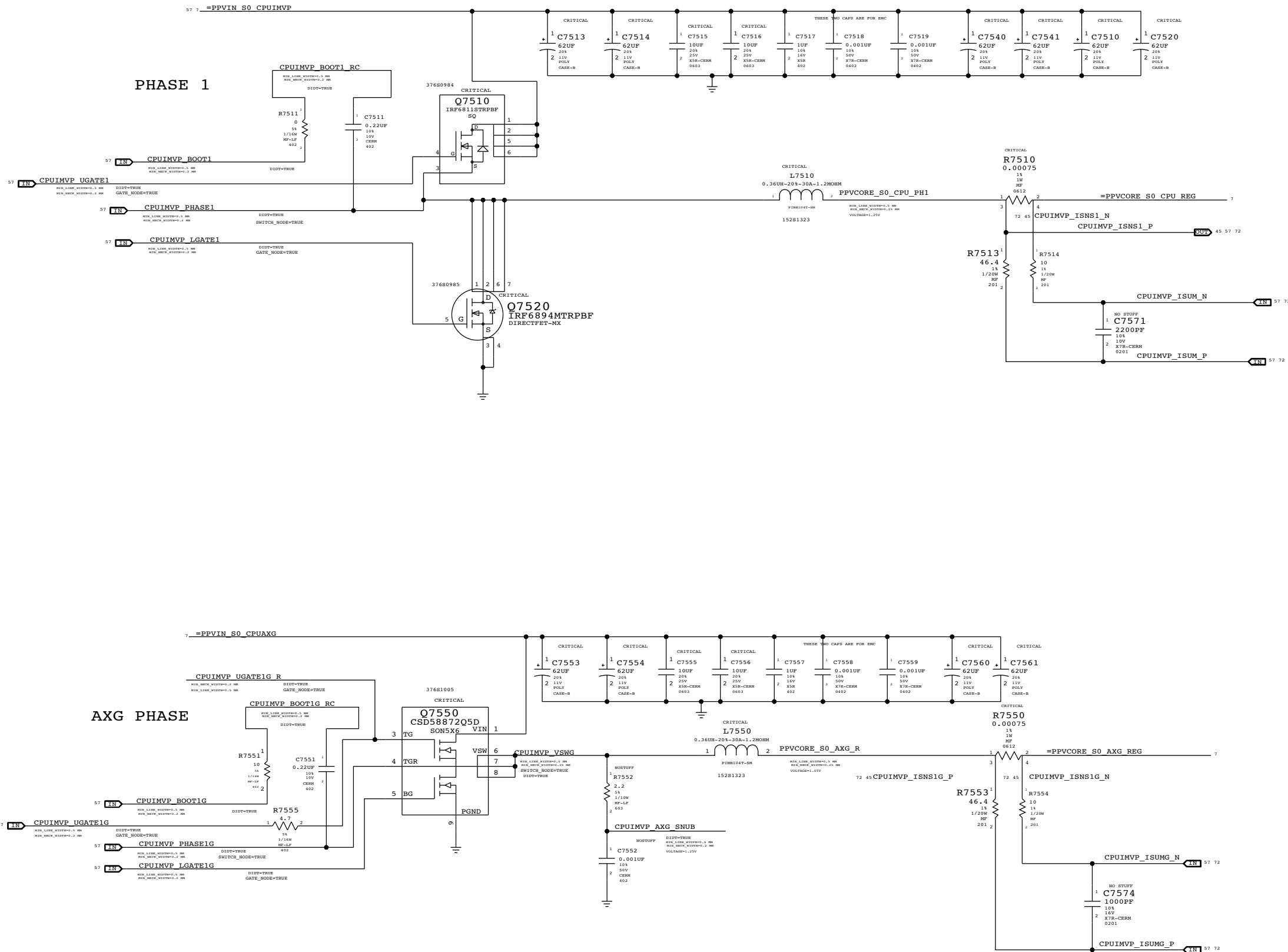


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0460	1	RES, MF, 60.4KOHM, 1/1/20W, 0201	R7316		LVDDR3_HW: YES

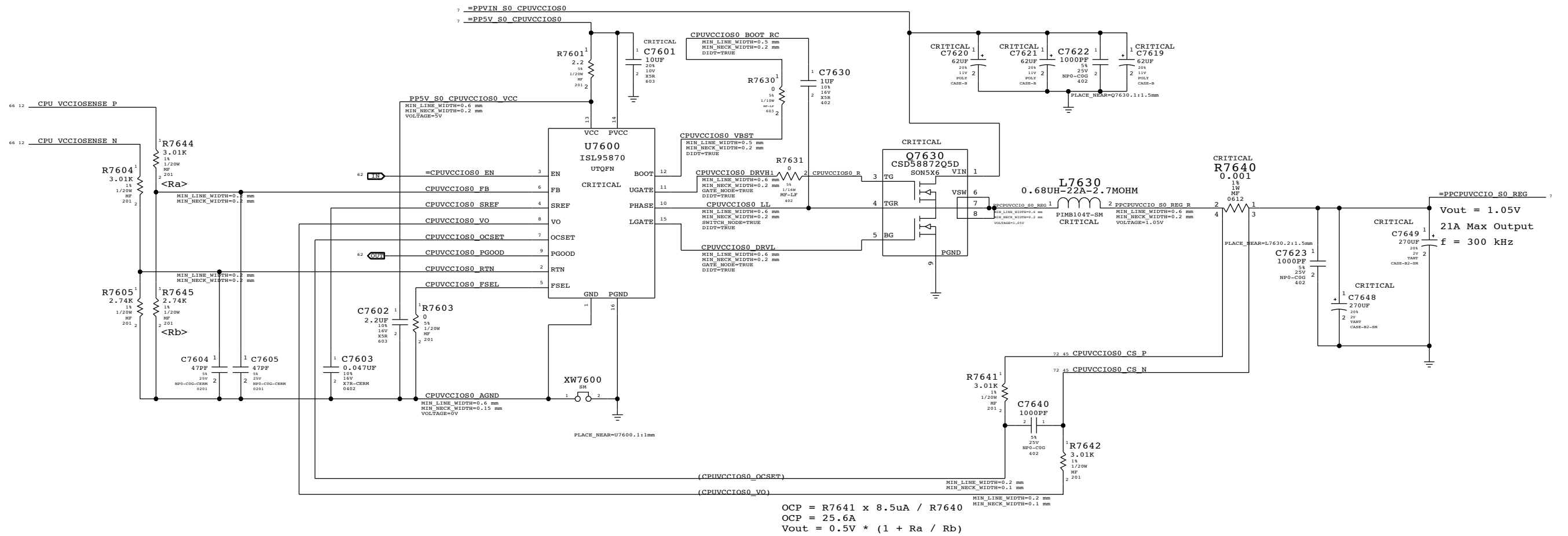
If LVDDR3_HW:NO is turned ON, switch R2821 & R7971 back to the original value for 1.5V DDR unless 1V5R1V35_SW is turned ON

A

CPU=IV Bridge ULV, AXG=GT2



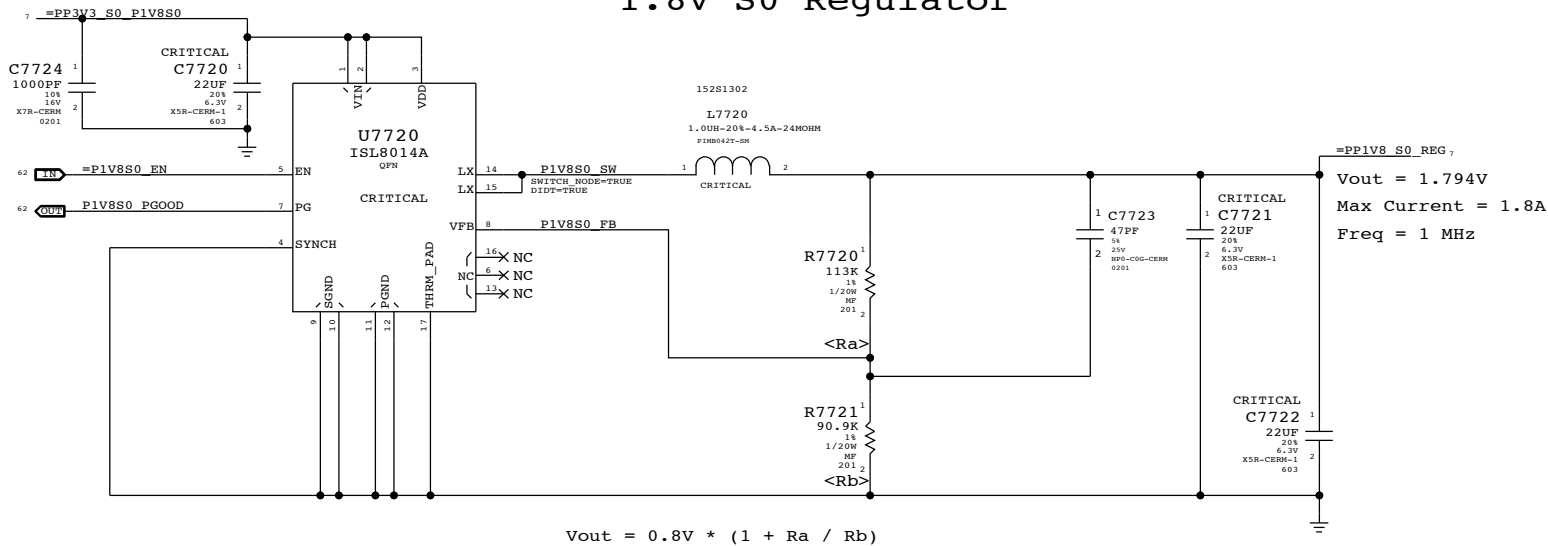
CPU VCCIO (1.05V S0) Regulator



OCF = R7641 x 8.5uA / R7640
OCF = 25.6A
Vout = 0.5V * (1 + Ra / Rb)

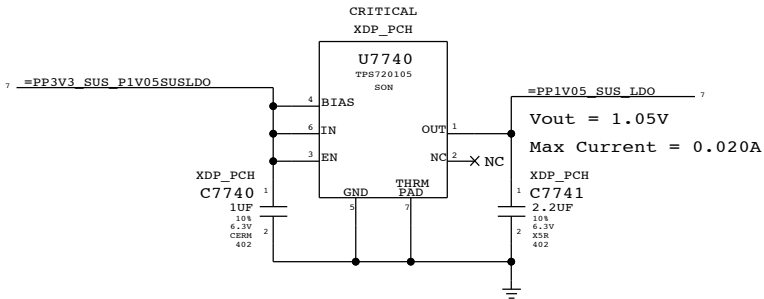
DRAWING NUMBER		SIZE	
051-9277		D	
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1.8V S0 Regulator

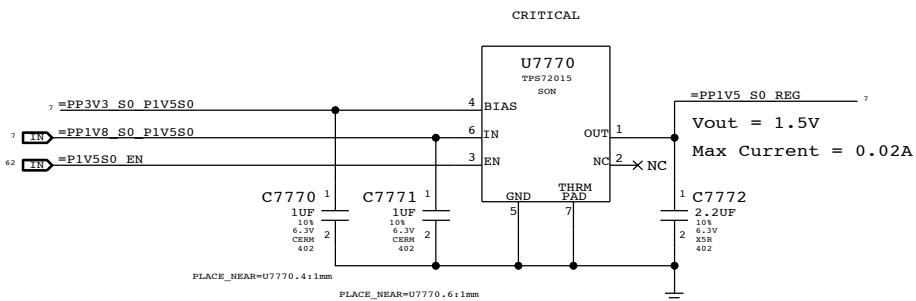


1.05V SUS LDO

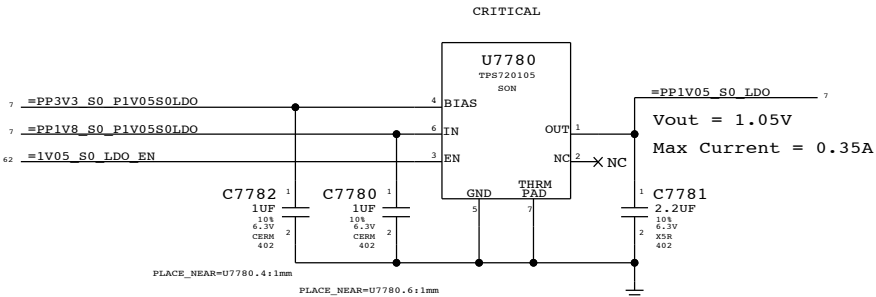
Cougar Point requires JTAG pull-ups to be powered at 1.05V when SUS suspend well is active. Pull-ups (3) must be 51 ohms to support XDP (not required in production). 70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.

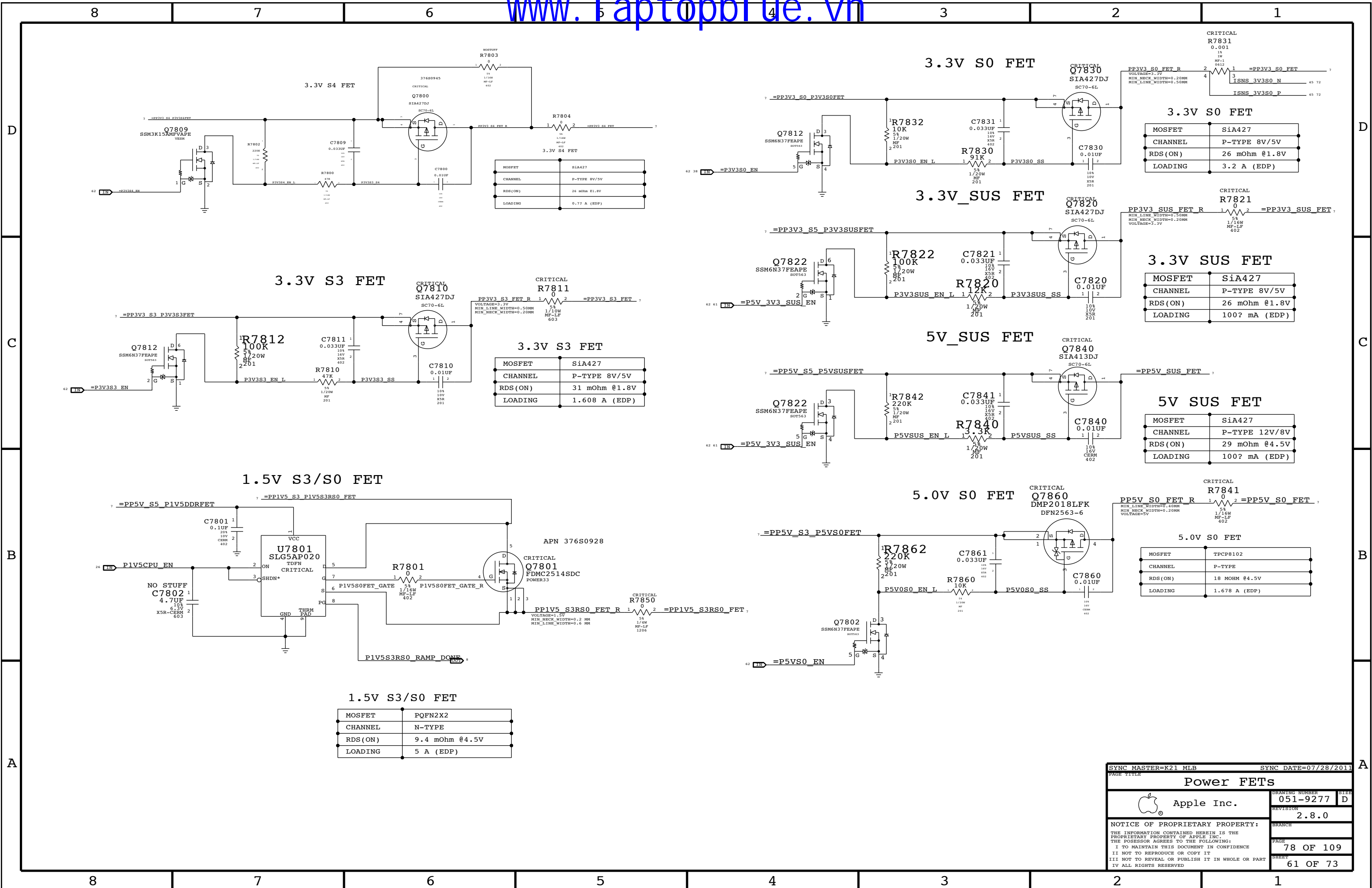


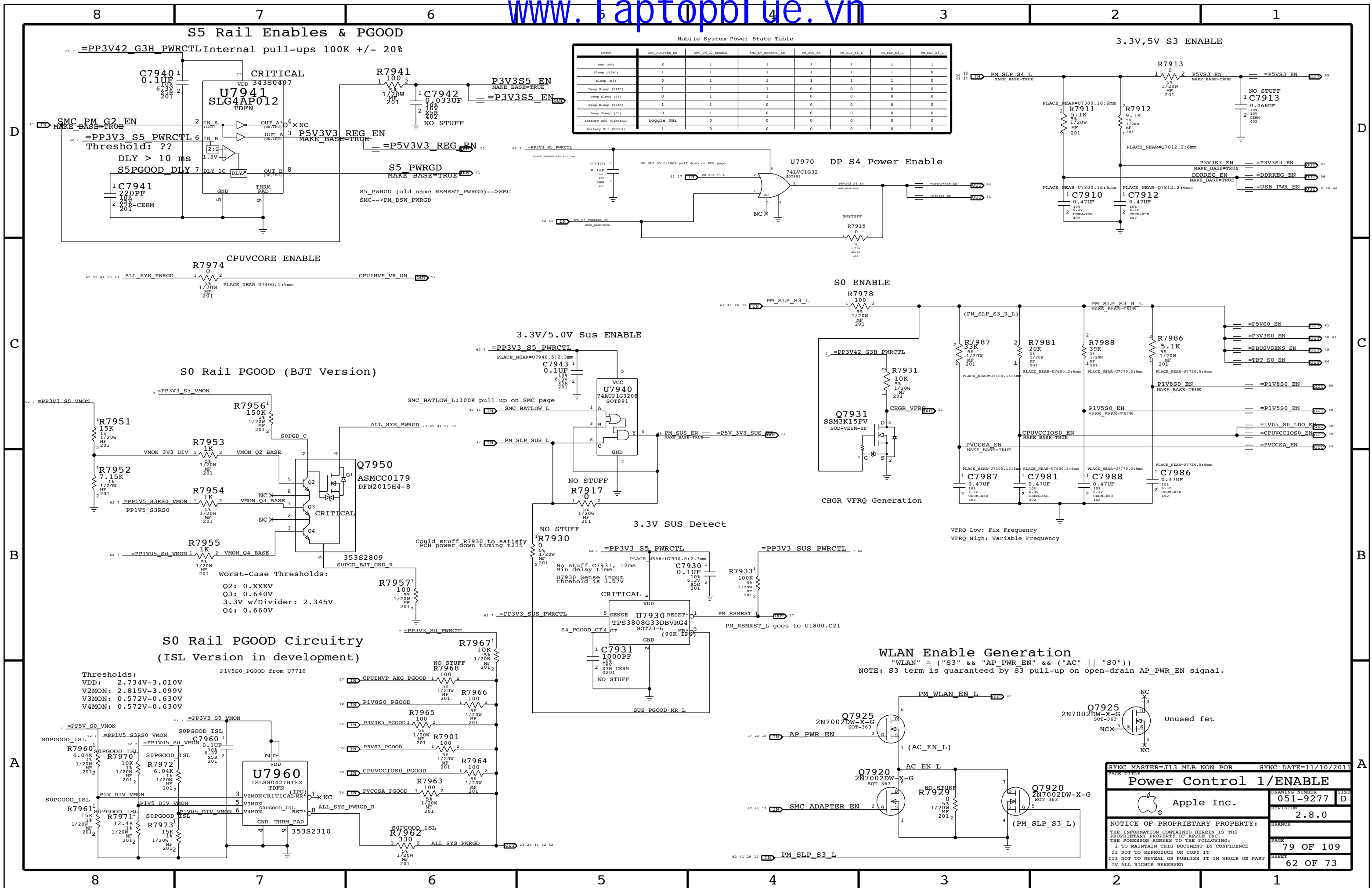
1.5V S0 LDO

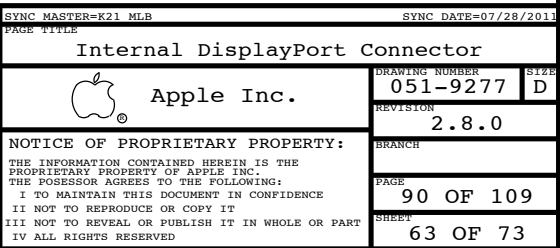


1.05V S0 LDO








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	Nominal	Min	Max
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)

SYNC MASTER-J11 MLB		SYNC DATE=10/03/2011	
PAGE TITLE			
Thunderbolt Connector A		DRAWING NUMBER	
 Apple Inc.		051-9277	
		D	
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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	0.100 MM	0.100 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_AGTL	*	=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_8MIL	*	*	CPU_8MIL_2ANY

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_ITP	*	*	CPU_ITP_2ANY

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	CPU_COMP	*	CPU_COMP_2SELF
CPU_COMP	*	*	CPU_COMP_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	*	=4x_DIELECTRIC	?
CPU_COMP_2OTHER	*	=6x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_VCCSENSE	CPU_VCCSENSE	*	CPU_VCCSENSE_2SELF
CPU_VCCSENSE	*	*	CPU_VCCSENSE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	*	=4x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	*	=6x_DIELECTRIC	?

PCI-Express Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
CLK_PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

PCIe Clock Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	CLK_PCIE	*	CLK_PCIE_2SELF
CLK_PCIE	*	*	CLK_PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	*	=4x_DIELECTRIC	?
CLK_PCIE_2OTHER	*	=6x_DIELECTRIC	?

CPU PCIe Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_CPU_TX	PCIE_CPU_TX	*	PCIE_TX2TX
PCIE_CPU_RX	PCIE_CPU_RX	*	PCIE_RX2RX
PCIE_CPU_TX	*_CPU_TX	*	PCIE_TX2OTHERTX
PCIE_CPU_RX	*_CPU_RX	*	PCIE_RX2OTHERRX
PCIE_CPU_TX	*_CPU_TX	*	PCIE_TX2RX
PCIE_CPU_RX	*_CPU_TX	*	PCIE_RX2TX
PCIE_CPU_TX	*_TX	*	PCIE_2OTHERHS
PCIE_CPU_RX	*_TX	*	PCIE_2OTHERHS
PCIE_CPU_TX	*_RX	*	PCIE_2OTHERHS
PCIE_CPU_RX	*_RX	*	PCIE_2OTHERHS
PCIE_CPU_TX	*	*	PCIE_2OTHER
PCIE_CPU_RX	*	*	PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	*	=2.5x_DIELECTRIC	?
PCIE_RX2RX	*	=2.5x_DIELECTRIC	?
PCIE_TX2OTHERTX	*	=4x_DIELECTRIC	?
PCIE_RX2OTHERRX	*	=4x_DIELECTRIC	?
PCIE_TX2TX	*	=6x_DIELECTRIC	?
PCIE_RX2TX	*	=6x_DIELECTRIC	?
PCIE_2OTHERHS	*	=4x_DIELECTRIC	?
PCIE_2OTHER	*	=3x_DIELECTRIC	?

PCH PCIe Spacing


NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_PCH_TX	PCIE_PCH_TX	*	PCIE_TX2TX
PCIE_PCH_RX	PCIE_PCH_RX	*	PCIE_RX2RX
PCIE_PCH_TX	*_PCH_TX	*	PCIE_TX2OTHERTX
PCIE_PCH_RX	*_PCH_RX	*	PCIE_RX2OTHERRX
PCIE_PCH_TX	*_PCH_RX	*	PCIE_TX2RX
PCIE_PCH_RX	*_PCH_TX	*	PCIE_RX2TX
PCIE_PCH_TX	*_TX	*	PCIE_2OTHERHS
PCIE_PCH_RX	*_TX	*	PCIE_2OTHERHS
PCIE_PCH_TX	*_RX	*	PCIE_2OTHERHS
PCIE_PCH_RX	*_RX	*	PCIE_2OTHERHS
PCIE_PCH_TX	*	*	PCIE_2OTHER
PCIE_PCH_RX	*	*	PCIE_2OTHER

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

CPU Net Properties

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
DMI_S2N	PCIE_80D	PCIE_PCH_TX	DMI_S2N_P<3:0>
DMI_S2N	PCIE_80D	PCIE_PCH_TX	DMI_S2N_N<3:0>
DMI_N2S	PCIE_80D	PCIE_PCH_RX	DMI_N2S_P<3:0>
DMI_N2S	PCIE_80D	PCIE_PCH_RX	DMI_N2S_N<3:0>
FDI_DATA	PCIE_80D	PCIE_PCH_RX	FDI_DATA_P<7:0>
FDI_DATA	PCIE_80D	PCIE_PCH_RX	FDI_DATA_N<7:0>
	CPU_45S	CPU_AGTL	FDI_FSYNC<1..0>
	CPU_45S	CPU_AGTL	FDI_LSYNC<1..0>
	CPU_45S	CPU_AGTL	FDI_INT
CPU_PECT	CPU_45S	CPU_COMP	CPU_PECT
PM_SYNC	CPU_45S	CPU_AGTL	PM_SYNC
PM_MEM_PWRGD	CPU_45S	CPU_AGTL	PM_MEM_PWRGD
	CPU_45S	CPU_ITP	XDP_DBRESET_L
	CPU_45S	CPU_ITP	XDP_CPU_RDY_L
	CPU_45S	CPU_ITP	XDP_CPU_PREQ_L
	CPU_27P4S	CPU_COMP	EDP_COMP
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<0>
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<1>
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2>
	CPU_45S	CPU_ITP	CPU_CFG<11..0>
CPU_CATERR_L	CPU_45S	CPU_AGTL	CPU_CATERR_L
	CPU_45S	CPU_AGTL	CPU_VCCIO_SEL
CPU_PROCHOT_L	CPU_45S	CPU_AGTL	CPU_PROCHOT_L
CPU_PWRGD	CPU_45S	CPU_AGTL	CPU_PWRGD
PM_THRMTRIP_L	CPU_45S	CPU_8MIL	PM_THRMTRIP_L
DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M_CPU_P
DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M_CPU_N
DPLL_REF_CLK120M	CLK_PCIE_80D	CLK_PCIE	DPLL_REF_CLKP
DPLL_REF_CLK120M	CLK_PCIE_80D	CLK_PCIE	DPLL_REF_CLKN
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_P
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_N
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPXDP_CLK100M_P
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPXDP_CLK100M_N
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_P
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_N
XDP_TDI	CPU_45S	CPU_ITP	XDP_CPU_TDI
XDP_TDO	CPU_45S	CPU_ITP	XDP_CPU_TDO
XDP_TMS	CPU_45S	CPU_ITP	XDP_CPU_TMS
XDP_TCK	CPU_45S	CPU_ITP	XDP_CPU_TCK
XDP_TRST_L	CPU_45S	CPU_ITP	XDP_CPU_TRST_L
XDP_BPM_L	CPU_45S	CPU_ITP	XDP_BPM_L<3..0>
(XDP_BPM_L_R_CFG)	CPU_45S	CPU_ITP	XDP_BPM_L<7..4>
(XDP_BPM_L_R_CFG)	CPU_45S	CPU_ITP	XDP_OBSDATA_B<3..0>
(FSB_CPURST_L)	CPU_45S	CPU_ITP	CPU_CFG<15..12>
	CPU_45S	CPU_ITP	XDP_CPURST_L
CPU_VCCSENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_P
CPU_VCCSENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_N
CPU_VCCIOSENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_P
CPU_VCCIOSENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_N
CPU_AXG_SENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_P
CPU_AXG_SENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_N
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_P
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_N
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N
CPU_SVIDALERT_L	CPU_45S	CPU_COMP	CPU_VIDALERT_L
CPU_SVIDSClk	CPU_45S	CPU_COMP	CPU_VIDSClk
CPU_SVIDSOUT	CPU_45S	CPU_COMP	CPU_VIDSOUT
PCIE_CPU_MUX_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_P<0>
PCIE_CPU_MUX_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_N<0>
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_MUX_IN_P
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_MUX_IN_N
PCIE_CPU_MUX_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_P<0>
PCIE_CPU_MUX_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_N<0>
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_MUX_OUT_P
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_MUX_OUT_N
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_R2D_C_P<1>
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_R2D_C_N<1>
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_P<1>
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_N<1>
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_P<1>
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_N<1>
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_P<1>
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_N<1>
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_P
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_N
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_P<3..0>
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_N<3..0>
	DP_80D	DP_TX	DP_INT_ML_F_P<3..0>
	DP_80D	DP_TX	DP_INT_ML_F_N<3..0>
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_P
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_N
	DP_80D	DP_AUX	DP_INT_AUX_CH_P
	DP_80D	DP_AUX	DP_INT_AUX_CH_N

Note: DisplayPort tables are on Page 103

SYNC MASTER=J13 CONSTRAINTS		SYNC DATE=01/11/2012	
PAGE TITLE			
CPU Constraints			
 Apple Inc.		DRAWING NUMBER	051-9277
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		REVISION	2.8.0
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		PAGE	100 OF 109
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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=3x_DIELECTRIC	?
MEM_CMD2CMD	*	=3x_DIELECTRIC	?
MEM_CMD2CTRL	*	=3x_DIELECTRIC	?
MEM_CTRL2CTRL	*	=3x_DIELECTRIC	?
MEM_CLK2CLK	*	=6x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=PWR_P2MM	?
MEM_2GND	*	=GND_P2MM	?
MEM_2OTHER	*	=6x_DIELECTRIC	?

PalPilot Spacing

=2x_DIELECTRIC
=5.7x_DIELECTRIC
=4x_DIELECTRIC
=4x_DIELECTRIC
=4x_DIELECTRIC
=8.6x_DIELECTRIC
=5.7x_DIELECTRIC
=PWR_P2MM
=GND_P2MM
=8.6x_DIELECTRIC

"Real" Spacing

=2x_DIELECTRIC
=3x_DIELECTRIC
=3x_DIELECTRIC
=3x_DIELECTRIC
=3x_DIELECTRIC
=6x_DIELECTRIC
=4x_DIELECTRIC
=PWR_P2MM
=GND_P2MM
=6x_DIELECTRIC

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_DQS2OWNDATA

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	*	*	MEM_2OTHER
MEM_A_DQS_1	*	*	MEM_2OTHER
MEM_A_DQS_2	*	*	MEM_2OTHER
MEM_A_DQS_3	*	*	MEM_2OTHER
MEM_A_DQS_4	*	*	MEM_2OTHER
MEM_A_DQS_5	*	*	MEM_2OTHER
MEM_A_DQS_6	*	*	MEM_2OTHER
MEM_A_DQS_7	*	*	MEM_2OTHER
MEM_B_DQS_0	*	*	MEM_2OTHER
MEM_B_DQS_1	*	*	MEM_2OTHER
MEM_B_DQS_2	*	*	MEM_2OTHER
MEM_B_DQS_3	*	*	MEM_2OTHER
MEM_B_DQS_4	*	*	MEM_2OTHER
MEM_B_DQS_5	*	*	MEM_2OTHER
MEM_B_DQS_6	*	*	MEM_2OTHER
MEM_B_DQS_7	*	*	MEM_2OTHER

MEM_A_DATA_0	*	*	MEM_2OTHER
MEM_A_DATA_1	*	*	MEM_2OTHER
MEM_A_DATA_2	*	*	MEM_2OTHER

MEM_A_DATA_3	*	*	MEM_2OTHER
MEM_A_DATA_4	*	*	MEM_2OTHER
MEM_A_DATA_5	*	*	MEM_2OTHER
MEM_A_DATA_6	*	*	MEM_2OTHER
MEM_A_DATA_7	*	*	MEM_2OTHER

MEM_B_DATA_0	*	*	MEM_2OTHER
MEM_B_DATA_1	*	*	MEM_2OTHER
MEM_B_DATA_2	*	*	MEM_2OTHER
MEM_B_DATA_3	*	*	MEM_2OTHER
MEM_B_DATA_4	*	*	MEM_2OTHER
MEM_B_DATA_5	*	*	MEM_2OTHER
MEM_B_DATA_6	*	*	MEM_2OTHER
MEM_B_DATA_7	*	*	MEM_2OTHER

MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
MEM_A_CLK	MEM_72D	MEM_CLK	MEM A CLK P<5..0>	8 11 27 28 32
MEM_A_CLK	MEM_72D	MEM_CLK	MEM A CLK N<5..0>	8 11 27 28 32
MEM_A_CTRL	MEM_45S	MEM_CTRL	MEM A CKE<3..0>	11 27 28 32
MEM_A_CTRL	MEM_45S	MEM_CTRL	MEM A CS L<3..0>	11 27 28 32
MEM_A_CTRL	MEM_45S	MEM_CTRL	MEM A ODT<3..0>	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM A A<15..0>	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM A BA<2..0>	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM A RAS L	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM A CAS L	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM A WE L	11 27 28 32
MEM_A_DO_BYTE0	MEM_45S	MEM_A_DATA_0	MEM A DO<7..0>	11 27
MEM_A_DO_BYTE1	MEM_45S	MEM_A_DATA_1	MEM A DO<15..8>	11 27
MEM_A_DO_BYTE2	MEM_45S	MEM_A_DATA_2	MEM A DO<23..16>	11 27
MEM_A_DO_BYTE3	MEM_45S	MEM_A_DATA_3	MEM A DO<31..24>	11 27
MEM_A_DO_BYTE4	MEM_45S	MEM_A_DATA_4	MEM A DO<39..32>	11 28
MEM_A_DO_BYTE5	MEM_45S	MEM_A_DATA_5	MEM A DO<47..40>	11 28
MEM_A_DO_BYTE6	MEM_45S	MEM_A_DATA_6	MEM A DO<55..48>	11 28
MEM_A_DO_BYTE7	MEM_45S	MEM_A_DATA_7	MEM A DO<63..56>	11 28
MEM_A_DQS0	MEM_80D	MEM_A_DQS_0	MEM A DQS P<0>	11 27
MEM_A_DQS0	MEM_80D	MEM_A_DQS_0	MEM A DQS N<0>	11 27
MEM_A_DQS1	MEM_80D	MEM_A_DQS_1	MEM A DQS P<1>	11 27
MEM_A_DQS1	MEM_80D	MEM_A_DQS_1	MEM A DQS N<1>	11 27
MEM_A_DQS2	MEM_80D	MEM_A_DQS_2	MEM A DQS P<2>	11 27
MEM_A_DQS2	MEM_80D	MEM_A_DQS_2	MEM A DQS N<2>	11 27
MEM_A_DQS3	MEM_80D	MEM_A_DQS_3	MEM A DQS P<3>	11 27
MEM_A_DQS3	MEM_80D	MEM_A_DQS_3	MEM A DQS N<3>	11 27
MEM_A_DQS4	MEM_80D	MEM_A_DQS_4	MEM A DQS P<4>	11 28
MEM_A_DQS4	MEM_80D	MEM_A_DQS_4	MEM A DQS N<4>	11 28
MEM_A_DQS5	MEM_80D	MEM_A_DQS_5	MEM A DQS P<5>	11 28
MEM_A_DQS5	MEM_80D	MEM_A_DQS_5	MEM A DQS N<5>	11 28
MEM_A_DQS6	MEM_80D	MEM_A_DQS_6	MEM A DQS P<6>	11 28
MEM_A_DQS6	MEM_80D	MEM_A_DQS_6	MEM A DQS N<6>	11 28
MEM_A_DQS7	MEM_80D	MEM_A_DQS_7	MEM A DQS P<7>	11 28
MEM_A_DQS7	MEM_80D	MEM_A_DQS_7	MEM A DQS N<7>	11 28
MEM_B_CLK	MEM_72D	MEM_CLK	MEM B CLK P<5..0>	8 11 29 30 32
MEM_B_CLK	MEM_72D	MEM_CLK	MEM B CLK N<5..0>	8 11 29 30 32
MEM_B_CTRL	MEM_45S	MEM_CTRL	MEM B CKE<3..0>	11 29 30 32
MEM_B_CTRL	MEM_45S	MEM_CTRL	MEM B CS L<3..0>	11 29 30 32
MEM_B_CTRL	MEM_45S	MEM_CTRL	MEM B ODT<3..0>	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM B A<15..0>	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM B BA<2..0>	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM B RAS L	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM B CAS L	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM B WE L	11 29 30 32
MEM_B_DO_BYTE0	MEM_45S	MEM_B_DATA_0	MEM B DO<7..0>	11 29
MEM_B_DO_BYTE1	MEM_45S	MEM_B_DATA_1	MEM B DO<15..8>	11 29
MEM_B_DO_BYTE2	MEM_45S	MEM_B_DATA_2	MEM B DO<23..16>	11 29
MEM_B_DO_BYTE3	MEM_45S	MEM_B_DATA_3	MEM B DO<31..24>	11 29
MEM_B_DO_BYTE4	MEM_45S	MEM_B_DATA_4	MEM B DO<39..32>	11 30
MEM_B_DO_BYTE5	MEM_45S	MEM_B_DATA_5	MEM B DO<47..40>	11 30
MEM_B_DO_BYTE6	MEM_45S	MEM_B_DATA_6	MEM B DO<55..48>	11 30
MEM_B_DO_BYTE7	MEM_45S	MEM_B_DATA_7	MEM B DO<63..56>	11 30
MEM_B_DQS0	MEM_80D	MEM_B_DQS_0	MEM B DQS P<0>	11 29
MEM_B_DQS0	MEM_80D	MEM_B_DQS_0	MEM B DQS N<0>	11 29
MEM_B_DQS1	MEM_80D	MEM_B_DQS_1	MEM B DQS P<1>	11 29
MEM_B_DQS1	MEM_80D	MEM_B_DQS_1	MEM B DQS N<1>	11 29
MEM_B_DQS2	MEM_80D	MEM_B_DQS_2	MEM B DQS P<2>	11 29
MEM_B_DQS2	MEM_80D	MEM_B_DQS_2	MEM B DQS N<2>	11 29
MEM_B_DQS3	MEM_80D	MEM_B_DQS_3	MEM B DQS P<3>	11 29
MEM_B_DQS3	MEM_80D	MEM_B_DQS_3	MEM B DQS N<3>	11 29
MEM_B_DQS4	MEM_80D	MEM_B_DQS_4	MEM B DQS P<4>	11 30
MEM_B_DQS4	MEM_80D	MEM_B_DQS_4	MEM B DQS N<4>	11 30
MEM_B_DQS5	MEM_80D	MEM_B_DQS_5	MEM B DQS P<5>	11 30
MEM_B_DQS5	MEM_80D	MEM_B_DQS_5	MEM B DQS N<5>	11 30
MEM_B_DQS6	MEM_80D	MEM_B_DQS_6	MEM B DQS P<6>	11 30
MEM_B_DQS6	MEM_80D	MEM_B_DQS_6	MEM B DQS N<6>	11 30
MEM_B_DQS7	MEM_80D	MEM_B_DQS_7	MEM B DQS P<7>	11 30
MEM_B_DQS7	MEM_80D	MEM_B_DQS_7	MEM B DQS N<7>	11 30
		MEM_PWR	PP1V5 S3RS0	6 7
		MEM_PWR	PP1V5 S3	6 7
		MEM_PWR	PP0V75 S3 MEM_VREFCA_A	27 28 31
		MEM_PWR	PP0V75 S3 MEM_VREFDO_A	27 28 31

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_ICOMP	*	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA3_PCH_TX	SATA3_PCH_TX	*	SATA3_TX2TX
SATA3_PCH_RX	SATA3_PCH_RX	*	SATA3_RX2RX
SATA3_PCH_TX	*_PCH_TX	*	SATA3_TX2OTHERTX
SATA3_PCH_RX	*_PCH_RX	*	SATA3_RX2OTHERRX
SATA3_PCH_TX	*_PCH_RX	*	SATA3_TX2RX
SATA3_PCH_RX	*_PCH_TX	*	SATA3_RX2TX
SATA3_PCH_TX	*_TX	*	SATA3_2OTHERHS
SATA3_PCH_RX	*_TX	*	SATA3_2OTHERHS
SATA3_PCH_TX	*_RX	*	SATA3_2OTHERHS
SATA3_PCH_RX	*_RX	*	SATA3_2OTHERHS
SATA3_PCH_TX	*	*	SATA3_2OTHER
SATA3_PCH_RX	*	*	SATA3_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA3_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
SATA3_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
SATA3_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
SATA3_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA3_TX2TX	*	=2.5x_DIELECTRIC	?
SATA3_RX2RX	*	=2.5x_DIELECTRIC	?
SATA3_TX2OTHERTX	*	=4x_DIELECTRIC	?
SATA3_RX2OTHERRX	*	=4x_DIELECTRIC	?
SATA3_TX2RX	*	=6x_DIELECTRIC	?
SATA3_RX2TX	*	=6x_DIELECTRIC	?
SATA3_2OTHERHS	*	=4x_DIELECTRIC	?
SATA3_2OTHER	*	=3x_DIELECTRIC	?

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

UART Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
UART_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
UART	*	=2x_DIELECTRIC	?

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIA5	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.8

USB 3.0 Interface Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_PCH_TX	USB3_PCH_TX	*	USB3_TX2TX
USB3_PCH_RX	USB3_PCH_RX	*	USB3_RX2RX
USB3_PCH_TX	*_PCH_TX	*	USB3_TX2OTHERTX
USB3_PCH_RX	*_PCH_RX	*	USB3_RX2OTHERRX
USB3_PCH_TX	*_PCH_RX	*	USB3_TX2RX
USB3_PCH_RX	*_PCH_TX	*	USB3_RX2TX
USB3_PCH_TX	*_TX	*	USB3_2OTHERHS
USB3_PCH_RX	*_TX	*	USB3_2OTHERHS
USB3_PCH_TX	*_RX	*	USB3_2OTHERHS
USB3_PCH_RX	*_RX	*	USB3_2OTHERHS
USB3_PCH_TX	*	*	USB3_2OTHER
USB3_PCH_RX	*	*	USB3_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
USB3_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	*	=2.5x_DIELECTRIC	?
USB3_RX2RX	*	=2.5x_DIELECTRIC	?
USB3_TX2OTHERTX	*	=4x_DIELECTRIC	?
USB3_RX2OTHERRX	*	=4x_DIELECTRIC	?
USB3_TX2RX	*	=6x_DIELECTRIC	?
USB3_RX2TX	*	=6x_DIELECTRIC	?
USB3_2OTHERHS	*	=4x_DIELECTRIC	?
USB3_2OTHER	*	=3x_DIELECTRIC	?

SOURCE: 471984_Cheif_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
SATA_PCH_MUX_R2D	SATA_80D	SATA3_PCH_TX	SATA_HDD_R2D_C_P
SATA_PCH_MUX_R2D	SATA_80D	SATA3_PCH_TX	SATA_HDD_R2D_C_N
SATA_PCH_MUX_R2D	SATA_80D	SATA3_PCH_TX	SATA_SSD_R2D_MUX_IN_P
SATA_PCH_MUX_R2D	SATA_80D	SATA3_PCH_TX	SATA_SSD_R2D_MUX_IN_N
SATA_MUX_SSD_R2D	SATA_80D	SATA3_PCH_TX	SATA_SSD_R2D_P
SATA_MUX_SSD_R2D	SATA_80D	SATA3_PCH_TX	SATA_SSD_R2D_N
SATA_PCH_MUX_D2R	SATA_80D	SATA3_PCH_RX	SATA_HDD_D2R_P
SATA_PCH_MUX_D2R	SATA_80D	SATA3_PCH_RX	SATA_HDD_D2R_N
SATA_PCH_MUX_D2R	SATA_80D	SATA3_PCH_RX	SATA_SSD_D2R_MUX_OUT_P
SATA_PCH_MUX_D2R	SATA_80D	SATA3_PCH_RX	SATA_SSD_D2R_MUX_OUT_N
SATA_MUX_SSD_D2R	SATA_80D	SATA3_PCH_RX	SATA_SSD_D2R_P
SATA_MUX_SSD_D2R	SATA_80D	SATA3_PCH_RX	SATA_SSD_D2R_N
PCH_SATA_ICOMP		SATA_ICOMP	PCH_SATAICOMP
USB_HUB1_UP	USB_80D	USB	USB_HUB_UP_P
USB_HUB1_UP	USB_80D	USB	USB_HUB_UP_N
USB_BT	USB_80D	USB	USB_BT_P
USB_BT	USB_80D	USB	USB_BT_N
USB_BT	USB_80D	USB	USB_BT_CONN_P
USB_BT	USB_80D	USB	USB_BT_CONN_N
USB_BT	USB_80D	USB	USB_BT_WAKE_P
USB_BT	USB_80D	USB	USB_BT_WAKE_N
USB_TPAD	USB_80D	USB	USB_TPAD_P
USB_TPAD	USB_80D	USB	USB_TPAD_N
USB_TPAD	USB_80D	USB	USB_TPAD_CONN_P
USB_TPAD	USB_80D	USB	USB_TPAD_CONN_N
USB_TPAD_HUB	USB_80D	USB	USB_TPAD_HUB_P
USB_TPAD_HUB	USB_80D	USB	USB_TPAD_HUB_N
USB_TPAD_HUB	USB_80D	USB	USB_TPAD_R_P
USB_TPAD_HUB	USB_80D	USB	USB_TPAD_R_N
USB_TPAD_M	USB_80D	USB	USB_TPAD_M_P
USB_TPAD_M	USB_80D	USB	USB_TPAD_M_N
USB_SDCARD	USB_80D	USB	USB_SDCARD_P
USB_SDCARD	USB_80D	USB	USB_SDCARD_N
USB_SMC	USB_80D	USB	USB_SMC_P
USB_SMC	USB_80D	USB	USB_SMC_N
USB_CAMERA	USB_80D	USB	USB_CAMERA_P
USB_CAMERA	USB_80D	USB	USB_CAMERA_N
USB_EXT_A	USB_80D	USB	USB_EXT_A_P
USB_EXT_A	USB_80D	USB	USB_EXT_A_N
UART_45S	UART	SMC_DEBUGPRT_TX_L	
UART_45S	UART	SMC_DEBUGPRT_RX_L	
USB2_EXT_A_MUXED_P	USB_80D	USB	USB2_EXT_A_MUXED_P
USB2_EXT_A_MUXED_N	USB_80D	USB	USB2_EXT_A_MUXED_N
USB2_EXT_A_MUXED_F_P	USB_80D	USB	USB2_EXT_A_MUXED_F_P
USB2_EXT_A_MUXED_F_N	USB_80D	USB	USB2_EXT_A_MUXED_F_N
USB3_EXT_A_RX	USB_80D	USB3_PCH_RX	USB3_EXT_A_RX_P
USB3_EXT_A_RX	USB_80D	USB3_PCH_RX	USB3_EXT_A_RX_N
USB3_EXT_A_TX	USB_80D	USB3_PCH_TX	USB3_EXT_A_TX_P
USB3_EXT_A_TX	USB_80D	USB3_PCH_TX	USB3_EXT_A_TX_N
USB3_EXT_A_RX_F_P	USB_80D	USB3_PCH_RX	USB3_EXT_A_RX_F_P
USB3_EXT_A_RX_F_N	USB_80D	USB3_PCH_RX	USB3_EXT_A_RX_F_N
USB3_EXT_A_TX_F_P	USB_80D	USB3_PCH_TX	USB3_EXT_A_TX_F_P
USB3_EXT_A_TX_F_N	USB_80D	USB3_PCH_TX	USB3_EXT_A_TX_F_N
USB3_EXT_A_TX_C_P	USB_80D	USB3_PCH_TX	USB3_EXT_A_TX_C_P
USB3_EXT_A_TX_C_N	USB_80D	USB3_PCH_TX	USB3_EXT_A_TX_C_N
USB_EXTB	USB_80D	USB	USB_EXTB_P
USB_EXTB	USB_80D	USB	USB_EXTB_N
USB_EXTB_EHCI_P	USB_80D	USB	USB_EXTB_EHCI_P
USB_EXTB_EHCI_N	USB_80D	USB	USB_EXTB_EHCI_N
USB_EXTB_XHCI_P	USB_80D	USB	USB_EXTB_XHCI_P
USB_EXTB_XHCI_N	USB_80D	USB	USB_EXTB_XHCI_N
USB3_EXTB_RX	USB_80D	USB3_PCH_RX	USB3_EXTB_RX_P
USB3_EXTB_RX	USB_80D	USB3_PCH_RX	USB3_EXTB_RX_N
USB3_EXTB_RX_RC_P	USB_80D	USB3_PCH_RX	USB3_EXTB_RX_RC_P
USB3_EXTB_RX_RC_N	USB_80D	USB3_PCH_RX	USB3_EXTB_RX_RC_N
USB3_EXTB_RX_CONN_P	USB_80D	USB3_PCH_RX	USB3_EXTB_RX_CONN_P
USB3_EXTB_RX_CONN_N	USB_80D	USB3_PCH_RX	USB3_EXTB_RX_CONN_N
USB3_EXTB_TX_P	USB_80D	USB3_PCH_TX	USB3_EXTB_TX_P
USB3_EXTB_TX_N	USB_80D	USB3_PCH_TX	USB3_EXTB_TX_N
USB3_EXTB_TX_C_P	USB_80D	USB3_PCH_TX	USB3_EXTB_TX_C_P
USB3_EXTB_TX_C_N	USB_80D	USB3_PCH_TX	USB3_EXTB_TX_C_N
(USB_TPAD_HUB)	USB_80D	USB	USB_EXTD_XHCI_P
(USB_TPAD_HUB)	USB_80D	USB	USB_EXTD_XHCI_N
PCH_USB_RBIA5	PCH_USB_RBIA5		PCH_USB_RBIA5
PCH_DIFFECLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_PCH_P
PCH_DIFFECLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_PCH_N
PCH_DIFFECLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCH_CLK96M_DOT_P
PCH_DIFFECLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCH_CLK96M_DOT_N
PCH_DIFFECLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCH_CLK100M_SATA_P
PCH_DIFFECLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCH_CLK100M_SATA_N
PCH_DIFFECLK_UNUSED	CPU_45S	CLK_PCIE	PCH_CLK14P3M_REFCLK

SATA SSD


USB Hub nets

USB Camera nets

USB EXT_A nets (Right USB port)

USB EXT_B nets (Left USB port)

Unused USB nets

SYNC MASTER=J13 CONSTRAINTS		SYNC DATE=01/11/2012	
PAGE TITLE			
PCH Constraints 1			
	Apple Inc.	DRAWING NUMBER	051-9277
		SIZE	D
REVISION		2.8.0	
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PAGE		102	OF 109
SHEET		68	OF 73

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=3x_DIELECTRIC	?
CLK_LPC	*	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ihex Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S_R_50S	TOP,BOTTOM	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE		
SMB_45S_R_50S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ihex Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=4x_DIELECTRIC	?

XDP Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_ITP	*	=2+1_SPACING	?

DisplayPort

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2DP	*	=3x_DIELECTRIC	?	DP_2DP	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_2OTHERHS	*	=4x_DIELECTRIC	?	DP_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
DP_2OTHER	*	=3x_DIELECTRIC	?	DP_2OTHER	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_AUX	*	=3x_DIELECTRIC	?	DP_AUX	TOP,BOTTOM	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DP_TX	DP_TX	*	DP_2DP
DP_TX	*_TX	*	DP_2OTHERHS
DP_TX	*_RX	*	DP_2OTHERHS
DP_TX	*	*	DP_2OTHER

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
LPC_AD	LPC_45S	LPC	LPC AD<3..0>	6 16 41 43
LPC_FRAME_L	LPC_45S	LPC	LPC FRAME_L	6 16 41 43
LPC_45S	LPC_45S	LPC	LPCPLUS RESET_L	6 25 43
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_SMC	25 41
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_SMC_R	18 25
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_LPCPLUS	6 25 43
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_LPCPLUS_R	18 25
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	PCH_CLK33M_PCIIN	16 25
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	PCH_CLK33M_PCIOUT	18 25
SMBUS_PCH_CLK	SMB_45S_R_50S	SMB	SMBUS_PCH_CLK	16 44
SMBUS_PCH_DATA	SMB_45S_R_50S	SMB	SMBUS_PCH_DATA	16 44
SMBUS_PCH_0_CLK	SMB_45S_R_50S	SMB	SML_PCH_0_CLK	16 44
SMBUS_PCH_0_DATA	SMB_45S_R_50S	SMB	SML_PCH_0_DATA	16 44
SMBUS_GMC_1_80_SCT	SMB_45S_R_50S	SMB	SML_PCH_1_CLK	16 44
SMBUS_GMC_1_80_SDA	SMB_45S_R_50S	SMB	SML_PCH_1_DATA	16 44
HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK	6 16 40
HDA_BIT_CLK_R	HDA_45S	HDA	HDA_BIT_CLK_R	16
HDA_SYNC	HDA_45S	HDA	HDA_SYNC	6 16 40
HDA_SYNC_R	HDA_45S	HDA	HDA_SYNC_R	16
HDA_RST_L	HDA_45S	HDA	HDA_RST_R_L	16
HDA_RST_L	HDA_45S	HDA	HDA_RST_L	6 16 40
HDA_SDIN0	HDA_45S	HDA	HDA_SDIN0	6 16 40
HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT	6 16 40
HDA_SDOUT_R	HDA_45S	HDA	HDA_SDOUT_R	16 25
PM_SUS_CLK	CLK_SLOW_45S	CLK_SLOW	PM_CLK32K_SUSCLK_R	17 42
SMC_CLK32K	CLK_SLOW_45S	CLK_SLOW	SMC_CLK32K	41 42
SPI_CLK_R	SPT_45S	SPT	SPI_CLK_R	16 43
SPI_CLK	SPT_45S	SPT	SPI_CLK	43
SPI_MOSI_R	SPT_45S	SPT	SPI_MOSI_R	16 43
SPI_MOSI	SPT_45S	SPT	SPI_MOSI	43
SPI_MISO	SPT_45S	SPT	SPI_MISO	16 43
SPI_CS0_R_L	SPT_45S	SPT	SPI_CS0_R_L	16 43
SPI_CS0_L	SPT_45S	SPT	SPI_CS0_L	43
SPI_SMC_CLK	SPT_45S	SPT	SPI_SMC_CLK	41 42
SPI_SMC_MOSI	SPT_45S	SPT	SPI_SMC_MOSI	41 42
SPI_SMC_MISO	SPT_45S	SPT	SPI_SMC_MISO	41 42
SPI_SMC_CS_L	SPT_45S	SPT	SPI_SMC_CS_L	41 42
SPI_MLB_CLK	SPT_45S	SPT	SPI_MLB_CLK	42 43 50
SPI_MLB_MOSI	SPT_45S	SPT	SPI_MLB_MOSI	42 43 50
SPI_MLB_MISO	SPT_45S	SPT	SPI_MLB_MISO	42 43 50
SPI_MLB_CS_L	SPT_45S	SPT	SPI_MLB_CS_L	42 43 50
PCIE_AP_R2D_P	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_P	6 37
PCIE_AP_R2D_N	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_N	6 37
PCIE_AP_R2D_C_P	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_C_P	16 37
PCIE_AP_R2D_C_N	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_C_N	16 37
PCIE_AP_D2R_P	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_P	6 16 37
PCIE_AP_D2R_N	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_N	6 16 37
PCIE_CLK100M_AP_P	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_P	6 16 37
PCIE_CLK100M_AP_N	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_N	6 16 37
PCIE_TBT_R2D_P<3..0>	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_P<3..0>	34
PCIE_TBT_R2D_N<3..0>	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_N<3..0>	34
PCIE_TBT_R2D_C_P<3..0>	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_C_P<3..0>	8 34
PCIE_TBT_R2D_C_N<3..0>	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_C_N<3..0>	8 34
PCIE_TBT_D2R_P<3..0>	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_P<3..0>	8 34
PCIE_TBT_D2R_N<3..0>	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_N<3..0>	8 34
PCIE_TBT_D2R_C_P<3..0>	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_C_P<3..0>	34
PCIE_TBT_D2R_C_N<3..0>	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_C_N<3..0>	34
PCIE_CLK100M_TBT_P	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_TBT_P	16 34
PCIE_CLK100M_TBT_N	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_TBT_N	16 34
PEG_CLK100M_P	CLK_PCIE_80D	CLK_PCIE	PEG_CLK100M_P	8 16
PEG_CLK100M_N	CLK_PCIE_80D	CLK_PCIE	PEG_CLK100M_N	8 16
XDP_PCH_TDI	PCH_45S	PCH_ITP	XDP_PCH_TDI	16 23
XDP_PCH_TDO	PCH_45S	PCH_ITP	XDP_PCH_TDO	16 23
XDP_PCH_TMS	PCH_45S	PCH_ITP	XDP_PCH_TMS	16 23
XDP_PCH_TCK	PCH_45S	PCH_ITP	XDP_PCH_TCK	16 23

Chipset Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
DP_TBTSNK0_ML_P<3..0>	DP_80D	DP_TX	DP_TBTSNK0_ML_P<3..0>	34
DP_TBTSNK0_ML_N<3..0>	DP_80D	DP_TX	DP_TBTSNK0_ML_N<3..0>	34
DP_TBTSNK0_ML_C_P<3..0>	DP_80D	DP_TX	DP_TBTSNK0_ML_C_P<3..0>	8 34
DP_TBTSNK0_ML_C_N<3..0>	DP_80D	DP_TX	DP_TBTSNK0_ML_C_N<3..0>	8 34
DP_TBTSNK0_AUXCH_P	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_P	34
DP_TBTSNK0_AUXCH_N	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_N	34
DP_TBTSNK0_AUXCH_C_P	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_P	8 34
DP_TBTSNK0_AUXCH_C_N	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_N	8 34
DP_TBTSNK1_ML_P<3..0>	DP_80D	DP_TX	DP_TBTSNK1_ML_P<3..0>	34
DP_TBTSNK1_ML_N<3..0>	DP_80D	DP_TX	DP_TBTSNK1_ML_N<3..0>	34
DP_TBTSNK1_ML_C_P<3..0>	DP_80D	DP_TX	DP_TBTSNK1_ML_C_P<3..0>	8 34
DP_TBTSNK1_ML_C_N<3..0>	DP_80D	DP_TX	DP_TBTSNK1_ML_C_N<3..0>	8 34
DP_TBTSNK1_AUXCH_P	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_P	34
DP_TBTSNK1_AUXCH_N	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_N	34
DP_TBTSNK1_AUXCH_C_P	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_C_P	8 34
DP_TBTSNK1_AUXCH_C_N	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_C_N	8 34

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	SYSCLK_CLK32K_RTC	16 25
SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB	16 25
SYSCLK_CLK25M_SB_R	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB_R	16
SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT	25 34
SYSCLK_CLK25M_TBT_R	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R	34
SYSCLK_CLK25M_X1	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X1	25
SYSCLK_CLK25M_X2	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2	25
SYSCLK_CLK25M_X2_R	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2_R	25

DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
TBTDP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP_TX	TBTDP_TX	*	TBTDP_TX2TX
TBTDP_RX	TBTDP_RX	*	TBTDP_RX2RX
TBTDP_TX	TBTDP_RX	*	TBTDP_TX2RX
TBTDP_RX	TBTDP_TX	*	TBTDP_TX2RX
TBTDP_TX	*_TX	*	TBTDP_2OTHERHS
TBTDP_RX	*_TX	*	TBTDP_2OTHERHS
TBTDP_TX	*_RX	*	TBTDP_2OTHERHS
TBTDP_RX	*_RX	*	TBTDP_2OTHERHS
TBTDP_TX	*	*	TBTDP_2OTHER
TBTDP_RX	*	*	TBTDP_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
TBTDP_TX2TX	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_RX2RX	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_TX2RX	TOP,BOTTOM	=10x_DIELECTRIC	?
TBTDP_2OTHERHS	TOP,BOTTOM	=10x_DIELECTRIC	?
TBTDP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
TBTDP_TX2TX	*	=4x_DIELECTRIC	?
TBTDP_RX2RX	*	=4x_DIELECTRIC	?
TBTDP_TX2RX	*	=6x_DIELECTRIC	?
TBTDP_2OTHERHS	*	=6x_DIELECTRIC	?
TBTDP_2OTHER	*	=4x_DIELECTRIC	?

Thunderbolt/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
TBT_A_R2D	TBTDP_80D	TBTDP_TX	TBT_A_R2D_C_P<1..0> 34 64
TBT_A_R2D	TBTDP_80D	TBTDP_TX	TBT_A_R2D_C_N<1..0> 34 64
	TBTDP_80D	TBTDP_TX	TBT_A_R2D_P<1..0> 64
	TBTDP_80D	TBTDP_TX	TBT_A_R2D_N<1..0> 64
DP_TBTPA_ML1	DP_80D	DP_TX	DP_TBTPA_ML_C_P<1> 34 64
DP_TBTPA_ML1	DP_80D	DP_TX	DP_TBTPA_ML_C_N<1> 34 64
DP_TBTPA_ML3	DP_80D	DP_TX	DP_TBTPA_ML_C_P<3> 34 64
DP_TBTPA_ML3	DP_80D	DP_TX	DP_TBTPA_ML_C_N<3> 34 64
	DP_80D	DP_TX	DP_TBTPA_ML_P<3..1:2> 64
	DP_80D	DP_TX	DP_TBTPA_ML_N<3..1:2> 64
	DP_80D	DP_TX	DP_A_LSX_ML_P<1> 64
	DP_80D	DP_TX	DP_A_LSX_ML_N<1> 64
	TBTDP_80D	TBTDP_RX	TBT_A_D2R_C_P<1..0> 64
	TBTDP_80D	TBTDP_RX	TBT_A_D2R_C_N<1..0> 64
TBT_A_D2R1	TBTDP_80D	TBTDP_RX	TBT_A_D2R_P<1> 34 64
TBT_A_D2R1	TBTDP_80D	TBTDP_RX	TBT_A_D2R_N<1> 34 64
TBT_A_D2R0	TBTDP_80D	TBTDP_RX	TBT_A_D2R_P<0> 34 64
TBT_A_D2R0	TBTDP_80D	TBTDP_RX	TBT_A_D2R_N<0> 34 64
TBT_A_AUXCH	DP_80D	DP_AUX	DP_TBTPA_AUXCH_C_P 34 64
TBT_A_AUXCH	DP_80D	DP_AUX	DP_TBTPA_AUXCH_C_N 34 64
	DP_80D	DP_AUX	DP_TBTPA_AUXCH_P 64
	DP_80D	DP_AUX	DP_TBTPA_AUXCH_N 64
	DP_80D	DP_AUX	DP_A_AUXCH_DDC_P 64
	DP_80D	DP_AUX	DP_A_AUXCH_DDC_N 64
	TBTDP_80D	TBTDP_RX	TBT_A_D2R1_AUXDDC_P 64
	TBTDP_80D	TBTDP_RX	TBT_A_D2R1_AUXDDC_N 64
TBT_B_R2D	TBTDP_80D	TBTDP_TX	TBT_B_R2D_C_P<1..0> 8 34
TBT_B_R2D	TBTDP_80D	TBTDP_TX	TBT_B_R2D_C_N<1..0> 8 34
	TBTDP_80D	TBTDP_TX	TBT_B_R2D_P<1..0> 64
	TBTDP_80D	TBTDP_TX	TBT_B_R2D_N<1..0> 64
DP_TBTPB_ML	DP_80D	DP_TX	DP_TBTPB_ML_C_P<3..1:2> 8 34
DP_TBTPB_ML	DP_80D	DP_TX	DP_TBTPB_ML_C_N<3..1:2> 8 34
	DP_80D	DP_TX	DP_TBTPB_ML_P<3..1:2> 64
	DP_80D	DP_TX	DP_TBTPB_ML_N<3..1:2> 64
	DP_80D	DP_TX	DP_B_LSX_ML_P<1> 64
	DP_80D	DP_TX	DP_B_LSX_ML_N<1> 64
	TBTDP_80D	TBTDP_RX	TBT_B_D2R_C_P<1..0> 64
	TBTDP_80D	TBTDP_RX	TBT_B_D2R_C_N<1..0> 64
TBT_B_D2R	TBTDP_80D	TBTDP_RX	TBT_B_D2R_P<1..0> 8 34
TBT_B_D2R	TBTDP_80D	TBTDP_RX	TBT_B_D2R_N<1..0> 8 34
TBT_B_AUXCH	DP_80D	DP_AUX	DP_TBTPB_AUXCH_C_P 8 34
TBT_B_AUXCH	DP_80D	DP_AUX	DP_TBTPB_AUXCH_C_N 8 34
	DP_80D	DP_AUX	DP_TBTPB_AUXCH_P 64
	DP_80D	DP_AUX	DP_TBTPB_AUXCH_N 64
	DP_80D	DP_AUX	DP_B_AUXCH_DDC_P 64
	DP_80D	DP_AUX	DP_B_AUXCH_DDC_N 64
	TBTDP_80D	TBTDP_RX	TBT_B_D2R1_AUXDDC_P 64
	TBTDP_80D	TBTDP_RX	TBT_B_D2R1_AUXDDC_N 64

Only used on dual-port hosts.

Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
	DP_80D	DP_TX	DP_TBTSRC_ML_C_P<3..0> 34
	DP_80D	DP_TX	DP_TBTSRC_ML_C_N<3..0> 34
	DP_80D	DP_AUX	DP_TBTSRC_AUXCH_C_P 34
	DP_80D	DP_AUX	DP_TBTSRC_AUXCH_C_N 34
TBT_SPI_CLK	TBT_SPI_45S	TBT_SPI	TBT_SPI_CLK 34
TBT_SPI_MOSI	TBT_SPI_45S	TBT_SPI	TBT_SPI_MOSI 34
TBT_SPI_MISO	TBT_SPI_45S	TBT_SPI	TBT_SPI_MISO 34
TBT_SPI_CS_L	TBT_SPI_45S	TBT_SPI	TBT_SPI_CS_L 34

Only used on hosts supporting Thunderbolt video-in

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



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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

NET TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
 SMBUS_SMC_0_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_0_S0_SCL 41 44
 SMBUS_SMC_0_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_0_S0_SDA 41 44
 SMBUS_SMC_1_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SCL 41 44
 SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SDA 41 44
 SMBUS_SMC_2_S3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_2_S3_SCL 41 44
 SMBUS_SMC_2_S3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_2_S3_SDA 41 44
 SMBUS_SMC_3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_3_SCL 41 44
 SMBUS_SMC_3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_3_SDA 41 44
 SMBUS_SMC_5_G3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_5_G3_SCL 41 44
 SMBUS_SMC_5_G3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_5_G3_SDA 41 44


SMBus Charger Net Properties

NET TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
 SENSE_DIFFPAIR	1:1_DIFFPAIR		CHGR_CSI_P 53
 SENSE_DIFFPAIR	1:1_DIFFPAIR		CHGR_CSI_N 53
 SENSE_DIFFPAIR	1:1_DIFFPAIR		CHGR_CSI_R_P 53
 SENSE_DIFFPAIR	1:1_DIFFPAIR		CHGR_CSI_R_N 53
 SENSE_DIFFPAIR	1:1_DIFFPAIR		CHGR_CSO_P 53
 SENSE_DIFFPAIR	1:1_DIFFPAIR		CHGR_CSO_N 53
 SENSE_DIFFPAIR	1:1_DIFFPAIR		CHGR_CSO_R_P 53
 SENSE_DIFFPAIR	1:1_DIFFPAIR		CHGR_CSO_R_N 53

SYNC MASTER=J13 CONSTRAINTS

SYNC DATE=01/11/2012

SMC Constraints

 Apple Inc.

DRAWING NUMBER

051-9277

SIZE

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REVISION

2.8.0

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PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
SENSE_1TO1_45S	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
SENSE_1TO1_P2MM	*	=1:1_DIFFPAIR	0.200_MM	0.100_MM	=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_45S	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
SPKR_DIFFPAIR	*	=1:1_DIFFPAIR	0.300_MM	0.100_MM	=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?
























































SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
GND_P2MM	*	0.20_MM	1000
PWR_P2MM	*	0.20_MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	CLK_PCIE	*	GND_P2MM
GND	PCIE*	*	GND_P2MM
GND	SATA*	*	GND_P2MM
GND	USB*	*	GND_P2MM
GND	LVDS*	*	GND_P2MM
SB_POWER	CLK_PCIE	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM


J11/J13 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
 SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	INLET_THMSNS_D1_P	46 47
 SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	INLET_THMSNS_D1_N	46 47
 SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBT_THERMD_P	47
 SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBT_THERMD_N	47
 SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBT_MLBBOT_THMSNS_P	47
 SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBT_MLBBOT_THMSNS_N	47
 SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBTTHMSNS_D2_R_P	47
 SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBTTHMSNS_D2_R_N	47
 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPU_THERMD_P	9 47
 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPU_THERMD_N	9 47
 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUTHMSNS_D2_P	47
 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUTHMSNS_D2_N	47
 SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUVCCIOS0_CS_N	45 59
 SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUVCCIOS0_CS_P	45 59
 SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISNS1_P	45 57 58
 SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISNS1_N	45 58
 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUIMVP_ISUM_R_P	45
 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUIMVP_ISUM_R_N	45
 SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISNS1G_P	45 58
 SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISNS1G_N	45 58
 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUIMVP_ISUMG_R_P	45
 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUIMVP_ISUMG_R_N	45
 SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	VCCSAS0_CS_P	45 54
 SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	VCCSAS0_CS_N	45 54
 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	VCCSAISNS_R_P	45
 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	VCCSAISNS_R_N	45
 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_3V3S0_P	45 61
 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_3V3S0_N	45 61
 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_3V3S0_R_P	45
 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_3V3S0_R_N	45
 SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISUMG_P	57 58
 SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISUMG_N	57 58
 SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISUM_P	57 58
 SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISUM_N	57 58
 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_N	8 46
 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_P	8 46
 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER_N	46
 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER_P	46
 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V5_S3_N	46 56
 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V5_S3_P	46 56
 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_N	37 46
 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_P	37 46
 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_SSD_N	38 46
 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_SSD_P	38 46
 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_N	8 46
 SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_P	8 46
 AUD_DIFF	1:1_DIFFPAIR	AUDIO	SPKRAMP_INR_P	6 40 51
 AUD_DIFF	1:1_DIFFPAIR	AUDIO	SPKRAMP_INR_N	6 40 51
 SENSE_DIFFPAIR	1:1_DIFFPAIR	AUDIO	MAX98300_R_P	51
 SENSE_DIFFPAIR	1:1_DIFFPAIR	AUDIO	MAX98300_R_N	51
 SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT_P	6 51 52
 SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT_N	6 51 52
 SB_POWER		SB_POWER	PP3V3_S5	6 7
 SB_POWER		SB_POWER	PP3V3_S0	6 7
 GND		GND	GND	

SYNC MASTER=J13 CONSTRAINTS

SYNC DATE=01/11/2012

Project Specific Constraints

 Apple Inc.

DRAWING NUMBER

051-9277

SIZE

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REVISION

2.8.0

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J11/J13 Board-Specific Spacing & Physical Constraints

BOARD LAYERS				BOARD AREAS		BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM				NO_TYPE, BGA		MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
DEFAULT	TOP, BOTTOM	Y	=50_OHM_SE	=50_OHM_SE			
DEFAULT	ISL2, ISL11	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	ISL3, ISL10	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	ISL4, ISL9	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	*	N	100 MM	100 MM	10 MM	0 MM	0 MM
STANDARD	*	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT

Single-ended Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
27P4_OHM_SE	TOP, BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	ISL2, ISL11	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	ISL3, ISL10	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	ISL4, ISL9	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
35_OHM_SE	TOP, BOTTOM	Y	0.195 MM	0.195 MM			
35_OHM_SE	ISL2, ISL11	Y	0.125 MM	0.125 MM			
35_OHM_SE	ISL3, ISL10	Y	0.125 MM	0.125 MM			
35_OHM_SE	ISL4, ISL9	Y	0.125 MM	0.125 MM			
35_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
40_OHM_SE	TOP, BOTTOM	Y	0.170 MM	0.170 MM			
40_OHM_SE	ISL2, ISL11	Y	0.096 MM	0.096 MM			
40_OHM_SE	ISL3, ISL10	Y	0.096 MM	0.096 MM			
40_OHM_SE	ISL4, ISL9	Y	0.099 MM	0.099 MM			
40_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
45_OHM_SE	TOP, BOTTOM	Y	0.135 MM	0.135 MM			
45_OHM_SE	ISL2, ISL11	Y	0.075 MM	0.075 MM			
45_OHM_SE	ISL3, ISL10	Y	0.075 MM	0.075 MM			
45_OHM_SE	ISL4, ISL9	Y	0.080 MM	0.080 MM			
45_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
50_OHM_SE	TOP, BOTTOM	Y	0.110 MM	0.110 MM			
50_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
55_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Differential Pair Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
72_OHM_DIFF	TOP, BOTTOM	Y	0.165 MM	0.165 MM		0.130 MM	0.130 MM
72_OHM_DIFF	ISL2, ISL11	Y	0.109 MM	0.109 MM		0.150 MM	0.150 MM
72_OHM_DIFF	ISL3, ISL10	Y	0.109 MM	0.109 MM		0.150 MM	0.150 MM
72_OHM_DIFF	ISL4, ISL9	Y	0.114 MM	0.114 MM		0.150 MM	0.150 MM
72_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
80_OHM_DIFF	TOP, BOTTOM	Y	0.132 MM	0.132 MM		0.130 MM	0.130 MM
80_OHM_DIFF	ISL2, ISL11	Y	0.081 MM	0.081 MM		0.115 MM	0.115 MM
80_OHM_DIFF	ISL3, ISL10	Y	0.081 MM	0.081 MM		0.115 MM	0.115 MM
80_OHM_DIFF	ISL4, ISL9	Y	0.088 MM	0.088 MM		0.110 MM	0.110 MM
80_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD


Spacing Constraints

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
1:1_SPACING	*	0.100 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
1x_DIELECTRIC	TOP, BOTTOM	0.071 MM	?
1x_DIELECTRIC	ISL3, ISL10	0.053 MM	?
1x_DIELECTRIC	ISL4, ISL9	0.050 MM	?
1x_DIELECTRIC	*	0.090 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM

SYNC MASTER=J13 CONSTRAINTS		SYNC DATE=01/11/2012	
PAGE TITLE			
PCB Rule Definitions			
 Apple Inc.		DRAWING NUMBER	SIZE
		051-9277	D
		REVISION	
		2.8.0	
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