

# K36C MLB SCHEMATIC

APR/10/2009

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.  
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.  
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.


REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
02		691395	ENGINEERING RELEASED	04/09/09	?

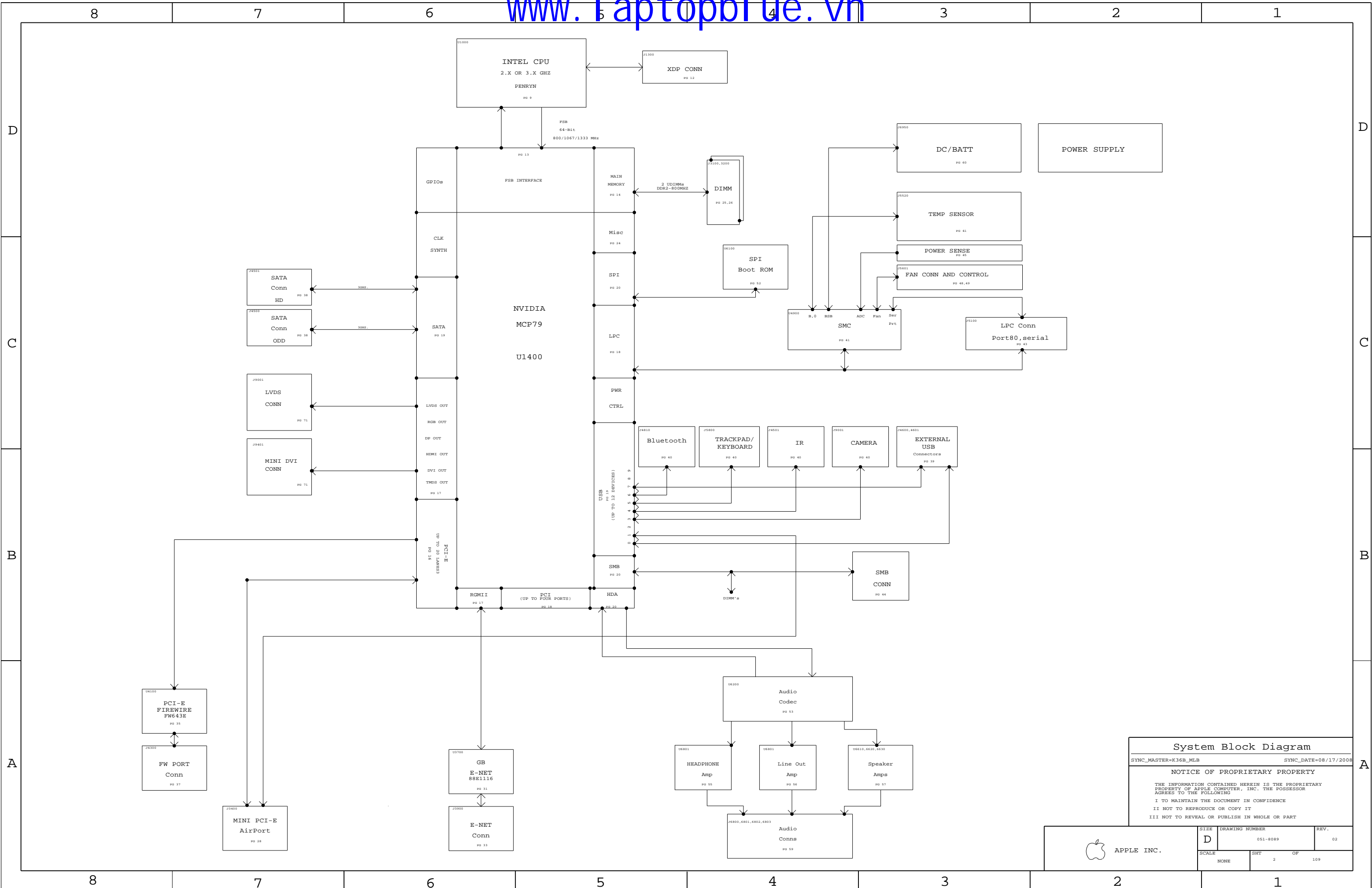
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Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8089	1	SCHEM, MLB, K36C	SCH	CRITICAL	
820-2496	1	PCBF, MLB, K36B	PCB	CRITICAL	

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		SIZE D		REV. 02	
				SHT 1 OF 109	



**System Block Diagram**

SYNC\_MASTER=K36B\_MLB SYNC\_DATE=08/17/2008

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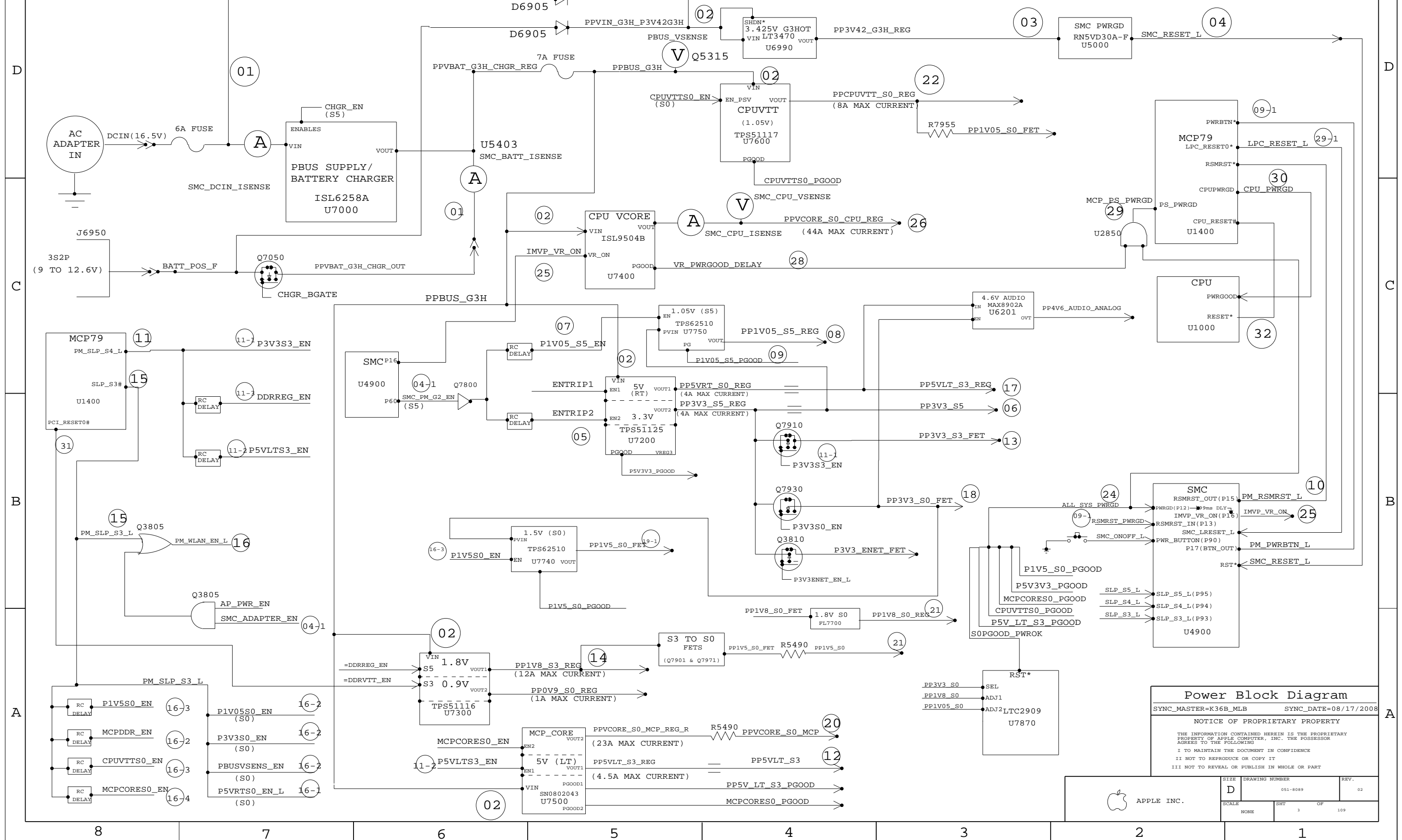
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# K36B POWER SYSTEM ARCHITECTURE



Page Notes

Power aliases required by this page:  
(NONE)

Signal aliases required by this page:  
(NONE)

BOM options provided by this page:  
(NONE)

BOM OPTION

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S2420	1	IC, SMC, HSB/2117, 8X9MM, TLP, HF, BLANK	U4900	CRITICAL	SMC_PROG
341S2418	1	IC, FLASH, SPI, 32MBIT, 3.3V, 86MHZ, 8-SOP	U6100	CRITICAL	BOOTROM_PROG
341S2093	1	IC, CYPRESS, CY7C63833	U4800	CRITICAL	
338S0654	1	IC, PM643E, 1394B PHY/ONC1 LINK/PCI-E, 127	U4100	CRITICAL	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
826-4393	1	LBL, P/N LABEL, PCB, 28MMX6MM	[EEE:3TN]	CRITICAL	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S3769	1	PCD, SLOTT, 2.26, 25W, 1046, R0, 3W, BGA, P7750	U1000	CRITICAL	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0702	1	IC, ONCIP, MCP79, 35X35MM, BGA1437, R03	U1400	CRITICAL	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0694	1	IC, RTL8251CA-VB-GR, GIGE TRANSCEIVER, 48P	U3700	CRITICAL	

ALTERNATES OPTION

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0218		ALL	ALTERNATE PER CYNDI
152S0694	152S0138		ALL	ALTERNATE PER CYNDI
152S0847	152S0586		ALL	ALTERNATE PER CYNDI
152S0874	152S0516		ALL	ALTERNATE PER CYNDI
152S0796	152S0685		ALL	ALTERNATE PER CYNDI
152S0778	152S0693		ALL	ALTERNATE PER CYNDI
157S0058	157S0055		ALL	ALTERNATE PER CYNDI

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0665	1	CONN, RCPT, MINI-DVI, 32P, R/A	J9401	CRITICAL	
514-0666	1	CONN, RCPT, 3.5MM AUDIO IN, R/A	J6750	CRITICAL	
514-0667	1	CONN, RCPT, 3.5MM AUDIO OUT, R/A	J6700	CRITICAL	
514-0668	1	CONN, RCPT, RJ45, NO FILTER, 8P	J3900	CRITICAL	
514-0669	1	CONN, RCPT, USB, 4P, MIDPLANE	J4600	CRITICAL	
514-0669	1	CONN, RCPT, USB, 4P, MIDPLANE	J4601	CRITICAL	

BOARD STACK-UP AND CONSTRUCTION

Top	SIGNAL
2	GROUND
3	SIGNAL(High Speed)
4	SIGNAL(High Speed)
5	GROUND
6	POWER
7	POWER
8	GROUND
9	SIGNAL(High Speed)
10	SIGNAL(High Speed)
11	GROUND
BOTTOM	SIGNAL

CONFIGURATION OPTIONS

SYNC\_MASTER=K36B\_MLB    SYNC\_DATE=08/17/2008

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DRAWING NUMBER

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REV.

02

SCALE

NONE

SHT

4

OF

109

8		7	6	5	4	3	2	1	
D	<div>Revision History</div> <div>*****2008/08/21*****</div> <div>PAGE 61:</div> <div>- U7500 PIN V5DRV1 LINK TO PP5V_S0_MCPREG_VCC.</div> <div>- U7500 PIN TONSEL LINK TO GND DIRECTLY.</div> <div>PAGE 64:</div> <div>- R7859 CHANGE TO 100 OHM.</div> <div>- R7879 CHANGE TO 100K OHM.</div> <div>PAGE 65:</div> <div>- DELETE 1.05V S0 FET CIRCUIT.</div> <div>PAGE 57:</div> <div>- R7011 CHANGE TO 9.31K OHM, 1%</div> <div>*****2008/08/22*****</div> <div>PAGE 7:</div> <div>- ADD SMC_EXCARD_PWR_EN TEST_POINT</div> <div>PAGE 8:</div> <div>- ADD =PP3V42_G3H_RTC_D LINK TO =PP3V42_G3H_REG</div> <div>PAGE 14:</div> <div>- R1410 CHANGE TO 49.9 OHM</div> <div>- CHANGE R1440 TO 150_5% AND NO STUFF</div> <div>PAGE 26:</div> <div>- R2872 CHANGE TO 0OHM</div> <div>- RTC FOLLOW M97 DESIGN AND USE SUPERCAP SOLUTION</div> <div>- MCP S0 PWRGD FOLLOW M97 DESIGN</div> <div>PAGE 29:</div> <div>- PULL R3240 DOWN TO GND. PULL R3241 HIGH</div> <div>PAGE 32,33,34</div> <div>- FOLLOW M97 DESIGN</div> <div>PAGE 39:</div> <div>- D4600/D4601/PIN-6 CONNECT TO USB VBUS (FOLLOW M97D)</div> <div>PAGE 44:</div> <div>- R5270/R5271 = 1K (FOLLOW M97D)</div> <div>- R5280/R5281 = 1K (FOLLOW M97D)</div> <div>PAGE 68:</div> <div>- CHANGE C9411, C9412 TO 220PF</div> <div>- CHANGE R9462, R9463 TO 2.7KOHM</div> <div>- ADD C9480 0.1UF_16V_0402 FROM GND_CHASSIS_TMDS_DOWN TO GND</div> <div>- CHANGE R9460,R9461 TO 0OHM,</div> <div>- CHANG C9442 AND C9443 TO 47PF</div> <div>*****2008/08/23*****</div> <div>MODIFY ALL NOSTUFF TO NO STUFF.</div> <div>PAGE 6:</div> <div>- REMOVE ETHERNET CIRCUIT.</div> <div>PAGE 8:</div> <div>- ADD =PP3V3_S5_P3V3ENETFET LINK TO PP3V3_S5</div> <div>- ADD =PP1V05_ENET_PHY LINK TO PP1V2R1V05_ENET.</div> <div>PAGE 9:</div> <div>- ADD =RTL8211_ENSWRE LINK TO GND.</div> <div>- ADD =PP3V3_ENET_PHY_VDDREG LINK TO TP_PP3V3_ENET_PHY_VDDREG.</div> <div>- ADD =RTL8211_REGOUT LINK TO NC_RTL8211_REGOUT.</div> <div>- =P3V3ENET_EN_L LINK TO PM_SLP_RMG_T_L</div> <div>- =P1V05ENET_EN LINK TO PM_SLP_RMG_T_L</div> <div>PAGE 10:</div> <div>- CHANGE XDP_TDO_CONN TO XDP_TDO</div> <div>PAGE 13:</div> <div>- XDP FOLLOW M98 DESIGN. CONNECTOR FROM 516S0625 CHANGE TO 998-1571.</div> <div>PLAGE 23:</div> <div>- DELETE R2400-R2413 FOR MCP A01 VERSION.</div> <div>PAGE 31:</div> <div>- REMOVE R3400, R3401</div> <div>- L3401 FROM NO STUFF CHANGE TO STUFF.</div> <div>PAGE 39</div> <div>- DELETE R4699.</div> <div>- R4690 FROM NO STUFF CHANGE TO STUFF.</div> <div>PAGE 41:</div> <div>- SMC_NB_DDR_ISENSE CHANGE TO SMC_MCP_DDR_ISENSE</div> <div>- SMC_NB_CORE_ISENSE CHANGE TO SMC_MCP_CORE_ISENSE</div> <div>PAGE 46:</div> <div>- SMC_NB_DDR_ISENSE CHANGE TO SMC_MCP_DDR_ISENSE</div> <div>- SMC_NB_CORE_ISENSE CHANGE TO SMC_MCP_CORE_ISENSE</div> <div>- R5417 ADD BOM OPTION FOR NO STUFF</div> <div>- R5416 ADD BOM OPTION FOR NO STUFF</div> <div>PAGE 50:</div> <div>- ADD C5926 (10UF,20%.0603) TO =PP3V3_S3_SMS</div> <div>PAGE 63:</div> <div>- REMOVE USB_PWR_EN_S3</div> <div>PAGE 66:</div> <div>- REMOVE R9010, R9011</div> <div>*****2008/08/24*****</div> <div>PAGE 6:</div> <div>- R0602 BOMOPTION FROM JTAG_1DEV CHANGE TO NO STUFF.</div> <div>PAGE 13:</div> <div>- XDP FOLLOW M97 DESIGN. CONNECTOR FROM 998-1571 CHANGE TO 516S0625.</div> <div>PAGE 18:</div> <div>- R1860 AND R1861 CHANGE TO PAGE 68.</div> <div>PAGE 25:</div> <div>- C2504-C2507 FROM 138S0578(402) CHANGE TO 138S0614(402-1)</div> <div>- C2516-C2517 FROM 138S0578(402) CHANGE TO 138S0614(402-1)</div> <div>PAG3 35:</div> <div>- R4150 FROM 118S0343 (0201) CHANGE TO 116S0056(0402)</div> <div>PAGE 58:</div> <div>- C7281, C7241, C7272 FROM 138S0555(603) CHANGE TO 138S0615(603-1)</div> <div>- C7280, C7240 FROM 128S0092(POLY) CHANGE TO 128S0128(POLY-TANT)</div> <div>- C7291, C7292, C7252, C7251 FROM 128S0115(POLY,CASE-B2) CHANGE TO 128S0222(POLY,CASE-B2-SM)</div> <div>- Q7260, Q7261 FROM 376S0512 CHANGE TO 376S0652 (H-F)</div> <div>PAGE 59:</div> <div>- Q7320 FROM 376S0512 CHANGE TO 376S0652 (H-F)</div> <div>- Q7321 FROM 376S0511 CHANGE TO 376S0651 (H-F)</div> <div>- C7321 FROM 128S0111(POLY) CHANGE TO 128S0218 (POLY,CASE-D2E-SM)</div> <div>- C7343 FROM 128S0073 CHANGE TO 128S0233.</div> <div>PAGE 60:</div> <div>- XW7400 ADD BOMOPTION OMIT.</div> <div>- Q7400, Q7402 FROM 376S0472 CHANGE TO 376S0617.</div> <div>PAGE 61:</div> <div>- L7500 FROM 152S0869 CHANGE TO 152S0685.</div> <div>- Q7500 FROM 376S0512 CHANGE TO 376S0652.</div> <div>- C7560 FROM 128S0092 CHANGE TO 128S0218.</div> <div>PAGE 62:</div> <div>- Q7620 FROM 376S0512 CHANGE TO 376S0652.</div> <div>- C7601 FROM 138S0578 CHANGE TO 138S0614.</div>								
	<div>*****2008/08/25*****</div> <div>CHANGE CSA BASE ON WILL'S SUGGESTION.</div> <div>PAGE 9:</div> <div>- ADD GMUX_JTAG_TMS AND GMUX_JTAG_TDI IN MISC NC MCP79 ALIASES.</div> <div>PAGE 18:</div> <div>- NETNAME ENET_INTR_L CHANGE TO TP_ENET_INTR_L.</div> <div>- ENET_PWRDWN_L CHANGE TO TP_ENET_PWRDWN_L</div> <div>PAGE 19:</div> <div>- DELETE R1987,R1988,R1995,R1970,R1971,R1972,R1973,R1996,R1997,R1998,R1999,R1978,R1979</div> <div>(FOLLOW M97 DESIGN).</div> <div>- NET DPMUX_LOWPWR_L SYNC M97 NETNAME AUD_IPHS_SWITCH_EN</div> <div>- NET LVDSMUX_SEL_IG_L SYNC M97 NETNAME</div> <div>- NET DPMUX_SEL_IG_L SYNC M97 NETNAME</div> <div>PAGE 28:</div> <div>- REMOVE NET DIMM_OVERTEMPA_L</div> <div>PAGE 29:</div> <div>- REMOVE NET DIMM_OVERTEMPA_L</div> <div>PAGE 42:</div> <div>- ADD SMC_EXCARD_PWR_EN TO TP_SMC_EXCARD_PWR_EN</div> <div>- ADD SMC_RSTGATE_L TO TP_SMC_RSTGATE_L</div> <div>- ADD ALS_GAIN TO NC_ALS_GAIN</div> <div>- ADD ESTARLDO_EN TO NC_ESTARLDO_EN</div> <div>- ADD SMC_ANALOG_ID TO NC_SMC_ANALOG_ID</div> <div>- ADD SMC_SYS_KBDLED TO NC_SMC_SYS_KBDLED</div> <div>- ADD R5054 10KOHM LINK SMC_GPU_ISENSE PULL DOWN TO GND.</div> <div>- ADD R5055 10KOHM LINK SMC_NB_MISC_ISENSE PULL DOWN TO GND.</div> <div>PAGE 43:</div> <div>- R5142 CHANGE TO NO STUFF.</div> <div>PAGE 46:</div> <div>- R5416 CHANGE TO 4.53K AND DELETE BOM OPTION.</div> <div>- R5417 CHANGE TO 4.53K AND DELETE BOM OPTION.</div> <div>- R5418 CHANGE TO 4.53K AND DELETE BOM OPTION.</div> <div>PAGE 57:</div> <div>- NETNAME FROM CHGR LOWCURRENT REF CHANGE TO CHGR_LOWCURRENT_REF</div> <div>- NETNAME FROM CHGR LOWCURRENT GATE CHANGE TO CHGR_LOWCURRENT_GATE</div> <div>PAGE :</div> <div>- REMOVE R7884 AND C7884</div> <div>PAGE 66:</div> <div>- REMOVE J9001 PIN 20 AND PIN21 NET.</div> <div>*****2008/09/02*****</div> <div>PAGE 45:</div> <div>- CHANGE ODD CONNECTOR FROM 516S0720 TO 516S0719</div> <div>*****2008/09/27*****</div> <div>PAGE 9:</div> <div>- ADD STANDOFF 860-0964 X 4</div> <div>- ADD STANDOFF 860-0723 X 1</div> <div>- ADD STANDOFF 860-0749 X 1</div> <div>PAGE 29:</div> <div>- REMOVE BOMOPTION TABLE OF R2903/R2905/R2909/R2911</div> <div>PAGE 66:</div> <div>- C6601/C6603 CHANGE TO APN 128S0135, and REMOVE BOMOPTION OMIT</div> <div>- C6605 CHANGE TO APN 128s0148, HF APN 128s0221, and REMOVE BOMOPTION OMIT</div> <div>PAGE 68:</div> <div>- C6830/C6831 CHANGE TO APN 128S0220, and REMOVE BOMOPTION OMIT</div> <div>PAGE 72:</div> <div>- R7272 CHANGE FROM 57.6K 1%(114s0389) TO 75K 1%(114s0399)</div> <div>*****2008/10/20*****</div> <div>PAGE 29:</div> <div>- ADD R2903/R2905 BOMOTION AND CHANGE VALUE TO 200 OHM</div> <div>PAGE 50:</div> <div>- REMOVE ALT TABLE</div> <div>PAGE 74:</div> <div>- REMOVE ALT TABLE</div> <div>PAGE 94:</div> <div>- REMOVE K36 BOM OPTION TABLE AND ALT TABLE</div> <div>*****2008/10/22*****</div> <div>PAGE 12:</div> <div>- C1200 ~ C1219 CHANGE TO 138S0580</div> <div>PAGE 28:</div> <div>- C2870 CHANGE TO 138S0614</div> <div>PAGE 37:</div> <div>- ADD R3731 (116s0026 22 ohm 5% 0402) FOR EMI 125MHZ NOISE</div> <div>- TP_RTL8211_CLK125 CHANGE TO RTL8211_CLK125</div> <div>PAGE 48:</div> <div>- C4803 CHANGE TO 138S0614</div> <div>PAGE 66:</div> <div>- C6605 CHANGE TO HF APN 128S0221</div> <div>PAGE 70:</div> <div>- C7040/C7041/C7047 CHANGE TO 138S0614</div> <div>PAGE 90:</div> <div>- L9002 CHANGE TO 116S0004(0ohm,5%,0402)</div> <div>- C9003 CHANGE TO 116S0004(0ohm,5%,0402)</div> <div>*****2008/10/24*****</div> <div>PAGE 19:</div> <div>- R1950/R1951/R1952/1953 CHANGE TO 116s0004 (0 OHM,5%,0402)</div> <div>PAGE 28:</div> <div>- R2825/R2826 CHANGE TO 116s0004 (0 OHM,5%,0402)</div> <div>PAGE 34:</div> <div>- J3400 516S0635 CHANGE TO HF APN 516S0729</div> <div>PAGE 52:</div> <div>- ADD C5250/C5251/C5270/C5271/C5260/C5261/C5281 131S1104 (22pF,5%,0402) NO STUFF</div> <div>- TEXT "ALS" CHANGE TO "MINI-PCIE"</div> <div>- I2C_ALS_SCL CHANGE TO I2C_MINI_PCIE_SCL</div> <div>- I2C_ALS_SDA CHANGE TO I2C_MINI_PCIE_SDA</div> <div>PAGE 67:</div> <div>- J6700 514-0604 CHANGE TO HF APN 514-0521</div> <div>- J6750 514-0603 CHANGE TO HF APN 514-0519</div> <div>PAGE 69:</div> <div>- J6950 516S0620 CHANGE TO HF APN 516S0735</div> <div>*****2008/10/25*****</div> <div>PAGE 52:</div> <div>- STUFF C5250/C5251/C5270/C5271/C5260/C5261/C5280/C5281</div> <div>*****2008/10/28*****</div> <div>PAGE 34:</div> <div>- J3400 516S0729 CHANGE TO 516S0635</div> <div>*****2008/10/30*****</div> <div>PAGE 69:</div> <div>- J6950 516S0735 CHANGE TO 516S0620</div>								
	<div>*****2008/10/31*****</div> <div>PAGE 41:</div> <div>- U4100 CHANGE FROM 338S0523 TO 338S0654</div> <div>*****2008/11/01*****</div> <div>PAGE 4:</div> <div>- BOM change U1400 CHANGE FROM 338S0678 TO 338S0702</div> <div>*****2008/11/05*****</div> <div>PAGE 62:</div> <div>- C6210 CHANGE FROM 127S0062 TO 127S0108</div> <div>PAGE 68:</div> <div>- C6832, C6833 CHANGE FROM 127S0062 TO 127S0108</div> <div>PAGE 45:</div> <div>- DELETE L4502, NET SATA_HDD_D2R_UF_P / SATA_HDD_D2R_UF_N</div> <div>- L4501 / F14520 / FL4525 CHANGE FROM 155S0303 TO 155S0371</div> <div>PAGE 102:</div> <div>- DELETE PHYSICAL/SPACING SETTING OF SATA_HDD_D2R_UF_P / SATA_HDD_D2R_UF_N</div> <div>*****2008/11/06*****</div> <div>- U5413 CHANGE FROM 353S1432 TO 353S2220</div> <div>- R7417 CHANGE FROM 5.36K(114S0289) TO 4.42K(114S0280)</div> <div>*****2008/11/12*****</div> <div>- U1000 CHANGE FROM 373S3646 TO 373S3702</div> <div>*****2008/11/19*****</div> <div>- J6950 CHANGE FROM 516S0620 TO 516S0735</div> <div>- J9401 CHANGE FROM 514-0517 TO 514-0665</div> <div>- J6750 CHANGE FROM 514-0519 TO 514-0666</div> <div>- J6700 CHANGE FROM 514-0521 TO 514-0667</div> <div>- J3900 CHANGE FROM 514-0523 TO 514-0668</div> <div>- J4600, J4601 CHANGE FROM 514-0527 TO 514-0669</div> <div>- U3700 CHANGE FROM 338S0570 TO 338S0694</div> <div>*****2008/11/26*****</div> <div>- PAGE 61 NOTE : CORRECT REFERENCE TO R5164 AND R5144</div> <div>- J3400 CHANGE TO 516S0729</div> <div>*****2008/12/12*****</div> <div>- R5144 and R5164 changed to 10K 5% 0402 (116S0090)</div> <div>*****2008/12/17*****</div> <div>- U4900 symbol update</div> <div>*****2008/12/20*****</div> <div>- R5156, R5157, R5158 change from 0 to 33 ohm, 5%, 0402(116s0030)</div>								

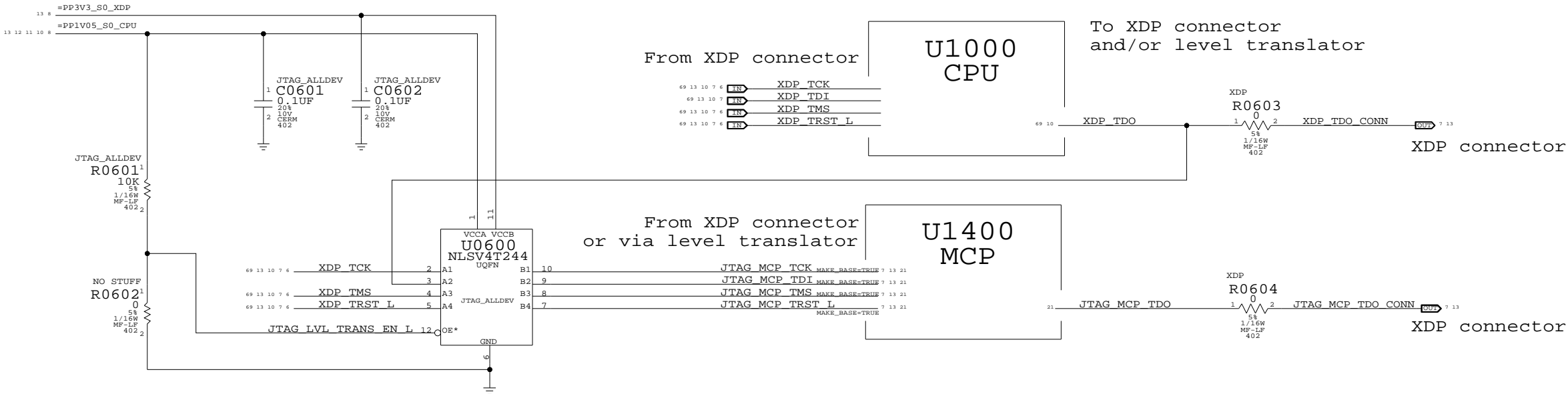
C								
B								
A								

NOTE: All page numbers are .csa, not PDF. See page 1 for .csa -> PDF mapping.

D

D

1.05V TO 3.3V LEVEL TRANSLATOR (K36B: ON ICT FIXTURE)



C

C


B

B

A

A

JTAG Scan Chain		
SYNC_MASTER=K36B_MLB		SYNC_DATE=08/17//2008
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 APPLE INC.	SIZE D	DRAWING NUMBER 051-8089	REV. 02
	SCALE NONE	SHT 6 OF 109	

Functional Test Points

D

#J5601 Fan Connectors

#J5601	TRUE	PP5VRT_S0	7 8
#J5601	TRUE	FAN_RT_PWM	48
#J5601	TRUE	FAN_RT_TACH	48
#J5601	TRUE	GND	

#J6950 Battery/Lid Connector

#J6950	TRUE	SMC_BS_ALRT_L_F	56
#J6950	TRUE	SMBUS_BATT_SCL_F	56
#J6950	TRUE	SMBUS_BATT_SDA_F	56
#J6950	TRUE	PPVBAT_G3H_CONN_F	56
#J6950	TRUE	SMC_LID_F	56
#J6950	TRUE	GND_SMC_LID_F	56
#J6950	TRUE	PP3V42_G3H_LIDSWITCH_F	56
#J6950	TRUE	GND	Need 6 TP

#J6900 MagSafe DC Power Jack

#J6900	TRUE	PP18V5_DCIN_FUSE	Need 2 TP
#J6900	TRUE	ADAPTER_SENSE	56
#J6900	TRUE	GND	Need 2 TP

#J9000 INVERTER Connector

#J9000	TRUE	PPBUS_ALL_INV_CONN	Need 2 TP
#J9000	TRUE	INV_GND	66
#J9000	TRUE	PP5V_INV_F	66
#J9000	TRUE	INV_BKLIGHT_PWM_L	Need 4 TP

#J9001 LCD + CAMERA CONNECTOR

#J9001	TRUE	PP3V3_LCDVDD_SW_F	66
#J9001	TRUE	PP3V3_S0_LCD_F	66
#J9001	TRUE	LVDS_IG_DDC_CLK	18 66
#J9001	TRUE	LVDS_IG_DDC_DATA	18 66
#J9001	TRUE	LVDS_IG_A_DATA_N<0>	18 66 71
#J9001	TRUE	LVDS_IG_A_DATA_P<0>	18 66 71
#J9001	TRUE	LVDS_IG_A_DATA_N<1>	18 66 71
#J9001	TRUE	LVDS_IG_A_DATA_P<1>	18 66 71
#J9001	TRUE	LVDS_IG_A_DATA_N<2>	18 66 71
#J9001	TRUE	LVDS_IG_A_DATA_P<2>	18 66 71
#J9001	TRUE	LVDS_IG_A_CLK_F_N	66
#J9001	TRUE	LVDS_IG_A_CLK_F_P	66
#J9001	TRUE	USB2_CAMERA_CONN_P	66 72
#J9001	TRUE	USB2_CAMERA_CONN_N	66 72
#J9001	TRUE	PP5V_S3_CAMERA_F	66
#J9001	TRUE	GND	

# J6701 MIC CONNECTOR

#J6701	TRUE	MIC_LO_CONN	54
#J6701	TRUE	MIC_HI_CONN	54
#J6701	TRUE	MIC_SHLD_CONN	54 55

#J6702 Left SPEAKER CONNECTOR

#J6702	TRUE	SPKRCONN_L_P_OUT	53 54
#J6702	TRUE	SPKRCONN_L_N_OUT	53 54

#J6703 Right SUB SPEAKER CONNECTOR

#J6703	TRUE	SPKRCONN_SUB_P_OUT	53 54
#J6703	TRUE	SPKRCONN_SUB_N_OUT	53 54
#J6703	TRUE	SPKRCONN_R_P_OUT	53 54
#J6703	TRUE	SPKRCONN_R_N_OUT	53 54

# J5800 GEYSER AND DIMM0 REMOTE TEMP SENSORS

#J5800	TRUE	TPAD_GND_F	49
#J5800	TRUE	CONN_TPAD_ONOFF_FLTR_L	49
#J5800	TRUE	CONN_TPAD_USB_P	49 72
#J5800	TRUE	CONN_TPAD_USB_N	49 72
#J5800	TRUE	SMC_LID_LC	49
#J5800	TRUE	PP5V_S3_TPAD_F	49

#J5520 CPU/MCP Thermal Sensor

#J5520	TRUE	CPUTHMSNS_D2_P	47
#J5520	TRUE	CPUTHMSNS_D2_N	47
#J5520	TRUE	MCPTHMSNS_D2_P	47
#J5520	TRUE	MCPTHMSNS_D2_N	47

#J4810 BLUETOOTH

#J4810	TRUE	PP3V3_S3_BT_F_CONN	40
#J4810	TRUE	USB2_BT_F_N_CONN	40 72
#J4810	TRUE	USB2_BT_F_P_CONN	40 72
#J4810	TRUE	GND_BT_F_CONN	40

#J4500 SATA ODD

#J4500	TRUE	SATA_ODD_R2D_UF_P	38 71
#J4500	TRUE	SATA_ODD_R2D_UF_N	38 71
#J4500	TRUE	SATA_ODD_D2R_C_N	38 71
#J4500	TRUE	SATA_ODD_D2R_C_P	38 71
#J4500	TRUE	PP3V3_S0	Need 4 TP
#J4500	TRUE	SMC_ODD_DETECT	38 41
#J4500	TRUE	GND	Need 6 TP

# J4501 SATA HD System LED and IR

#J4501	TRUE	SATA_HDD_R2D_P	38 71
#J4501	TRUE	SATA_HDD_R2D_N	38 71
#J4501	TRUE	SATA_HDD_D2R_C_N	38 71
#J4501	TRUE	SATA_HDD_D2R_C_P	38 71
#J4501	TRUE	PP5V_S0_HDD_FLT	Need 4 TP
#J4501	TRUE	SYS_LED_ANODE_L	38
#J4501	TRUE	IR_RX_OUT	38 40
#J4501	TRUE	PP5V_S3_IR_CONN	38
#J4501	TRUE	GND	Need 4 TP

#J3400 Airport

#J3400	TRUE	PCIE_WAKE_L	17 31
#J3400	TRUE	MINI_CLKREQ_L	17 31
#J3400	TRUE	PCIE_CLK100M_MINI_N	17 31 71
#J3400	TRUE	PCIE_CLK100M_MINI_P	17 31 71
#J3400	TRUE	PCIE_MINI_D2R_N	17 31 71
#J3400	TRUE	PCIE_MINI_D2R_P	17 31 71
#J3400	TRUE	PCIE_MINI_R2D_N	31 71
#J3400	TRUE	PCIE_MINI_R2D_P	31 71
#J3400	TRUE	PP3V3_WLAN	Need 4 TP
#J3400	TRUE	PP1V5_S0_R	Need 3 TP
#J3400	TRUE	MINI_RESET	31
#J3400	TRUE	PP3V3_S3_AIRPORT_CONN	31
#J3400	TRUE	I2C_MINI_PCIE_SCL	31 44
#J3400	TRUE	I2C_MINI_PCIE_SDA	31 44
#J3400	TRUE	USB2_AIRPORT_N	31 72
#J3400	TRUE	USB2_AIRPORT_P	31 72
#J3400	TRUE	GND	Need 6 TP

# Other Func Test Points

#J3400	TRUE	ALL_SYS_PWRGD	26 41 64
#J3400	TRUE	PPVCORE_S0_CPU	8
#J3400	TRUE	PPCPUVTT_S0	7 8
#J3400	TRUE	PPVCORE_S0_MCP_R	8
#J3400	TRUE	PPVCORE_S0_MCP	8
#J3400	TRUE	PP0V9_S0	8
#J3400	TRUE	PP1V05_S0	7 8
#J3400	TRUE	PP1V5_S0_R	7 8
#J3400	TRUE	PP1V8_S0	8
#J3400	TRUE	PP1V8_S0_R	8
#J3400	TRUE	PP1V05_S0_MCP_PEX_AVDD	8 24
#J3400	TRUE	PP1V05_S0	7 8
#J3400	TRUE	PP1V05_S0_MCP_SATA_AVDD	8 24
#J3400	TRUE	PP1V05_S0	7 8
#J3400	TRUE	PP5VRT_S0	7 8
#J3400	TRUE	PP3V3_S0	7 8
#J3400	TRUE	PP1V0_FW	8
#J3400	TRUE	PP1V8_S3	8
#J3400	TRUE	PP3V3_S3	8
#J3400	TRUE	PP5VLT_S3	8
#J3400	TRUE	PPVTT_S3_DDR_BUF	8
#J3400	TRUE	PP1V05_S5_REG	8
#J3400	TRUE	PP3V3_S5	8
#J3400	TRUE	PP3V42_G3H	7 8
#J3400	TRUE	PP18V5_G3H	8
#J3400	TRUE	PPBUS_G3H	8
#J3400	TRUE	PPBUS_G3H_CPU_ISNS	8
#J3400	TRUE	PP3V3_ENET_PHY	8
#J3400	TRUE	PP1V2R1V05_ENET	8
#J3400	TRUE	PPVP_FW	8

#J1300 XDP

#J1300	TRUE	XDP_BPM_L<5>	10 13 69
#J1300	TRUE	XDP_BPM_L<4>	10 13 69
#J1300	TRUE	XDP_BPM_L<3>	10 13 69
#J1300	TRUE	XDP_BPM_L<2>	10 13 69
#J1300	TRUE	XDP_BPM_L<1>	10 13 69
#J1300	TRUE	XDP_BPM_L<0>	10 13 69
#J1300	TRUE	TP_XDP_OBSFN_B0	13
#J1300	TRUE	TP_XDP_OBSFN_B1	13
#J1300	TRUE	TP_XDP_OBSDATA_B0	13
#J1300	TRUE	TP_XDP_OBSDATA_B1	13
#J1300	TRUE	TP_XDP_OBSDATA_B2	13
#J1300	TRUE	TP_XDP_OBSDATA_B3	13
#J1300	TRUE	XDP_PWRGD	13
#J1300	TRUE	XDP_OBS20	13
#J1300	TRUE	PM_LATRIGGER_L	13 19
#J1300	TRUE	JTAG_MCP_TCK	6 13 21
#J1300	TRUE	SMBUS_MCP_0_DATA	13 21 44 72
#J1300	TRUE	SMBUS_MCP_0_CLK	13 21 44 72
#J1300	TRUE	XDP_TCK	6 10 13 69
#J1300	TRUE	PPCPUVTT_S0	7 8
#J1300	TRUE	PP3V3_S0	7 8
#J1300	TRUE	JTAG_MCP_TDO_CONN	6 13
#J1300	TRUE	JTAG_MCP_TRST_L	6 13 21
#J1300	TRUE	MCP_DEBUG<0>	13 19 72
#J1300	TRUE	MCP_DEBUG<1>	13 19 72
#J1300	TRUE	MCP_DEBUG<2>	13 19 72
#J1300	TRUE	MCP_DEBUG<3>	13 19 72
#J1300	TRUE	JTAG_MCP_TDI	6 13 21
#J1300	TRUE	JTAG_MCP_TMS	6 13 21
#J1300	TRUE	MCP_DEBUG<4>	13 19 72
#J1300	TRUE	MCP_DEBUG<5>	13 19 72
#J1300	TRUE	MCP_DEBUG<6>	13 19 72
#J1300	TRUE	MCP_DEBUG<7>	13 19 72
#J1300	TRUE	FSB_CLK_ITP_P	13 14 69
#J1300	TRUE	FSB_CLK_ITP_N	13 14 69
#J1300	TRUE	XDP_CPUST_L	13 69
#J1300	TRUE	XDP_DBRESET_L	10 13 26
#J1300	TRUE	XDP_TDO_CONN	6 13
#J1300	TRUE	XDP_TRST_L	6 10 13 69
#J1300	TRUE	XDP_TDI	6 10 13 69
#J1300	TRUE	XDP_TMS	6 10 13 69
#J1300	TRUE	GND	Need 8 TP

# J5100 LPC+SPI Connector

#J5100	TRUE	PP3V42_G3H	7 8
#J5100	TRUE	PP5VRT_S0	7 8
#J5100	TRUE	LPC_AD<0>	19 41 43 72
#J5100	TRUE	LPC_AD<1>	19 41 43 72
#J5100	TRUE	SPI_ALT_MOSI	43
#J5100	TRUE	SPI_ALT_MISO	43
#J5100	TRUE	LPC_FRAME_L	19 41 43 72
#J5100	TRUE	PM_CLKRUN_L	19 41 43
#J5100	TRUE	SMC_TMS	41 42 43
#J5100	TRUE	DEBUG_RESET_L	26 43
#J5100	TRUE	SMC_TDO	41 42 43
#J5100	TRUE	SMC_TRST_L	41 43
#J5100	TRUE	SMC_MD1	41 43
#J5100	TRUE	SMC_TX_L	39 41 42 43
#J5100	TRUE	LPC_CLK33M_LPCPLUS	26 43 72
#J5100	TRUE	LPC_AD<2>	19 41 43 72
#J5100	TRUE	LPC_AD<3>	19 41 43 72
#J5100	TRUE	SPIROM_USE_MLB	43
#J5100	TRUE	SPI_ALT_CLK	43
#J5100	TRUE	SPI_ALT_CS_L	43
#J5100	TRUE	LPC_SERIRQ	19 41 43
#J5100	TRUE	LPC_PWRDWN_L	19 41 43
#J5100	TRUE	SMC_TDI	41 42 43
#J5100	TRUE	SMC_TCK	41 42 43
#J5100	TRUE	SMC_RESET_L	41 42 43
#J5100	TRUE	SMC_NMI	41 43
#J5100	TRUE	SMC_RX_L	39 41 42 43
#J5100	TRUE	LPCPLUS_GPIO	18 43
#J5100	TRUE	GND	Need 2 TP

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FUNC TEST

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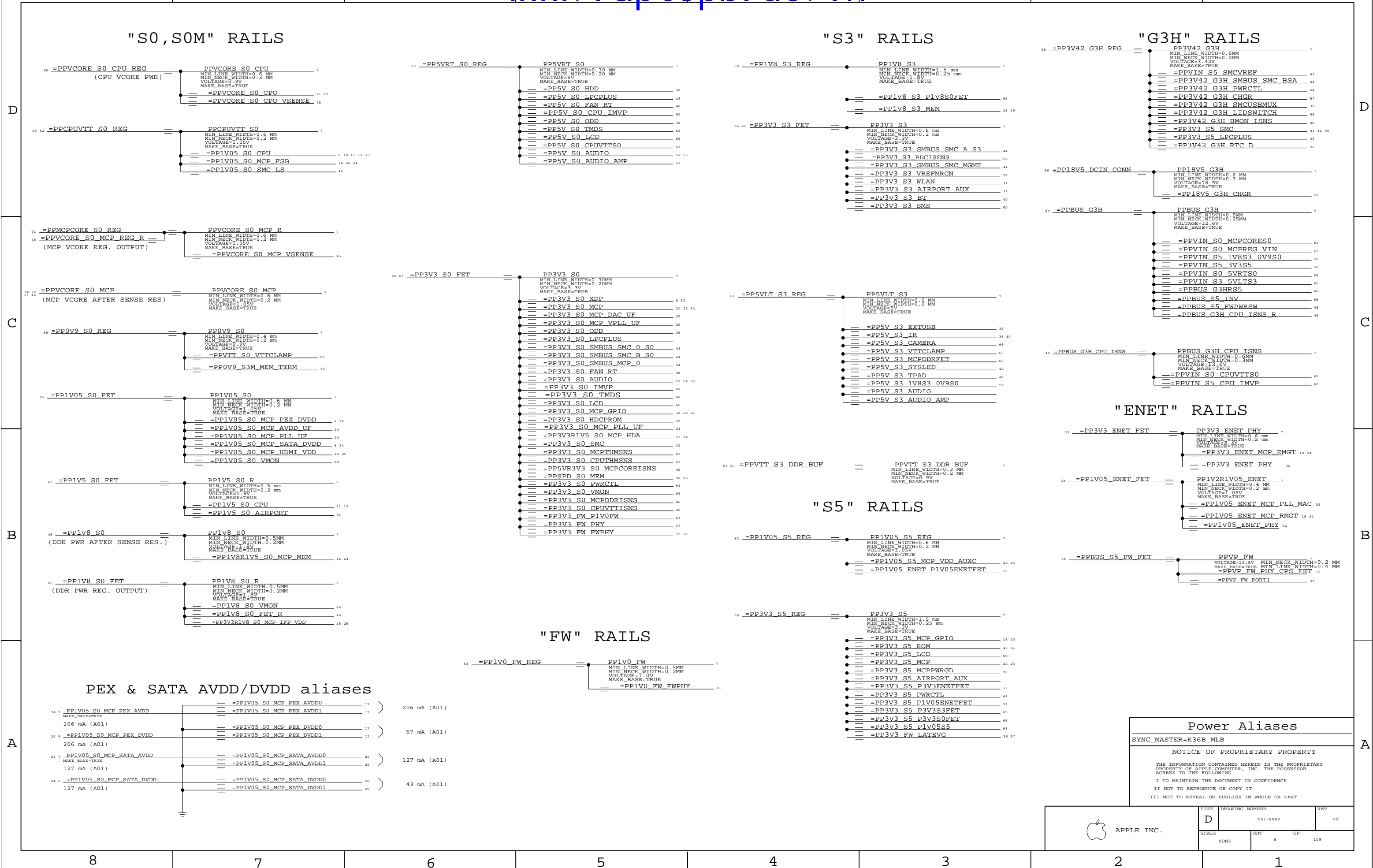
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PCI-E ALIASES

UNUSED GPU LANES

17	=PEG D2R N<15:0>	=	NC PEG D2R N<15:0>	NO_TEST=TRUE	MAKE_BASE=TRUE
17	=PEG D2R P<15:0>	=	NC PEG D2R P<15:0>	NO_TEST=TRUE	MAKE_BASE=TRUE
17	=PEG R2D C N<15:0>	=	NC PEG R2D C N<15:0>	NO_TEST=TRUE	MAKE_BASE=TRUE
17	=PEG R2D C P<15:0>	=	NC PEG R2D C P<15:0>	NO_TEST=TRUE	MAKE_BASE=TRUE
17	PEG PRSNT L	=	TP PEG PRSNT L	MAKE_BASE=TRUE	
17	PEG CLKREQ L	=	TP PEG CLKREQ L	MAKE_BASE=TRUE	
17	PEG CLK100M P	=	TP PEG CLK100MP	MAKE_BASE=TRUE	
17	PEG CLK100M N	=	TP PEG CLK100MN	MAKE_BASE=TRUE	
17	EXTGPU PWR EN	=	TP EXTGPU PWR EN	MAKE_BASE=TRUE	
17	EXTGPU RESET L	=	TP EXTGPU RESET L	MAKE_BASE=TRUE	

ETHERNET ALIASES

33	=P3V3ENET_EN	=	PM SLP RMGT L	MAKE_BASE=TRUE	21
33	=P1V05ENET_EN	=			
32	=PP3V3_ENET_PHY_VDDREG	=	PP3V3_ENET_PHY_VDDREG	MAKE_BASE=TRUE	
32	=RTL8211_REGOUT	=	NC RTL8211_REGOUT	MAKE_BASE=TRUE	
32	=RTL8211_ENSWREG	=			

LVDS ALIASES

UNUSED LVDS SIGNALS

71	18	LVDS IG A DATA P<3>	=	NC LVDS IG A DATA P3	NO_TEST=TRUE	MAKE_BASE=TRUE
71	18	LVDS IG A DATA N<3>	=	NC LVDS IG A DATA N3	NO_TEST=TRUE	MAKE_BASE=TRUE
71	18	LVDS IG B CLK P	=	NC LVDS IG B CLKP	NO_TEST=TRUE	MAKE_BASE=TRUE
71	18	LVDS IG B CLK N	=	NC LVDS IG B CLKN	NO_TEST=TRUE	MAKE_BASE=TRUE
71	18	LVDS IG B DATA P<3:0>	=	NC LVDS IG B DATA P<3:0>	NO_TEST=TRUE	MAKE_BASE=TRUE
71	18	LVDS IG B DATA N<3:0>	=	NC LVDS IG B DATA N<3:0>	NO_TEST=TRUE	MAKE_BASE=TRUE

MISC NC MCP79 ALIASES

14	CPU PECI MCP	=	TP CPU PECI MCP	MAKE_BASE=TRUE
19	GMUX JTAG TDI	=	TP GMUX JTAG TDI	MAKE_BASE=TRUE
19	GMUX JTAG TMS	=	TP GMUX JTAG TMS	MAKE_BASE=TRUE
16	MCP MEM RESET L	=	TP MCP MEM RESET L	MAKE_BASE=TRUE

SO-DIMM ALIASES

UNUSED ADDRESS PINS

28	MEM A A<15>	=	TP MEM A A15	MAKE_BASE=TRUE
29	MEM B A<15>	=	TP MEM B A15	MAKE_BASE=TRUE

UNUSED EXPRESS CARD LANE

71	17	PCIE_EXCARD_D2R_P	=	TP_PCIE_EXCARD_D2RP	MAKE_BASE=TRUE
71	17	PCIE_EXCARD_D2R_N	=	TP_PCIE_EXCARD_D2RN	MAKE_BASE=TRUE
71	17	PCIE_EXCARD_R2D_C_P	=	TP_PCIE_EXCARD_R2D_CP	MAKE_BASE=TRUE
71	17	PCIE_EXCARD_R2D_C_N	=	TP_PCIE_EXCARD_R2D_CN	MAKE_BASE=TRUE
17	PCIE_EXCARD_PRSNT_L	=	TP_PCIE_EXCARD_PRSNT_L	MAKE_BASE=TRUE	
17	EXCARD_CLKREQ_L	=	TP_EXCARD_CLKREQ_L	MAKE_BASE=TRUE	
71	17	PCIE_CLK100M_EXCARD_P	=	TP_PCIE_CLK100M_EXCARD_P	MAKE_BASE=TRUE
71	17	PCIE_CLK100M_EXCARD_N	=	TP_PCIE_CLK100M_EXCARD_N	MAKE_BASE=TRUE

USB ALIASES

UNUSED USB PORTS

72	20	USB_EXTCP_P	=====	TP USB_EXTCP	MAKE_BASE=TRUE
72	20	USB_EXTCP_N	=====	TP USB_EXTCN	MAKE_BASE=TRUE
72	20	USB_EXTDP_P	=====	TP USB_EXTDP	MAKE_BASE=TRUE
72	20	USB_EXTDP_N	=====	TP USB_EXTDN	MAKE_BASE=TRUE
72	20	USB_EXCARD_P	=====	TP USB_EXCARDP	MAKE_BASE=TRUE
72	20	USB_EXCARD_N	=====	TP USB_EXCARDN	MAKE_BASE=TRUE
31		=USB_MINI_P	=====	USB_MINI_P	20 72
31		=USB_MINI_N	=====	USB_MINI_N	20 72

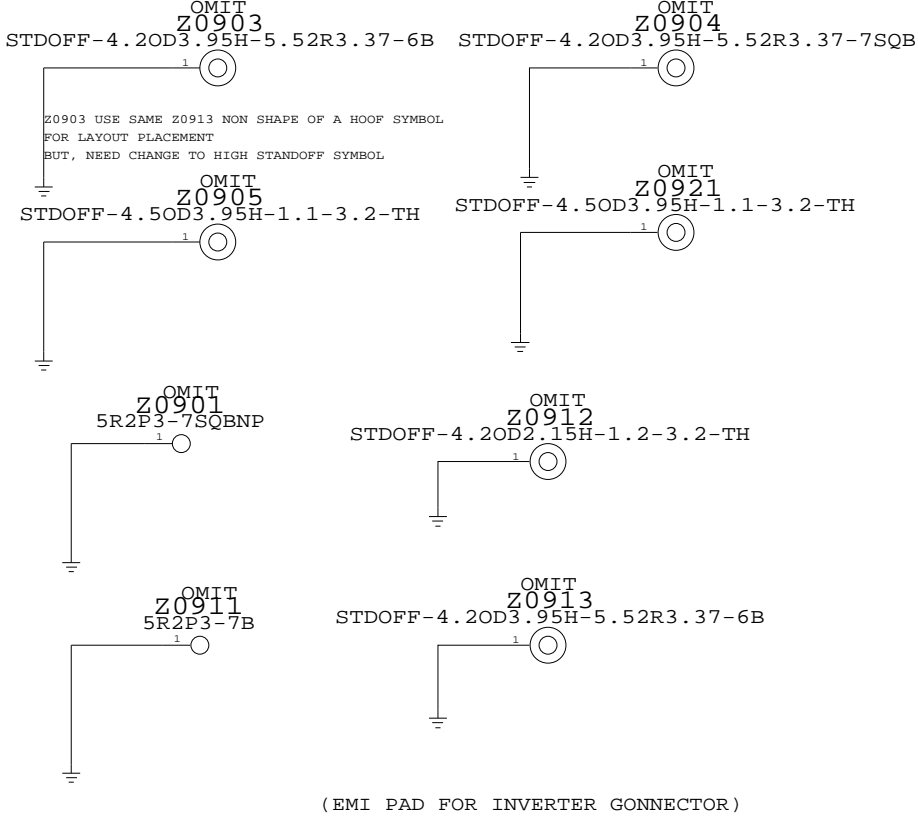
TRACKPAD (WELLSPRING)

49	=USB2_TPAD_P	=	USB_TPAD_P	MAKE_BASE=TRUE	20	72
49	=USB2_TPAD_N	=	USB_TPAD_N	MAKE_BASE=TRUE	20	72

BLUETOOTH

40	=USB2_BT_P	=	USB_BT_P	MAKE_BASE=TRUE	20	72
40	=USB2_BT_N	=	USB_BT_N	MAKE_BASE=TRUE	20	72

CPU HEATSINK STANDOFF SCREW HOLE



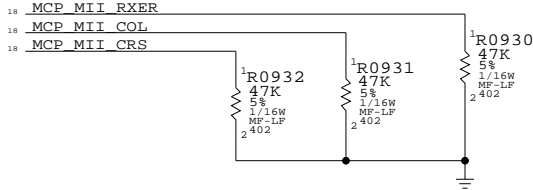
CPU FSB FREQUENCY STRAPS

BSEL<2..0>	FSB MHZ
0 0 0	266
0 0 1	133
0 1 0	200
0 1 1	(166)
1 0 0	100
1 0 1	333
1 1 1	(400) (RSVD)

HDA PULL-DOWN



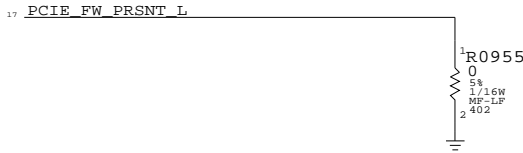
LAN ALIASES



DP HOTPLUG PULL-DOWN

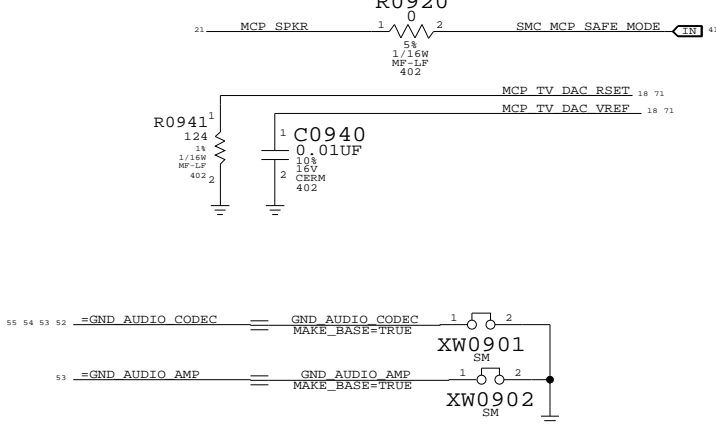


FW PULL-DOWN



MCP\_SAFE\_MODE SIGNAL TO SUPPORT

ROM FAILURE OVERRIDE



SIGNAL ALIAS

SYNC\_MASTER=K36B\_MLB

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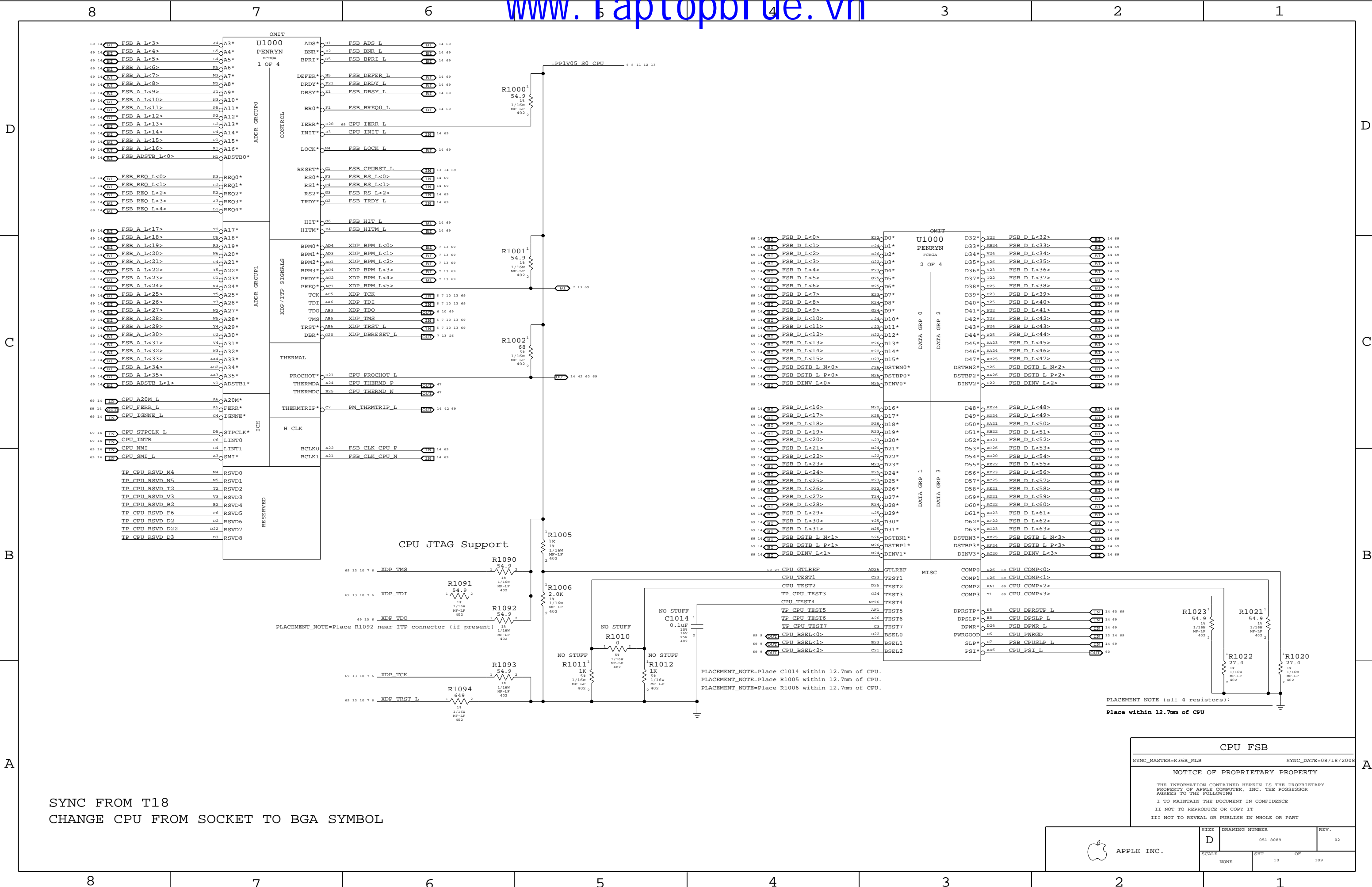
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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
860-0964	4	THERMAL STANDOFF	Z0903, Z0904, Z0905, Z0921	?	STANDOFF
860-0723	1	STANDOFF WIRELESS	Z0912	?	STANDOFF
860-0749	1	STANDOFF W/THRU HOLES, WIRELESS	Z0913	?	STANDOFF



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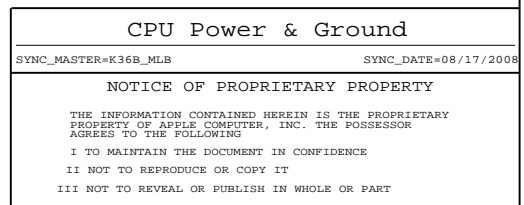



SYNC FROM T18  
CHANGE CPU FROM SOCKET TO BGA SYMBOL

CPU FSB  
SYNC\_MASTER=K36B\_MLB  
SYNC\_DATE=08/18/2008  
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Current numbers from Merom for Santa Rosa EMTS, doc #20905.



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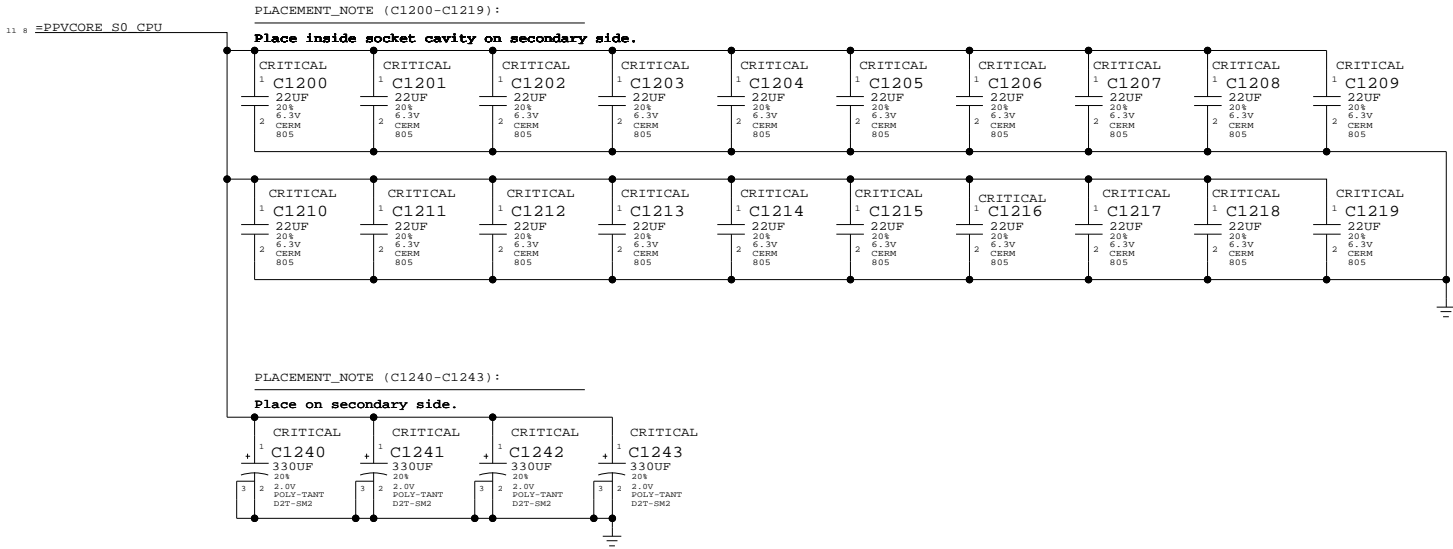
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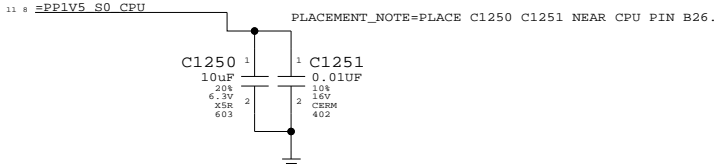
### CPU VCore HF and Bulk Decoupling

6x 330uF. 32x 22uF 0805 (20 stuffed)



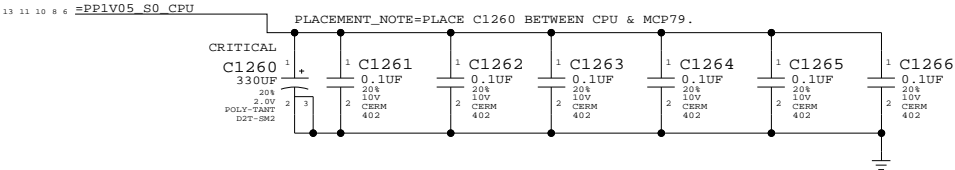
### VCCA (CPU AVdd) DECOUPLING

1x 10uF, 1x 0.01uF



### VCCP (CPU I/O) DECOUPLING

1x 330uF, 6x 0.1uF 0402



SYNC FROM T18

#### CPU Decoupling

SYNC\_MASTER=K36B\_MLB

SYNC\_DATE=08/17/2008

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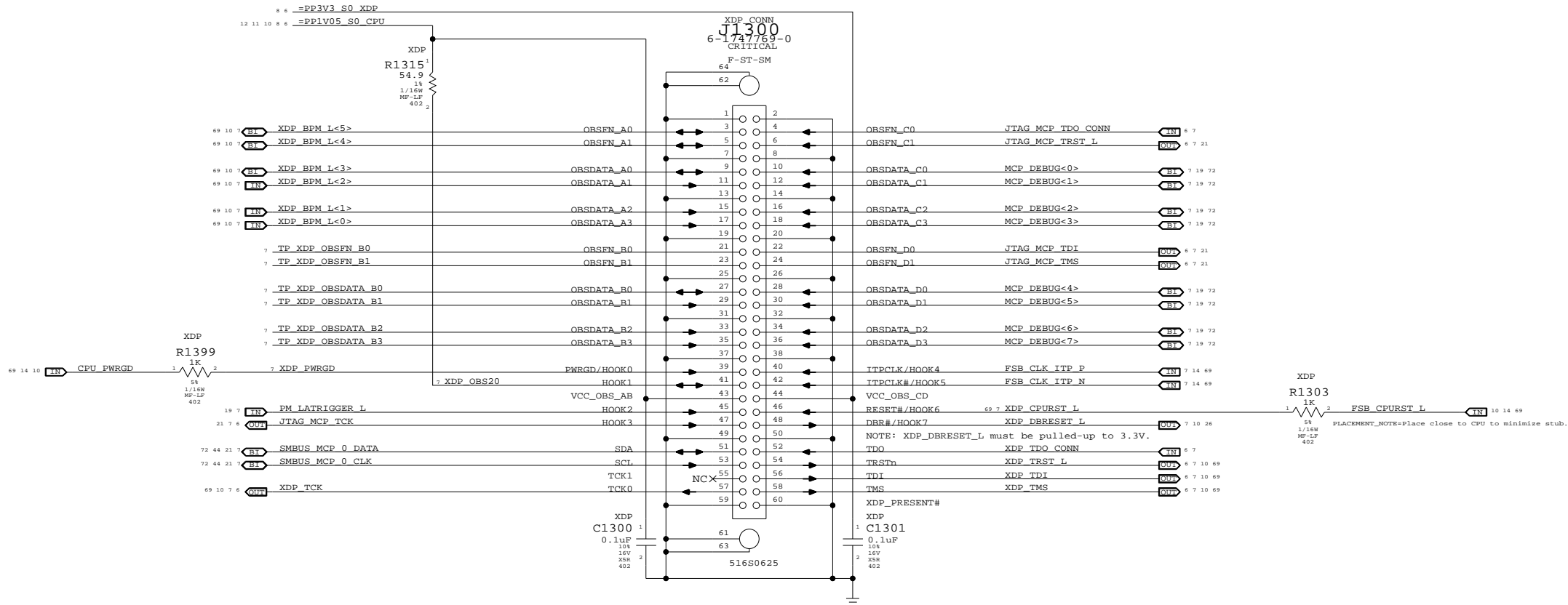
SHT  
12

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109

Mini-XDP Connector

NOTE: This is not the standard XDP pinout.  
Use with 920-0620 adapter board to support CPU, MCP debugging.

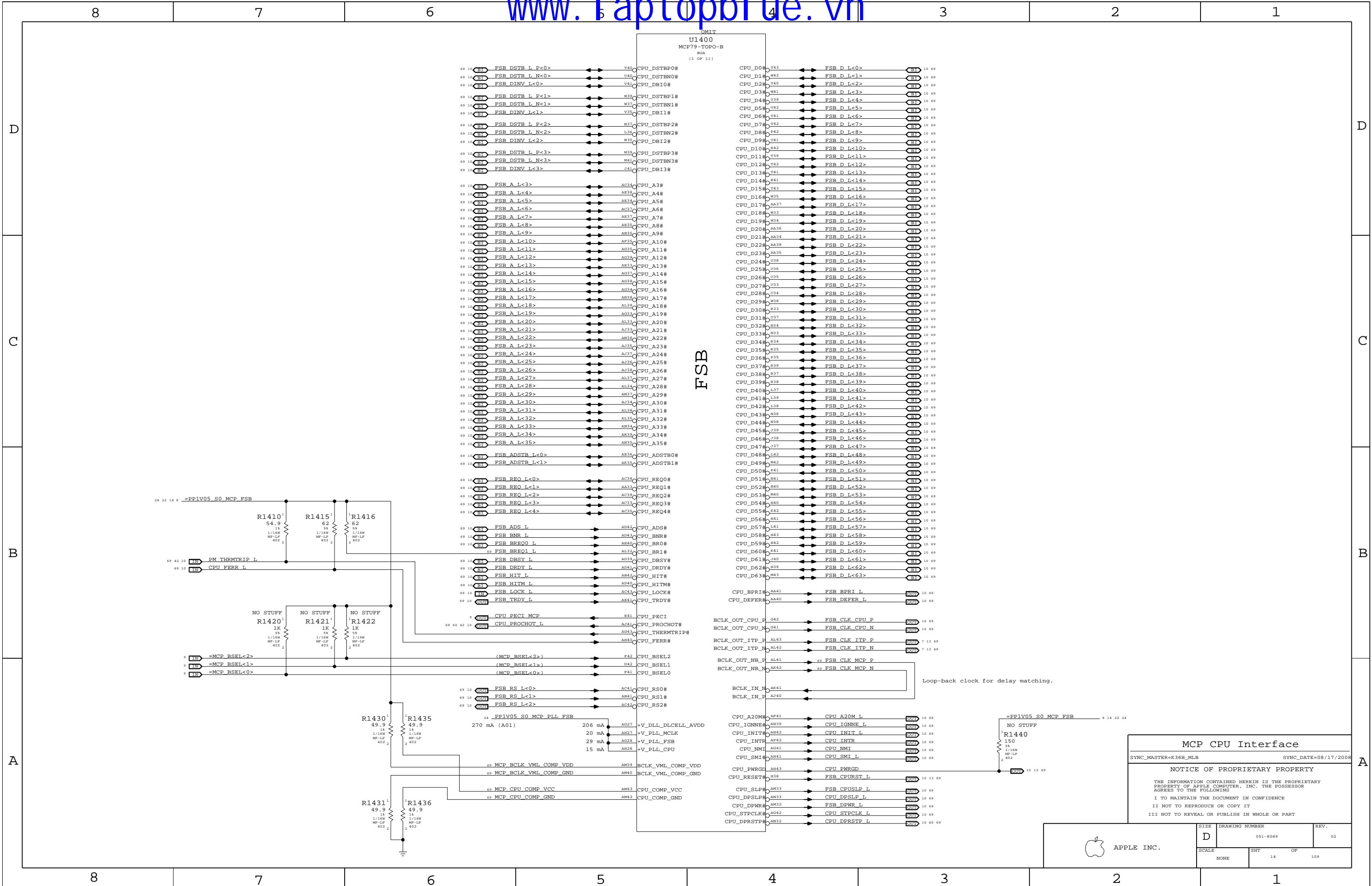
MCP79-specific pinout



Direction of XDP module  
Please avoid any obstructions  
on even-numbered side of J1300

eXtended Debug Port (MiniXDP)  
SYNC\_MASTER=M99\_MLB SYNC\_DATE=01/08/2008  
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MCP Memory Interface

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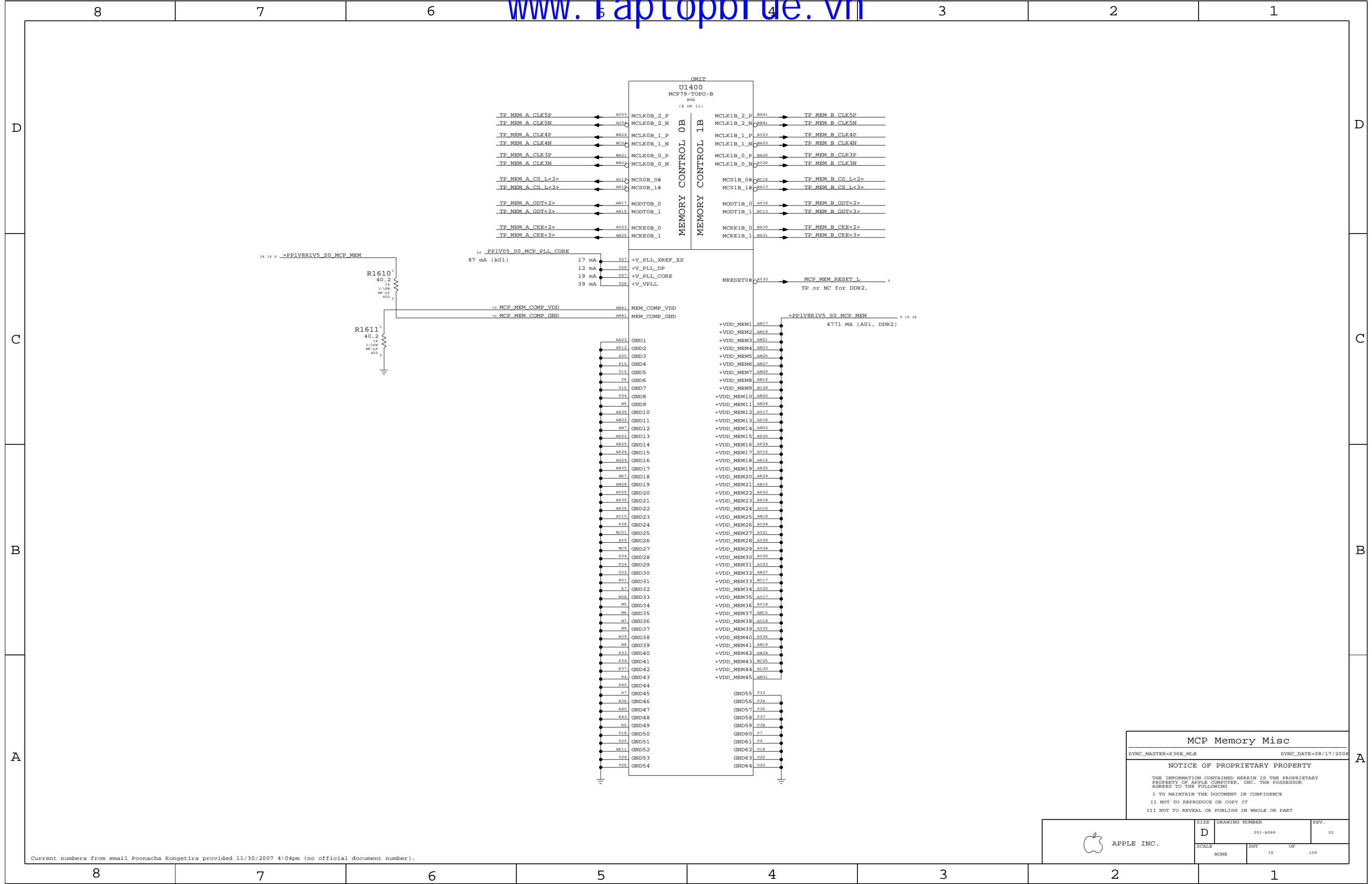
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MCP Memory Misc

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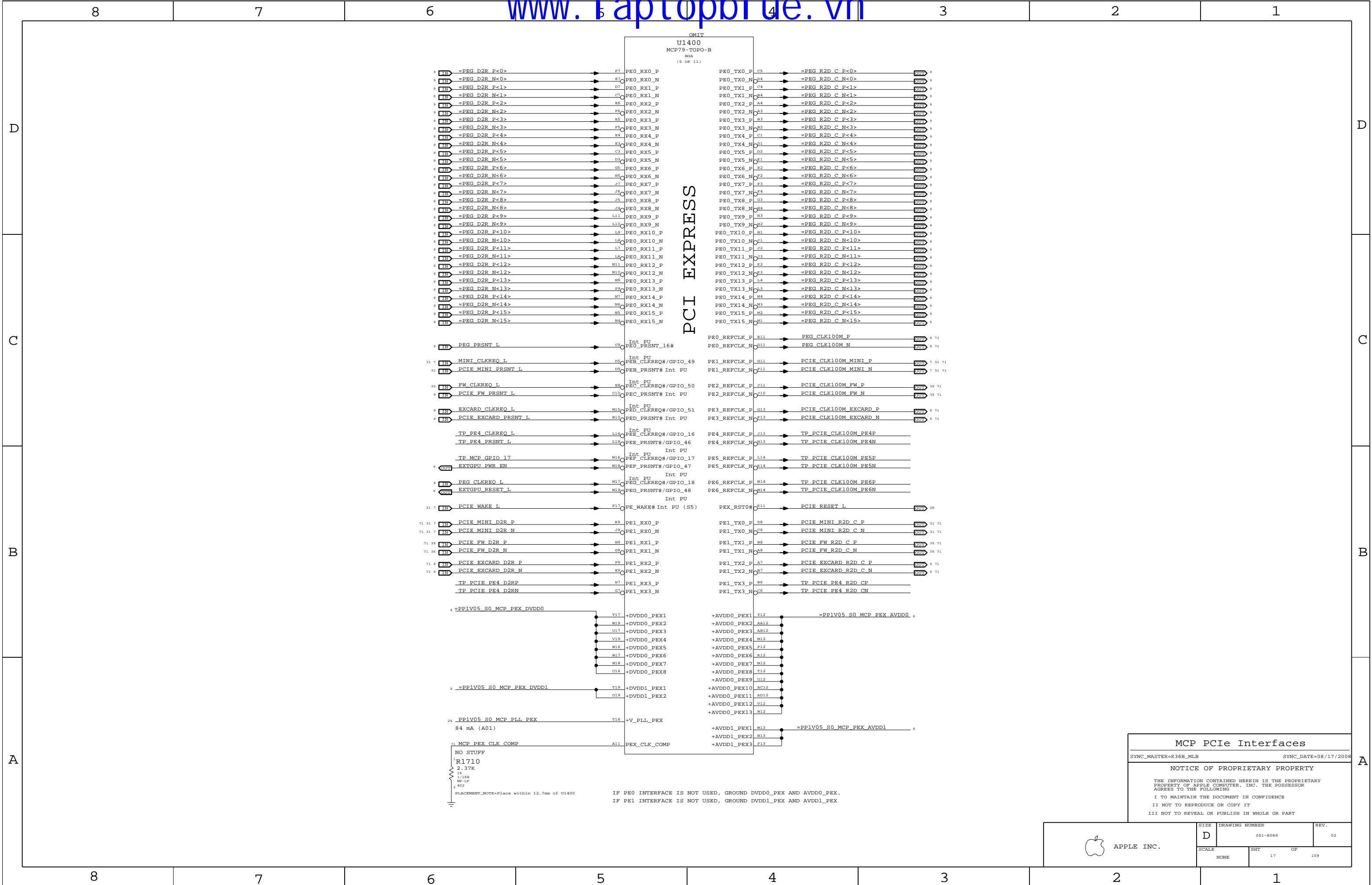
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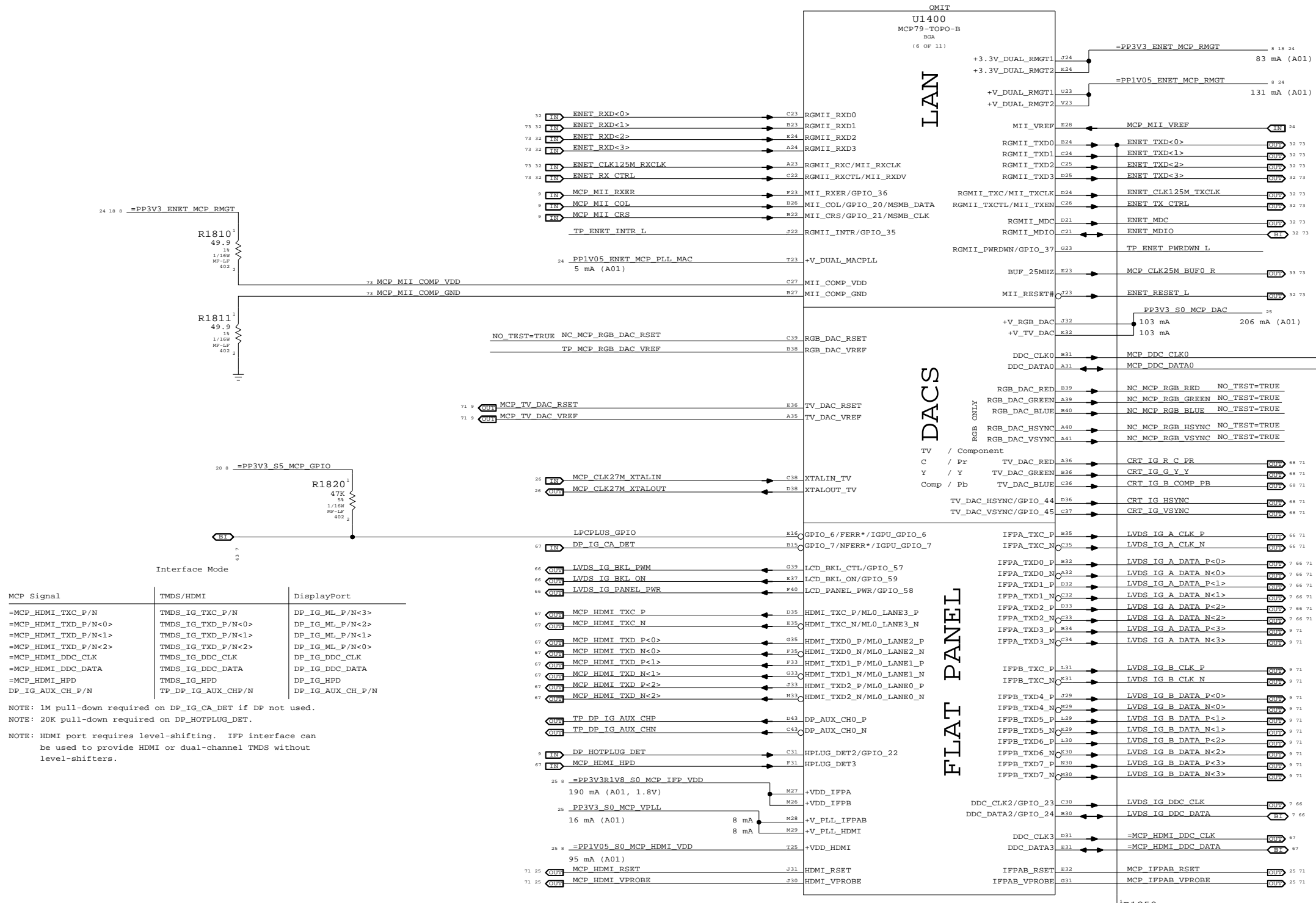
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Network Interface Select

Interface	ENET_TXD<0>
RGMII	1
MII	0

NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

MCP Signal	TMDS/HDMI	DisplayPort
=MCP_HDMI_TXC_P/N	TMDS_IG_TXC_P/N	DP_IG_ML_P/N<3>
=MCP_HDMI_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	DP_IG_ML_P/N<2>
=MCP_HDMI_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	DP_IG_ML_P/N<1>
=MCP_HDMI_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	DP_IG_ML_P/N<0>
=MCP_HDMI_DDC_CLK	TMDS_IG_DDC_CLK	DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA	TMDS_IG_DDC_DATA	DP_IG_DDC_DATA
=MCP_HDMI_HPD	TMDS_IG_HPD	DP_IG_HPD
DP_IG_AUX_CH_P/N	TP_DP_IG_AUX_CH_P/N	DP_IG_AUX_CH_P/N

NOTE: 1M pull-down required on DP\_IG\_CA\_DET if DP not used.  
NOTE: 20K pull-down required on DP\_HOTPLUG\_DET.  
NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.

GPIO 57-59 ( IF LCD PANEL IS USED):  
IN MCP79 THESE PINS HAVE UNDOCUMENTED PULL HIGH (~10K TO 3.3V). TO ENSURE PINS ARE LOW BY DEFAULT, PULL DOWN(1K OR SRONGER) MUST BE USED

MCP Ethernet & Graphics

SYNC\_MASTER=K36B\_MLBSYNC\_DATE=08/17/2008

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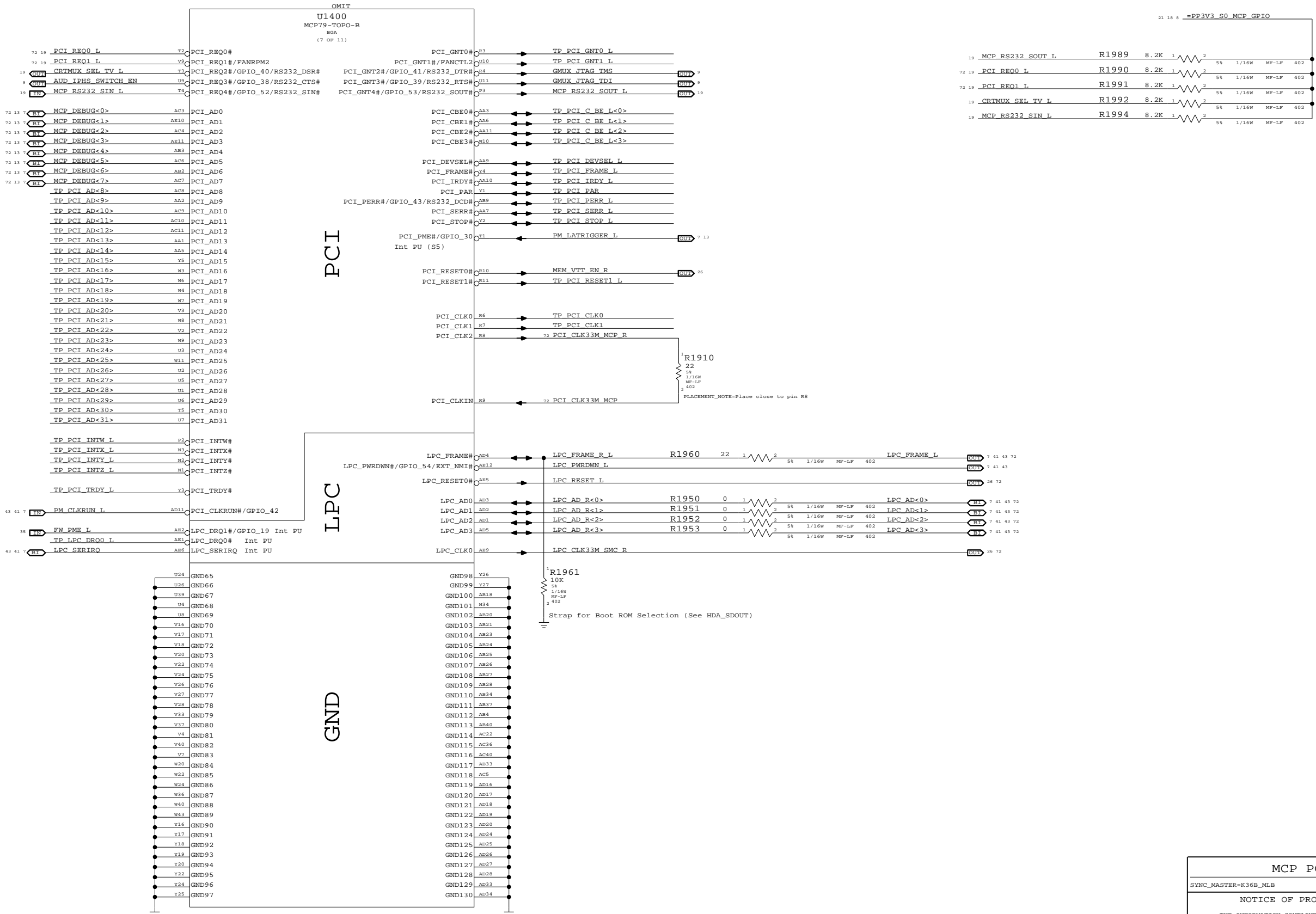
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MCP PCI & LPC

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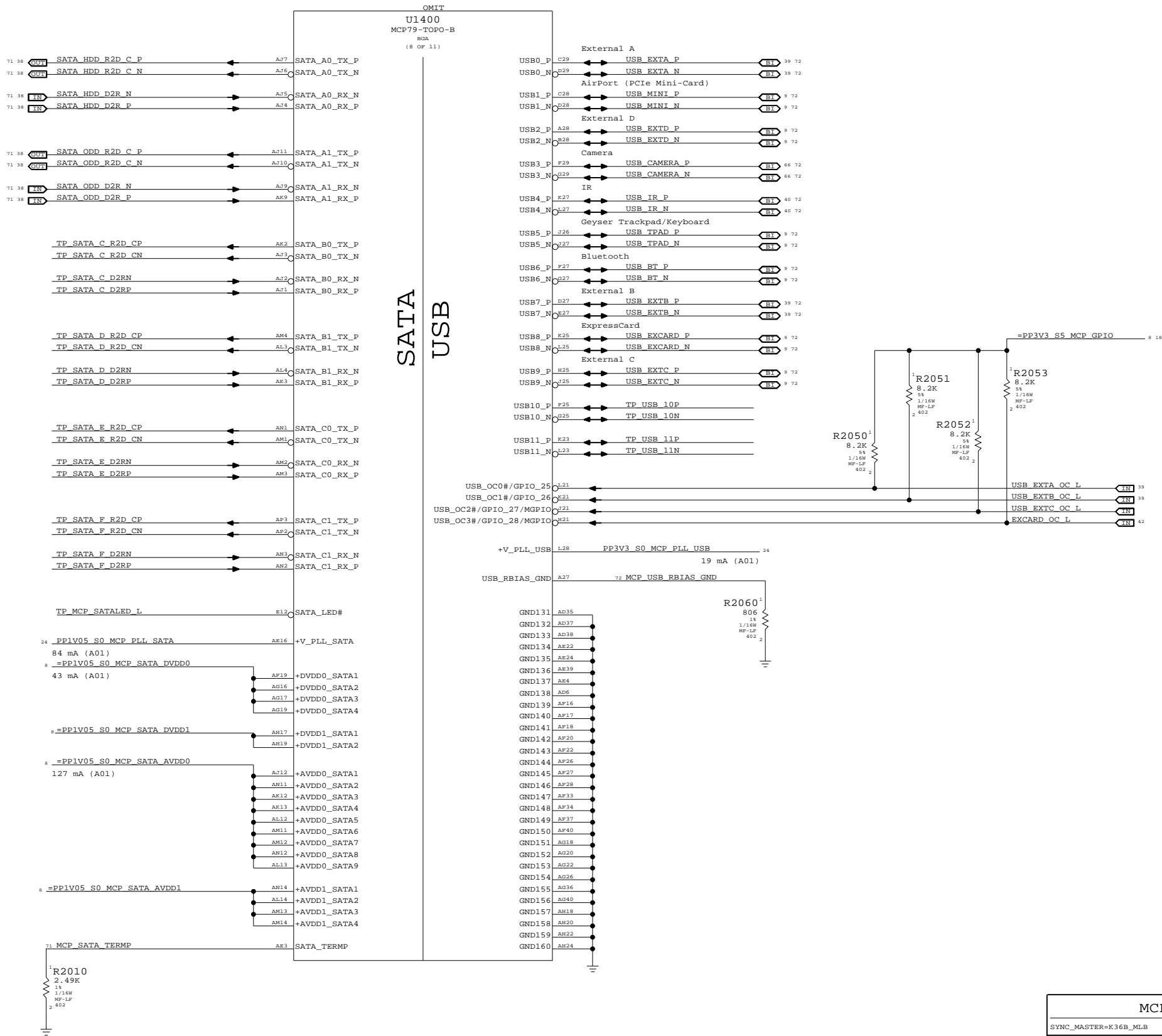
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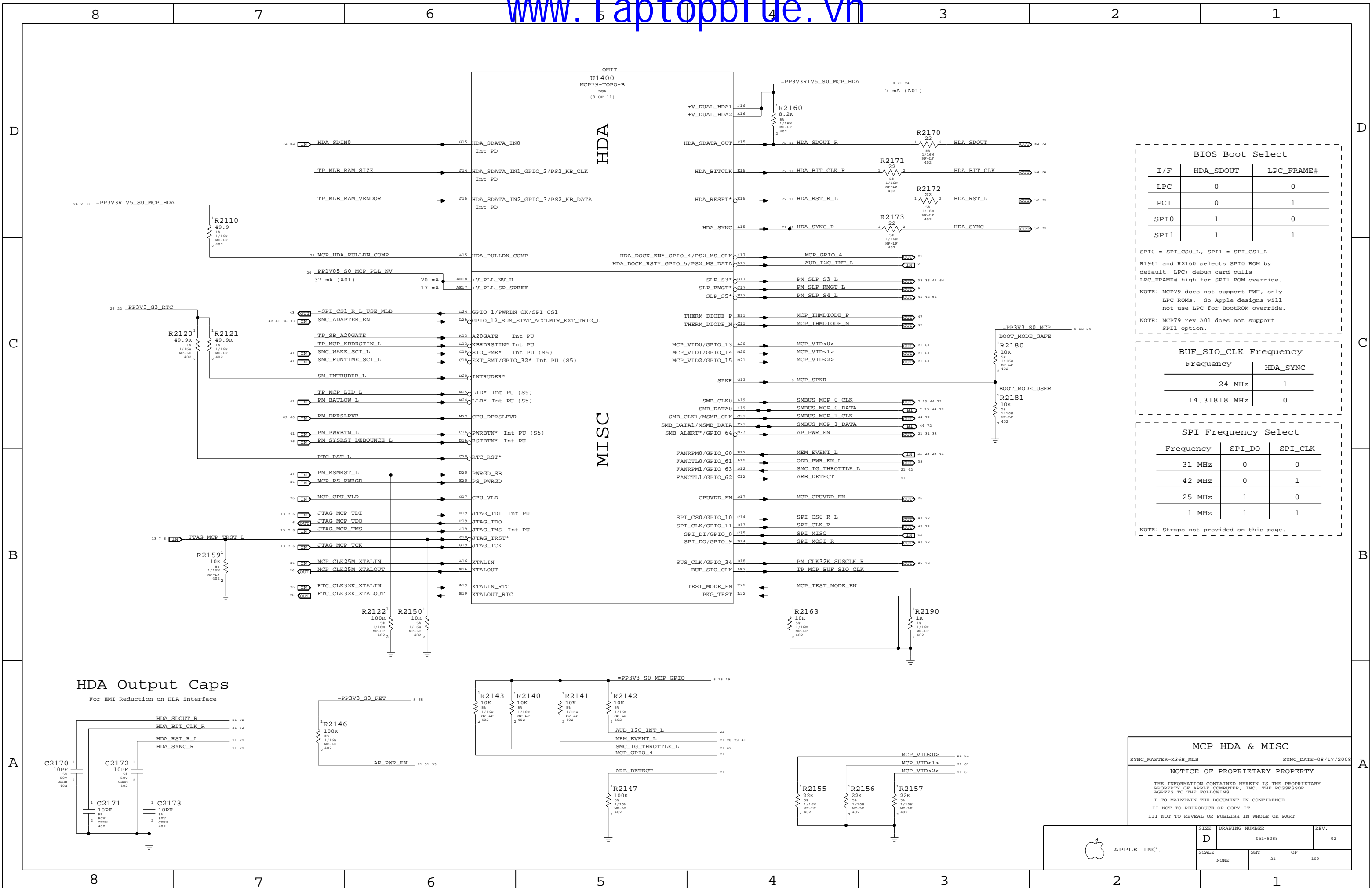
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MCP SATA & USB		
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BIOS Boot Select		
I/F	HDA_SDOUT	LPC_FRAME#
LPC	0	0
PCI	0	1
SPI0	1	0
SPI1	1	1

SPI0 = SPI\_CS0\_L, SPI1 = SPI\_CS1\_L

R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC\_FRAME# high for SPI1 ROM override.

NOTE: MCP79 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.

NOTE: MCP79 rev A01 does not support SPI1 option.

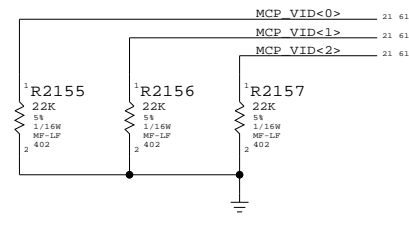
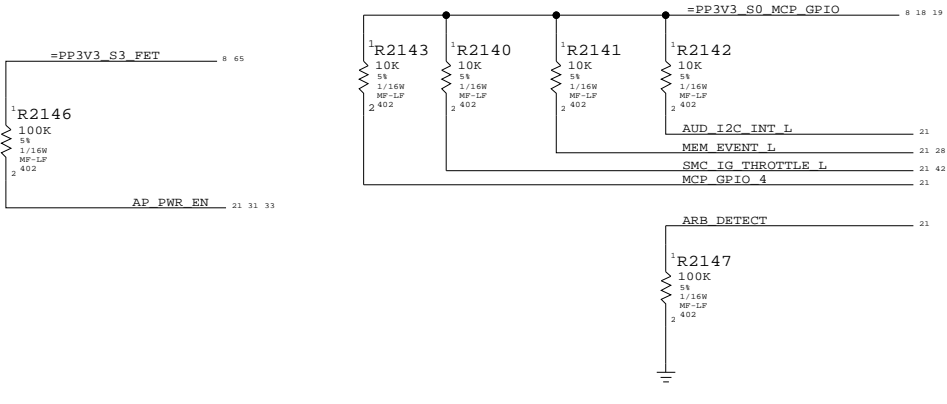
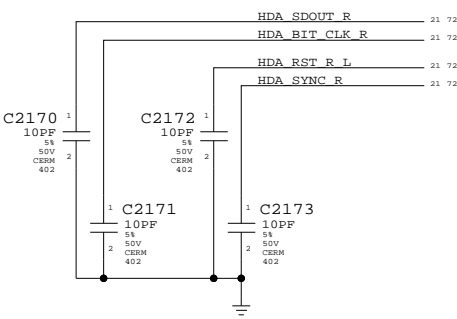
BUF_SIO_CLK Frequency	
Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

SPI Frequency Select		
Frequency	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: Straps not provided on this page.

### HDA Output Caps

For EMI Reduction on HDA interface



MCP HDA & MISC

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SYNC\_DATE=08/17/2008

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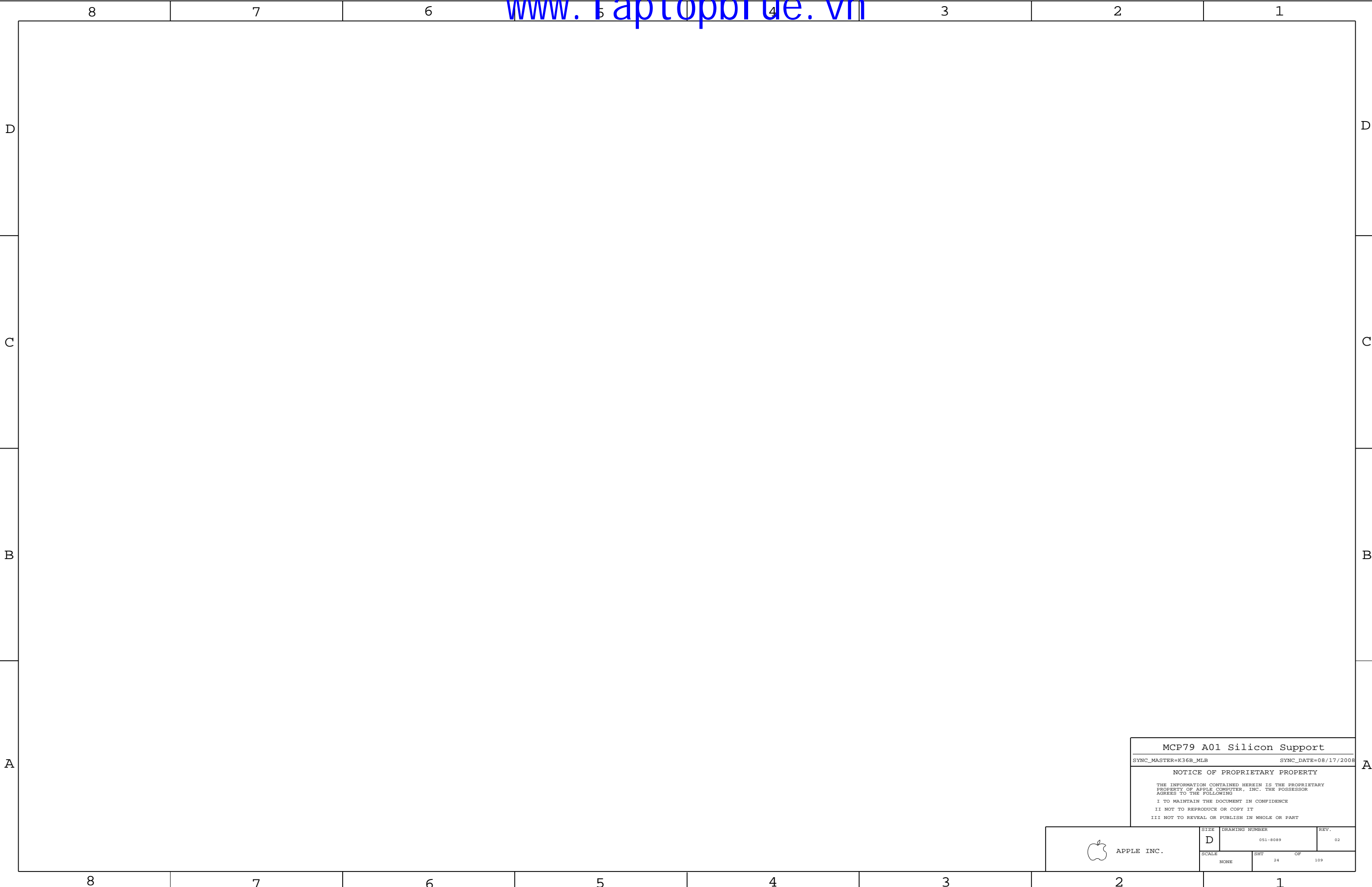
REV.: 02


SCALE: NONE

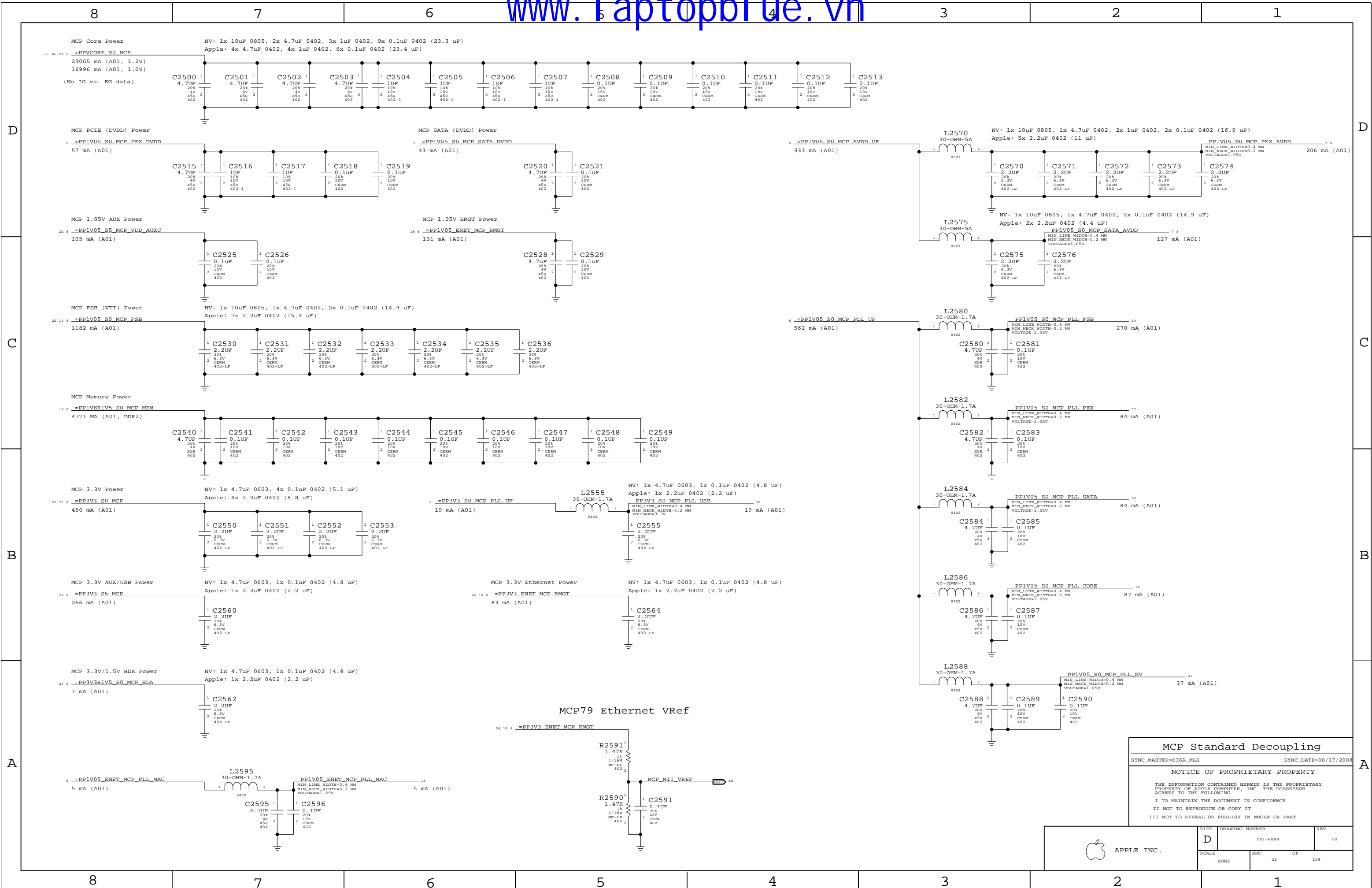
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MCP79 A01 Silicon Support			
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MCP Standard Decoupling

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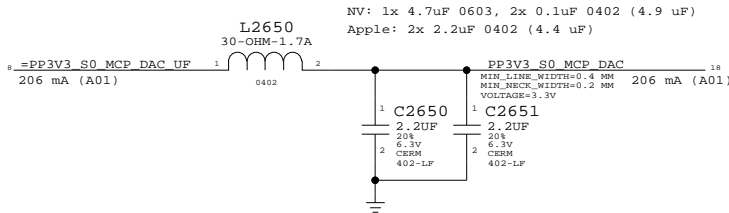
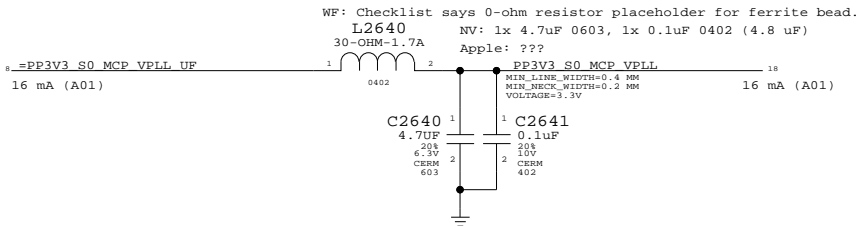
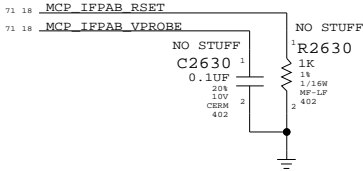
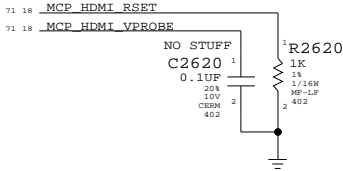
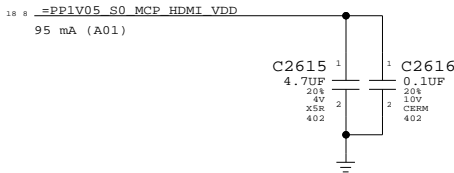
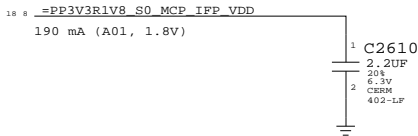
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE INC.

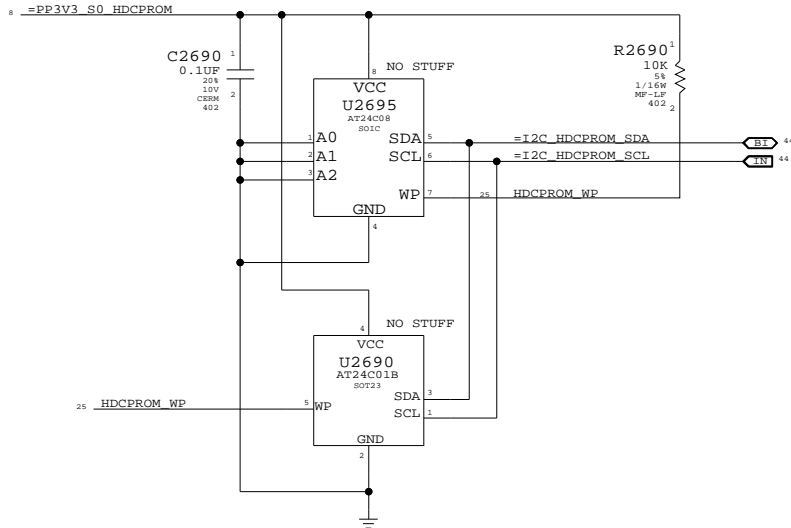
SIZE	DRAWING NUMBER	REV.
D	051-8089	02
SCALE	SHT	OF
NONE	25	109

WF: Checklist says 0-ohm resistor placeholder for ferrite bead.  
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)  
Apple: 1x 2.2uF 0402 (2.2 uF)



### HDCP ROM

WF: Open question on which package option(s) nVidia can support.

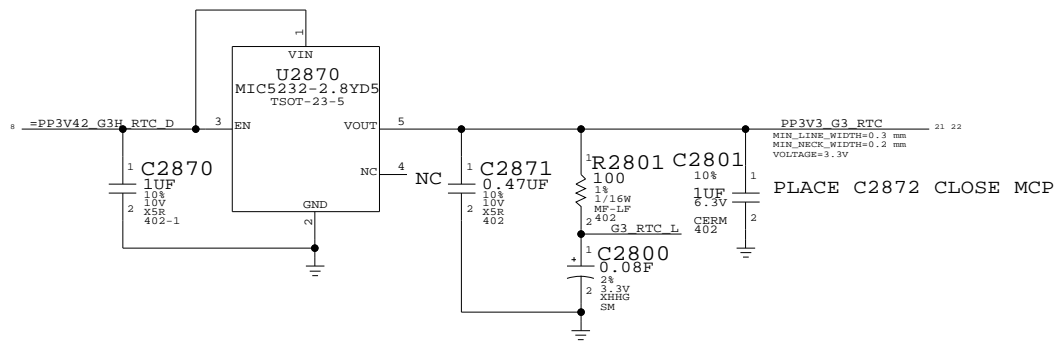


SYNC FROM T18  
REMOVE MCP 27MHZ CRYSTAL CRICUIT SINCE NOT SUPPORTING TV-OUT  
REMOVE DAC TERMINATIONS R2665,C2665 AND R2670 TO R2672

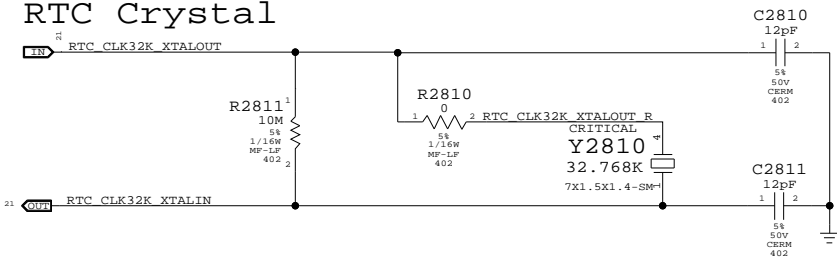
MCP Graphics Support		
SYNC_MASTER=K36B_MLB		SYNC_DATE=08/17/2008
NOTICE OF PROPRIETARY PROPERTY		
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	D	051-8089	02
SCALE		SHT	OF
NONE		26	109

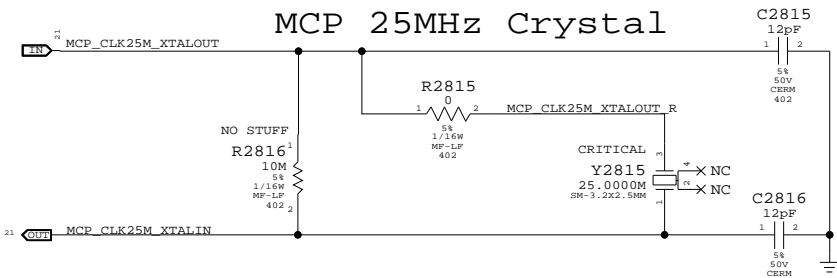
RTC Power Sources



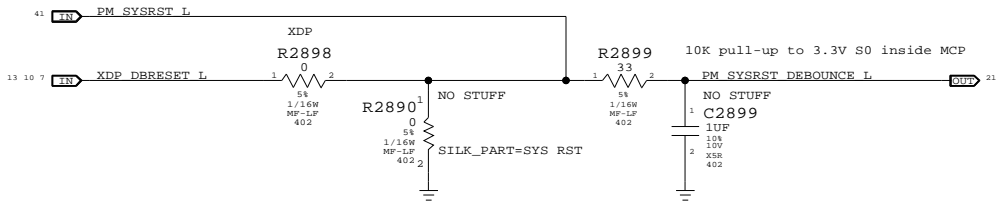
RTC Crystal



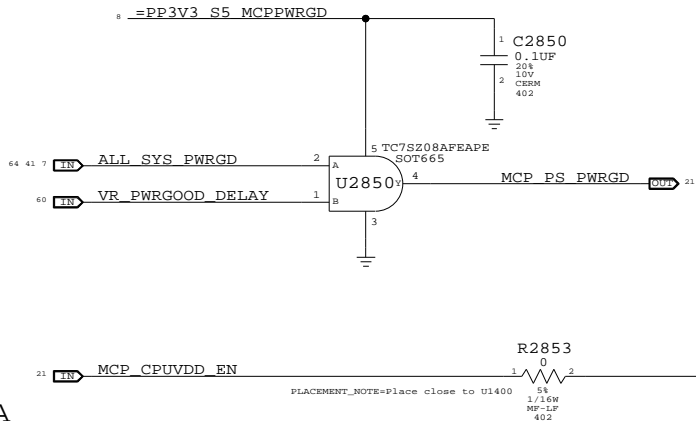
MCP 25MHz Crystal



Reset Button

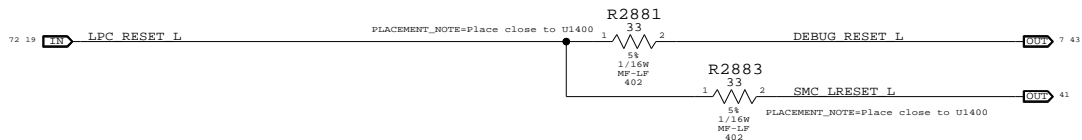


MCP S0 PWRGD

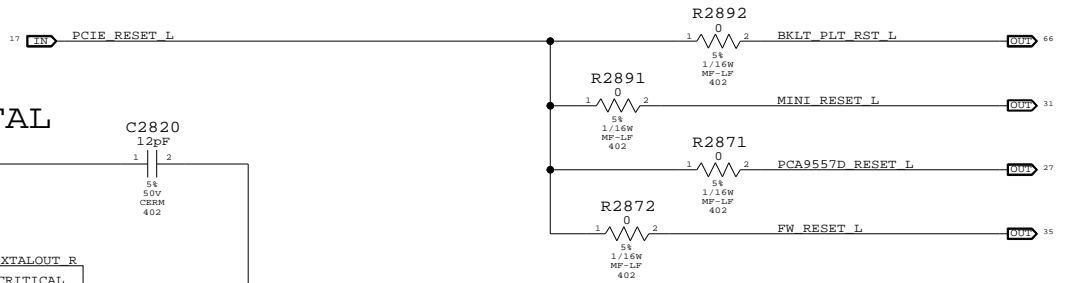


Platform Reset Connections

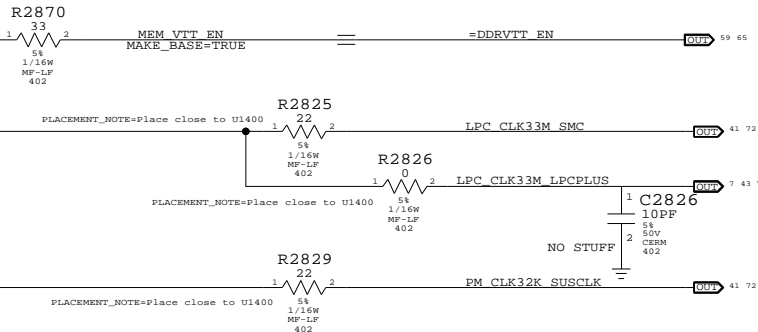
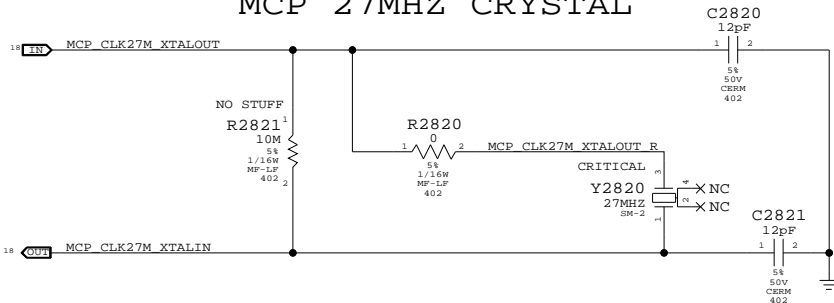
LPC Reset (Unbuffered)



PCIE Reset (Unbuffered)



MCP 27MHZ CRYSTAL



SYNC FROM T18  
CHANGE RESET BUTTON TO RESET PADS  
REMOVE UNUSED PCIE RESET SIGNALS  
REMOVE R2824 AND NET PCI\_CLK33M\_SLOT\_A  
CHANGE RTC POWER SOURCE FROM COIN CELL TO SUPER CAPS  
ALIAS MEM\_VTT\_EN TO =DDRVTT\_EN  
CHANGE Y2810 AND U2850 TO SMALLER PARTS

SB Misc	
SYNC_MASTER=K36B_MLB	SYNC_DATE=08/17/2008
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	D	051-8089	02
SCALE		SHT	OF
NONE		28	109

Power aliases required by this page:

- =PP3V13\_S3\_VREFMRGN
- =PP3V13\_S5\_VREFMRGN
- =PPVTT\_S3\_DDR\_BUF

---

Signal aliases required by this page:

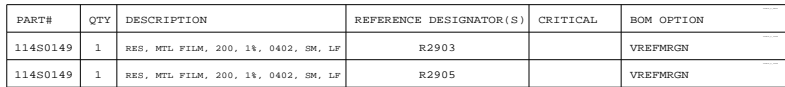
- =I2C\_VREFDACS\_SCL
- =I2C\_VREFDACS\_SDA
- =I2C\_PCA9557D\_SCL
- =I2C\_PCA9557D\_SDA

---

BOM options provided by this page:

VREFMRGN AND NO VREFMRGN

### BOM OPTION TO SELECT VREF SOURCE



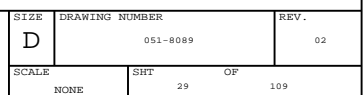
SYNC_MASTER=K36B_MLB	SYNC_DATE=08/17/2008
----------------------	----------------------

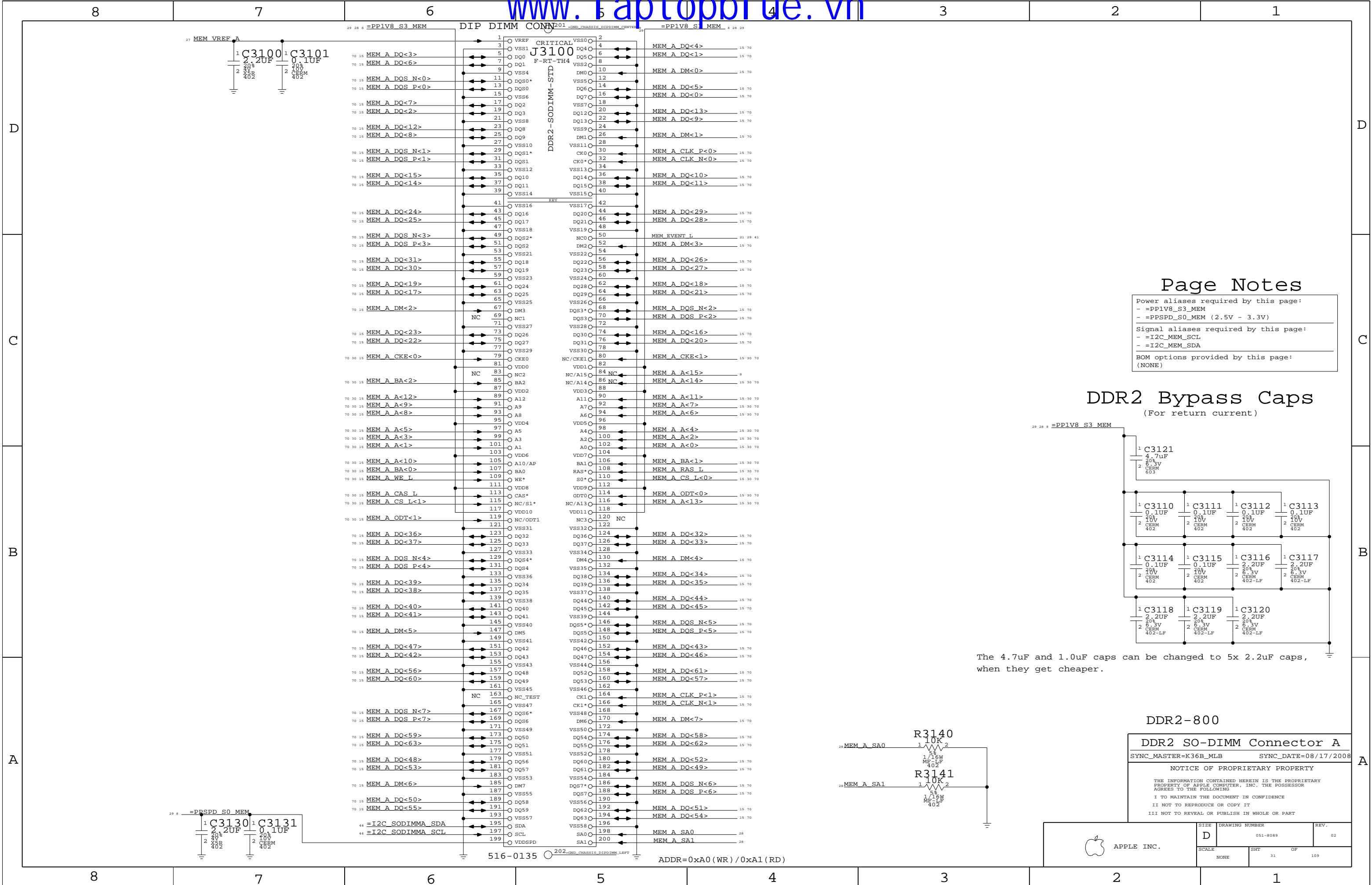
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Page Notes

Power aliases required by this page:

- =PP1V8\_S3\_MEM
- =PPSPD\_S0\_MEM (2.5V - 3.3V)

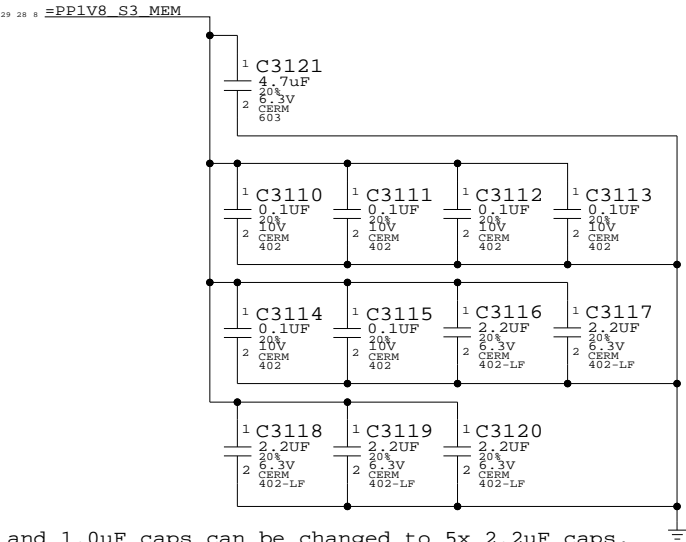
Signal aliases required by this page:

- =I2C\_MEM\_SCL
- =I2C\_MEM\_SDA

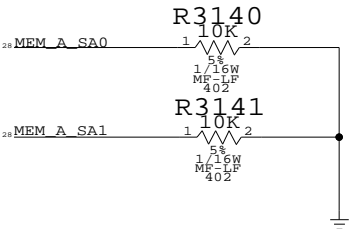
BOM options provided by this page:

(NONE)

DDR2 Bypass Caps  
(For return current)



The 4.7uF and 1.0uF caps can be changed to 5x 2.2uF caps, when they get cheaper.



DDR2-800

DDR2 SO-DIMM Connector A

SYNC\_MASTER=K36B\_MLB SYNC\_DATE=08/17/2008

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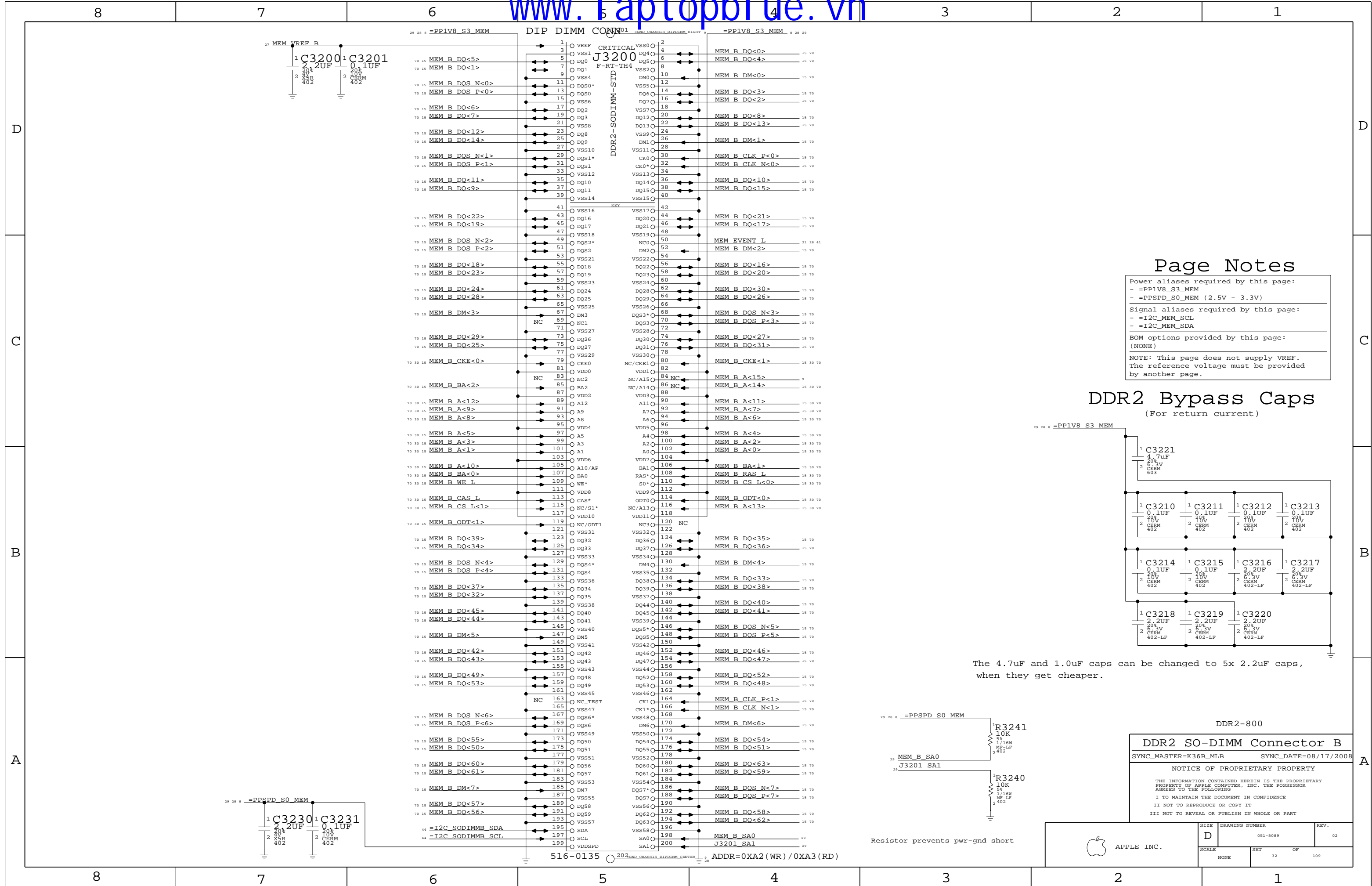
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8089	02
SCALE	SHT	OF
NONE	31	109



## Page Notes

Power aliases required by this page:

- =PP1V8\_S3\_MEM
- =PPSPD\_S0\_MEM (2.5V - 3.3V)

Signal aliases required by this page:

- =I2C\_MEM\_SCL
- =I2C\_MEM\_SDA

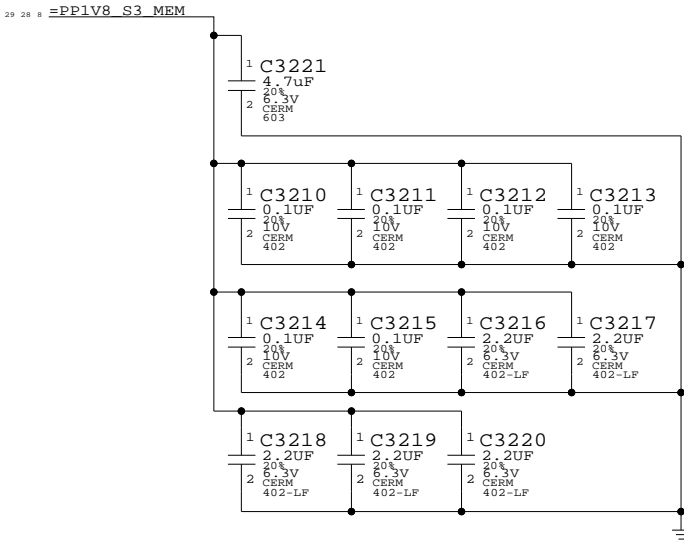
BOM options provided by this page:

(NONE)

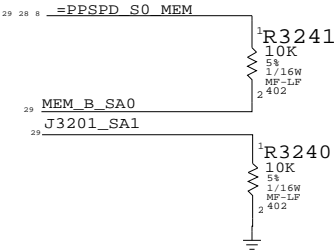
NOTE: This page does not supply VREF.  
The reference voltage must be provided  
by another page.

## DDR2 Bypass Caps

(For return current)



The 4.7uF and 1.0uF caps can be changed to 5x 2.2uF caps,  
when they get cheaper.



Resistor prevents pwr-gnd short

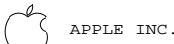
DDR2-800

### DDR2 SO-DIMM Connector B

SYNC\_MASTER=K36B\_MLB SYNC\_DATE=08/17/2008

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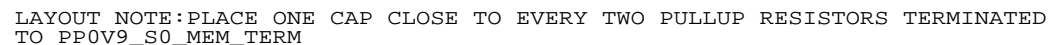
SIZE DRAWING NUMBER REV.

D 051-8089 02

SCALE SHT OF

NONE 32 109

A



III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
------	----------------	------

1

051-8089

REV.

SCALE	

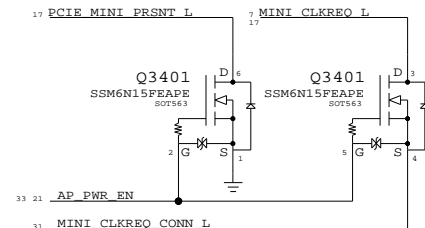
SHT

---

NON

33

## A



Right Clutch Connector

SYNCH\_MASTER=K36B\_MLB

SYNCH\_DATE=08/17/2008

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D

C

B

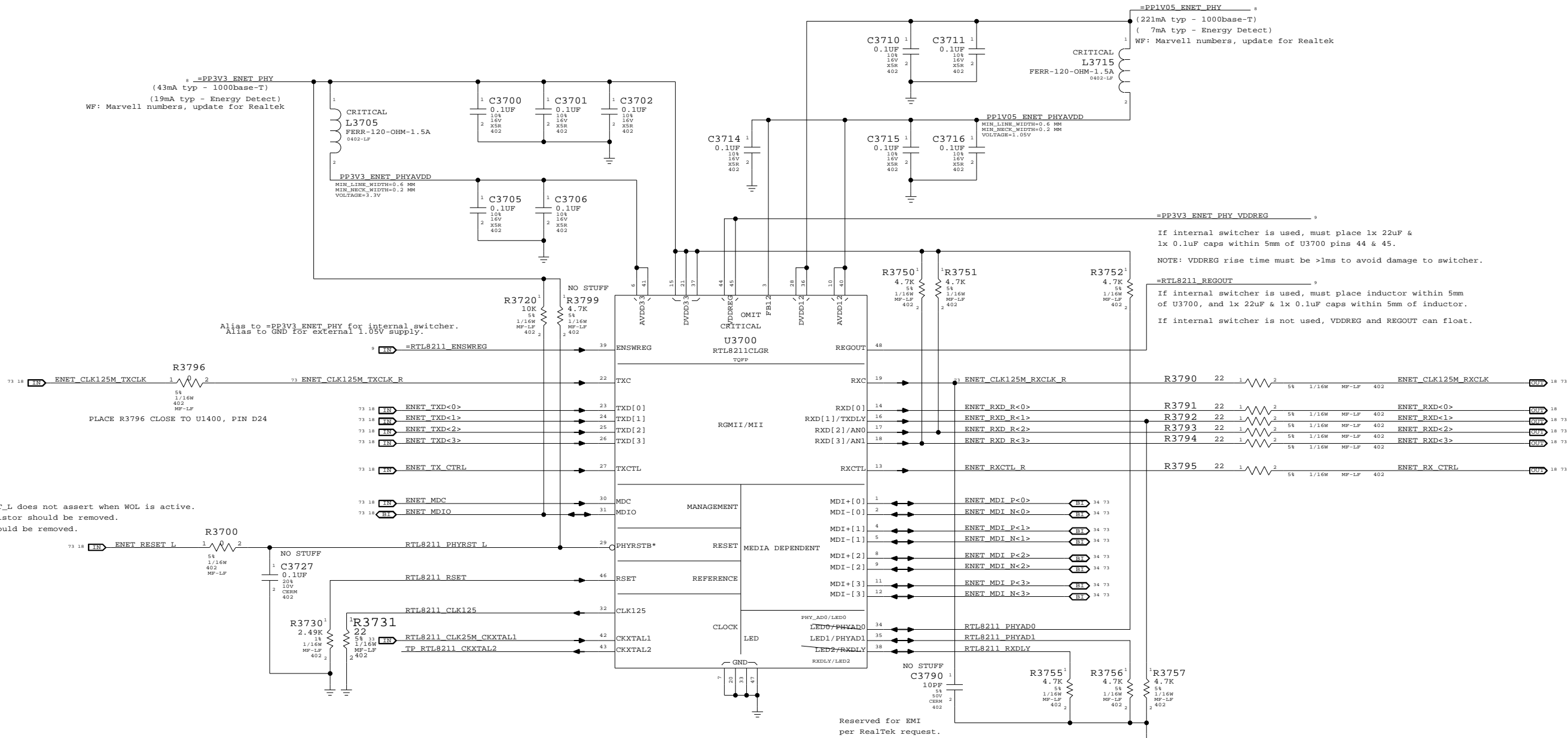
A

D

C

B


A



Configuration Settings:

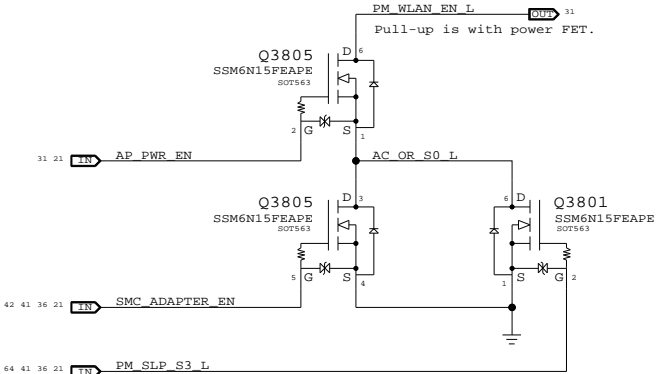
PHYAD = 01 (PHY Address 00001)  
AN[1:0] = 11 (Full auto-negotiation)  
RXDLY = 0 (RXCLK transitions with data)  
TXDLY = 0 (No TXCLK Delay)

Ethernet PHY (RTL8211CL)		
SYNC_MASTER=SUMA		SYNC_DATE=03/20/2008
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 APPLE INC.	SIZE D	DRAWING NUMBER 051-8089	REV. 02
	SCALE NONE	SHT 37	OF 109

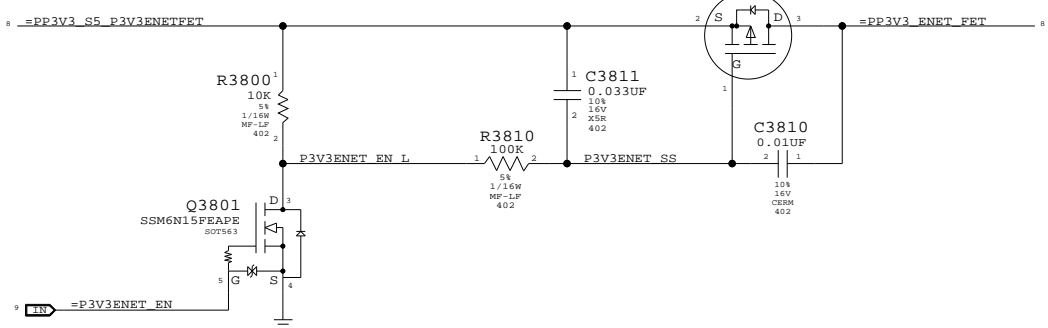
WLAN Enable Generation

"WLAN" = ("S3" && "AP\_PWR\_EN" && ("AC" || "S0"))  
NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP\_PWR\_EN signal.



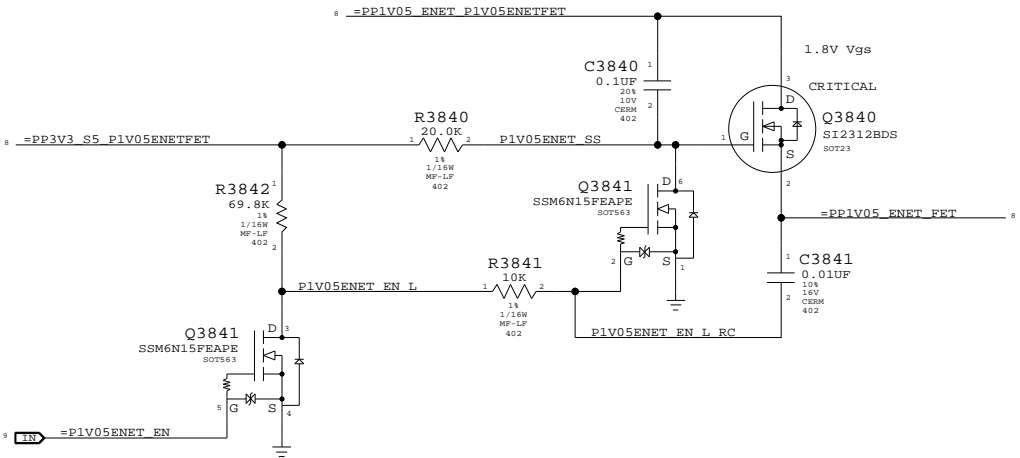
3.3V ENET FET

@ 2.5V Vgs:  
Rds(on) = 90mOhm max  
I(max) = 1.7A (85C)



MOBILE:  
Recommend aliasing PM\_SLP\_RMGT\_L and  
=P3V3ENET\_EN. Nets separated on  
ARB for alternate power options.

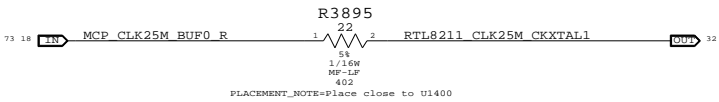
1.05V ENET FET



Non-ARB:  
Recommend aliasing PM\_SLP\_RMGT\_L and  
=P1V05ENET\_EN. Nets separated on  
ARB for alternate power options.

RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.  
Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.

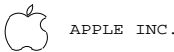


Ethernet & AirPort Support

SYNC\_MASTER=SUMA SYNC\_DATE=04/04/2008

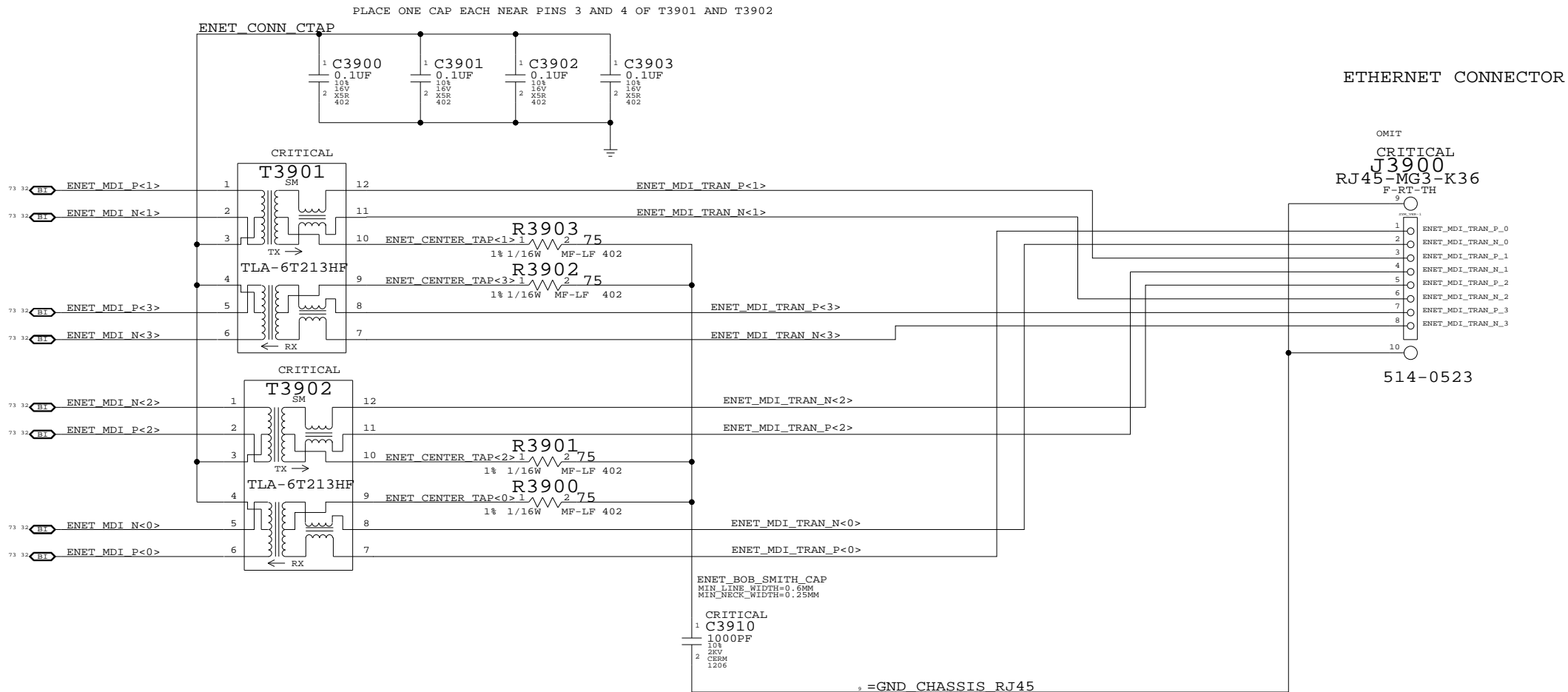
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SIZE	DRAWING NUMBER	REV.
D	051-8089	02
SCALE	SHT	OF
NONE	38	109

- COPY THIS PAGE FROM K36 CSA.39



ETHERNET CONNECTOR

SYNC\_MASTER=SUMA SYNC\_DATE=04/04/2008

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SIZE

D

DRAWING NUMBER

051-8089

REV.

02

SCALE

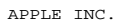
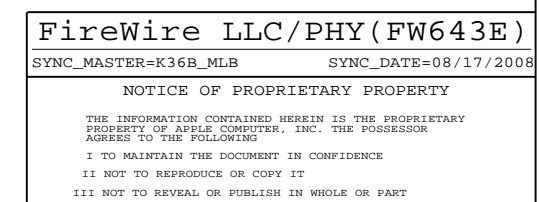
NONE

SHT

39

OF

109

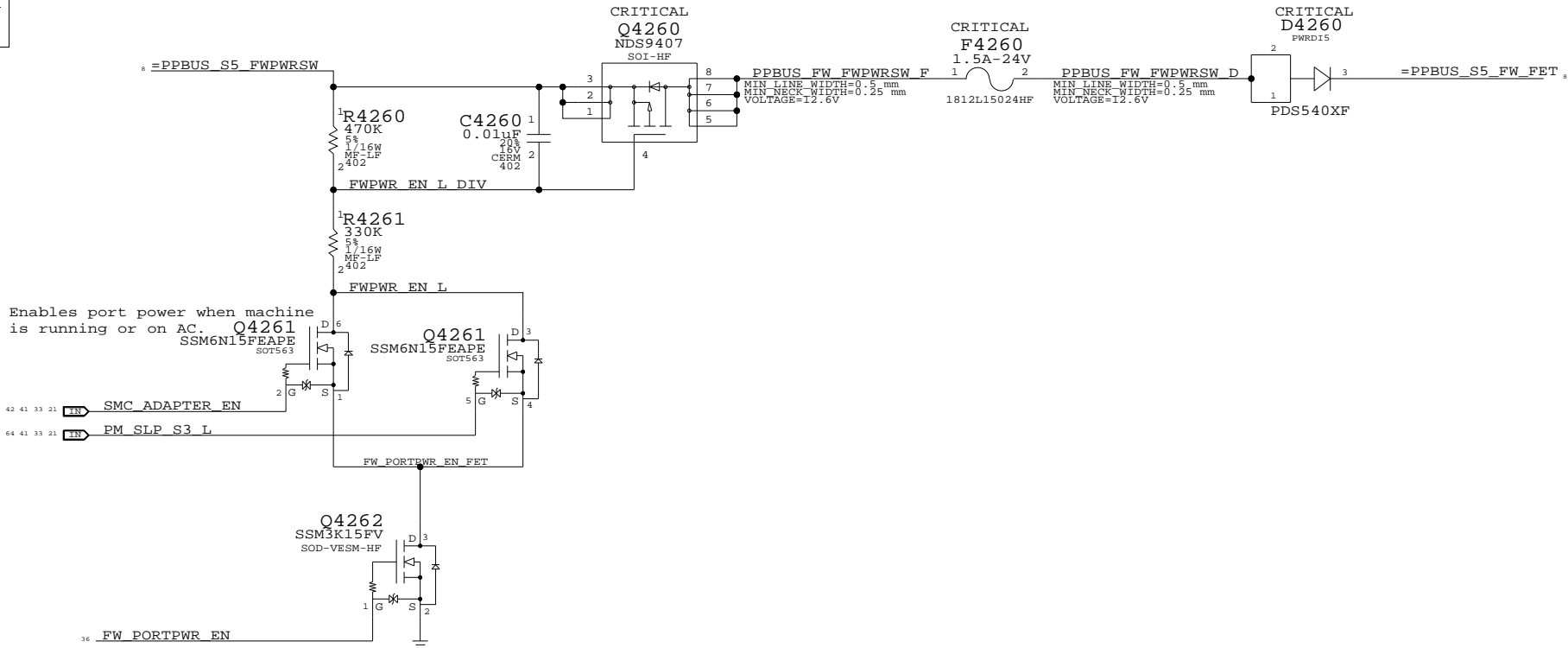


SIZE D	DRAWING NUMBER 051-8089	REV.
SCALE NONE	SHT 41	OF 109

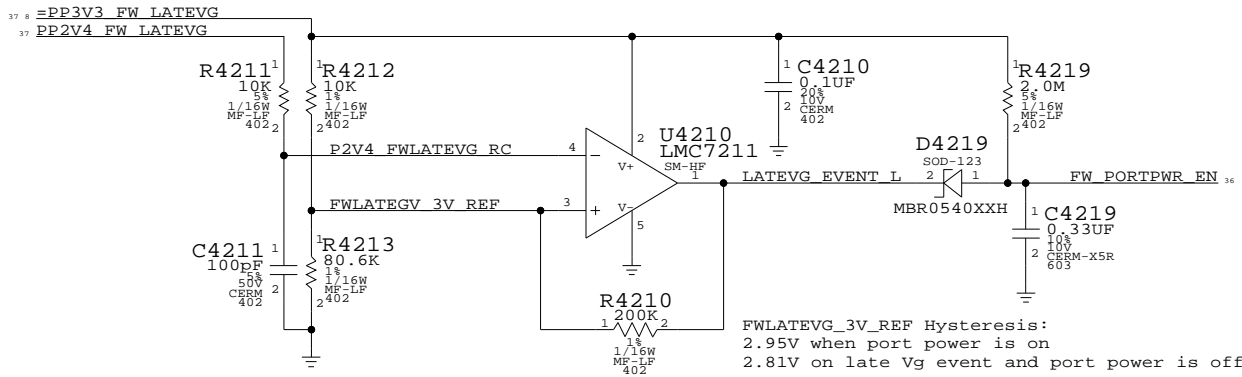
Page Notes

Power aliases required by this page:  
- =PPBUS\_S5\_FWPWSW (system supply for bus power)  
- =PP3V3\_FW\_LATEVG\_ACTIVE  
- =PPVP\_FW\_SUMNODE (power passthru summation node)  
Signal aliases required by this page:  
(NONE)  
BOM options provided by this page:  
- FW\_PORT\_FAULT\_PU

FireWire Port Power Switch



Late-VG Event Detection



FireWire Port Power

SYNC\_MASTER=K36B\_MLB SYNC\_DATE=08/17/2008

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SIZE	DRAWING NUMBER	REV.
D	051-8089	02
SCALE	SHT	OF
NONE	42	109

Page Notes

Power aliases required by this page:

- =PPVP\_FW\_PORT1  
- =PP3V3\_FW\_LATEVG

Signal aliases required by this page:  
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:  
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

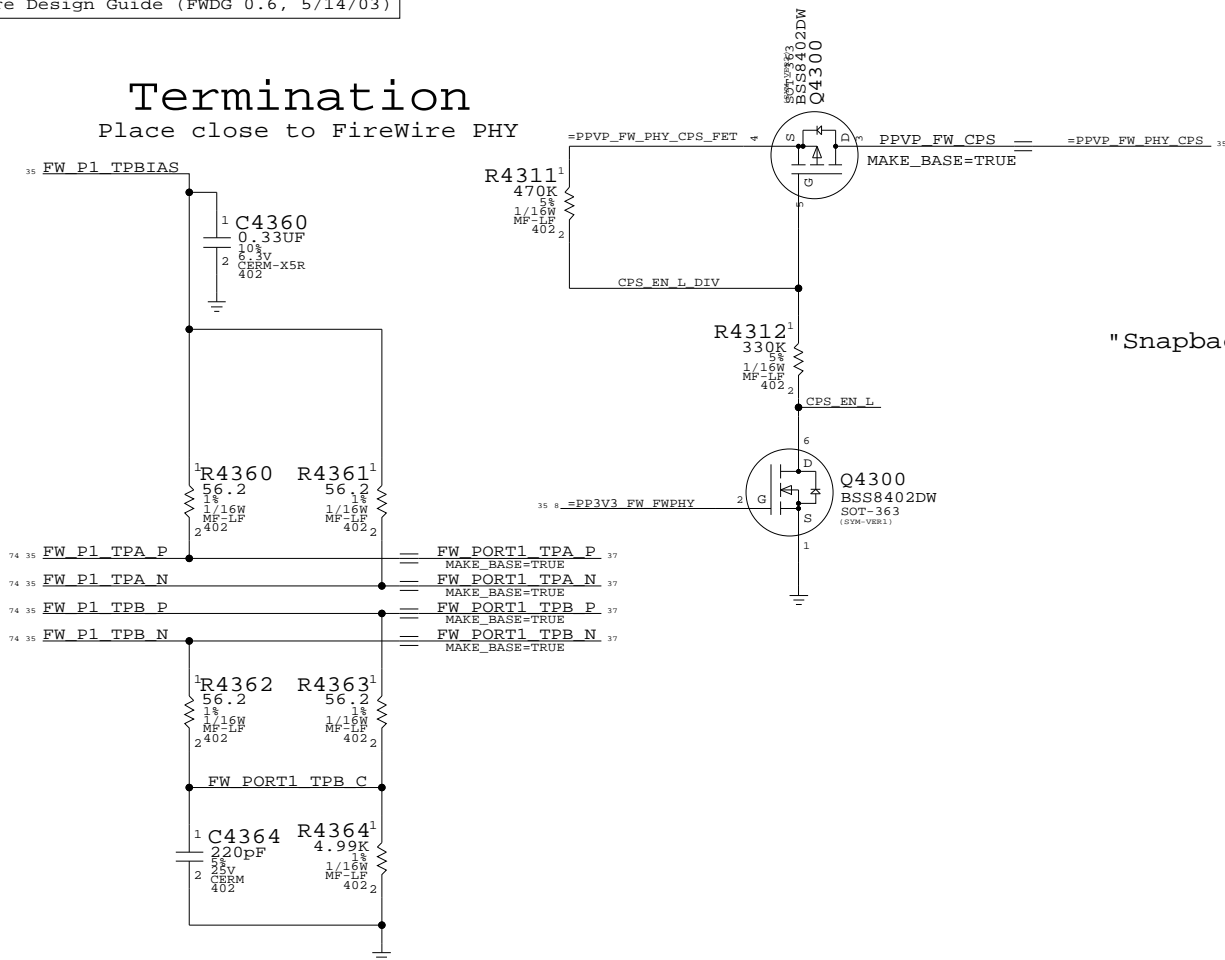
FireWire PHY Config Straps

Configures PHY for:

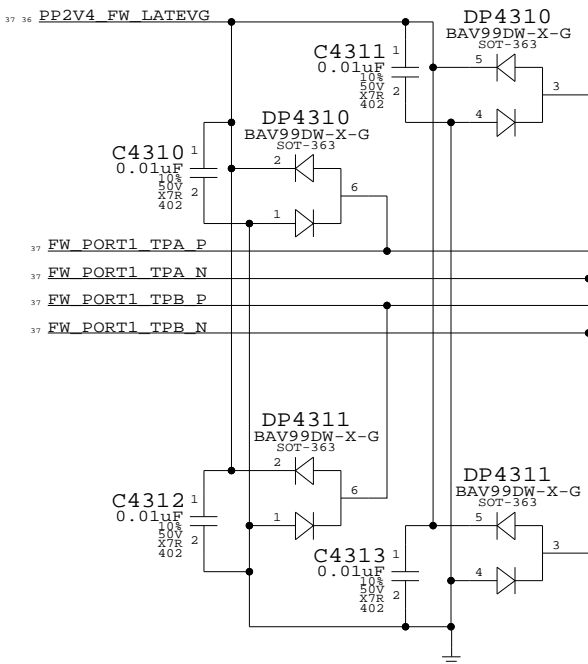
- 1-port Portable Power Class (0)

Termination

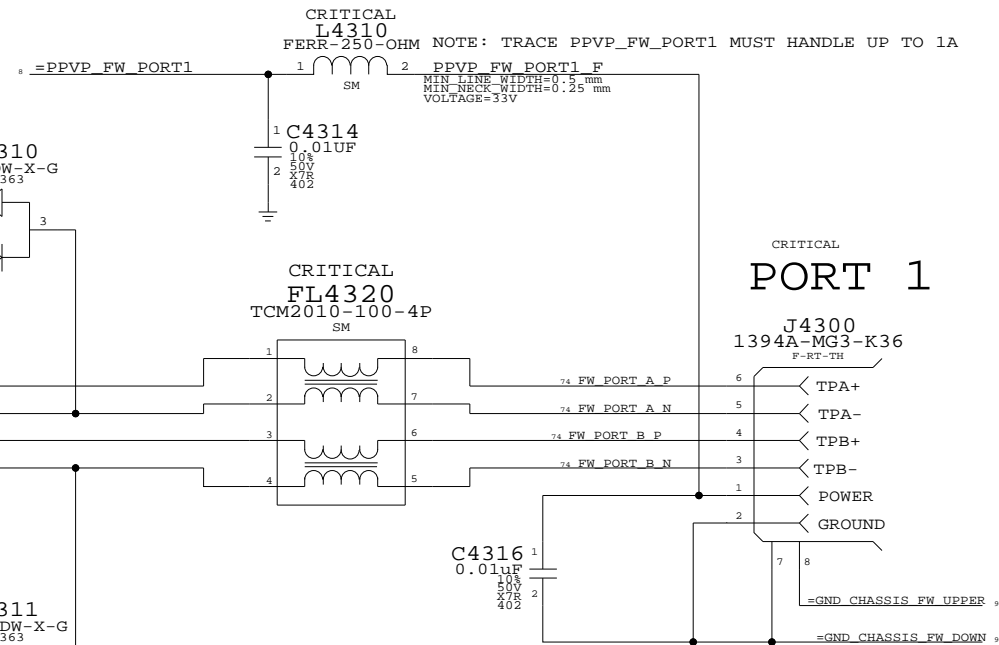
Place close to FireWire PHY



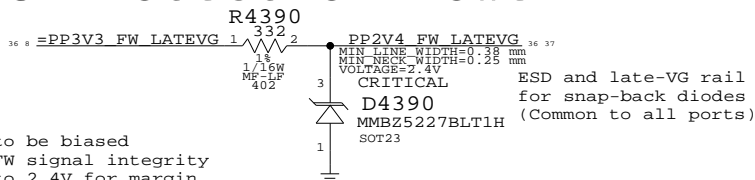
"Snapback" & "Late VG" Protection



Cable Power



Late-VG Protection Power



FireWire Ports

SYNC\_MASTER=K36B\_MLB SYNC\_DATE=(MASTER)

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SIZE D DRAWING NUMBER 051-8089 REV. 02

SCALE NONE SHT 43 OF 109

ODD Power Control

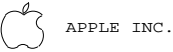
NOTE: 3.3V must be S0 if 5V is S3 or S5 to ensure the drive is unpowered in S3/S5.

SATA ODD Port

SATA CONNECTOR

SYSTEM (SLEEP) LED FILTER

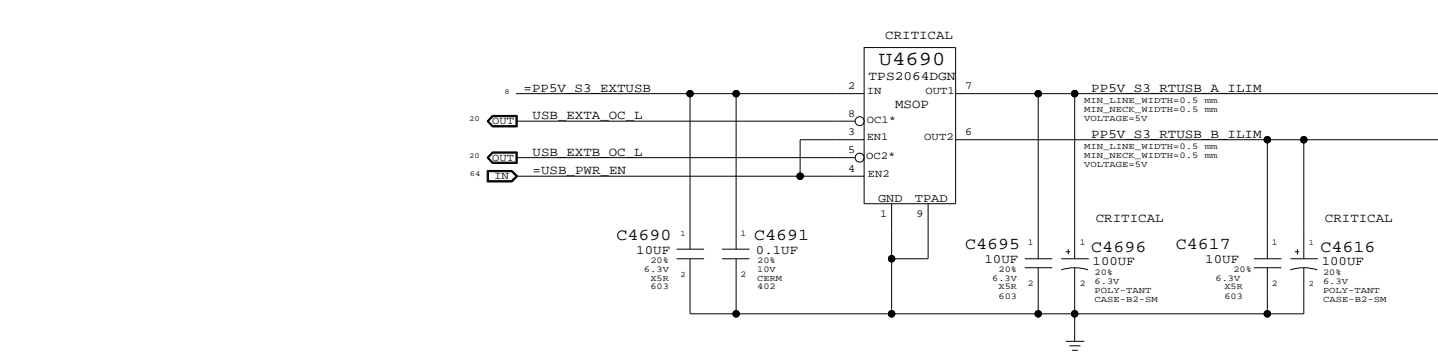
SATA Connectors		
SYNC_MASTER=K36B_MLB		SYNC_DATE=08/17/2008
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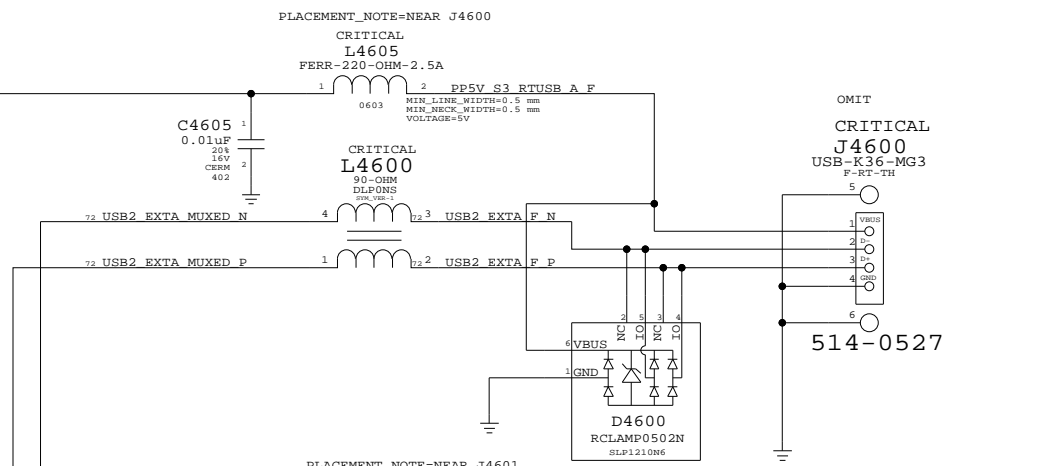
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8089	02
SCALE	SHT	OF
NONE	45	109

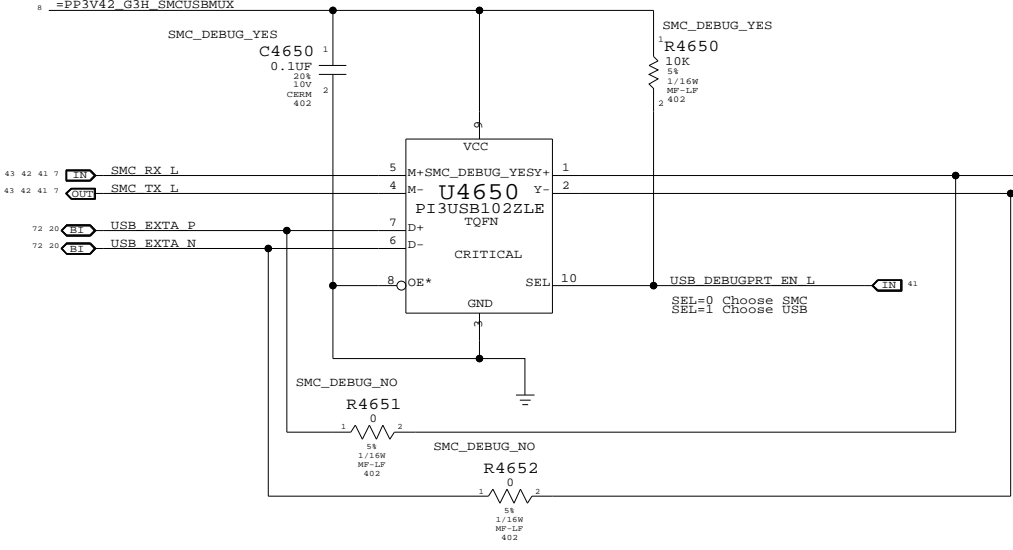
Port Power Switch



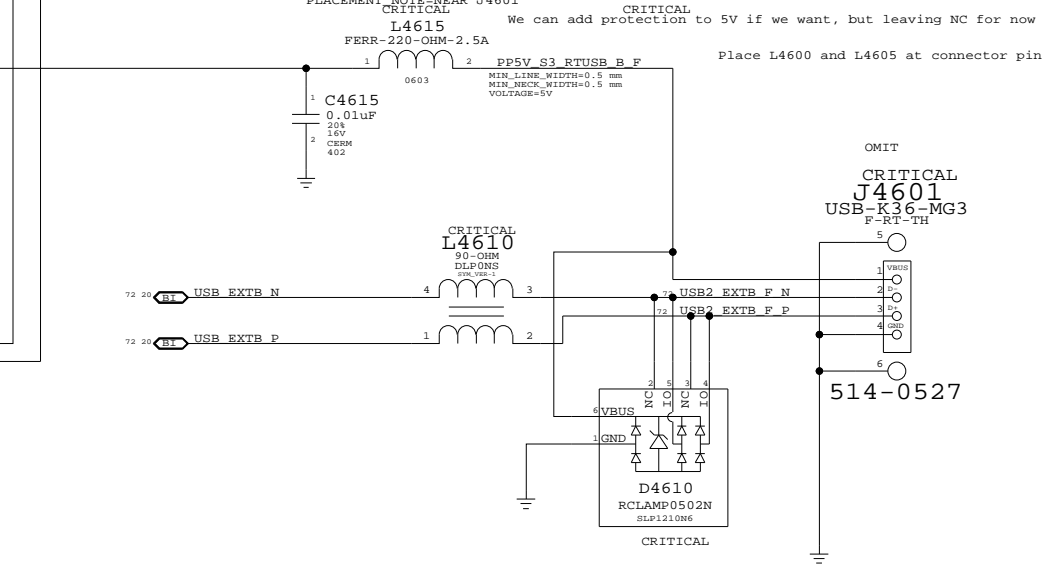
Left USB Port A



USB/SMC Debug Mux

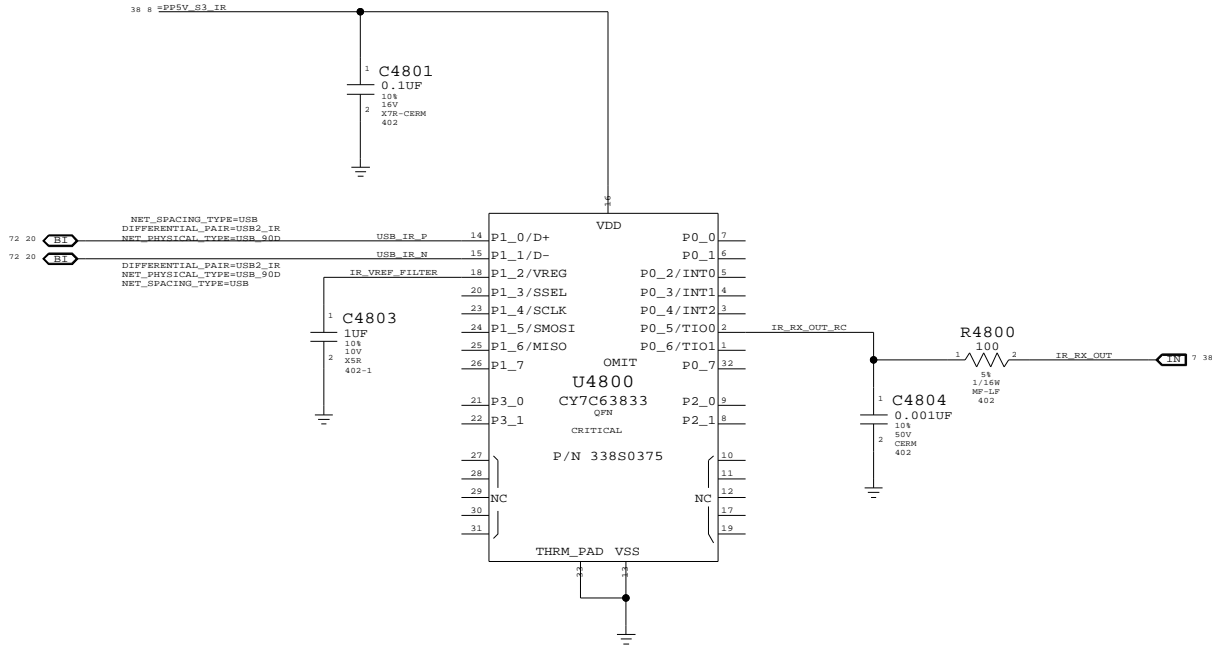


Left USB Port B



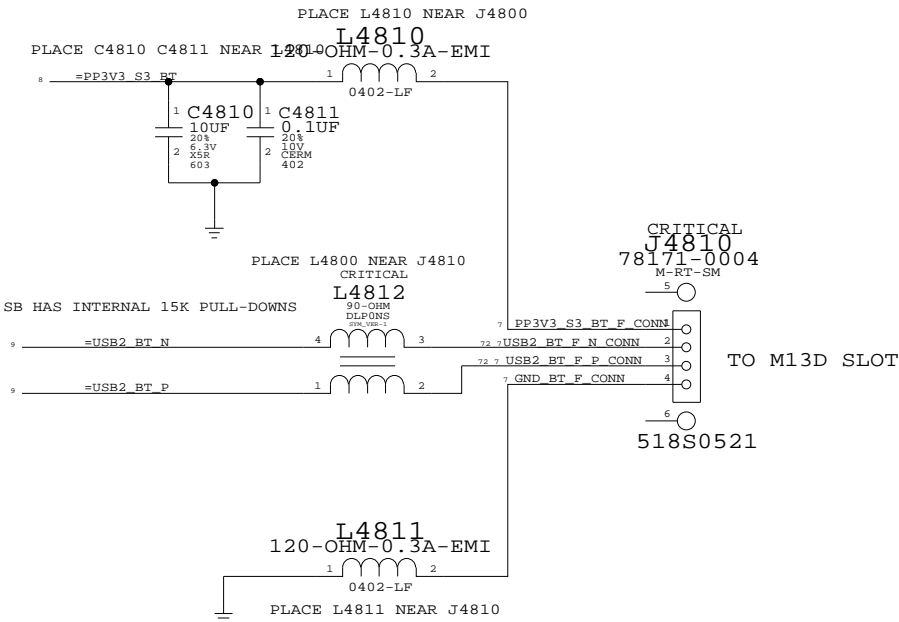
External USB Connectors		
SYNC_MASTER=K36B_MLB		SYNC_DATE=08/17/2008
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	SCALE NONE	SHT 46
	OF 109	REV. 02

IR CTRL



CYPRESS 'ENCORE II' USB CONTROLLER

BLUETOOTH



Front Flex Support

SYNC\_MASTER=K36B\_MLB SYNC\_DATE=07/17/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8089	02
SCALE	SHT	OF
NONE	48	109

NOTE: Unused pins have "SMC\_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

D

C

B

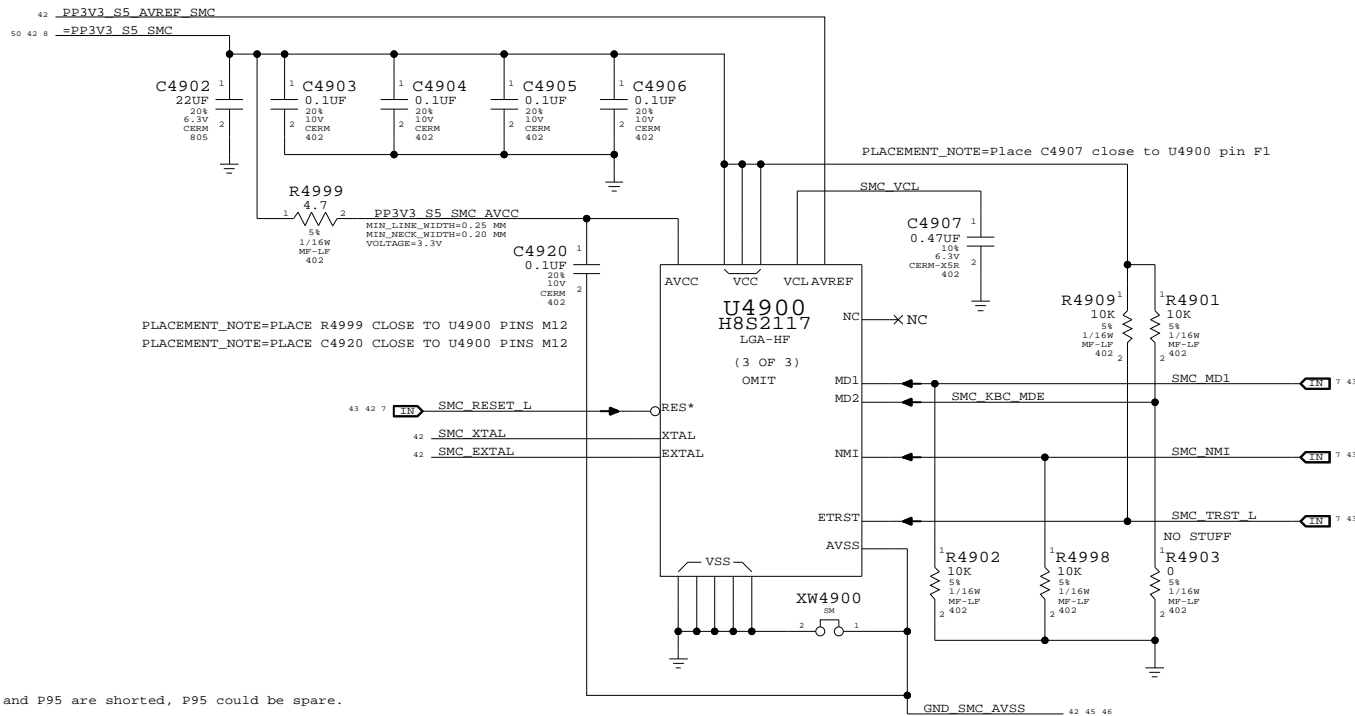
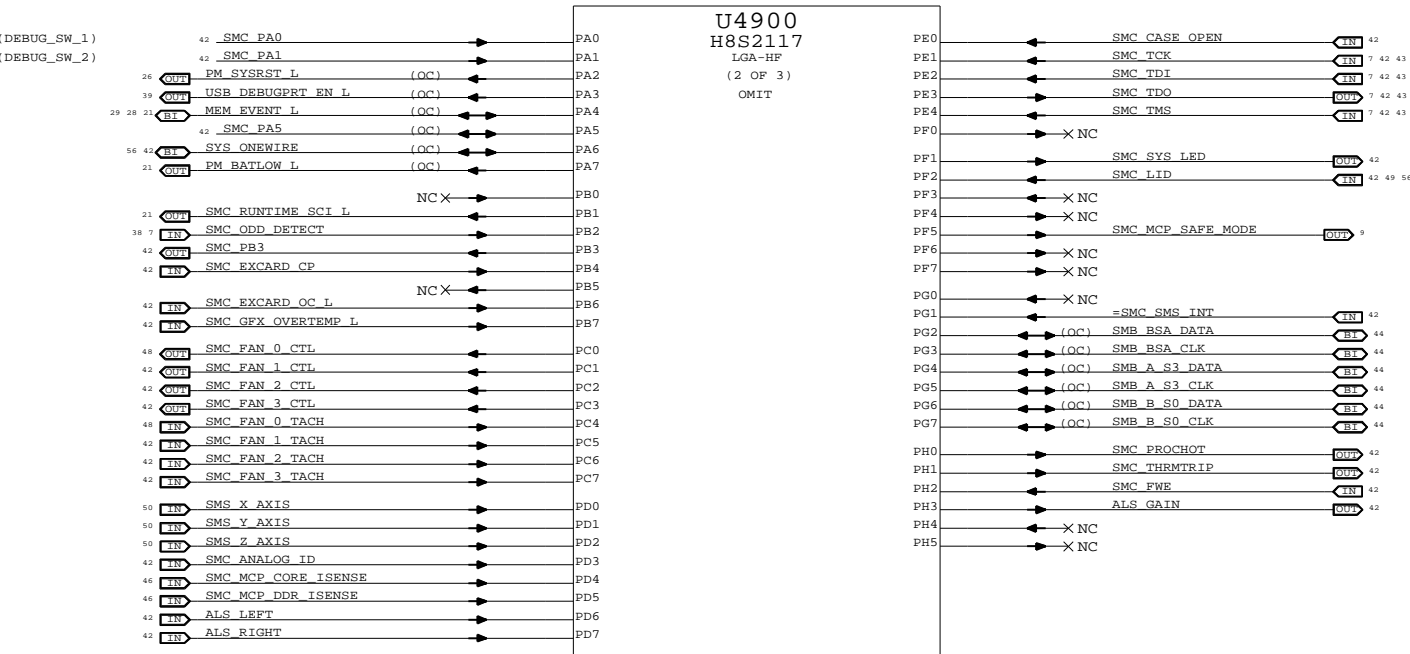
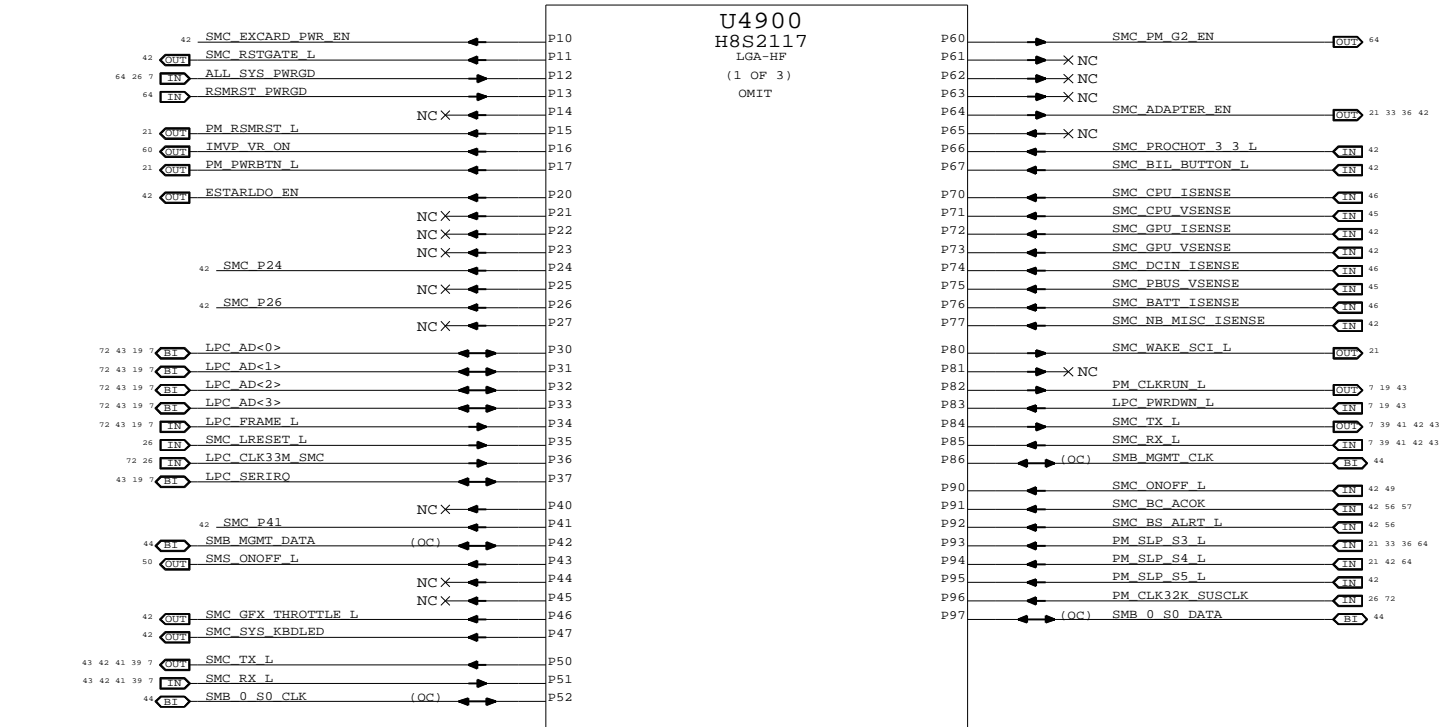
A

D

C

B

A



NOTE: P94 and P95 are shorted, P95 could be spare.

NOTE: SMS Interrupt can be active high or low, rename net accordingly. If SMS interrupt is not used, pull up to SMC rail.

SMC		
SYNC_MASTER=K36B_MLB		SYNC_DATE=08/17/2008
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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8089	02
SCALE	SHT	OF
NONE	49	109

D

D

C

C

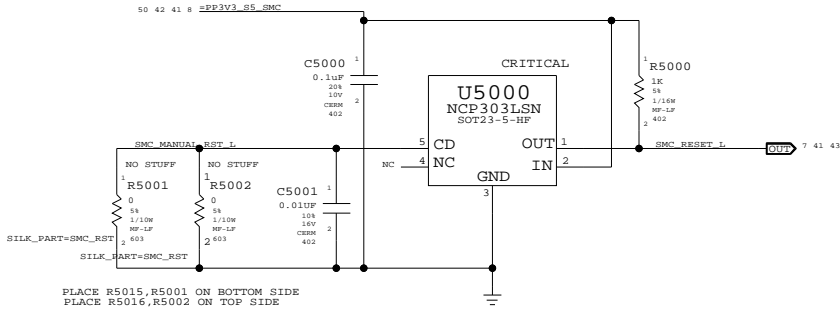
B

B

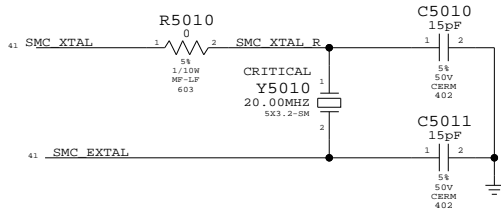
A

A

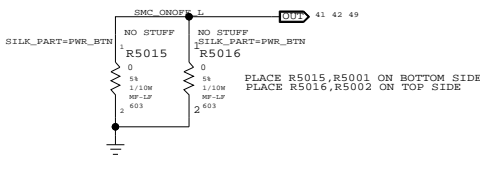
SMC Reset "Button" / Brownout Detect



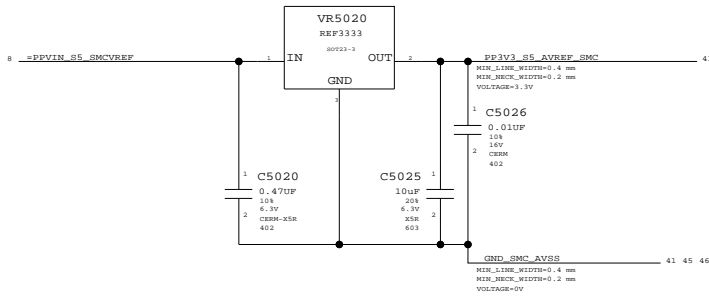
SMC Crystal Circuit



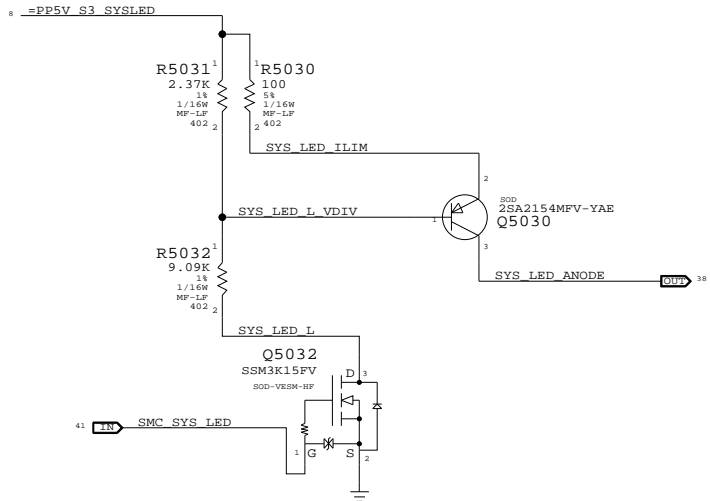
Debug Power "Button"



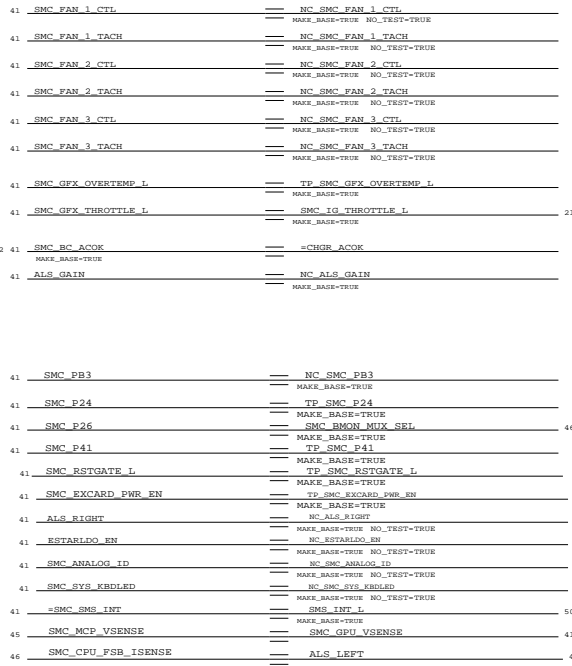
SMC AVREF Supply



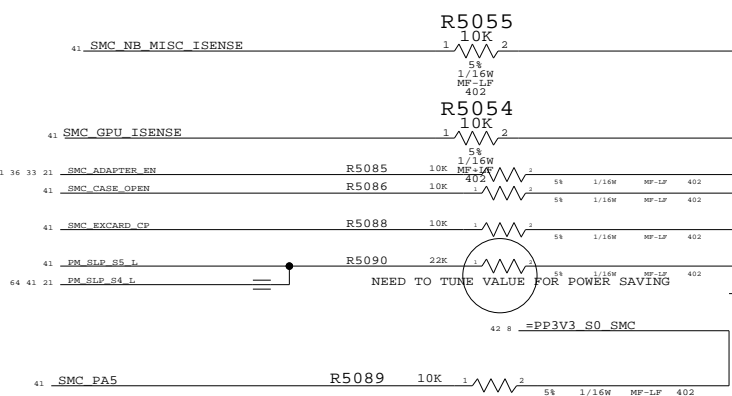
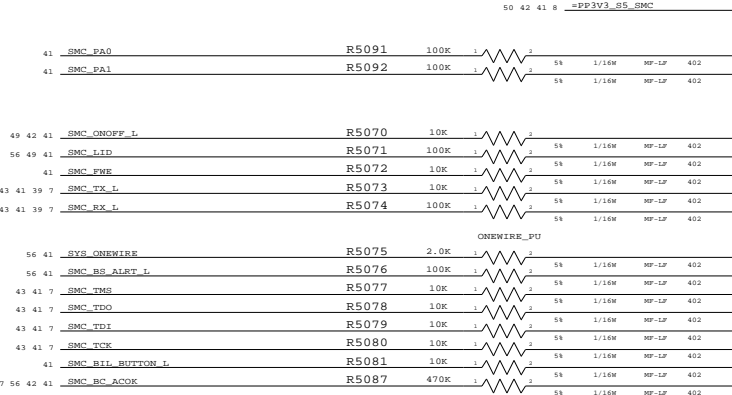
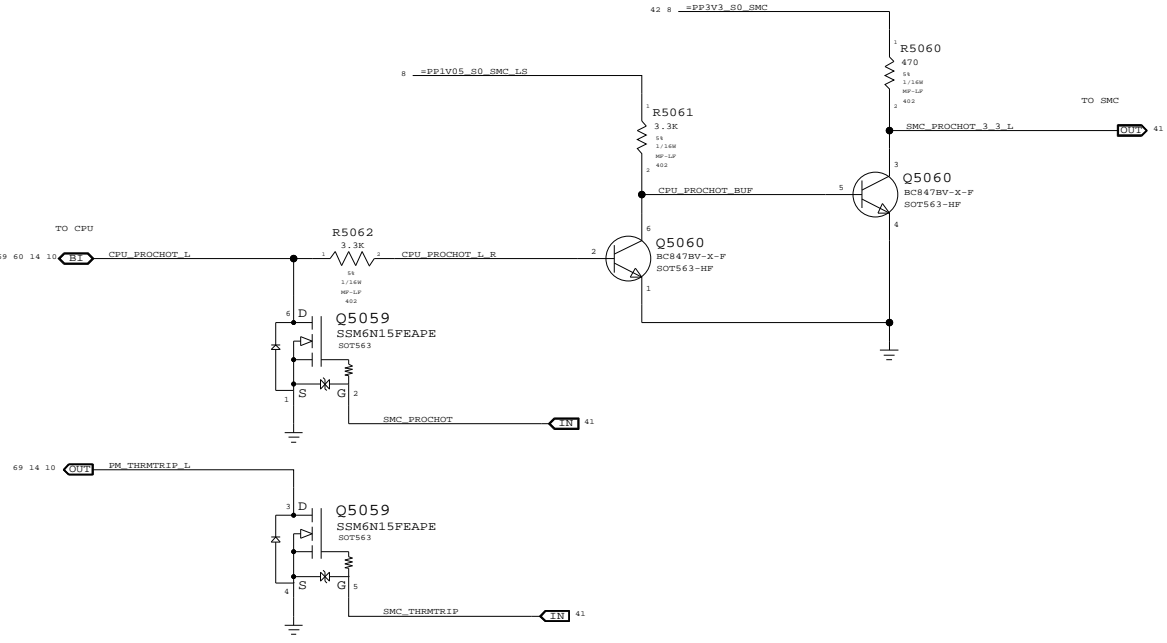
System (Sleep) LED Circuit



ADD NC ALIASES FOR FAN1 SIGNALS



SMC FSB to 3.3V Level Shifting



SMC Support

SYNC\_MASTER=K36B\_MLB SYNC\_DATE=08/17/2008

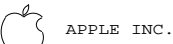
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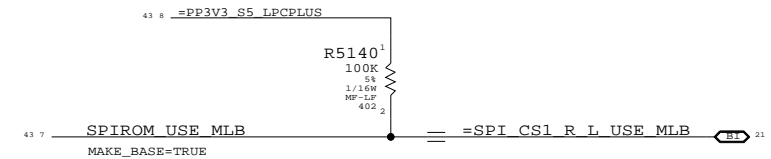
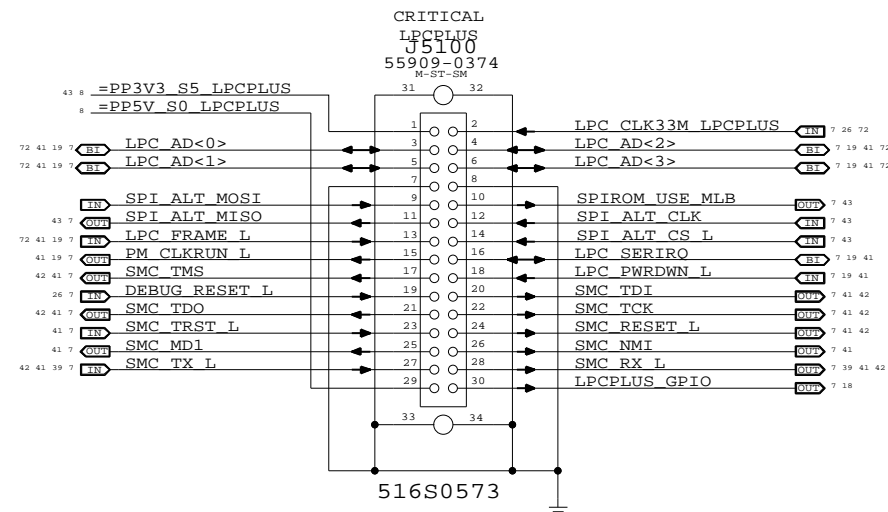
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APPLE INC.

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D	051-8089	02
SCALE	SHT	OF
NONE	50	109

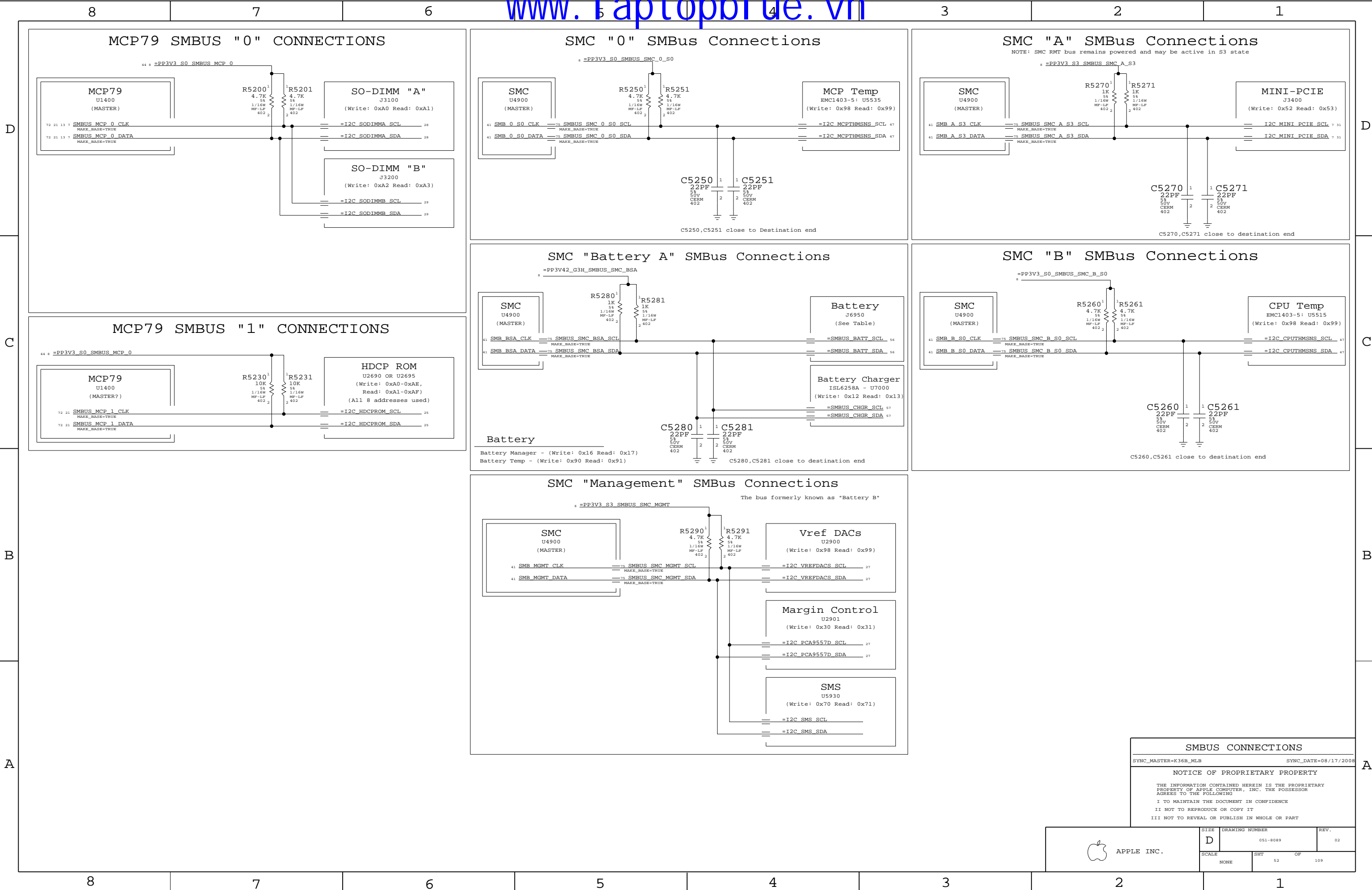


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**SMBUS CONNECTIONS**

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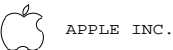
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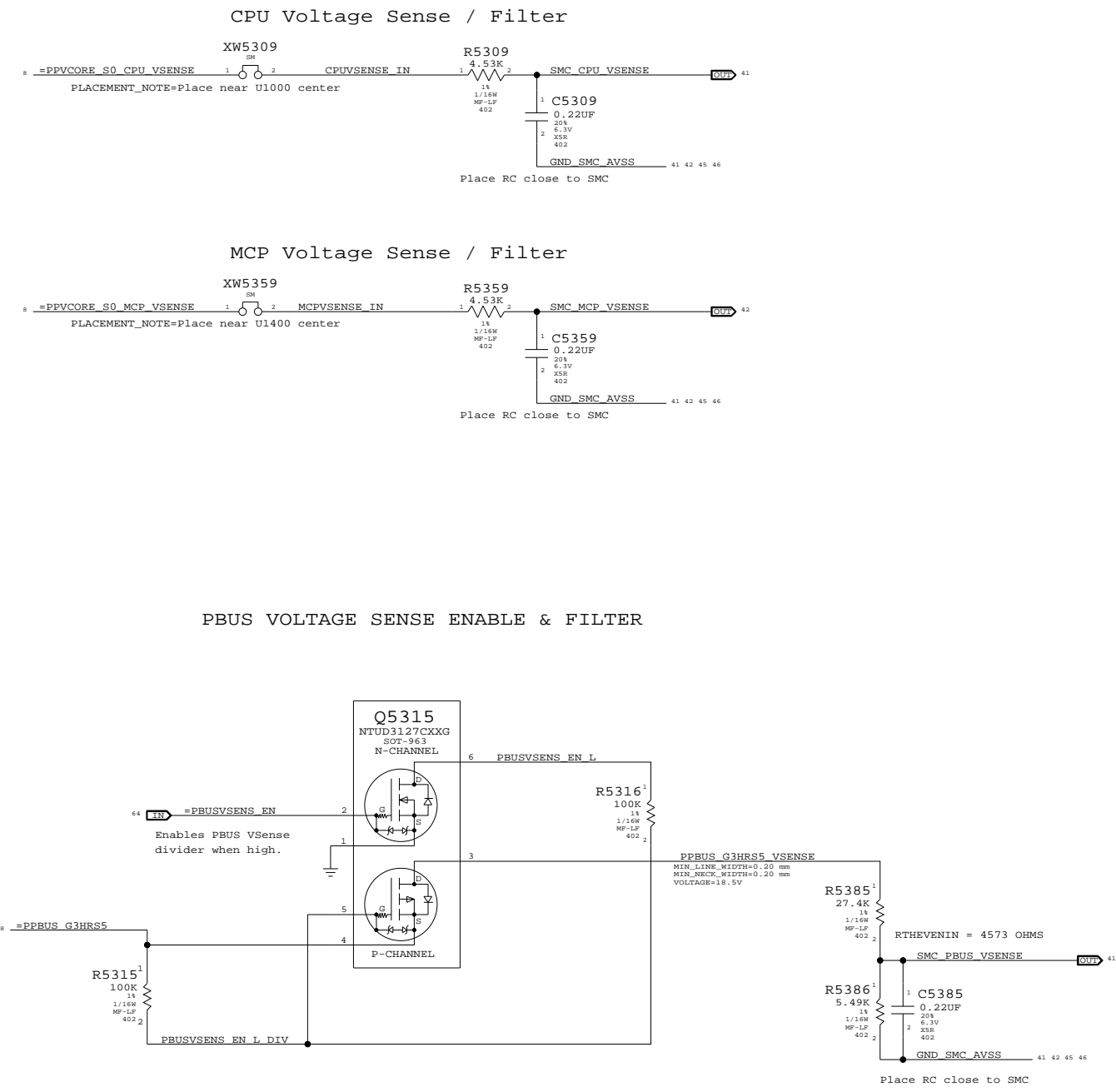
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SIZE	DRAWING NUMBER	REV.
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SCALE	SHT	OF
NONE	52	109



VOLTAGE SENSING

SYNC\_MASTER=K36B\_MLB

SYNC\_DATE=08/17/2008

NOTICE OF PROPRIETARY PROPERTY

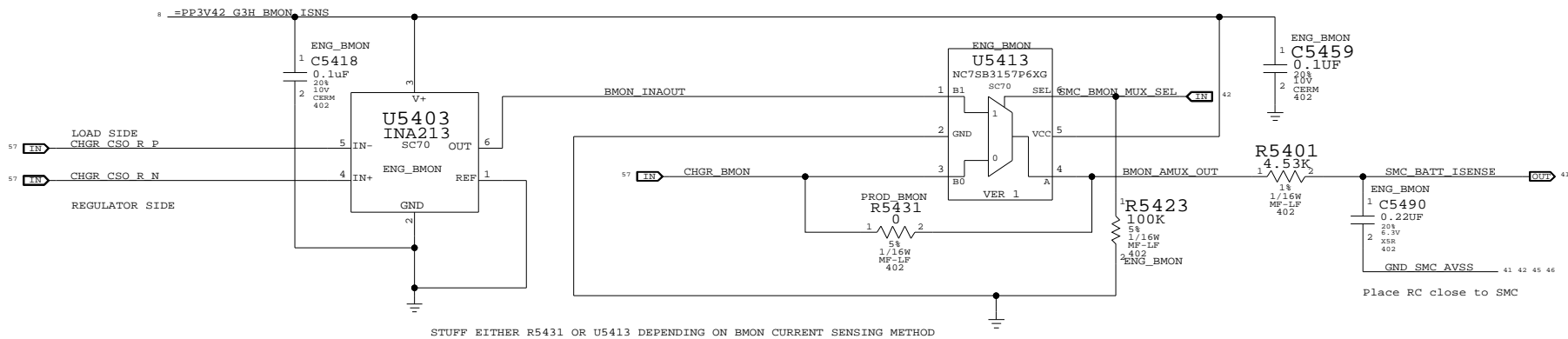
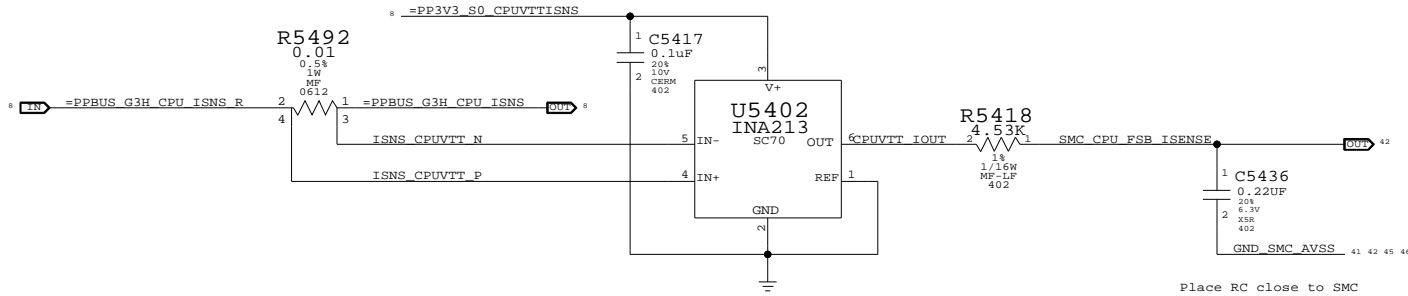
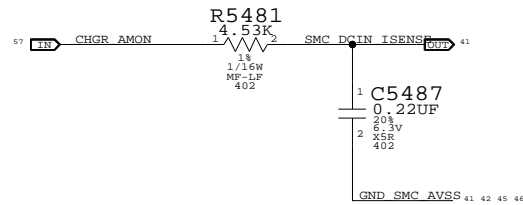
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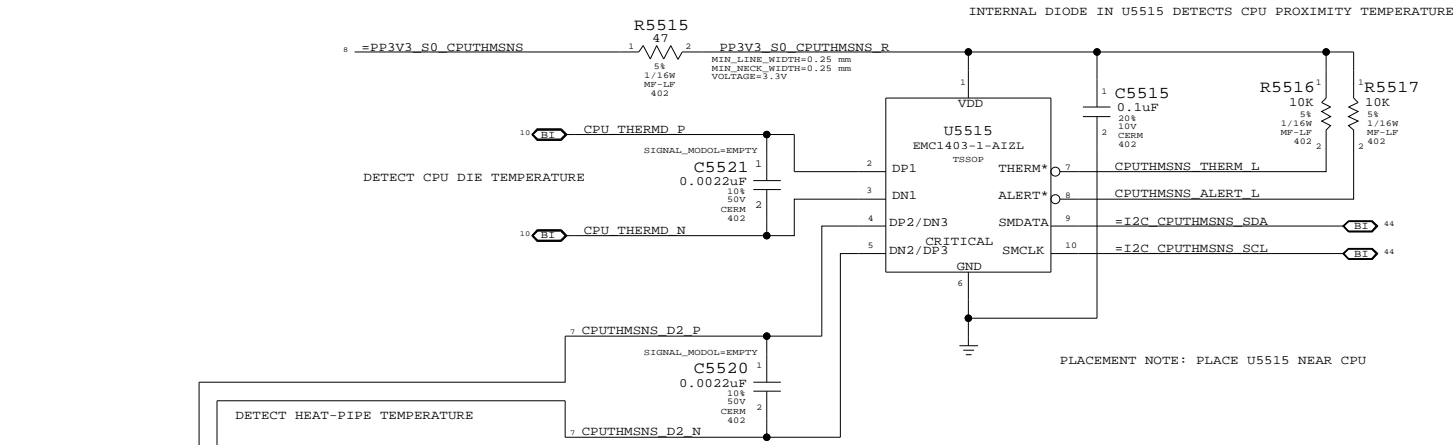
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-8089	02
SCALE		SHT	OF
NONE		53	109

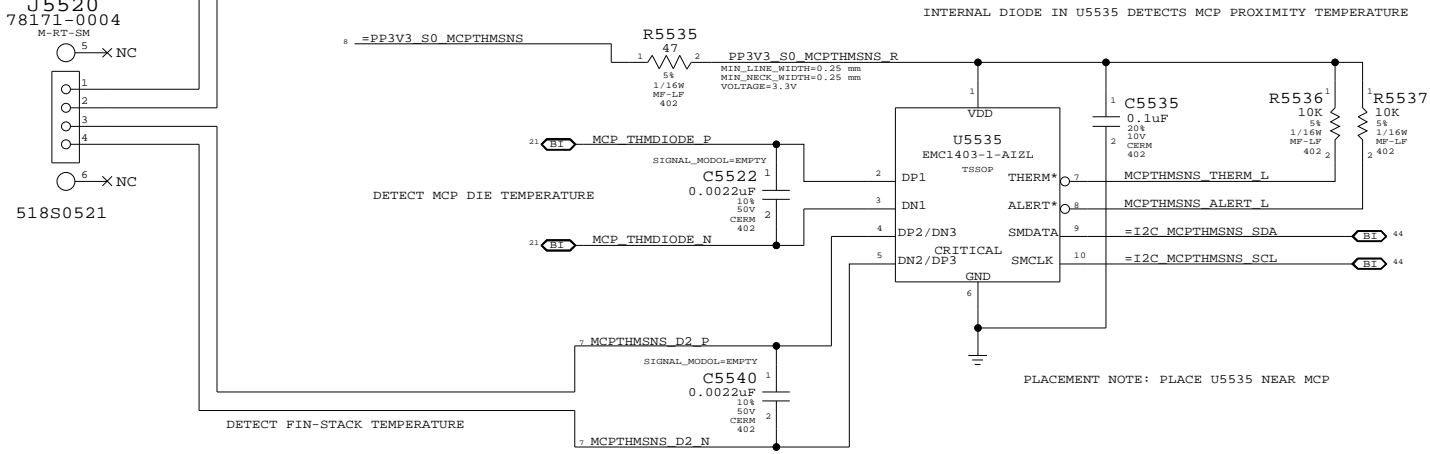


APPLE INC.

CPU T-Diode Thermal Sensor



MCP T-Diode Thermal Sensor



Thermal Sensors

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APPLE INC.

SIZE

D

DRAWING NUMBER

051-8089

REV.

02

SCALE

NONE

SHT

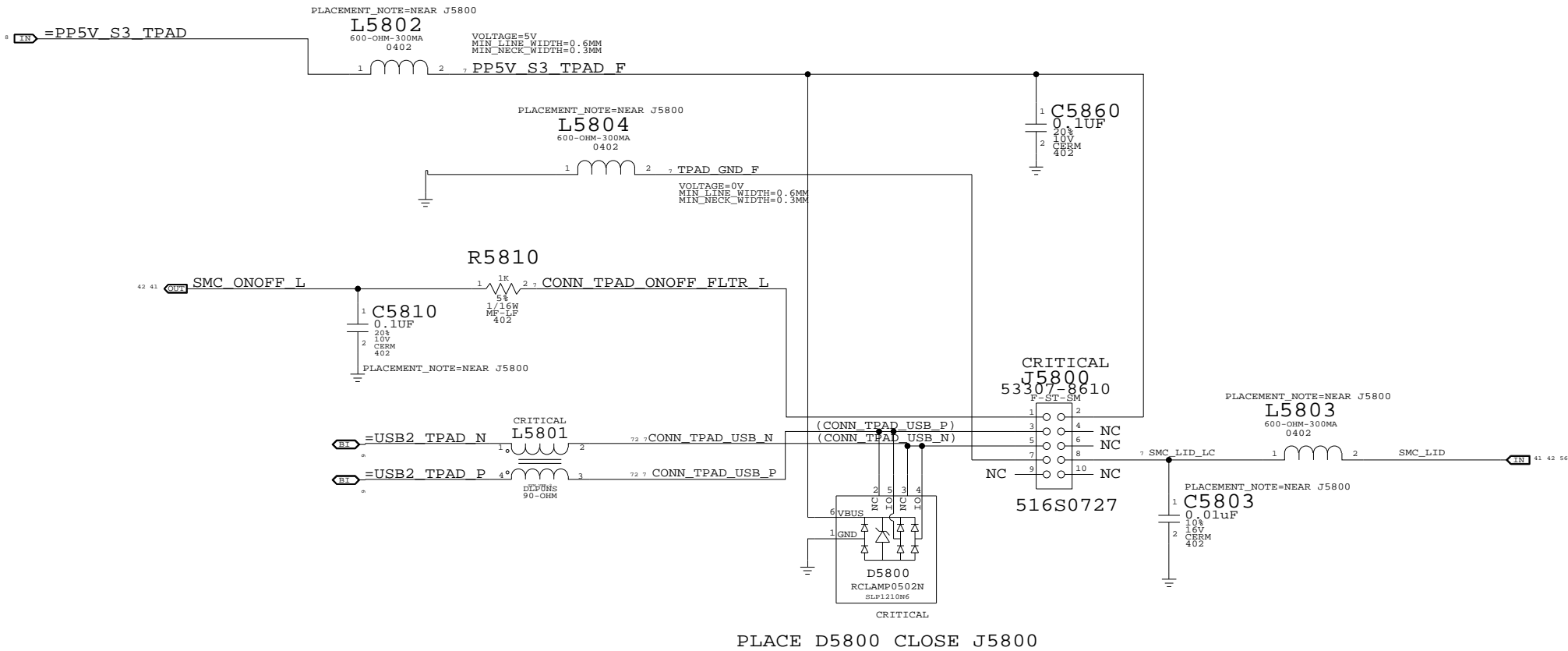
55

OF

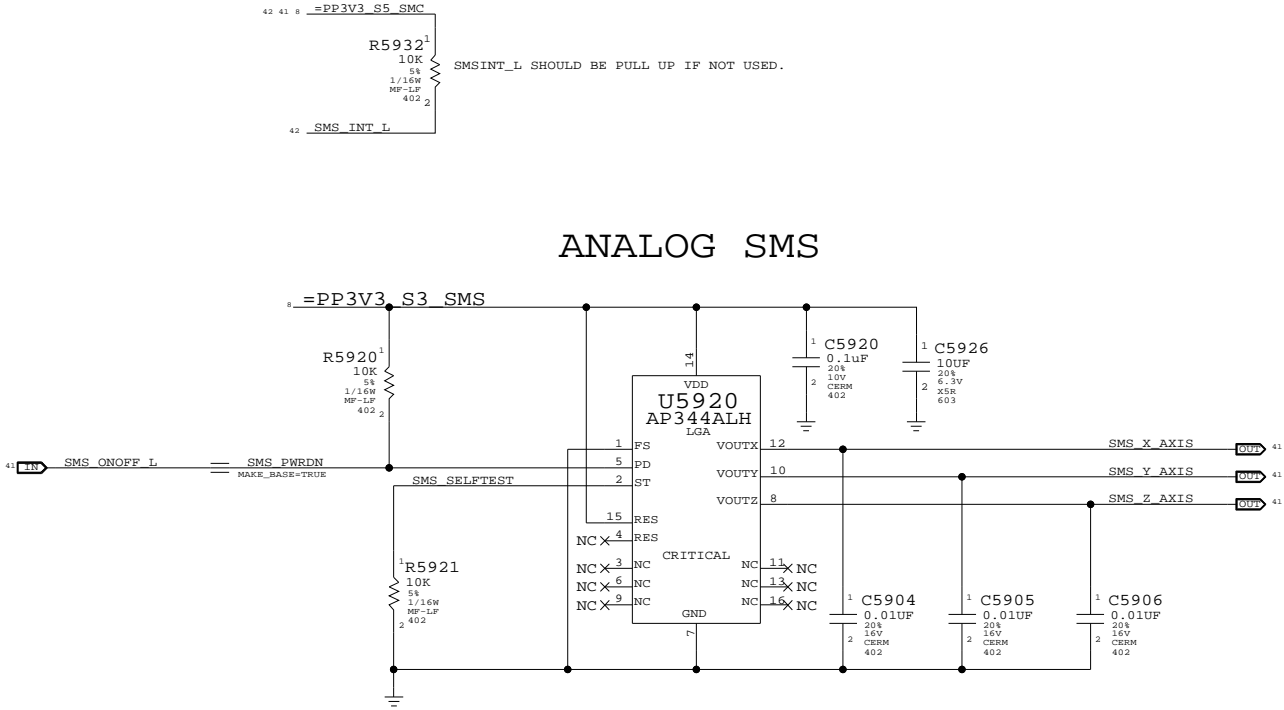
109



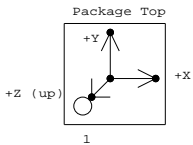
```
PLACE L5800,L5801,L5803 NEAR J5800
PLACE C5800,C5810,C5803 NEAR J5800
PLACE D5800 NEAR J5800
```



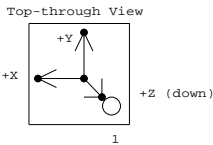
SYNC_MASTER=K36B_MLB		SYNC_DATE=08/17/2008	
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SIZE	DRAWING NUMBER		REV.
D	051-0809		02
SCALE	SHT	OF	
NONE	58	109	



Desired orientation when  
placed on board top-side:



Desired orientation when  
placed on board bottom-side:



Front of system

SMS

SYNC\_MASTER=K36B\_MLB

SYNC\_DATE=08/17/2008

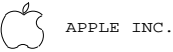
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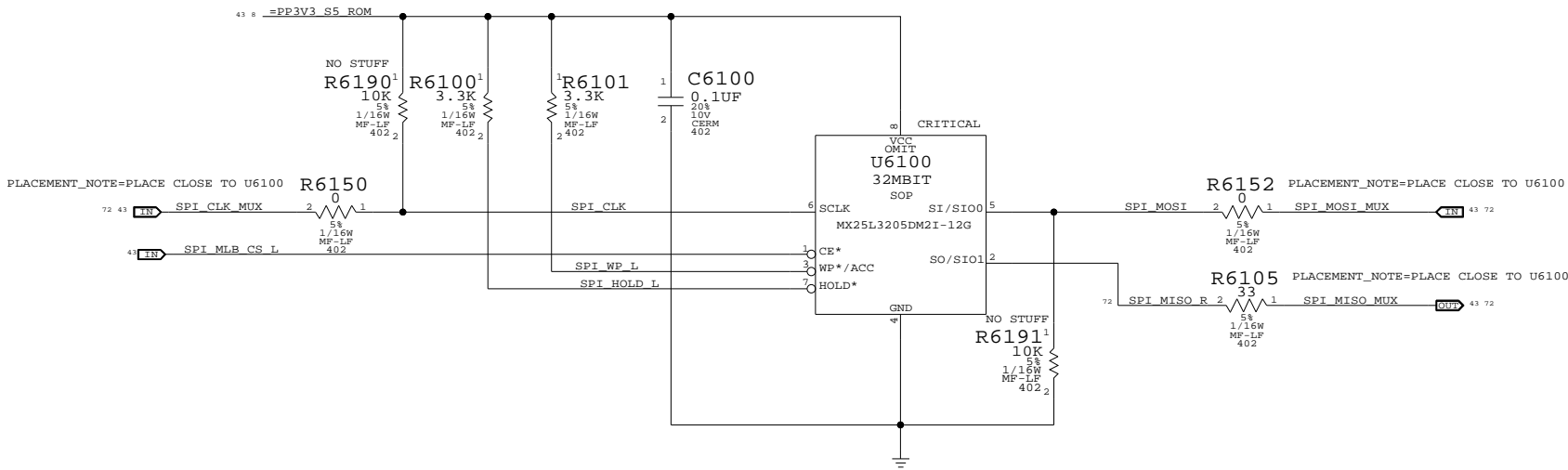
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D	051-8089	02
SCALE	SHT	OF
NONE	59	109



MCP79 SPI Frequency Select		
Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

25MHZ IS SECELECTED WITH R5164 AND R5144  
ANY FO THE 4 FREQUENCIES CAN BE SELECTED  
WITH R6190, R6191, R5164 AND R5144

SPI ROM

SYNC\_MASTER=K36B\_MLBSYNC\_DATE=081/17/2008

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## D



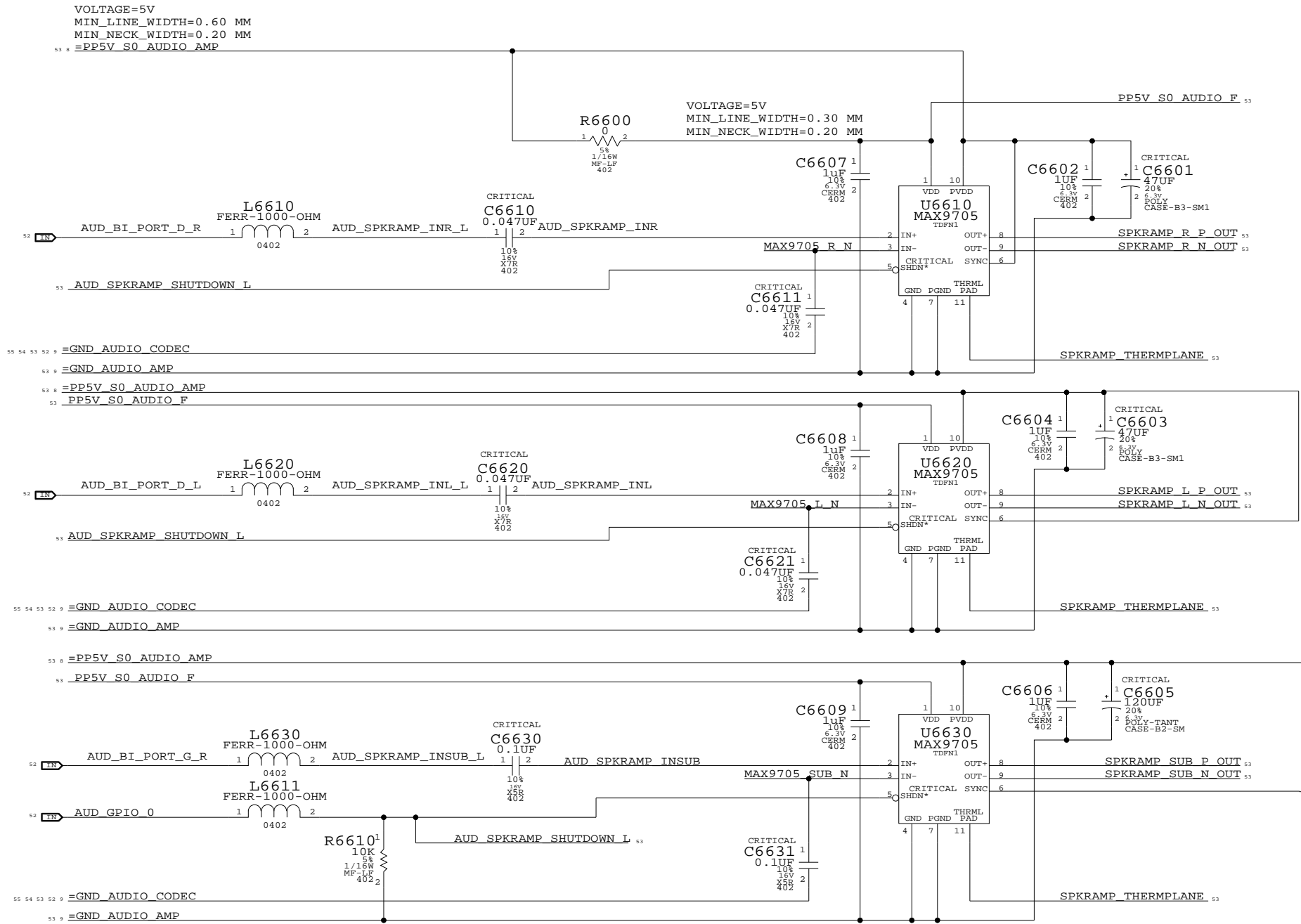
## B

A

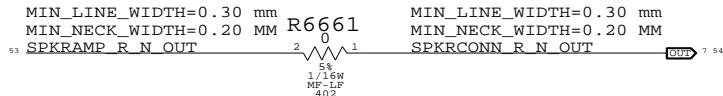
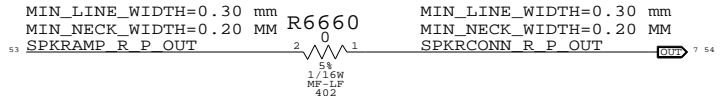
 APPLE INC.

SATELLITE & SUB TWEETER AMPLIFIER APN:353S1595

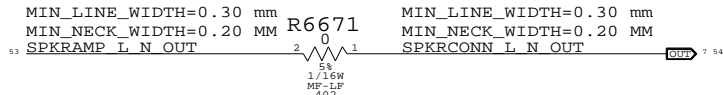
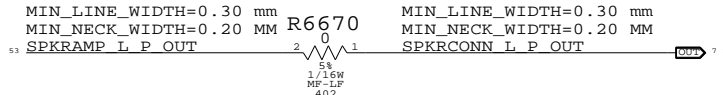
SATELLITE 169 HZ < FC < 282 HZ  
SUB 80 HZ < FC < 132 HZ  
GAIN 12DB



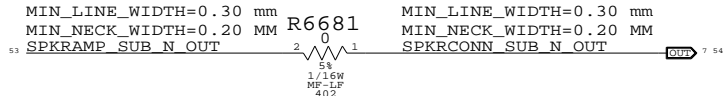
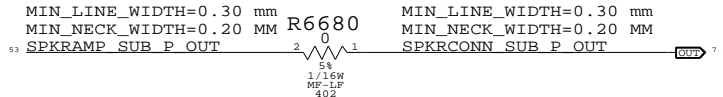
MIN\_LINE\_WIDTH=0.60 MM  
MIN\_NECK\_WIDTH=0.20 MM  
=GND\_AUDIO\_AMP  
XW6600  
SM  
SPKRAMP\_THERMPLANE



RIGHT SATELLITE



LEFT SATELLITE



SUB-TWEETER

AUDIO0: SPEAKER AMP

SYNC\_MASTER=K36A\_MLB SYNC\_DATE=08/29/2008

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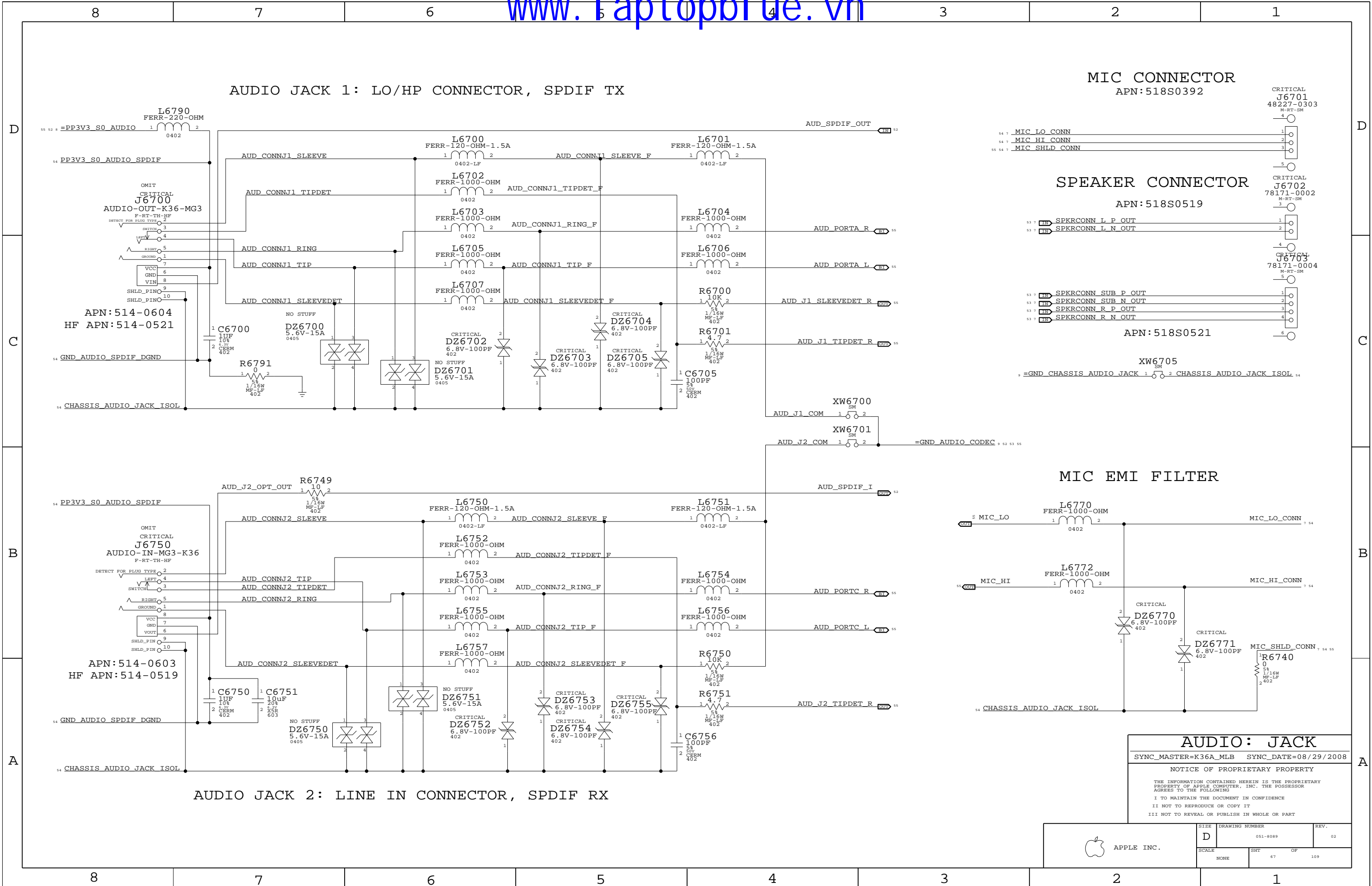
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SIZE D DRAWING NUMBER 051-8089 REV. 02

SCALE NONE SHT 66 OF 109

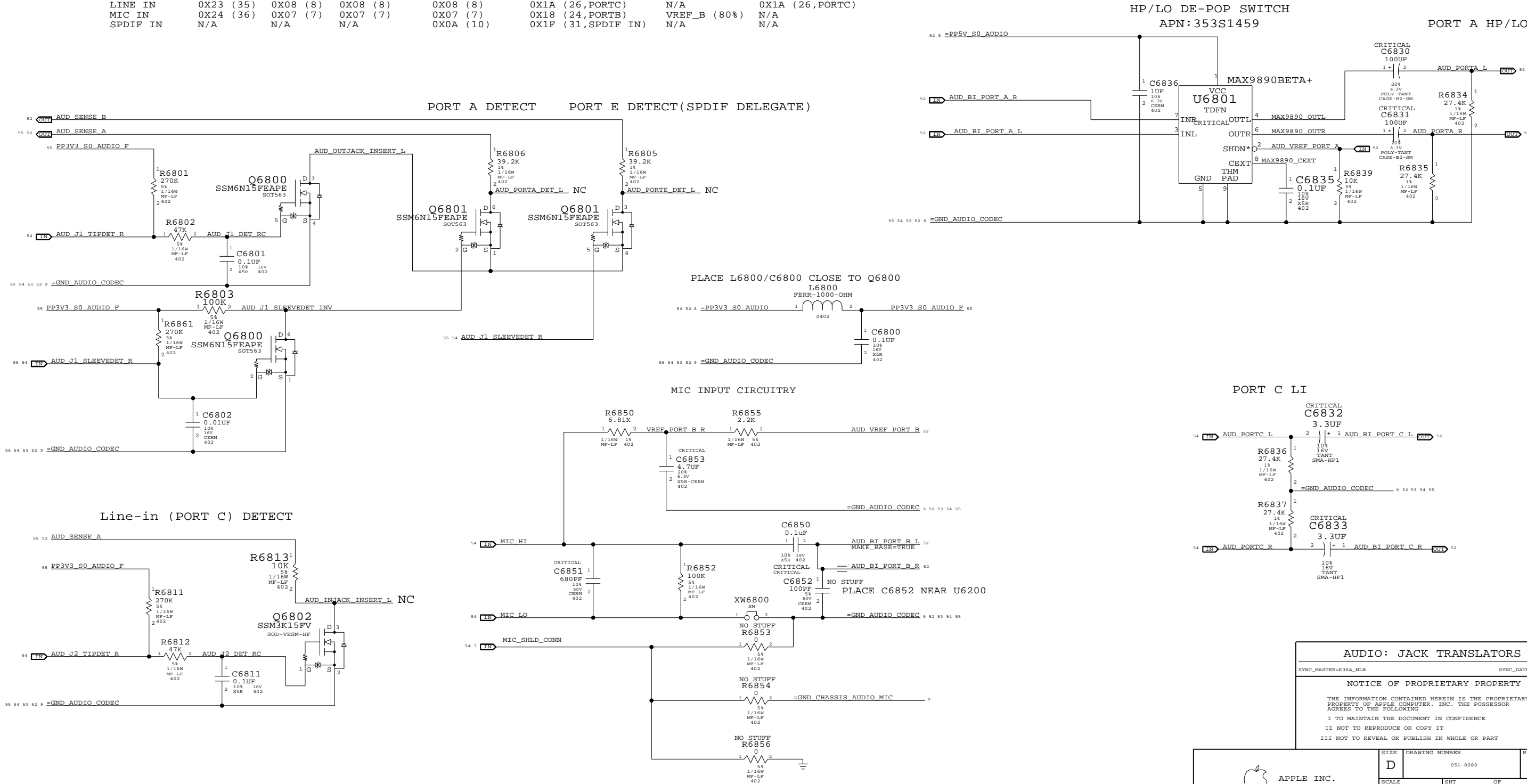


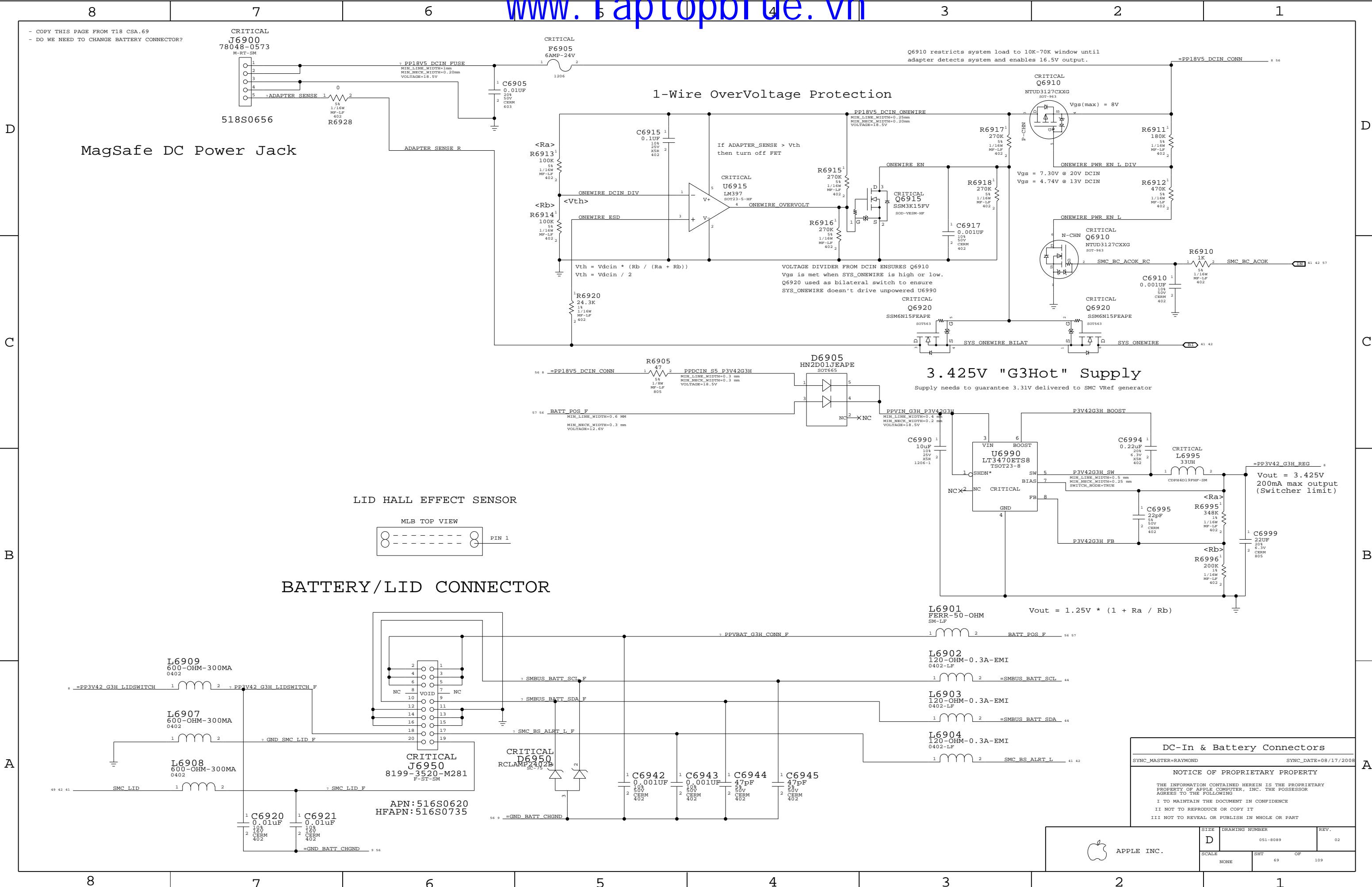
CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP OUT	0X0F (15)	0X05 (5)	0X15 (21,PORTA)	VREF_A(100%)	0X15 (21,PORTA)
SAT SPKR	0X26 (38)	0X25 (37)	0X14 (20,PORTD)	GPIO 0	N/A
SUB SPKR	0X0E (14)	0X04 (4)	0X16 (22,PORTG)	GPIO 0	N/A
SPDIF OUT	N/A	0X06 (6)	0X1E (30,SPDIF OUT)	N/A	0X1B (27,PORTE)

CODEC INPUT SIGNAL PATHS

FUNCTION	MIXER	VOLUME	MUTE CONTROL	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X23 (35)	0X08 (8)	0X08 (8)	0X08 (8)	0X1A (26,PORTC)	N/A	0X1A (26,PORTC)
MIC IN	0X24 (36)	0X07 (7)	0X07 (7)	0X07 (7)	0X18 (24,PORTB)	VREF_B (80%)	N/A
SPDIF IN	N/A	N/A	N/A	0X0A (10)	0X1F (31,SPDIF IN)	N/A	N/A

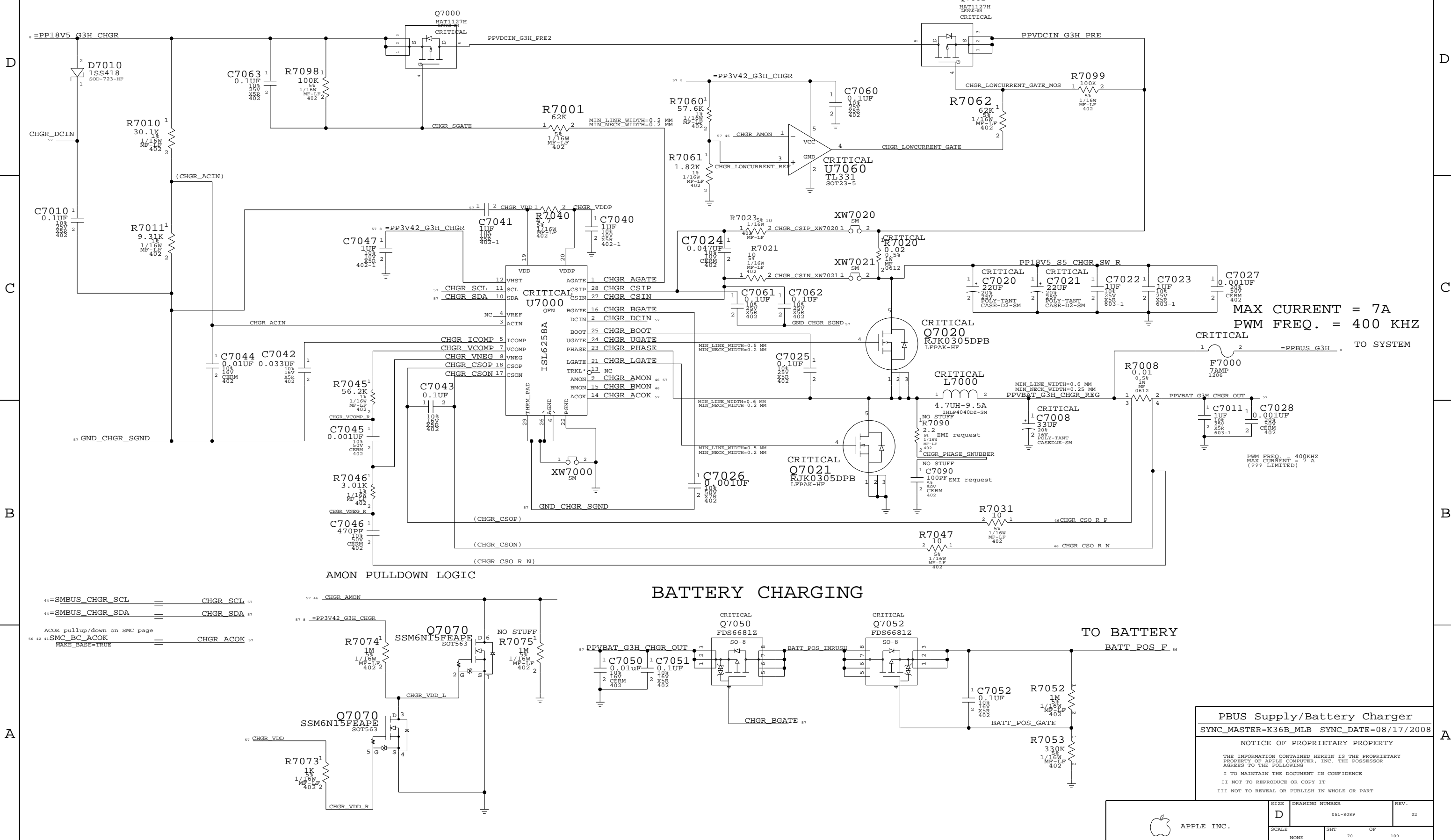




DC-In & Battery Connectors		
SYNC_MASTER=RAYMOND		SYNC_DATE=08/17/2008
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-8089	02
SCALE		SHT	OF
NONE		69	109

# PBUS SUPPLY / BATTERY CHARGER



PBUS Supply/Battery Charger  
SYNC\_MASTER=K36B\_MLB SYNC\_DATE=08/17/2008

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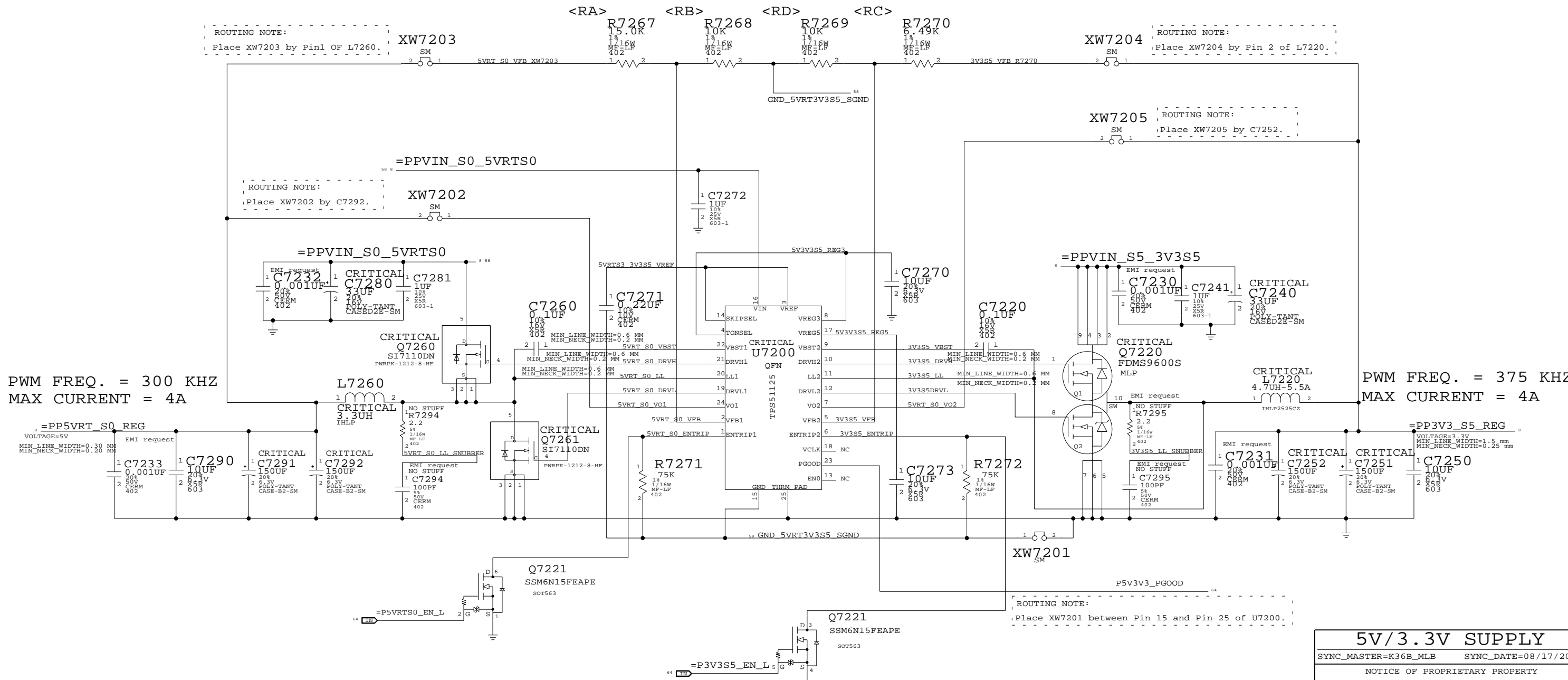
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-8089	02
	SCALE	SHT	OF
	NONE	70	109

# 5V\_RT/3.3V POWER SUPPLY

$$VOUT = (2 * RA / RB) + 2$$
$$VOUT = (2 * RC / RD) + 2$$



5V/3.3V SUPPLY

SYNC\_MASTER=K36B\_MLB    SYNC\_DATE=08/17/2008

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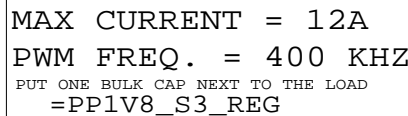
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

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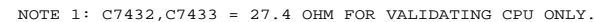
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-8089	02
SCALE		SHT	OF
NONE		72	109

# 1.8V / 0.9V ( DDR2 ) POWER SUPPLY



STATE	PM_SLP_S4_L	PM_SLP_S3_L	PP1V8_S3	PP0V9_S0
S0	HIGH	HIGH	1.8V	0.9V
S3	HIGH	LOW	1.8V	0.0V
S5/G3HOT	LOW	LOW	0.0V	0.0V



```
R1100/R1101  **ON THE CPU PAGE**  PROTECT THE IMVP6 IF THE CPU IS NOT INSTALLED
```

	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
60 IMVP6 PHASE1	1.5 MM	0.25 MM	
60 IMVP6 BOOT1	0.25 MM	0.25 MM	
60 IMVP6 UGATE1	1.5 MM	0.25 MM	
60 IMVP6 LGATE1	1.5 MM	0.25 MM	
60 IMVP6 ISEN1	0.25 MM	0.25 MM	

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAIS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
CPU_VCCSENSE_P		
CPU_VCCSENSE_N		
IMVP6_RTIN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

IMVP6 CPU VCore Regulator  
SYNC\_MASTER=K36B\_MLB SYNC\_DATE=08/17/2008

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CEP	EDAMING NEEDED
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SIZE	DRAWING NUMBER	REV.
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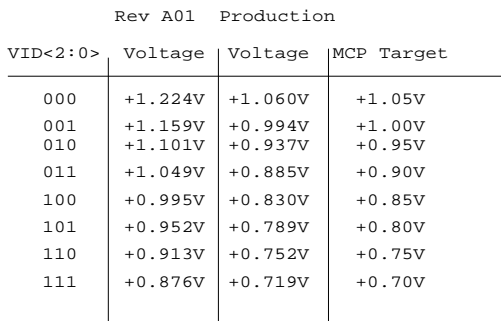
 APPLE INC.

SIZE	DRAWING NUMBER	REV.
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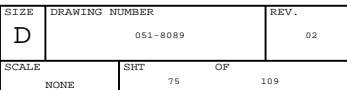
D	051-8089	
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D		
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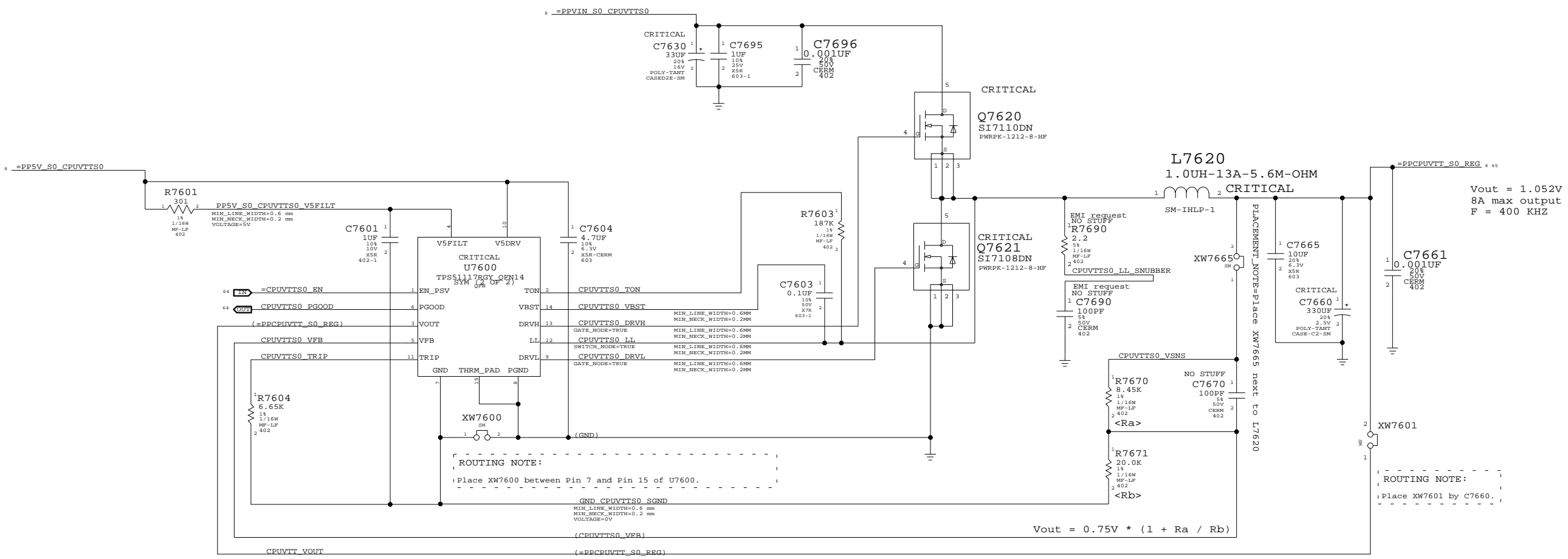
SCALE	SHT	OF
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MCP VCORE REGULATOR	
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CPUVTT POWER SUPPLY



CPU VTT(1.05V) SUPPLY

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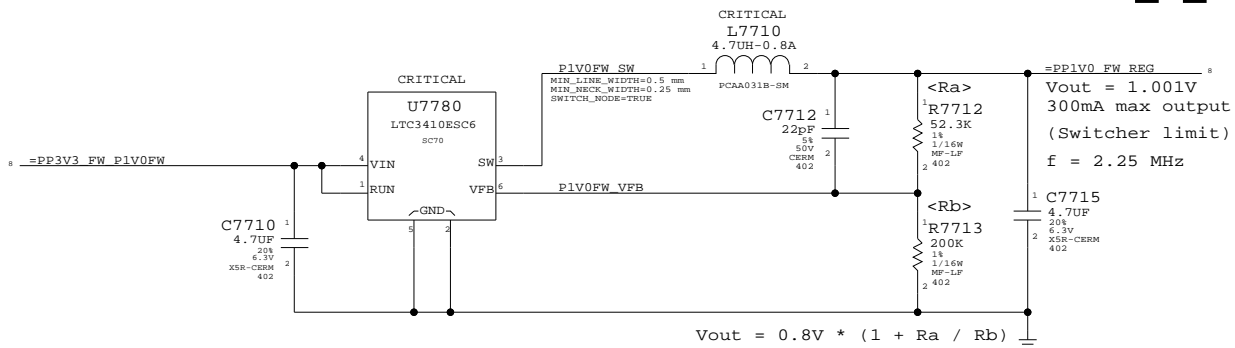
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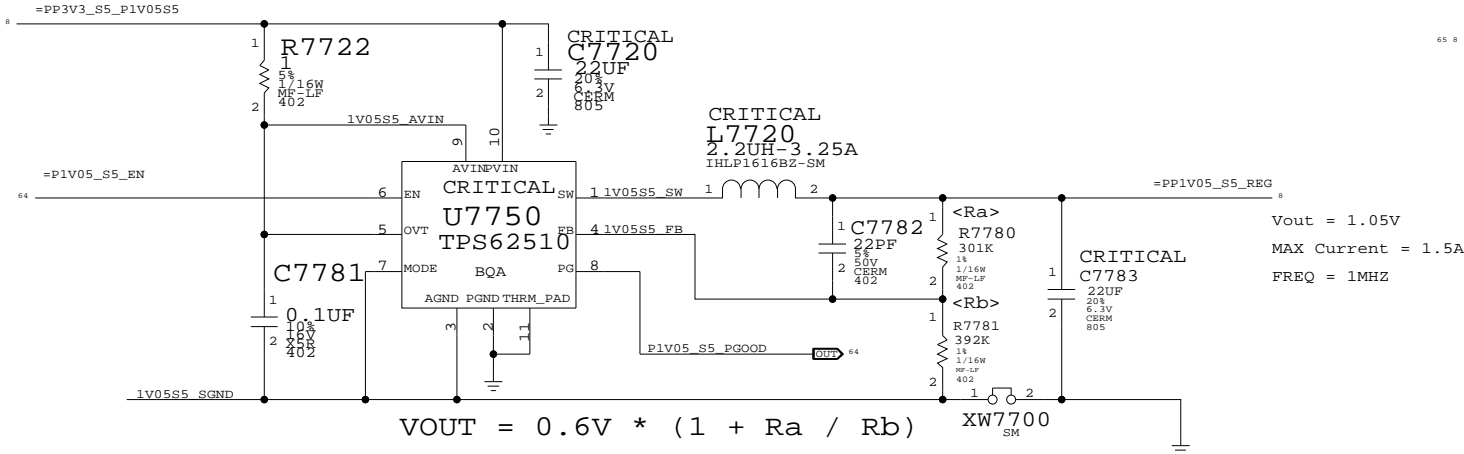
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NONE		76	109

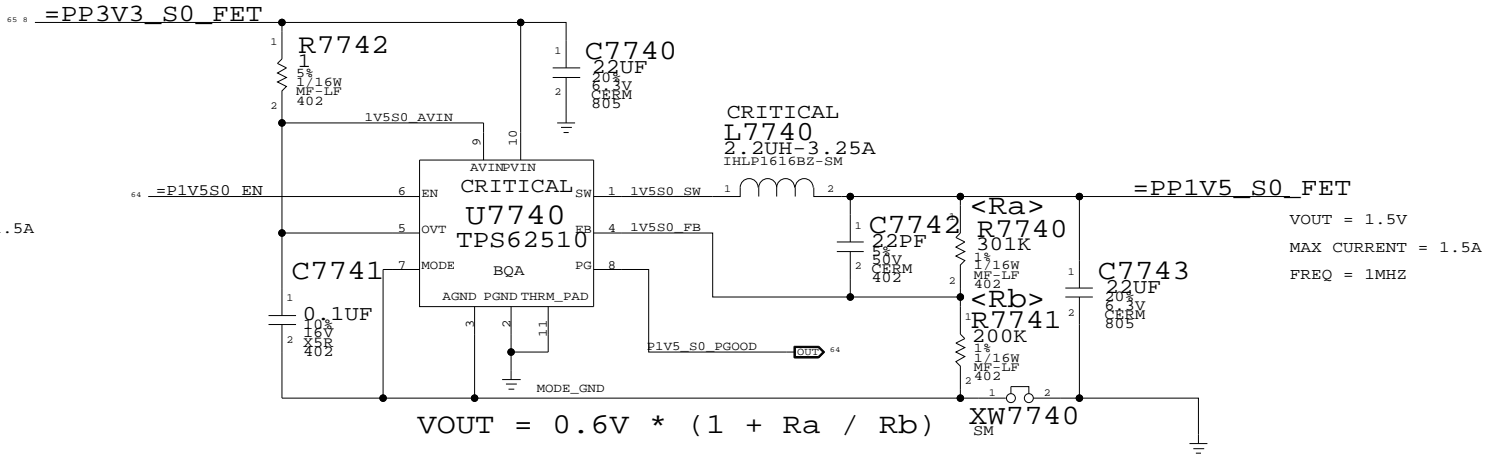
FireWire 1.0V (Core) Supply



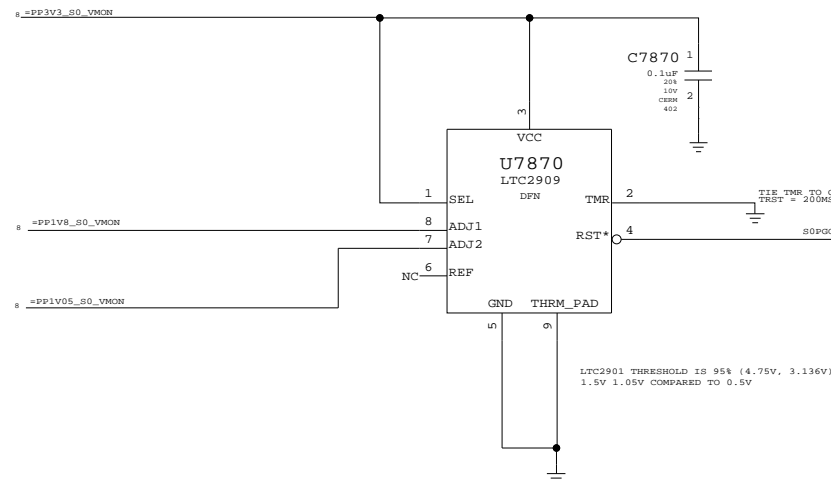
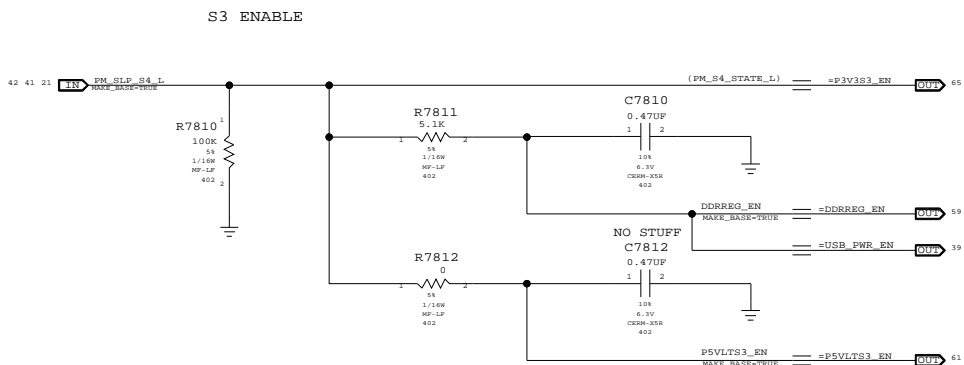
MCP 1.05V\_S5 AUXC SUPPLY



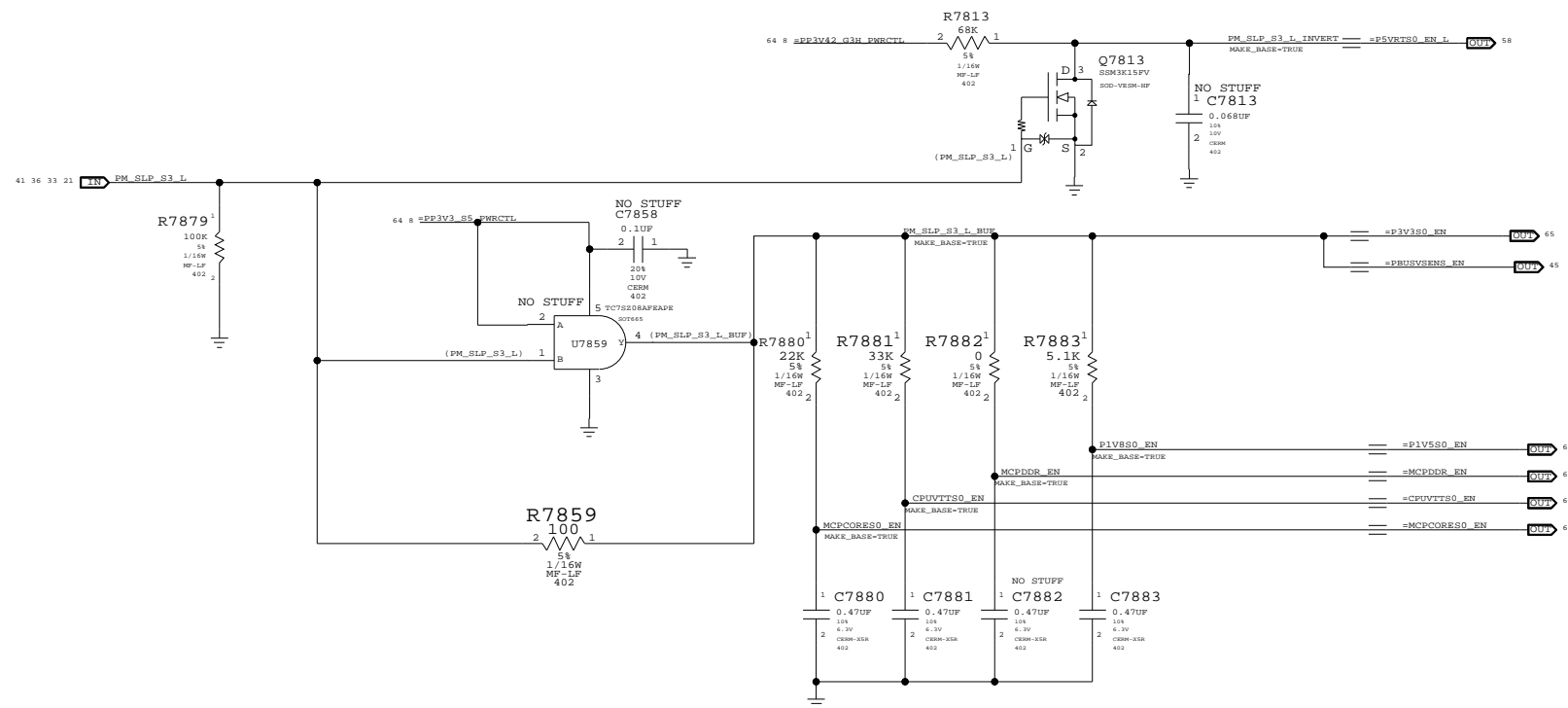
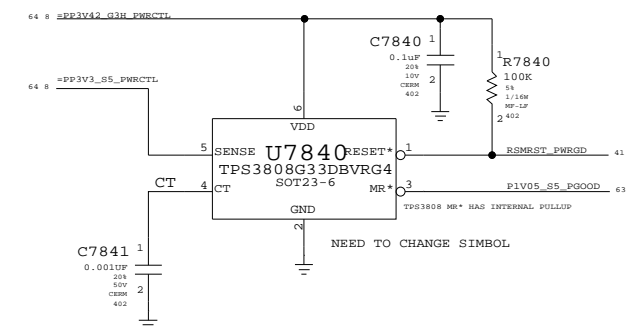
1.5V S0 SWITCH



MISC POWER SUPPLIES  
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```
5VLT_S0, 3.3V_S0, 1.8V_S0 ENABLE
MCPDDR, CPUVTT, MCPCORES0 ENABLE
1.5V S0 AND 1.05V S0 ENABLE
```

[illegible]

```
TP_ENETLV_PGOOD      — ENETLV_PGOOD
MAKE BASE-TRUE      —
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 APPLE INC.

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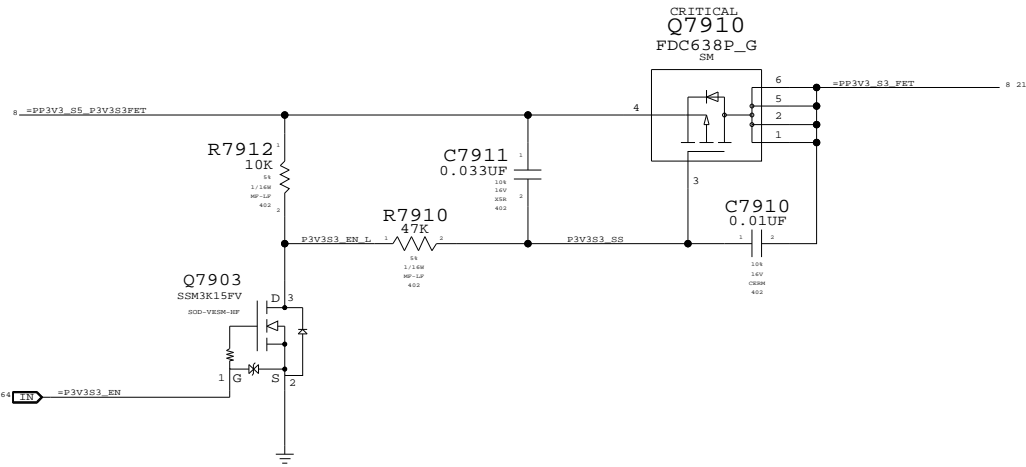
D

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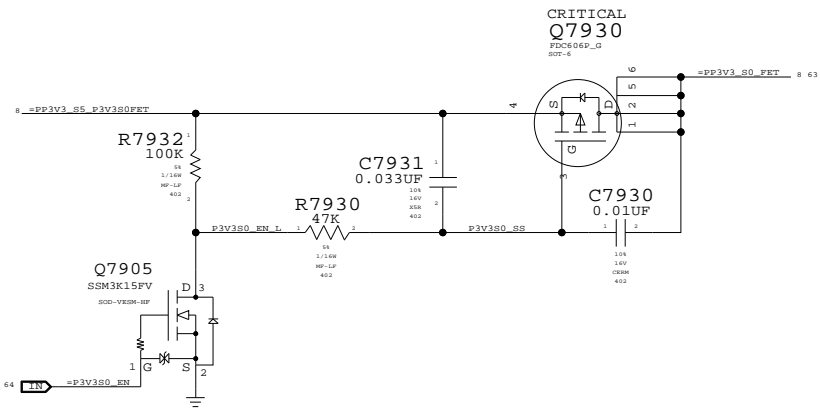
3.3V S3 FET



3.3V S3 FET

MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.182 A (EDP)

3.3V S0 FET

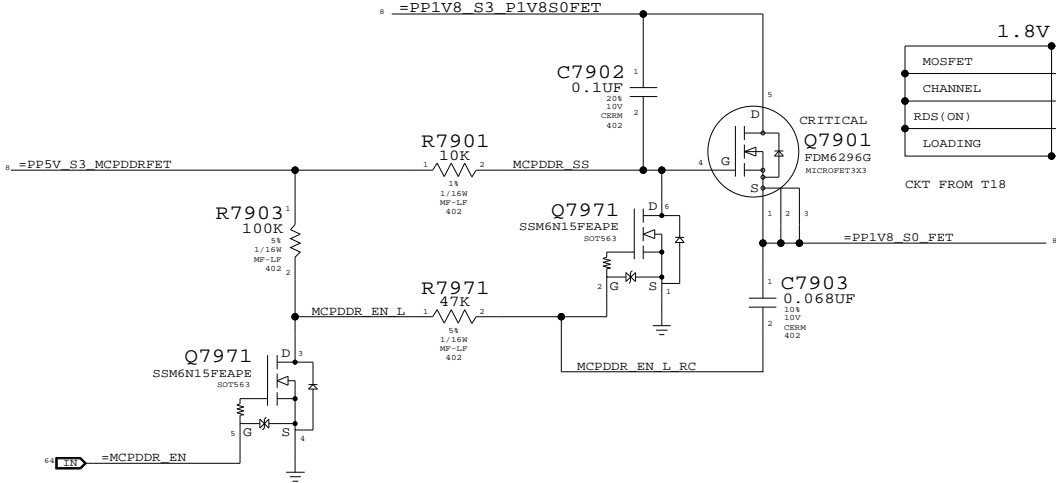


3.3V S0 FET

MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 MOHM @4.5V
LOADING	1.431 A (EDP)

1.8V S0 FET

(1.8V S0 FET FOR DDR2 MEM)

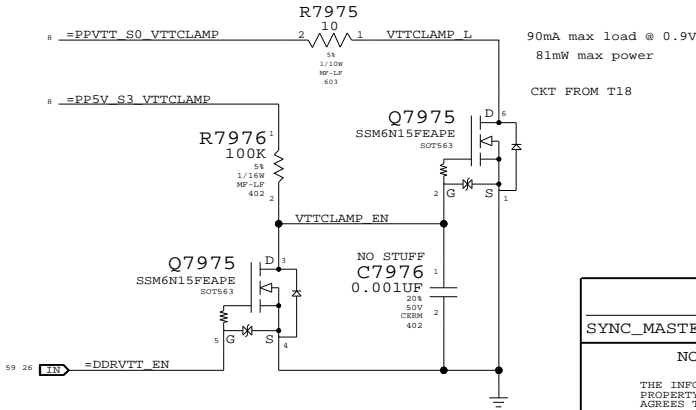


1.8V S0 FET

MOSFET	FDM6296G
CHANNEL	N-TYPE
RDS(ON)	15 MOHM @4.5V VGS
LOADING	5A (EDP)

MCP79 DDRVTT FET

MCP79 DDR PAD LEAKAGE IS HIGH ENOUGH THAT NVIDIA RECOMMENDS UNPOWERING DURING SLEEP. IN ORDER TO SUPPORT UNPOWERING RAIL, HARDWARE MUST GUARANTEE MEM\_CKE SIGNALS ARE LOW BEFORE RAIL IS TURNED OFF, AND REMAINS LOW UNTIL AFTER RAIL TURNS BACK ON OR DIMMS WILL EXIT SELF-REFRESH PREMATURELY. MEM\_VTT\_EN OUTPUT FROM MCP79 USED TO ENABLE CLAMP ON VTT RAIL, WHICH PULLS ALL CKE SIGNALS LOW THROUGH VTT TERMINATION RESISTORS.



POWER FETS

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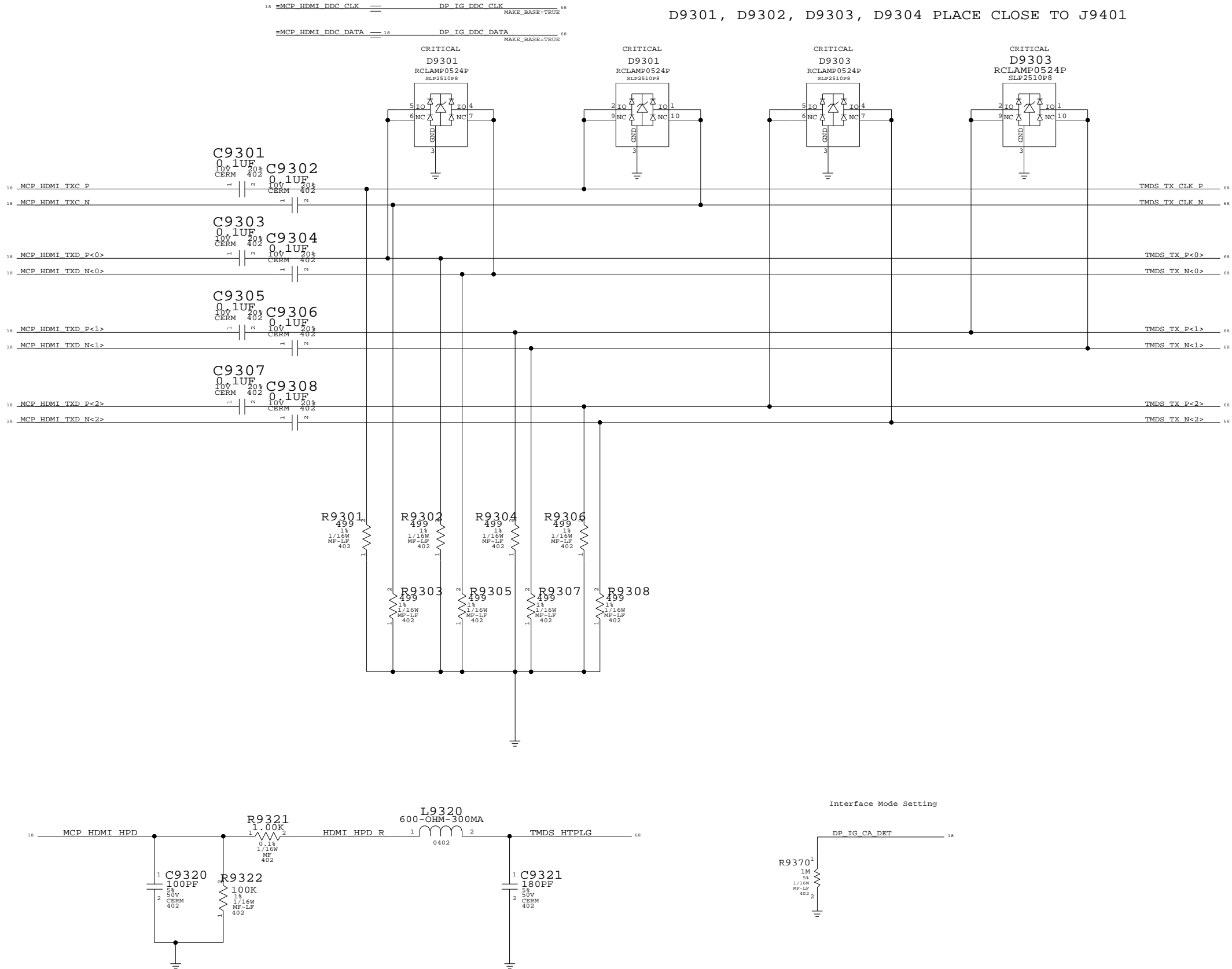
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TMDS ALIASES

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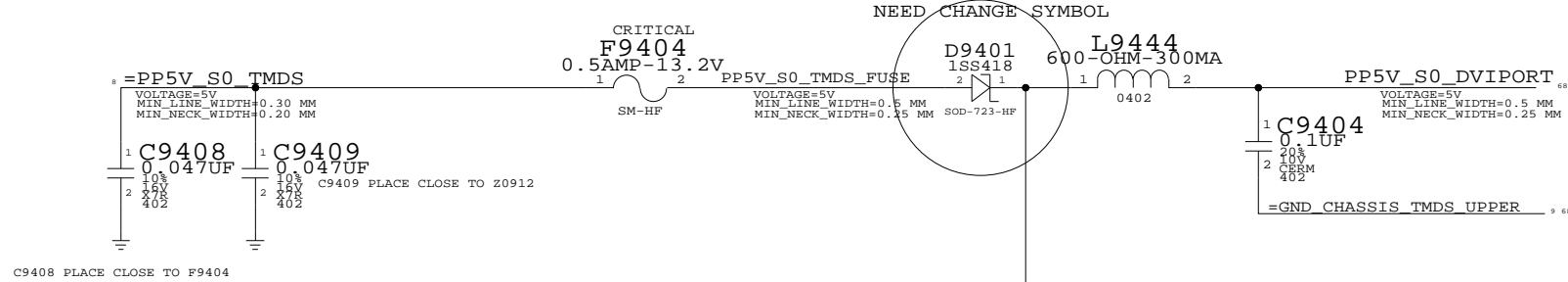
 APPLE INC.	SIZE	DRAWING NUMBER		REV.
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SCALE		SHT	OF	REV.
NONE		93	109	

Video Connectors

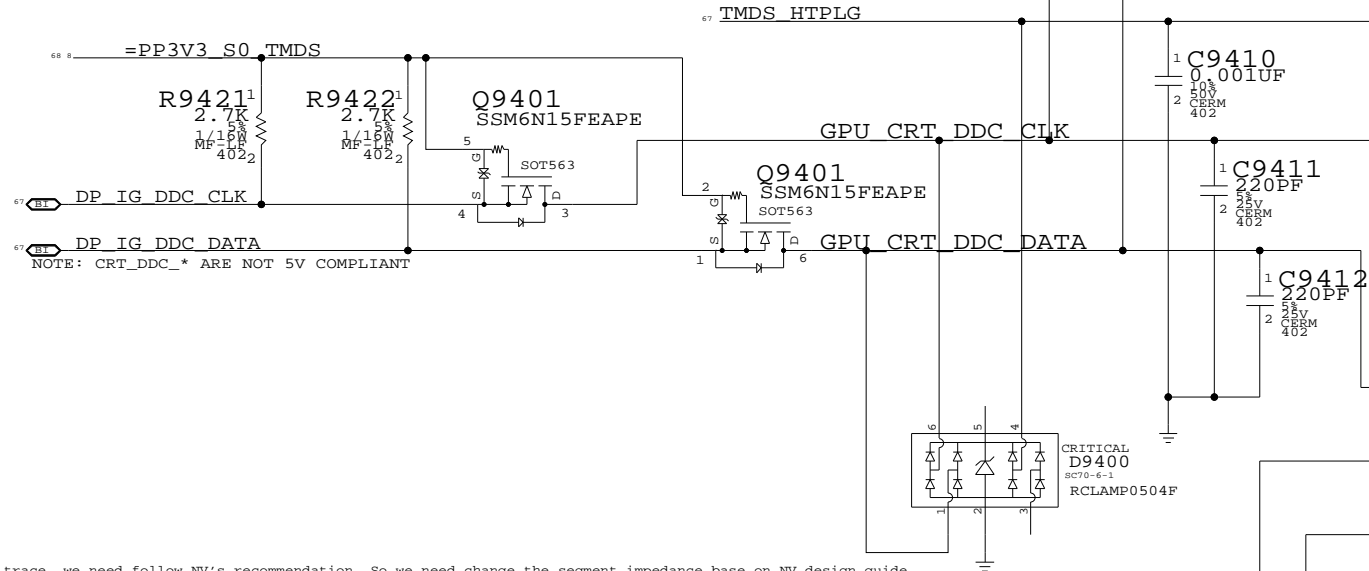
EXTERNAL VIDEO (VGA) INTERFACE

Isolation required for DVI power switch

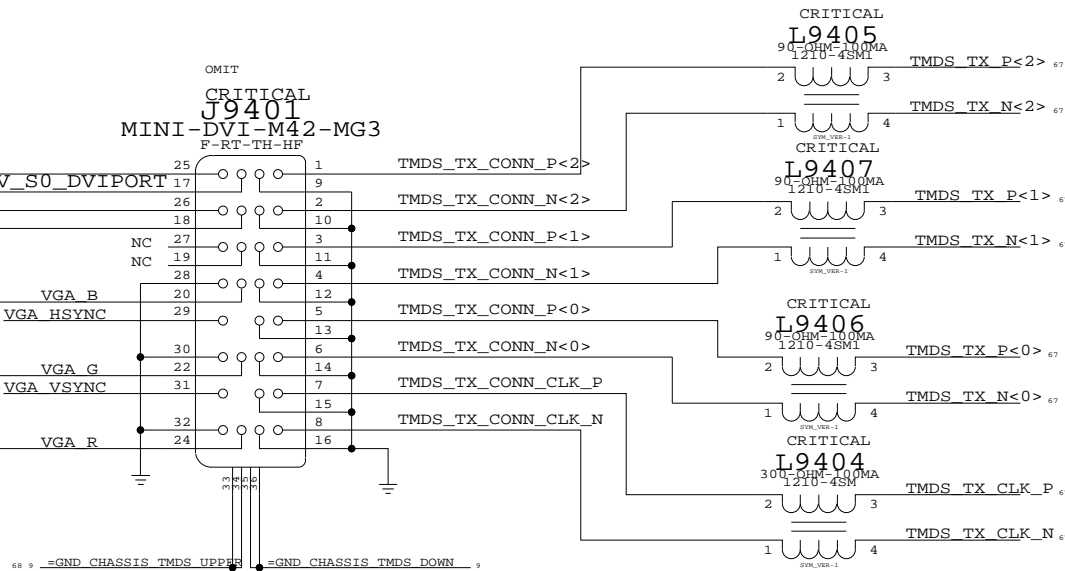
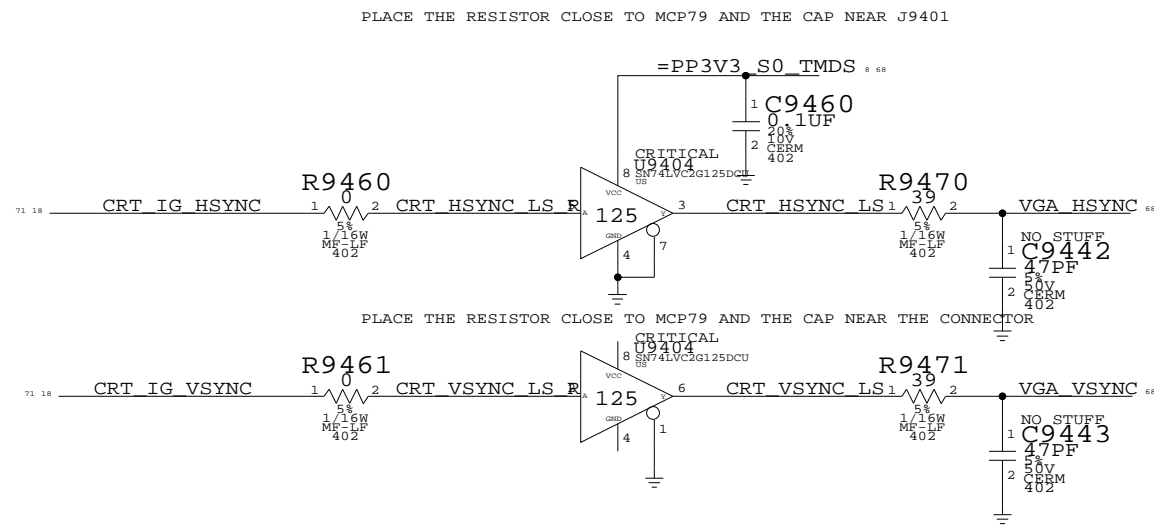
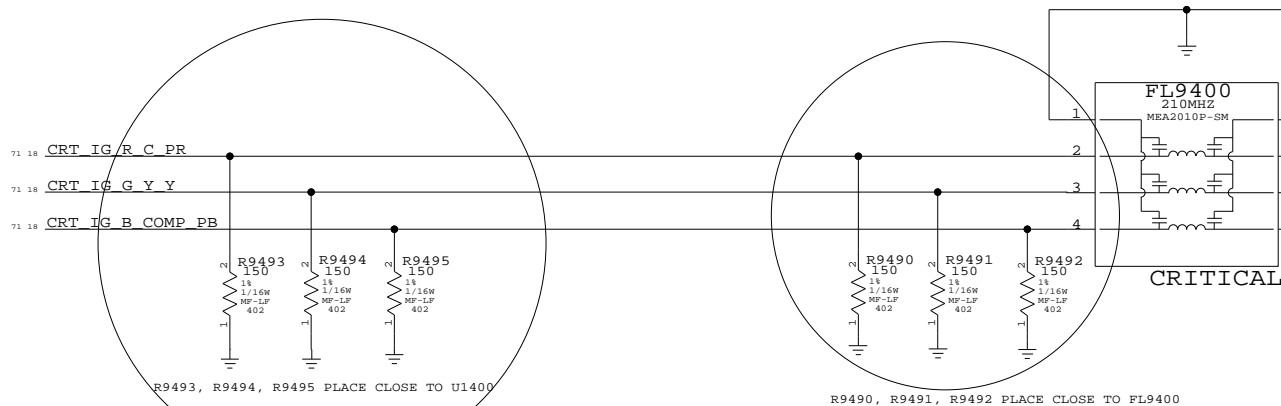
TMDS(MINI DVI) INTERFACE



DVI power DIODE on page 95 (D9500)



for VG signal trace, we need follow NV's recommendation. So we need change the segment impedance base on NV design guide.  
for A segment: 37.5 ohm from MCP to 150 ohm PD res. inner layer width is 0.18 mm  
for B segment: 50 ohm B/W 2 150 PF res. inner layer width is 0.09 mm top/bottom layer width is 0.115 mm  
for C segment: 75 ohm from FL to connector, top/bottom layer width is 0.076 mm.



MINI-DVI CONNECTOR

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SCALE	SHT	OF
NONE	94	109

D

D

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?	FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?	FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?	FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	*	=2x_DIELECTRIC	?	FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?	FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.  
Signals within each 4x group should be matched within 5 ps of strobe.  
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.  
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.  
DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.  
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.  
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.  
Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.  
Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2  
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?	CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_8MIL	*	8 MIL	?				
CPU_COMP	*	25 MIL	?				
CPU_GTLREF	*	25 MIL	?				
CPU_ITP	*	=2:1_SPACING	?				
CPU_VCCSENSE	*	25 MIL	?				

Most CPU signals with impedance requirements are 55-ohm single-ended.  
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2  
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?	CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2.5

A

A

CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB D L<15..0>	10 14
FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB DINV L<0>	10 14
FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<0>	10 14
FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<0>	10 14
FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB D L<31..16>	10 14
FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB DINV L<1>	10 14
FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<1>	10 14
FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<1>	10 14
FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB D L<47..32>	10 14
FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB DINV L<2>	10 14
FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<2>	10 14
FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<2>	10 14
FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB D L<63..48>	10 14
FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB DINV L<3>	10 14
FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<3>	10 14
FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<3>	10 14
FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB A L<16..3>	10 14
FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB REQ L<4..0>	10 14
FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB ADSTB L<0>	10 14
FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB A L<35..17>	10 14
FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB ADSTB L<1>	10 14
FSB_1X	FSB_50S	FSB_1X	FSB ADS L	10 14
FSB_BREQ0_1	FSB_50S	FSB_1X	FSB BREQ0 L	10 14
FSB_BREQ1_1	FSB_50S	FSB_1X	FSB BREQ1 L	14
FSB_1X	FSB_50S	FSB_1X	FSB BNR L	10 14
FSB_1X	FSB_50S	FSB_1X	FSB BPRI L	10 14
FSB_1X	FSB_50S	FSB_1X	FSB DBSY L	10 14
FSB_1X	FSB_50S	FSB_1X	FSB DEFER L	10 14
FSB_1X	FSB_50S	FSB_1X	FSB DRDY L	10 14
FSB_1X	FSB_50S	FSB_1X	FSB HIT L	10 14
FSB_1X	FSB_50S	FSB_1X	FSB HITM L	10 14
FSB_1X	FSB_50S	FSB_1X	FSB LOCK L	10 14
FSB_CPURST_L	FSB_50S	FSB_1X	FSB CPURST L	10 13 14
FSB_1X	FSB_50S	FSB_1X	FSB RS L<2..0>	10 14
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L	10 14
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU A20M L	10 14
CPU_BSEL	CPU_50S	CPU_AGTL	CPU BSEL<2..0>	9 10
CPU_FERR_L	CPU_50S	CPU_SMIL	CPU FERR L	10 14
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU IGNNL	10 14
CPU_INIT_L	CPU_50S	CPU_AGTL	CPU INIT L	10 14
CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU INTR	10 14
CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU NMI	10 14
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU PROCHOT L	10 14 42 60
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU PWRGD	10 13 14
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU SMI L	10 14
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU STPCLK L	10 14
PM_THRMTRIP_L	CPU_50S	CPU_SMIL	PM THRMTRIP L	10 14 42
FSB_CPUSLP_L	CPU_50S	CPU_AGTL	FSB CPUSLP L	10 14
CPU_FERR_SR	CPU_50S	CPU_AGTL	CPU FERR L	10 14
CPU_DPRSTP_L	CPU_50S	CPU_AGTL	CPU DPRSTP L	10 14 60
CPU_ASYNC	CPU_50S	CPU_AGTL	FSB DPWR L	10 14
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP VDD	14
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP GND	14
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP VCC	14
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP GND	14
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB CLK CPU P	10 14
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB CLK CPU N	10 14
FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB CLK ITP P	7 13 14
FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB CLK ITP N	7 13 14
FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB CLK MCP P	14
FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB CLK MCP N	14
CPU_FERR_1	CPU_50S		CPU IERR L	10
PM_DPRSILPVR	CPU_50S	CPU_AGTL	PM DPRSLPVR	21 60
(See above)	CPU_50S	CPU_AGTL	IMVP DPRSLPVR	60
CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU GTLREF	10 27
CPU_COMP	CPU_50S	CPU_COMP	CPU COMP<3>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<2>	10
CPU_COMP	CPU_50S	CPU_COMP	CPU COMP<1>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<0>	10
XDP_TDI	CPU_50S	CPU_ITP	XDP TDI	6 7 10 13
XDP_TDO	CPU_50S	CPU_ITP	XDP TDO	6 10
XDP_TMS	CPU_50S	CPU_ITP	XDP TMS	6 7 10 13
XDP_TCK	CPU_50S	CPU_ITP	XDP TCK	6 7 10 13
XDP_TRST_L	CPU_50S	CPU_ITP	XDP TRST L	6 7 10 13
XDP_BPM_1	CPU_50S	CPU_ITP	XDP BPM L<4..0>	7 10 13
XDP_BPM_15	CPU_50S	CPU_ITP	XDP BPM L<5>	7 10 13
(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP CPURST L	7 13
	CPU_50S	CPU_SMIL	CPU VID<6..0>	11 60
	CPU_50S	CPU_SMIL	IMVP6 VID<6..0>	11 60
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE P	11 60
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE N	11 60
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN P	
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN N	

FSB 4X Signal Groups

FSB 2X Signals

FSB 1X Signals

CPU/FSB Constraints

SYNC\_MASTER=K36B\_MLB SYNC\_DATE=08/17/2008

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SIZE

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051-8089

REV.

02

SCALE

NONE

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OF

109

87654321

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM\_\*-style wildcards!

DDR2:

DQ signals should be matched within 20 ps of associated DQS pair.

DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.

All DQS pairs should be matched within 100 ps of clocks.

CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.

A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.

All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).

DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:

DQ signals should be matched within 5 ps of associated DQS pair.

DQS intra-pair matching should be within 1 ps, inter-pair matching should be within 180 ps

No DQS to clock matching requirement.

CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.

A/BA/cmd signals should be matched within 5 ps of CLK pairs.

All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).

DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.3

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	7 MIL	7 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM A CLK P<5..0>	15 28
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM A CLK N<5..0>	15 28
MEM_A_CTRL	MEM_40S_VDD	MEM_CTRL	MEM A CKE<3..0>	15 28 30
MEM_A_CTRL	MEM_40S_VDD	MEM_CTRL	MEM A CS L<3..0>	15 28 30
MEM_A_CTRL	MEM_40S_VDD	MEM_CTRL	MEM A ODT<3..0>	15 28 30
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A A<14..0>	15 28 30
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A BA<2..0>	15 28 30
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A RAS L	15 28 30
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A CAS L	15 28 30
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A WE L	15 28 30
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM A DQ<7..0>	15 28
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM A DQ<15..8>	15 28
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM A DQ<23..16>	15 28
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM A DQ<31..24>	15 28
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM A DQ<39..32>	15 28
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM A DQ<47..40>	15 28
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM A DQ<55..48>	15 28
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM A DQ<63..56>	15 28
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM A DM<0>	15 28
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM A DM<1>	15 28
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM A DM<2>	15 28
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM A DM<3>	15 28
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM A DM<4>	15 28
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM A DM<5>	15 28
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM A DM<6>	15 28
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM A DM<7>	15 28
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM A DQS P<0>	15 28
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM A DQS N<0>	15 28
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM A DQS P<1>	15 28
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM A DQS N<1>	15 28
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM A DQS P<2>	15 28
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM A DQS N<2>	15 28
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM A DQS P<3>	15 28
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM A DQS N<3>	15 28
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM A DQS P<4>	15 28
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM A DQS N<4>	15 28
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM A DQS P<5>	15 28
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM A DQS N<5>	15 28
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM A DQS P<6>	15 28
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM A DQS N<6>	15 28
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM A DQS P<7>	15 28
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM A DQS N<7>	15 28
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM B CLK P<5..0>	15 29
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM B CLK N<5..0>	15 29
MEM_B_CTRL	MEM_40S_VDD	MEM_CTRL	MEM B CKE<3..0>	15 29 30
MEM_B_CTRL	MEM_40S_VDD	MEM_CTRL	MEM B CS L<3..0>	15 29 30
MEM_B_CTRL	MEM_40S_VDD	MEM_CTRL	MEM B ODT<3..0>	15 29 30
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B A<14..0>	15 29 30
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B BA<2..0>	15 29 30
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B RAS L	15 29 30
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B CAS L	15 29 30
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B WE L	15 29 30
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM B DQ<7..0>	15 29
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM B DQ<15..8>	15 29
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM B DQ<23..16>	15 29
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM B DQ<31..24>	15 29
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM B DQ<39..32>	15 29
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM B DQ<47..40>	15 29
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM B DQ<55..48>	15 29
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM B DQ<63..56>	15 29
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM B DM<0>	15 29
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM B DM<1>	15 29
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM B DM<2>	15 29
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM B DM<3>	15 29
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM B DM<4>	15 29
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM B DM<5>	15 29
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM B DM<6>	15 29
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM B DM<7>	15 29
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM B DQS P<0>	15 29
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM B DQS N<0>	15 29
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM B DQS P<1>	15 29
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM B DQS N<1>	15 29
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM B DQS P<2>	15 29
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM B DQS N<2>	15 29
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM B DQS P<3>	15 29
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM B DQS N<3>	15 29
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM B DQS P<4>	15 29
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM B DQS N<4>	15 29
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM B DQS P<5>	15 29
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM B DQS N<5>	15 29
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM B DQS P<6>	15 29
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM B DQS N<6>	15 29
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM B DQS P<7>	15 29
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM B DQS N<7>	15 29
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP_VDD	16
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP_GND	16

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Memory Constraints

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MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001\_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001\_v01), Section 2.7.4

ELECTRICAL_CONSTRAINT_SET	NET_TYPE	
	PHYSICAL	SPACING
MCP_MII_COMP	MCP_MII_COMP	
MCP_MII_COMP	MCP_MII_COMP	
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK
ENET_INTR_L	ENET_MII_55S	ENET_MII
ENET_MDIO	ENET_MII_55S	ENET_MII
ENET_MDC	ENET_MII_55S	ENET_MII
ENET_PWRDWN_L	ENET_MII_55S	ENET_MII
ENET_RXCLK	ENET_MII_55S	ENET_MII
ENET_RXCLK	ENET_MII_55S	ENET_MII
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII
ENET_RXD	ENET_MII_55S	ENET_MII
ENET_TXCLK	ENET_MII_55S	ENET_MII
ENET_TXCLK	ENET_MII_55S	ENET_MII
ENET_TXD0	ENET_MII_55S	ENET_MII
ENET_TXD	ENET_MII_55S	ENET_MII
ENET_TXD	ENET_MII_55S	ENET_MII
ENET_RESET_L	ENET_MII_55S	ENET_MII
ENET_MDI	ENET_MDI_100D	ENET_MDI
ENET_MDI_100D	ENET_MDI_100D	ENET_MDI

Ethernet Constraints

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











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FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
 FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_P	35 37
 FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_N	35 37
 FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_P	35 37
 FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_N	35 37
 FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_P	35 37
 FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_N	35 37
 FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_P	35 37
 FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_N	35 37
 FW_P1_TPA	FW_110D	FW_TP	FW_PORT_A_P	37
 FW_P1_TPA	FW_110D	FW_TP	FW_PORT_A_N	37
 FW_P1_TPB	FW_110D	FW_TP	FW_PORT_B_P	37
 FW_P1_TPB	FW_110D	FW_TP	FW_PORT_B_N	37
Port 2 Not Used				

FireWire Constraints

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








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

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PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
1Tol_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties		
ELECTRICAL_CONSTRAINT_SET	NET_TYPE	
	PHYSICAL	SPACING
 SMBUS_SMC_A_S3_SCL	SMB_55G	SMB
 SMBUS_SMC_A_S3_SDA	SMB_55G	SMB
 SMBUS_SMC_B_S0_SCL	SMB_55G	SMB
 SMBUS_SMC_B_S0_SDA	SMB_55G	SMB
 SMBUS_SMC_0_S0_SCL	SMB_55G	SMB
 SMBUS_SMC_0_S0_SDA	SMB_55G	SMB
 SMBUS_SMC_BSA_SCL	SMB_55G	SMB
 SMBUS_SMC_BSA_SDA	SMB_55G	SMB
 SMBUS_SMC_MGMT_SCL	SMB_55G	SMB
 SMBUS_SMC_MGMT_SDA	SMB_55G	SMB

SMBus Charger Net Properties		
ELECTRICAL_CONSTRAINT_SET	NET_TYPE	
	PHYSICAL	SPACING
 CHGR_CSI_P	1Tol_DIFFPAIR	
 CHGR_CSI_N	1Tol_DIFFPAIR	
 CHGR_CSO_P	1Tol_DIFFPAIR	
 CHGR_CSO_N	1Tol_DIFFPAIR	

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SMC Constraints

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CBADCBA

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_FSB	*	BGA_P1MM	BGA_P2MM
CLK_LPC	*	BGA_P1MM	BGA_P2MM
CLK_PCI	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P2MM
CLK_SLOW	*	BGA_P1MM	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA_P1MM	BGA_P3MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	TOP,BOTTOM	0.140 MM	?
3X_DIELECTRIC	TOP,BOTTOM	0.210 MM	?
4X_DIELECTRIC	TOP,BOTTOM	0.280 MM	?
5X_DIELECTRIC	TOP,BOTTOM	0.350 MM	?
2X_DIELECTRIC	-	0.152 MM	?
3X_DIELECTRIC	-	0.228 MM	?
4X_DIELECTRIC	-	0.304 MM	?
5X_DIELECTRIC	-	0.380 MM	?



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