

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

M42B MLB NO_LDO SCHEMATIC

3/22/2007

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
07		355269	ENGINEERING RELEASED	12/10/04	?

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16	16	NB Power 1	DK	NB	07/25/2005
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31	31	Memory Vtt Supply	LT	(MASTER)	(MASTER)
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37	37	ETHERNET CONNECTOR	ES	ENET	11/14/2005
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39	39	FIREWIRE PORT	ES	ENET	11/16/2005
40	40	CONNECTOR MISC	ES	ENET	11/16/2005
41	41	IR CONTROLLER	ES	ENET	11/09/2005
42	42		ES	ENET	11/01/2005
43	43		ES	ENET	08/19/2005
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45	45	SMC	MK	SMC	08/18/2005
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50	50	SPI BOOTROM	ES	MASTER	5/23/05
51	51	Fan	MK	ENET	11/10/2005
52	52	SMS	RX	SMC	08/23/2005
53	53	TPM	DK	SMC	07/18/2005
54	54	AUDIO: CODEC	DK	M42AUDIO	08/05/2006
55	55	AUDIO: SPEAKER AMP	DK	M42AUDIO	08/05/2006
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59	59	5V / 3.3V Power Supply	MK	POWER	07/13/2005
60	60	2.5V/1.2V Regulator	MK	ENET	12/06/2005
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62	62	1.5V / 1.05V Power Supply	MK	POWER	07/13/2005
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64	64	Power Conn / Alias	MK	ENET	11/16/2005
65	65	DC-In & Battery Connectors	MK	POWER	07/13/2005
66	66	PBUS Supply/Battery Charger	ES	SMC	08/19/2005
67	67	INVERTER,LVDS,TMDS	DK	GRAPHIC	06/06/2005
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69	69	MINI-DVI CONNECTOR		EUGENE	05/21/05
70	70	Cross Reference Page			
71	71	Cross Reference Page			
72	72	Cross Reference Page			
73	73	Cross Reference Page			
74	74	Cross Reference Page			
75	75	Cross Reference Page			
76	76	Cross Reference Page			
77	77	Cross Reference Page			
78	78	Cross Reference Page			
79	79	Cross Reference Page			



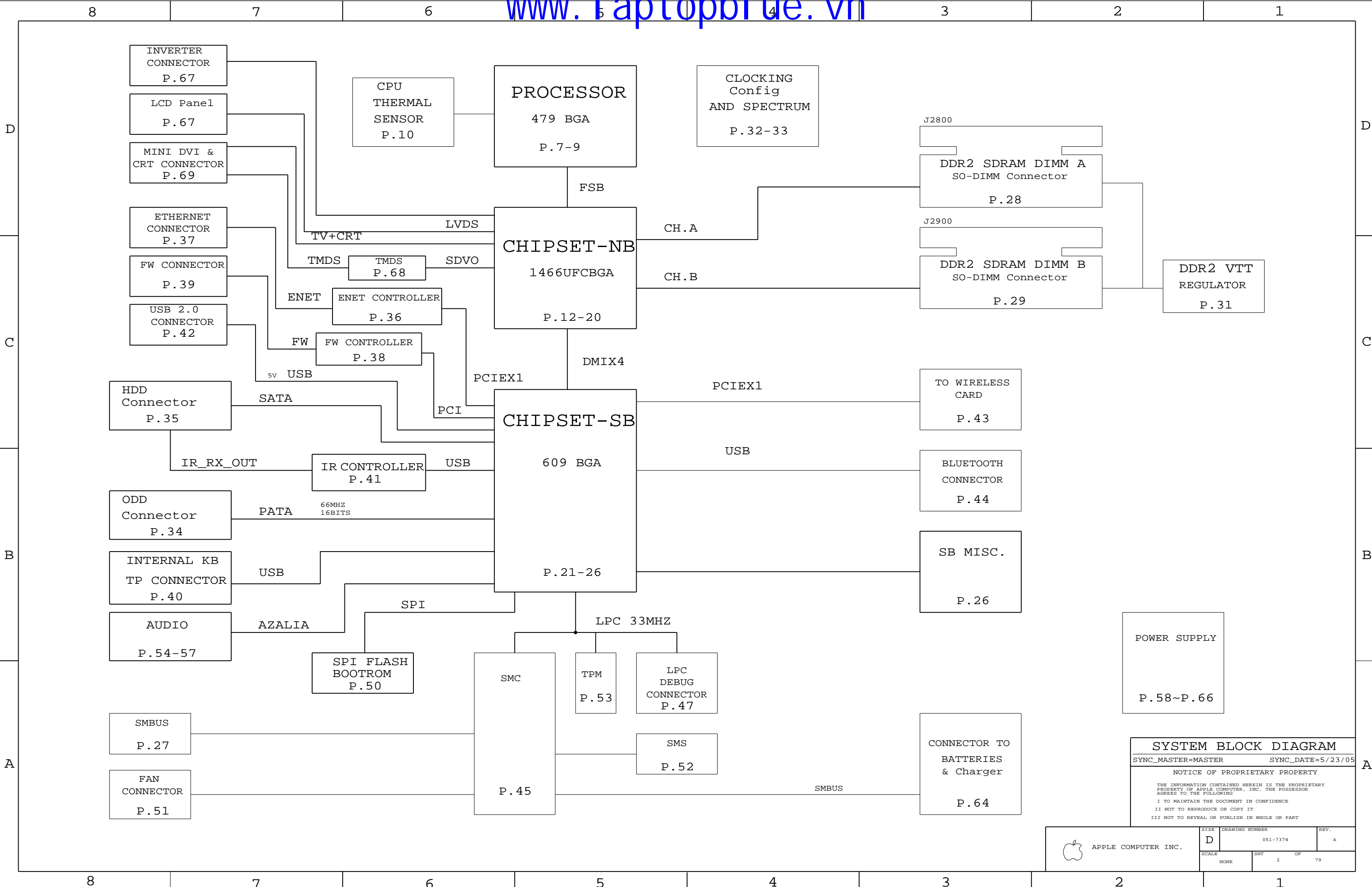
EE DRIS:

RX-RAYMOND XU
DK-DINESH KUMAR
RC-RAY CHANG
MK-MARC KLINGELHOFFER
LT-LAWRENCE TAN
LD-LINDA DUNN

Schematic / PCB #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-7374	1	SCHEM,M42B,MLB NO_LDO	SCH	
820-1889	1	PCBF,M42,MLB NO_LDO	PCB	

DIMENSIONS ARE IN MILLIMETERS XX ± _____ X.XX ± _____ X.XXX ± _____ ANGLES ± _____ DO NOT SCALE DRAWING THIRD ANGLE PROJECTION	METRIC		Apple Computer Inc.				
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	ENG APPD	MFG APPD					
	QA APPD	DESIGNER					
RELEASE	SCALE	TITLE					
	NONE	SCHEM,MLB NO_LDO,M42B					
MATERIAL/FINISH NOTED AS APPLICABLE		SIZE	D	DRAWING NUMBER	051-7374	REV.	A
				SHT 1 OF 79			



SYSTEM BLOCK DIAGRAM

SYNC_MASTER=MASTER

SYNC_DATE=5/23/05

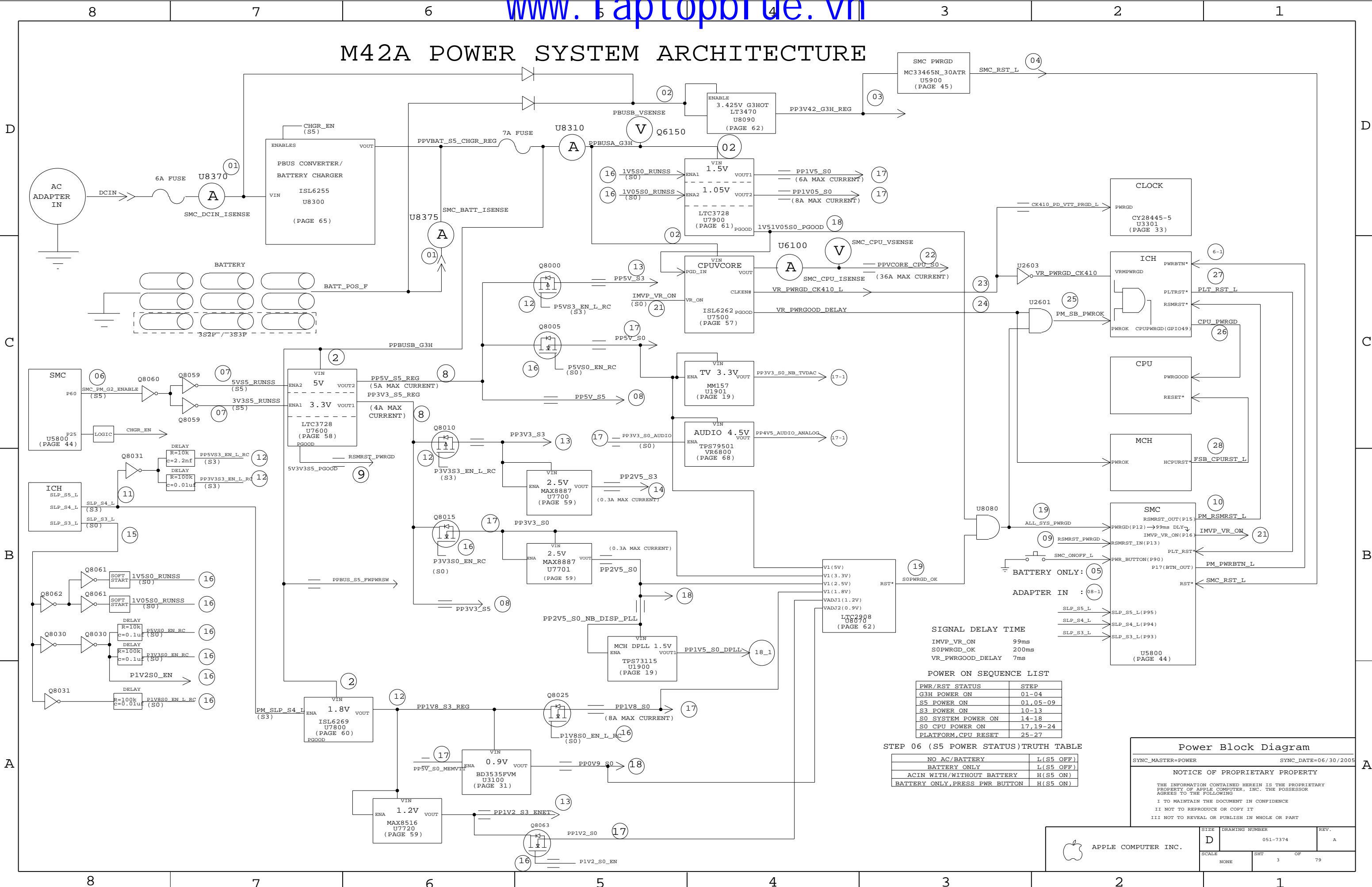
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Page Notes

Power aliases required by this page: (NONE)
Signal aliases required by this page: (NONE)
BOM options provided by this page: (NONE)



BOM OPTION

BOMOPTION	M42A GOOD ST MICRO 630-7795 EVT	M42A BETTER ST MICRO 630-7796 EVT	M42A BEST KIONIX 630-7799 EVT	M42A GOOD KIONIX 630-7798 EVT	M42A BETTER KIONIX 630-7736 EVT	M42A BEST ST MICRO 630-7797 EVT
1V51V05S0_CONT						
1V51V05S0_SKIP	V	V	V	V	V	V
5V3V3S3_CONT						
5V3V3S3_SKIP	V	V	V	V	V	V
ACCEL_KIONIX			V	V	V	
ACCEL_ST	V	V				V
INVERTER_BUF	V	V	V	V	V	V
INVERTER_UNBUF						
ITP						
LEMENU	V	V	V	V	V	V
MEMVIT_EN_PU	V	V	V	V	V	V
NBCFG_DMI_REVERSE						
NBCFG_DMI_X2						
NBCFG_DYN_ODT_DISABLE						
NBCFG_PEG_REVERSE						
NBCFG_SDVO_AND_PCIE						
NBCFG_VCC_1V5						
NO_REBOOT_MODE						
USB_C_OC_PU	V	V	V	V	V	V
USB_D_OC_PU	V	V	V	V	V	V
USB_E_OC_PU	V	V	V	V	V	V
GOOD	V			V		
BETTER		V			V	
BEST			V			V
M42A_PGM	V	V	V	V	V	V
ONEWIRE_PULLUP	V	V	V	V	V	V
ONEWIRE_PULLUP_OLD						
ONEWIRE_PU_PROT	V	V	V	V	V	V
ONEWIRE_PU_ACOK						
ONEWIRE_PWRCTL	V	V	V	V	V	V
ONEWIRE_ALWAYSON						
3V3_IND_2MM8	V	V	V	V	V	V
3V3_IND_3MM						
NORMAL	V	V		V	V	
FANCY			V			V
STANDOFF	V	V	V	V	V	V
FET_FDN6296	V	V	V	V	V	V
FET_STL8NH3LL						
GOOD-ST	V					
BETTER-ST		V				
BEST-KIONIX			V			
GOOD-KIONIX				V		
BETTER-KIONIX					V	
BEST-ST						V
TPM						
PVT-DIMM						
POST-RAMP-DIMM35	V	V	V	V	V	V
M42						
M42A	V	V	V	V	V	V

Top	SIGNAL
2	GROUND
3	SIGNAL(High Speed)
4	SIGNAL(High Speed)
5	GROUND
6	POWER
7	POWER
8	GROUND
9	SIGNAL(High Speed)
10	SIGNAL(High Speed)
11	GROUND
BOTTOM	SIGNAL

LAYER	THICKNESS (MM)	TRACE WIDTH (MM)
CONFORMAL_COAT	0.018	
L1 SIGNAL(TOP)	0.047	0.1
L1-L2	0.07	
L2 GROUND	0.014	---
L2-L3	0.076	
L3 SIGNAL	0.014	0.079
L3-L4	0.156	
L4 SIGNAL	0.014	0.079
L4-L5	0.076	
L5 GND	0.014	---
L5-L6	0.07	
L6 POWER	0.031	---
L6-L7	0.076	
L7 POWER	0.031	---
L7-L8	0.07	
L8 GROUND	0.014	---
L8-L9	0.076	
L9 SIGNAL	0.014	0.1
L9-L10	0.156	
L10 SIGNAL	0.014	0.1
L10-L11	0.076	
L11 GROUND	0.014	0.1
L11-L12	0.07	
L12 SIGNAL(BOTTOM)	0.047	0.1
CONFORMAL_COAT	0.018	
TOTAL	1.276	---

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
337S3450	1	IC, MEMOM, CPU L2 1.83GHZ, 479 PGA	U0700	GOOD
337S3389	1	IC, MEMOM, CPU 2.00GHZ, 479 PGA	U0700	BETTER
337S3391	1	IC, MEMOM, CPU 2.16GHZ, 479 PGA	U0700	BEST

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
338S0268	1	IC, FW32306, 1394A LINK, BGA, 129P	U4400	LEMENU
338S0270	1	IC, 88E8053, GIGABIT ENET XCVR, 64P QFN, NO	U4101	LEMENU
359S0109	1	IC, SIOB1P436, CLOCK GEN, 68PIN QFN	U3301	LEMENU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S2131	1	IC, 16MBIT 8-PIN SPI SERIAL FLASH, S08P8	U6301	M42A_PGM
341S1797	1	IC, EEPROM, SERIAL IIC, 8KBIT, S08	U4102	M42A_PGM
341S2133	1	IC, SMC, 176P BGA, H58/2116	U5800	M42A_PGM
341S1890	1	IC, PSOC-M/USB, 56P, MLP, CY8C24794	U5100	M42A_PGM

341S2132 FOR M42B LOCKED BOOTROM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
826-4393	1	LBL, P/N LABEL, PCB, 28MMX6MM	EEE:YCT	CRITICAL	BEST-KIONIX
826-4393	1	LBL, P/N LABEL, PCB, 28MMX6MM	EEE:YCS	CRITICAL	BETTER-KIONIX
826-4393	1	LBL, P/N LABEL, PCB, 28MMX6MM	EEE:YCR	CRITICAL	GOOD-KIONIX

CONFIGURATION OPTIONS

SYNC_MASTER=SMC SYNC_DATE=07/18/2005

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SIZE	DRAWING NUMBER	REV.
D	051-7374	A
SCALE	SHT	OF
NONE	4	79

Functional Test Points

Power Supply NO_TESTS

NO_TEST		
IMVP6_RBIAS	58A4	58B7
IMVP6_COMP	58A4	58B7
5VS5_RUNSS	5984	63C7
1V5S0_RUNSS	62B5	63B7
1V8S3_COMP	61B6	
1V8S3_FSET	61C5	
TRUE 3V3S5_COMP		
TRUE 3V3S5_FSET		
TRUE 1V05S0_COMP		
TRUE 1V05S0_FSET		
TRUE P3V42G3H_FB	63D2	

CLOCK NO_TESTS

NO_TEST		
TRUE CK410_CPU0_N	32C4	33D5
TRUE CK410_CPU0_P	32C4	33D5
TRUE CK410_CPU1_N	32C4	33D5
TRUE CK410_CPU1_P	32C4	33D5
TRUE CK410_CPU2_ITP_SRC10_N	32C4	33D5
TRUE CK410_CPU2_ITP_SRC10_P	32C4	33D5
TRUE CK410_DOT96_27M_N	32A4	33B5
TRUE CK410_DOT96_27M_P	32A4	33B5
TRUE CK410_LVDS_N	32B4	33A5
TRUE CK410_LVDS_P	32B4	33A5
TRUE CK410_PCI4_CLK_SPN		
TRUE CK410_PCI4_CLK	32B6	33D8
TRUE CK410_SRC1_N_SPN	6B3	
TRUE CK410_SRC1_P_SPN	6B3	
TRUE CK410_SRC2_N	32B4	33C5
TRUE CK410_SRC2_P	32B4	33C5
TRUE CK410_SRC3_N_SPN	6B3	
TRUE CK410_SRC3_P_SPN	6B3	
TRUE CK410_SRC4_N	32B4	33B5
TRUE CK410_SRC4_P	32B4	33B5
TRUE CK410_SRC5_N	32B4	33C5
TRUE CK410_SRC5_P	32B4	33C5
TRUE CK410_SRC6_N	32B4	33C5
TRUE CK410_SRC6_P	32B4	33D5
TRUE CK410_SRC7_N_SPN	6B3	
TRUE CK410_SRC7_P_SPN	6B3	
TRUE CK410_SRC8_N	32A4	33C5
TRUE CK410_SRC8_P	32A4	33C5
TRUE CK410_SRC_CLKREQ01_L_SPN	6B3	
TRUE CK410_SRC_CLKREQ03_L_SPN	6B3	
TRUE CK410_SRC_CLKREQ08_L	32A4	33A5

FIREWARE NO_TESTS

NO_TEST		
TRUE FW_B_TPA_N_SPN	6D1	
TRUE FW_B_TPA_P_SPN	6D1	
TRUE FW_B_TPBIAS_SPN	6D1	
TRUE FW_B_TPB_N_SPN	6D1	
TRUE FW_B_TPB_P_SPN	6D1	
TRUE FW_C_TPA_N_SPN	6D1	
TRUE FW_C_TPA_P_SPN	6D1	
TRUE FW_C_TPBIAS_SPN	6D1	
TRUE FW_C_TPB_N_SPN	6D1	
TRUE FW_C_TPB_P_SPN	6D1	

LVDS NO_TESTS

NO_TEST		
TRUE LVDS_B_CLK_N_SPN	6D5	
TRUE LVDS_B_CLK_P_SPN	6D5	
TRUE LVDS_B_DATA_N0_SPN	6D5	
TRUE LVDS_B_DATA_N1_SPN	6D5	
TRUE LVDS_B_DATA_N2_SPN	6D5	
TRUE LVDS_B_DATA_P1_SPN	6D5	
TRUE LVDS_B_DATA_P2_SPN	6D5	

ETHERNET NO_TESTS

NO_TEST		
TRUE ENET_MDI_TRAN_P<2>	37B5	
TRUE ENET_MDI_TRAN_N<2>	37B5	
TRUE ENET_MDI_TRAN_P<3>	37B5	

NO_TEST		
TRUE SMC_FAN_3_TACH	45B8	46C3
TRUE ALS_LEFT	45A8	46C3

Fan Connectors

FUNC_TEST		
TRUE =PP5V_S0_FAN_RT	51C4	64D3
TRUE FAN_RT_PWM	51B3	
TRUE FAN_RT_TACH	51C3	
TRUE =PP3V3_S0_FAN_RT	51C4	64A6
TRUE SMC_FAN_1_CTL	45B8	51B4
TRUE SMC_FAN_1_TACH	45B8	51C4

LPC+ Debug Connector

FUNC_TEST		
TRUE =PP3V42_G3H_LPCPLUS	47C6	64D1
TRUE =PP5V_S0_LPCPLUS	47C6	64D3
TRUE LPC_AD<0>	31D4	45D8 47C5 53C6
TRUE LPC_AD<1>	31D4	45D8 47C5 53C6
TRUE LPC_FRAME_L	21C5	45C8 47C6 53C5
TRUE PM_CLKRUN_L	32C8	38A5 45D5 47C5
TRUE BOOT_LPC_SPI_L	32C5	45C8 47C6
TRUE SMC_TMS	45B5	46C6 47C6
TRUE DEBUG_RST_L	36B1	47C6
TRUE SMC_TRST_L	45C1	47C6
TRUE SMC_TDO	45C5	46C6 47B6
TRUE SMC_MD1	45C2	47B6
TRUE SMC_TX_L	45C8	46B2 46D6 47B5
TRUE FWH_INIT_L	5B2	21C4 47C5
TRUE PCI_CLK_PORT80_LPC	33D6	47C5
TRUE LPC_AD<2>	31D4	45D8 47C5 53C6
TRUE LPC_AD<3>	31D4	45D8 47C5 53C6
TRUE INT_SERIRQ	32C8	45C8 47C5 53C6
TRUE PM_SUS_STAT_L	32C5	45D5 46B3 47C5
TRUE SMC_TDI	45C5	46C6 47C5
TRUE SMC_TCK	45C5	46C6 47C5
TRUE SMC_RST_L	45C3	46D7 47C5
TRUE SMC_NMI	45C1	47B5
TRUE SMC_RX_L	45C8	46B2 46D6 47B5
TRUE SV_SET_UP	33B6	33C3 47B5

Other Func Test Points

FUNC_TEST		
TRUE =PP1V05_S0_REG	62B1	64D8

SMBus FUNC_TEST		
TRUE SMBUS_SMC_MLB_SCL	27C5	
TRUE SMBUS_SMC_MLB_SDA	27B5	

FIREWIRE FUNC_TEST

TRUE PPFW_SWITCH	39D4	
SLEEP LED FUNC_TEST		
TRUE SYS_LED_ANODE	35C5	46A3

SMC FUNC_TEST

TRUE SMC_LID	4D04	45B5 46C6 65A8
TRUE SMC_MANUAL_RST_L	46D8	
TRUE SMC_CPU_VSENSE	45D5	48B1

Power Supply FUNC_TEST

TRUE ALL_SYS_PWRGD	26A5	45D8 63B1
TRUE PPVCORE_CPU_S0	64D7	
TRUE PP1V05_S0	64D7	
TRUE PP1V5_S0	64C7	
TRUE PP1V8_S0	64C7	
TRUE PP2V5_S0	64B7	
TRUE PP3V3_S0	64B7	
TRUE PP5V_S0	64D4	
TRUE PP1V2_S3	64C4	
TRUE PP1V8_S3	64C4	
TRUE PP2V5_S3	64C4	
TRUE PP3V3_S3	64B4	
TRUE PP5V_S3	64B4	
TRUE PP3V3_S5	64A4	
TRUE PP5V_S5	64A4	
TRUE PP3V42_G3H	64D1	
TRUE PPBUS_A_G3H		
TRUE PPBUS_B_G3H	64C1	
TRUE PP18V5_G3H	64C1	
TRUE PP0V9_S0	64D7	

Battery Digital Connector

FUNC_TEST		
TRUE SMC_BS_ALRT_L	45C5	46C6 65A2
TRUE SMBUS_BATT_SCL_F	65B6	
TRUE SMBUS_BATT_SDA_F	65A6	
TRUE BATT_IN		
TRUE BATT_POS	65A6	
TRUE BATT_NEG	65A6	

Audio FUNC_TEST

TRUE PP5V_S0_AUDIO_PWR		
TRUE PP5V_S0_AUDIO		
TRUE GND_AUDIO_PWR	64B2	
TRUE GND_AUDIO_CODEC	64B2	
TRUE ACZ_SDATIN<0>	21C7	54D7
TRUE ACZ_SDATAOUT	21C7	54D7
TRUE ACZ_BITCLK	21C7	54D7
TRUE ACZ_RST_L	21C7	54C7 57C3
TRUE ACZ_SYNC	21C7	54D7

Battery FUNC_TEST

TRUE SMC_BATT_ISET	45B5	66B7
TRUE SMC_BATT_CHG_EN	45D8	46B6 66A4
TRUE SMC_BC_ACOK	45C5	46B6 65C3
TRUE SMC_PS_ON	39C6	45D5 46B3
TRUE SMC_BATT_TRICKLE_EN_L	45C8	46B6 66A3
TRUE SYS_ONEWIRE	45B8	46D6 65C8

USB FUNC_TEST

TRUE TP_USBP_E	6C2	
TRUE TP_USBN_E	6C2	
TRUE TP_USBP_F		
TRUE TP_USBN_F		

DC-JACK FUNC_TEST

TRUE ACIN_ENABLE_GATE	65C3	
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Battery charger FUNC_TEST

TRUE PPVBAT_G3H_CHGR_OUT	66B5	66C2
--------------------------	------	------

INVERTER CONNECTOR FUNC_TEST

TRUE PPBUS_ALL_INV_CONN	67D3	
TRUE INV_GND	67D2	
TRUE PP5V_INV_F	67D3	
TRUE INV_BKLIGHT_PWM_L	67D2	

FUNC TEST 1 OF 2

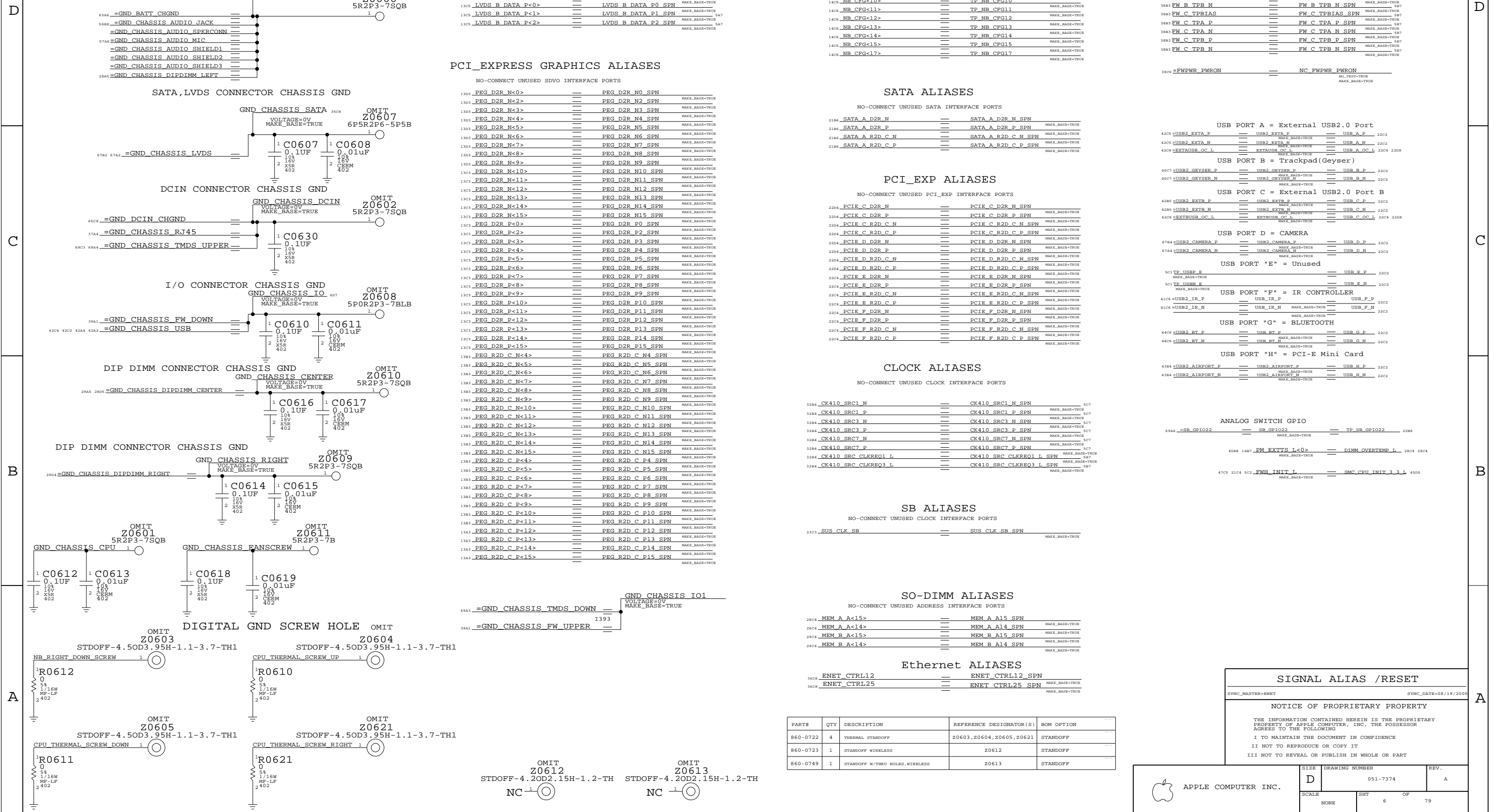
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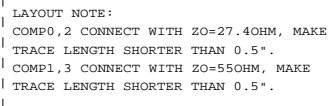
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SIZE	DRAWING NUMBER	REV.
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SCALE	SHT	OF
NONE	5	79

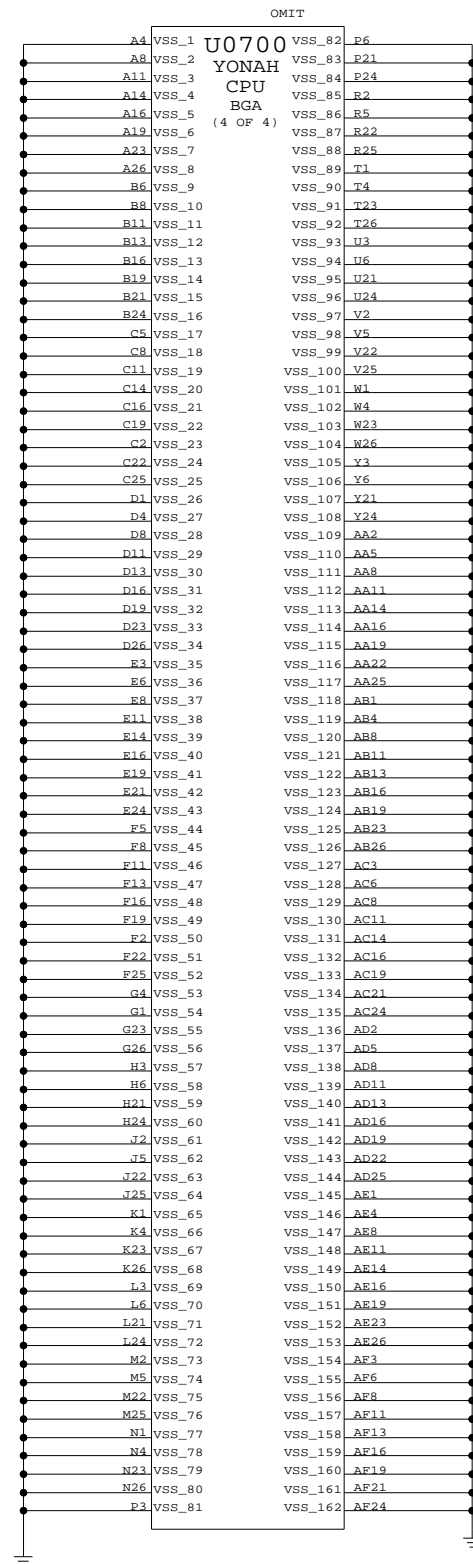
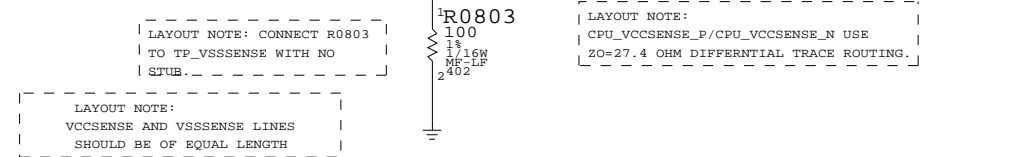




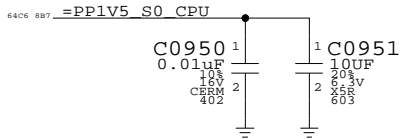
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CPU 1 OF 2-FSB
SYNC_MASTER=MASTER                                SYNC_DATE=05/03/2005
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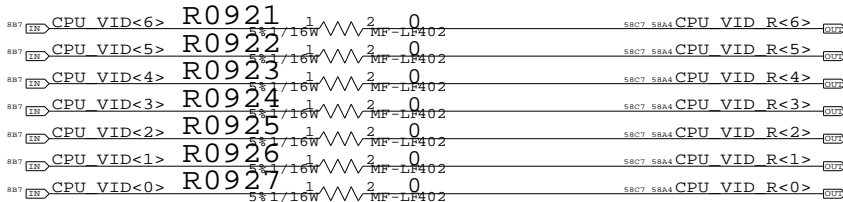


VCCA DECOUPLING
(CPU INTERNAL PLL POWER 1.5V)



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0603	138S0602	?	ALL	USE SAMSUNG AND MURATA ONLY
138S0606	138S0602	?	ALL	USE TAIYO

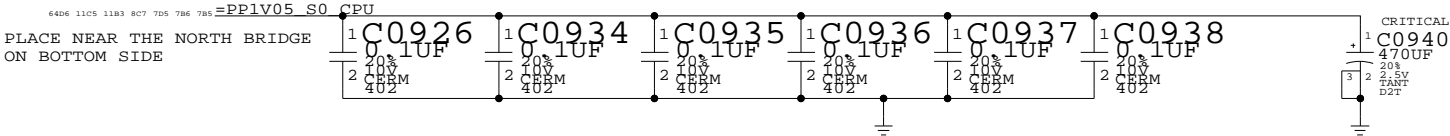
CPU CORE VID<> SETTINGS



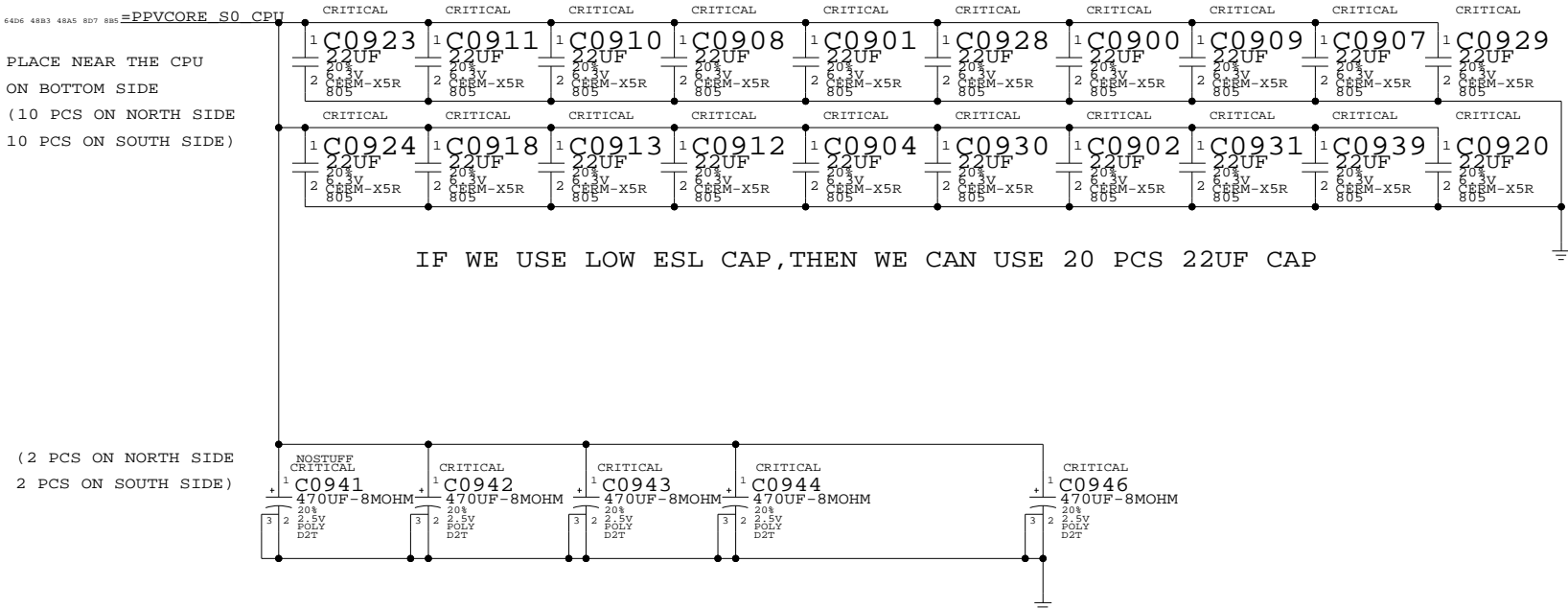
R0921~R0927 FOR CPU VOLTAGE MANUAL SETTING

VCCP CORE DECOUPLING
(CPU IO POWER 1.05V)

THIS 470UF FOR CPU,GMCH FSB BUS 1.05V



VCC CORE DECOUPLING
(CPU CORE POWER)



IF WE USE LOW ESL CAP,THEN WE CAN USE 20 PCS 22UF CAP

	MIN	TYP	MAX
DUAL CORE SV CPU	VCCHFM 1.1625		1.30
	VCCLFM	TBD	TBD
SINGLE CORE SV CPU	VCCHFM 1.1625		1.30
	VCCLFM	TBD	
DUAL CORE LV CPU	VCCHFM 1.0		1.1625
	VCCLFM	TBD	
ULV CPU	VCCHFM TBD		TBD
	VCCLFM	TBD	

UNIT: V

- # ALL PROCESSOR DEFAULT VCORE FOR INITIAL POWER UP IS 1.2V
TWO PROCESSORS AT THE SAME FREQUENCY MAY HAVE DIFFERENT SETTING WITH THE VID RANGE(VCORE VOLTAGE)!
REFER TO YONAH PROCESSOR EMTS REV 1.0
VCCHFM: VCORE AT HIGHEST FREQUENCY MODE
VCCLFM: VCORE AT LOWEST FREQUENCY MODE

CPU DECAPS & VID<>

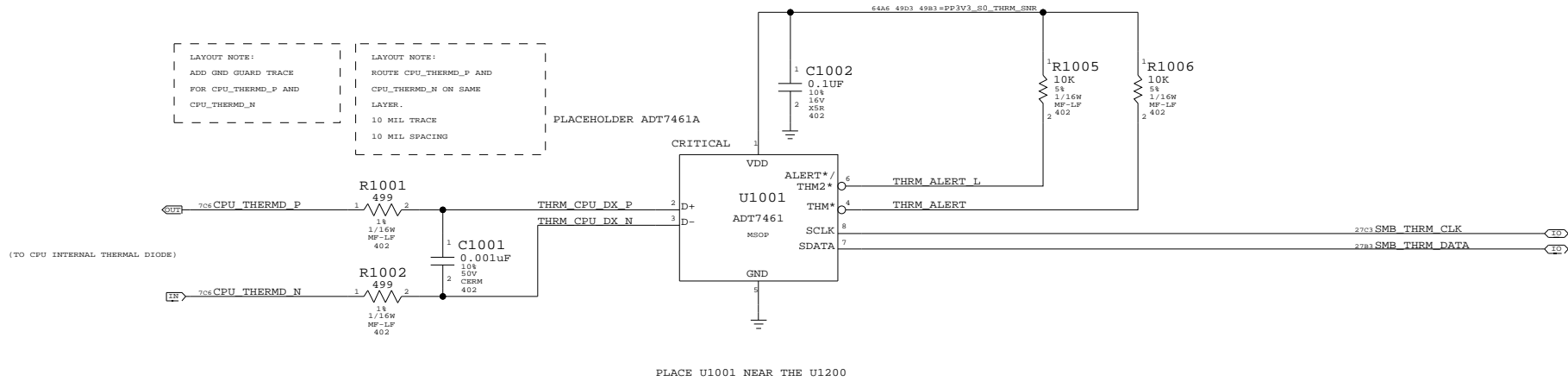
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SIZE	DRAWING NUMBER	REV.
D	051-7374	A
SCALE	SHT	OF
NONE	9	79

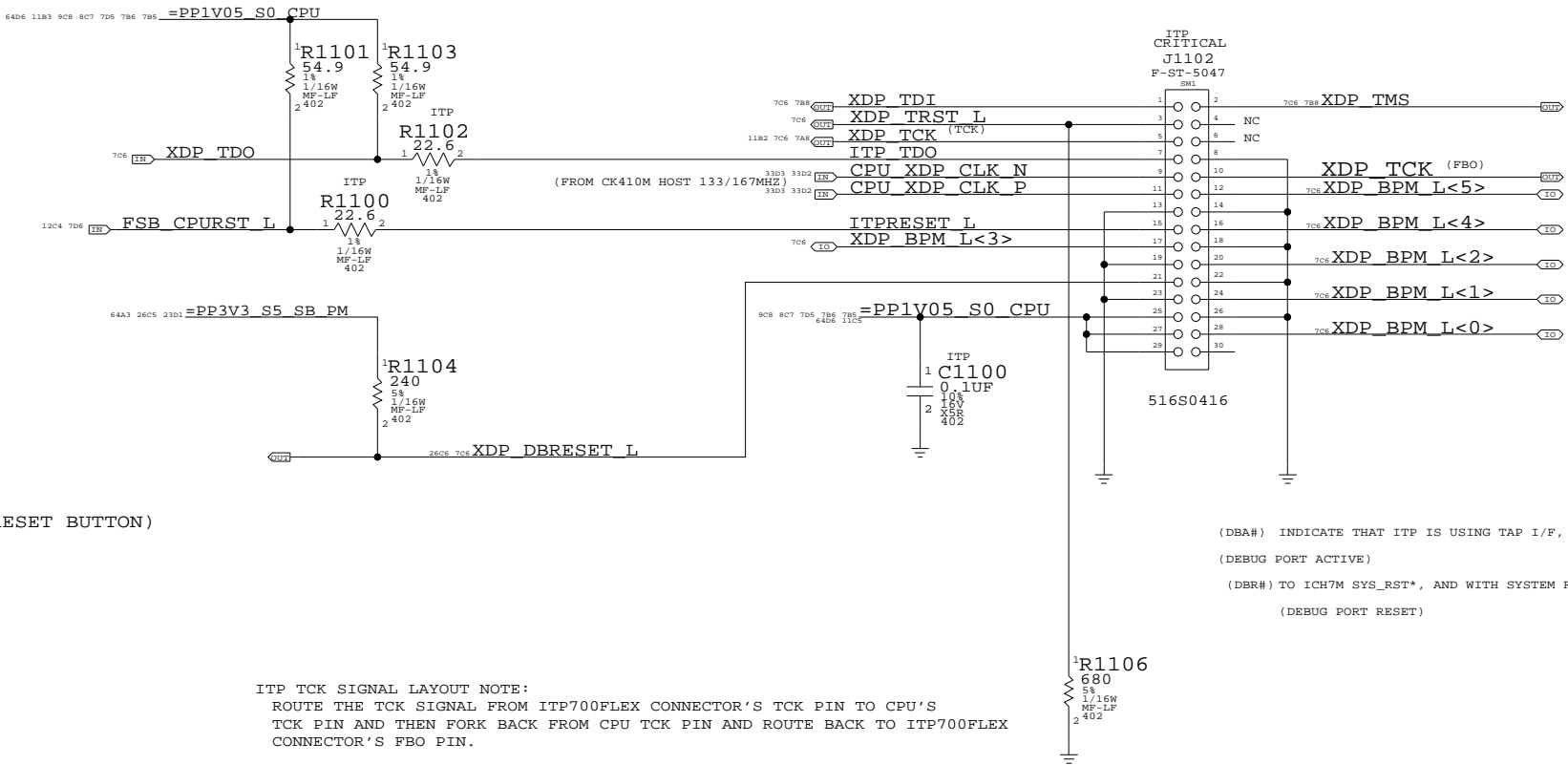
CPU ZONE THERMAL SENSOR



CPU MISC1-TEMP SENSOR		
SYNC_MASTER=ENET		SYNC_DATE=08/19/2005
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	SCALE NONE	SHT 10	OF 79

CPU ITP700FLEX DEBUG SUPPORT



(AND WITH RESET BUTTON)

(DBA#) INDICATE THAT ITP IS USING TAP I/F, NC IN 945GM CHIPSET SYSTEM.
(DEBUG PORT ACTIVE)
(DBR#) TO ICH7M SYS_RST*, AND WITH SYSTEM RESET LOGIC
(DEBUG PORT RESET)

ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S
TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX
CONNECTOR'S FBO PIN.



CPU ITP700FLEX DEBUG		
SYNC_MASTER=MASTER		SYNC_DATE=5/23/05
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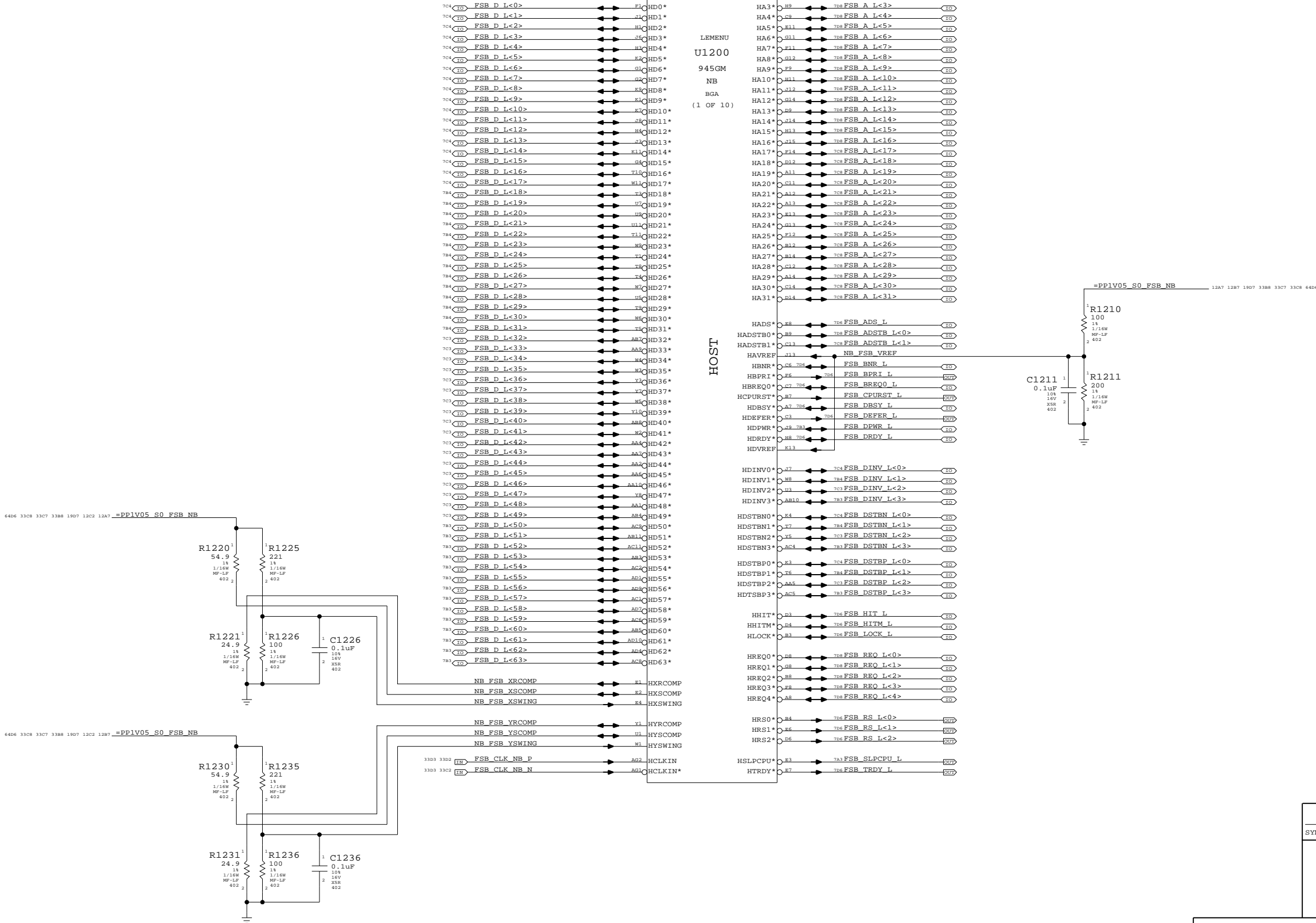
A

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NB CPU Interface

SYNC_MASTER=NB SYNC_DATE=07/25/2005

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B

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LVDS Disable

Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

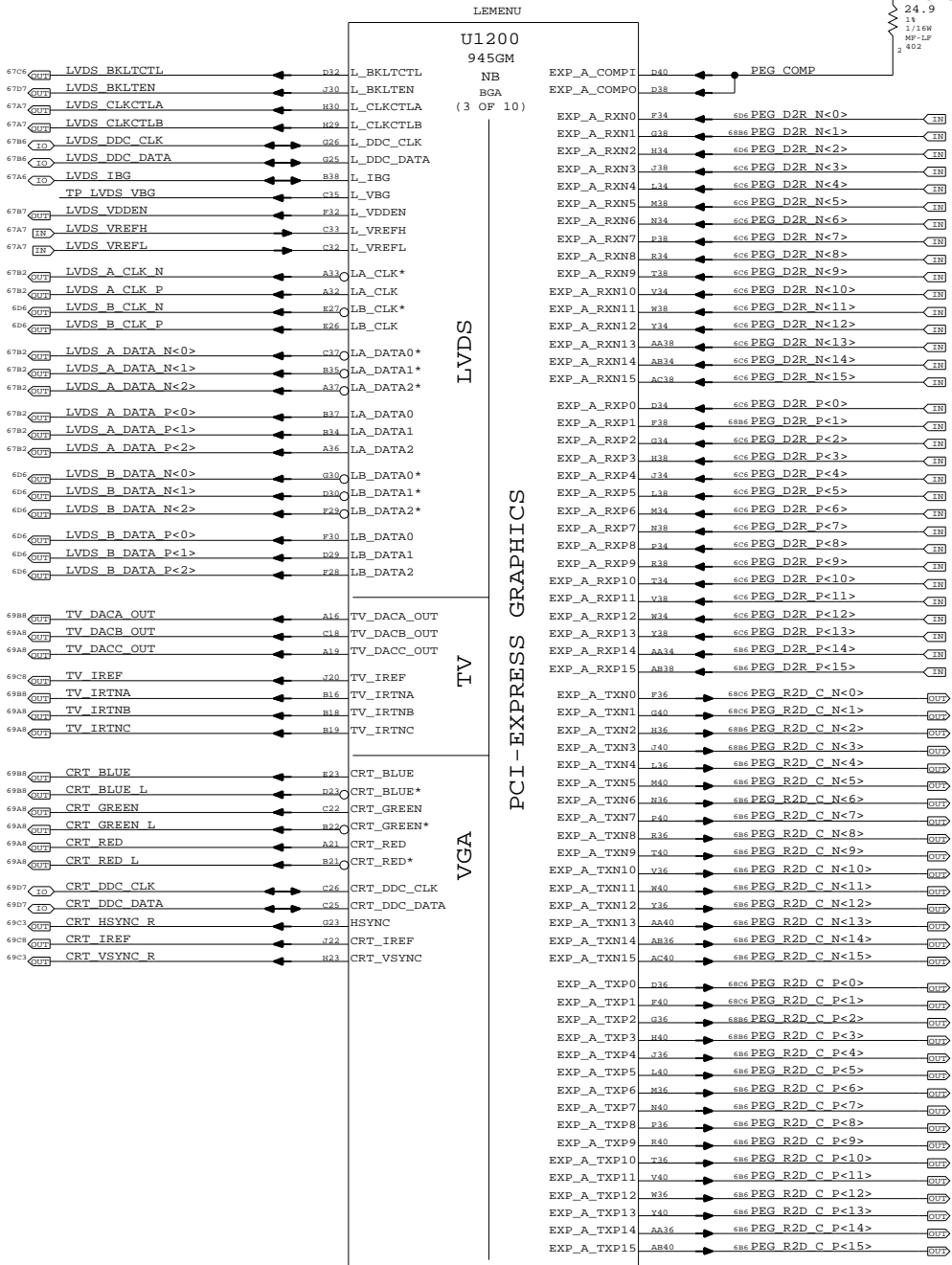
Unused DAC outputs must remain powered, but can omit
filtering components. Unused DAC outputs should
connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



SDVO Alternate Function

SDVO_TVCLKIN#
SDVO_INT#
SDVO_FLDSTALL#

SDVO_TVCLKIN
SDVO_INT
SDVO_FLDSTALL

SDVOB_RED#
SDVOB_GREEN#
SDVOB_BLUE#
SDVOB_CLKN
SDVOC_RED#
SDVOC_GREEN#
SDVOC_BLUE#
SDVOC_CLKN

SDVOB_RED
SDVOB_GREEN
SDVOB_BLUE
SDVOB_CLKP
SDVOC_RED
SDVOC_GREEN
SDVOC_BLUE
SDVOC_CLKP

NB PEG / Video Interfaces

SYNC_MASTER=NB

SYNC_DATE=07/25/2005

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SIZE

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DRAWING NUMBER

051-7374

REV.

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SCALE

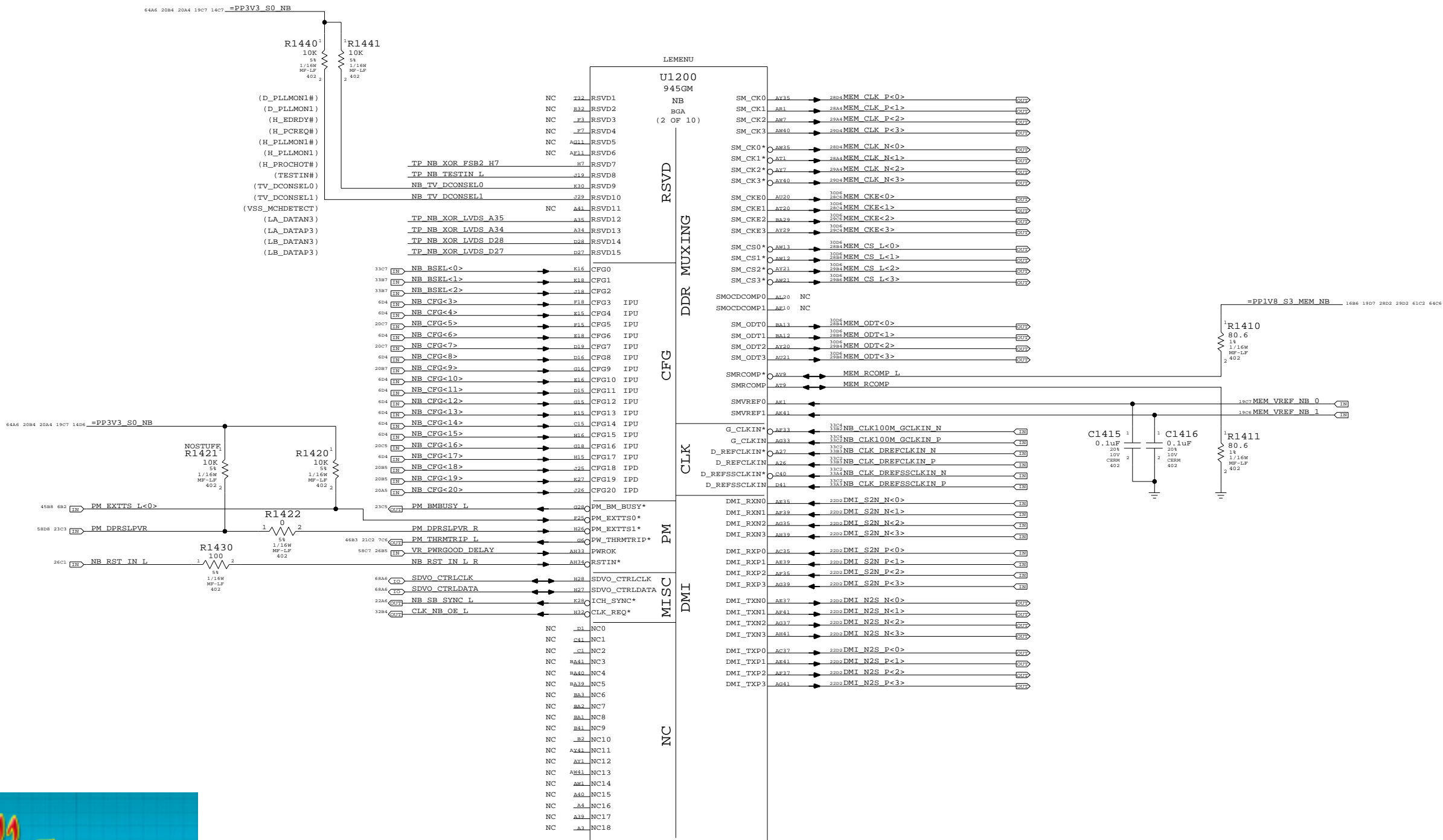
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SHT

13

OF

79



NB Misc Interfaces	
SYNC_MASTER=NB	SYNC_DATE=08/15/2005
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	D	051-7374	A
SCALE		SHT	OF
NONE		14	79



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NCTF balls are Not Critical To Function
These connections can break without
impacting part performance.

NCTF

U1200
945GM
NB
BGA
(7 OF 10)

VCC_NCTF0
VCC_NCTF1
VCC_NCTF2
VCC_NCTF3
VCC_NCTF4
VCC_NCTF5
VCC_NCTF6
VCC_NCTF7
VCC_NCTF8
VCC_NCTF9
VCC_NCTF10
VCC_NCTF11
VCC_NCTF12

VSS_NCTF0
VSS_NCTF1
VSS_NCTF2
VSS_NCTF3
VSS_NCTF4
VSS_NCTF5
VSS_NCTF6
VSS_NCTF7
VSS_NCTF8
VSS_NCTF9
VSS_NCTF10
VSS_NCTF11
VSS_NCTF12

VCCAUX_NCTF0
VCCAUX_NCTF1
VCCAUX_NCTF2
VCCAUX_NCTF3
VCCAUX_NCTF4
VCCAUX_NCTF5
VCCAUX_NCTF6
VCCAUX_NCTF7
VCCAUX_NCTF8
VCCAUX_NCTF9
VCCAUX_NCTF10
VCCAUX_NCTF11
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=PP1V5_S0_NB_VCCAUX

1786 1586
1907 6406

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NB Power 1

SYNC_MASTER=NB

SYNC_DATE=07/25/2005

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SIZE

D

DRAWING NUMBER

051-7374

REV.

A

SCALE

NONE

SHT

16

OF

79

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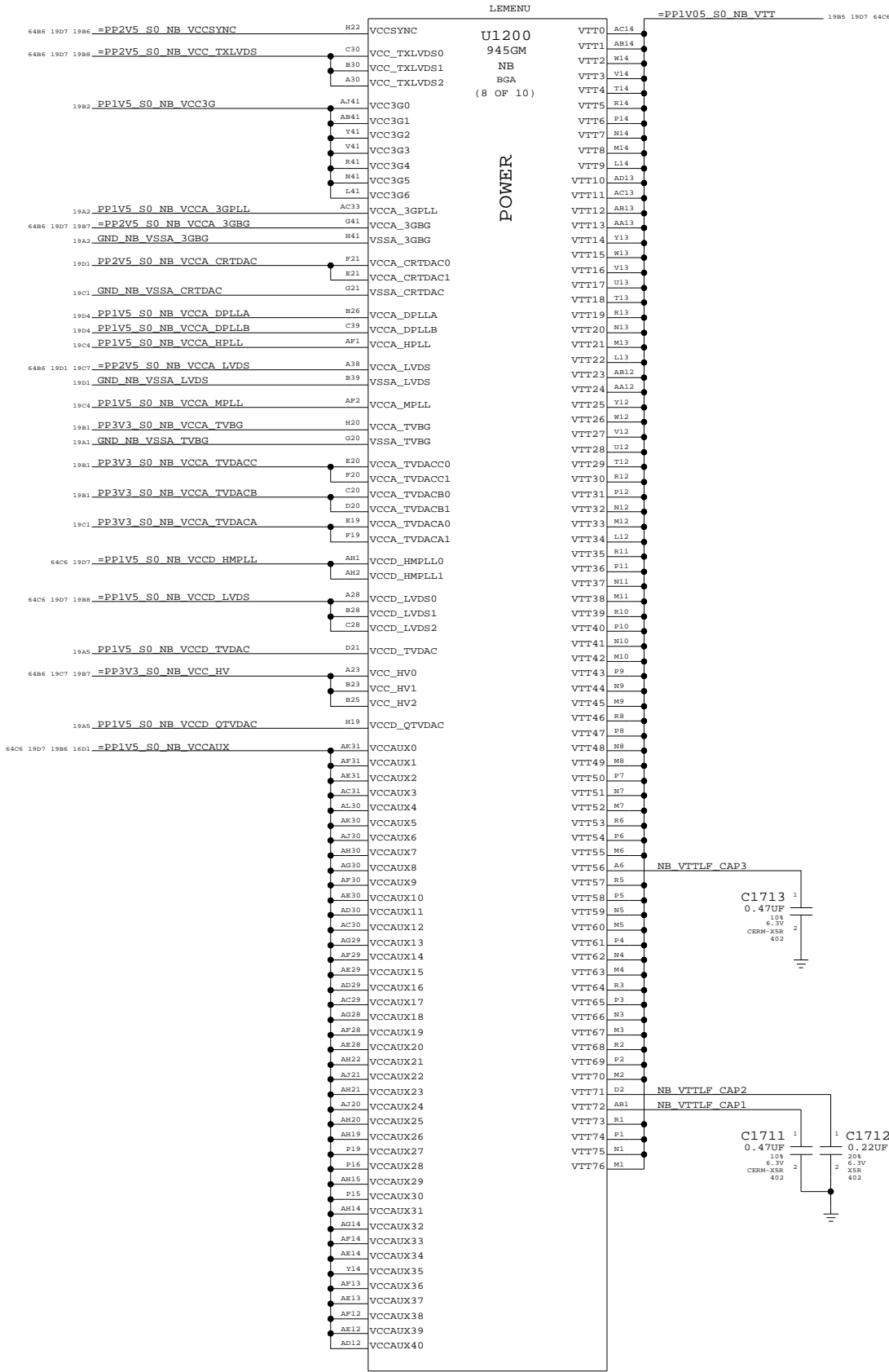
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NB Power 2

SYNC_MASTER=NB SYNC_DATE=07/25/2005

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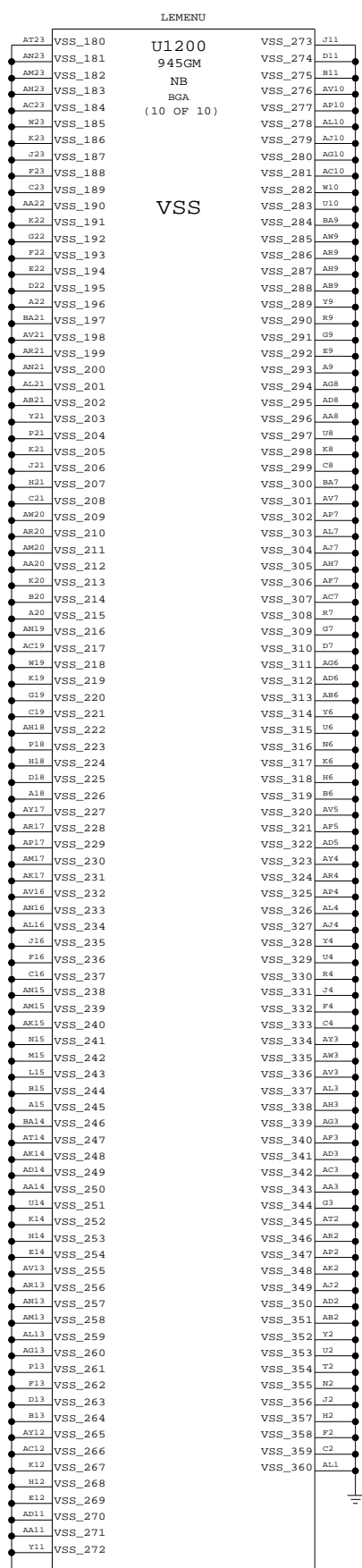
SIZE D

DRAWING NUMBER 051-7374


REV. A

SCALE NONE

SHT 17 OF 79



NB Grounds	
SYNC_MASTER=NB	SYNC_DATE=07/25/2005
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	D	051-7374	A
	SCALE	SHT OF	
	NONE	18 79	

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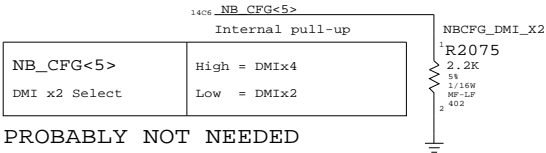
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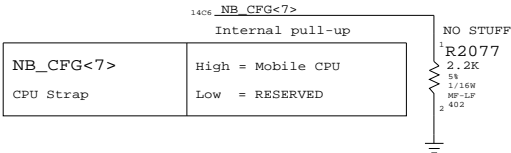
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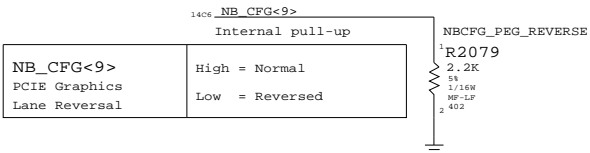
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NB_CFG<6>	RESERVED
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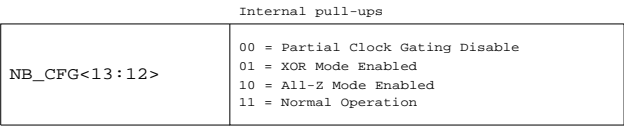


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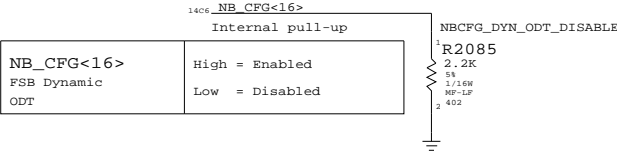
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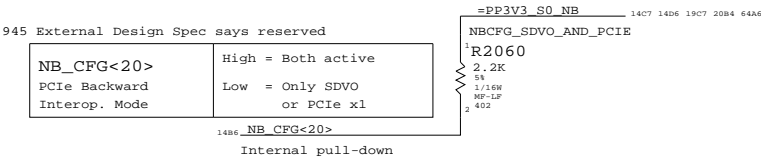
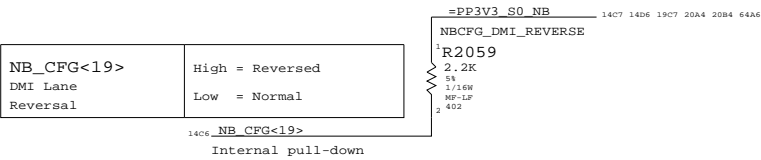
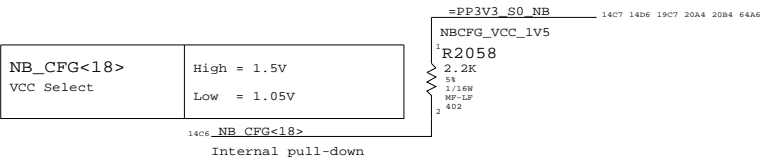


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NB_CFG<15>	RESERVED
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NB_CFG<17>	RESERVED
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PROBABLY NOT NEEDED



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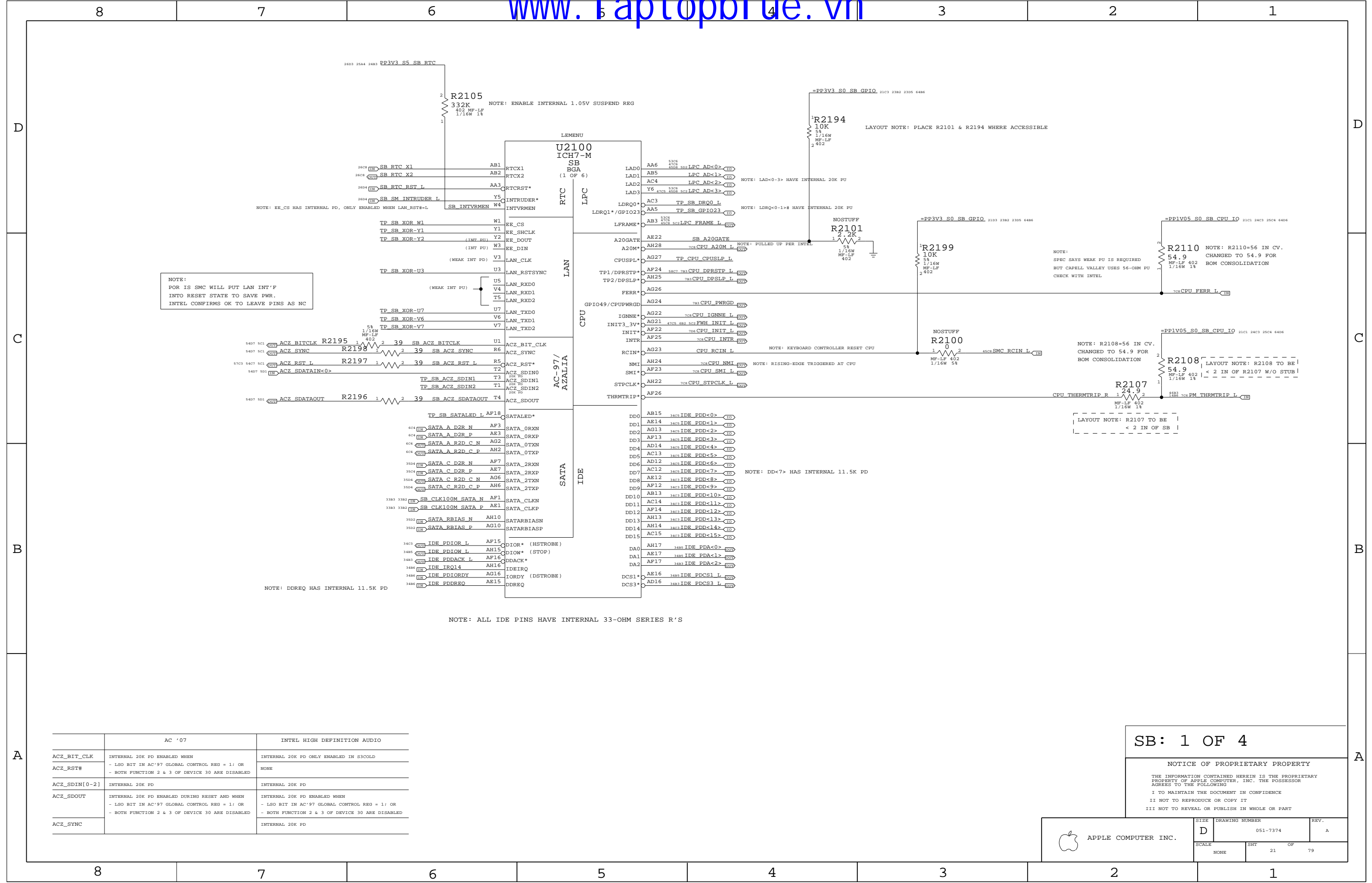
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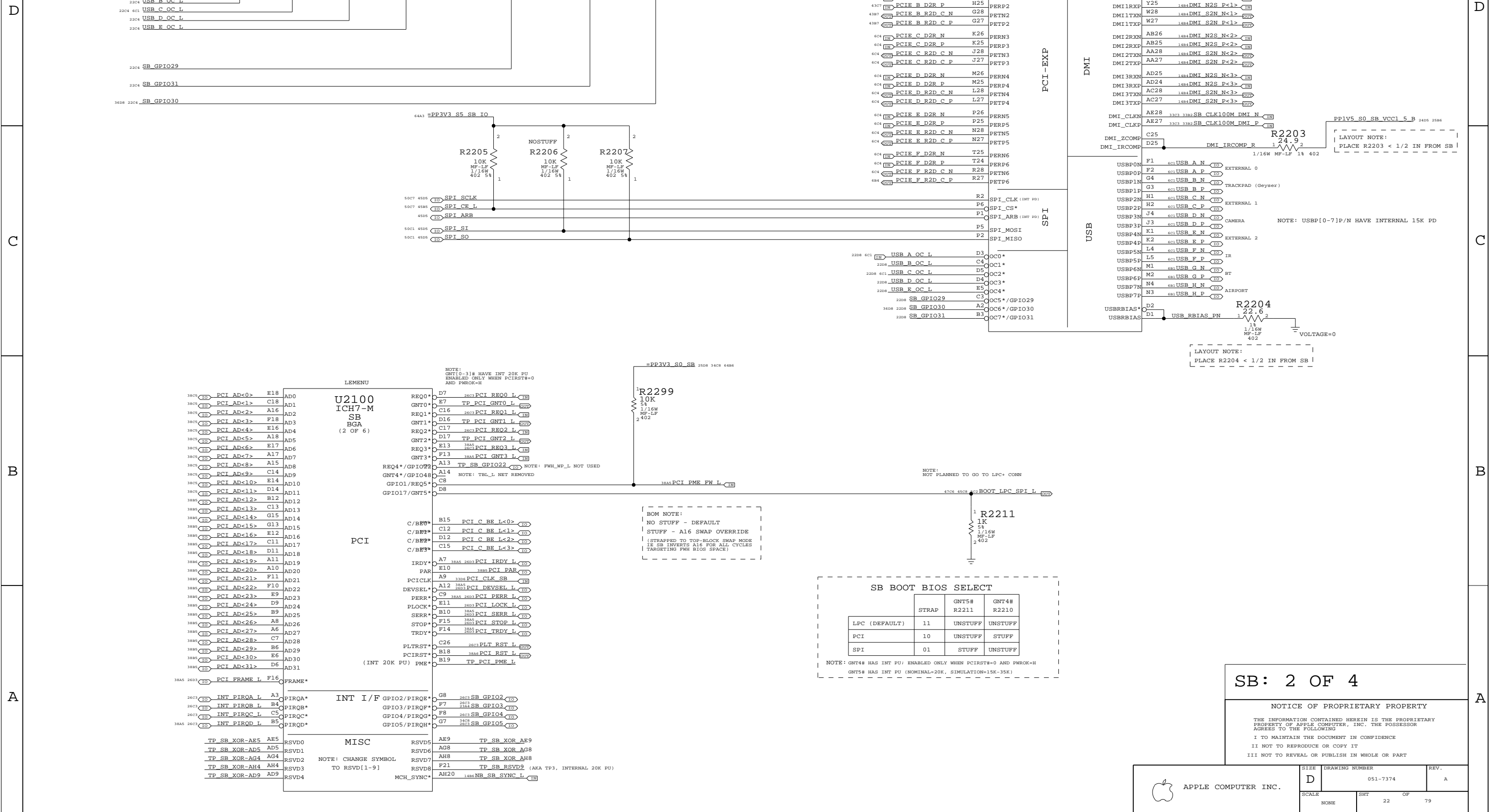
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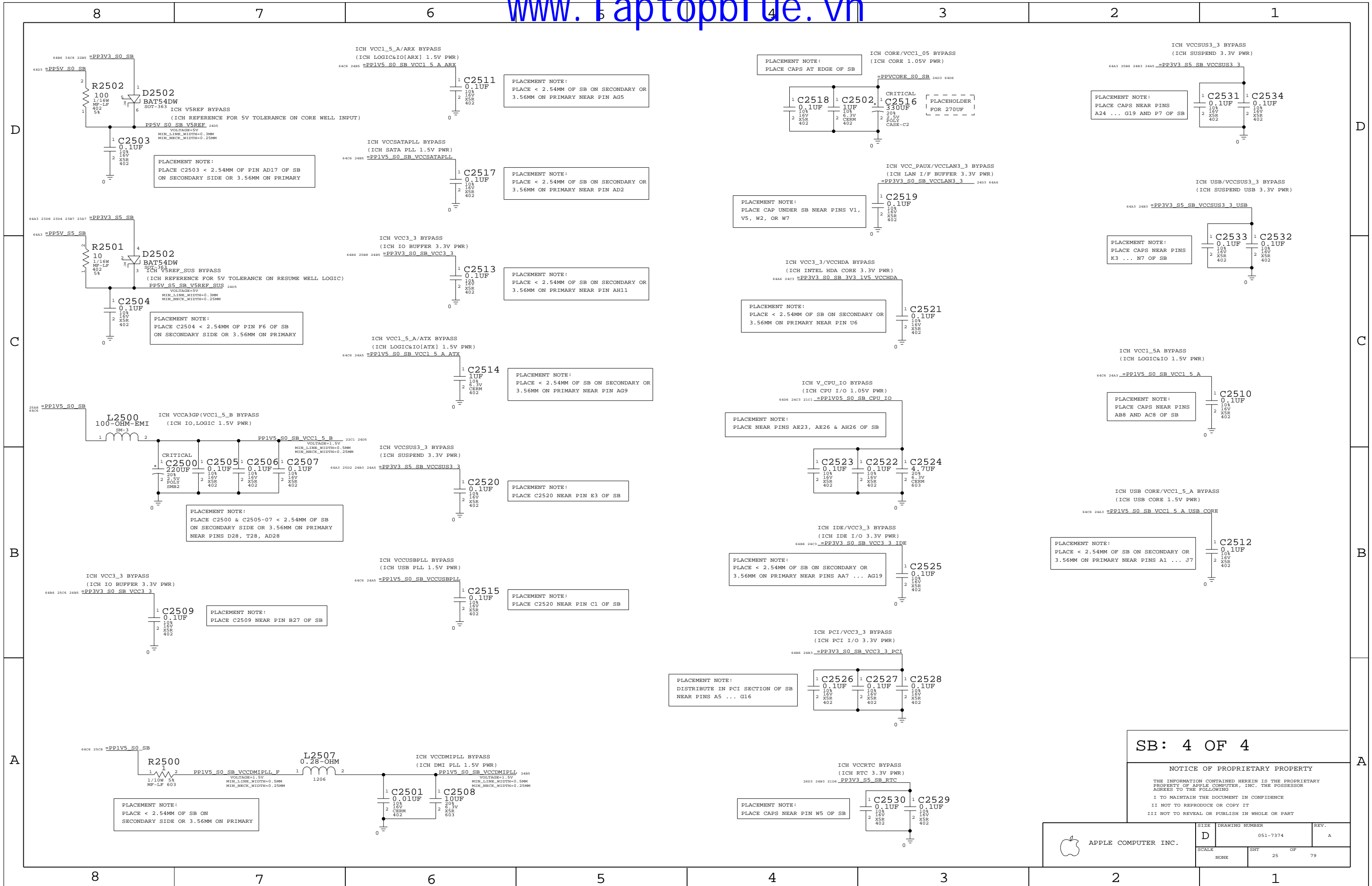
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NB Config Straps	
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NONE	25	79

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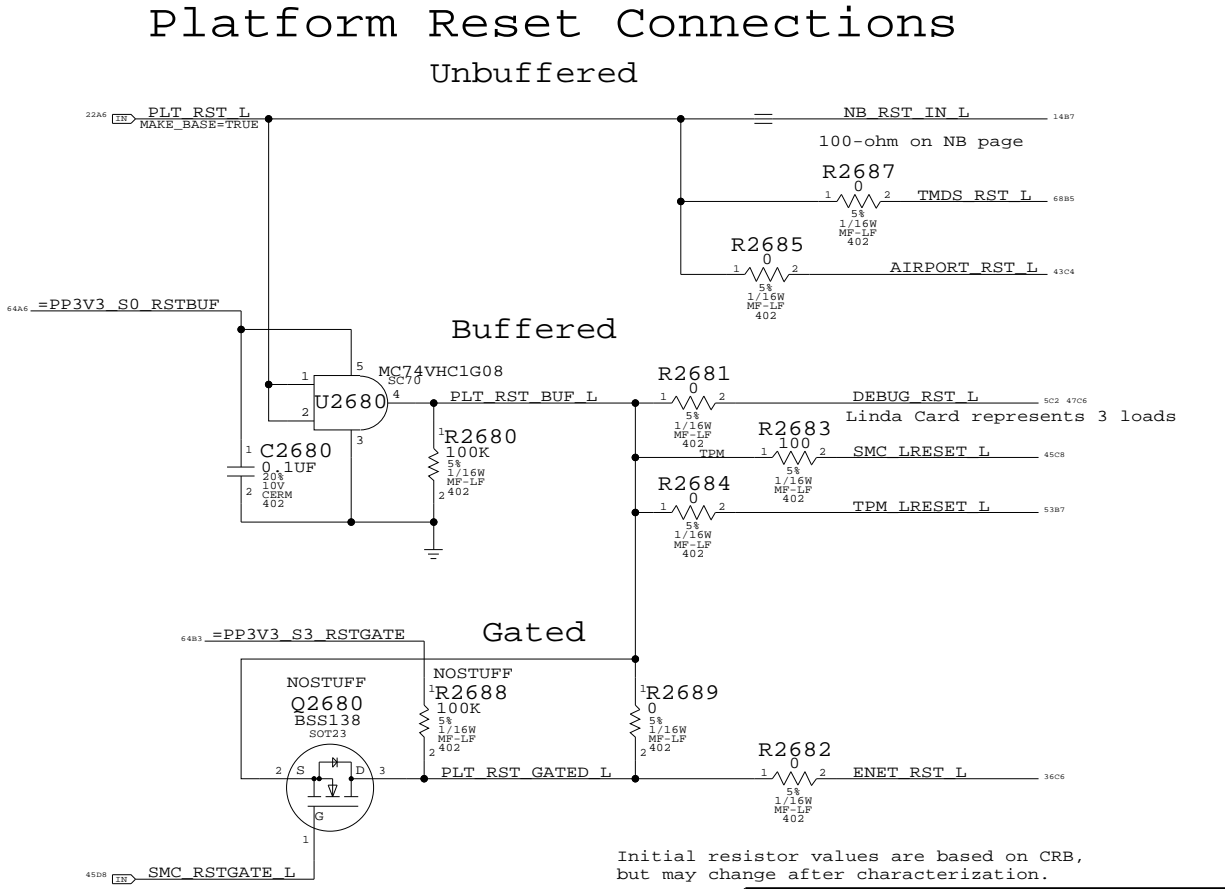
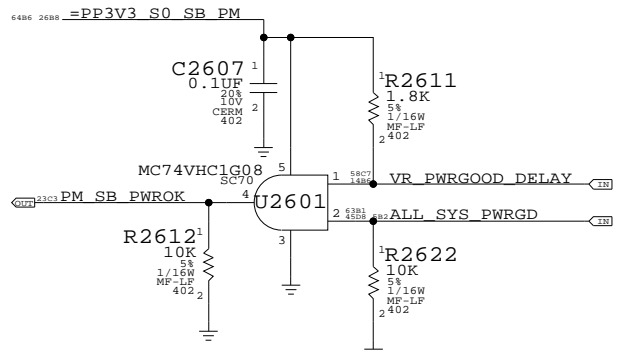
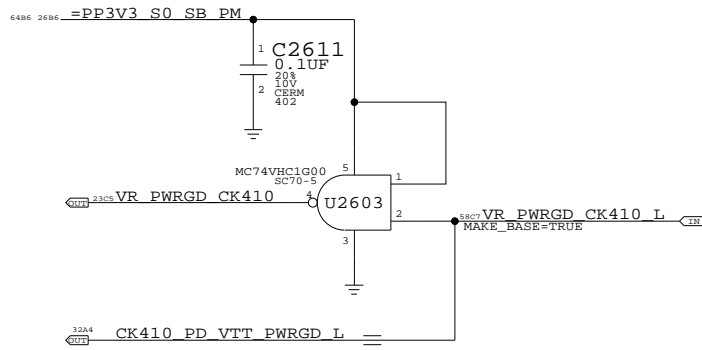
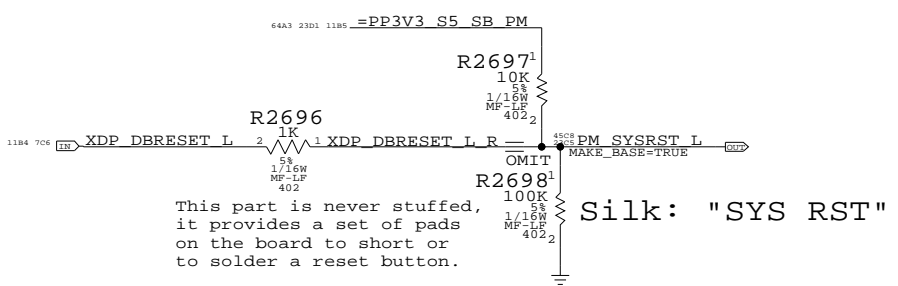
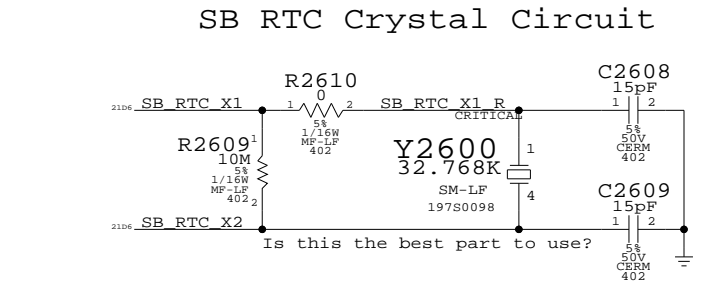
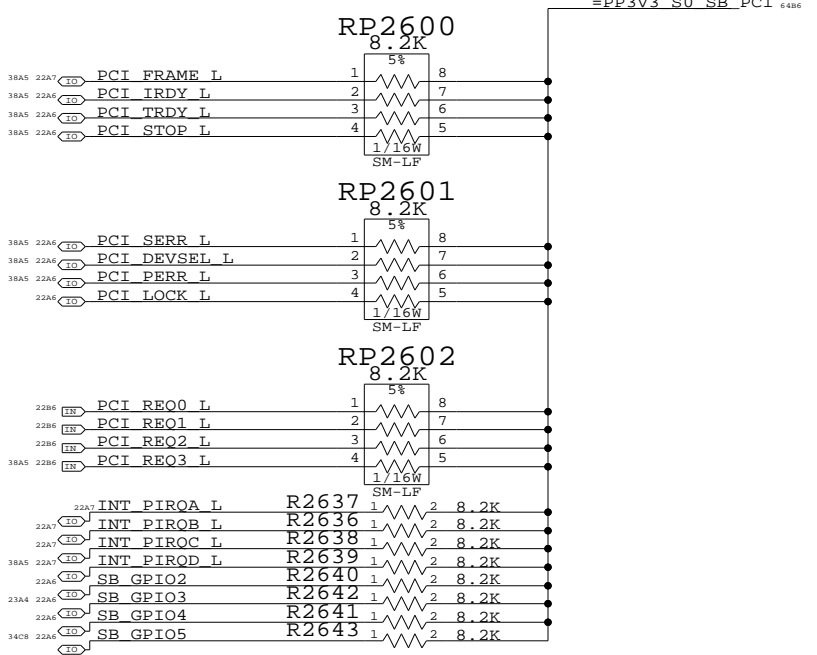
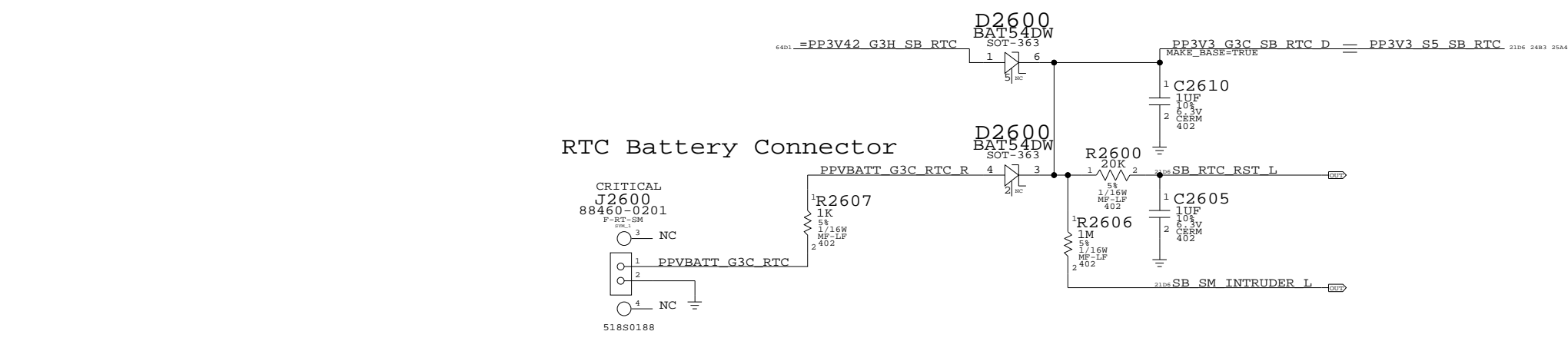
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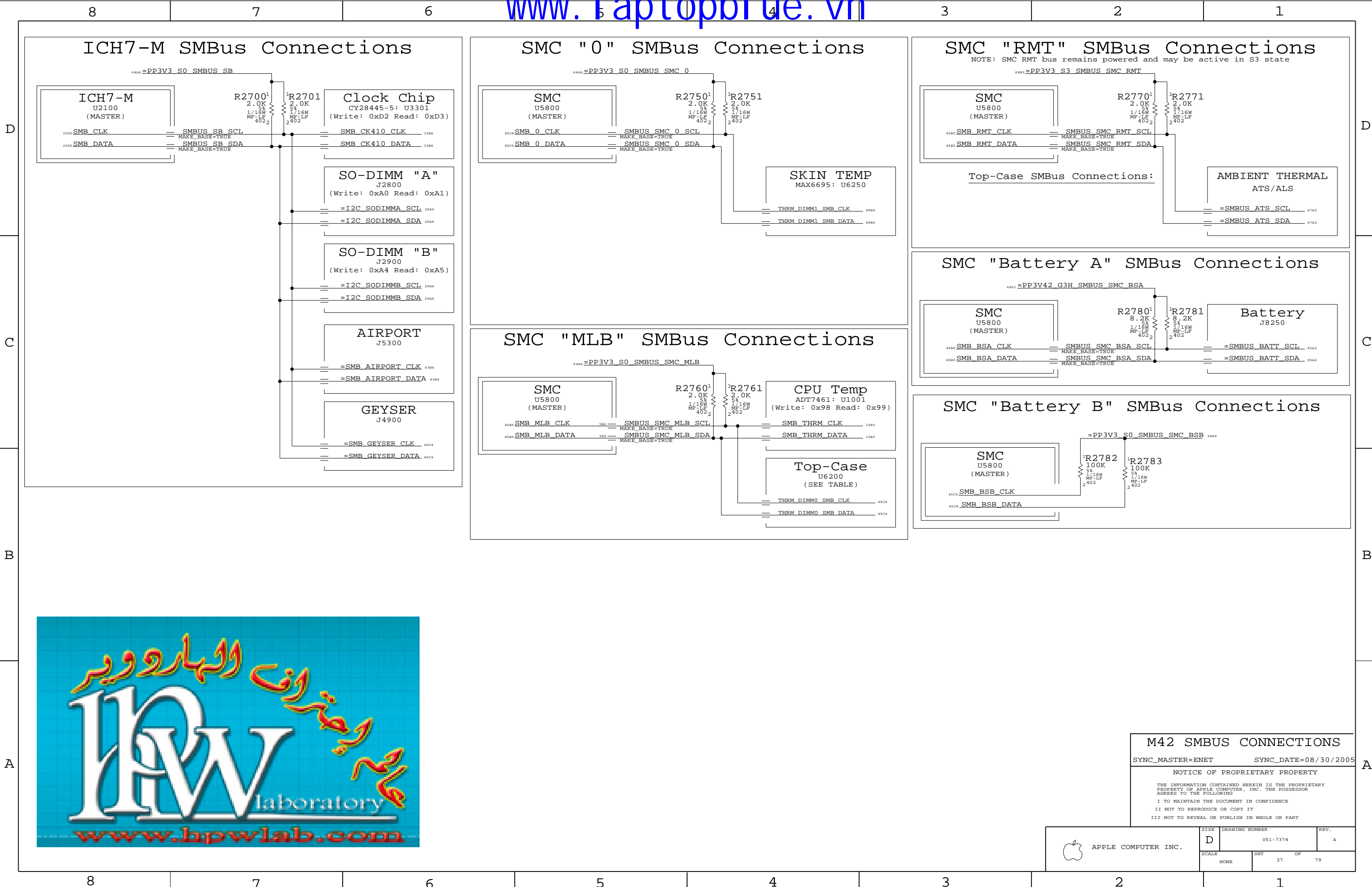
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SB Misc	
SYNC_MASTER=NB	SYNC_DATE=07/26/2005
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SCALE		SHT	OF
NONE		26	79



M42 SMBUS CONNECTIONS

SYNC_MASTER=ENET SYNC_DATE=08/30/2005

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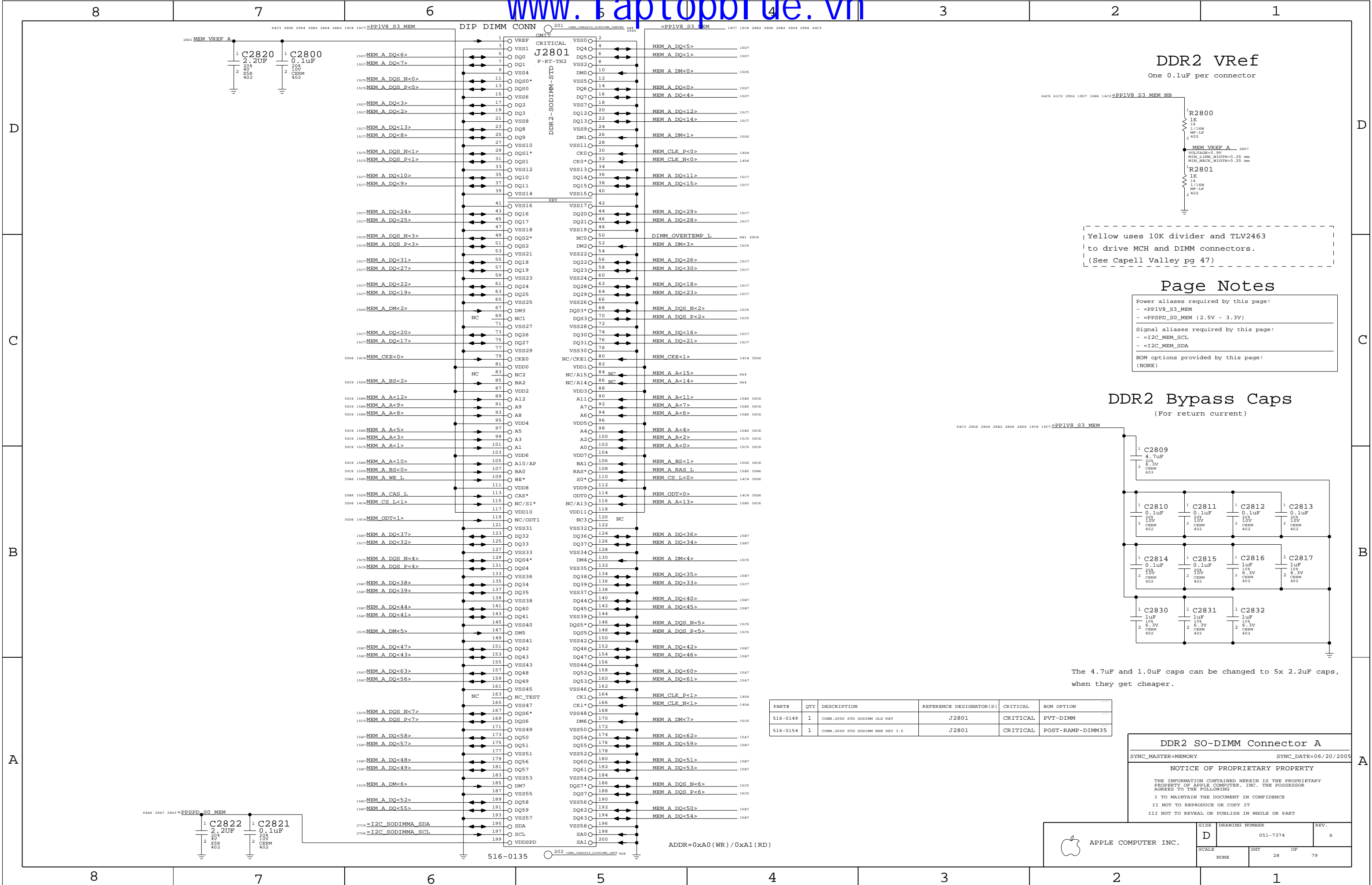
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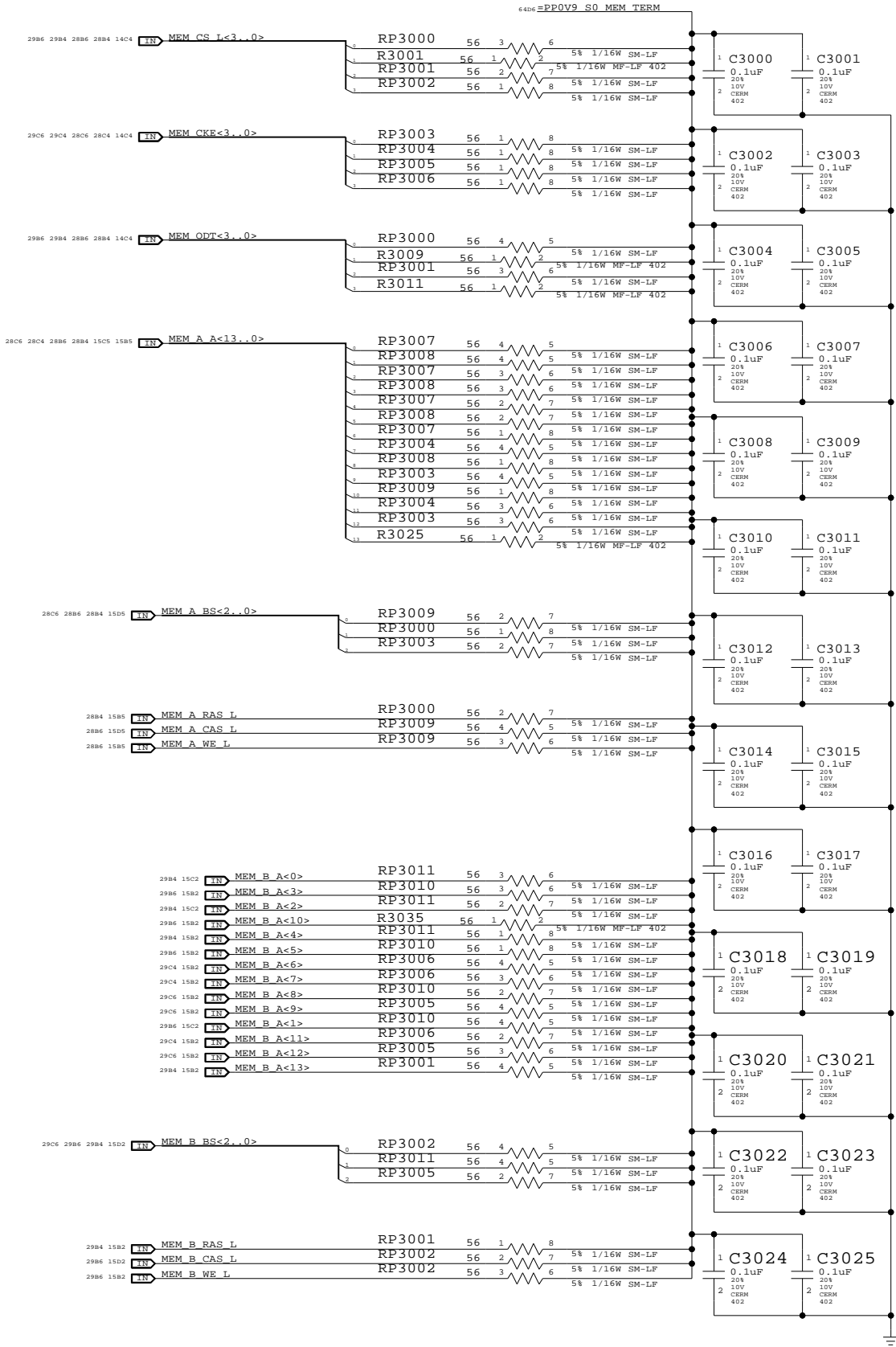
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7374	REV. A
	SCALE NONE	SHT 27	OF 79





One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it



LAYOUT NOTE:PLACE ONE CAP CLOSE TO EVERY TWO PULLUP RESISTORS TERMINATED TO PP0V9_S0_MEM_TERM

Memory Active Termination

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NONE		30	79

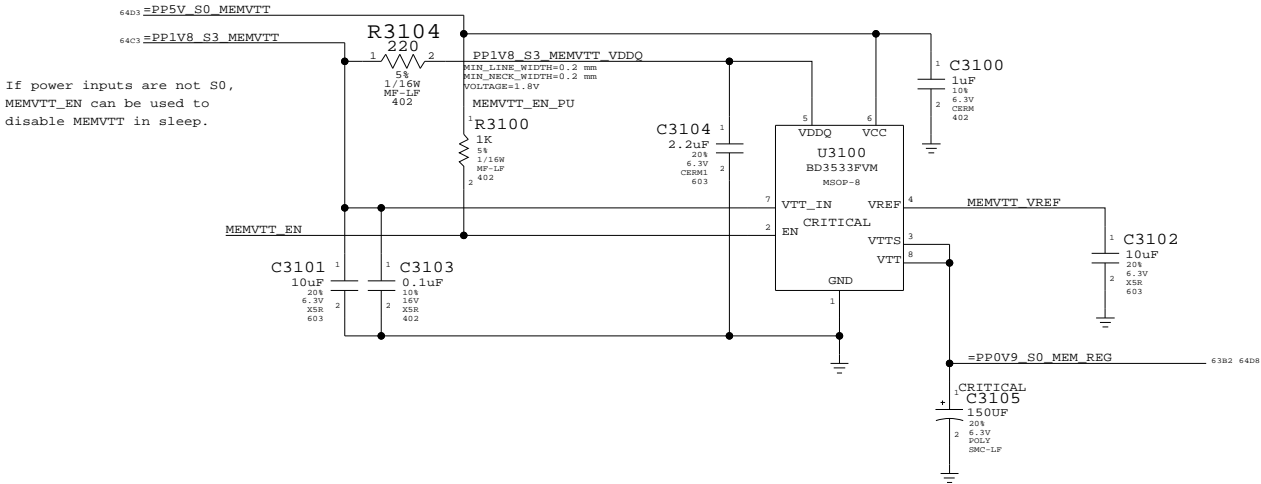
Page Notes

Power aliases required by this page:
- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

DDR2 Vtt Regulator



Memory Vtt Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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D	051-7374	A
SCALE	SHT	OF
NONE	31	79

D

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NEED TO CHECK CAP VALUE

(EACH POWER PIN PLACED ONE 0.1UF)
(PLACED 0.1UF NEAR THE RELATIVE POWER PIN)

NEED TO DECIDE THE CLKREQ CONNECTION,TO GPIO?

FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST
0	1	DOT96T	DOT96C	SRCT0	SRCC0
1	0	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0
1	1	OFF LOW	TBD	SRCT0	SRCC0

* FOR INT. GRAPHIC SYSTEM

* FOR EXT. GRAPHIC SYSTEM

CLOCKS

SYNC_MASTER=CLOCK

SYNC_DATE=06/03/2005

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APPLE COMPUTER INC.

SIZE

D

DRAWING NUMBER

051-7374

REV.

A

SCALE

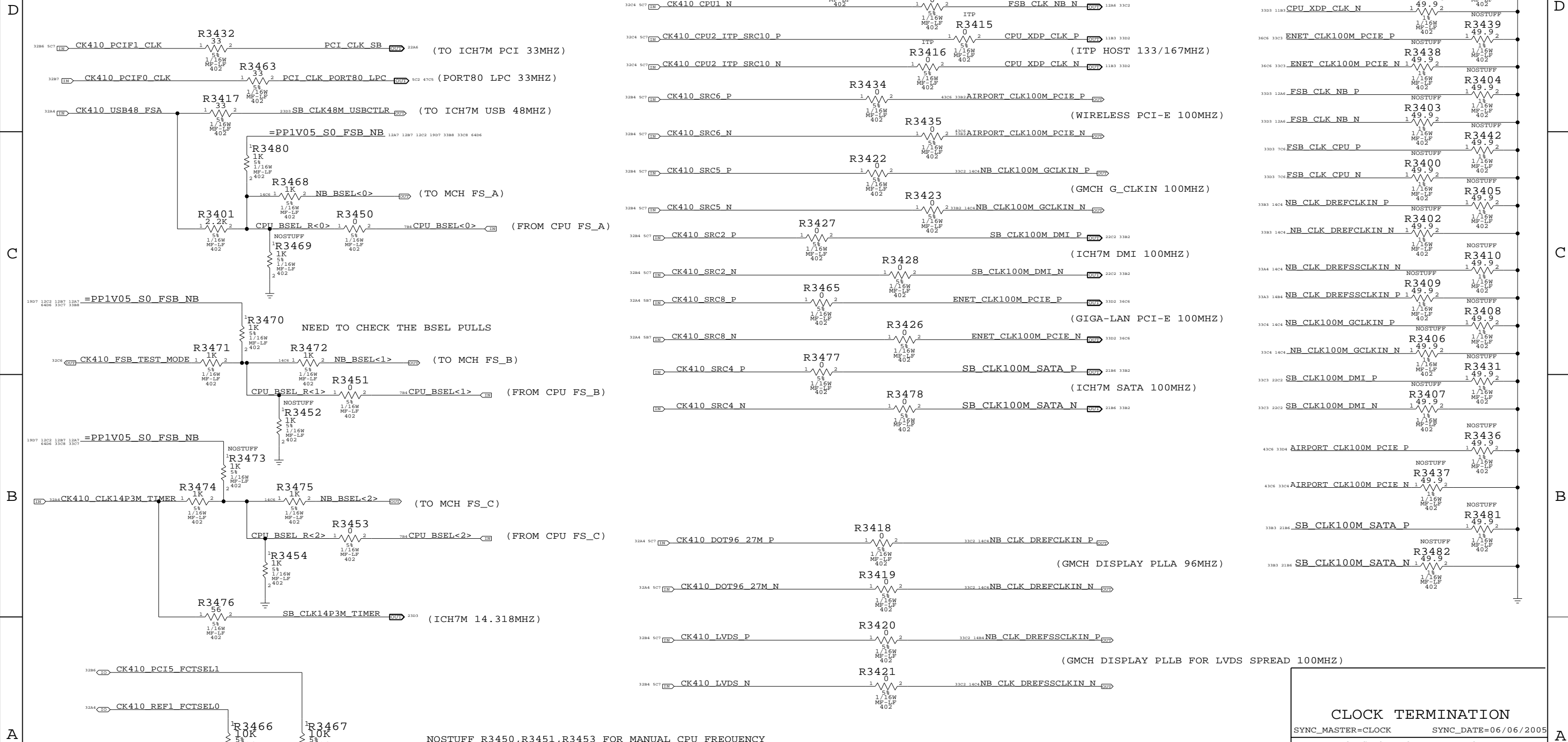
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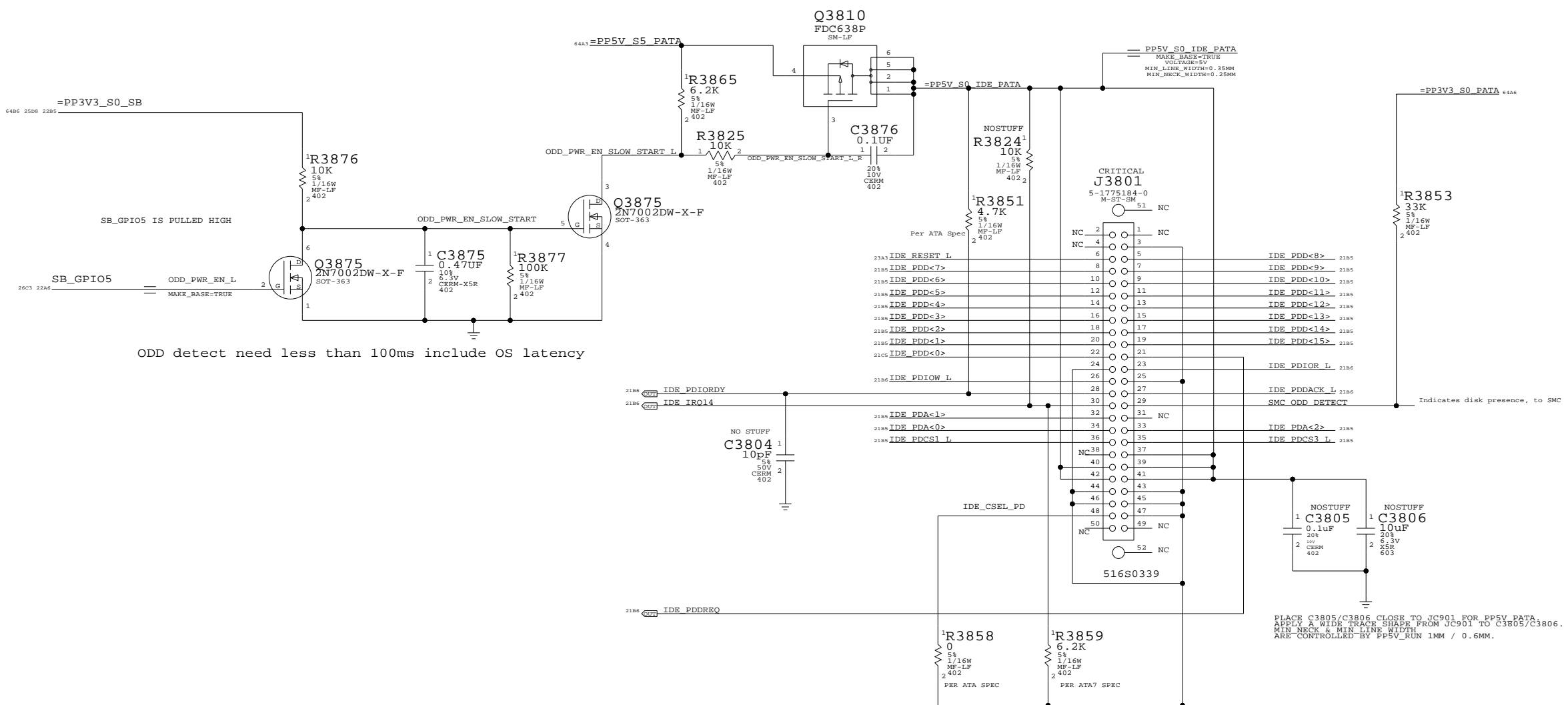
SHT

32

OF

79





PATA CONNECTOR

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7374	REV. A
	SCALE NONE	SHT 34	OF 79

SATA CONNECTOR

D

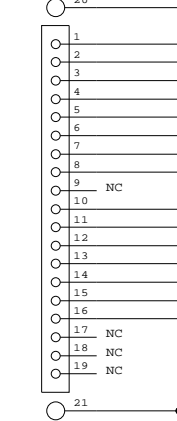
C

B

A

518S0390

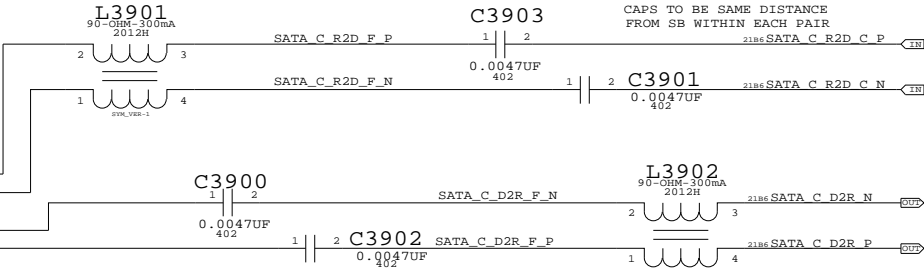
CRITICAL
J3901
20247-019E
F-ST-SM
20



GND CHASSIS SATA

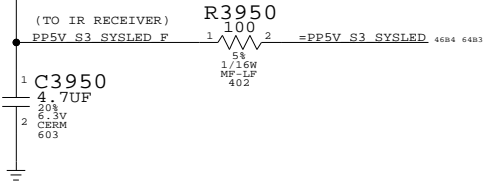
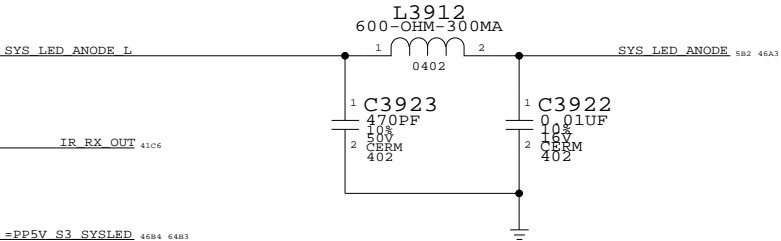
Place L3901 near J3901

VALUE=3900PF IN REFERENCE SCHEM

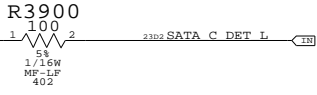


PLACE L3902 NEAR SB

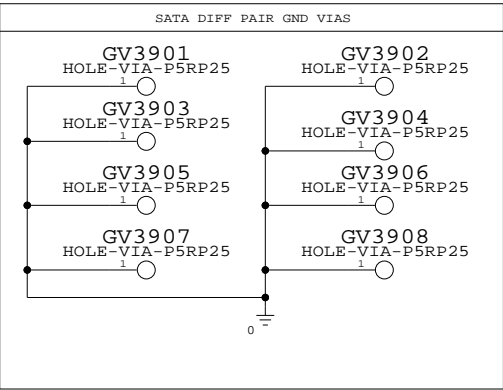
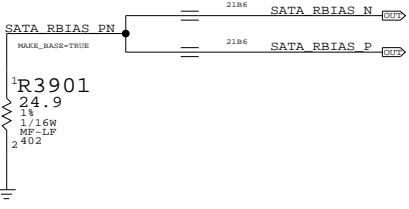
SYSTEM (SLEEP) LED FILTER



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0227	155S0164	?	L3901, L3902	KEEP MAG LAYER IN BOM



PLACE NEAR ICH7 PIN



D

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A

SATA CONNECTOR

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7374	A
SCALE	SHT	OF
NONE	35	79

D

C

B

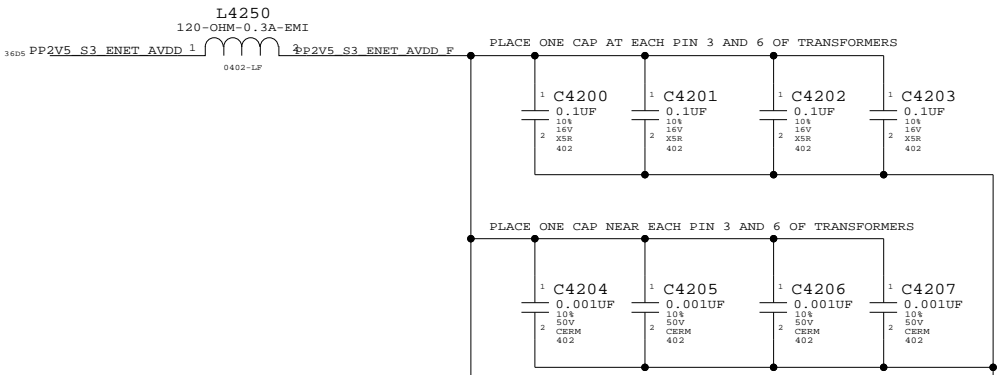
A

D

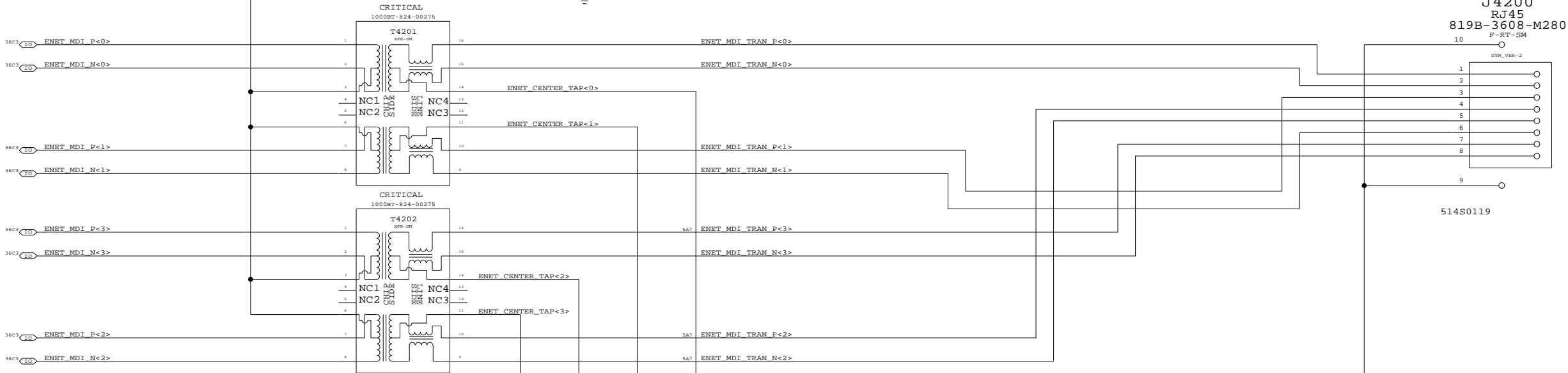
C

B

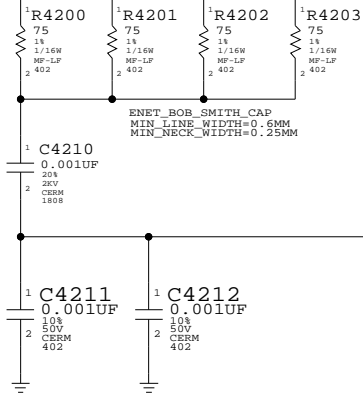
A



CROSS-OVERS ARE IN SCHEMATIC TO EASE ROUTING




PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
157S0037	157S0011	?	T4201, T4202	SEE AMD DELTA TRANSFORMER



PLACE C4211 AND C4212 ON EACH SIDE OF J4200

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514S0143	1	CONN, SP RJ-45 JACK, MIDPLANE, M33, LF	J4200	CRITICAL	NORMAL
514S0144	1	CONN, SP RJ-45 JACK, MIDPLANE, BLACK, LF	J4200	CRITICAL	FANCY

APPLE COMPUTER INC.

ETHERNET CONNECTOR

SYNC_MASTER=ENET

SYNC_DATE=11/14/2005

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SIZE D

DRAWING NUMBER 051-7374

REV. A

SCALE NONE

SHT 37 OF 79

PAGE NOTES

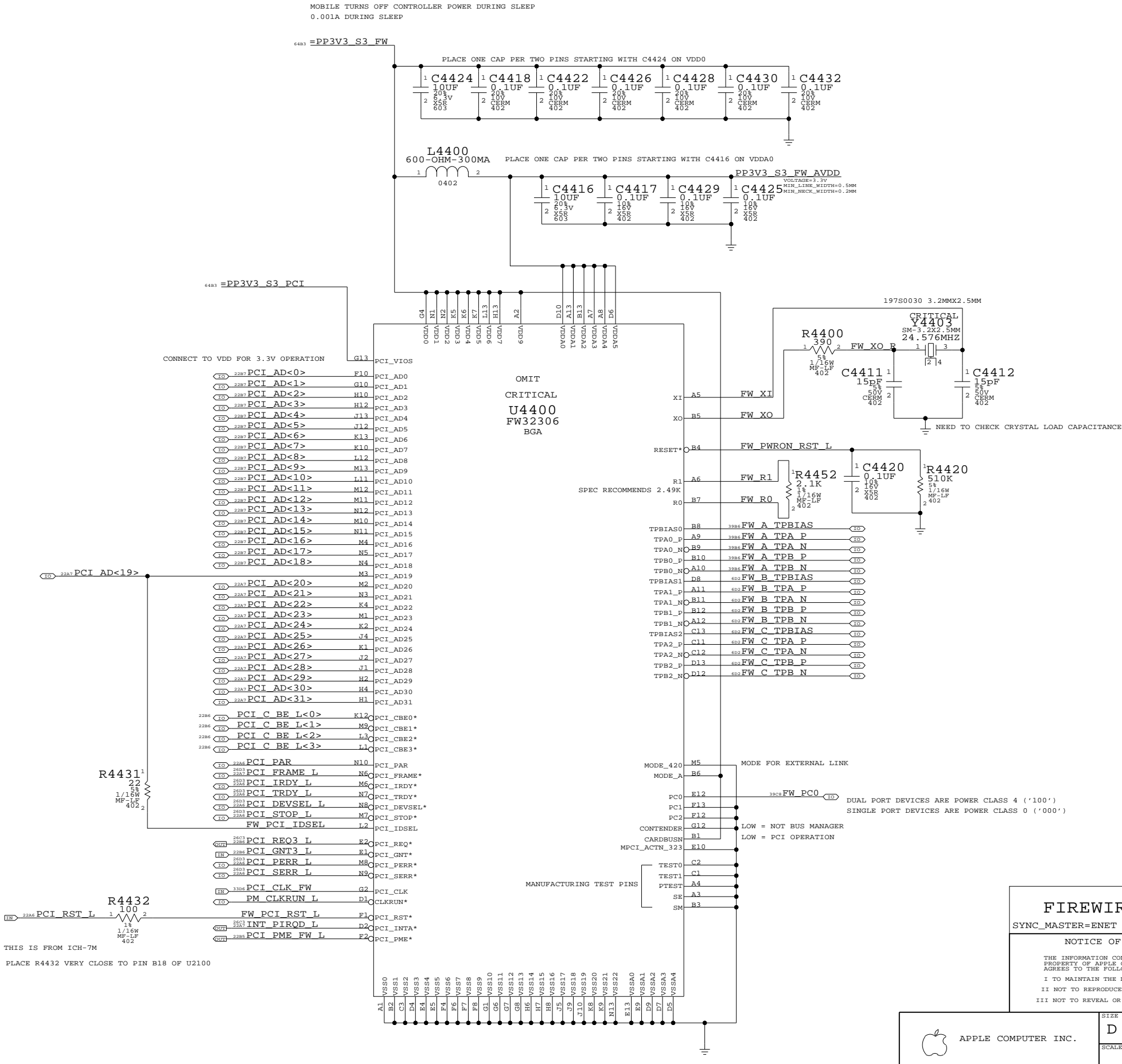
INPUT
=PP3V3_S0_FW - 3.3V POWER FOR FIREWIRE (MOBILE: OFF DURING SLEEP)
=PP3V3_S0_PCI - 3.3V POWER FOR PCI FIREWIRE (MOBILE: OFF DURING SLEEP)
PCI_GNT3_L - PCI GRANT FROM SB
PCI_CLK_FW - NEED TO REFERENCE TO ALIAS PAGE
PCI_RST_L - PCI RESET FROM SB
FW_PC0 - FIREWIRE POWER CLASS IDENTIFIER

INPUT/OUTPUT
PCI_AD<0..31>, PCI_C_BE_L<0..3>, PCI_FRAME_L, PCI_IRDY_L, PCI_TRDY_L,
PCI_DEVSEL_L, PCI_STOP_L, PCI_PAR, PCI_PERR_L, PCI_SERR_L
FW_A_TPA_P/N, FW_A_TPB_P/N, FW_A_TPBIAS - PORT 0 FIREWIRE DIFF PAIRS
FW_B_TPA_P/N, FW_B_TPB_P/N, FW_B_TPBIAS - PORT 1 FIREWIRE DIFF PAIRS
FW_C_TPA_P/N, FW_C_TPB_P/N, FW_C_TPBIAS - PORT 2 FIREWIRE DIFF PAIRS

OUTPUT
PCI_REQ3_L - PCI REQUEST TO SB
PM_CLKRUN_L - CLOCK-RUN PCI PROTOCOL
INT_PIRQD_L - INTERRUPT TO SB
PCI_PME_FW_L - DEDICATED PME FOR FIREWIRE (SB GPIO1)

PAGE HISTORY

5/19/2005 - FIRST REVISION OF PAGE
6/20/2005 - BGA VERSION OF FW323-06 ADDED
6/21/2005 - CHANGED INT* TO INT_PIRQD_L (PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED PCI_ID TO AD19 (PER ARCHITECTURAL DEFINITION)
6/22/2005 - CHANGED REQ3/GNT TO REQ3/GNT3 (PER ARCHITECTURAL DEFINITION)
6/22/2005 - ADDED 510K PULL-DOWN ON RST* AND REMOVED CONNECTION TO PLT_RST_L
6/22/2005 - CHANGED CLK_PME DIFF PAIR NAMES TO BE RE-USE COMPLIANT
6/22/2005 - REMOVED CONSTRAINT SETS AS THEY WILL BE MANAGED ON BOARD SIDE
6/22/2005 - REMOVED C4421 - REDUNDANT
6/22/2005 - BRING OUT PC0 CONNECTION TO BE CONNECTED ON PORT PAGE
7/26/2005 - CONNECTED PIN E10 TO GND



FIREWIRE CONTROLLER

SYNC_MASTER=ENET SYNC_DATE=08/30/2005

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APPLE COMPUTER INC.

SIZE D DRAWING NUMBER 051-7374 REV. A

SCALE NONE SHT 38 OF 79

Page Notes

INPUT:
=PPBUS_FW - PORT POWER
=PP3V3_S5_FW - DIGITAL POWER
=GND_CHASSIS_FW_PORT0 - CHASSIS GROUND
=FWPWR_PWRON - ADDITIONAL POWER CONTROL

INPUT/OUTPUT:
FW_TPA0_P/N,FW_TPB0_P/N,FW_TPBIA50 - FIREWIRE DIFF PAIRS

OUTPUT:
FW_PC0 - POWER CLASS IDENTIFIER (SINGLE PORT - TIE LOW)

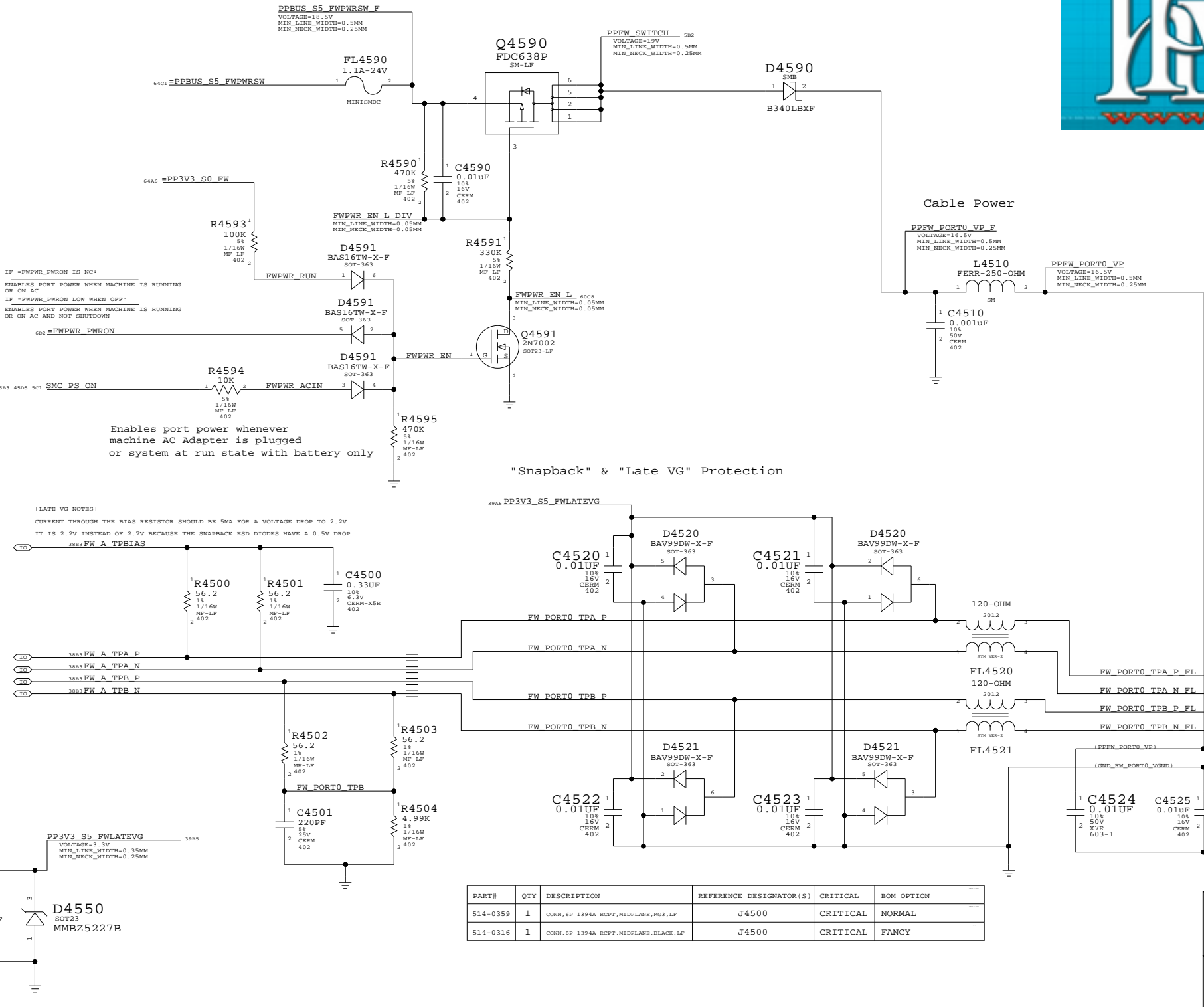
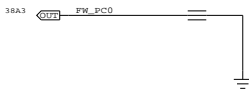
PAGE HISTORY

5/19/05 - INITIAL REVISION
6/22/05 - CHANGED DIFF PAIR NAMES TO MATCH REUSE
6/22/05 - REMOVED CONSTRAINTS BECAUSE USING ALLEGRO CONST MANAGER
6/22/05 - CONNECTED FW_PC0 FOR SINGLE PORT
7/26/05 - UPDATED LATE-VG POWER SAIL CIRCUIT FROM M1
7/26/05 - CHANGED CONNECTOR PORT NAMING TO PORT0
7/26/05 - SWITCHED TO 514-0124 FOR FIRE-PROT0 CONNECTOR
7/26/05 - REMOVED R4520 - IT HASN'T BEEN STUFFED FOR MANY PRODUCTS
7/26/05 - CHANGED FL4590 TO 1.1A VERSION
7/26/05 - REMOVED ETHERNET LOW-POWER MODE CIRCUIT
7/26/05 - UPDATED SIGNAL NAMES FOR FW PORT POWER ENABLE

1394b implementation based on Apple
FireWire Design Guide (FWDG 0.6, 5/14/03)

PORT POWER CLASS

0 FOR SINGLE PORT
1 FOR DUAL PORT



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0359	1	CONN,6P 1394A RCPT,MIDPLANE,MQ3,LF	J4500	CRITICAL	NORMAL
514-0316	1	CONN,6P 1394A RCPT,MIDPLANE,BLACK,LF	J4500	CRITICAL	FANCY

FIREWIRE PORT

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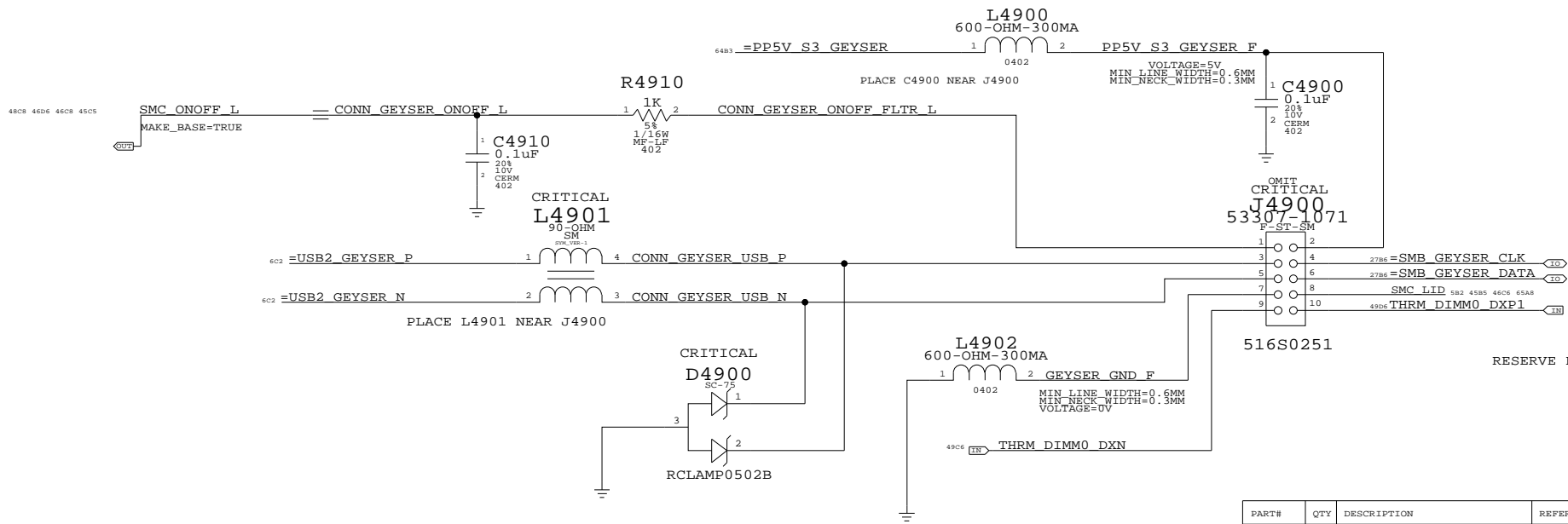


APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7374	A
SCALE	SHT	OF
NONE	39	79



GEYSER AND DIMM0 REMOTE TEMP SENSORS



CONNECTOR MISC

SYNC_MASTER=ENET SYNC_DATE=11/16/2005

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SIZE
D

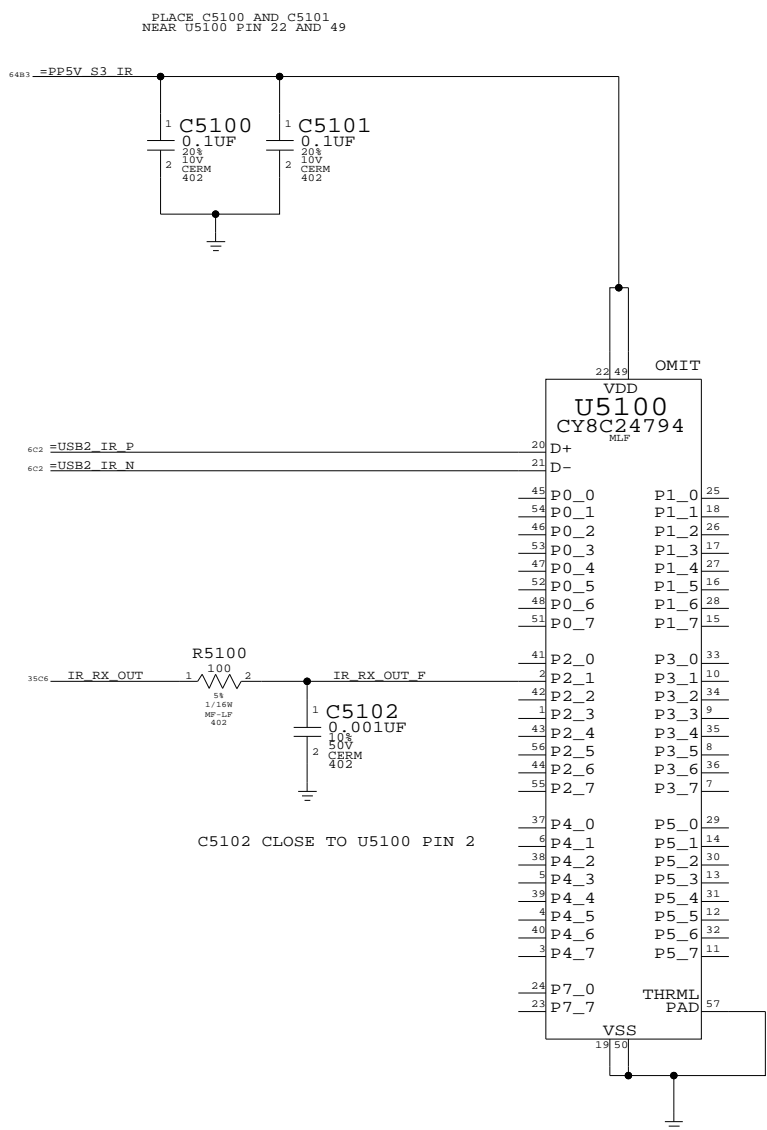
DRAWING NUMBER
051-7374

REV.
A

SCALE
NONE

SHT
40

OF
79



IR CONTROLLER

SYNC_MASTER=ENET

SYNC_DATE=11/09/2005

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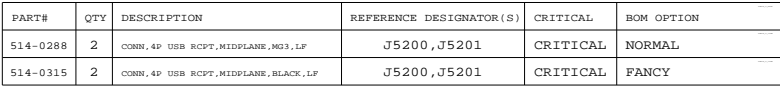
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

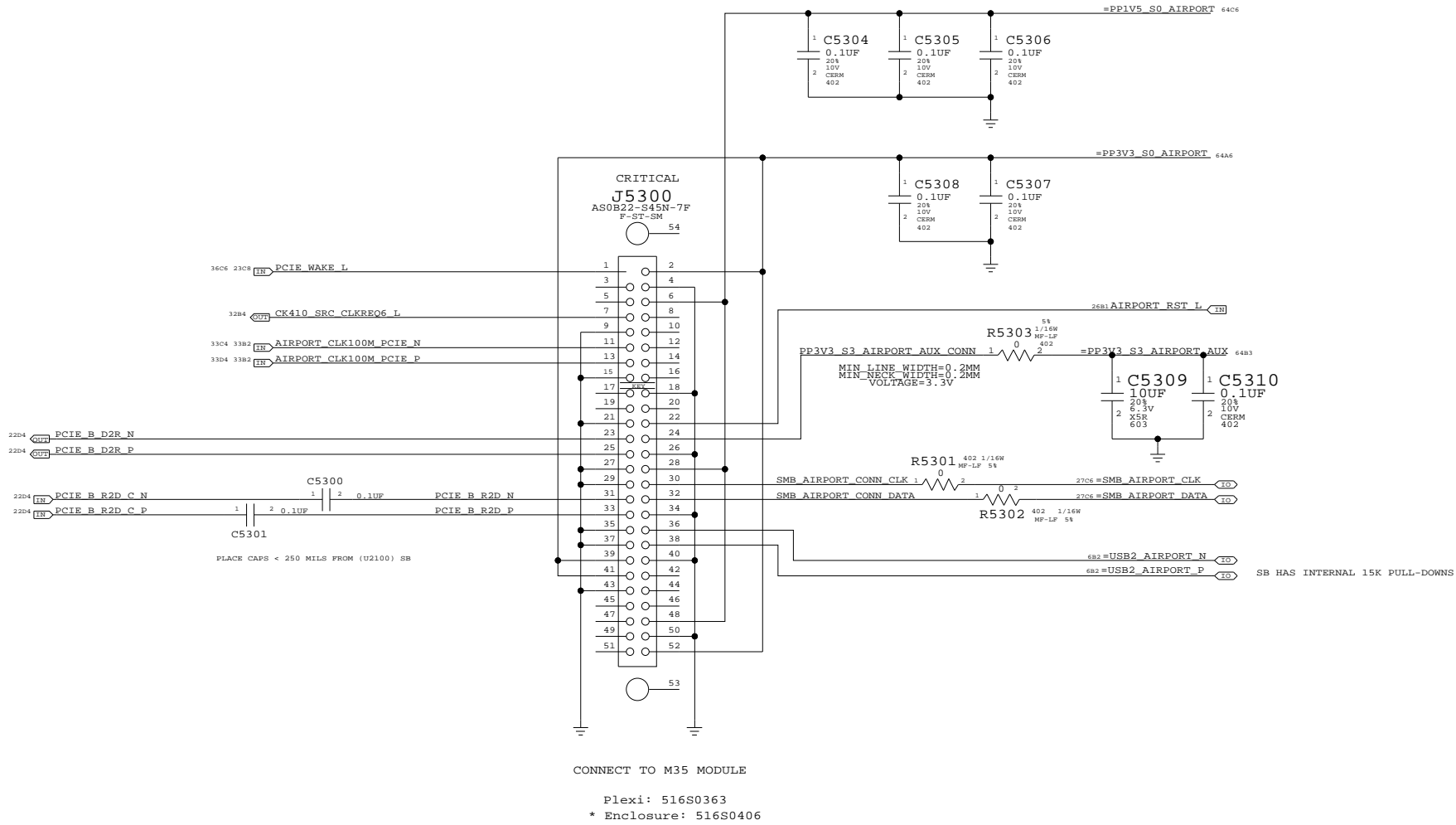
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7374	REV. A
	SCALE NONE	SHT 41	OF 79

A





AIRPORT CONN

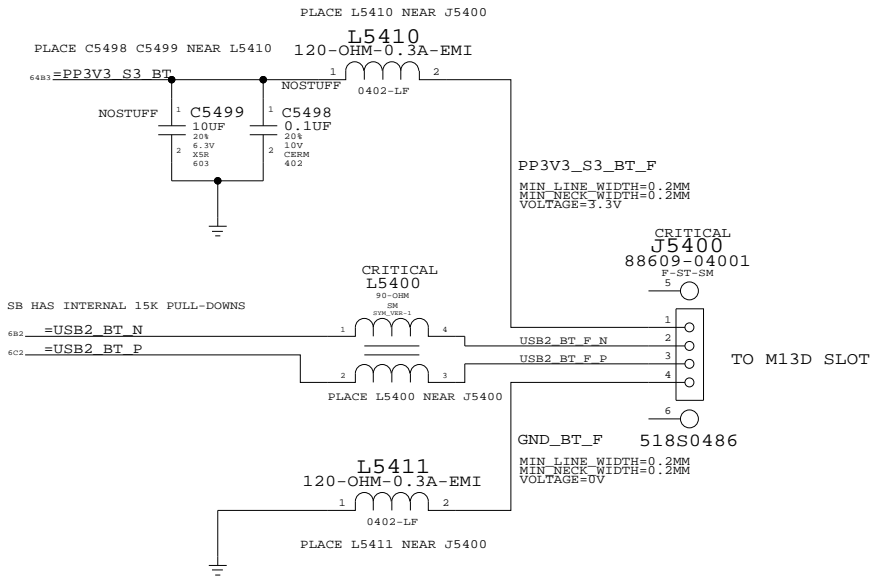
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D	051-7374	A
SCALE	SHT	OF
NONE	43	79



BLUETOOTH INTERFACE

NOTICE OF PROPRIETARY PROPERTY

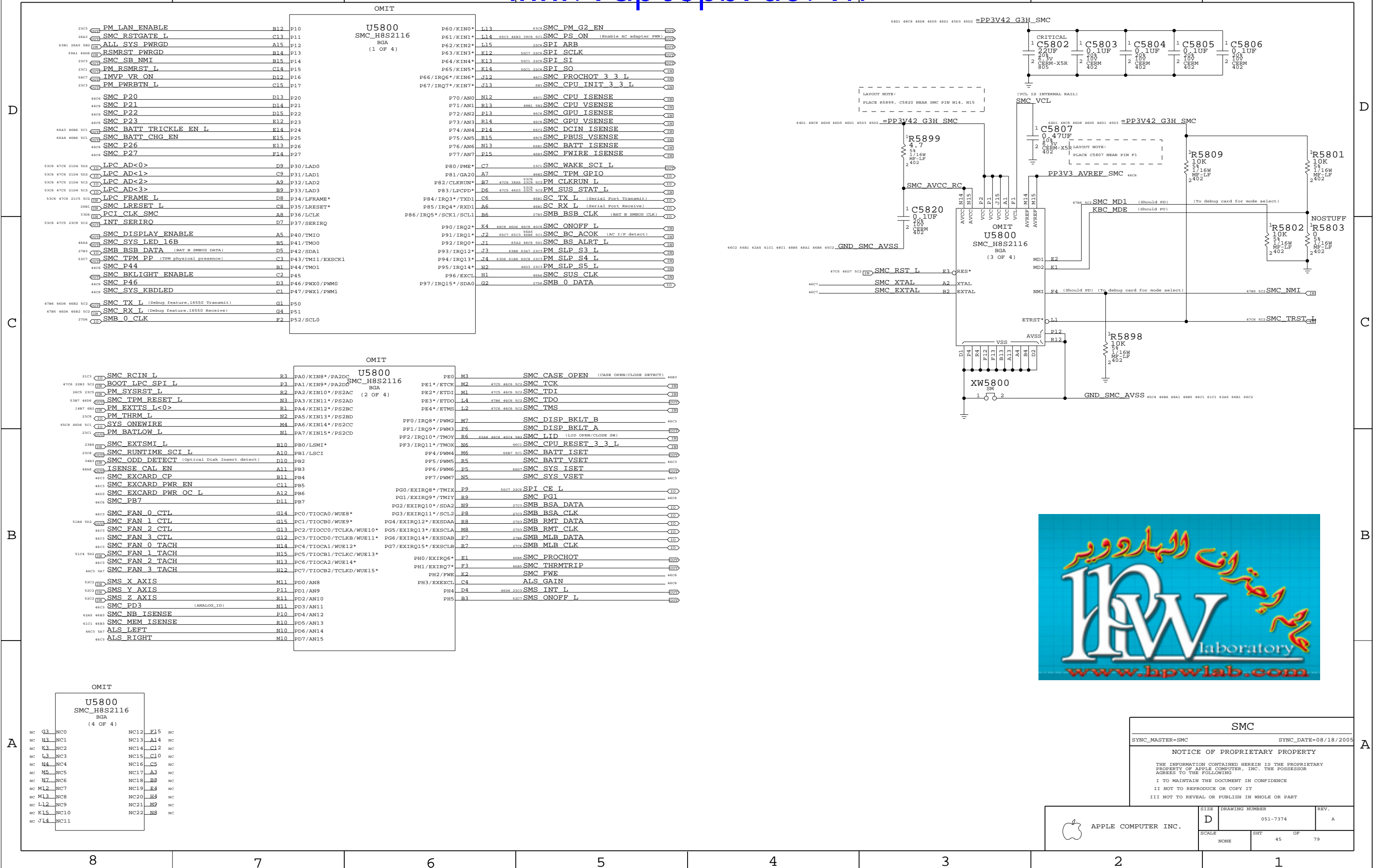
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I I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

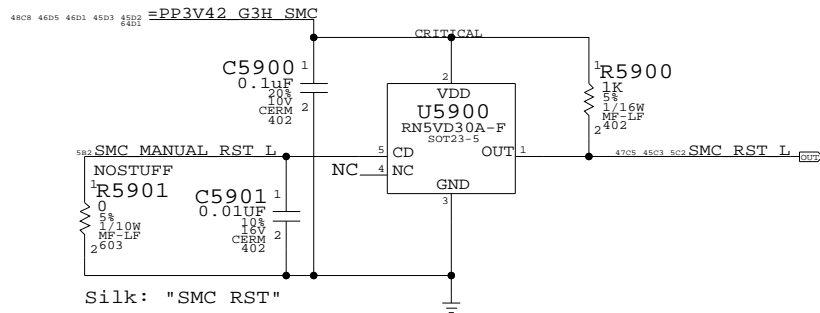
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

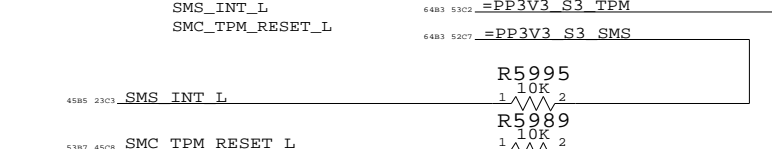
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7374	REV. A
	SCALE NONE	SHT 44	OF 79



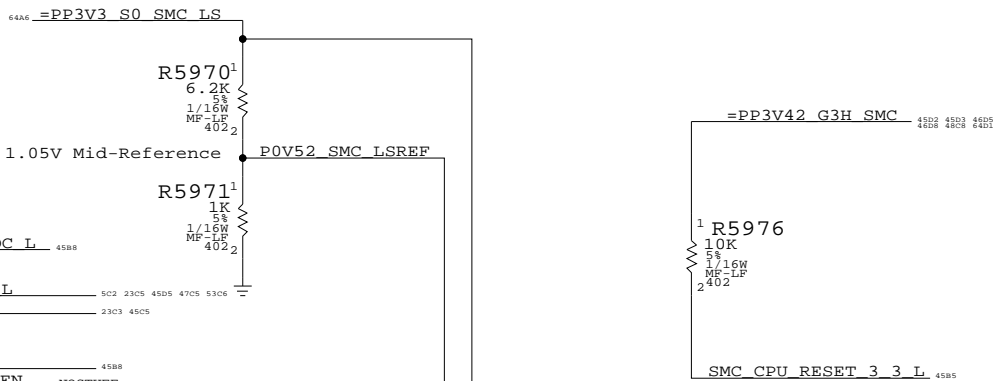
SMC Reset Button / Brownout Detect



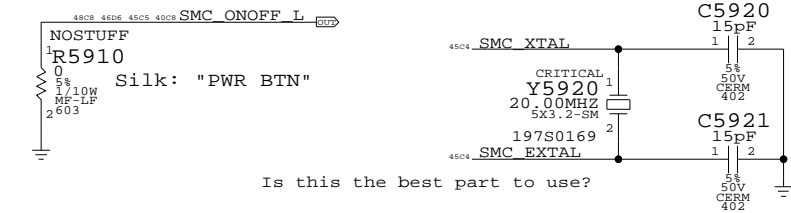
THESE NEED TO BE PULLED TO THE PROPER RAIL:



SMC 1.05V to 3.3V Level Shifting

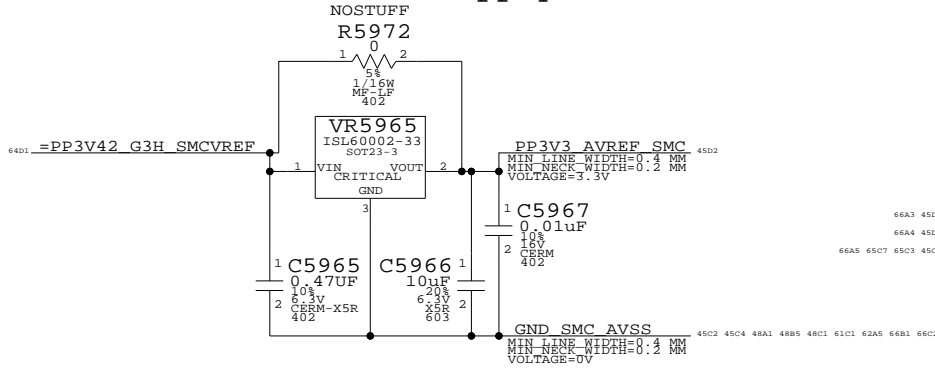


Debug Power Button SMC Crystal Circuit



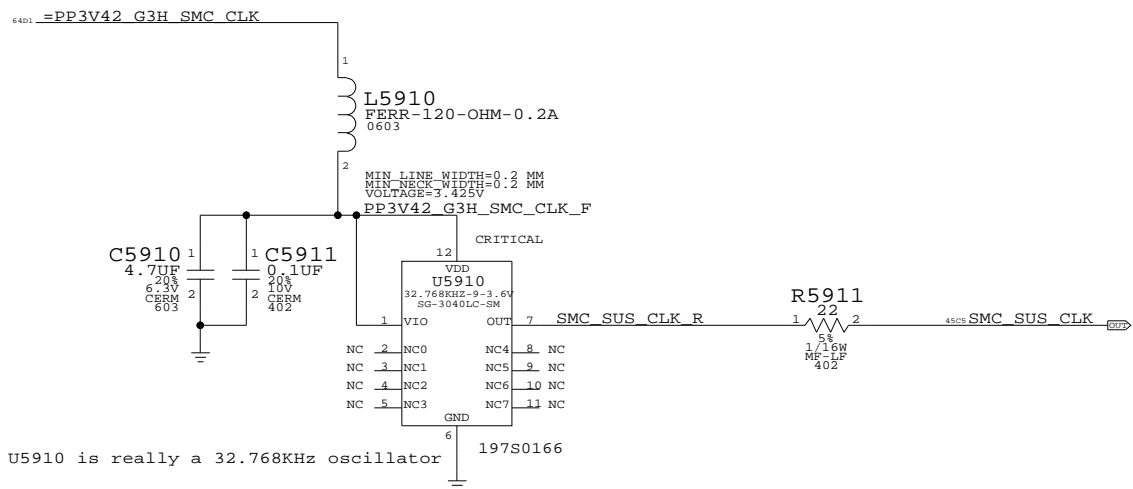
Is this the best part to use?

SMC AVREF Supply

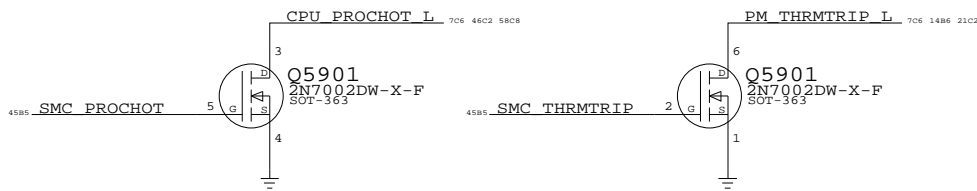


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1278	353S1381	?	VR5965	TI REF3133

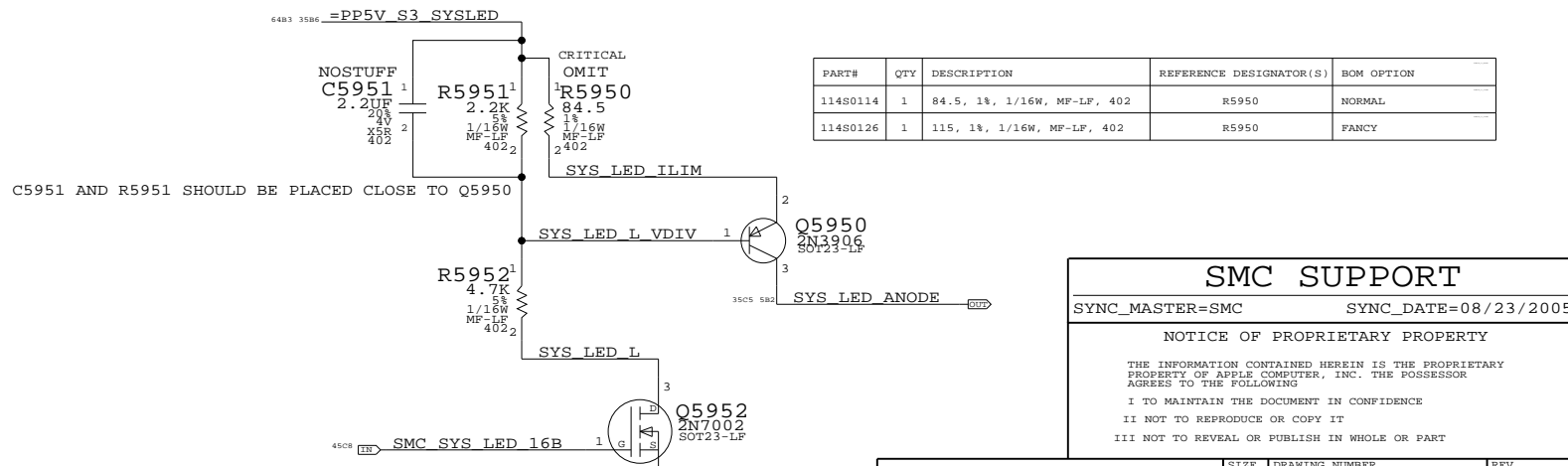
SMC G3HOT OSCILLATOR



SMC 3.3V to 1.05V Level Shifting



System (Sleep) LED Circuit



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0114	1	84.5, 1%, 1/16W, MF-LF, 402	R5950	NORMAL
114S0126	1	115, 1%, 1/16W, MF-LF, 402	R5950	FANCY

SMC SUPPORT	
SYNC_MASTER=SMC	SYNC_DATE=08/23/2005
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	SCALE NONE	SHT 46	OF 79

D

D

C

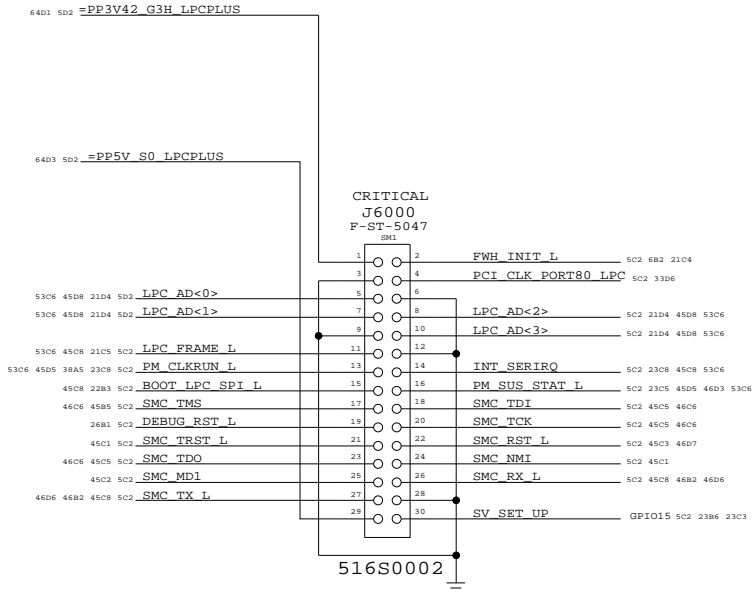
C

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A



LPC+ Debug Connector

SYNC_MASTER=NBSYNC_DATE=06/30/2005

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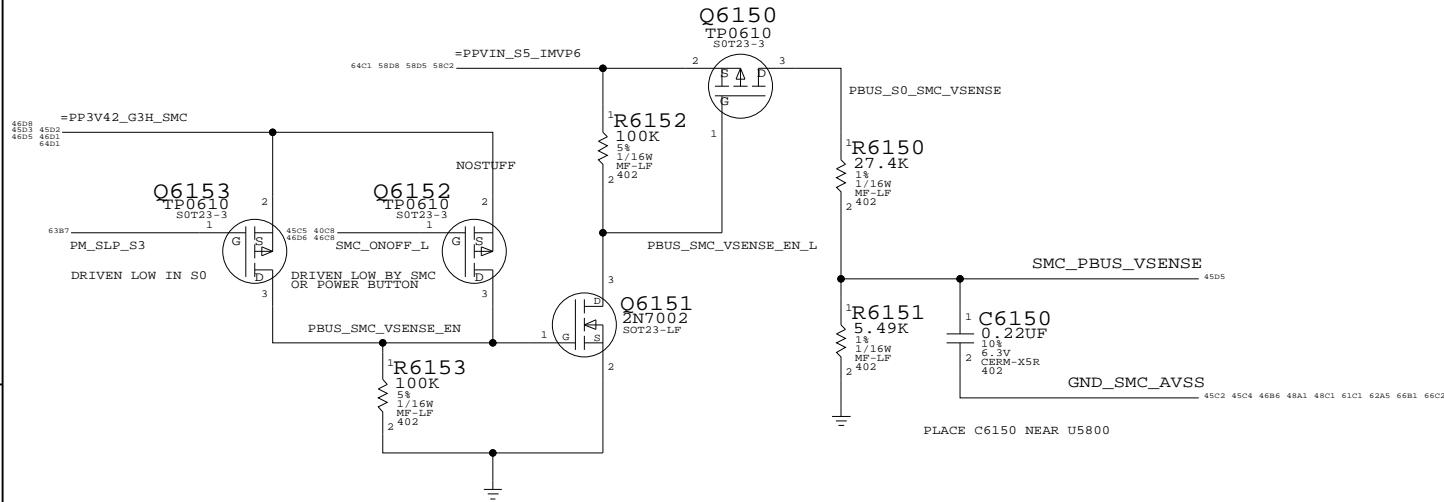
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II NOT TO REPRODUCE OR COPY IT

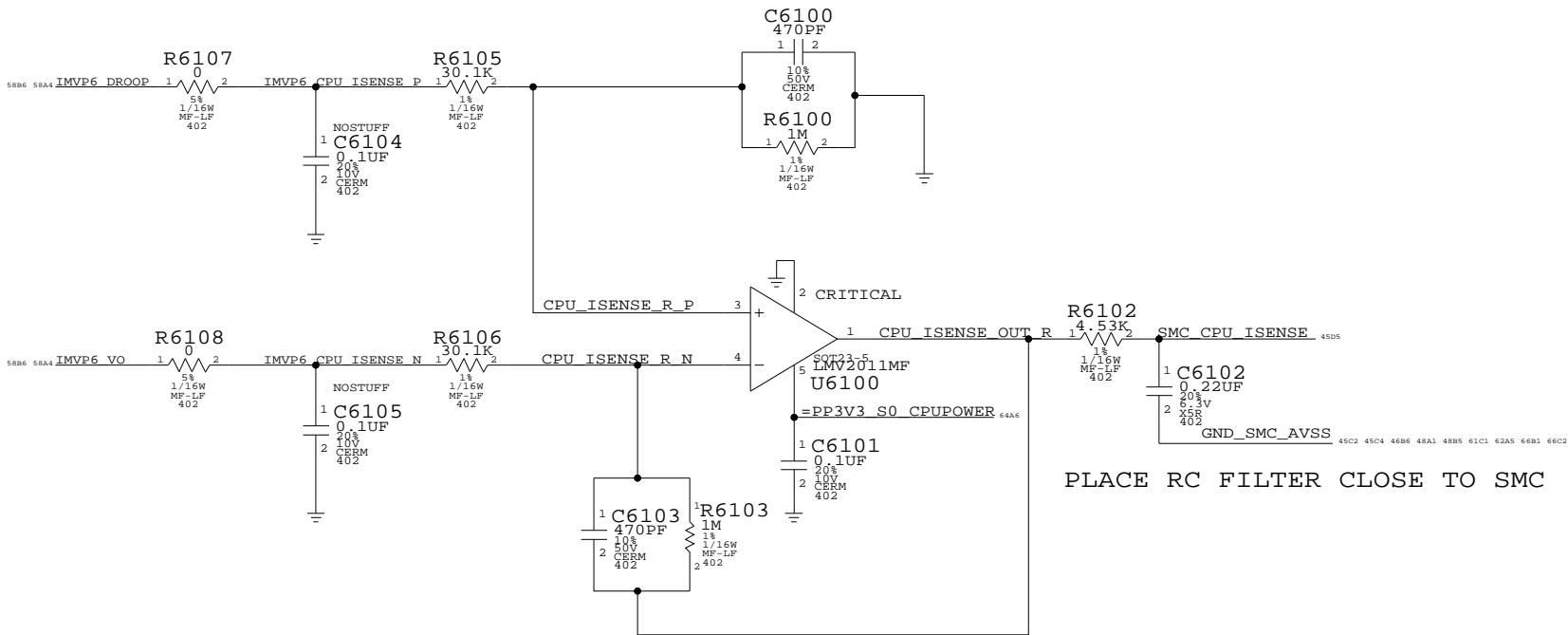
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7374	REV. A
	SCALE NONE	SHT 47	OF 79

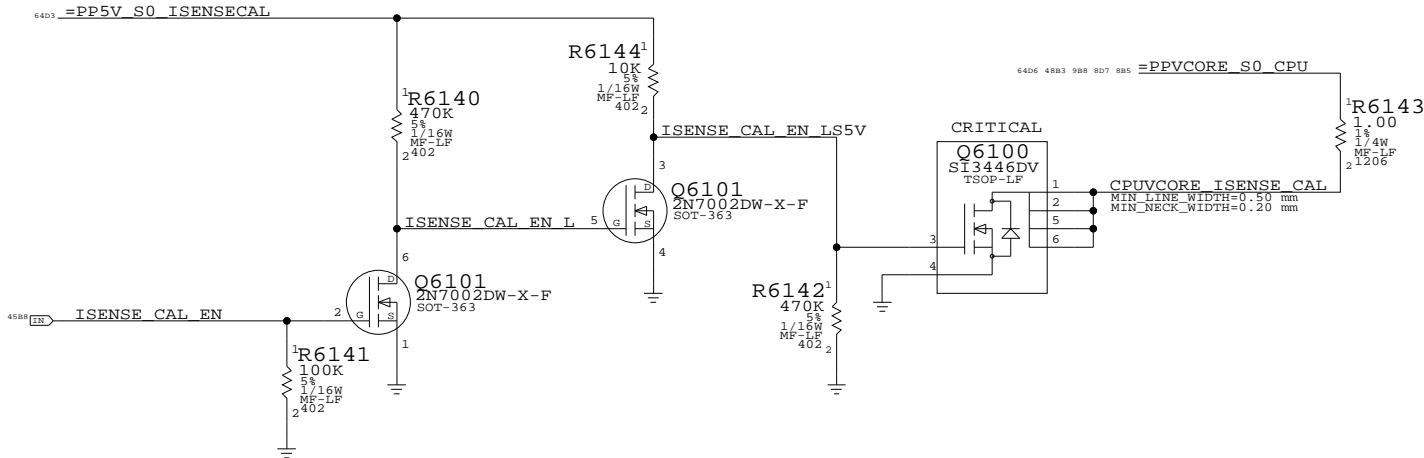
PROCESSOR DCIN VOLTAGE SENSE



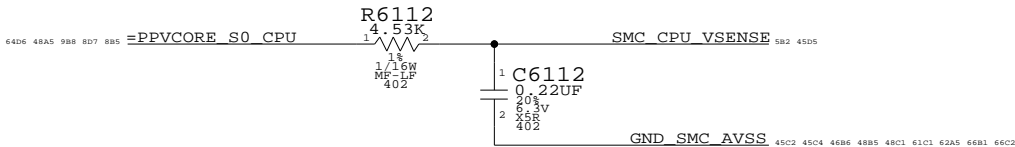
CPU CURRENT SENSE



Current Sense Calibration Circuit
Switches in fixed load on power supplies to calibrate current sense circuits



CPU VOLTAGE SENSE



CPU Current & Voltage Sense

SYNC_MASTER=ENET SYNC_DATE=08/30/2005

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SIZE

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DRAWING NUMBER

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A

SCALE

NONE

SHT

48

OF

79

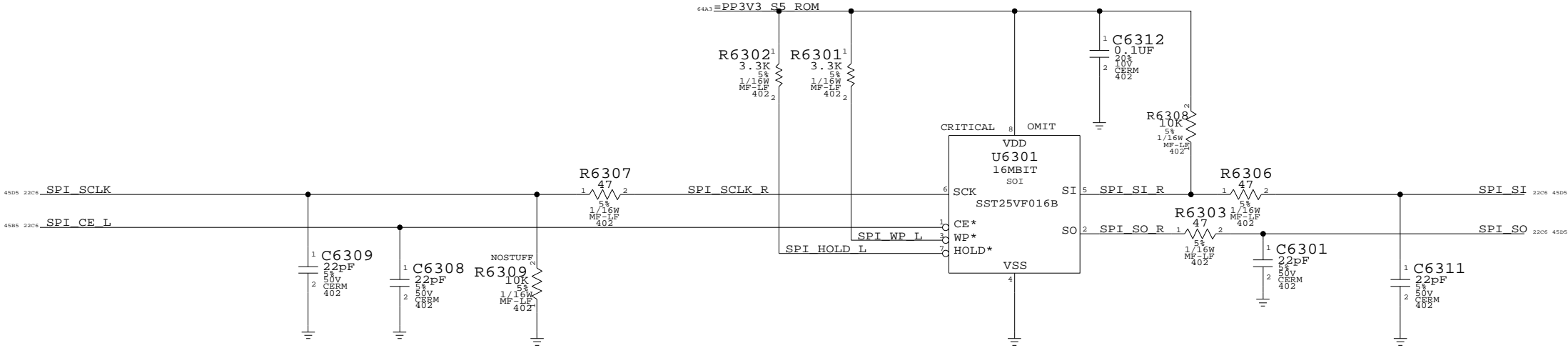
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TEMPERATURE SENSE	
SYNC_MASTER=ENET	SYNC_DATE=11/09/2005
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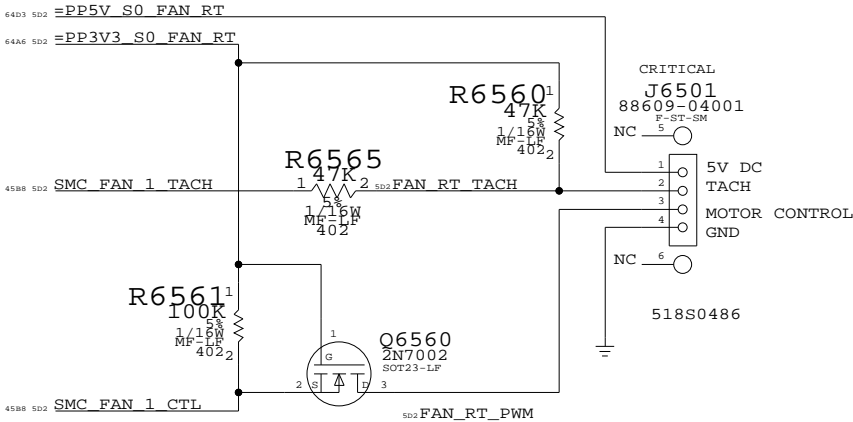
R6309 IS NOT NEEDED WHEN SHARING SPI FLASH WITH ICH7M AND TEKOA(LAN CHIP)

R6307 AND R6306 SHOULD BE PLACED LESS THAN 100 MILS FORM ICH7M
R6303 SHOULD BE PLACED LESS THAN 100 MILS FORM FLASH ROM



SPI BOOTROM		
SYNC_MASTER=MASTER		SYNC_DATE=5/23/05
NOTICE OF PROPRIETARY PROPERTY		
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7374	REV. A
	SCALE NONE	SHT 50	OF 79



Fan

SYNC_MASTER=ENET SYNC_DATE=11/10/2005

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SIZE

D

DRAWING NUMBER

051-7374

REV.

A

SCALE

NONE

SHT

51

OF

79

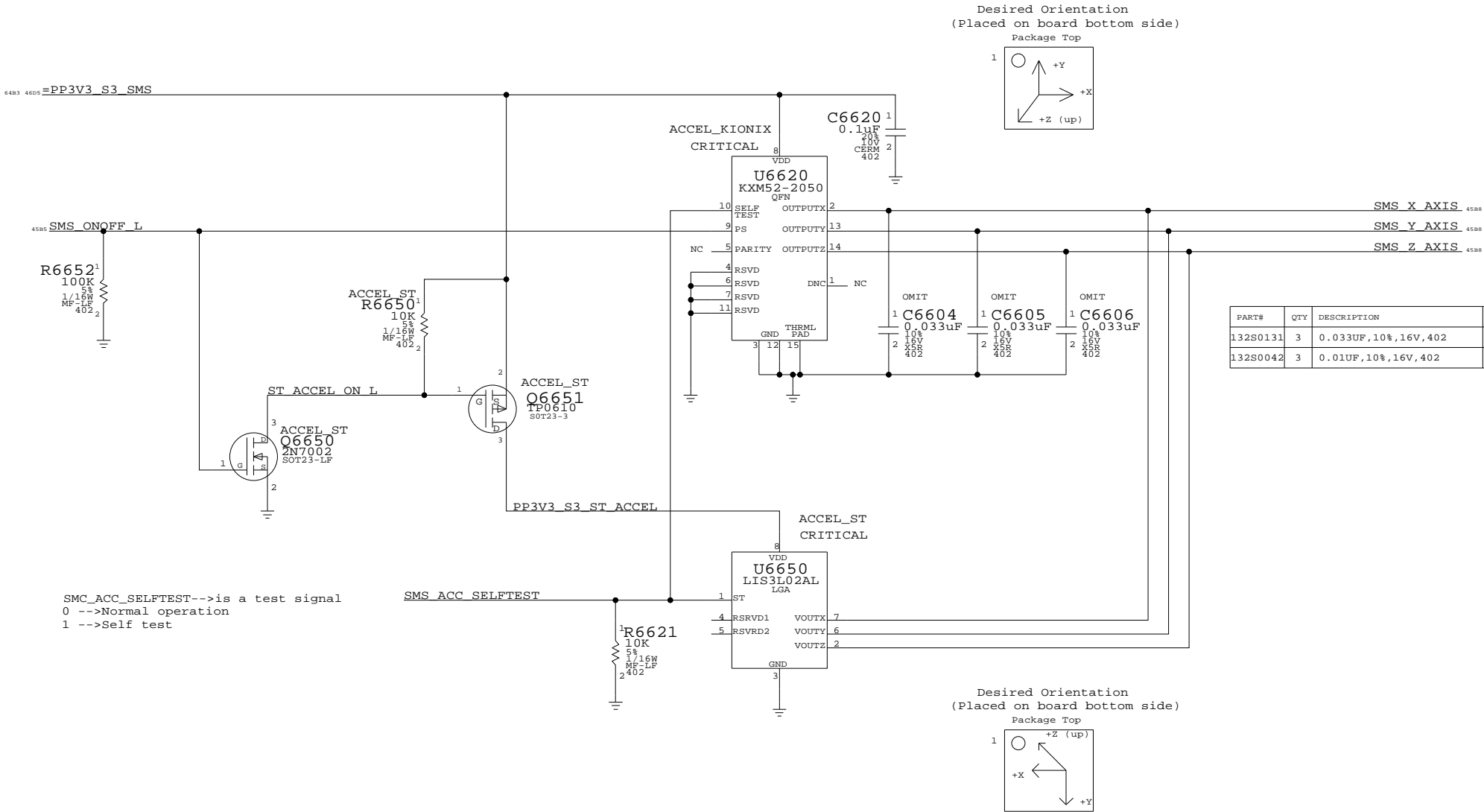
PAGE NOTES

INPUT
=PP3V3_S3_SMS - 3.3V POWER FOR SMS (STAYS ALIVE IN SLEEP)
SMS_ONOFF_L - CONNECT TO SMC TO BE ABLE TO PUT SMS INTO LOW-POWER MODE

OUTPUT
SMS_ACC_*_AXIS - ACCELEROMETER OUTPUT TO SCU

PAGE HISTORY

5/19/2005 - FIRST REVISION OF PAGE
7/26/2005 - REMOVED BOM TABLE AND UPDATED SYMBOL TO KXM52-2050
7/26/2005 - CONNECTED PD PIN TO SMC'S SMS_ONOFF_L



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
132S0131	3	0.033UF,10%,16V,402	C6604,C6605,C6606		ACCEL_KIONIX
132S0042	3	0.01UF,10%,16V,402	C6604,C6605,C6606		ACCEL_ST

SMS

SYNC_MASTER=SMC

SYNC_DATE=08/23/2005

NOTICE OF PROPRIETARY PROPERTY

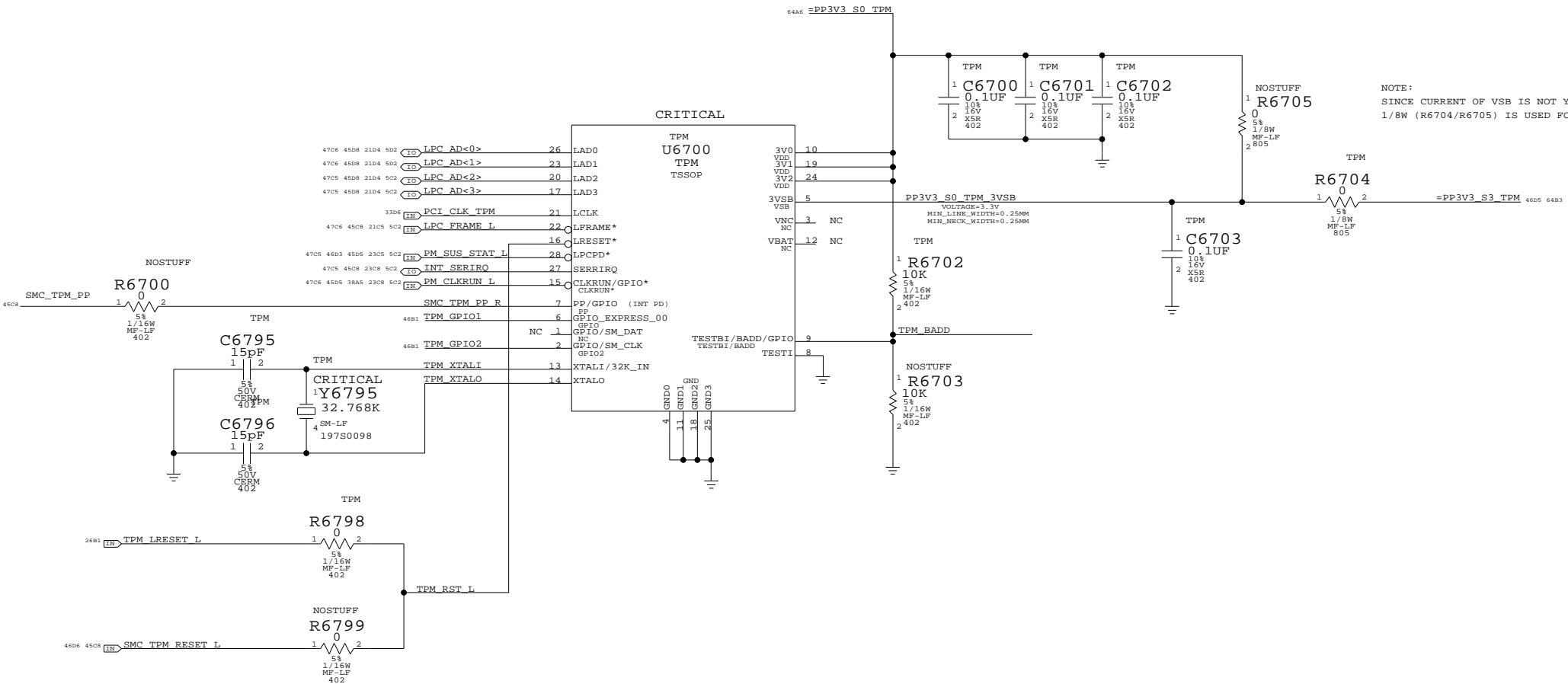
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7374	REV. A
	SCALE NONE	SHT 52	OF 79



TPM

SYNC_MASTER=SMC

SYNC_DATE=07/18/2005

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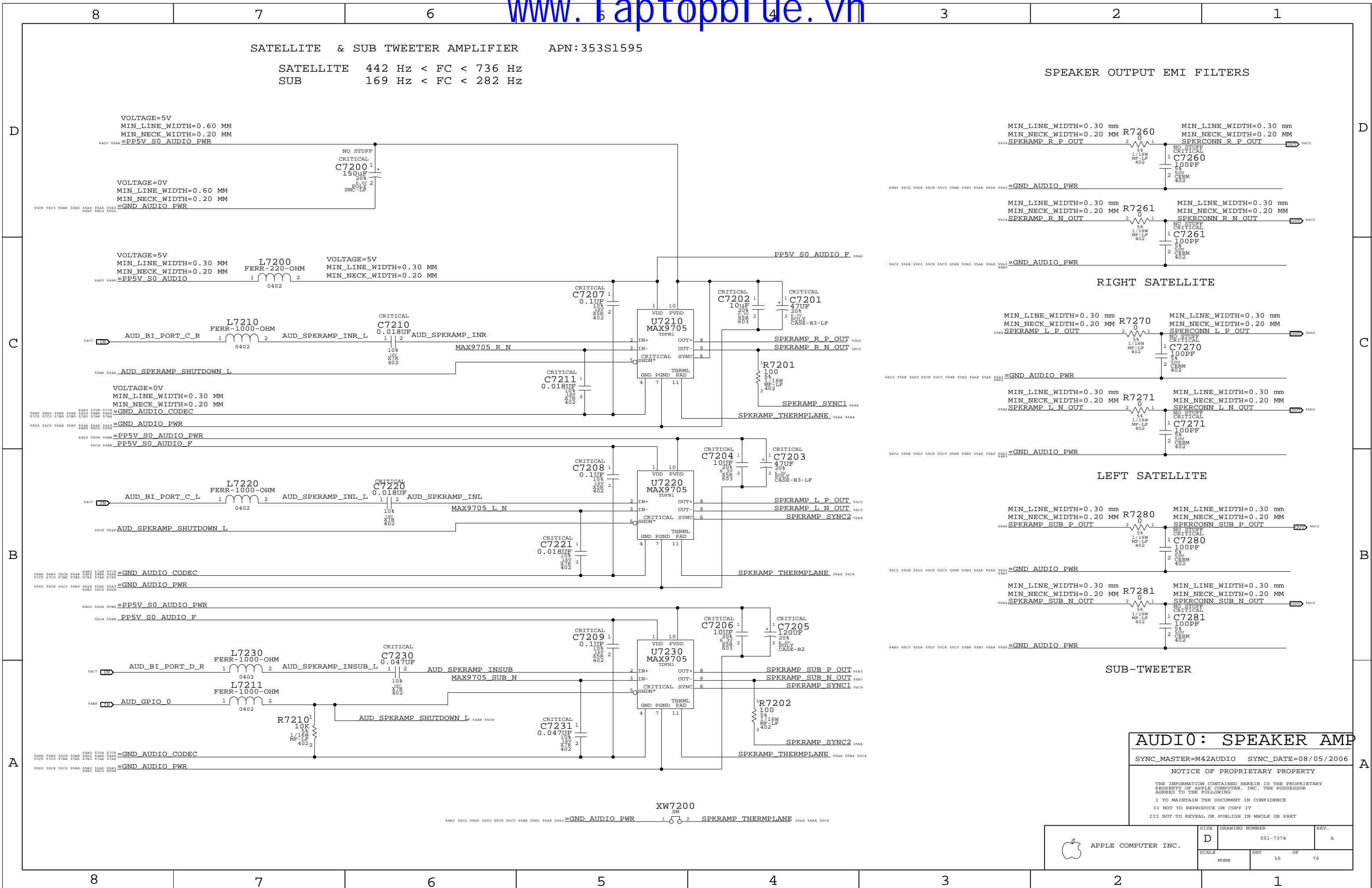
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7374	A
SCALE		SHT	OF
NONE		53	79



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
518S0491	518S0332	?	J7302	IMPROVED TWO PIN CONNECTOR

MIC CONNECTOR
APN:514S0392

56B1 MIC LO CONN
56B1 MIC HI CONN
56B1 MIC SHLD CONN

CRITICAL
J7301
48227-0301
M-RT-SM1
4

SPEAKER CONNECTOR
APN:518S0332

55C1 SPKRCONN L P OUT
55C1 SPKRCONN L N OUT

CRITICAL
J7302
88611-02001
F-ST-SM
3

NO STUFF
R7380

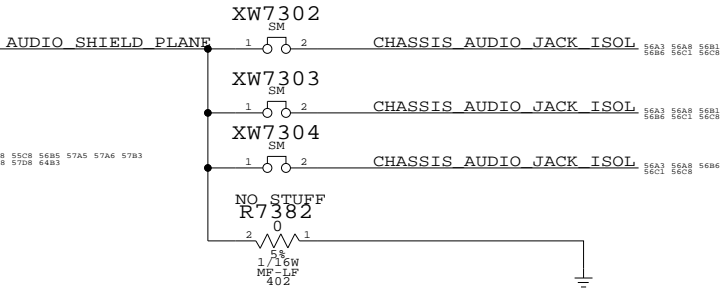
64B3 55D8 55D3 55C8 55C3 55B8 55B3 55A8 55A5 55A1 =GND AUDIO_PWR

CRITICAL
J7303
88609-04001
F-ST-SM
5

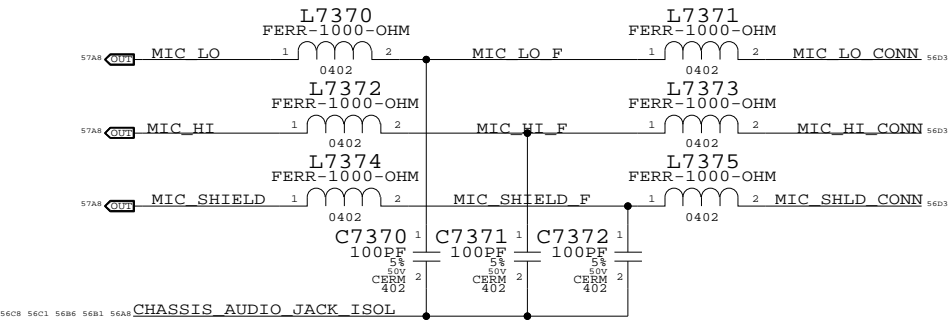
55B1 SPKRCONN SUB P OUT
55B1 SPKRCONN SUB N OUT
55D1 SPKRCONN R P OUT
55C1 SPKRCONN R N OUT

REPLACE 518S0334 WITH 518S0486

AUDIO SHIELD FILL



MIC EMI FILTER



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0290	1	CONN, 3.5MM COMBO AUDIO OUT, RA, MG3, LF	J7300	CRITICAL	NORMAL
514-0291	1	CONN, 3.5MM COMBO AUDIO IN, RA, MG3, LF	J7350	CRITICAL	NORMAL
514-0317	1	CONN, 3.5MM COMBO AUDIO OUT, RA, BLACK, LF	J7300	CRITICAL	FANCY
514-0318	1	CONN, 3.5MM COMBO AUDIO IN, RA, BLACK, LF	J7350	CRITICAL	FANCY

AUDIO: JACK

SYNC_MASTER=M42AUDIO SYNC_DATE=08/05/2006

NOTICE OF PROPRIETARY PROPERTY

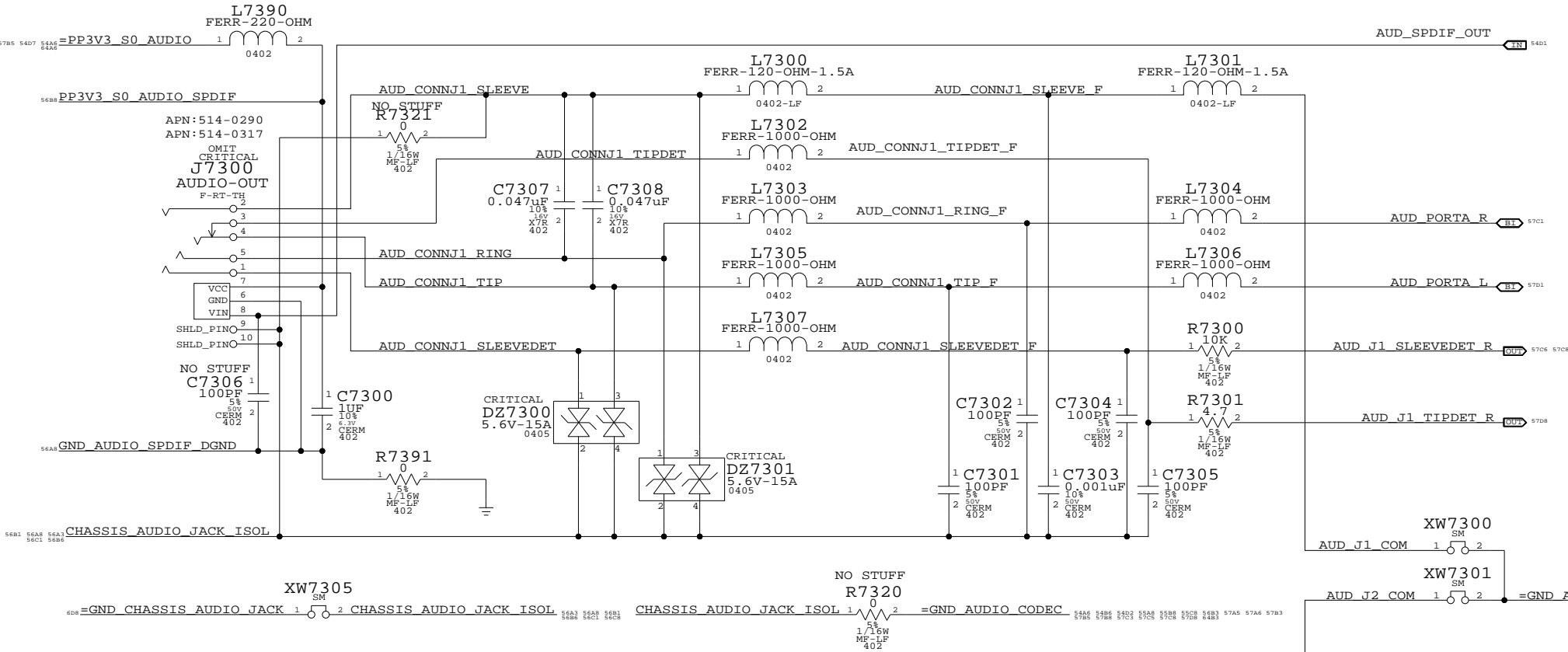
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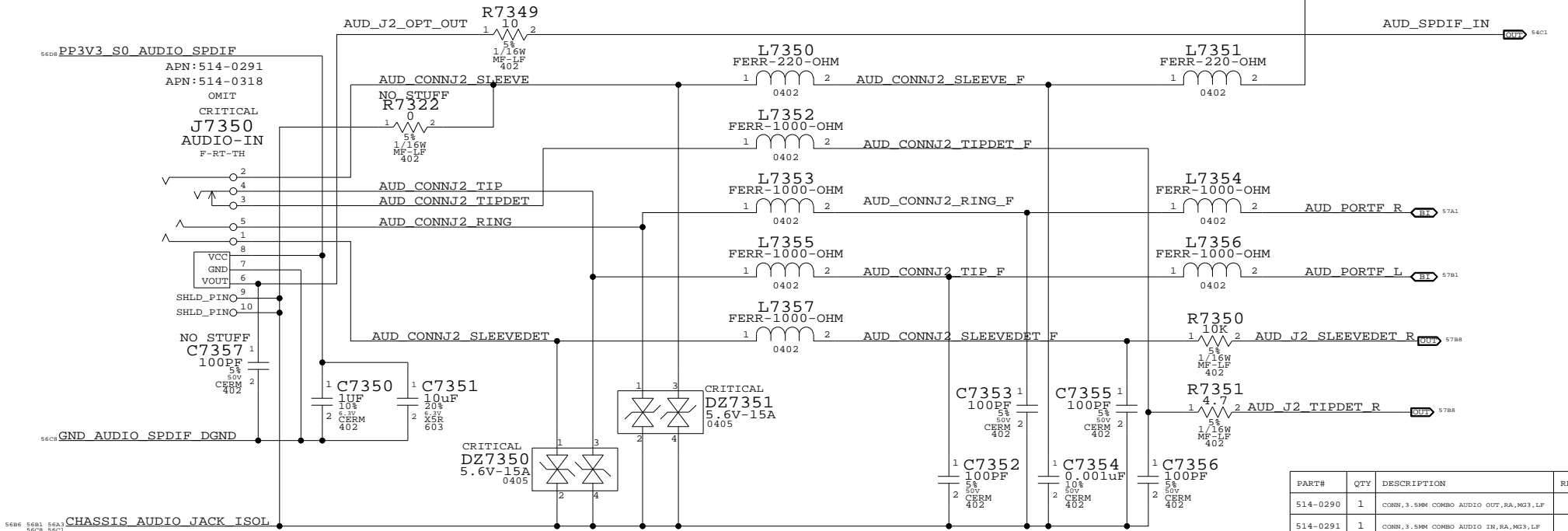
APPLE COMPUTER INC.

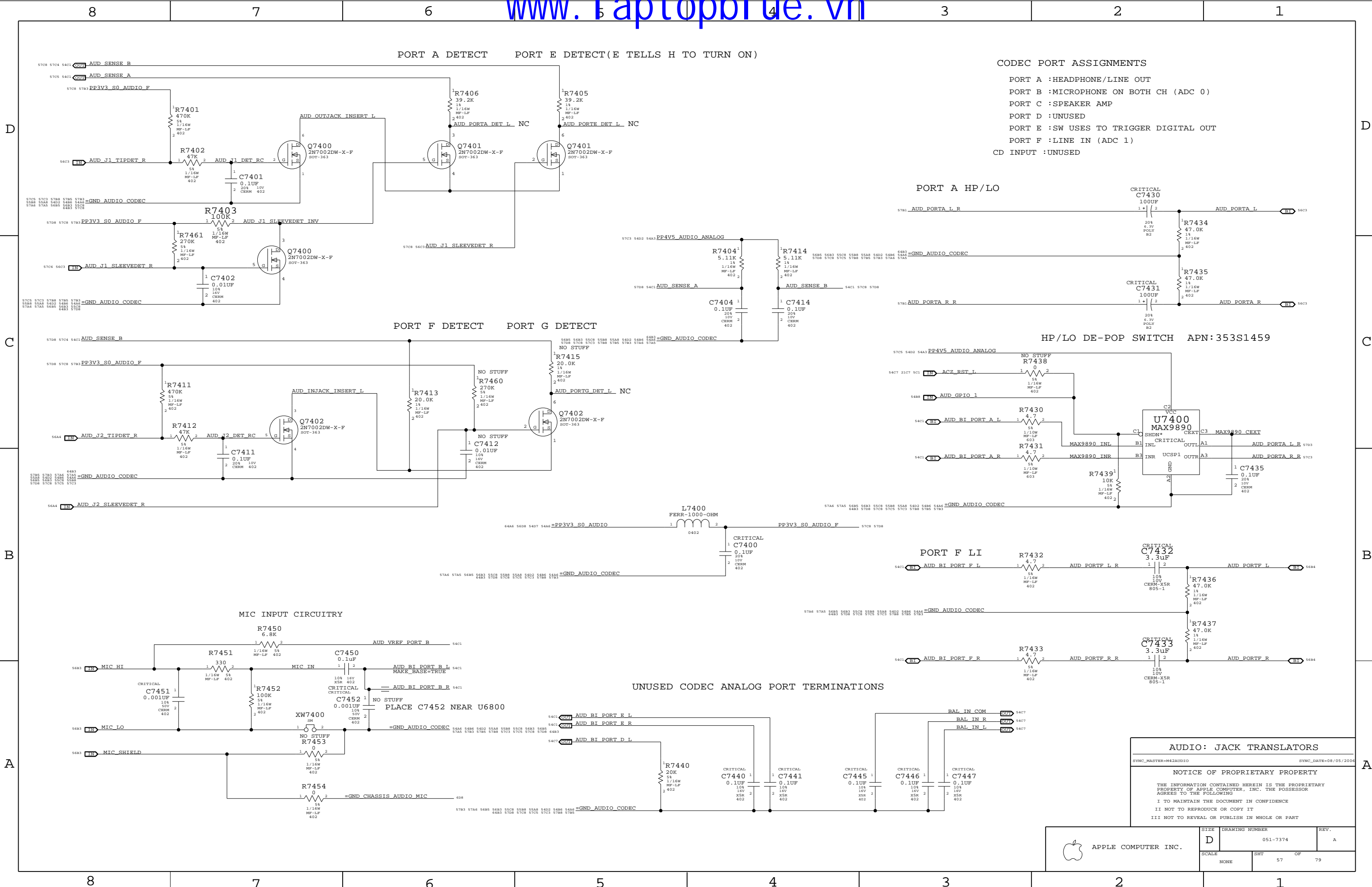
SIZE	DRAWING NUMBER	REV.
D	051-7374	A
SCALE	SHT	OF
NONE	56	79

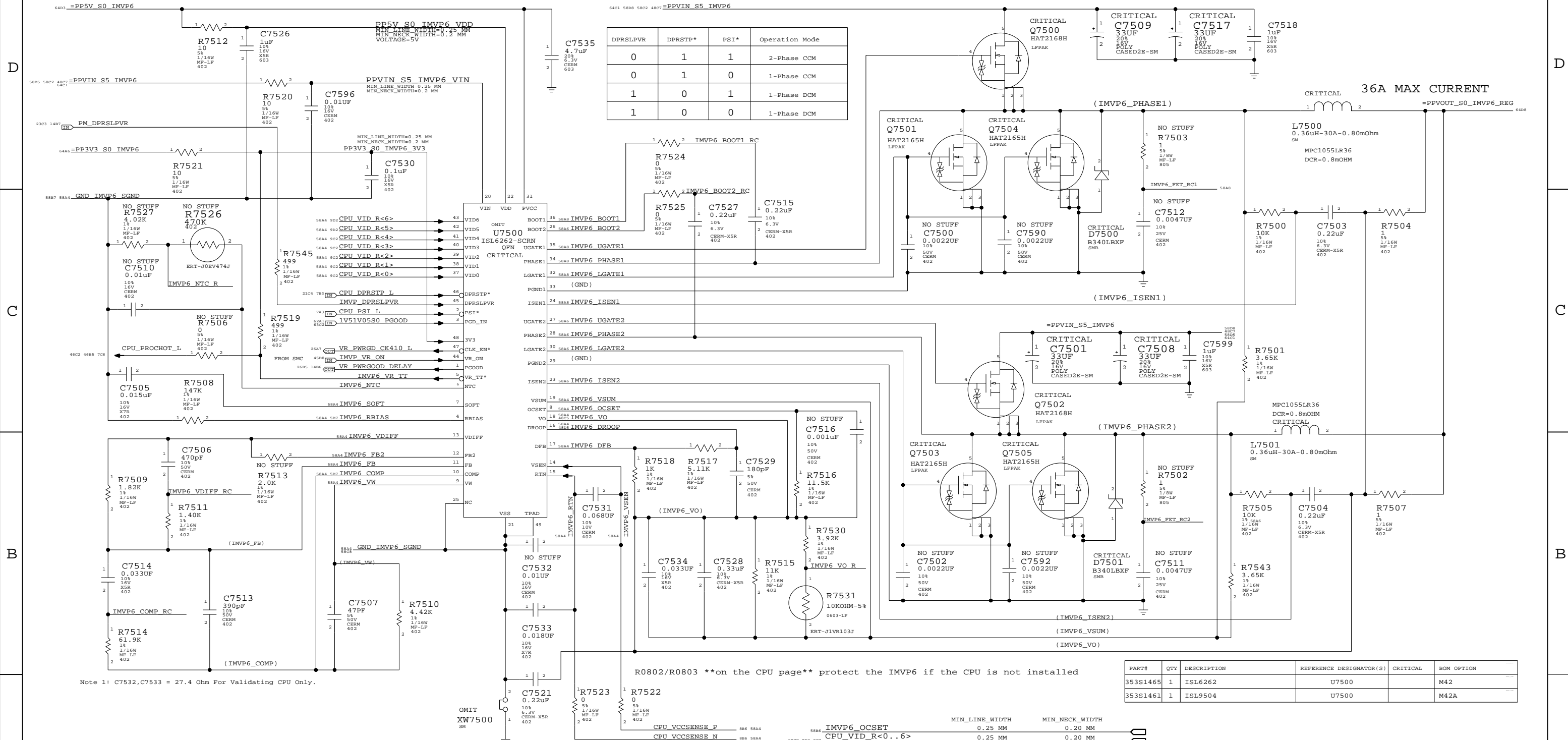
AUDIO JACK 1: LO/HP CONNECTOR, SPDIF TX



AUDIO JACK 2: LINE IN CONNECTOR, SPDIF RX







Note 1: C7532,C7533 = 27.4 Ohm For Validating CPU Only.

R0802/R0803 **on the CPU page** protect the IMVP6 if the CPU is not installed

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S1465	1	ISL6262	U7500		M42
353S1461	1	ISL9504	U7500		M42A

IMVP6 CPU VCore Regulator			
5808	5887	GND_IMVP6_SGND	0.50 MM 0.20 MM
5886	48C5	IMVP6_VO	0.25 MM 0.20 MM
5886	48D9	IMVP6_DROOP	0.25 MM 0.20 MM
		TMVP6_DRP	0.25 MM 0.20 MM

[illegible][illegible]

IMVP6 CPU VCore Regulator

Electrical Connections:

- SW7500
- 6.3V VCORE
- CSRM-XSR 402
- NP-LP 402
- NP-LP 402
- CPU_VCCSENSE_P 8B6 58A4
- CPU_VCCSENSE_N 8B6 58A4

Pinout:

Pin	Signal	MIN_LINE_WIDTH	MIN_NECK_WIDTH
5886	IMVP6_OCSET	0.25 MM	0.20 MM
58C7 9D2 9C2	CPU_VID_R<0..6>	0.25 MM	0.20 MM
58C6	IMVP6_VSUM	0.25 MM	0.20 MM
58C8 58B7	GND_IMVP6_SGND	0.50 MM	0.20 MM
58B6 48C5	IMVP6_VO	0.25 MM	0.20 MM
58B6 48C5	IMVP6_DROOP	0.25 MM	0.20 MM
58B6 48C5	IMVP6_DFB	0.25 MM	0.20 MM
58C7	IMVP6_SOFT	0.25 MM	0.20 MM
58B7 5D7	IMVP6_RBIA5	0.25 MM	0.20 MM
58B7	IMVP6_VDIFF	0.25 MM	0.20 MM
58B7	IMVP6_FB2	0.25 MM	0.20 MM
58B7	IMVP6_FB	0.25 MM	0.20 MM
58B7 5D7	IMVP6_COMP	0.25 MM	0.20 MM
58B7	IMVP6_VW	0.25 MM	0.25 MM
58A5 8B6	CPU_VCCSENSE_P	0.25 MM	0.25 MM
58A5 8B6	CPU_VCCSENSE_N	0.25 MM	0.25 MM
58B6	IMVP6_RTN	0.25 MM	0.25 MM
58B5	IMVP6_VSEN	0.25 MM	0.25 MM

Regulatory Information:

IMVP6 CPU VCore Regulator

SYNC_MASTER=POWER SYNC_DATE=07/13/2005

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SIZE: D DRAWING NUMBER: 051-7374 REV: A

TMVP6 CPU VCore Regulator			
SR06 480V	TMVP6_VO	0.25 MM	0.20 MM
SR06 480V	TMVP6_DROOP	0.25 MM	0.20 MM

IMVP6 CPU VCore Regulator

58C7	IMVP6_BIAS	0.25 MM	0.20 MM	
58C7	IMVP6_RBIAS	0.25 MM	0.20 MM	
				NOTICE OF PROPRIETARY PROPERTY

[illegible]

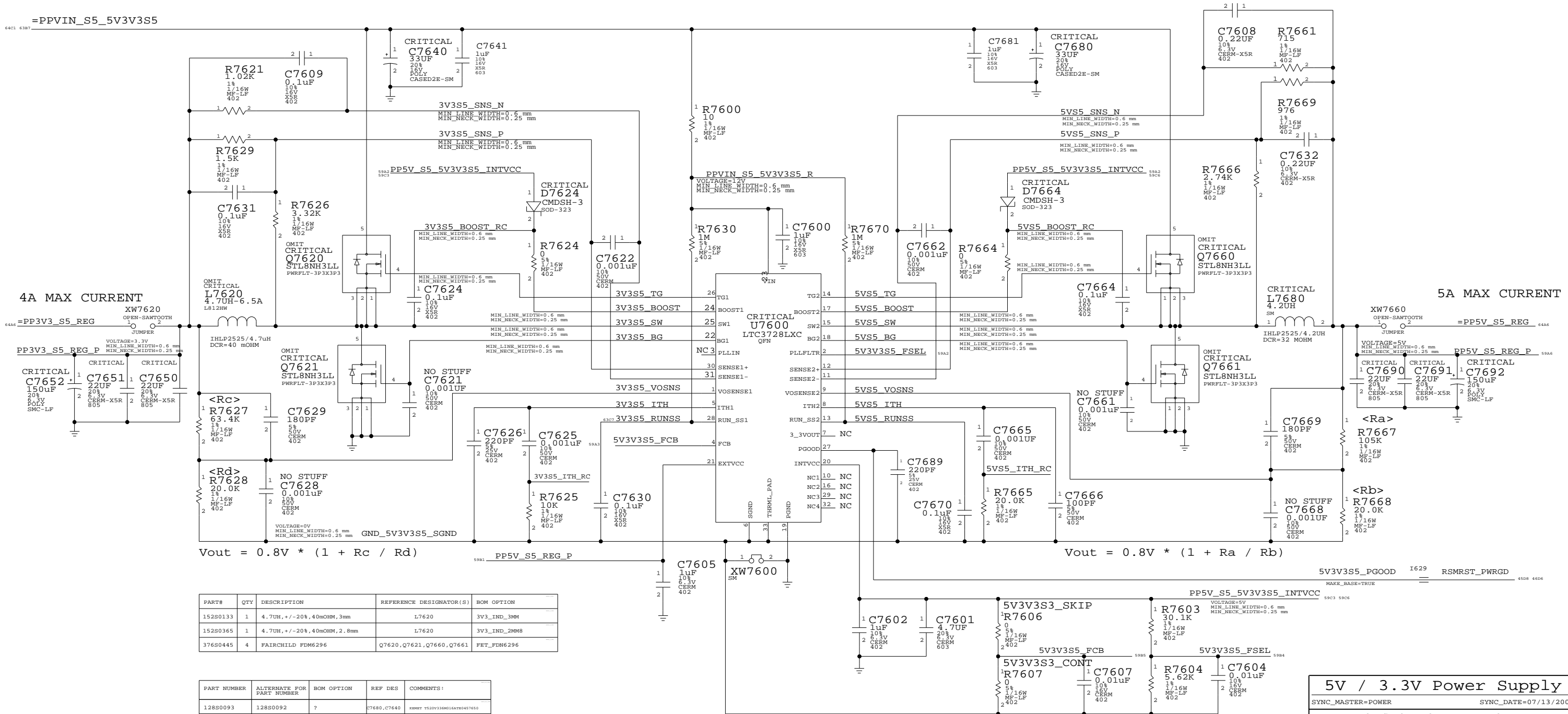
S8C6	IMVP6_FET_RC1	0.25 MM	0.25 MM		S8C7	IMVP6_FET_RC2	0.25 MM	0.25 MM		S8AS S8V	CPU_VCCSENSE_N	0.25 MM	0.25 MM	
S8C2	IMVP6_VSUM_R1	0.25 MM	0.25 MM		S8B2	IMVP6_VSUM_R2	0.25 MM	0.25 MM		S8AS S8V	IMVP6_RTN	0.25 MM	0.25 MM	
	IMVP6_VO_R1	0.25 MM	0.25 MM			IMVP6_VO_R2	0.25 MM	0.25 MM		S8B6	IMVP6_VSEN	0.25 MM	0.25 MM	

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7374	A

SCALE	SHT	OF	TOTAL
NONE	58	79	

5V/3.3V POWER SUPPLY



5V / 3.3V Power Supply

SYNC_MASTER=POWER SYNC_DATE=07/13/2005

NOTICE OF PROPRIETARY PROPERTY

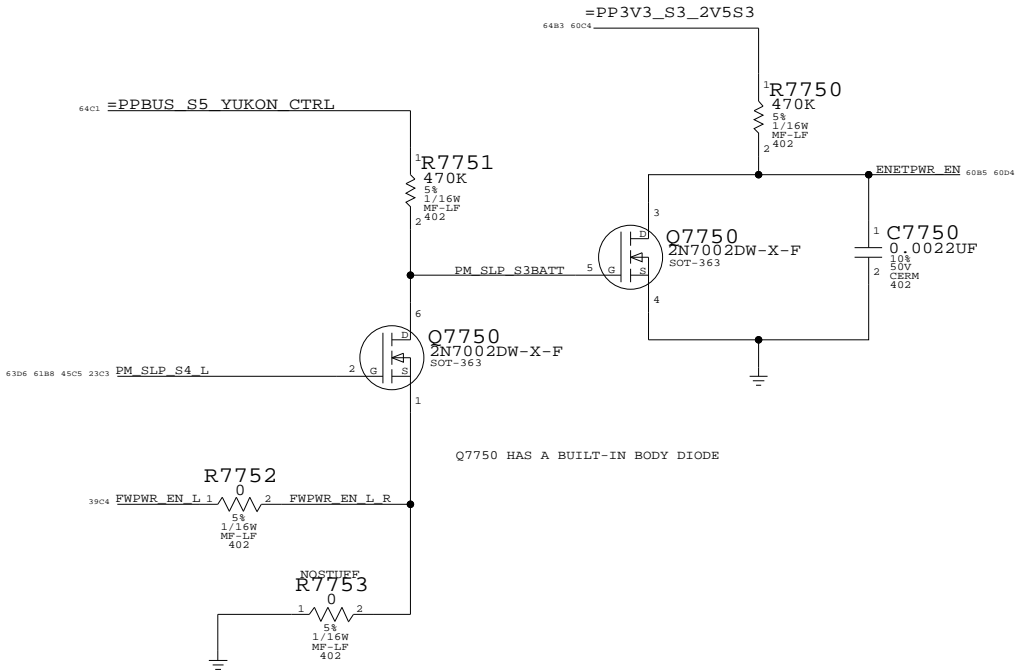
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YUKON POWER CONTROL

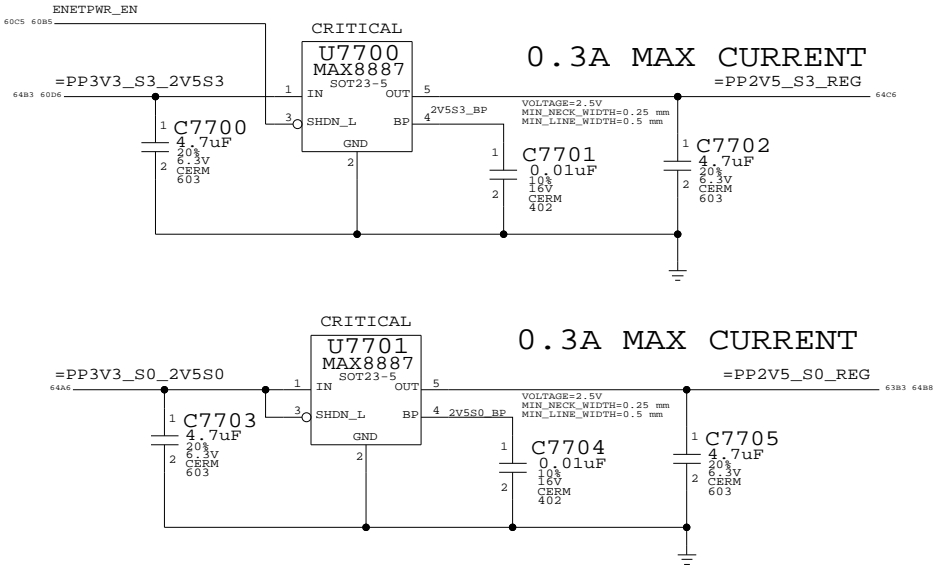


NAME	PM_SLP_S4_L	FWPWR_EN_L	PM_SLP_S3BATT	ENETPWR_EN
LOGIC	S3 S0	~S0 ~SMC_PS_ON		POWER YUKON
S3 ON BATTERY	TRUE (3.3V)	TRUE (PBUS 12.6V)	TRUE (PBUS 12.6V)	FALSE (0V)
S0 OR S3 ON AC	TRUE (3.3V)	FALSE (0V)	FALSE (0V)	TRUE (3.3V)
S5 ON AC	FALSE (0V)	TRUE (PBUS 12.6V)	TRUE (PBUS 12.6V)	FALSE (0V)
S5 ON BATT	FALSE (0V)	FALSE (0V)	TRUE (PBUS 12.6V)	FALSE (0V)

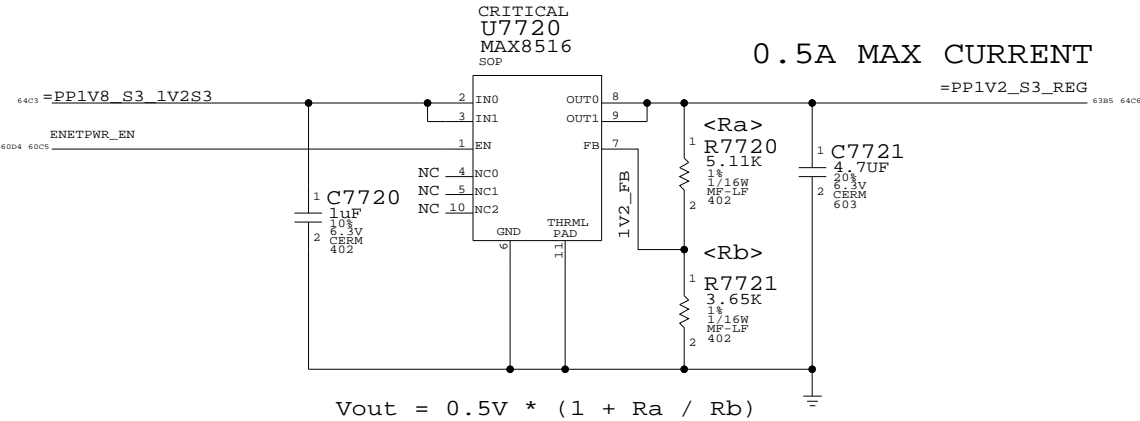
NOTE: IF CHANGE TO STUFFING R7753 THEN ENETPWR_EN IS BUFFERED PM_SLP_S4_L



2.5V REGULATORS



1.2V REGULATOR



2.5V/1.2V Regulator

SYNC_MASTER=ENET

SYNC_DATE=12/06/2005

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APPLE COMPUTER INC.

SIZE

D

DRAWING NUMBER

051-7374

REV.

A

SCALE

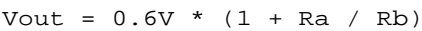
NONE

SHT

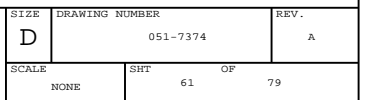
60

OF

79



1.8V Supply	
SYNC_MASTER=POWER	SYNC_DATE=07/13/2005
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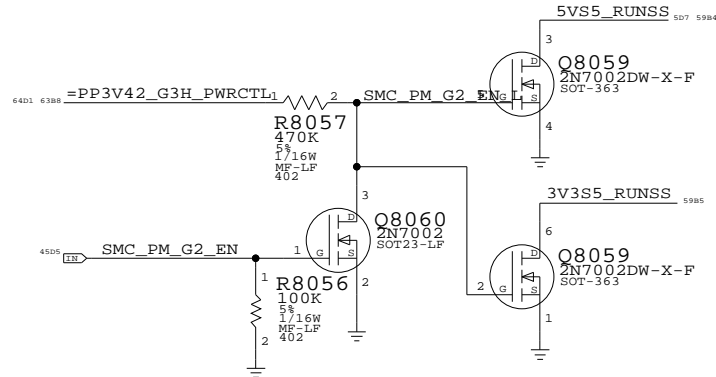


POWER CONTROL SIGNALS

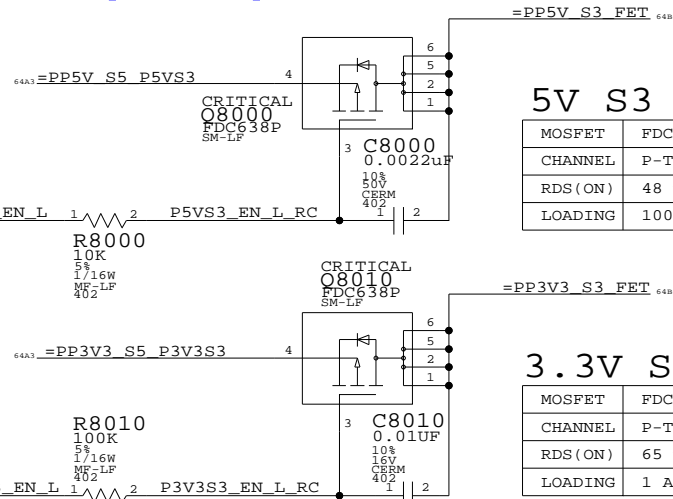
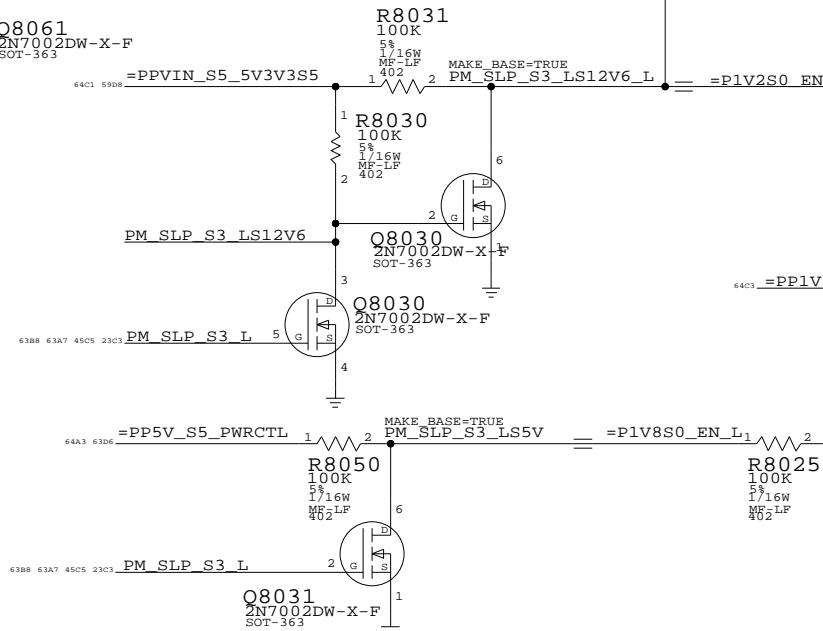
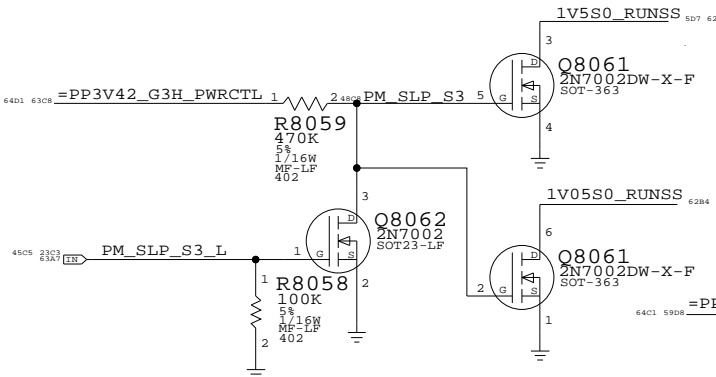
These rails are monitored by LTC2908

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

5V/3.3V S5 RUN/SS CONTROL

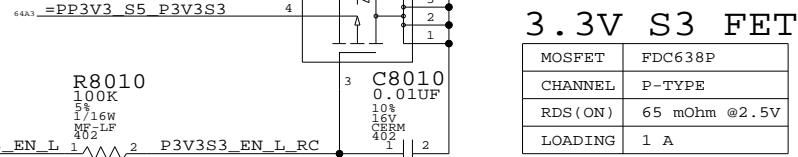


1.5V/1.05V S0 RUN/SS CONTROL



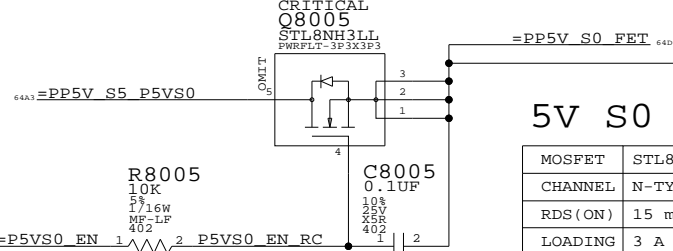
5V S3 FET

MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	100 mA



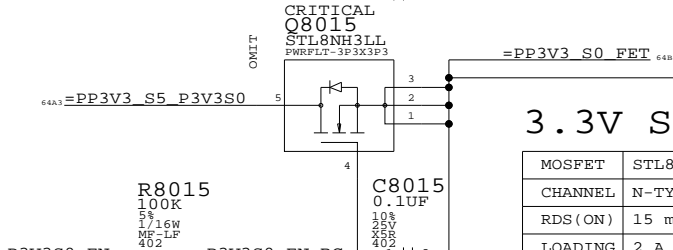
3.3V S3 FET

MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	65 mOhm @2.5V
LOADING	1 A



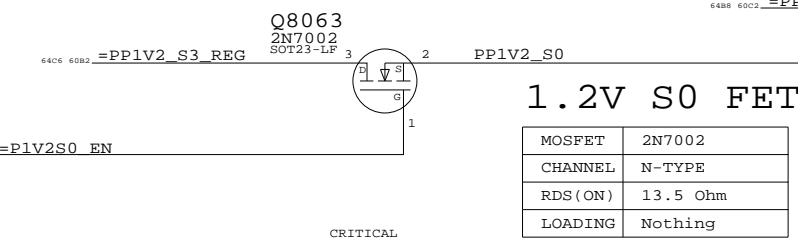
5V S0 FET

MOSFET	STL8NH3LL
CHANNEL	N-TYPE
RDS(ON)	15 mOhm @10V
LOADING	3 A



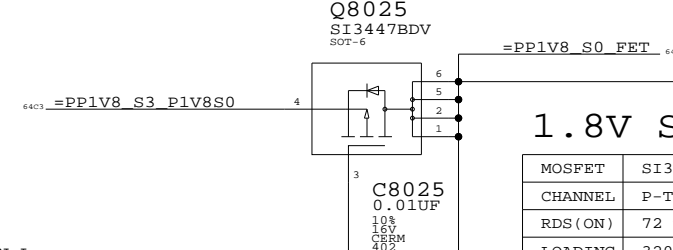
3.3V S0 FET

MOSFET	STL8NH3LL
CHANNEL	N-TYPE
RDS(ON)	15 mOhm @10V
LOADING	2 A



1.2V S0 FET

MOSFET	2N7002
CHANNEL	N-TYPE
RDS(ON)	13.5 Ohm
LOADING	Nothing

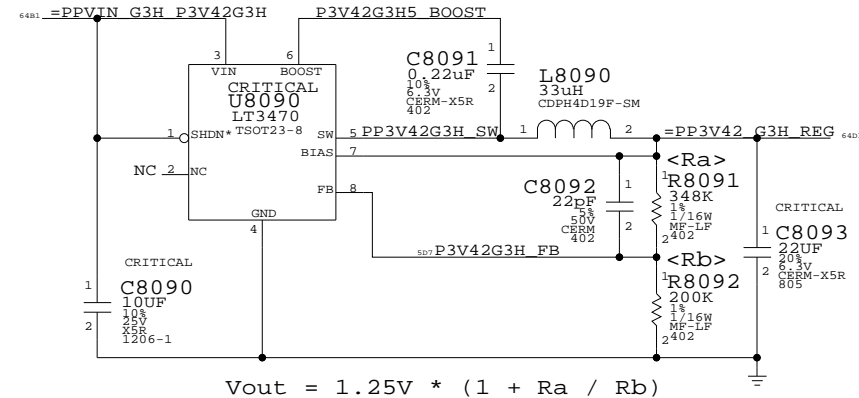


1.8V S0 FET

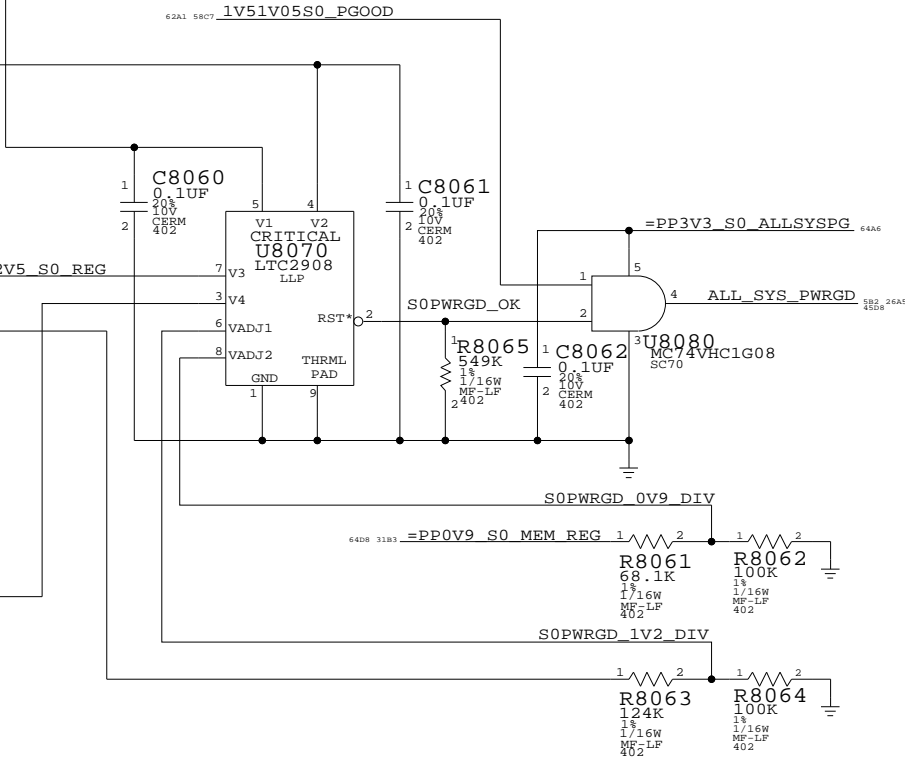
MOSFET	SI3447BDV
CHANNEL	P-TYPE
RDS(ON)	72 mOhm @1.8V
LOADING	320 mA

3.425V "G3Hot" SUPPLY

Supply needs to guarantee 3.31V delivered to SMC VRef generator



ALL SYSTEM PWRGD CIRCUIT



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
376S0445	2	FAIRCHILD FDM6296	Q8005,Q8015	FET_FDM6296

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0448	376S0445	?	Q8005,Q8015	VISHAY SI7806ADN

S3/S0 FETS, G3H SUPPLY

SYNC_MASTER=ENET SYNC_DATE=08/30/2005

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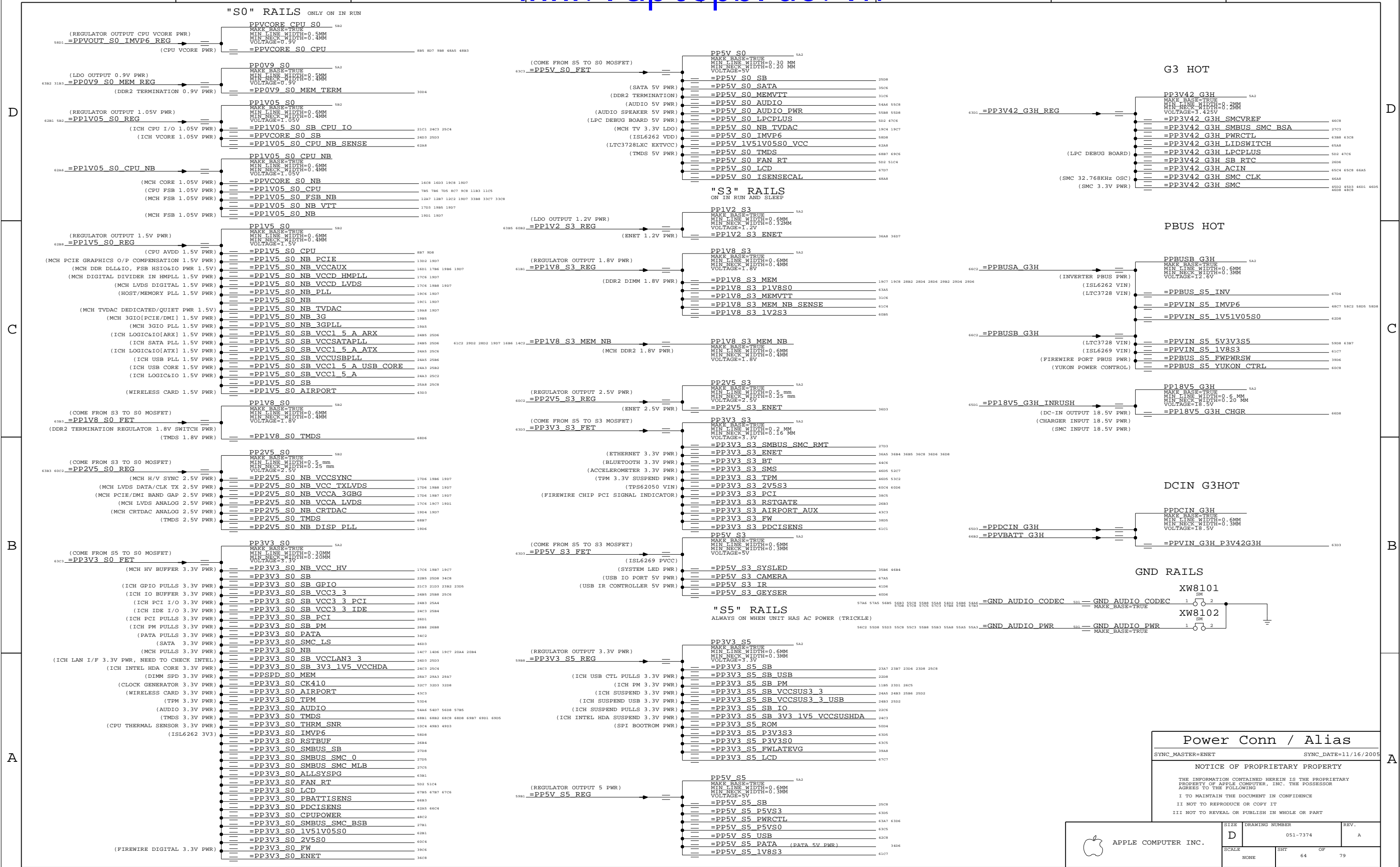
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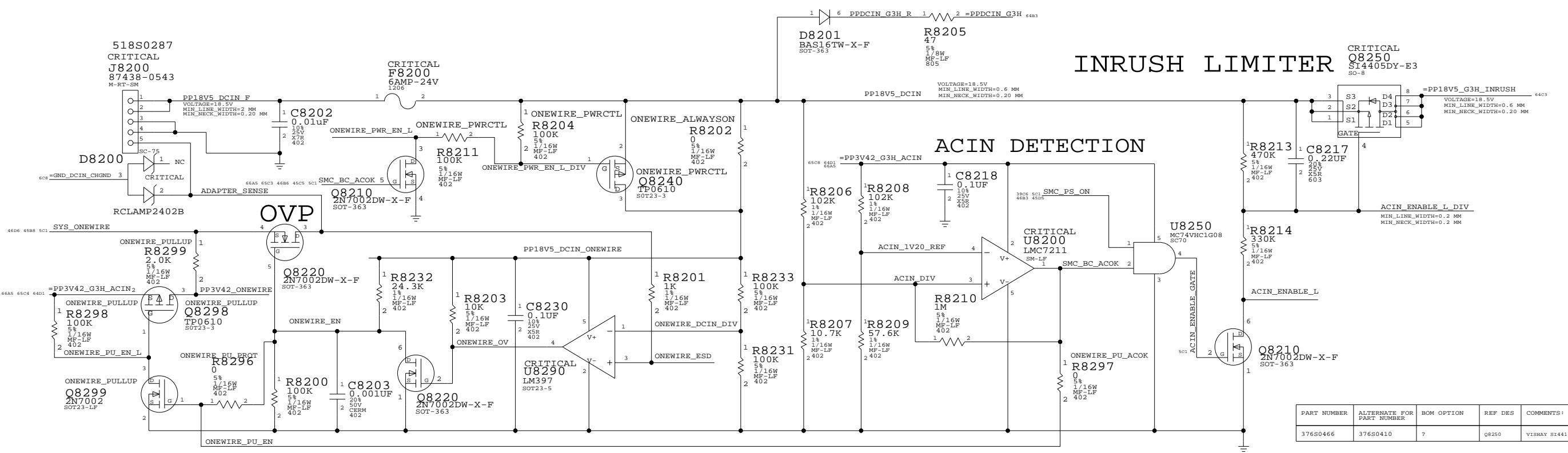
APPLE COMPUTER INC.

SIZE D DRAWING NUMBER 051-7374 REV. A

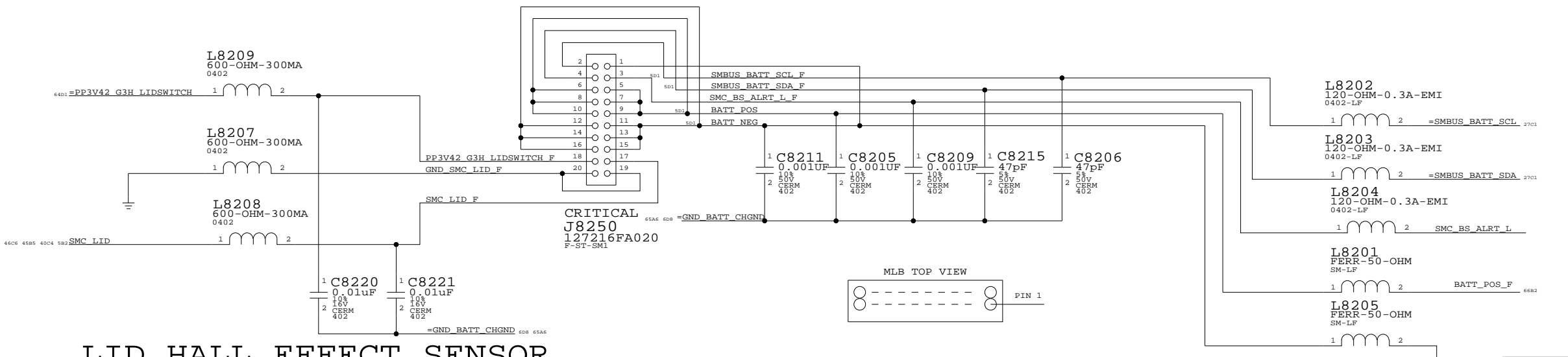
SCALE NONE SHT 63 OF 79



DC-JACK INTERFACE



BATTERY INTERFACE



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0466	376S0410	7	Q8250	VISHAY SI4413ADY

DC-In & Battery Connectors
SYNC_MASTER=POWER SYNC_DATE=07/13/2005

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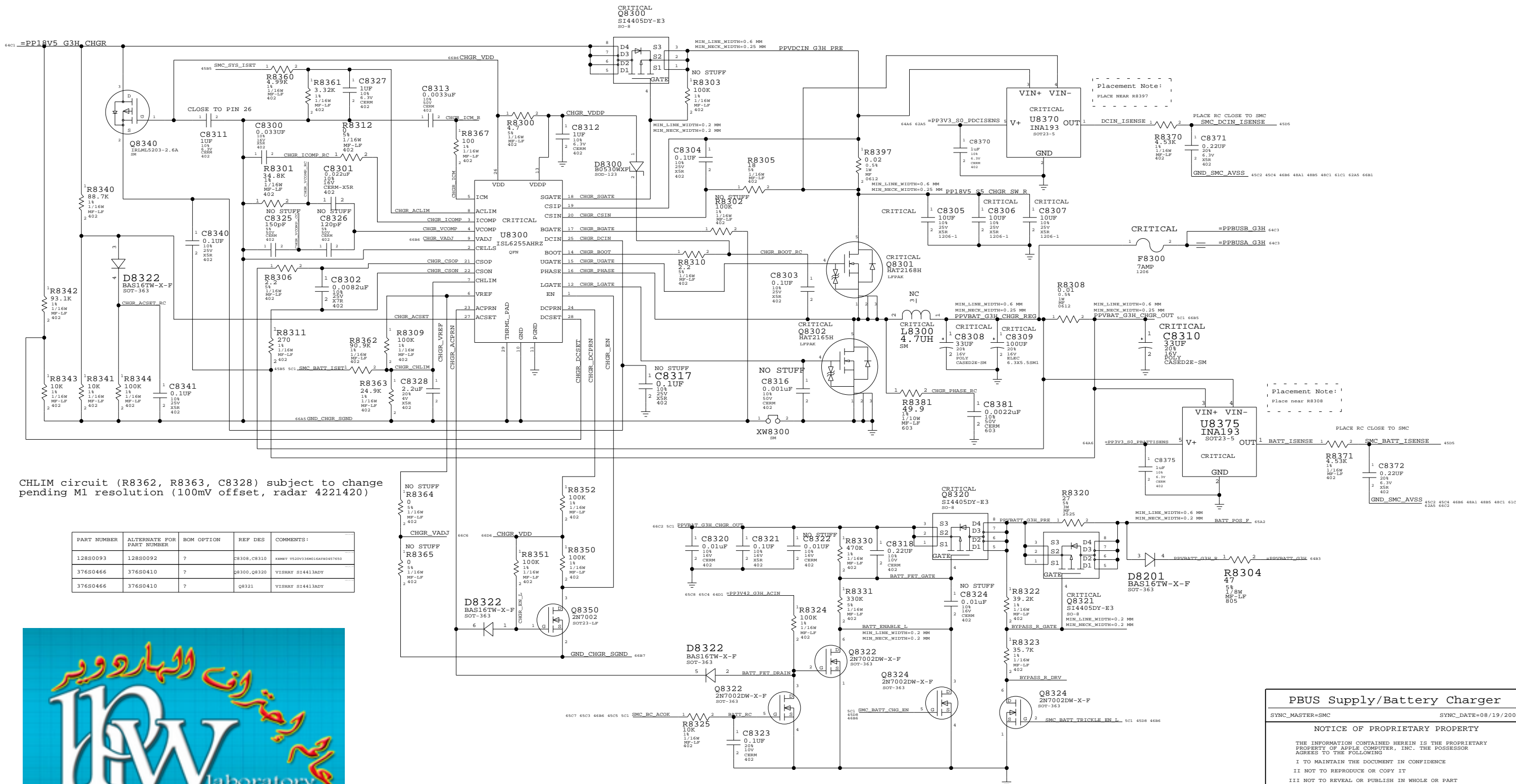
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PBUS SUPPLY / BATTERY CHARGER



PBUS Supply/Battery Charger

SYNC_MASTER=SMC SYNC_DATE=08/19/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7374	A
SCALE	NONE	SHT	OF
		66	79

D

C

B

A

D

C

B

A

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0227	155S0164	?	PP5V_S0_TMD5	KEEP MAG LAYER 28 WORK

Video Connectors

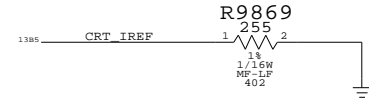
EXTERNAL VIDEO (VGA) INTERFACE

TMDS(MINI DVI) INTERFACE

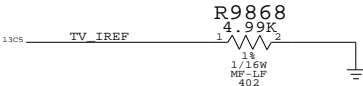
PLACE THE RESISTOR CLOSE TO GMCH AND THE CAP NEAR CONNECTOR

PLACE THE RESISTOR CLOSE TO GMCH AND THE CAP NEAR THE CONNECTOR

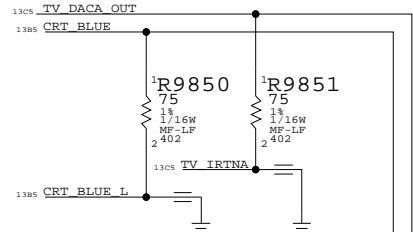
A 255 OHM 1% RESISTOR IS REQUIRED BETWEEN CRT_IREF AND GROUND



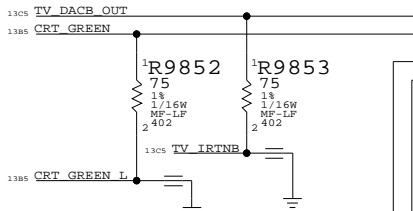
TV REFERENCE CURRENT, USES AN EXTERNAL RESISTOR OF 5K OHM 1% TO SET INTERNAL VOLTAGE LEVELS



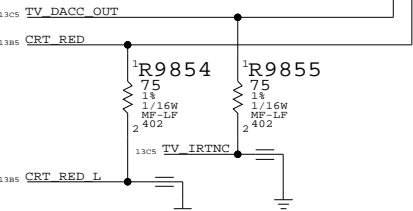
PLACE THE RESISTOR CLOSE TO GMCH



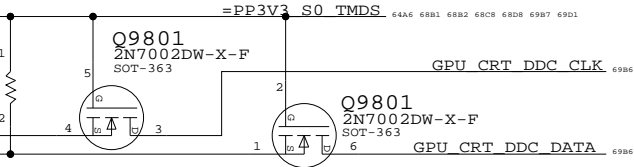
PLACE THE RESISTOR CLOSE TO GMCH



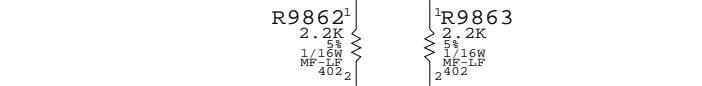
PLACE THE RESISTOR CLOSE TO GMCH



Isolation required for DVI power switch



DVI power DIODE on page 95 (D9500)



TMDS HTPLG

GPU CRT DDC CLK

GPU CRT DDC DATA

EXT_COMPVID_B

EXT_Y_G

EXT_C_R

=SB GPIO22

OMIT CRITICAL J9801 MINI-DVI RT-TH

PP5V_S0_DVIPORT

VGA B

VGA G

VGA R

=GND CHASSIS TMD5 UPPER

=GND CHASSIS TMD5 DOWN

CRITICAL L9805

90-OHM-300mA

2012H

CRITICAL L9807

90-OHM-300mA

2012H

CRITICAL L9806

90-OHM-300mA

2012H

CRITICAL L9804

370-OHM-280mA

SM1

MINI-DVI CONNECTOR

SYNC_MASTER=EUGENE SYNC_DATE=05/21/05

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0292	1	CONN, 32P MINI-DVI RCPT, RA, MG3, LF	J9801	CRITICAL	NORMAL
514-0319	1	CONN, 32P MINI-DVI RCPT, RA, BLACK, LF	J9801	CRITICAL	FANCY



APPLE COMPUTER INC.

SIZE

DRAWING NUMBER

REV.

SCALE

SHT

OF

79

