

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.  
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.  
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD DATE
C	0000813234	PRODUCTION RELEASED	2009-11-01

# K84 MLB SCHEMATIC

## PROD OK2FAB 11/01/2009


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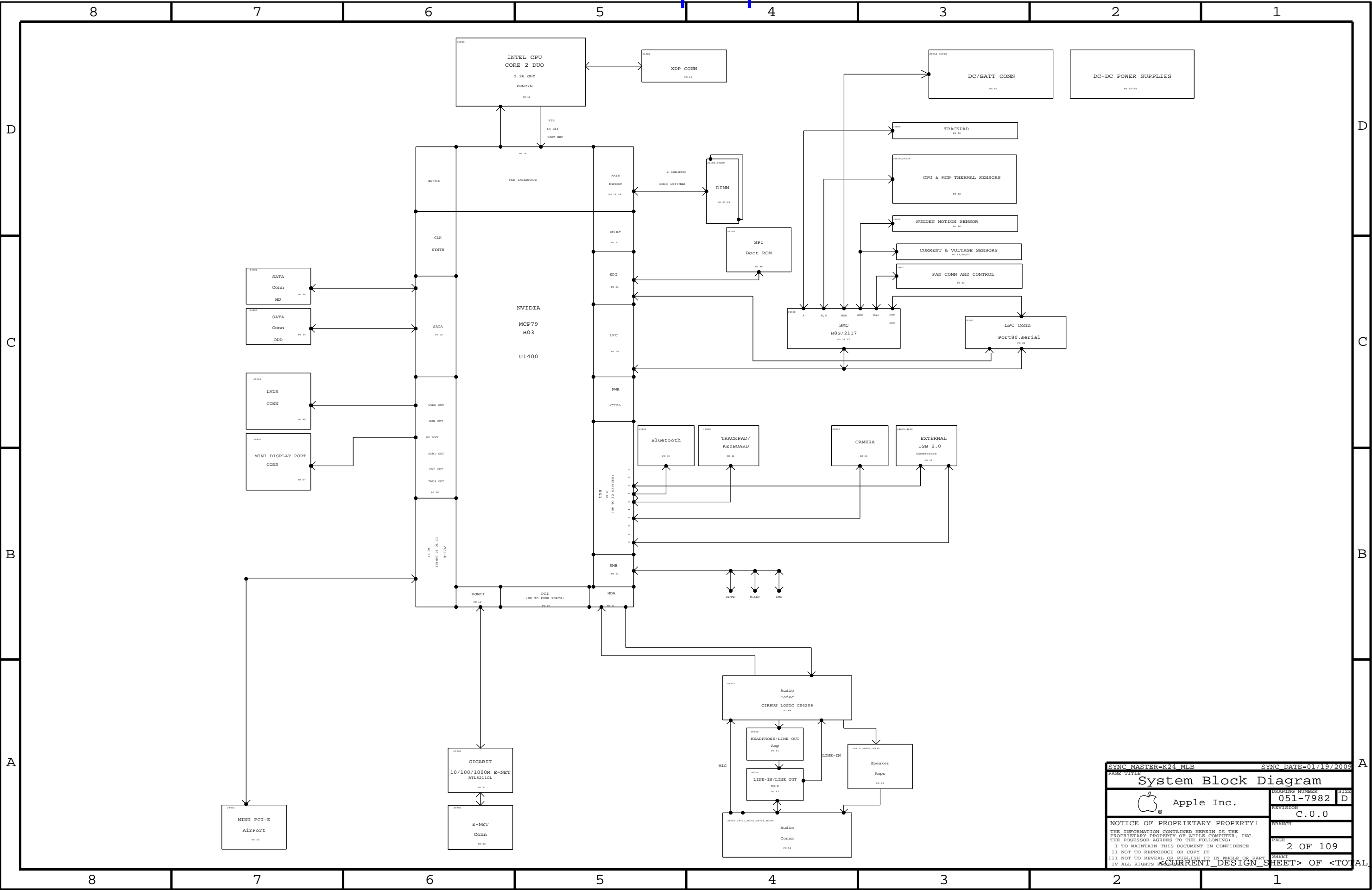
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Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7982	1	SCHEM_MLB,K84	SCB	CRITICAL	
820-2567	1	PCBF_MLB,K84	PCB	CRITICAL	

DRAWING TITLE			
SCHEM,MLB,K84			
 Apple Inc.	DRAWING NUMBER	051-7982	SIZE D
	REVISION	C.0.0	
	BRANCH		
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BOM Variants		
BOM NUMBER	BOM NAME	BOM OPTIONS
639-0035	PCBA,MLB,FOX DDR CONN,K84	K84_COMMON,CPU_2_OGHZ,FOX_DDR_CONN,EEE_BCG
639-0254	PCBA,MLB,MLX DDR CONN,K84	K84_COMMON,CPU_2_OGHZ,MLX_DDR_CONN,EEE_A36
085-0748	K84 MLB DEVELOPMENT BOM	K84_DEVEL_ENG
639-0554	PCBA,MLB,FOX DDR CONN,PVT K84	K84_COMMON_PVT,CPU_2_OGHZ,FOX_DDR_CONN,EEE_CXR
639-0555	PCBA,MLB,MLX DDR CONN,PVT K84	K84_COMMON_PVT,CPU_2_OGHZ,MLX_DDR_CONN,EEE_CV1
085-1076	K84 MLB DEVELOPMENT PVT	K84_DEVEL_PVT

BOM GROUP	BOM OPTIONS
K84_COMMON	COMMON,ALTERNATE,K84_MCP,K84_MISC,K84_DEBUG_ENG,K84_PRODPARTS
K84_COMMON_PVT	COMMON,ALTERNATE,K84_MCP,K84_MISC,K84_DEBUG_PROD,K84_PRODPARTS
K84_MCP	MCP_B03,BOOT_MODE_USER,MCPSEQ_SMC
K84_MISC	ONWIRE_PU,DP_ESD,MIKEY,LDO_NO,MEM_SENSE,1P05_HIGH_SIDE_SENSE,MCP_T_DIODE_SENSOR,MCP5MC_DIGITEMP_YES
K84_PRODPARTS	BOOTROM_PROD,SMC_PROD,WELLSPRING_PROD
K84_DEBUG_ENG	DEVEL_BOM,SMC_DEBUG_YES,XDP
K84_DEBUG_PVT	DEVEL_BOM_PVT,SMC_DEBUG_YES,XDP,NO_VREFMRGN
K84_DEBUG_PROD	SMC_DEBUG_YES,XDP,LPCPLUS_NOT,NO_VREFMRGN
K84_DEVEL_ENG	DEBUG_ADC,XDP_CONN,LPCPLUS,VREFMRGN
K84_DEVEL_PVT	XDP_CONN,LPCPLUS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
33783769	1	FOX,500V,2.0K,20K,100K,50,9K,60K,97000	U1000	CRITICAL	CPU_2_OGHZ
33880710	1	IC,SMCP,MCP79,35X30MM,BGA1437,B03	U1400	CRITICAL	MCP_B03
51680706	1	CONN,204P,SOD128,SOCKET,DDR3,RAM,B0A	J3200	CRITICAL	FOX_DDR_CONN
516-0201	1	CONN,204P,SOD128,P+0,60M	J3100	CRITICAL	FOX_DDR_CONN
51680790	1	CONN,204P,SOD128,SOCKET,DDR3,RAM,ROM/IC	J3200	CRITICAL	MLX_DDR_CONN
516-0213	1	CONN,204P,SOD128,P+0,60M,8P	J3100	CRITICAL	MLX_DDR_CONN
452-1708	4	SCW,M3,630,3306,0,04,NO,3,BLE,M07	SCREW1,SCREW2,SCREW3,SCREW4	CRITICAL	
514-0704	1	CONN,RCPT,RJ45,PLASTIC,WP,K83/K84	J3900	CRITICAL	
514-0705	2	CONN,RCPT,USB,4P,PLASTIC,WP,K83/K84	J4600,J4610	CRITICAL	
514-0706	1	CONN,RCPT,MDP,20P,PLASTIC,WP,K83/K84	J9400	CRITICAL	
514-0718	1	CONN,RCPT,S/PDIF,TX,WP,CPL,K83/K84	J6700	CRITICAL	
35382718	1	IC,1518042,4X 9 W007F,2.7A/2.80V,T088	U7870	CRITICAL	
870-1885	4	POSD P1H,MED,NOISE-IMPROVED,K84	ZS0900,ZS0901,ZS0902,ZS0903	CRITICAL	
870-1885	3	POSD P1H,MED,NOISE-IMPROVED,K84	ZS0908,ZS0909,ZS0911	CRITICAL	
870-1886	5	POSD P1H,TALL,NOISE-IMPROVED,K84	ZS0904,ZS0905,ZS0906,ZS0907,ZS0910	CRITICAL	
870-1886	5	POSD P1H,TALL,NOISE-IMPROVED,K84	ZS0912,ZS0913,ZS0914,ZS0915,ZS0919	CRITICAL	
870-1887	3	POSD P1H,TWIN,NOISE-IMPROVED,K84	ZS0917,ZS0918,ZS0916	CRITICAL	
10480033	4	RES,WP,1/4W,6,800M,5A,0805,0MD	R6612,R6617,R6630,R6633	CRITICAL	
51880774	1	CONN,RCPT,60P,P+0,4,02K,MY 1.0	J1300	CRITICAL	XDP_CONN

35382718 IS NEW INTERSIL PART FOR FIXING B4 DONGLE ISSUE  
514-0704 IS CLOUD GREY 4/LB3 PLASTIC W/PDNI PLATING VERSION OF 514-0692 PART FOR RJ45 CONNECTOR  
514-0705 IS CLOUD GREY 4/LB3 PLASTIC W/PDNI PLATING VERSION OF 514-0689 PART FOR USB CONNECTORS  
514-0706 IS CLOUD GREY 4/LB3 PLASTIC W/PDNI PLATING VERSION OF 514-0691 PART FOR MINI DP CONNECTOR  
514-0718 IS CLOUD GREY 4/LB3 PLASTIC W/PDNI PLATING VERSION OF 514-0694 PART FOR AUDIO CONNECTOR

DEVELOPMENT BOM					
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-0748	1	K84 MLB DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM
085-1076	1	K84 MLB DEVELOPMENT PVT	DEVEL_PVT	CRITICAL	DEVEL_BOM_PVT

Programmable Parts					
33880563	1	IC,SMC,MR/3117,5X9MM,TLE,WP	U4900	CRITICAL	SMC_BLANK
34182485	1	IC,SMC,K84	U4900	CRITICAL	SMC_PROD
33580610	1	IC,FLASH,SP1,128MBIT,3.3V,80Mhz,8-SOP	U6100	CRITICAL	BOOTROM_BLANK
34182487	1	IC,PROGRAM,EP1 BOOTROM,UNLOCK,K84	U6100	CRITICAL	BOOTROM_PROD
33782893	1	IC,PSDCA W/ USB,5A P1H,WP,CY8C24794	U5701	CRITICAL	WELLSPRING_BLANK
34182491	1	IC,WELLSPRING CONTROLLER,K84	U5701	CRITICAL	WELLSPRING_PROD

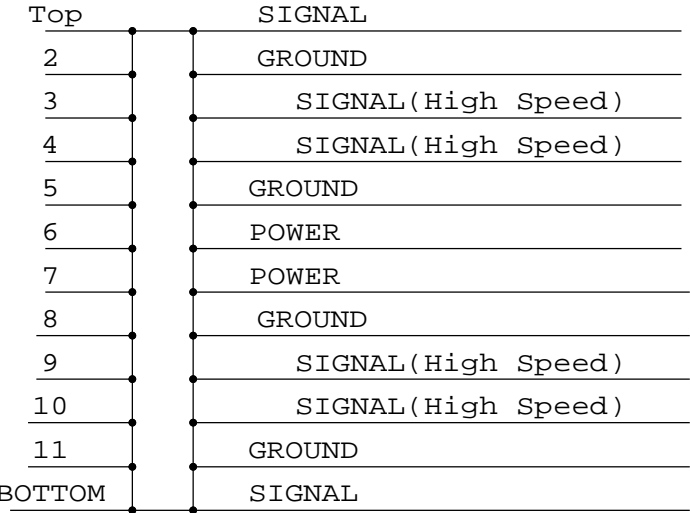
LOCKED BOOTROM APW IS 34182488

Alternate Parts				
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
15280693	15280778		ALL	DATE/VERSION, MACLAYERS AS ALTERNATE
15280796	15280685		ALL	CY82C0 AS ALTERNATE
15780058	15780055		ALL	DELTA AS ALTERNATE
13880603	13880602		ALL	MURATA AS ALTERNATE
12880093	12880218		ALL	FERRET AS ALTERNATE
15280874	15280516		ALL	MACLAYERS AS ALTERNATE
15280847	15280586		ALL	MACLAYERS AS ALTERNATE
10480018	10480023		ALL	DATE/VERSION AS ALTERNATE

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LABEL,P/N LABEL,PCB,20MM X 6 MM	[EEE:BCD]	CRITICAL	EEE_BCD
826-4393	1	LABEL,P/N LABEL,PCB,20MM X 6 MM	[EEE:A36]	CRITICAL	EEE_A36
826-4393	1	LABEL,P/N LABEL,PCB,20MM X 6 MM	[EEE:CXR]	CRITICAL	EEE_CXR
826-4393	1	LABEL,P/N LABEL,PCB,20MM X 6 MM	[EEE:CV1]	CRITICAL	EEE_CV1

K84 BOARD STACK-UP



SYNC MASTER=K24 MLB

SYNC DATE=01/19/2009

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Functional Test Points

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FAN CONNECTORS FUNC\_TEST

PP5V	TRUE	PP5VRT S0	7 8
PP5V	TRUE	FAN RT PWM	43
PP5V	TRUE	FAN RT TACH	43
(NEED TO ADD 1 GND TP)			

MIC FUNC\_TEST

PP5V	TRUE	BI MIC LO	53 54
PP5V	TRUE	BI MIC HI	53 54
PP5V	TRUE	BI MIC SHIELD	53 54

SPEAKER FUNC\_TEST

PP5V	TRUE	SPKRAMP L N OUT	52 53
PP5V	TRUE	SPKRAMP L P OUT	52 53
PP5V	TRUE	SPKRAMP R N OUT	52 53
PP5V	TRUE	SPKRAMP R P OUT	52 53
PP5V	TRUE	SPKRAMP SUB N OUT	52 53
PP5V	TRUE	SPKRAMP SUB P OUT	52 53

LVDS FUNC\_TEST

PP5V	TRUE	PP3V3 LCDVDD_SW_F	7 65 (NEED 2 TP)
PP5V	TRUE	PP3V3_S0_LCD_F	65
PP5V	TRUE	PPVOUT_S0_LCDBKLT	7 47 65 68 (NEED 2 TP)
PP5V	TRUE	LVDS_IG_DDC_CLK	18 65
PP5V	TRUE	LVDS_IG_DDC_DATA	18 65
PP5V	TRUE	LVDS_IG_A_DATA_N<0>	18 65 72
PP5V	TRUE	LVDS_IG_A_DATA_P<0>	18 65 72
PP5V	TRUE	LVDS_IG_A_DATA_N<1>	18 65 72
PP5V	TRUE	LVDS_IG_A_DATA_P<1>	18 65 72
PP5V	TRUE	LVDS_IG_A_DATA_N<2>	18 65 72
PP5V	TRUE	LVDS_IG_A_DATA_P<2>	18 65 72
PP5V	TRUE	LVDS_IG_A_CLK_F_N	65 72
PP5V	TRUE	LVDS_IG_A_CLK_F_P	65 72
PP5V	TRUE	LED_RETURN_1	65 68
PP5V	TRUE	LED_RETURN_2	65 68
PP5V	TRUE	LED_RETURN_3	65 68
PP5V	TRUE	LED_RETURN_4	65 68
PP5V	TRUE	LED_RETURN_5	65 68
PP5V	TRUE	LED_RETURN_6	65 68
PP5V	TRUE	PP5V_S3_CAMERA_F	7 65
PP5V	TRUE	USB_CAMERA_CONN_P	65 73
PP5V	TRUE	USB_CAMERA_CONN_N	65 73
(NEED TO ADD 5 GND TP)			

SATA ODD CONN FUNC\_TEST

PP5V	TRUE	PP5V_SW_ODD	(NEED 2 TP) 7 34 47
PP5V	TRUE	SMC_ODD_DETECT	34 36
PP5V	TRUE	SATA_ODD_D2R_C_P	34 72
PP5V	TRUE	SATA_ODD_D2R_C_N	34 72
PP5V	TRUE	SATA_ODD_R2D_P	34 72
PP5V	TRUE	SATA_ODD_R2D_N	34 72
(NEED TO ADD 2 GND TP)			

SATA HDD/SIL FUNC\_TEST

PP5V	TRUE	PP5V_S0_HDD_FLT	(NEED 2 TP) 7 34
PP5V	TRUE	SATA_HDD_R2D_P	34 72
PP5V	TRUE	SATA_HDD_R2D_N	34 72
PP5V	TRUE	SATA_HDD_D2R_C_P	34 72
PP5V	TRUE	SATA_HDD_D2R_C_N	34 72
PP5V	TRUE	SYS_LED_ANODE_R	34
(NEED TO ADD 3 GND TP)			

BATT POWER CONN FUNC\_TEST

PP5V	TRUE	SMBUS_SMC_BSA_SCL	39 75
PP5V	TRUE	SMBUS_SMC_BSA_SDA	39 75
PP5V	TRUE	SYS_DETECT_L	55
PP5V	TRUE	BATT_POS_F	55 56
(NEED TO ADD 2 GND TP) (NEED 2 TP)			

HALL EFFECT CONNECTOR FUNC\_TEST

PP5V	TRUE	PP3V42_G3H	7 8
PP5V	TRUE	SMC_LID_R	55

X16 WIRELESS CONN FUNC\_TEST

PP5V	TRUE	PP3V3_S3_BT_F	30
PP5V	TRUE	CONN_PCIE_MINI_D2R_P	30 72
PP5V	TRUE	CONN_PCIE_MINI_D2R_N	30 72
PP5V	TRUE	CONN_PCIE_MINI_R2D_P	30 72
PP5V	TRUE	CONN_PCIE_MINI_R2D_N	30 72
PP5V	TRUE	PCIE_CLK100M_MINI_CONN_P	30 72
PP5V	TRUE	PCIE_CLK100M_MINI_CONN_N	30 72
PP5V	TRUE	PP3V3_WLAN	7 30 (NEED 2 TP)
PP5V	TRUE	PCIE_WAKE_L	17 30
PP5V	TRUE	CONN_USB2_BT_P	30 73
PP5V	TRUE	CONN_USB2_BT_N	30 73
PP5V	TRUE	MINI_CLKREQ_Q_L	30
PP5V	TRUE	MINI_RESET_CONN_L	30
(NEED TO ADD 2 GND TP)			

IPD\_FLEX\_CONN FUNC\_TEST

PP5V	TRUE	PP3V3_S3_LDO	7 45
PP5V	TRUE	PP18V5_S3	7 45
PP5V	TRUE	Z2_CS_L	44 45
PP5V	TRUE	Z2_DEBUG3	44 45
PP5V	TRUE	Z2_MOSI	44 45
PP5V	TRUE	Z2_MISO	44 45
PP5V	TRUE	Z2_SCLK	44 45
PP5V	TRUE	Z2_BOOST_EN	45
PP5V	TRUE	Z2_HOST_INTN	44 45
PP5V	TRUE	Z2_CLKIN	44 45
PP5V	TRUE	Z2_KEY_ACT_L	44 45
PP5V	TRUE	Z2_RESET	44 45
PP5V	TRUE	PSOC_MISO	44 45
PP5V	TRUE	PSOC_MOSI	44 45
PP5V	TRUE	PSOC_SCLK	44 45
PP5V	TRUE	SMBUS_SMC_A_S3_SDA	39 75
PP5V	TRUE	SMBUS_SMC_A_S3_SCL	39 75
PP5V	TRUE	PSOC_F_CS_L	44 45
PP5V	TRUE	PICKB_L	44 45
(NEED TO ADD 2 GND TP)			

KEYBOARD CONN FUNC\_TEST

PP5V	TRUE	PP3V3_S3	7 8
PP5V	TRUE	PP3V42_G3H	7 8
PP5V	TRUE	WS_KBD1	44
PP5V	TRUE	WS_KBD2	44
PP5V	TRUE	WS_KBD3	44
PP5V	TRUE	WS_KBD4	44
PP5V	TRUE	WS_KBD5	44
PP5V	TRUE	WS_KBD6	44
PP5V	TRUE	WS_KBD7	44
PP5V	TRUE	WS_KBD8	44
PP5V	TRUE	WS_KBD9	44
PP5V	TRUE	WS_KBD10	44
PP5V	TRUE	WS_KBD11	44
PP5V	TRUE	WS_KBD12	44
PP5V	TRUE	WS_KBD13	44
PP5V	TRUE	WS_KBD14	44
PP5V	TRUE	WS_KBD15_CAP	44
PP5V	TRUE	WS_KBD16_NUM	44
PP5V	TRUE	WS_KBD17	44
PP5V	TRUE	WS_KBD18	44
PP5V	TRUE	WS_KBD19	44
PP5V	TRUE	WS_KBD20	44
PP5V	TRUE	WS_KBD21	44
PP5V	TRUE	WS_KBD22	44
PP5V	TRUE	WS_KBD23	44
PP5V	TRUE	WS_KBD_ONOFF_L	44
PP5V	TRUE	WS_LEFT_SHIFT_KBD	44
PP5V	TRUE	WS_LEFT_OPTION_KBD	44
PP5V	TRUE	WS_CONTROL_KBD	44
(NEED TO ADD 1 GND TP)			


POWER NETS FUNC\_TEST

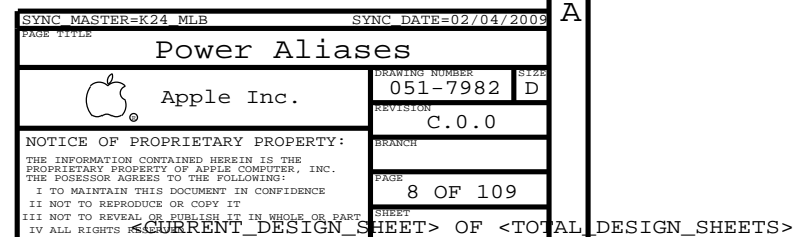
PP5V	TRUE	PPVCORE_S0_CPU	8
PP5V	TRUE	PPVCORE_S0_MCP	8
PP5V	TRUE	PP0V75_S0	8
PP5V	TRUE	PP1V05_S0	8
PP5V	TRUE	PP1V5_S0	8
PP5V	TRUE	PP1V8_S0	8
PP5V	TRUE	PP5VLT_S0	8
PP5V	TRUE	PP5VRT_S0	7 8
PP5V	TRUE	PP3V3_S0	8
PP5V	TRUE	PP1V5_S3	8
PP5V	TRUE	PP3V3_S3	7 8
PP5V	TRUE	PP5V_S3	8
PP5V	TRUE	PP1V1R1V05_S5	8
PP5V	TRUE	PP3V3_S5	8
PP5V	TRUE	PP3V42_G3H	7 8
PP5V	TRUE	PPBUS_G3H	8
PP5V	TRUE	PP3V3_ENET_PHY	8
PP5V	TRUE	PP1V2R1V05_ENET	8
PP5V	TRUE	PP3V3_G3_RTC	21 22 25
PP5V	TRUE	PP3V3_WLAN	7 30
PP5V	TRUE	PP5V_SW_ODD	7 34 47
PP5V	TRUE	PP5V_S0_HDD_FLT	7 34
PP5V	TRUE	PP3V3_S5_AVREF_SMC	36 37
PP5V	TRUE	PP18V5_S3	7 45
PP5V	TRUE	PP3V3_S3_LDO	7 45
PP5V	TRUE	PP3V3_LCDVDD_SW_F	7 65
PP5V	TRUE	PPVOUT_S0_LCDBKLT	7 47 65 68
PP5V	TRUE	PP4V5_AUDIO_ANALOG	49
PP5V	TRUE	SMC_PM_G2_EN	36 57 63
PP5V	TRUE	PM_SLP_S4_L	21 32 36 63 67
PP5V	TRUE	PM_SLP_S3_L	21 32 36 63 67
PP5V	TRUE	PP5V_S3_CAMERA_F	7 65

(NEED TO ADD 1 GND TP)

DC POWER CONN FUNC\_TEST

PP5V	TRUE	PP18V5_DCIN_FUSE (NEED 2 TP)	55
PP5V	TRUE	ADAPTER_SENSE	55
(NEED TO ADD 2 GND TP)			

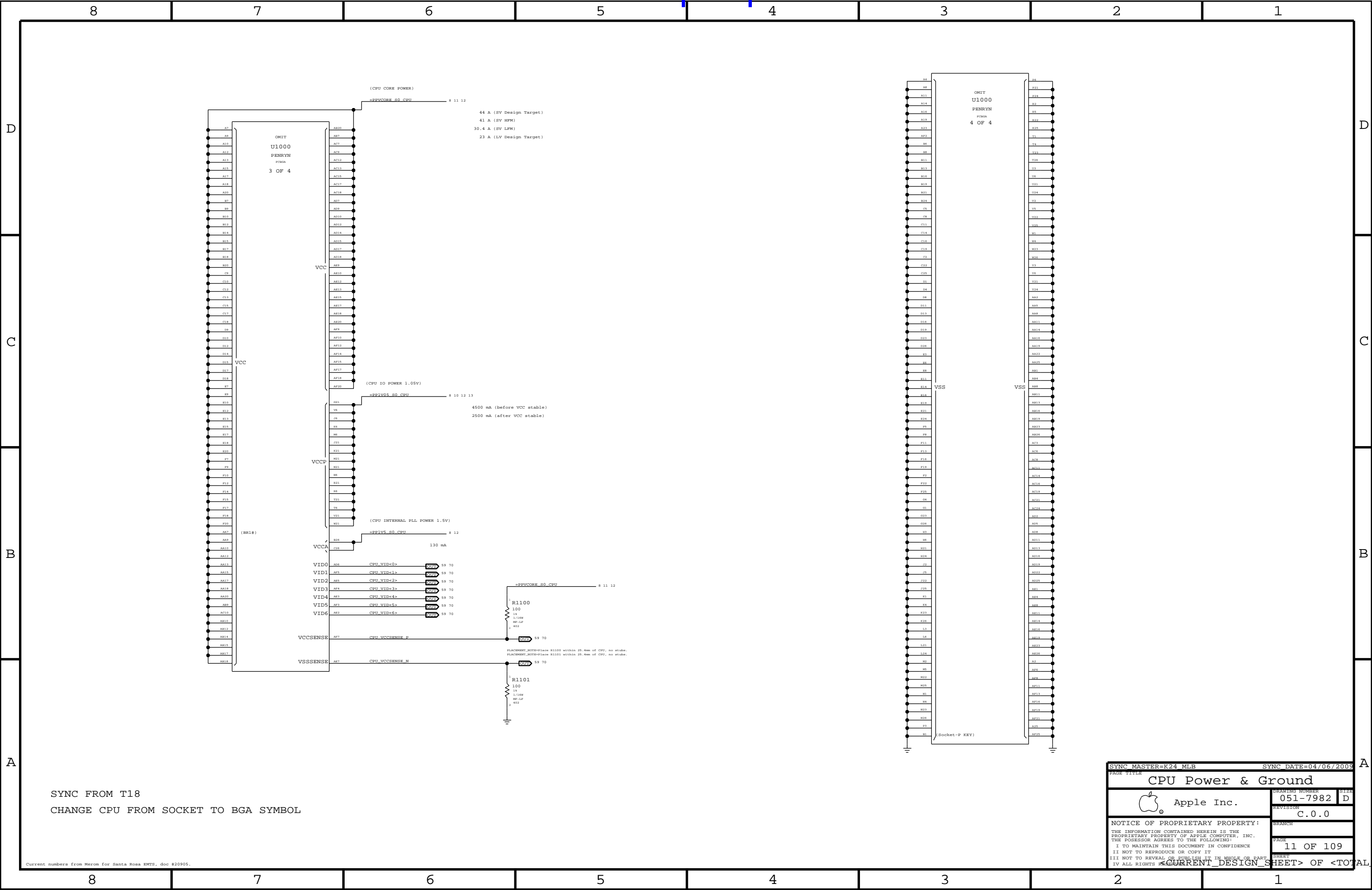
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PAGE TITLE			
FUNC TEST			
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		7 OF 109	
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SYNC FROM T18  
CHANGE CPU FROM SOCKET TO BGA SYMBOL

SYNC MASTER=K24 MLB		SYNC DATE=04/06/2009	
PAGE TITLE			
CPU Power & Ground			
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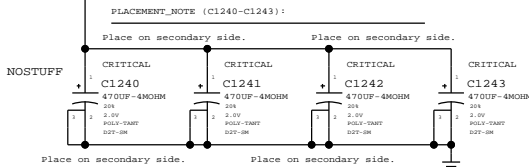
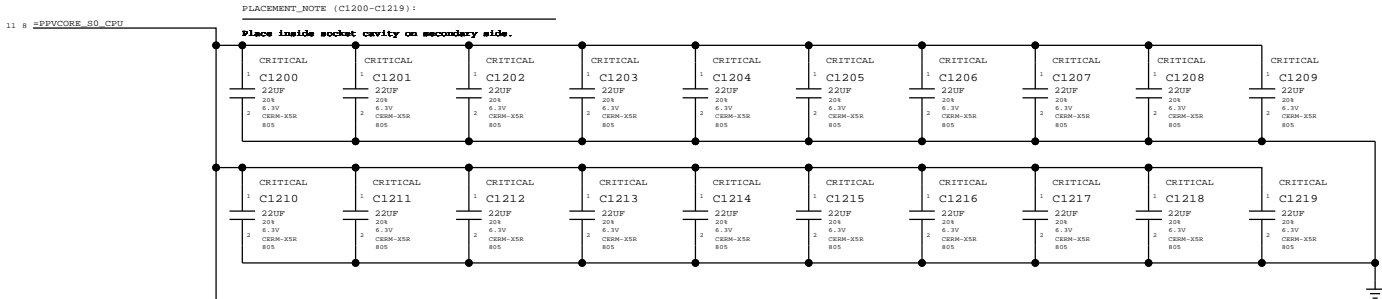
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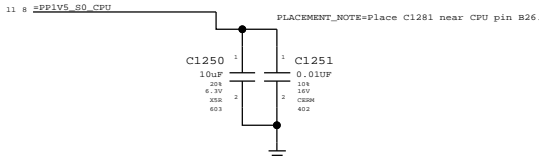
CPU VCore HF and Bulk Decoupling

4X 330UF, 20X 22UF 0805



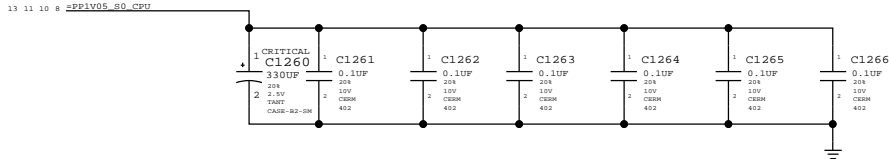
VCCA (CPU AVdd) DECOUPLING

1x 10uF, 1x 0.01uF




VCCP (CPU I/O) DECOUPLING

1x 330uF, 6x 0.1uF 0402



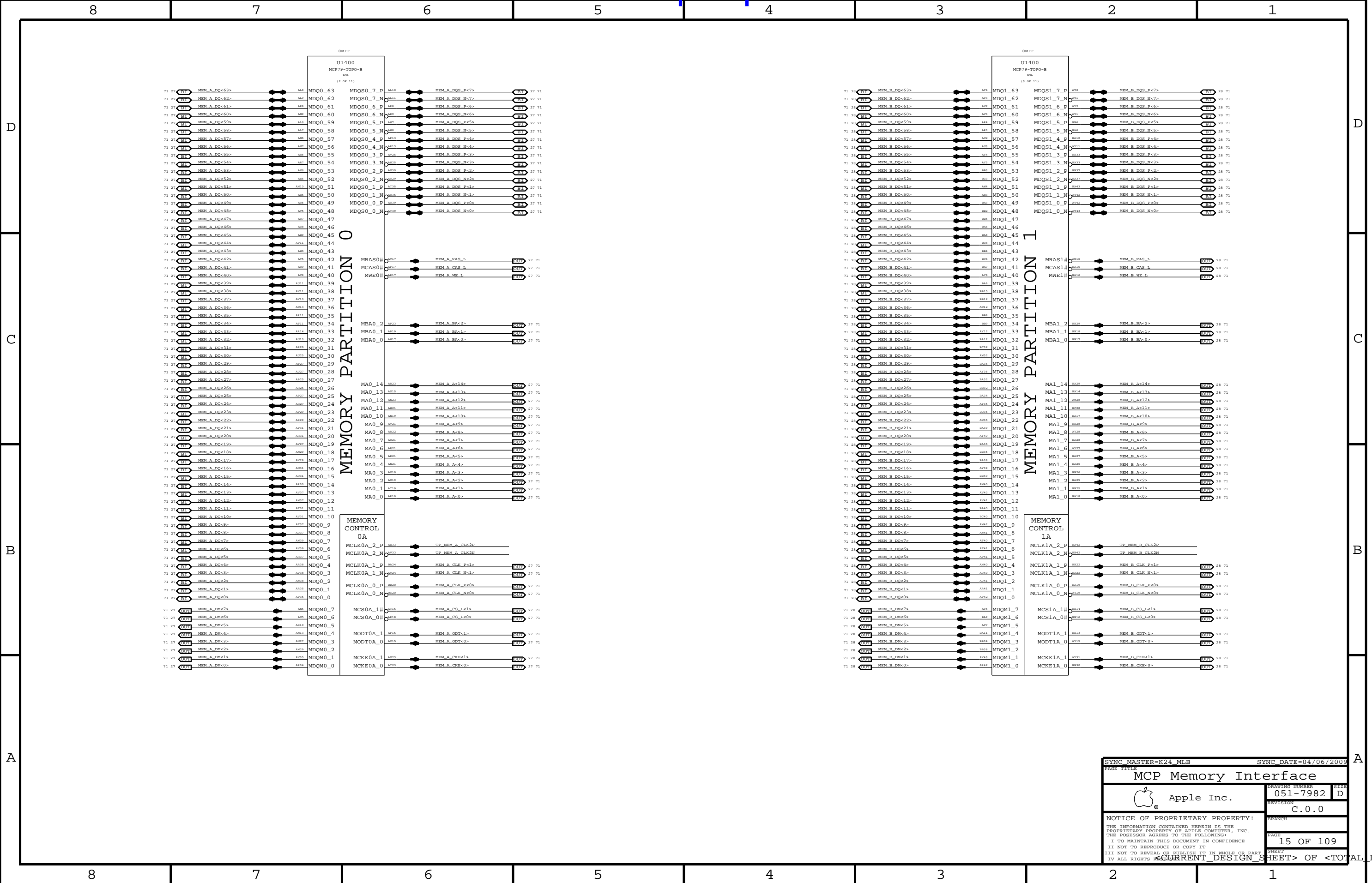
SYNC FROM T18  
REMOVE NO STUFF CAPS C1220 TO C1231  
REMOVE C1244 & C1245  
CHANGE C1240-C1243 AND C1260 FROM 128S0241(9 MILLI-OHM) TO 128S0231(6 MILLI-OHM)

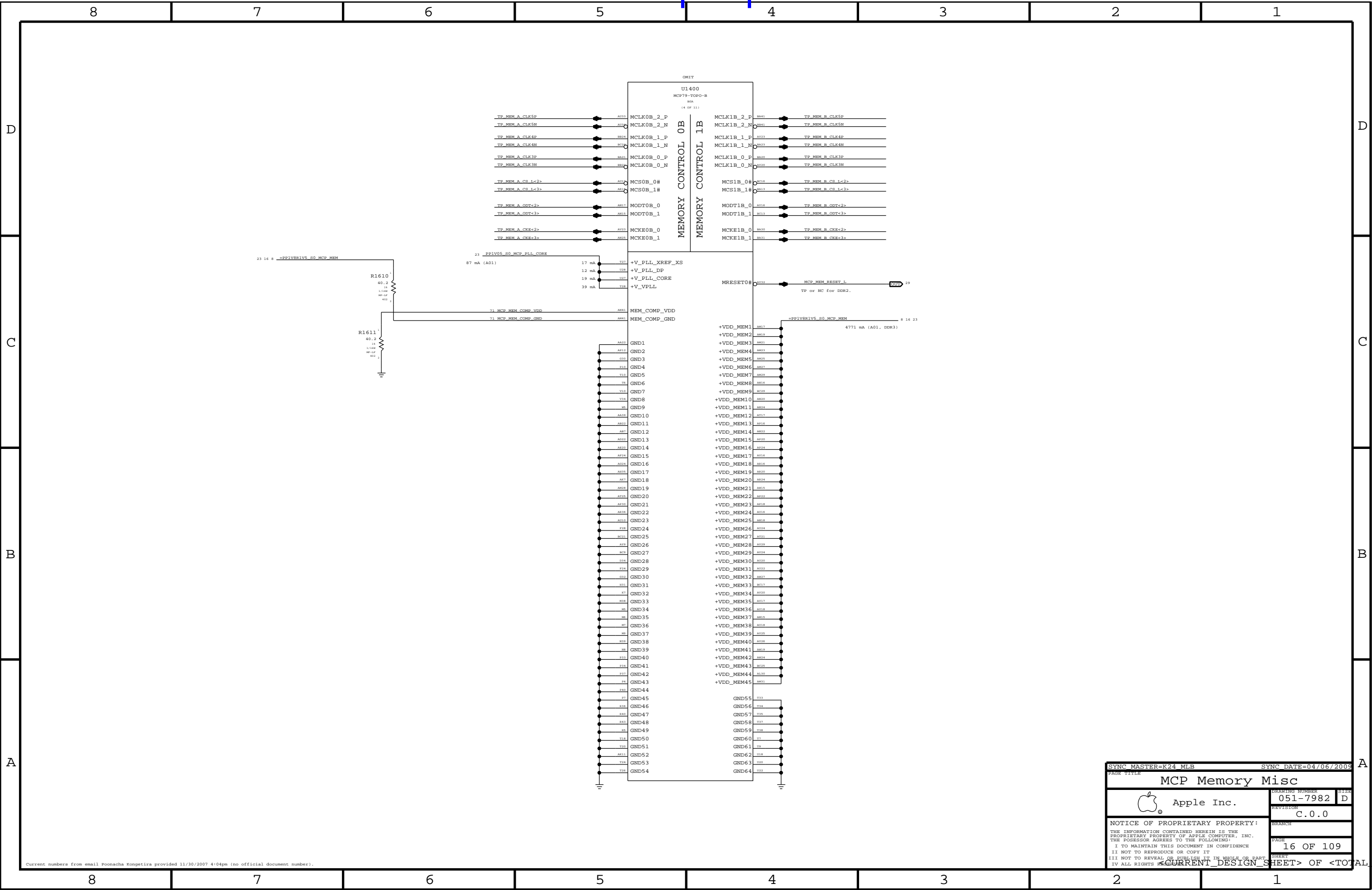
SYNC MASTER=K24 MLB		SYNC DATE=03/30/2009	
PAGE TITLE			
CPU Decoupling			
	Apple Inc.	DRAWING NUMBER	SHEET
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SYNC DATE=04/06/2009

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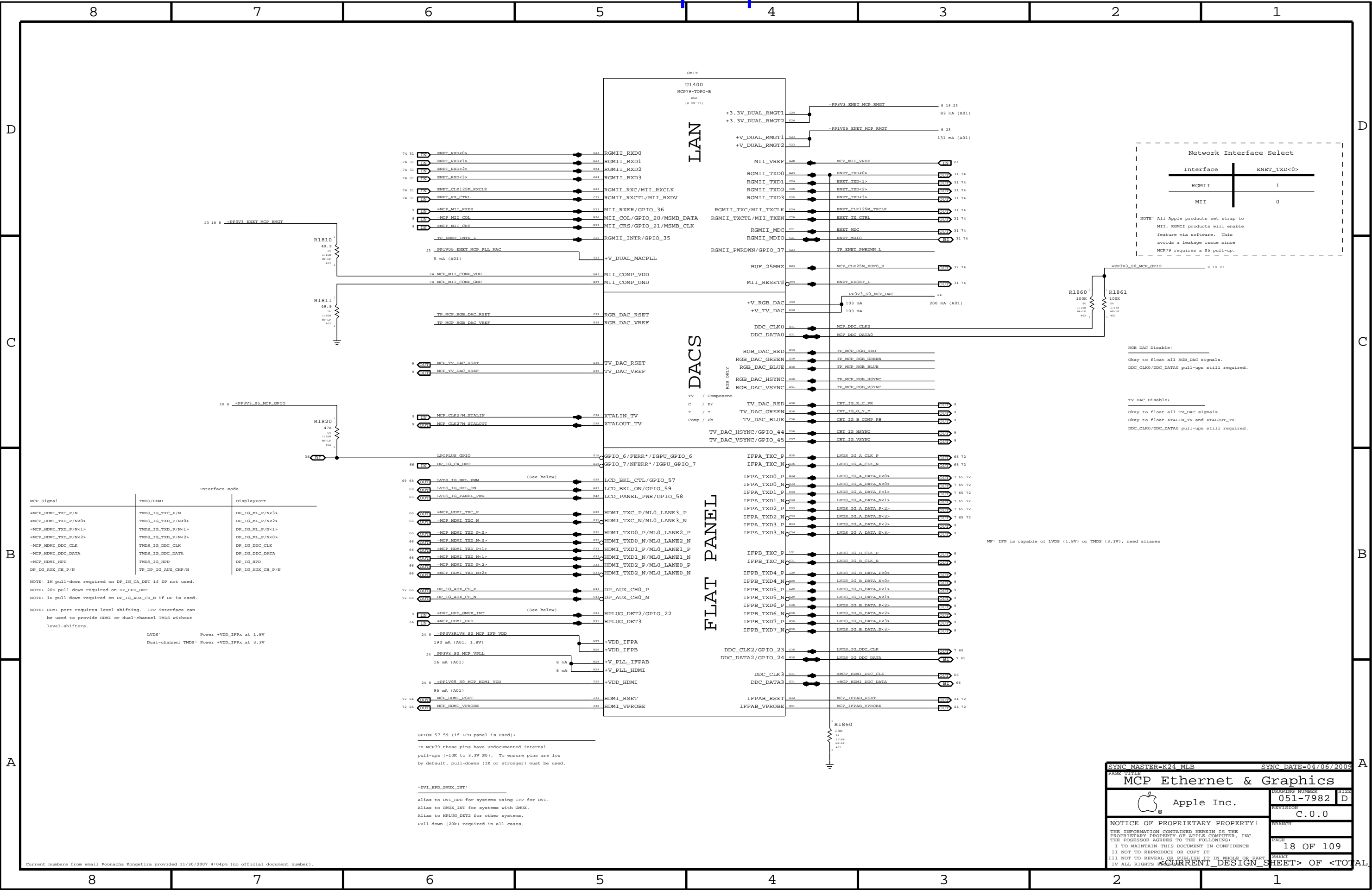
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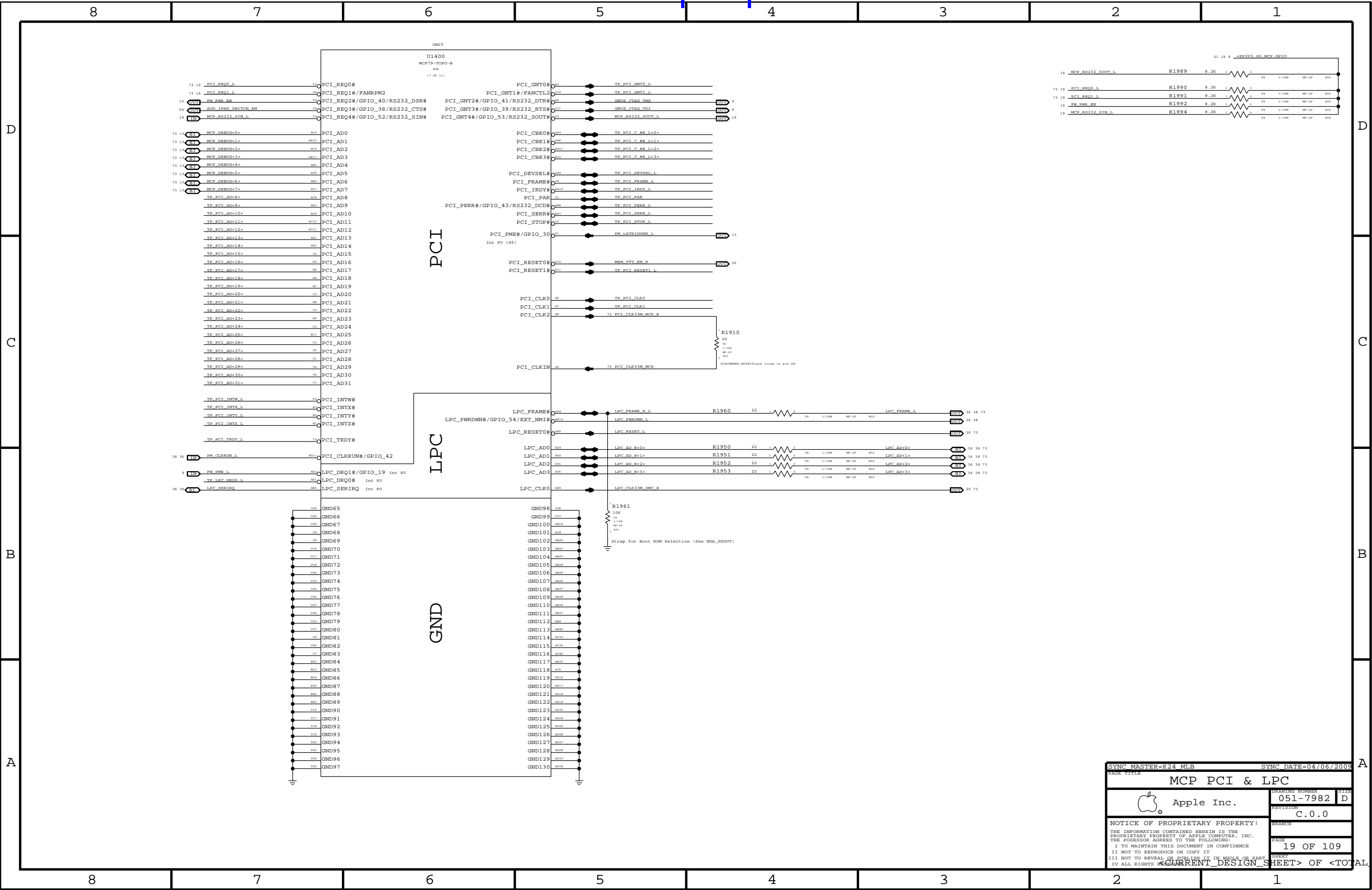
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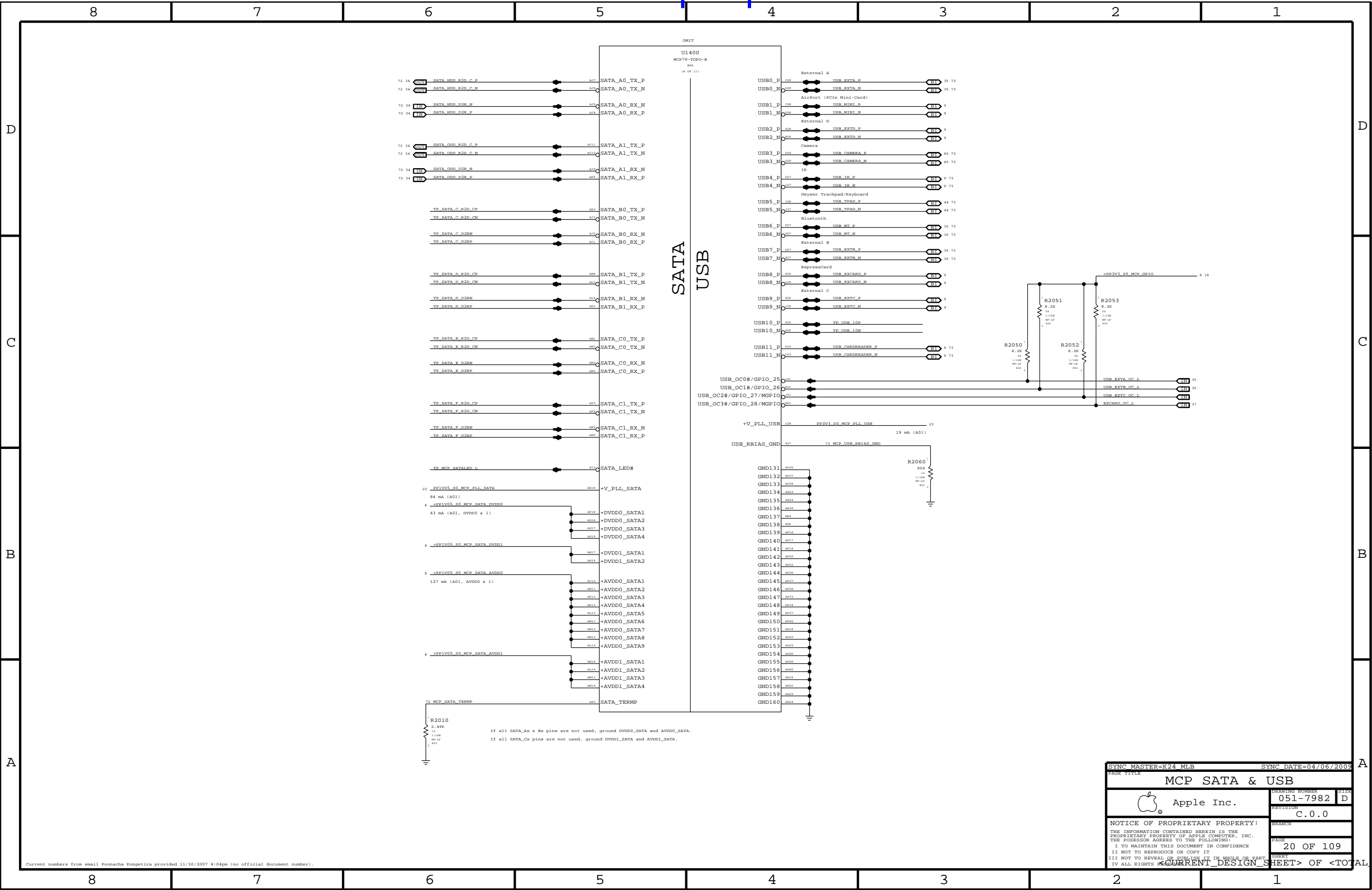
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SYNC MASTER=K24 MLB

SYNC DATE=04/06/2009

MCP SATA & USB

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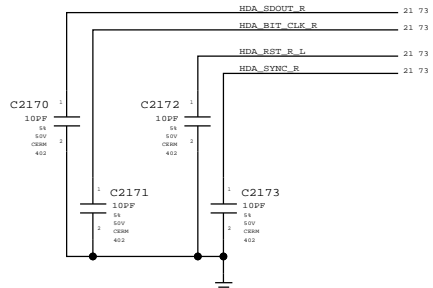
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OF <TOTAL DESIGN SHEETS>

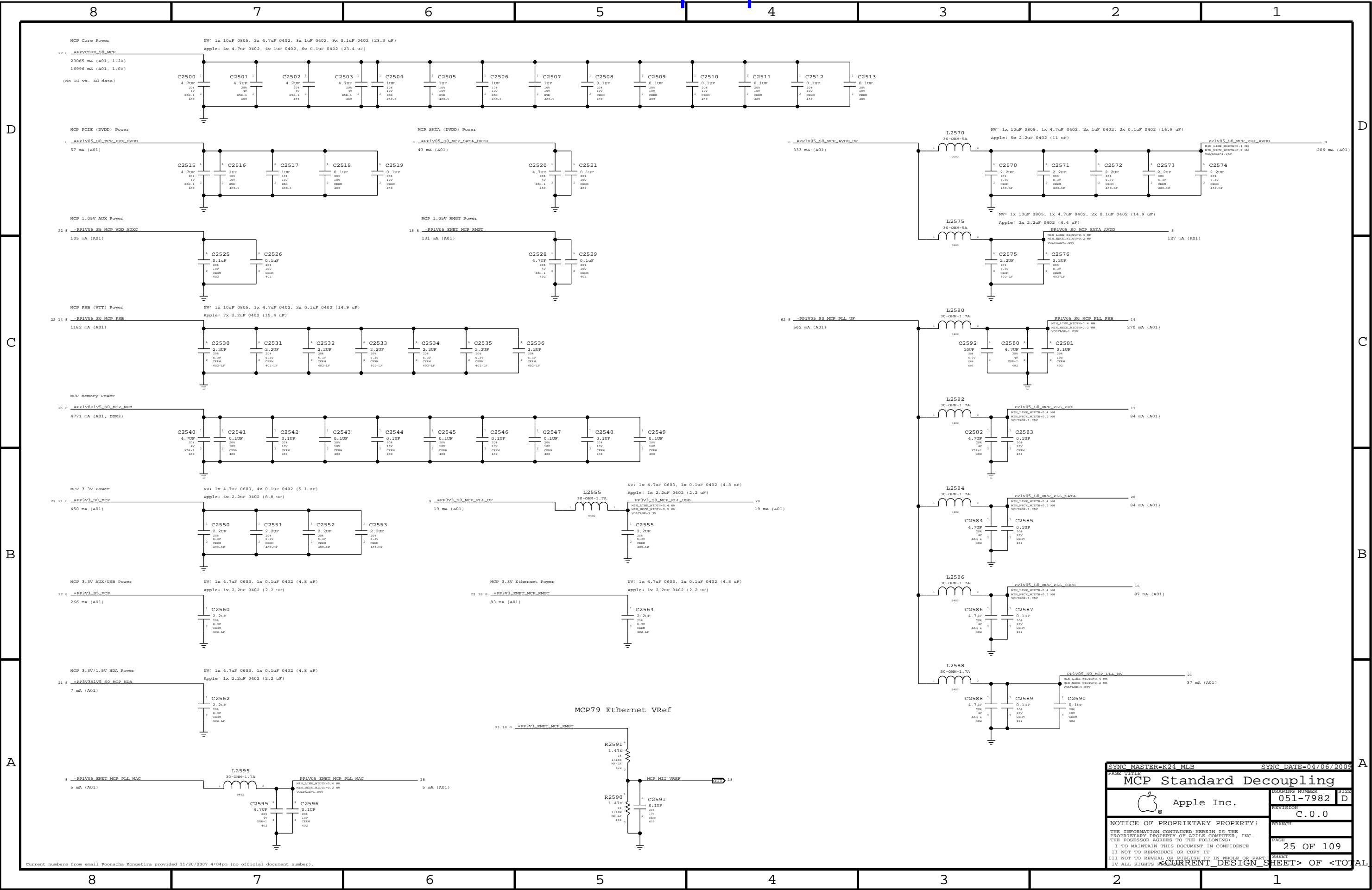




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SYNC MASTER=K24 MLB		SYNC DATE=04/06/2009	
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MCP Standard Decoupling			
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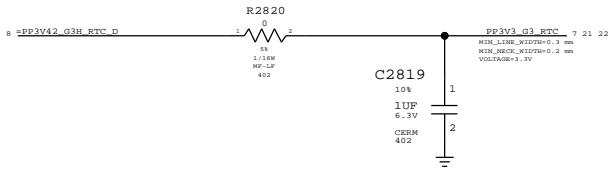
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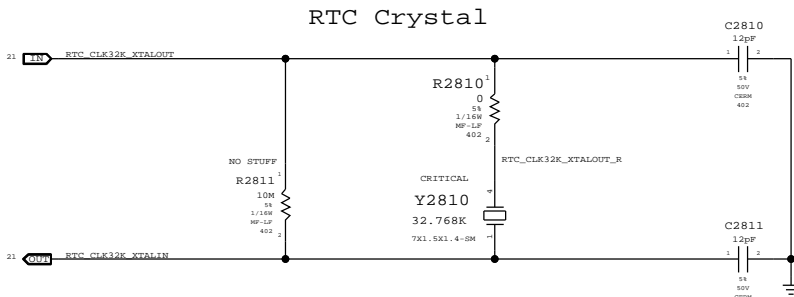
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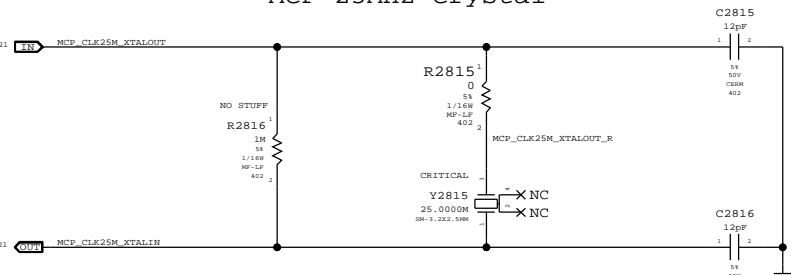
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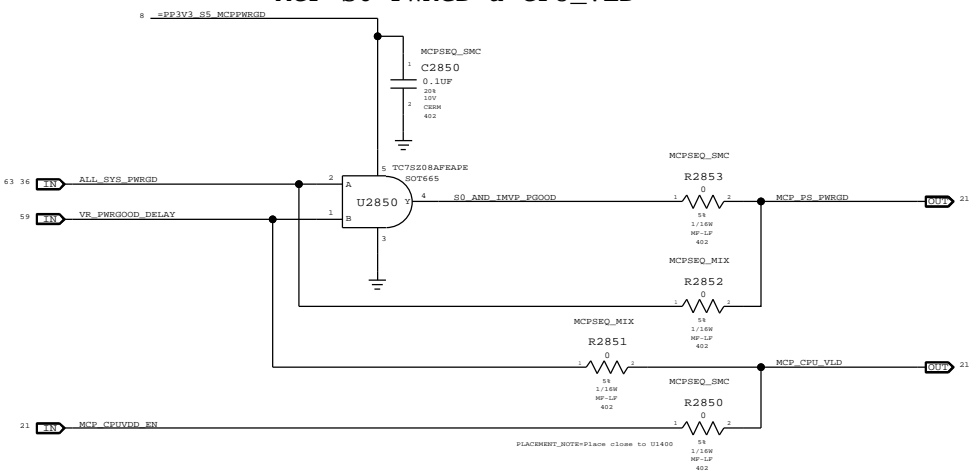
PLACEMENT\_NOTE=PLACE C2819 CLOSE TO MCP79  
PLACE C2819 CLOSE TO MCP79



MCP 25MHz Crystal



MCP S0 PWRGD & CPU\_VLD



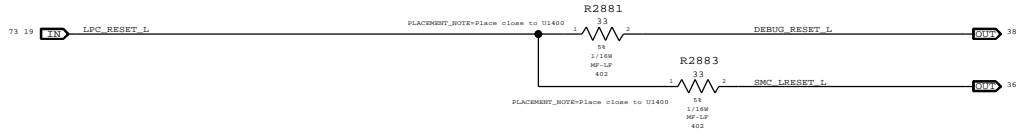
MCPSEQ\_SMC represents MCP79 'MLB' power sequencing connections, but results in MCP79 ROMSIP sequence happening after CPU powers up. MCPSEQ\_MIX is cross between MLB and internal power sequencing, which results in earlier ROMSIP and MCP PSB I/O interface initialization. SMC 99ms delay from ALL\_SYS\_PWRGD to IMVP\_VR\_ON plus IMVP6 delay for VR\_PWRGOOD\_DELAY should guarantee CPU\_VLD does not go high before CPUVDD\_EN (which is 40-100ms after PS\_PWRGD assertion).

NOTE: If CPU\_VLD deasserts during S0 MCP79 will take system to S5 immediately.

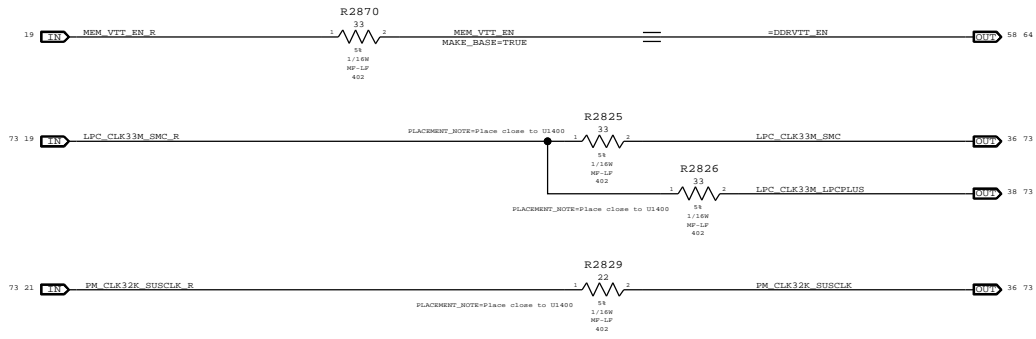
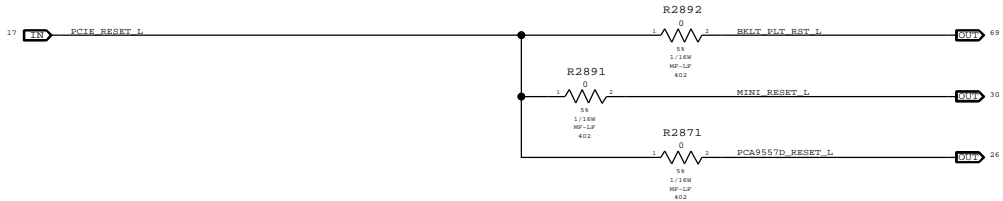
SYNC FROM T18  
CHANGE RESET BUTTON TO RESET PADS  
REMOVE UNUSED PCIE RESET SIGNALS  
REMOVE R2824 AND NET PCI\_CLK33M\_SLOT\_A  
CHANGE RTC COIN CELL TO LDO & SUPERCAP  
ALIAS MEM\_VTT\_EN TO =DDRVTT\_EN  
CHANGE Y2810 AND U2850 TO SMALLER PARTS

### Platform Reset Connections

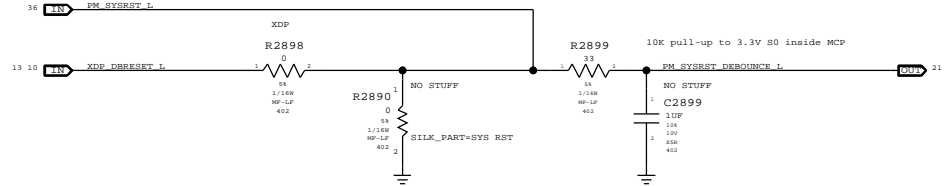
#### LPC Reset (Unbuffered)




#### PCIE Reset (Unbuffered)



#### Reset Button



SYNC MASTER=K24 MLB		SYNC DATE=02/15/2009	
PAGE TITLE			
SB Misc			
 Apple Inc.		DRAWING NUMBER	051-7982
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## Page Notes

Power aliases required by this page:

- =PP3V3\_S3\_VREFMRGN

- =PP3V3\_S5\_VREFMRGN

```
- =PPVTT_S3_DDR_BUF
```

Signal aliases required by this page:

```
- =I2C_VREFDACS_SCL
```

```
- #I2C_VREFDACS_SDA
```

```
- =I2C_PCA9557D_SCL
```

- =I2C\_PCA9557D\_SDA

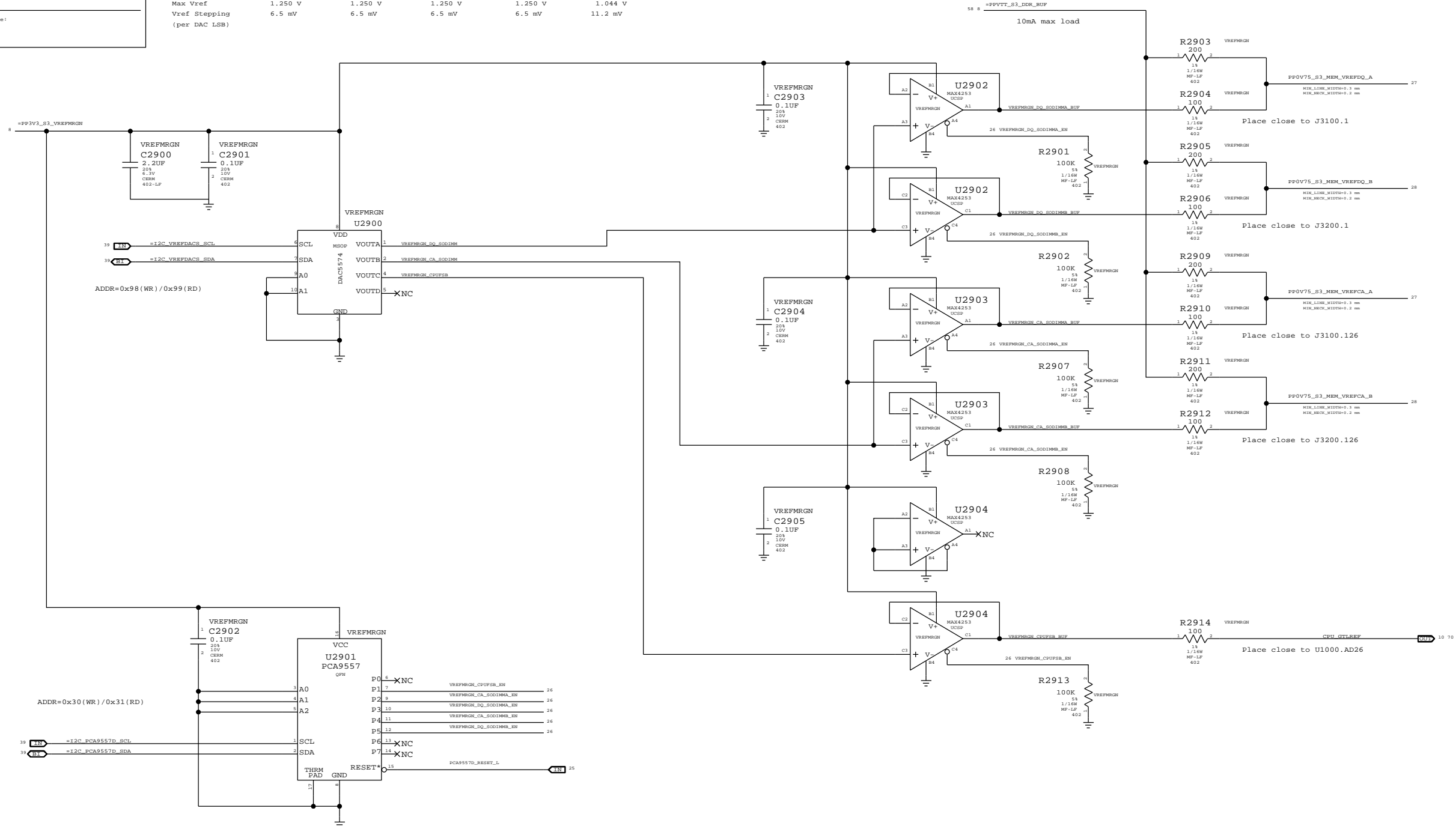
BOM options provided by this page:

VREFMRGN

NO\_VREFMRGN

	MEM A VREF DQ	MEM A VREF CA	MEM B VREF DQ	MEM B VREF CA	CPU FSB VREF
DAC channel	A	B	A	B	C
Min DAC code	0x00	0x00	0x00	0x00	0x00
Max DAC code	0x87	0x87	0x87	0x87	0x55
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA
Max source I	5 mA	5 mA	5 mA	5 mA	0.52 mA
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately (i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES_MTL FILM, 0.5K,0402,SM,LF	R2903	CRITICAL	NO_VREFMRGN
116S0004	1	RES_MTL FILM, 0.5K,0402,SM,LF	R2905	CRITICAL	NO_VREFMRGN
116S0004	1	RES_MTL FILM, 0.5K,0402,SM,LF	R2909	CRITICAL	NO_VREFMRGN
116S0004	1	RES_MTL FILM, 0.5K,0402,SM,LF	R2911	CRITICAL	NO_VREFMRGN

SYNC\_MASTER=K24\_MLB SYNC\_DATE=04/06/2009

PAGE	TITLE
ESB / DDB3	Prof Margining

FSB/DDR3 VIEL Margining



**Apple Tree**

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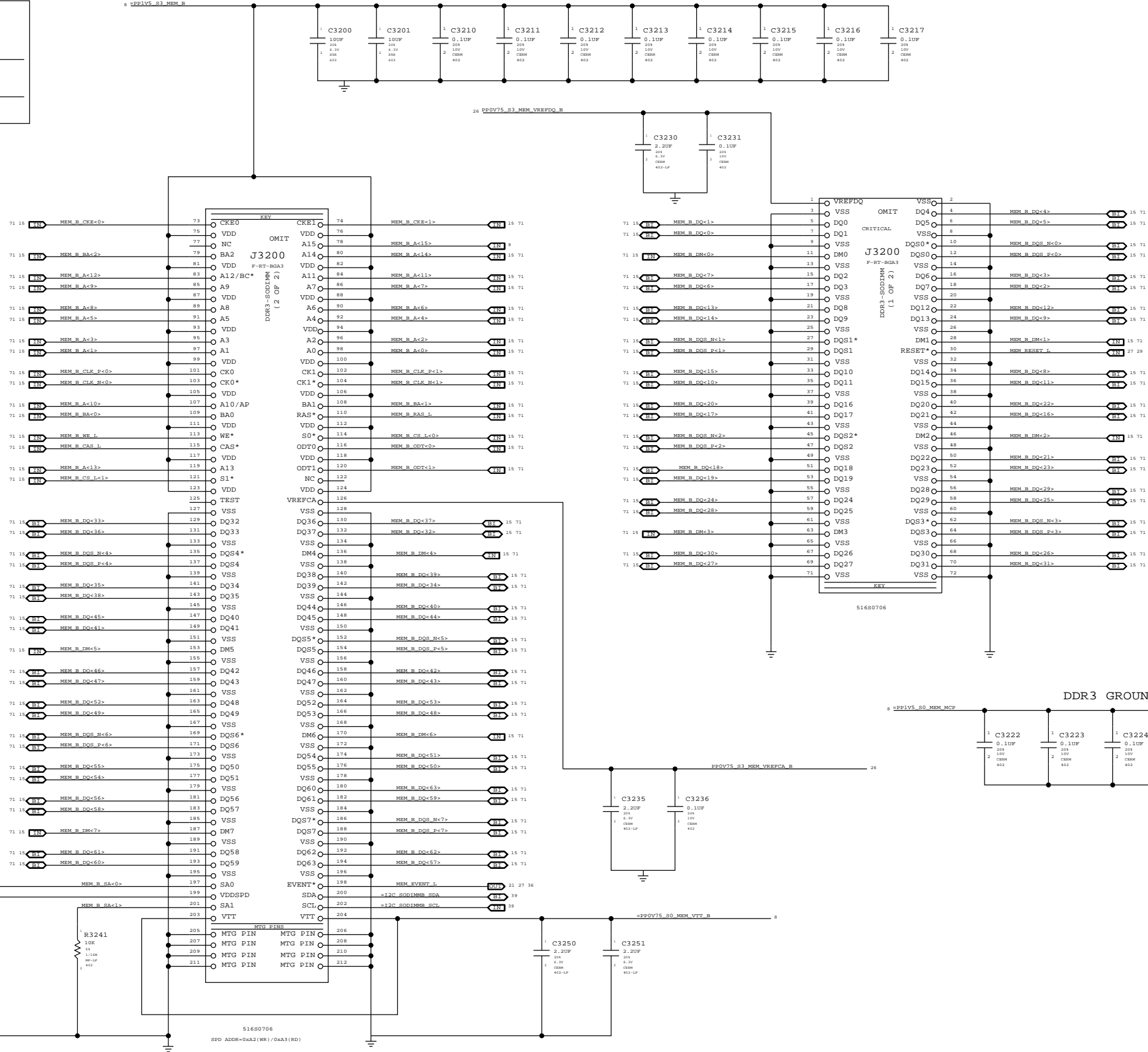
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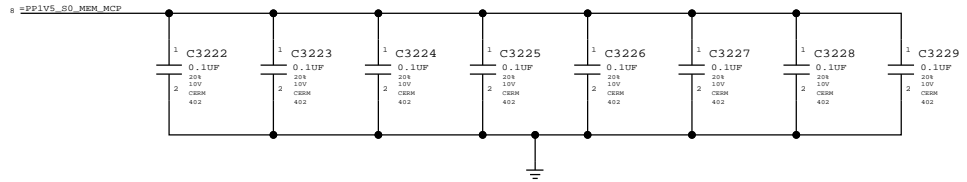
Page Notes

Power aliases required by this page:  
- >PP1V5\_E3\_MEM\_B  
- >PP1V5\_E3\_MEM\_B  
- >PP0V75\_S0\_MEM\_VTT\_B  
- >PP0V75\_S0\_MEM\_VTT\_B  
- >PP0V75\_S0\_MEM\_B (2.5 - 3.3V)  
Signal aliases required by this page:  
- >I2C\_S0D1MMH\_SCL  
- >I2C\_S0D1MMH\_SDA  
ROM options provided by this page:  
(NONE)

DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)



DDR3 GROUND RETURN CAPS (MCP SIDE)



PAGE TITLE		PAGE NUMBER	
DDR3 SO-DIMM Connector B		051-7982 D	
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"Expansion" (bottom) slot

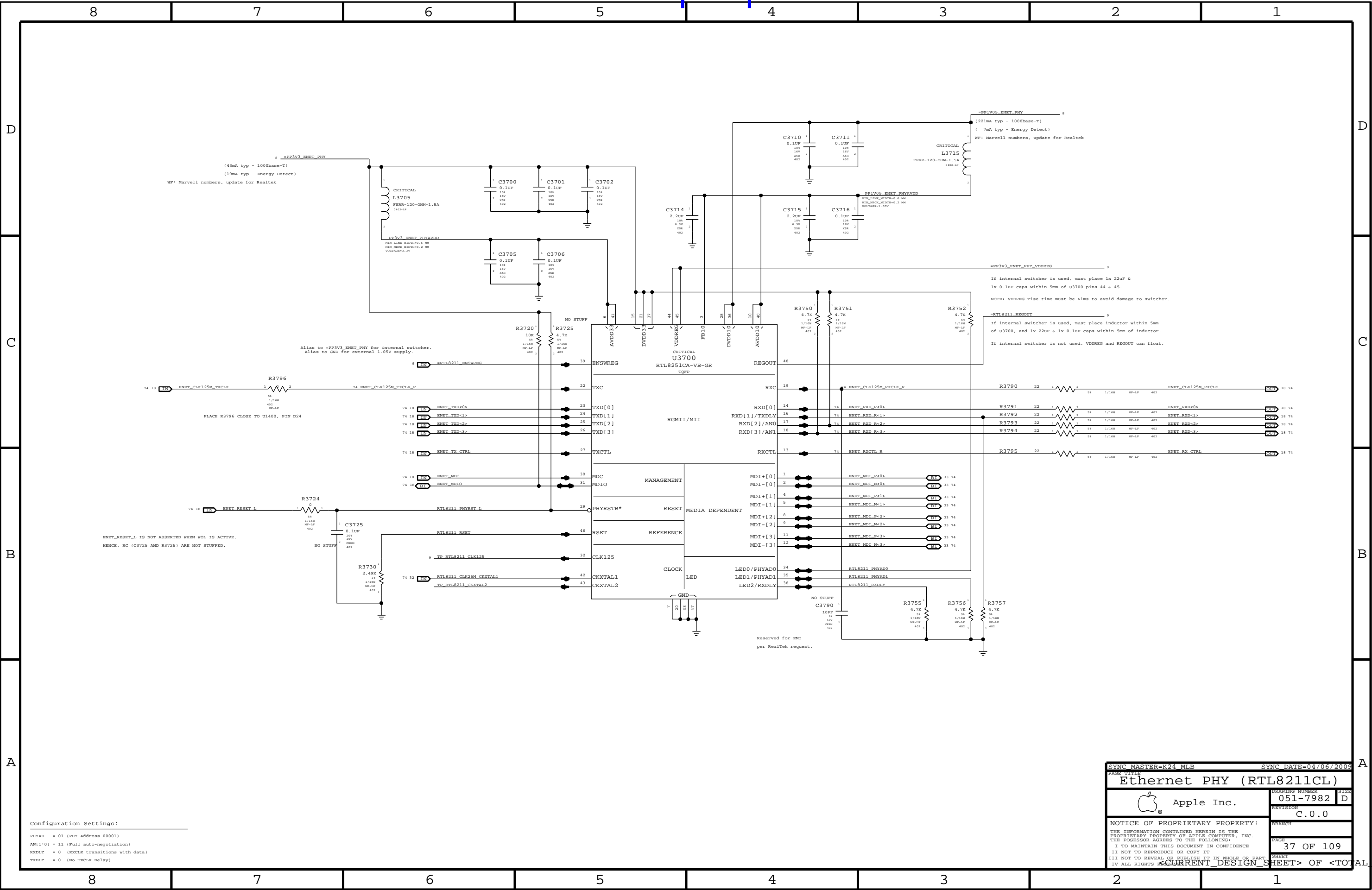







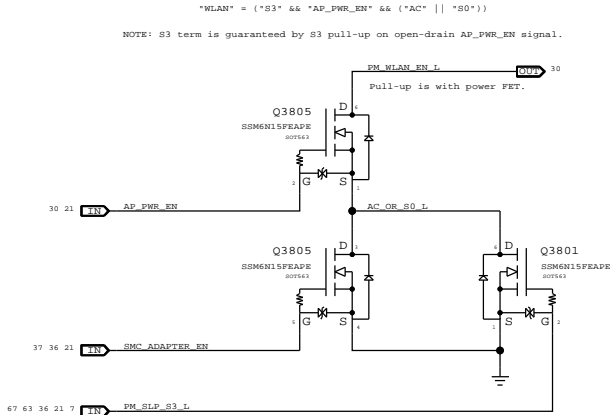
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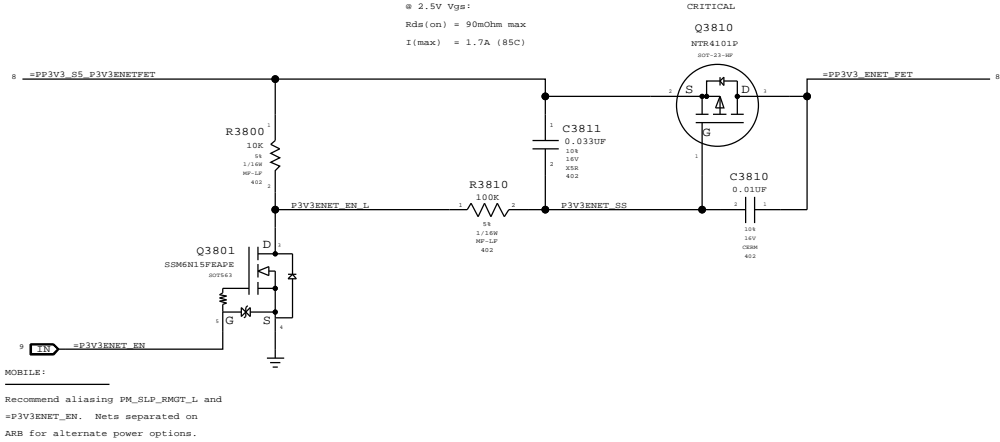


SYNC MASTER=K24 MLB		SYNC DATE=04/06/2009	
PAGE TITLE			
Ethernet PHY (RTL8211CL)			
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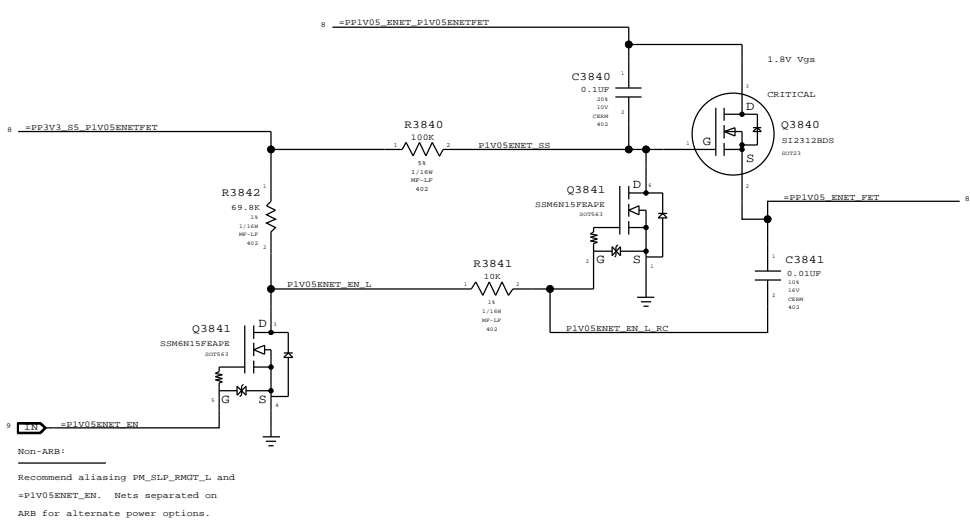
WLAN Enable Generation



3.3V ENET FET

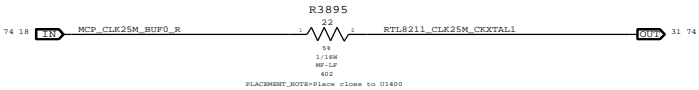


1.05V ENET FET



RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.  
Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.



SYNC MASTER=K24 MLB

SYNC DATE=04/06/2009

Ethernet & AirPort Support

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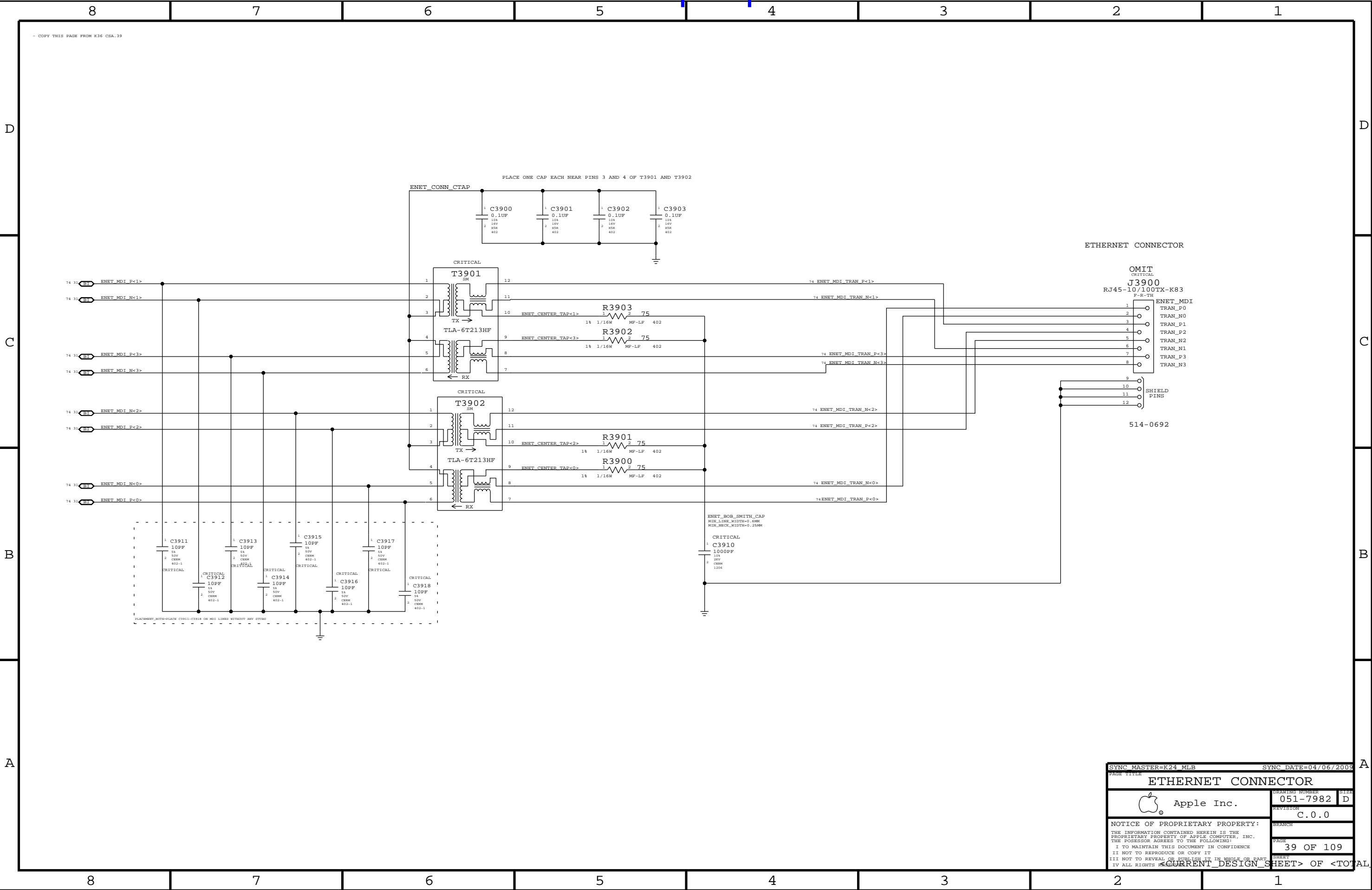
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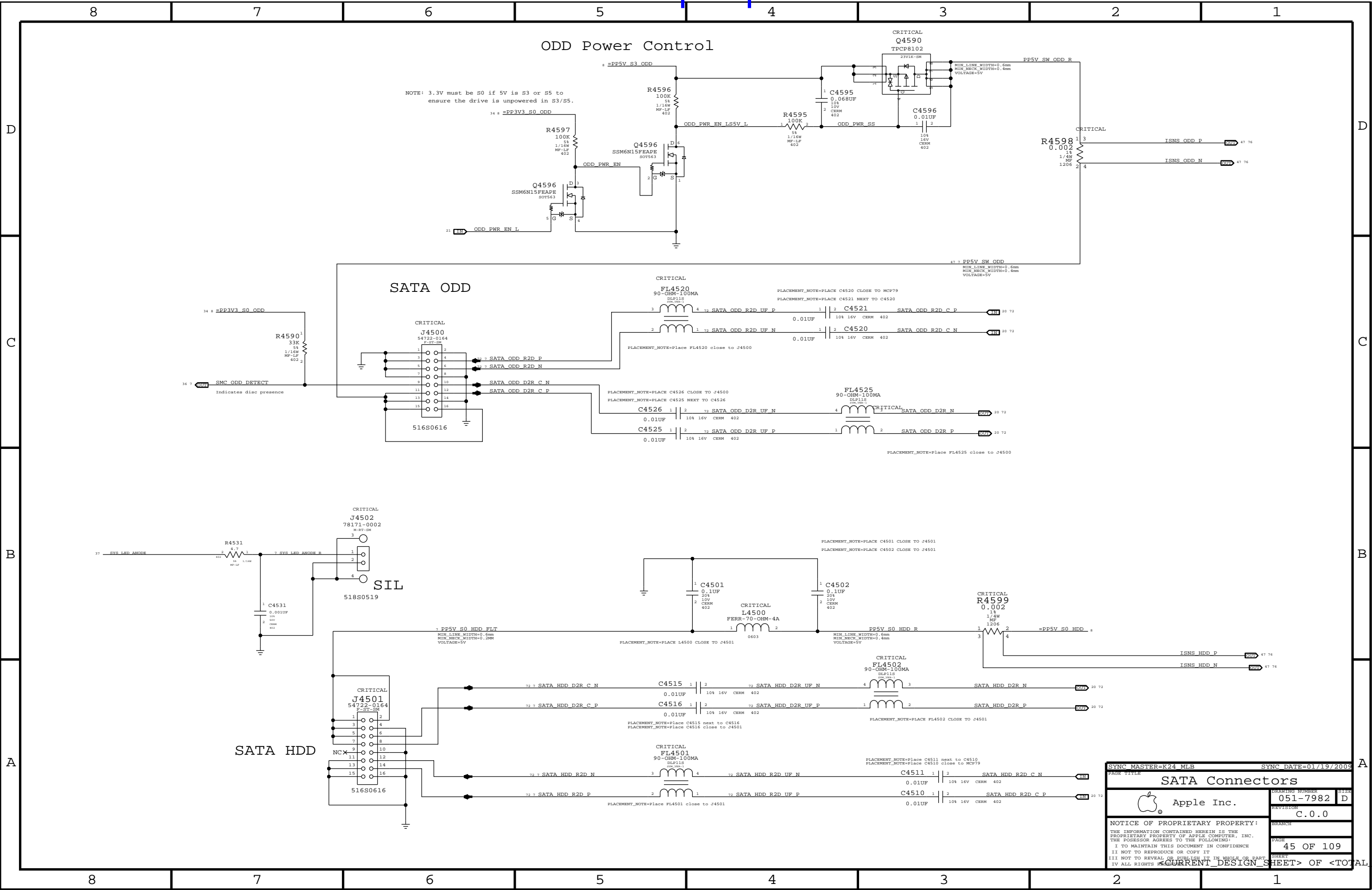
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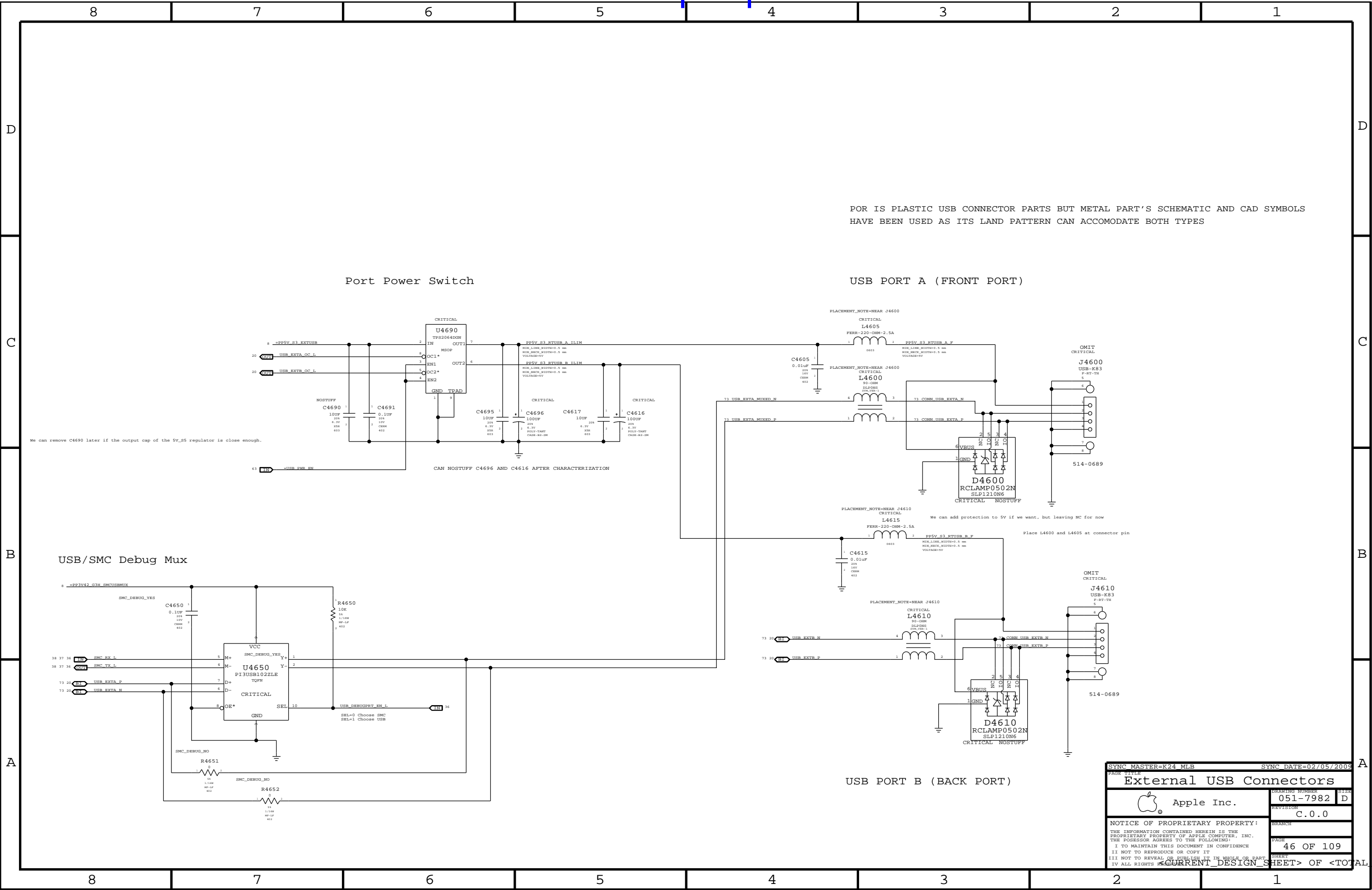
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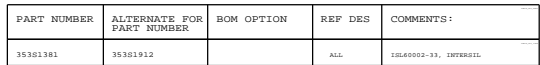
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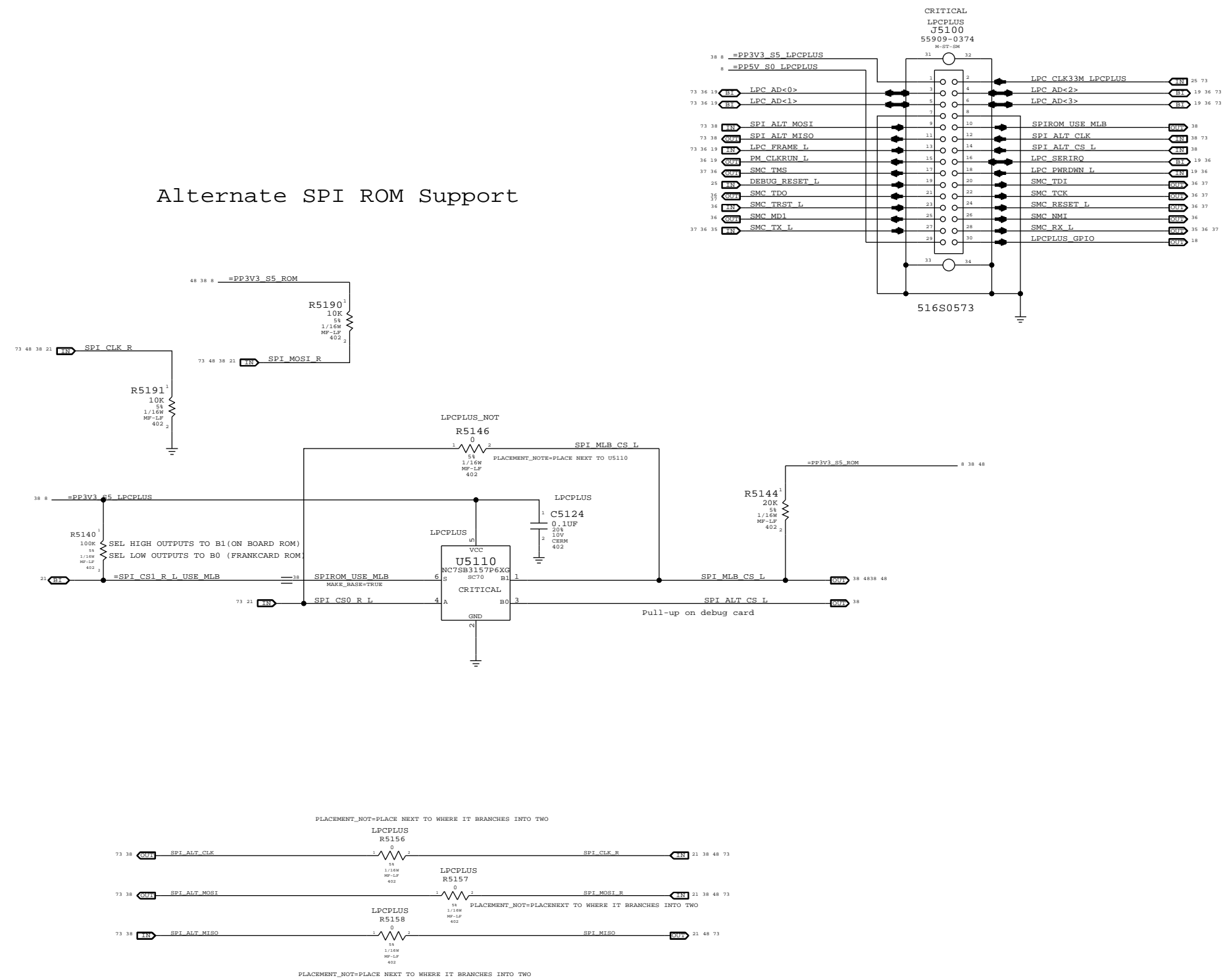


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Alternate SPI ROM Support


LPC+SPI Connector



SYNC MASTER=K24 MLB

SYNC DATE=02/15/2009

LPC+SPI Debug Connector

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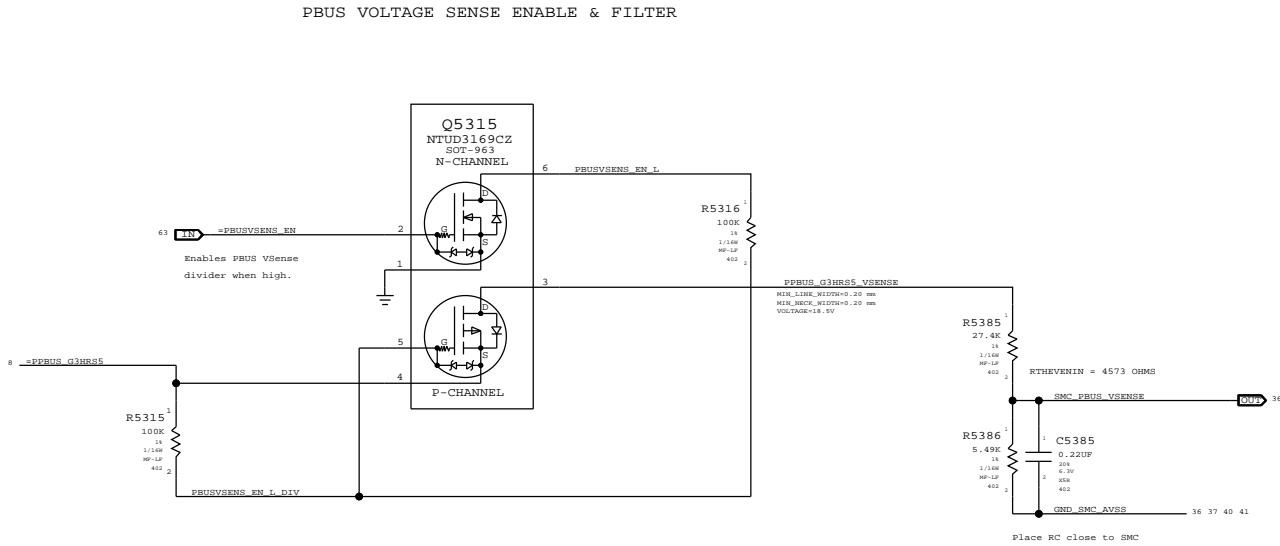
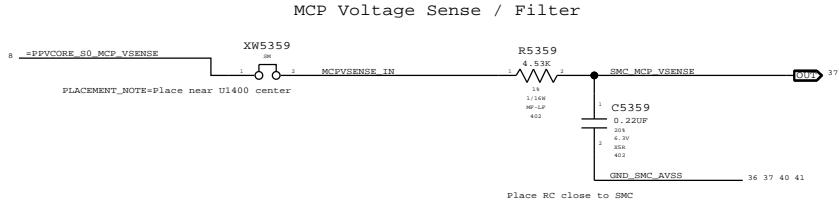
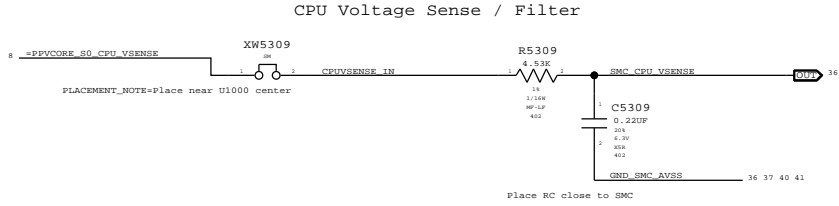
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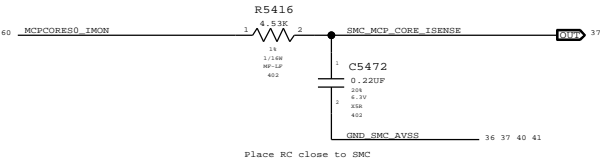
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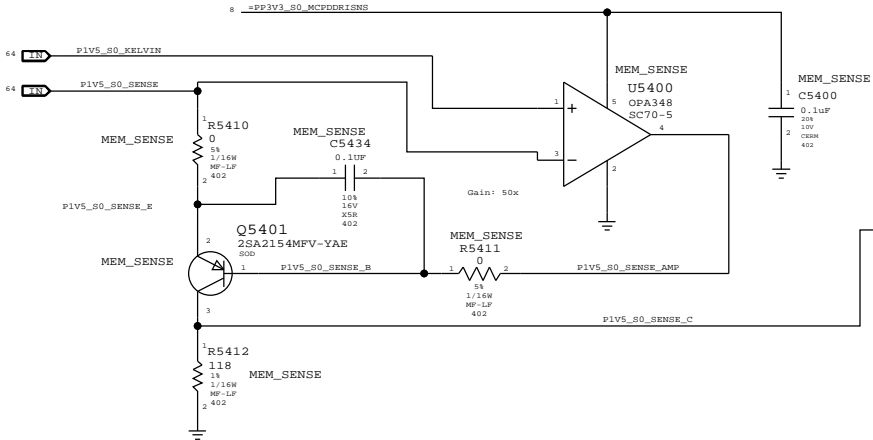
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VOLTAGE SENSING			
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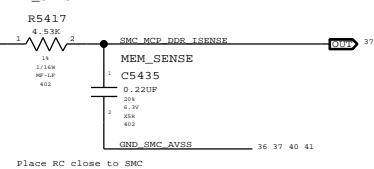
MCP VCore Current Sense Filter



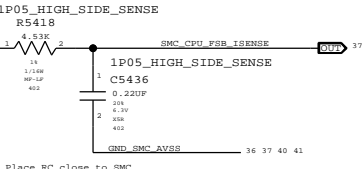
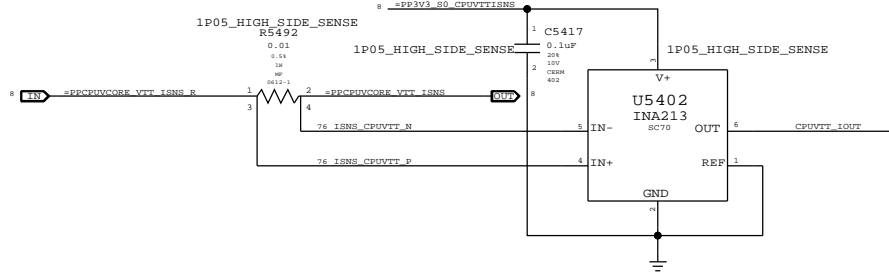
MCP MEM VDD Current Sense



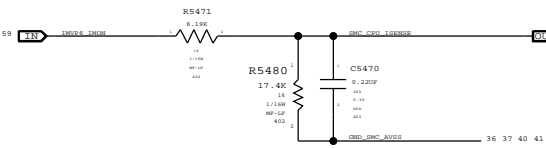
MCP MEM VDD Current Sense Filter



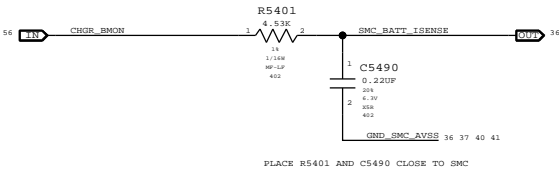
CPU 1.05V AND CPU VCore HIGH SIDE CURRENT SENSE



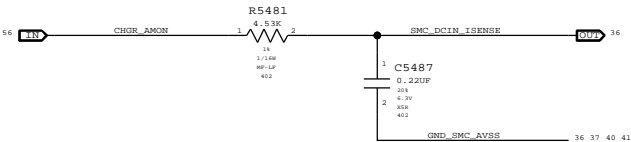
CPU VCore Load Side Current Sense / Filter



DC-IN (BMON) CURRENT SENSE



DC-IN (AMON) CURRENT SENSE



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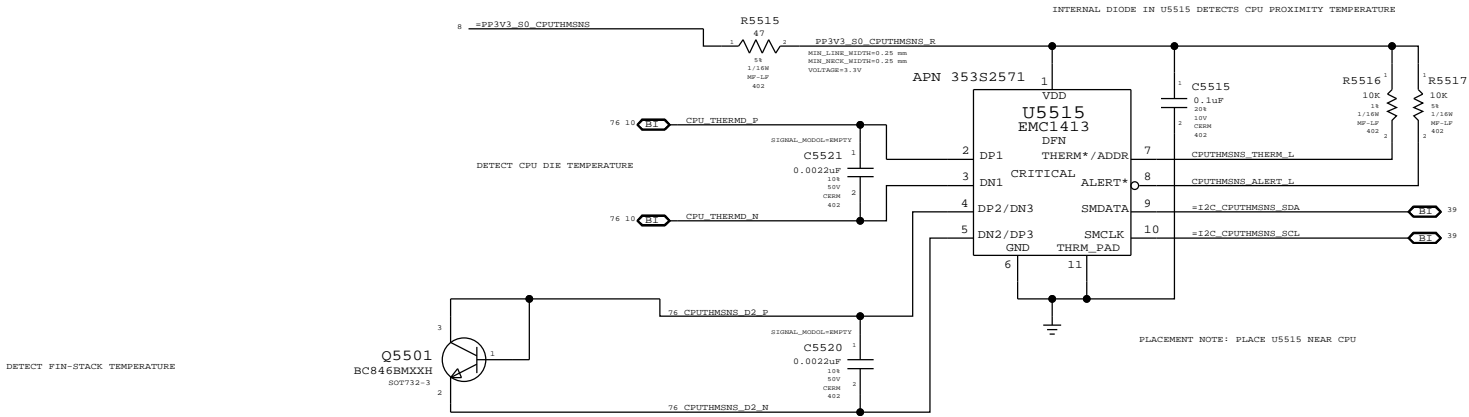
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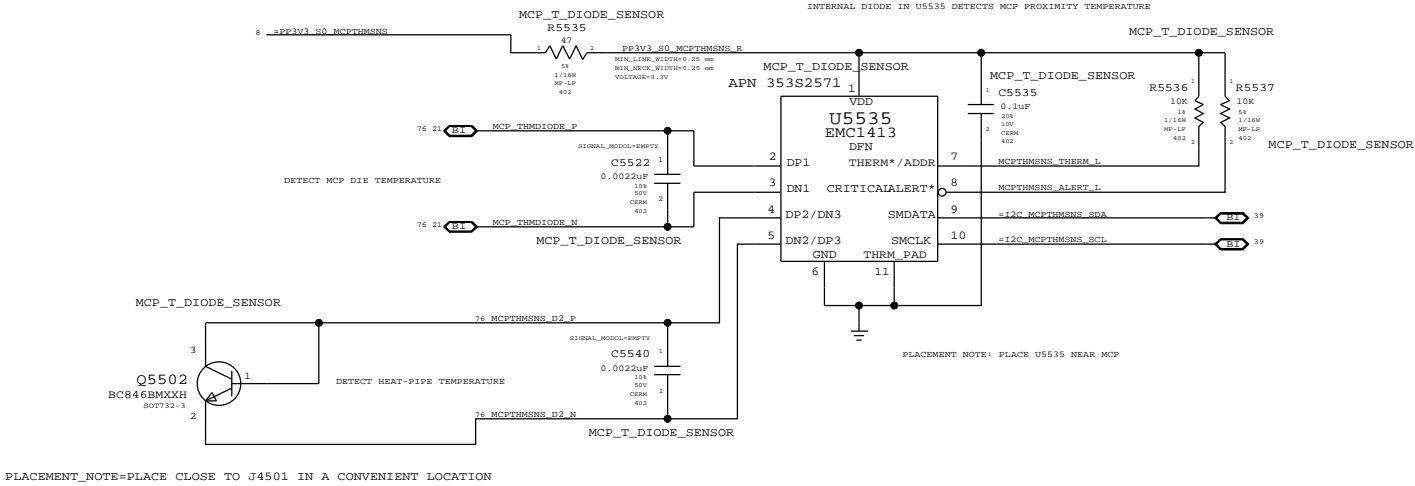
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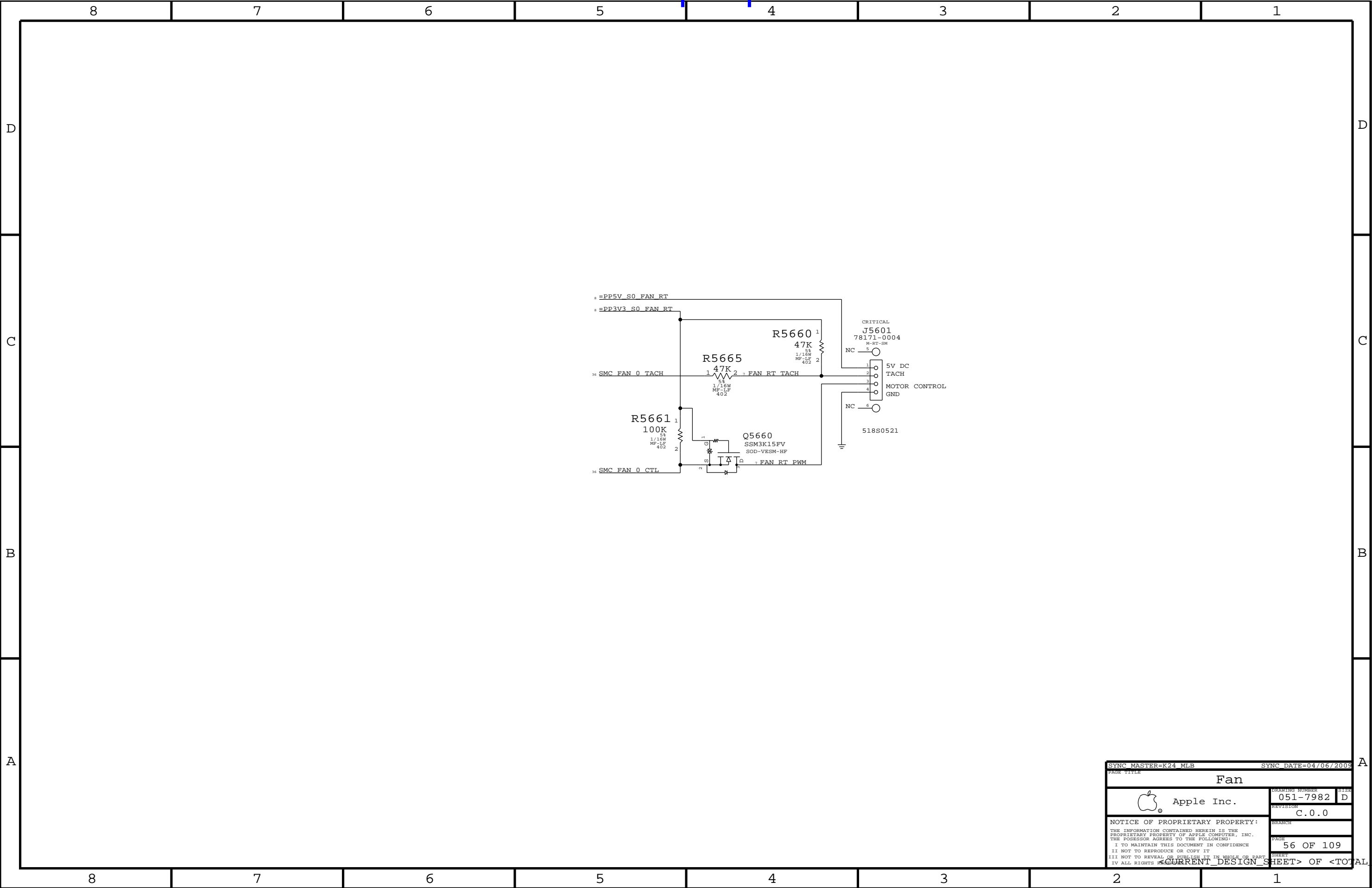
CPU T-Diode Thermal Sensor



MCP T-Diode Thermal Sensor




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Thermal Sensors			
	Apple Inc.		DRAWING NUMBER
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SYNC DATE=04/06/2009

Fan

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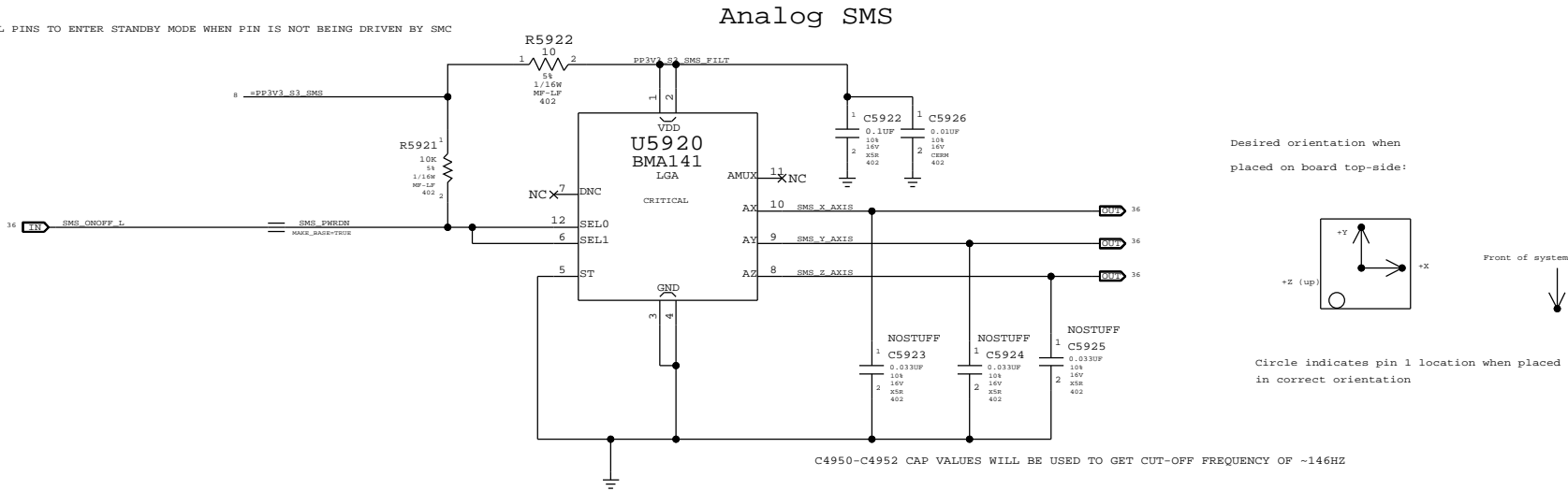
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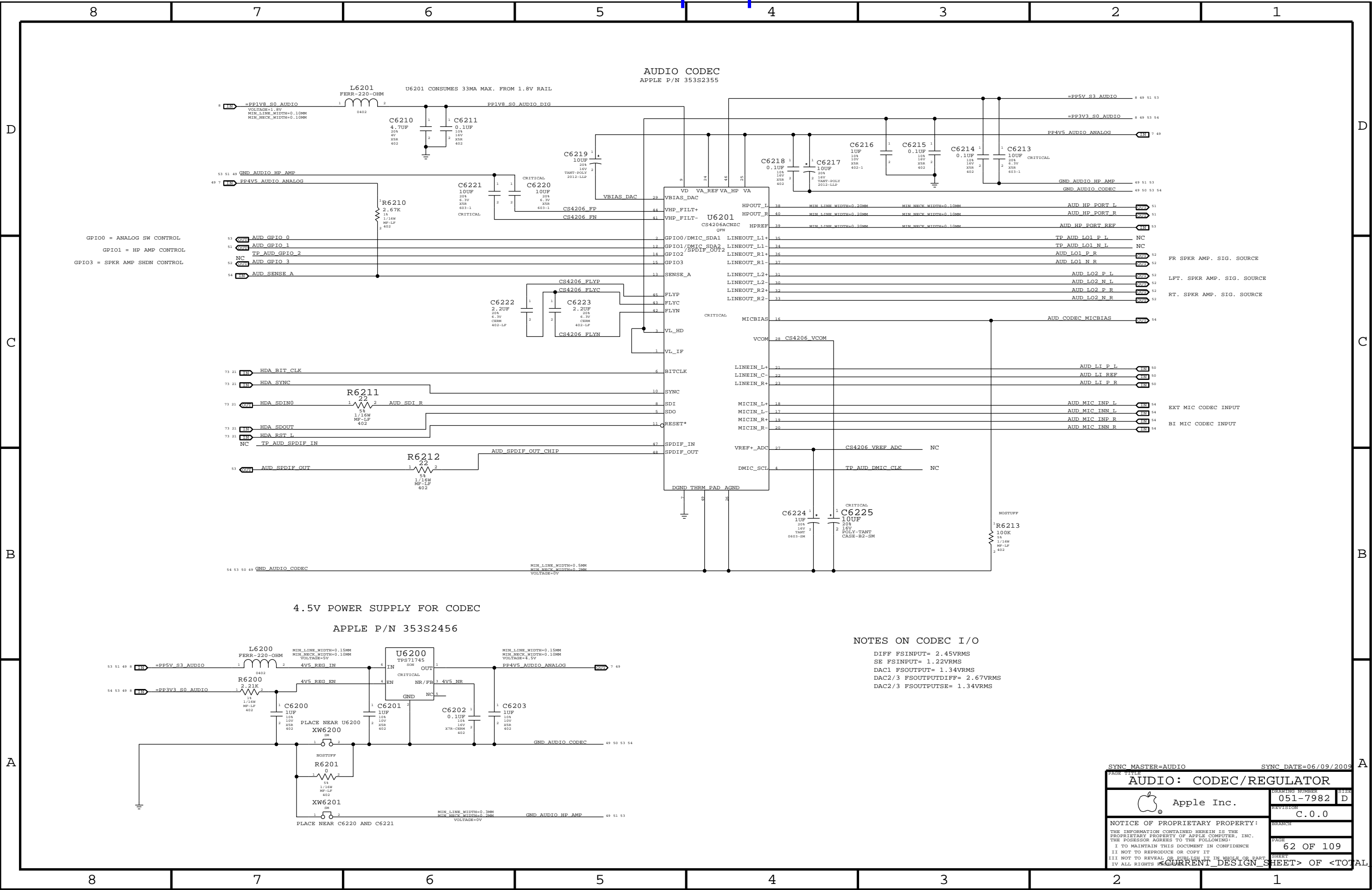
R5921 PULLS UP SEL PINS TO ENTER STANDBY MODE WHEN PIN IS NOT BEING DRIVEN BY SMC



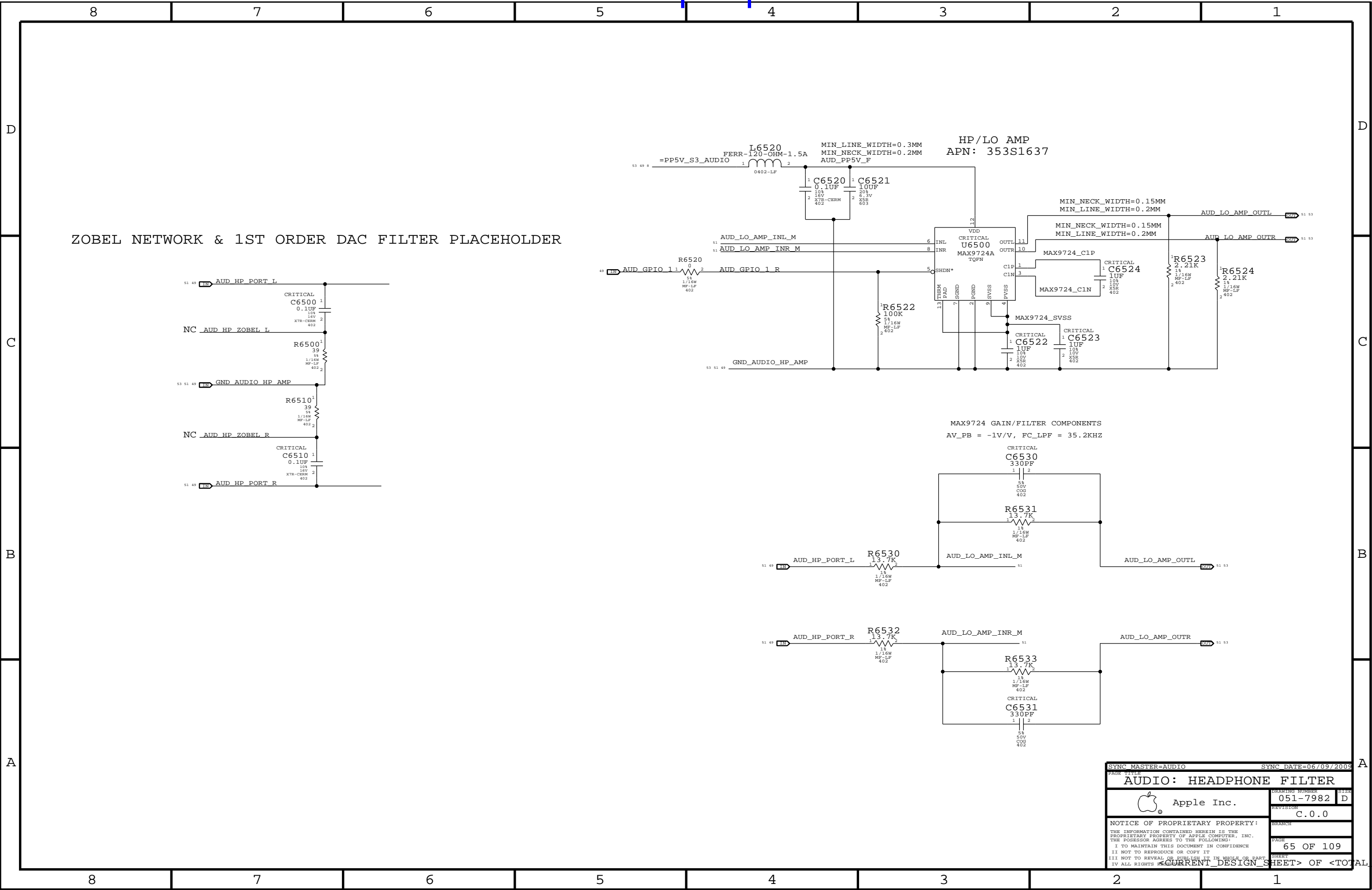












## C

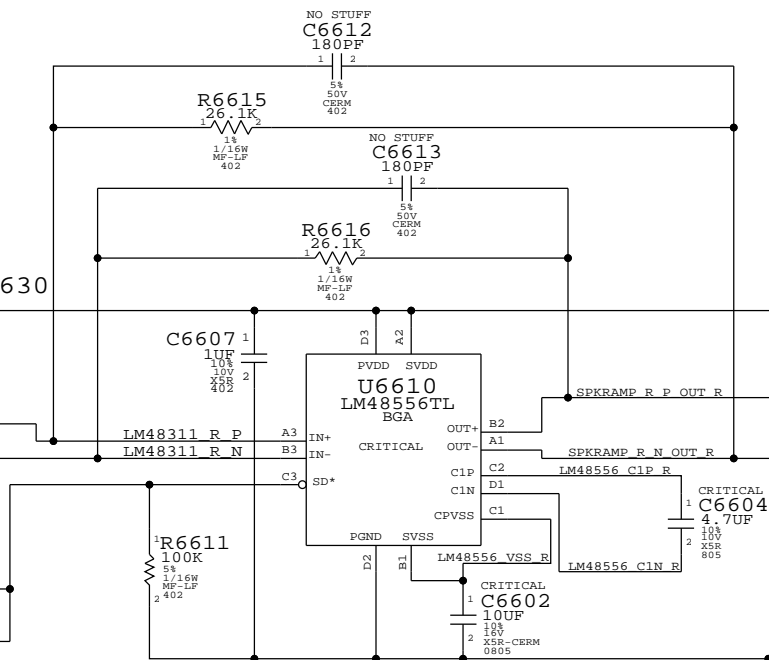
B

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```

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MIN_NECK_WIDTH=0.20 MM
SPKRAMP R P OUT
7 53
MIN_LINE_WIDTH=0.30 mm
MIN_NECK_WIDTH=0.20 MM
SPKRAMP R N OUT
7 53

```



1 CRITICAL  
1 C6601  
10UF  
18V  
2 XSR-CERM  
0805

OMIT  
R6612  
6.8  
1 2

5%  
1/8W  
MF-LP  
805

MIN\_LINE\_WIDTH=0.30 mm  
MIN\_NECK\_WIDTH=0.20 MM  
SPKRAMP R P OUT 7 53

OMIT  
R6617  
6.8  
1 2

5%  
1/8W  
MF-LP  
805

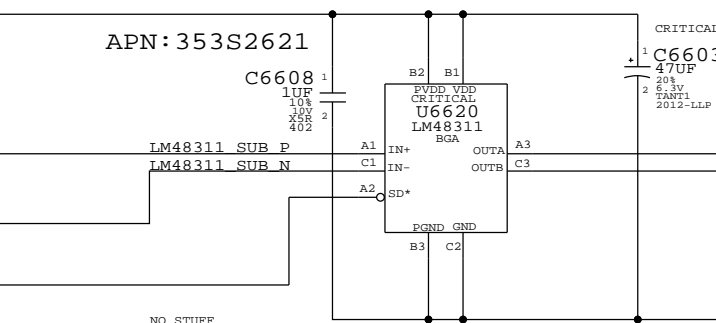
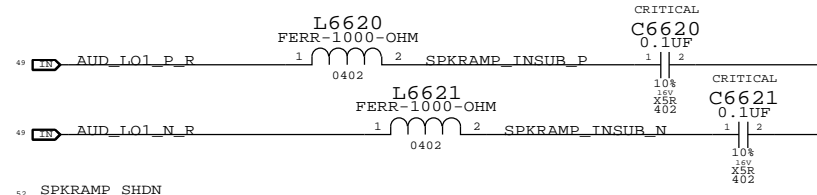
MIN\_LINE\_WIDTH=0.30 mm  
MIN\_NECK\_WIDTH=0.20 MM  
SPKRAMP R N OUT 7 53

CRITICAL

1 C6603  
47UF  
20%  
6.3V  
TANT1

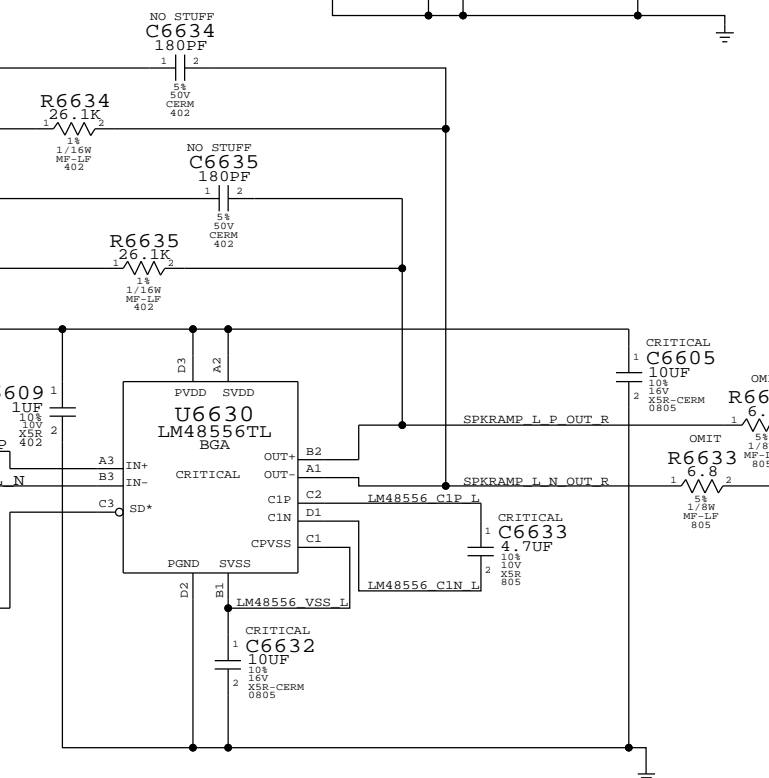
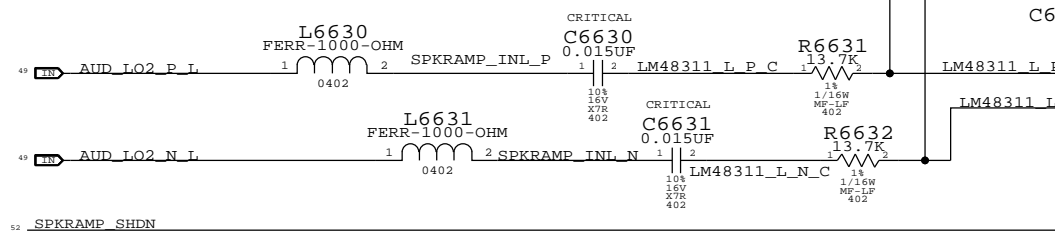
```
MIN_LINE_WIDTH=0.30 mm
MIN_NECK_WIDTH=0.20 MM
SPKRAMP SUB P OUT 7 53
```

```
MIN_LINE_WIDTH=0.30 mm
MIN_NECK_WIDTH=0.20 MM
SPKRAMP SUB N OUT
```



```
MIN_LINE_WIDTH=0.30 mm
MIN_NECK_WIDTH=0.20 MM
SPKRAMP L P OUT
```

```
MIN_LINE_WIDTH=0.30 mm
MIN_NECK_WIDTH=0.20 MM
SPKRAMP_L_N_OUT
```



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051		300

DRAWING NUMBER	SIZE
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051-7982	D
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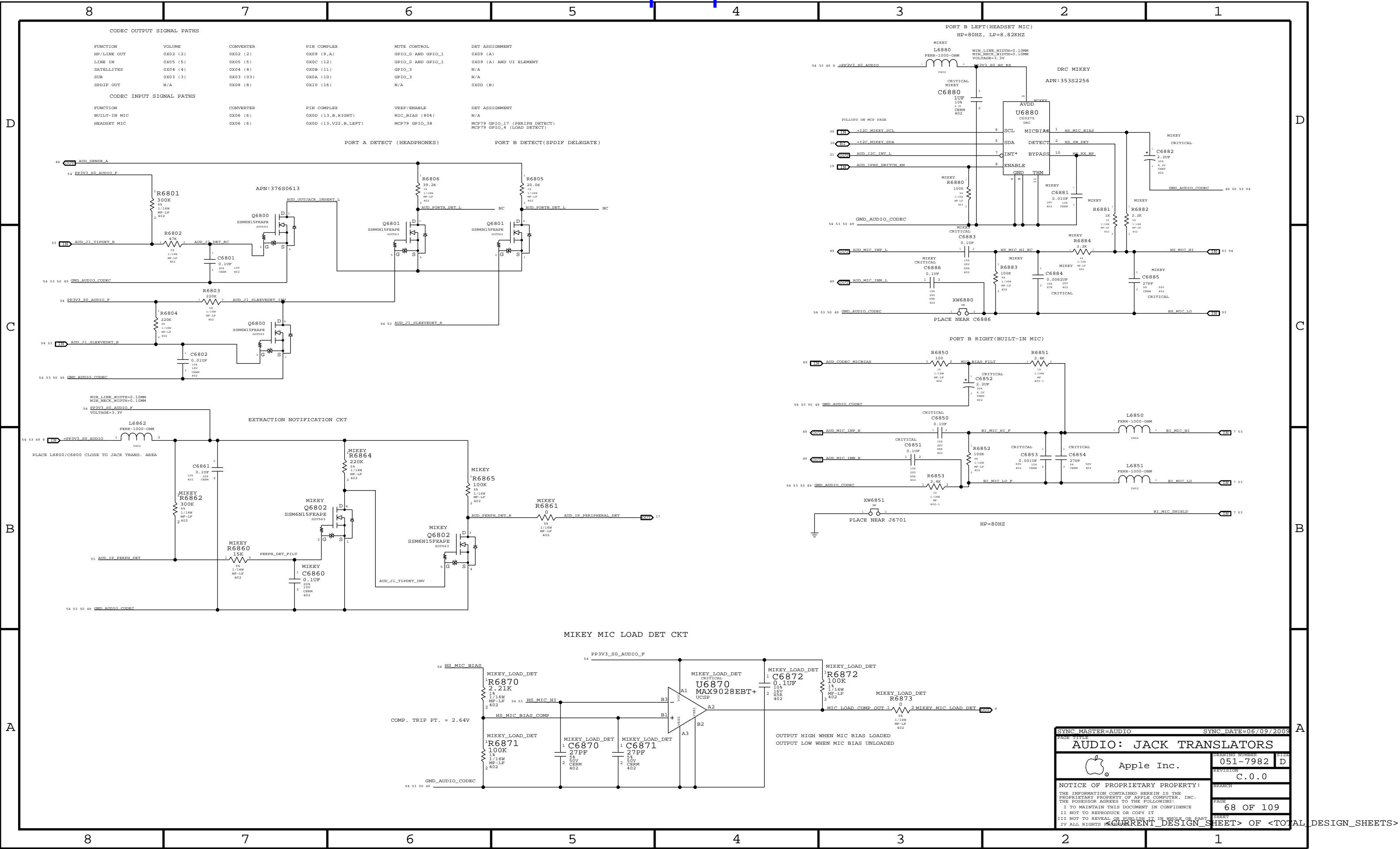
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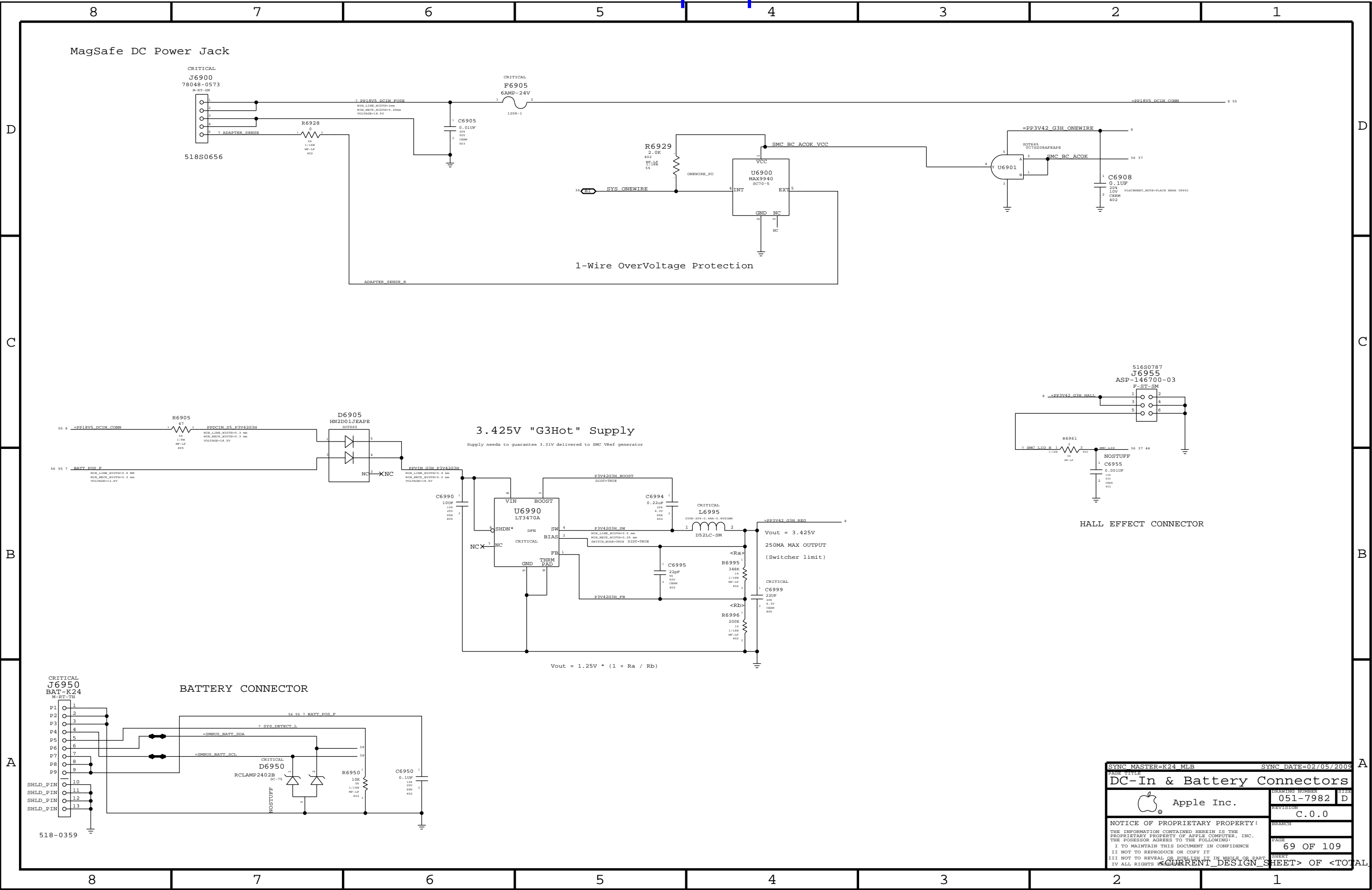
AUDIO: JACK TRANSLATORS

Apple Inc.

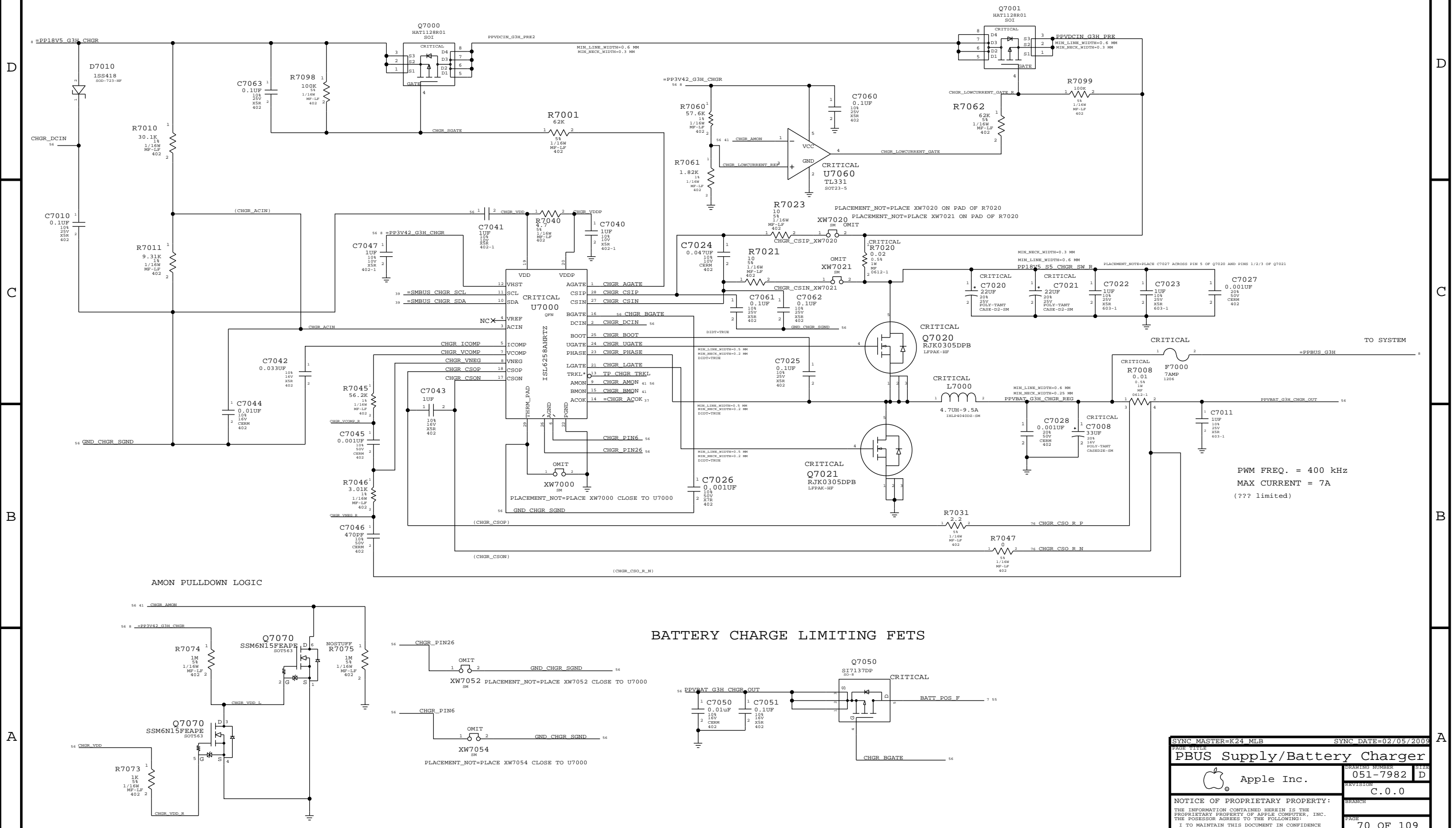
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PBUS SUPPLY / BATTERY CHARGER




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SYNC DATE=02/05/2009

PAGE TITLE

PBUS Supply/Battery Charger

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C

## C

$$V_{OUT} = (2 * RC / RD) + 2$$



B

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SEPERATED MASTER PGOOD FOR BOTH 5V AND 3V3.

## D

BA

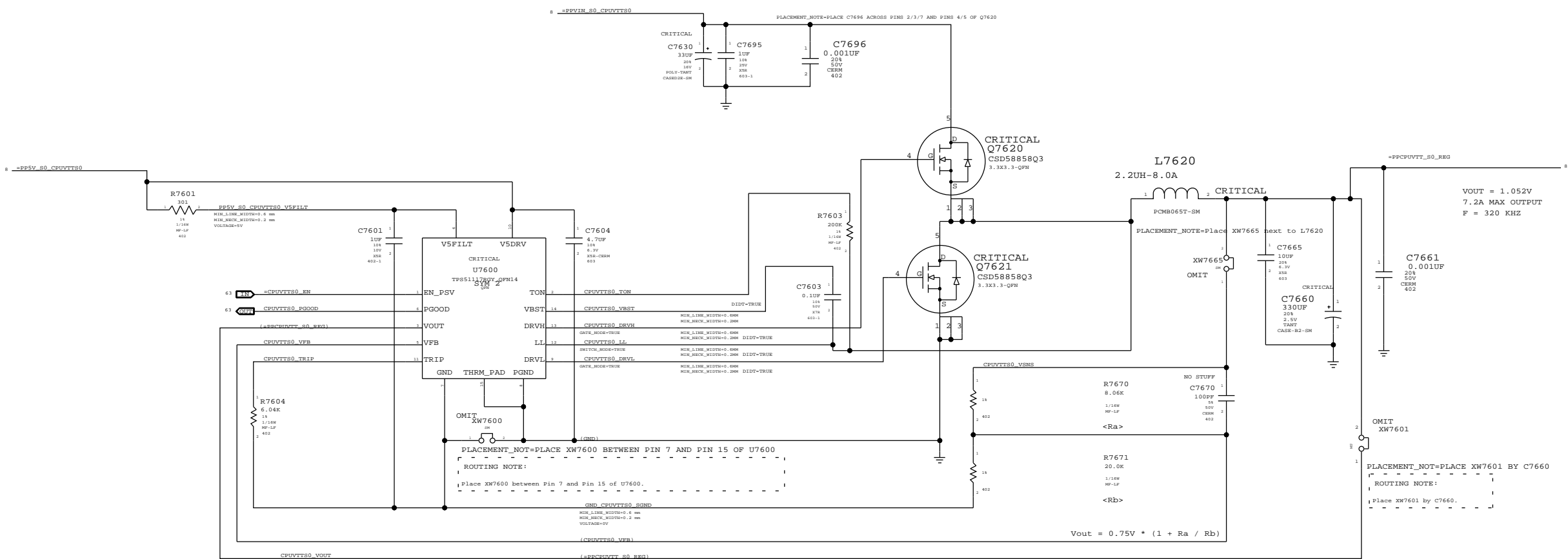






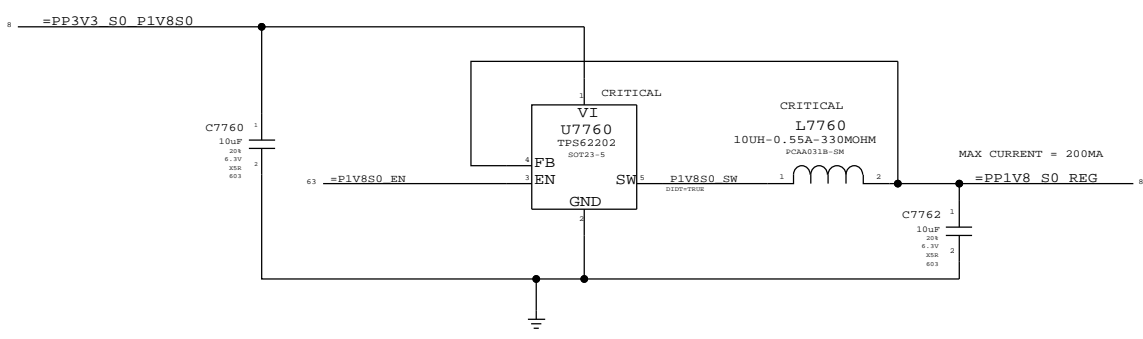
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000	+1.05V
001	+1.00V
010	+0.95V
011	+0.90V
100	+0.85V
101	+0.80V
110	+0.75V
111	+0.70V

CPUVTT POWER SUPPLY

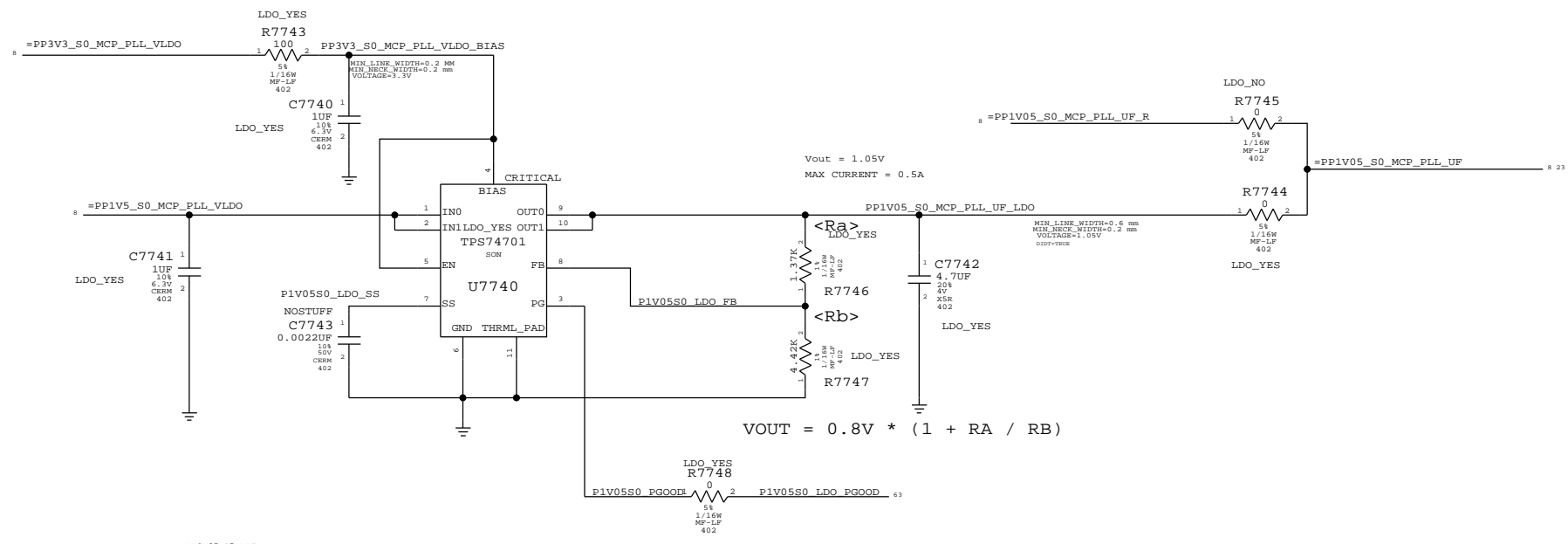


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PAGE TITLE		CPU VTT(1.05V) SUPPLY	
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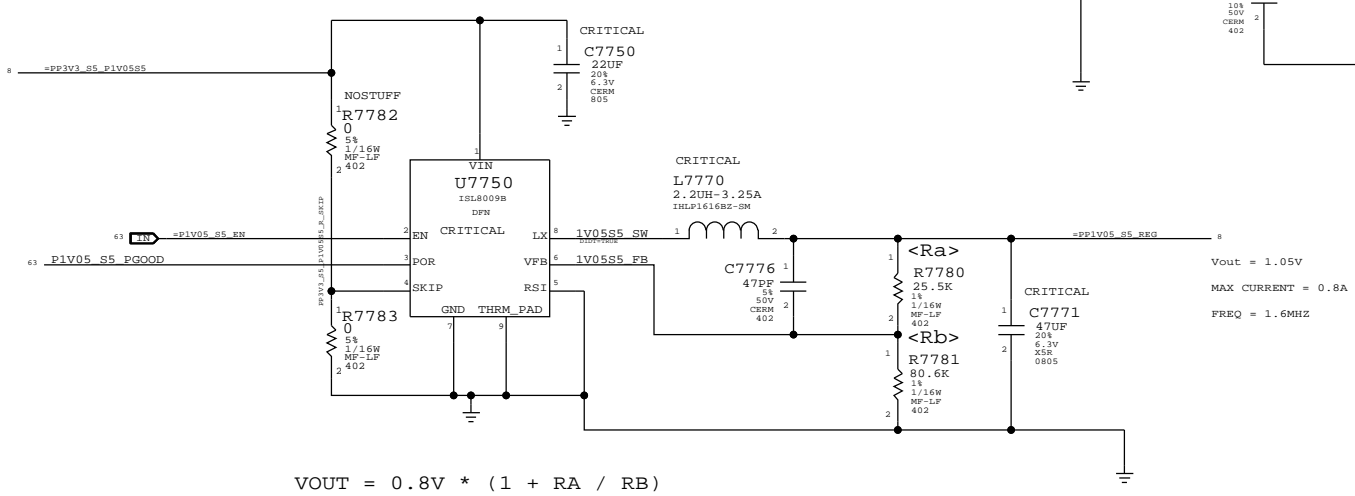
1.8V S0 SWITCHER



1.05V S0 PLL LDO



MCP 1.05V S5 (AUXC) SUPPLY



SYNC MASTER=K24 MLB

SYNC DATE=03/24/2009

MISC POWER SUPPLIES

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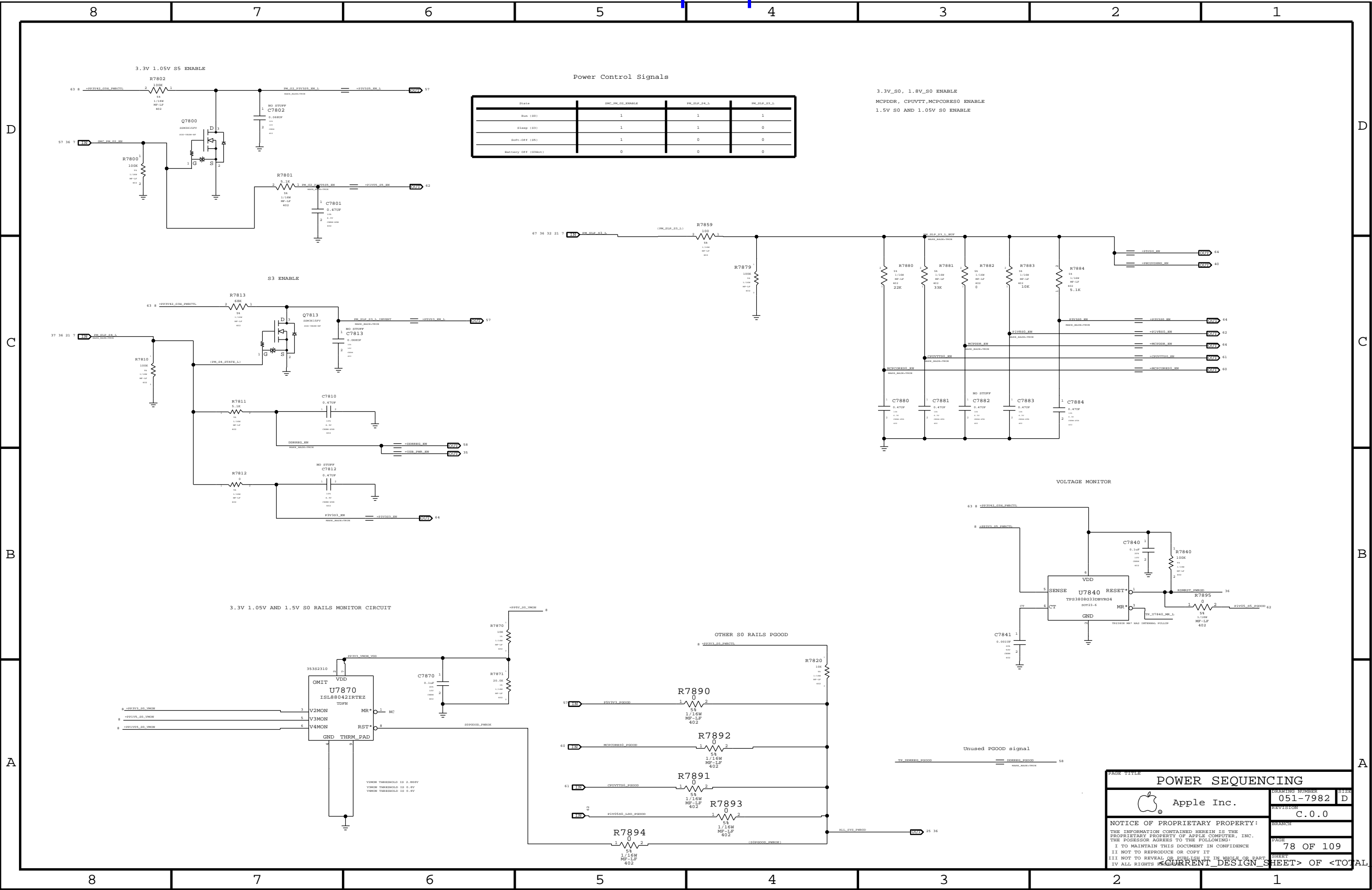
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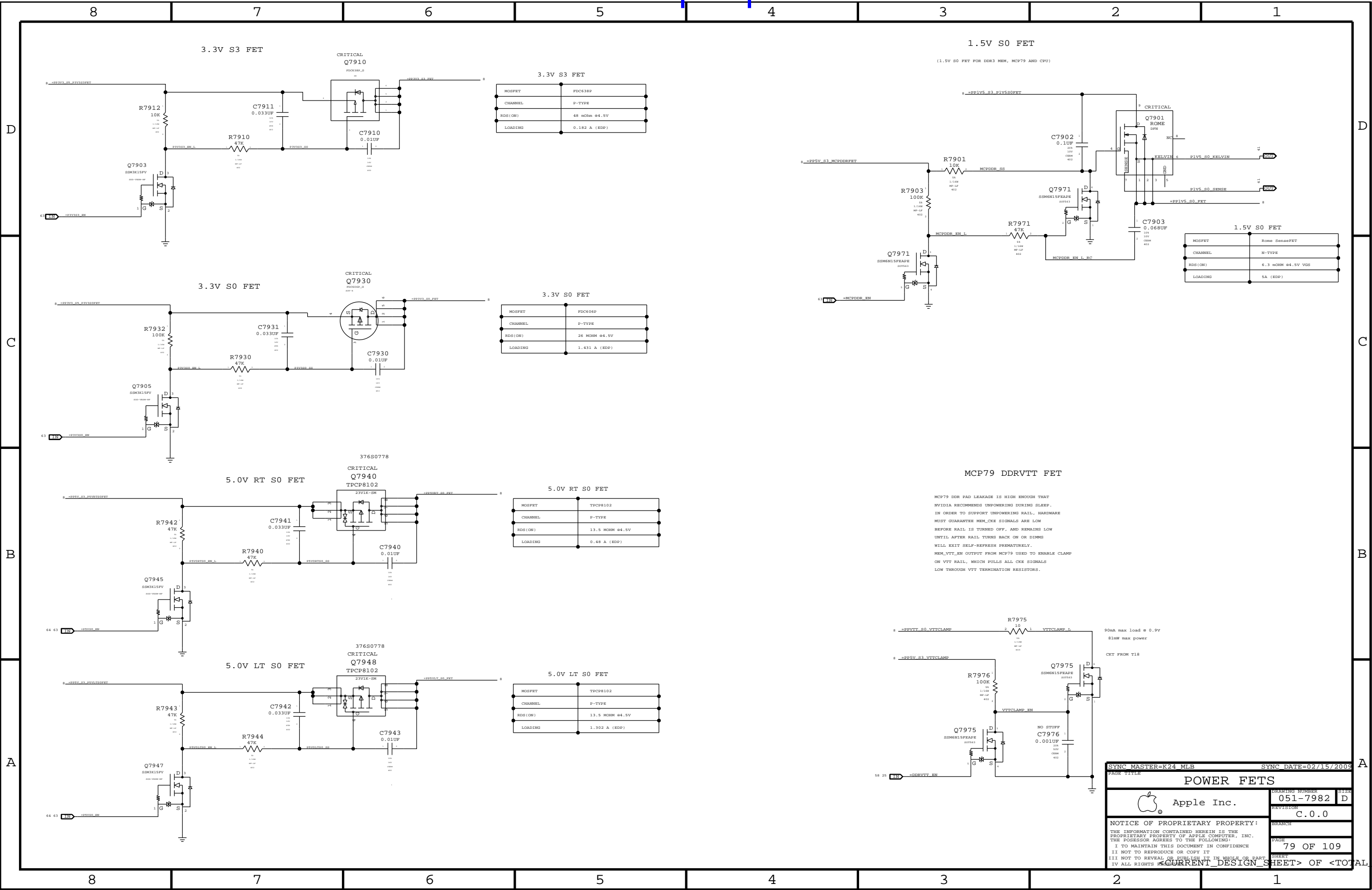
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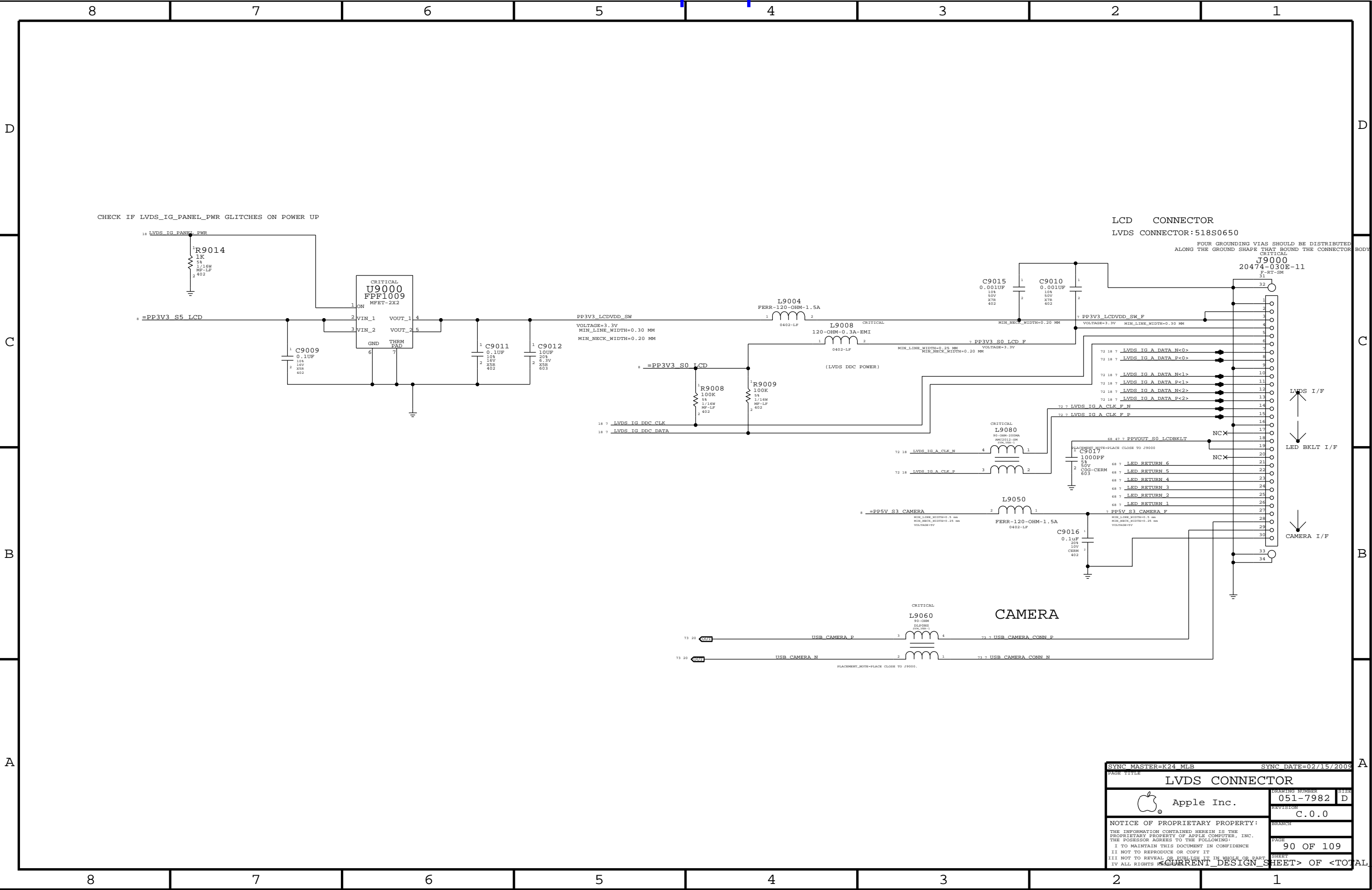
1

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SYNC MASTER=K24 MLB

SYNC DATE=02/15/2009

LVDS CONNECTOR

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051-7982 D

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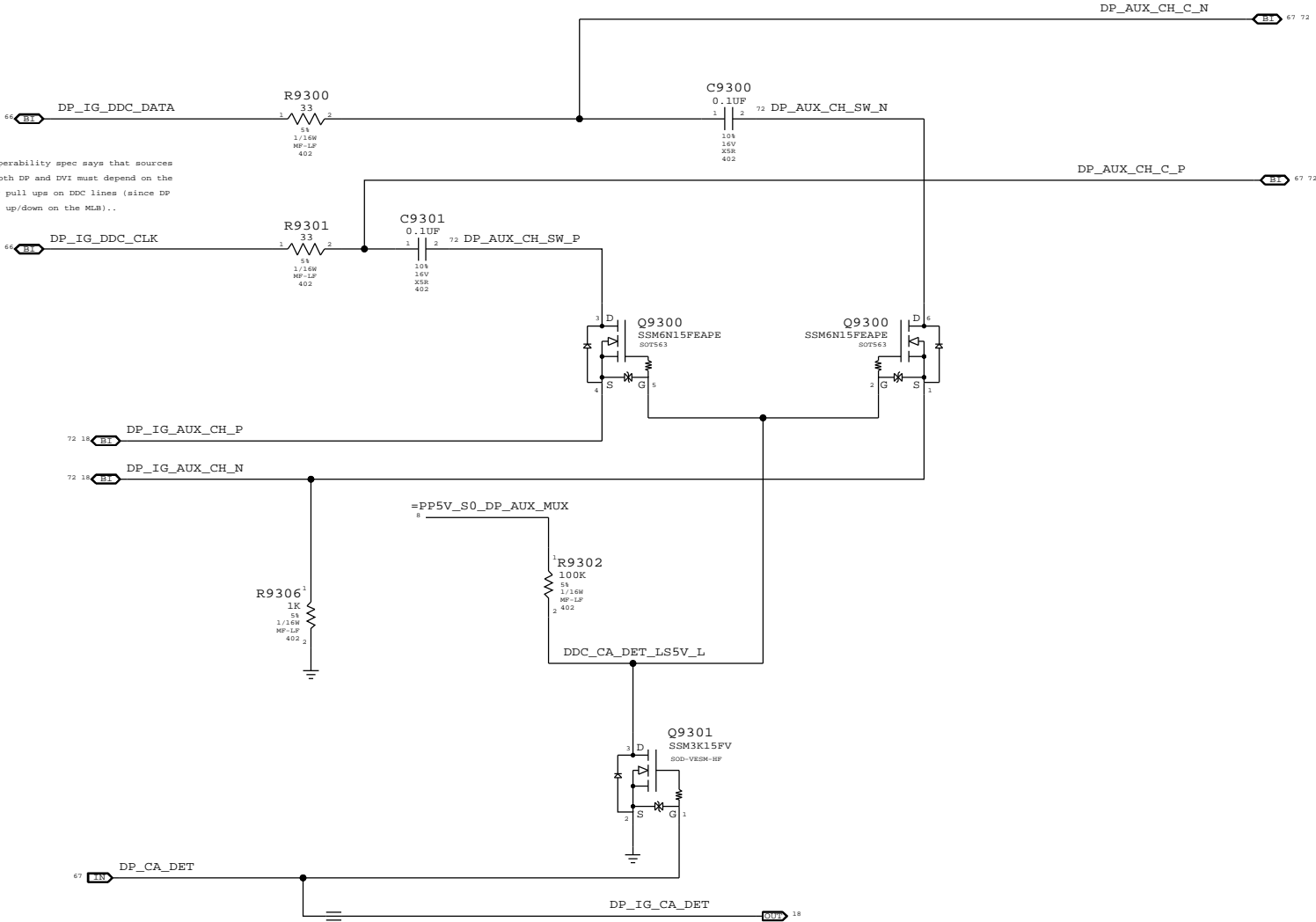
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
B

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18	=MCP_HDMI_HPD	DP_HPD	MAKE_BIAS=TRUE	67	
18	=MCP_HDMI_DDC_CLK	DP_IG_DDC_CLK	MAKE_BIAS=TRUE	66	
18	=MCP_HDMI_DDC_DATA	DP_IG_DDC_DATA	MAKE_BIAS=TRUE	66	

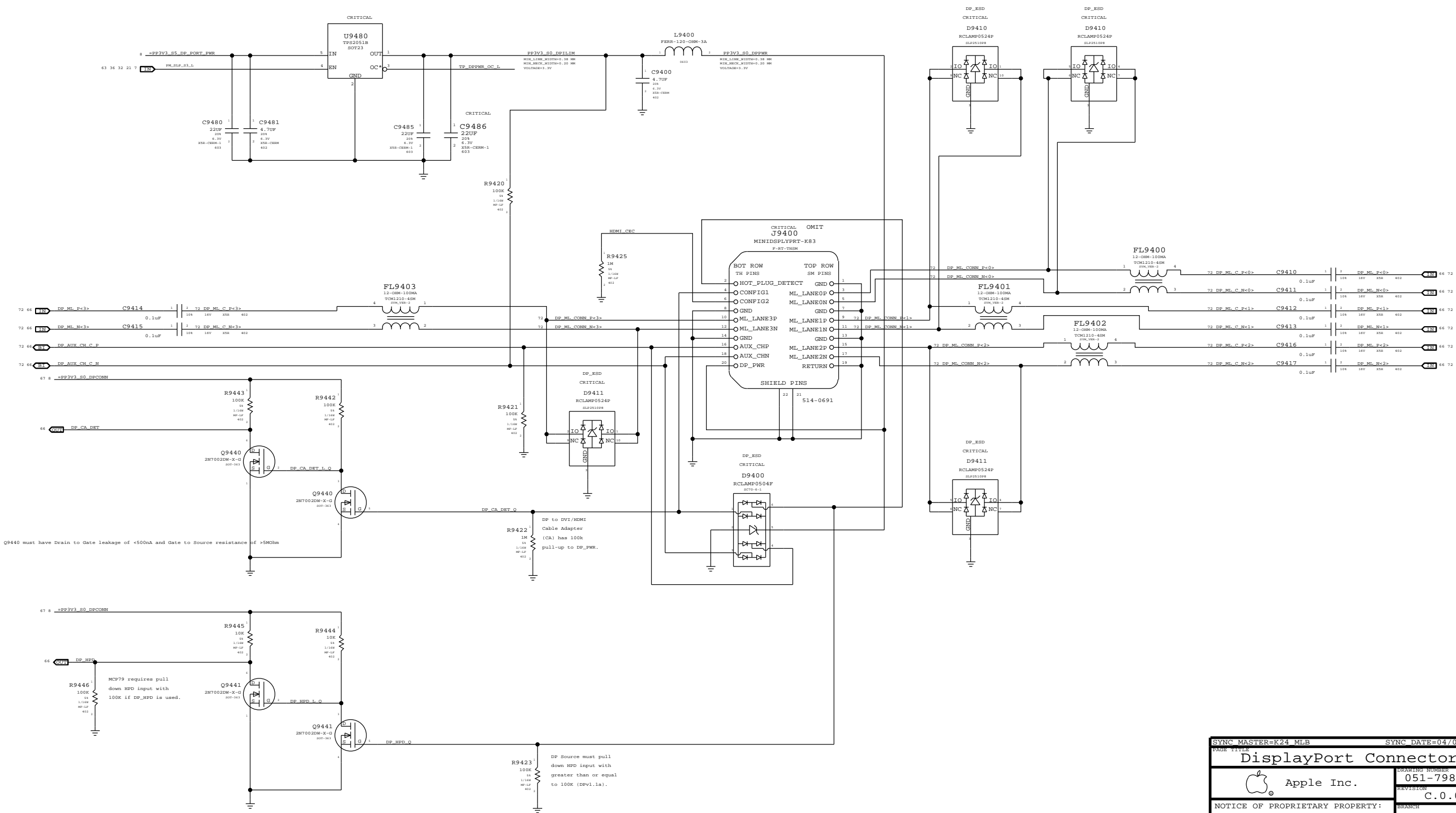
Display Port Interoperability spec says that sources or sinks which do both DP and DVI must depend on the external adapter for pull ups on DDC lines (since DP AUX CH has 100K pull up/down on the MLB)..



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DISPLAYPORT SUPPORT			
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POR IS PLASTIC MINI DP CONNECTOR BUT METAL PART'S SCHEMATIC AND CAD SUMBOLS  
HAVE BEEN USED BEACUSE ITS LAND PATTERN CAN ACCOMODATE BOTH TYPES

Port Power Switch



SYNC MASTER=K24 MLB

SYNC DATE=04/06/2009

DisplayPort Connector

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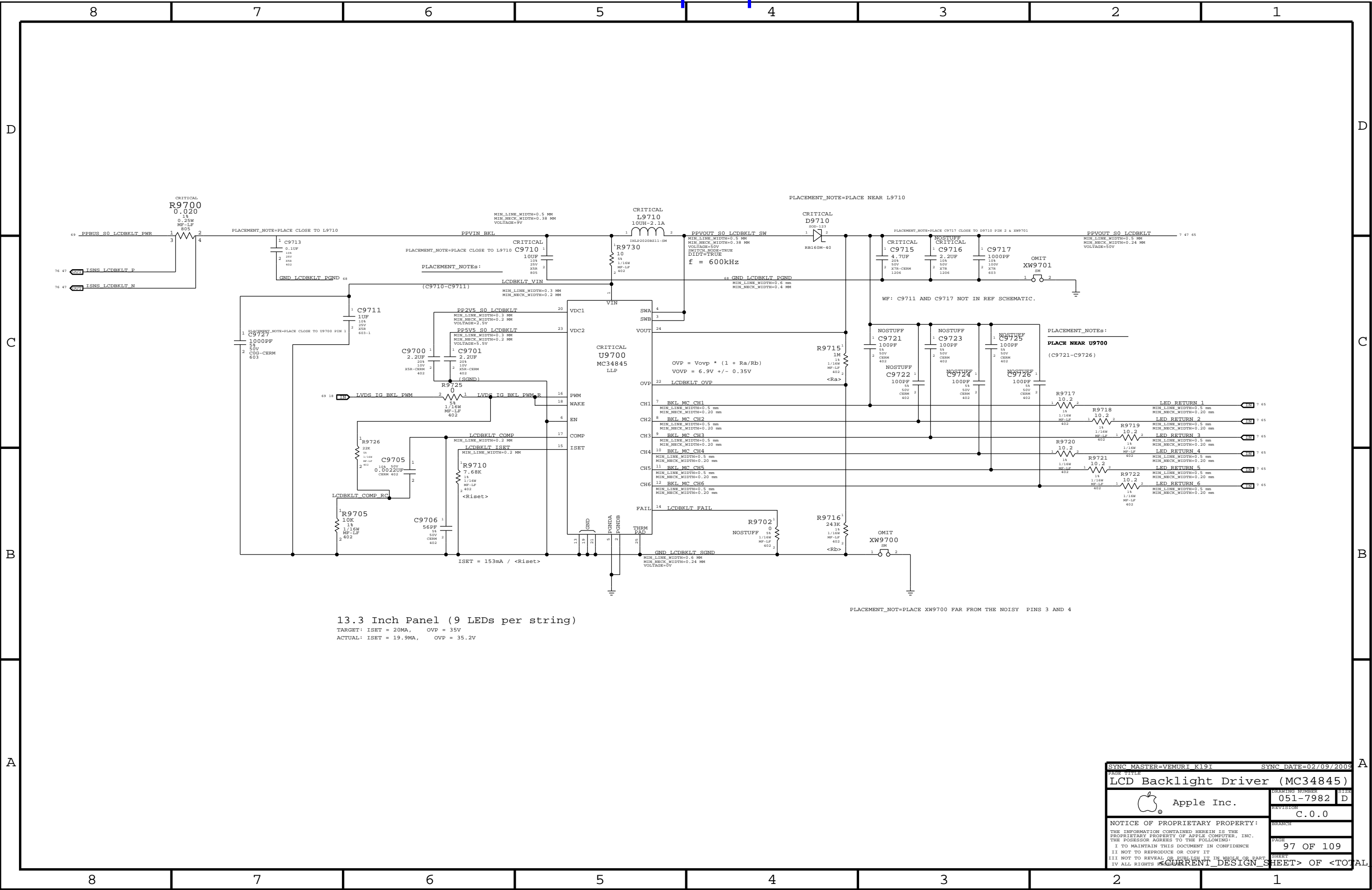
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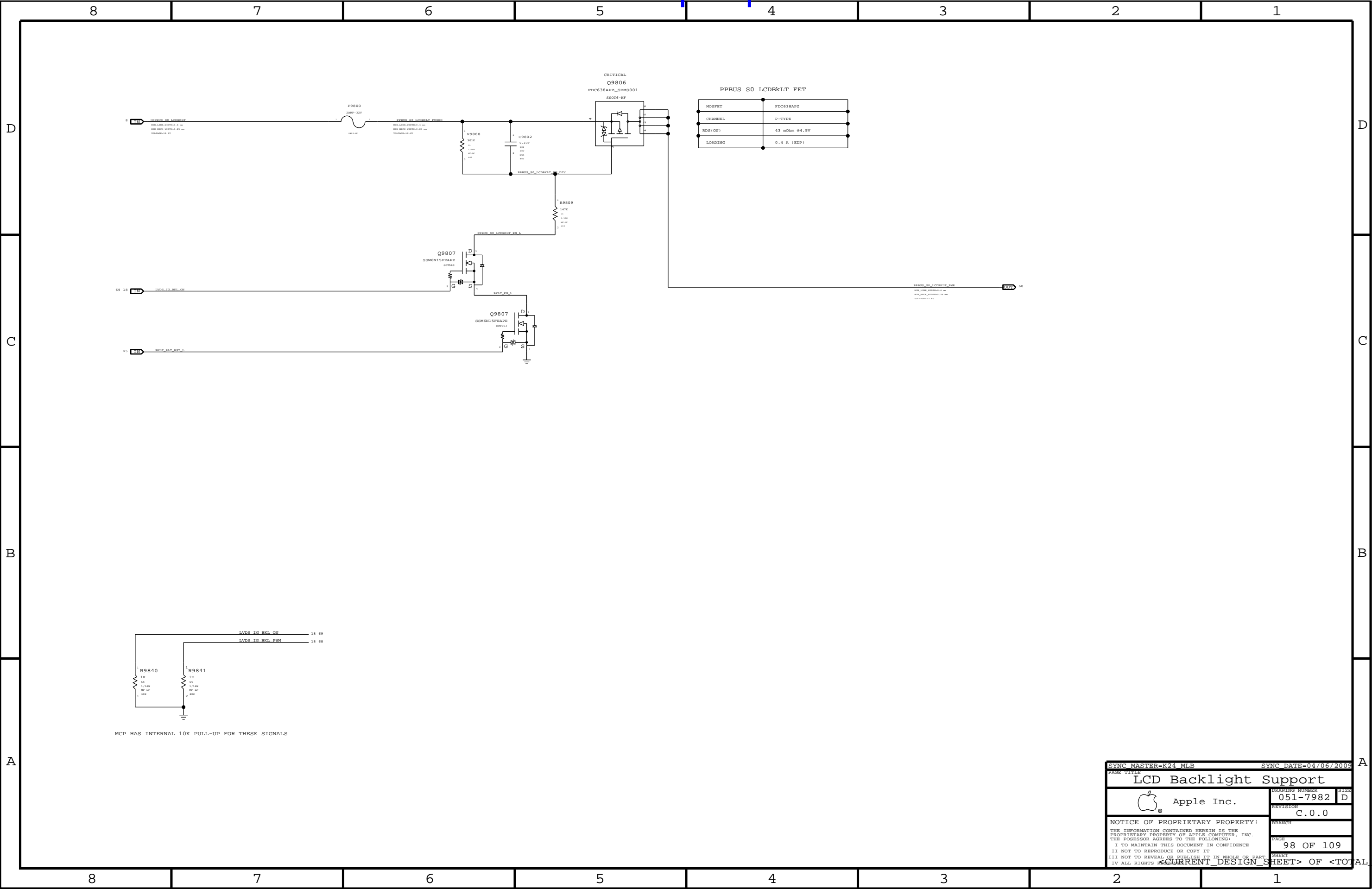
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8	7	6	5	4	3	2	1																																
PCI-Express																																							
<table><tr><th>PHYSICAL_RULE_SET</th><th>LAYER</th><th>ALLOW ROUTE ON LAYER?</th><th>MINIMUM LINE WIDTH</th><th>MINIMUM NECK WIDTH</th><th>MAXIMUM NECK LENGTH</th><th>DIFFPAIR PRIMARY GAP</th><th>DIFFPAIR NECK GAP</th></tr><tr><td>PCIe_RSD</td><td>*</td><td>+90_OHM_DIFF</td><td>+90_OHM_DIFF</td><td>+90_OHM_DIFF</td><td>+90_OHM_DIFF</td><td>+90_OHM_DIFF</td><td>+90_OHM_DIFF</td></tr><tr><td>CLK_PCIe_100D</td><td>*</td><td>+100_OHM_DIFF</td><td>+100_OHM_DIFF</td><td>+100_OHM_DIFF</td><td>+100_OHM_DIFF</td><td>+100_OHM_DIFF</td><td>+100_OHM_DIFF</td></tr></table>				PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	PCIe_RSD	*	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF	CLK_PCIe_100D	*	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF												
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP																																
PCIe_RSD	*	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF																																
CLK_PCIe_100D	*	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF																																
<table><tr><th>SPACING_RULE_SET</th><th>LAYER</th><th>LINE-TO-LINE SPACING</th><th>WEIGHT</th></tr><tr><td>PCIe</td><td>*</td><td>+3x_DIELECTRIC</td><td>7</td></tr><tr><td>CLK_PCIe</td><td>*</td><td>20 MIL</td><td>7</td></tr><tr><td>MCP_PEX_COMP</td><td>*</td><td>8 MIL</td><td>7</td></tr></table>				SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	PCIe	*	+3x_DIELECTRIC	7	CLK_PCIe	*	20 MIL	7	MCP_PEX_COMP	*	8 MIL	7	<table><tr><th>SPACING_RULE_SET</th><th>LAYER</th><th>LINE-TO-LINE SPACING</th><th>WEIGHT</th></tr><tr><td>PCIe</td><td>TOP,BOTTOM</td><td>+4x_DIELECTRIC</td><td>7</td></tr></table>				SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	PCIe	TOP,BOTTOM	+4x_DIELECTRIC	7								
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT																																				
PCIe	*	+3x_DIELECTRIC	7																																				
CLK_PCIe	*	20 MIL	7																																				
MCP_PEX_COMP	*	8 MIL	7																																				
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT																																				
PCIe	TOP,BOTTOM	+4x_DIELECTRIC	7																																				
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.4																																							
Digital Video Signal Constraints																																							
<table><tr><th>PHYSICAL_RULE_SET</th><th>LAYER</th><th>ALLOW ROUTE ON LAYER?</th><th>MINIMUM LINE WIDTH</th><th>MINIMUM NECK WIDTH</th><th>MAXIMUM NECK LENGTH</th><th>DIFFPAIR PRIMARY GAP</th><th>DIFFPAIR NECK GAP</th></tr><tr><td>DP_100D</td><td>*</td><td>+100_OHM_DIFF</td><td>+100_OHM_DIFF</td><td>+100_OHM_DIFF</td><td>+100_OHM_DIFF</td><td>+100_OHM_DIFF</td><td>+100_OHM_DIFF</td></tr><tr><td>LVDS_100D</td><td>*</td><td>+100_OHM_DIFF</td><td>+100_OHM_DIFF</td><td>+100_OHM_DIFF</td><td>+100_OHM_DIFF</td><td>+100_OHM_DIFF</td><td>+100_OHM_DIFF</td></tr><tr><td>MCP_DV_COMP</td><td>*</td><td>7</td><td>20 MIL</td><td>20 MIL</td><td>+STANDARD</td><td>+STANDARD</td><td>+STANDARD</td></tr></table>				PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	DP_100D	*	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	LVDS_100D	*	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	MCP_DV_COMP	*	7	20 MIL	20 MIL	+STANDARD	+STANDARD	+STANDARD				
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP																																
DP_100D	*	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF																																
LVDS_100D	*	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF																																
MCP_DV_COMP	*	7	20 MIL	20 MIL	+STANDARD	+STANDARD	+STANDARD																																
<table><tr><th>SPACING_RULE_SET</th><th>LAYER</th><th>LINE-TO-LINE SPACING</th><th>WEIGHT</th></tr><tr><td>DISPLAYPORT</td><td>*</td><td>+3x_DIELECTRIC</td><td>7</td></tr><tr><td>LVDS</td><td>*</td><td>+3x_DIELECTRIC</td><td>7</td></tr></table>				SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	DISPLAYPORT	*	+3x_DIELECTRIC	7	LVDS	*	+3x_DIELECTRIC	7	<table><tr><th>SPACING_RULE_SET</th><th>LAYER</th><th>LINE-TO-LINE SPACING</th><th>WEIGHT</th></tr><tr><td>DISPLAYPORT</td><td>TOP,BOTTOM</td><td>+4x_DIELECTRIC</td><td>7</td></tr><tr><td>LVDS</td><td>TOP,BOTTOM</td><td>+4x_DIELECTRIC</td><td>7</td></tr></table>				SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	DISPLAYPORT	TOP,BOTTOM	+4x_DIELECTRIC	7	LVDS	TOP,BOTTOM	+4x_DIELECTRIC	7								
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LVDS	TOP,BOTTOM	+4x_DIELECTRIC	7																																				
LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length. DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps. DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals. Max length of LVDS/DisplayPort/TMDS traces: 12 inches. SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.																																							
SATA Interface Constraints																																							
<table><tr><th>PHYSICAL_RULE_SET</th><th>LAYER</th><th>ALLOW ROUTE ON LAYER?</th><th>MINIMUM LINE WIDTH</th><th>MINIMUM NECK WIDTH</th><th>MAXIMUM NECK LENGTH</th><th>DIFFPAIR PRIMARY GAP</th><th>DIFFPAIR NECK GAP</th></tr><tr><td>SATA_100D</td><td>*</td><td>+100_OHM_DIFF</td><td>+100_OHM_DIFF</td><td>+100_OHM_DIFF</td><td>+100_OHM_DIFF</td><td>+100_OHM_DIFF</td><td>+100_OHM_DIFF</td></tr><tr><td>SATA_RSD_HDD</td><td>*</td><td>+90_OHM_DIFF</td><td>+90_OHM_DIFF</td><td>+90_OHM_DIFF</td><td>+90_OHM_DIFF</td><td>+90_OHM_DIFF</td><td>+90_OHM_DIFF</td></tr></table>				PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	SATA_100D	*	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	SATA_RSD_HDD	*	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF												
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SATA_RSD_HDD	*	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF																																
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SYNC MASTER=K24 MLB		SYNC DATE=04/06/2009	
PAGE TITLE			
Ethernet Constraints			
 Apple Inc.		DRAWING NUMBER 051-7982	SIZE D
		REVISION C.0.0	
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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1701_DIFFPAIR	*	*STANDARD	*STANDARD	*STANDARD	*STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE	
		PHYSICAL	SPACING
	SMBUS_SMC_A_S3_SCL	SMG_100	100
	SMBUS_SMC_A_S3_SDA	SMG_100	100
	SMBUS_SMC_B_S0_SCL	SMG_100	100
	SMBUS_SMC_B_S0_SDA	SMG_100	100
	SMBUS_SMC_C_S0_SCL	SMG_100	100
	SMBUS_SMC_C_S0_SDA	SMG_100	100
	SMBUS_SMC_D_S0_SCL	SMG_100	100
	SMBUS_SMC_D_S0_SDA	SMG_100	100
	SMBUS_SMC_EISA_SCL	SMG_100	100
	SMBUS_SMC_EISA_SDA	SMG_100	100
	SMBUS_SMC_MGMT_SCL	SMG_100	100
	SMBUS_SMC_MGMT_SDA	SMG_100	100

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE	
		PHYSICAL	SPACING
	CHGR_CS1	1701_DIFFPAIR	
	CHGR_CS1_N	1701_DIFFPAIR	
	CHGR_CS0	1701_DIFFPAIR	
	CHGR_CS0_N	1701_DIFFPAIR	

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SMC Constraints

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C									C
B									B
A									A
	8	7	6	5	4	3	2	1	

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DIFFPAIR	*	*STANDARD	*STANDARD	*STANDARD	*STANDARD	0.1 MM	0.1 MM


K84 SENSOR NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE	
	PHYSICAL	SPACING
00000000	00000000	CHOR_CSD_R_P 56
00000000	00000000	CHOR_CSD_R_N 56
00000000	00000000	CPUTHMNS_D2_P 42
00000000	00000000	CPUTHMNS_D2_N 42
00000000	00000000	CPU_THERMD_P 10 42
00000000	00000000	CPU_THERMD_N 10 42
00000000	00000000	ISNS_CPDTVT_P 41
00000000	00000000	ISNS_CPDTVT_N 41
00000000	00000000	ISNS_HDD_P 34 47
00000000	00000000	ISNS_HDD_N 34 47
00000000	00000000	ISNS_HDD_R_P 47
00000000	00000000	ISNS_HDD_R_N 47
00000000	00000000	MCPTHMNS_D2_P 42
00000000	00000000	MCPTHMNS_D2_N 42
00000000	00000000	MCP_THMDIODR_P 21 42
00000000	00000000	MCP_THMDIODR_N 21 42
00000000	00000000	ISNS_ODD_P 34 47
00000000	00000000	ISNS_ODD_N 34 47
00000000	00000000	ISNS_ODD_R_P 47
00000000	00000000	ISNS_ODD_R_N 47
00000000	00000000	ISNS_AIRPORT_P 30 47
00000000	00000000	ISNS_AIRPORT_N 30 47
00000000	00000000	ISNS_AIRPORT_R_P 47
00000000	00000000	ISNS_AIRPORT_R_N 47
00000000	00000000	ISNS_IVS_83_P 47 58
00000000	00000000	ISNS_IVS_83_N 47 58
00000000	00000000	ISNS_IVS_83_R_P 47
00000000	00000000	ISNS_IVS_83_R_N 47
00000000	00000000	ISNS_LCDENLT_P 47 68
00000000	00000000	ISNS_LCDENLT_N 47 68

SYNC MASTER=K24 MLB

SYNC DATE=01/19/2009

K84 SPECIAL CONSTRAINTS

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K84 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS									
BOARD LAYERS				BOARD AREAS		BOARD UNITS (MIL OR MM)	ALLEGRO VERSION		
TOP, 10L2, 10L3, 10L4, 10L5, 10L6, 10L7, 10L8, 10L9, 10L10, 10L11, BOTTOM				NO_TYPE, BGA_P1000		MM	15.5.1		
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		
DEFAULT	*	Y	<BGA_OHM_SE	0.100MM	30 MM	0 MM	0 MM		
STANDARD	*	Y	<DEFAULT	<DEFAULT	12.7 MM	<DEFAULT	<DEFAULT		
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		
55_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM					
55_OHM_SE	*	Y	0.076 MM	0.076 MM	<STANDARD	<STANDARD	<STANDARD		
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		
50_OHM_SE	TOP, BOTTOM	Y	0.115 MM	0.115 MM					
50_OHM_SE	*	Y	0.076 MM	0.076 MM	<STANDARD	<STANDARD	<STANDARD		
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		
40_OHM_SE	TOP, BOTTOM	Y	0.165 MM	0.100 MM					
40_OHM_SE	*	Y	0.126 MM	0.100 MM	<STANDARD	<STANDARD	<STANDARD		
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		
2704_OHM_SE	TOP, BOTTOM	Y	0.310 MM	0.310 MM					
2704_OHM_SE	*	Y	0.222 MM	0.222 MM	<STANDARD	<STANDARD	<STANDARD		
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		
70_OHM_DIFF	*	N	<STANDARD	<STANDARD	<STANDARD	<STANDARD	<STANDARD		
70_OHM_DIFF	10L3, 10L4, 10L5, 10L6	Y	0.151 MM	0.100 MM	<STANDARD	0.224 MM	0.224 MM		
70_OHM_DIFF	TOP, BOTTOM	Y	0.185 MM	0.100 MM		0.200 MM	0.200 MM		
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		
90_OHM_DIFF	*	N	<STANDARD	<STANDARD	<STANDARD	<STANDARD	<STANDARD		
90_OHM_DIFF	10L3, 10L4, 10L5, 10L6	Y	0.095 MM	0.095 MM		0.234 MM	0.234 MM		
90_OHM_DIFF	TOP, BOTTOM	Y	0.112 MM	0.112 MM		0.220 MM	0.220 MM		
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		
100_OHM_DIFF	*	N	<STANDARD	<STANDARD	<STANDARD	<STANDARD	<STANDARD		
100_OHM_DIFF	10L3, 10L4, 10L5, 10L6	Y	0.075 MM	0.075 MM		0.244 MM	0.244 MM		
100_OHM_DIFF	TOP, BOTTOM	Y	0.091 MM	0.091 MM		0.230 MM	0.230 MM		
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		
100_OHM_DIFF_HSD	*	N	<STANDARD	<STANDARD	<STANDARD	<STANDARD	<STANDARD		
100_OHM_DIFF_HSD	10L3, 10L4, 10L5, 10L6	Y	0.083 MM			0.400 MM	0.400 MM		
100_OHM_DIFF_HSD	TOP, BOTTOM	Y	0.095 MM	0.095 MM		0.400 MM	0.400 MM		
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		
110_OHM_DIFF	*	N	<STANDARD	<STANDARD	<STANDARD	<STANDARD	<STANDARD		
110_OHM_DIFF	10L3, 10L4, 10L5, 10L6	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM		
110_OHM_DIFF	TOP, BOTTOM	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM		
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		
111_DIFFPAIR	*	Y	<STANDARD	<STANDARD	<STANDARD	0.1 MM	0.1 MM		