

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.  
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.  
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
C	0000897412	PRODUCTION RELEASED	2010-04-26


SCHEM MLB\_LDO K87  
SCRATCHO  
04/26/2010

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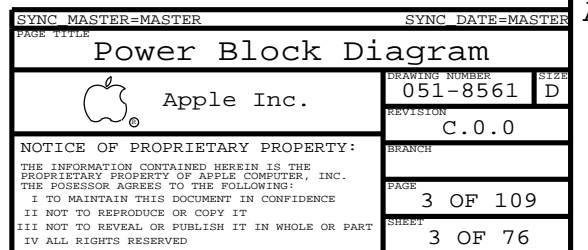
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Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8561	1	SCHEM_MLB_LDO_K87	SCM	CRITICAL	
820-2877	1	PCBP_MLB_LDO_K87	PCB	CRITICAL	

DRAWING TITLE		
SCHEM_MLB_LDO_SCRATCHO_K87		
 Apple Inc.	DRAWING NUMBER	051-8561
	REVISION	C.0.0
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CB

A

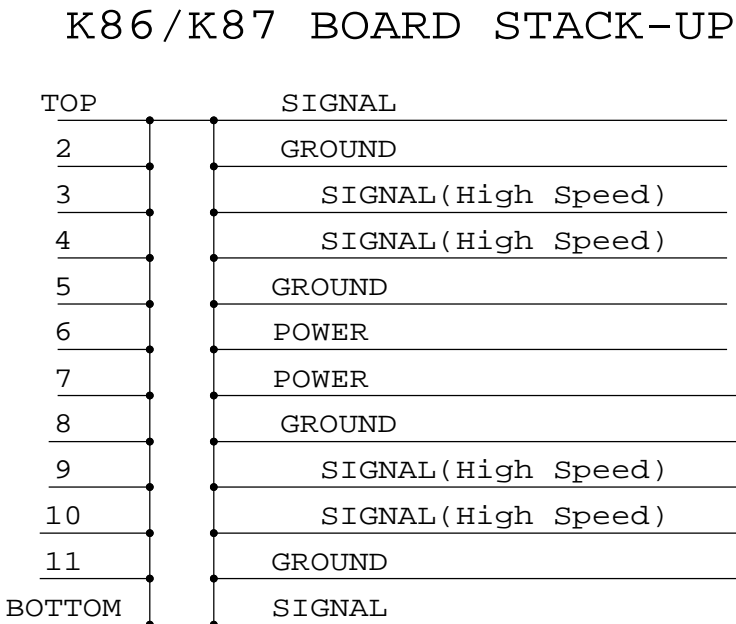
DC


B

A

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEEE_DD16]	CRITICAL	EEEE:DD16
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEEE_DD17]	CRITICAL	EEEE:DD17
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEEE_DD18]	CRITICAL	EEEE:DD18
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEEE_DD19]	CRITICAL	EEEE:DD19

Part Substitutions (differences with K6/K69)					
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0125	1	RES,MTL P21M,1/16W,113 OHM,1.0402,SMD,LF	R5714		LED:K86_K87



SYNC MASTER=(K84 MLB)		SYNC DATE=(01/19/2009)	
PAGE TITLE			
BOM Configuration			
 Apple Inc.		DRAWING NUMBER	D
		051-8561	SIZE
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8	7	6	5	4	3	2	1				
<div>Revision History</div> <div>NOTE: All page numbers are .csa, not PDF. See page 1 for .csa -&gt; PDF mapping.</div> <div>10/1/2009:INITIAL RELEASE 0.0.1- - ALL PAGES SYNC'ED FROM K84 - REPAIRED K84 MCP AND CPU PAGES WITH K6 PAGES - UPDATED SCHEMATIC AND PCB PART NUMBER INFO</div> <div>2009-12-03: Proto 0 release 1.0.0</div> <div>2009-12-04: 1.1.0 csa 3: Updated CPU block text to include CPU description for both K86 and K87 csa 3: Updated text note to include K86 in title csa 4: Added BOM entry under Module Parts table to include CULV processor (33783779) to minimize delta on this page between K86 and K87 per Diana</div> <div>2009-12-07: 1.2.0 csa 74: Component value changes per Leo (Intersil): R7417 from 5.36k =&gt; 6.34k, 1% (11450295) C7417 from 0.12uF to 0.22uF (13250102) Implemented different stuffing options for 1-phase vs 2-phase: Added IMVP6:2PHASE to the following components: R7417, C7428, R7409, R7411, C7406, R7414, C7414, C7413 Added BOM table to insert the following APNs for IMVP6:1PHASE: R7417 = 7.68K 1% (11450304) C7428 = 0.22uF 10% (13250102) R7409 = 5.9K 1% (13250256) R7411 = 25% 1% (11450160) C7406 = 4700pF 10% (13250720) R7414 = 97.5k 1% (11450410) C7414 = 1000pF 10% (13250045) C7413 = 100uF 5% (13151027) Updated table to add new values for lphase (PWM freq., Max current, Load line) csa 4: STILL NEED TO UPDATE VALUE OF C7428!</div> <div>2009-12-08: 1.3.0 csa 45: Added passive deemphasis to SATA HDD D2R lines: Added R4585, R4586 (51.1 ohm, 1% (11450093) and OMITTED Added R4585, C4586 (10pF, 5% (13150199) and NOSTUFFED Added BOM table to stuff 0-ohms until we get go-ahead for filter</div> <div>2009-12-08: 1.4.0 csa 8: Deleted net properties for the following nets: =PP3V3_S0_CPUVTT1SENSE =PP5V_S0_HDP =PP5V_S0_MCPWRG0 =PP1V05_S0_MCP_AVDD_UF =PP3V3_S0_MCM_R =PP3V3_S0_PMRCTL =PP3V3_S0_DCCONN csa 34: Deleted net properties for =PP3V3_S3_WLAN csa 74: Changed C7434 from NOSTUFF to IMVP6:2PHASE per Intersil Added IMVP6:2PHASE to R7413 per Intersil Changed C7428 from 0.47uF to 0.33uF (13250101) per Intersil Changed component color to Green Cosmetic cleanup csa 90: Deleted net properties for =PP5V_S3_CAMERA csa 98: Deleted net properties for =PPBUS_S0_LCDCLKLT csa 108: Added NET_PHYSICAL property to SATA_HDD_D2R_FILT_P and _N</div> <div>2009-12-09: 1.5.0 multiple: Added parentheses for SYNC_DATE property on all pages that have broken sync. csa 4: Deleted entry in Module Parts table for R6612, R6617, R6630, R6633 since they were removed when we switched from piezo to dynamic speakers csa 69: Changed J6955 symbol to K87 Hall effect assembly (33580114)</div> <div>2009-12-10: 1.6.0 csa 69: Added OMIT to J6955, BOM table to stuff K84 Hall effect connector</div> <div>2009-12-11: 1.7.0 csa 45: Added PLACEMENT NOTE for passive deemphasis circuit. csa 74: Changed 1PHASE BOM table to correctly call out 13250080 (0.22uF) instead of 0.022uF</div> <div>2009-12-16: 1.8.0 *** Resynced all synced pages and picked up the following (change notes from T27): csa 18: T27: Swapped USB_EXTB and USB_EXTD for NVRN-612340 (pg. 18). &lt;radar://7416825&gt; Ensure USB_EXTB is on ports 8-11 (NVRN-612340) csa 20: T27: Changed USB_BIAS from 931-ohms to 887-ohms per DG v1.3 (pg. 18). &lt;radar://7459260&gt; Design Guide v1.3 updates *** Started syncing the following pages: csa 29,31: Began syncing from T27 per &lt;radar://7424246&gt; BOM: K87 needs omit on J3100 and J2900 from T27 csa 54: T27: Added BOMOPTIONS and APNs for Foxconn and Molex 80-DIMM connectors (pg. 29, 31). C5490 changed from CAP 402-0.022UF,10%,16V,CERM-X5R to CAP 402-0.022UF,20%,16V,CERM T27: Added CKPLUS_WAIVE properties to dismisal false errors (pg. 54). T27: Added gain note for U5402 and SMC_BATT_SENSE (pg. 54). T27: Changed RC balance on BATT_SENSE, same time constant (pg. 54). csa 57: Began syncing from T27 per &lt;radar://7404029&gt; T27 schematic bom option for R5714 &amp; R5030 to keep K87 in sync R5714 has BOMOPTION LED_K6_K69, and we need to substitute a different part on csa 4 *** Made the following changes to follow T27 on the following unsynced pages: csa 25: T27: Removed R2575 &amp; R2580 per DG v1.3 (pg. 25). per &lt;radar://7459260&gt; Design Guide v1.3 updates *** Other changes: csa 4: Added BOM table to substitute in parts that have BOMOPTION xxx-K6_K69 (to allow sync with T27) Added R5714 (11450125) to table with BOMOPTION LED_K86_K87</div> <div>2009-12-17: 1.9.0 csa 4: Added BOM table entry for MCP89-A02 per &lt;radar://7416858&gt; Task: Get part numbers for A02 rev. csa 34: Changed K87_MCP BOM group to call out MCP89-A02 Changed R3440 from AP002 part to AP016 (34350311) per &lt;radar://7459498&gt; BOM: APN updates for PFP1009 and SAK parts Changed R3454 to 100K, 1% (11450411) to match T27 and K69 Updated DLY text note for U3440 to match T27 csa 72: Changed R3440 color to green, deleted WF text note about needing PU Changed R3420 from 15250691 to 15250778 per &lt;radar://problem/7347216&gt; K69 L7260 combo footprint Alternates table on csa 4 already has 15250778 as alternate to 15250693</div> <div>2009-12-22: 1.10.0 csa 4: Per &lt;radar://problem/7473229&gt; K86: Move to MCP83 Added BOM table entry for MCP83M (33783876) This is for K86 ONLY. Adding entry to minimize delta on csa 4 between K87 and K86 BOMOPTION is MCP83M Per &lt;radar://problem/7495072&gt; K87: Call out LED_K86_K87 BOMOPTION in the K87_MISC BOM group Added LDO_K86_K87 BOMOPTION to the K87_MISC BOM group Per &lt;radar://problem/7495116&gt; K87: remove ON Semi alternate for Q2300 (376S0624) Removed table entry for alternate for 376S0624 Per &lt;radar://problem/7495021&gt; K86/K87: Replace "S" APNs with "*" APNs for programmed SMC and BR Changed BOMTRON:PROG to call out 34170251 (SUBASSY_IC_BOOT ROM_K86/K87) Created SMC:PROG_K87 pointing to 34170252 (SUBASSY_IC_SMC_K87) Created SMC:PROG_K86 pointing to 34170250 (SUBASSY_IC_SMC_K86) Changed K87_PRODPARTS BOM group to point to SMC:PROG_K87 csa 69: Per &lt;radar://problem/7494087&gt; K87: remove OMIT from J6955 and delete BOM table Deleted BOM table for Hall effect assembly Changed text note to say "HALL EFFECT ASSEMBLY" Deleted OMIT BOMOPTION from J6955 Added text note with part numbers for components of the assembly Assembly APN: 3350114 - BOM: 639-0680 - PCB: 820-2801 - MCO: 056-3515 Conn APN:51850788 csa 74: Cosmetic change, moved R7413, C7406 BOMOPTION label so they don't look like wire name csa 78: Per &lt;radar://problem/7495000&gt; K87: Add NOSTUFF to R7872 to disconnect U7870 from ALL_SYS_PWRGD Changed BOMOPTION for R7872 from SUPGOOD_ISL to NOSTUFF</div> <div>2010-01-06: 1.11.0 csa 7: Per &lt;radar://problem/7517432&gt; K86/K87 functional net property needed on signals in schematics Added the following functional test points under the J5100 LPC/SP1 CORN FUNC_TEST group LPCPLUS_GP10 LPCPLUS_GP11 LPCPLUS_GP12 SMC_TMS</div> <div>2010-01-07: 1.12.0 csa 23: *** BROKE SYNC WITH T27 Per &lt;radar://problem/7519025&gt; K86/K87: update all instances of 376S0786 schematic symbols Updated Q2355 and Q2356 with new schematic symbols Need to resync with T27 once the change has been made there csa 70: Per &lt;radar://problem/7519048&gt; K86/K87: change U7000 to 353S2929 Changed U7000 from 353S2392 to 353S2929 Updated APN text note</div> <div>2010-01-08: 2.0.0 csa 45: Per &lt;radar://problem/7524364&gt; K86/K87: change SATA HDD D2R passive EQ values Removed NOSTUFF from C4585, C4586 Removed OMIT from R4585, R4586 Deleted BOM table that stuffed the bypass option Changed R4585, R4586 to 11450065 (27.4 ohm, 1%) Changed C4585, C4586 to 13154713 (47pF, 5%)</div> <div>2010-01-13: 2.1.0 csa 4: Per &lt;radar://problem/7540383&gt; K86: Update CPU part number to 33783792 Changed U1000 CPU:1.2GHZ BOMOPTION from 33783779 to 33783792</div> <div>2010-01-13: 2.2.0 csa 4: Cosmetic: changed text sizes and alignment Per &lt;radar://problem/7540522&gt; K86/K87: Production Debug Components Changed DBS-1093 to call out K87_DEVEL_PVT instead of K87_DEVEL_ENG Changed K87_COMMON to call out K87_DEBUG_PVT instead of K87_DEBUG_ENG Diff from the two changes above: Toggled: VREFPWRGN:YES ==&gt; VREFPWRGN:NO BMON:ENG ==&gt; BMON:PROD BKLT:ENG ==&gt; BKLT:PROD SENS_R:ENG ==&gt; SENS_R:PROD Removed: DEBUG_ADC, S0PGOOD_ISL, EFI_DEBUG, MCPPLL_LDO, EXTIV05, MCP_T_DIODE_SENSOR, XDP_CON Unchanged: LPCPLUS_DEVEL_BOM, SMC_DEBUG:YES, XDP Added LPCPLUS_CON to K87_DEVEL_ENG (does not change BOM for DVT) Changed all instances of "K87_DEBUG_XXXX" to K87_DEBUG:XXXX Changed all instances of "K87_DEVEL_XXXX" to K87_DEVEL:XXXX csa 51: (Per &lt;radar://problem/7540522&gt; K86/K87: Production Debug Components) Changed J5100 BOMOPTION from LPCPLUS to LPCPLUS_CON to unstuff connector at DVT</div> <div>2010-01-15: 2.3.0 csa 74: Per &lt;radar://7525313&gt; K86 CPU loadline, OCP update Keeping K86 and K87 pos identical for CSA 74, modifying BOM table for IMVP 1 phase on K87's schematic to reflect changes for K86. IMVP6:1PHASE BOM Table: R7417 changed to 87K (APN 11450305) R7416 added to BOM Table, 16.9K (APN 11450336) Added IMVP6:2PHASE BOM option to R7416 for K87's 13.7K csa 74, csa 79: Per &lt;radar://7542674&gt; K86/K87 Text note change Cleaned up text notes for lphase, 2phase, and edp #s per radar request.</div> <div>2010-01-18: 2.4.0 csa 4: Per &lt;radar://problem/7549122&gt; K86/K87: Switch to new BOM group structure Reverted back to ENG BOM, no longer PROD BOM (i.e. reverted much of 2.2.0 changes) Changed BOM group structure to match that in the radar (see PDF attached to radar) Net change was to move LPCPLUS to the 639 (from the 085) Switching from Engineering to Production BOM should only require changing PROJECT_PHASE:DEV to PROJECT_PHASE:PROD Per &lt;radar://problem/7544629&gt; K86/K87: Update MCP83 description on csa 4 Changed Description for 33783876 to "IC,MCP83M-A02,31X31MM,BQAL168" *** Started syncing with K6 Syncing with K6 to pick up new symbols for Q2355 and Q2356 Should switch syncing back to T27 once it is updated there csa 37: Per &lt;radar://problem/7548726&gt; K86/K87 Ethernet series R's need to be 0 ohmed Changed R3790-R3795 to 116S0004 (0-ohm, 0402) from 22-ohm</div>				<div>2010-01-19: 2.5.0 csa 37: Per &lt;radar://problem/7554342&gt; K86/K87: Change L3720 to 152S1182 Changed L3720 to 152S1182 (IND,PWR,SHD,4.7UH,20V,0.91A,31X31X12MM) for lower ESR</div> <div>2010-01-22: 2.6.0 csa 4: Per &lt;radar://problem/7571786&gt; K86/K87: Add E3T EEE code for K86 to schematic Added row to EEE table for E3T Changed BOMOPTIONS to be mutually exclusive (changed "_" to "::")</div> <div>2010-01-28: 2.7.0 *** Resynced with T27 and K6 (no differences) *** Resynced Audio pages with the following changes: pg. 62: changed R6211 to 22 Ohms pg. 66: changed C9602 to 0.068uF pg. 67: no stuffed R6712 and R6713 csa 45: Per &lt;radar://problem/7561001&gt; K87 BOM: Radiated Emissions: Right Audio emissions fail Added L4530, L4531 (APN 155S0137) to S1L connector pins csa 97: Per &lt;radar://problem/7589365&gt; K86/K87: Compensation settings change to provide more phase margin, reduce ripple Changed R7572 changed to 147K to 10K (11450315) and removed NOSTUFF Changed C9705 from 8.2nF to 33nF (132S0131) Changed C9706 from 120pF to 220pF (131S2225)</div> <div>2010-02-02: 2.8.0 *** Resynced with T27 and K6 (no differences) *** Resynced Audio pages with the following changes: pg. 67: added BOM options for U6700, R6712, and R6713 to support MAX14560 and MAX14504 csa 97: Changed R9710 from 7.32K 0402 1% to 7.68K (APN 11450304) to support old K84 panel csa 4: Added OLD_AUDIO_SWITCH BOM OPTION to K86_K87_COMMON</div> <div>2010-02-15: 2.9.0 2010-02-15: 2.10.0 csa 54: Broke sync with T27. Per &lt;radar://problem/7605797&gt; K69/K86/K87 sensor INIC unreliable U5400 changed from OPA348 to OPA330. C5434 changed to NOSTUFF</div> <div>2010-02-16: 2.11.0 Resync with T27 and K6. Clean up and rerelease schematic.</div> <div>2010-02-18: 2.12.0 Per &lt;radar://7644836&gt; K87 power component update csa 74: R7417 changed to 5.90K, C7428 changed to 0.47uF, C7434 changed to 0.033uF csa 75: R7572 changed to 147K to 10K (11450315) and removed NOSTUFF csa 70: R7015 changed to 56.2K, C7015 changed to 1000pF, C7042 changed to 0.068uF Per &lt;radar://7634730&gt; K86/K87: add an RC on the LVDS_IG_BKL_PWM csa 97: R9725 changed to 200ohm, C9799 of 47pF added. R9726.1 connection moved to LVDS_IG_BKLPWM</div> <div>2010-02-18: 2.16.0 Per &lt;radar://7676934&gt; K86/K87: Hall eff documentation change. Substitute 607-6831 for doc purposes csa 69: J6955 BOMOPTION change to OMIT. Added BOM table with 607-6831 for J6955</div> <div>2010-02-18: 2.17.0 Per &lt;radar://7488543&gt; K86/K86 Task: Measure each Power supply in MLB csa 74: For K86 only: C1234 = 0.7uF added, C1235 = 0.7uF added, R7417 changed to 8.25kohm csa 12: For K86 only: C1272 = 330uF added. Per &lt;radar://7685202&gt; K86/K87 schematic: change U9700 to 353S2965 for Freescale backlight issue csa 97: U9700 changed to APN 514-0718 to 514-0750</div> <div>2010-02-18: 2.18.0 Per &lt;radar://7685811&gt; K86/K87 schematic: add additional 639 for differentiation between Foxconn and Molex DIMM connectors csa 4: MOLEX_DDR_CONN added to Module Parts, removed from Alternate table. Added second 639 and EEEE to BOM table</div> <div>2010-02-25: 2.19.0, 2.20.0 Per &lt;radar://7678513&gt; K87:EMC:ESD: System hangs on air/contact discharge to MPM connector csa 69: C6970, C6971, C6972 of 1000pF (APN 131S0222) added</div> <div>2010-02-26: 2.21.0 Per &lt;radar://7488543&gt; K87/K86 Task Measure each power supply in mlb. csa 12: C1208, C1208, C1207, C1209, C1211, C1219, C1202, C1216 NOSTUFFED csa 12: Added pads for 0603 caps (APN 138S0635). Components C1230, C1231, C1232, C1233, C1234, C1235, C1236, C1237. csa 74: Changed C7434 from 0.033uF to 0.047uF (APN 132S0189) per Liang</div> <div>2010-03-04: B.0.0 Per &lt;radar://7683852&gt; K87 Protol: 5 of 6 systems failing graphics noise (Underwater) acoustic spec by up to 3.1db csa 12: C1233, C1230, C1237, C1234 changed from NOSTUFF to STUFFED.</div>				<div>** MLB LDO branch</div> <div>2010-03-09: 0.8.0 Summary of changes for MLB LDO: csa 25: U2590 added, APN 353S2971. R2592 of 10K and C2592 of 1uF, C2593 of 1uF added. Nets MCP_PLL_LDO_EN and PP3V3_S0_LDO_R added.</div> <div>2010-03-22: A.1.0 csa 25: Copied from K6 Added C2599, R2597, R2596, U2593, Q2592, R2599, C2594, U2594, R2598, C2598 with BOMOPTION HTOL_SENSE:YES Added R2594 and R2591 with LDO:ADJ BOMOPTION Changed BOMOPTION names from LDO:YES and LDO:NO to MCPHVDV:P2V5 and MCPHVDV:P3V3 Added BOM TABLE with LDO:FIXED, LDO:ADJ, and HTOL_SENSE:NO stuffing options csa 50: Removed SMC alias to TP for SMC_NB_MISC_SENSE to enable sense circuitry connection to SMC Removed SMC_P10 alias to TP SMC_P10 csa 8: Added =PP3V42_G3H_OPA330 alias to power U2594 Added =PP3V3_S0_OPA330 alias to power U2593 csa 4: Added MCPHVDV:P2V5, LDO:FIXED, HTOL_SENSE:YES to BOM Group K86_K87_DEBUG:PROD</div> <div>2010-03-22: A.2.0 Per &lt;radar://7783507&gt; K87: Add cap to DDC line to avoid DDC line glitch issue csa 93: Added C9303 3300pF cap on DP_CA_DET csa 25: Changed U2594 power to 3V3_S0 from 3V42_G3H.</div> <div>2010-03-22: A.3.0 csa 77: Deleted U7740 1.05V LDO circuit to free space for U2592 and current mirror circuit.</div> <div>2010-03-22: A.4.0 Reverted the changes and synced back to A.0.0 Per &lt;radar://7783507&gt; K87: Add cap to DDC line to avoid DDC line glitch issue csa 93: Added C9303 3300pF cap on DP_CA_DET.</div> <div>2010-03-22: A.5.0 csa 25: Added R2591,R2594 for LDO:ADJ option. Changed U2592 to LDO:FIXED option. csa 4: Added Alternate part for U2592 LDO. 353S2987(TI), 353S2988(Micrel) to 353S2986(Intersil). LDO:FIXED, MCPHVDV:P2V5 added in bom table.</div> <div>2010-03-30: A.7.0 Reverted the changes and synced back to A.2.0 csa 4: Added Alternate part for U2592 LDO. 353S2987(TI), 353S2988(Micrel) to 353S2986(Intersil). LDO:FIXED, MCPHVDV:P2V5 added in bom table.</div> <div>2010-03-31: A.8.0 csa 25,49,50: Changed Q2592 gate control pin to SMC_P24 from SMC_P10.</div> <div>2010-04-1: A.9.0 csa 25: Added R2600 0ohm resistor to help layout change.</div> <div>2010-04-1: A.10.0 csa 25: Changed R2600 refiles to R2550 to match with page#.</div> <div>2010-04-14: B.0.0 rdar://7822714 csa 69: R6905 kept same lohm. C6900 changed to 2.2uF. 138S0592. csa 4: Devel BOM# changed to 085-1799. And BOM OPTIONS to K86_K87_DEVELOPMENT_PVT. Removed Intersil LDO(353S2986).</div> <div>2010-04-14: C.0.0 csa 4: Added Toshiba(376S0908), Fairchild(376S0907) as an alternate to 376S0634. Added Onsemi new spec part(376S0912) as an alternate to Q2300(376S0868).</div>			
8	7	6	5	4	3	2	1				

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Functional Test Points

FAN CONNECTORS FUNC\_TEST

PP5V_S0	7 8 62
FAN_RT_PWM	42
FAN_RT_TACH	42
(NEED TO ADD 1 GND TP)	

MIC FUNC\_TEST

BI_MIC_N	52 53 75
BI_MIC_P	52 53 75
BI_MIC_SHIELD	52 53

SPEAKER FUNC\_TEST

SPKRAMP_L_N_OUT	51 52
SPKRAMP_L_P_OUT	51 52
SPKRAMP_R_N_OUT	51 52
SPKRAMP_R_P_OUT	51 52
SPKRAMP_SUB_N_OUT	51 52
SPKRAMP_SUB_P_OUT	51 52

LVDS FUNC\_TEST

PP3V3_S0_LCD_DDC_F	64
PP3V3_SW_LCD_PANEL_F	(NEED 2 TP)
PPVOUT_S0_LCDBKLT	7 46 64 67 (NEED 2 TP)
LVDS_IG_DDC_CLK	9 64
LVDS_IG_DDC_DATA	9 64
LVDS_IG_A_DATA_N<0>	9 64 71
LVDS_IG_A_DATA_P<0>	9 64 71
LVDS_IG_A_DATA_N<1>	9 64 71
LVDS_IG_A_DATA_P<1>	9 64 71
LVDS_IG_A_DATA_N<2>	9 64 71
LVDS_IG_A_DATA_P<2>	9 64 71
LVDS_IG_A_CLK_F_N	44 75
LVDS_IG_A_CLK_F_P	44 75
LED_RETURN_1	64 67
LED_RETURN_2	64 67
LED_RETURN_3	64 67
LED_RETURN_4	64 67
LED_RETURN_5	64 67
LED_RETURN_6	64 67
PP5V_S3_CAMERA_F	7 64
USB_CAMERA_CONN_P	64 75
USB_CAMERA_CONN_N	64 75
(NEED TO ADD 5 GND TP)	

SATA ODD CONN FUNC\_TEST

PP5V_SW_ODD	7 33 46 (NEED 4 TP)
SMC_ODD_DETECT	33 35
SATA_ODD_D2R_C_P	33 71
SATA_ODD_D2R_C_N	33 71
SATA_ODD_R2D_P	33 71
SATA_ODD_R2D_N	33 71
(NEED TO ADD 4 GND TP)	

SATA HDD/SIL FUNC\_TEST

PP5V_S0_HDD_FLT	(NEED 4 TP)
SATA_HDD_R2D_P	33 71
SATA_HDD_R2D_N	33 71
SATA_HDD_D2R_C_P	33 71
SATA_HDD_D2R_C_N	33 71
SYS_LED_ANODE_R	33
(NEED TO ADD 4 GND TP)	

BATT POWER CONN FUNC\_TEST

PPVBAT_G3H_CONN	54 55 (NEED 3 TP)
SMBUS_SMC_BSA_SCL	38 74
SMBUS_SMC_BSA_SDA	38 74
SYS_DETECT_L	54
(NEED TO ADD 3 GND TP)	

HALL EFFECT CONNECTOR FUNC\_TEST

PP3V42_G3H	7 8 (NEED 2 TP)
SMC_LID_R	54
(NEED TO ADD 3 GND TP)	

X16 WIRELESS CONN FUNC\_TEST

PP3V3_S3_BT_F	30
CONN_PCIE_MINI_D2R_P	9 30 75
CONN_PCIE_MINI_D2R_N	9 30 75
CONN_PCIE_MINI_R2D_P	9 30 75
CONN_PCIE_MINI_R2D_N	9 30 75
PCIE_CLK100M_MINI_CONN_P	30 75
PCIE_CLK100M_MINI_CONN_N	30 75
PP3V3_WLAN	(NEED 4 TP)
PCIE_WAKE_L	16 30
CONN_USB2_BT_P	30 75
CONN_USB2_BT_N	30 75
AP_CLKREQ_O_L	30
AP_RESET_CONN_L	30
(NEED TO ADD 4 GND TP)	

IPD\_FLEX\_CONN FUNC\_TEST

PP3V3_S3	7 8
PP18V5_S3	7 44
Z2_CS_L	43 44
Z2_DEBUG3	43 44
Z2_MOSI	43 44
Z2_MISO	43 44
Z2_SCLK	43 44
Z2_BOOST_EN	44
Z2_HOST_INTN	43 44
Z2_CLKIN	43 44
Z2_KEY_ACT_L	43 44
Z2_RESET	43 44
PSOC_MISO	43 44
PSOC_MOSI	43 44
PSOC_SCLK	43 44
SMBUS_SMC_A_S3_SDA	38 74
SMBUS_SMC_A_S3_SCL	38 74
PSOC_F_CS_L	43 44
PICKB_L	43 44
(NEED TO ADD 2 GND TP)	

KEYBOARD CONN FUNC\_TEST

PP3V3_S3	7 8
PP3V42_G3H	7 8
WS_KBD1	43
WS_KBD2	43
WS_KBD3	43
WS_KBD4	43
WS_KBD5	43
WS_KBD6	43
WS_KBD7	43
WS_KBD8	43
WS_KBD9	43
WS_KBD10	43
WS_KBD11	43
WS_KBD12	43
WS_KBD13	43
WS_KBD14	43
WS_KBD15_CAP	43
WS_KBD16_NUM	43
WS_KBD17	43
WS_KBD18	43
WS_KBD19	43
WS_KBD20	43
WS_KBD21	43
WS_KBD22	43
WS_KBD23	43
WS_KBD_ONOFF_L	43
WS_LEFT_SHIFT_KBD	43
WS_LEFT_OPTION_KBD	43
WS_CONTROL_KBD	43
(NEED TO ADD 1 GND TP)	

DC POWER CONN FUNC\_TEST

PP18V5_DCIN_FUSE	(NEED 2 TP)
ADAPTER_SENSE	54
(NEED TO ADD 2 GND TP)	

POWER NETS FUNC\_TEST

PPVCORE_S0_CPU	8 39
PPVCORE_S0_MCP	8 39
PP1V05_S0	8 62
PP1V5_S0	8 62 75
PP1V8_S0	8
PP5V_S0	7 8 62
PP5V_S0	7 8 62
PP3V3_S0	8 62 75
PP1V5R1V35_S3	8 75
PP3V3_S3	7 8
PP5V_S3	8
PP3V3_S5	8 62 75
PP3V42_G3H	7 8
PPBUS_G3H	8 39
PP0V9_ENET	8
PP3V3_ENET	8
PP3V3_G3_RTC	8 19 20 23
PP3V3_WLAN	7 30
PP5V_SW_ODD	7 33 46
PP5V_S0_HDD_FLT	7 33
PP3V3_S5_AVREF_SMC	35 36
PP18V5_S3	7 44
PP3V3_SW_LCD_PANEL_F	7 64
PPVOUT_S0_LCDBKLT	7 46 64 67
PP4V5_AUDIO_ANALOG	48
SMC_PM_G2_EN	35 62
PM_SLP_S4_L	19 35 36 62
PM_SLP_S3_L	19 35 62 66
PP5V_S3_CAMERA_F	7 64
PP0V9_S5	8
PPDDRVTT_S0	8
PP1V05_S0_MCP_PLL_UP	8
PPVTT_S3_DDR_BUF	8
(NEED TO ADD 6 GND TP)	

FSB SIGNALS WITH NOTEST

NO_TESTTRUE_FSB_A_L<35..3>	10 14 69
NO_TESTTRUE_FSB_ADS_L	10 14 69
NO_TESTTRUE_FSB_ADSTB_L<1..0>	10 14 69
NO_TESTTRUE_FSB_D_L<63..0>	10 14 69
NO_TESTTRUE_FSB_DINV_L<3..0>	10 14 69
NO_TESTTRUE_FSB_DSTB_L_N<3..0>	10 14 69
NO_TESTTRUE_FSB_DSTB_L_P<3..0>	10 14 69
NO_TESTTRUE_FSB_HIT_L	10 14 69
NO_TESTTRUE_FSB_HITM_L	10 14 69
NO_TESTTRUE_FSB_LOCK_L	10 14 69
NO_TESTTRUE_FSB_REQ_L<4..0>	10 14 69

J5100 LPC+SPI CONN FUNC\_TEST

PP3V42_G3H	7 8
SPI_CLK	37 72
SPI_CS0_L	37 72
SPI_MISO	19 37 72
SPI_MOSI	37 72
SPIROM_USE_MLB	19 37 47
LPCPLUS_GPIO	19 37
LPC_SERIRQ	19 35 37
SMC_TMS	35 36 37
(NEED TO ADD 2 GND TP)	

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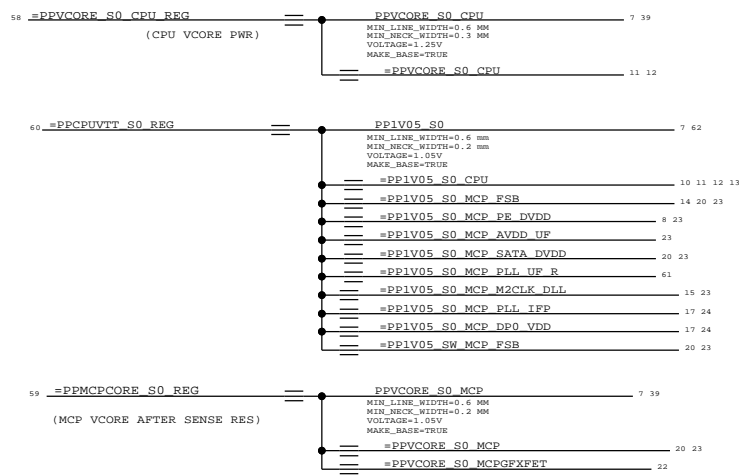
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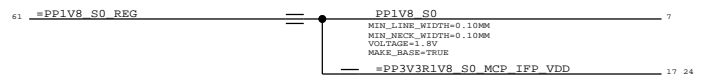
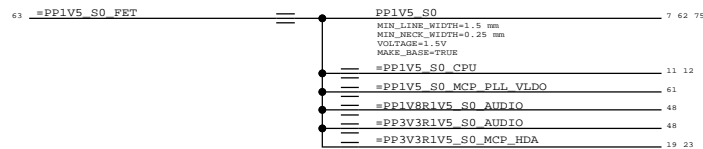
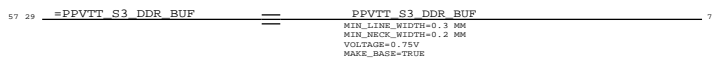
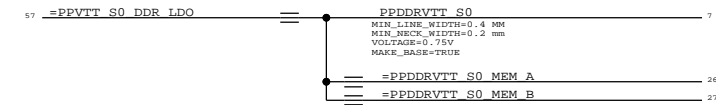
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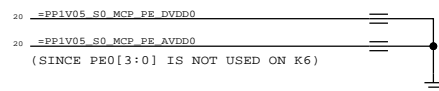
"S0,S0M" RAILS



LVDDR Vref/VTT (0.75V/0.675V) Rails

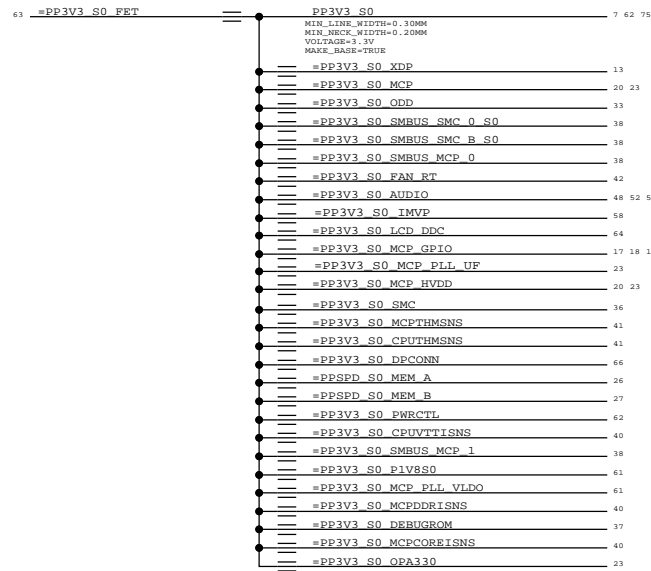
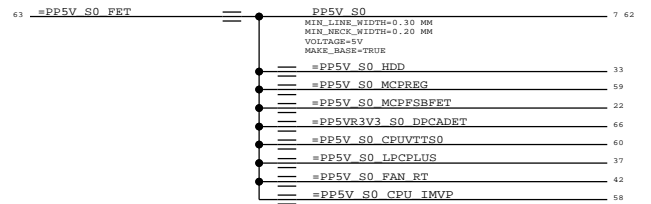


UNUSED MCP PE0[3:0] AVDD/DVDD

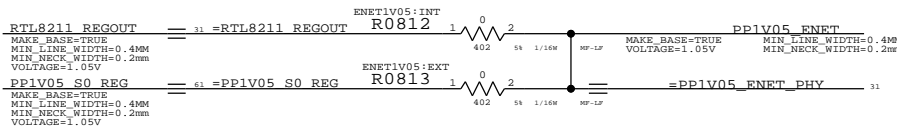
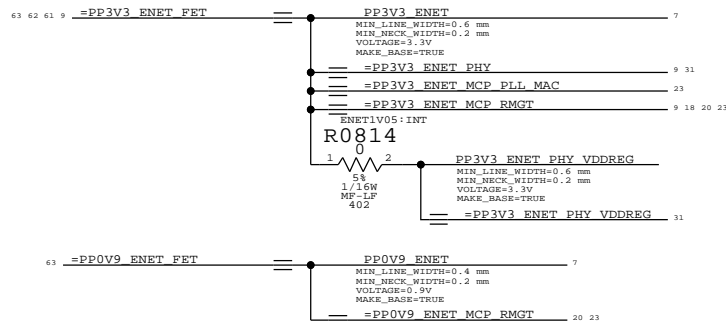


(CONNECTS TO MCP BALLS) 20 =PP1V05\_S0\_MCP\_PE\_DVDD1 =PP1V05\_S0\_MCP\_PE\_DVDD 8 (CONNECTS TO THE DECAPS)

(CONNECTS TO MCP BALLS) 20 =PP1V05\_S0\_MCP\_PE\_AVDD1 =PP1V05\_S0\_MCP\_PE\_AVDD 23 (CONNECTS TO THE DECAPS)

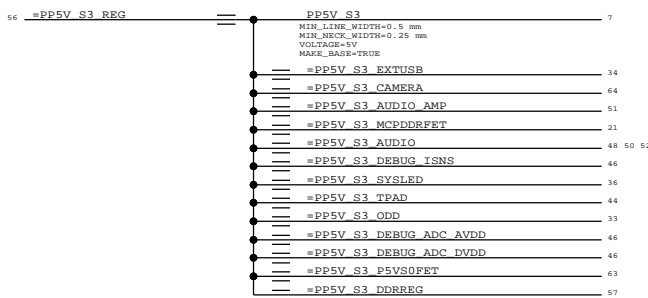
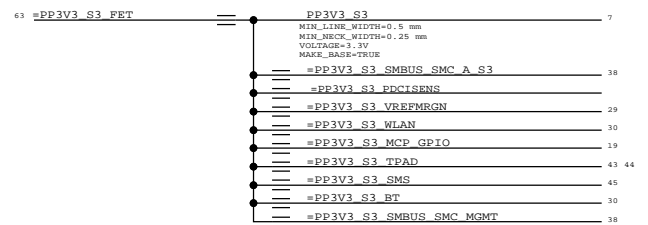
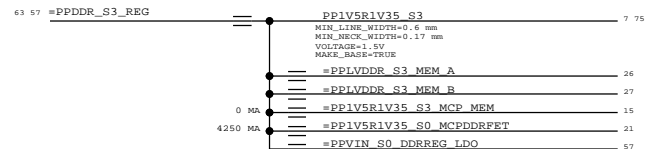


"ENET" RAILS

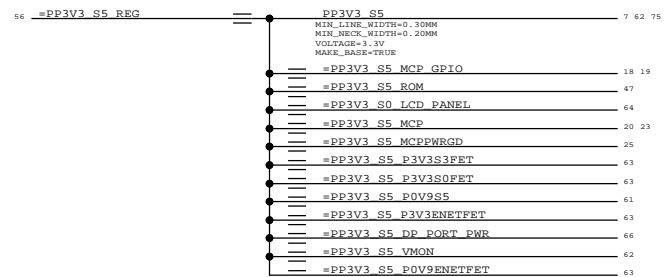
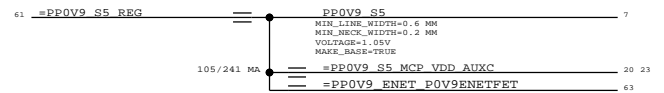


FIX ME!! OUTPUT OF REGULATOR VALUES

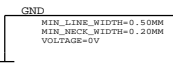
"S3" RAILS



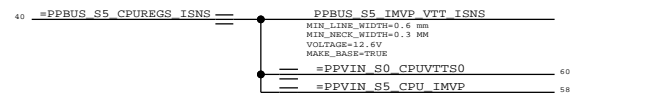
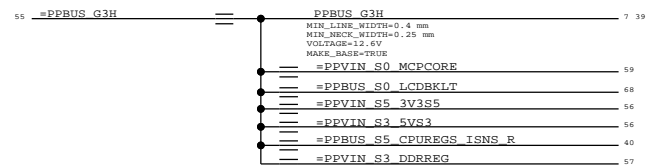
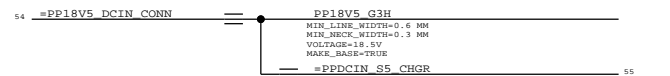
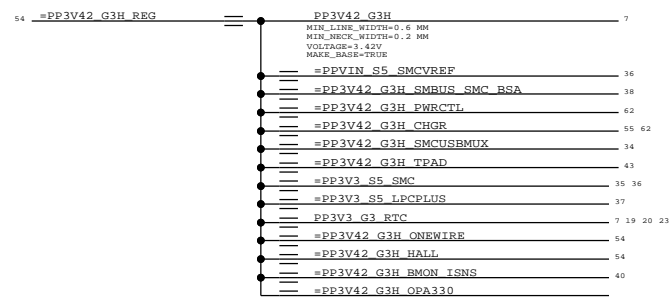
"S5" RAILS



DIGITAL GROUND



"G3H" RAILS

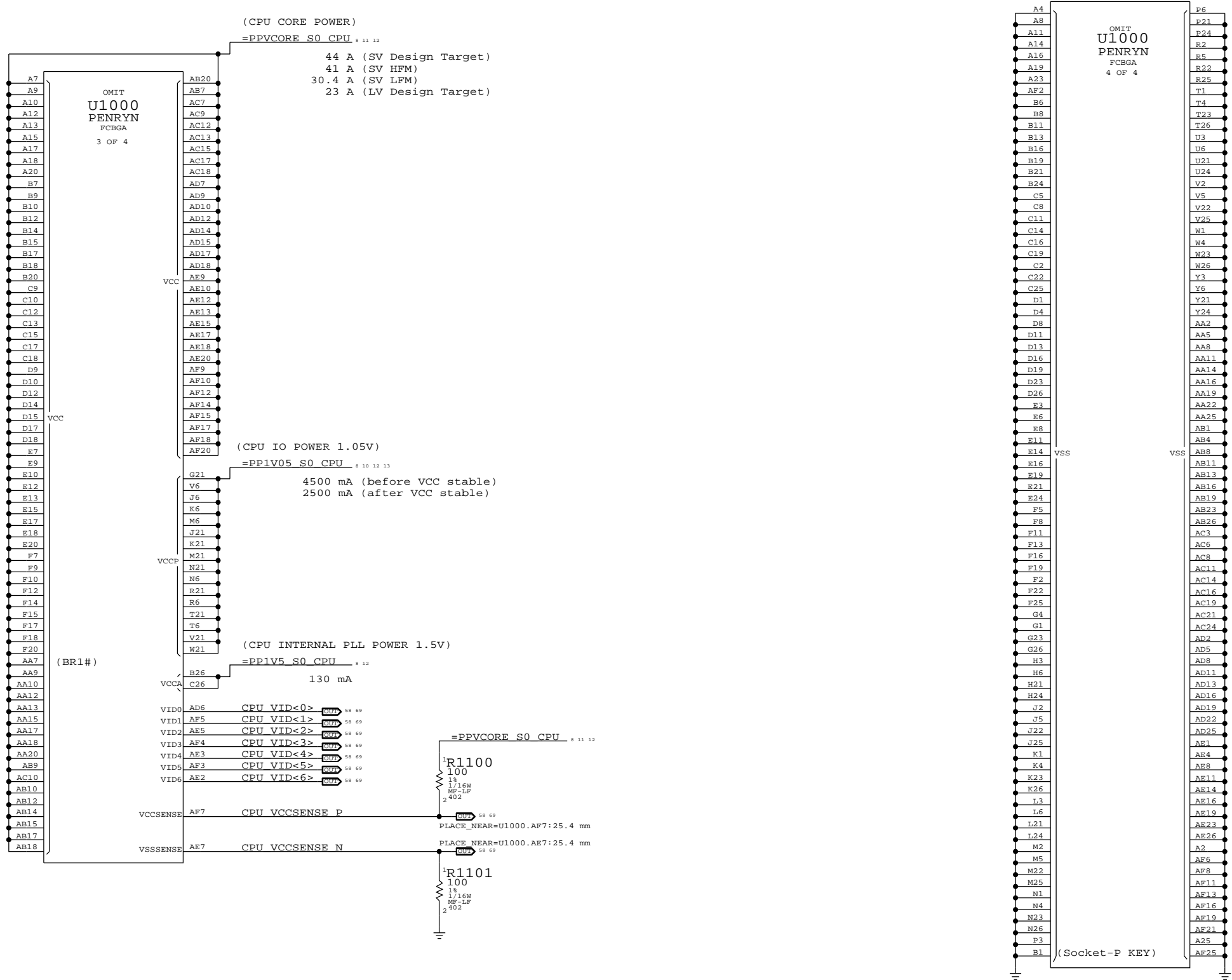


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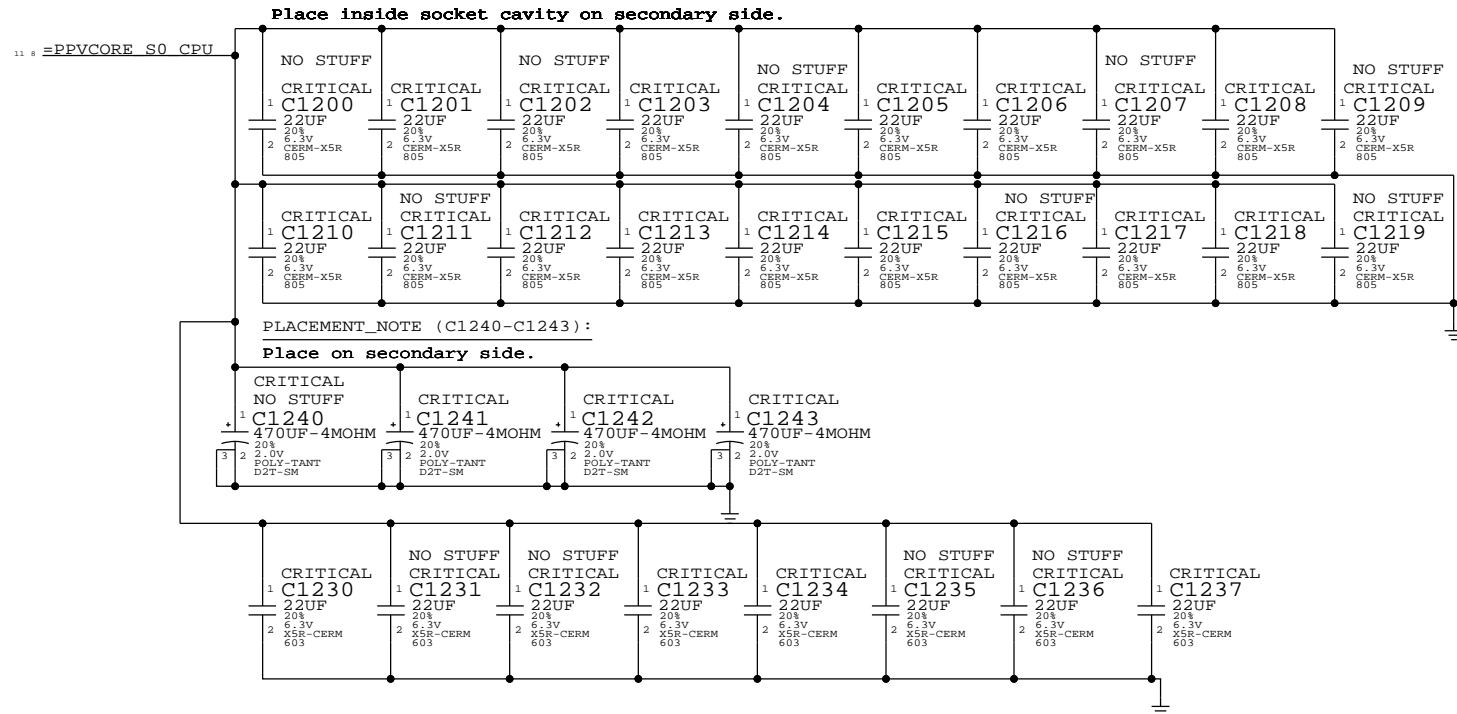




## CPU VCore HF and Bulk Decoupling

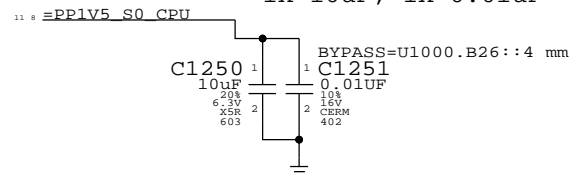
4X 330UF. 20X 22UF 0805

PLACEMENT\_NOTE (C1200-C1219):



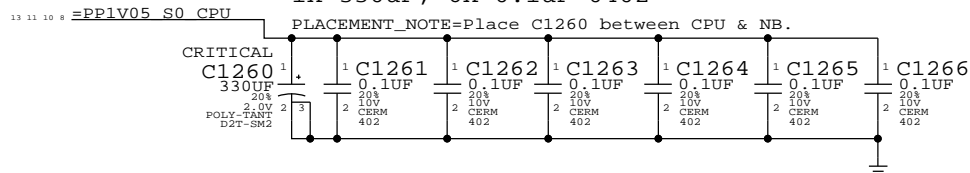
## VCCA (CPU AVdd) DECOUPLING

1x 10uF, 1x 0.01uF



## VCCP (CPU I/O) DECOUPLING

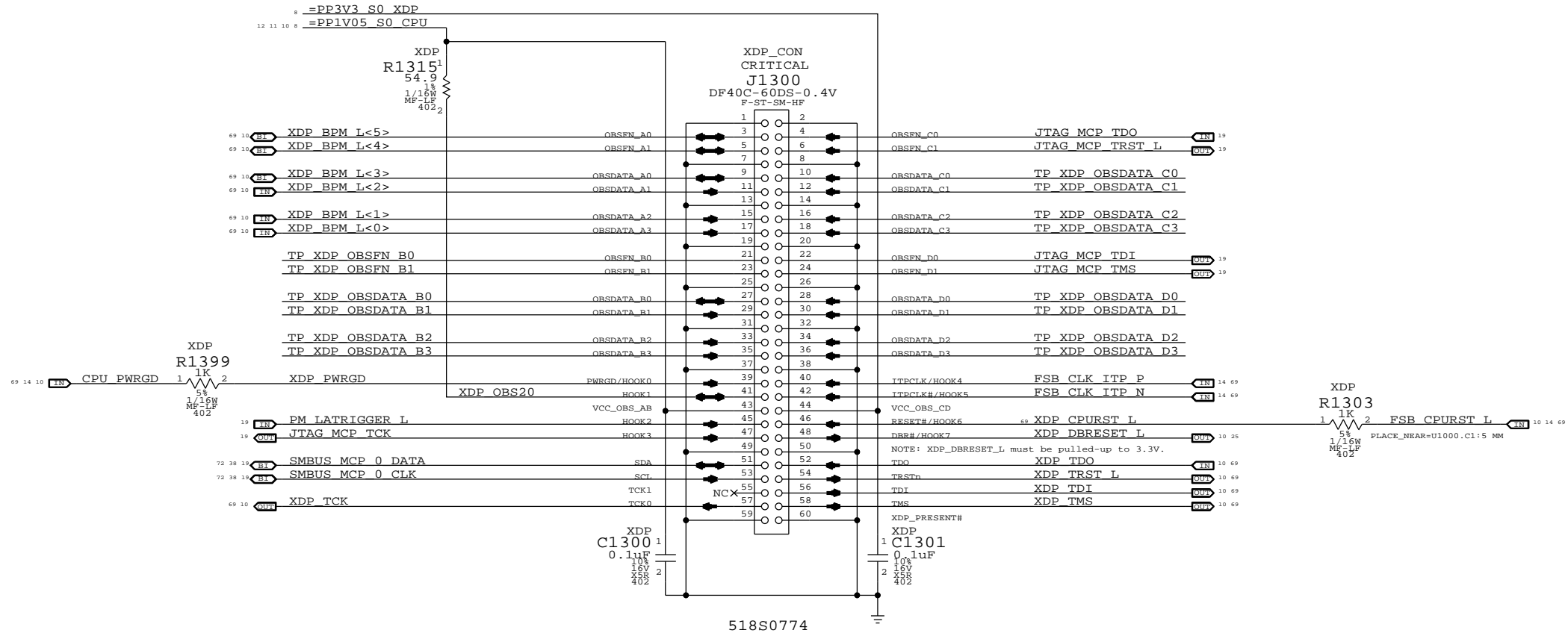
1x 330uF, 6x 0.1uF 0402



# Mini-XDP Connector

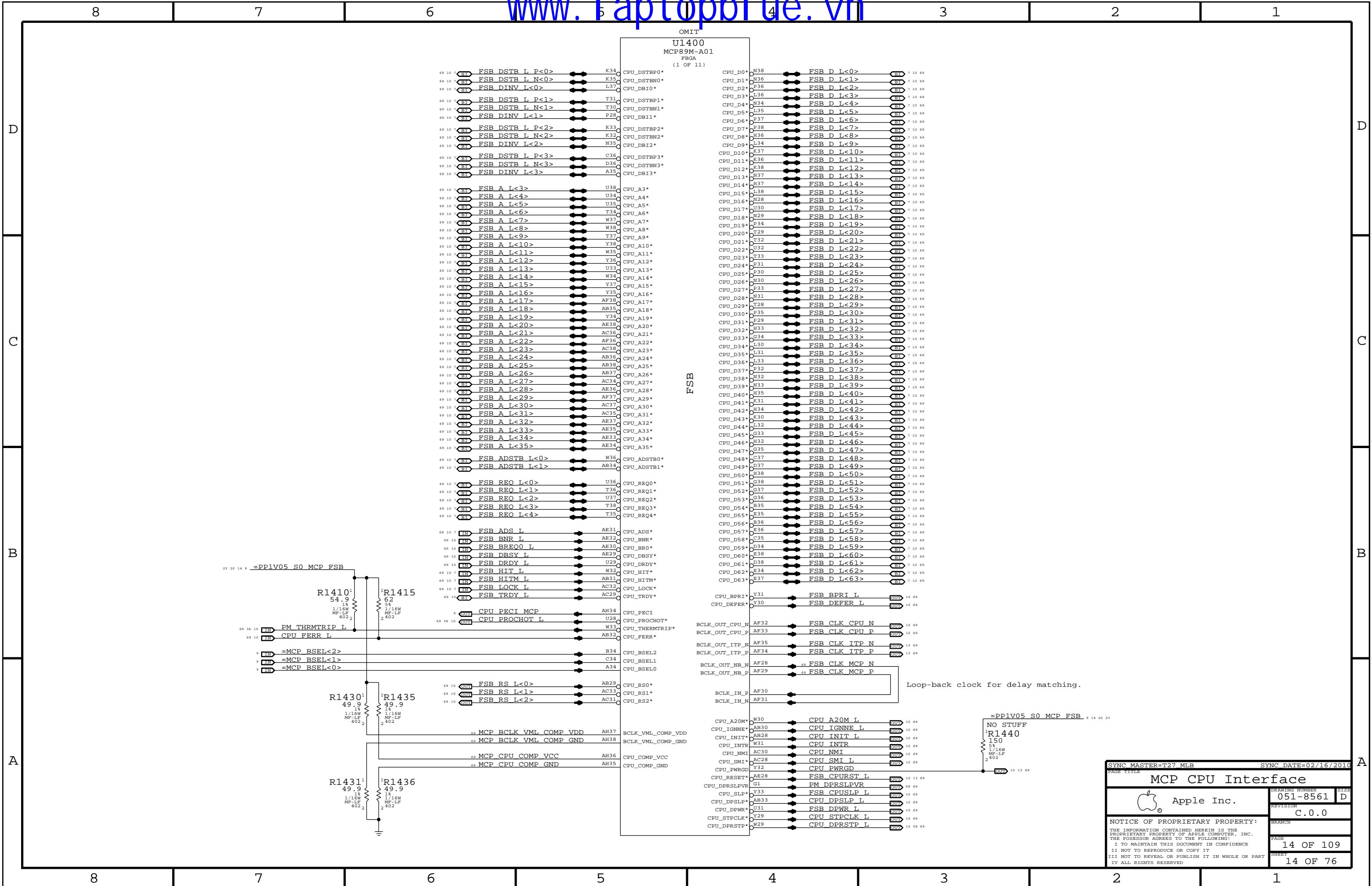
NOTE: This is not the standard XDP pinout.  
USE WITH 920-0782 ADAPTER FLEX TO SUPPORT CPU, MCP DEBUGGING.

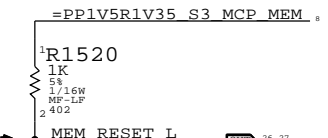
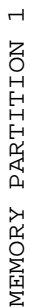
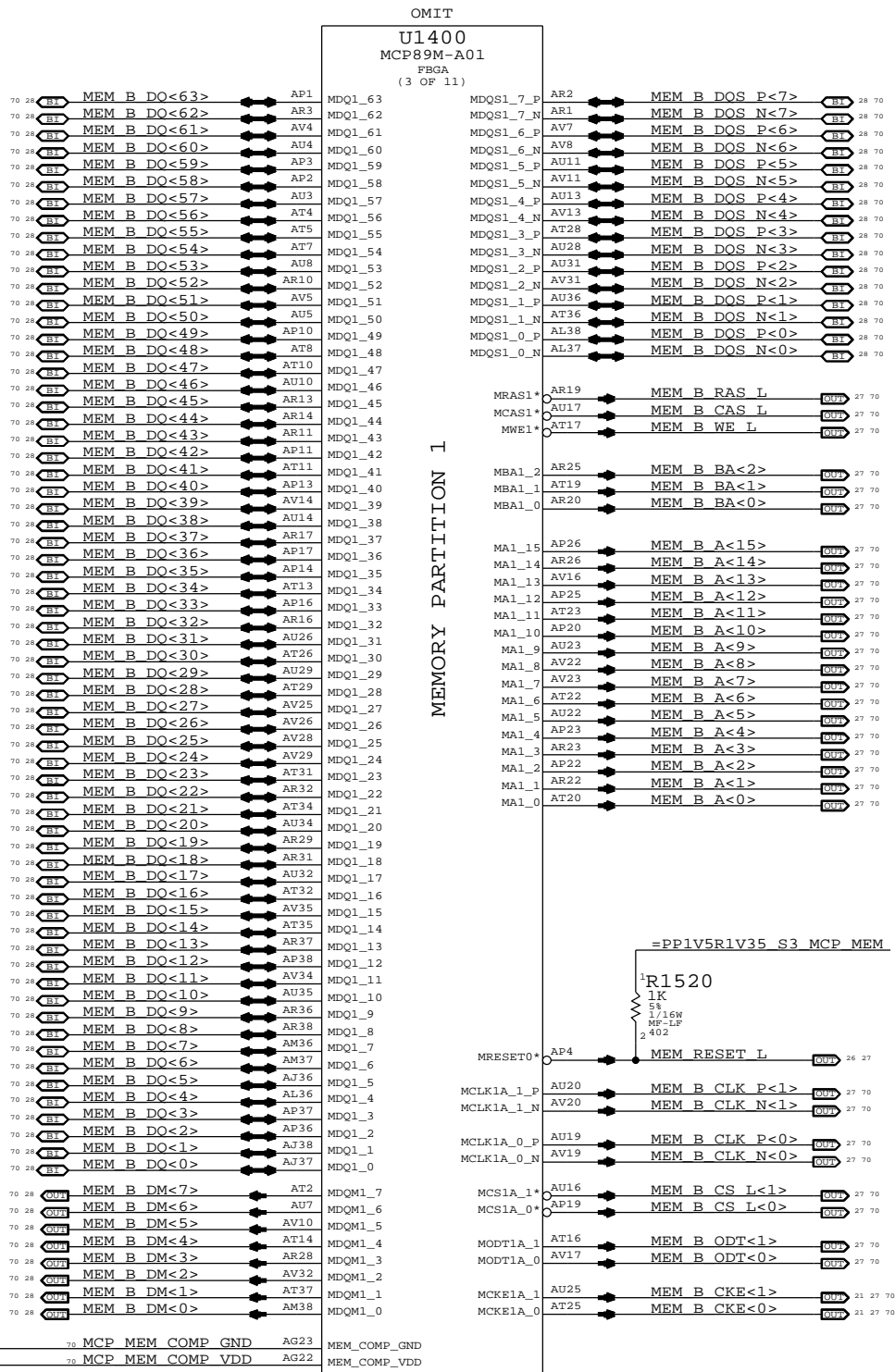
## MCP89-SPECIFIC PINOUT



Direction of XDP module  
Please avoid any obstructions  
ON ODD-NUMBERED SIDE OF J1300







D

D

C

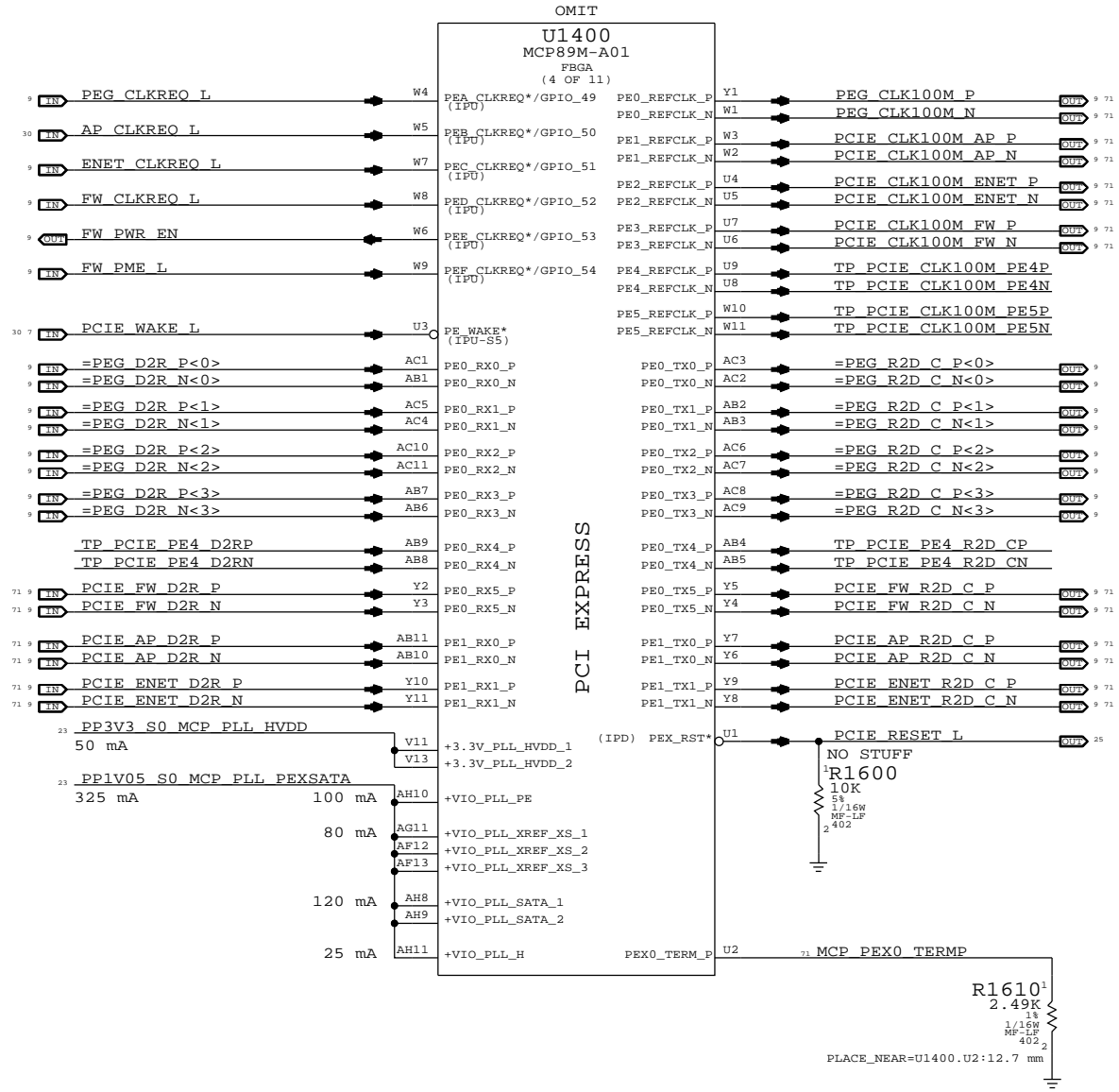
C

B

B

A

A



PE0 ports are Gen2-capable. 4 RCs: 4x, x2, x1, x1  
PE1 ports are Gen1-only. 2 RCs: x1, x1

If PE0[3:0] are not used,  
+VIO\_PE\_AVDD0 and +VIO\_PE\_DVDD0 can be GND

If PE0[4:5] and PE1[0:1] are not used,  
+VIO\_PE\_AVDD1 and +VIO\_PE\_DVDD1 can be GND



## A

B

## A

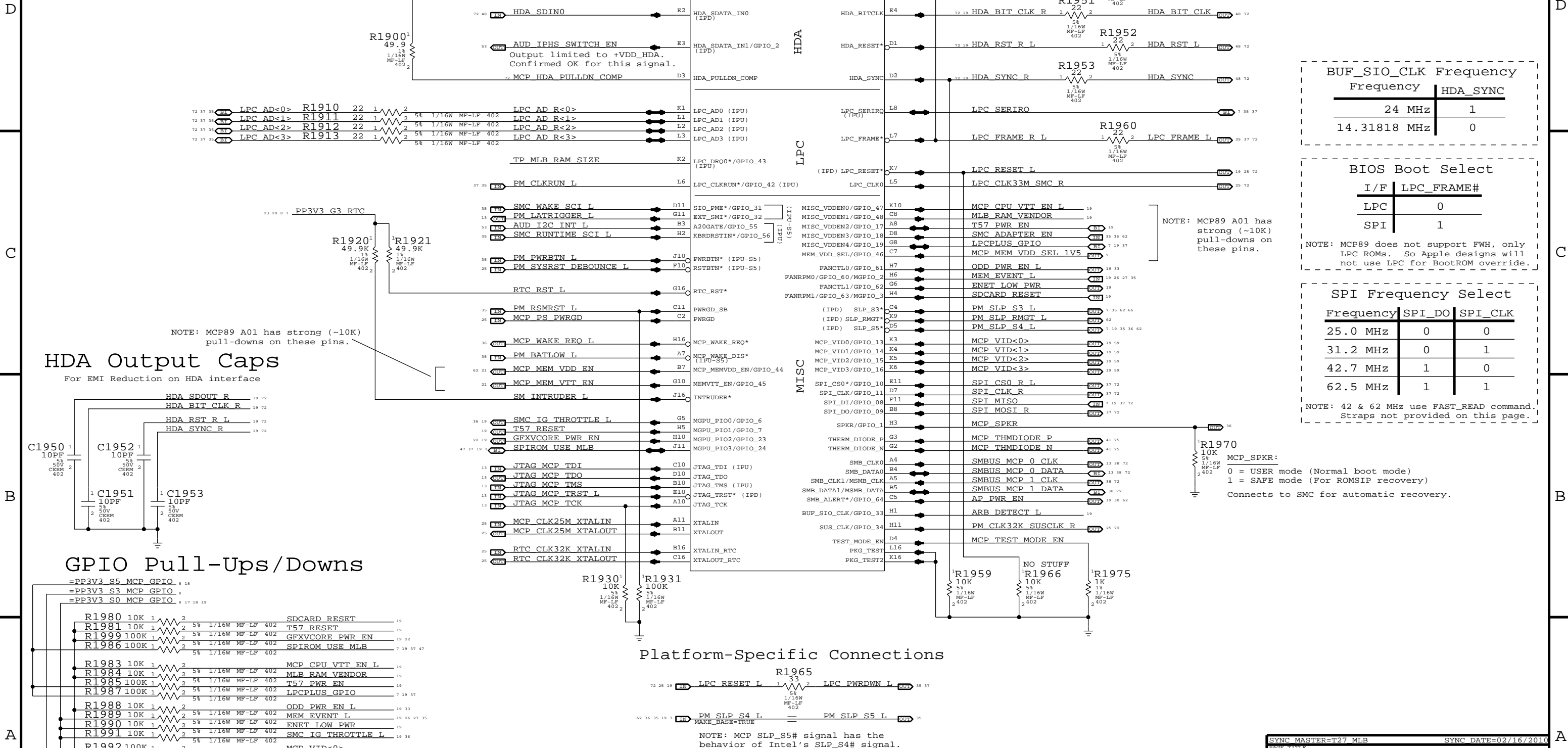


current numbers from MCP89 A01 Bring-Up Support document (MCP89\_TDP\_EDP\_Bringup\_Targets\_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.







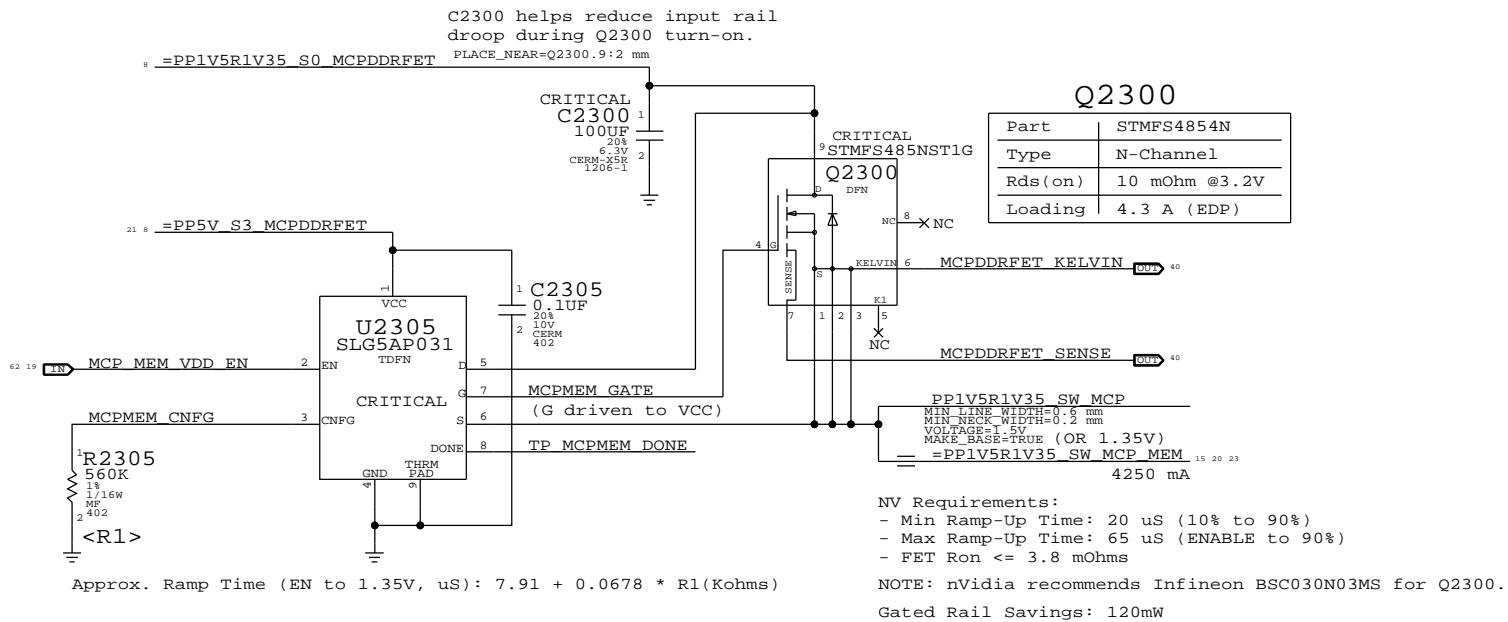


Frequency	SPI_DO	SPI_CLK
25.0 MHz	0	0
31.2 MHz	0	1
42.7 MHz	1	0
62.5 MHz	1	1

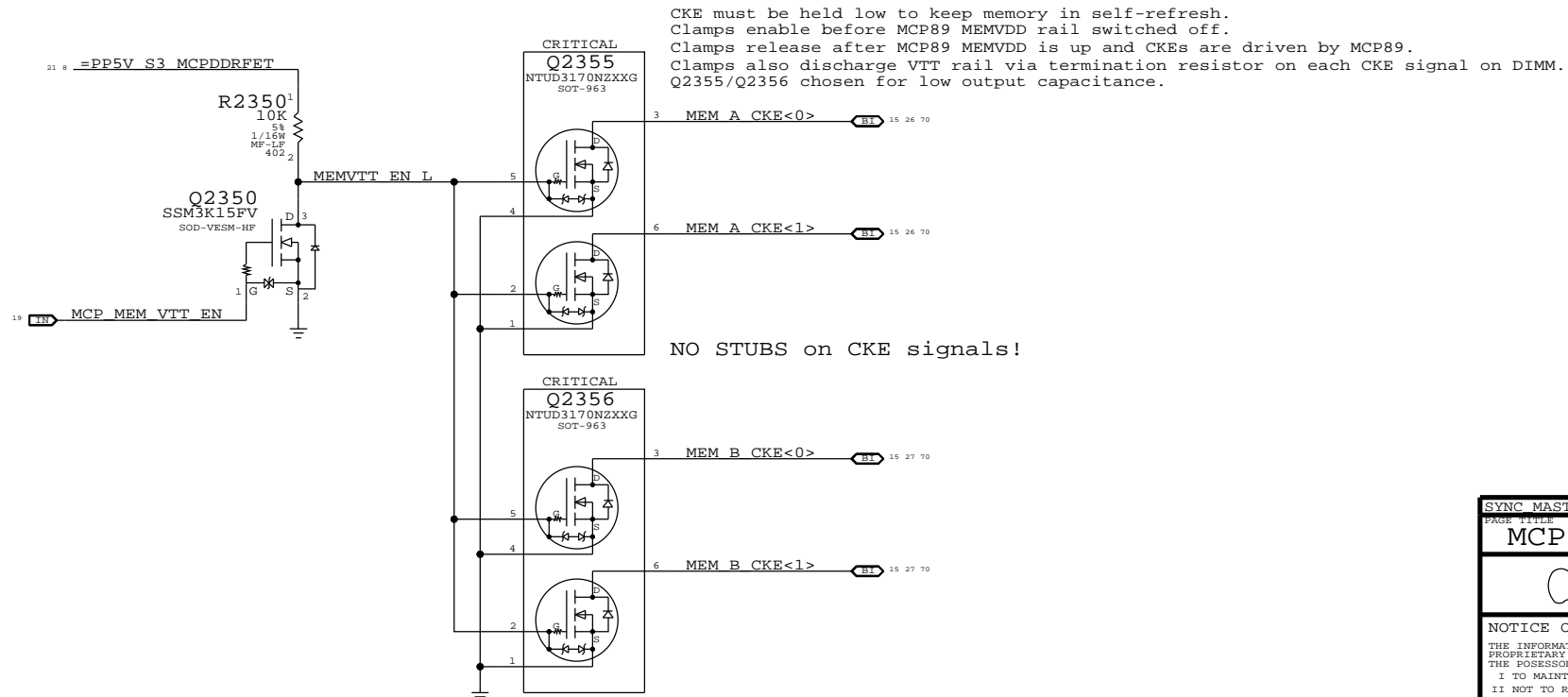
NOTE: MCP89 A01 has strong (~10K) pull-downs on these pins.

MCP\_SPKR:  
0 = USER mode (Normal boot mode)  
1 = SAFE mode (For ROMSIP recovery)  
Connects to SMC for automatic recovery.



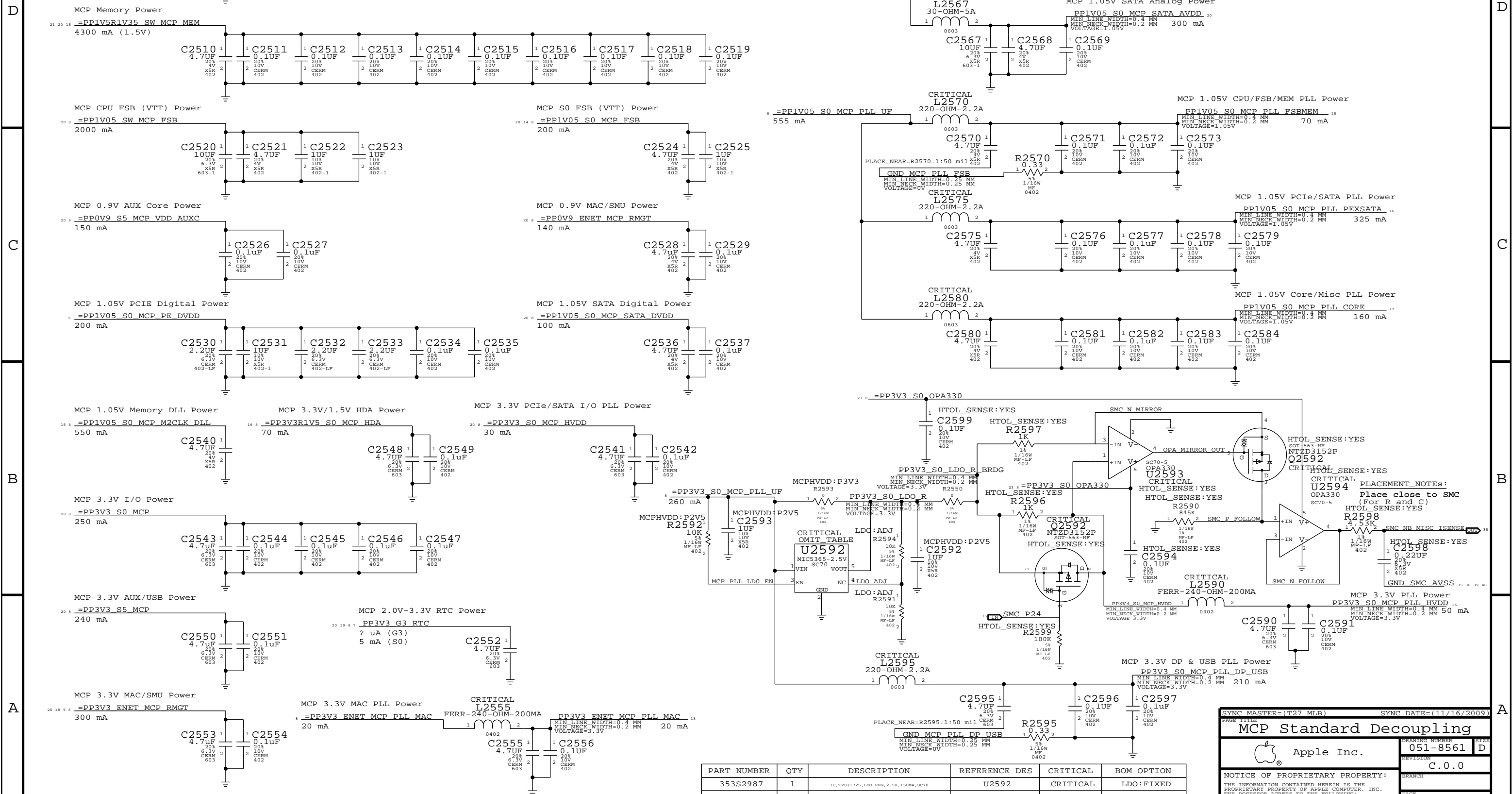


## DIMM CKE Clamps






B	A
---	---



Current #s from MCP89 A01 Bring-Up Support doc (MCP89\_TDP\_EDP\_Bringup\_Targets\_Apple.pdf, dated August 5, 2009)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S2987	1	IC,TPS71725,LDO REG,2.5V,150MA,SC70	U2592	CRITICAL	LDO:FIXED
353S2979	1	IC,LDO,TPS717,ADJ,150MA,3%,SC70,HFLF	U2592	CRITICAL	LDO:ADJ
116S0004	1	RES,0402,0,5%,1/16W	R2596	CRITICAL	HTOL_SENSE:NO

SYNC MASTER=(T27 MLB)		SYNC DATE=(11/16/2009)	
PAGE TITLE			
MCP Standard Decoupling			
 Apple Inc.		DRAWING NUMBER	SIZE
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		C.0.0	
		BRANCH	
		PAGE	25 OF 109
		SHEET	
		23 OF 76	



D

D

C

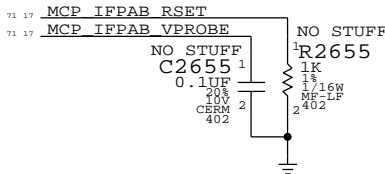
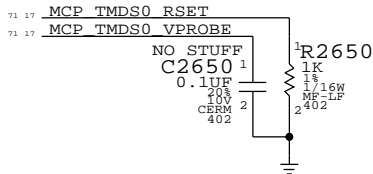
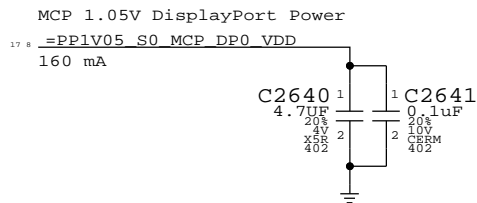
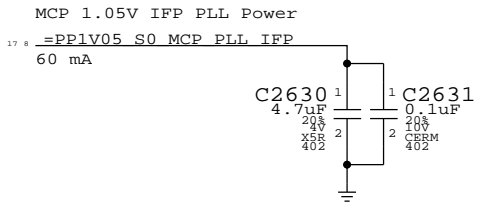
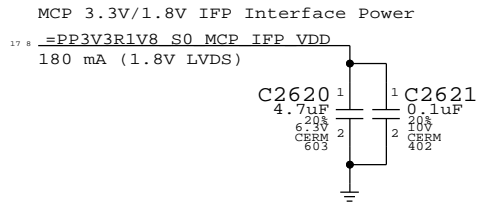
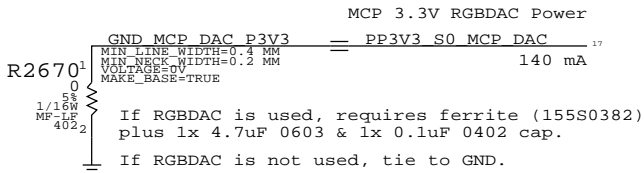
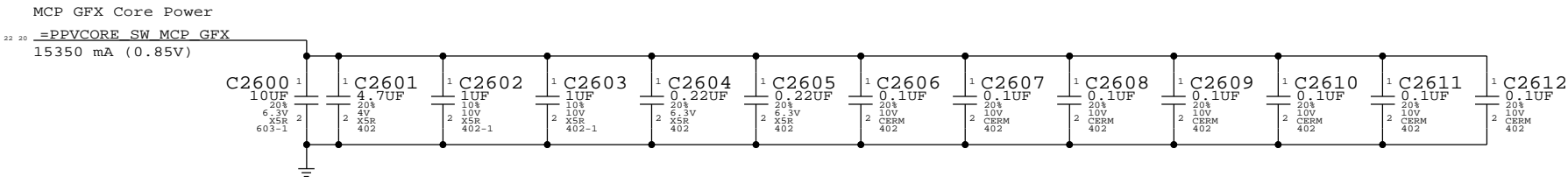
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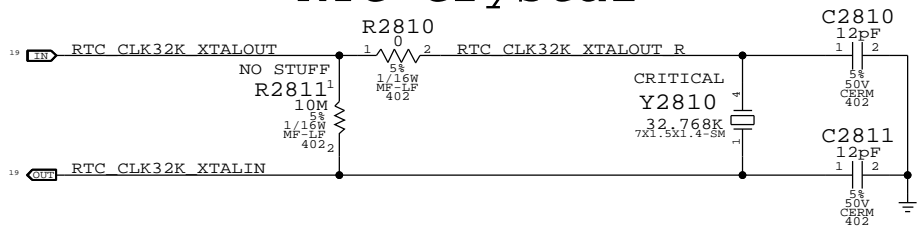
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A

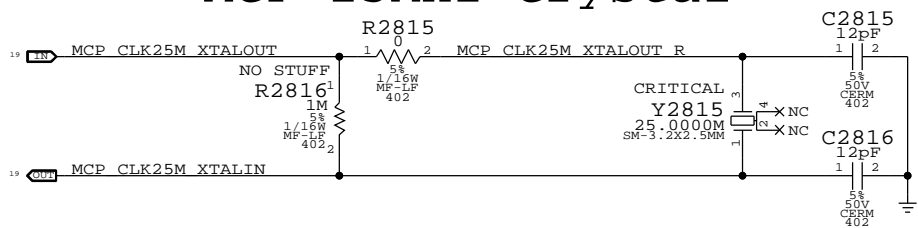
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RTC Crystal

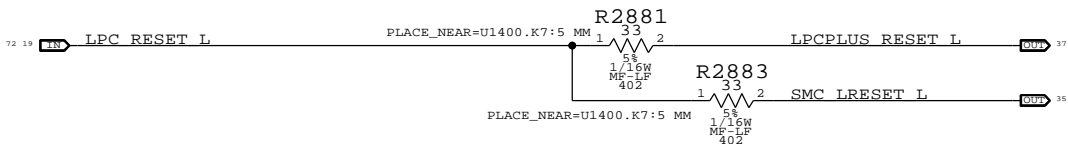


MCP 25MHz Crystal

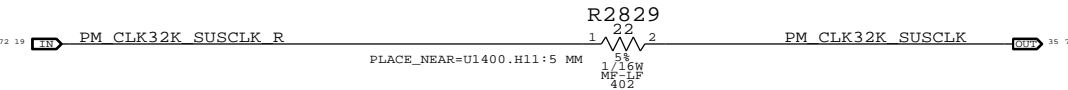
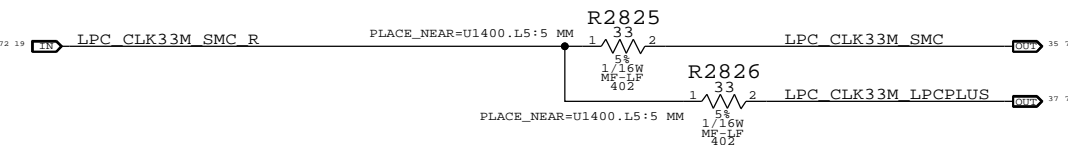
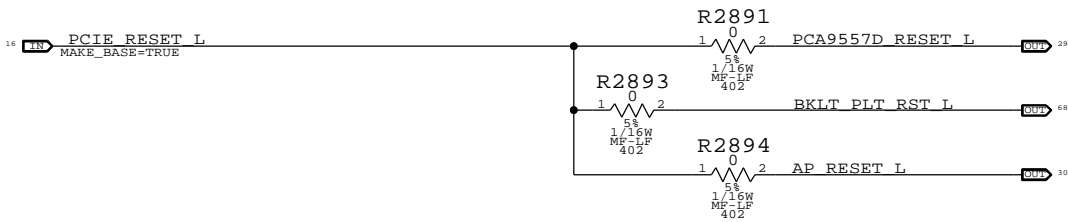


Platform Reset Connections

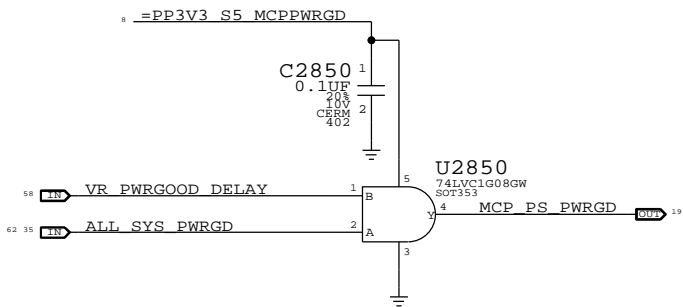
LPC Reset (Unbuffered)



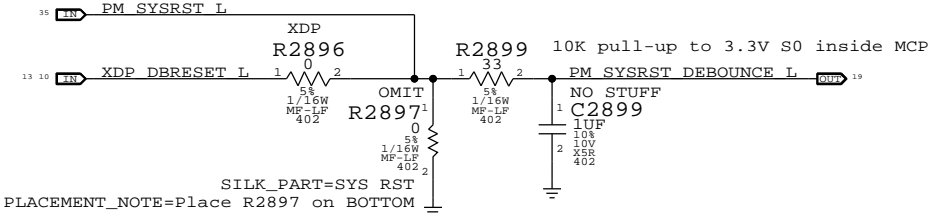
PCIE Reset (Unbuffered)



MCP S0 PWRGD & CPU\_VLD



System Reset Circuit



PAGE TITLE		PAGE NUMBER	
SB Misc		051-8561	
Apple Inc.		C.0.0	
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Page Notes

Power aliases required by this page:

- =PPLVDDR\_S3\_MEM\_A
- =PPDDRVTT\_S0\_MEM\_A
- =PPSPD\_S0\_MEM\_A (2.5 - 3.3V)

Signal aliases required by this page:

- =I2C\_SODIMMA\_SCL
- =I2C\_SODIMMA\_SDA

BOM options provided by this page:

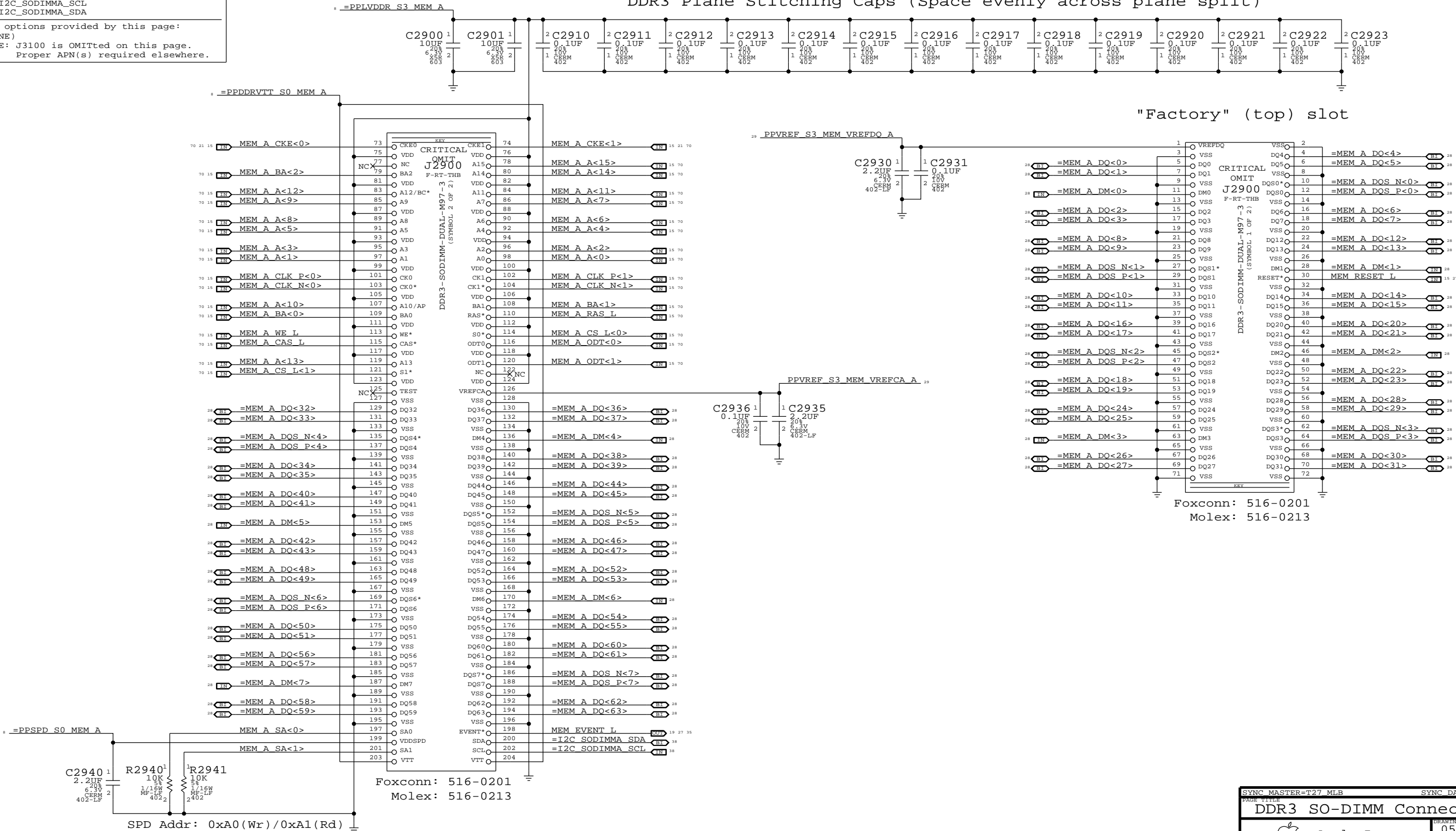
(NONE)


NOTE: J3100 is OMITted on this page.

Proper APN(s) required elsewhere.

DDR3 Plane Stitching Caps (Space evenly across plane split)

"Factory" (top) slot



SYNC MASTER=T27 MLB		SYNC DATE=02/16/2010	
PAGE TITLE			
DDR3 SO-DIMM Connector A			
 Apple Inc.		DRAWING NUMBER	051-8561
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- =PPLVDDR\_S3\_MEM\_B
- =PPDDRVTT\_S0\_MEM\_B
- =PPSPD\_S0\_MEM\_B (2.5 - 3.3V)

Signal aliases required by this page:

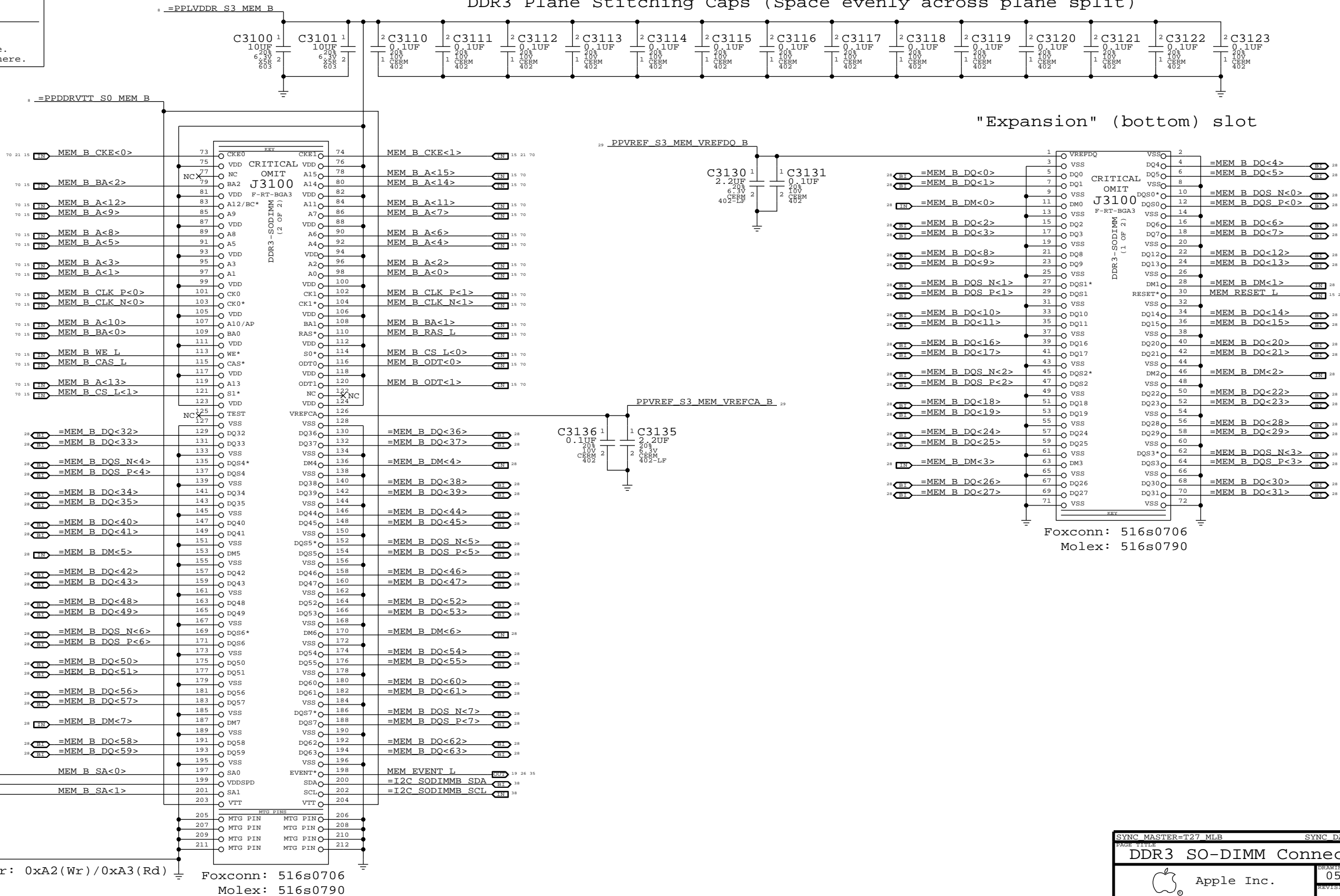
- =I2C\_SODIMMB\_SCL
- =I2C\_SODIMMB\_SDA


BOM options provided by this page:

(NONE)

NOTE: J3100 is OMITted on this page.  
Proper APN(s) required elsewhere.


DDR3 Plane Stitching Caps (Space evenly across plane split)



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PAGE TITLE			
DDR3 SO-DIMM Connector B			
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		REVISION	C.0.0
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BRANCH		PAGE	31 OF 109
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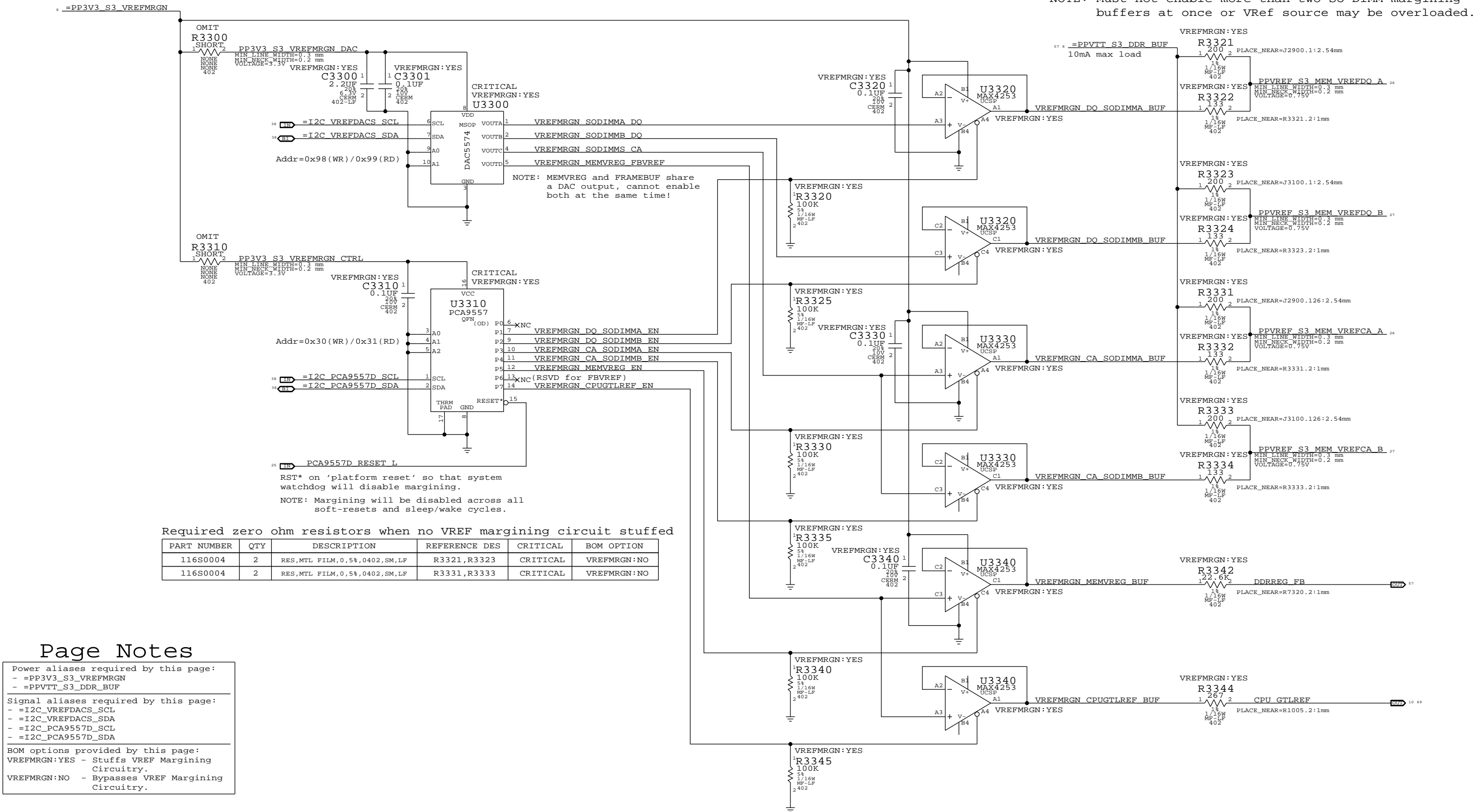
AA

SYNC MASTER=MASTER		SYNC DATE=MASTER	
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SO-DIMM Pinswaps			
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	REVISION		
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D  
C  
B  
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D  
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B  
A



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3321,R3323	CRITICAL	VREFMRGN:NO
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3331,R3333	CRITICAL	VREFMRGN:NO


## Page Notes

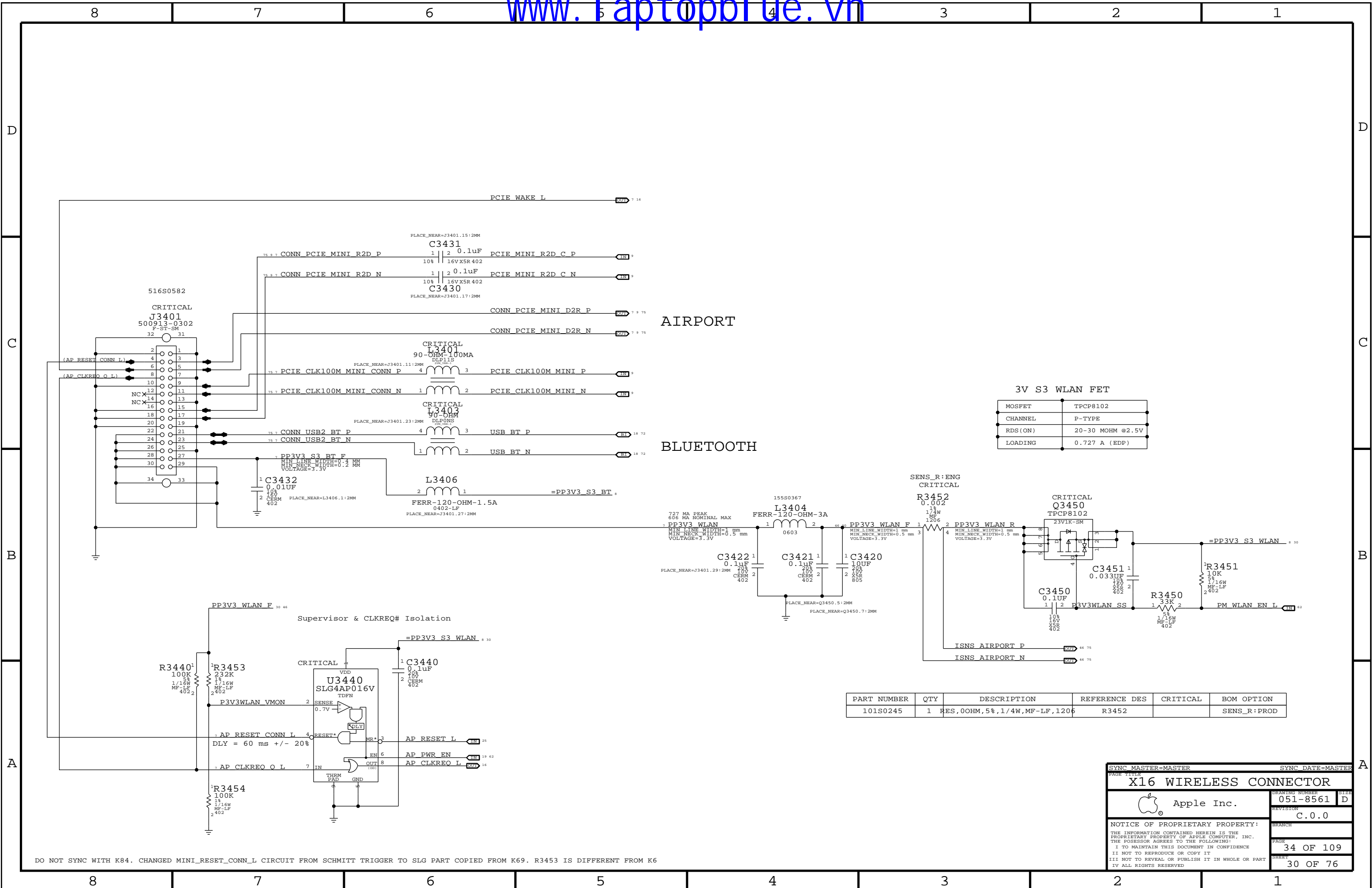
Power aliases required by this page:  
- =PP3V3\_S3\_VREFMRGN  
- =PPVTT\_S3\_DDR\_BUF

Signal aliases required by this page:  
- =I2C\_VREFDACS\_SCL  
- =I2C\_VREFDACS\_SDA  
- =I2C\_PCA9557D\_SCL  
- =I2C\_PCA9557D\_SDA

BOM options provided by this page:  
VREFMRGN:YES - Stuffs VREF Margining Circuitry.  
VREFMRGN:NO - Bypasses VREF Margining Circuitry.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	CPU GTLREF (FSB)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	7
Nominal value			0.75V (DAC: 0x3A)		1.5V (DAC: 0x3A)	0.7V (DAC: 0x8B)
Margined target:			0.300V - 1.200V (+/- 450mV)		1.998V - 1.002V (+/- 498mV)	0.200V - 1.050V (+/- 500mV)
DAC range:			0.000V - 1.501V (0x00 - 0x74)		0.000V - 1.501V (0x00 - 0x74)	0.000V - 1.191V (0x00 - 0x5C)
Vref current:			+3.4mA - -3.4mA (- = sourced)		+33uA - -33uA (- = sourced)	+750uA - -528uA (- = sourced)
DAC step size:			7.69mV / step @ output		8.59mV / step @ output	9.24mV / step @ output

SYNC MASTER=T27_MLB		SYNC DATE=02/16/2010	
PAGE TITLE			
FSB/DDR3 Vref Margining			
 Apple Inc.		DRAWING NUMBER	051-8561
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DO NOT SYNC WITH K84. CHANGED MINI\_RESET\_CONN\_L CIRCUIT FROM SCHMITT TRIGGER TO SLG PART COPIED FROM K69. R3453 IS DIFFERENT FROM K6

SYNC MASTER=MASTER

SYNC DATE=MASTER

X16 WIRELESS CONNECTOR

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051-8561

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30 OF 76

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C

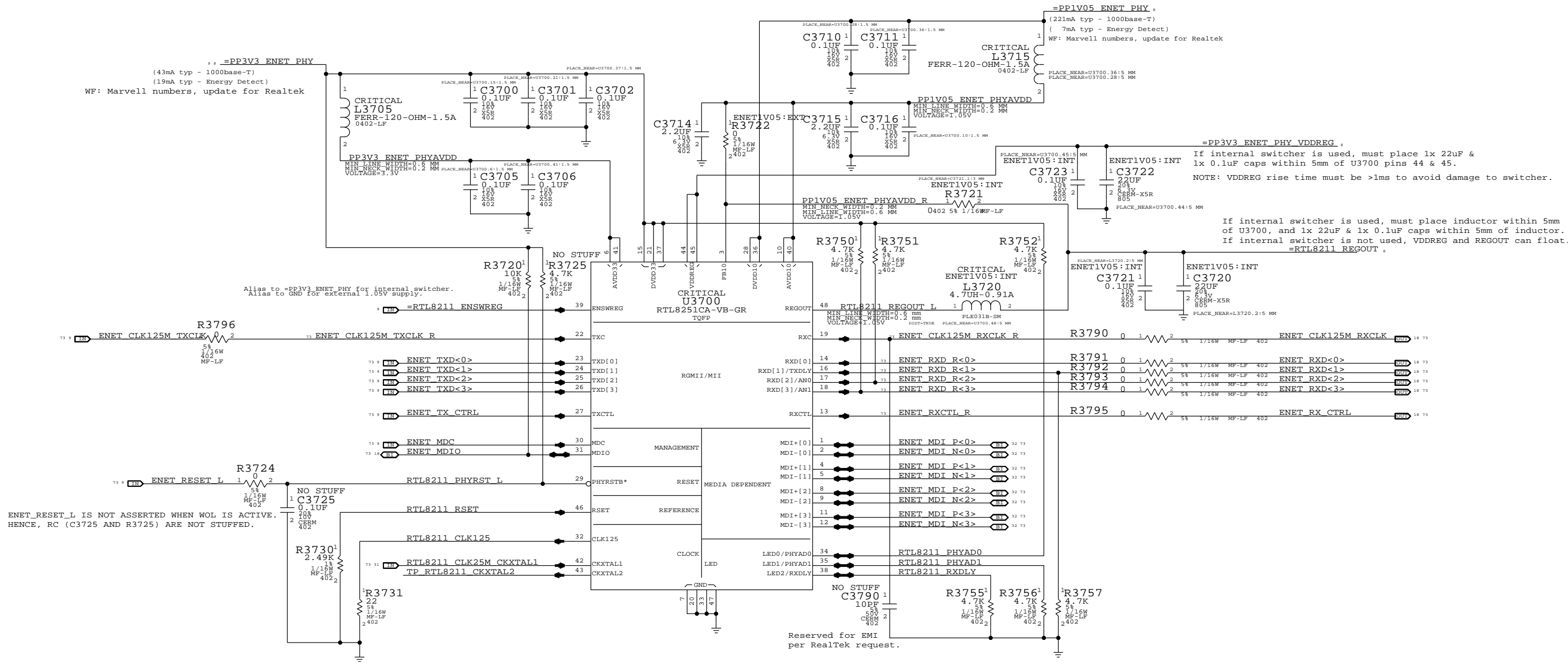
C

B

B

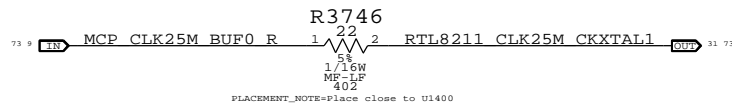
A

A



### RTL8211 25MHz Clock

NOTE: MCP89 CAN PROVIDE 25MHZ CLOCK, BUT CLOCK RUNS WHENEVER RMGT RAILS ARE POWERED.  
Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.



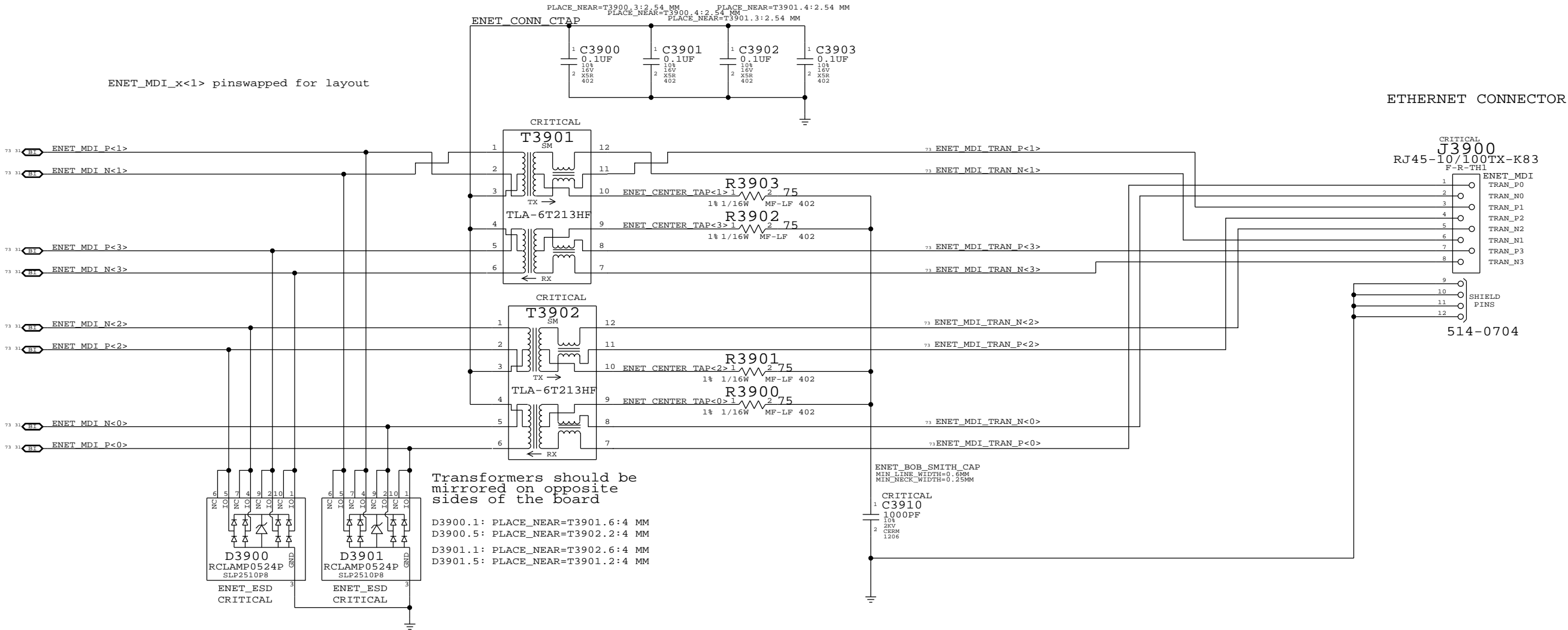
#### Configuration Settings:

PHYAD = 01 (PHY Address 00001)  
AN[1:0] = 11 (Full auto-negotiation)  
RXDLY = 0 (RXCLK transitions with data)  
TXDLY = 0 (No TXCLK Delay)


DO NOT SYNC, EXTERNAL 1.05V REGULATOR OPTION

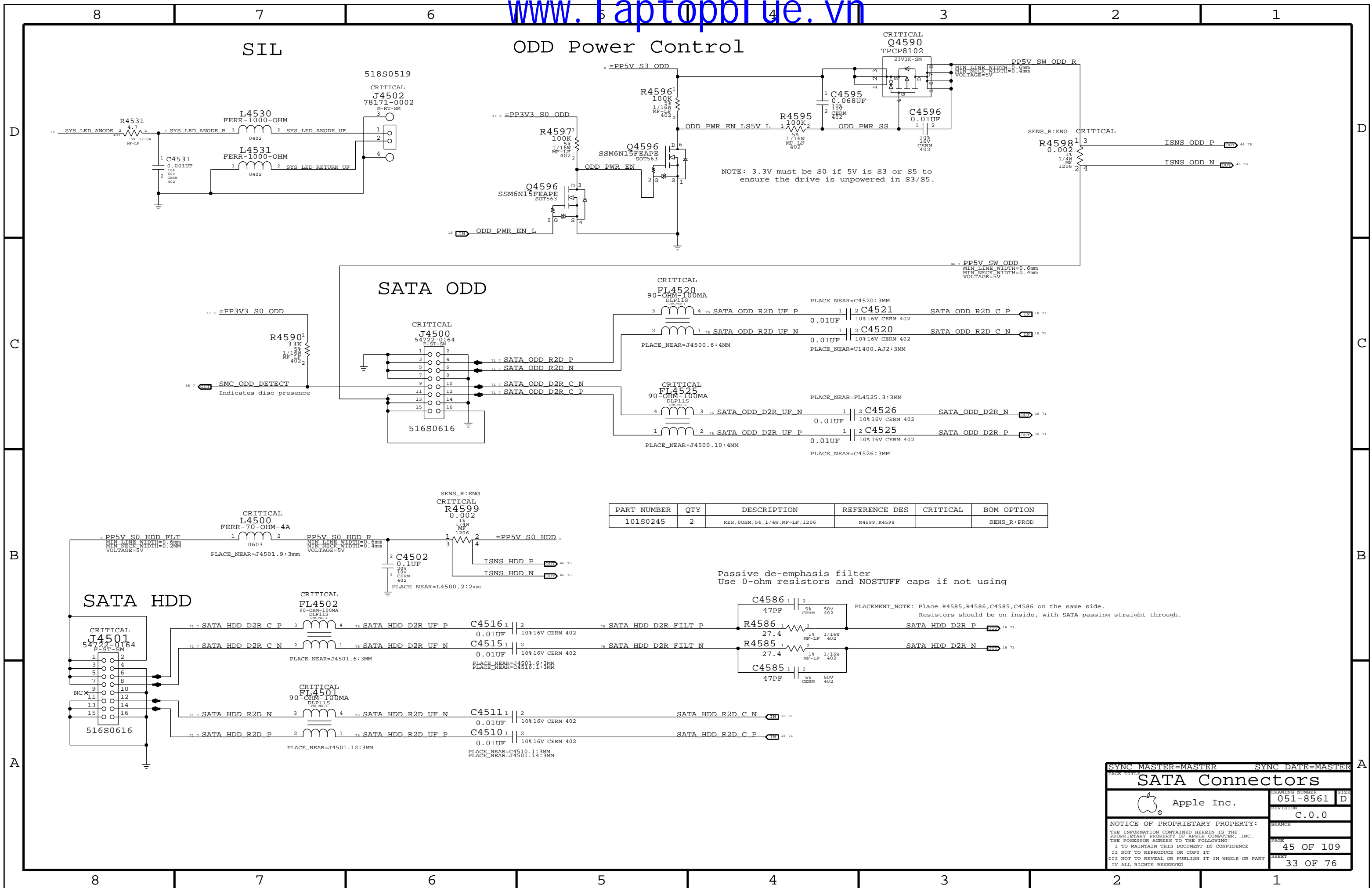
SYNC MASTER=MASTER		SYNC DATE=MASTER	
PAGE TITLE		PAGE	
Ethernet PHY (RTL8211CL)		DRAWING NUMBER	051-8561
Apple Inc.		REVISION	C.0.0
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- COPY THIS PAGE FROM K36 CSA.39



DO NOT SYNC FROM K6, WITH K84'S CONNECTOR

SYNC MASTER=MASTER		SYNC DATE=MASTER	
ETHERNET CONNECTOR			
 Apple Inc.		DRAWING NUMBER	051-8561
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		SHEET	32 OF 76
		SIZE	D

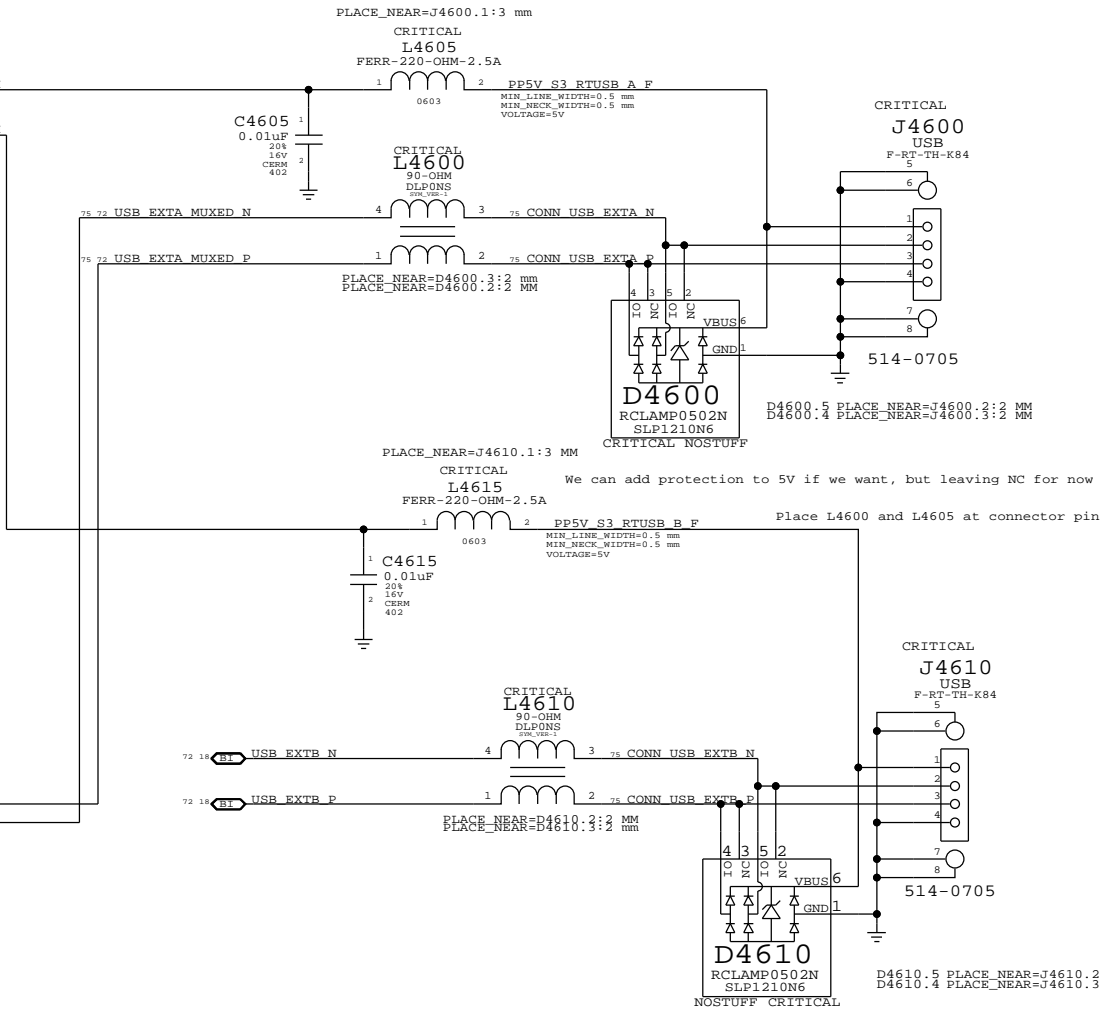
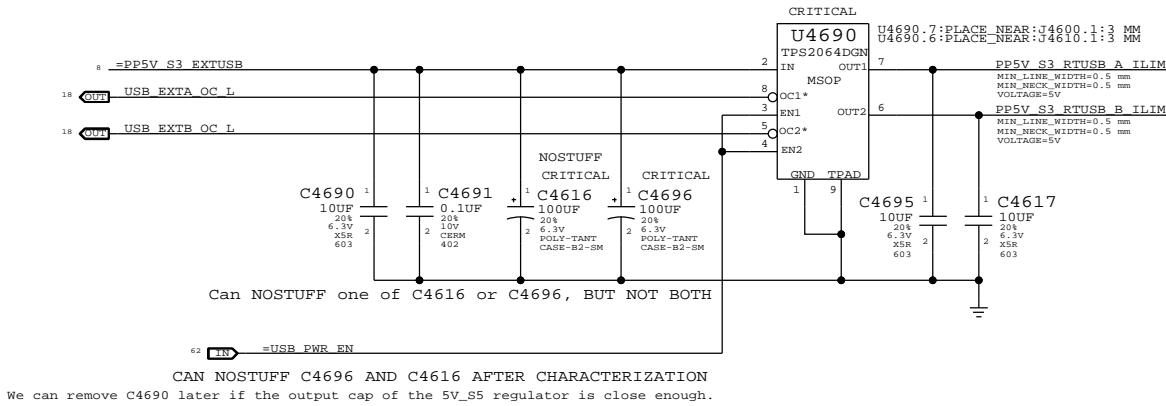




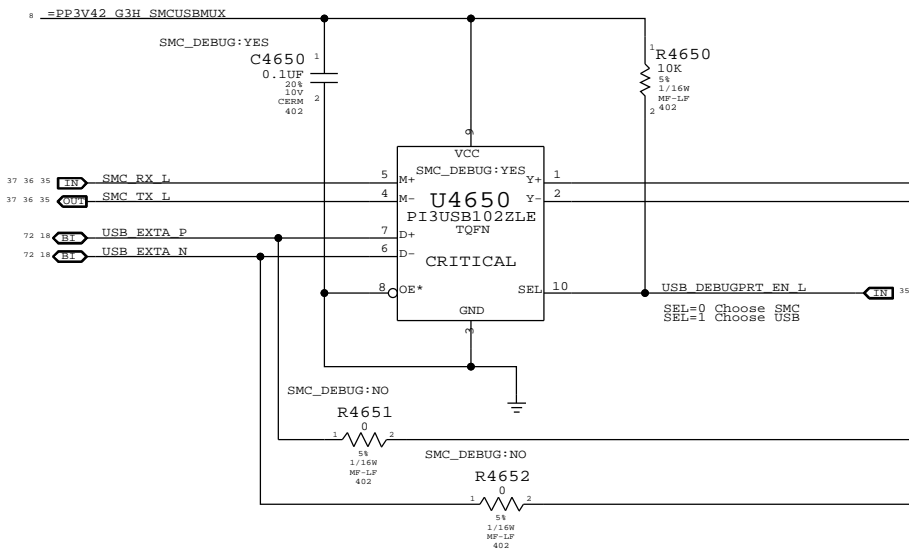
POR IS METAL USB CONNECTOR PARTS

Port Power Switch

USB PORT A (FRONT PORT)




USB/SMC Debug Mux

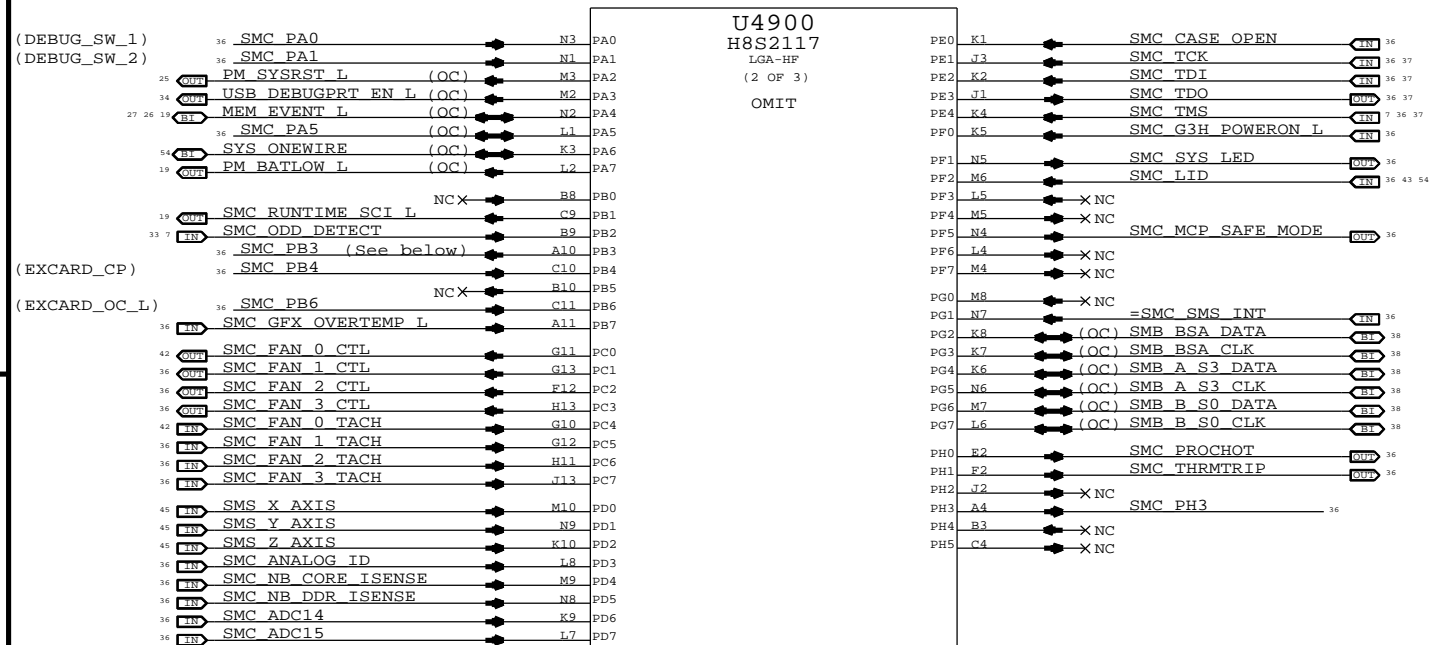
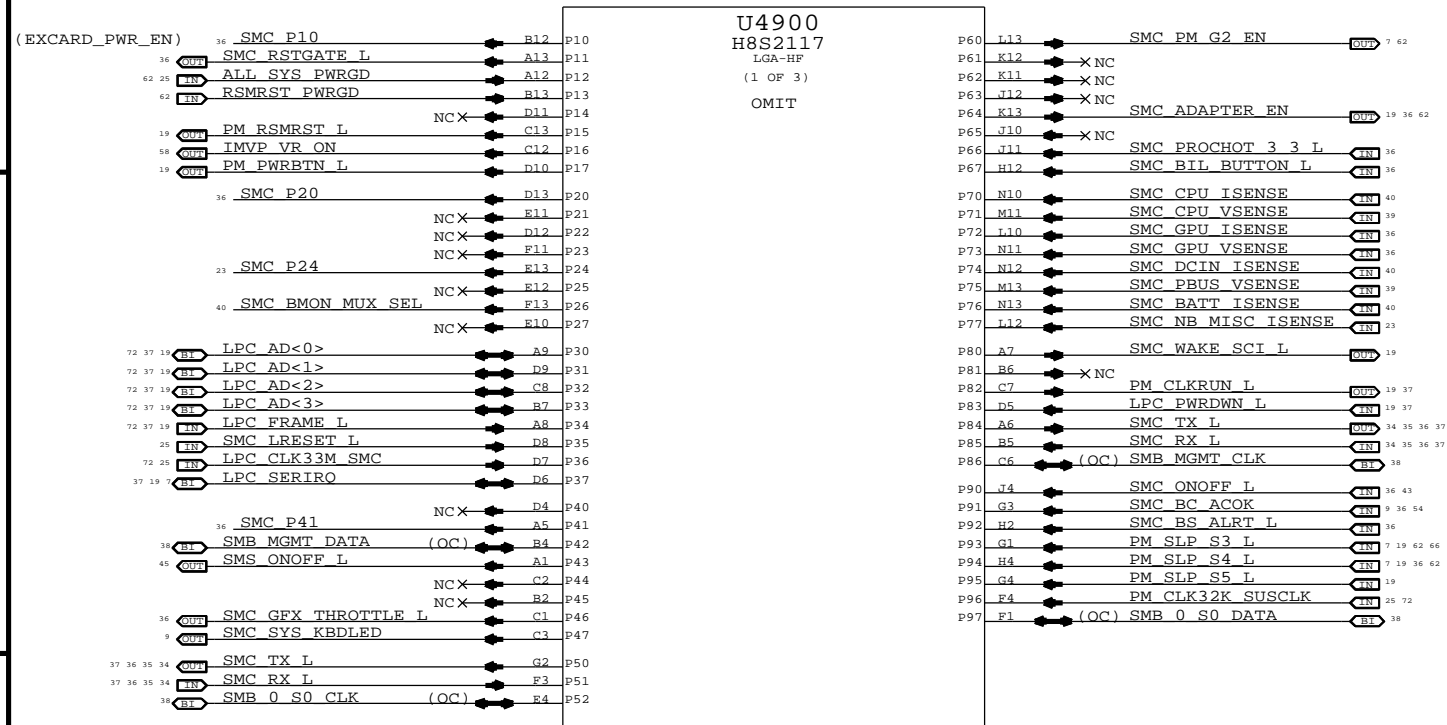


USB PORT B (BACK PORT)

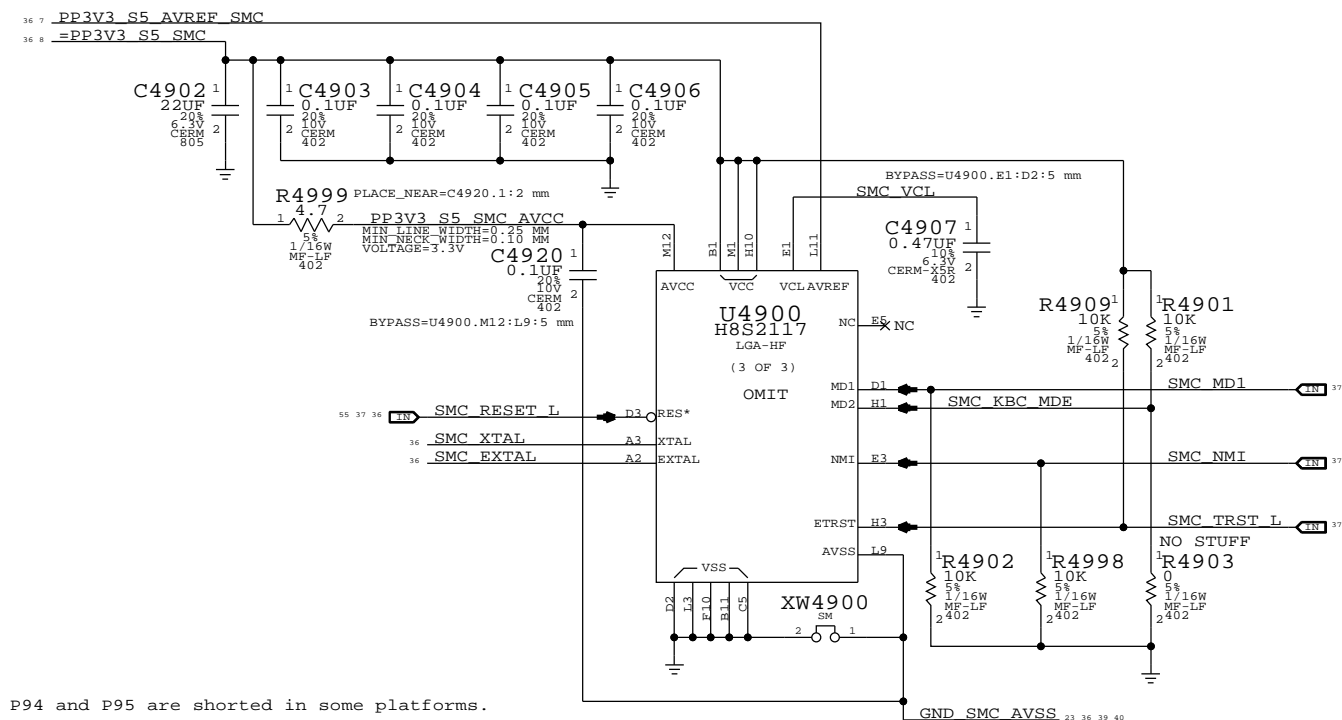
DO NOT SYNC WITH K84. UPDATED PLACE NEAR NOTES  
UPDATED SMC\_DEBUG BOMOPTION, STUFFED C4690

SYNC MASTER=(K84_MLB)		SYNC DATE=(10/03/2009)	
PAGE TITLE			
External USB Connectors			
 Apple Inc.		DRAWING NUMBER	8142
		051-8561	D
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NOTE: Unused pins have "SMC\_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.




SMC\_PB3:  
SMC\_IG\_THROTTLE\_L for MG systems.  
Otherwise, TP/NC okay.



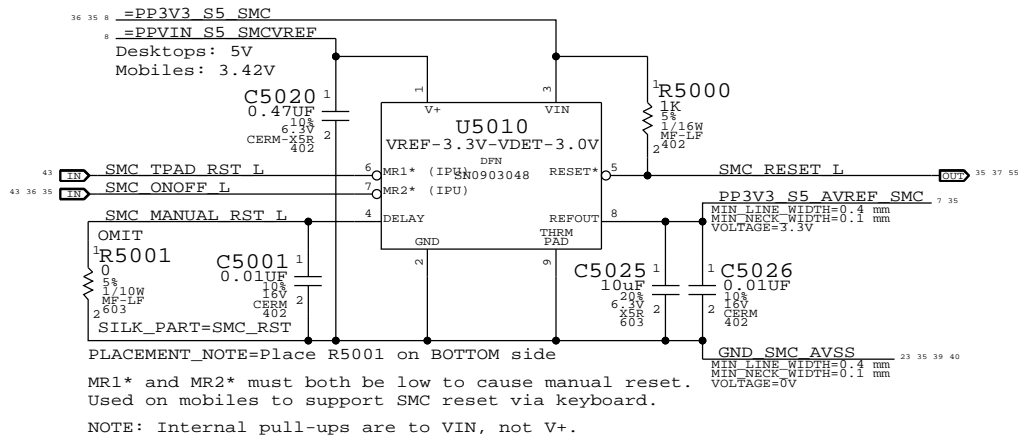
NOTE: P94 and P95 are shorted in some platforms.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.  
If SMS interrupt is not used, pull up to SMC rail.

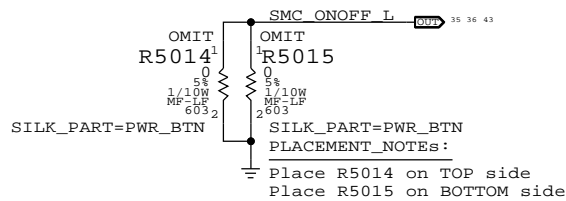
```
H8S2117-R:
(SMC_PECI)
(SMC_PECI_VREF)
(SMC_PECI_VSTP)
```

SYNC MASTER=T27 MLB		SYNC DATE=02/16/2010	
PAGE TITLE			
SMC			
 Apple Inc.		DRAWING NUMBER <b>051-8561</b>	
		SIZE <b>D</b>	
		REVISION <b>C.0.0</b>	
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		SHEET <b>35 OF 76</b>	

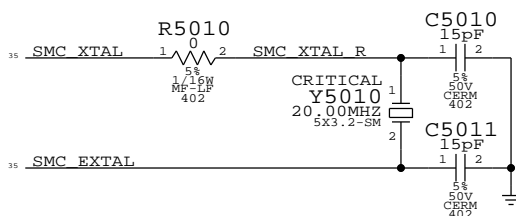
## SMC Reset "Button", Supervisor & AVREF Supply



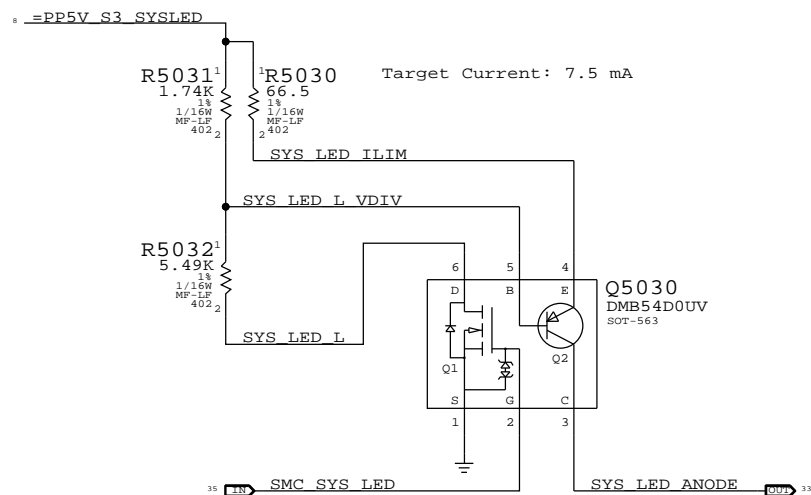
## Debug Power "Buttons"



## SMC Crystal Circuit

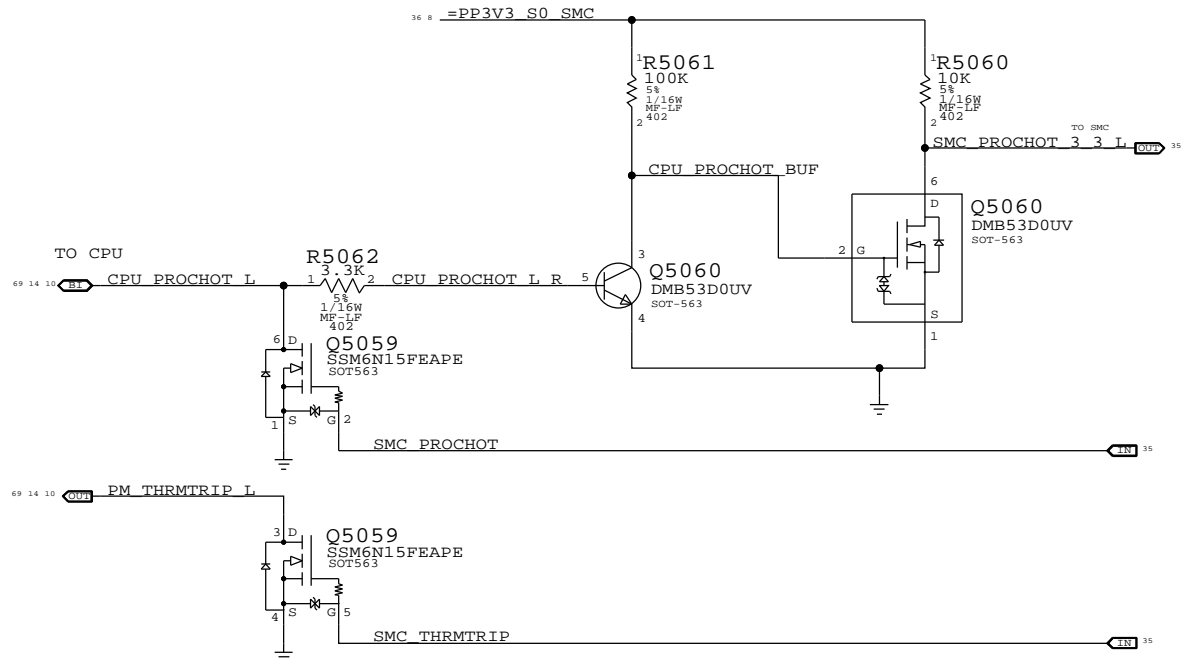


## System (Sleep) LED Circuit

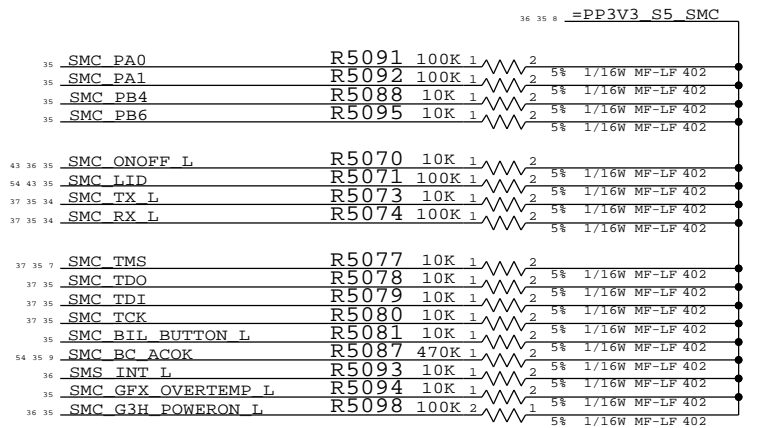


R5030,R5031,R5032 CHANGED FOR DIMMER LED

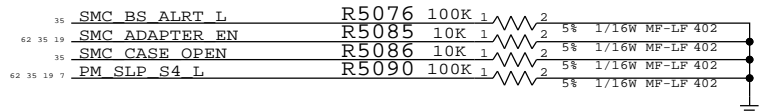
## SMC FSB to 3.3V Level Shifting



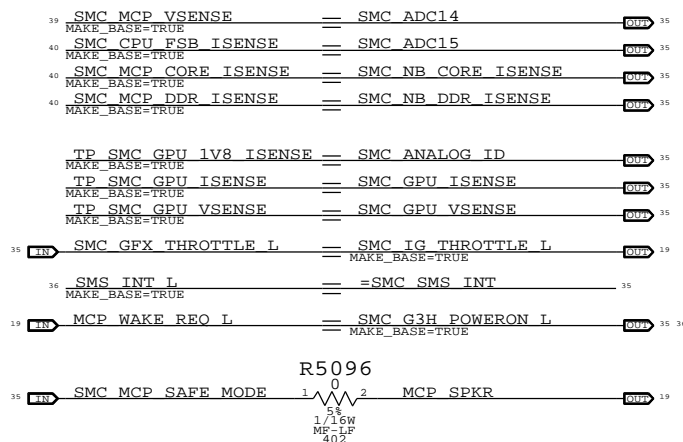
## SMC Pull-ups



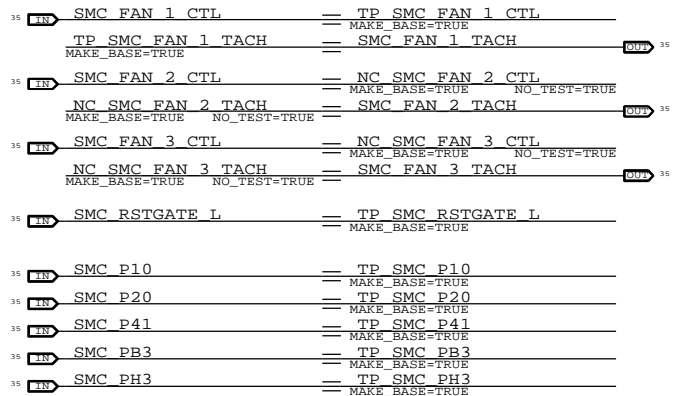
## SMC Pull-downs



## SMC Aliases

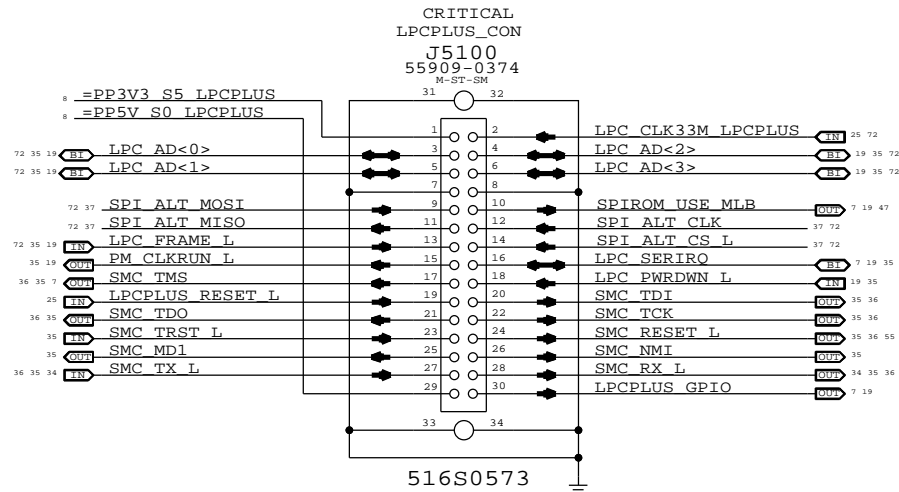


## Unused Pins

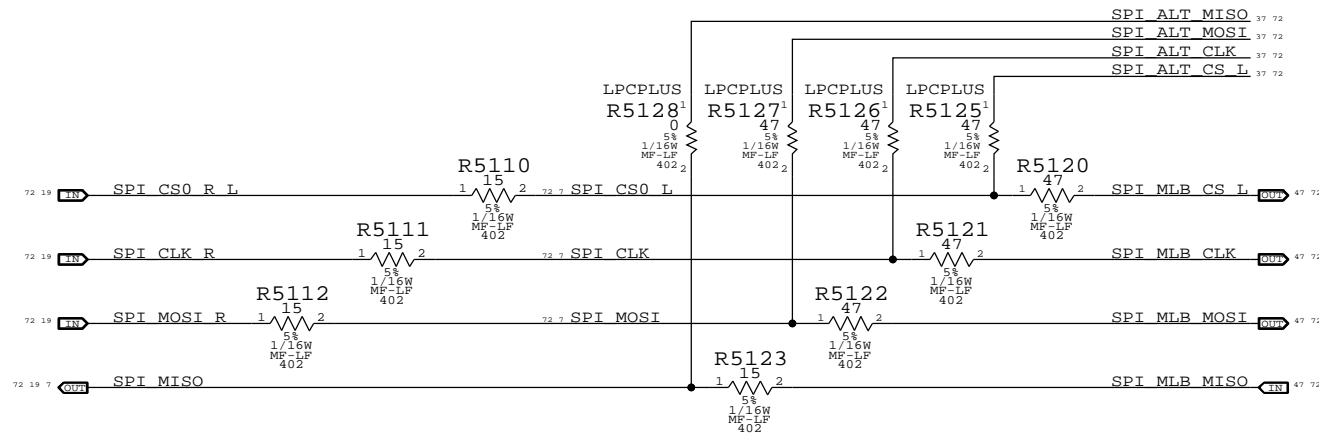


SYNC MASTER=(T27 MLB)		SYNC DATE=(10/27/2009)	
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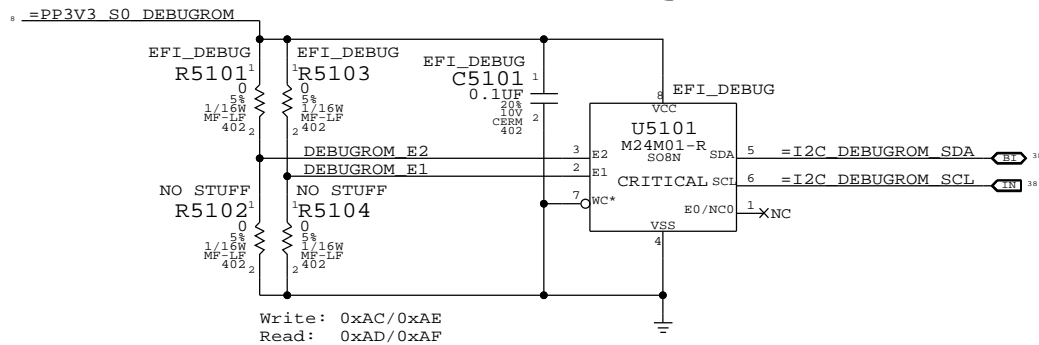
## LPC+SPI Connector




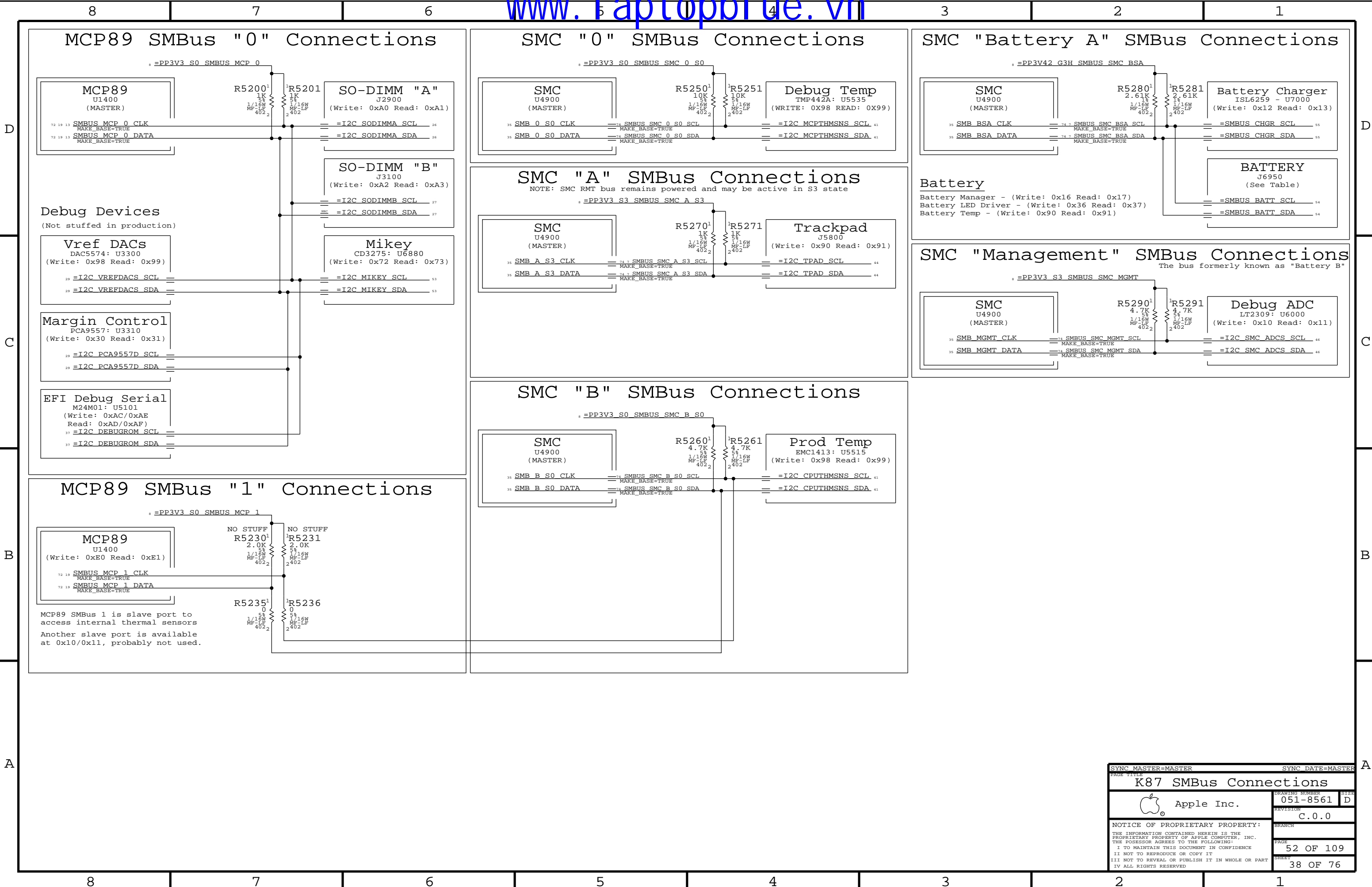
## SPI Bus Series Termination



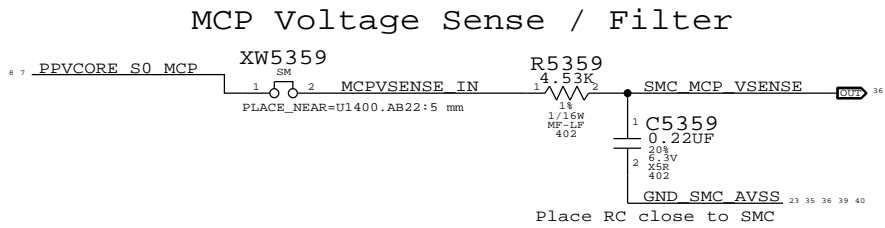
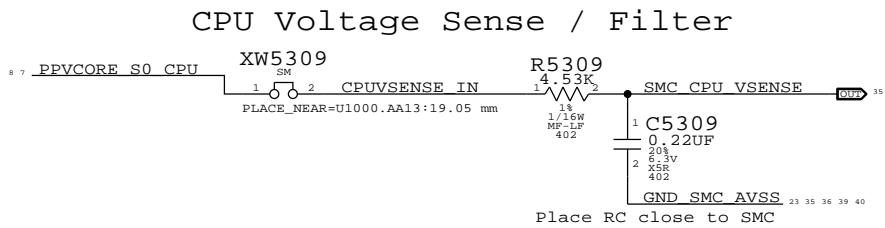
## EFI Debug ROM



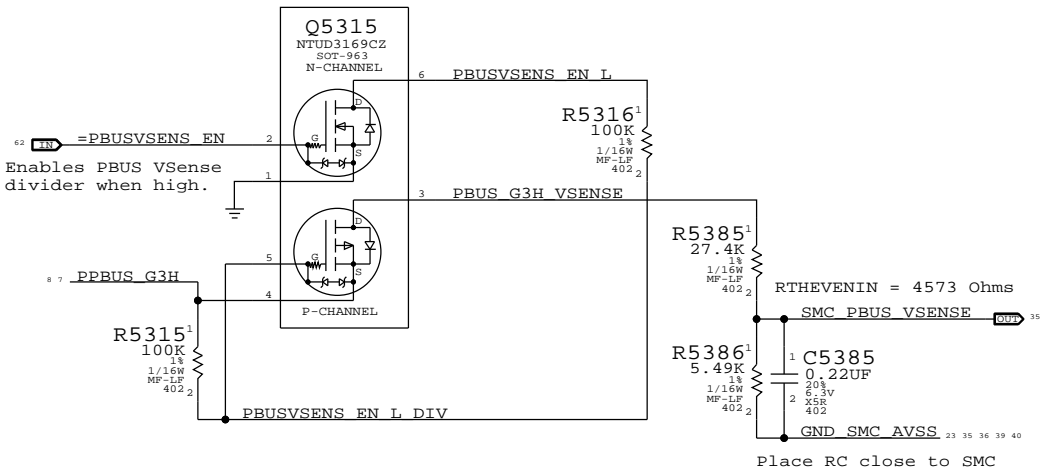
SYNC MASTER=(T27 MLB)		SYNC DATE=(12/15/2009)	
PAGE TITLE			
LPC+SPI Debug Connector			
 Apple Inc.		DRAWING NUMBER	051-8561
		SIZE	D
		REVISION	C.0.0
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PBUS Voltage Sense Enable & Filter



D

C

B

A

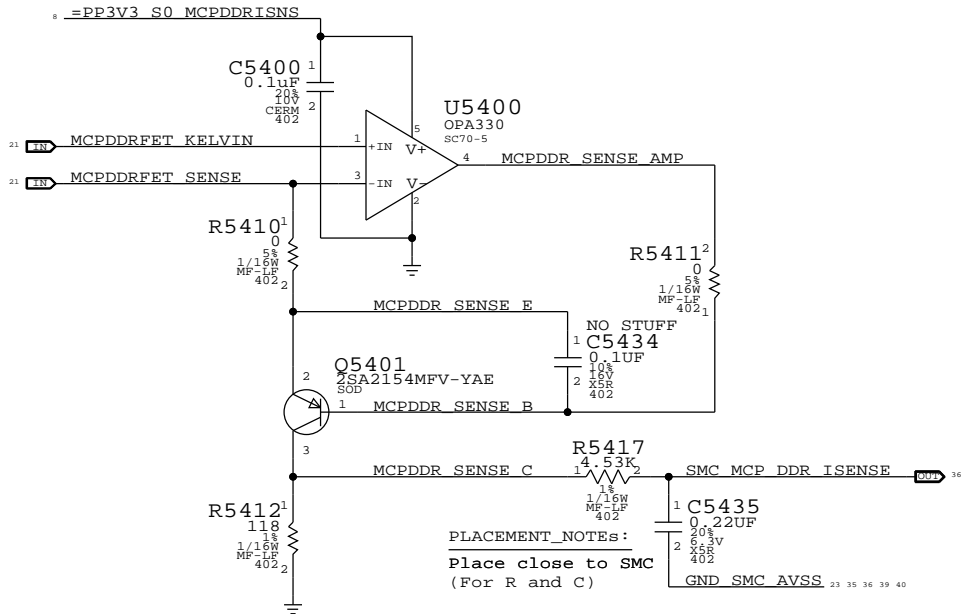
D

C

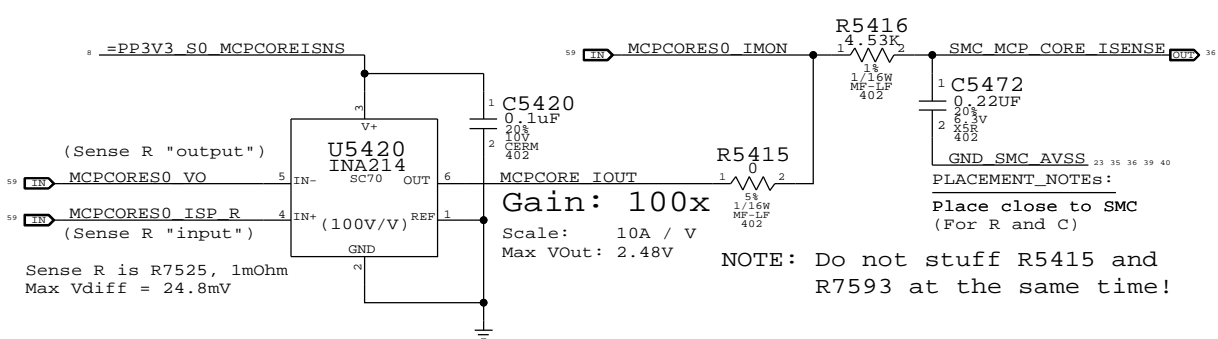
B

A

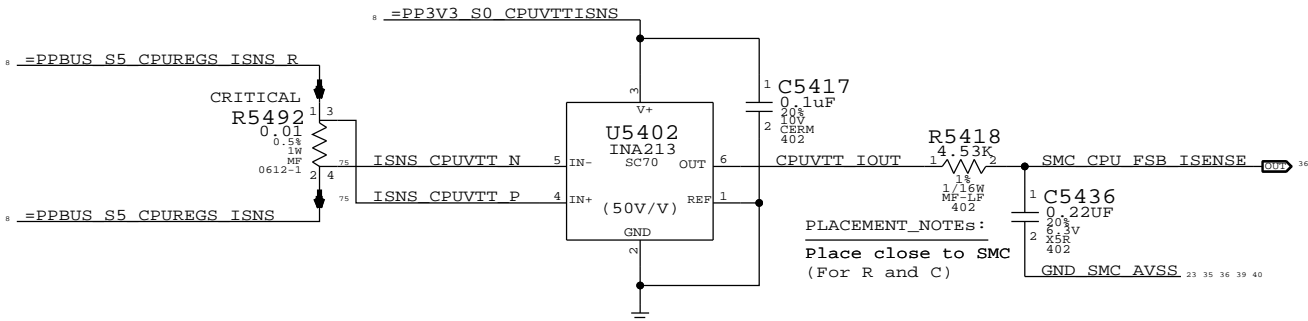
MCP MEM VDD Current Sense / Filter



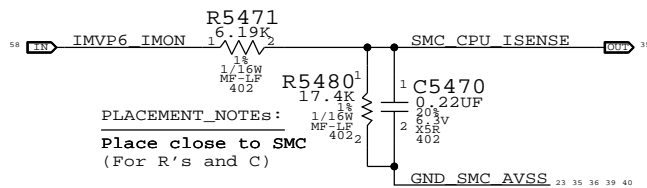
MCP VCore Current Sense Filter



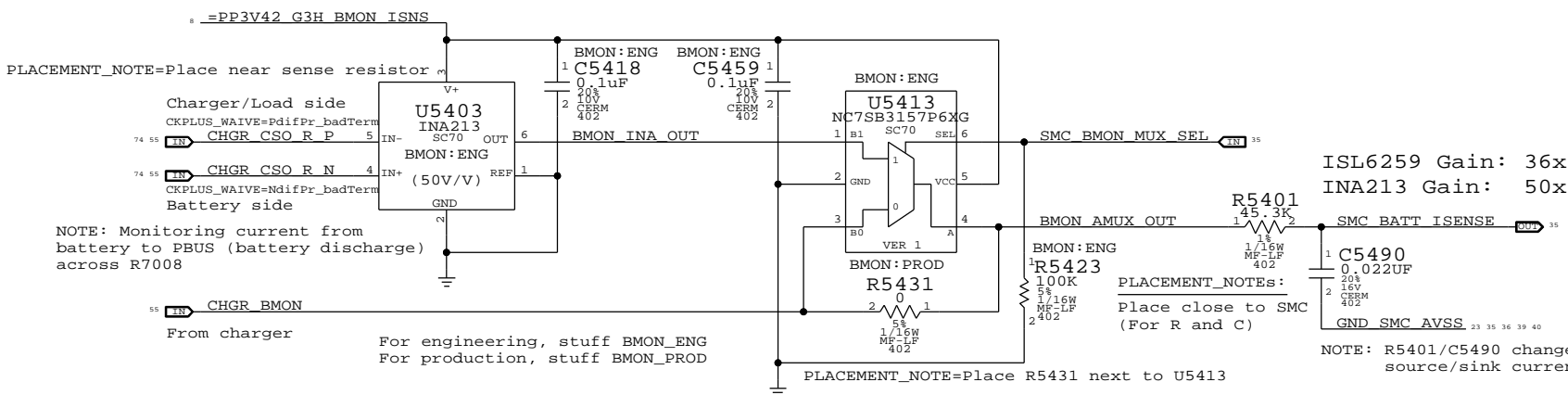
MCP/CPU 1.05V AND CPU VCore High-Side Current Sense / Filter



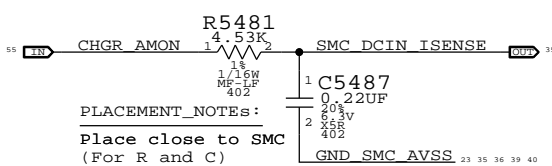
CPU VCore Load Side Current Sense / Filter



Battery (BMON) Current Sense, MUX & Filter



DC-IN (AMON) Current Sense Filter



SYNC MASTER=T27 MLB		SYNC DATE=02/02/2010	
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## D



## B



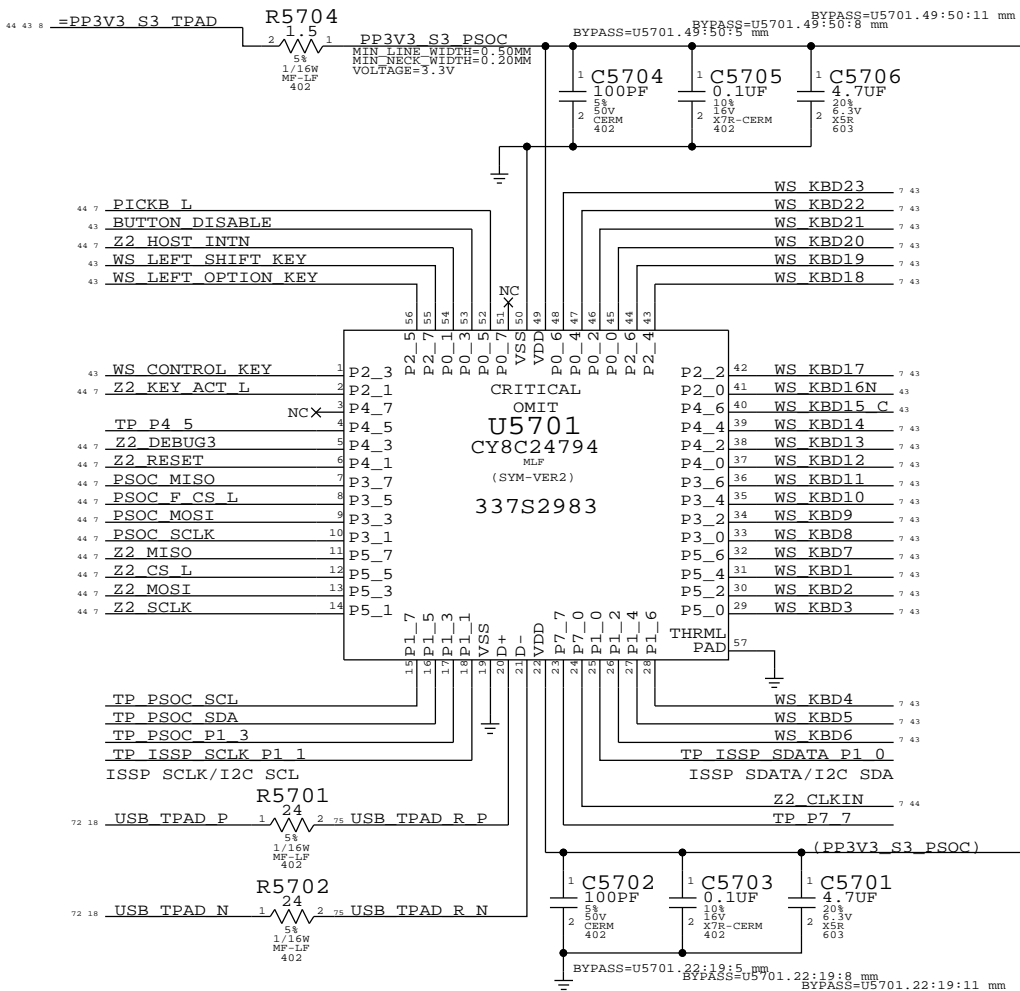
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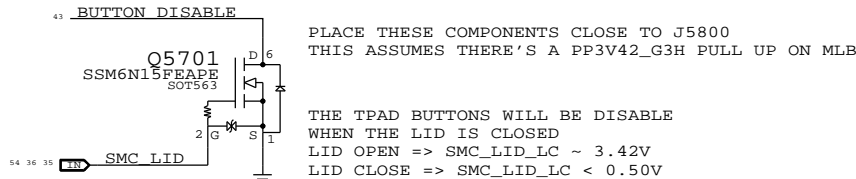
1

## PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER

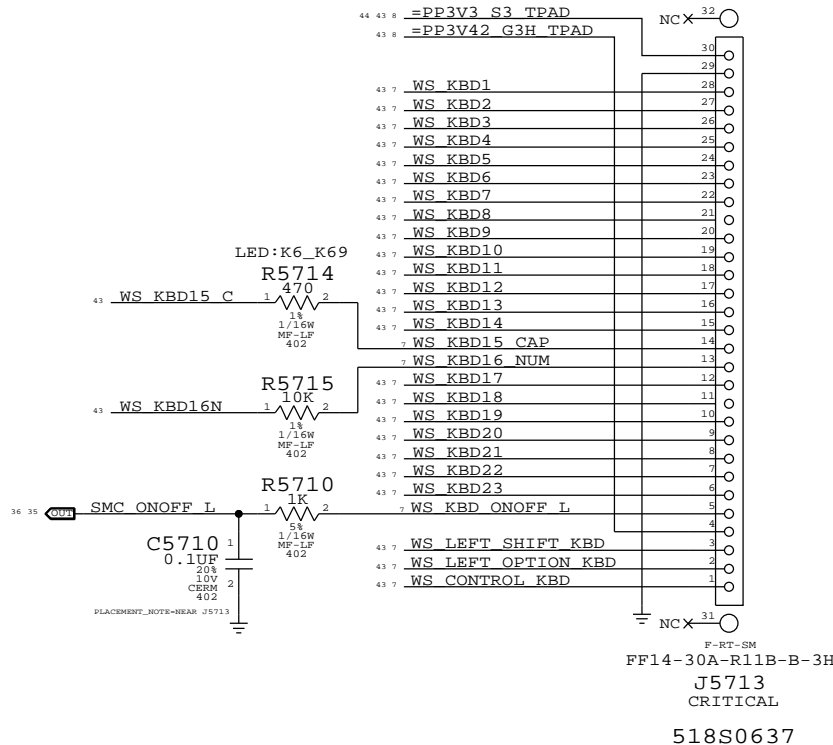


## TPAD Buttons Disable



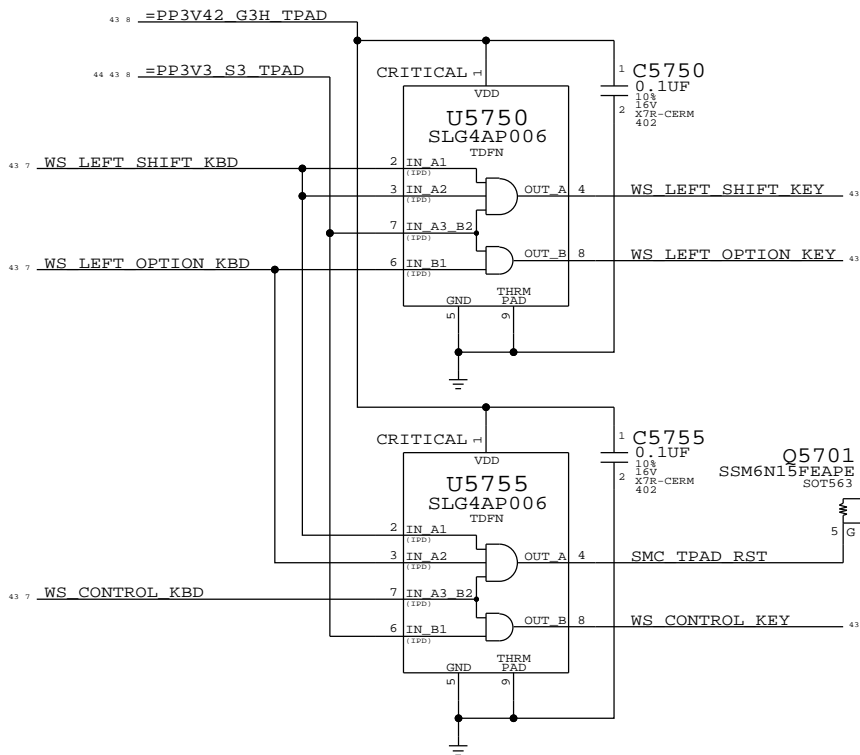
IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

## Keyboard Connector



## SMC Manual Reset & Isolation

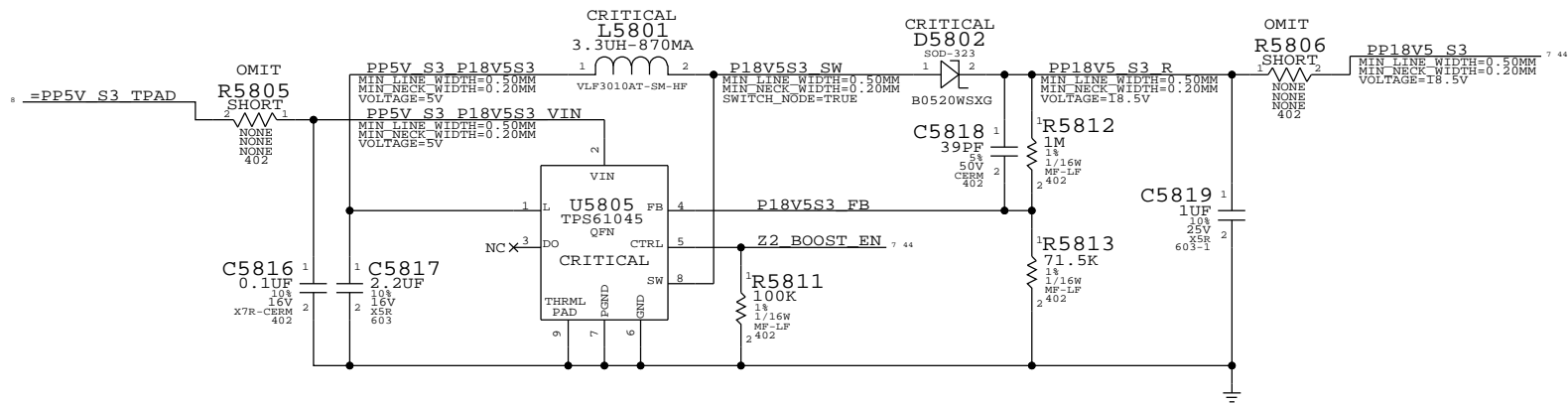
Left shift, option & control keys combined with power button cause SMC RESET# assertion. Keys ANDed with PSOC power to isolate when PSOC is not powered.



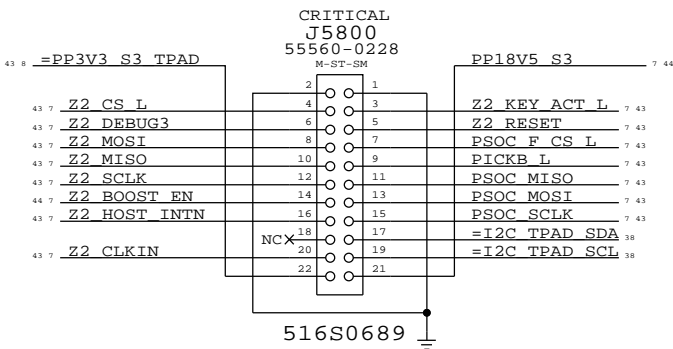


BOOSTER +18.5VDC FOR SENSORS

BOOSTER DESIGN CONSIDERATION:  
- POWER CONSUMPTION  
- DROOP LINE REGULATION  
- RIPPLE TO MEET ERS  
- 100-300 KHZ CLEAN SPECTRUM  
- STARTUP TIME LESS THAN 2MS  
- R5812,R5813,C5818 MODIFIED

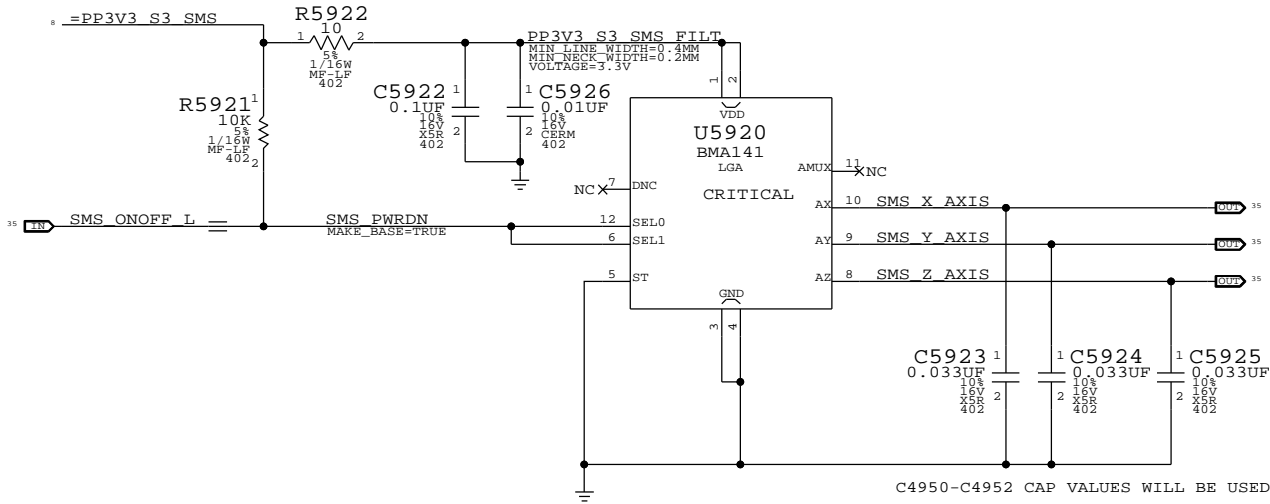


IPD Flex Connector

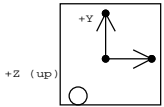


R5921 PULLS UP SEL PINS TO ENTER STANDBY MODE WHEN PIN IS NOT BEING DRIVEN BY SMC

Analog SMS



Desired orientation when placed on board top-side:



Front of system


Circle indicates pin 1 location when placed in correct orientation


C4950-C4952 CAP VALUES WILL BE USED TO GET CUT-OFF FREQUENCY OF ~146HZ

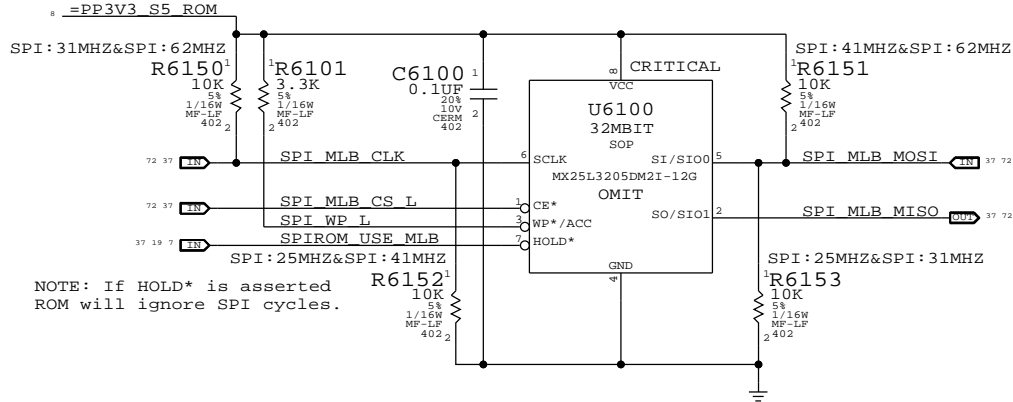
PLACE\_NEARs:

C5923.1:PLACE\_NEAR=U4900.M10:2.54MM  
C5924.1:PLACE\_NEAR=U4900.N9:2.54MM  
C5925.1:PLACE\_NEAR=U4900.R10:2.54MM

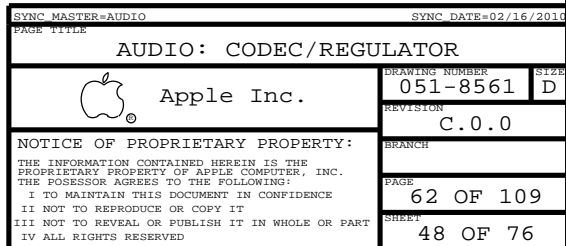
DO NOT SYNC WITH K84. REMOVED NO STUFF ON C5923,C5924,C5925. ADDED PLACE NEARS

SYNC_MASTER=MASTER		SYNC_DATE=MASTER	
PAGE TITLE			
SMS			
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		PAGE	59 OF 109
		SHEET	45 OF 76

SYNC MASTER=MASTER		SYNC DATE=MASTER	
PAGE TITLE		PAGE NO.	
DEBUG SENSORS AND ADC			
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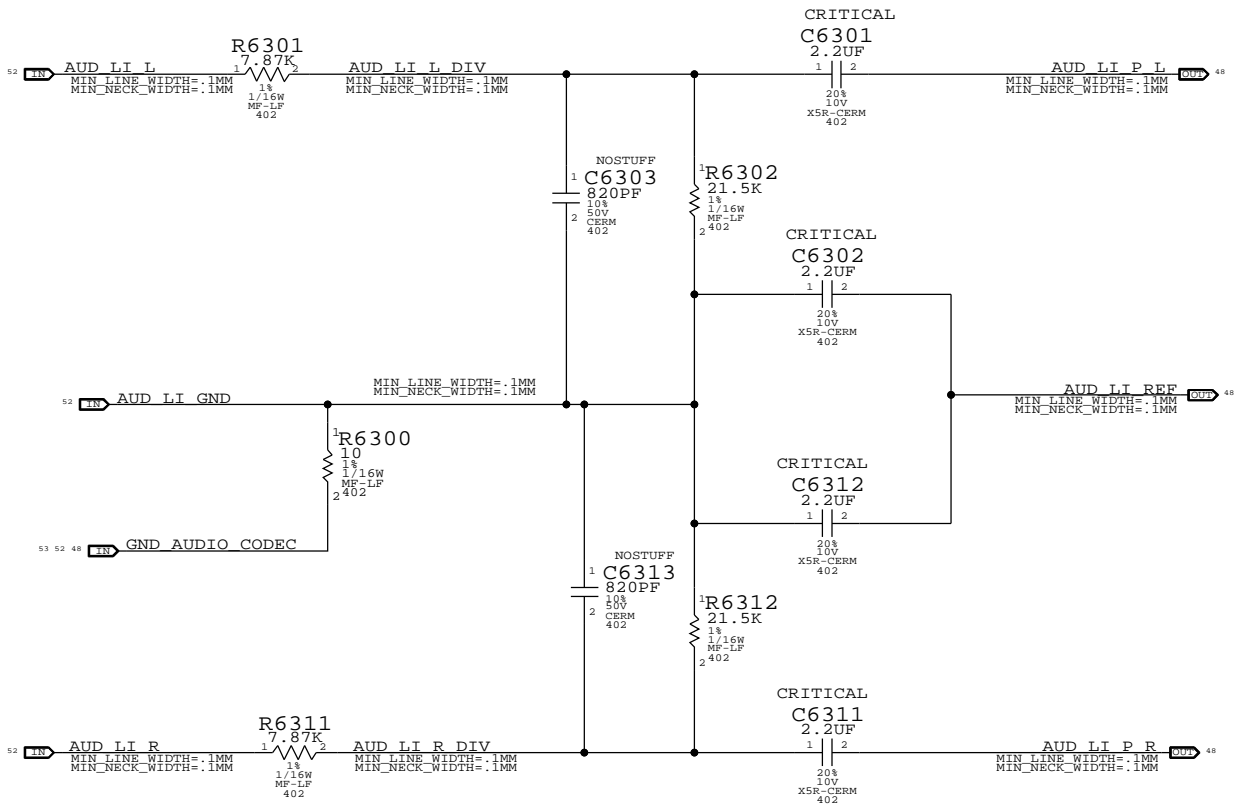
MCP89 SPI Frequency Select		
Frequency	SPI_MOSI	SPI_CLK
25.0 MHz	0	0
31.2 MHz	0	1
41.7 MHz	1	0
62.5 MHz	1	1
NOTE: 42 & 62 MHz use FAST_READ command.		



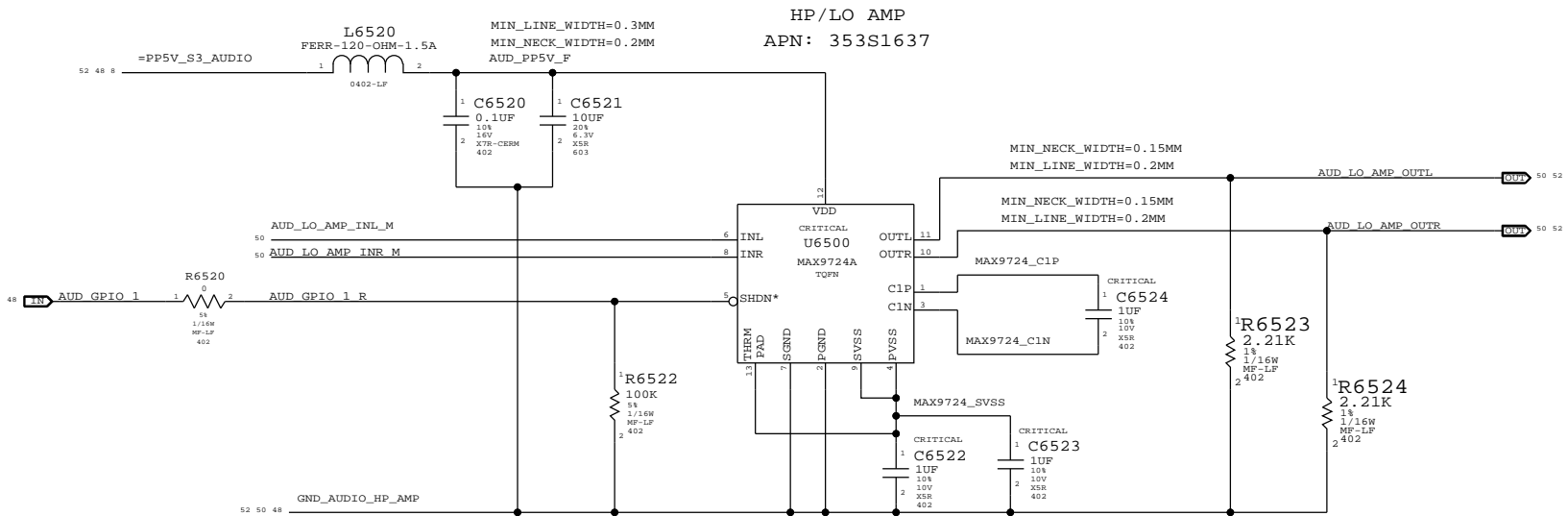
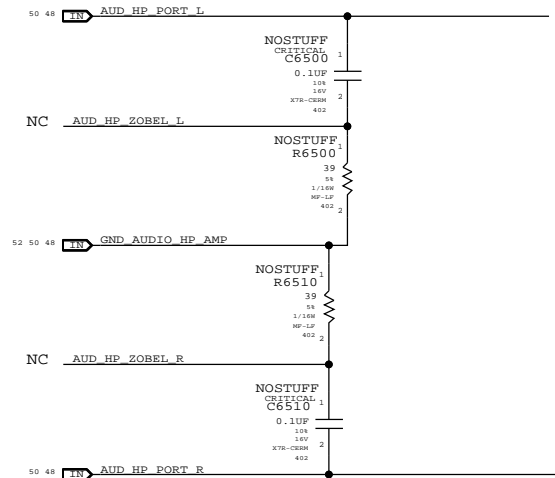


LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS  
NET RIN = 10.36K OHMS (INCLUDING PULL-DOWNS AT ANALOG SWITCH COM PINS)  
FC\_HP = 3.6 HZ  
FC\_LP = 43KHZ  
VIN = 2VRMS, CODEC VIN = 1.14 VRMS

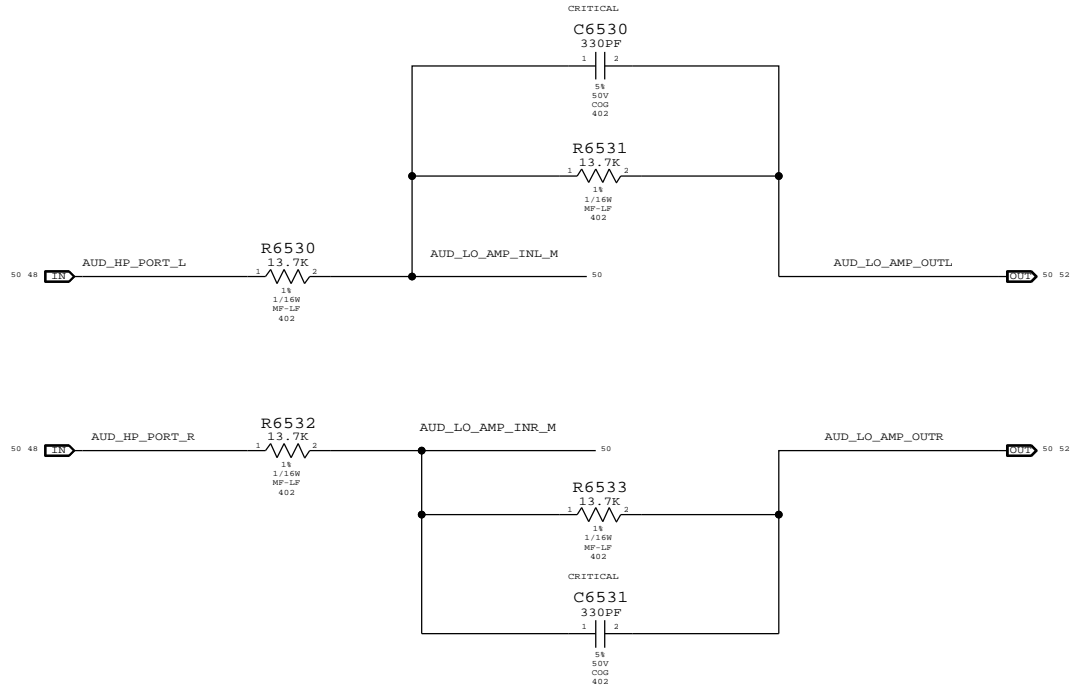



CS4206 HP OUTPUT ZOBEL NETWORK



MAX9724 GAIN/FILTER COMPONENTS

AV\_PB = -1V/V, FC\_LPF = 35.2KHZ



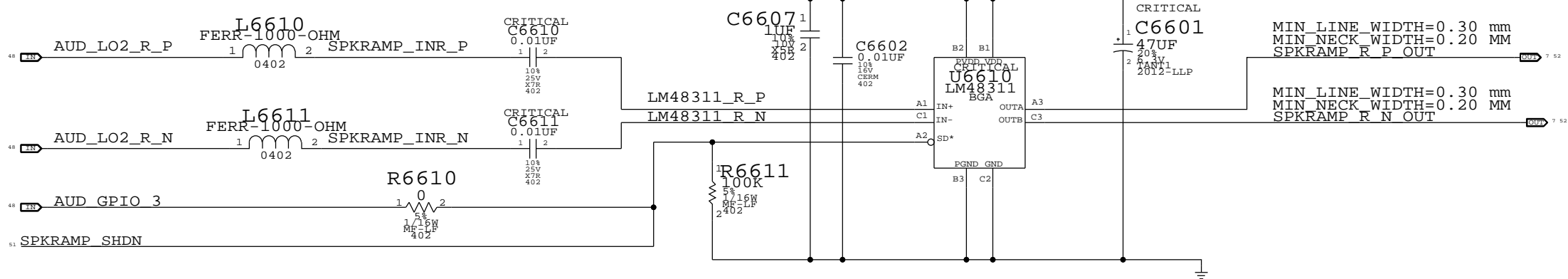
SYNC MASTER=AUDIO		SYNC DATE=02/16/2010	
PAGE TITLE			
AUDIO: HEADPHONE FILTER		DRAWING NUMBER	
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		C.0.0	
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SATELLITE 796Hz < HPF FC < 936Hz  
SUB 80 Hz < HPF FC < 94 Hz  
GAIN 6DB (2V/V)  
SPRK AMP. INPUT REFERRED CLIP POINT = ~-6dBFS

ALIAS OF PP5V\_S3\_REG, MIN\_LINE\_WIDTH=0.60MM, MIN\_NECK\_WIDTH=0.20MM

51 8 =PP5V\_S3\_AUDIO\_AMP

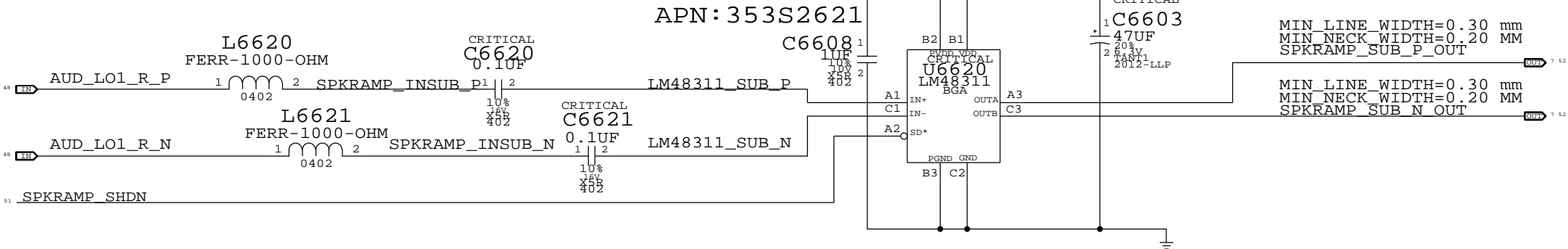
APN: 353S2621



ALIAS OF PP5V\_S3\_REG, MIN\_LINE\_WIDTH=0.60MM, MIN\_NECK\_WIDTH=0.20MM

51 8 =PP5V\_S3\_AUDIO\_AMP

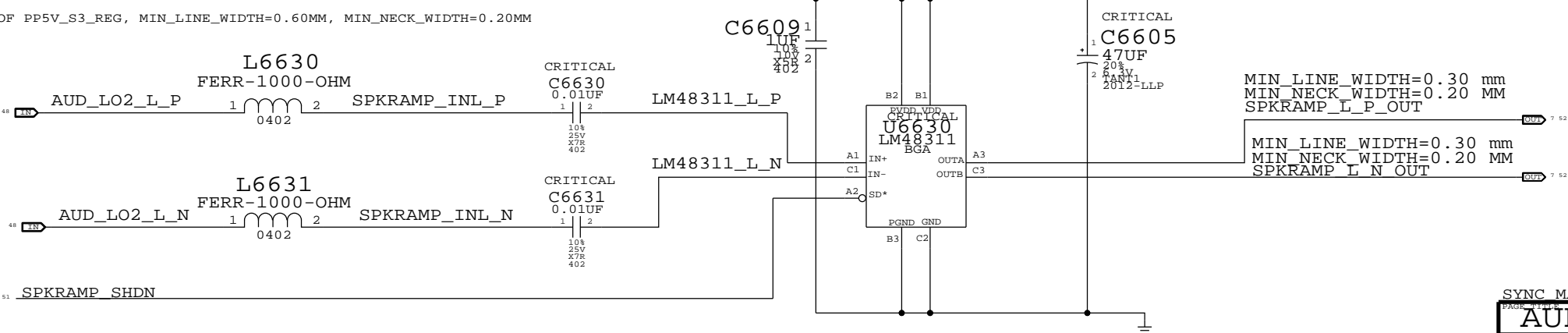
APN: 353S2621




APN: 353S2621

51 8 =PP5V\_S3\_AUDIO\_AMP

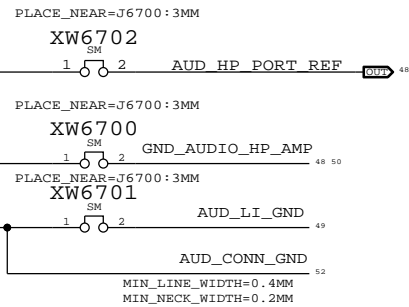
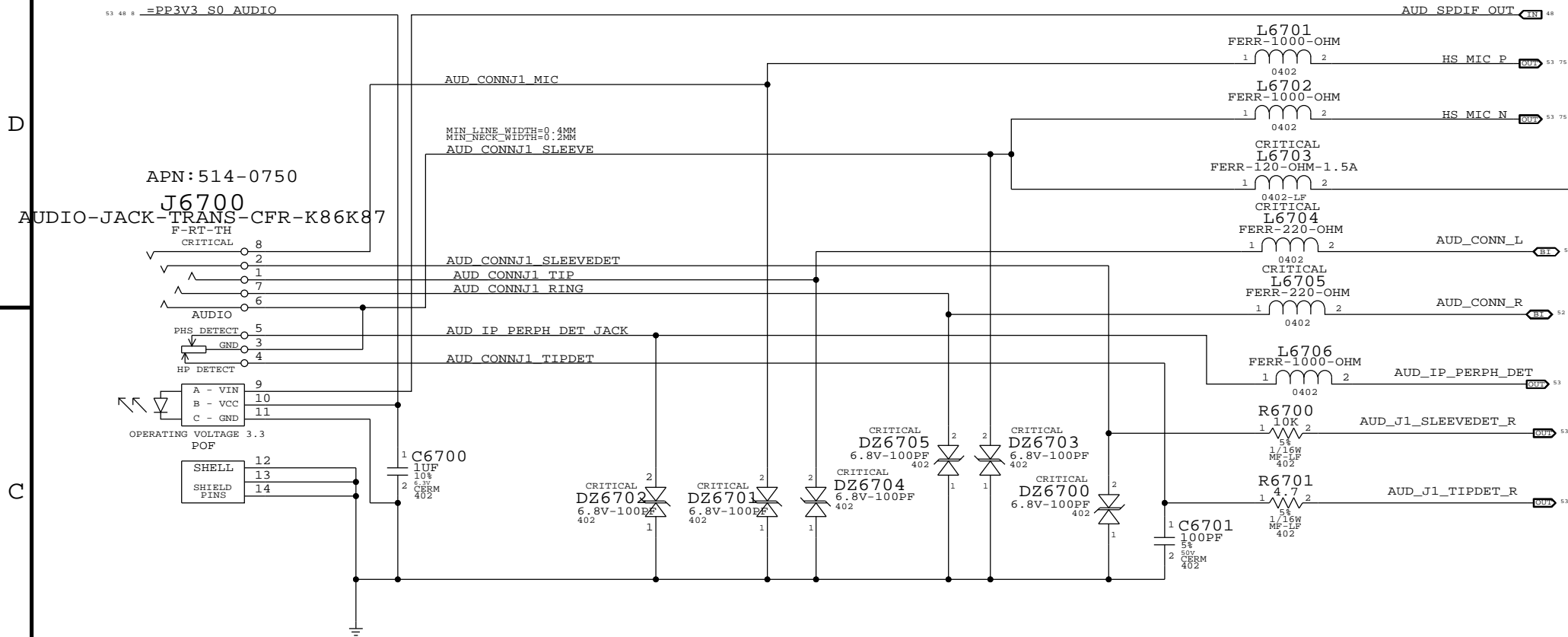
ALIAS OF PP5V\_S3\_REG, MIN\_LINE\_WIDTH=0.60MM, MIN\_NECK\_WIDTH=0.20MM



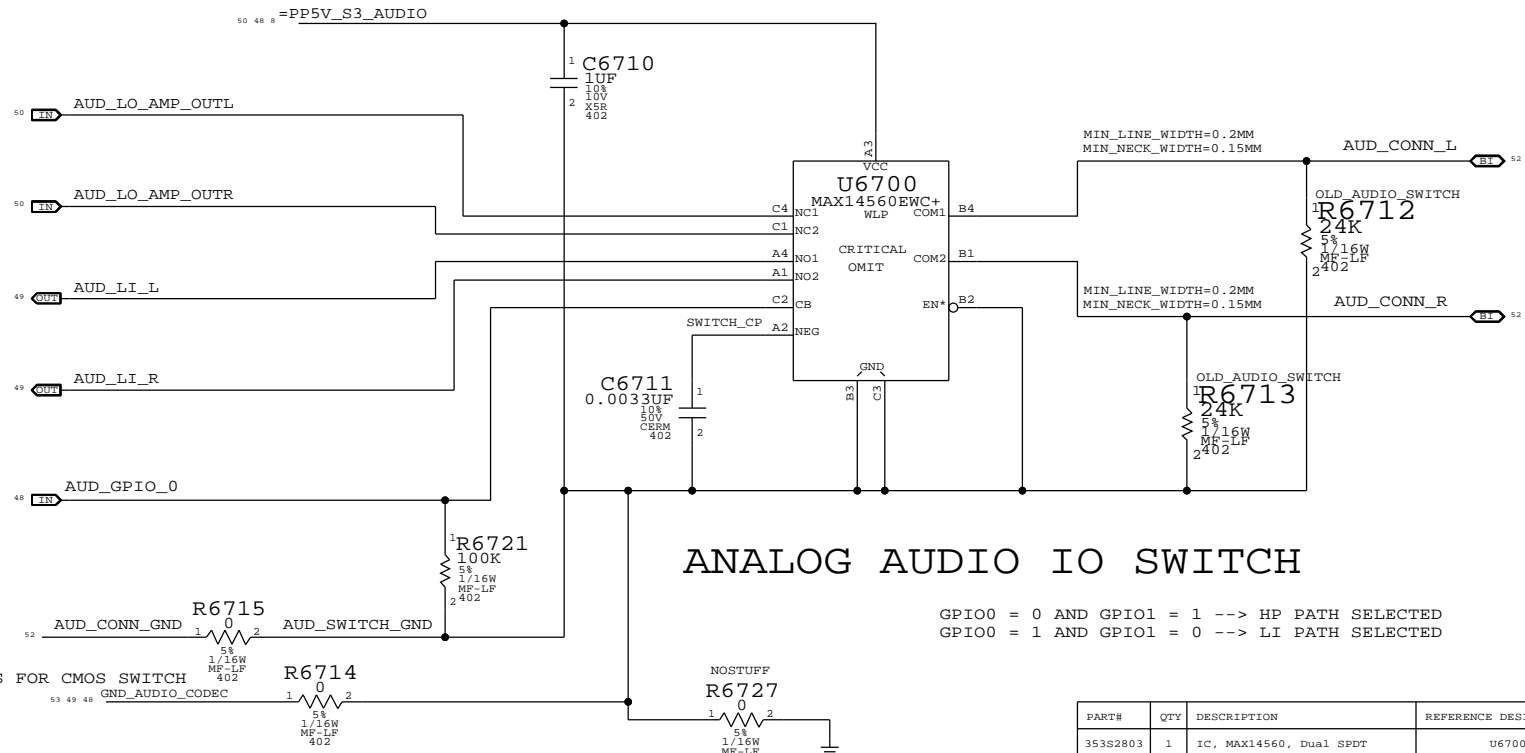
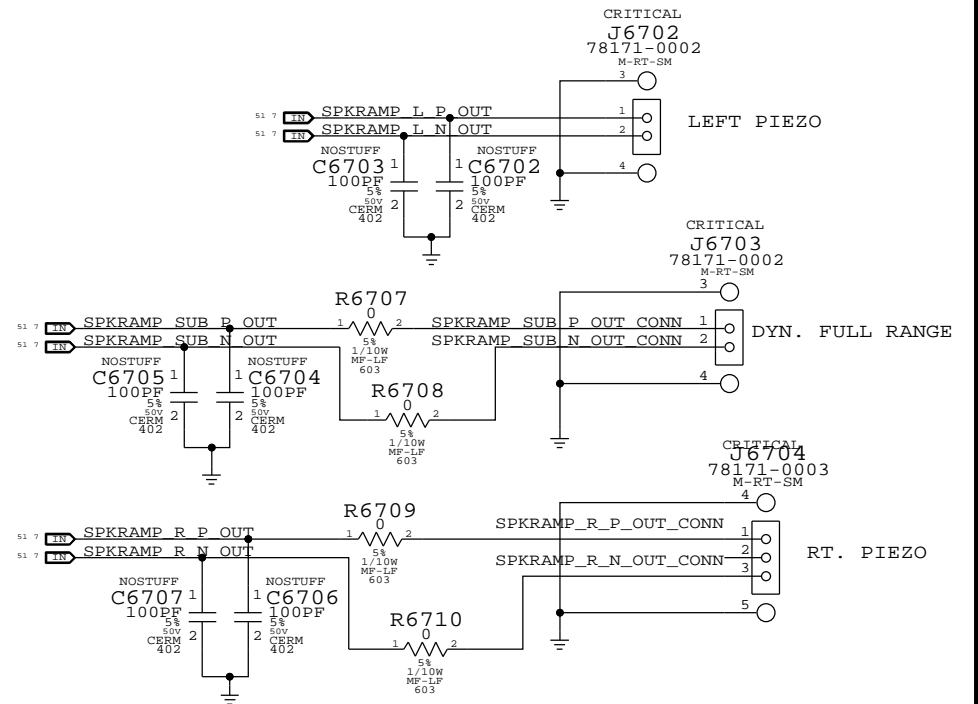
SYNC MASTER=AUDIO SYNC DATE=02/16/2010

AUDIO0: SPEAKER AMP		
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AUDIO JACK: LI/LO/HP CONNECTOR, SPDIF TX



SPEAKER CONNECTORS  
APN:518S0519



GPIO0 = 0 AND GPIO1 = 1 --> HP PATH SELECTED  
GPIO0 = 1 AND GPIO1 = 0 --> LI PATH SELECTED

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BCM OPTION
353S2803	1	IC, MAX14560, Dual SPDT	U6700	CRITICAL	NEW_AUDIO_SWITCH
353S2536	1	IC, MAX14504, Dual SPDT	U6700	CRITICAL	OLD_AUDIO_SWITCH

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AUDIO: JACK		DRAWING NUMBER	051-8561
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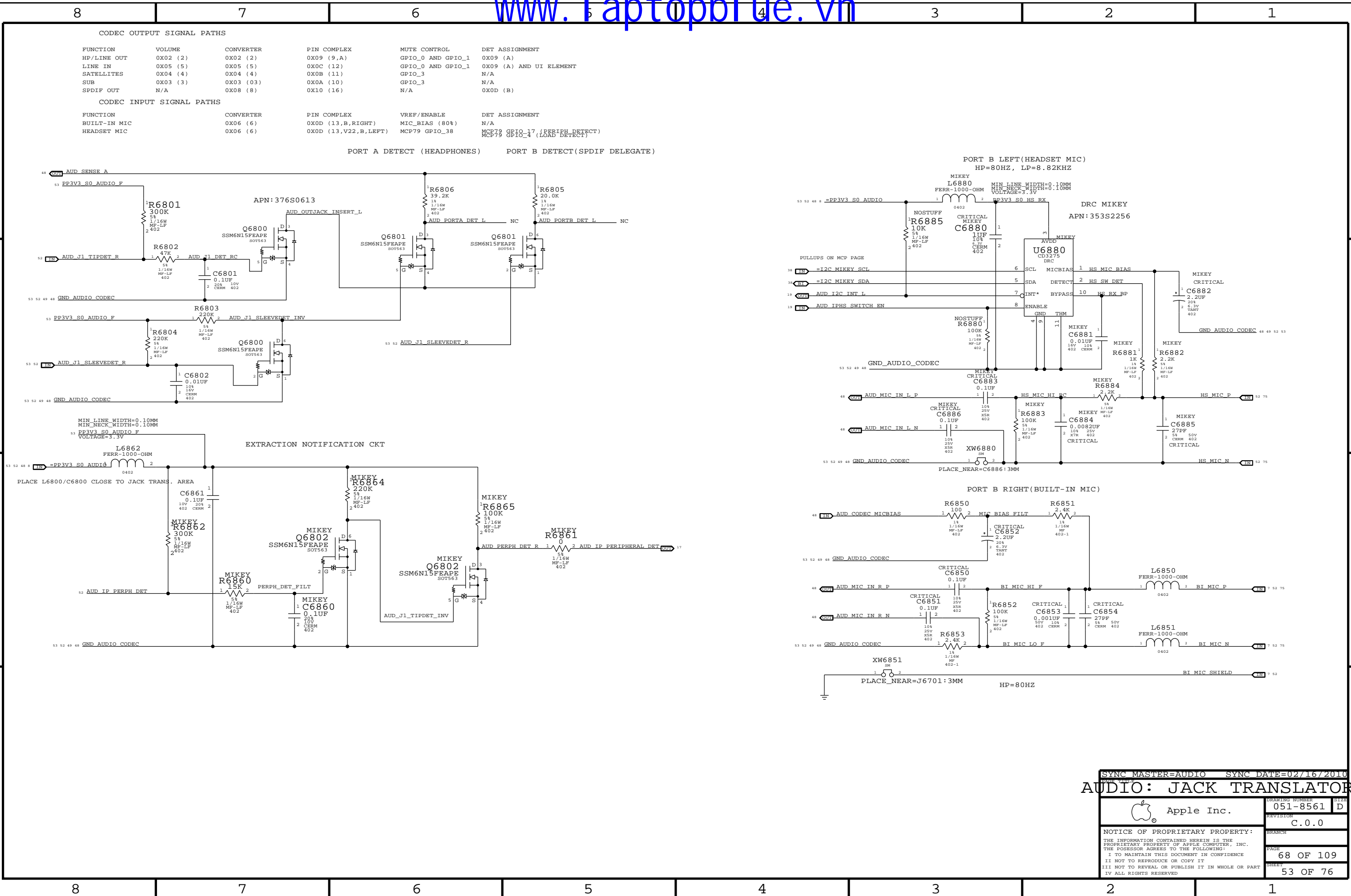
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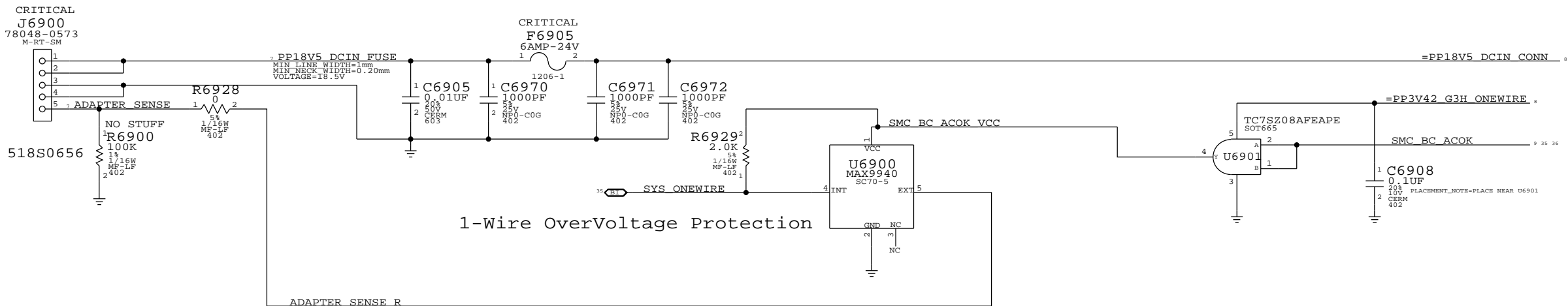
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53 OF 76

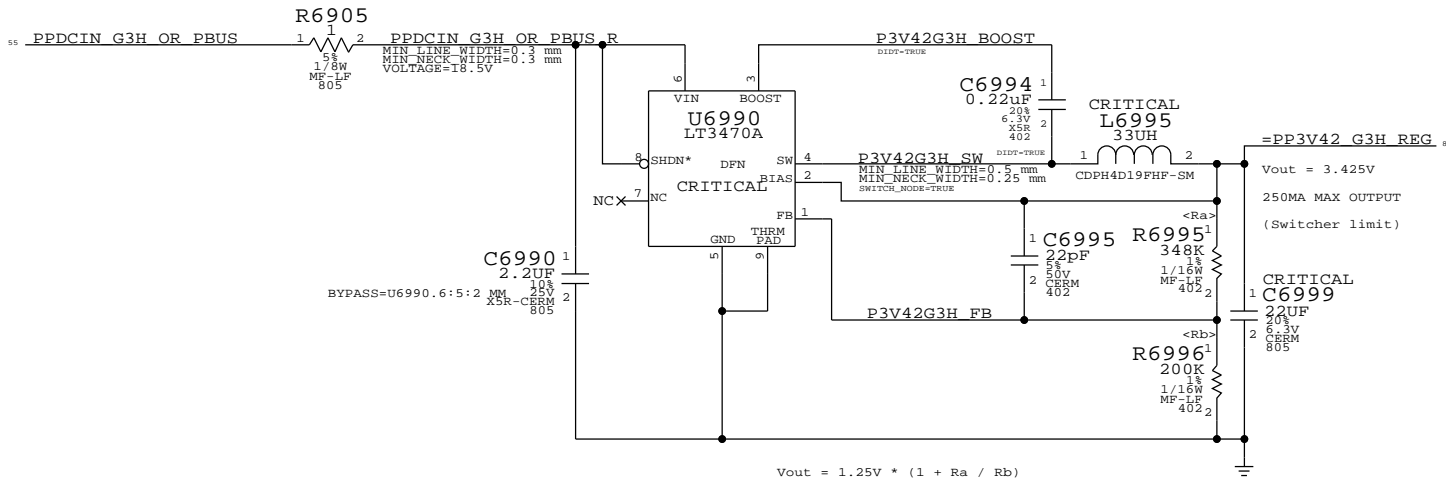


MagSafe DC Power Jack



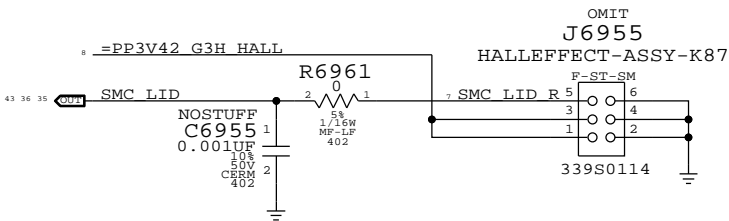
3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



HALL EFFECT ASSEMBLY

- Assembly APN: 339S0114  
- BOM: 639-0680  
- PCBF: 820-2801  
- MCO: 056-3515  
- Conn APN: 518S0788

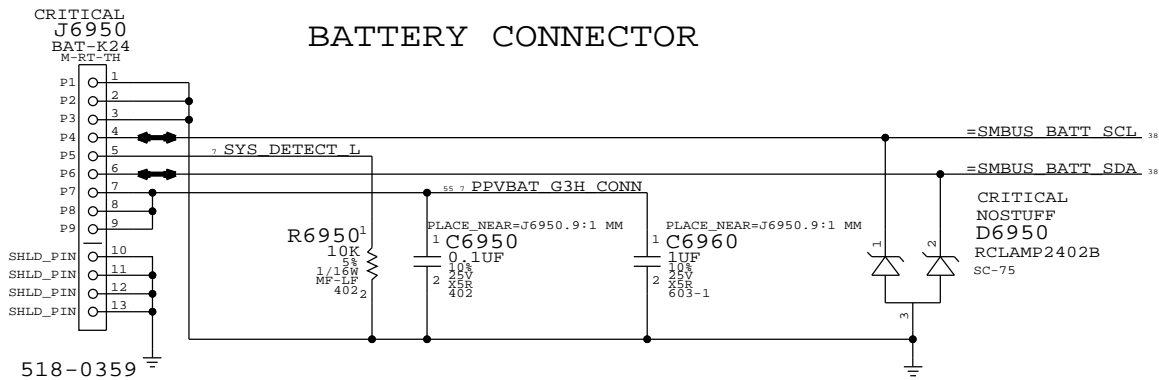


PROTO 0: STUFFING K84 CONNECTOR ONTO MODIFIED K84 PADS  
PROTO 1: STUFFING K87 HALL EFFECT ASSEMBLY ONTO K87 PADS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
607-6831	1	SUB ASSY - HALL EFFECT, K86 K87	J6955	CRITICAL	

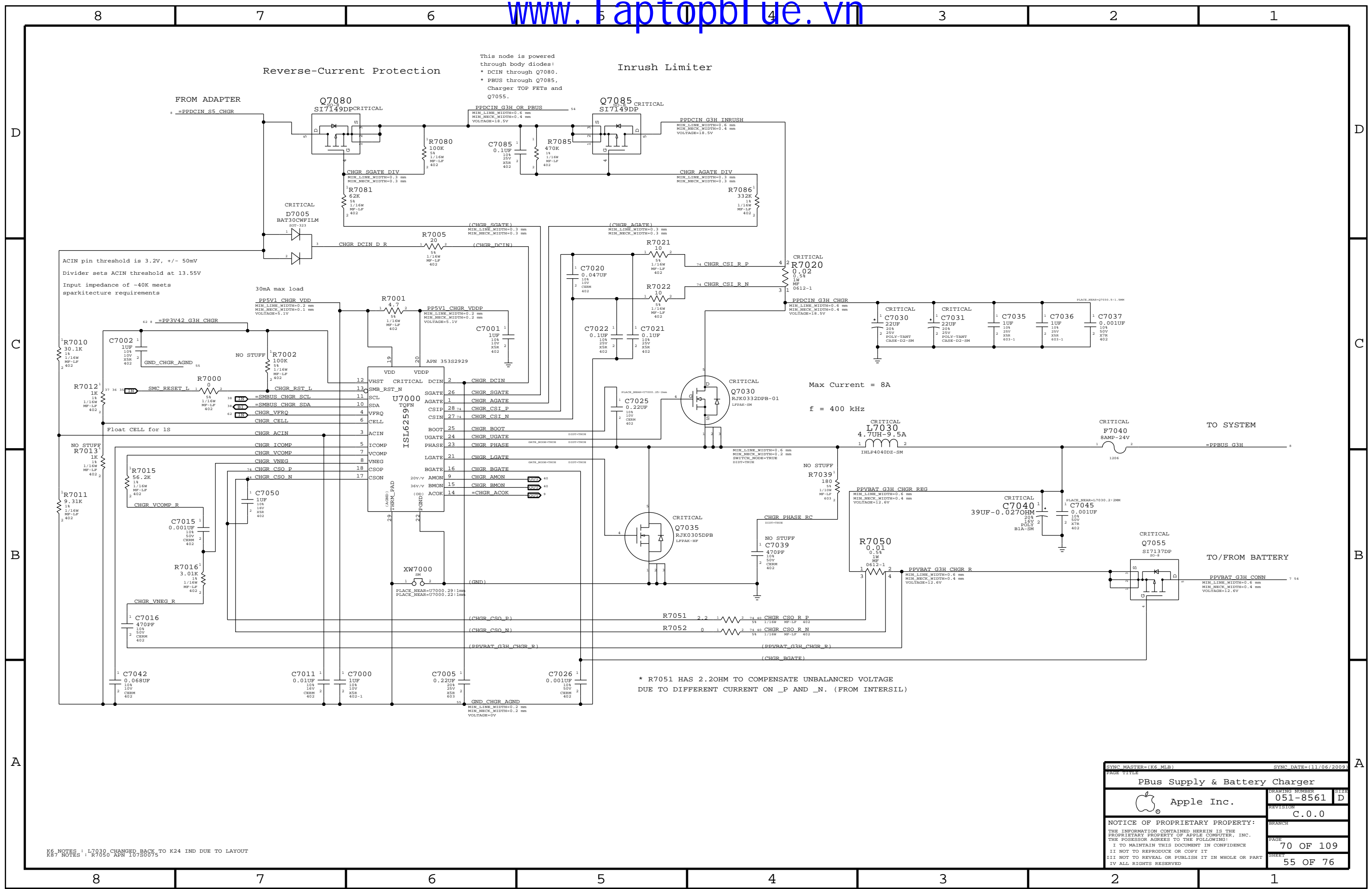
PN: 607-6831 for WCPM. PN: 339S0114 for schematic/board layout

BATTERY CONNECTOR



DO NOT SYNC WITH K84. R6900,C6960,SIGNAL NAMES CHANGED. HALL EFFECT CONNECTOR CHANGED.

PAGE TITLE		SYNC DATE=MASTER	
DC-In & Battery Connectors		DRAWING NUMBER	
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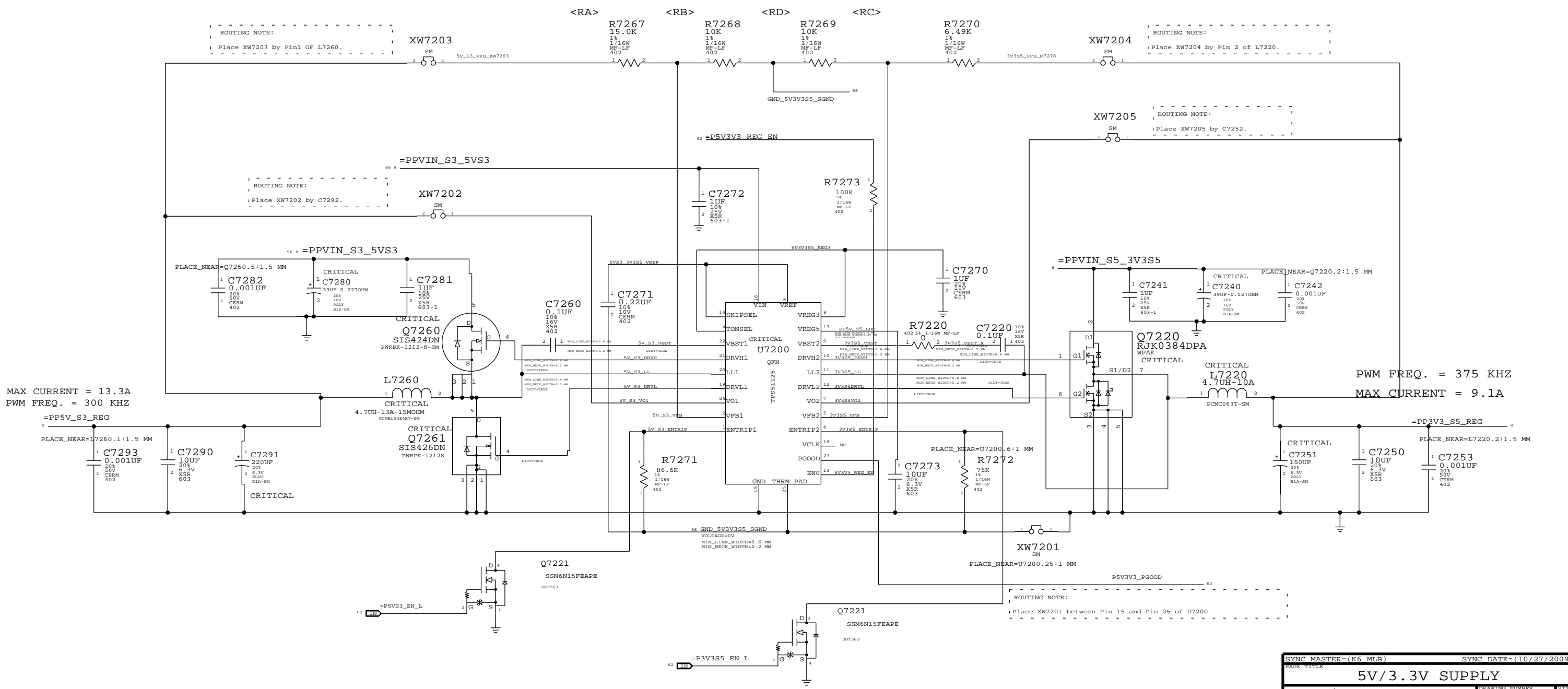
\* R7051 HAS 2.20HM TO COMPENSATE UNBALANCED VOLTAGE  
DUE TO DIFFERENT CURRENT ON \_P AND \_N. (FROM INTERSIL)

K6 NOTES : L7030 CHANGED BACK TO K24 IND DUE TO LAYOUT  
K87 NOTES : R7050 APN 10750075

PAGE TITLE		DRAWING NUMBER		REVISION	
PBus Supply & Battery Charger		051-8561		C.0.0	
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# 5V\_S3 / 3.3V\_S5 POWER SUPPLY

$$V_{OUT} = (2 * R_A / R_B) + 2$$
$$V_{OUT} = (2 * R_C / R_D) + 2$$



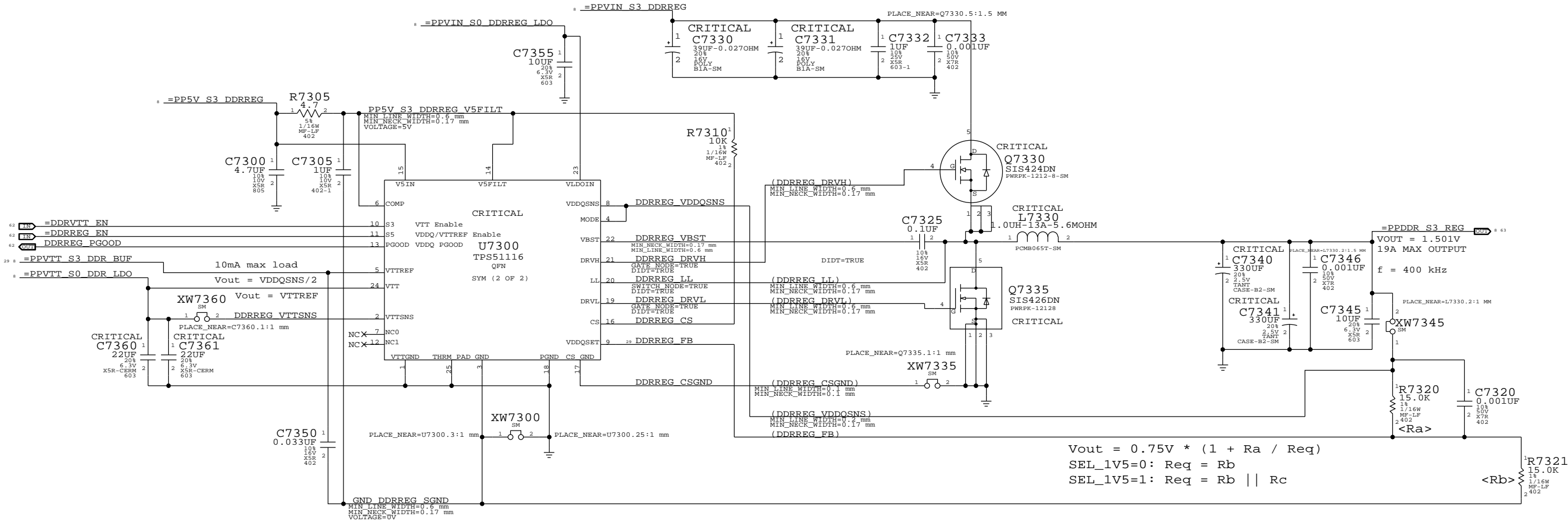
MAX CURRENT = 13.3A  
PWM FREQ. = 300 KHZ

PWM FREQ. = 375 KHZ  
MAX CURRENT = 9.1A

NOTE: DONT SYNC THIS PAGE FROM T27


PAGE TITLE		PAGE NUMBER	
5V/3.3V SUPPLY		051-8561	
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1.5V/0.75 DDR3 POWER SUPPLY

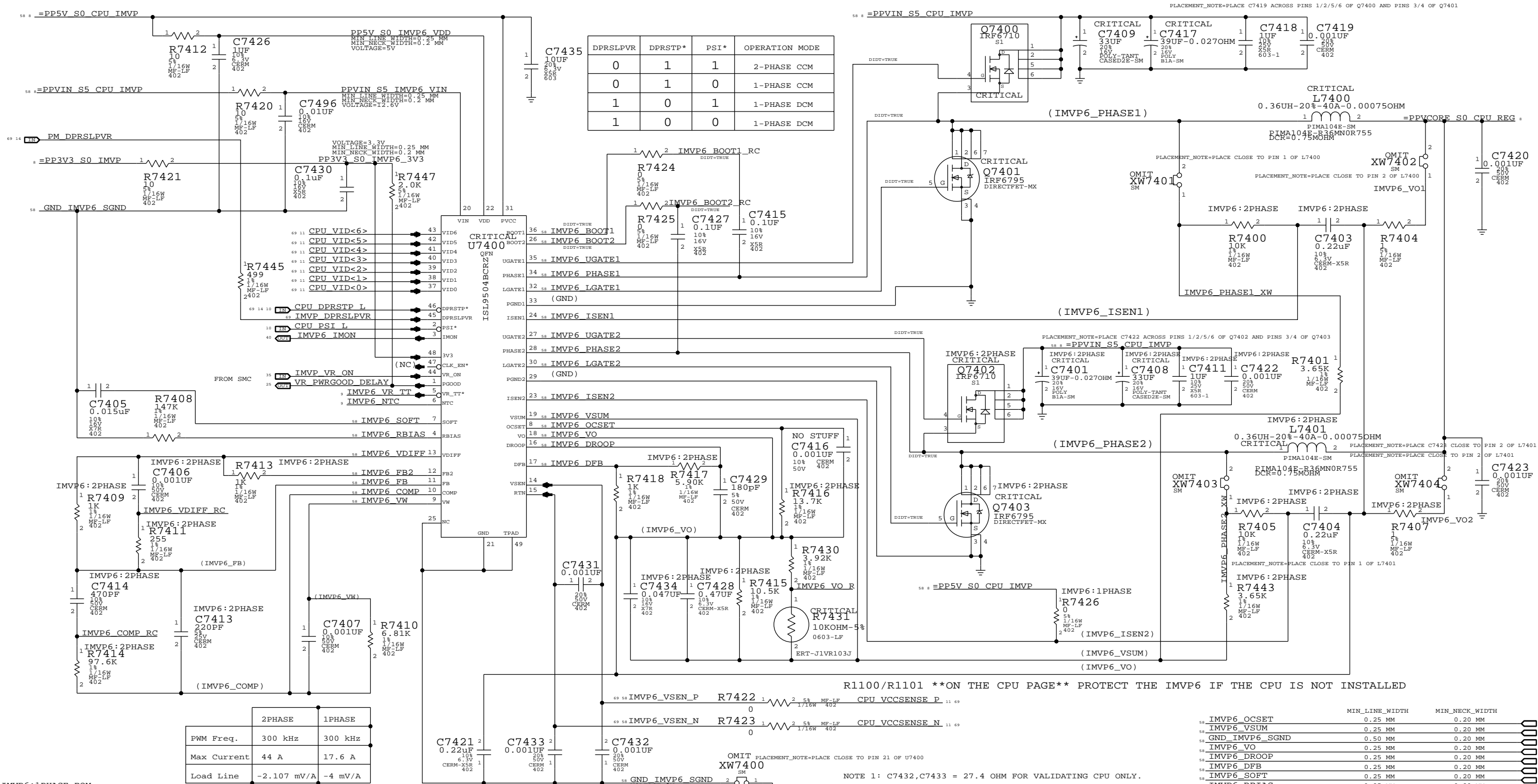


$$V_{out} = 0.75V * (1 + R_a / R_{eq})$$
$$SEL\_1V5=0: R_{eq} = R_b$$
$$SEL\_1V5=1: R_{eq} = R_b || R_c$$

NOTE: DONT SYNC THIS PAGE FROM T27. C7330 AND C7331 IS CHANGED TO OSCON CAPS  
NOTE: DONT SYNC THIS PAGE FROM K6 REMOVED R7380

SYNC MASTER=(K6 MLB)		SYNC DATE=(11/06/2009)	
PAGE TITLE			
1.5V/0.75V DDR3 SUPPLY			
 Apple Inc.		DRAWING NUMBER	8142
		051-8561	D
		REVISION	
		C.0.0	
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# IMVP6 CPU VCORE REGULATOR



IMVP6:1PHASE BOM					
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0307	1	RES,MTL,FILM,1/16W,8.25K,1,0402,SMD,LF	R7417		IMVP6:1PHASE
114S0336	1	RES,MTL,FILM,1/16W,16.9K,1,0402,SMD,LF	R7416		IMVP6:1PHASE
132S0080	1	CAP,CER,220P,20,6.3V,XSR,0402	C7428		IMVP6:1PHASE
114S0236	1	RES,MTL,FILM,1/16W,1.58K,1,0402,SMD,LF	R7409		IMVP6:1PHASE
114S0160	1	RES,MTL,FILM,1/16W,255 OHM,1,0402,SMD,LF	R7411		IMVP6:1PHASE
132S4720	1	CAP,CER,470PF,+-10%,50V,0402,SMD	C7406		IMVP6:1PHASE
114S0410	1	RES,MTL,FILM,1/16W,97.6K,1,0402,SMD,LF	R7414		IMVP6:1PHASE
132S0045	1	CAP,CER,1000PF,50V,10%,X7R,0402,SMD	C7414		IMVP6:1PHASE
131S1027	1	CAP,CER,1000PF,50V,CC0402	C7413		IMVP6:1PHASE

IMVP6:2PHASE BOM					
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0307	1	RES,MTL,FILM,1/16W,8.25K,1,0402,SMD,LF	R7417		IMVP6:1PHASE
114S0336	1	RES,MTL,FILM,1/16W,16.9K,1,0402,SMD,LF	R7416		IMVP6:1PHASE
132S0080	1	CAP,CER,220P,20,6.3V,XSR,0402	C7428		IMVP6:1PHASE
114S0236	1	RES,MTL,FILM,1/16W,1.58K,1,0402,SMD,LF	R7409		IMVP6:1PHASE
114S0160	1	RES,MTL,FILM,1/16W,255 OHM,1,0402,SMD,LF	R7411		IMVP6:1PHASE
132S4720	1	CAP,CER,470PF,+-10%,50V,0402,SMD	C7406		IMVP6:1PHASE
114S0410	1	RES,MTL,FILM,1/16W,97.6K,1,0402,SMD,LF	R7414		IMVP6:1PHASE
132S0045	1	CAP,CER,1000PF,50V,10%,X7R,0402,SMD	C7414		IMVP6:1PHASE
131S1027	1	CAP,CER,1000PF,50V,CC0402	C7413		IMVP6:1PHASE

IMVP6:3PHASE BOM					
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0307	1	RES,MTL,FILM,1/16W,8.25K,1,0402,SMD,LF	R7417		IMVP6:1PHASE
114S0336	1	RES,MTL,FILM,1/16W,16.9K,1,0402,SMD,LF	R7416		IMVP6:1PHASE
132S0080	1	CAP,CER,220P,20,6.3V,XSR,0402	C7428		IMVP6:1PHASE
114S0236	1	RES,MTL,FILM,1/16W,1.58K,1,0402,SMD,LF	R7409		IMVP6:1PHASE
114S0160	1	RES,MTL,FILM,1/16W,255 OHM,1,0402,SMD,LF	R7411		IMVP6:1PHASE
132S4720	1	CAP,CER,470PF,+-10%,50V,0402,SMD	C7406		IMVP6:1PHASE
114S0410	1	RES,MTL,FILM,1/16W,97.6K,1,0402,SMD,LF	R7414		IMVP6:1PHASE
132S0045	1	CAP,CER,1000PF,50V,10%,X7R,0402,SMD	C7414		IMVP6:1PHASE
131S1027	1	CAP,CER,1000PF,50V,CC0402	C7413		IMVP6:1PHASE

IMVP6:4PHASE BOM					
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0307	1	RES,MTL,FILM,1/16W,8.25K,1,0402,SMD,LF	R7417		IMVP6:1PHASE
114S0336	1	RES,MTL,FILM,1/16W,16.9K,1,0402,SMD,LF	R7416		IMVP6:1PHASE
132S0080	1	CAP,CER,220P,20,6.3V,XSR,0402	C7428		IMVP6:1PHASE
114S0236	1	RES,MTL,FILM,1/16W,1.58K,1,0402,SMD,LF	R7409		IMVP6:1PHASE
114S0160	1	RES,MTL,FILM,1/16W,255 OHM,1,0402,SMD,LF	R7411		IMVP6:1PHASE
132S4720	1	CAP,CER,470PF,+-10%,50V,0402,SMD	C7406		IMVP6:1PHASE
114S0410	1	RES,MTL,FILM,1/16W,97.6K,1,0402,SMD,LF	R7414		IMVP6:1PHASE
132S0045	1	CAP,CER,1000PF,50V,10%,X7R,0402,SMD	C7414		IMVP6:1PHASE
131S1027	1	CAP,CER,1000PF,50V,CC0402	C7413		IMVP6:1PHASE

SYNC MASTER=(K84 MLB)SYNC DATE=(11/18/2009)

IMVP6 CPU VCore Regulator

Apple Inc.

051-8561

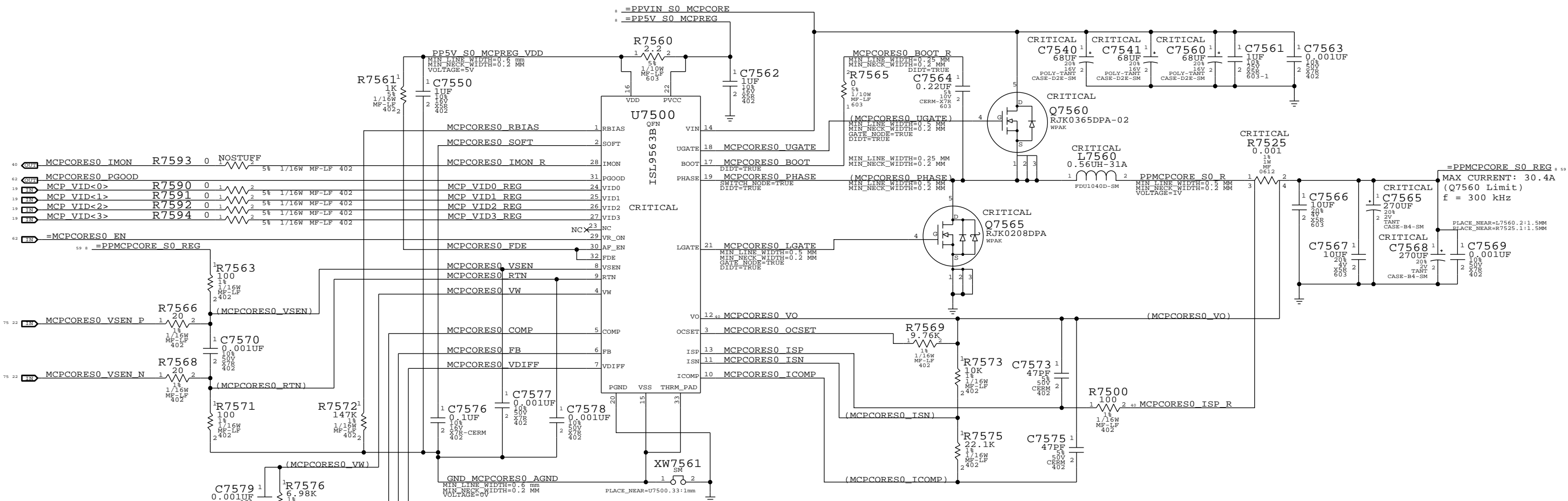
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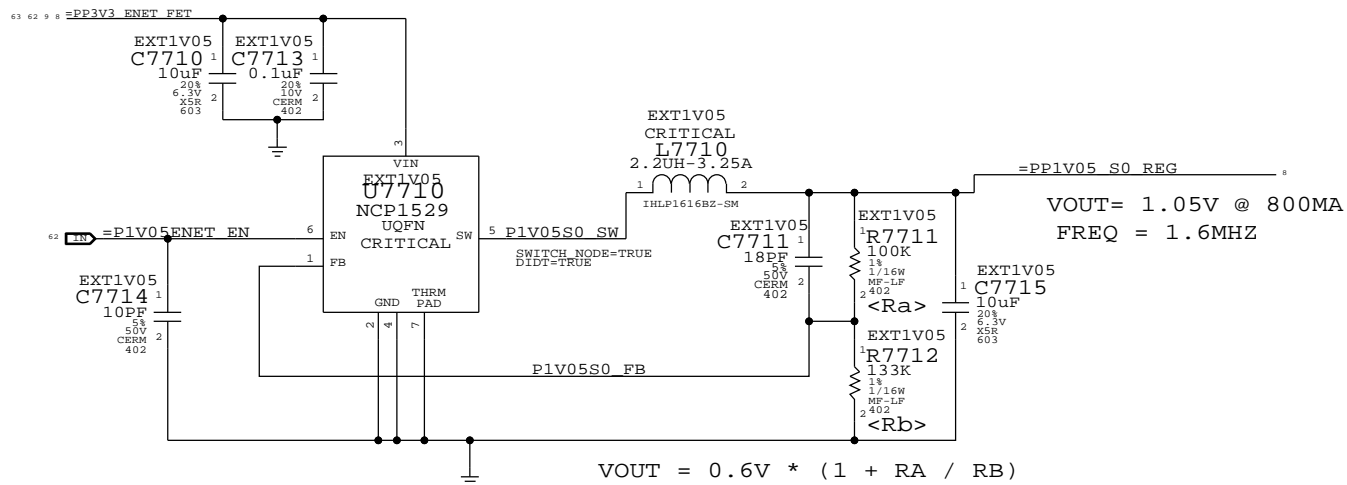
VID<3:0>	VOLTAGE
1100	0.9750V
1101	0.9625V
1110	0.9500V
1111	0.9375V
0000	0.9250V
0001	0.9125V
0010	0.9000V
0011	0.8875V
0100	0.8750V
0101	0.8625V
0110	0.8500V
0111	0.8375V
1000	0.8250V
1001	0.8125V
1010	0.8000V
1011	0.7875V

K6 NOTES : XOR AND INVERTER IS REMOVED, CANNOT SYNC THIS PAGE FROM T27

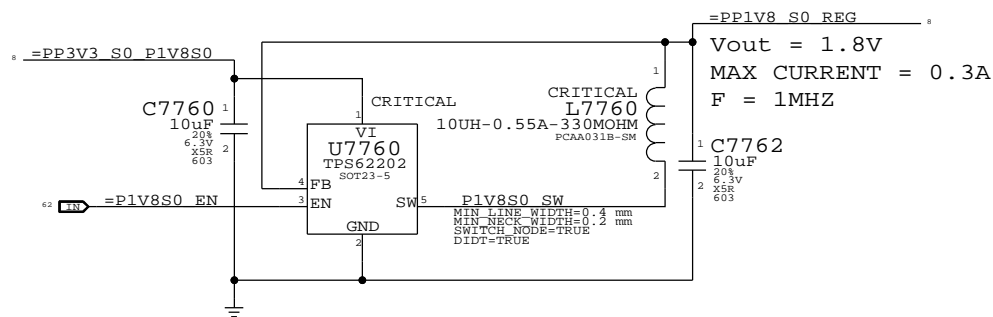
SYNC MASTER=(K6 MLB)		SYNC DATE=(10/27/2009)	
PAGE TITLE			
MCP VCore Regulator			
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PAGE TITLE			
CPU VTT(1.05V)		SUPPLY	
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		REVISION	
		C.0.0	
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		76	OF 109
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		60	OF 76

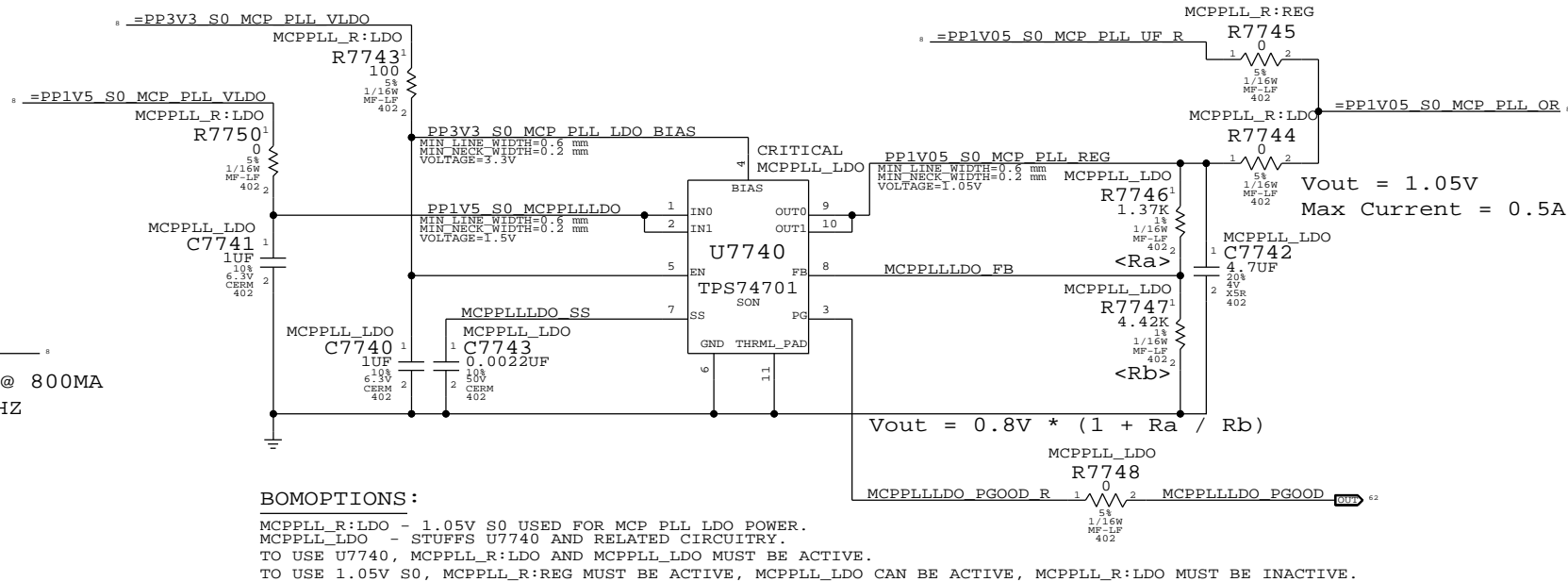
## 1.05V ENET Switcher



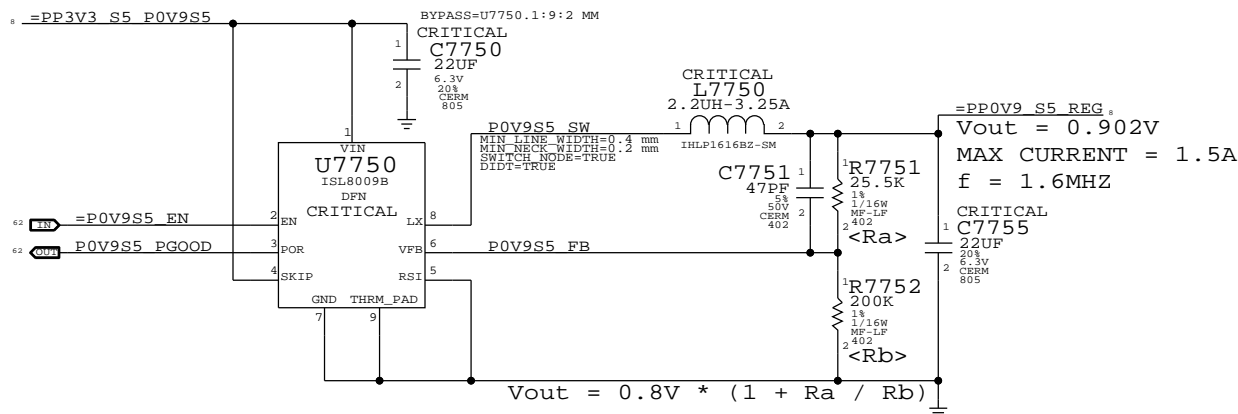
## 1.8V S0 Switcher



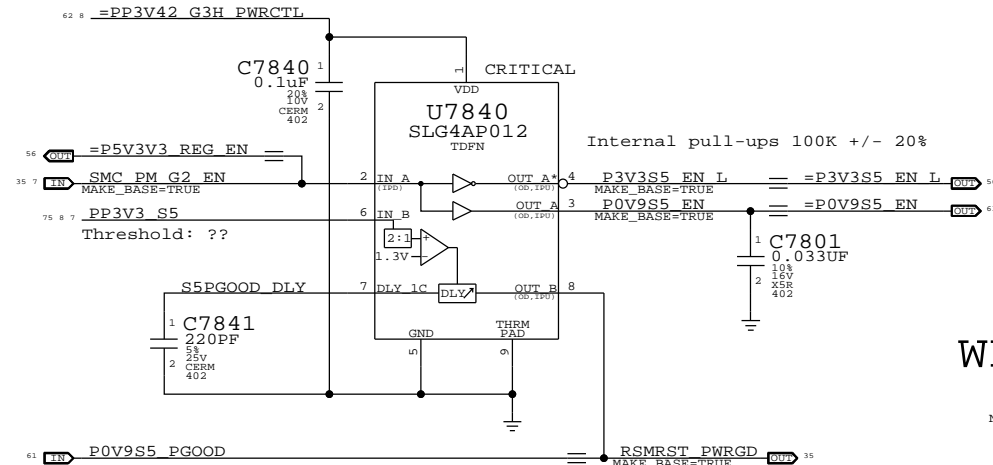
## 1.05V S0 MCP PLL LDO



## MCP 0.9V S5 (AUXC) Switcher



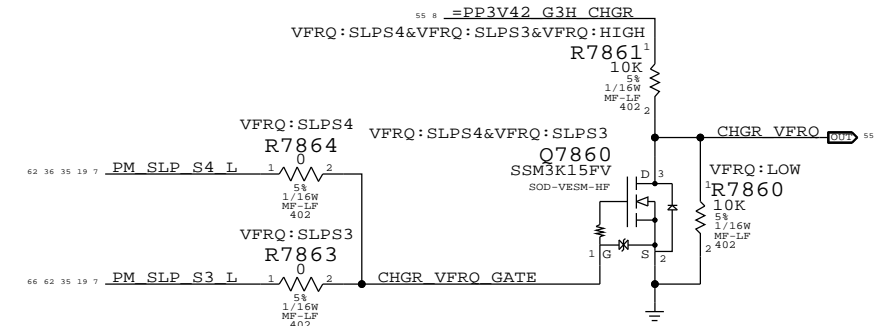
# S5 Rail Enables & PGOOD



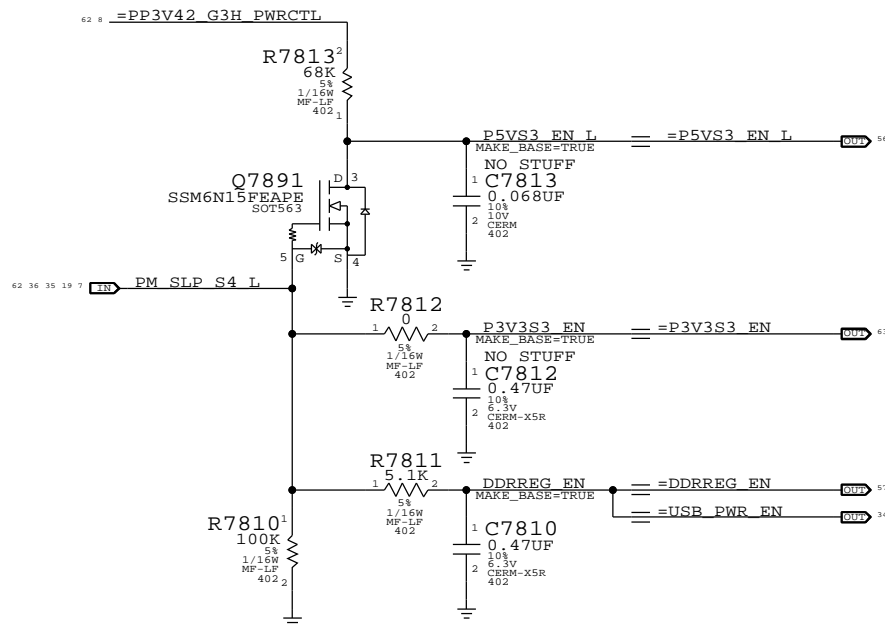
## Power Control Signals

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

## ISL6259 Frequency Select



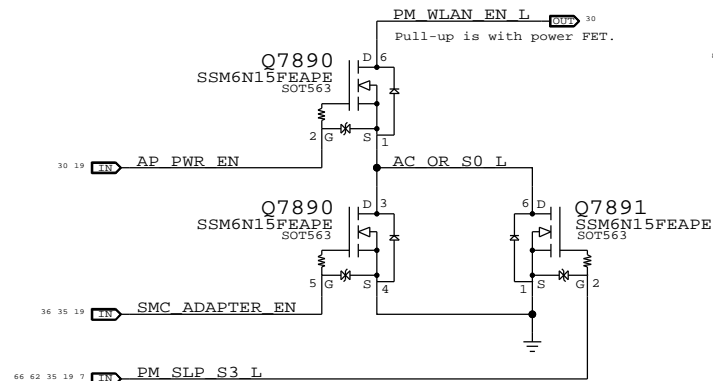
## S3 Rail Enables



## WLAN Enable Generation

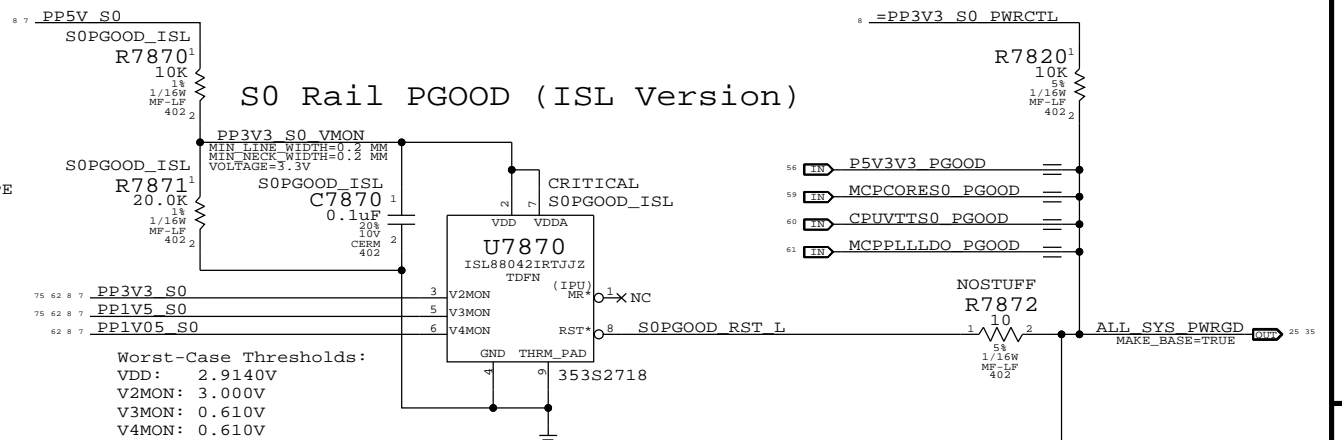
```
"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))
```

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP\_PWR\_EN signal.

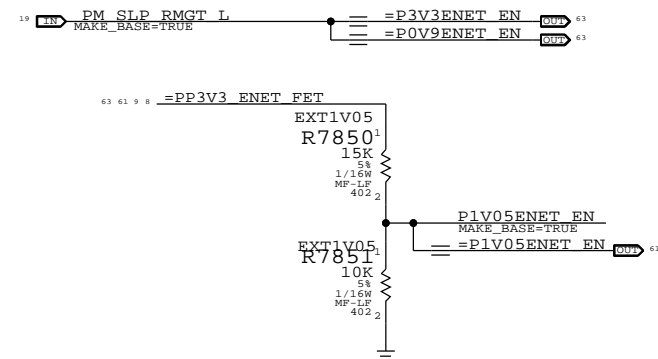


## S0 Rail PGOOD Circuitry

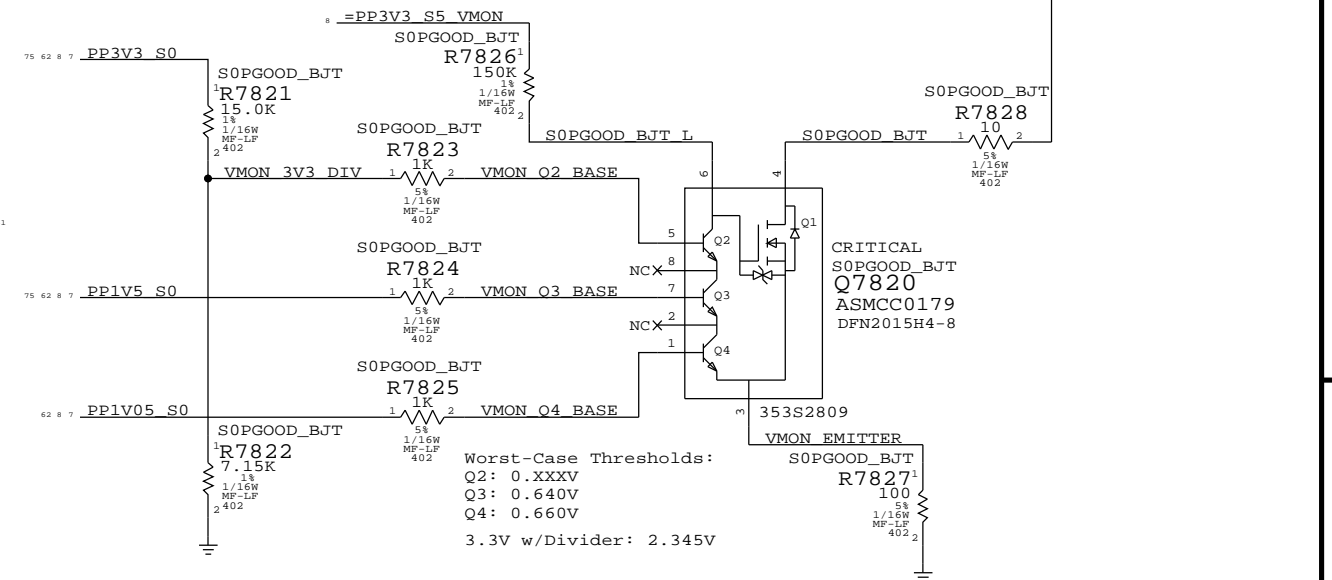
S0 Rail PGOOD (ISL Version)



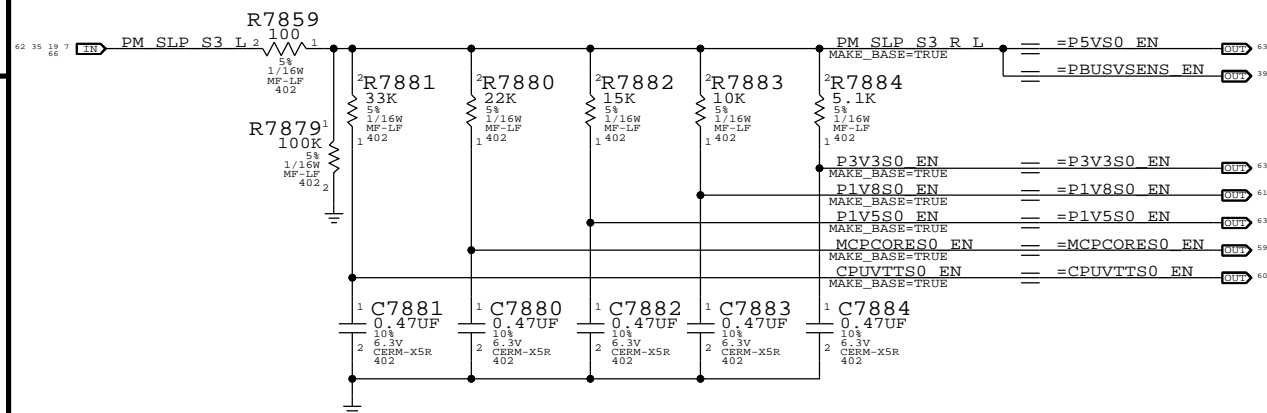
## ENET Rail Enables



## S0 Rail PGOOD (BJT Version)



S0 Rail Enables

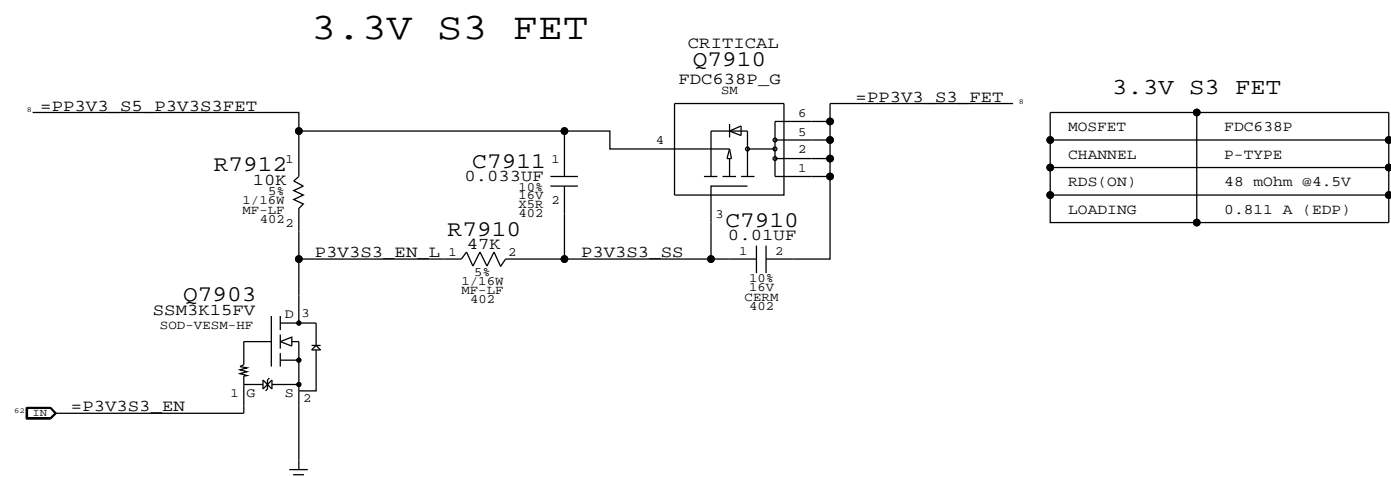


## VTT Rail Enable

VTT rail must ramp up in about the same time as MEMVDD rail (Q2300).

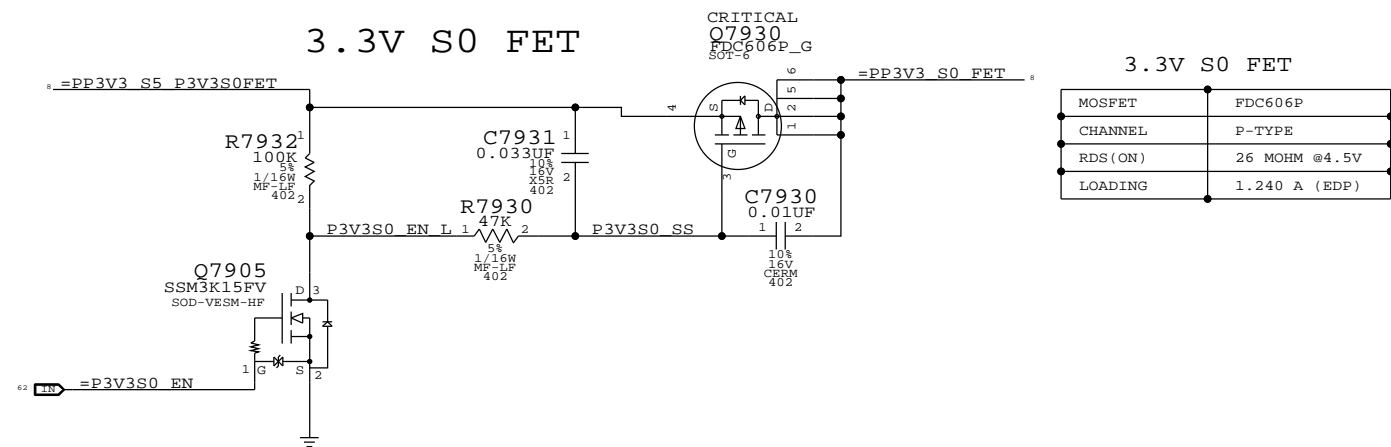
Unused PGOOD signal





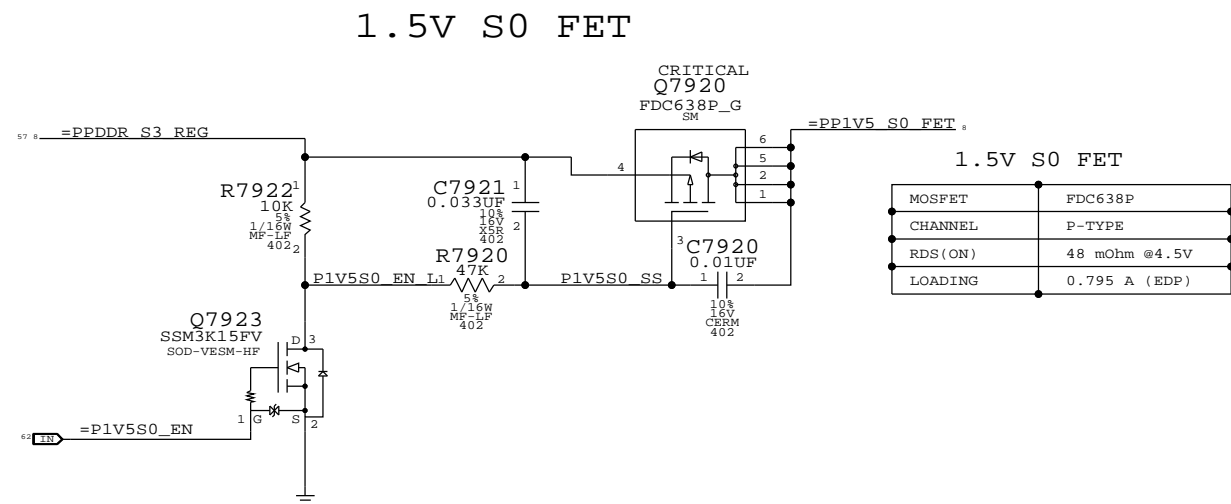
### 3.3V S3 FET

MOSFET	FDC638P
CHANNEL	P-TYPE
RDS (ON)	48 mOhm @4.5V
LOADING	0.811 A (EDP)

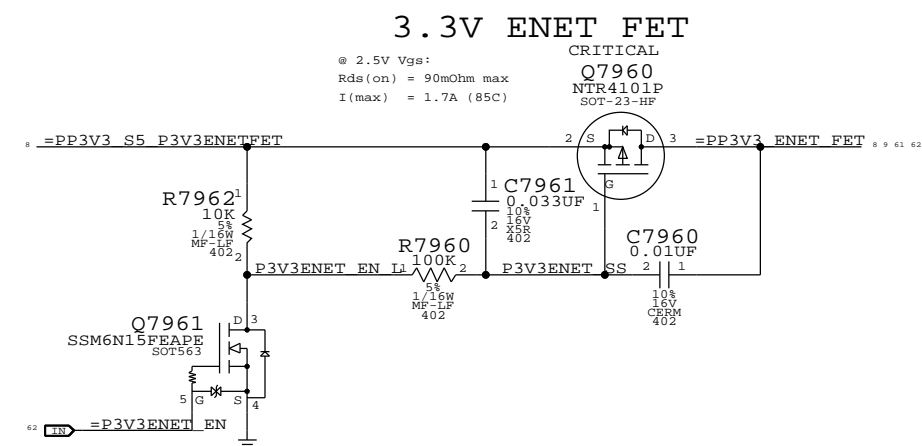


### 3.3V S0 FET

MOSFET	FDC606P
CHANNEL	P-TYPE
RDS (ON)	26 MOHM @4.5V
LOADING	1.240 A (EDP)



1.5V S0 FET	
MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.795 A (EDP)

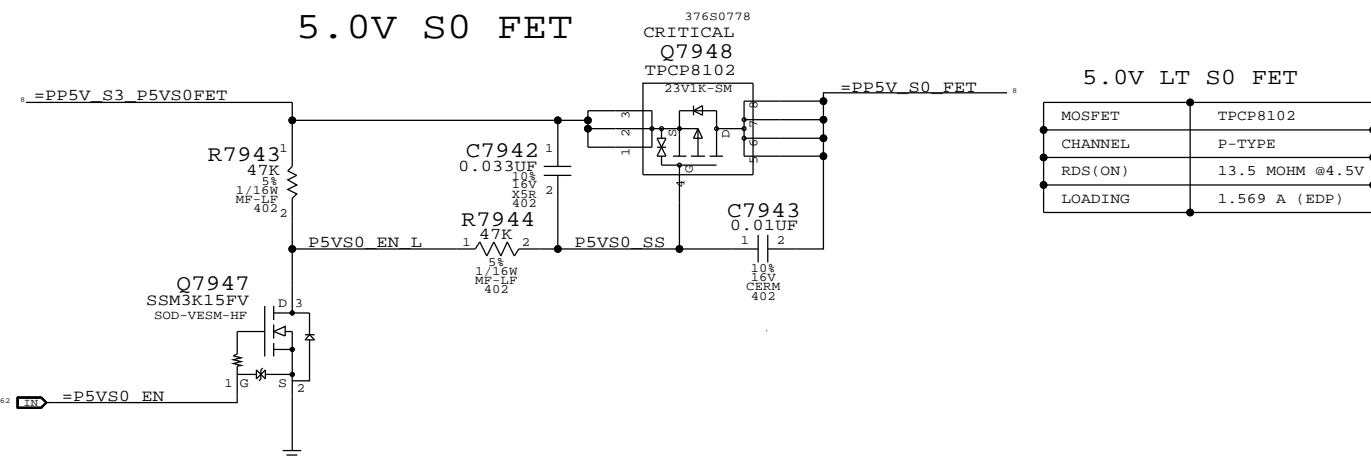
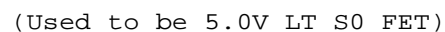


@ 2.5V Vgs:  
Rds(on) = 90mOhm max.  
I(max) = 1.7A (85C)

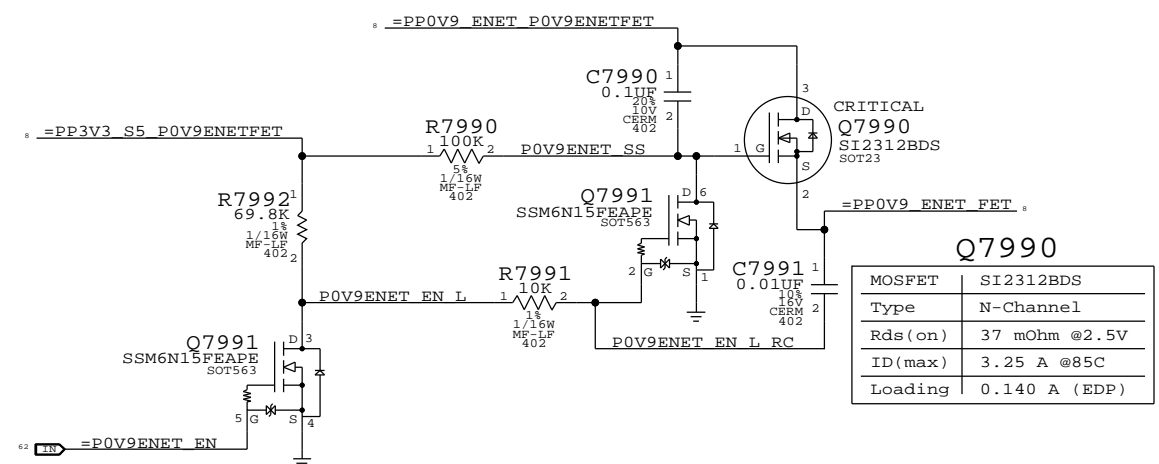
CRITICAL  
Q7960  
NTR4101P  
SOT-23-HF

MOBILE:

Recommend aliasing PM\_SLP\_RMGT\_L and  
=P3V3ENET\_EN. Nets separated on  
ARB for alternate power options.

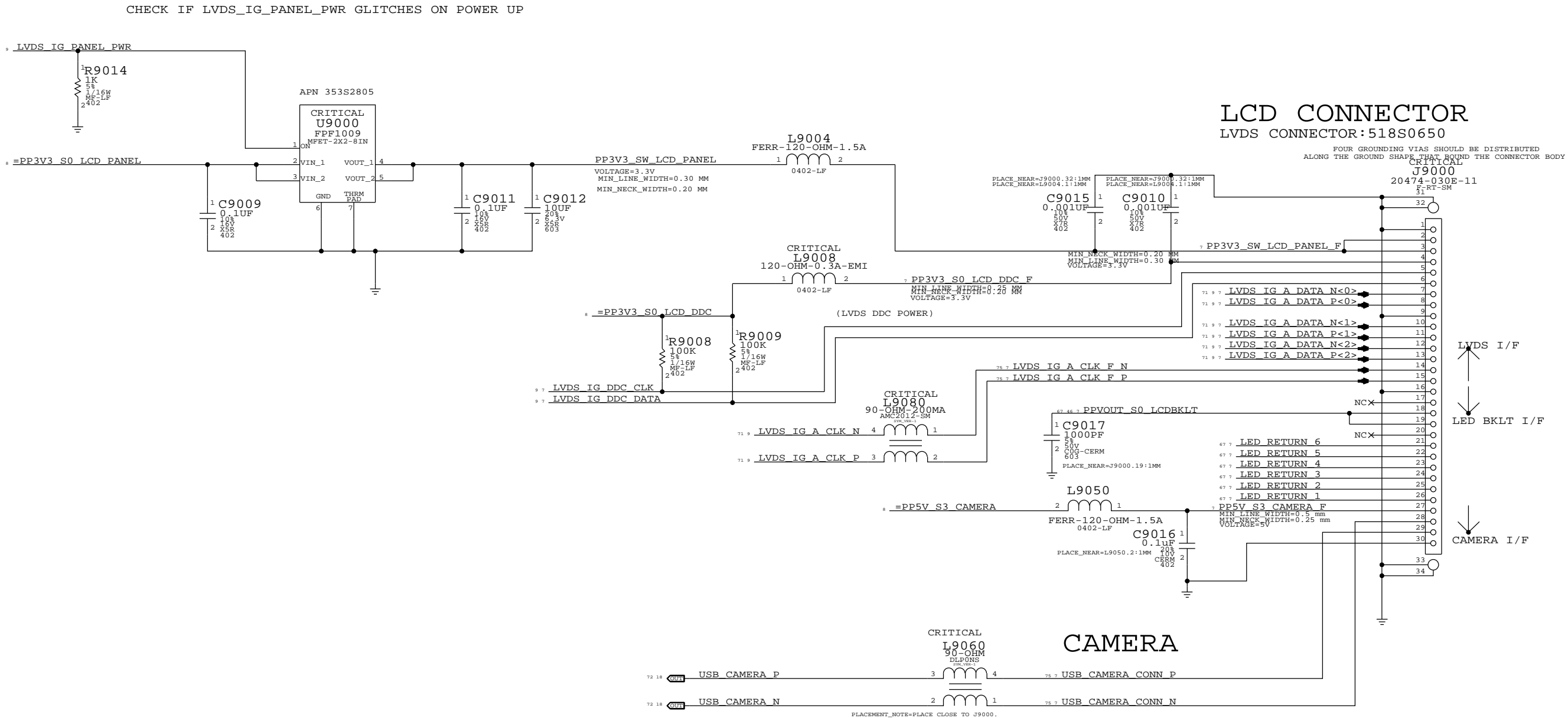


5.0V LT S0 FET	
MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	13.5 MOHM @4.5V
LOADING	1.569 A (EDP)

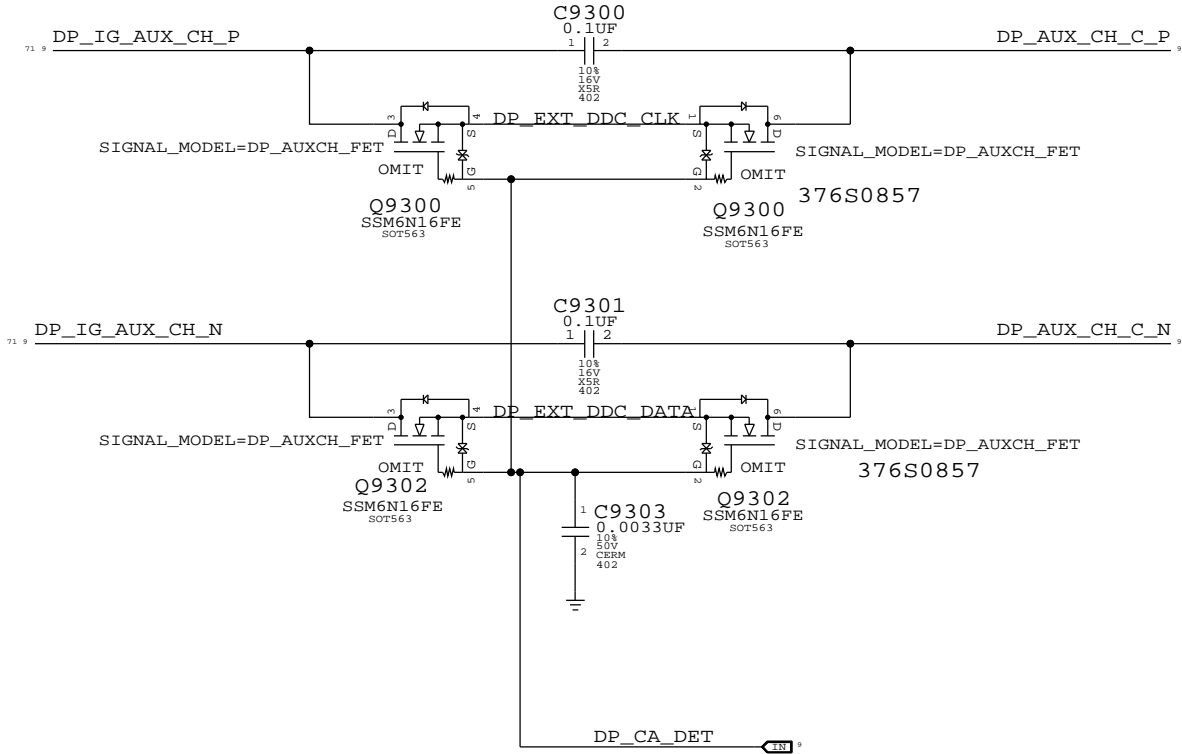


MOSFET	SI2312BDS
Type	N-Channel
Rds(on)	37 mOhm @2.5V
ID(max)	3.25 A @85°C
Loading	0.140 A (EDP)





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LVDS CONNECTOR		LVDS CONNECTOR	
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0859	2	XSTR,PT,N-CH,DUAL,SOT-563	Q9300,Q9302	CRITICAL	

SYNC MASTER=K6 MLB

SYNC DATE=02/16/2010

DISPLAYPORT SUPPORT

 Apple Inc.

051-8561

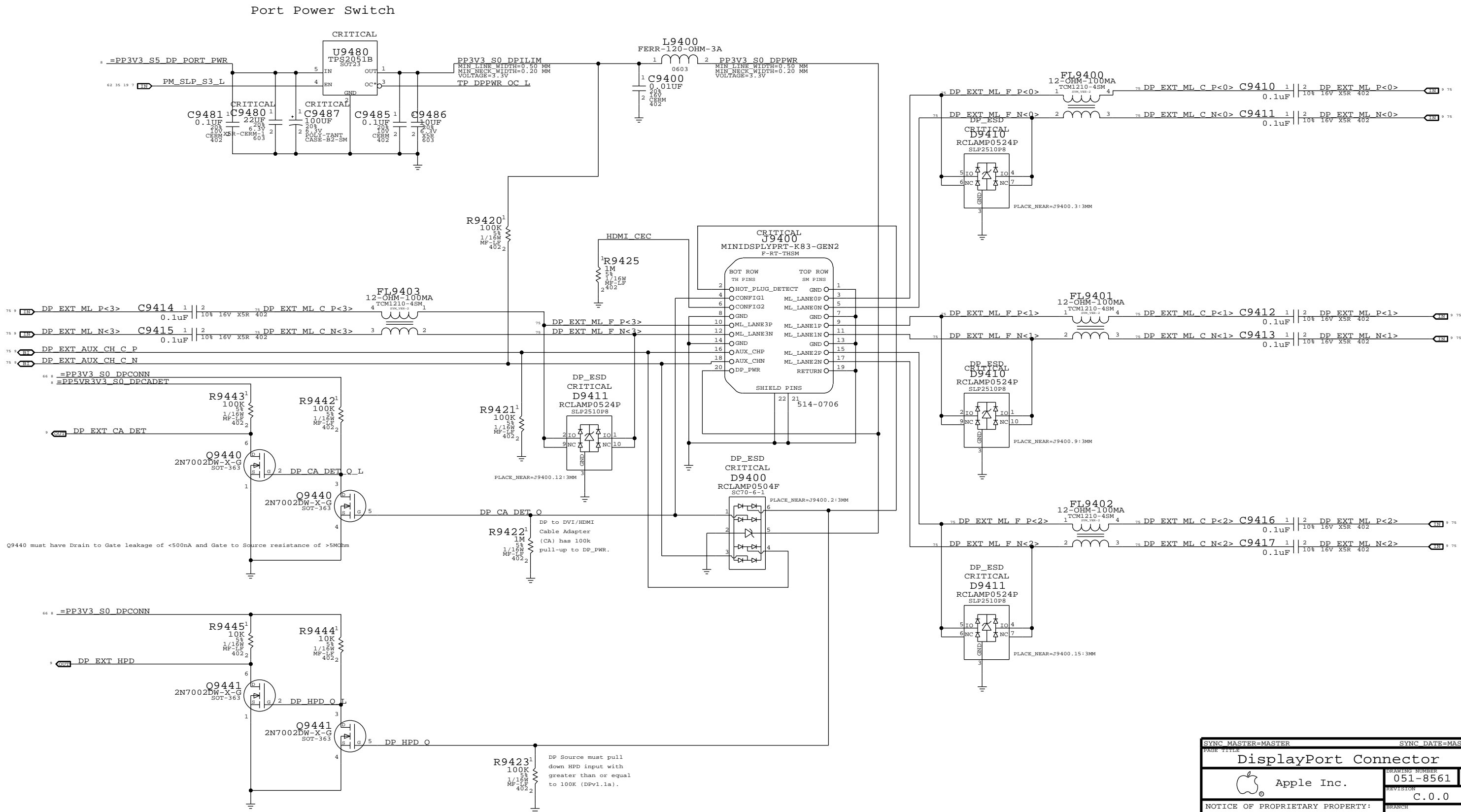
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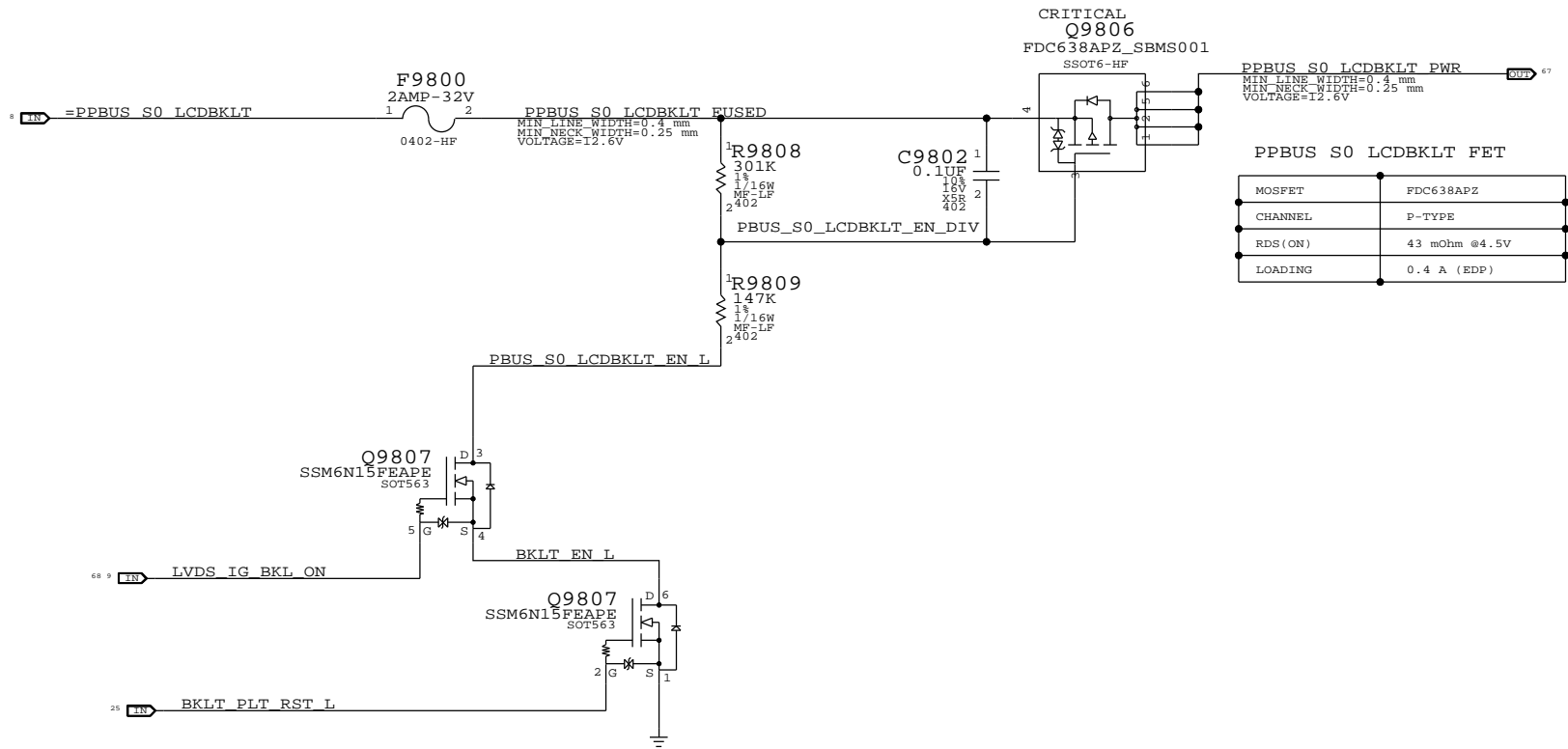


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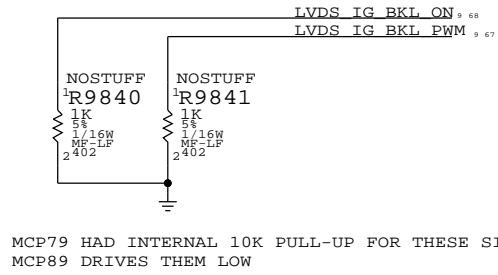
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		SHEET	66 OF 76



8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---



PPBUS S0 LCDBKLT FET	
MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS (ON)	43 mOhm @4.5V
LOADING	0.4 A (EDP)



SYNC MASTER=(K84\_MLB)

SYNC DATE=(10/19/2009)

LCD Backlight Support

Apple Inc.

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FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.

Signals within each 4x group should be matched within 5 ps of strobe.

DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 135 ps.

Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.

FSB 2X signals / groups shown in signal table on right.

Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 270 ps.

Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.

Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP89 Interface DG (DG-04625-001\_v0.9), Section 2.1

SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.

Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP89 Interface DG (DG-04625-001\_v0.9), Section 2.1

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP89 Interface DG (DG-04625-001\_v0.9), Section 2.1.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF


SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2.5

CPU / FSB Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
		PHYSICAL	SPACING	
FSB 4X Signal Groups	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB D L<15..0> 7 10 14
	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB DINV L<0> 7 10 14
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<0> 7 10 14
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<0> 7 10 14
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB D L<31..16> 7 10 14
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB DINV L<1> 7 10 14
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<1> 7 10 14
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<1> 7 10 14
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB D L<47..32> 7 10 14
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB DINV L<2> 7 10 14
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<2> 7 10 14
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<2> 7 10 14
FSB 2X Signals	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB D L<63..48> 7 10 14
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB DINV L<3> 7 10 14
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<3> 7 10 14
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<3> 7 10 14
	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB A L<16..3> 7 10 14
	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB REQ L<4..0> 7 10 14
	FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB ADSTB L<0> 7 10 14
	FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB A L<35..17> 7 10 14
	FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB ADSTB L<1> 7 10 14
	FSB_1X	FSB_50S	FSB_1X	FSB ADS L 7 10 14
	FSB_BREQ0_L	FSB_50S	FSB_1X	FSB_BREQ0_L 10 14
	FSB_1X	FSB_50S	FSB_1X	FSB BNR L 10 14
FSB 1X Signals	FSB_1X	FSB_50S	FSB_1X	FSB BPRI L 10 14
	FSB_1X	FSB_50S	FSB_1X	FSB DBSY L 10 14
	FSB_1X	FSB_50S	FSB_1X	FSB DEFER L 10 14
	FSB_1X	FSB_50S	FSB_1X	FSB DRDY L 10 14
	FSB_1X	FSB_50S	FSB_1X	FSB HIT L 7 10 14
	FSB_1X	FSB_50S	FSB_1X	FSB HITM L 7 10 14
	FSB_1X	FSB_50S	FSB_1X	FSB LOCK L 7 10 14
	FSB_CPURST_L	FSB_50S	FSB_1X	FSB_CPURST L 10 13 14
	FSB_1X	FSB_50S	FSB_1X	FSB RS L<2..0> 10 14
	FSB_1X	FSB_50S	FSB_1X	FSB TRDY L 10 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU A20M L 10 14
	CPU_BSEL	CPU_50S	CPU_AGTL	CPU_BSEL<2..0> 9 10
	CPU_FERR_L	CPU_50S	CPU_8MIL	CPU FERR L 10 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU IGNE L 10 14
	CPU_INIT_L	CPU_50S	CPU_AGTL	CPU INIT L 10 14
	CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU INTR 10 14
	CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU NMI 10 14
	CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU PROCHOT L 10 14 36
	CPU_PWRGD	CPU_50S	CPU_AGTL	CPU PWRGD 10 13 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU SMI L 10 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU STPCLK L 10 14
	PM_THERMTRIP_L	CPU_50S	CPU_8MIL	PM THERMTRIP L 10 14 36
	FSB_CPUSLP_L	CPU_50S	CPU_AGTL	FSB_CPUSLP L 10 14
	CPU_FROM_SR	CPU_50S	CPU_AGTL	CPU DPSLP L 10 14
	CPU_DPRSTP_L	CPU_50S	CPU_AGTL	CPU DPRSTP L 10 14 58
	CPU_ASYNC	CPU_50S	CPU_AGTL	FSB DPWR L 10 14
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB CLK CPU P 10 14
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB CLK CPU N 10 14
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB CLK ITP P 13 14
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB CLK ITP N 13 14
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB CLK MCP P 14
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB CLK MCP N 14
	CPU_IERR_L	CPU_50S		CPU IERR L 10
	PM_DPRSLEVR	CPU_50S	CPU_AGTL	PM DPRSLEVR 14 58
	(See above)	CPU_50S	CPU_AGTL	IMVP DPRSLEVR 58
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP VDD 14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP GND 14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP VCC 14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP GND 14
	CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU GTLREF 10 29
	CPU_COMP	CPU_50S	CPU_COMP	CPU COMP<3> 10
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<2> 10
	CPU_COMP	CPU_50S	CPU_COMP	CPU COMP<1> 10
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<0> 10
	XDP_TDI	CPU_50S	CPU_ITP	XDP TDI 10 13
	XDP_TDO	CPU_50S	CPU_ITP	XDP TDO 10 13
	XDP_TMS	CPU_50S	CPU_ITP	XDP TMS 10 13
	XDP_TCK	CPU_50S	CPU_ITP	XDP TCK 10 13
	XDP_TRST_L	CPU_50S	CPU_ITP	XDP TRST L 10 13
	XDP_BPM_L	CPU_50S	CPU_ITP	XDP BPM L<4..0> 10 13
	XDP_BPM_L5	CPU_50S	CPU_ITP	XDP BPM L<5> 10 13
	(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP CPURST L 13
		CPU_50S	CPU_8MIL	CPU VID<6..0> 11 58
		CPU_50S	CPU_8MIL	IMVP6 VID<6..0> 11 58
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE P 11 58
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE N 11 58
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN P 58
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN N 58

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CPU/FSB Constraints			
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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_20OTHER	*	25 MIL	?

NV DG says 3x inner, 4x outer

NV DG says 2x inner, 4x outer

NV DG says 2x inner, 4x outer

NV DG says 2x inner, 4x outer

NV DG says 2x inner, 4x outer

NV DG says 2x inner, 4x outer

NV DG says 2x inner, 4x outer

NV DG says 4x inner, 5x outer

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_20OTHER
MEM_CTRL	*	*	MEM_20OTHER
MEM_CMD	*	*	MEM_20OTHER
MEM_DATA	*	*	MEM_20OTHER
MEM_DQS	*	*	MEM_20OTHER

DDR3:  
DQ signals should be matched within 5 ps of associated DQS pair.  
DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 360 ps  
No DQS to clock matching requirement.  
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.  
CMD/CTRL signals should be matched within 150 ps.  
All memory signals maximum length is 1.030 ps.

SOURCE: MCP89 Interface DG (DG-04625-001\_v0.9), Section 2.2.3  
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints


PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001\_v0.9), Section 2.2.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
MEM_A_CLK	MEM_70D	MEM_CLK	MEM A CLK P<5..0>	15 26
MEM_A_CLK	MEM_70D	MEM_CLK	MEM A CLK N<5..0>	15 26
MEM_A_CKE	MEM_40S	MEM_CTRL	MEM A CKE<3..0>	15 21 26
MEM_A_CNTRL	MEM_40S	MEM_CTRL	MEM A CS L<3..0>	15 26
MEM_A_CNTRL	MEM_40S	MEM_CTRL	MEM A ODT<3..0>	15 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A A<15..0>	15 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A BA<2..0>	15 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A RAS L	15 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A CAS L	15 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A WE L	15 26
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM A DQ<7..0>	15 28
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM A DQ<15..8>	15 28
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM A DQ<23..16>	15 28
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM A DQ<31..24>	15 28
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM A DQ<39..32>	15 28
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM A DQ<47..40>	15 28
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM A DQ<55..48>	15 28
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM A DQ<63..56>	15 28
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM A DM<0>	15 28
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM A DM<1>	15 28
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM A DM<2>	15 28
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM A DM<3>	15 28
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM A DM<4>	15 28
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM A DM<5>	15 28
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM A DM<6>	15 28
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM A DM<7>	15 28
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM A DQS P<0>	15 28
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM A DQS N<0>	15 28
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM A DQS P<1>	15 28
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM A DQS N<1>	15 28
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM A DQS P<2>	15 28
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM A DQS N<2>	15 28
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM A DQS P<3>	15 28
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM A DQS N<3>	15 28
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM A DQS P<4>	15 28
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM A DQS N<4>	15 28
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM A DQS P<5>	15 28
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM A DQS N<5>	15 28
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM A DQS P<6>	15 28
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM A DQS N<6>	15 28
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM A DQS P<7>	15 28
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM A DQS N<7>	15 28
MEM_B_CLK	MEM_70D	MEM_CLK	MEM B CLK P<5..0>	15 27
MEM_B_CLK	MEM_70D	MEM_CLK	MEM B CLK N<5..0>	15 27
MEM_B_CKE	MEM_40S	MEM_CTRL	MEM B CKE<3..0>	15 21 27
MEM_B_CNTRL	MEM_40S	MEM_CTRL	MEM B CS L<3..0>	15 27
MEM_B_CNTRL	MEM_40S	MEM_CTRL	MEM B ODT<3..0>	15 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B A<15..0>	15 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B BA<2..0>	15 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B RAS L	15 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B CAS L	15 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B WE L	15 27
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM B DQ<7..0>	15 28
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM B DQ<15..8>	15 28
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM B DQ<23..16>	15 28
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM B DQ<31..24>	15 28
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM B DQ<39..32>	15 28
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM B DQ<47..40>	15 28
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM B DQ<55..48>	15 28
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM B DQ<63..56>	15 28
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM B DM<0>	15 28
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM B DM<1>	15 28
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM B DM<2>	15 28
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM B DM<3>	15 28
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM B DM<4>	15 28
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM B DM<5>	15 28
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM B DM<6>	15 28
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM B DM<7>	15 28
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM B DQS P<0>	15 28
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM B DQS N<0>	15 28
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM B DQS P<1>	15 28
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM B DQS N<1>	15 28
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM B DQS P<2>	15 28
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM B DQS N<2>	15 28
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM B DQS P<3>	15 28
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM B DOS N<3>	15 28
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM B DQS P<4>	15 28
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM B DQS N<4>	15 28
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM B DQS P<5>	15 28
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM B DQS N<5>	15 28
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM B DQS P<6>	15 28
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM B DQS N<6>	15 28
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM B DQS P<7>	15 28
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM B DQS N<7>	15 28
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP VDD	15
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP GND	15

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PAGE TITLE			
Memory Constraints		DRAWING NUMBER	051-8561
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PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001\_v0.9), Section 2.3

NEED PCIe Gen1/Gen2 notes!

Analog Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CRT	*	20 MIL	?
CRT_2CRT	*	15 MIL	?
CRT_2CLK	*	50 MIL	?
CRT_2SWITCHER	*	250 MIL	?
CRT_SYNC	*	=4x_DIELECTRIC	?
MCP_DAC_COMP	*	=2x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT

CRT signal single-ended impedance varies by location:  
- 37.5-ohm from MCP to first termination resistor.  
- 50-ohm from first to second termination resistor.  
- 75-ohm from output of three-pole filter to connector (if possible).  
R/G/B signals should be matched as close as possible and < 10 inches.  
SOURCE: MCP89 Interface DG (DG-04625-001\_v0.9), Section 2.4.1.

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be matched within 100 mils.  
NOTE: NV DG recommends 90 ohm differential for LVDS, but cable/display assume 100 ohm.  
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 100 ps.  
DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.  
Max trace length: LVDS 10 inches, DP 8.5 inches.  
SOURCE: MCP89 Interface DG (DG-04625-001\_v0.9), Section 2.4.2

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF


SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=3x_DIELECTRIC	?
SATA_TERMPP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=4x_DIELECTRIC	?

SATA intra-pair matching should be 1 ps.  
Max trace length: 12 inches for SATA Gen1/Gen2, TBD for SATA Gen3.  
SOURCE: MCP89 Interface DG (DG-04625-001\_v0.9), Section 2.6

MCP89 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
	PCIE_90D	PCIE	PEG R2D P<15..0>
	PCIE_90D	PCIE	PEG R2D N<15..0>
PEG_R2D	PCIE_90D	PCIE	PEG R2D C P<15..0>
	PCIE_90D	PCIE	PEG R2D C N<15..0>
PEG_D2R	PCIE_90D	PCIE	PEG D2R P<15..0>
	PCIE_90D	PCIE	PEG D2R N<15..0>
	PCIE_90D	PCIE	PEG D2R C P<15..0>
	PCIE_90D	PCIE	PEG D2R C N<15..0>
	PCIE_90D	PCIE	PCIE AP R2D P
	PCIE_90D	PCIE	PCIE AP R2D N
PCIE_AP_R2D	PCIE_90D	PCIE	PCIE AP R2D C P
	PCIE_90D	PCIE	PCIE AP R2D C N
PCIE_AP_D2R	PCIE_90D	PCIE	PCIE AP D2R P
	PCIE_90D	PCIE	PCIE AP D2R N
	PCIE_90D	PCIE	PCIE ENET R2D P
	PCIE_90D	PCIE	PCIE ENET R2D N
PCIE_ENET_R2D	PCIE_90D	PCIE	PCIE ENET R2D C P
	PCIE_90D	PCIE	PCIE ENET R2D C N
PCIE_ENET_D2R	PCIE_90D	PCIE	PCIE ENET D2R P
	PCIE_90D	PCIE	PCIE ENET D2R N
	PCIE_90D	PCIE	PCIE ENET D2R C P
	PCIE_90D	PCIE	PCIE ENET D2R C N
	PCIE_90D	PCIE	PCIE FW R2D P
	PCIE_90D	PCIE	PCIE FW R2D N
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE FW R2D C P
	PCIE_90D	PCIE	PCIE FW R2D C N
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE FW D2R P
	PCIE_90D	PCIE	PCIE FW D2R N
	PCIE_90D	PCIE	PCIE FW D2R C P
	PCIE_90D	PCIE	PCIE FW D2R C N
MCP_PE0_REECLK	CLK_PCIE_100D	CLK_PCIE	PEG CLK100M P
	CLK_PCIE_100D	CLK_PCIE	PEG CLK100M N
MCP_PE1_REECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M AP P
	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M AP N
MCP_PE2_REECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M ENET P
	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M ENET N
MCP_PE3_REECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M FW P
	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M FW N
MCP_PEX_CLK_COMP		MCP_PEX_COMP	MCP_PEX0_TERMPP
CRT_RED	CRT_50S	CRT	CRT IG R C PR
CRT_GREEN	CRT_50S	CRT	CRT IG G Y Y
CRT_BLUE	CRT_50S	CRT	CRT IG B COMP PB
CRT_SYNC	CRT_50S	CRT_SYNC	CRT IG HSYNC
CRT_SYNC	CRT_50S	CRT_SYNC	CRT IG VSYNC
MCP_DAC_RSET		MCP_DAC_COMP	MCP_TV_DAC_RSET
MCP_DAC_VREF		MCP_DAC_COMP	MCP_TV_DAC_VREF
TMDS_IG_TXC	DP_90D	DISPLAYPORT	TMDS IG TXC P
TMDS_IG_TXC	DP_90D	DISPLAYPORT	TMDS IG TXC N
TMDS_IG_TXD	DP_90D	DISPLAYPORT	TMDS IG TXD P<5..0>
TMDS_IG_TXD	DP_90D	DISPLAYPORT	TMDS IG TXD N<5..0>
DP_EXT_ML	DP_90D	DISPLAYPORT	DP IG ML P<3..0>
DP_EXT_ML	DP_90D	DISPLAYPORT	DP IG ML N<3..0>
DP_EXT_AUX_CH	DP_90D	DISPLAYPORT	DP IG AUX CH P
DP_EXT_AUX_CH	DP_90D	DISPLAYPORT	DP IG AUX CH N
MCP_TMDS0_RSET	MCP_DV_COMP		MCP_TMDS0_RSET
MCP_TMDS0_VPROBE			MCP_TMDS0_VPROBE
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS IG A CLK P
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS IG A CLK N
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS IG A DATA P<2..0>
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS IG A DATA N<2..0>
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS IG A DATA P<3>
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS IG A DATA N<3>
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS IG B CLK P
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS IG B CLK N
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS IG B DATA P<2..0>
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS IG B DATA N<2..0>
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS IG B DATA P<3>
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS IG B DATA N<3>
MCP_IFPAB_RSET	MCP_DV_COMP		MCP_IFPAB_RSET
MCP_IFPAB_VPROBE			MCP_IFPAB_VPROBE
SATA_HDD_R2D	SATA_90D	SATA	SATA HDD R2D C P
	SATA_90D	SATA	SATA HDD R2D C N
	SATA_90D	SATA	SATA HDD R2D P
	SATA_90D	SATA	SATA HDD R2D N
SATA_HDD_D2R	SATA_90D	SATA	SATA HDD D2R P
	SATA_90D	SATA	SATA HDD D2R N
	SATA_90D	SATA	SATA HDD D2R C P
	SATA_90D	SATA	SATA HDD D2R C N
SATA_ODD_R2D	SATA_90D	SATA	SATA ODD R2D C P
	SATA_90D	SATA	SATA ODD R2D C N
	SATA_90D	SATA	SATA ODD R2D P
	SATA_90D	SATA	SATA ODD R2D N
SATA_ODD_D2R	SATA_90D	SATA	SATA ODD D2R P
	SATA_90D	SATA	SATA ODD D2R N
	SATA_90D	SATA	SATA ODD D2R C P
	SATA_90D	SATA	SATA ODD D2R C N
MCP_SATA_TERMPP		SATA_TERMPP	MCP_SATA_TERMPP

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MCP Constraints 1		DRAWING NUMBER	051-8561
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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=1.5x_DIELECTRIC	?
CLK_LPC	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001\_v0.9), Section 2.7

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?	USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001\_v0.9), Section 2.8

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001\_v0.9), Section 2.9

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP89 Interface DG (DG-04625-001\_v0.9), Section 2.10

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=1.5x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001\_v0.9), Section 2.11

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=1.5x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001\_v0.9), Section 2.12

MCP89 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
LPC_AD	LPC_55S	LPC	LPC AD<3..0>	19 35 37
LPC_FRAME_L	LPC_55S	LPC	LPC FRAME L	19 35 37
LPC_RESET_L	LPC_55S	LPC	LPC RESET L	19 25
MCP_LPC_CLK0	CLK_LPC_55S	CLK_LPC	LPC CLK33M SMC R	19 25
	CLK_LPC_55S	CLK_LPC	LPC CLK33M SMC	25 35
	CLK_LPC_55S	CLK_LPC	LPC CLK33M LPCPLUS	25 37
USB_EXT_A	USB_90D	USB	USB EXT_A P	18 34
	USB_90D	USB	USB EXT_A N	18 34
	USB_90D	USB	USB EXT_A MUXED P	34 75
	USB_90D	USB	USB EXT_A MUXED N	34 75
USB_MINI	USB_90D	USB	USB MINI P	9 18
	USB_90D	USB	USB MINI N	9 18
USB_EXTD	USB_90D	USB	USB EXT_D P	9 18
	USB_90D	USB	USB EXT_D N	9 18
USB_CAMERA	USB_90D	USB	USB CAMERA P	18 64
	USB_90D	USB	USB CAMERA N	18 64
USB_BT	USB_90D	USB	USB BT P	18 30
	USB_90D	USB	USB BT N	18 30
USB_TPAD	USB_90D	USB	USB TPAD P	18 43
	USB_90D	USB	USB TPAD N	18 43
USB_IR	USB_90D	USB	USB IR P	9 18
	USB_90D	USB	USB IR N	9 18
USB_EXTR	USB_90D	USB	USB EXTB P	18 34
	USB_90D	USB	USB EXTB N	18 34
USB_T57	USB_90D	USB	USB T57 P	9 18
	USB_90D	USB	USB T57 N	9 18
USB_EXTC	USB_90D	USB	USB EXTC P	9 18
	USB_90D	USB	USB EXTC N	9 18
USB_SDCARD	USB_90D	USB	USB SDCARD P	9 18
	USB_90D	USB	USB SDCARD N	9 18
USB_WM	USB_90D	USB	USB WM P	9 18
	USB_90D	USB	USB WM N	9 18
MCP_USB_RBIAS	MCP_USB_RBIAS		MCP USB RBIAS GND	18
SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS MCP_0 CLK	13 19 38
SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS MCP_0 DATA	13 19 38
(SMBUS_SMC_MGMT_SCL)	SMB_55S	SMB	SMBUS MCP_1 CLK	19 38
(SMBUS_SMC_MGMT_SDA)	SMB_55S	SMB	SMBUS MCP_1 DATA	19 38
HDA_BIT_CLK	HDA_55S	HDA	HDA BIT_CLK	19 48
	HDA_55S	HDA	HDA BIT_CLK R	19
HDA_SYNC	HDA_55S	HDA	HDA SYNC	19 48
	HDA_55S	HDA	HDA SYNC R	19
HDA_RST_L	HDA_55S	HDA	HDA RST_R L	19
	HDA_55S	HDA	HDA RST_L	19 48
HDA_SDIN0	HDA_55S	HDA	HDA SDIN0	19 48
	HDA_55S	HDA	HDA SDIN0 CODEC	48
HDA_SDOUT	HDA_55S	HDA	HDA SDOUT	19 48
	HDA_55S	HDA	HDA SDOUT R	19
MCP_HDA_PULLDN_COMP		MCP_HDA_COMP	MCP HDA PULLDN COMP	19
MCP_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM CLK32K SUSCLK R	19 25
	CLK_SLOW_55S	CLK_SLOW	PM CLK32K SUSCLK	25 35
SPI_CLK	SPI_55S	SPI	SPI CLK R	19 37
	SPI_55S	SPI	SPI CLK	7 37
SPI_MOSI	SPI_55S	SPI	SPI MOSI R	19 37
	SPI_55S	SPI	SPI MOSI	7 37
SPI_MISO	SPI_55S	SPI	SPI MISO	7 19 37
SPI_CS0	SPI_55S	SPI	SPI CS0 R L	19 37
	SPI_55S	SPI	SPI CS0 L	7 37
	SPI_55S	SPI	SPI MLB_CLK	37 47
	SPI_55S	SPI	SPI MLB_MOSI	37 47
	SPI_55S	SPI	SPI MLB_MISO	37 47
	SPI_55S	SPI	SPI MLB_CS_L	37 47
	SPI_55S	SPI	SPI_ALT_CLK	37
	SPI_55S	SPI	SPI_ALT_MOSI	37
	SPI_55S	SPI	SPI_ALT_MISO	37
	SPI_55S	SPI	SPI_ALT_CS_L	37



MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	~STANDARD	7.5 MIL	7.5 MIL	~STANDARD	~STANDARD	~STANDARD
ENET_MII_55S	*	~55_OHM_SE	~55_OHM_SE	~55_OHM_SE	~55_OHM_SE	~STANDARD	~STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	~3:1_SPACING	?
ENET_MII	*	12 MIL	?

























SOURCE: MCP73 Interface DG (DG-02974-001\_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	~100_OHM_DIFF	~100_OHM_DIFF	~100_OHM_DIFF	~100_OHM_DIFF	~100_OHM_DIFF	~100_OHM_DIFF











SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001\_v01), Section 2.7.4









ELECTRICAL_CONSTRAINT_SET	SET_TYPE			
	PHYSICAL	SPACING		
 MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_VDD	18
 MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_GND	18
 MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0_R	9 31
 MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	RTL8211_CLK25M_CKXTAL1	31
 ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET_INTR_L	
 ENET_MDIO	ENET_MII_55S	ENET_MII	ENET_MDIO	18 31
 ENET_MDC	ENET_MII_55S	ENET_MII	ENET_MDC	9 31
 ENET_PWRDWN_L	ENET_MII_55S	ENET_MII	ENET_PWRDWN_L	
 ENET_CLK125M_RXCLK_R	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R	31
 ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK	18 31
 ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD_R<3..0>	31
 ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<0>	18 31
 ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<3..1>	18 31
 ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RX_CTRL	18 31
 ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RXCTL_R	31
 ENET_CLK125M_TXCLK_R	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK_R	31
 ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK	9 31
 ENET_TXD0	ENET_MII_55S	ENET_MII	ENET_TXD<0>	9 31
 ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<3..1>	9 31
 ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TX_CTRL	9 31
 ENET_RESET_L	ENET_MII_55S	ENET_MII	ENET_RESET_L	9 31
 ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_P<3..0>	31 32
 ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_N<3..0>	31 32
 ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_TRAN_P<3..0>	32
 ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_TRAN_N<3..0>	32

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
1T01_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
 SMBUS_SMC_A_S3_SCL	SMB_55S	SMB	SMBUS_SMC_A_S3_SCL 7 38
 SMBUS_SMC_A_S3_SDA	SMB_55S	SMB	SMBUS_SMC_A_S3_SDA 7 38
 SMBUS_SMC_B_S0_SCL	SMB_55S	SMB	SMBUS_SMC_B_S0_SCL 38
 SMBUS_SMC_B_S0_SDA	SMB_55S	SMB	SMBUS_SMC_B_S0_SDA 38
 SMBUS_SMC_0_S0_SCL	SMB_55S	SMB	SMBUS_SMC_0_S0_SCL 38
 SMBUS_SMC_0_S0_SDA	SMB_55S	SMB	SMBUS_SMC_0_S0_SDA 38
 SMBUS_SMC_BSA_SCL	SMB_55S	SMB	SMBUS_SMC_BSA_SCL 7 38
 SMBUS_SMC_BSA_SDA	SMB_55S	SMB	SMBUS_SMC_BSA_SDA 7 38
 SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL 38
 SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA 38

SMBus Charger Net Properties


NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
 CHGR_CSI	1T01_DIFFPAIR		CHGR_CSI_P 55
 CHGR_CSI_N	1T01_DIFFPAIR		CHGR_CSI_N 55
 CHGR_CSI_R_P	1T01_DIFFPAIR		CHGR_CSI_R_P 55
 CHGR_CSI_R_N	1T01_DIFFPAIR		CHGR_CSI_R_N 55
 CHGR_CSO	1T01_DIFFPAIR		CHGR_CSO_P 55
 CHGR_CSO_N	1T01_DIFFPAIR		CHGR_CSO_N 55
 CHGR_CSO_R_P	1T01_DIFFPAIR		CHGR_CSO_R_P 40 55
 CHGR_CSO_R_N	1T01_DIFFPAIR		CHGR_CSO_R_N 40 55

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# MCP Fanout Constraint Relaxations

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	5.8 MM OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	TOP	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MEM_COMP OVERRIDE	TOP	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MII_COMP OVERRIDE	TOP	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_USB_RBIAS OVERRIDE	TOP	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	*	OVERRIDE	OVERRIDE	0.25 MM OVERRIDE	250 MIL OVERRIDE	OVERRIDE	OVERRIDE

[illegible]


NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

## Misc Net Properties

## GRAPHICS NET PROPERTIES

## Power Net Properties

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SYNC MASTER=MASTER		SYNC DATE=MASTER	
PART TITLE		DRAWING NUMBER	
K87 SPECIFIC CONSTRAINTS		051-8561	
 Apple Inc.		SIZE	
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K87 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS							
BOARD LAYERS				BOARD AREAS		BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, 10L2, 10L3, 10L4, 10L5, 10L6, 10L7, 10L8, 10L9, 10L10, 10L11, BOTTOM				BG_TYPE, BGA_P10M		MM	16.5.1
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	<50_OHM_SE	0.100MM	30 MM	0 MM	0 MM
STANDARD	*	Y	<DEFAULT	<DEFAULT	12.7 MM	<DEFAULT	<DEFAULT
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	<STANDARD	<STANDARD	<STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.115 MM	0.115 MM			
50_OHM_SE	*	Y	0.076 MM	0.076 MM	<STANDARD	<STANDARD	<STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.165 MM	0.100 MM			
40_OHM_SE	*	Y	0.126 MM	0.100 MM	<STANDARD	<STANDARD	<STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP, BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	*	Y	0.222 MM	0.222 MM	<STANDARD	<STANDARD	<STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	<STANDARD	<STANDARD	<STANDARD	<STANDARD	<STANDARD
70_OHM_DIFF	10L3, 10L4, 10L9, 10L10	Y	0.151 MM	0.100 MM	<STANDARD	0.224 MM	0.224 MM
70_OHM_DIFF	TOP, BOTTOM	Y	0.185 MM	0.100 MM		0.200 MM	0.200 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	<STANDARD	<STANDARD	<STANDARD	<STANDARD	<STANDARD
90_OHM_DIFF	10L3, 10L4, 10L9, 10L10	Y	0.095 MM	0.095 MM		0.234 MM	0.234 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.112 MM	0.112 MM		0.220 MM	0.220 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	<STANDARD	<STANDARD	<STANDARD	<STANDARD	<STANDARD
100_OHM_DIFF	10L3, 10L4, 10L9, 10L10	Y	0.075 MM	0.075 MM		0.244 MM	0.244 MM
100_OHM_DIFF	TOP, BOTTOM	Y	0.091 MM	0.091 MM		0.230 MM	0.230 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1+1_DIFFPAIR	*	Y	<STANDARD	<STANDARD	<STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	<DEFAULT	?
BGA_P10M	*	<DEFAULT	?
BGA_P20M	*	<DEFAULT	?
BGA_P30M	*	<DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5X_DIELECTRIC	TOP, BOTTOM	0.105 MM	?
2X_DIELECTRIC	TOP, BOTTOM	0.140 MM	?
3X_DIELECTRIC	TOP, BOTTOM	0.210 MM	?
4X_DIELECTRIC	TOP, BOTTOM	0.280 MM	?
5X_DIELECTRIC	TOP, BOTTOM	0.350 MM	?
1.5X_DIELECTRIC	*	0.095 MM	?
2X_DIELECTRIC	*	0.126 MM	?
3X_DIELECTRIC	*	0.189 MM	?
4X_DIELECTRIC	*	0.252 MM	?
5X_DIELECTRIC	*	0.315 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P10M	BGA_P10M
MEM_CLK	*	BGA_P10M	BGA_P20M
CLK_FSB	*	BGA_P10M	BGA_P20M
CLK_LPC	*	BGA_P10M	BGA_P20M
CLK_PCIE	*	BGA_P10M	BGA_P20M
CLK_SLOW	*	BGA_P10M	BGA_P20M
FSB_DSTB	FSB_DSTB	BGA_P10M	BGA_P30M


NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_4DS	BGA_P10M	STANDARD

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SYNC MASTER=MASTER		SYNC DATE=MASTER			
PAGE TITLE					
K87 RULE DEFINITIONS					
 Apple Inc.		DRAWING NUMBER	SIZE		
		051-8561	D		
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