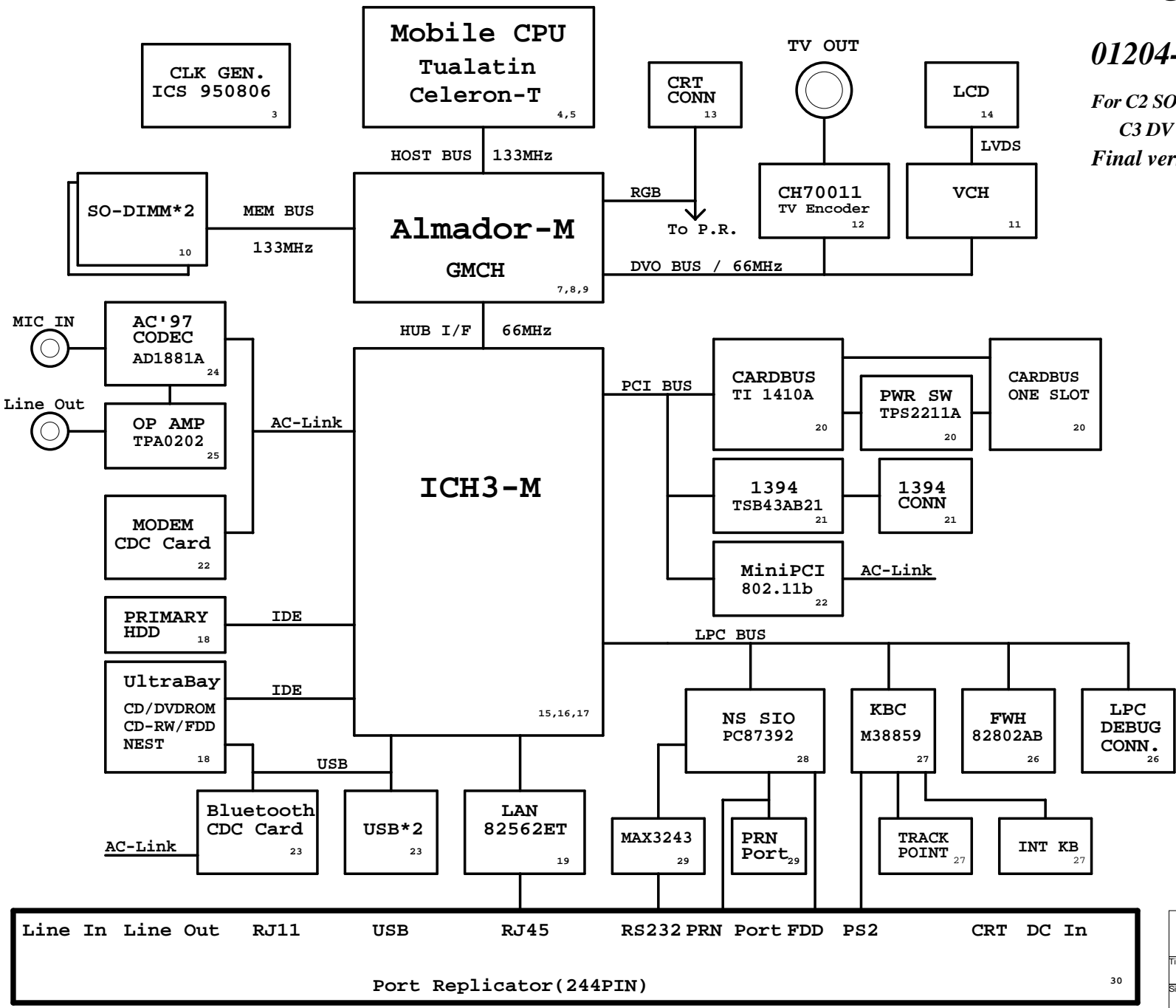


Jan. 11 2002

C-Note 2 Block Diagram



01204-3


For C2 SOVP  
C3 DV  
Final version

PCB LAYER	
L1:	Signal 1
L2:	GND
L3:	Signal 2
L4:	Signal 3
L5:	GND
L6:	POWER
L7:	Signal 4(weak)
L8:	Signal 5
L9:	GND
L10:	Signal 6

DC/DC&CHARGER Switching Power MAX1631/MAX1772	
INPUTS	OUTPUTS
DCBATOUT	LAN+3VAUX UBAY+5V +3VSUS +5VSUS +3VRUN +5VRUN
AD+	BT+ 33,36

CPU DC/DC Switching Power MAX1718/MAX1714	
INPUTS	OUTPUTS
DCBATOUT	+VCC_CORE +VCCT 31,32

OTHER DC/DC MAX1644/MAX1792	
INPUTS	OUTPUTS
+3.3VRUN +3.3VRUN	+1.8VRUN +1.5VRUN 32



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Title <b>Block Diagram</b>		
Size A3	Document Number <b>C-Note 2</b>	Rev -3
Date Friday, January 11, 2002	Sheet 1	of 37



# Cu-T & Tualatin SPEC Summary

July 3 '01

- 01.BLOCK DIAGRAM
- 02.TABLE OF CONTENT
- 03.CLOCK GENERATOR
- 04.CPU
- 05.CPU CONFIGURATION
- 06.OTP/Thermal/Fan Control/RFID
- 07.GMCH (1/3)
- 08.GMCH (2/3)
- 09.GMCH (3/3)
- 10.SO-DIMM
- 11.VCH
- 12.TV Encoder
- 13.CRT CONN
- 14.LCD/Inverter CONN
- 15.ICH3-M (1/3)
- 16.ICH3-M (2/3)
- 17.ICH3-M (3/3)
- 18.HDD & ULTRA BAY
- 19.LAN
- 20.PCMCIA Controller OZ6912
- 21.1394 TSB43AA22
- 22.Mini PCI SOCKET & MDC
- 23.USB I/F & BLUETOOTH
- 24.AC'97 CODEC-ALC200
- 25.OP AMP & PHONE JACK
- 26.FIRMWARE HUB
- 27.KBC-M38859
- 28.SIO-PC87392
- 29.Printer Port
- 30.PORT-REPLICATOR
- 31.CPU CORE
- 32.CPUIO/1.5V/1.8V/1.2V
- 33.3V/5V DC/DC
- 34.PWR PLANE & RESET LOGIC
- 35.CHARGER uP-MC68HC908SR
- 36.CHARGER CONTROLLER-MAX1772
- 37.SPARE Logic/TEST POINT

CG\_\* : CPU GTL+  
CC\_\* : CPU CMOS  
M\_\* : MEMORY BUS  
G\_\* : AGP BUS  
P\_\* : PCI BUS  
HL\_\* : HUB LINK I/F  
LPC\_\* : LPC I/F  
ICH\_AC\_\* : AC'97 LINK I/F  
IDE\_\* : IDE BUS

	Early Samples/ES	QS/ Production				
Tualatin	<p>VCC = 1.50V (perf mode)/ 1.15V (batt mode)</p> <p>VCCT = 1.3V (min), 1.365V (max)</p> <table border="1"><tr><td>R143 16K5R3F</td><td>R142 49K9R3F</td></tr></table> <p>Tj (min) = 10C</p>	R143 16K5R3F	R142 49K9R3F	<p>VCC = 1.40V (perf mode)/ 1.15V (batt mode)</p> <p>ICC,MAX = 13.71A</p> <p>VCCDPRSLP=0.85V ICC,DSL=2.09A</p> <p>VCCT = 1.25V +/- 5% (static) +/- 9%(transient)</p> <table border="1"><tr><td>R143 2D49KR3</td><td>R142 10KR3F</td></tr></table> <p>ICC =2.7A</p> <p>Tj (min) = 0C</p>	R143 2D49KR3	R142 10KR3F
R143 16K5R3F	R142 49K9R3F					
R143 2D49KR3	R142 10KR3F					
Cu-T	<p>VCC = 1.7V (perf Mode)/ 1.35V (Batt Mode)</p> <p>VCCT = 1.2V +/- 5% Functional at : VCCT = 1.3V (min), 1.365 (max)</p>	<p>VCC = 1.7V (perf Mode)/ 1.35V (Batt Mode)</p> <p>VCCT = 1.25V +/- 5% (static) +/- 9%(transient)</p>				
GMCH	<p>VCC/VTT = 1.2V +/- 5% Functional at : VCC/VTT= 1.3V (min), 1.365V (max)</p>	<p>VCC/ VTT = 1.25V +/- 5%</p>				

## MAX1718 Voltage Setting

D4	D3	D2	D1	D0	Yout (V)
0	0	0	0	0	1.75
0	0	0	0	1	1.70
0	0	0	1	0	1.65
0	0	0	1	1	1.60
0	0	1	0	0	1.55
0	0	1	0	1	1.50
0	0	1	1	0	1.45
0	0	1	1	1	1.40
0	1	0	0	0	1.35
0	1	0	0	1	1.30
0	1	0	1	0	1.25
0	1	0	1	1	1.20
0	1	1	0	0	1.15
0	1	1	0	1	1.10
0	1	1	1	0	1.05
0	1	1	1	1	1.00

Perf for Cu-T

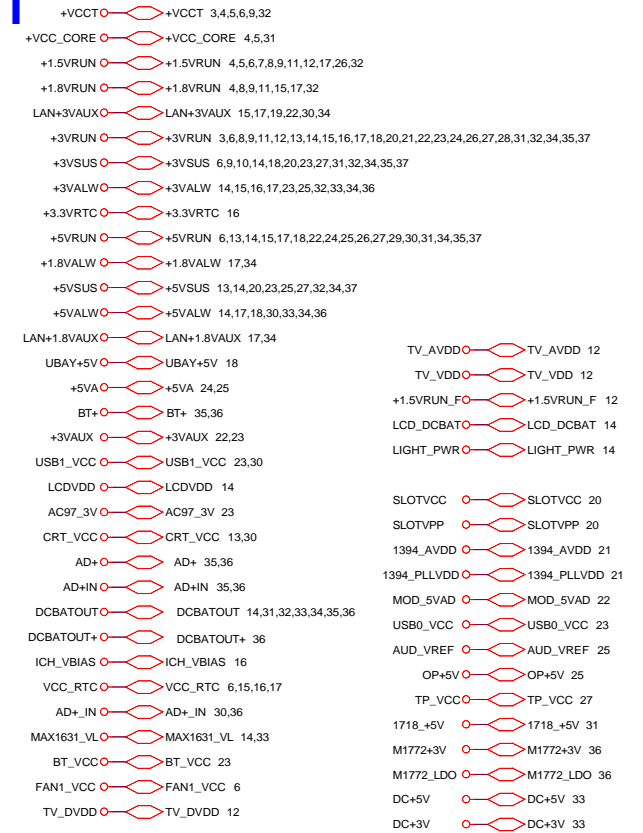
Perf for Tualatin

Batt for Cu-T

Batt for Tualatin

S1	S0	Yout (V)
GND	GND	0.975
GND	REF	0.950
GND	Float	0.925
GND	VCC	0.900
REF	GND	0.875
REF	REF	0.850
REF	Float	0.825
REF	VCC	0.800
Float	GND	0.775
Float	REF	0.750
Float	Float	0.725
Float	VCC	0.700
VCC	GND	0.675
VCC	REF	0.650
VCC	Float	0.625
VCC	VCC	0.600

ZMODE	SUS	Yout Determined by:
GND	GND	Logic Level of D0 - D4
VCC	GND	Impedance of D0 - D4
X	VCC	Logic Level of S0, S1



## PCI TABLE

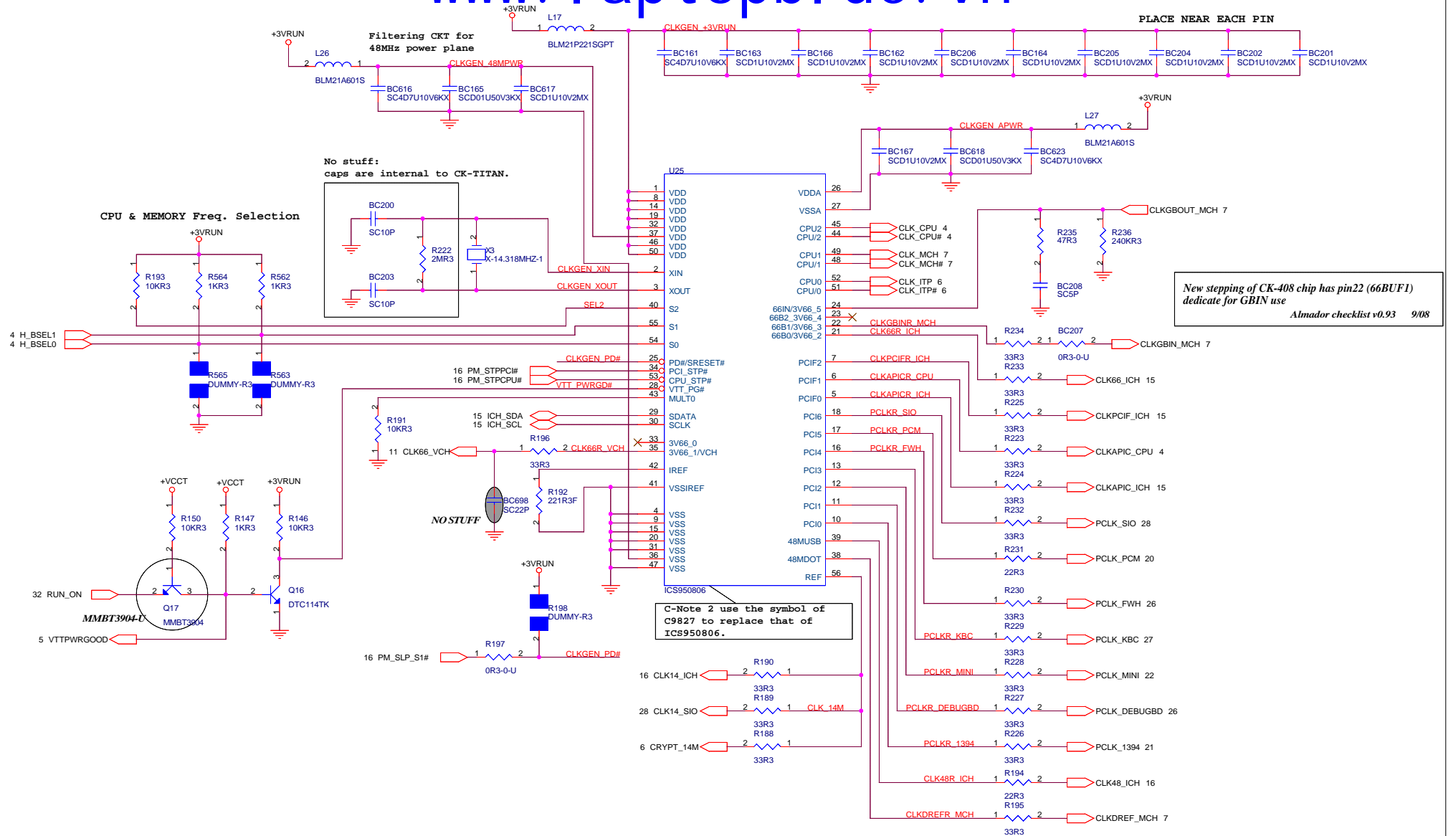
DEVICE	IDSEL	IRQ	REQ# / GNT#
TI 1394	AD19	Auto	REQ2# / GNT2#
MINIPCI SLOT	AD21	C,E	REQ3# / GNT3#
PCMCIA TI1410	AD25	B,D	REQ1# / GNT1#
AGP	AD17(Int.)	A,B	
LAN	AD24(Int.)	E	
USB	AD29	A,D,C	
Hub-to-PCI	AD30		
LPC Bridge/ IDE/AC97/ SMBus	AD15		



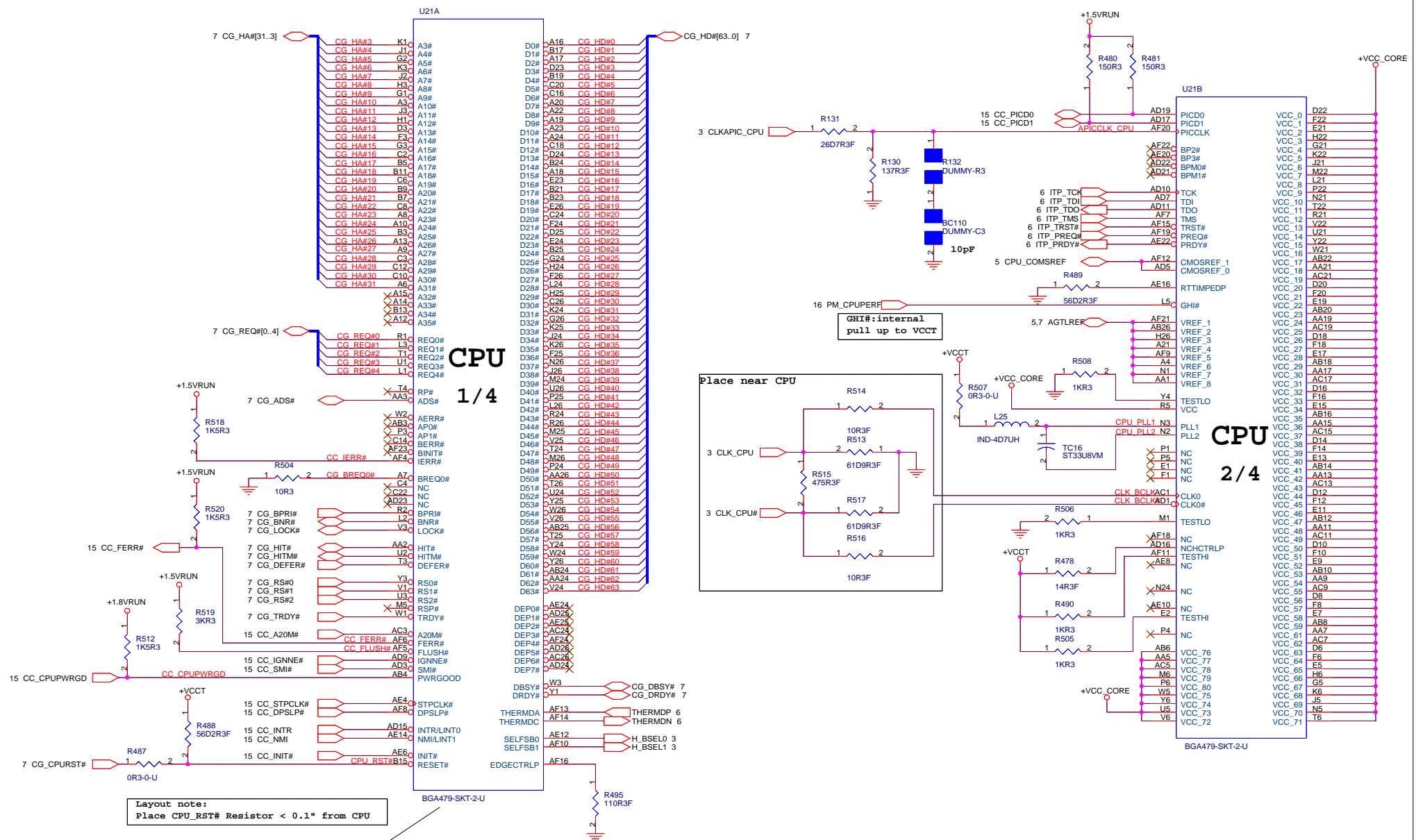
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Title	TABLE OF CONTENT		
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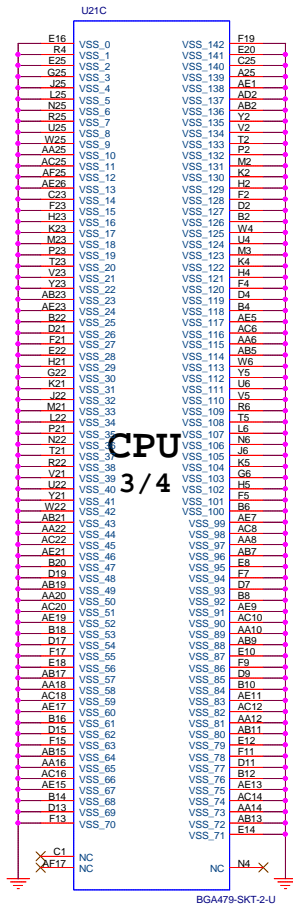




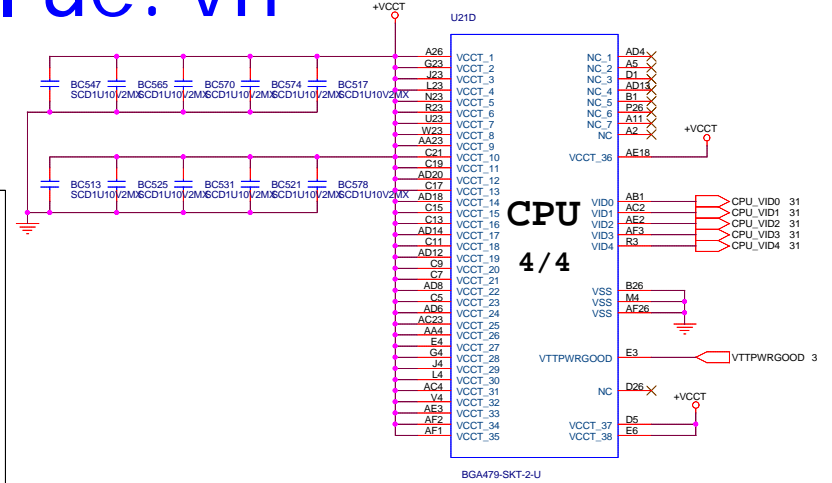
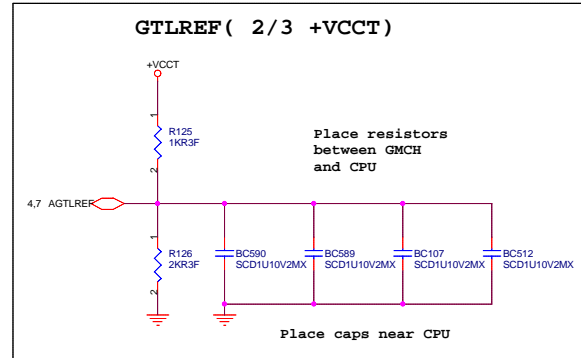
**P/N update to 62.10053.061 (BGA479-SKT-2-U)**  
7/12

AMP : 62.10053.061  
FOXCONN: 62.10055.011

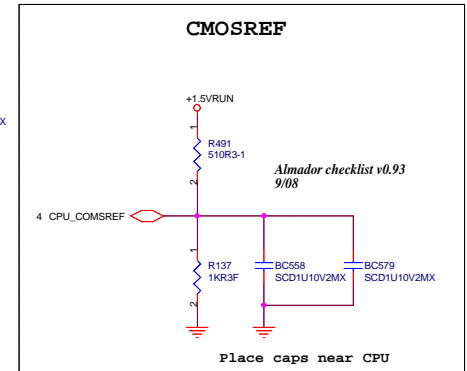
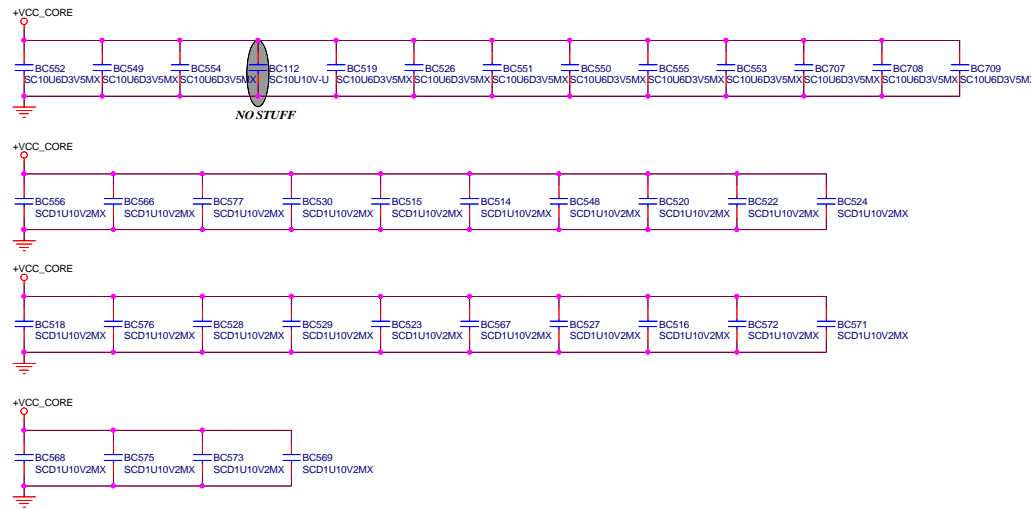




CPU 3/4



CPU 4/4



## Decoupling Recommendation

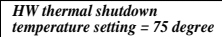
## C-Note 2

## Kenora Ver 0.93

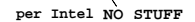
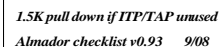
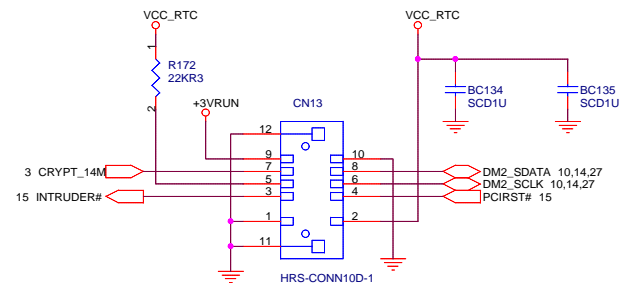
VCC_CORE	Underneath balls on solder side	0.22uF * 24	Use 2-3 vias per pad for reduced inductance during layout	0.1uF * 24	0.47uF * 24
	On the peripheral near balls	10uF / 6.3V * 10	Placement should be near processor for all	10uF / 10V * 10	10uF / 6.3V * 10 + 6 * NS
	Bulk Caps			220uF / 2.5V * 7	150uF / 4V * 12 + 2 * NS
VCCT	Place close to processor for all	1uF * 10	Use 2 vias per pad for reduced inductance during layout	0.1uF * 10	1uF * 10 + 2 * NS
	Bulk Caps			220uF / 2.5V * 2	150uF / 4V * 5 + 1 * NS

Almador-M Checklist Ver. 0.93 9/08

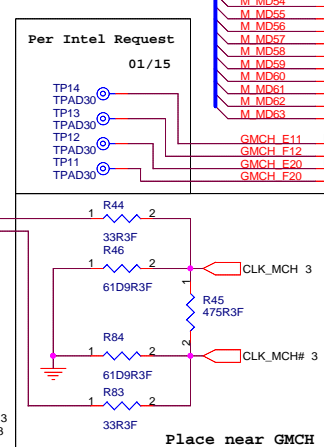




## Crypto Card CONN









Route 0.15"/±-50mil trace

Almador-M A3 stepping Design Guideline Update

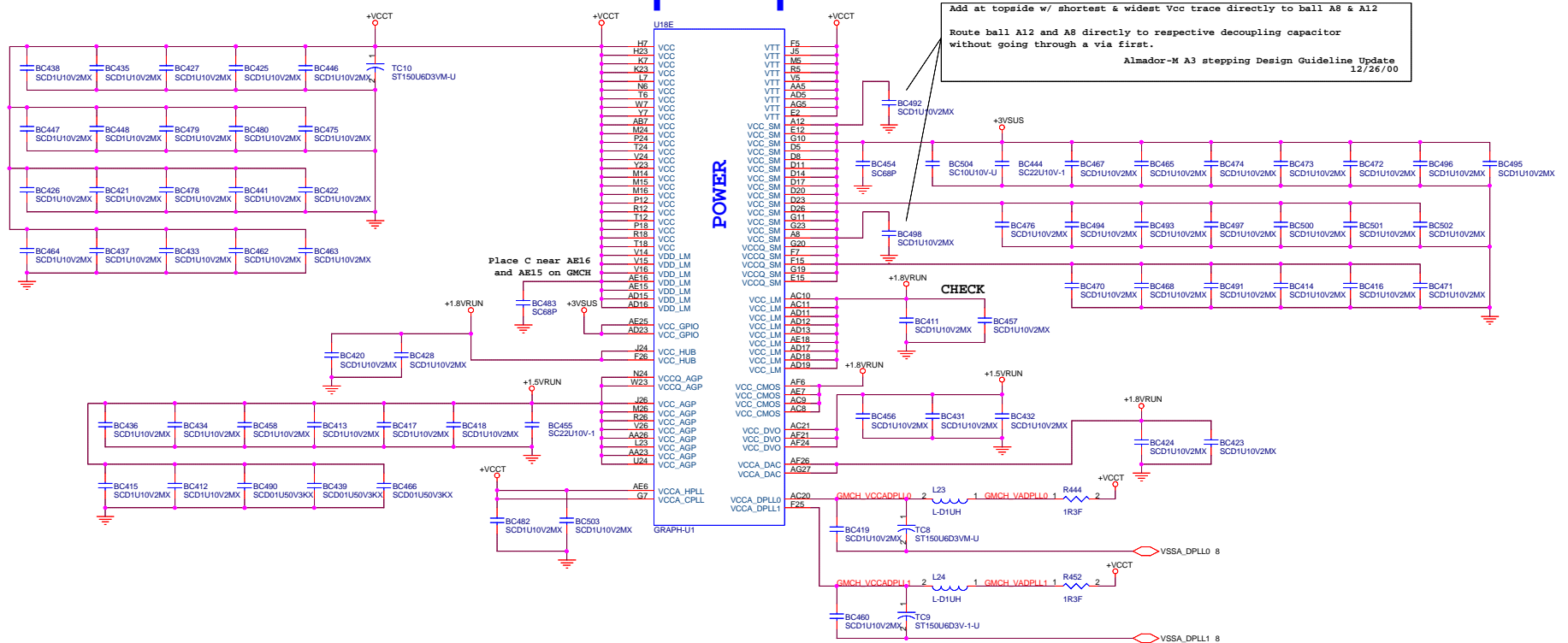
12/26/00

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Title				
<b>GMCH(1/3)</b>				
Size A3	Document Number			Rev
<b>C-Note 2</b>				<b>-3</b>
Date:	Friday, January 11, 2002	Sheet	7 of 3/	



Title			
GMCH(2/3)			
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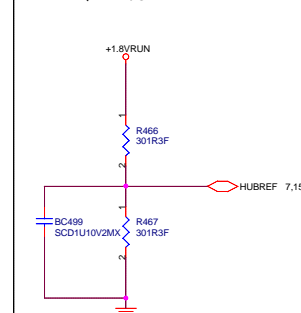


## Decoupling Recommendation

V1.2S_GMCH	Decoupling Caps	0.1uF * 10	Distribute as close as possible to GMCH-M processor Quadrant	0.1uF * 20	0.1uF * 20
	Bulk Caps	10uF * 1		150uF / 6.3V * 2	150uF / 4V * 5 + 1 * NS
V1.2S_GMCHCORE	Decoupling Caps	68pF * 1	Close to VDD_LM, near pins AE15 and AE16 on Almador	68pF * 1	68pF * 1
		0.1uF * 10		220uF / 2.5V * 2	0.1uF * 28
	Bulk Caps	10uF * 1			150uF / 4V * 6
V1.5S_GMCH	Decoupling Caps	0.1uF * 9	Distribute as close as possible to GMCH-M AGP/DVO Quadrant	0.1uF * 11 0.01uF * 3 10uF / 10V * 1	0.1uF * 9
		82pF * 4			82pF * 4
	Bulk Caps			22uF / 10V * 1	22uF / 20V * 1
V1.8S_GMCH	Decoupling Caps	0.1uF * 4 + 2	Distribute as close as possible to GMCH-M Local Memory Quadrant	0.1uF * 6	0.1uF * 4 + 2
		82pF * 2	Additional 4* 0.1uF shall be distributed as close as possible to VCCPCPMOS_LM		0.01uF * 2 82pF * 2 22uF / 20V * 2
	Bulk Caps				68uF / 10V * 5
V3_GMCH	Decoupling Caps	0.1uF * 12 + 2	Distribute as close as possible to GMCH-M System Memory Quadrant	0.1uF * 20+2 22uF 10V * 1 10uF 10V * 1 82pF * 1	0.1uF * 12 + 2 82pF * 4 22uF / 20V * 2
		82pF * 4	Additional 4* 0.1uF shall be distributed as close as possible to IO Quadrant		
	Bulk Caps				

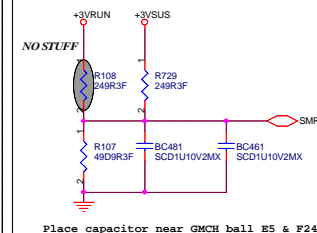
## C-Note 2      Kenora Ver 0.93

HUB INTERFACE REF  
1/2\*1.8V



Layout Note:  
Place divider pair in middle of bus.  
Place capacitors near GMCH.

SYSTEM MEMORY  
REF 0.55V



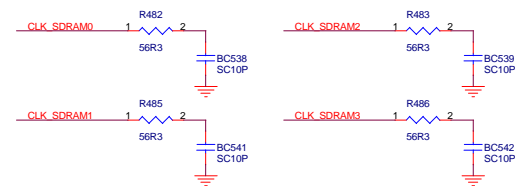
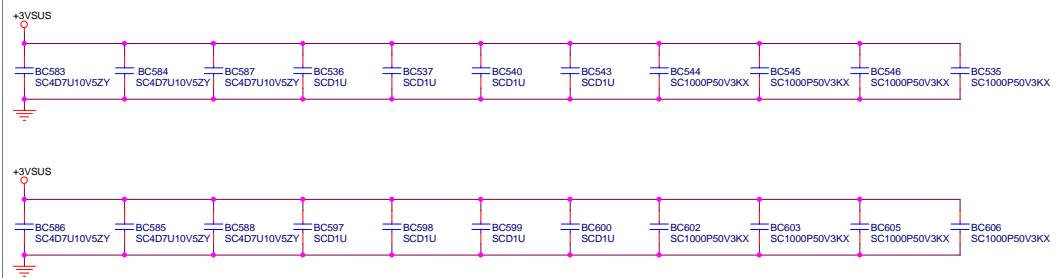
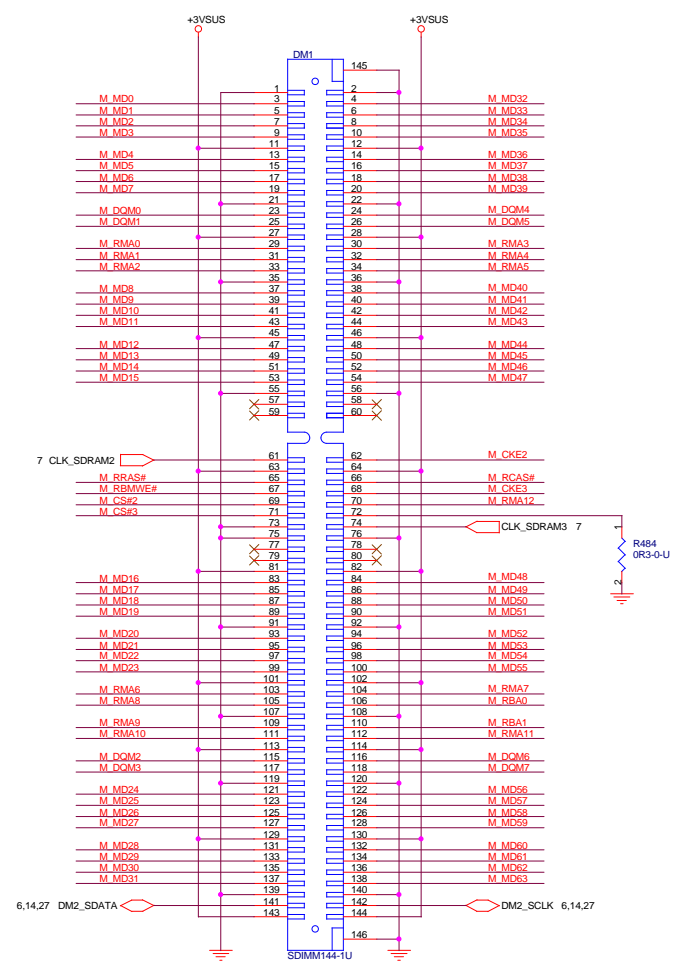
Place capacitor near GMCH ball E5 & F24.



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Title			
GMCH(3/3)			
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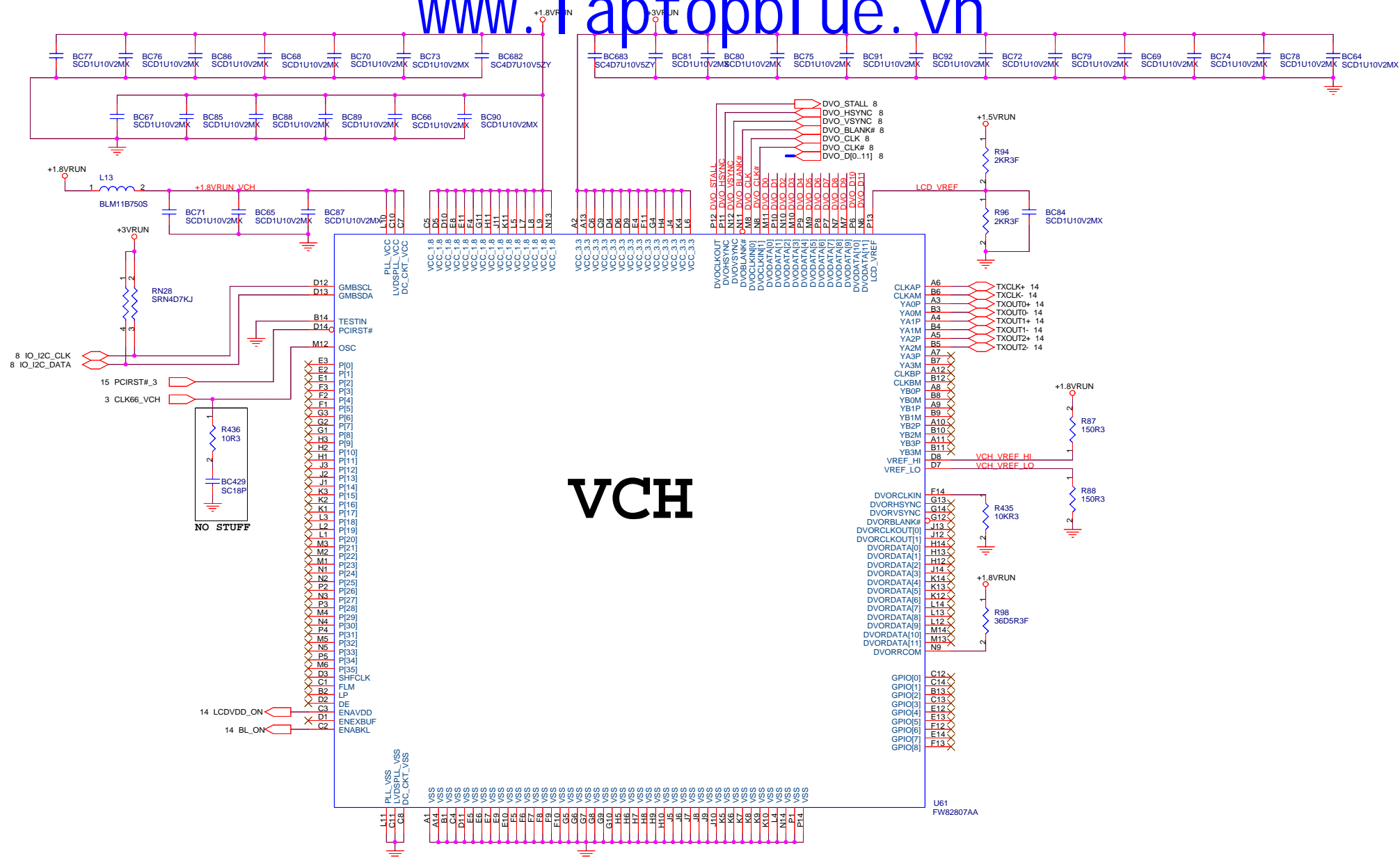




SDRAM clock AC terminations change from 33 Ohm 22p to 56 Ohm 10p.

12/14/00

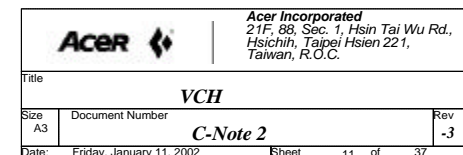




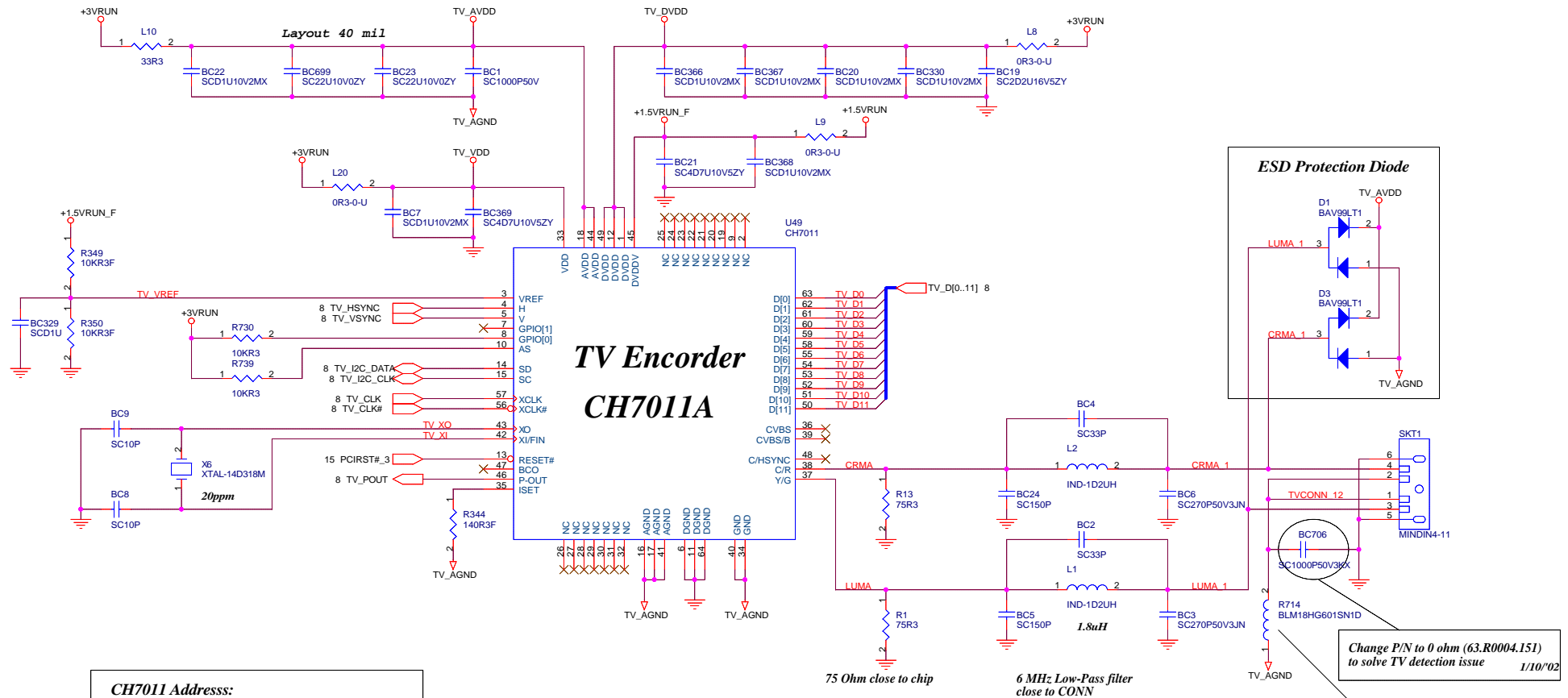
## Strapping Options

GPIO[5:2]	10 - 4.7K Ohm	Can be used for panel ID select. Default state is GPI w/ int. weak pull down.
GPIO6	10 - 4.7K Ohm	For normal VCH operation pin has to be read as low. Default state is GPI w/ int. weak pull down.
GPIO[8:7]	10 - 4.7K Ohm	Used for GMBus base address select. Default state is GPI w/ int. weak pull down.

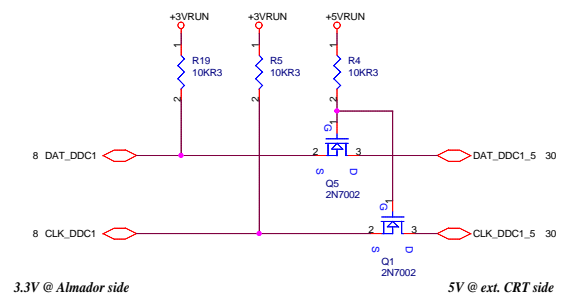
Almador checklist ver.0.93



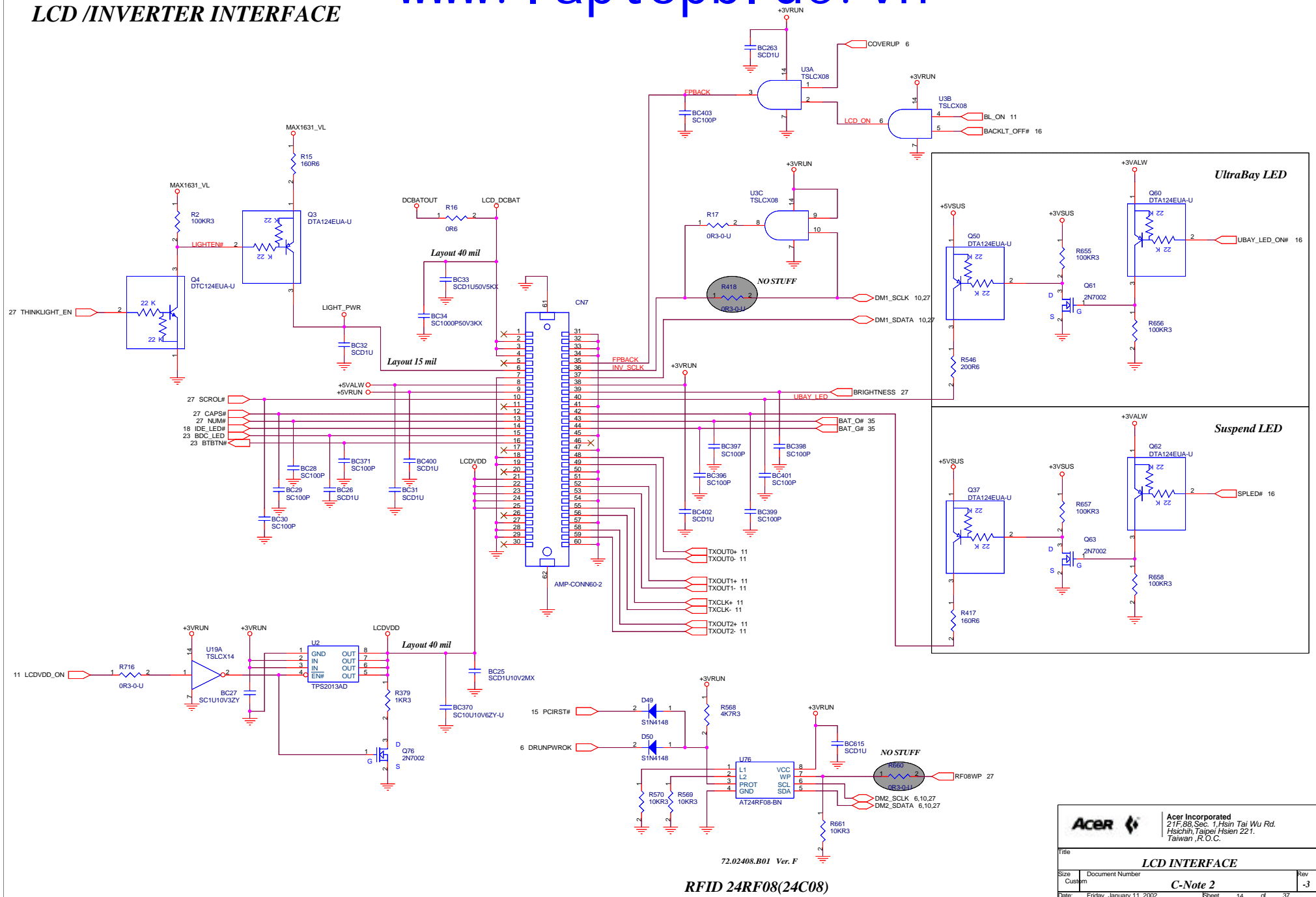






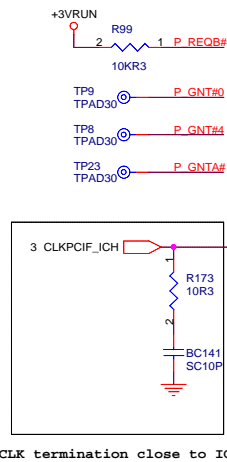
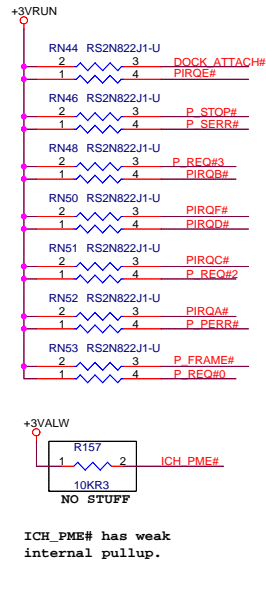






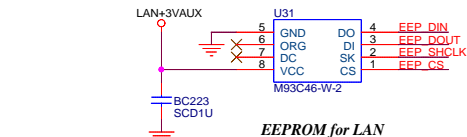


## PCI I/F Pullups

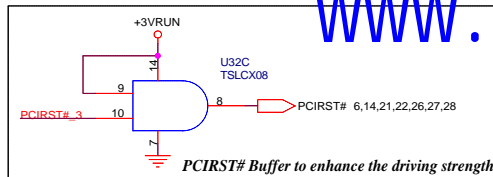


CLK termination close to ICH

**Part Number Change to 71.0ICH3.M03**

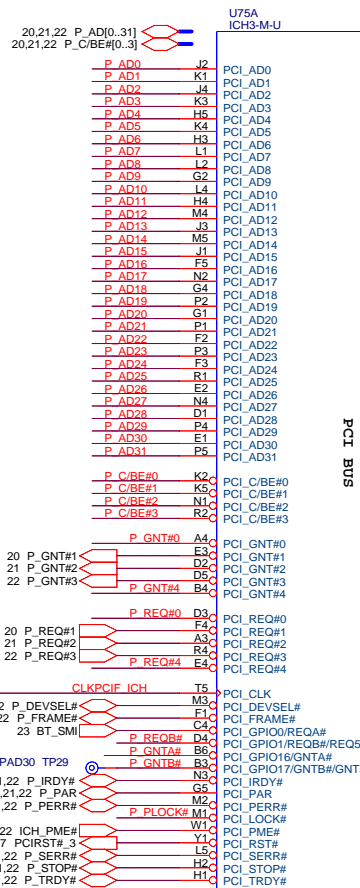
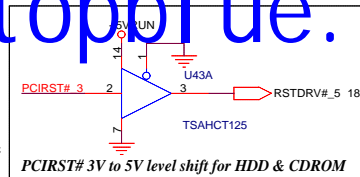
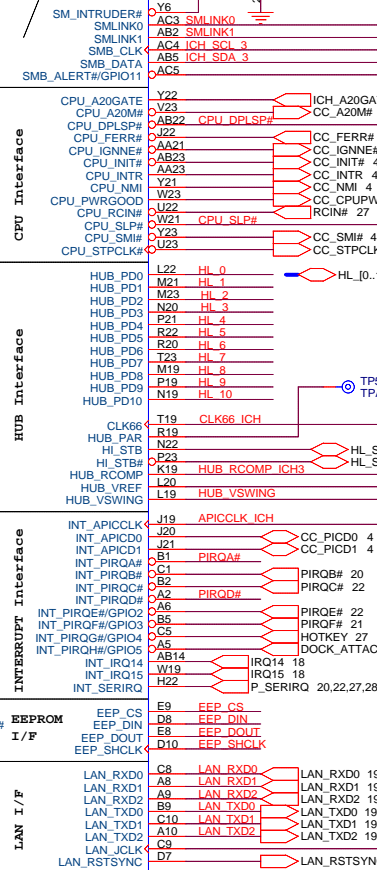


### EEPROM for LAN

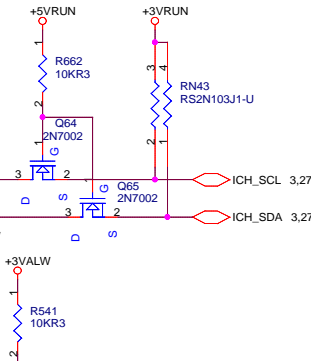


## ICH3-M

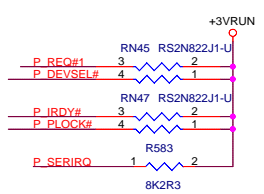
PART A

System  
Management  
I/F

### PCIRST# 3V to 5V level shift for HDD & CDROM



## Interrupt I/F Pullups



## HUB INTERFACE LAYOUT

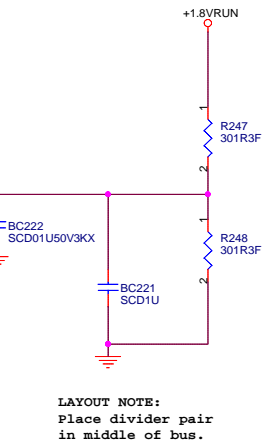
Route signals with 5/20 trace/space routing.  
Signals must match +/- 0.1" of HUB\_STB/STB# signals.

Kodiak Ver. 0.7



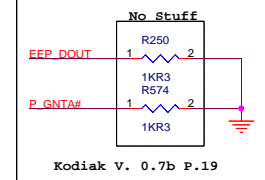
PLACE RCOMP resistor within 0.5  
of ICH pad using a thick trace  
RCOMP should be  $\frac{2}{3}$   
board impedance

## HUB I/F VSWING VOLTAGE



LAYOUT NOTE:  
Place divider pair  
in middle of bus.

## H/W Strapping



Kodiak V. 0.7b P.19



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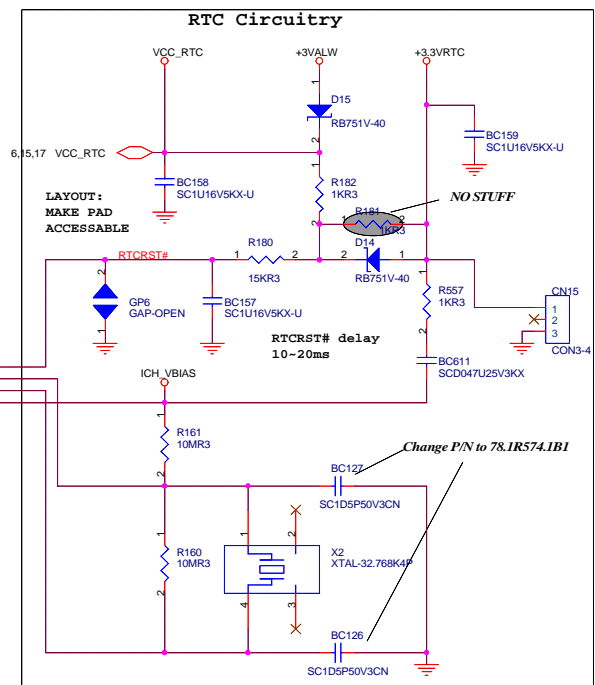
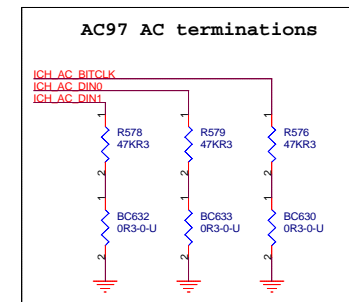
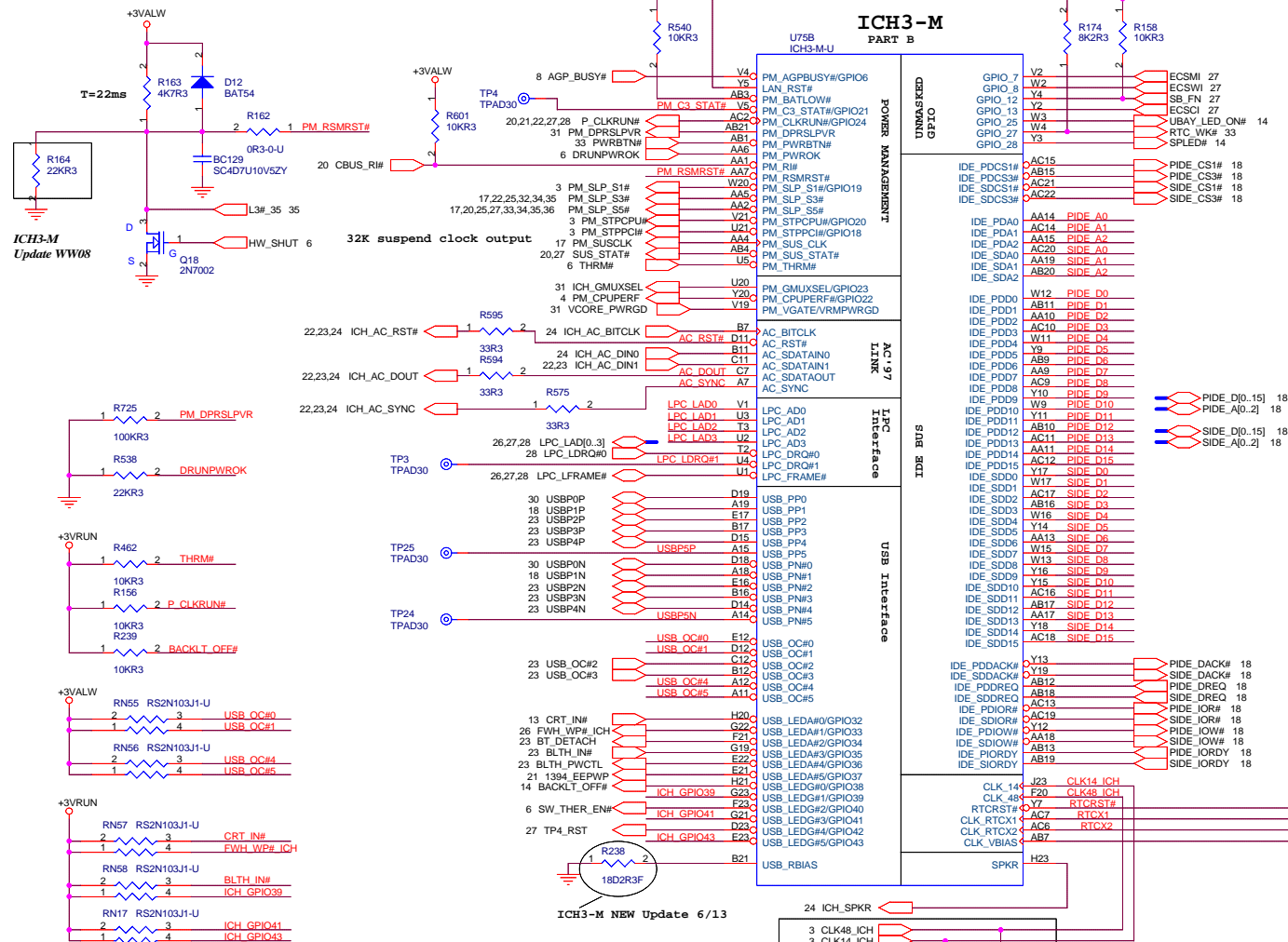
Title	<i>ICH3-M(1/3) PCI,HUBLINK,SM,CPU,INT</i>
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Size	Document Number	Rev
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A3	<i>C-Note 2</i>	.3
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Date: Friday, January 11, 2002 Sheet 15 of 37

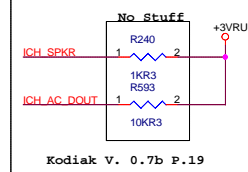




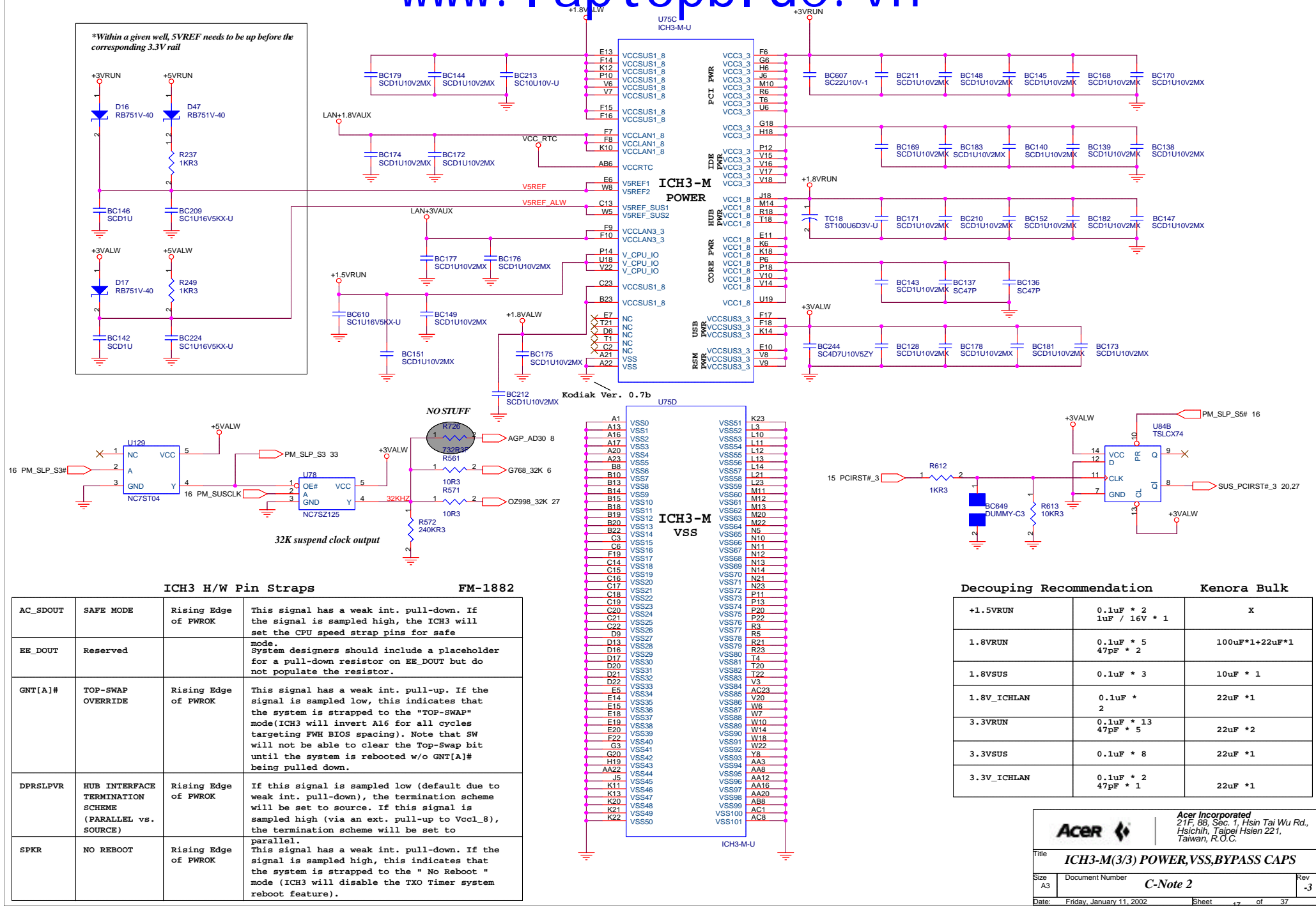
### ICH3 Integrated Pull-up and Pull-down Resistors

EE_DIN , EE_DOUT, LDRQ[1:0] , PME# GNT[B:A]#/GNT[5]#/GPIO[17:16] , LAD[3:0]#/FWH[3:0]# , PWRBTN#	ICH3 internal 24K pull-ups
LAN_RXD[2:0]	ICH3 internal 9K pull-ups
AC_BITCLK, AC_SDIN[0], AC_SDOUT, AC_SDIN[1]/GPIO[9], AC_SYNC,	ICH3 internal 20K pull-downs
SPKR	ICH3 internal 24K pull-downs
PDD[7]/SDD[7], PDDREQ / SDDREQ	ICH3 internal 5.9K pull-downs
DPRSPLVR	ICH3 internal TBD K pull-downs

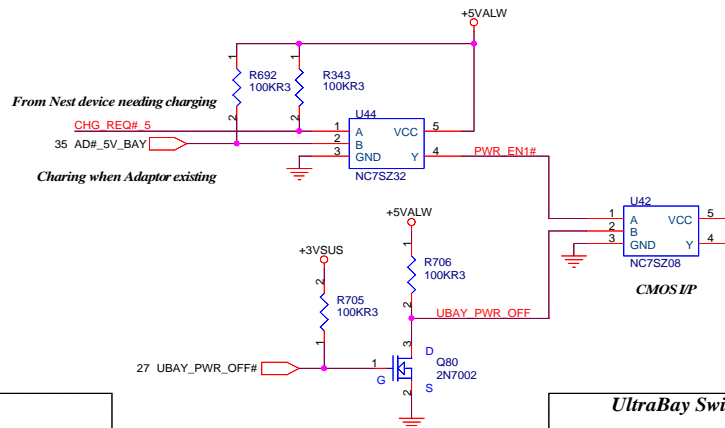
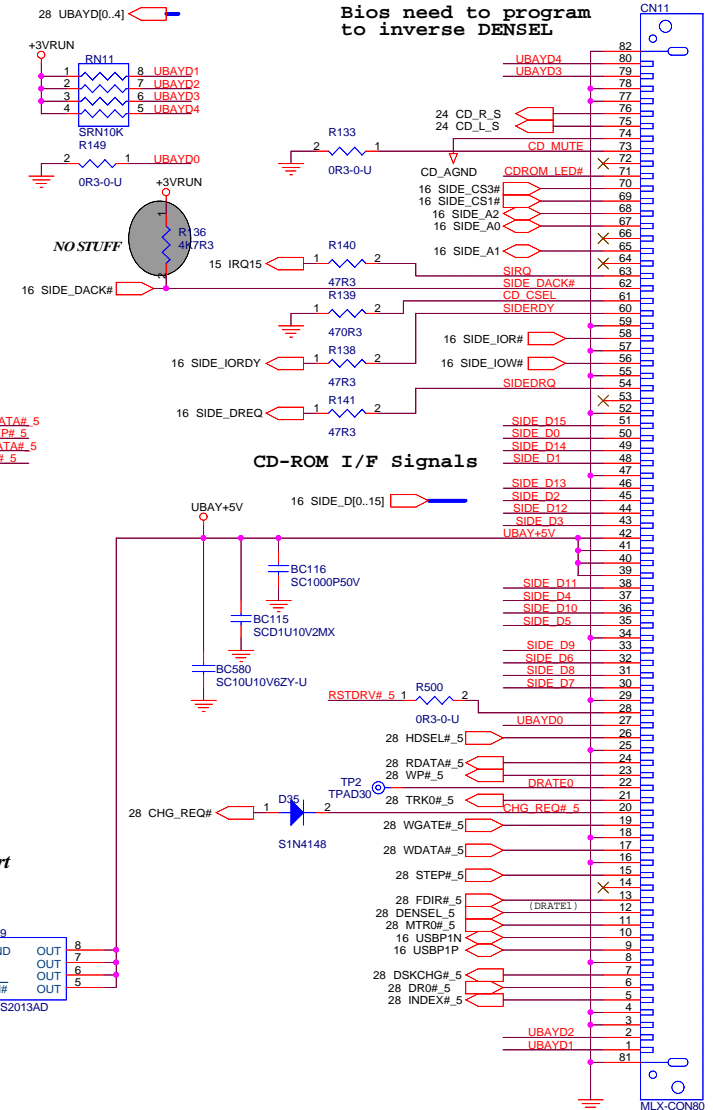
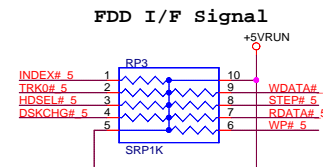
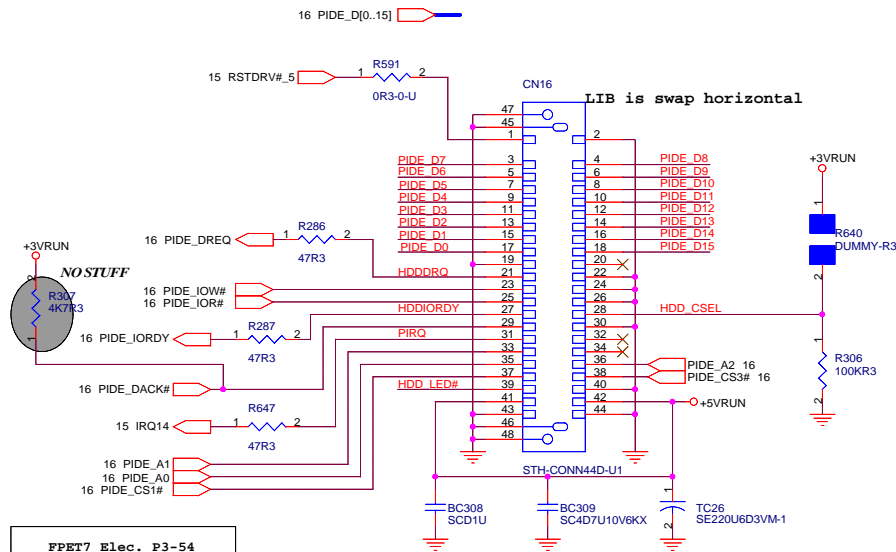
H/W Strapping





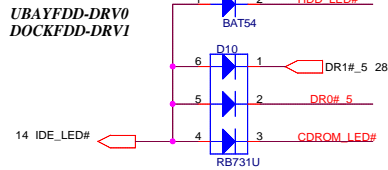
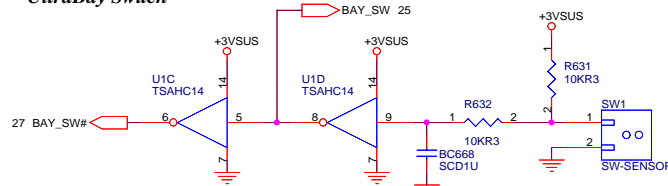




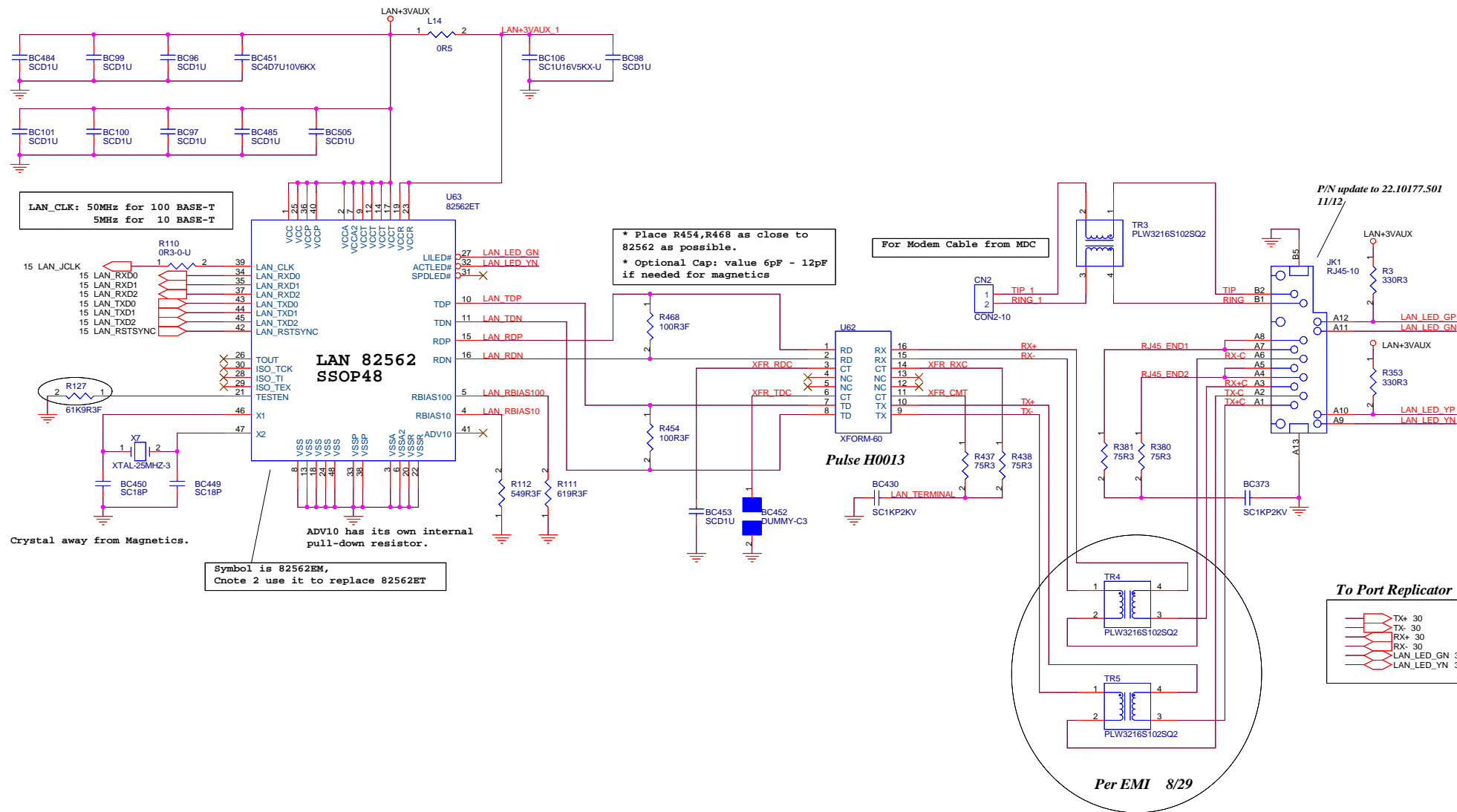


Nest Charging Support

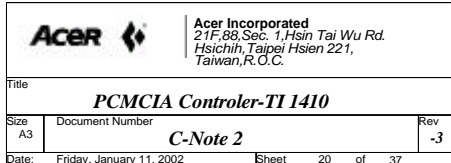
UltraBay Switch



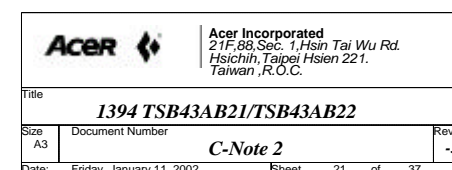




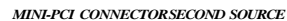









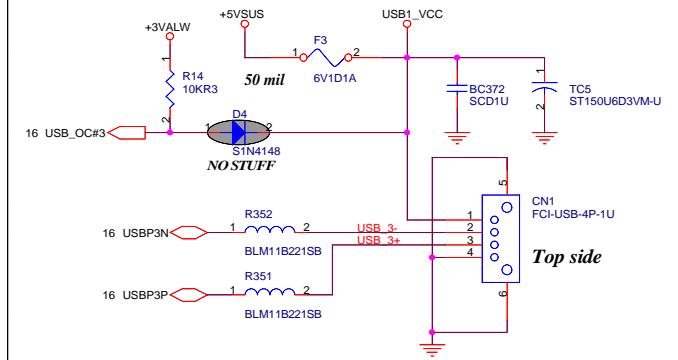
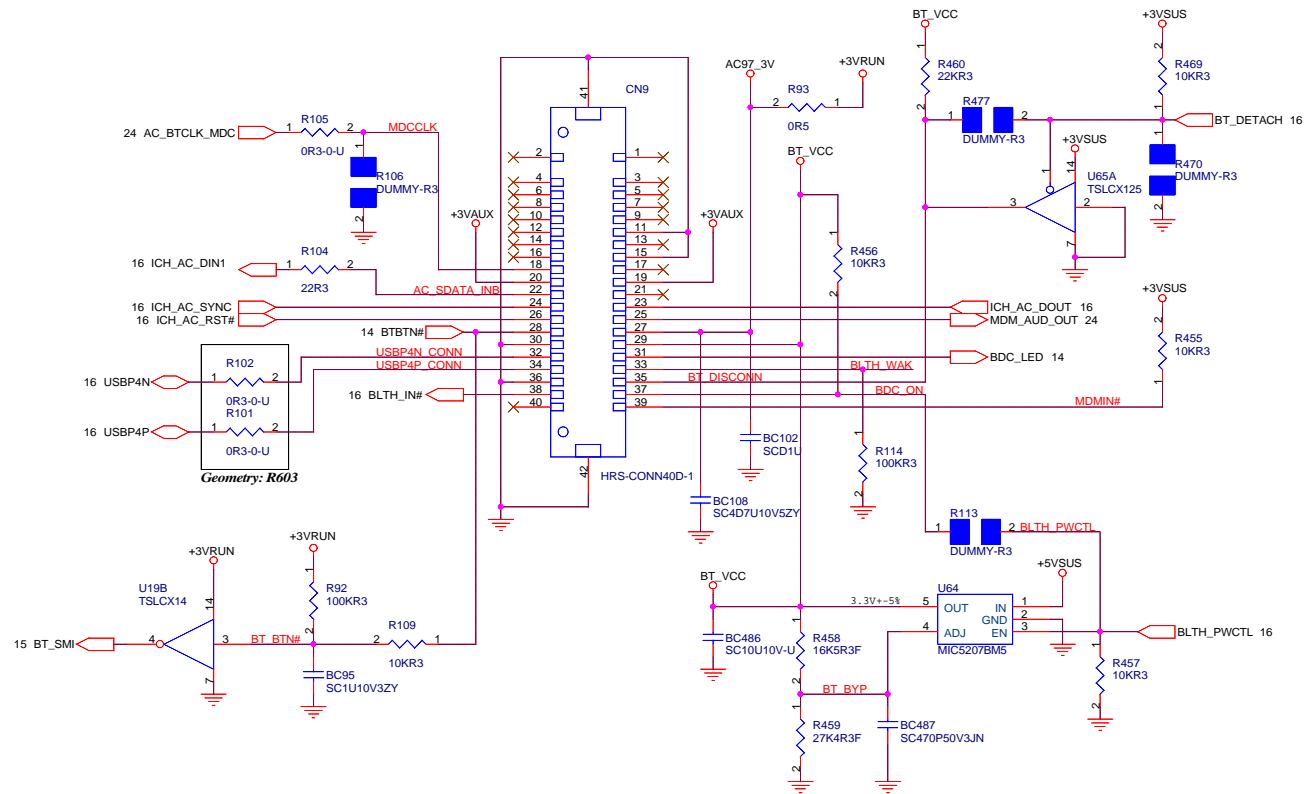




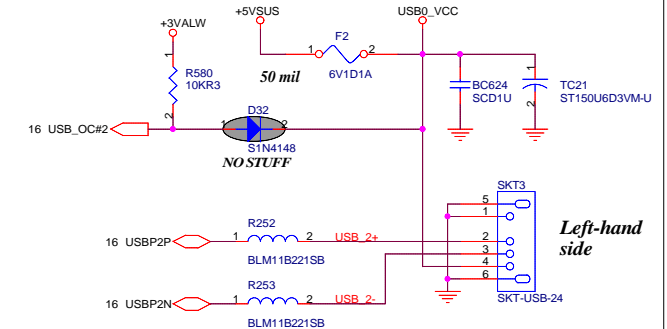
		<b>Acer Incorporated</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd. Hsichih, Taipei Hsien Z21. Taiwan, R.O.C.	
Title _____			
<b><i>Mini PCI SOCKET &amp; MDC MODEM</i></b>			
Size A3	Document Number	<b><i>C-Note 2</i></b>	
Date:	Friday, January 11, 2002	Sheet	22 of 37 Rev -3



## *CDC Connector*

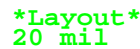
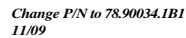


## USB PORT

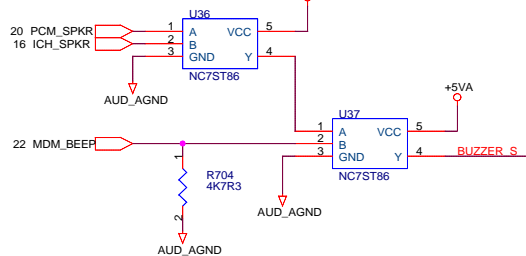




**\*Layout\***  
**20 mil**

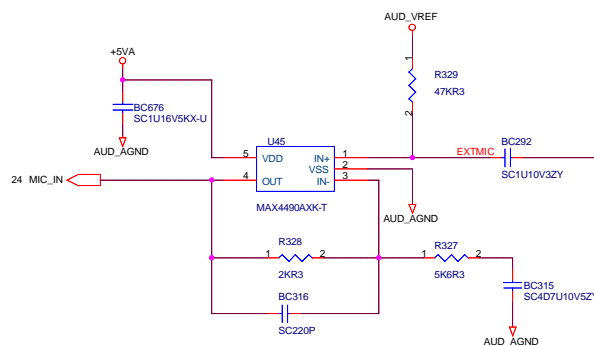


```
*Layout*
locate near audio moat opening
6 mil
+5VA
```

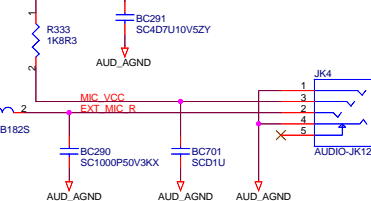
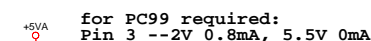




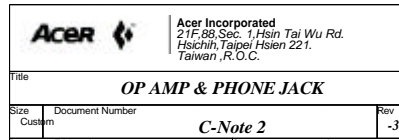
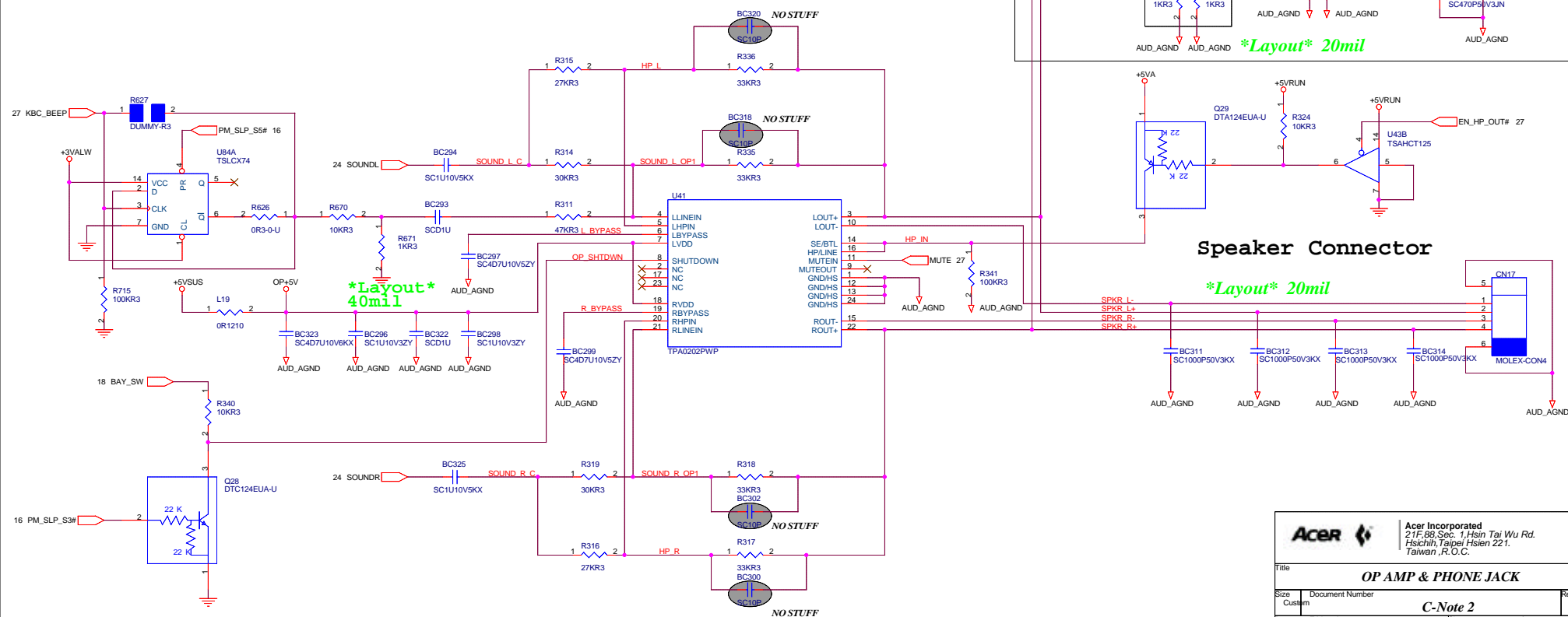
EXT. MICROPHONE IN



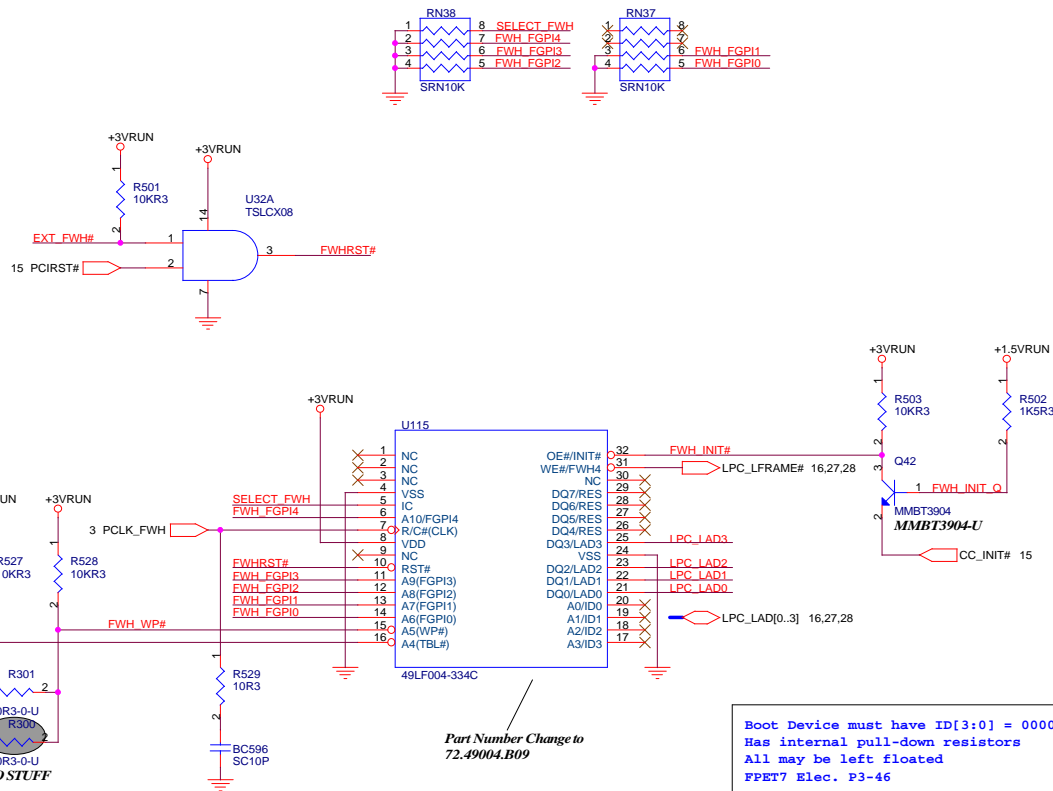
## Microphone Jack



# AUDIO OP AMPLIFIER

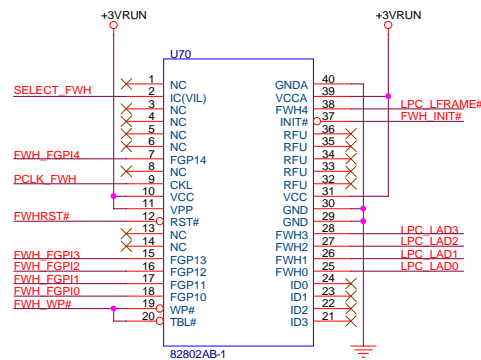






FIRMWARE HUB SECOND SOURCE

SST : 72.49004.B09  
STM : 72.50040.009

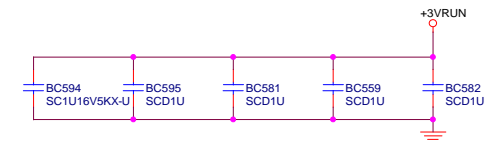
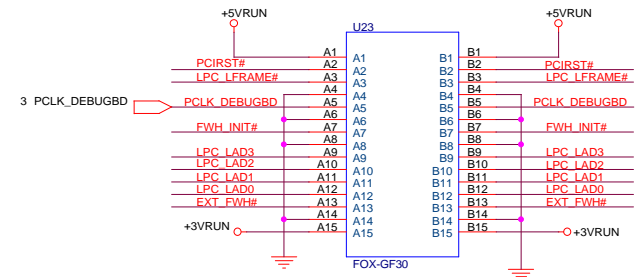


TOP VIEW

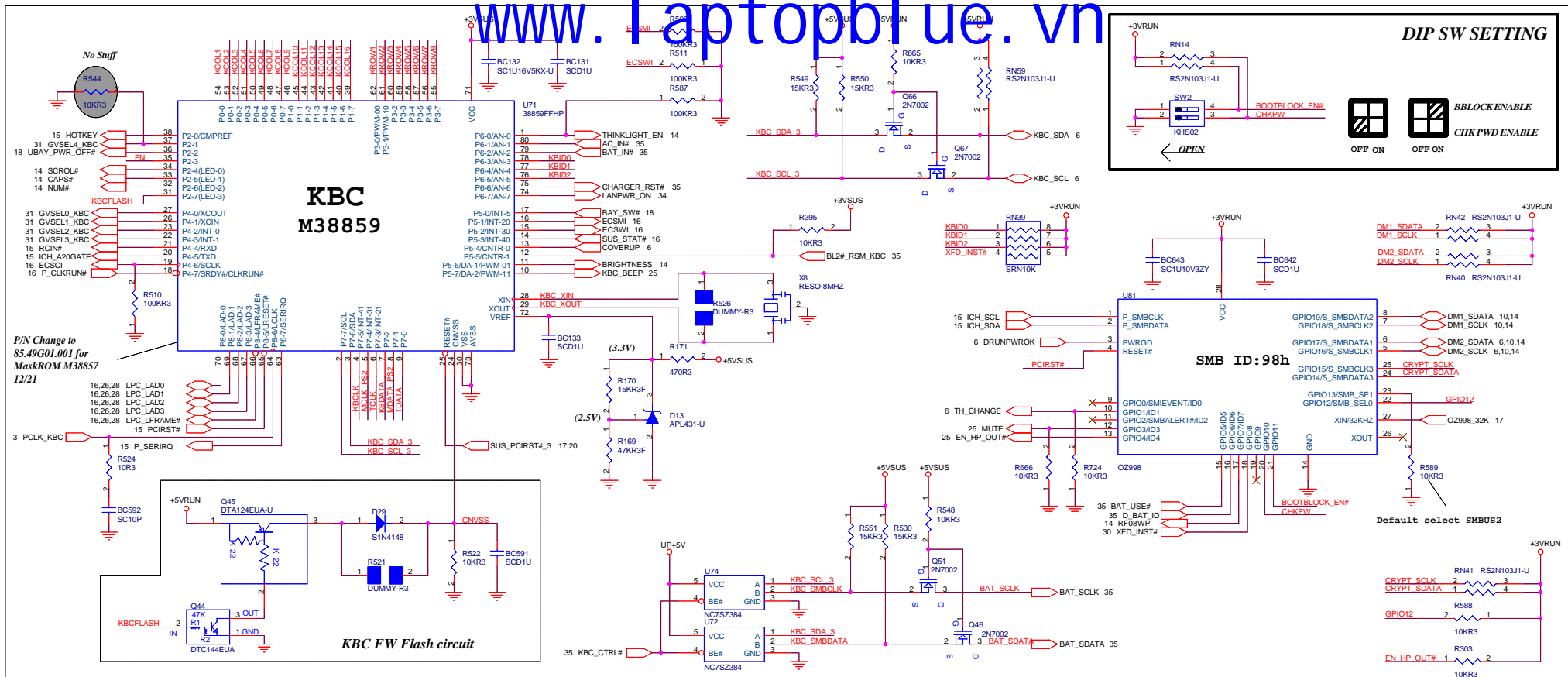
A15 (B1)  
A14 (B2)  
:  
:  
A2 (B14)  
A1 (B15)

(BOTTOM VIEW)

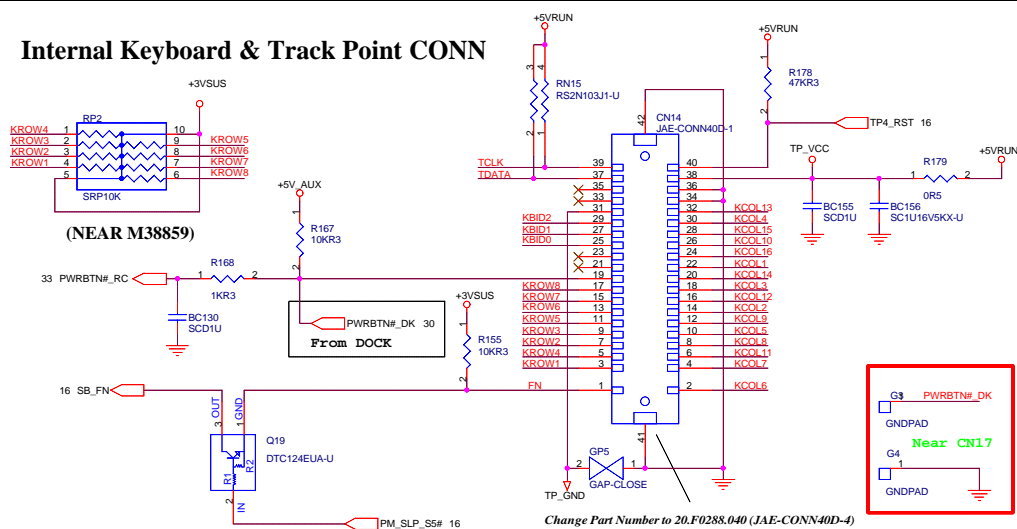
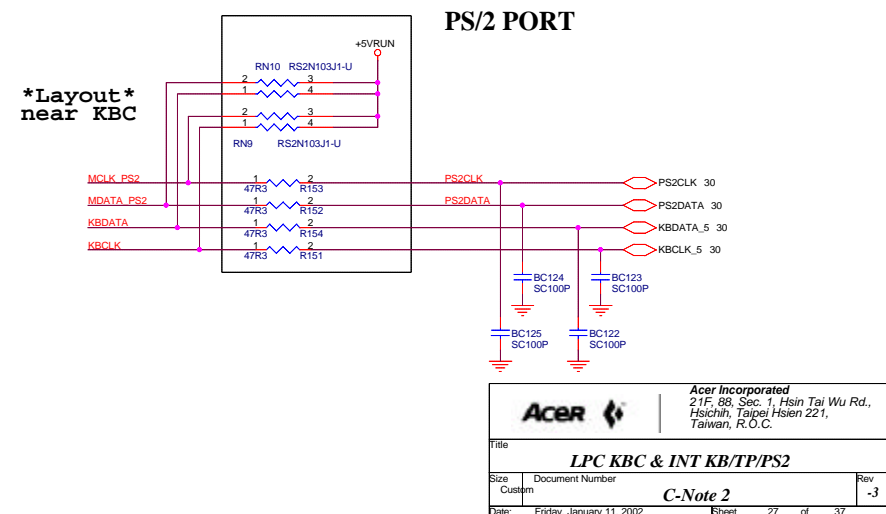
GOLDEN FINGER FOR DEBUG BOARD



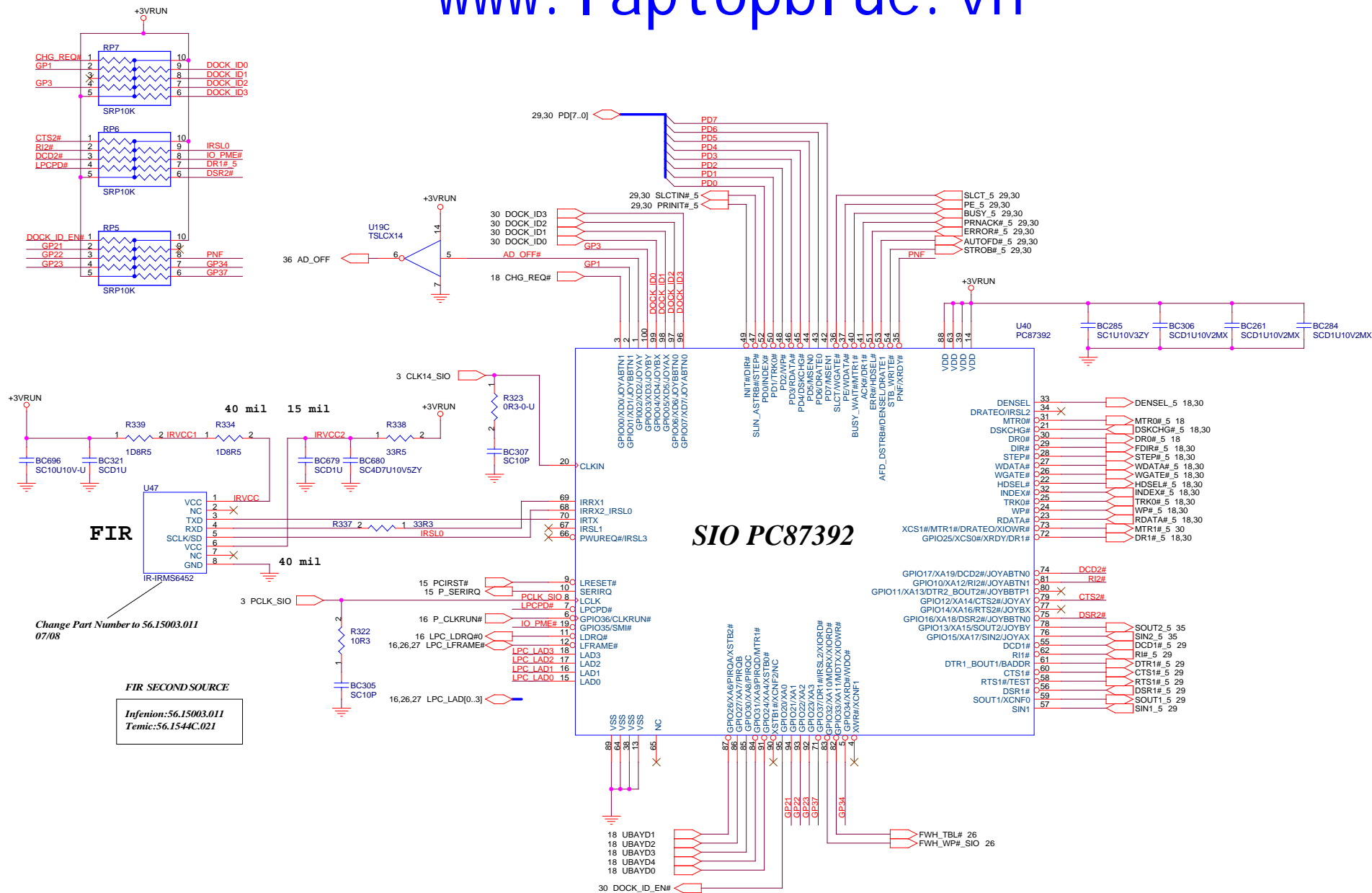




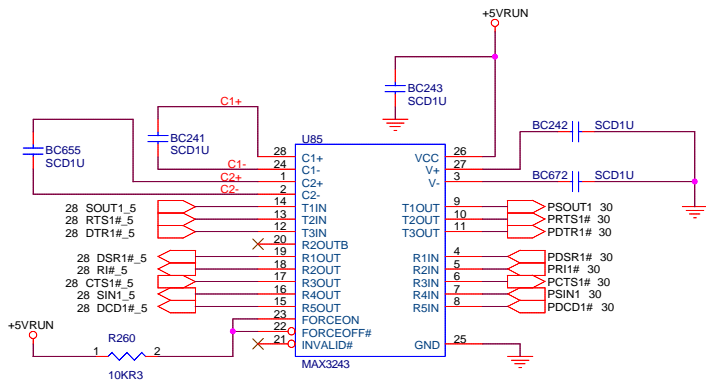
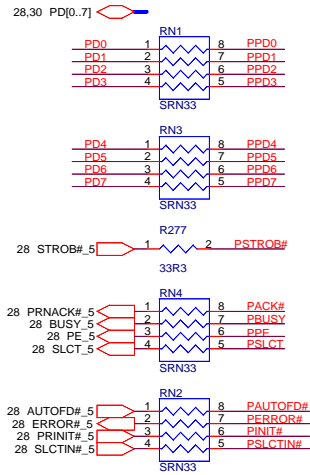
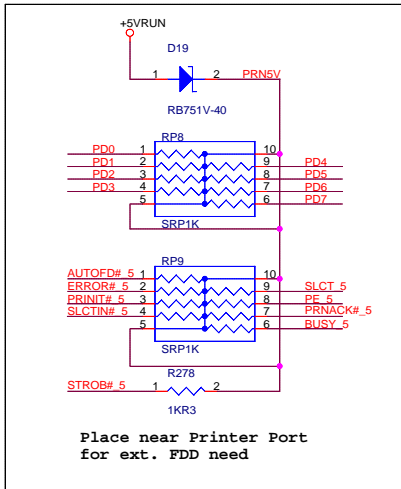
## Internal Keyboard & Track Point CONN

**PS/2 PORT**









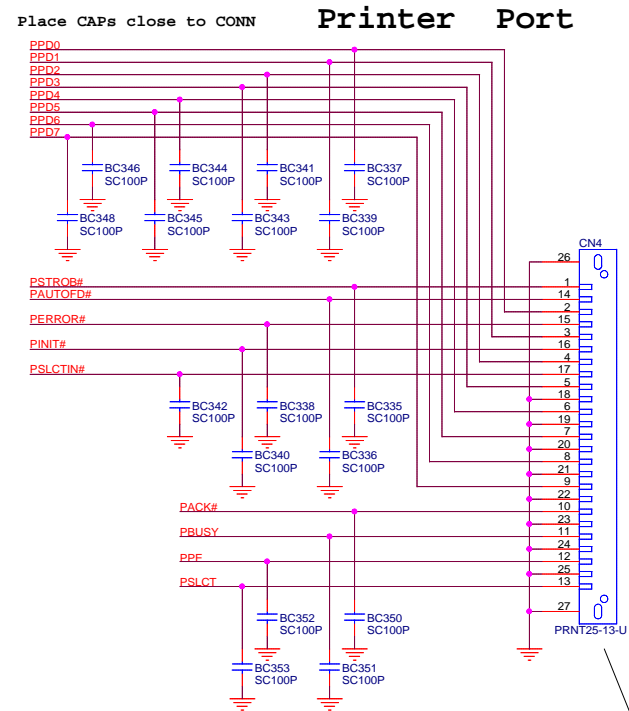
### *RS232 Transceiver*

*RS232 SECOND SOURCE*

```

MAXIM:74.03243.0F9
TI    :74.03243.FF9

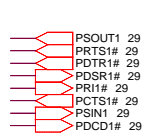
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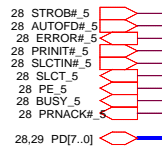
**Change Part Number to 20.B0028.025 (AMP-CON25)**  
07/08



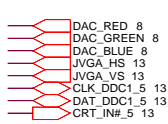
## SERIAL PORT I/F



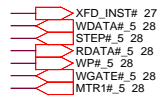
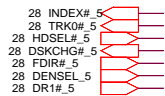
## LPT I/F



## CRT I/F



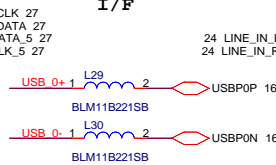
## FDD I/F Signal



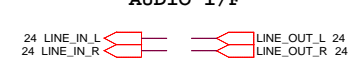
## KBC PS/2 I/F



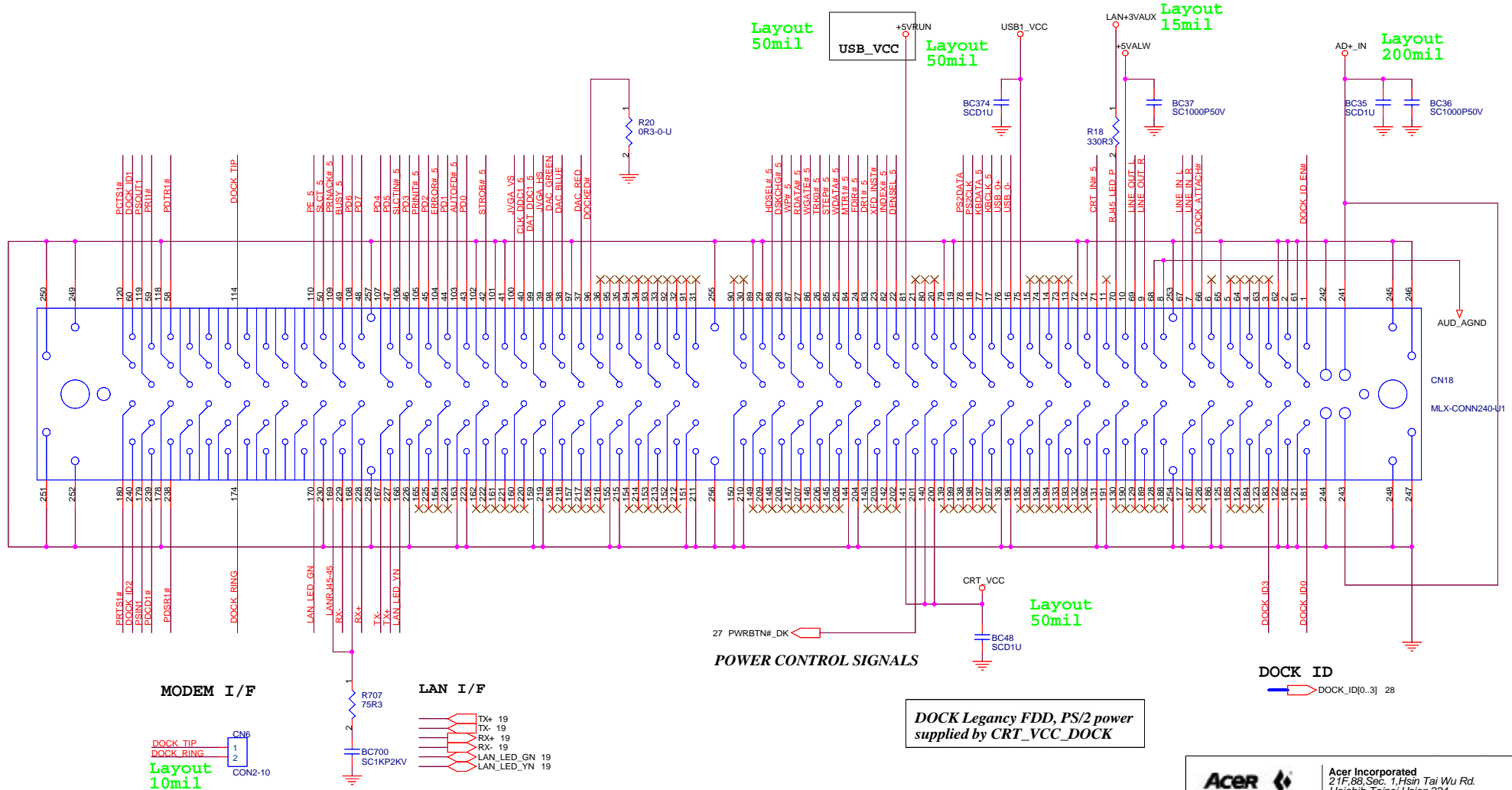
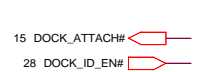
## USB I/F



## AUDIO I/F



## DOCK CONTROL SIGNAL



## POWER CONTROL SIGNALS

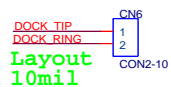
27 PWRBTN#\_DK

DOCK Legacy FDD, PS/2 power supplied by CRT\_VCC\_DOCK

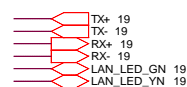
## DOCK ID

DOCK\_ID[0..3] 28

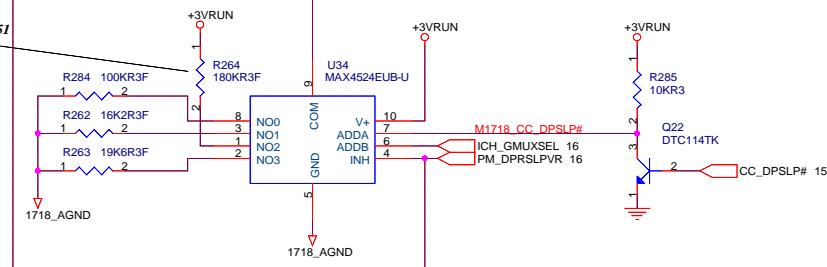
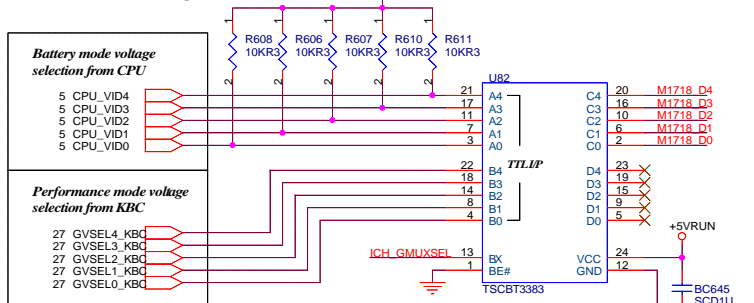
## MODEM I/F



## LAN I/F

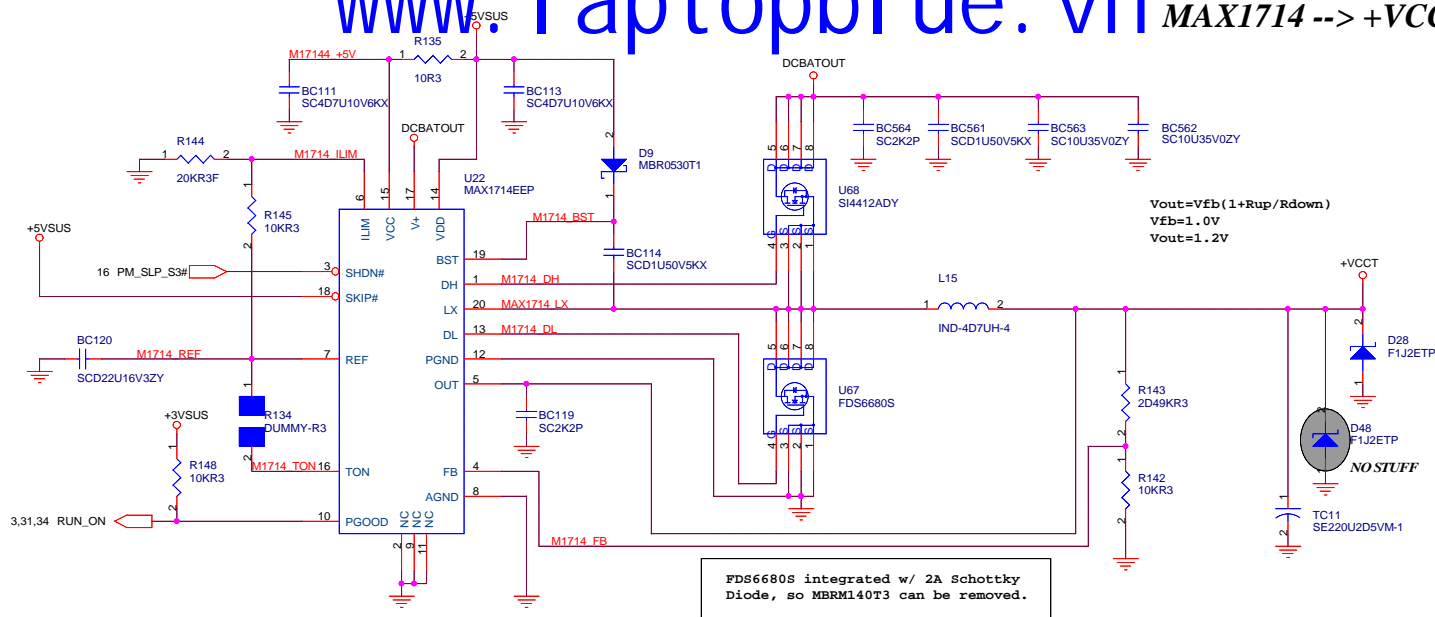




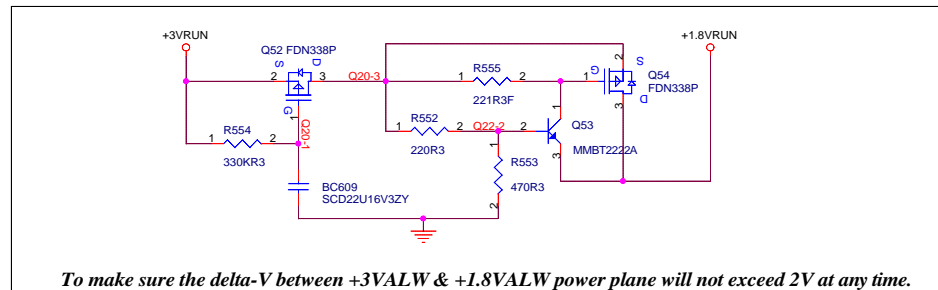
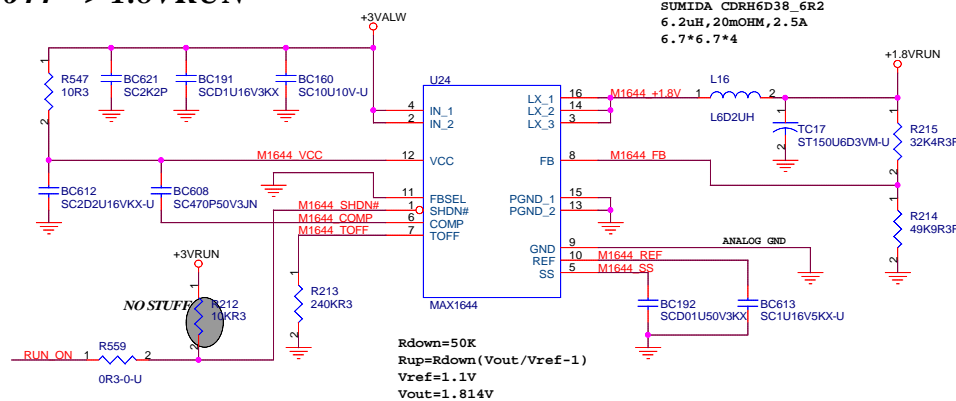


PM_DPSLSPVR	CC_DPSLP#	ICH_GMUXSEL	Voffset
1	X	X	0mV
0	0	0	-59mV
0	0	1	-52mV
0	1	0	-29mV
0	1	1	-3mV

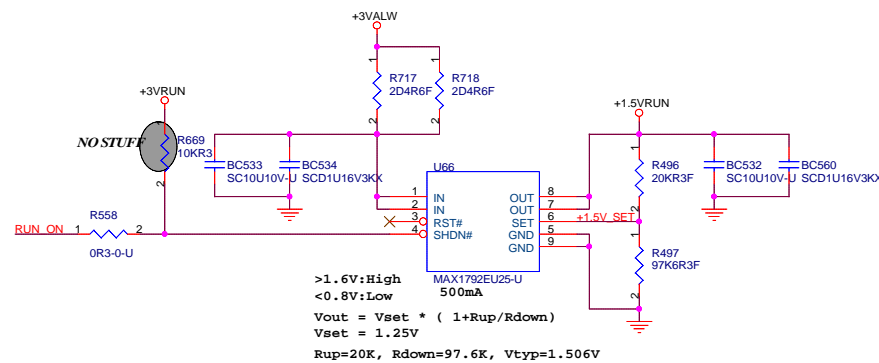




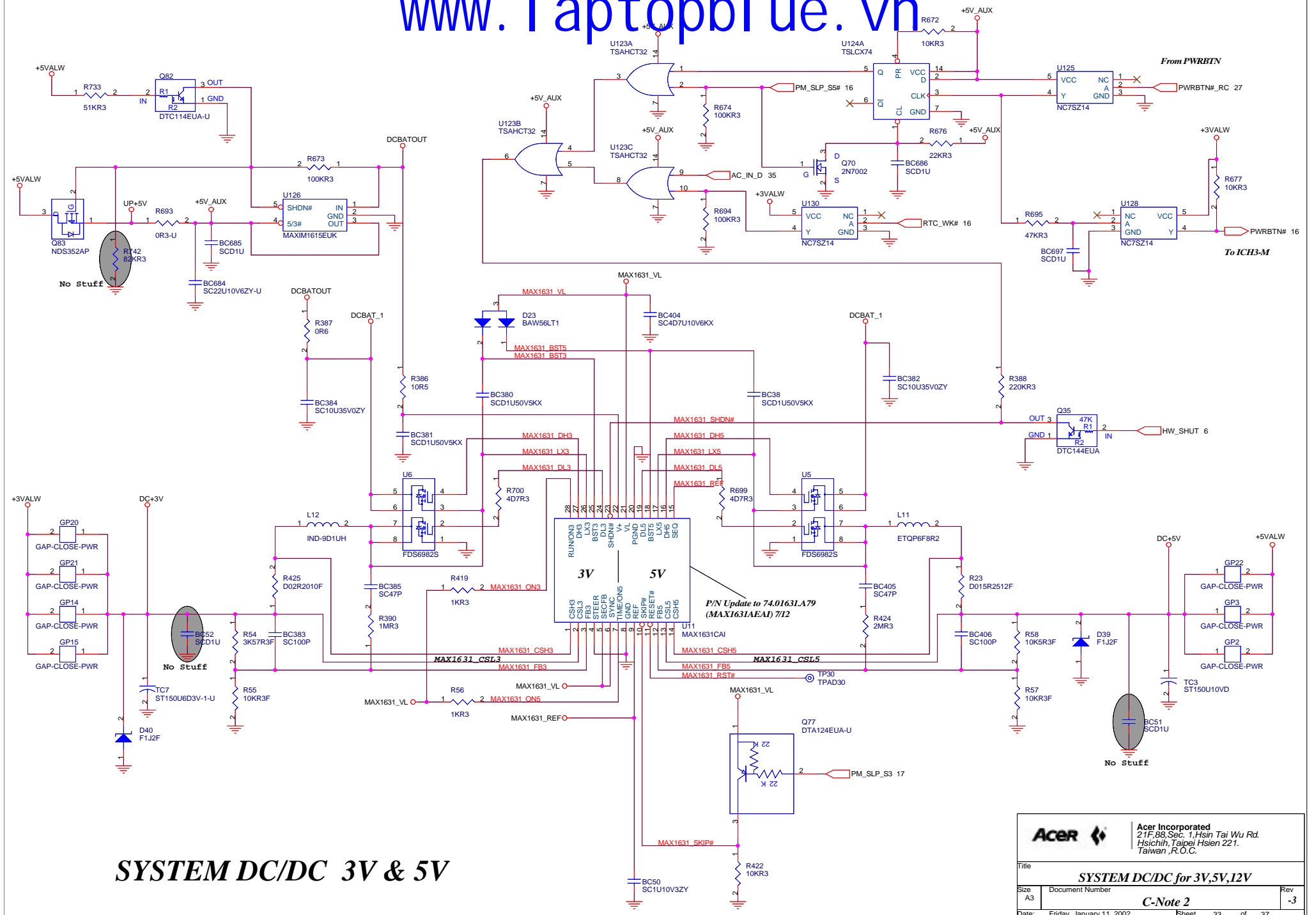
## MAX1644 --> 1.8VRUN



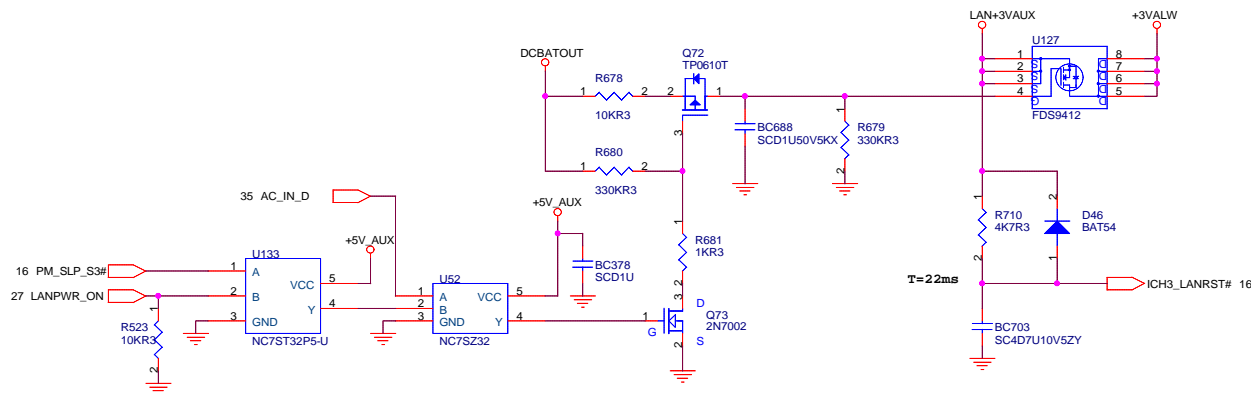
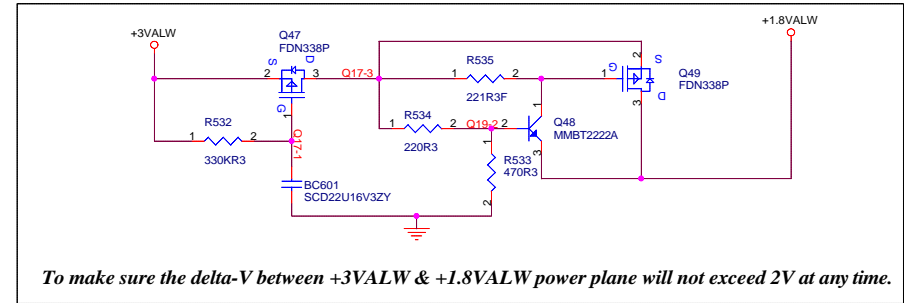
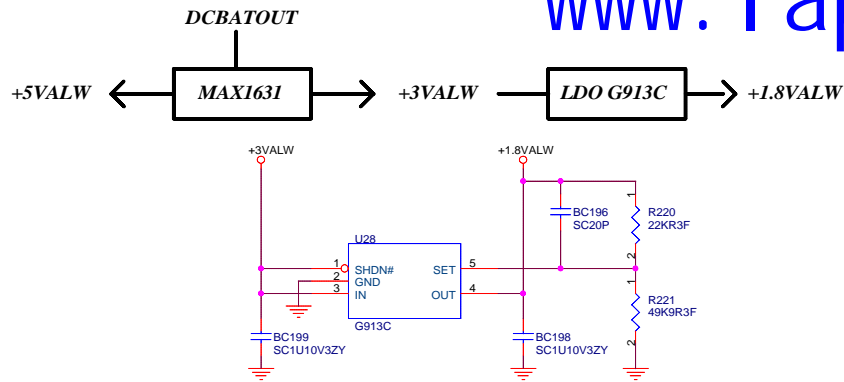
## MAX1792 --> 1.5VRUN





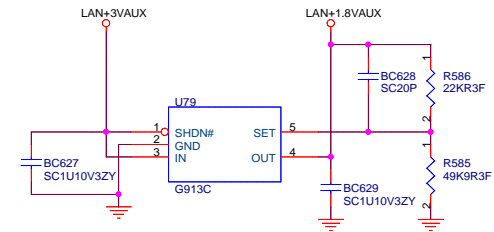




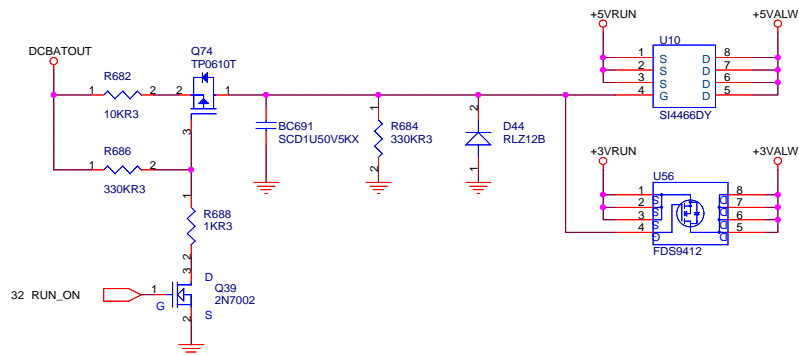


## LAN+3VAUX

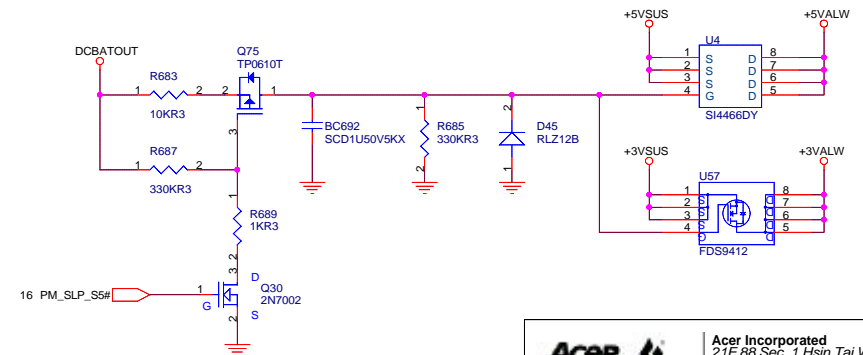
LAN+3VAUX — LDO G913C → LAN+1.8VALW



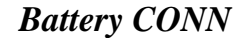
## Run Power



## Suspend Power







**BATTERY CONNECTOR SECOND SOURCE**

AMP : 20.80111.005  
STECH : 20.80114.005

C-Note don't keep HRS  
connector for MS LOGO

*/BTIN=0 when battery exist , system on & adaptor exist ,  
/BIU=0 when battery exist , system on & adaptor NOT exist*

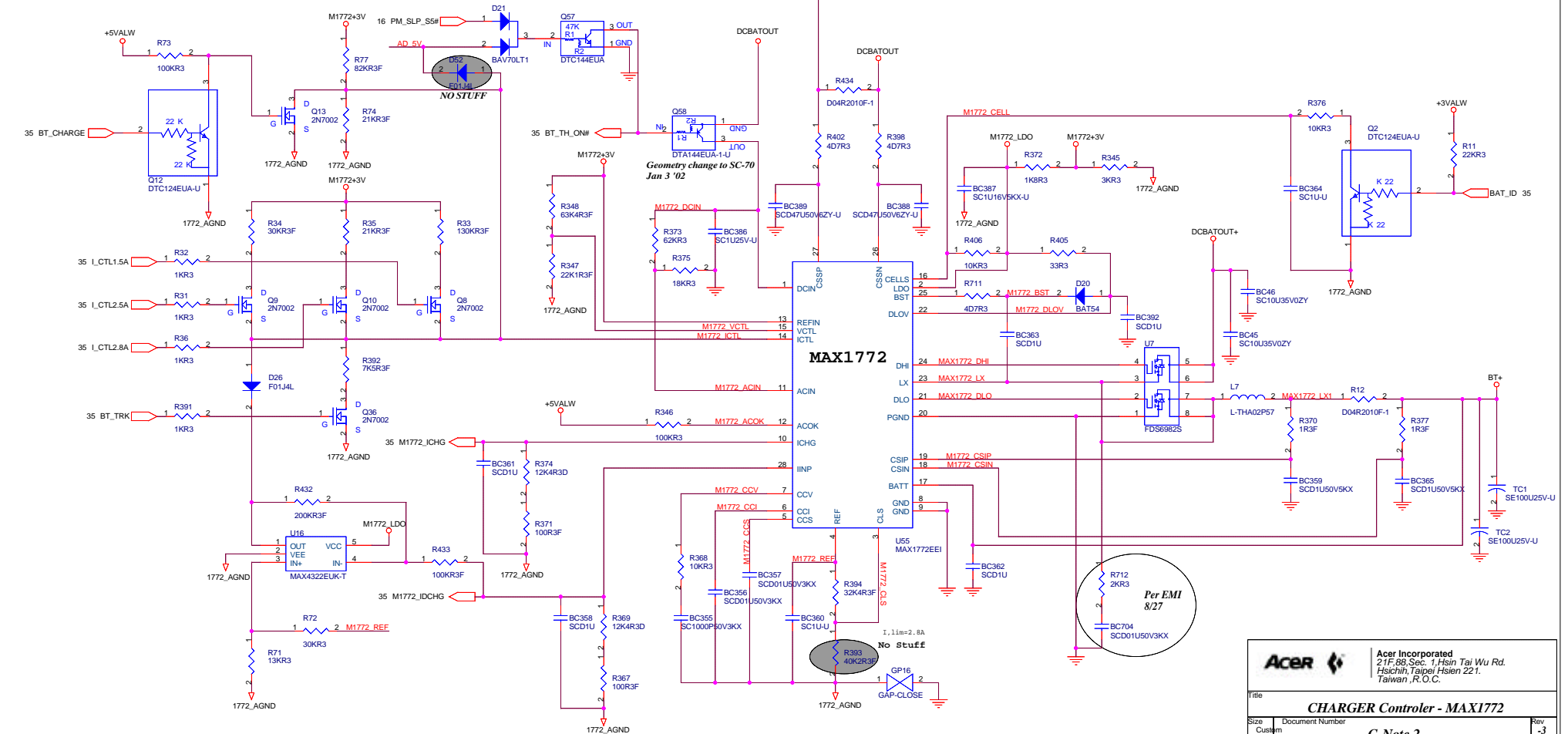
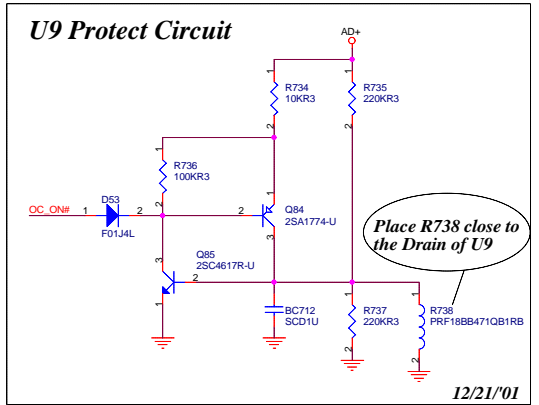
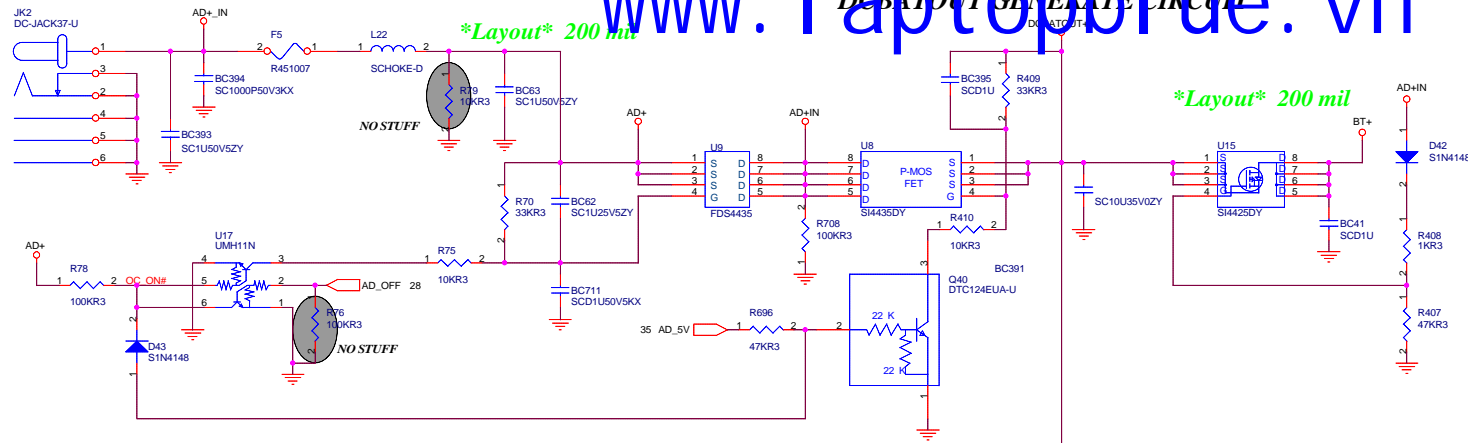
Acer &lt;+

**Acer Incorporated**  
21F, 88, Sec. 1, Hsin Tai Wu Rd.  
Hsichih, Taipei Hsien 221.  
Taiwan, R.O.C.

Title	<b>CHARGER FirmWare-MC68HC908SR</b>
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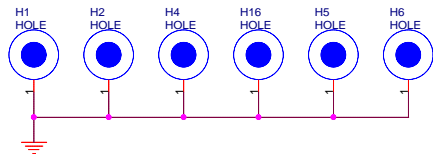
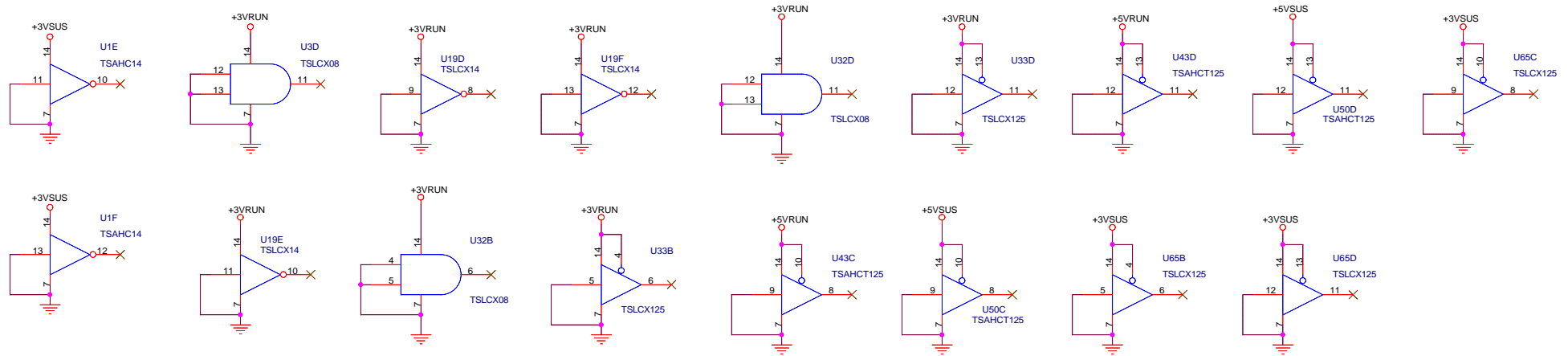
Size	Document Number	Rev
Custom	<b>C-Note 2</b>	-3
Date:	Friday, January 11, 2002	Sheet 35 of 37







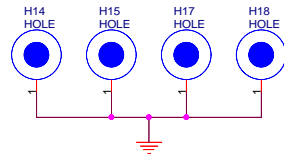
# NO USE LOGIC



**CDC BOSS**  
34.42G11.001



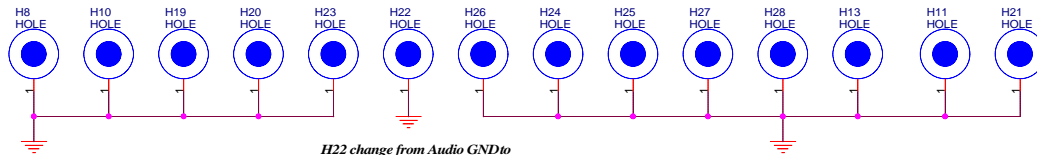
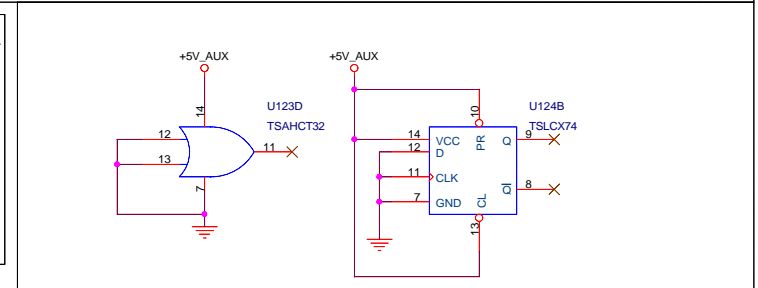
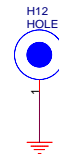
**CPU BOSS**  
34.49G03.001



**LCD BOSS**  
34.42G10.001

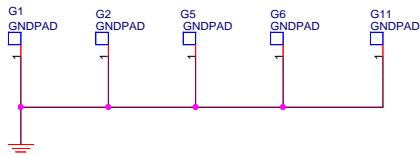


**HEAT SINK**  
34.47R08.001



H22 change from Audio GND to  
Digital GND to solve FIR noise  
Jan 04 '02

**EMI SPRING**  
34.42P26.001



**EMI SPRING (LCD)**  
34.47R27.001



**EMI SPRING (DIMM)**  
34.47R31.001

