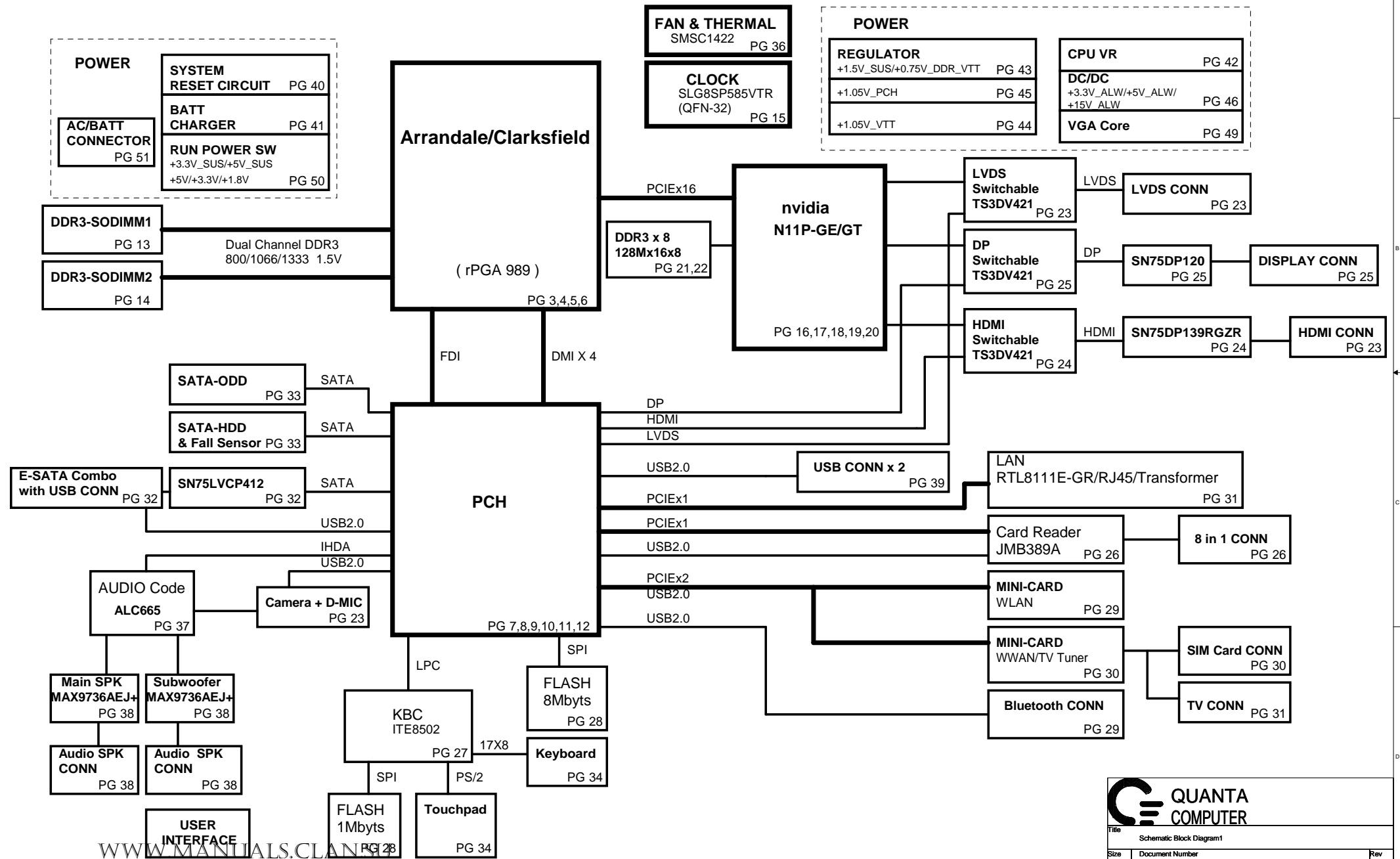


GM6B Studio Intel UMA and Discrete GFX




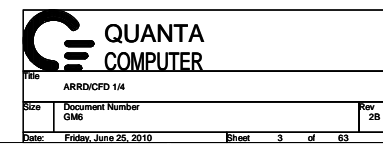
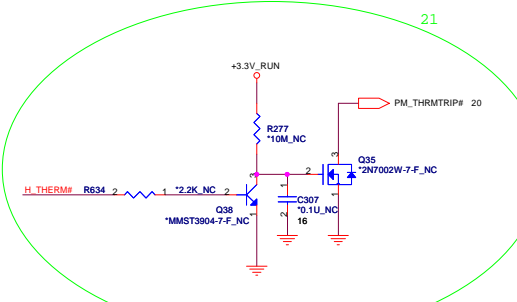
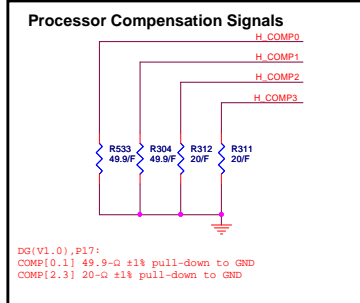
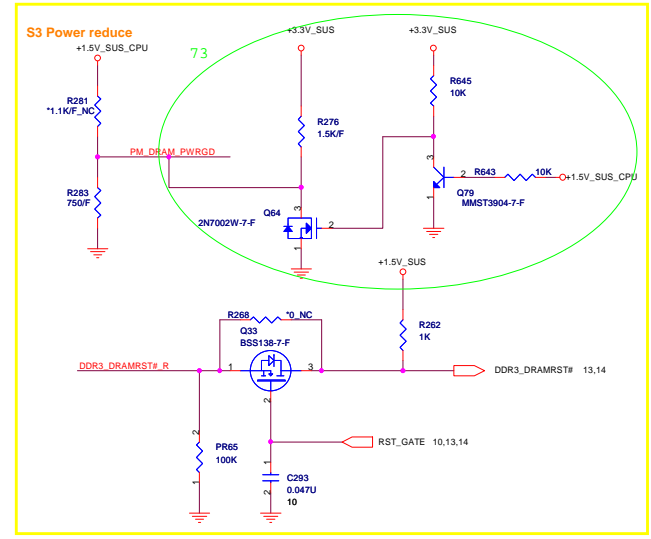
QUANTA
COMPUTER

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2	Front Page
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7-12	PCH
13-14	DDRIII SO-DIMM(204P)
15	Clock Generator
16-22	N11P-GE
23	LCD CONN
24	HDMI CONN
25	MINI DP CONN
26	Card Reader (JMB389)
27	SIO (ITE8502)
28	FLASH / RTC
29	MINI-Card (WLANWPAN)
30	MINI-Card (WWAN)
31	LAN(RTL8111EL/RJ-45)
32	Right PUSB/ESATA
33	SATA (HDD & ODD)
34	TP / KEYBOARD
35	SWITCH / LED / T-Screen
36	FAN / THERMAL
37	Azelia CODEC
38	AUDIO AMP
39	Left USB/MMB CONN
40	System Reset Circuit
41	Charger (ISL88731)
42	CPU CORE(ADP3212)
43	1.5_DDR/0.75(RT8207A)
44	1.05V_VTT(VT358)
45	1.05V_PCH(VT356)
46	3V/5V (TPS51427A)
47	GFX_CORE(ADP3211)
48	1.8V_RUN(HPA00835RTER)
49	VGA_N11P-dGFX(MAX17007)
50	Run Power Switch
51	DCin & Batt
52	PAD & SCREW
53	SMBUS BLOCK
54	THERMAL MAP
55	Power Block Diagram
56	Power sequence Block
57	
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POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	24,30,45,46,47,48,49,50,51	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	08,11,29,30	RTC		S0~S5
+5V_ALW2	+5V	37,46,52,53	LARGE POWER	MAIN POWER	S0~S5
+5V_ALW	+5V	13,33,44,46,47,48,49,50,51,52	LARGE POWER	ALW_ON	S0~S5
+3.3V_ALW	+3.3V	29,30,35,36,37,42,44,45,46,47,51,52,53	8051 POWER	3.3V_ALW_ON	S0~S5
+5V_SUS	+5V	11,33,34,37,51,52	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	07,08,09,10,11,13,14,19,24,28,29,37,41,42,44,48,49,50,52	SLP_S5# CTRLD POWER	SUS_ON	
+1.5V_SUS	+1.5V	03,05,13,14,47,50,52	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.75V	13,14,47,52	SODIMM POWER	RUN_ON	
+5V_RUN	+5V	11,18,24,25,35,36,38,39,40,51,52	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,7,8,9,10,11,13,14,15,17,24,25,26,28,29,30,31,32,33,35,37,38,39,40,41,42,46,51,52,60	SLP_S3# CTRLD POWER	RUN_ON	
+1.8V_RUN	+1.8V	05,11,44,52	SDVO POWER	RUN_ON	
+1.8V_RUN_GFX	+1.8V	17,18,21,22,44,52	VGA POWER	RUN_ON	
+1.5V_RUN	+1.5V	11,18,19,20,28,31,32,52	VGA POWER	RUN_ON	
+VCC_GFX_CORE	+0.9V~+1.2V	18,21,50	VGA POWER	RUN_ON	
+1.05V_PCH	+1.05V	08,09,11,15,48	PCH POWER	RUN_ON	
+VCC_CORE	+0.7V~+1.77V	05,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	24	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	35	MOD Power	MODC_EN	
+5V_HDD	+5V	35	HDD Power	HDDC_EN	
+1.1V_VTT	+1.1V	03,05,10,11,49,60	CPU POWER	RUN_ON	
+1.1V_GFX_PCIE	+1.1V	18,50	VGA POWER	GFX_ON	

GND PLANE	PAGE	DESCRIPTION
 GND	ALL	



AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

U46C

Clarksfield/Auburndale

DDR SYSTEM MEMORY A

Channel A DQ[15,32,48,54], DM[5]
Requires minimum 12mils spacing
with all other signals, including data signals.

U46D

Clarksfield/Auburndale

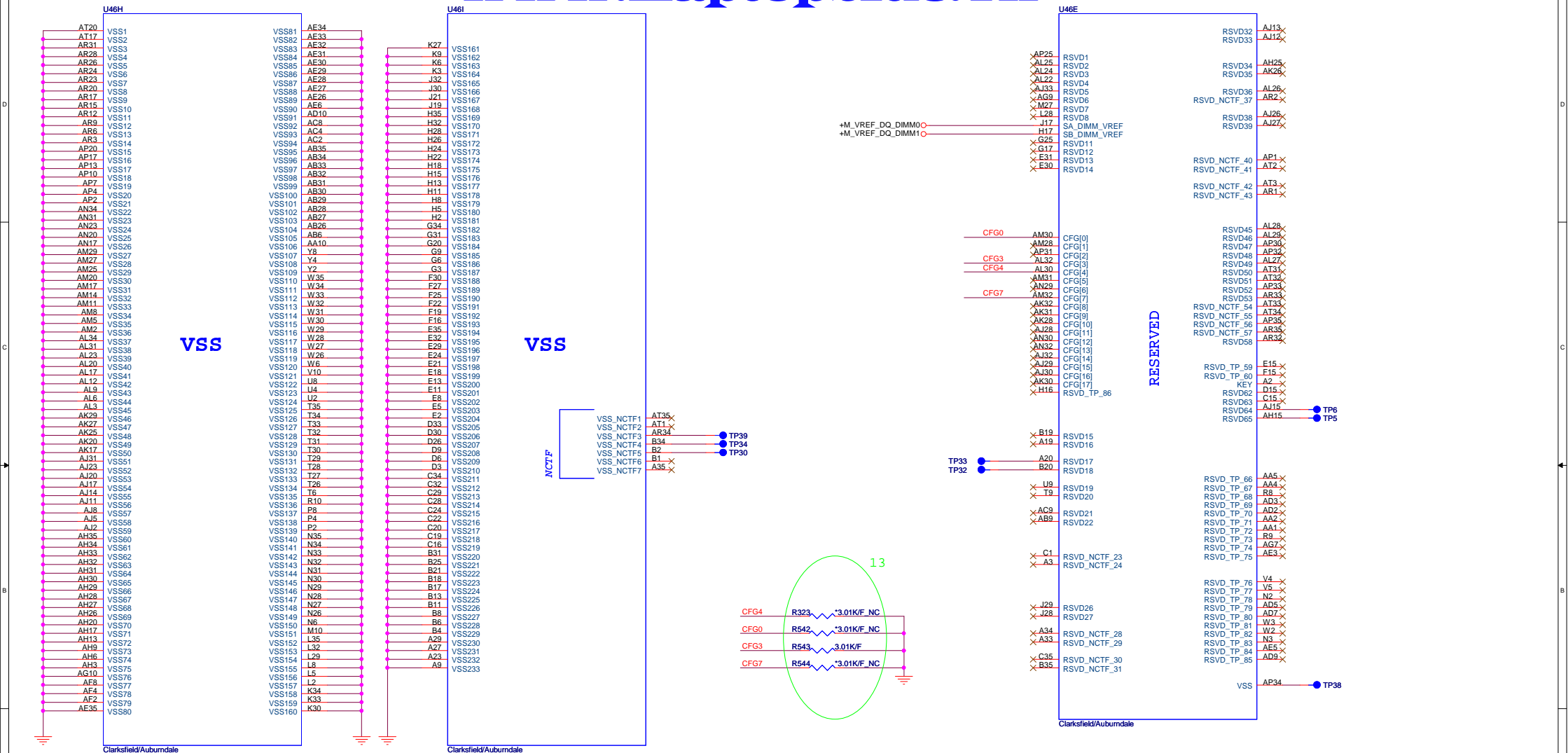
DDR SYSTEM MEMORY - B

Channel B DQ[16,18,36,42,56,57,60,61,62]
Requires minimum 12mils spacing
with all other signals, including data signals.



Title			ARRD/CFD 2/4
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Processor Strapping

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

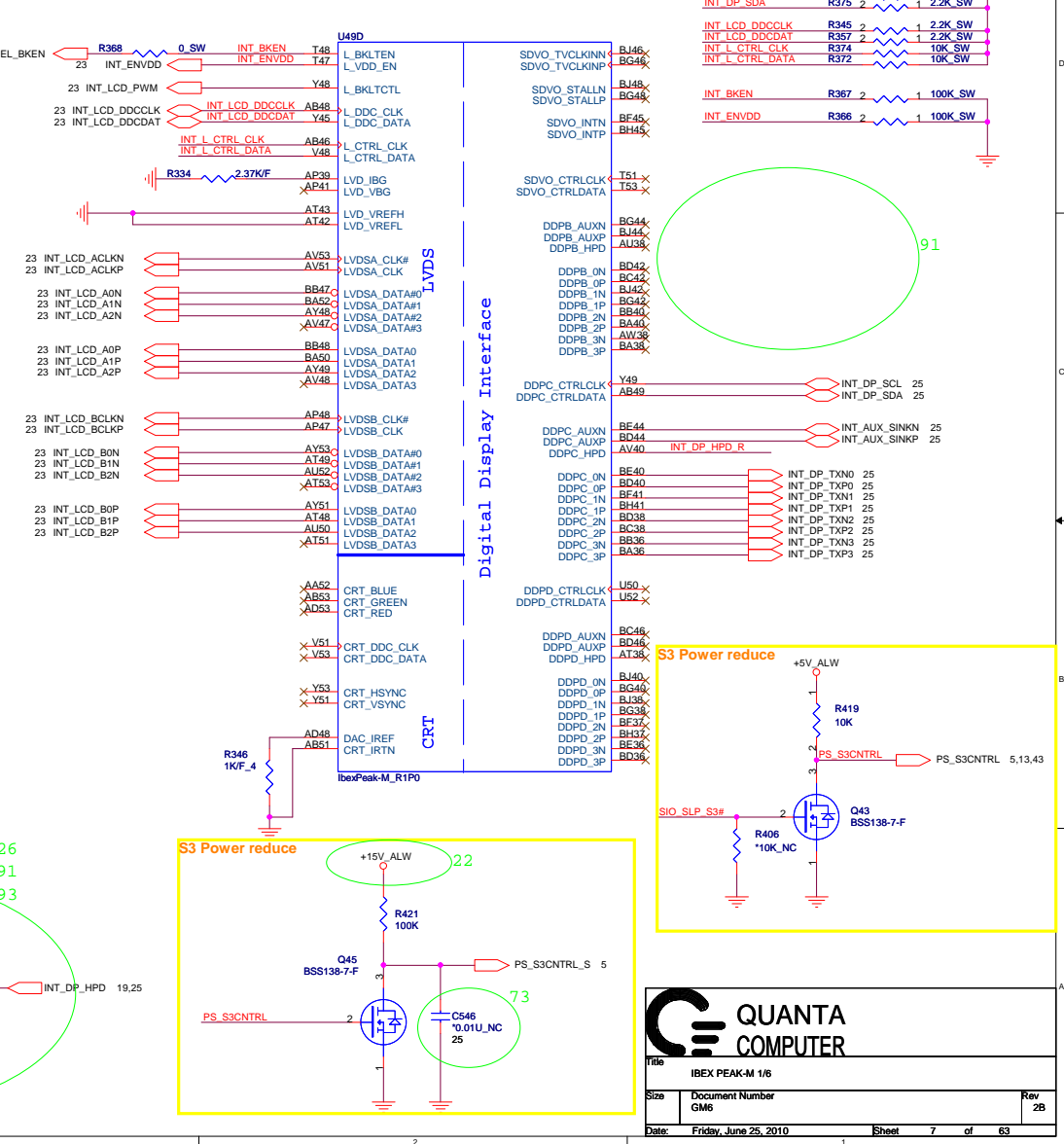
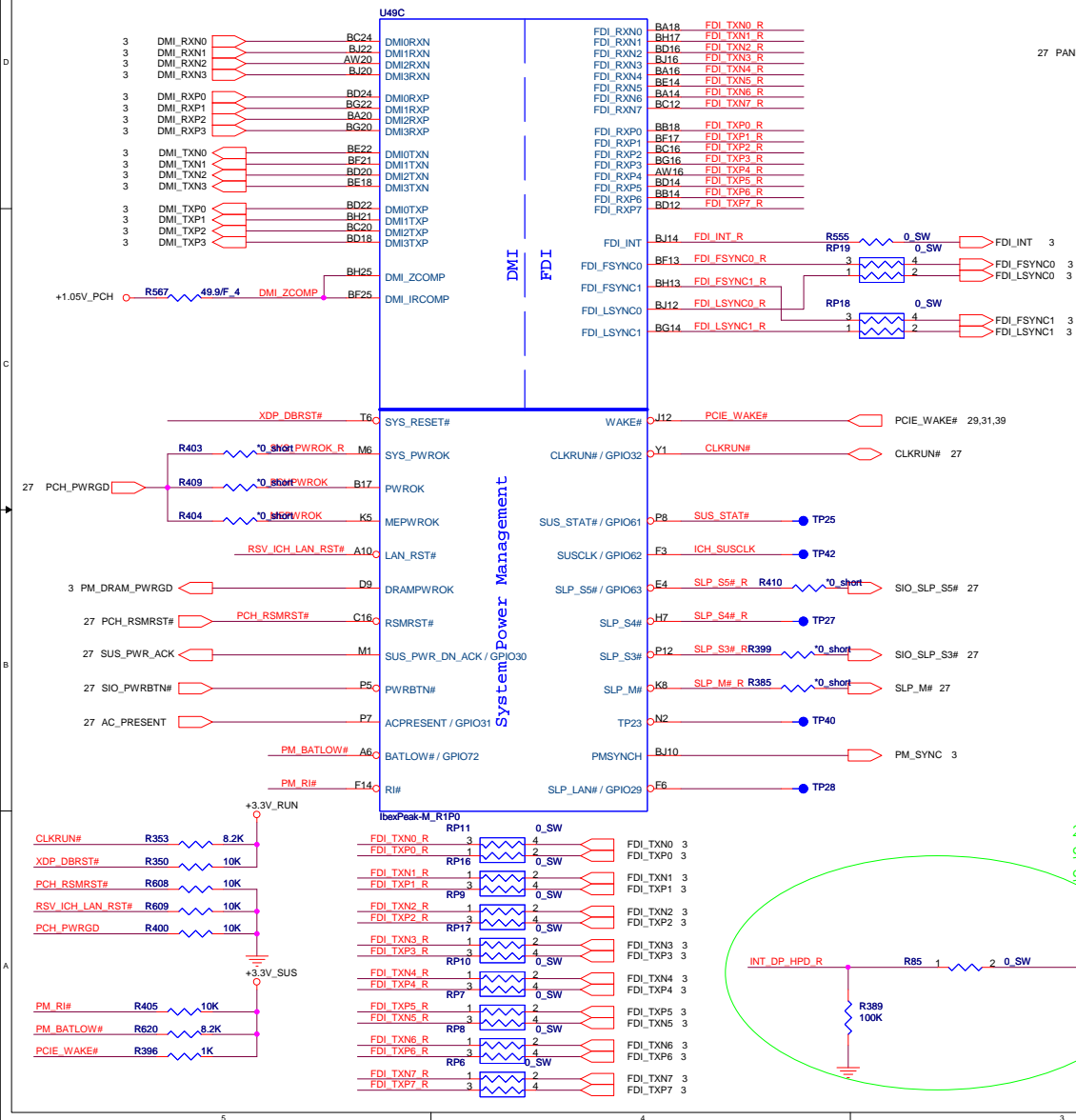
CFG[1:0] - PCI_Epress Configuration Select
* 11= 1 x 16 PEG
* 10= 2 x 8 PEG

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.(ES1 only)

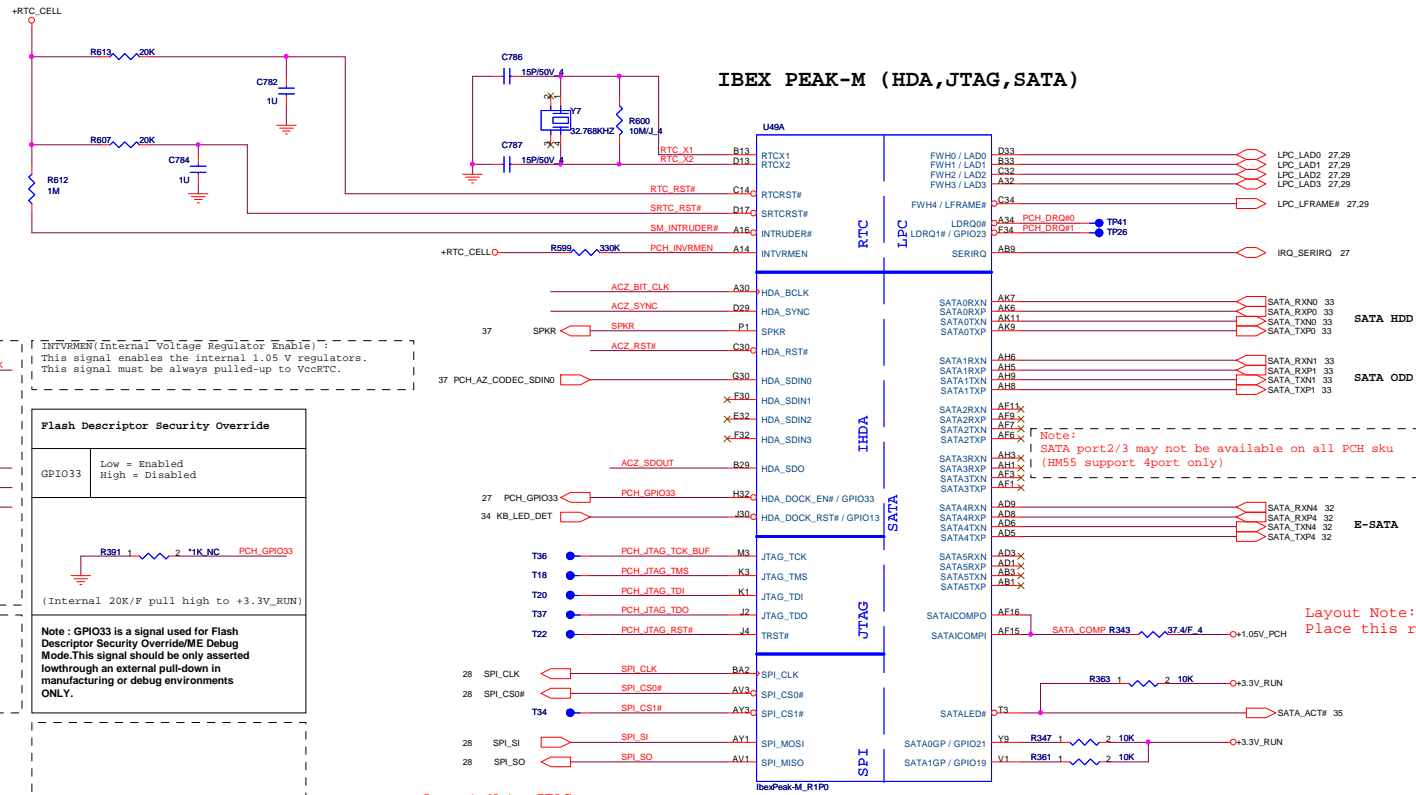
Title ARRD/CFD 4/4		
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IBEX PEAK-M (DMI, FDI, GPIO)

IBEX PEAK-M (LVDS, DDI)



IBEX PEAK-M (HDA,JTAG,SATA)



IntVrMEn(Internal Voltage Regulator Enable) :
This signal enables the internal 1.05 V regulators.
This signal must be always pulled-up to VccRTC.

Flash Descriptor Security Override	
GPIO33	Low = Enabled High = Disabled

R391 1 2 1K NC PCH_GPIO33
(Internal 20K/F pull high to +3.3V_RUN)

Note : GPIO33 is a signal used for Flash Descriptor Security Override/ME Debug Mode. This signal should be only asserted low through an external pull-down in manufacturing or debug environments ONLY.

R589 51 PCH_JTAG_TCK_BUF

Note : Only pop when PCH is production stage & need "JTAG boundary Scan". Remember to depop XDP side Res.

37 ICH_AZ_CODECLTCLK ACZ_BIT_CLK
37 ICH_AZ_CODECSYNC ACZ_SYNC
27,37 ICH_AZ_CODECRST# ACZ_RST#
37 ICH_AZ_CODECSOUT ACZ_SDOU

Place all series terms close to PCH except for SDIN input lines, which should be close to source. Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

+3.3V_RUN
R390 1 2 1K NC SPKR

No Reboot strap.	
SPKR	Low = Default. High = No Reboot.

Layout Note: JTAG
Test Pads are need to put on the same side of mother board.

Note:
SATA port 2/3 may not be available on all PCH sku
(HM55 support 4port only)

Layout Note:
Place this resistor close to PCH





dGPU_PRSENT# R362 10K/J

dGPU always exist

+NVRAM_VCCQ



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COMPUTER

Title INDEX PEAK M 1/5

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```
BMBUSY#:  
If not used, require a weak pull-up  
(8.2- KΩ to 10 kΩ) to Vcc3_3.  
CRB(V1.0)P28: it has 1K PU and  
100 ohm on this net for validation purpose.
```

A16 swap override Strap/Top-Block
Swap Override jumper

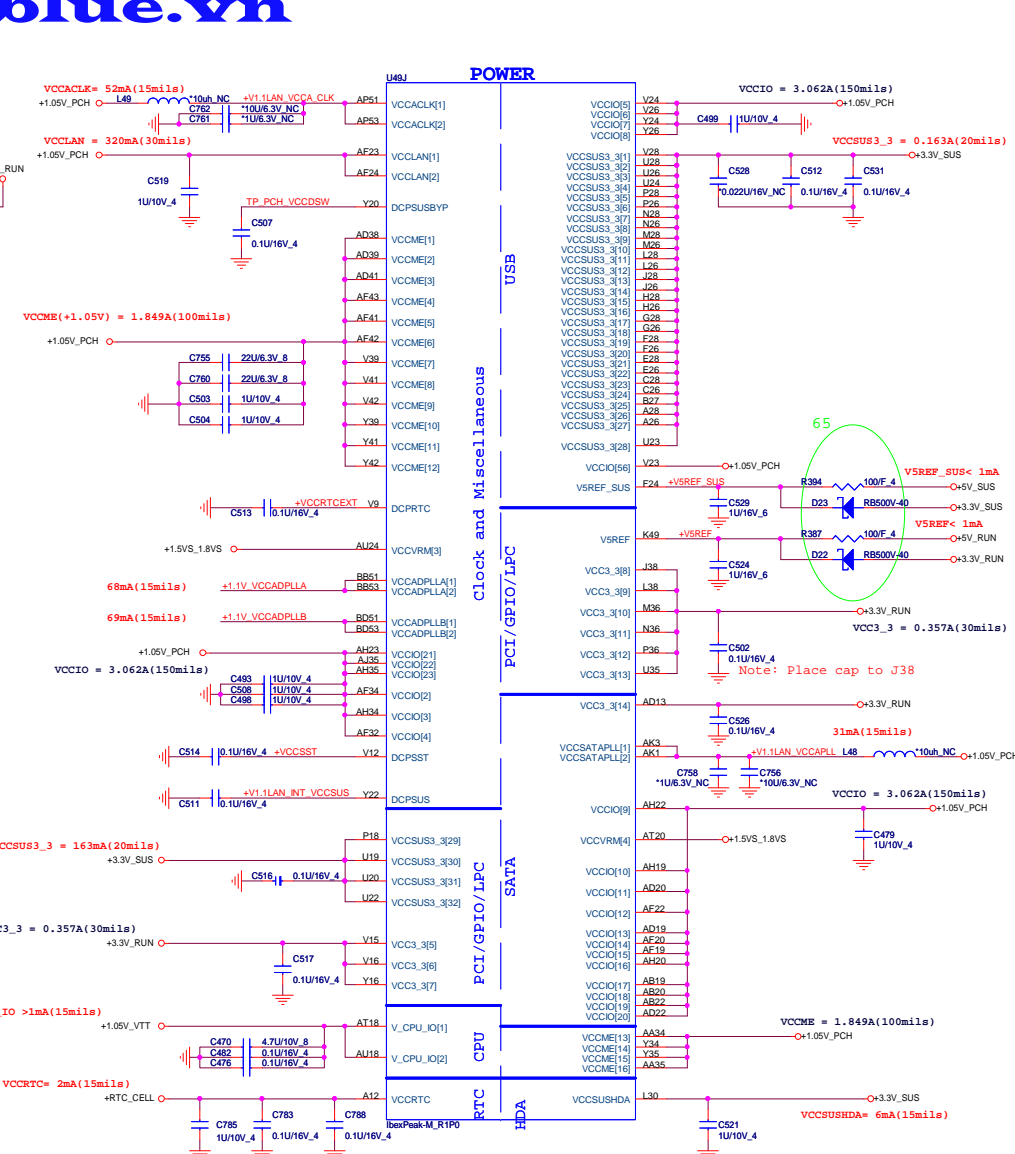
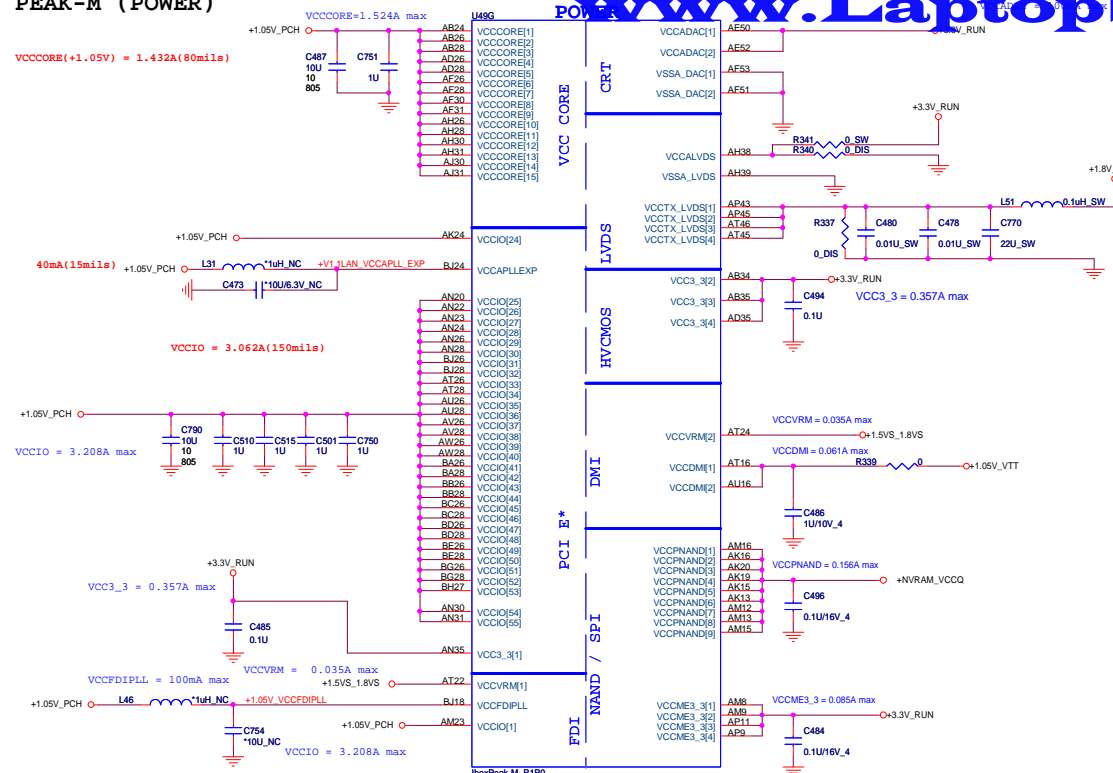
```

GNT3# override/Top-Block
      Swap Override enabled

```

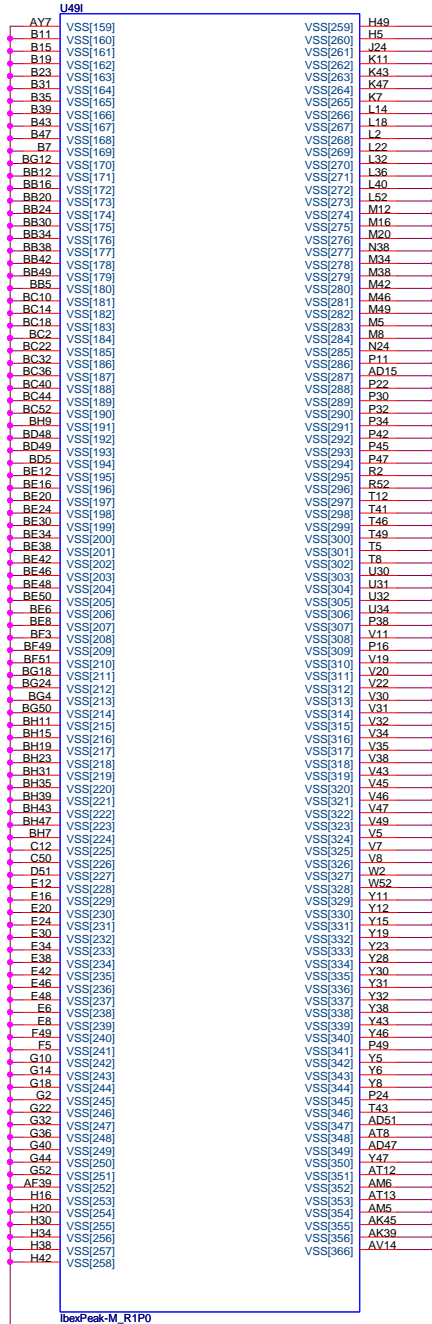
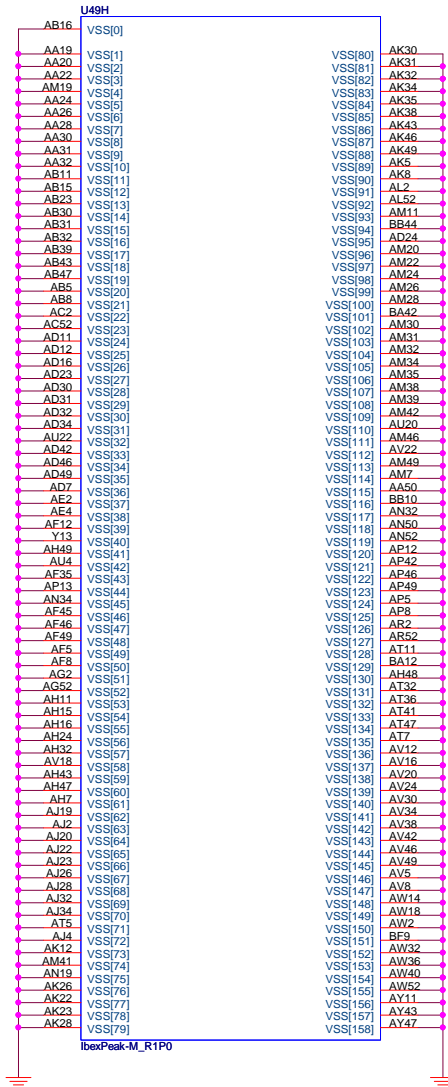
RSV_WOL_EN	Enable when sampled low Disable when sampled high
------------	--


SV_SET_UP	1-X High = Strong (Default)
-----------	-----------------------------



Title			IBEX PEAK-M 5/6		
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IBEX PEAK-M (GND)





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Title

IBEX PEAK-M 6/6

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Document Number

GM6

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Sheet

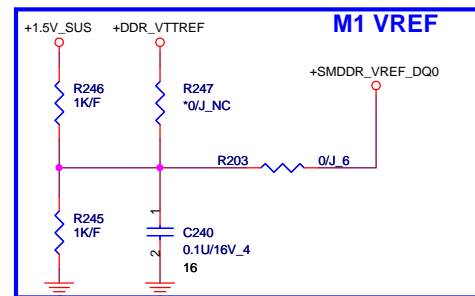
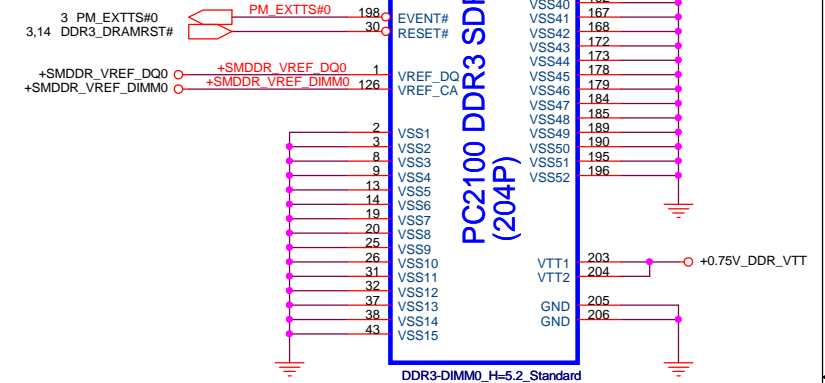
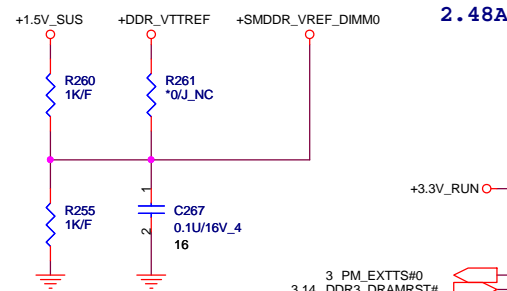
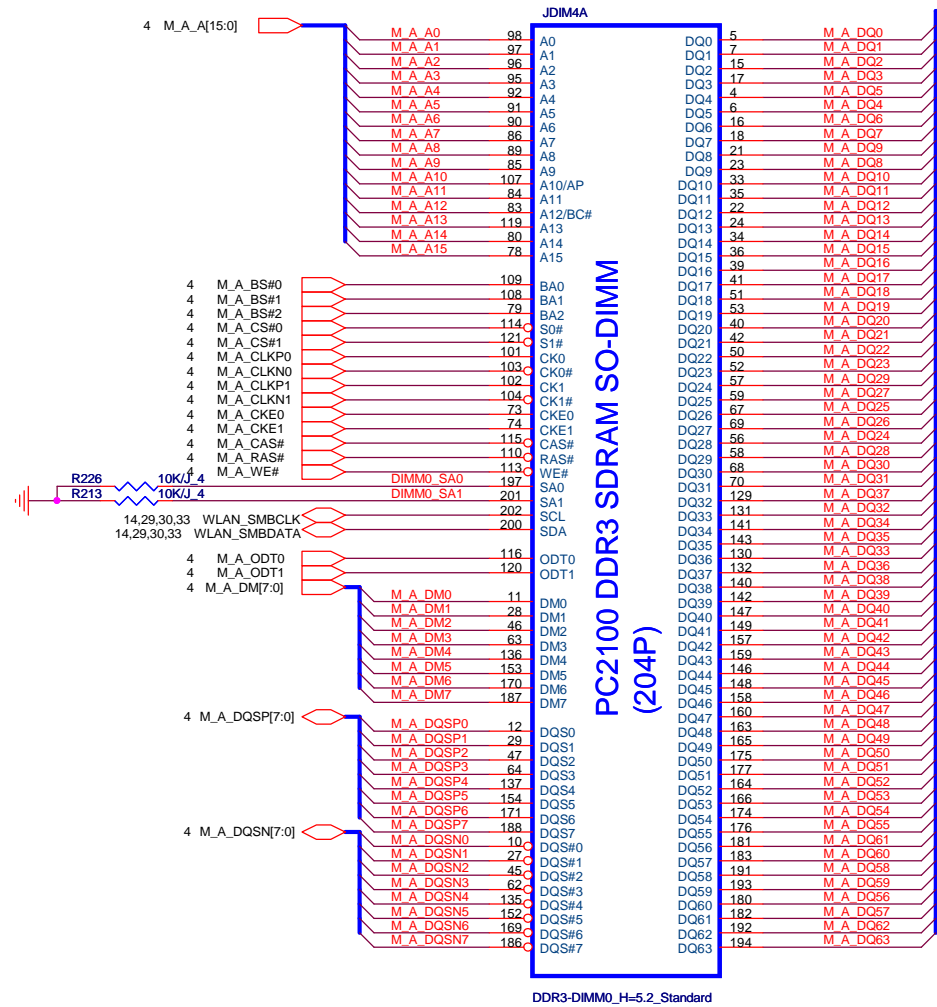
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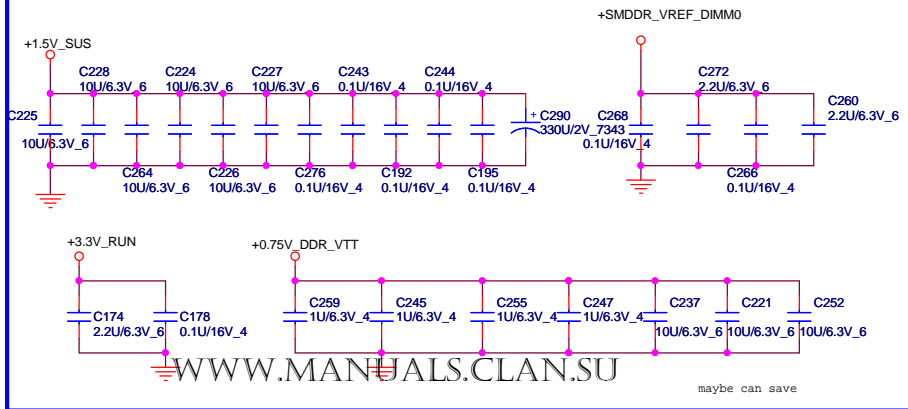
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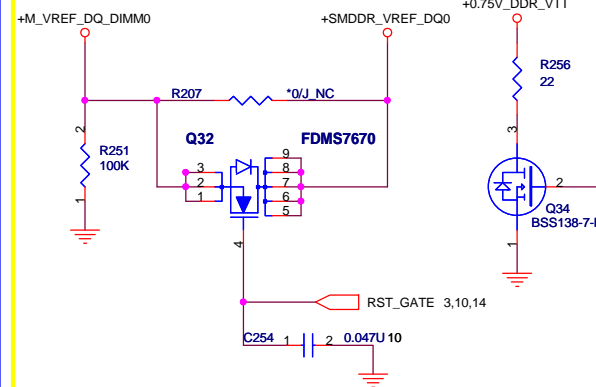


VREF_DQ	R203	R207	R247 (+DDR_VTTREF)
M1	Stuff	X	X
M3	X	Stuff	X

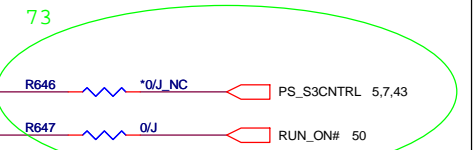
Place these Caps near So-Dimm0.

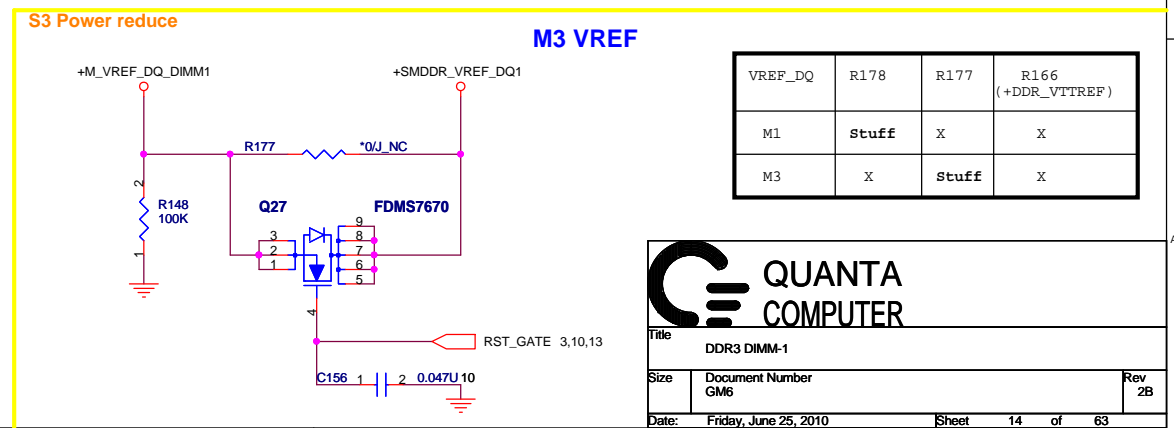
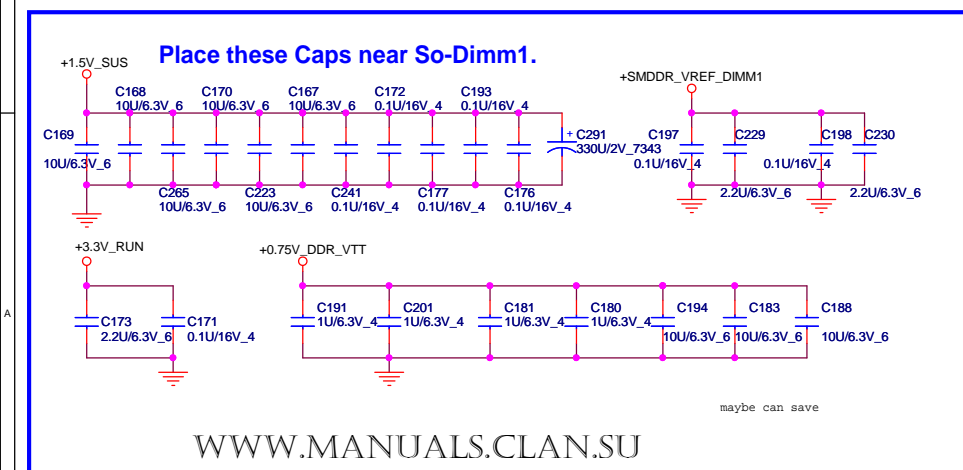
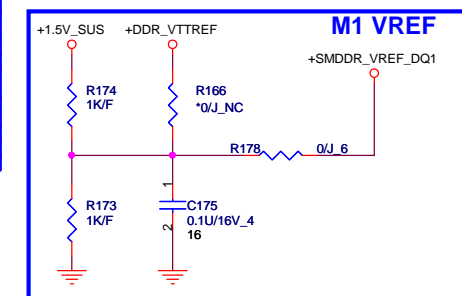
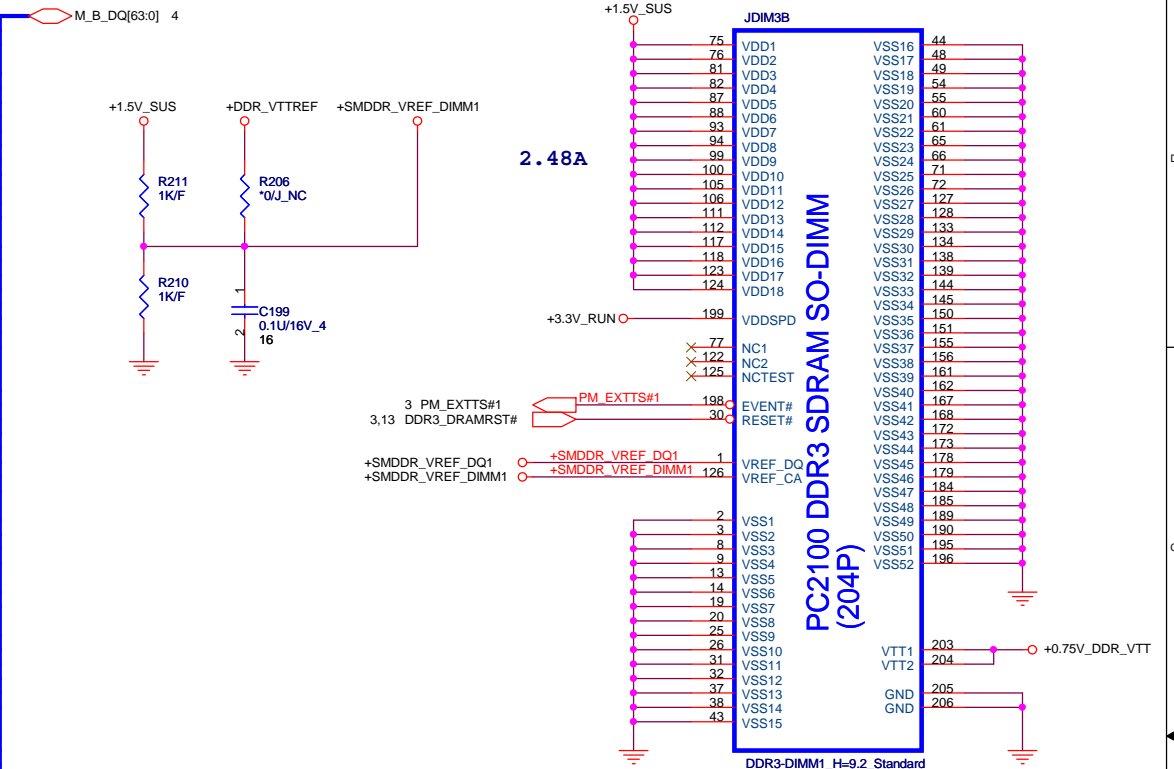
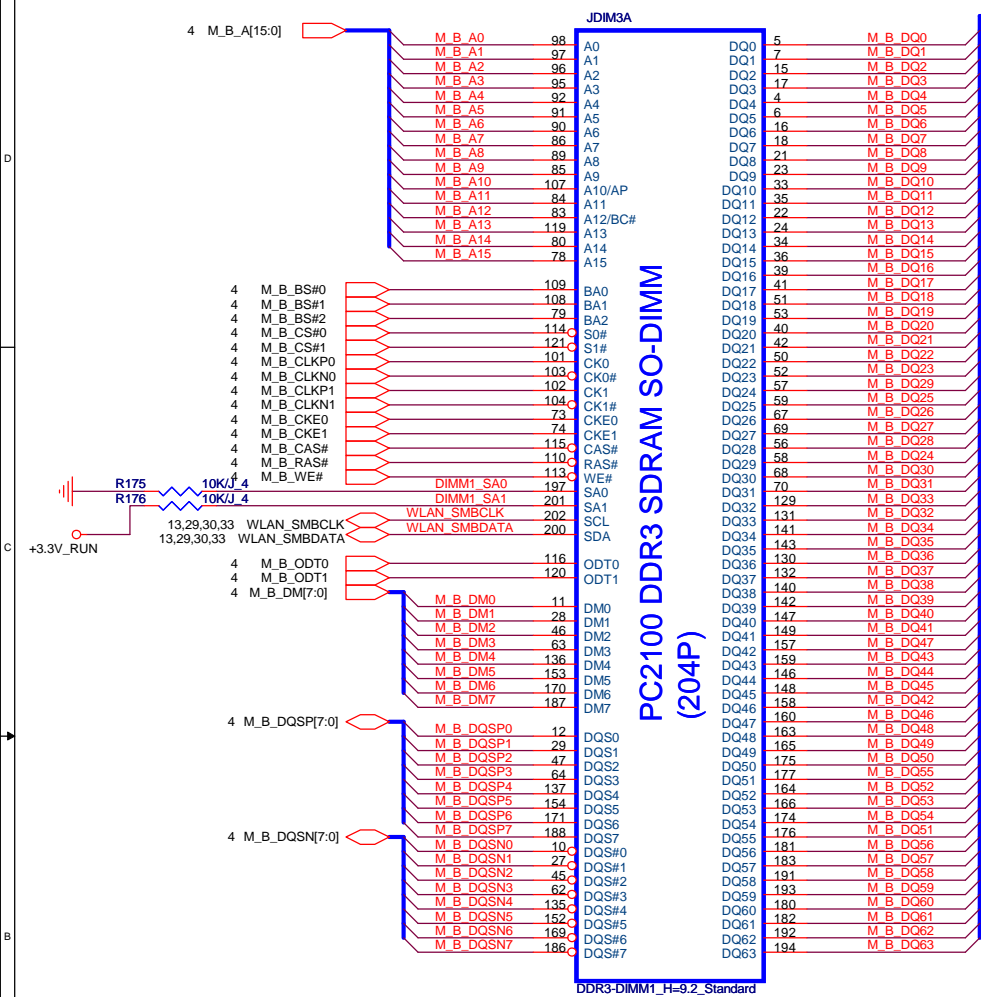


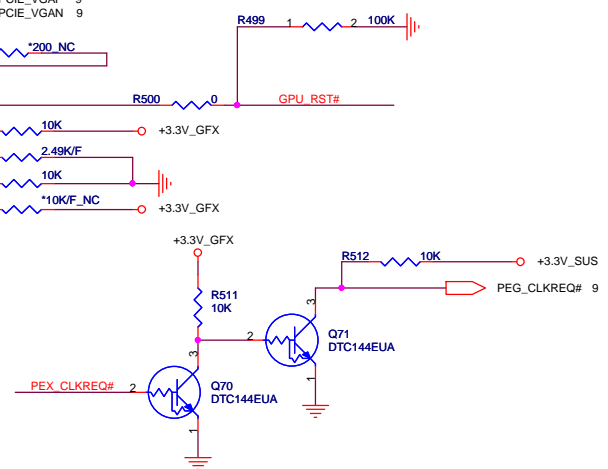
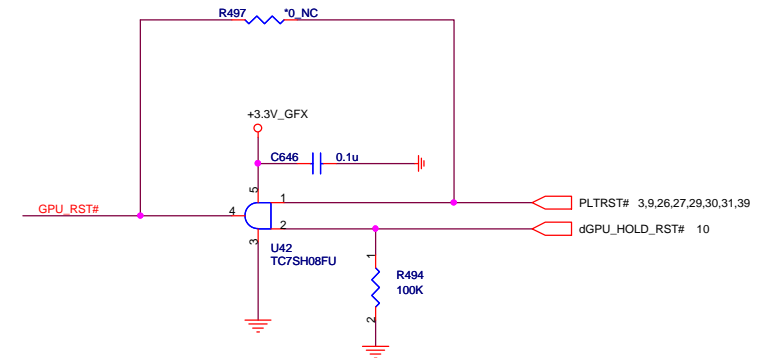
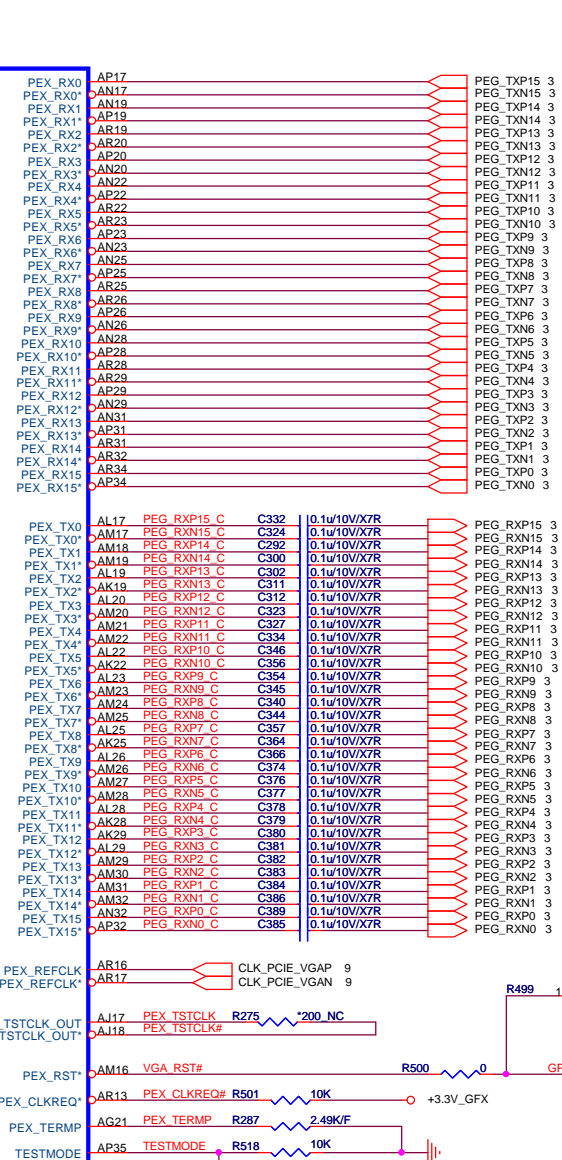
S3 Power reduce

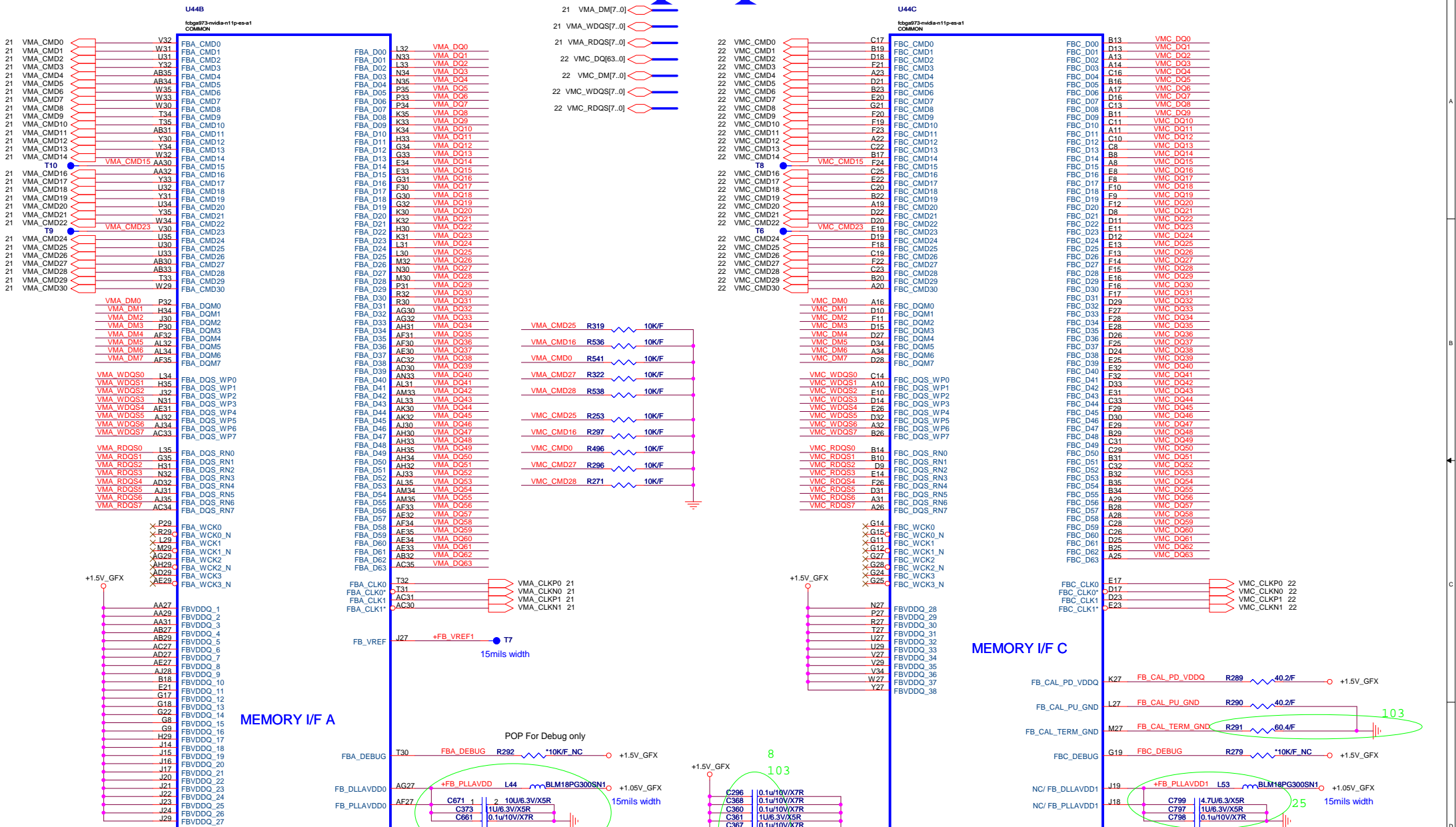


M3 VREF







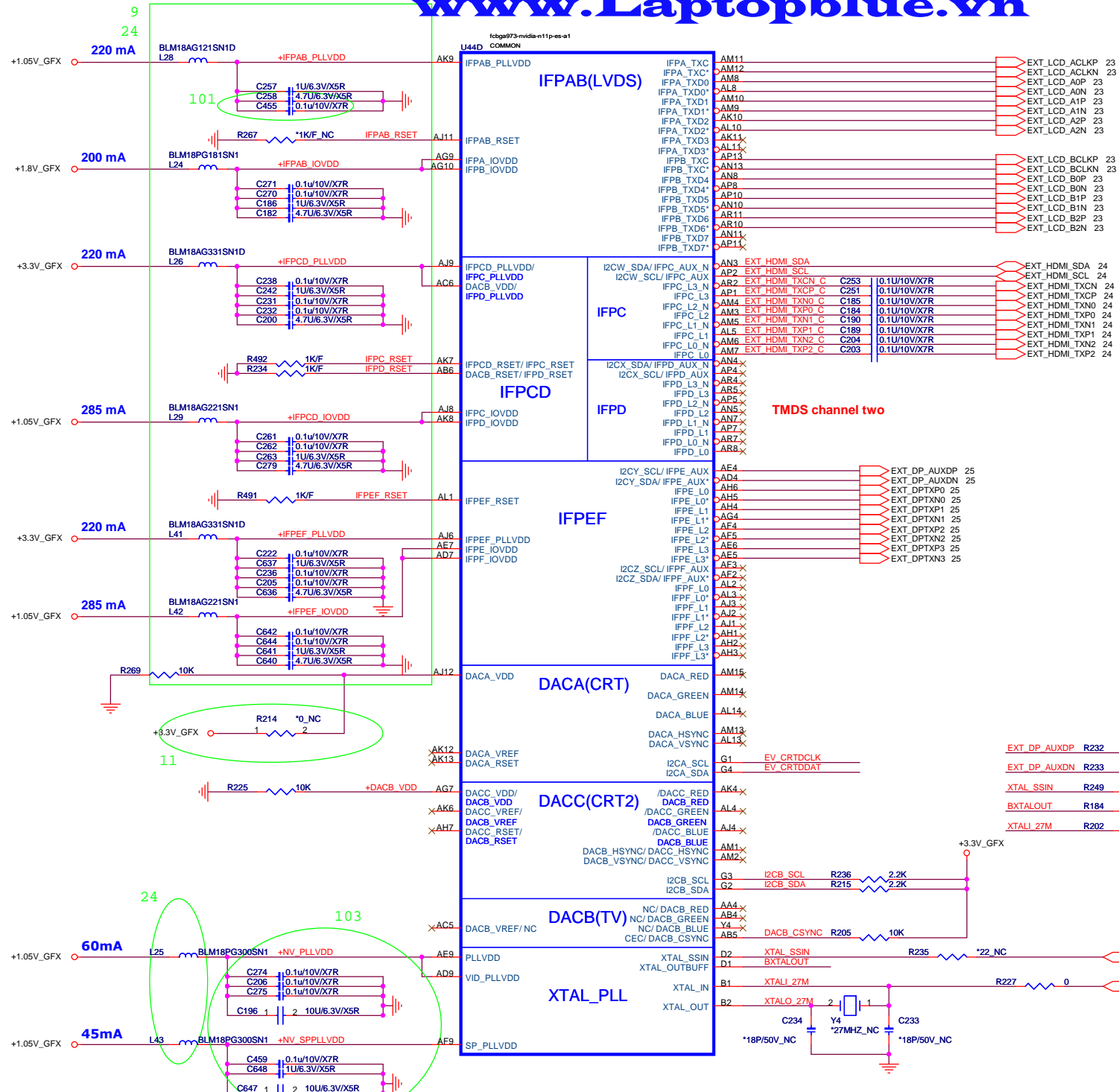


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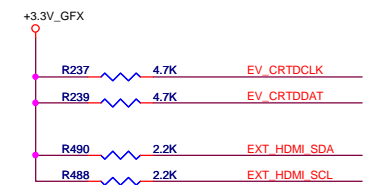
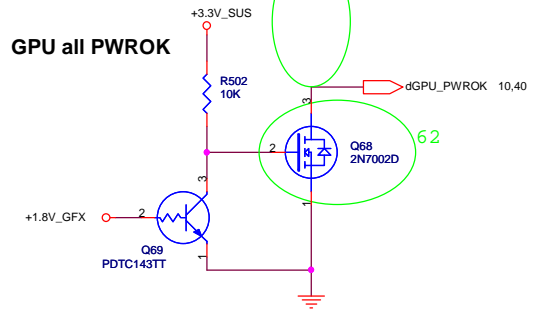
Title: VGA-N11P GE/GT (MEM IF)

Size: Document Number GM6 Rev 2B

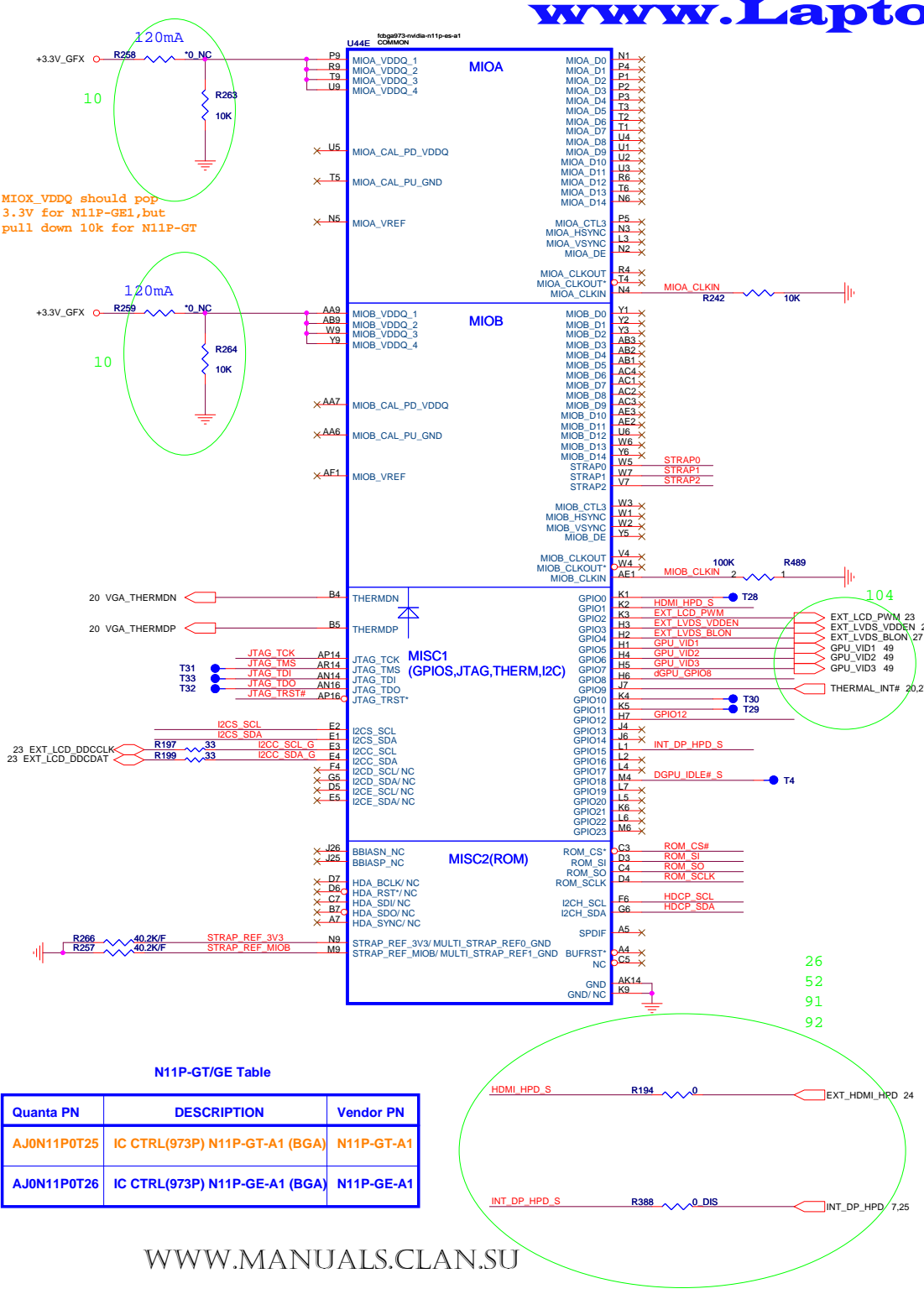
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GPU all PWROK



Title			VGA-N11P GE/GT (Display)
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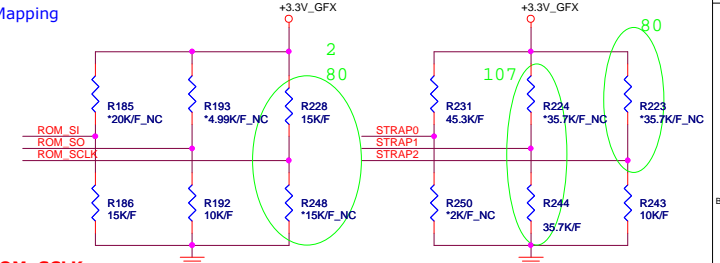
	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0		
ROM_SO	NB10X	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM		X010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]		XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]		XXXX
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]		1110
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]		1111

39 VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Quanta PN(Q buy)	Quanta PN(W buy)	Vendor PN
0x3(0011)	800MHz 512MB(64M*16) Samsung	AKDSLGGT502	AKDSLGGT505	K4W1G1646E-HC12
0x2(0010)	800MHz 512MB(64M*16) Hynix	AKDSLZGTW00	AKDSLZGTW03	H5TQ1G63BFR-12C
0x6(0110)	800MHz 1GB(128M*16) Hynix	AKD5MGGTW00	AKD5MGGTW03	H5TQ2G63BFR-12C
0x7(0111)	800MHz 1GB(128M*16) Samsung	AKD5MGGTW05		K4W2G1646C-HC12

ROM_SI Strap Bit for RAM Mapping

	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



STRAP2 ROM_SCLK

N11P-GE	PD 10K	PU 15K
N11P-GT	PD 15K	PU 15K

SUNSGUNG OR HYNIX
N11P-ES DeVID is 0x0DFE, so pull up ROM_SCLK with 15Kohm and STRAP2 pull up 35Kohm

HDCP_SCL	R218	10K
HDCP_SDA	R240	10K
GPU_VID2	R217	10K NC
GPU_VID1	R189	10K/F
GPU_VID3	R485	10K/F NC
JTAG_TMS	R504	10K/F NC
JTAG_TDI	R505	10K/F NC
GPIO12	R584	10K/F
DGPU_IDLE# S	R220	10K/F NC
I2CS_SCL	R188	2.2K
I2CS_SDA	R187	2.2K
I2CC_SCL G	R195	2.2K
I2CC_SDA G	R198	2.2K
ROM_CS#	R229	10K
dGPU_GPIO8	R219	10K

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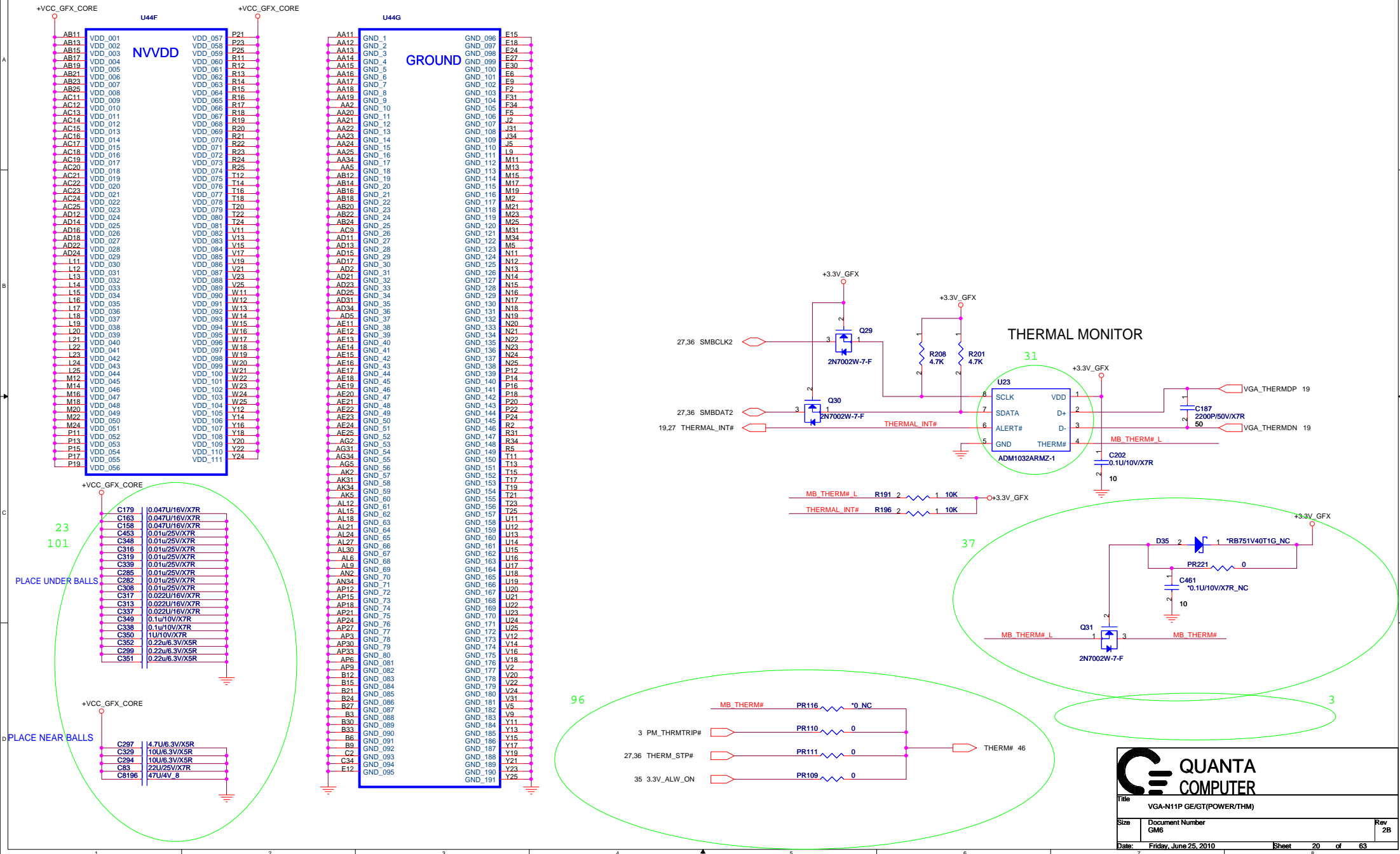
JTAG_TRST#	R506	1K/F
JTAG_TCK	R503	10K
HDMI_HPD_S	R204	100K
GPU_VID1	R190	10K NC
GPU_VID2	R486	10K/F
GPU_VID3	R482	10K/F
INT_DP_HPD_S	R221	100K
EXT_LCD_PWM	R212	10K
DGPU_IDLE# S	R241	10K
EXT LVDS_VDDEN	R238	10K
EXT LVDS_BLON	R209	10K

GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDV VID0
6	OUT	N/A	NVVDV VID1
7	OUT	N/A	NVVDV VID2
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

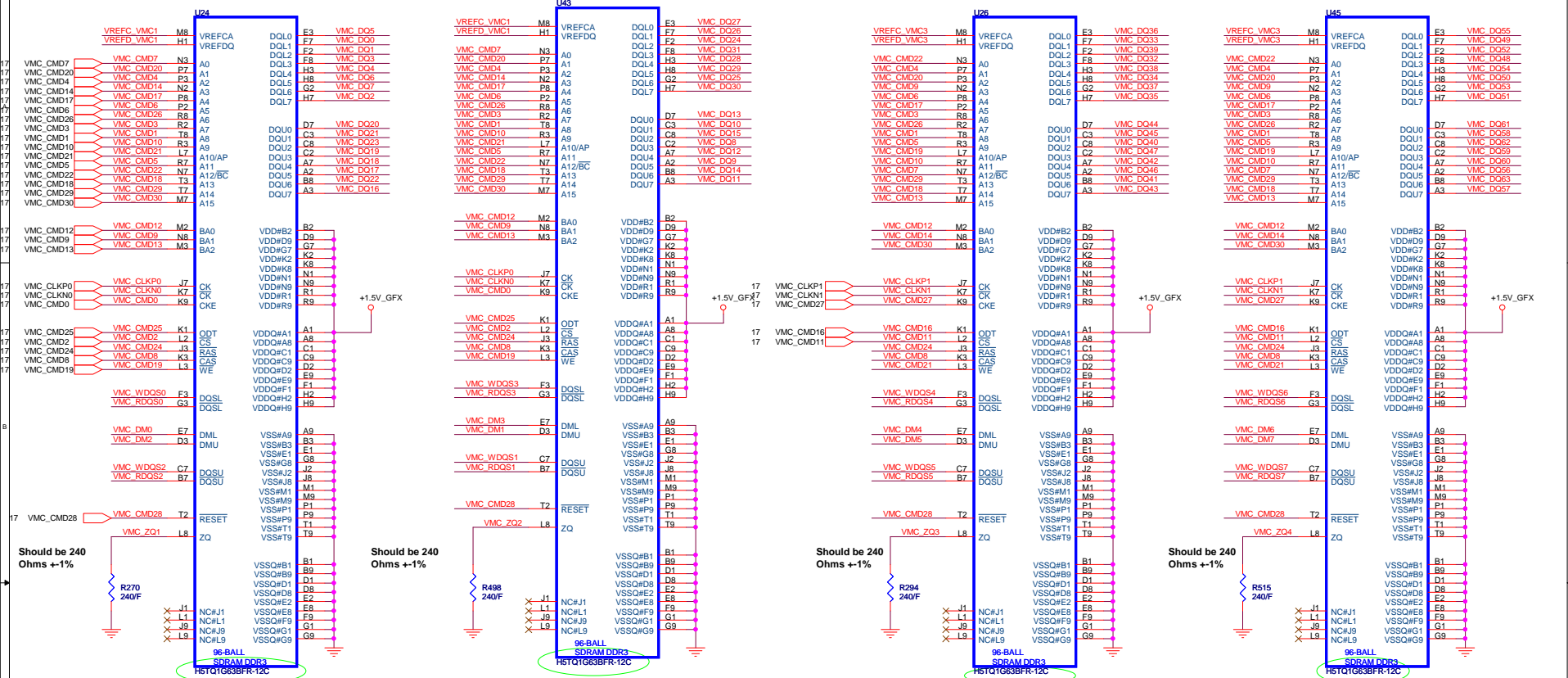


Title VGA-N11P GE/GT(GPIO/STRAP)			
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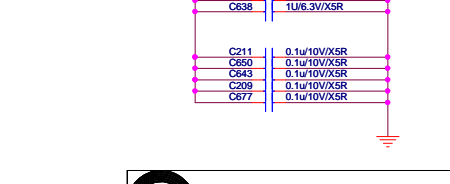
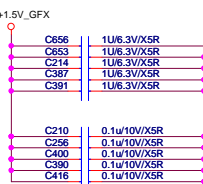
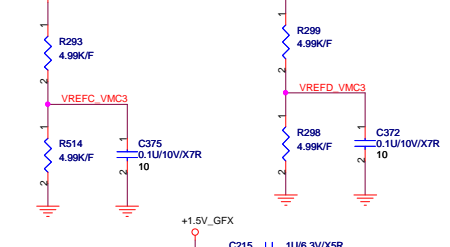
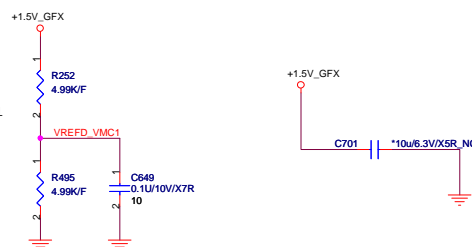
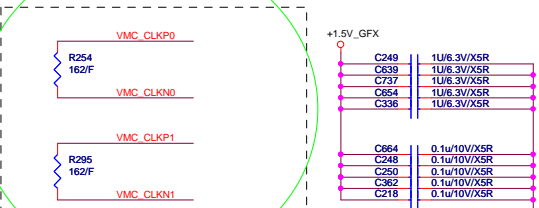
17 VMC_DQ[3..0]
17 VMC_CMD[7..0]
17 VMC_RDQS[7..0]
17 VMC_RDQS[7..0]



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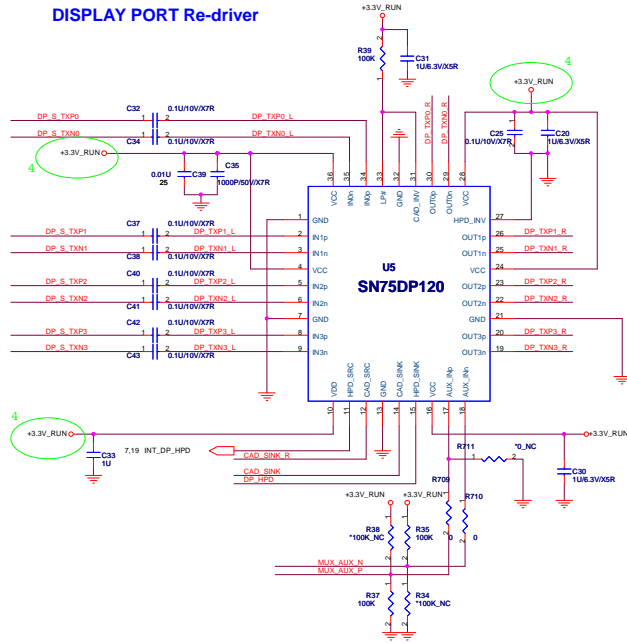
Placement has to be close to VRAM



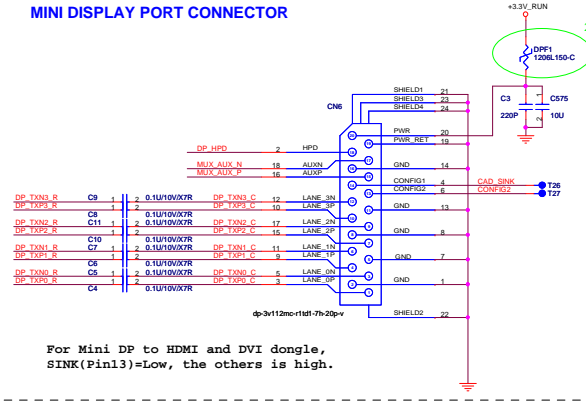




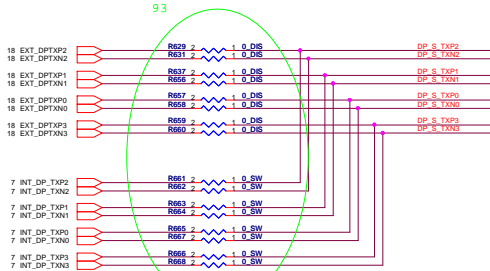
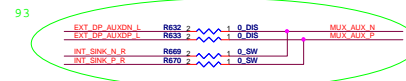
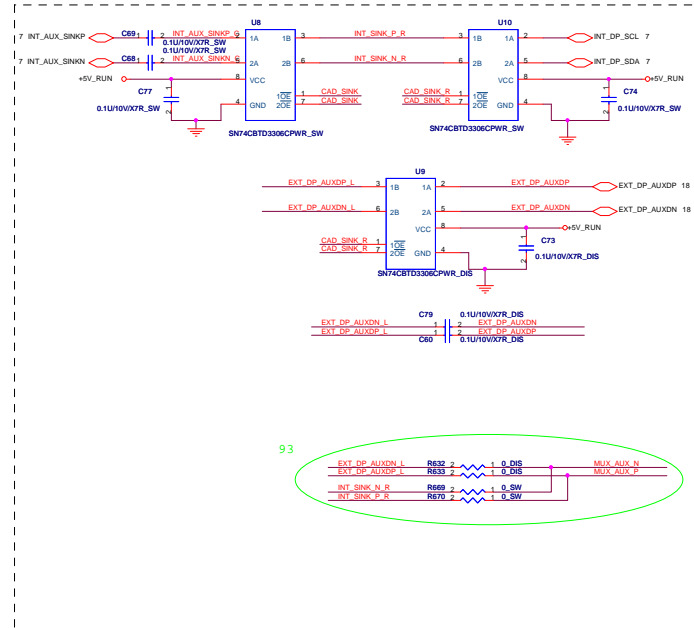
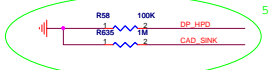
DISPLAY PORT Re-driver



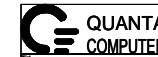
MINI DISPLAY PORT CONNECTOR



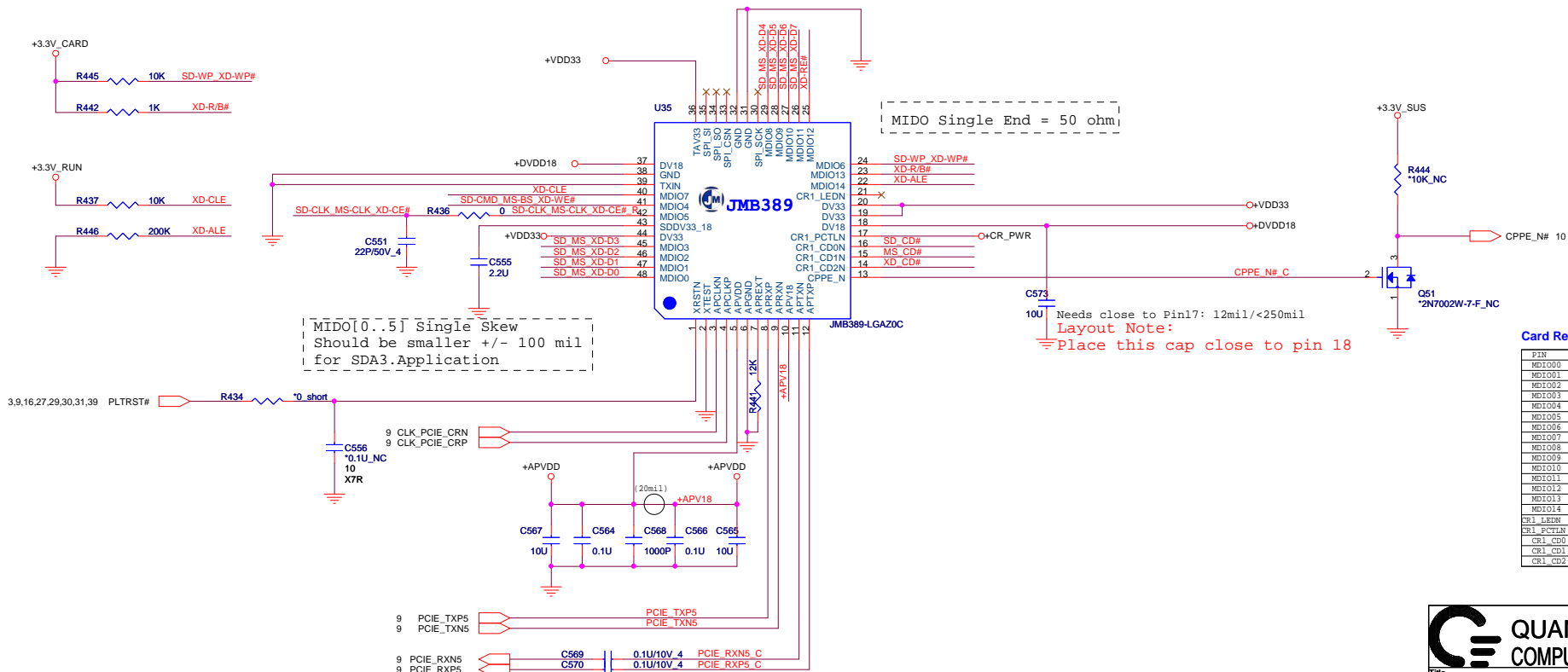
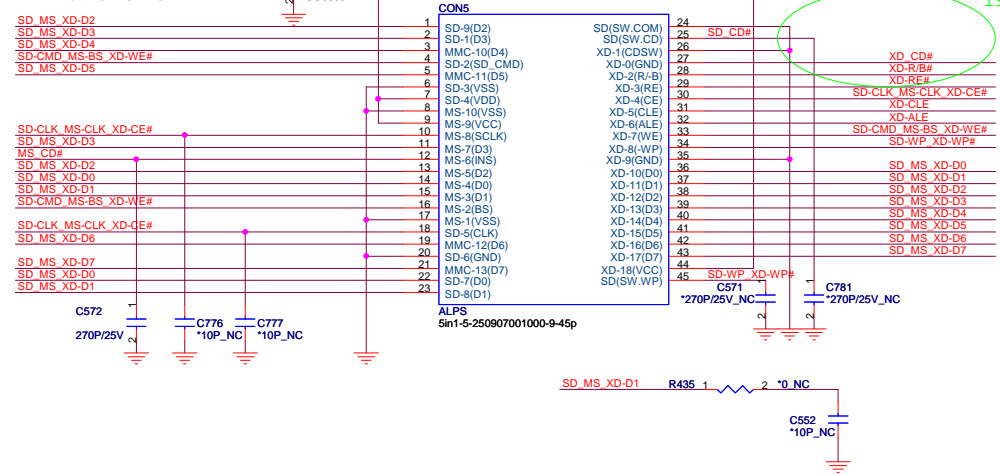
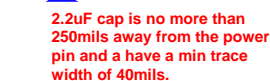
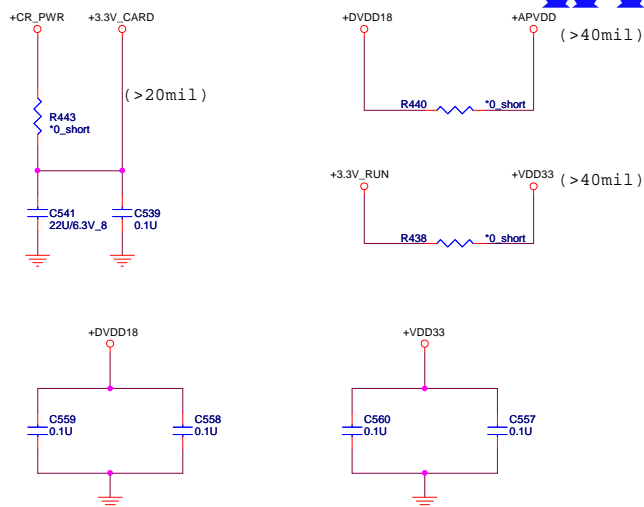
For Mini DP to HDMI and DVI dongle,
SINK(Pin13)=Low, the others is high.



OE	Output
L	A=B
H	Z



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MIDO Single End = 50 ohm

Needs close to Pin17: 12mil/<250mil
Layout Note:
Place this cap close to pin 18

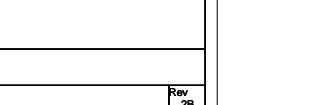
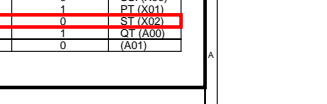
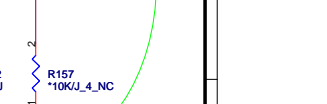
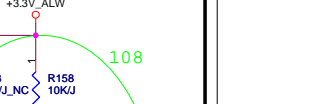
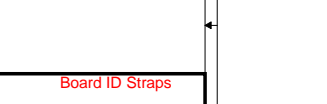
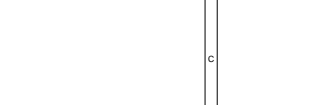
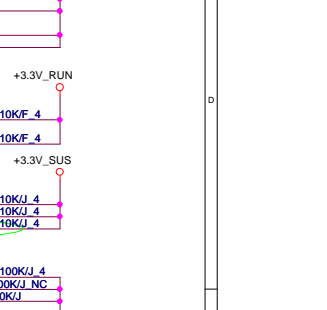
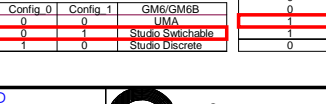
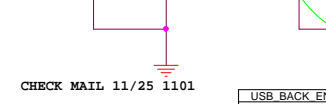
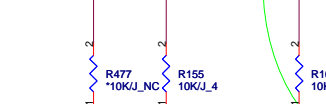
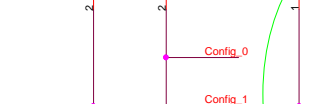
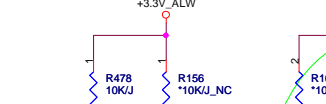
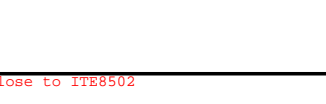
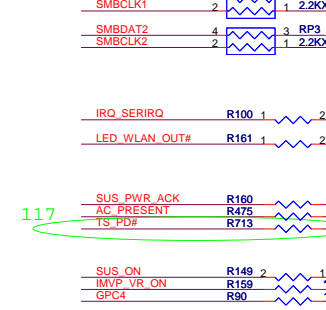
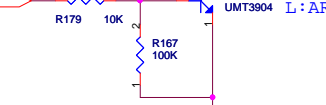
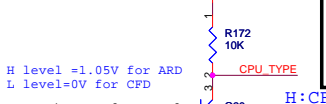
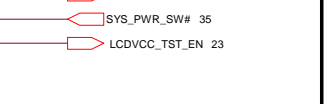
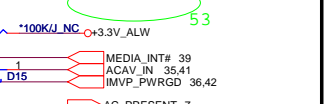
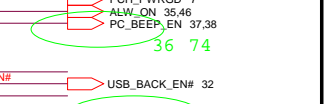
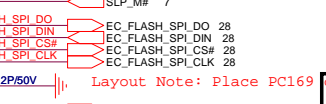
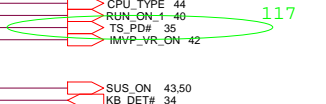
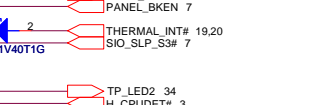
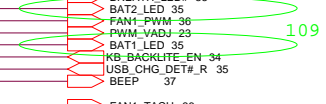
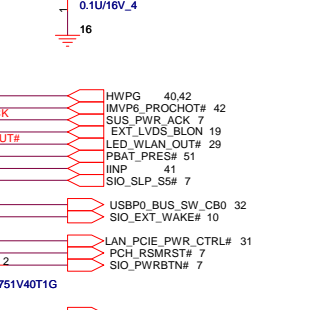
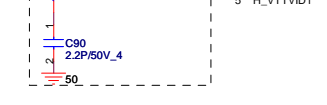
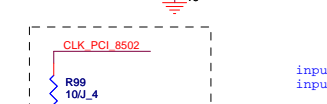
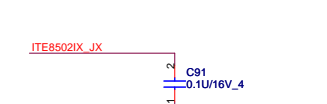
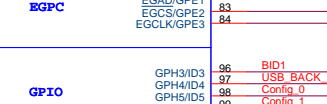
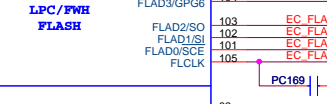
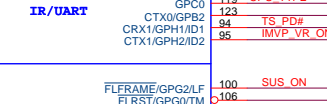
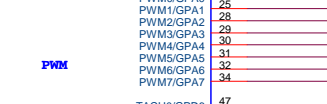
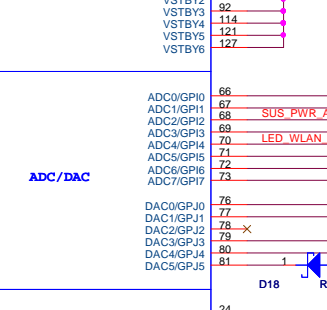
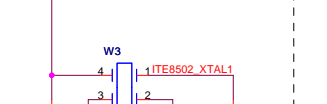
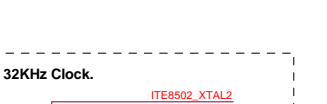
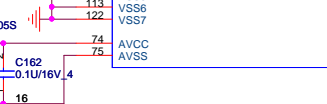
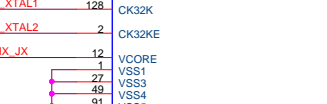
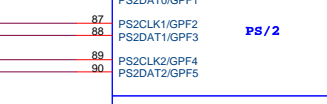
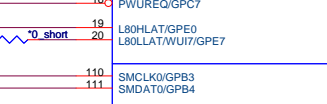
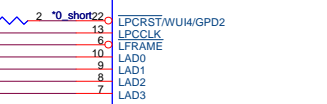
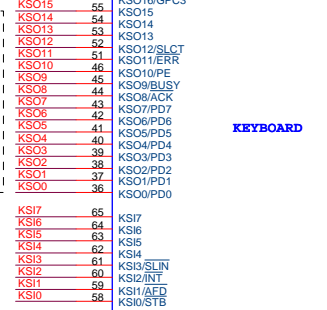
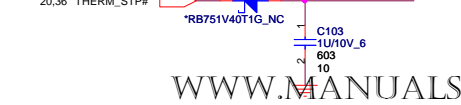
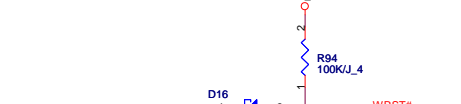
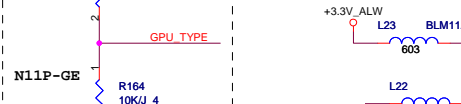
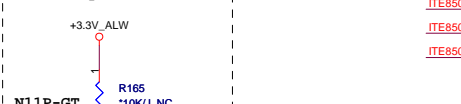
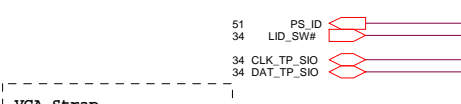
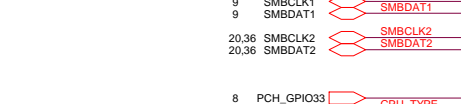
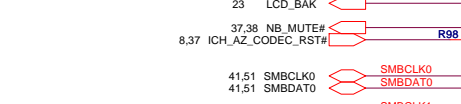
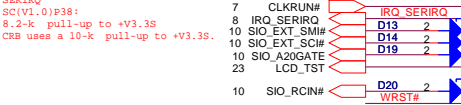
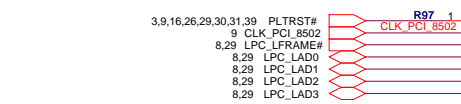
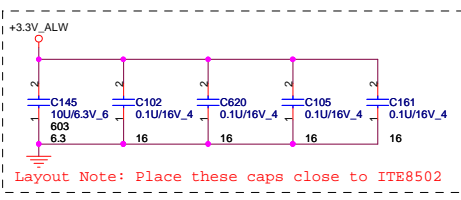
Card Reader interface signal mapping

PIN	Default	SD / MMC	MS	XD
MD1000	SD/MMC/MS/XD	SD	MS	XD
MD1001		SD D1	MS D1	XD D0
MD1002		SD D2	MS D2	XD D3
MD1003		SD D3	MS D3	XD D1
MD1004		SD CMD	MS BS	XD WE#
MD1005		SD CLK	MS CLK	XD CE#
MD1006		SD WP		XD WE#
MD1007				XD CLKS
MD1008		MMC D4	MS D4	XD D4
MD1009		MMC D5	MS D5	XD D5
MD1010		MMC D6	MS D6	XD D6
MD1011		MMC D7	MS D7	XD D7
MD1012				XD R#
MD1013				XD B#
MD1014				XD ALE
CR1_LERN		SD LER#	MS LER#	XD LER#
CR1_PCTIN		SD PPR#	MS PPR#	XD PPR#
CR1_CD0		SD CD#		
CR1_CD1			MS CD#	
CR1_CD2				XD CD#



Title			
Card Reader 8 IN 1			
Size	Document Number	Rev	
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ITE8502E LQFP-128L



Board ID Straps

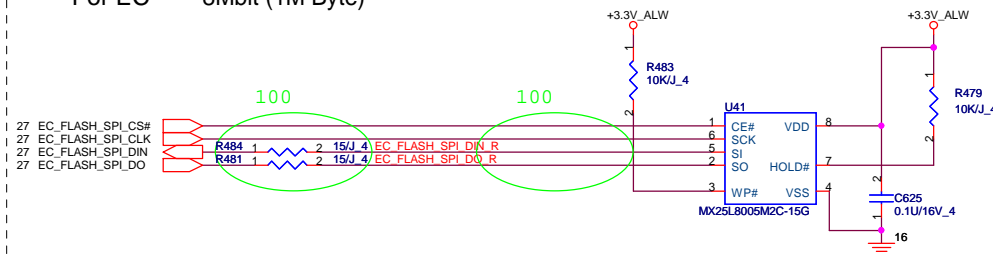
Layout Note: Place PC169 close to ITE8502

Layout Note: Place PC169 close to ITE8502

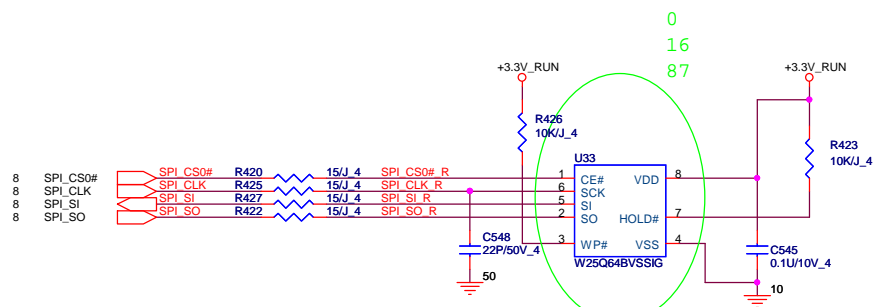
CHECK MAIL 11/25 1101

Config. 0	Config. 1	GM6/GM6B	SS1 (X00)	PT (X01)	ST (X02)	Q1 (A00)
0	0	UMA	0	0	0	0
1	0	Studio Switchable	1	0	1	1
1	0	Studio Discrete	0	0	0	0

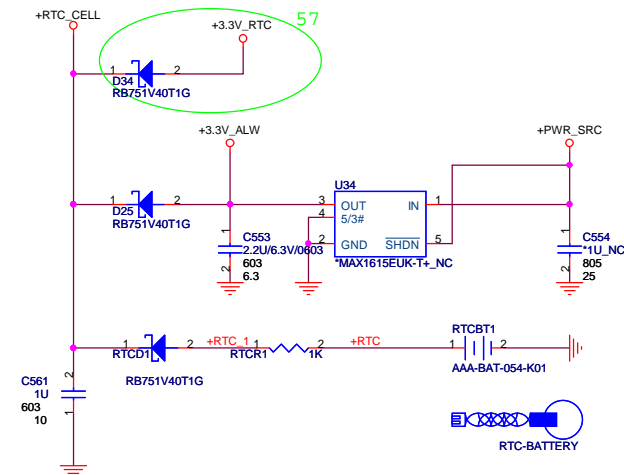
For EC 8Mbit (1M Byte)



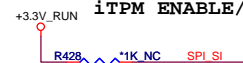
For PCH 32Mbit (4M Byte)



RTC BATTERY

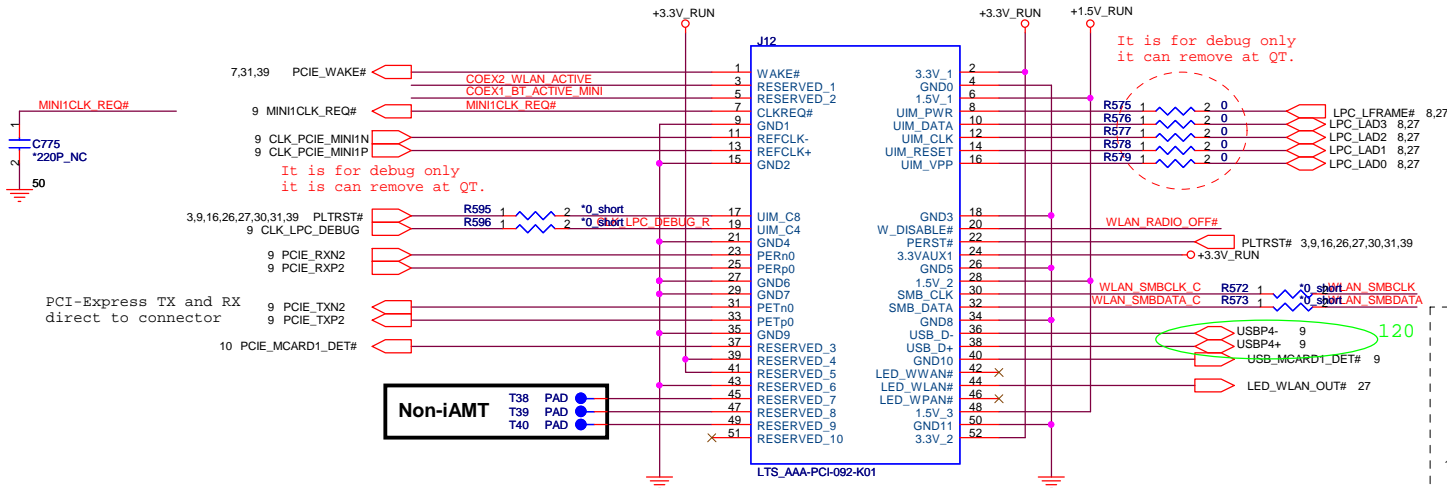


iTPM ENABLE/DISABLE



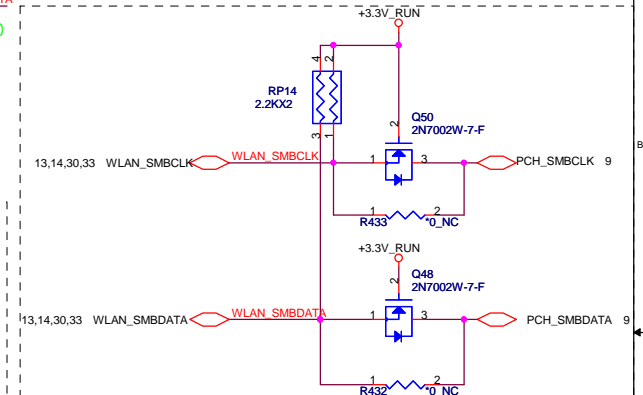
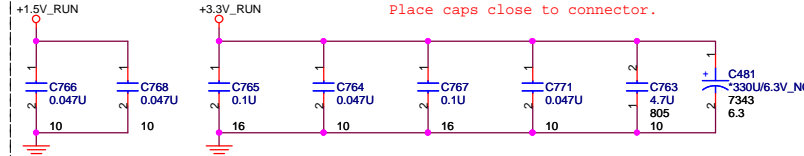
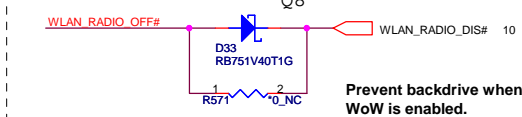
TPM Function	R428
Enable	Mount
Disable	NC (Default)

MiniCard WLAN connector

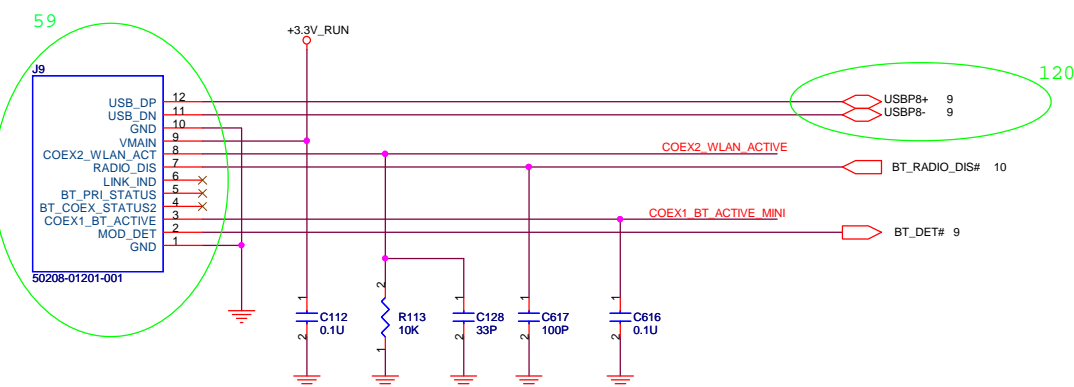


55
81
120

Support for WoW

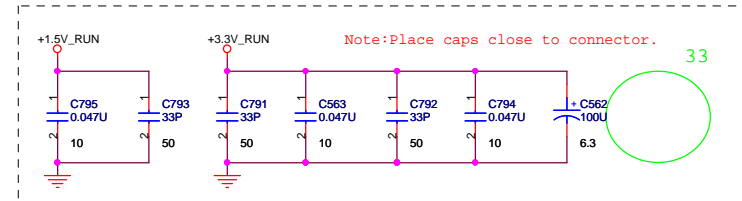
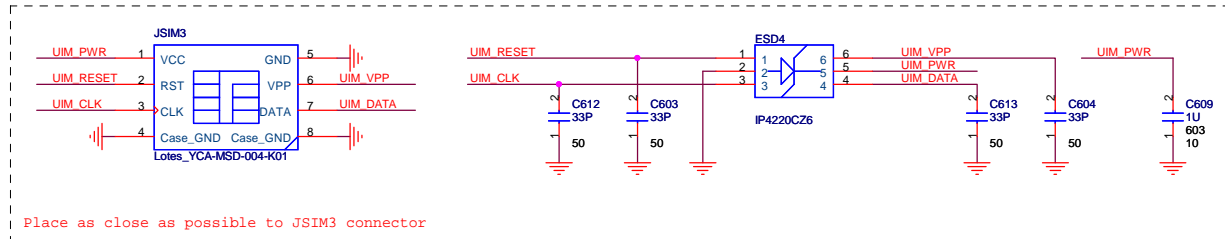
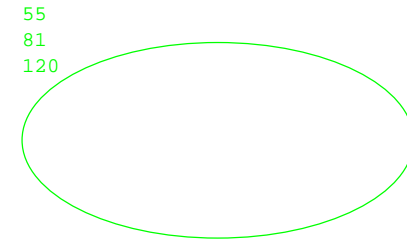
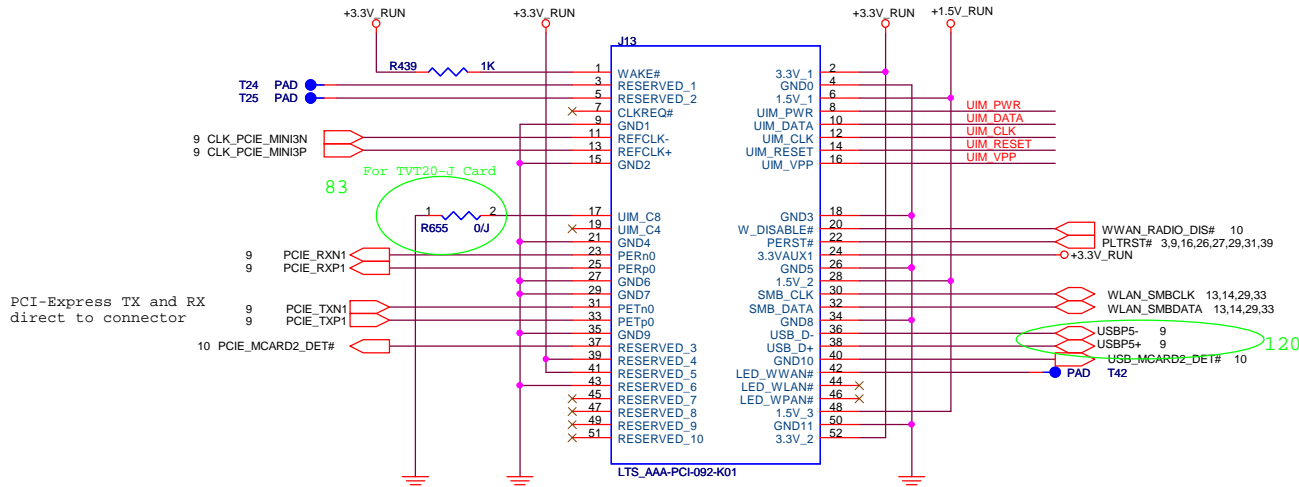


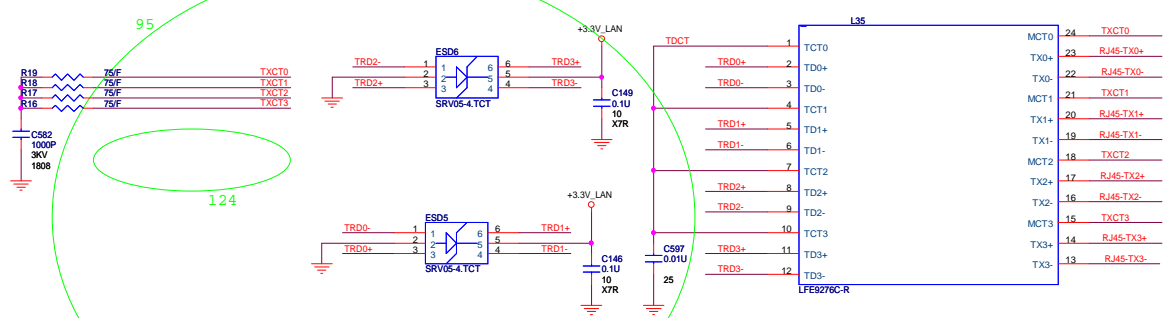
Support Dell BT375 (Little Stone) module (XPS) W TO B



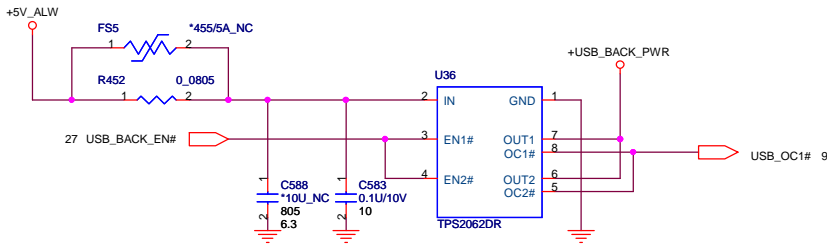
55
81
120

MiniCard WWAN connector

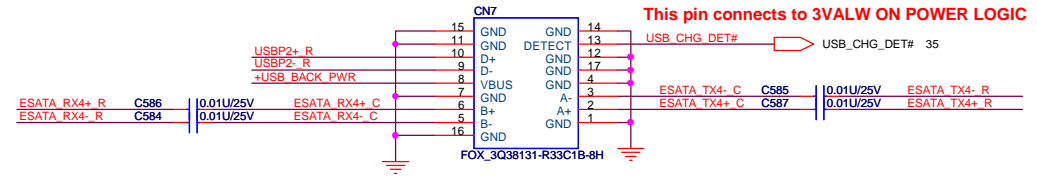
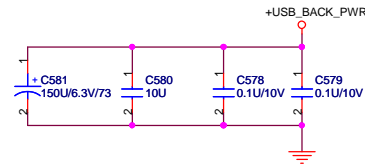




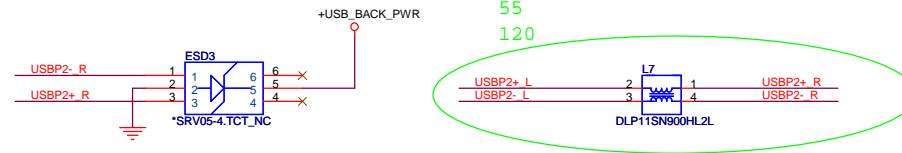
ESATA + USB Conn + Power Share



USB_BACK_EN# needs to be low when system S3 and S5 for USB charge

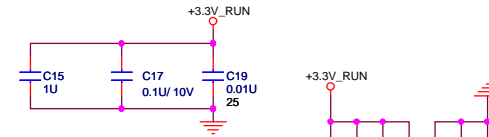


This pin connects to 3VALW ON POWER LOGIC



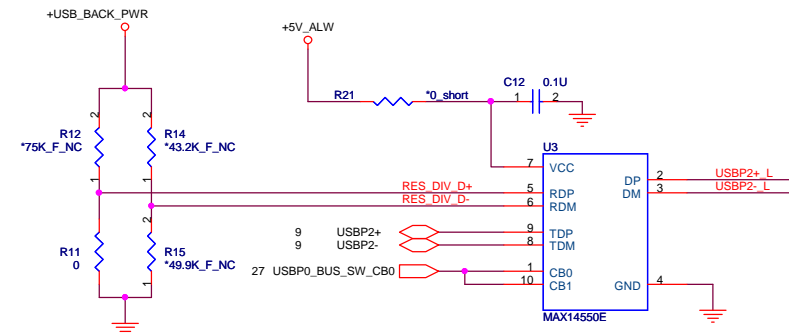
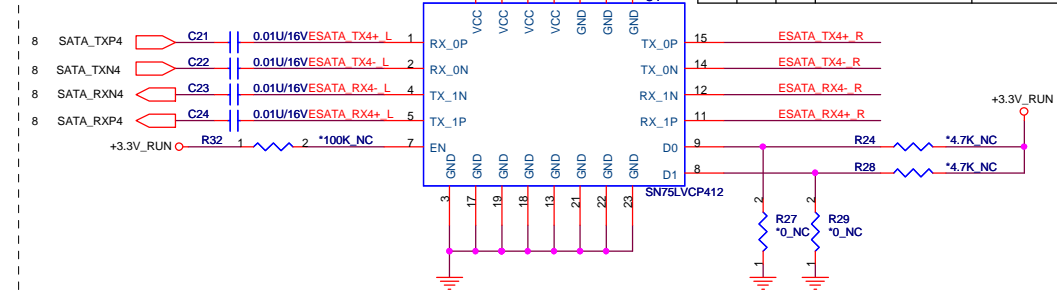
E-SATA Re-driver

Layout Note: Please put those on the same side of MB PCB



Note: Boost:5dB, Standard SATA:0dB

EN	D0	D1	CH : 0	CH : 1
0	X	X	Standby	Standby
1	0	0	Standard SATA	Standard SATA
1	1	0	Boost	Standard SATA
1	0	1	Standard SATA	Boost
1	1	1	Boost	Boost



EC needs to drive CB0/CB1 pins to low when system S3/S5 and drive high when system S0.

U49 PN and Footprint needs to double check

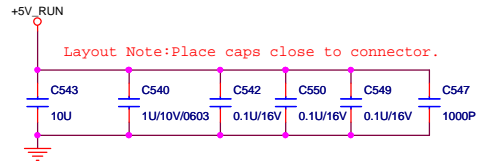
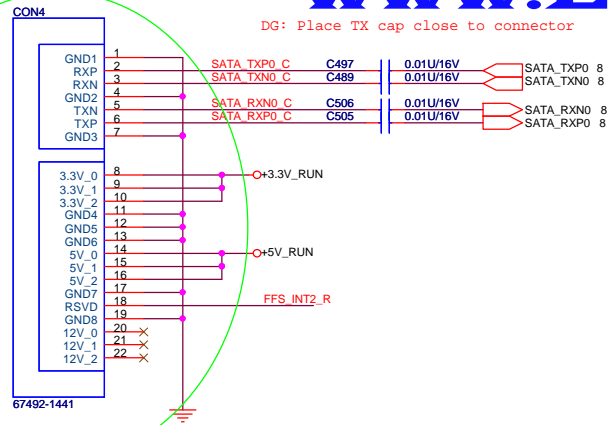
R15 needs to be 49.9K_F if we use external resistors.

CB0	CB1	Function
0	0	Auto Detection active
1	1	USB Function only

(5V)-43.2K-(D)-49.9K-GND (about 2.68V)
(5V)-75.0K-(D+)-49.9K-GND (about 2.00V)

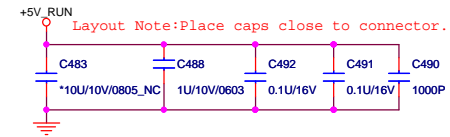
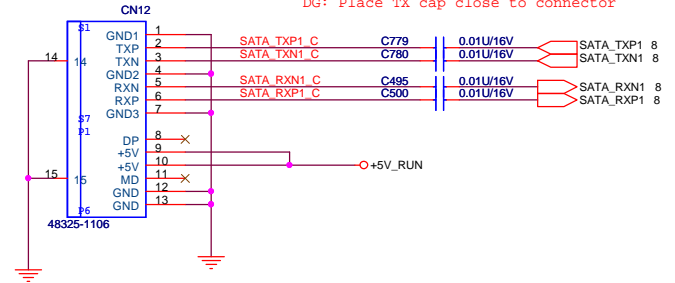
SATA Connector.

60

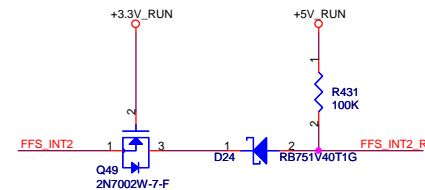
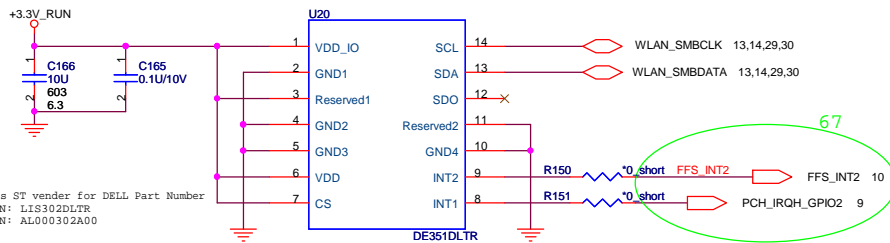


ODP Connector

DG: Place TX cap close to connector



3-axis Fall Sensor (HDD data protector)



ON:White light on
OFF:Amber light on



KEYBOARD CONNECTOR



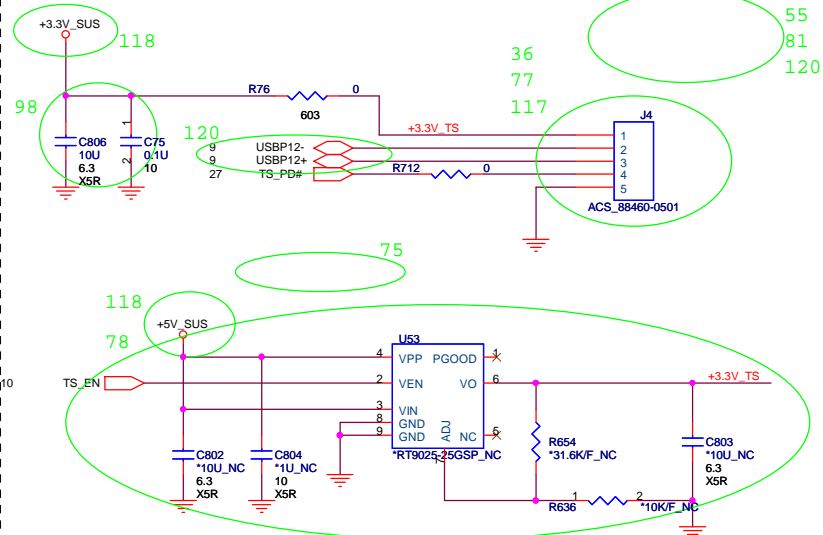
Layout Note: 100P CAPS CLOSE TO JKB3

Key board illumination

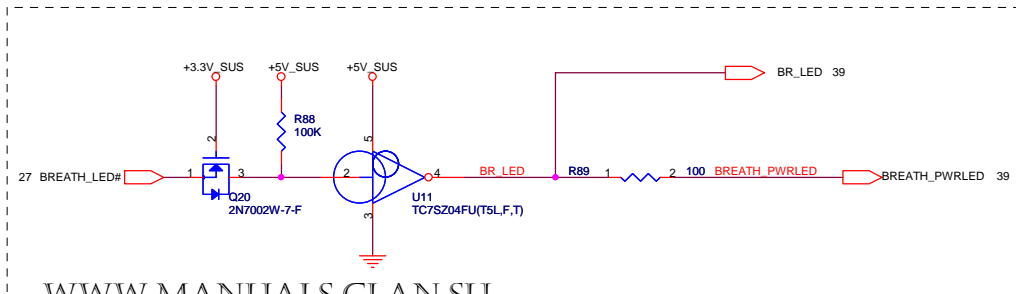
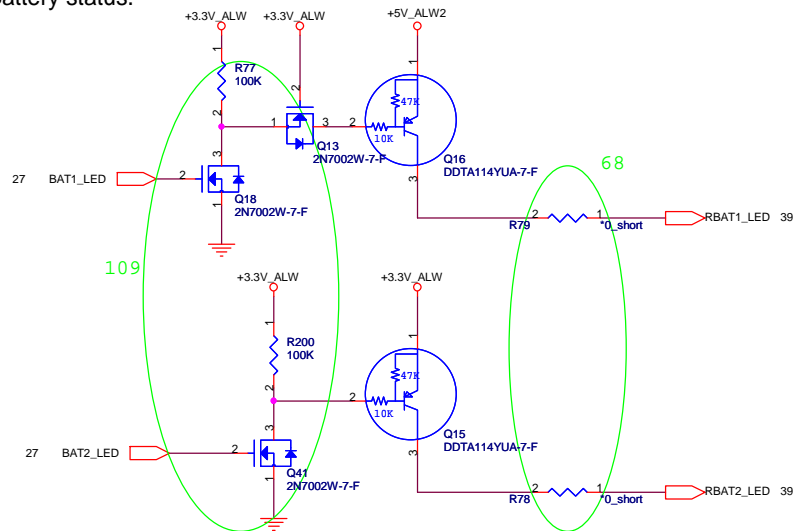
```
+KB_LED power trace width >10 mil
```



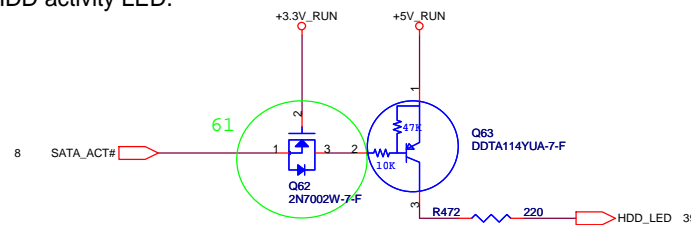
Touch Screen Module



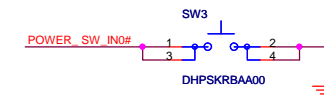
Battery status.



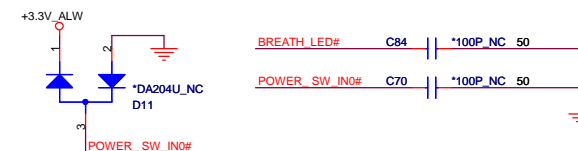
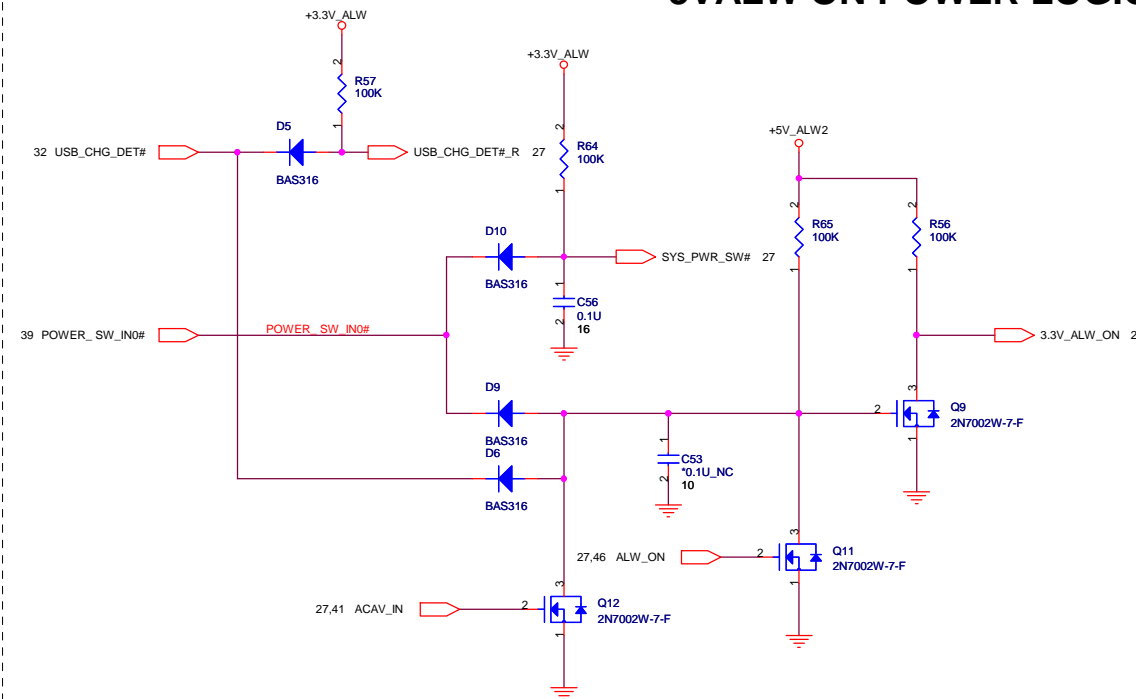
HDD activity LED.

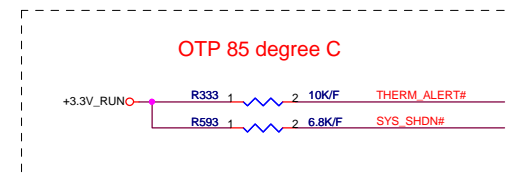
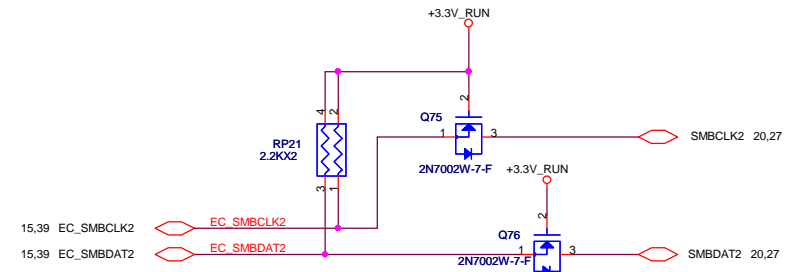
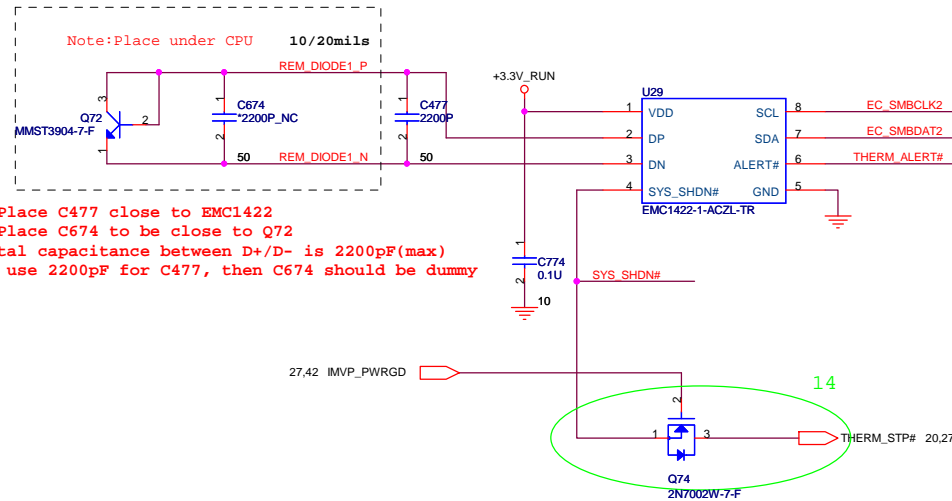
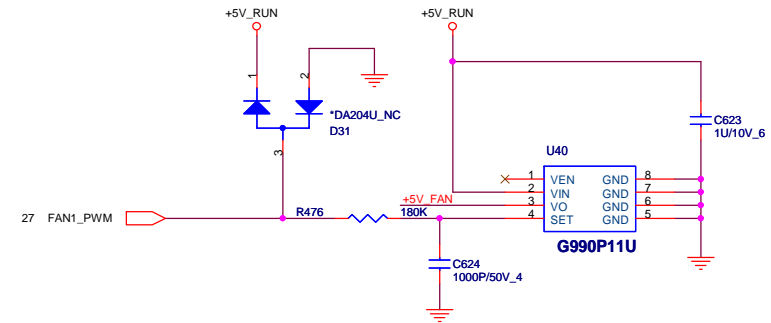
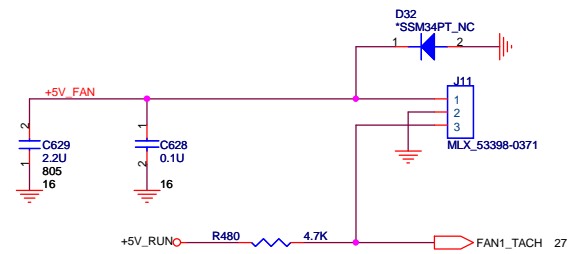


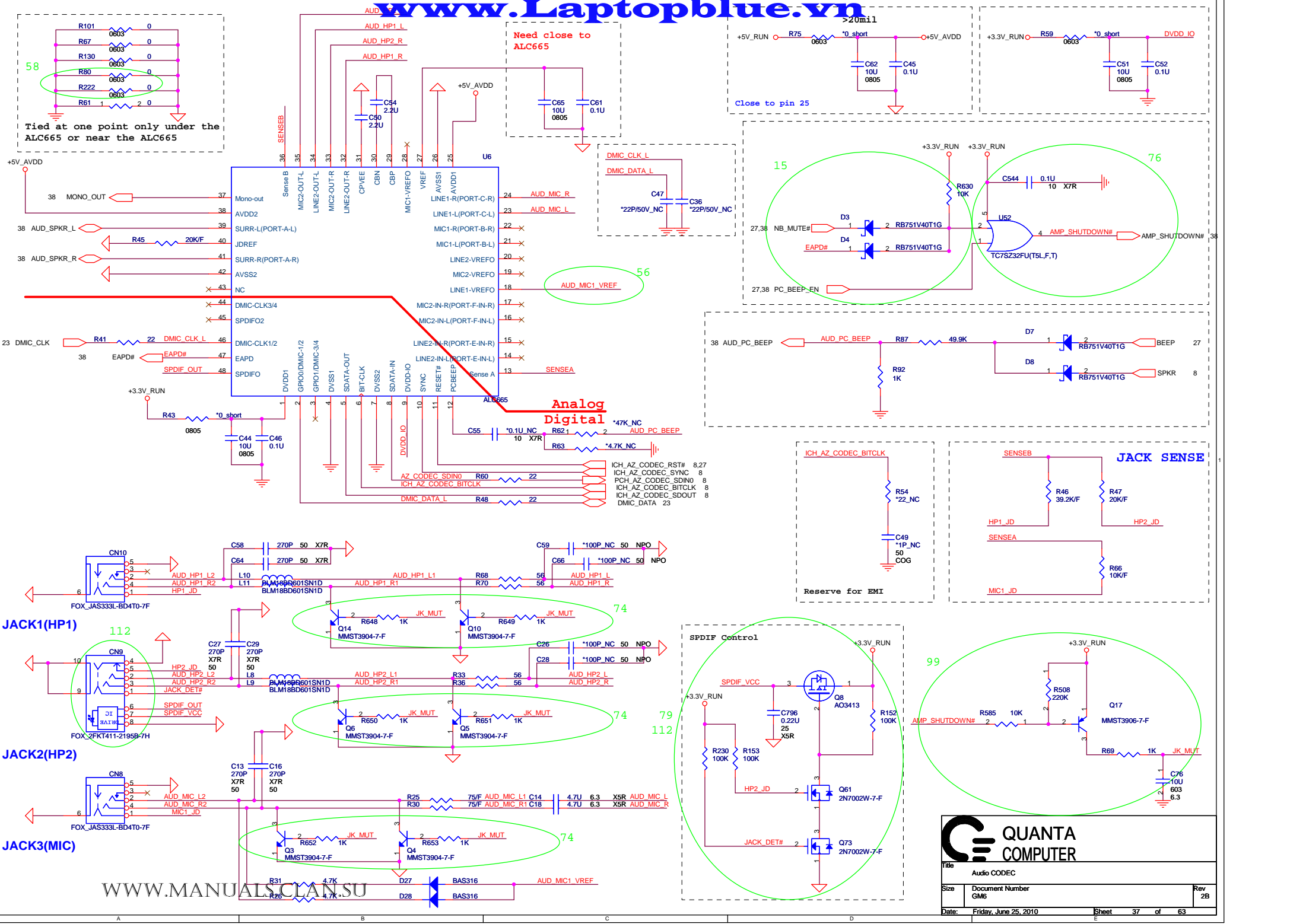
Power button for Engineer




3VALW ON POWER LOGIC

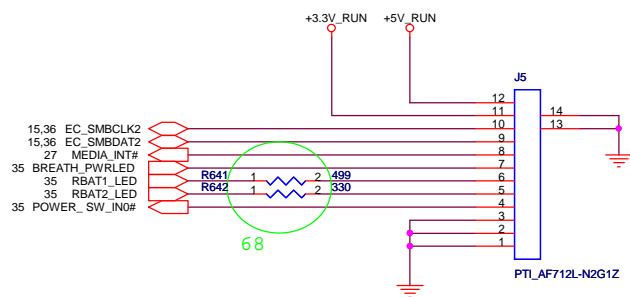
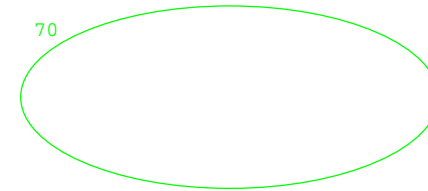
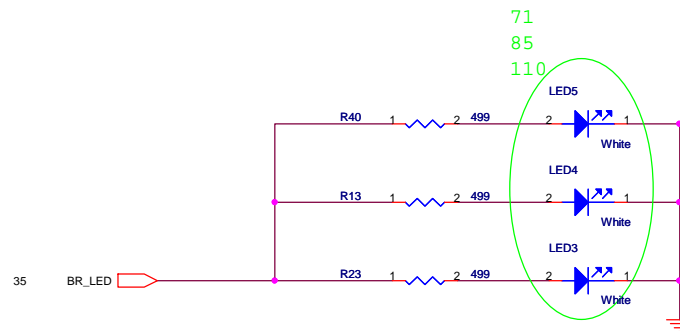
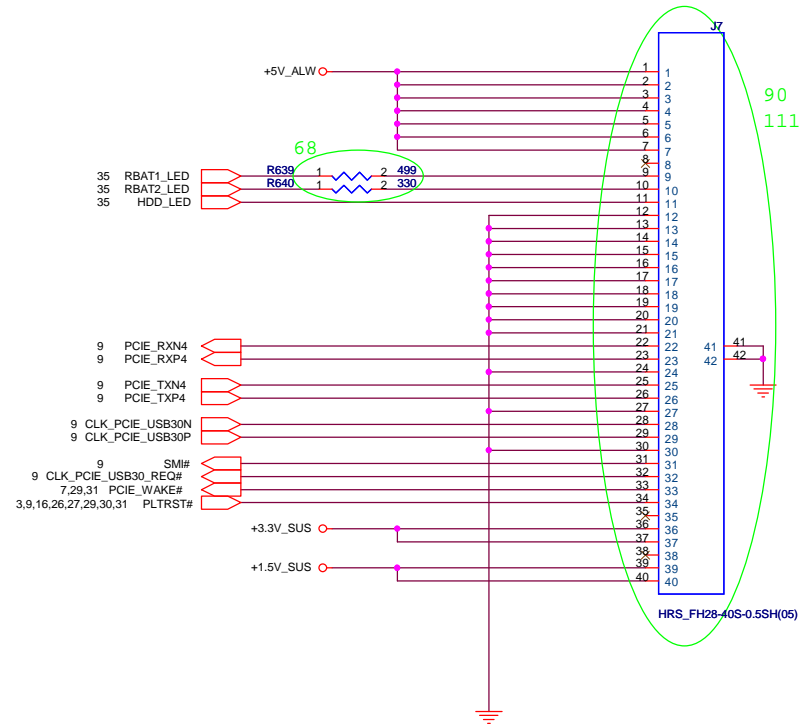


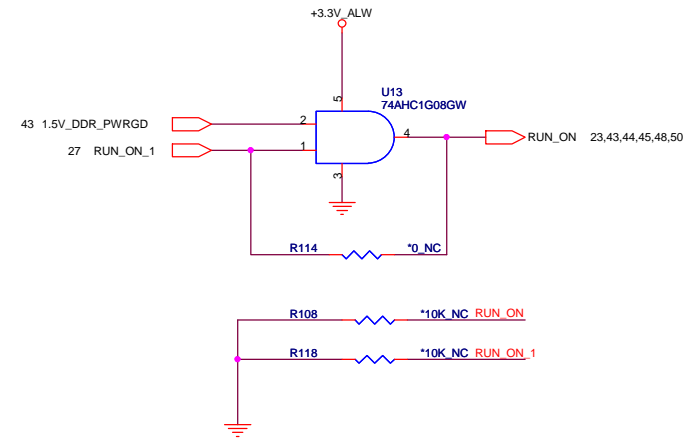
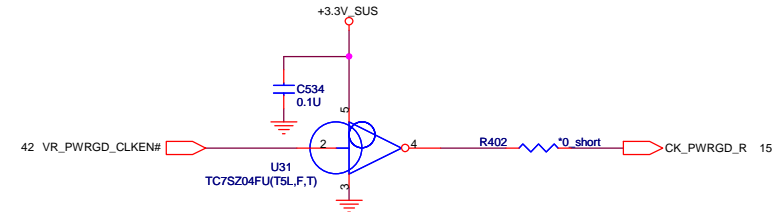
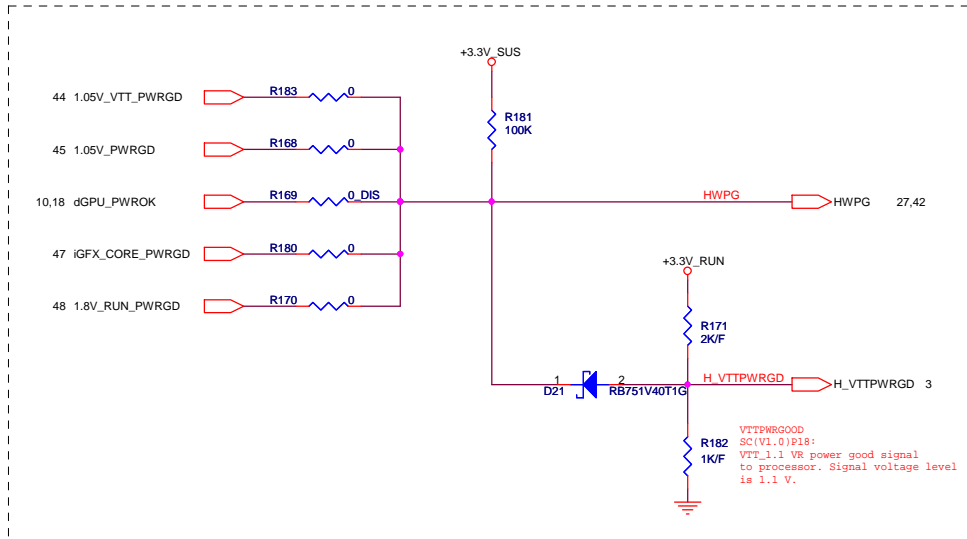


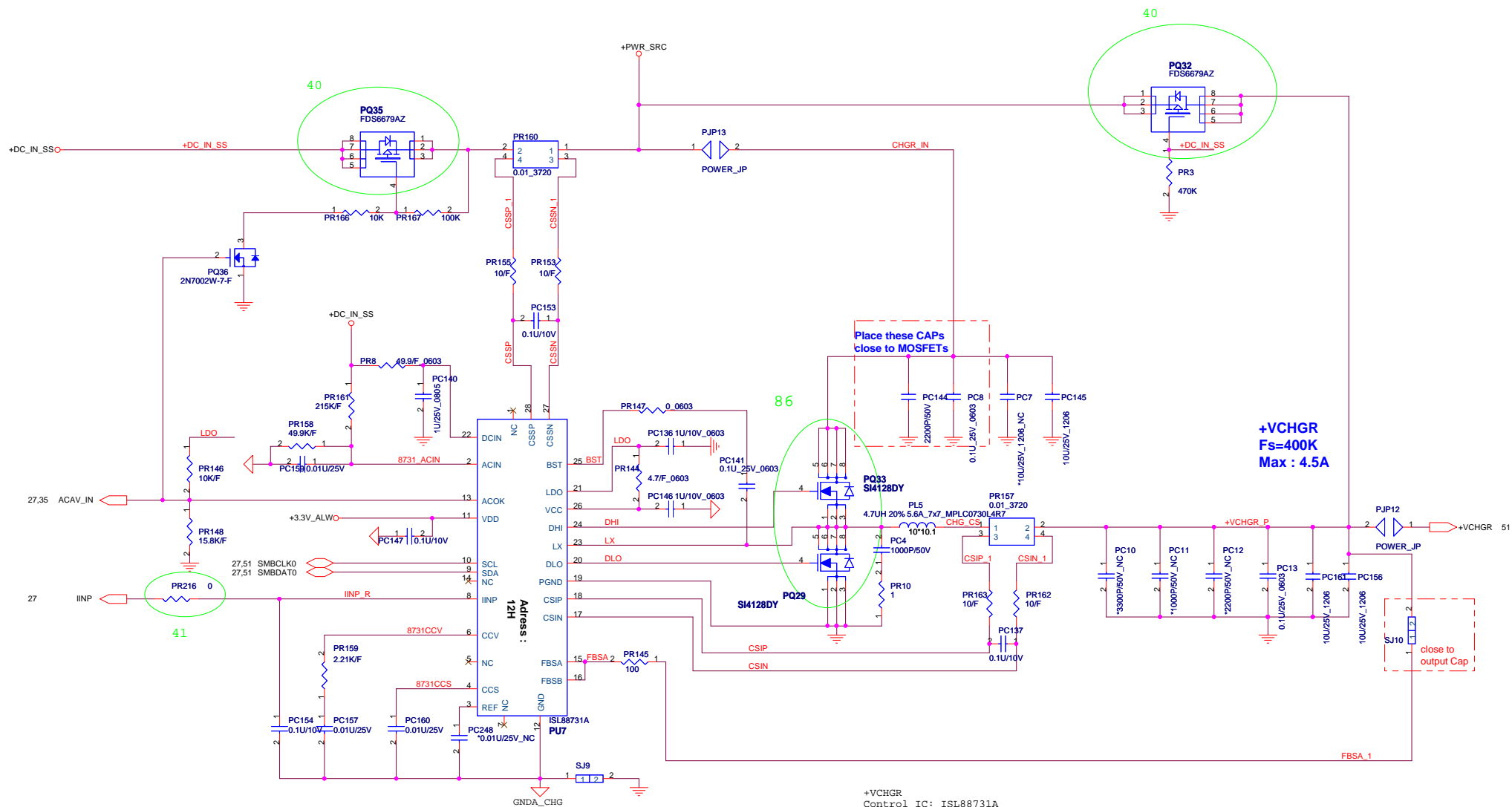




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AUDIO AMP				
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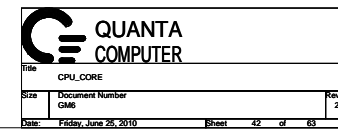


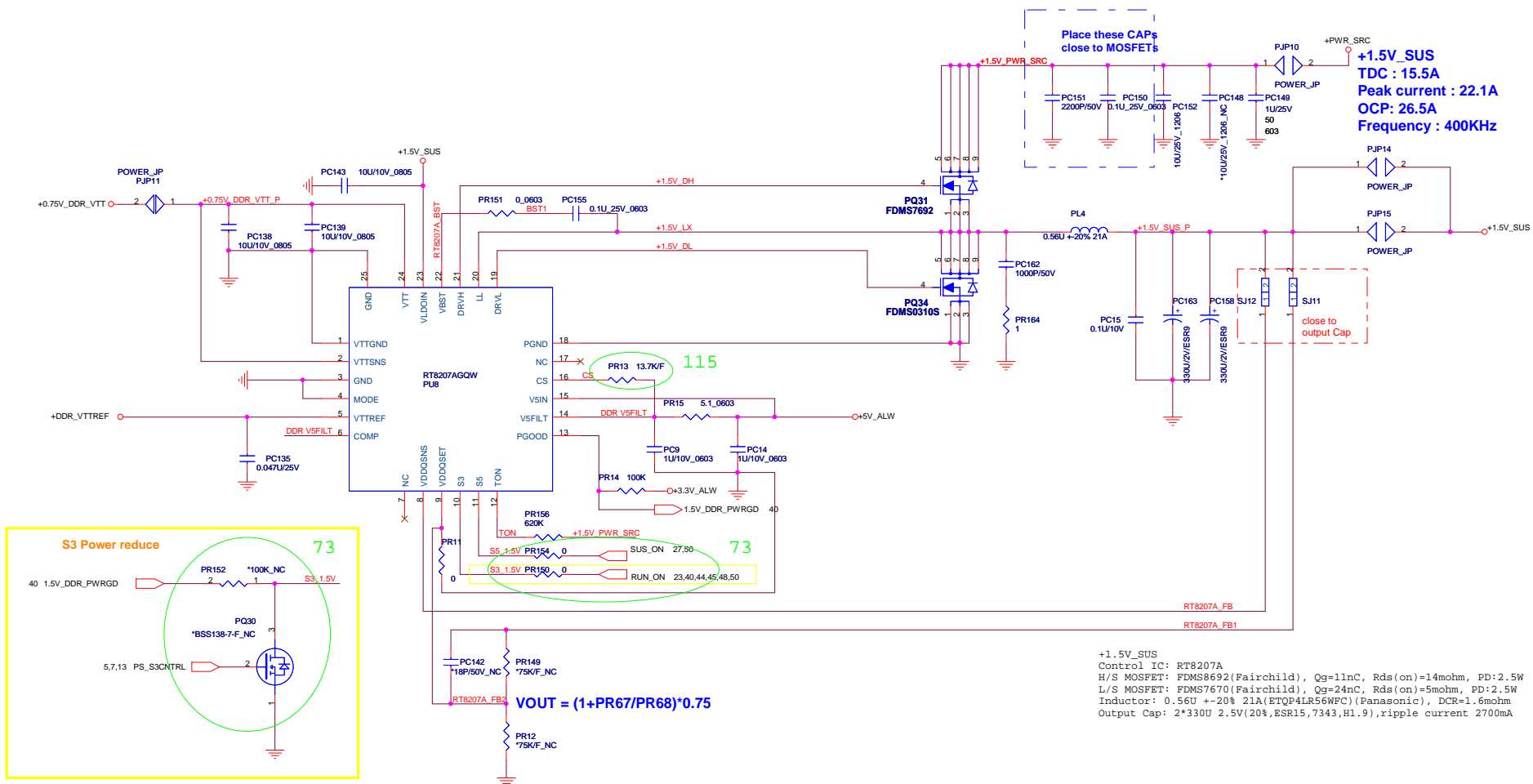
```
+VCHGR
Control IC: ISL88731A
H/S MOSFET: FDS8884(Fairchild), Qg=13nC, Rds(on)=30mohm, PD=2.5W
L/S MOSFET: FDS8884(Fairchild), Qg=13nC, Rds(on)=30mohm, PD=2.5W
Inductor: 5.8UH +/-30% 5.5A SDSL10D40F-5R8Y(TTA), DCR=21mohm
Output Cap: 2*10U 25V(+/-10%,X6S,1206)
```



Title	Charger (ISL88731)
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VDDQ and VTT discharge control

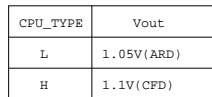
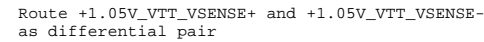
MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

VDDQ output voltage selection

VDDQSET	VDDQ(V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQSNS/2	DDR3
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

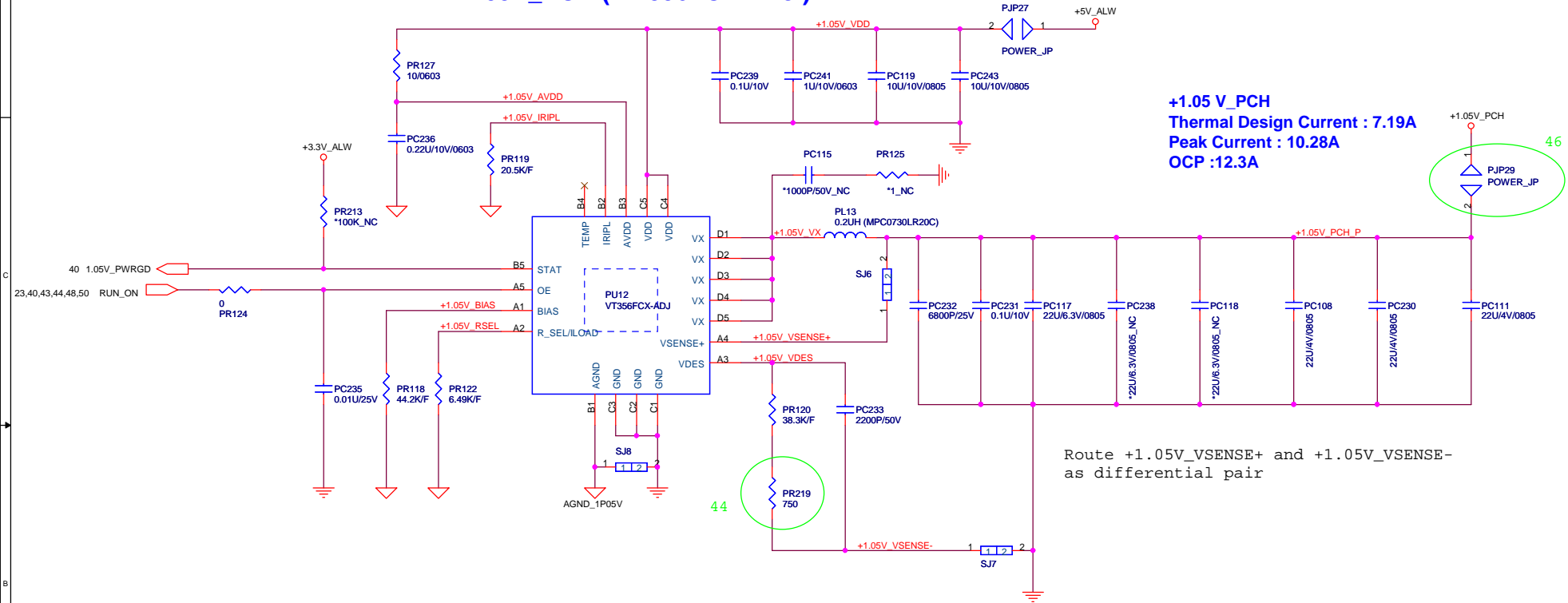
Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)

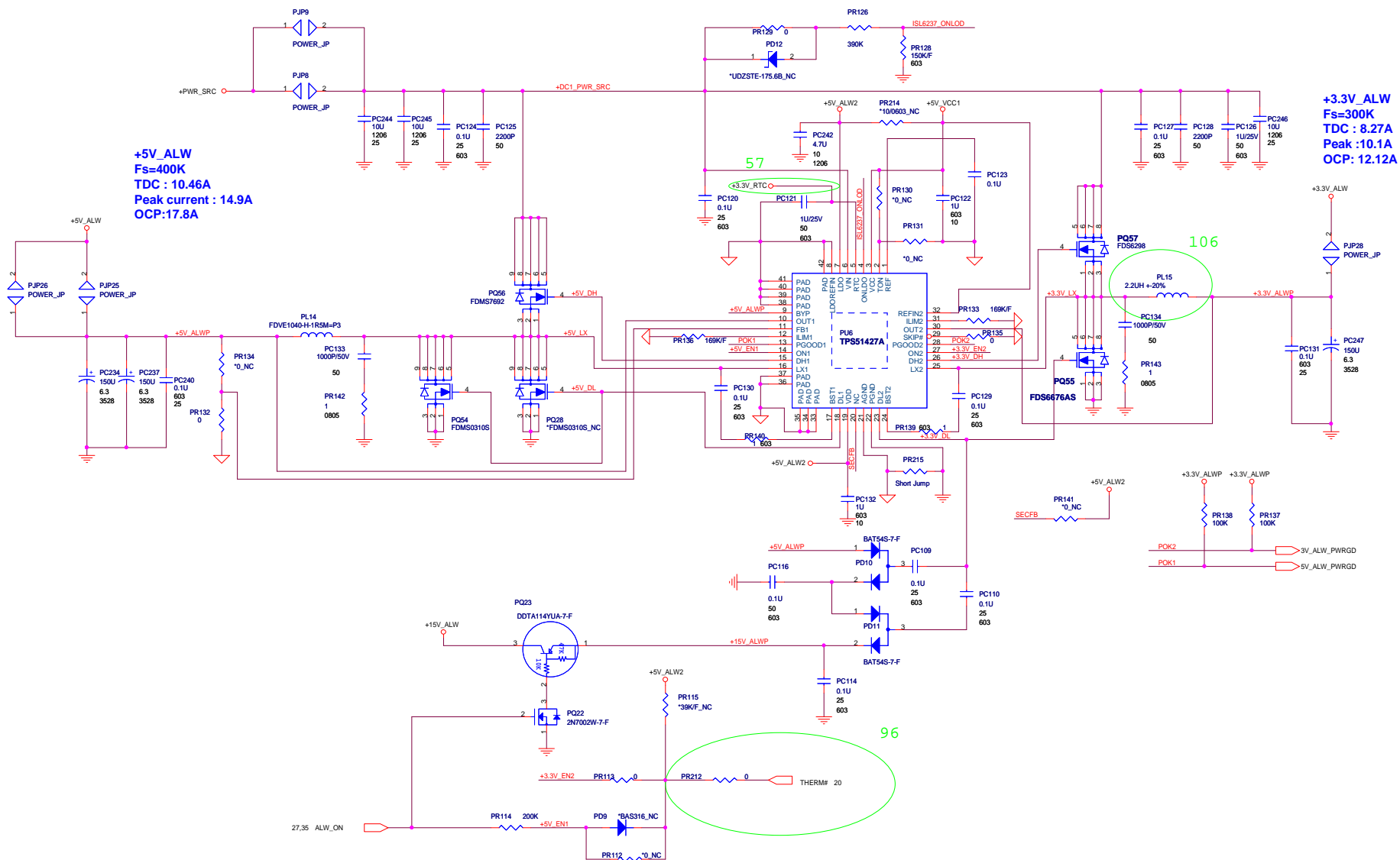


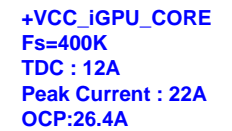
+1.05V_PCH (VT356FCX-ADJ)

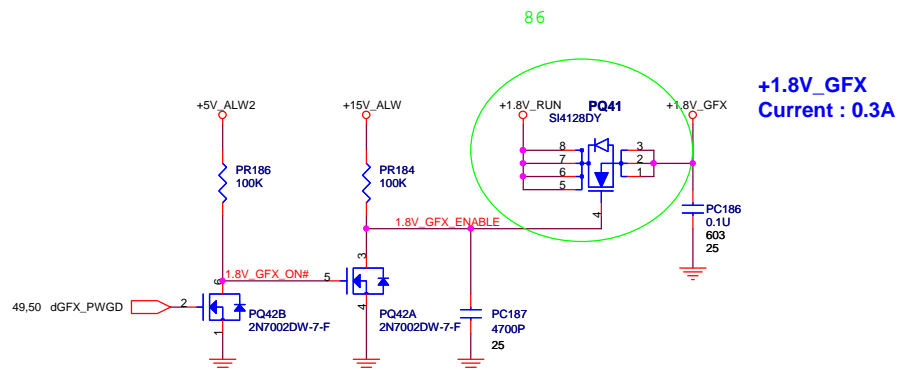
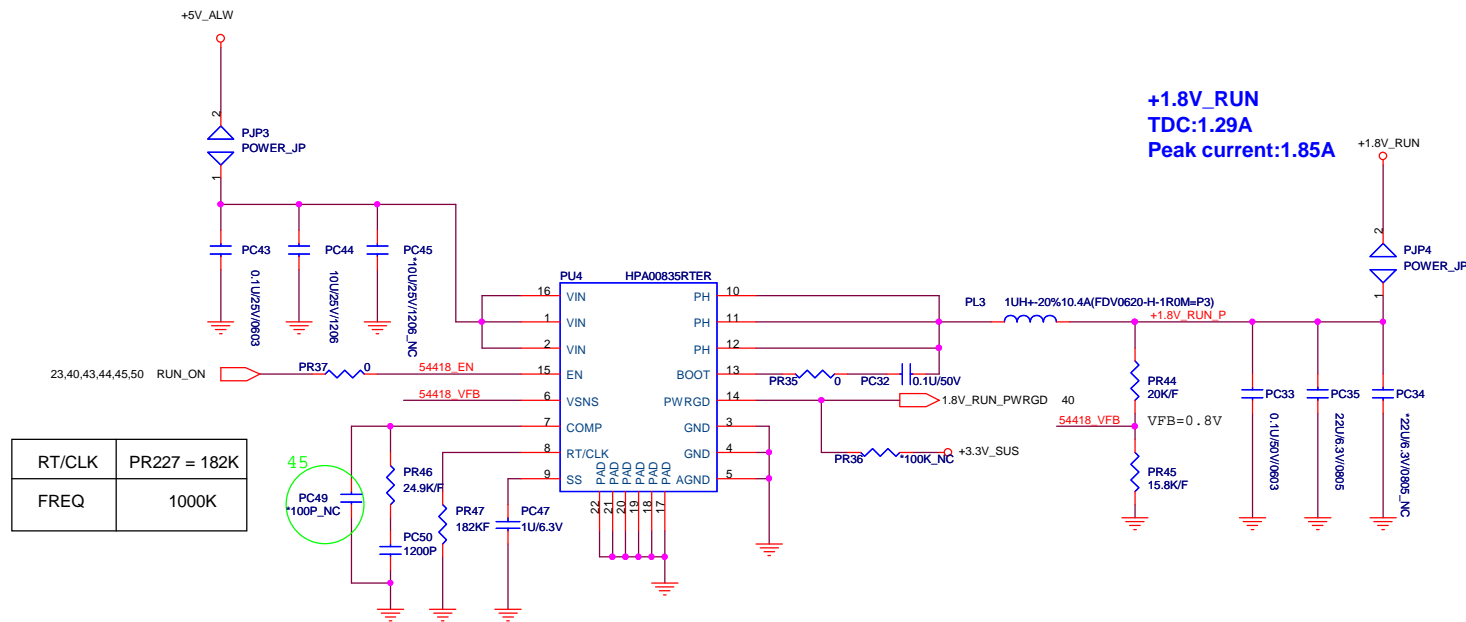
+1.05 V_PCH
Thermal Design Current : 7.19A
Peak Current : 10.28A
OCP :12.3A

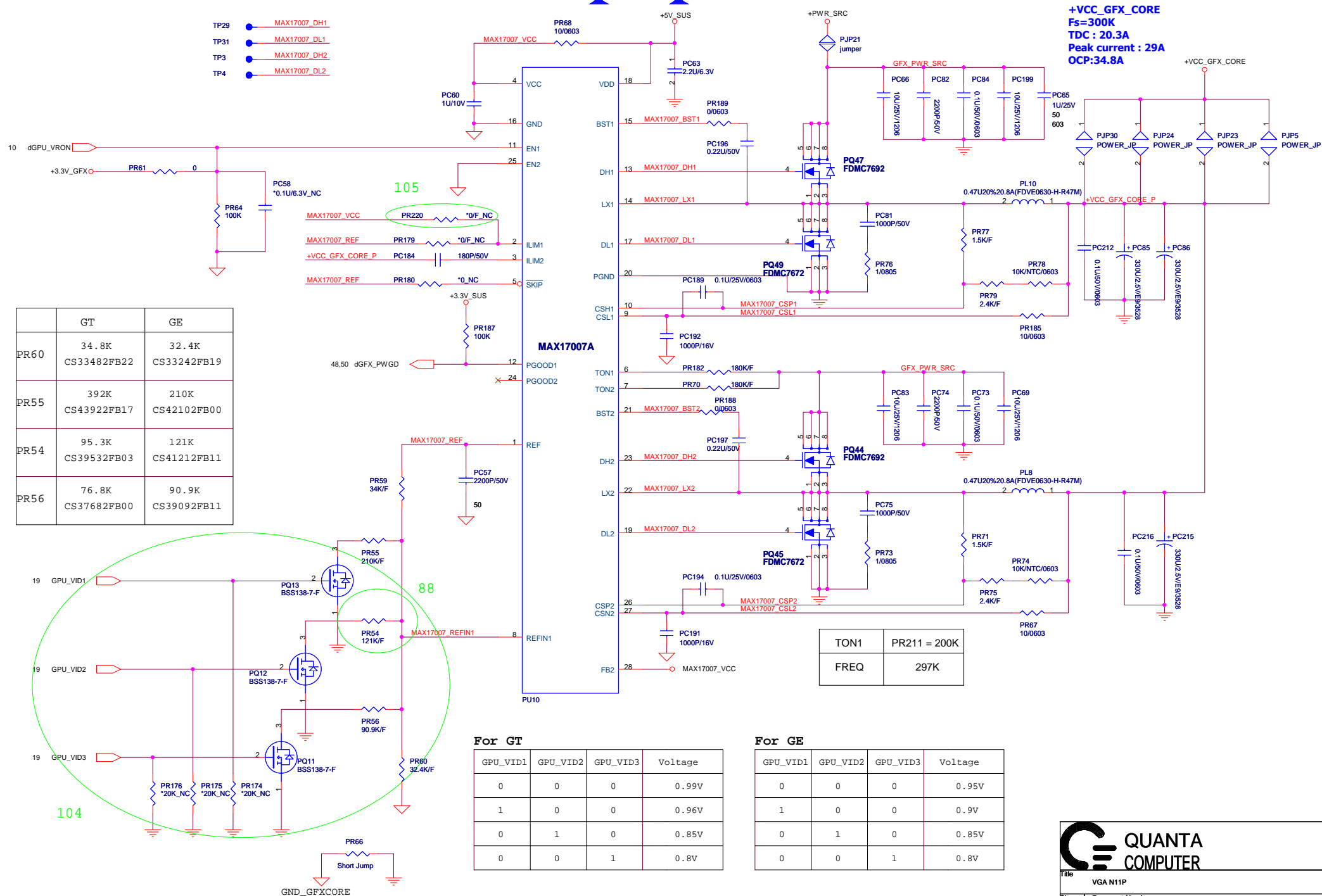


Route +1.05V_VSENSE+ and +1.05V_VSENSE- as differential pair



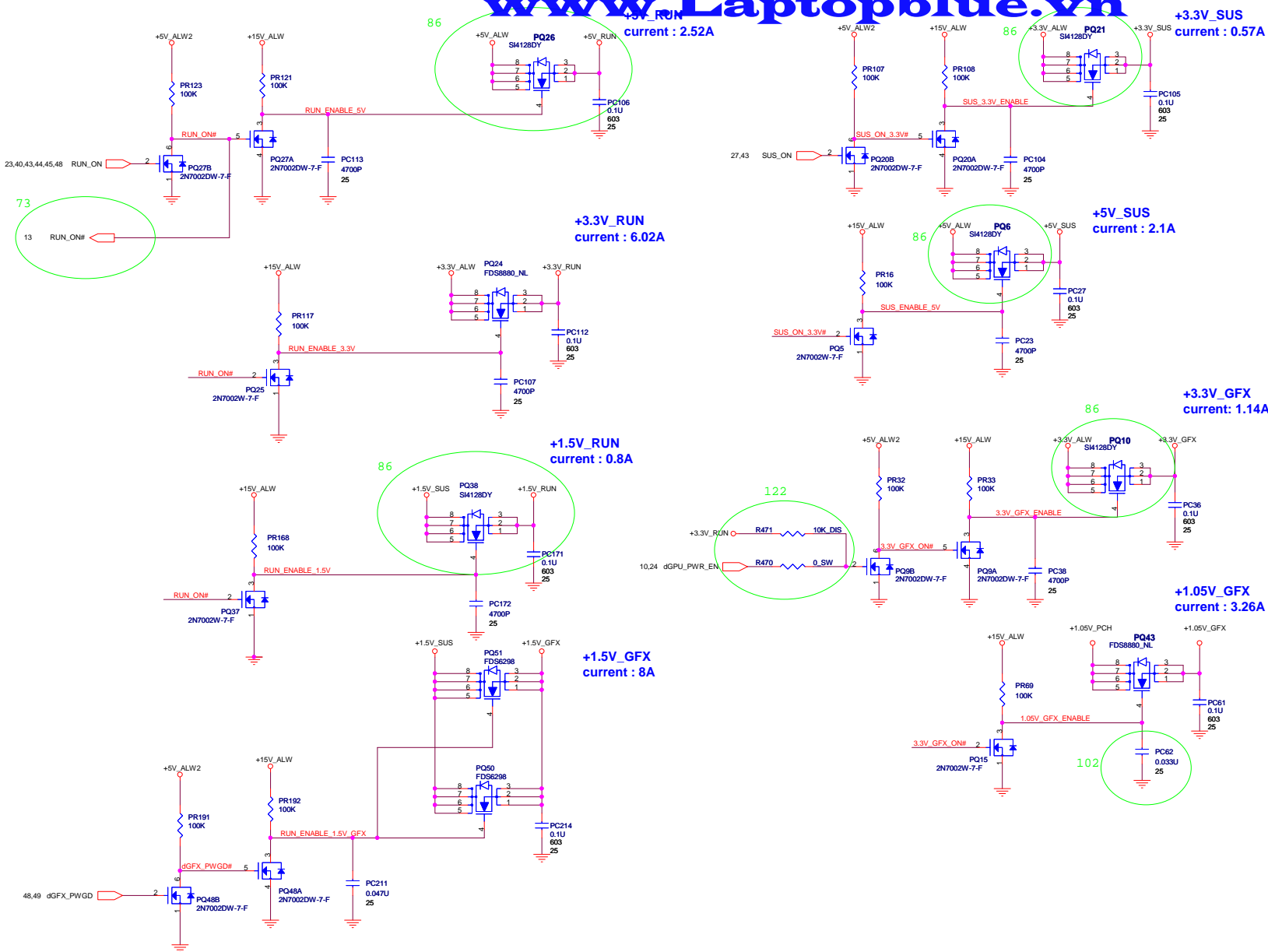




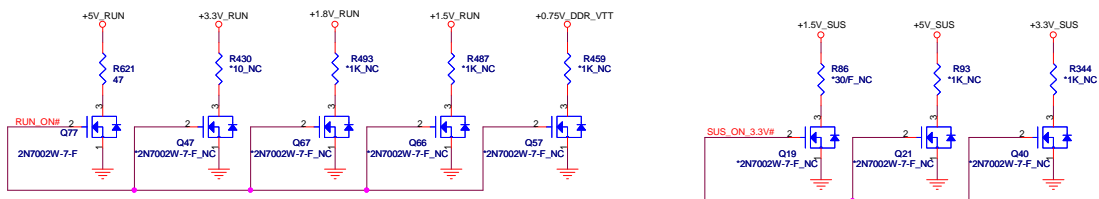


For GT			
GPU_VID1	GPU_VID2	GPU_VID3	Voltage
0	0	0	0.99V
1	0	0	0.96V
0	1	0	0.85V
0	0	1	0.8V

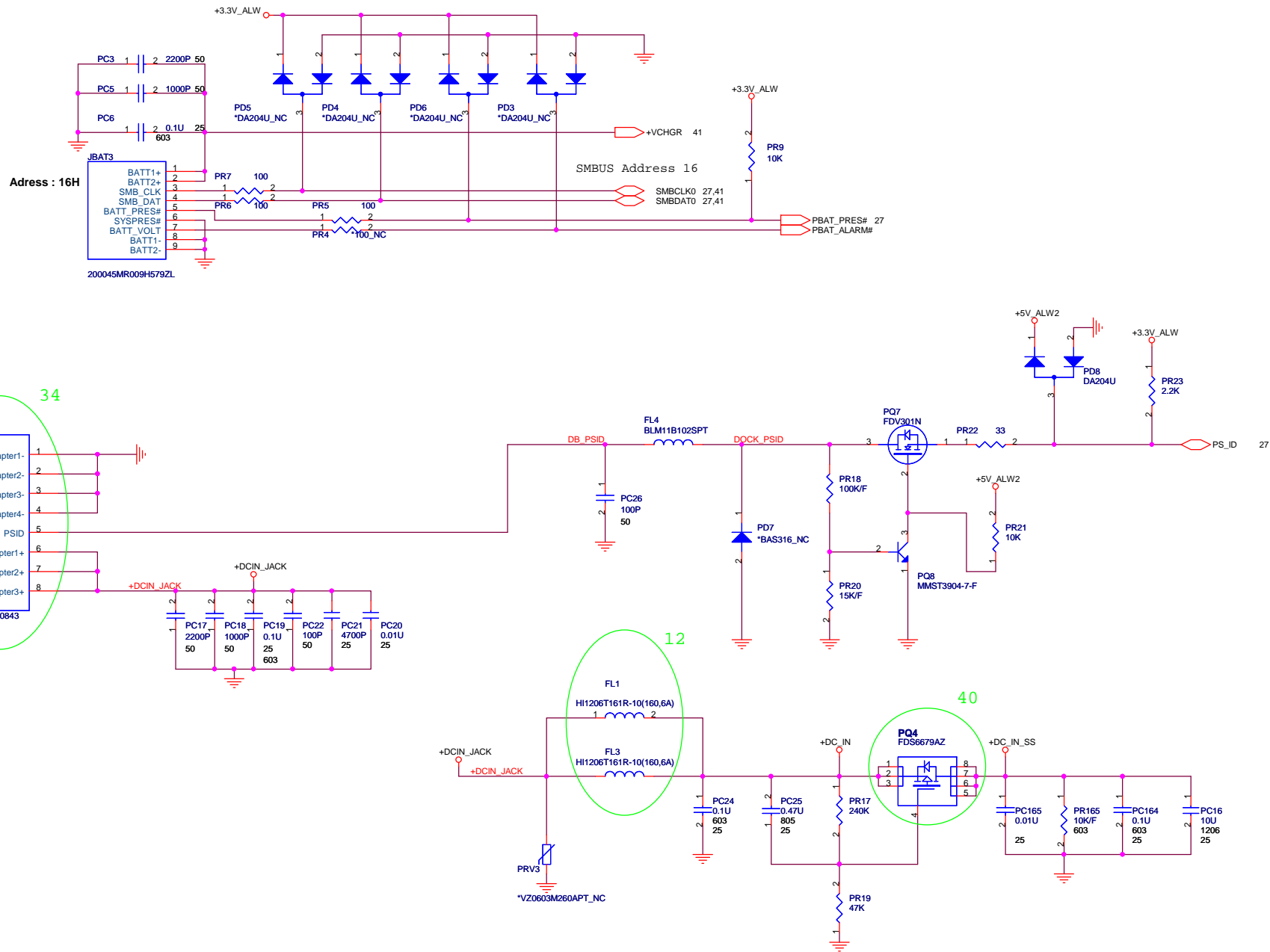
For GE			
GPU_VID1	GPU_VID2	GPU_VID3	Voltage
0	0	0	0.95V
1	0	0	0.9V
0	1	0	0.85V
0	0	1	0.8V

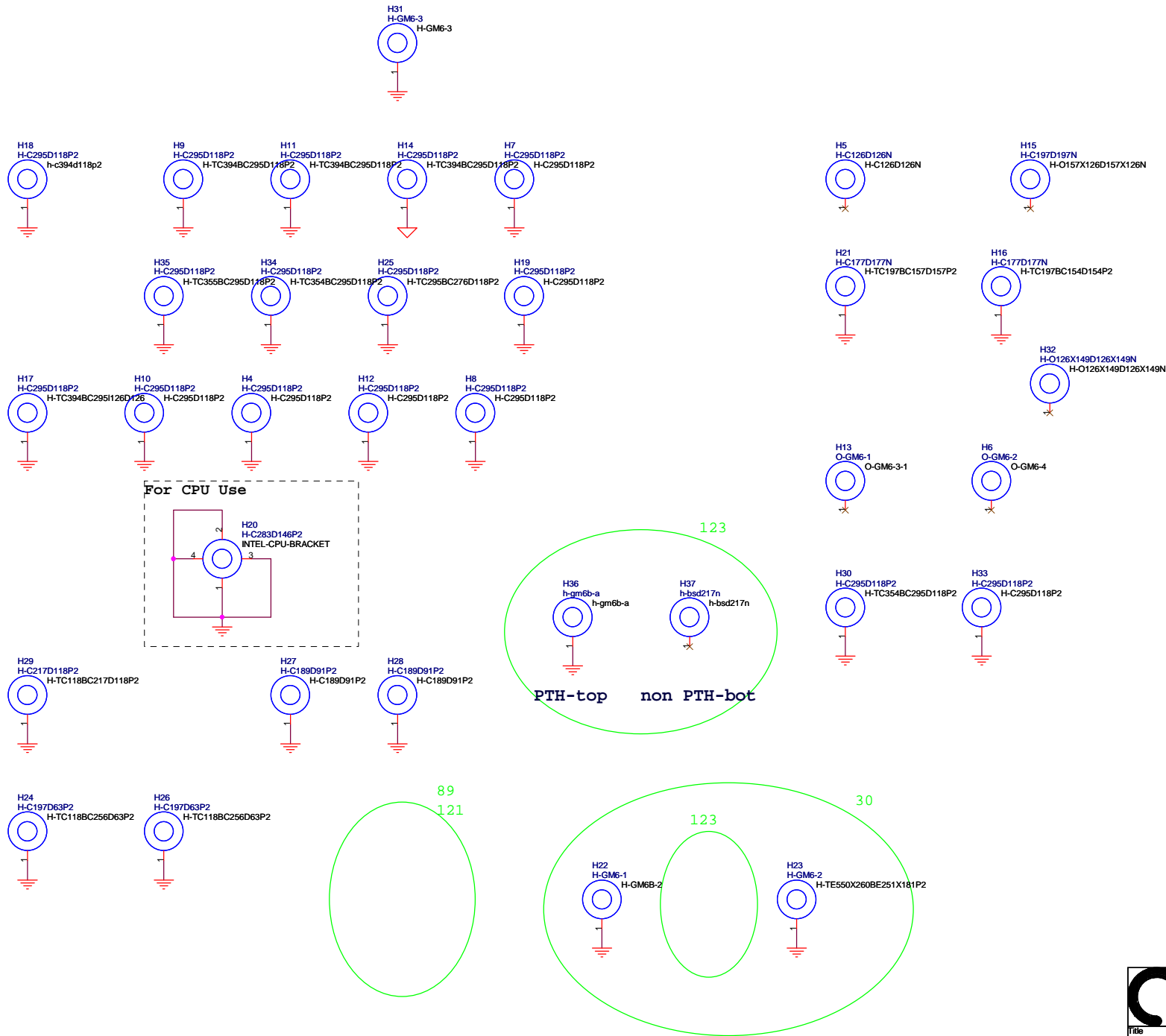


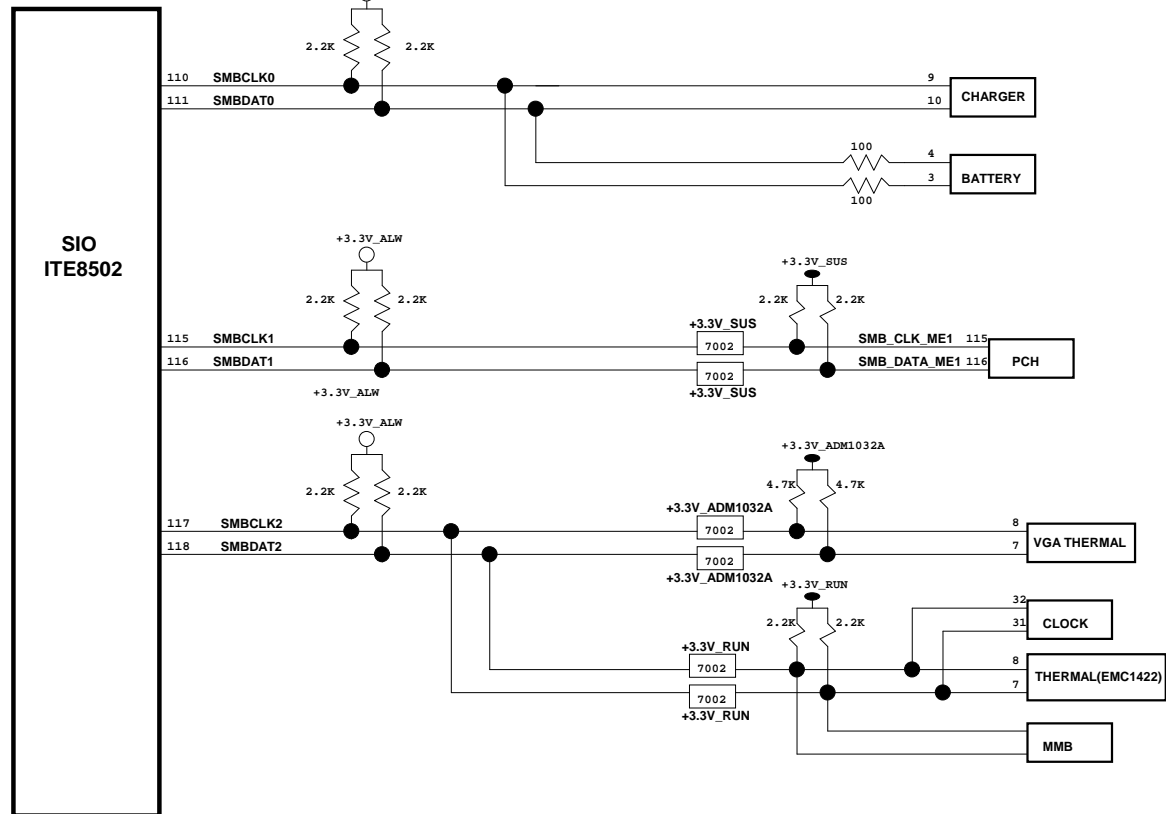
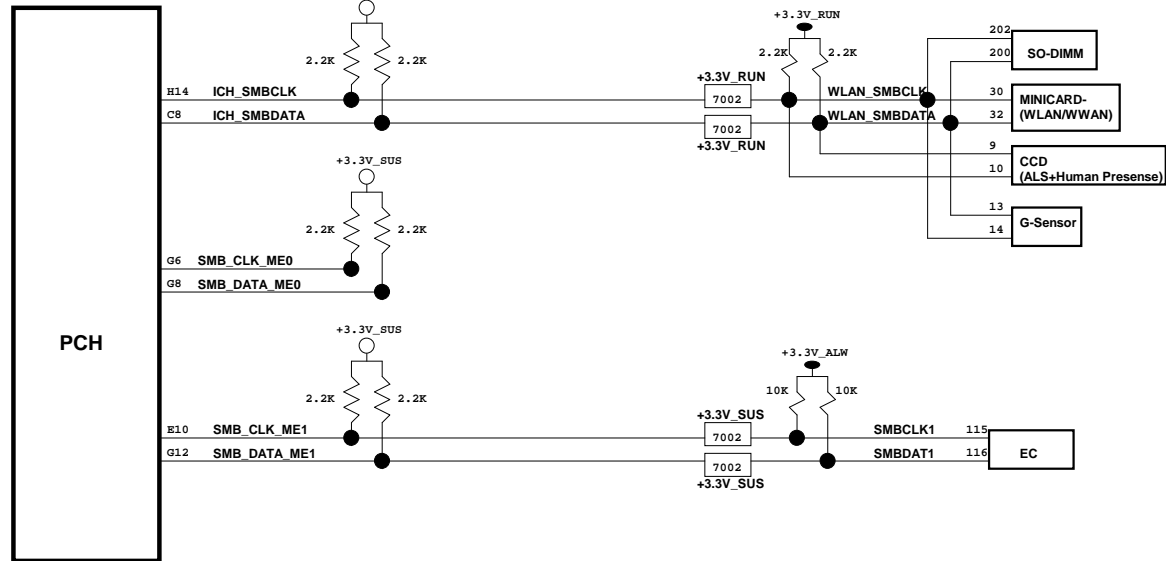
Reserve discharge path

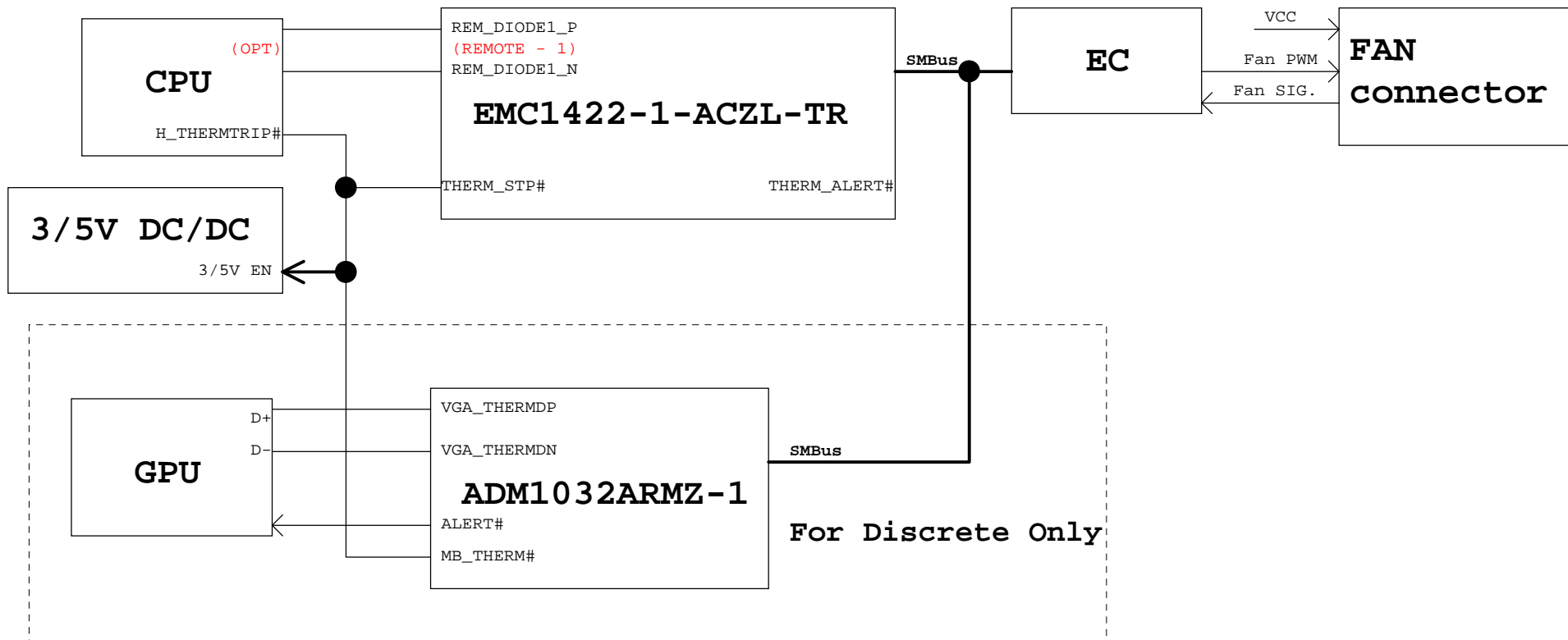


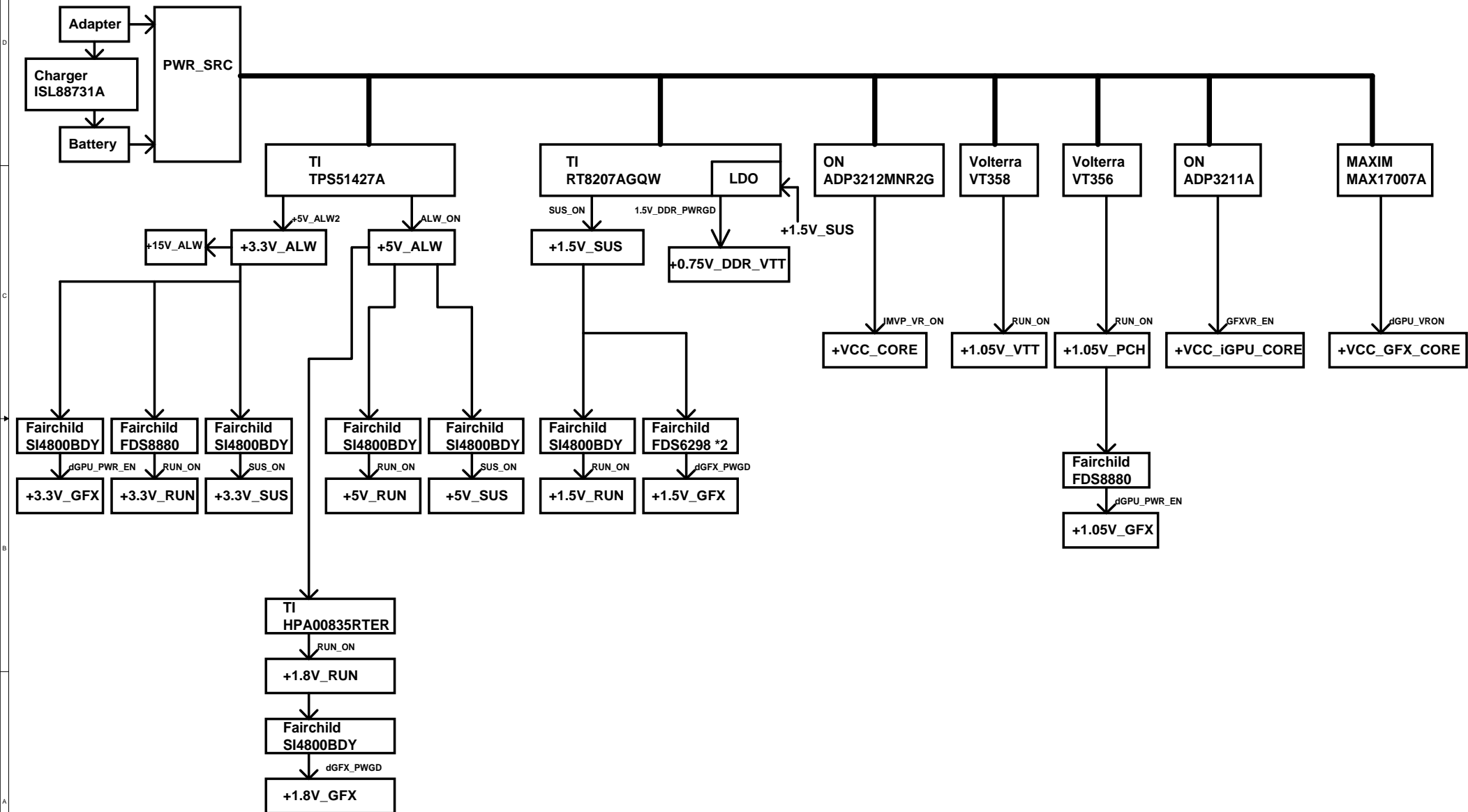
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FM9 Power Design Block Diagram 2009/12/28

