

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1
- LAYER 4 : SVCC
- LAYER 5 : IN2
- LAYER 6 : IN3
- LAYER 7 : SGND1
- LAYER 8 : BOT

www.Laptopblue.vn
BU4D Block Diagram

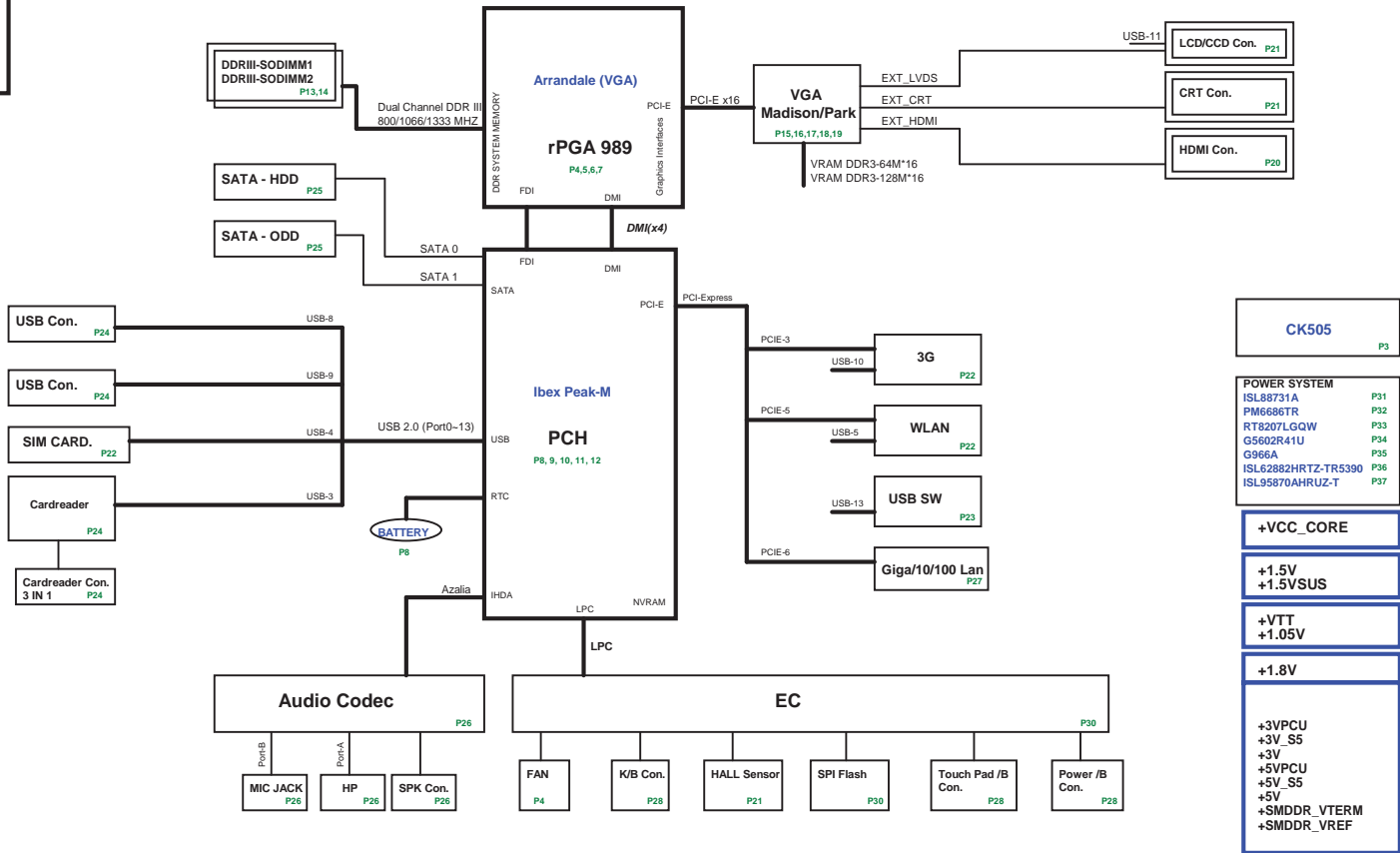




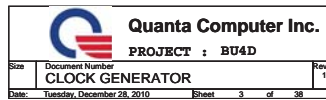
Table of Contents

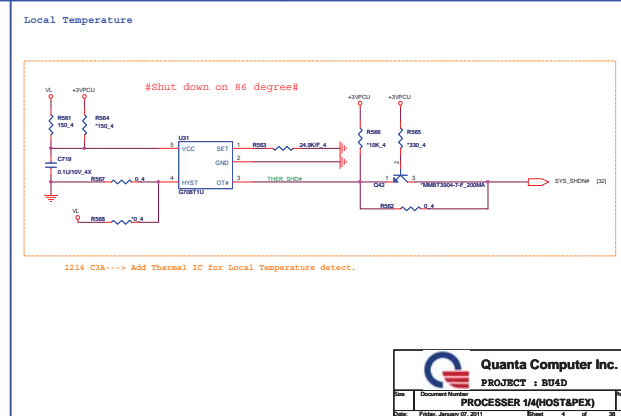
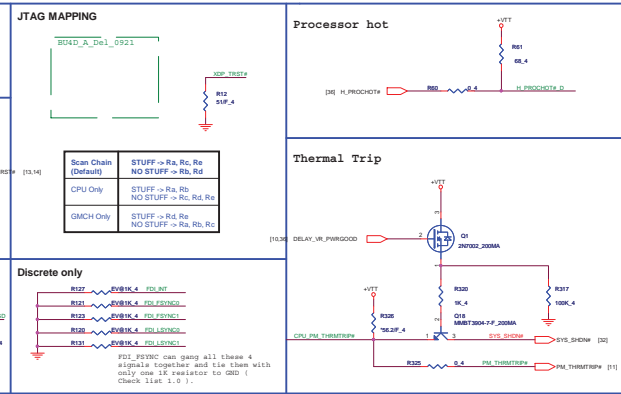
PAGE	DESCRIPTION	BOI-FUNCTIONS
1	Schematic Block Diagram	
2	Front Page	
3	Clk Gen	CLK
4-7	Processor	CPU
4	FAN-CPU	THC
8-12	PCH	CLG
8	RTC	RTC
13-14	DDRIII SO-DIMM	DDR
15-19	VGA Connector	VGA
20	HDMI comm part	HDM
	HDMI for GM	HMG
21	LCD Panel	LDS
	CRT & CRT BUS SWITCH	CRT
	CCD	CCD
	HALL SENSOR&BACK LIGHT SWITCH	HSR
22	MINI Card (Wi-Fi & WIMAX)	WLN
	MINI Card 3G	MNT
23	USB Connector	USB
	Sleep & Charging	SLC
24	USB	USB
	Card Reader	MMC
25	SATA ODD	ODD
	Main SATA HDD & 2nd SATA HDD	H1D
	G-Sensor	GSR
26	Codec (CX20671)	ADO
27	Atheros LAN	LAN
28	INT KeyBoard & K/B LED Power	KBC
	Power SW	PSW
	TP	TPD
	HOLE	
29	LED Board	LED
30	EC WPCE775L	KBC
31	Charger (ISL88731C)	PWM
32	System 5V/3V (PM6686TR)	PWM
33	DDR1.5V/+1.05V_USB3.0	PWM
34	+VTT /+1.05V(G5602R41U)	PWM
35	+1.8V (G966A)/Discharge	PWM
36	CPU Core (ISL62882C)	PWM
37	+GPU_CORE(ISL95870AHRUZ)	PWM
38	POWER TREE TABLE	PWM

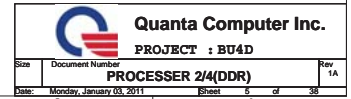
POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0-S5
+VCCRTC	+3.0V~+3.3V		S0-S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0-S5
+3V_HDP	+3.3V	MAIN_ON	S0
+3VPCU	+3.3V	AC/DC Insert enable	S0
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0-S5
+5VPCU	+5V	AC/DC Insert enable	S0-S5
WIMAX_P	+3.3V	WMAX_P for EC	
+3V_3G	+3.3V	+3V_3G for EC	
+1.8V	+1.8V	MAIN_ON	S0
+1.5V	+1.5V	MAIN_ON	S0
+1.5V_SUS	+1.5V	SUSON	S0-S3
+VCC_CORE		VRON	S0
+VTT	+1.05V~+1.1V	MAIN_ON	S0
+1.05V	+1.05V	MAIN_ON	S0
+VAXG		GF Xavier_EN	S0

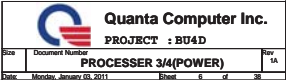
GND PLANE	PAGE
 ADOGND	26
 GND	ALL

ITEM	Value Code	FUNCTIONS
1	EV@	DISCRETE
2	IV@	UMA
3	U3@	USB 3.0
4	U2@	USB 2.0 (colay W USB 3.0)
5	HM@	HDMI
6	IHM@	Internal HDMI
7	EHM@	External HDMI
8	3G@	3G
9	C@	Cost issue
10	MDC@	Modem
11	51@	1G LAN
12	52@	10/100 LAN
13	51_52@	1G LAN or 10/100 LAN parts
14	GS@	G sensor
15		
16		
17		

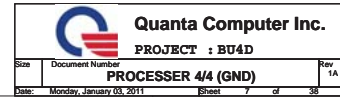






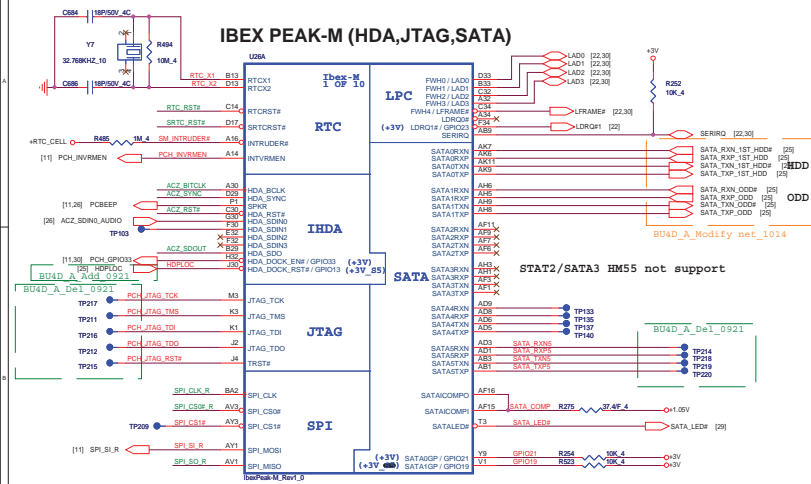


AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)

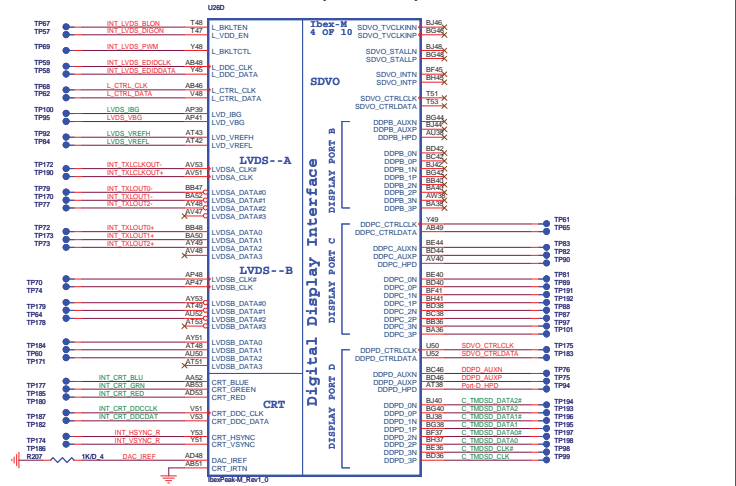


The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K \pm 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

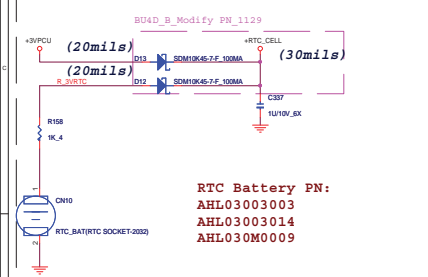
IBEX PEAK-M (HDA,JTAG,SATA)



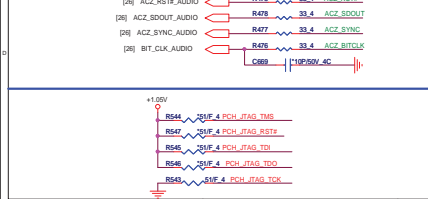
IBEX PEAK-M (LVDS,DDI)



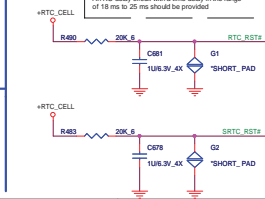
RTC BATTERY



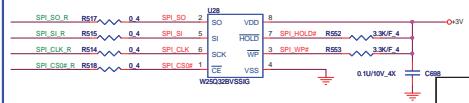
For AUDIO



RESET JUMP



4M byte SPI ROM



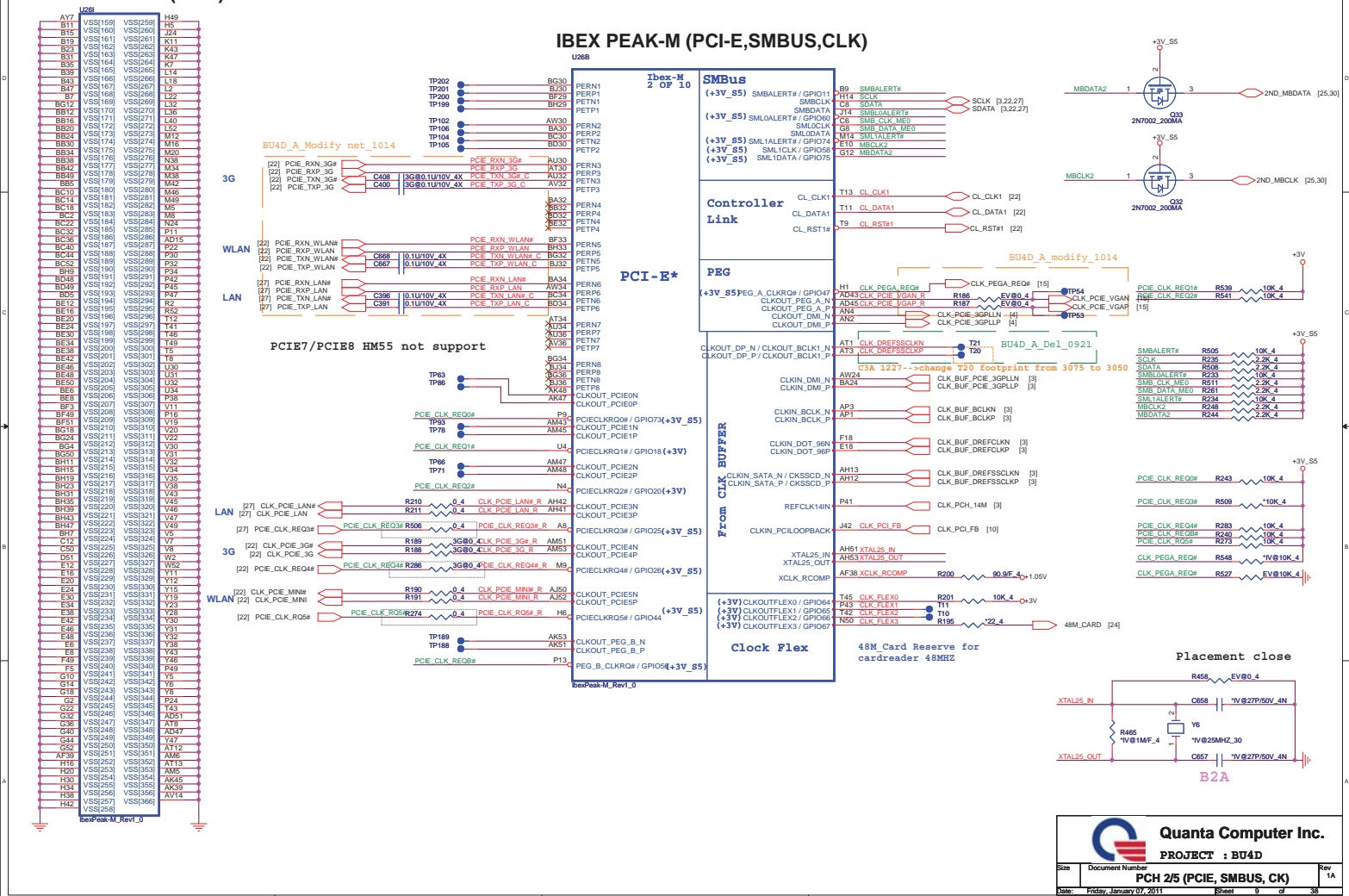
PCH	2MB	4MB	8MB
PM55	●		
HM55		●	
HM57/PM57		●	●
QM57/QS57			●

**Quanta Computer Inc.**

PROJECT : BU4D

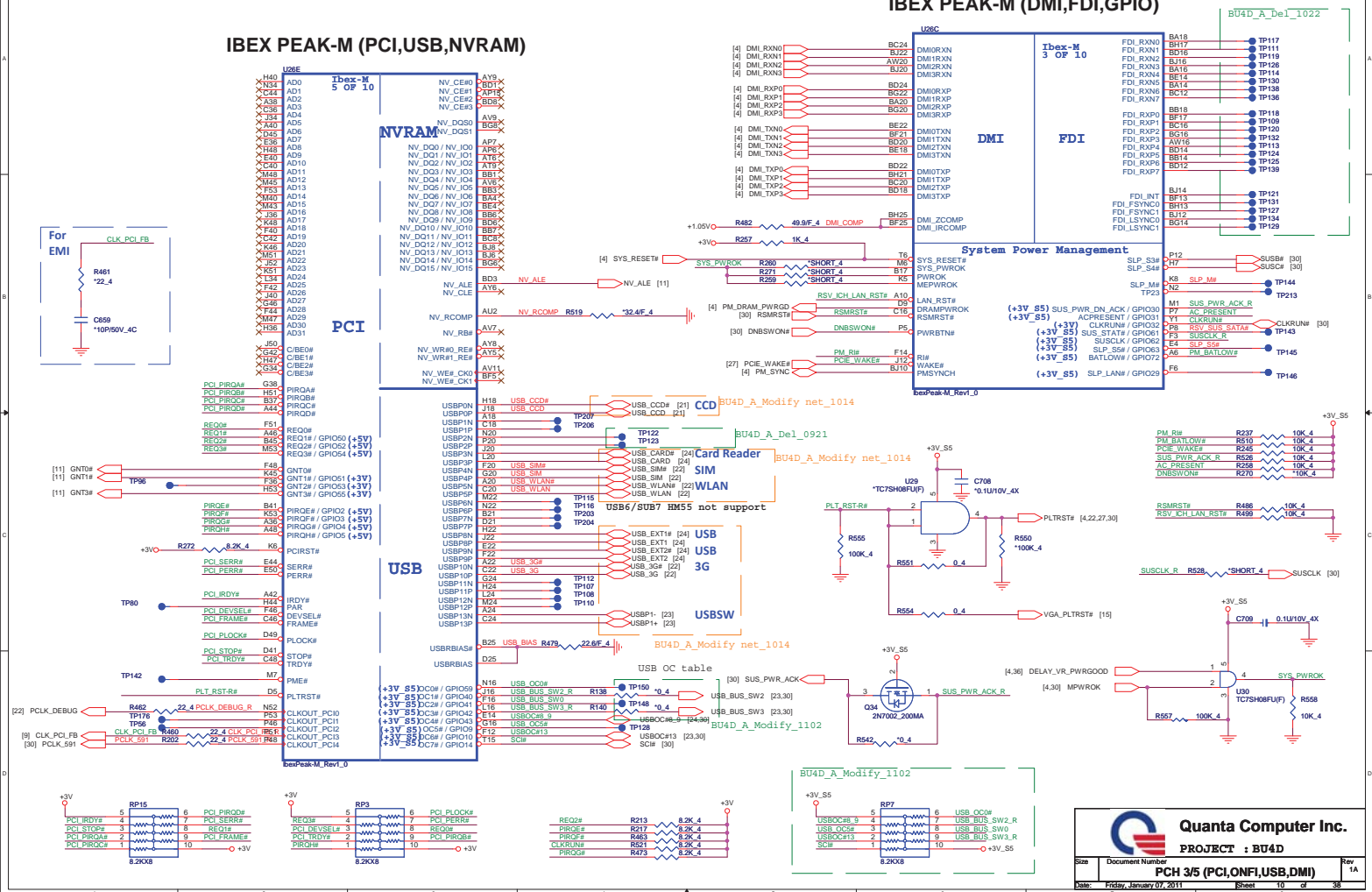
Size	Document Number	Rev
	PCH 1/5 (SATA,HDA,LPC)	1A
Date	Friday, January 07, 2011	Sheet 8 of 38

IBEX PEAK-M (GND)

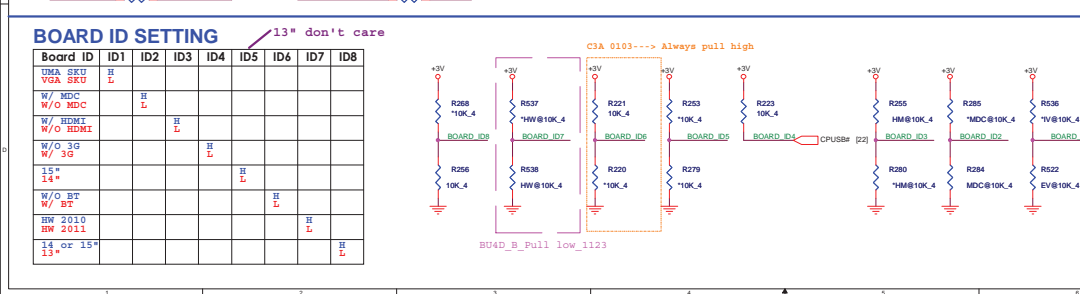









IBEX PEAK-M (DMI,USB,GPIO)


IBEX PEAK-M (PCI,USB,NVRAM)

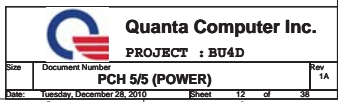


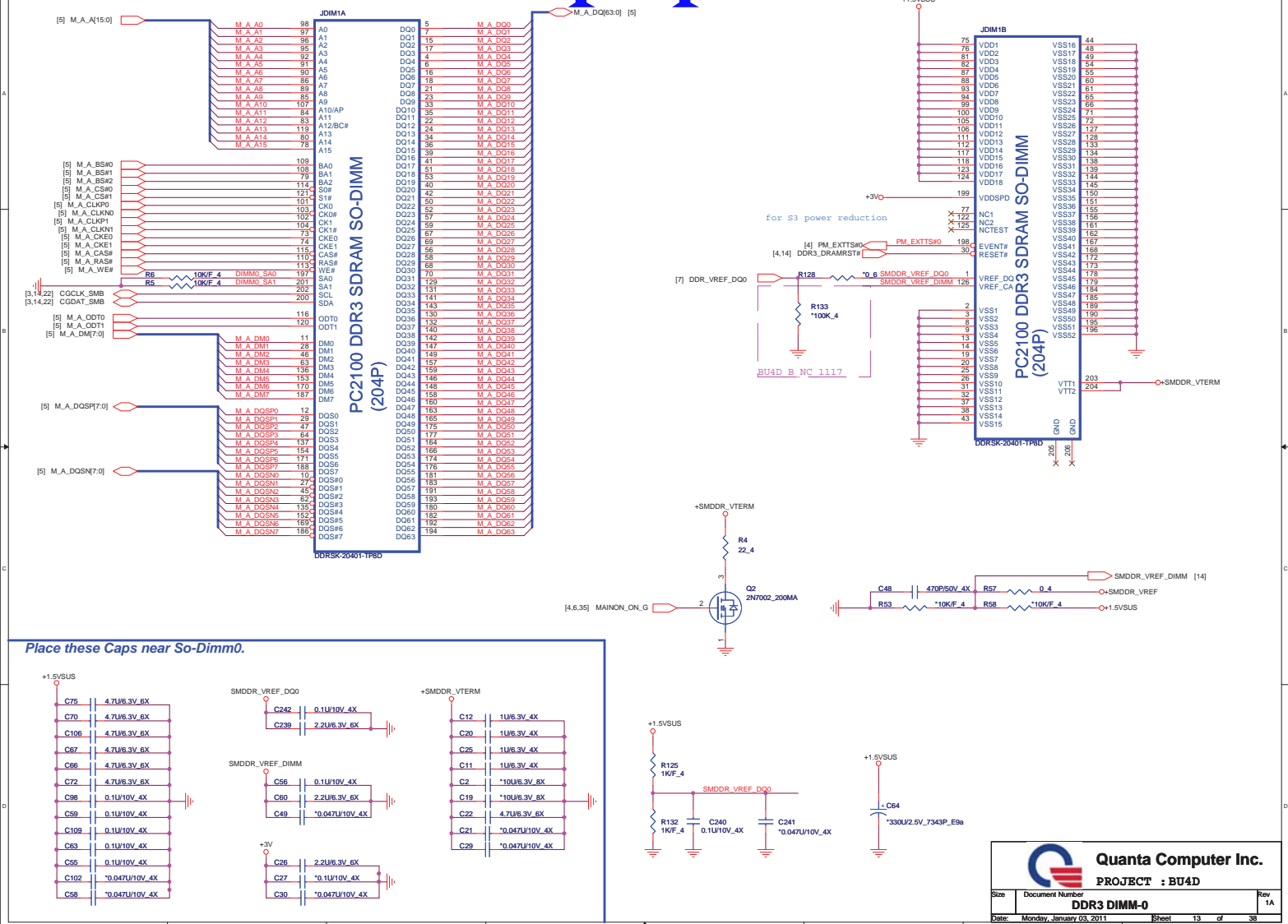
PCH Strap Pin Configuration Table

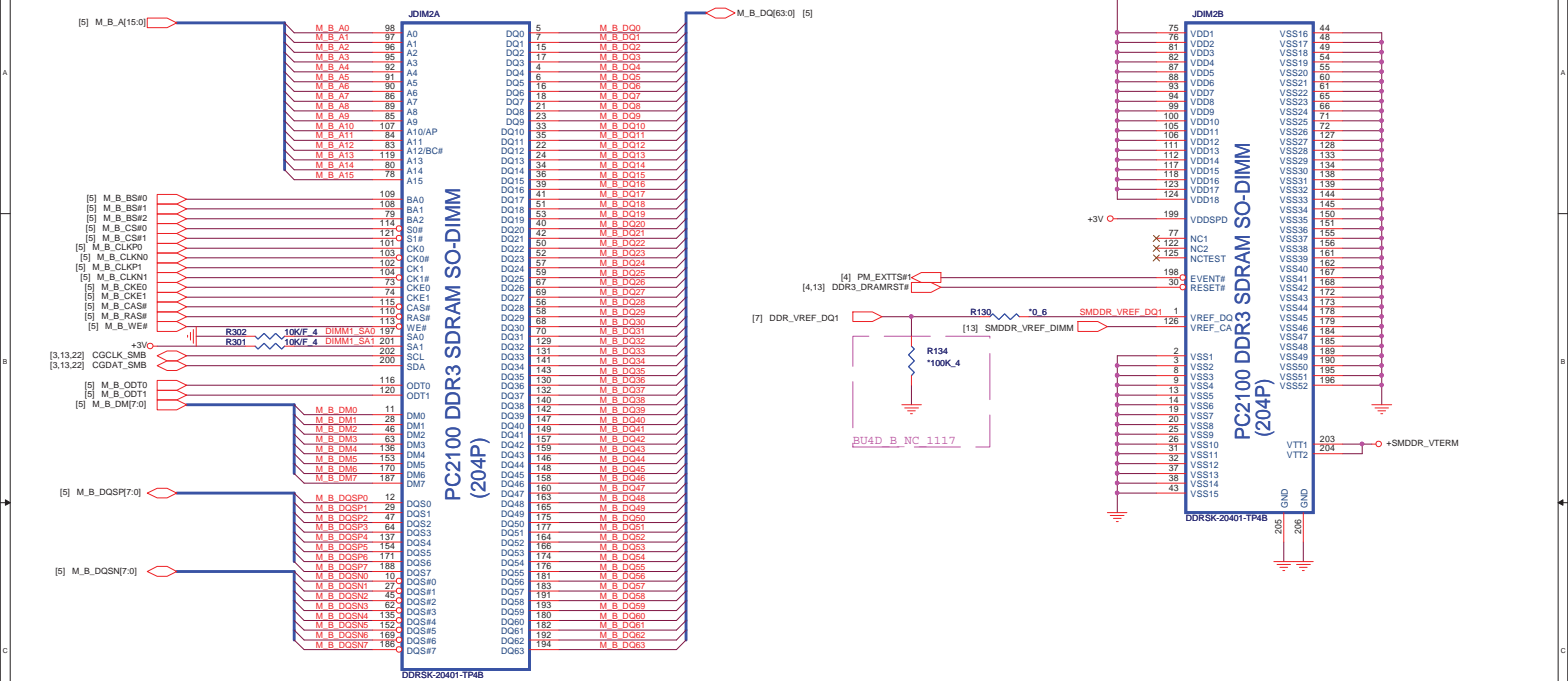


SPKR [B.36] PCBEPP																		
Reboot option at power-up	0 = Flash Mode (Internal weak Pull-down) 1 = No Reboot Mode with TCO Disabled																	
GN73#/ GPIO55 [10] GN73#																		
Top-Block Swap Override	0 = Top Block Swap Mode 1 = Default Mode (internal pull-up)																	
HDA_DOCK_EN #GPIO33 [B.30] PCH_GPIO33																		
Flash Descriptor Security Override	0 = Flash Descriptor Security will be overridden 1 = Security measure defined in the Flash Descriptor will be enabled.																	
GN70#, GN71# [10] GN70# [10] GN71#																		
<table><tr><th>Boot BIOS Strap</th><th rowspan="2"></th><th rowspan="2"></th></tr><tr><th>PCH_GN70#</th></tr><tr><td>0</td><td>0</td><td>LPC</td></tr><tr><td>0</td><td>1</td><td>PCI</td></tr><tr><td>1</td><td>0</td><td>Reserved (RAND)</td></tr><tr><td>1</td><td>1</td><td>2PI</td></tr></table>			Boot BIOS Strap			PCH_GN70#	0	0	LPC	0	1	PCI	1	0	Reserved (RAND)	1	1	2PI
Boot BIOS Strap																		
PCH_GN70#																		
0	0	LPC																
0	1	PCI																
1	0	Reserved (RAND)																
1	1	2PI																
SPI_MOSI [8] SPI_SLR																		
TPM Functionality Disable	1 = Enabled 0 = Disable																	
NV_ALE [10] NV_ALE																		
Intel® Anti-Theft Technology HDD Data Protection (Intel AT-t) Enable	1 = Enabled 0 = Disabled (Default)																	
GPIO8 [B.36] PCBEPP																		
Reserved	This signal has a weak internal pull up. NOTE: This signal should not be pulled low																	
GPIO15 [B.36] PCBEPP																		
Reserved	0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality																	
GPIO27 [B.36] PCBEPP																		
On-Die PLL Voltage Regulator	0 = Disables the VccVRM. Need to use on-board filter circuits for analog rails. 1 = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. This signal has a weak internal pull-up.																	
<div><div>+RTC_CELL</div><div>[B]</div></div> <div>INVRMEN - Integrated 1.1V VRM Enable High - Enable Internal VRS</div>																		

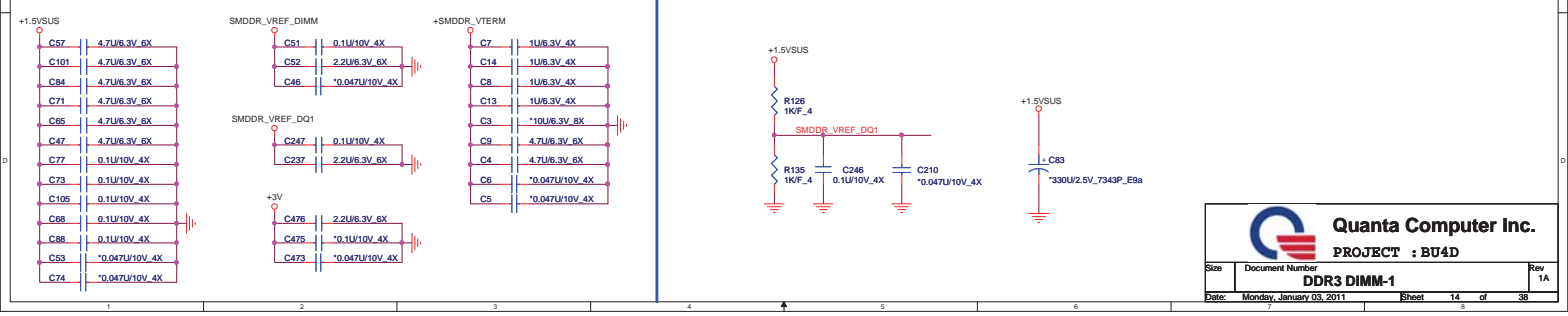
		Quanta Computer Inc.	
		PROJECT : BU4D	
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	PCH 45 (GPIO & Strap)	Date: Friday, January 07, 2011	Page: 11 of 38



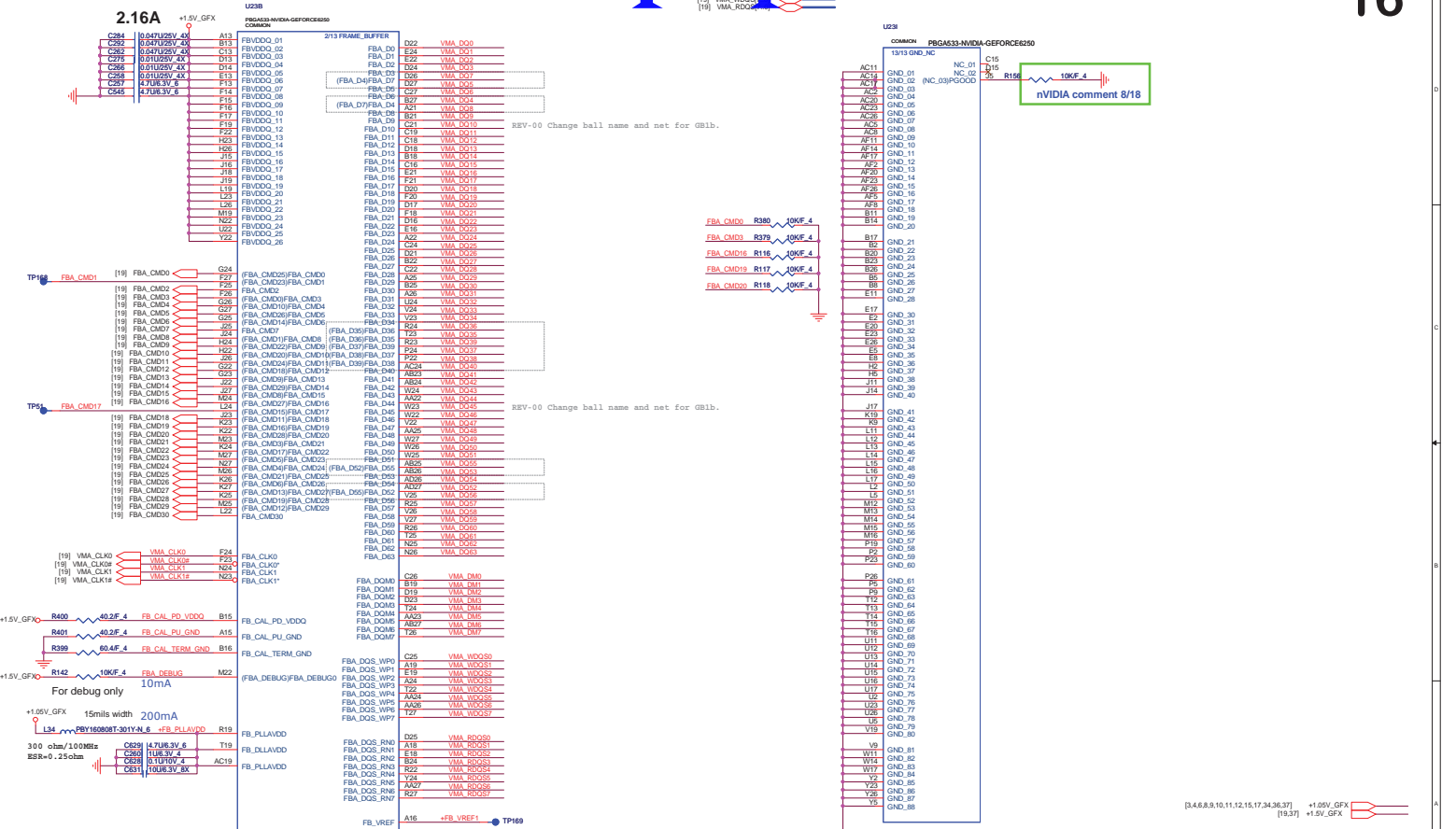


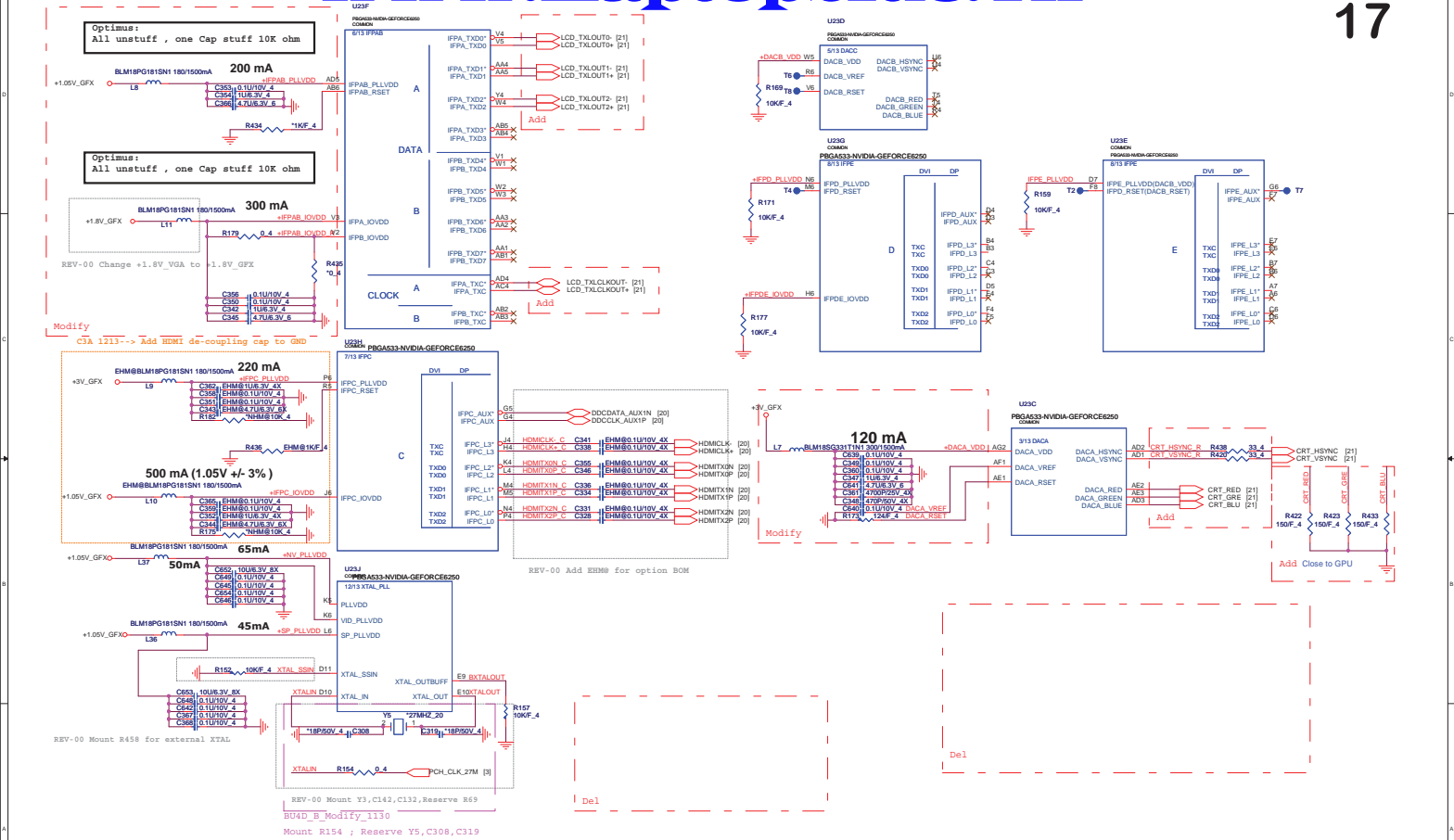


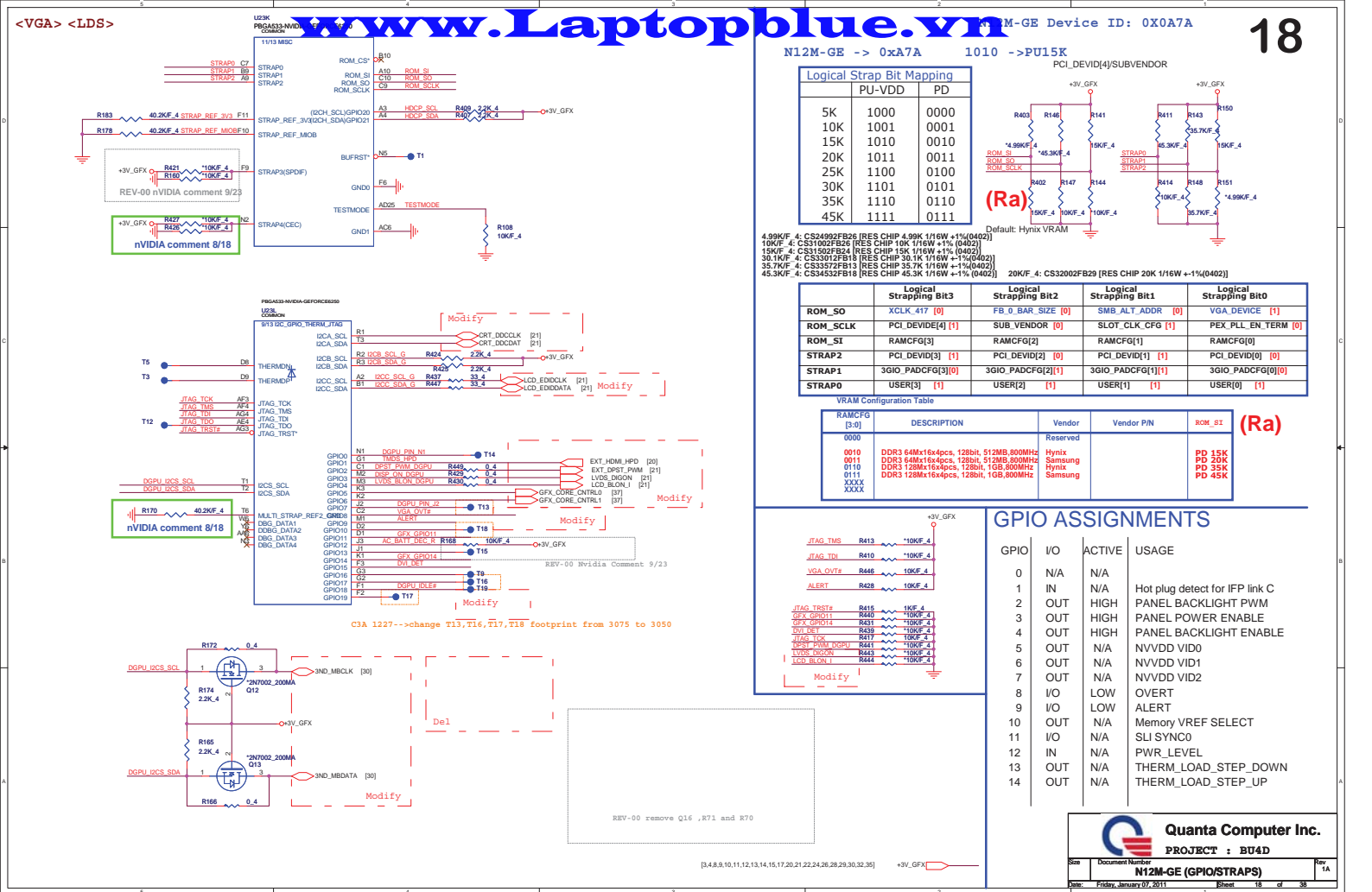
Place these Caps near So-Dimm1.

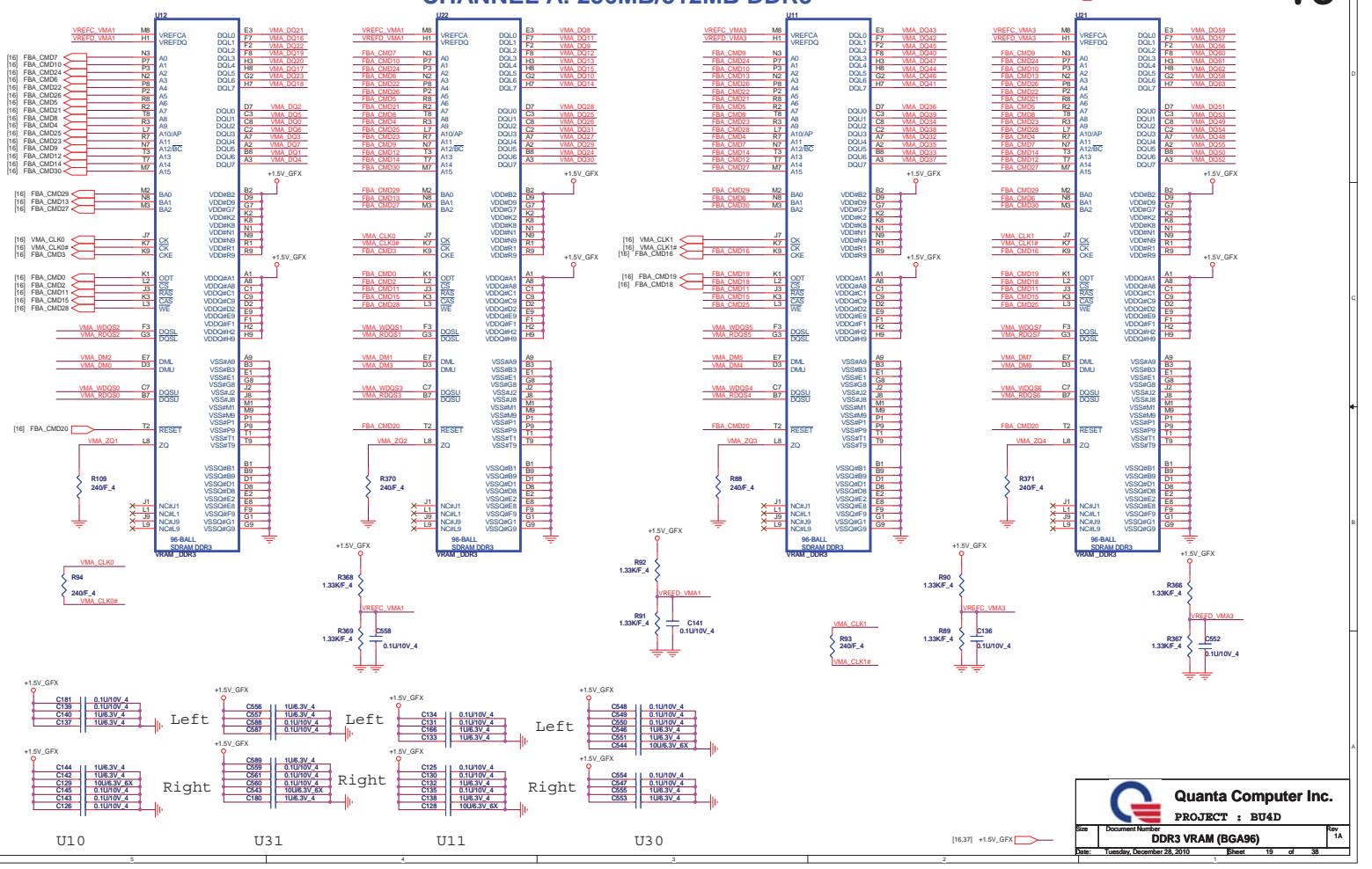








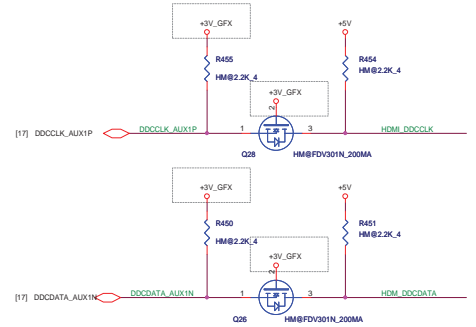
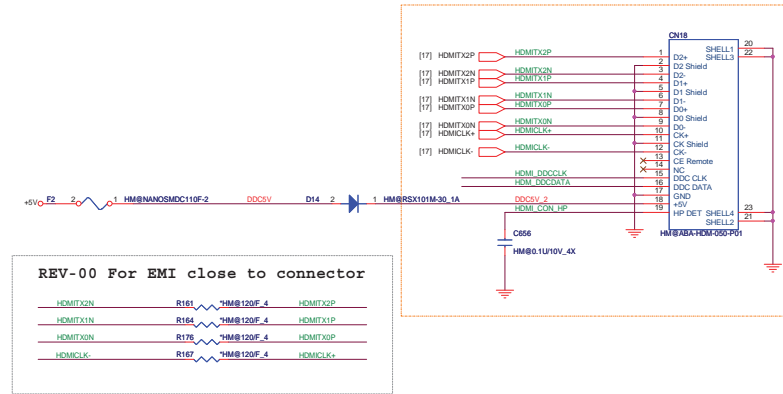




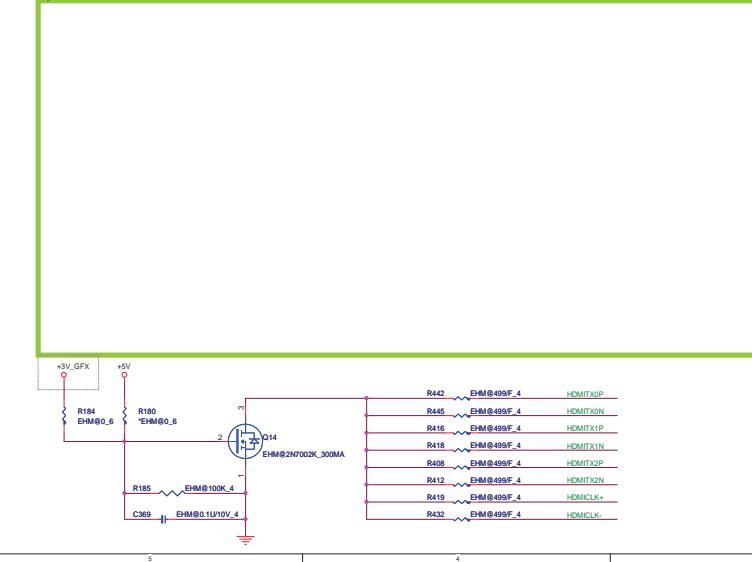
HDMI Conn <HDM>

HDMI-CONN

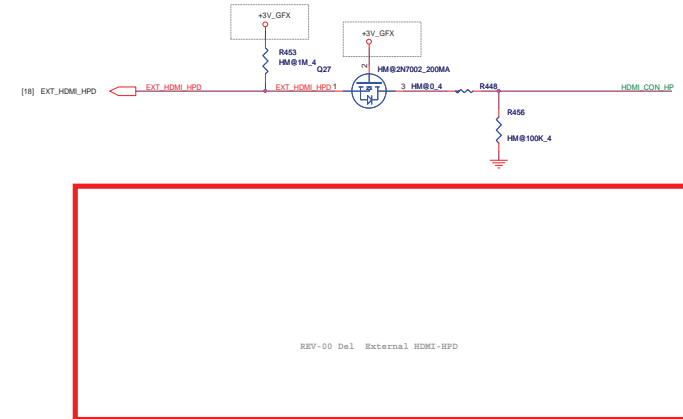
C3A 1216----> Change HDMI Conn. P/N & Footprint



HDMI-passive level shift <HDM>

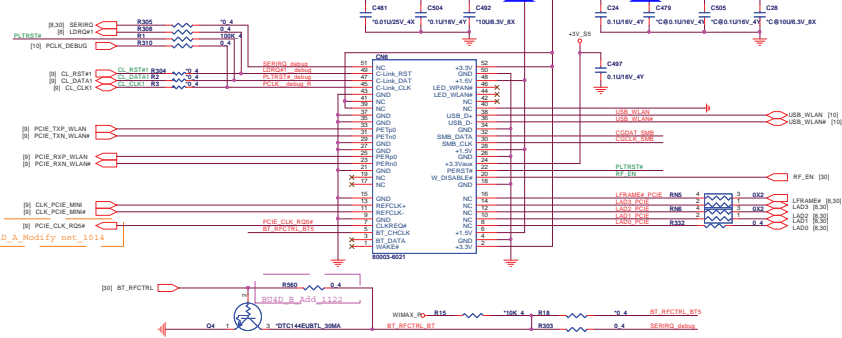


HDMI-HPD <HDM>

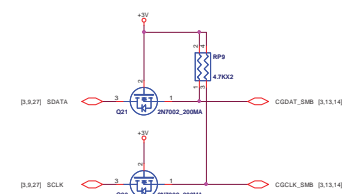




The schematic diagram shows the BQ4040B-PM1129 circuit. The input is 5V, which goes through a 1N4148 diode and a BQ4040B-PM1129 IC. The IC has pins for GND, VCC, and various control pins. The output is connected to a 100nF capacitor and a 10k resistor, which is then connected to a 5V output. The IC is labeled BQ4040B-PM1129.



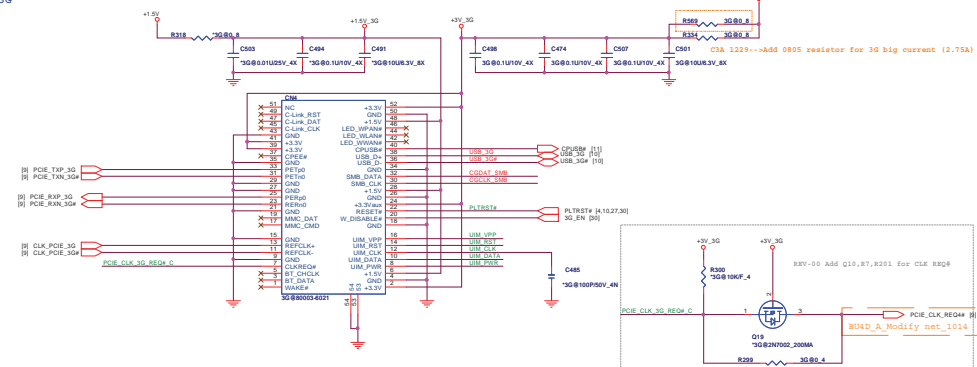
SMBus(DDR3/WLAN/3G)



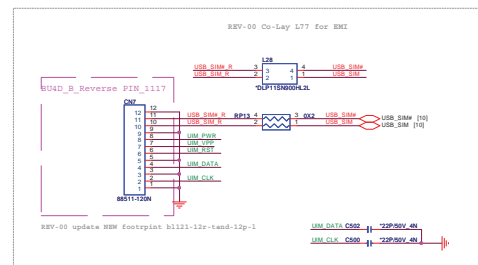
```

MINI Card Slot#2  <MNT>
3G

```

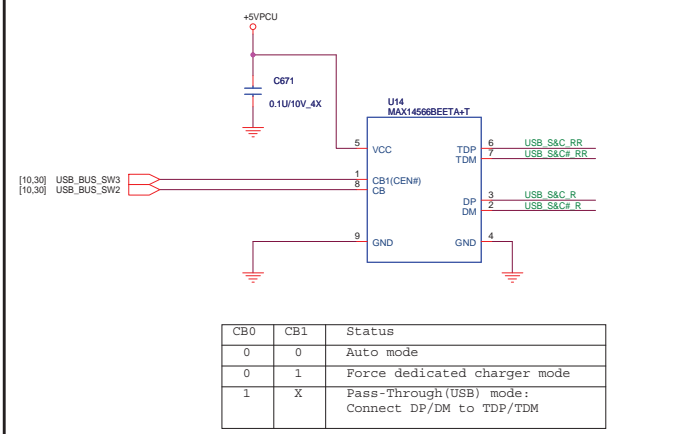


For SIM Card on daughter board

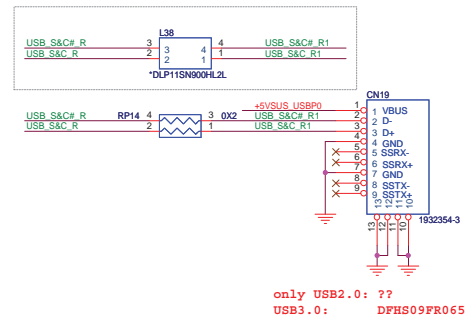


USB w S&C MAXIM SOLUTION <SLC>

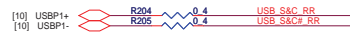
REV-00 Co-Lay L73 for EMI



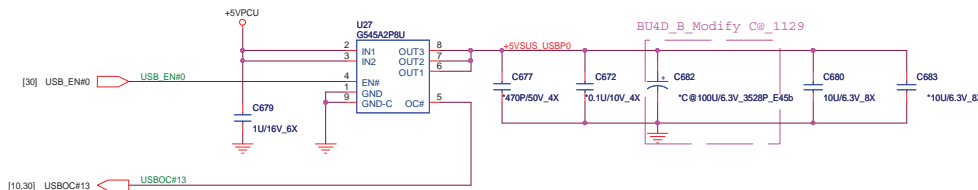
USB 2.0 CONN <USB>



<USB>



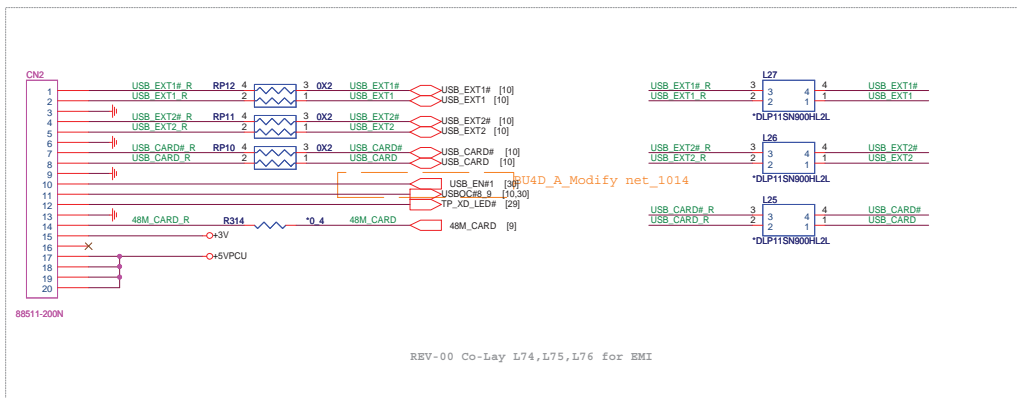
USB 2.0 Power switch <USB>

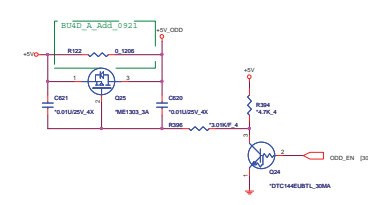


<EMC>

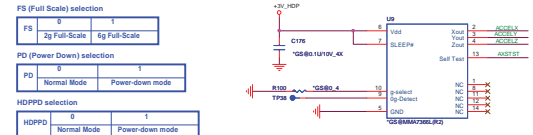


USB2.0 Left 1
USB2.0 Left 2 <USB> <MMC> <EMI>



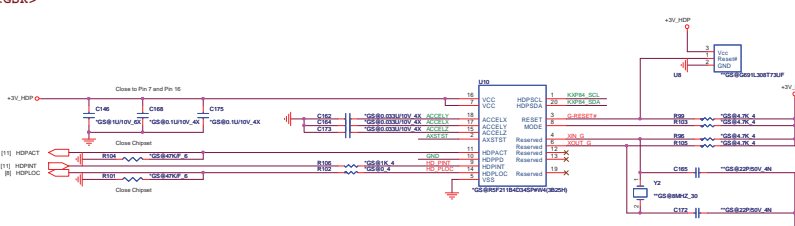


3D-Sensor IC <GSR>



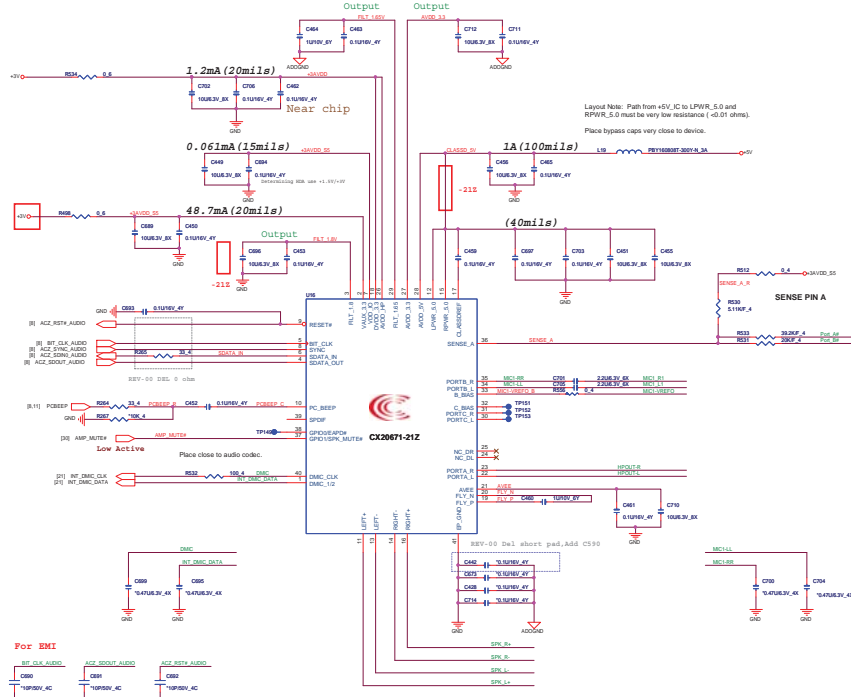
HDPPD	0	1
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3D-u-micro P <GSR>

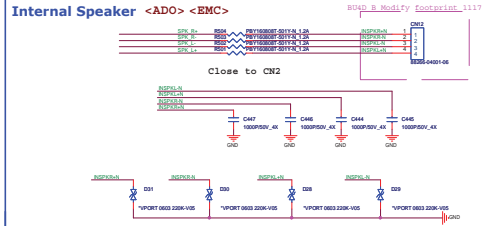
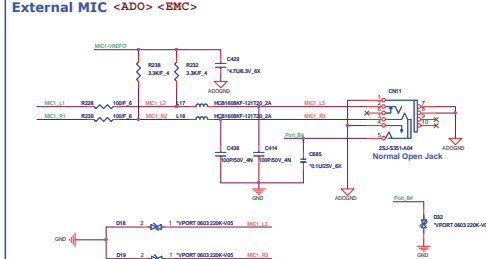
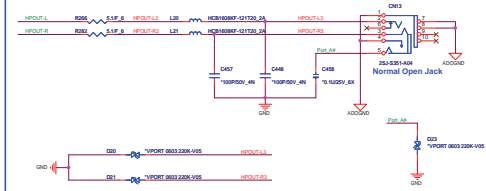


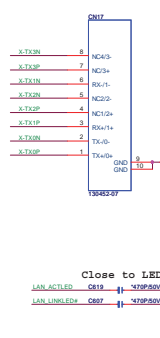
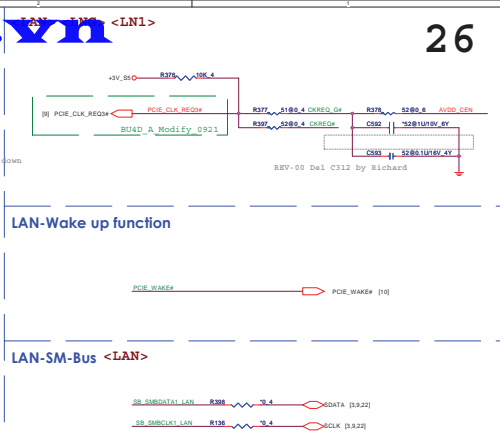
[11] HDPRINT

[12] HDPLC



Need to change 20671-21Z footprint



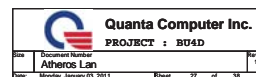


LED0 = LAN_ACTLED	1	Over-clocking enable (default = 1)
	0	Over-clocking disable
LED1 = LAN_LINKLED	1	SNR switch-mode regulator select Giga LAN pull High (default = 1)
	0	LDO linear regulator select 10/100M LAN pull Low
CERREQ# or CERREQ_G#	1	Normal function
	0	ATE test mode

Power on Strapping pin

LAN ACTLED R395 51K/F 6

+3V_Sd R399 5105.1K/F 6 R398 5205.1K/F 6 LAN LINKED#

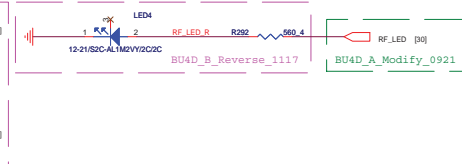
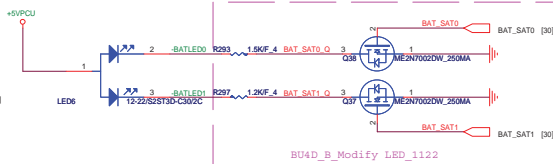
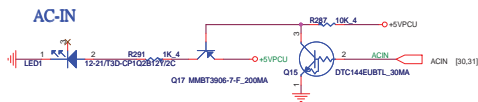


LED <LED>

BATTERY

D3A : LED luminance to light, 1K-ohm change 2.2K-ohm.

RF LED

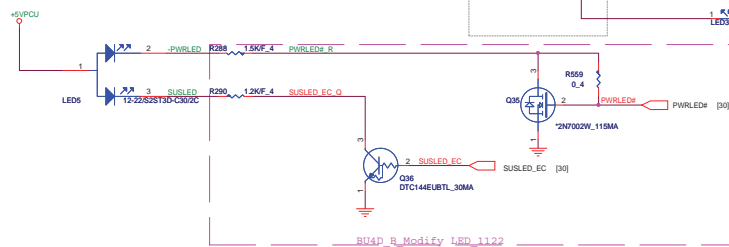


CARDREADER

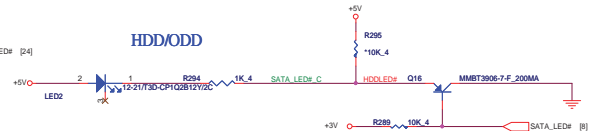
REV-00 remove R422

POWER

D3A : LED luminance to light, 1K-ohm change 2.2K-ohm.



HDD/ODD



ESD Protect <EMC>

FOR POWER LED

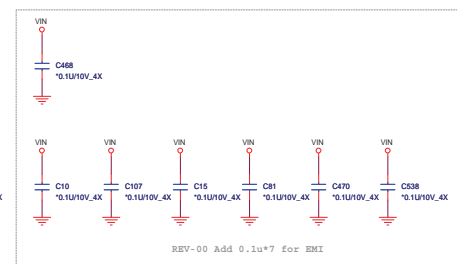
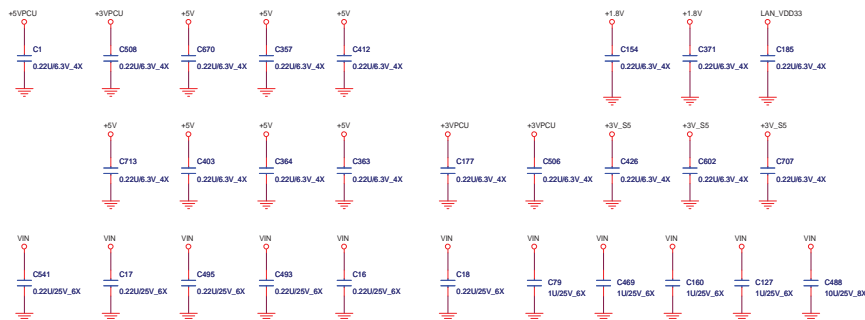
FOR BATTERY LED

FOR HDD/W-LAN LED

FOR 3G/CARDREADER LED



<EMI>



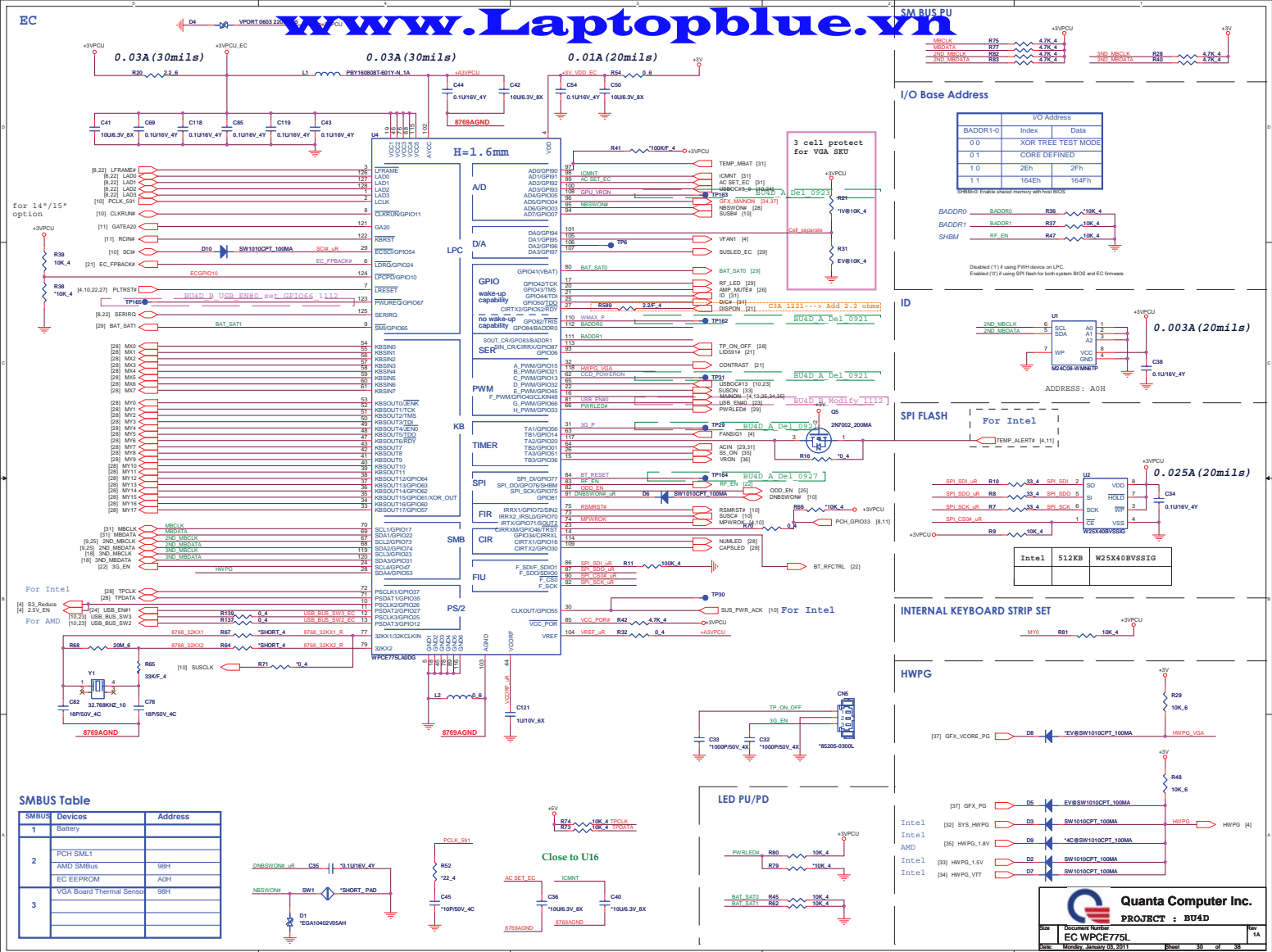
REV-00 Add 0.1u*7 for EMI



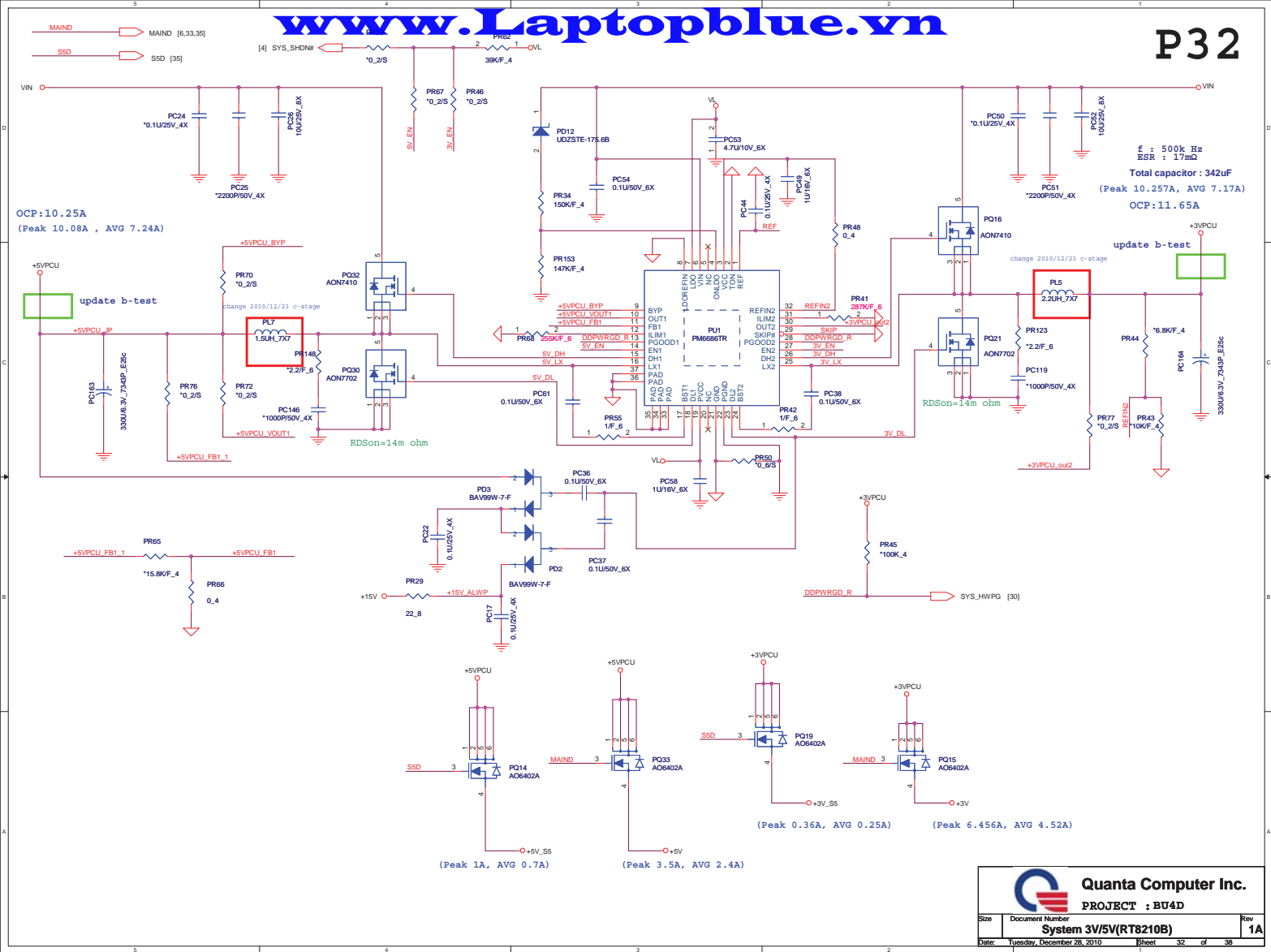
Quanta Computer Inc.

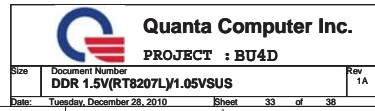
PROJECT : BU4D

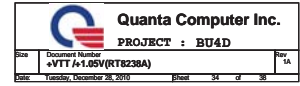
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	LED/HOLE	1A
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Size	Document Number +VTT /+1.05V(RT6238A)	Rev 1A
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