

Enrico/Caruso 15" UMA Schematics Document

Sandy Bridge

Intel PCH

2011-06-02

REV : A00

起点主板维修网 www.qdzbwx.com

DY :None Installed
PSL:10mW internal schematic
10mW: 10mW schematic installed
Surge: Surege schematic installed
GIGA: GIGA schematic installed
10/100: 10/100 schematic installed
HDMI: HDMI schematic installed
Debug: Debug schematic installed

DV15 HR Vos GIGA HDMI NoSurge



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Title

Cover Page

Size
A3

Document Number

Enrico/Caruso 15 HR

Rev
X01

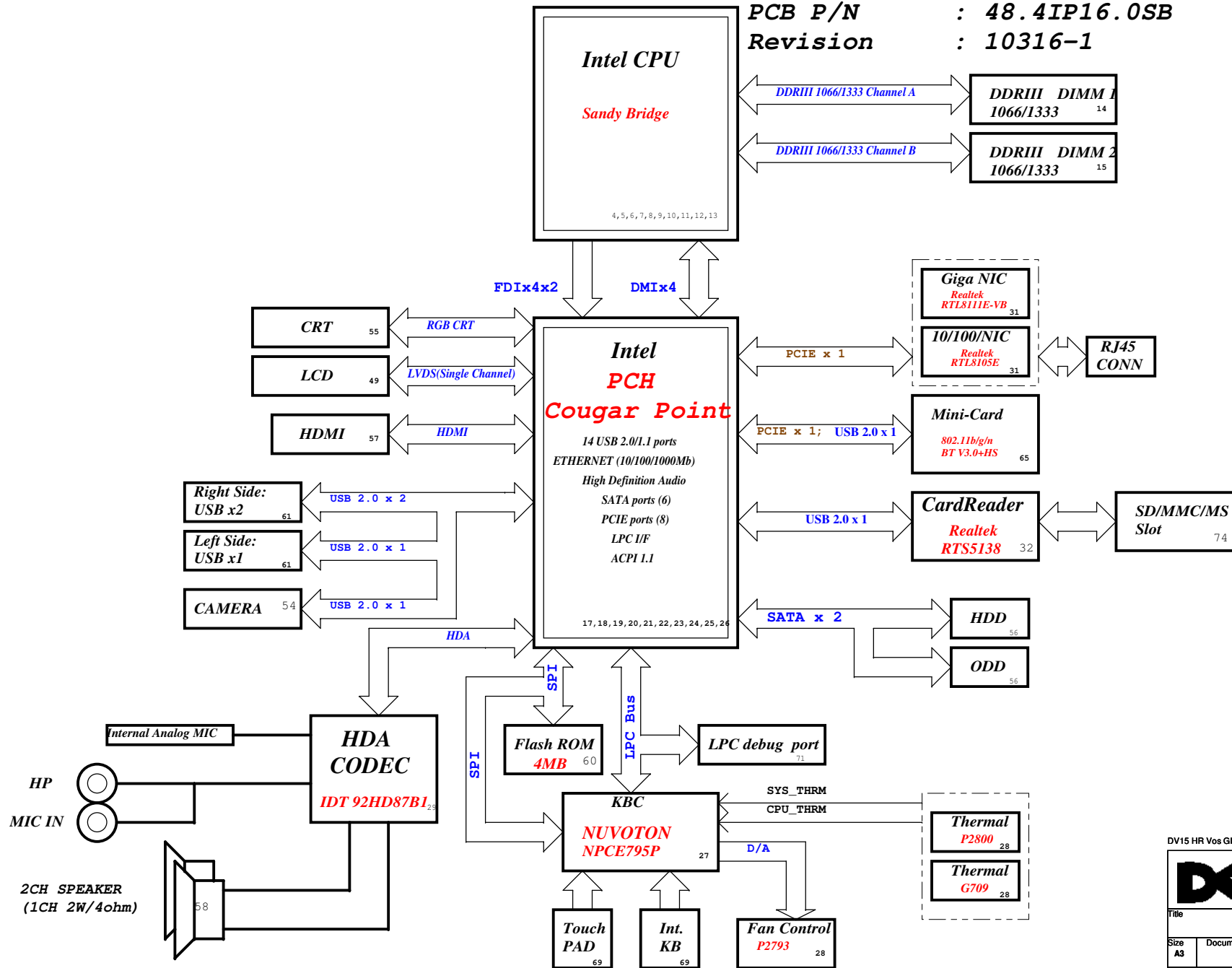
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DV15 Huron River UMA Block Diagram

起点主板维修网 www.qdzbwx.com

Project code : 91.4IP01.001
PCB P/N : 48.4IP16.0SB
Revision : 10316-1



SYSTEM DC/DC	
TPS51461	48
INPUTS	OUTPUTS
DCBATOUT	0D85V_S0
CPU DC/DC	
ISL95831HRTZ	42~44
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
GFX DC/DC	
ISL95831HRTZ	44
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE
SYSTEM DC/DC	
TPS51218	45
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT
SYSTEM DC/DC	
TPS51123RGER	41
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5 15V_S5
SYSTEM DC/DC	
TPS51216RUKR	46
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3
MAXIM CHARGER	
BQ24707	40
INPUTS	OUTPUTS
+DC_IN_S5 +PBATT	DCBATOUT
SYSTEM DC/DC	
TPS51311RGTR	47
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0
Switches	
INPUTS	OUTPUTS
1D5V_S3 5V_S5 3D3V_S5	1D5V_S0 5V_S0 3D3V_S0
PCB LAYER	
L1:Top	L4:Signal
L2:GND	L5:VCC
L3:Signal	L6:Bottom

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Block Diagram		
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Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	Enable Danbury: Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. Disable Danbury: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] Disable Danbury: Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

USB Table

PCIE Routing

LANE1	X
LANE2	Onboard LAN
LANE3	x
LANE4	Mini Card1 (WLAN)
LANE5	X
LANE6	X
LANE7	X
LANE8	X

SATA Table

SATA	
Pair	Device
0	HDD1
1	X
2	X
3	X
4	ODD1
5	X

Pair	Device
0	X
1	USB Ext. port 1
2	X
3	X
4	X
5	CARD READER
6	X
7	X
8	USB Ext. port 2
9	USB Ext. port 3
10	X
11	Mini Card1 (WLAN)
12	CAMERA
13	X

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		Disabled - No Physical Display Port attached to Embedded DisplayPort. 1: Embedded DisplayPort. 0: Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	PCI-Express Port Bifurcation Straps	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	PEG DEFER TRAINING	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails	
		ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC GFXCORE	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	9V-12.6V 9V-19V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

SMBus ADDRESSES

I ² C / SMBus Addresses		HURON RIVER ORB		
Device	Ref Des	Address	Hex	Bus
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH				SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) MINI				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

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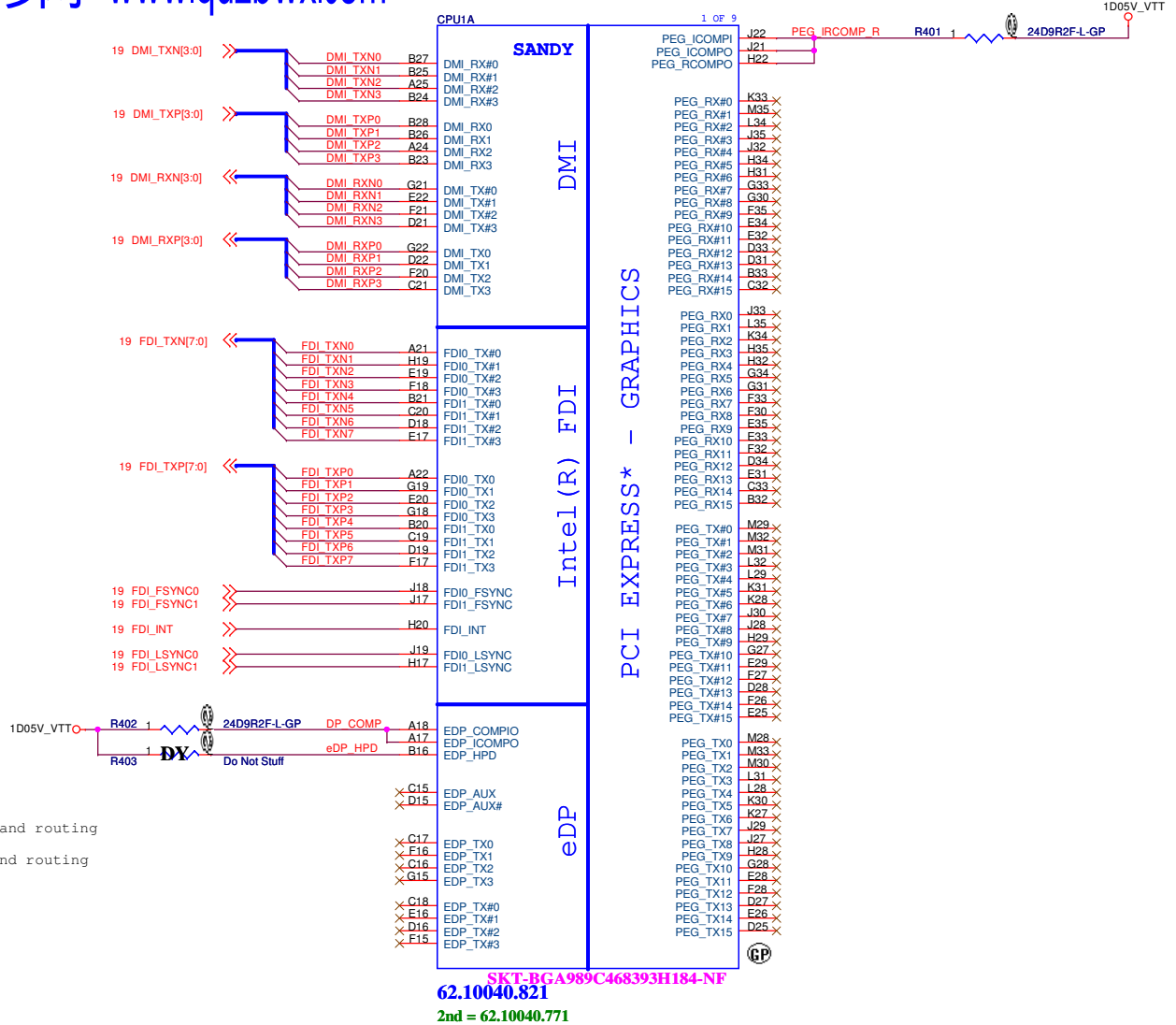
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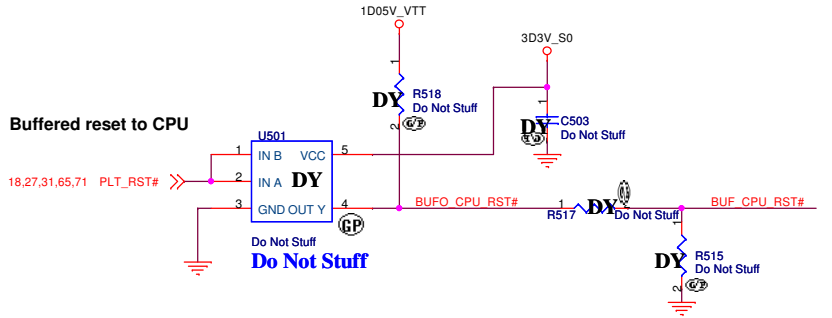
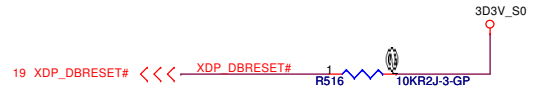
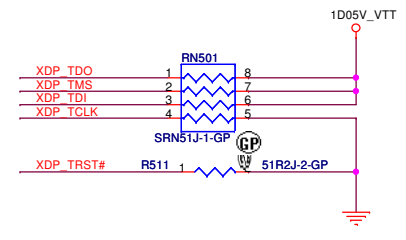
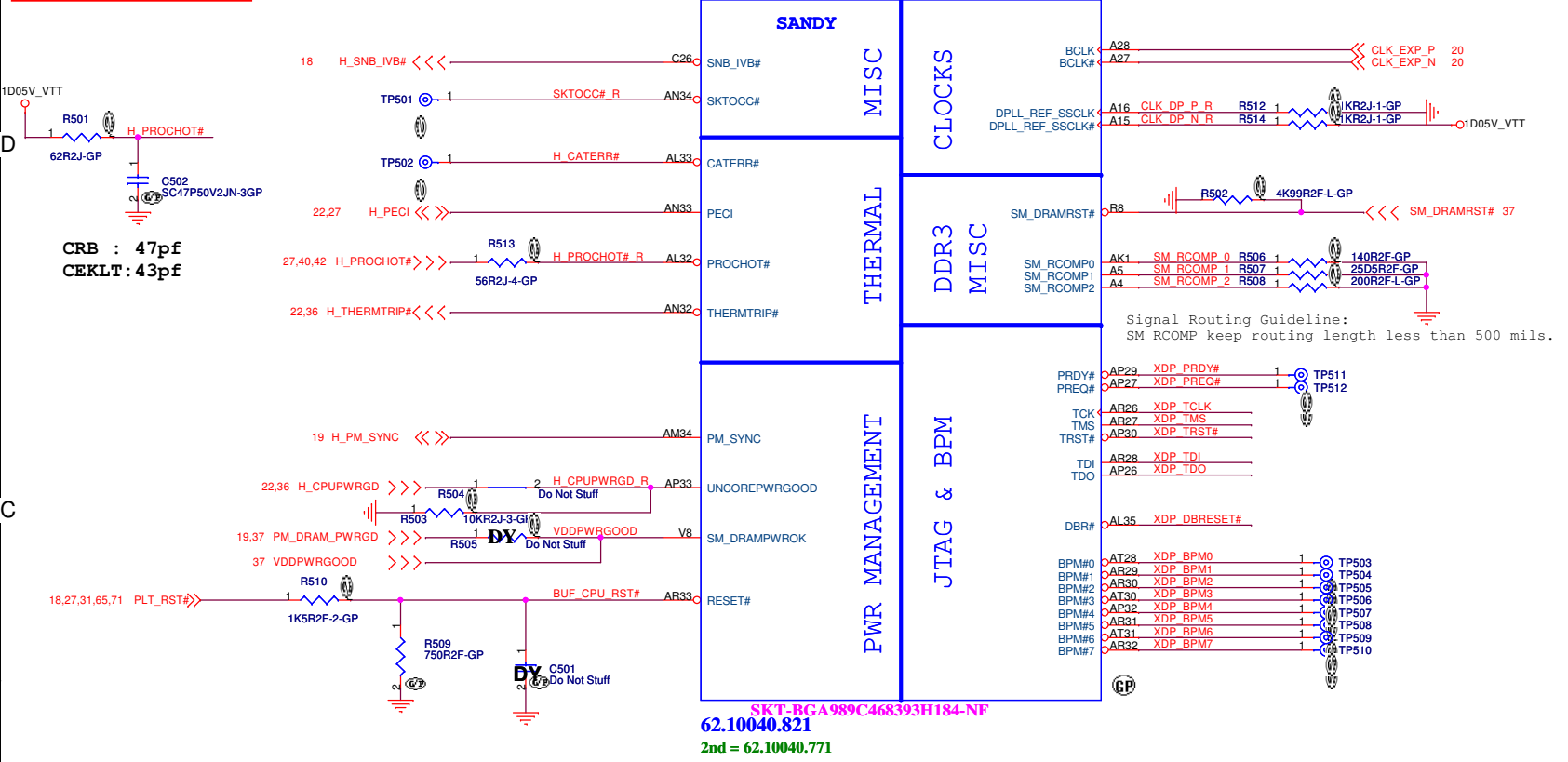
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Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils..
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.



Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

SSID = CPU



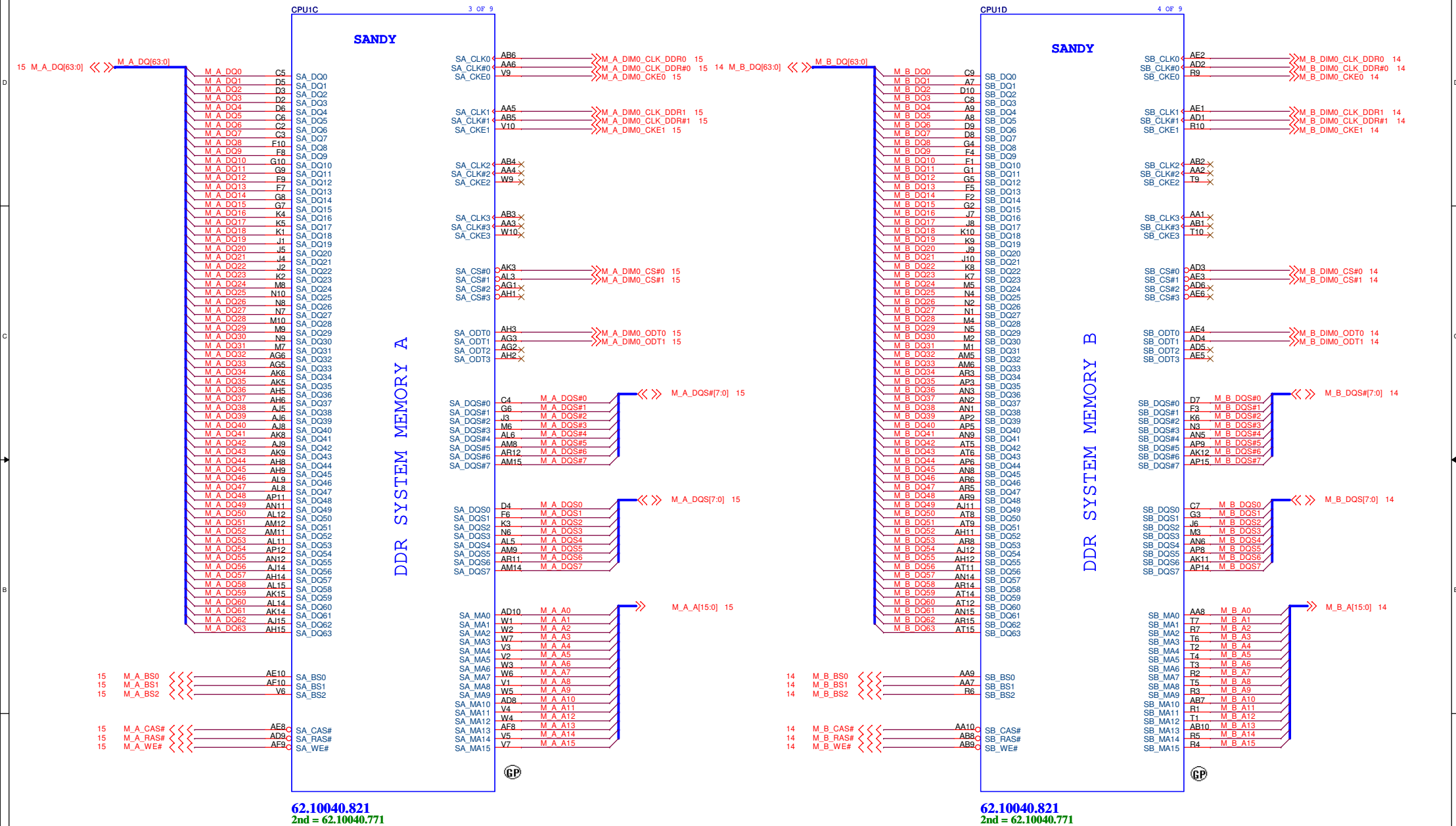
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CPU (THERMAL/CLOCK/PM)			
Title			
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SSID = CPU

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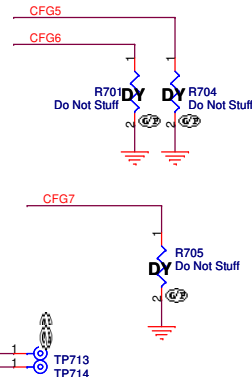
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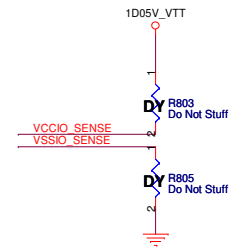
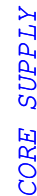
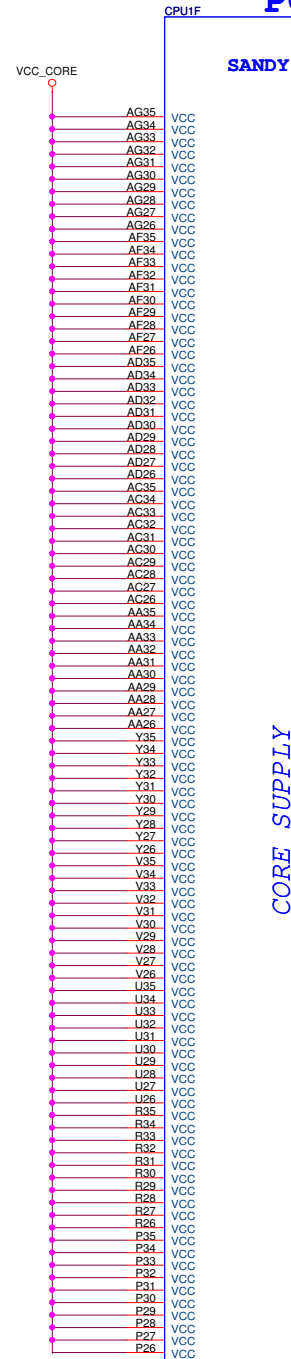
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2nd = 62.10040.771

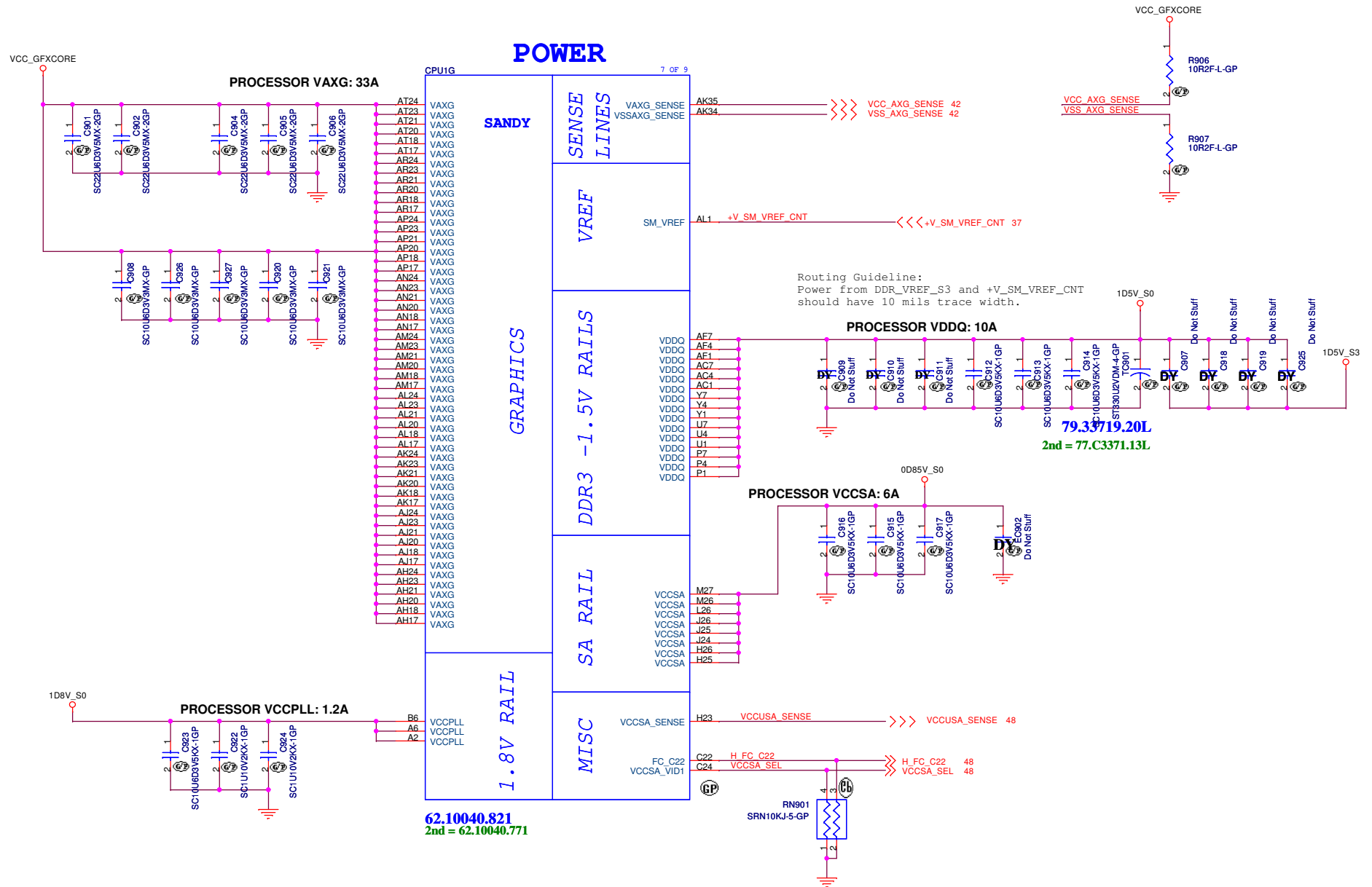


PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



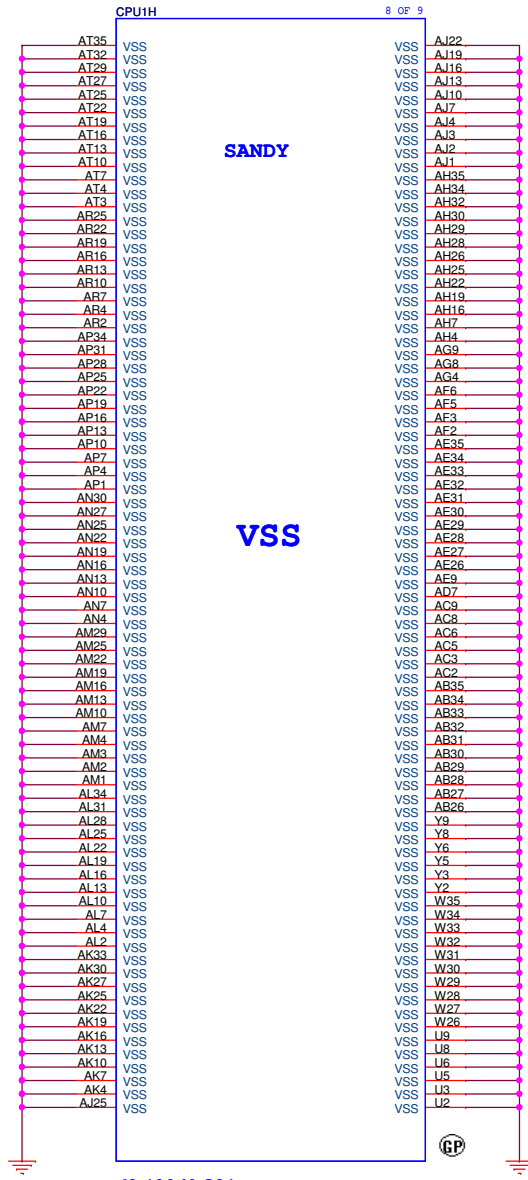
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2nd = 62.10040.771

SSID = CPU

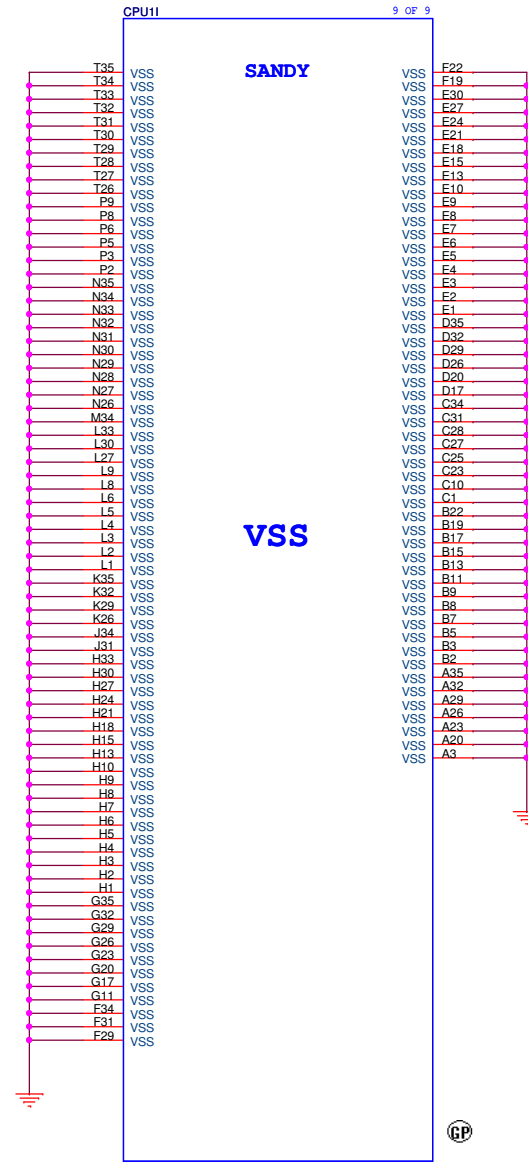


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SSID = CPU



62.10040.821
2nd = 62.10040.771



62.10040.821
2nd = 62.10040.771

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Title **CPU (VSS)**

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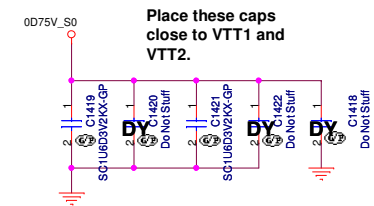
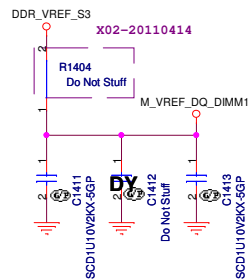
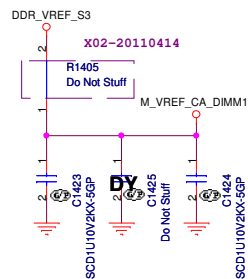
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SSID = MEMORY



Place these caps close to VTT1 and VTT2.

M_B_DQS# [7:0] 6
M_B_DQS [7:0] 6

M_B_DIM0_ODT0 6
M_B_DIM0_ODT1 6
M_VREF_CA_DIMM1
M_VREF_DQ_DIMM1
15.37 DDR3_DRAMRST#

M_B_A0 98
M_B_A1 97
M_B_A2 96
M_B_A3 95
M_B_A4 92
M_B_A5 91
M_B_A6 90
M_B_A7 89
M_B_A8 88
M_B_A9 87
M_B_A10 107
M_B_A11 84
M_B_A12 83
M_B_A13 119
M_B_A14 80
M_B_A15 78
M_B_BS2 6
M_B_BS0 6
M_B_DQ[63:0] 6

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M_B_DQ1 7
M_B_DQ2 15
M_B_DQ3 17
M_B_DQ4 4
M_B_DQ5 4
M_B_DQ6 16
M_B_DQ7 18
M_B_DQ8 21
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M_B_DQ62 192
M_B_DQ63 194

M_B_DQS#0 10
M_B_DQS#1 27
M_B_DQS#2 45
M_B_DQS#3 62
M_B_DQS#4 135
M_B_DQS#5 152
M_B_DQS#6 159
M_B_DQS#7 186
M_B_DQS0 12
M_B_DQS1 29
M_B_DQS2 47
M_B_DQS3 64
M_B_DQS4 137
M_B_DQS5 154
M_B_DQS6 171
M_B_DQS7 188

116 ODT0
120 ODT1
126 VREF_CA
1 VREF_DQ
30 RESET#
203 VTT1
204 VTT2

NP1 NP1
NP2 NP2
RAS# 110
WE# 113
CAS# 115
CS0# 114
CS1# 121
CKE0 73
CKE1 74
CK0 101
CK0# 103
CK1 102
CK1# 104
DM0 11
DM1 28
DM2 46
DM3 63
DM4 136
DM5 153
DM6 170
DM7 187

BA0 BA0
BA1 BA1
DM0 11
DM1 28
DM2 46
DM3 63
DM4 136
DM5 153
DM6 170
DM7 187

SDA 200
SCL 202
EVENT# 198
VDDSPD 199
SA0 DIM1 197
SA1 DIM1 201
NC#1 77
NC#2 122
NC#/TEST 125

VDD1 75
VDD2 76
VDD3 81
VDD4 82
VDD5 87
VDD6 88
VDD7 93
VDD8 94
VDD9 99
VDD10 100
VDD11 105
VDD12 106
VDD13 112
VDD14 117
VDD15 118
VDD16 123
VDD17 124

VSS 2
VSS 3
VSS 8
VSS 9
VSS 13
VSS 14
VSS 19
VSS 20
VSS 25
VSS 26
VSS 31
VSS 32
VSS 37
VSS 38
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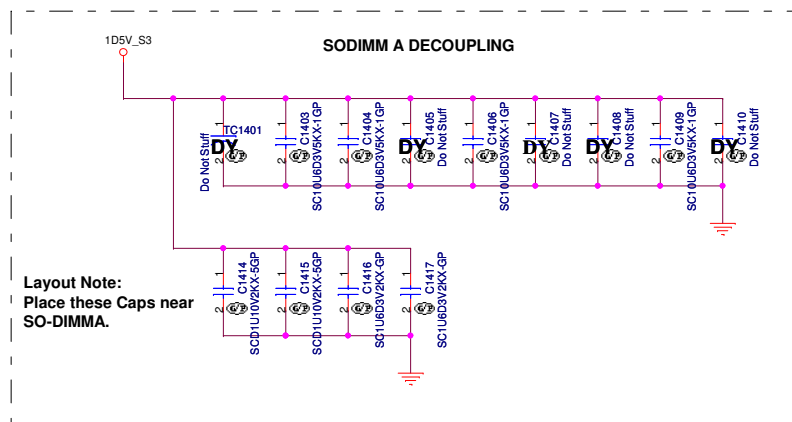
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DQS1# 27
DQS2# 45
DQS3# 62
DQS4# 135
DQS5# 152
DQS6# 159
DQS7# 186
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DQS2 47
DQS3 64
DQS4 137
DQS5 154
DQS6 171
DQS7 188

116 ODT0
120 ODT1
126 VREF_CA
1 VREF_DQ
30 RESET#
203 VTT1
204 VTT2

DDR3-204P-43-GP
62.10017.N71

M_B_RAS# 6
M_B_WE# 6
M_B_CAS# 6
M_B_DIM0_CS#0 6
M_B_DIM0_CS#1 6
M_B_DIM0_CKE0 6
M_B_DIM0_CKE1 6
M_B_DIM0_CLK_DDR0 6
M_B_DIM0_CLK_DDR#0 6
M_B_DIM0_CLK_DDR1 6
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PCH_SMBDATA 15.20.65
PCH_SMBCLK 15.20.65
TS#_DIMM0_1 15



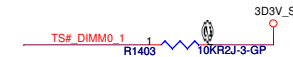
Layout Note:
Place these Caps near SO-DIMMA.

SODIMM A DECOUPLING

Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0_DIM0 = 0, SA1_DIM0 = 1
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

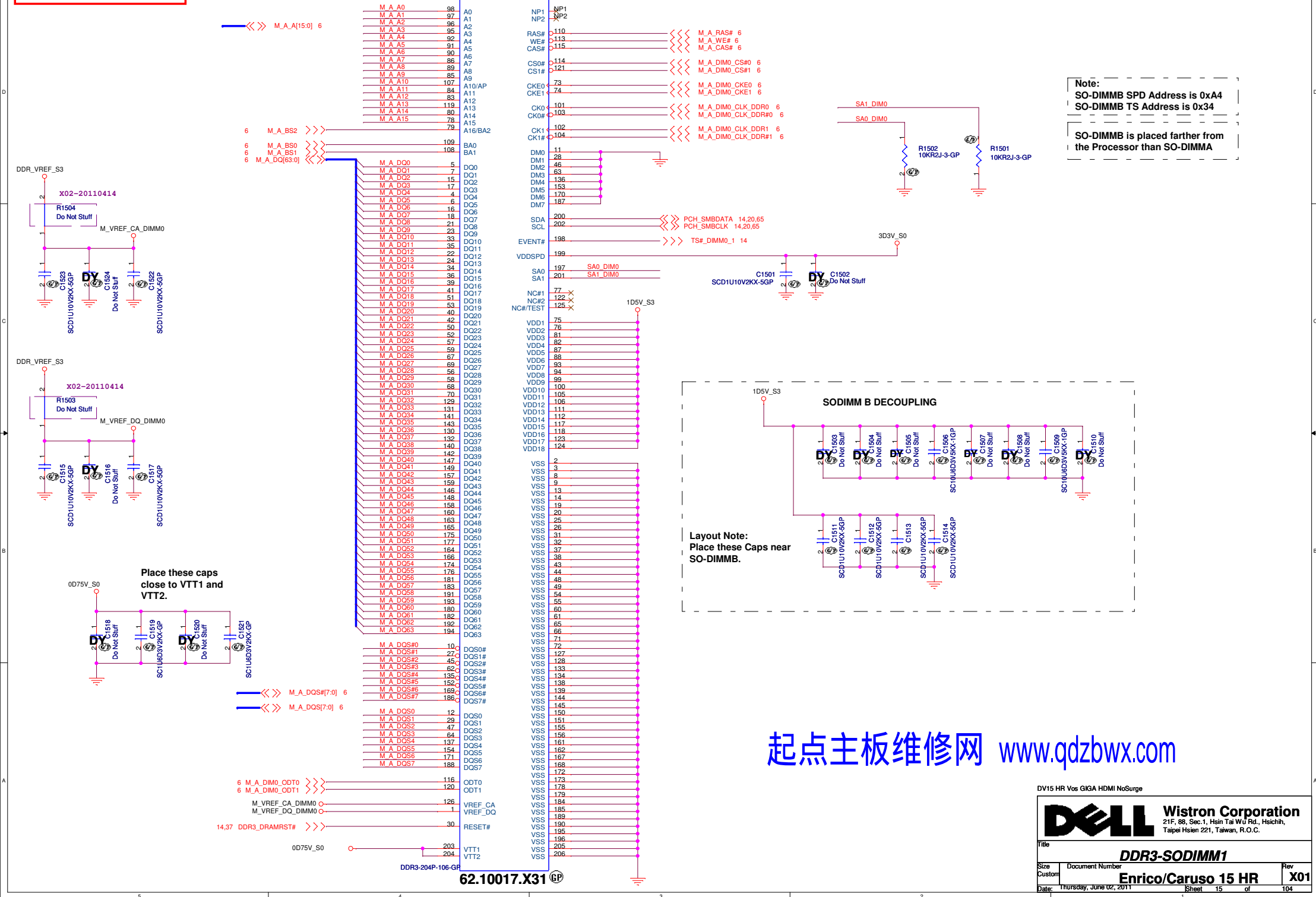
Thermal EVENT



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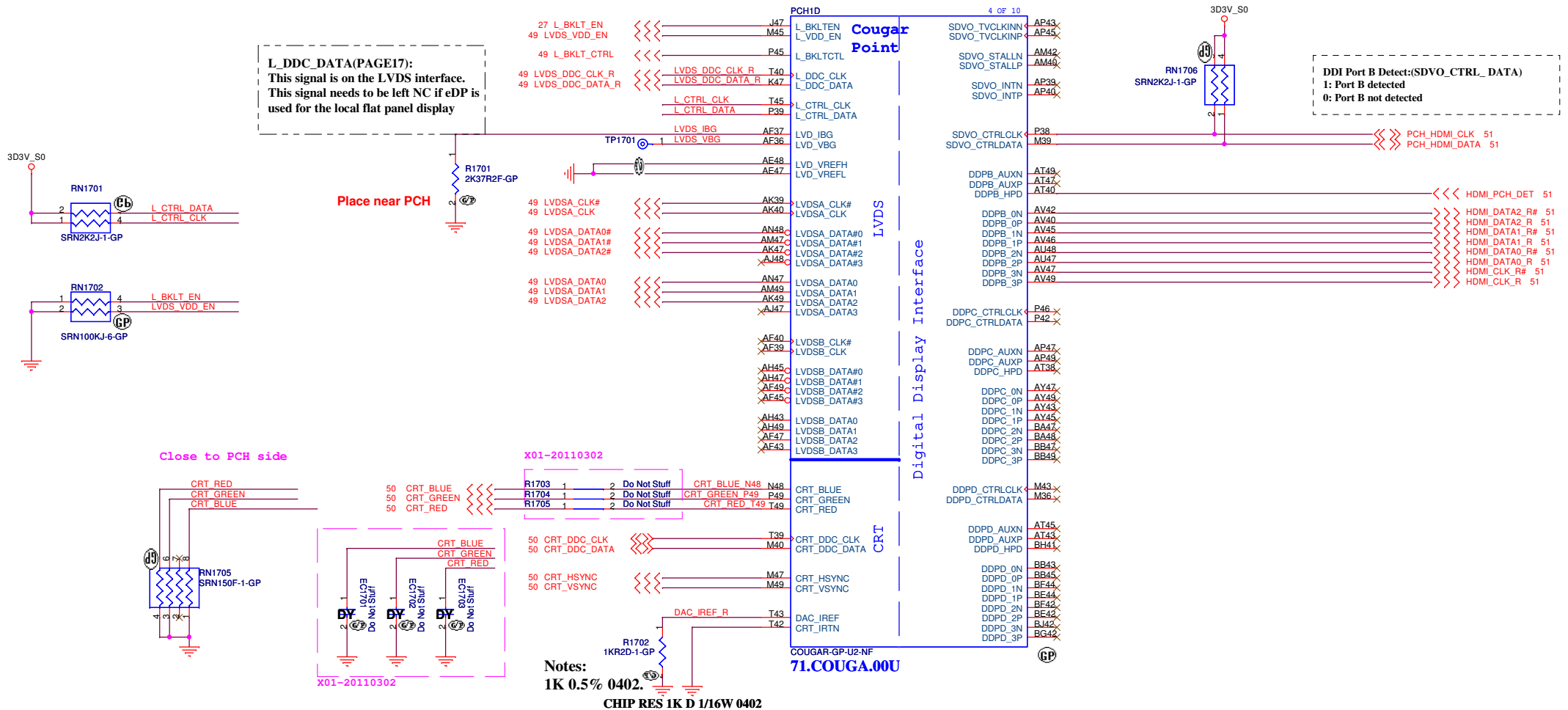
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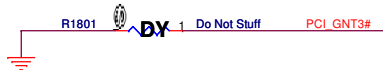
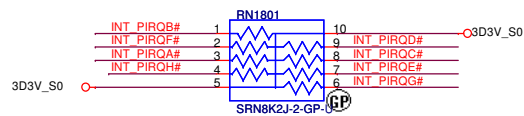
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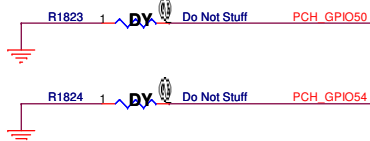
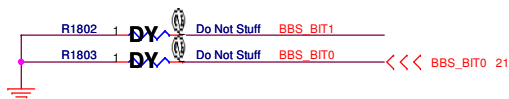


SSID = PCH

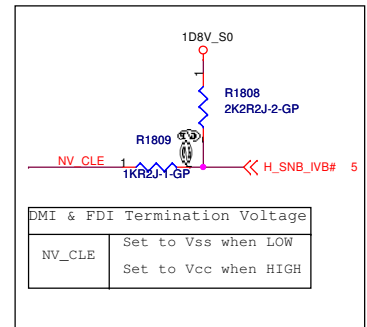
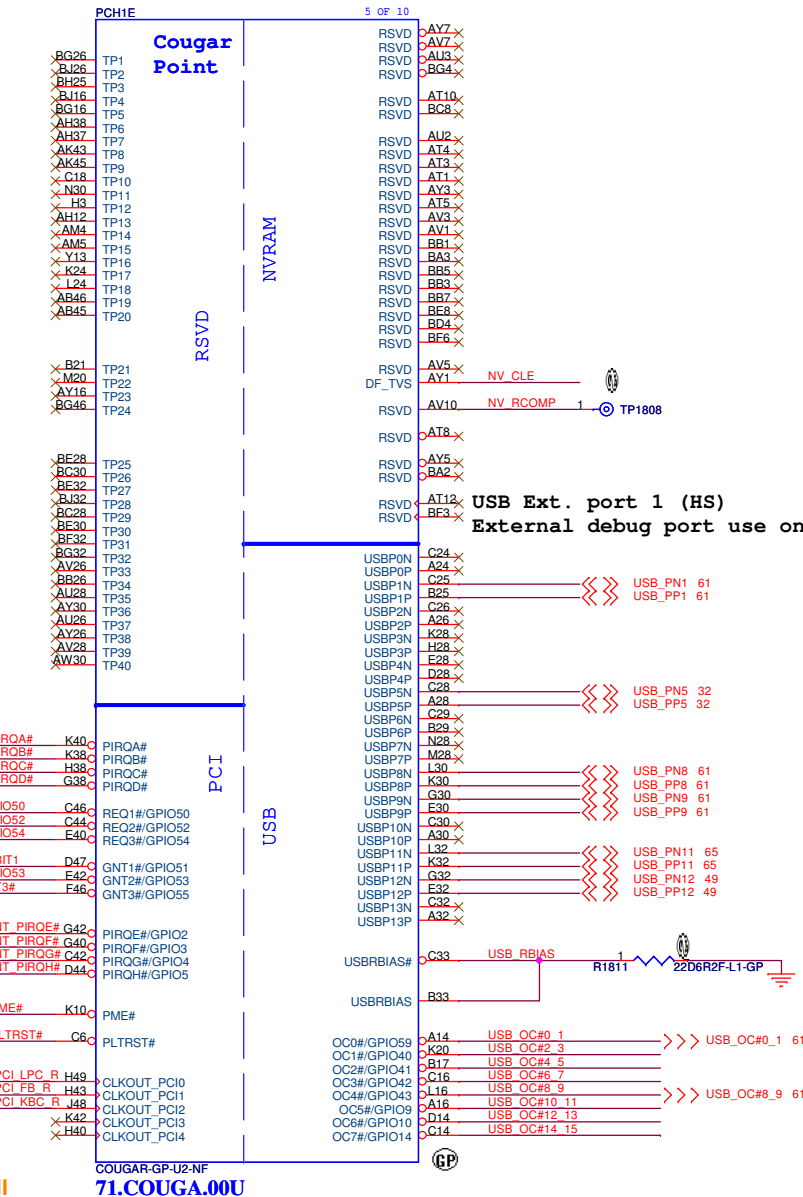
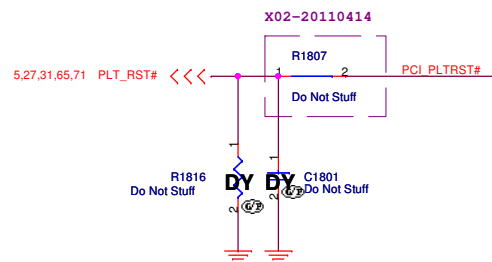
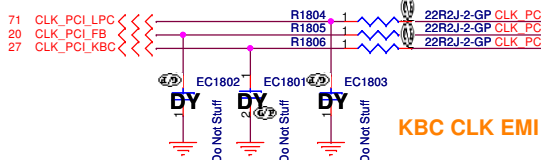
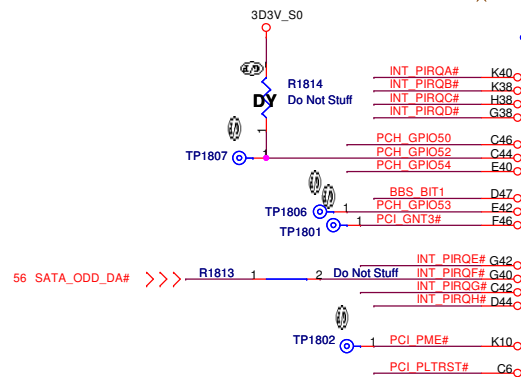
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A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

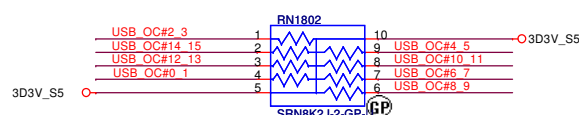


BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI (Default)



USB Table

Pair	Device
0	X
1	USB Ext. port 1 (HS)
2	X
3	X
4	X
5	CARD READER
6	X
7	X
8	USB Ext. port 2
9	USB Ext. port 3
10	X
11	Mini Card1 (WLAN)
12	CAMERA
13	X



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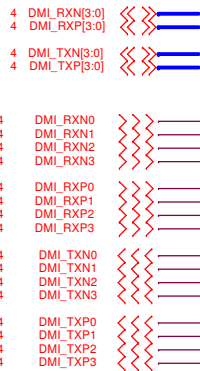


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SSID = PCH

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Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and
routing length less than 500
mils.
DMI_IRCOMP keep W=4 mils and
routing length less than 500
mils.



PCH1C

3 OF 10

Cougar
Point

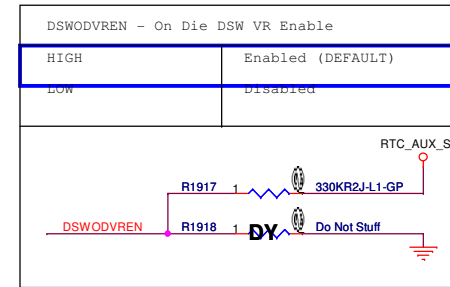
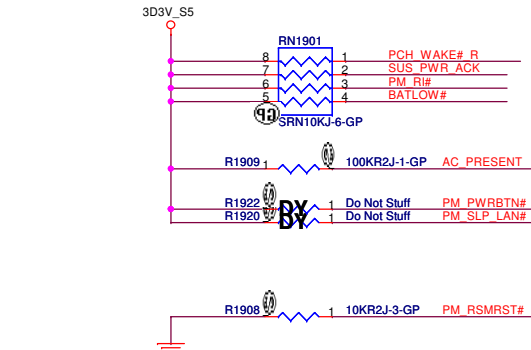
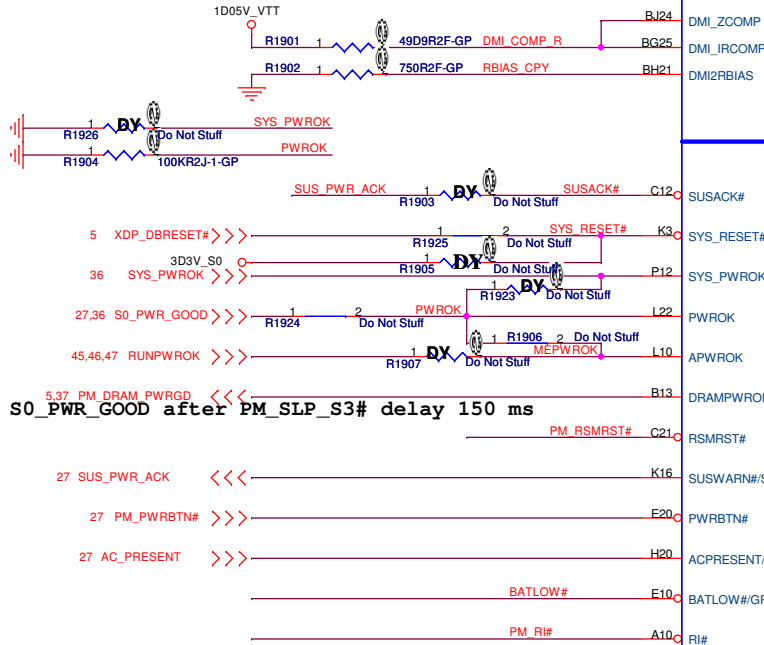
DMI

FDI



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71.COUGA.00U



15 HR Vos GIGA HDMI NoSurge

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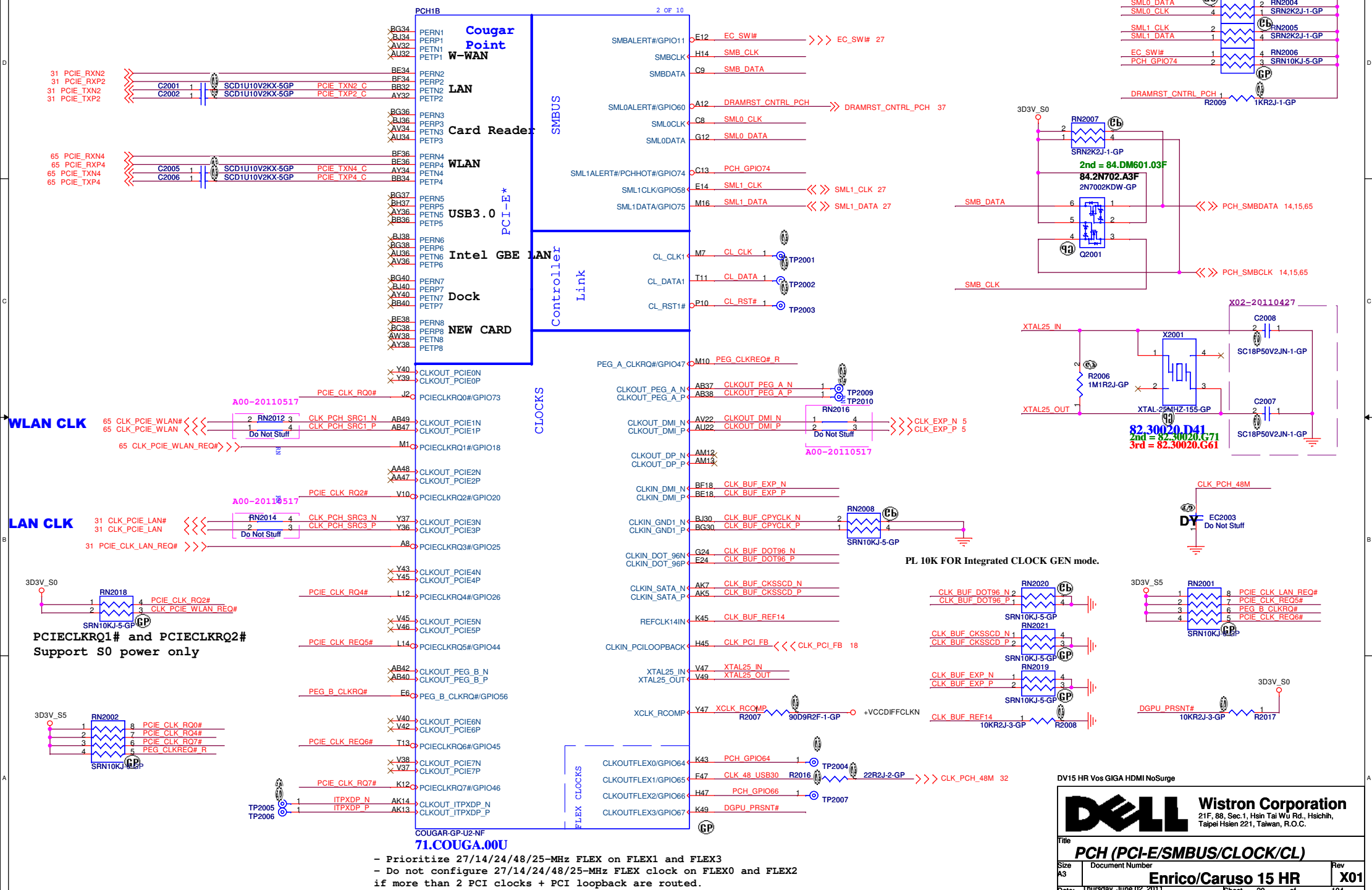
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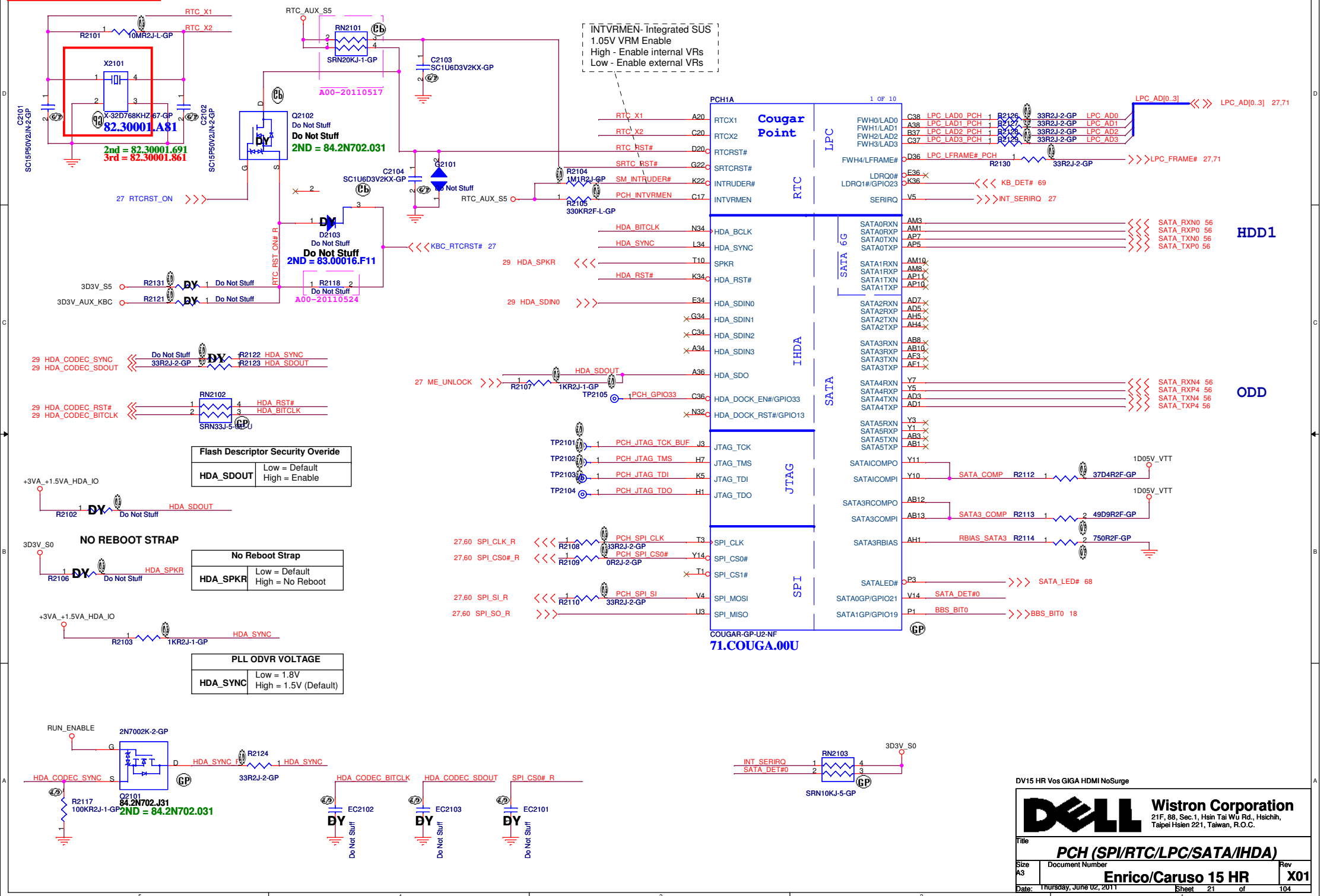
Size A3 Document Number **Enrico/Caruso 15 HR** Rev **X01**

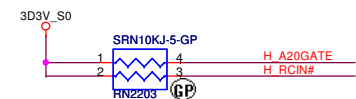
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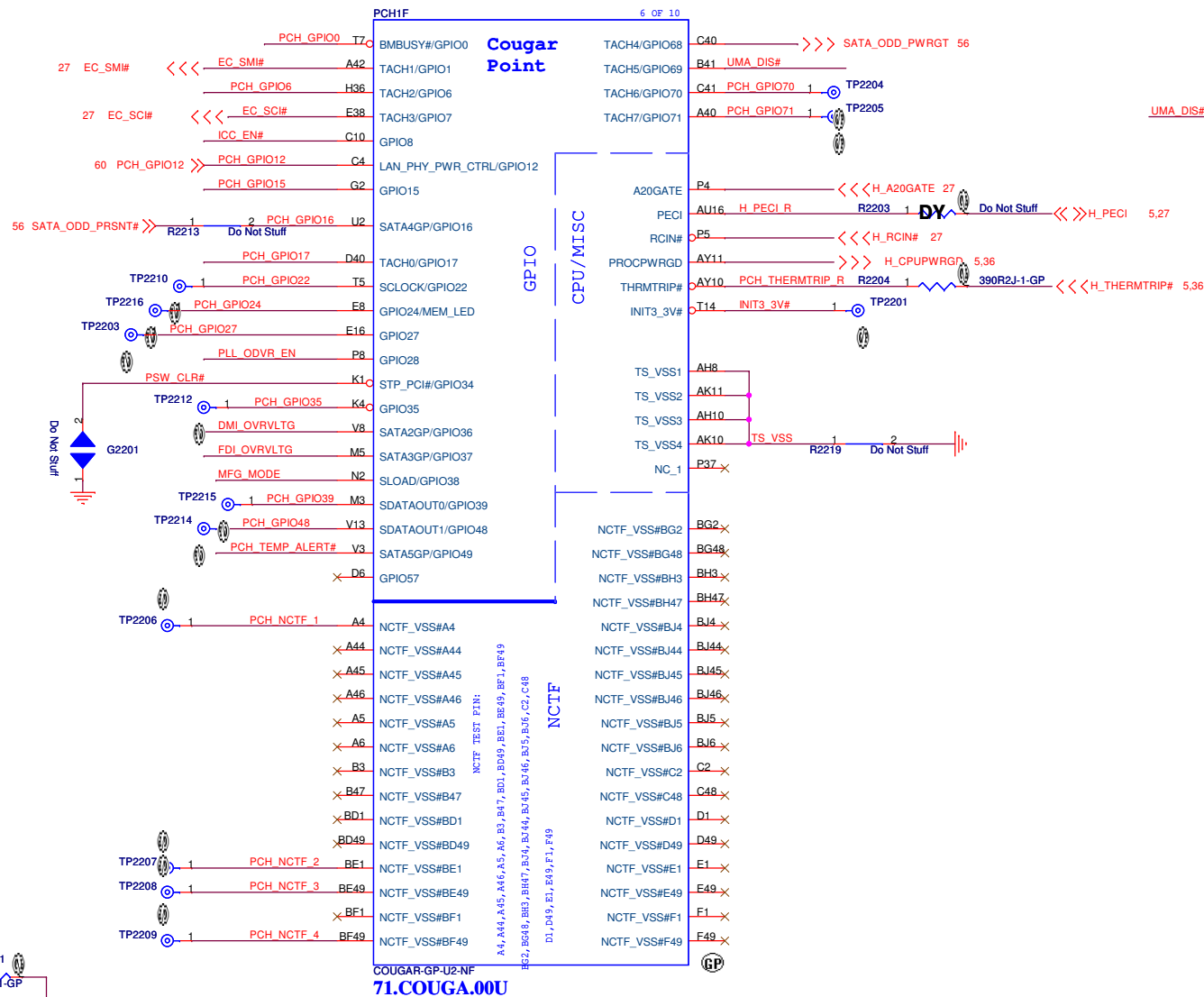
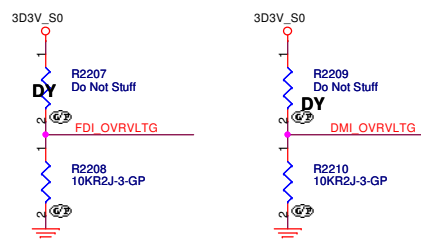
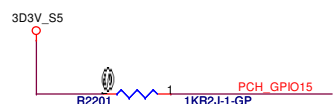
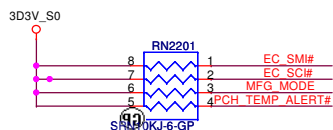
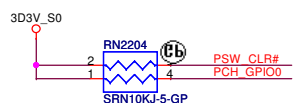
SSID = PCH





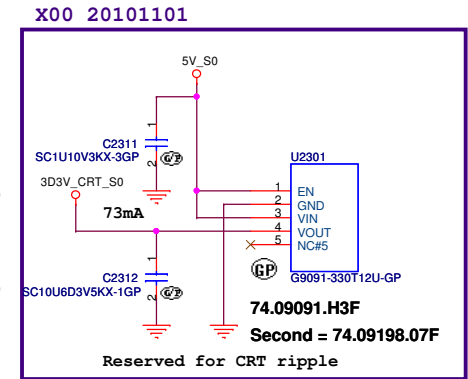
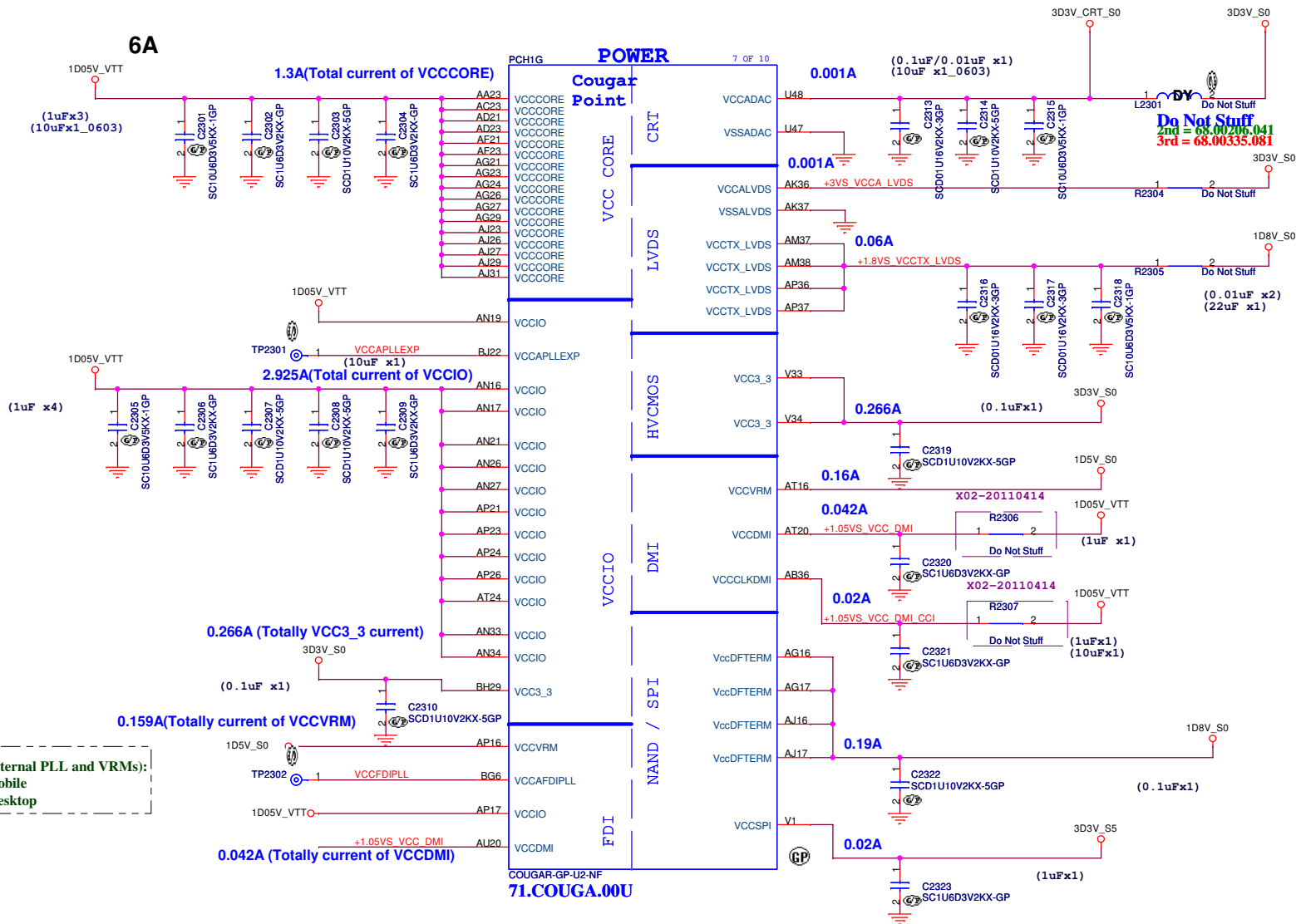


The image shows two circuit diagrams. The left diagram shows a 3D3V_S0 pin connected to a resistor R2220, which is then connected to PCH_GPIO48. A note 'Do Not Stuff' is placed between the resistor and the pin. The right diagram shows a 3D3V_S5 pin connected to a resistor R2224, which is then connected to PCH_GPIO12. Both diagrams include a ground symbol connected to the other end of the resistors.

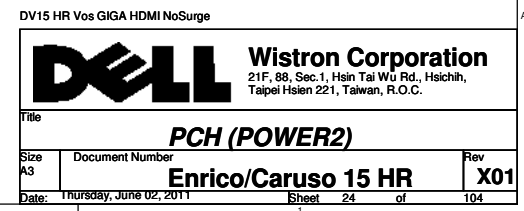


PLL ODVR EN **DY** 1 R2212 Do Not Stuff

SSID = PCH



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SSID = PCH

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PCH1H 8 OF 10		
H5	VSS	
AA17	VSS	AK38
AA2	VSS	AK4
AA3	VSS	AK42
AA33	VSS	AK46
AA34	VSS	AK8
AB11	VSS	AL16
AB14	VSS	AL17
AB39	VSS	AL19
AB4	VSS	AL2
AB43	VSS	AL21
AB5	VSS	AL23
AB7	VSS	AL26
AC19	VSS	AL27
AC2	VSS	AL31
AC21	VSS	AL33
AC24	VSS	AL34
AC33	VSS	AL48
AC34	VSS	AM11
AC48	VSS	AM14
AD10	VSS	AM36
AD11	VSS	AM39
AD12	VSS	AM43
AD13	VSS	AM45
AD19	VSS	AM46
AD24	VSS	AM7
AD26	VSS	AN2
AD27	VSS	AN29
AD33	VSS	AN3
AD34	VSS	AN31
AD36	VSS	AP12
AD37	VSS	AP19
AD38	VSS	AP28
AD39	VSS	AP30
AD4	VSS	AP32
AD40	VSS	AP38
AD42	VSS	AP4
AD43	VSS	AP42
AD45	VSS	AP46
AD46	VSS	AP8
AD8	VSS	AR2
AE2	VSS	AR48
AE3	VSS	AT11
AE10	VSS	AT13
AE12	VSS	AT18
AD14	VSS	AT22
AD16	VSS	AT26
AE16	VSS	AT28
AF19	VSS	AT30
AF24	VSS	AT32
AF26	VSS	AT34
AF27	VSS	AT39
AF29	VSS	AT42
AF31	VSS	AT46
AF38	VSS	AT7
AF4	VSS	AU24
AF42	VSS	AU30
AF46	VSS	AV16
AF5	VSS	AV20
AF7	VSS	AV24
AF8	VSS	AV30
AG19	VSS	AV38
AG2	VSS	AV4
AG31	VSS	AV43
AG48	VSS	AV8
AH11	VSS	AW14
AH3	VSS	AW18
AH36	VSS	AW2
AH39	VSS	AW22
AH40	VSS	AW26
AH42	VSS	AW28
AH46	VSS	AW32
AH7	VSS	AW34
AJ19	VSS	AW36
AJ21	VSS	AW40
AJ24	VSS	AW48
AJ33	VSS	AV11
AJ34	VSS	AY12
AK12	VSS	AY22
AK3	VSS	AY28

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PCH1I 9 OF 10		
AY4	VSS	H46
AY42	VSS	K18
AY46	VSS	K26
AY8	VSS	K39
B11	VSS	K46
B15	VSS	K7
B19	VSS	L18
B23	VSS	L2
B27	VSS	L20
B31	VSS	L26
B35	VSS	L28
B39	VSS	L36
B7	VSS	L48
F45	VSS	M12
BB12	VSS	P16
BB16	VSS	M18
BB20	VSS	M22
BB22	VSS	M24
BB24	VSS	M30
BB28	VSS	M32
BB30	VSS	M34
BB38	VSS	M38
BB4	VSS	M4
BB46	VSS	M42
BC14	VSS	M46
BC18	VSS	M8
BC2	VSS	N18
BC22	VSS	P30
BC26	VSS	N47
BC32	VSS	P11
BC34	VSS	P18
BC36	VSS	T33
BC40	VSS	P40
BC42	VSS	P43
BC48	VSS	P47
BD46	VSS	P7
BD5	VSS	R2
BE22	VSS	R48
BE26	VSS	T12
BE40	VSS	T31
BF10	VSS	T37
BF12	VSS	T4
BF16	VSS	W34
BF19	VSS	T46
BF22	VSS	T47
BF24	VSS	T8
BF26	VSS	V11
BF28	VSS	V17
BD3	VSS	V26
BF30	VSS	V27
BF38	VSS	V29
BF40	VSS	V31
BF8	VSS	V36
BG17	VSS	V39
BG21	VSS	V43
BG33	VSS	V7
BG44	VSS	W17
BT22	VSS	W19
BH11	VSS	W2
BH15	VSS	W27
BH17	VSS	W48
BH19	VSS	Y12
H10	VSS	Y38
BH27	VSS	Y4
BH31	VSS	Y42
BH33	VSS	Y46
BH35	VSS	Y8
BH39	VSS	BG29
BH43	VSS	N24
BH7	VSS	AJ3
D3	VSS	AD47
D12	VSS	B43
D16	VSS	BE10
D18	VSS	BG41
D22	VSS	G14
D24	VSS	H16
D26	VSS	T36
D30	VSS	BG22
D32	VSS	BG24
D34	VSS	C22
D38	VSS	AP13
D42	VSS	M14
D6	VSS	AP3
E18	VSS	AF1
E26	VSS	BE16
G18	VSS	BC16
G20	VSS	BG28
G26	VSS	BJ28
G28	VSS	
G36	VSS	
G48	VSS	
H12	VSS	
H18	VSS	
H22	VSS	
H24	VSS	
H26	VSS	
H30	VSS	
H32	VSS	
H34	VSS	
F3	VSS	

Cougar
Point

COUGAR-GP-U2-NF



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DV15 HR Vos GIGA HDMI NoSurge



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Title PCH (VSS)		
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Title

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Size
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Document Number

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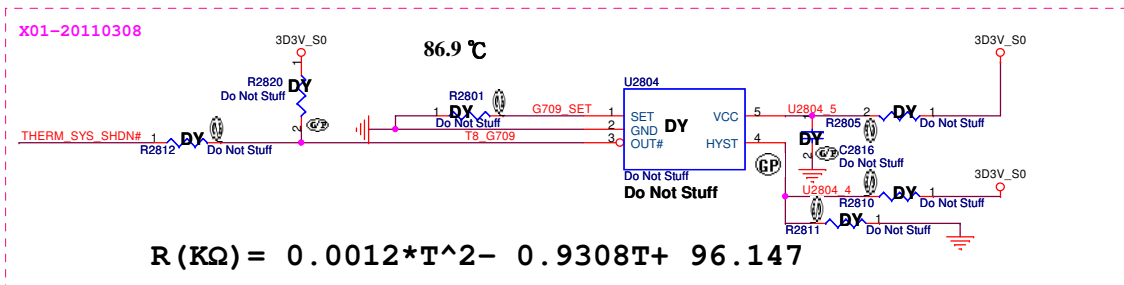
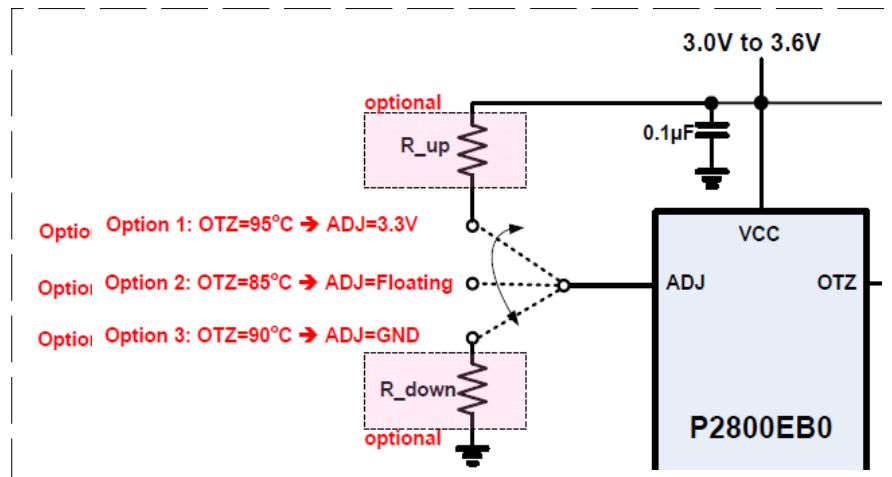
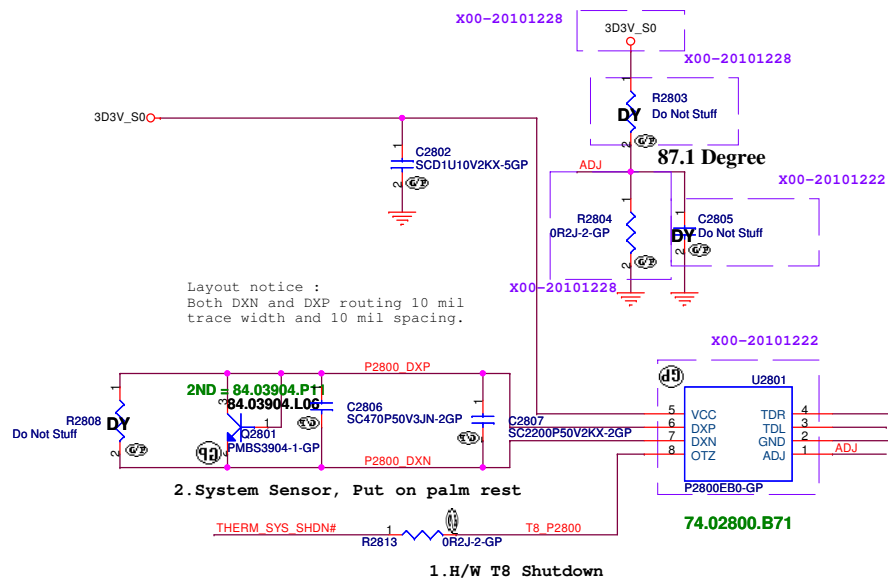
Rev
X01

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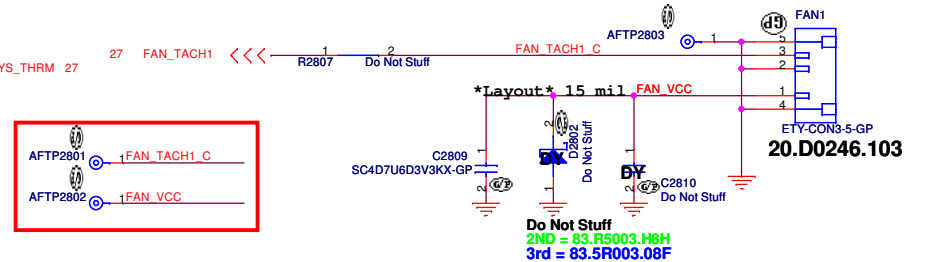
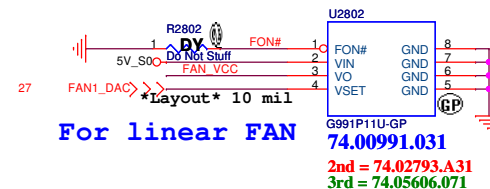
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SSID = Thermal

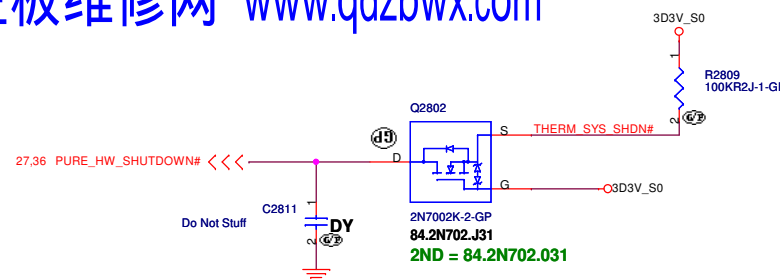
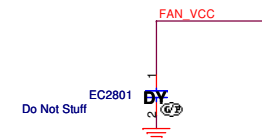
Thermal sensor P2800



Fan controller G991

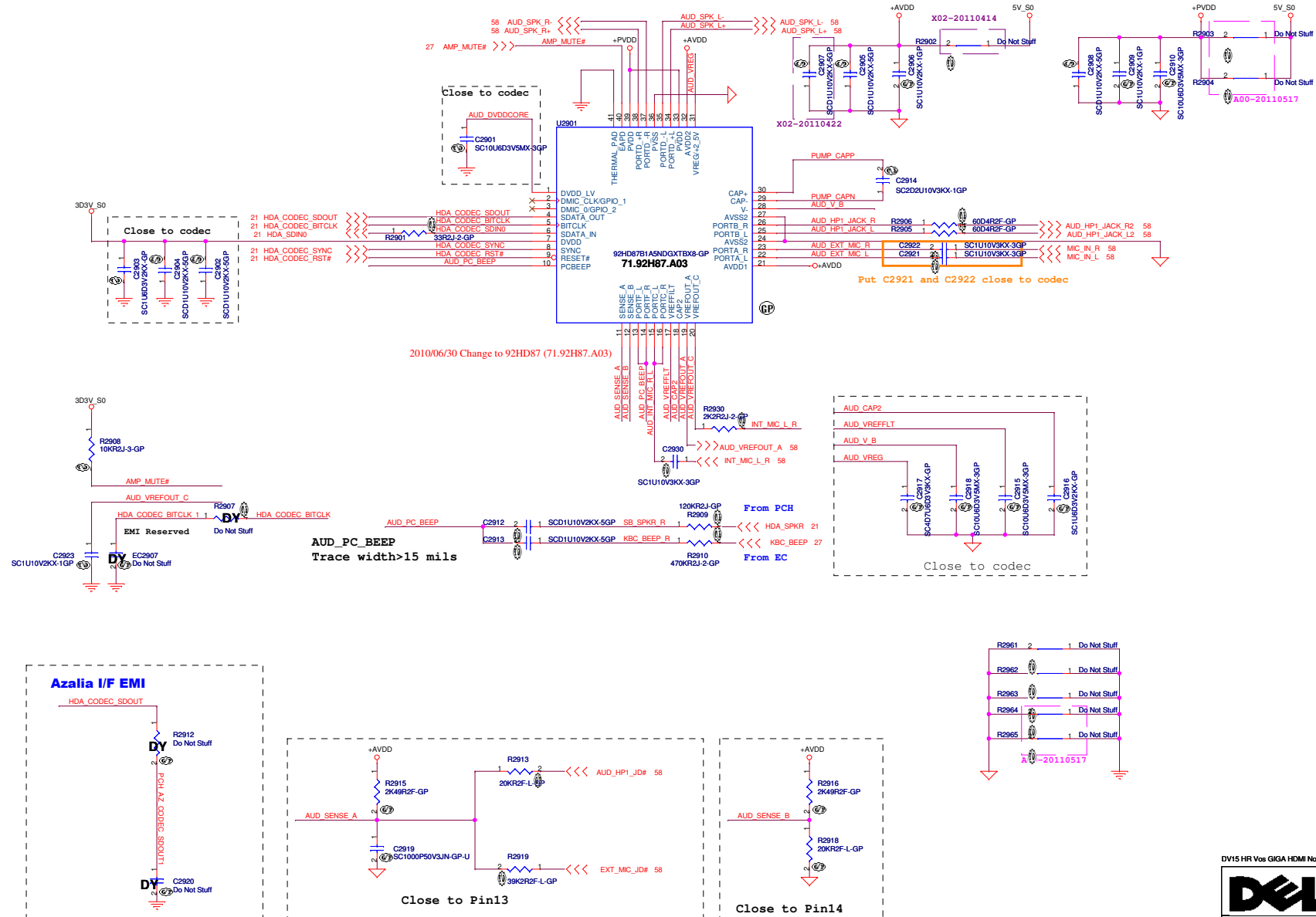


EMI/ESD



SSID = AUDIO

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Title

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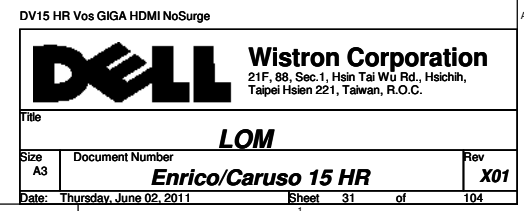
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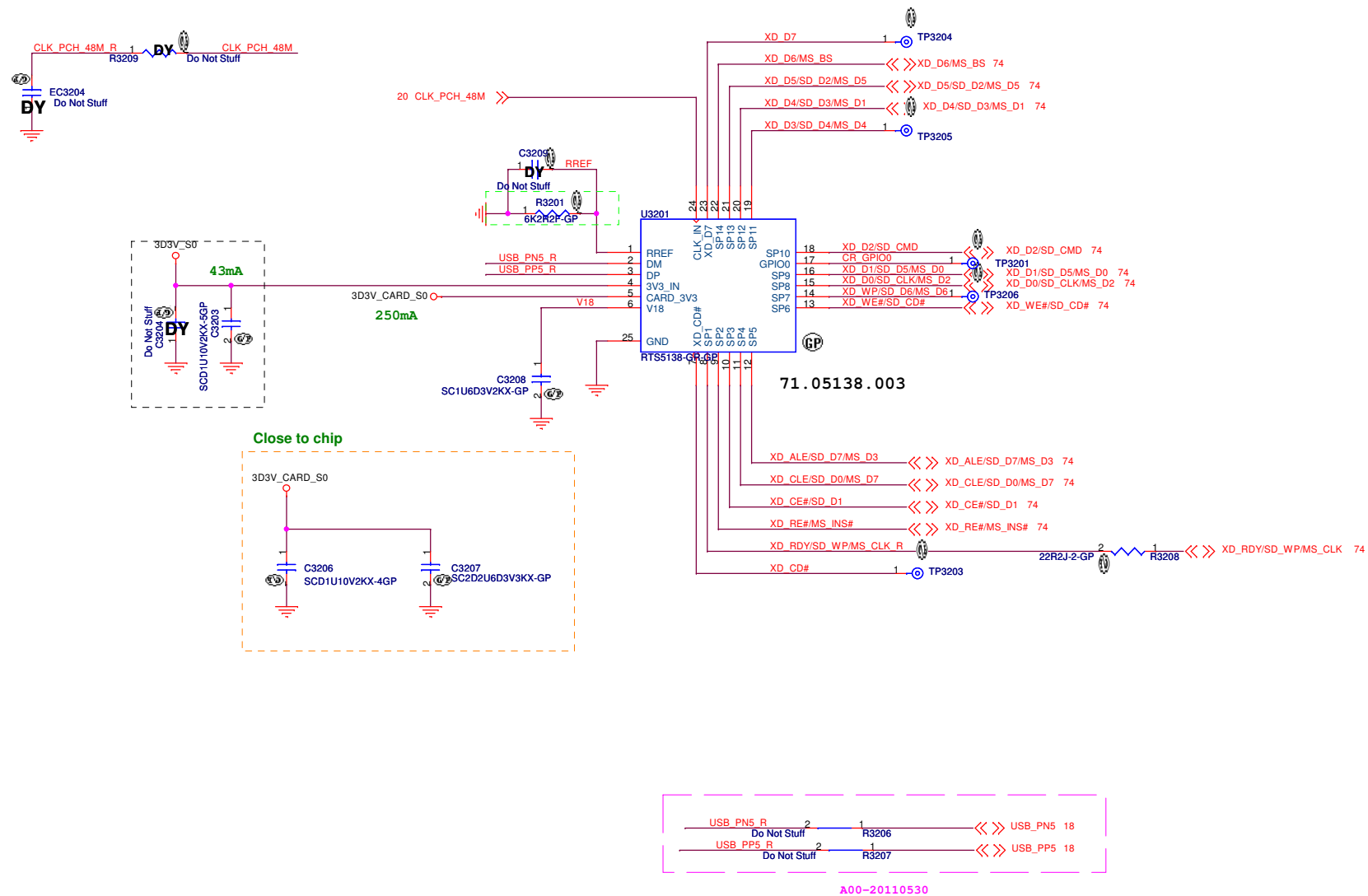
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SSID = SDIO



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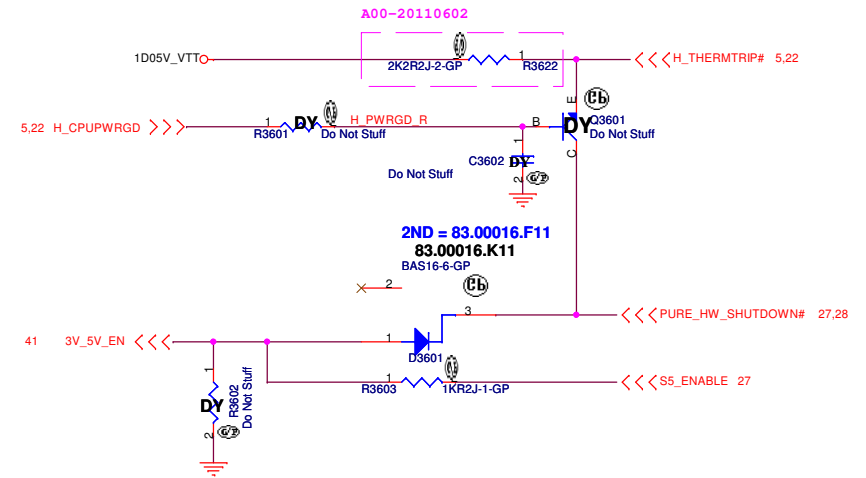
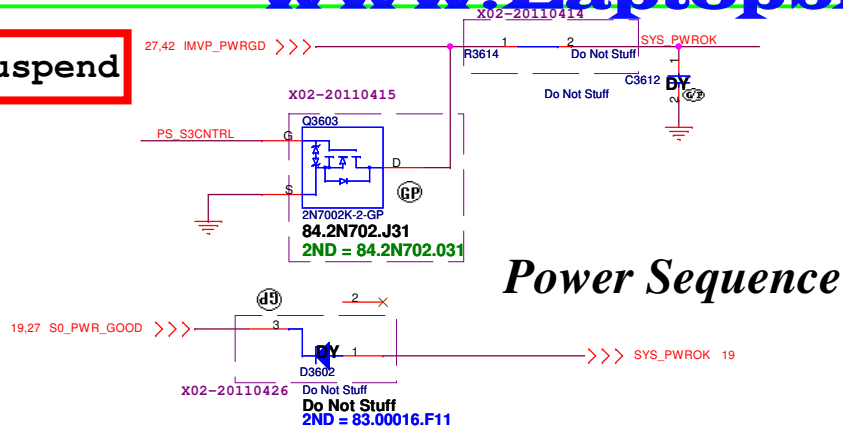
Rev

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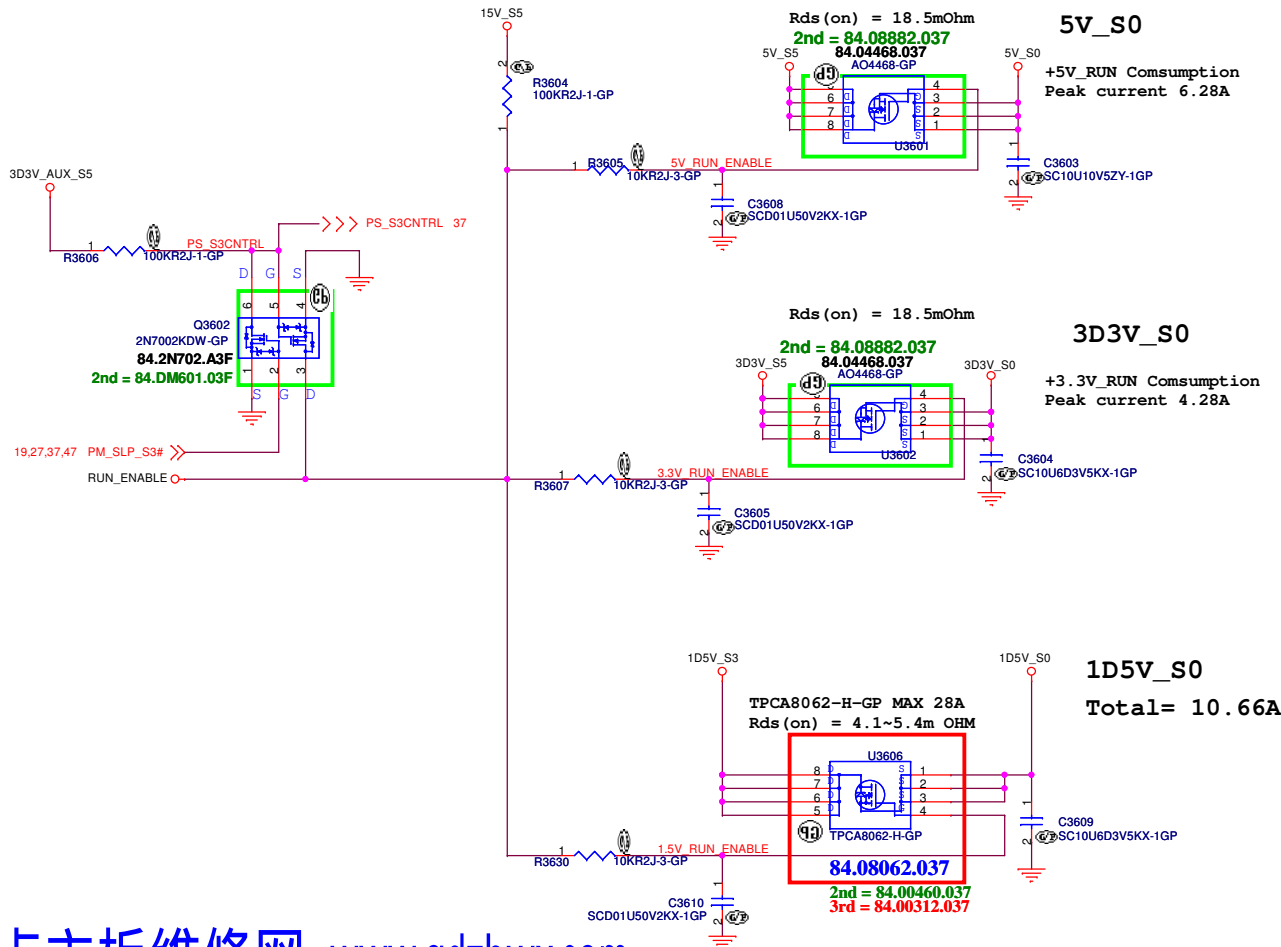
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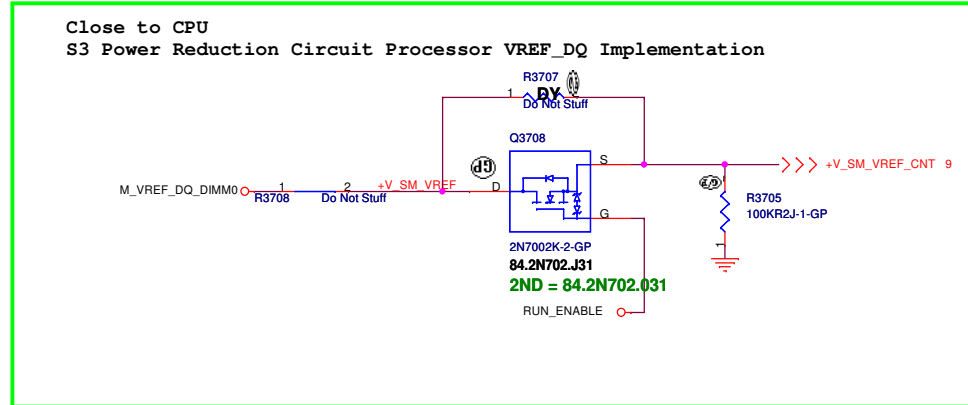
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SSID = Reset.Suspend

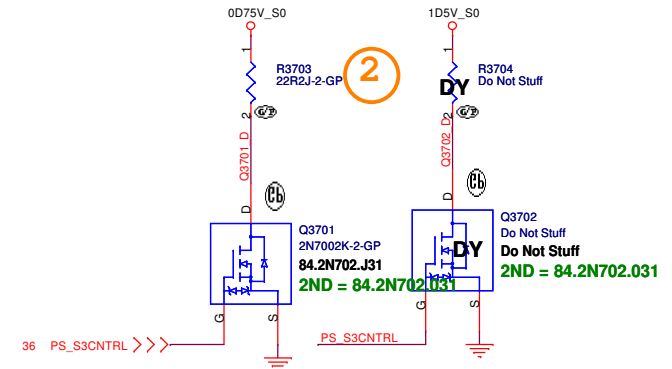


ROSA Run Power

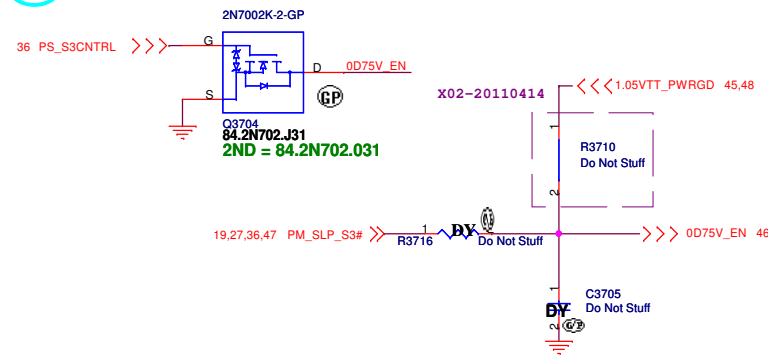




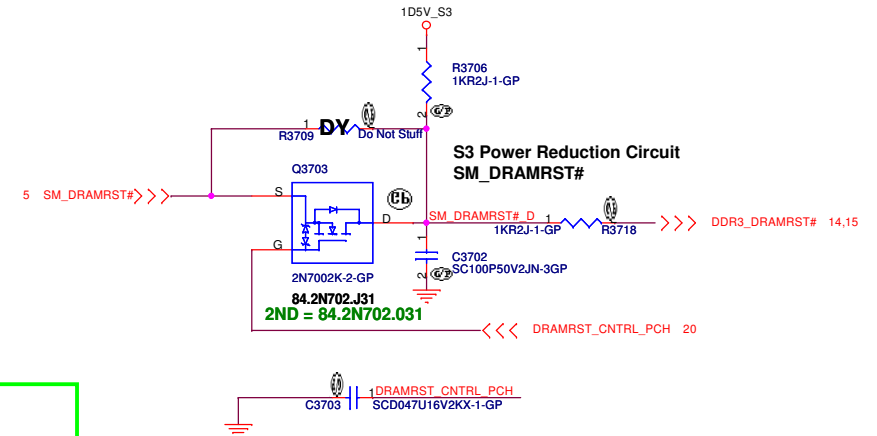
Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



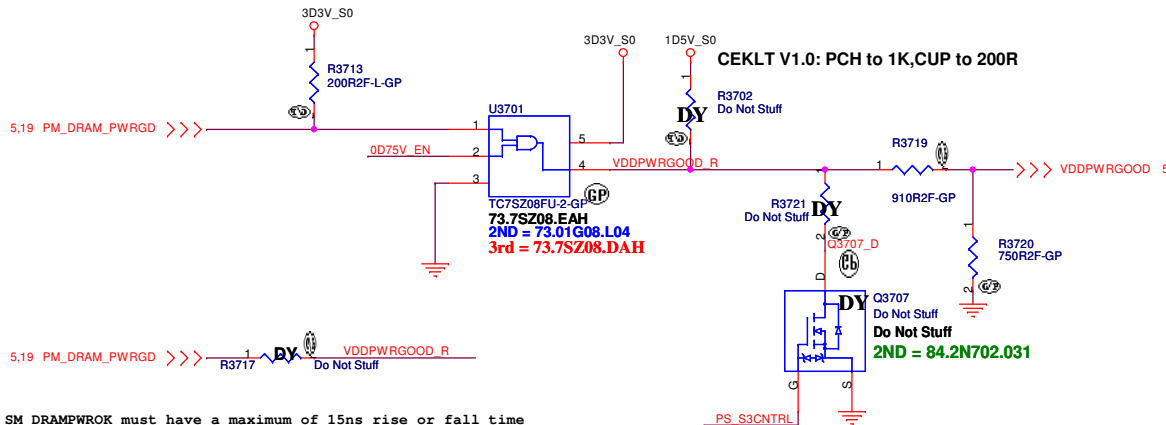
5 S3 Power Reduction



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK

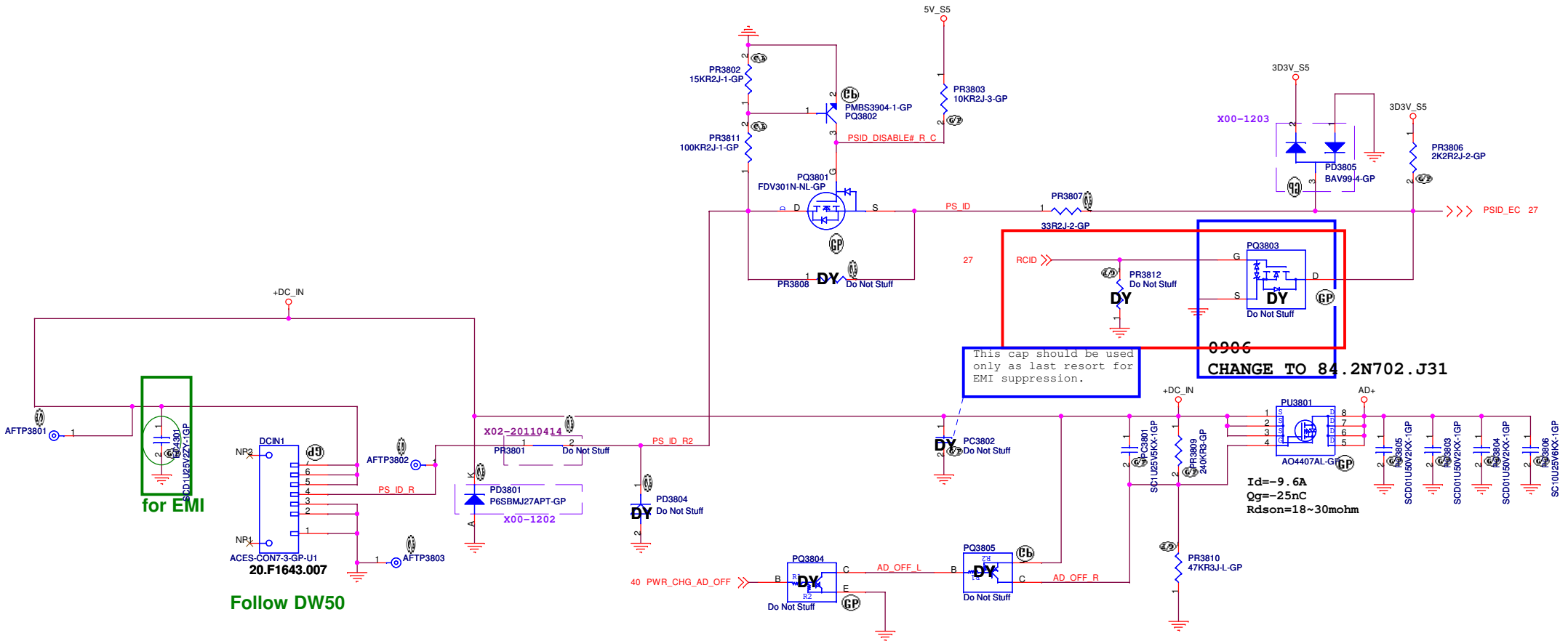


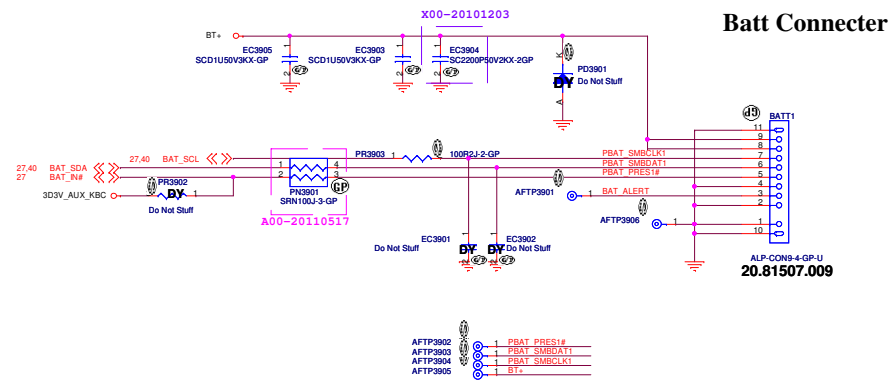
SM_DRAMPWROK must have a maximum of 15ns rise or fall time over VDDQ * 0.55± 200mV and the edge must be monotonic

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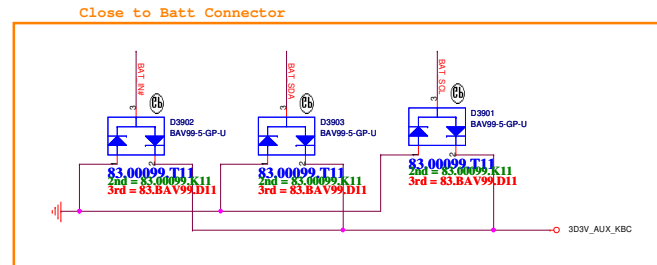
SSID = PWR.Support

DCin CONN



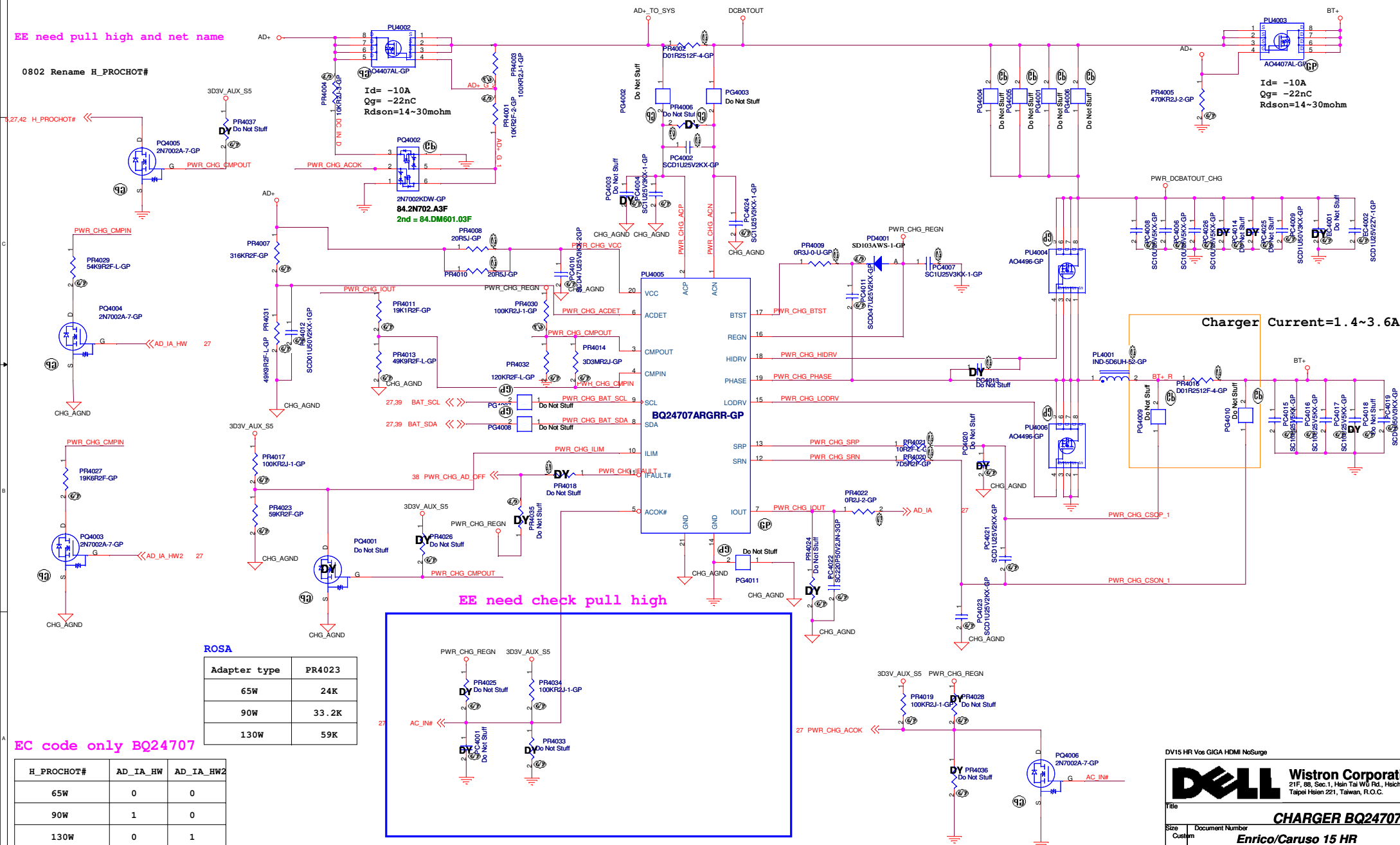


For actual location, need to be swap all pin



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0802 Rename H_PROCHOT#



DV15 HR V06 GIGA HDMI NoSurge



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[illegible]**CHARGER BQ24707**

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Document Number

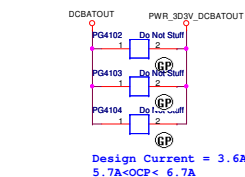
Enrico/Caruso 15 HR

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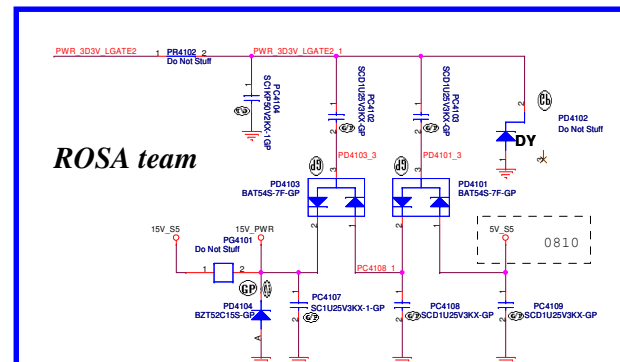
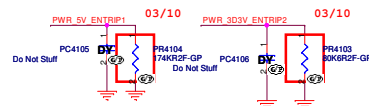
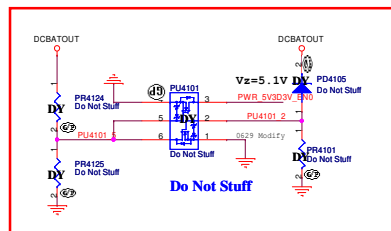
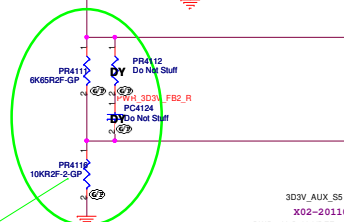
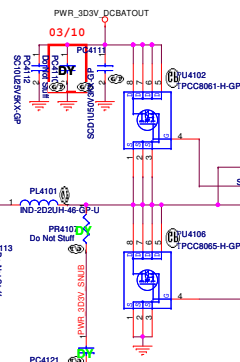
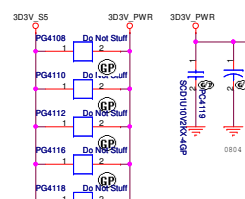
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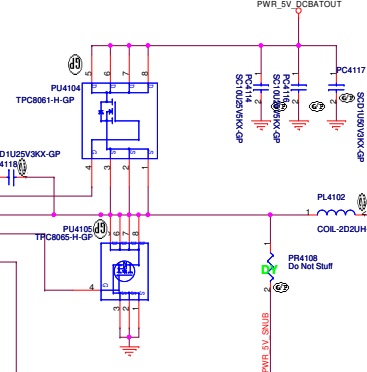
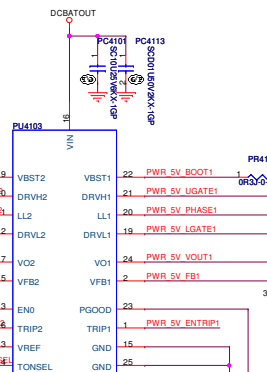
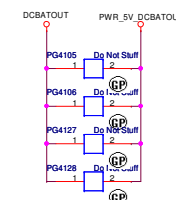
104



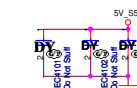
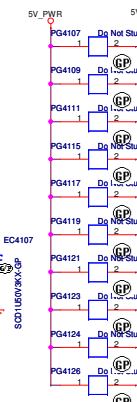
Design Current = 3.6A
5.7A < OCP < 6.7A



ROSA team



Design Current = 8.24A
12.3<OCP< 15.3A

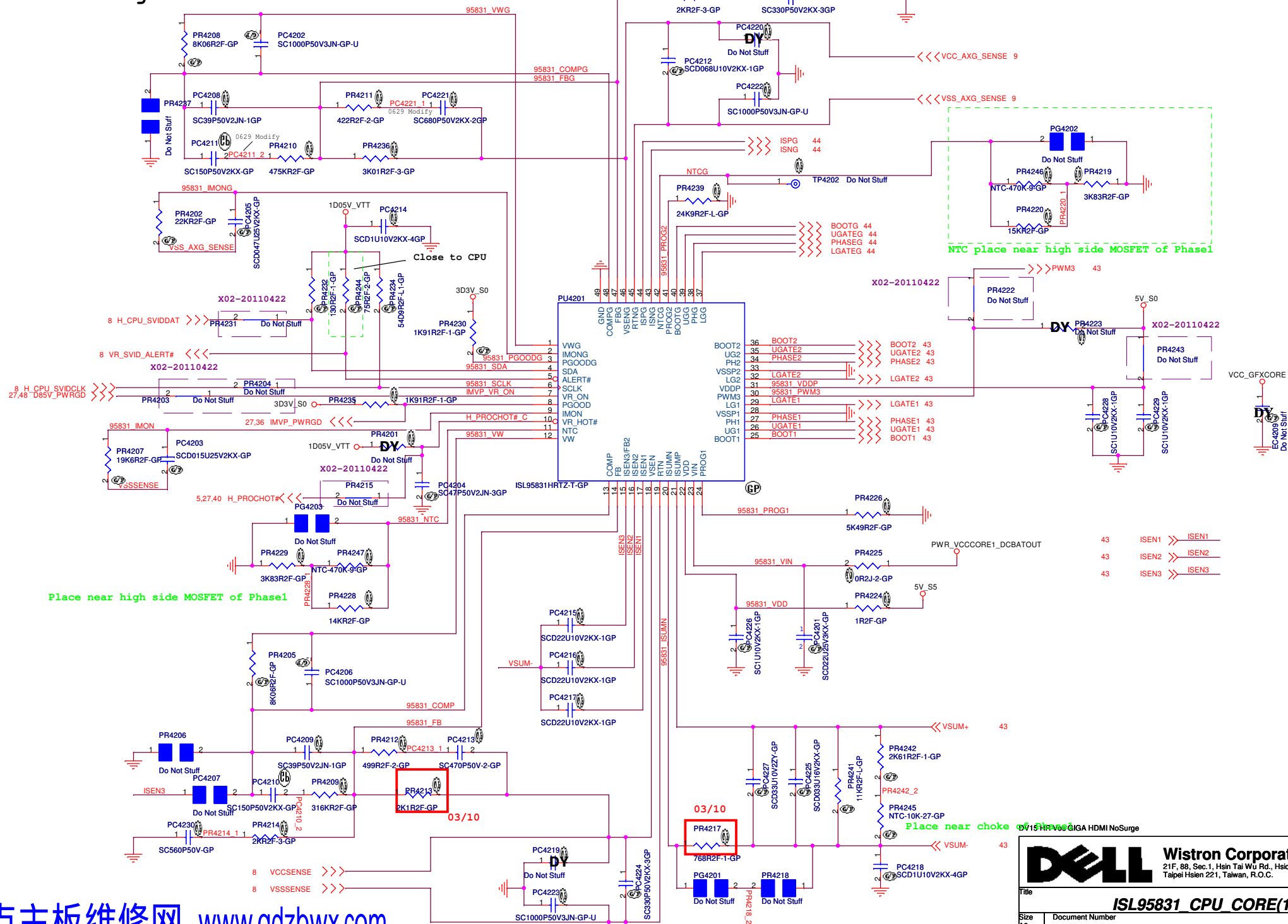


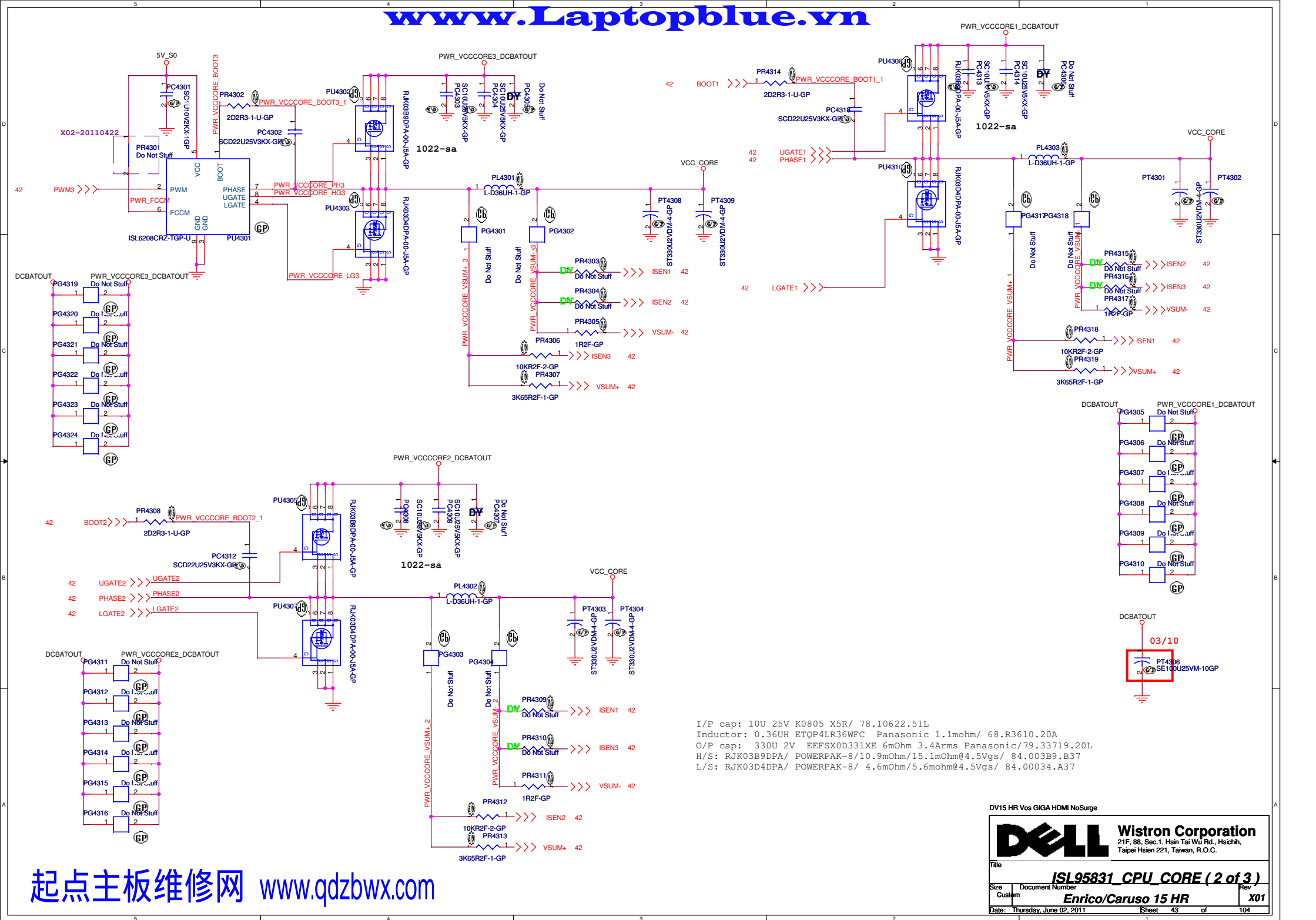
TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3 or VREG5	400kHz	500kHz

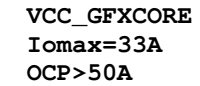
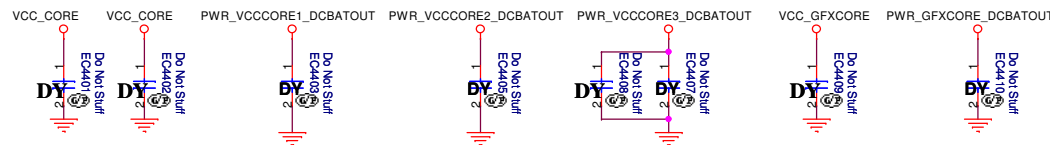
SKIPSEL	VREG3 or VREG5	VREF (2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 2.20UH PCMC104T-2R2 Cyntec 7mohm Isat =27Arms 68.2R201.20C
O/P cap: 330UE.63V M6.3*5.7 15mOhm 3.16Arms Matsuki/77.53371.04L
H/S: TPC8061-H / 21mohm/30mOhm@4.5Vgs/ 84.08061.037
L/S: TPC8065-H / 21mohm/15mOhm@4.5Vgs/ 84.08065.037

SSID = CPU.Regulator





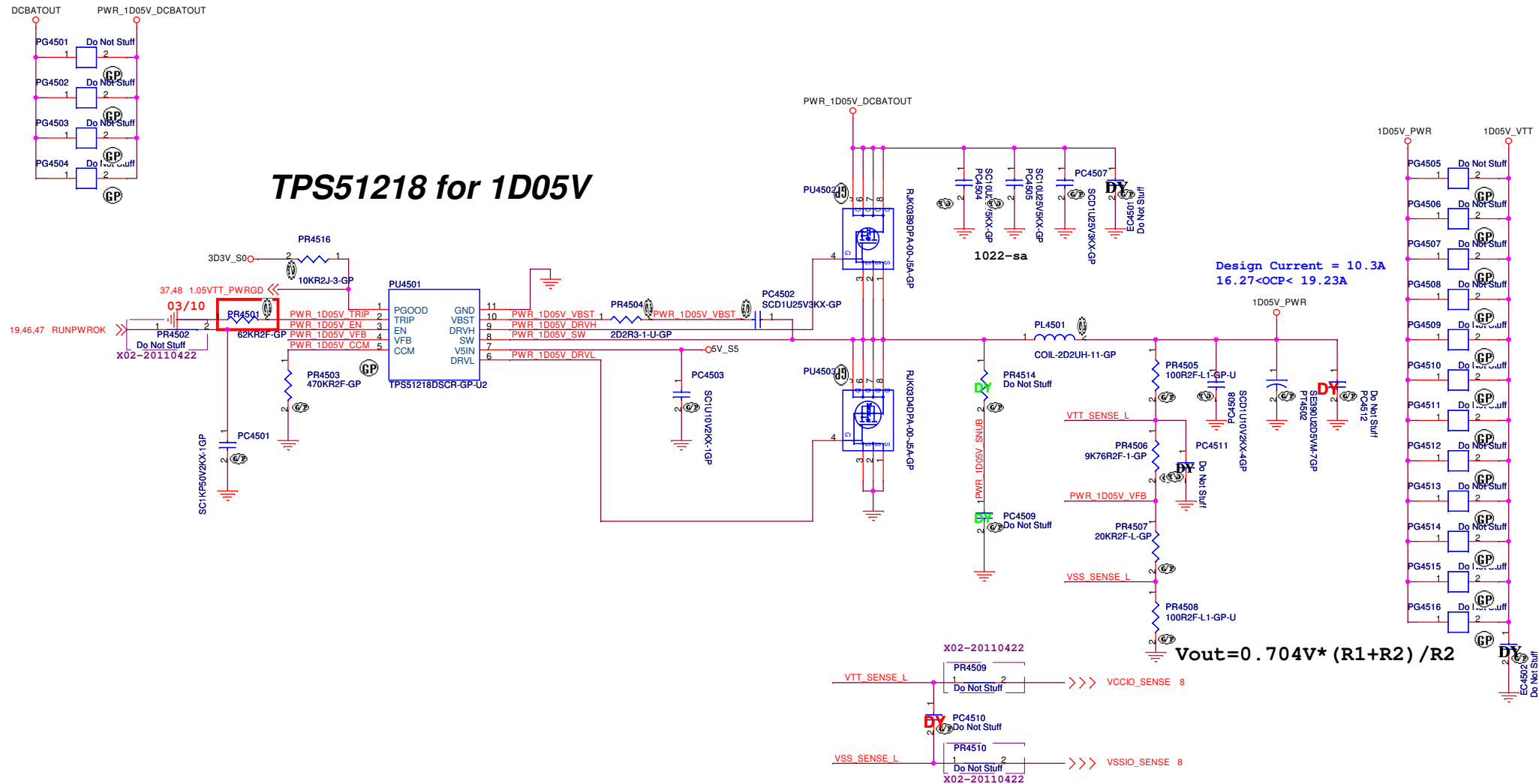
**EMI/ESD**

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Taipei Hsien 221, Taiwan, R.O.C.

ISL95831_CPU_CORE(3/3)

Enrico/Caruso 15 HR

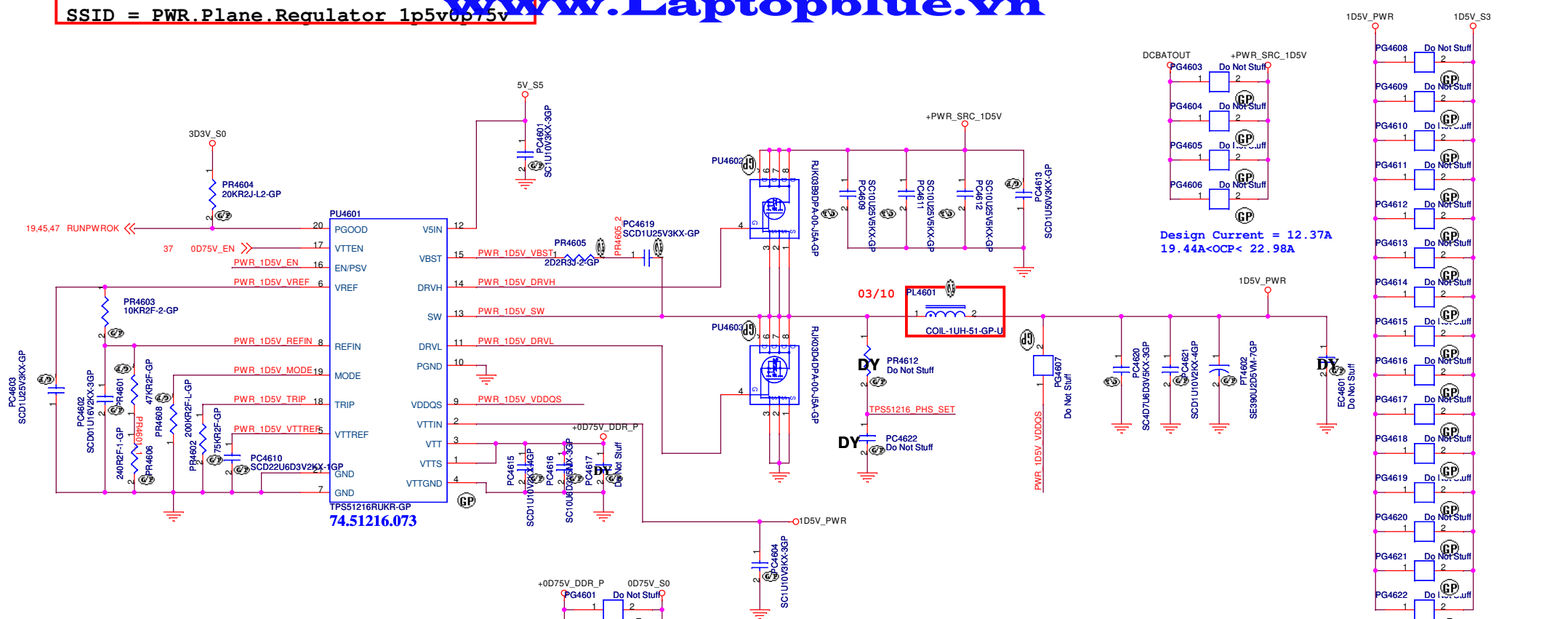
Sheet 44 of 104



I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 2.20UH PCMC104T-2R2 Cyntec 7mohm Isat =27Arms 68.2R210.20C
O/P cap: 390U 2.5V M 6.3*5.7/ 10mOhm 3.87Arms Matsuki/79.3971V.30L
H/S: RJK03B9DPA/ POWERPAK-8/10.9mOhm/15.1mOhm@4.5Vgs/ 84.003B9.B37
L/S: RJK03D4DPA/ POWERPAK-8/ 4.6mOhm/5.6mohm@4.5Vgs/ 84.00034.A37

SSID = PWR.Plane.Regulator 1p5v0p75v

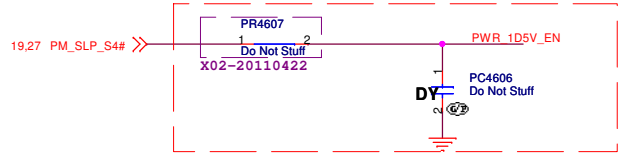
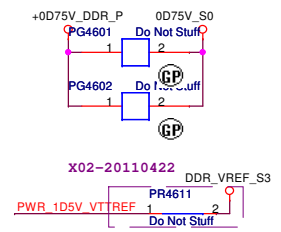
www.Laptopblue.vn



Design Current = 12.37A
19.44A < OCP < 22.98A

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE	PR4608	Frequency	Discharge Mode
	200k ohm	400kHz	Tracking Discharge
	100k ohm	300kHz	
	68k ohm	300kHz	Non-tracking Discharge
	47k ohm	400kHz	



I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 1.0UH PCB104T-1R0M Cyntec 3mohm Isat =28Arms 68.1R01C.10Q
O/P cap: 390U 2.5V M 6.3*5.7/ 10mOhm 3.87Arms Matsuki/79.3971V.30L
H/S: RJK03B9DPA/ POWERPAK-8/10.9mOhm/15.1mOhm@4.5Vgs/ 84.003B9.B37
L/S: RJK03D4DPA/ POWERPAK-8/ 4.6mOhm/5.6mohm@4.5Vgs/ 84.00034.A37

起点主板维修网 www.qdzbwx.com

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

File

TPS51116 +1.5V SUS

Size A3 Document Number

Enrico/Caruso 15 HR

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Rev

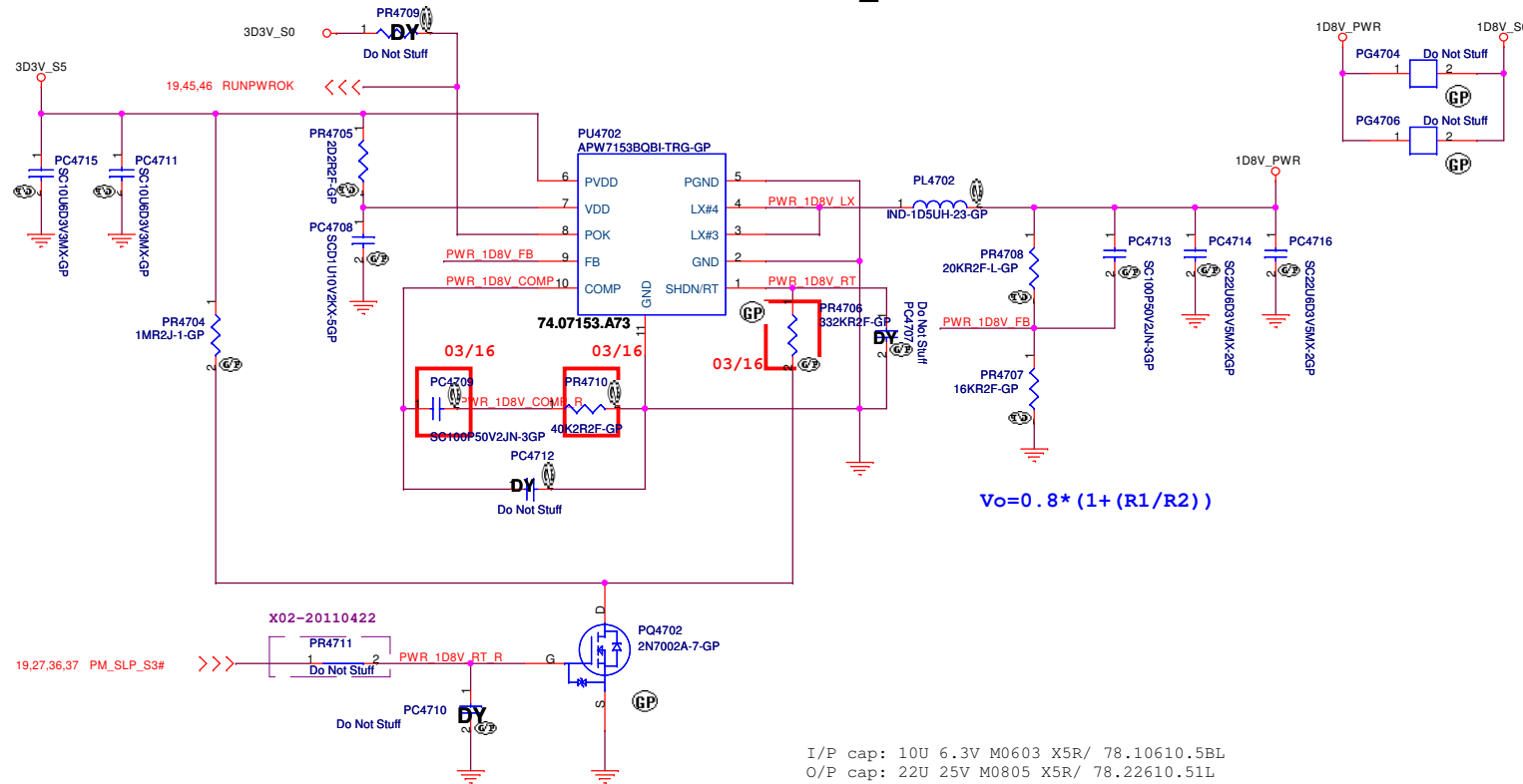
X01

SSID = PWR.Plane.Regulator_1D8V_S0

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+1.8V_RUN
Design current = 0.87A

APW7153B for 1D8V_S0



$$V_o = 0.8 * (1 + (R1/R2))$$

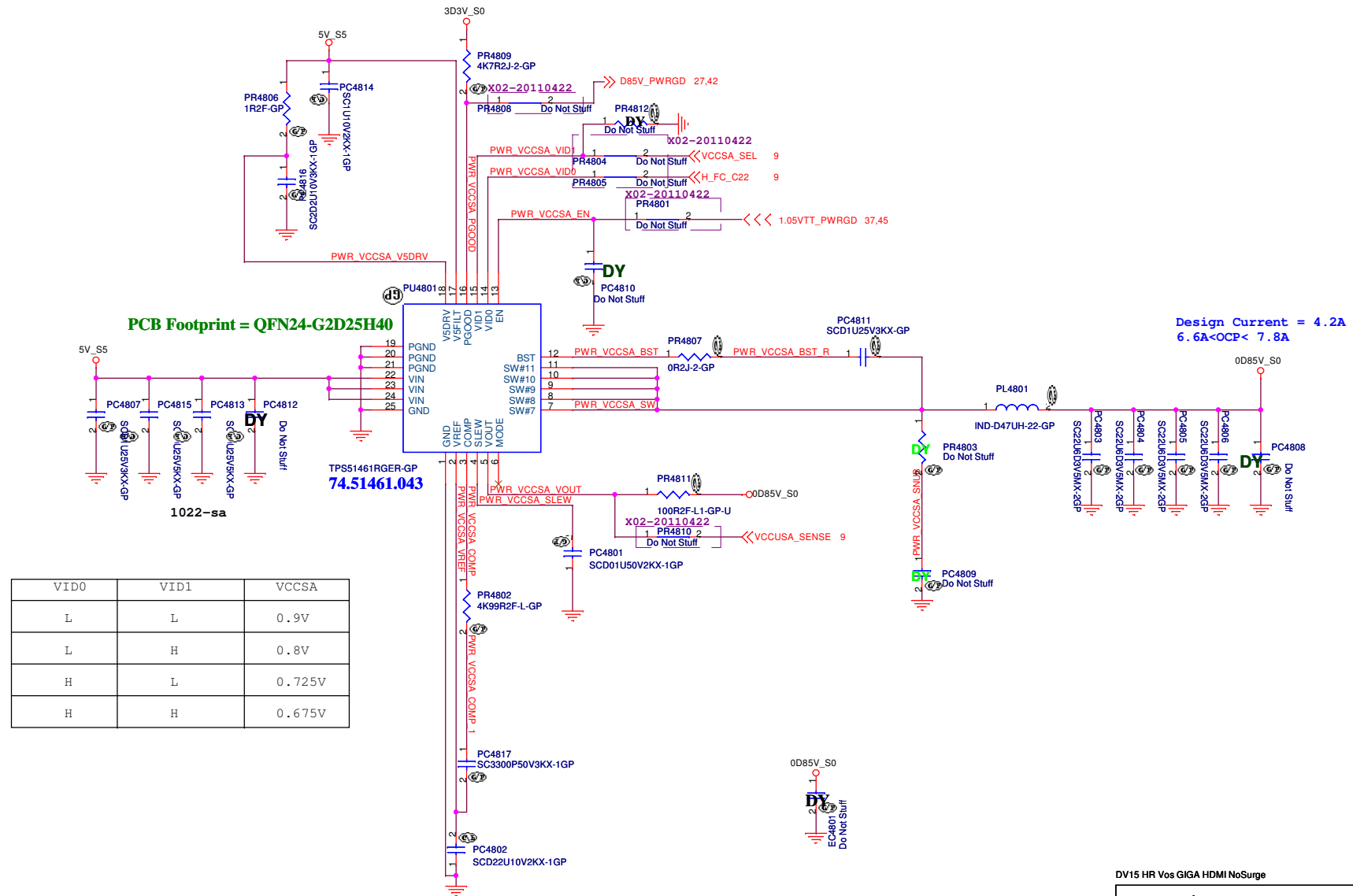
I/P cap: 10U 6.3V M0603 X5R/ 78.10610.5BL
O/P cap: 22U 25V M0805 X5R/ 78.22610.51L
Inductor: 1.5U PCMC063T Cyntec 14mohm/15mohm Isat =18Arms 68.1R510.10K

起点主板维修网 www.qdzbwx.com

DV15 HR Vos GIGA HDMI NoSurge

DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title TPS51311 for 1D8V_S0			
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TPS51461 for VCCSA

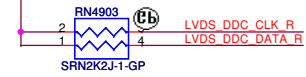


起点主板维修网 www.qdzbwx.com

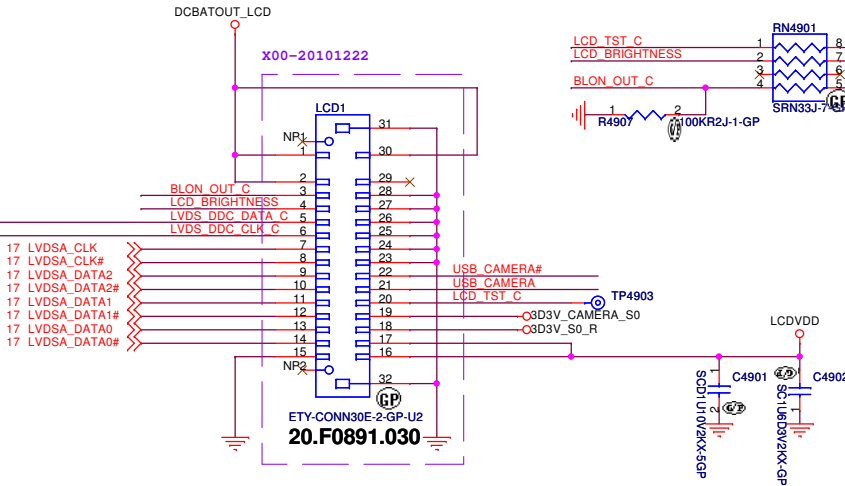
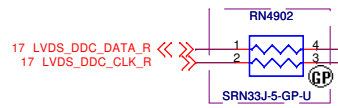
LVDS CONNECTOR

X01-20110307

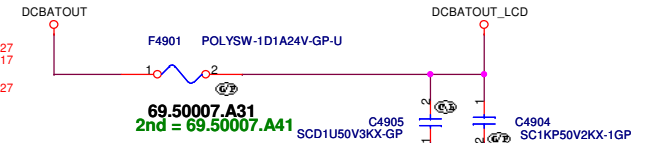
3D3V_S0_R



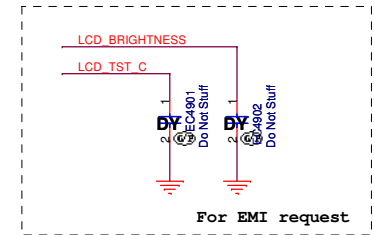
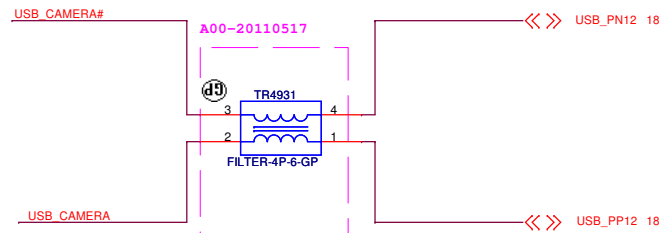
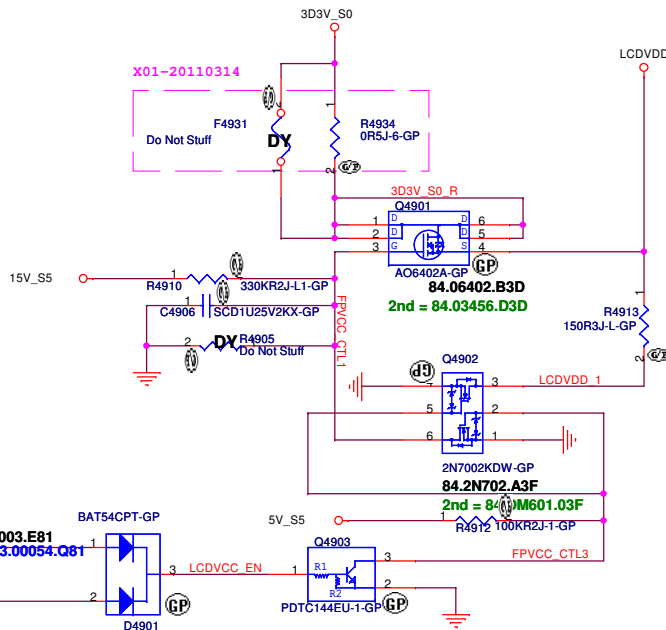
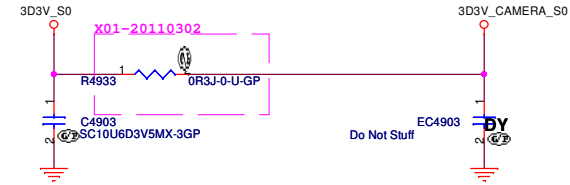
X02-20110415



INVERTER POWER



Camera Power



起点主板维修网 www.qdzbwx.com

DV15 HR Vos GIGA HDMI NoSurge

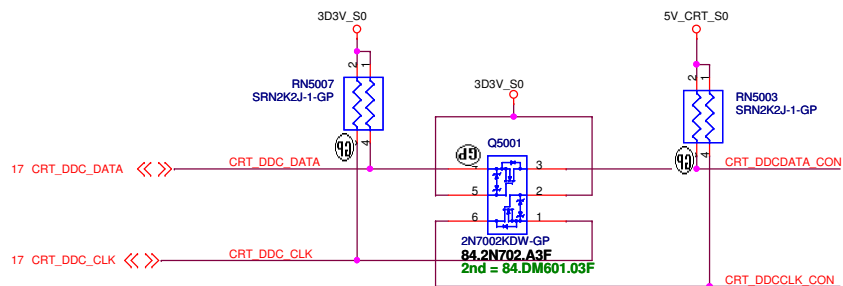
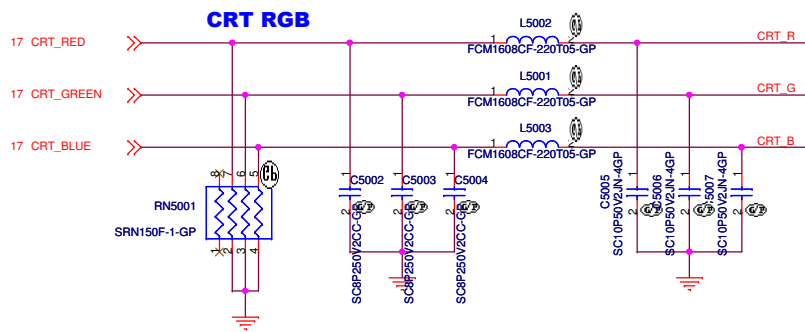
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
LCD Connector			
Size A3	Document Number	Enrico/Caruso 15 HR	Rev X01
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SSID = VIDEO

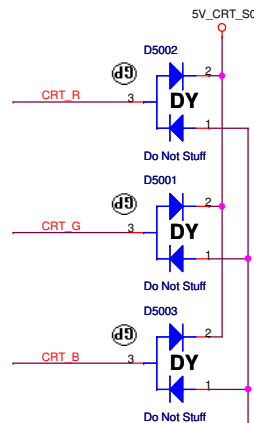
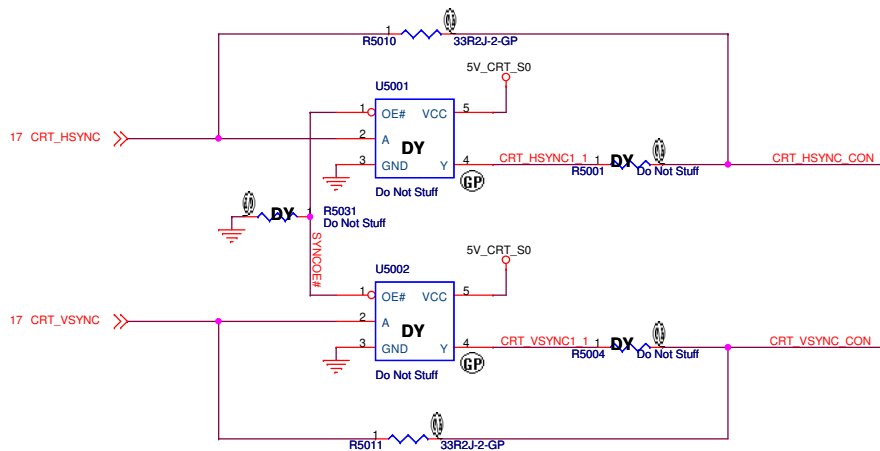
Layout Note:

*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.

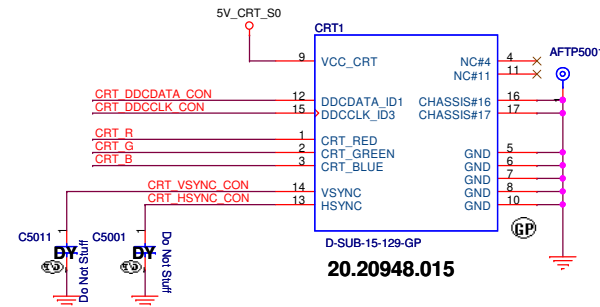
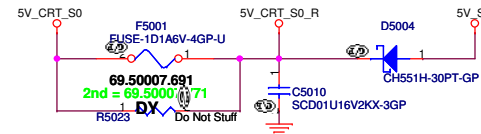
* RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.



Hsync & Vsync



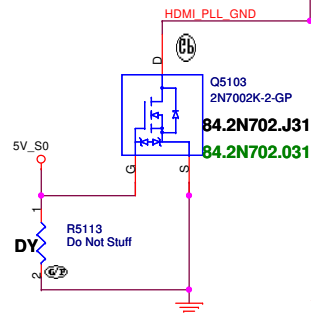
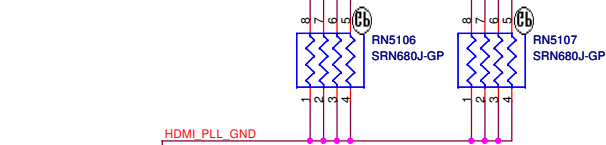
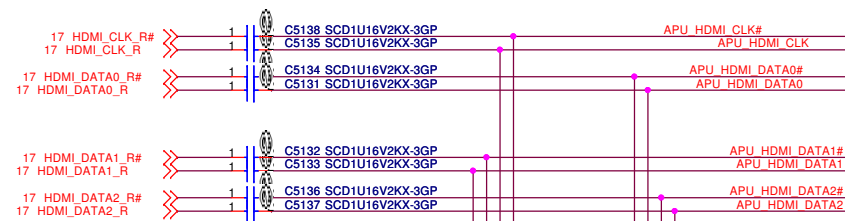
AFTP5002 1 5V CRT_S0
AFTP5003 1 CRT_DDCDATA_CON
AFTP5004 1 CRT_DDCCLK_CON
AFTP5005 1 CRT_R
AFTP5006 1 CRT_G
AFTP5007 1 CRT_B
AFTP5008 1 CRT_HSYNC_CON
AFTP5009 1 CRT_VSYNC_CON



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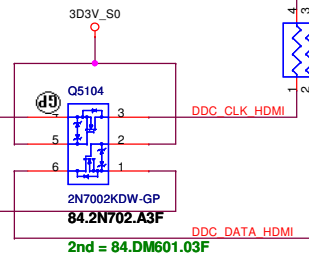
DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title CRT Connector			
Size Custom	Document Number	Rev	
Enrico/Caruso 15 HR		X01	
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SSID = VIDEO

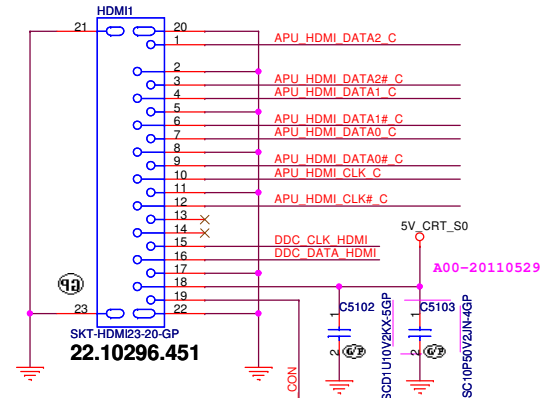


17 PCH_HDMI_CLK >>>

17 PCH_HDMI_DATA <<<



HDMI CONN

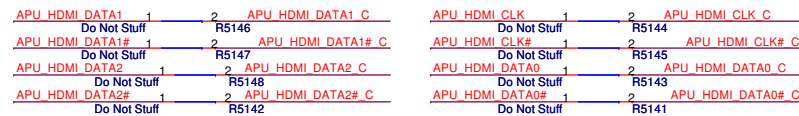
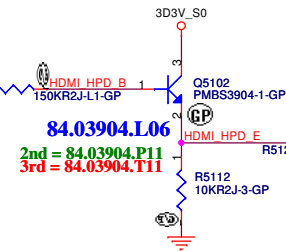


5V_CRT_S0

3D3V_S0

Do Not Stuff

Do Not Stuff



A00-20110530

起点主板维修网 www.qdzbwx.com

DV15 HR Vos GIGA HDMI NoSurge



Title HDMI Level Shifter/Connector		
Size A3	Document Number Enrico/Caruso 15 HR	Rev X01
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DV15 HR Vos GIGA HDMI NoSurge



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Title

Reserved

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(Blanking)

DV15 HR Vos GIGA HDMI NoSurge



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Title

LVDS Switch

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DV15 HR Vos GIGA HDMI NoSurge



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Title

Reserved

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Document Number

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SSID = User.Interface

(Blanking)

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Title

ITP/Fan Connector

Size
A3

Document Number
Enrico/Caruso 15 HR

Date: Thursday, June 02, 2011

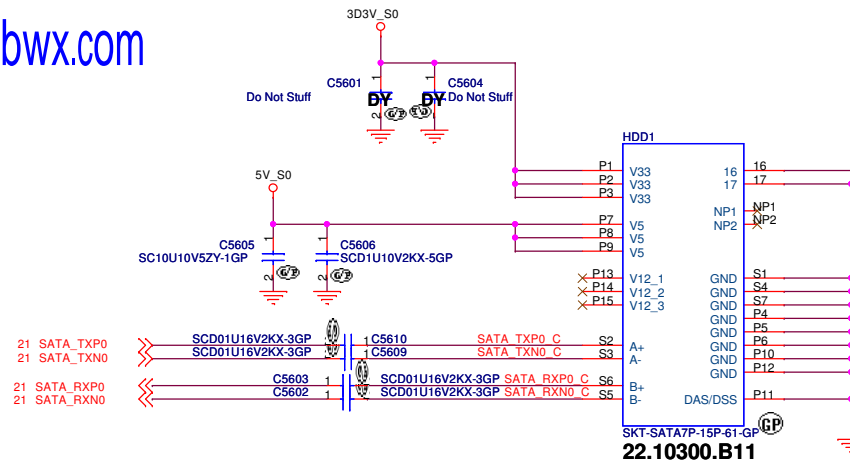
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X01

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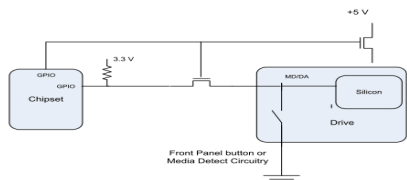
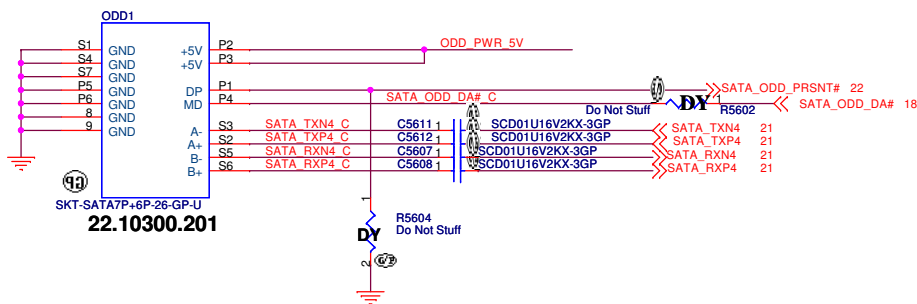
SSID = SATA

SATA HDD Connector

起点主板维修网 www.qdzbwx.com

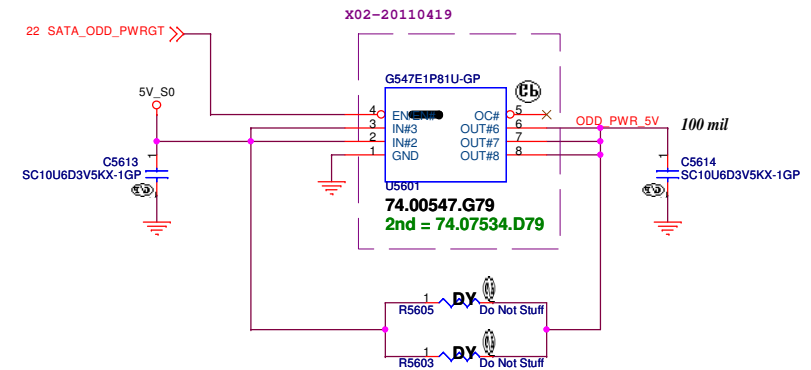
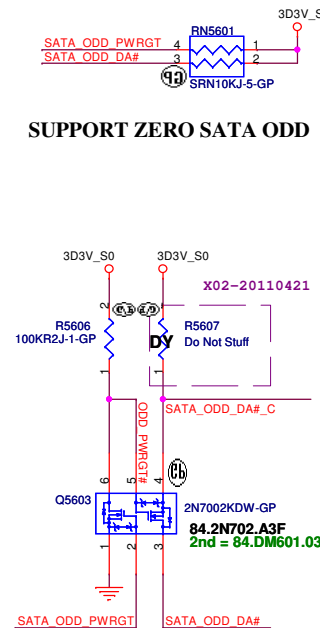


ODD Connector



When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON

SUPPORT ZERO SATA ODD



DV15 HR Vos GIGA HDMI NoSurge




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Title			
HDD/ODD			
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SSID = ESATA

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Taipei Hsien 221, Taiwan, R.O.C.

Title

ESATA

Size

A3

Document Number

Enrico/Caruso 15 HR

Rev

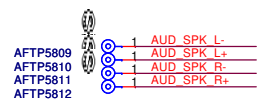
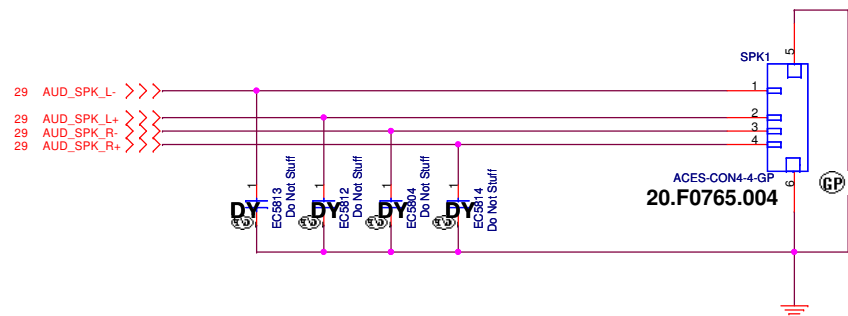
X01

Date: Thursday, June 02, 2011

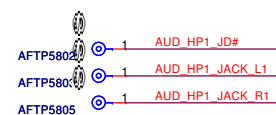
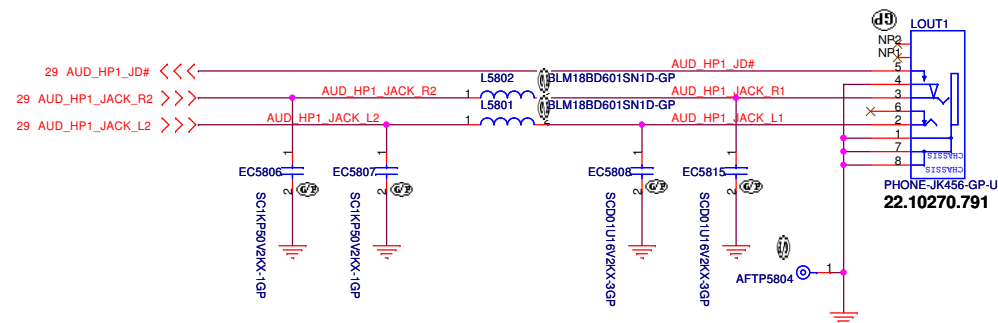
Sheet 57 of 104

SSID = AUDIO

Speaker Connector

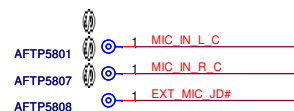
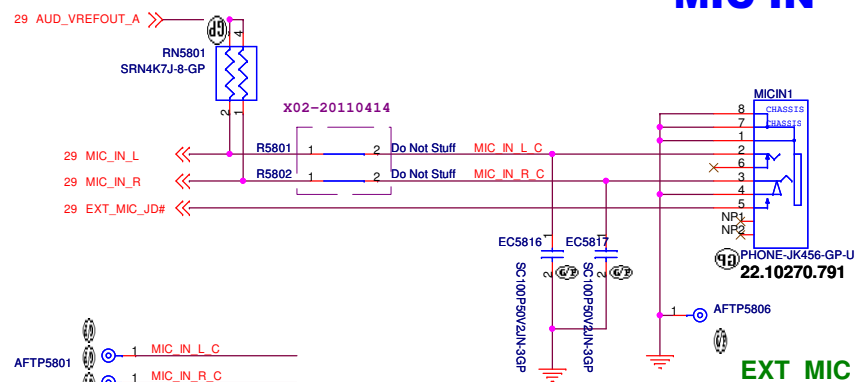


LINE1 OUT



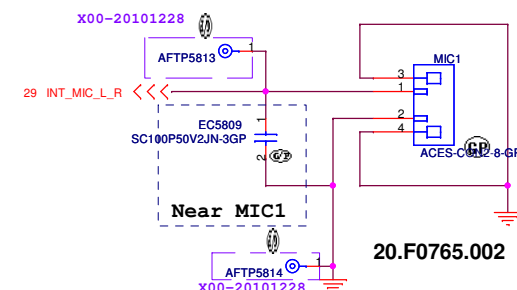
AUD_HP1_JD#
Normal Open

MIC IN



EXT_MIC_JD#
Normal Open

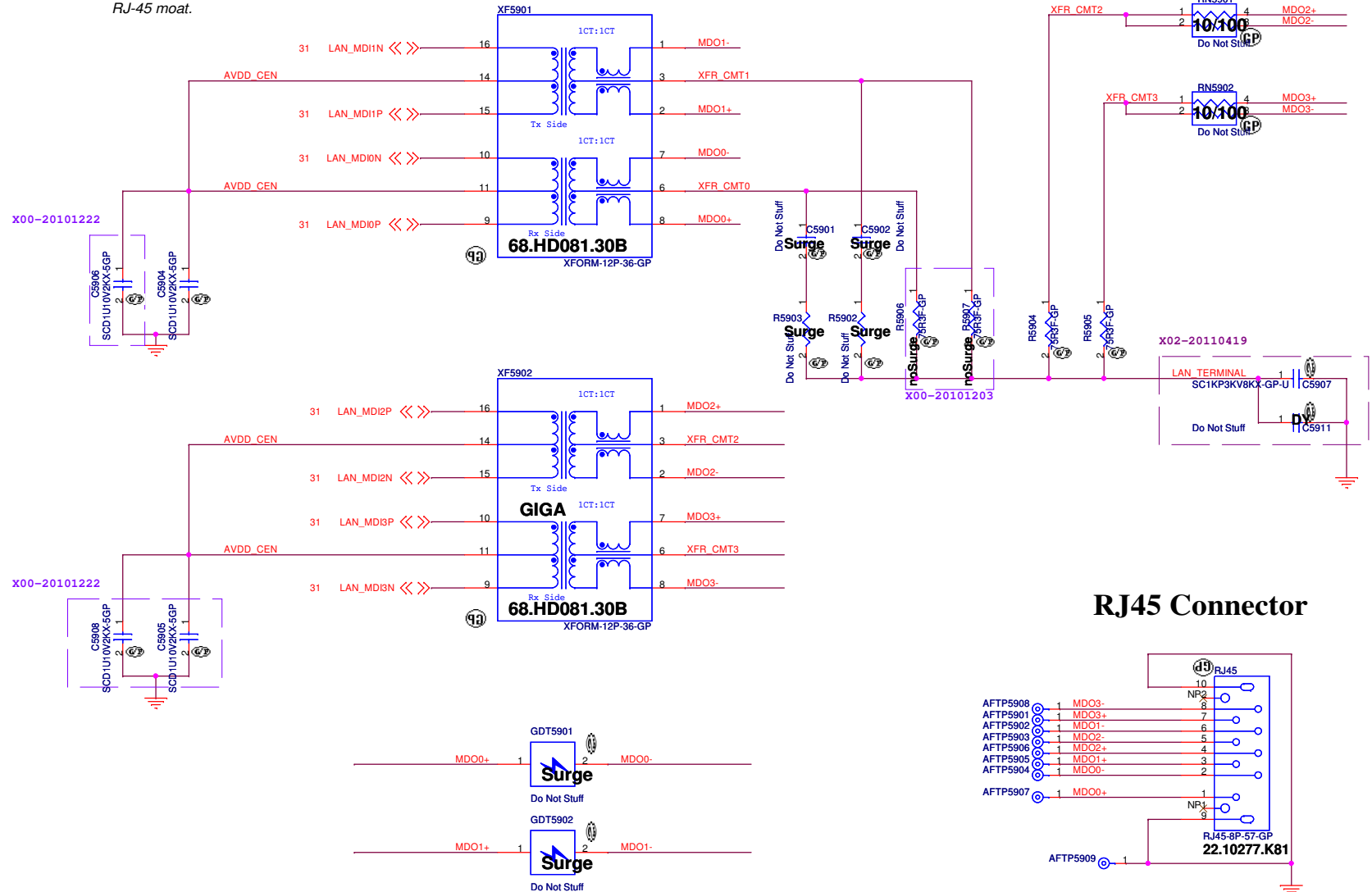
Internal Microphone



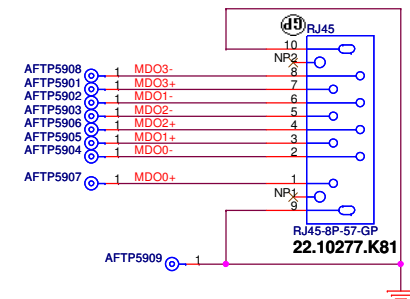
DV15 HR Vos GIGA HDMI NoSurge

- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

10/100M Lan Transformer



RJ45 Connector

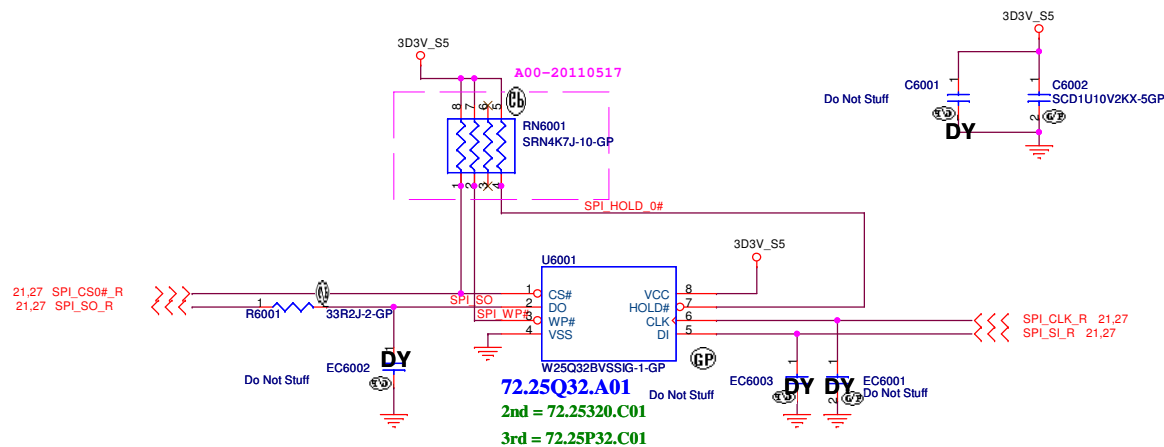


DV15 HR Vos GIGA HDMI NoSurge

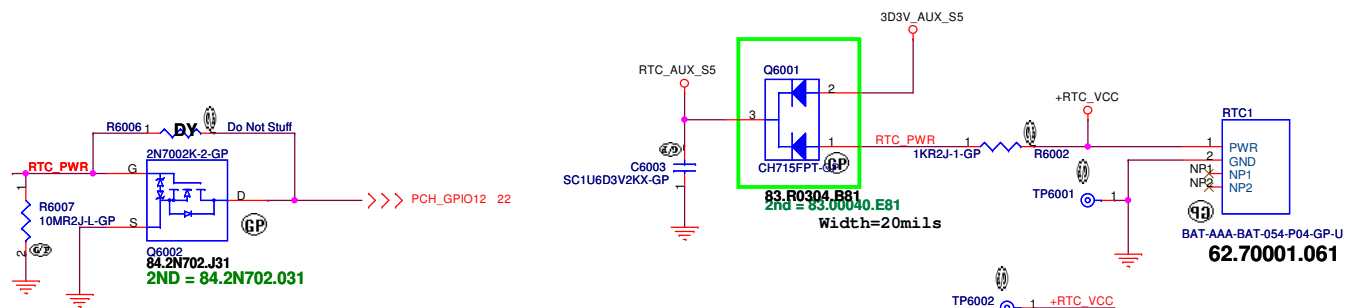
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title: Reserved	
Size A3	Document Number	Rev X01	
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```
SSID = Flash.ROM
```

SPI FLASH ROM (4M byte) for PCH



SSID = RBATT



起点主板维修网 www.gdzbwx.com

DV15 HR Vos GIGA HDMI NoSurge

DELL

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Flash/RTC

Size
A3

Document Number	
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Enrico/Caruso 15 HR

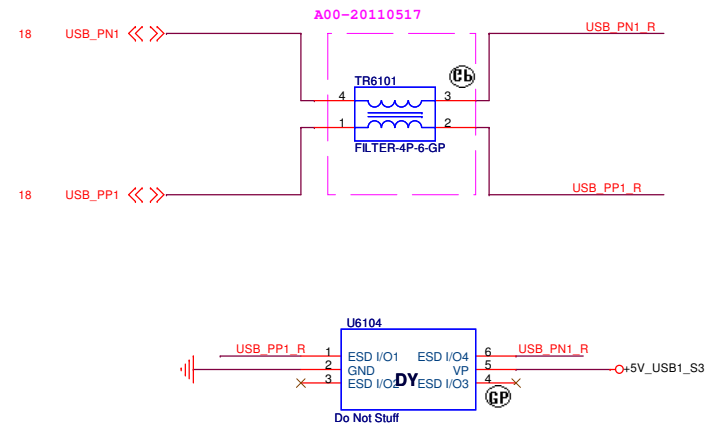
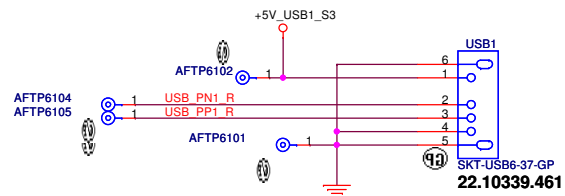
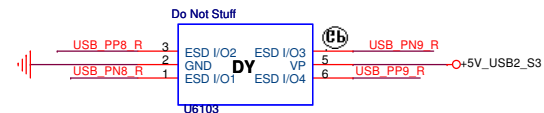
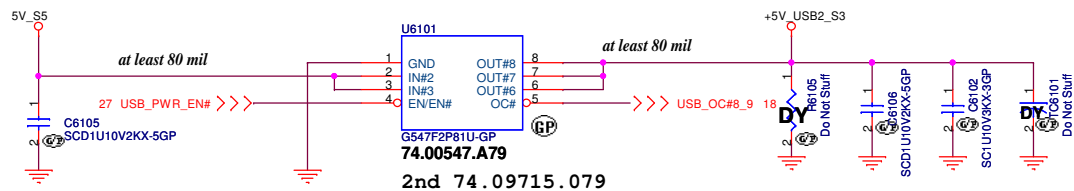
Rev

X01

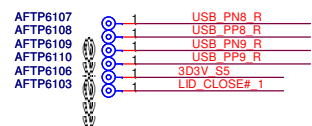
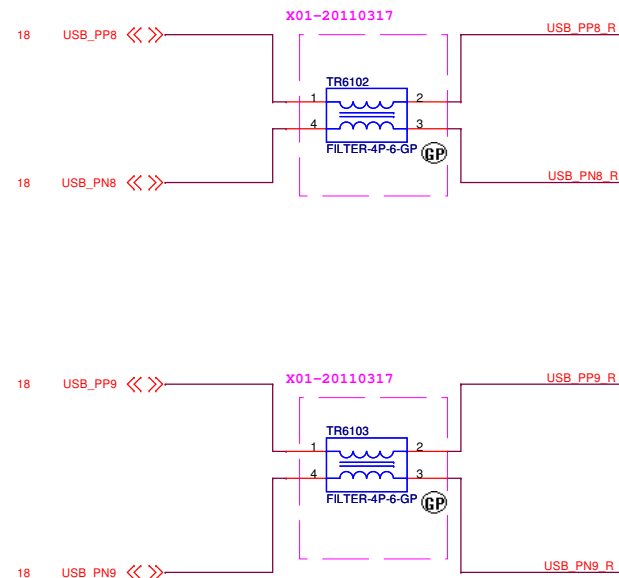
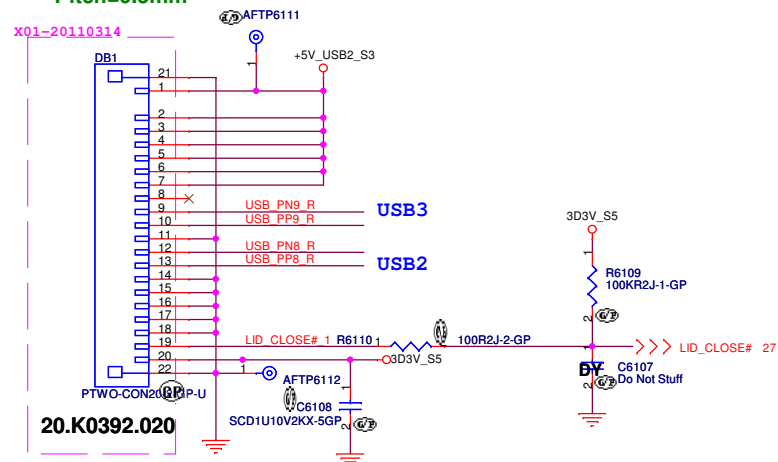
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Left USB Power x1

[illegible]**Right USB Power x2**

Pitch=0.5mm



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DV15 HR Vos GIGA HDMI NoSurge



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

USB Power SW

Size

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DV15 HR Vos GIGA HDMI NoSurge



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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

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SSID = User.Interface

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起点主板维修网 www.qdzbwx.com

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Title			
Bluetooth			
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
RESERVED			
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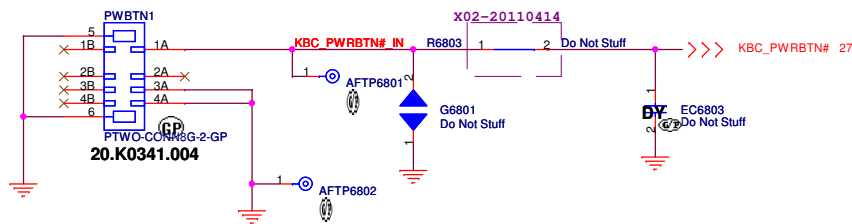


Wistron Corporation
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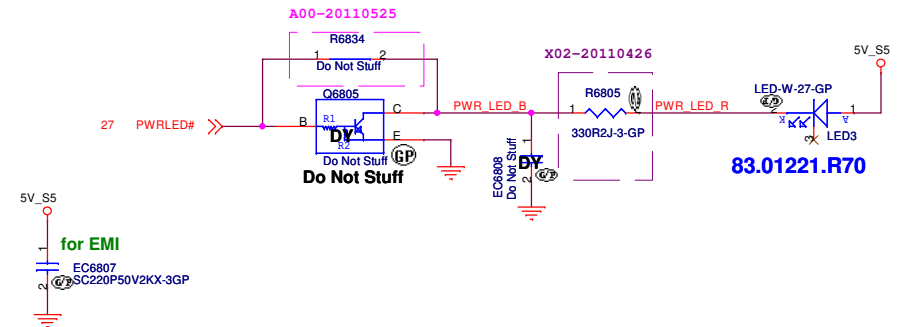
Title			Reserved		
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SSID = User.Interface

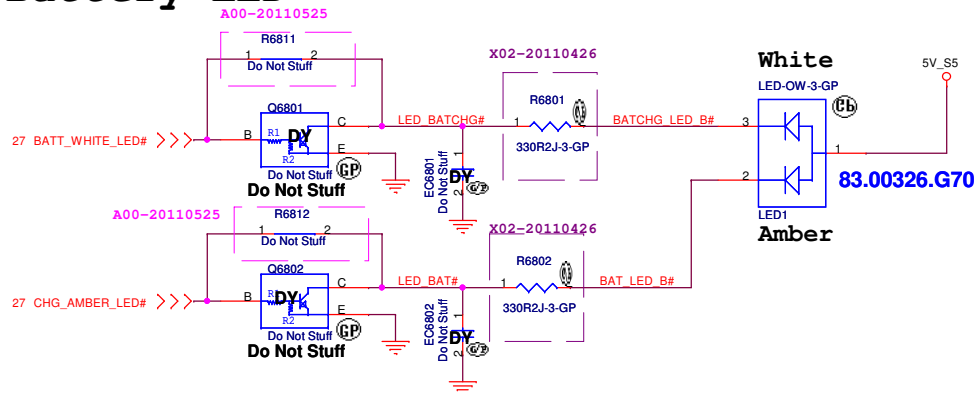
Power BTN Connector



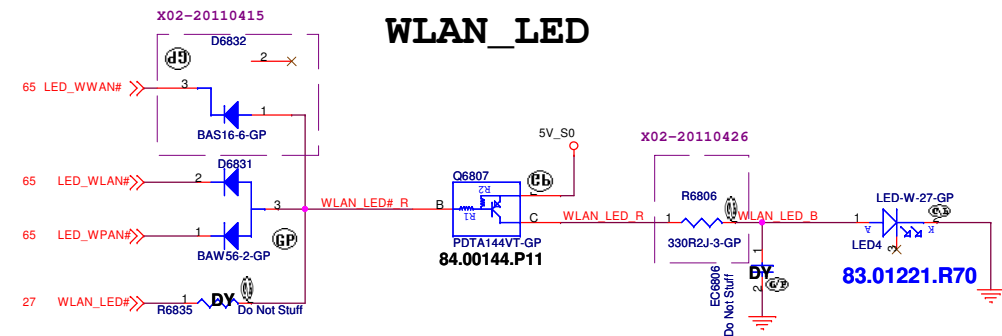
Power LED



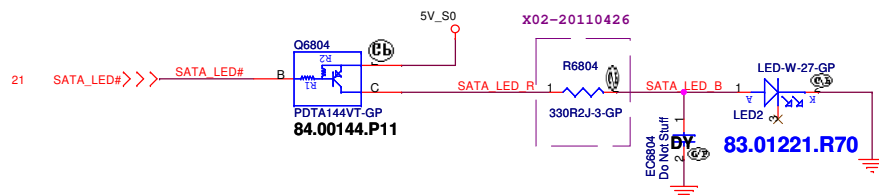
Battery LED



WLAN_LED



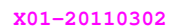
HDD LED



LED Location from left to right
(MB, Top View)

LED3 PWR LED2 HDD LED1 Battery LED4 WiFi

A

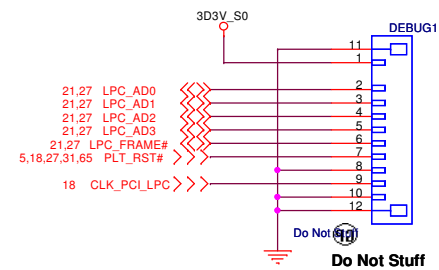


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DV15 HR Vos GIGA HDMI NoSurge

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Hall Sensor			
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Title			
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Title

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Rev

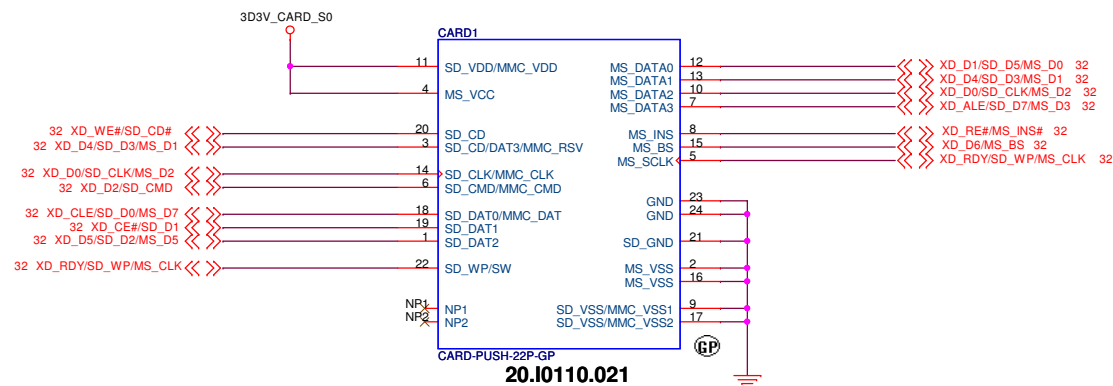
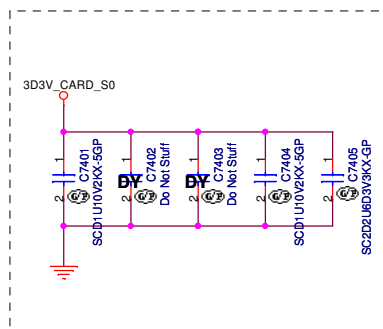
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Date: Thursday, June 02, 2011

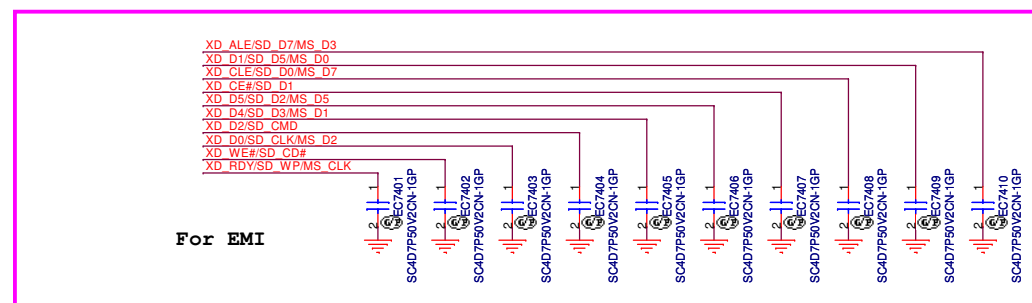
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SSID = SDIO

SD/MMC/MS Card Reader




X01-20110315




SSID = ExpressCard

DV15 HR Vos GIGA HDMI NoSurge

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Title					
Express Card					
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Title			
Reserved			
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Title

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Title

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SSID = User.Interface

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DV15 HR Vos GIGA HDMI NoSurge

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
Free Fall Sensor					
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Title

IO Board Connector

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			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
GPU PCIE/STRAPPING(1/5)					
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DV15 HR Vos GIGA HDMI NoSurge



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Title

GPU-VRAM1,2 (1/4)

Size
Custom

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Title

GPU-VRAM3,4 (2/4)

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Custom

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Title			GPU-VRAM5,6 (3/4)	
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
GPU-VRAM7,8 (4/4)			
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Title RT8208B +VGA CORE			
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Title LVDS Switch			
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title CRT Switch			
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SSID = SDIO

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Title

TOUCH PANEL

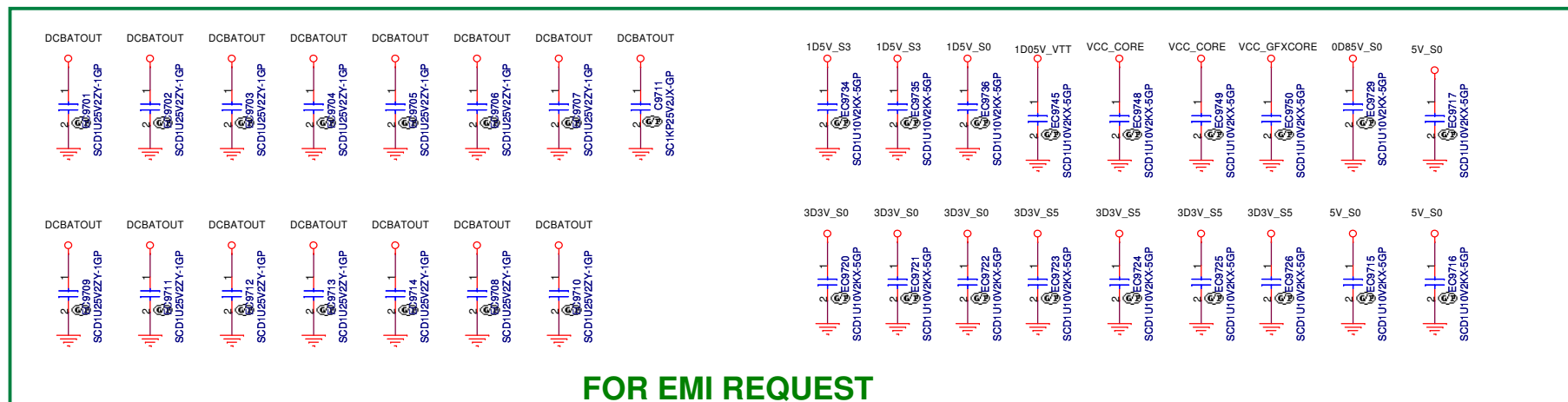
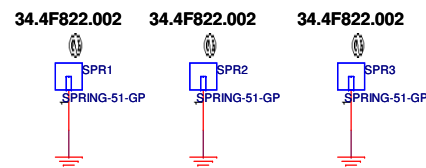
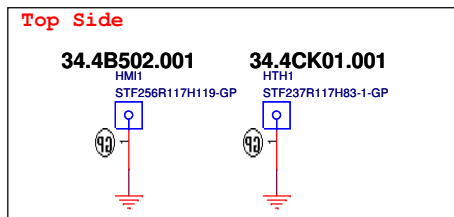
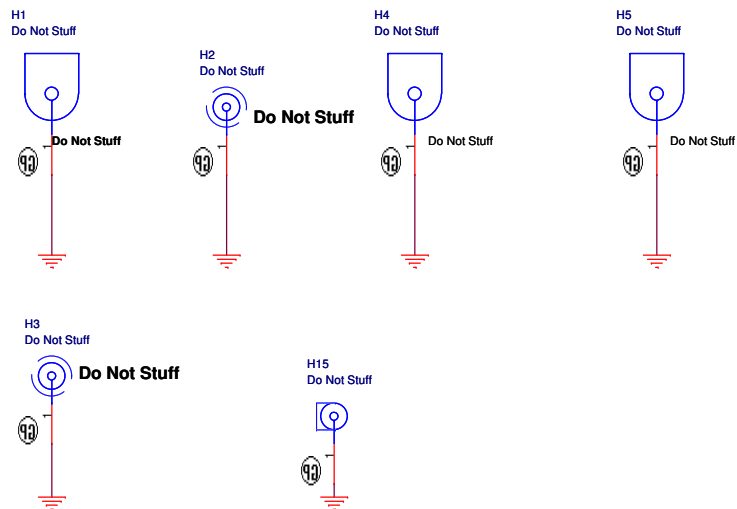
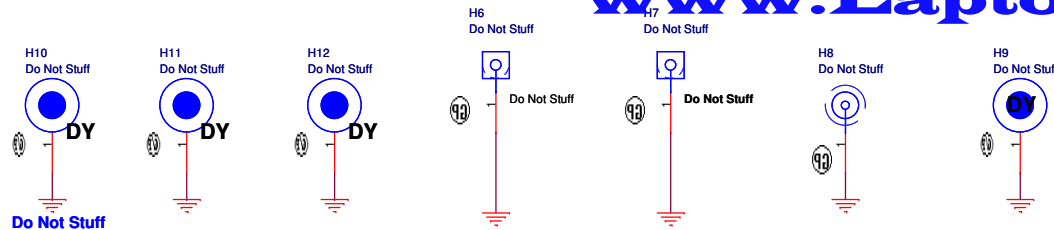
Size
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Title
UNUSED PARTS/EMI Capacitors

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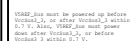
Rev X01

Sequence **www.Laptopblue.vn**

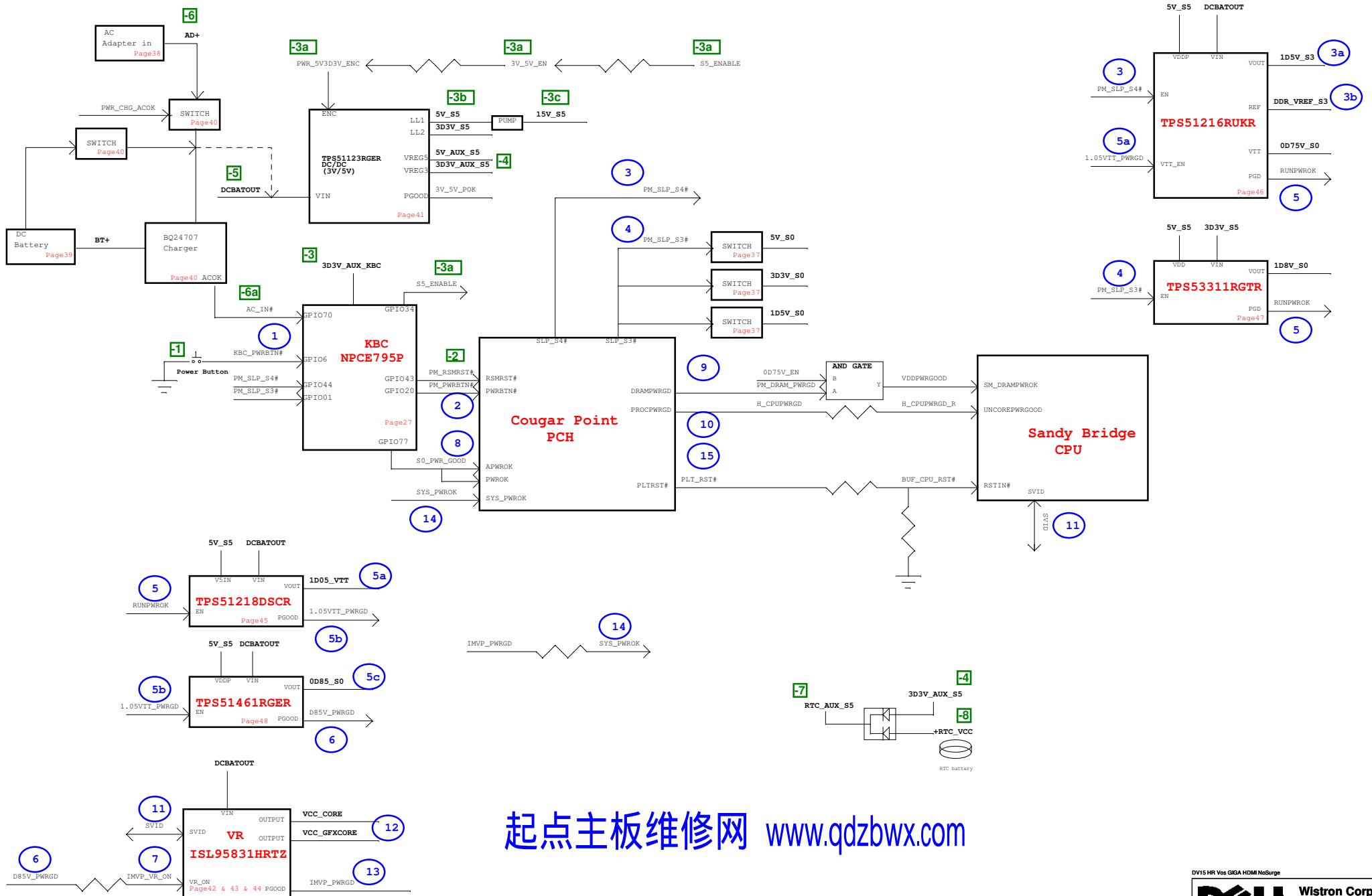
red word: KBC GPIO



red word: KBC GPIO

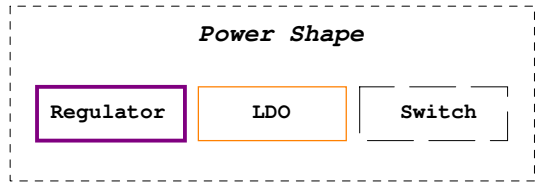
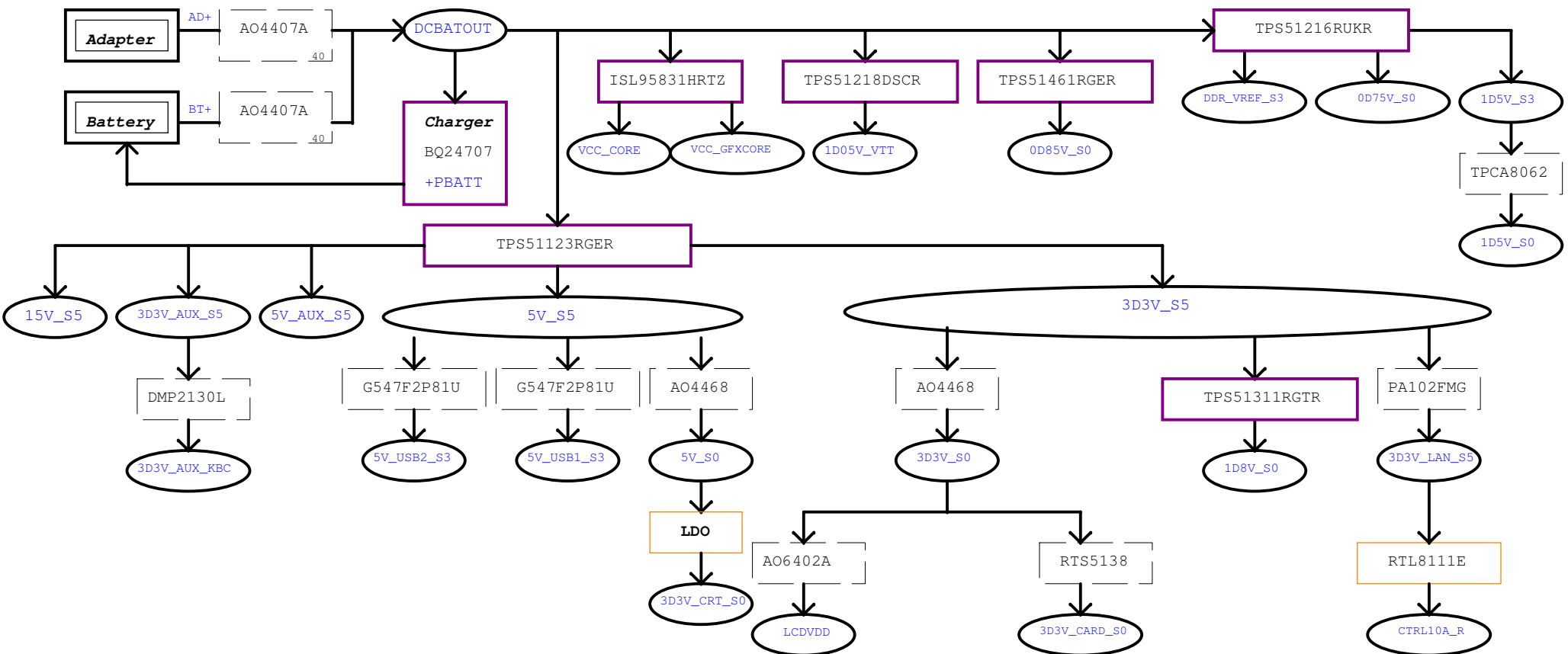


Wistron HURON RIVER POWER UP SEQUENCE DIAGRAM



起点主板维修网 www.qdzbwx.com

Power Up Sequence: -8 ~ 15



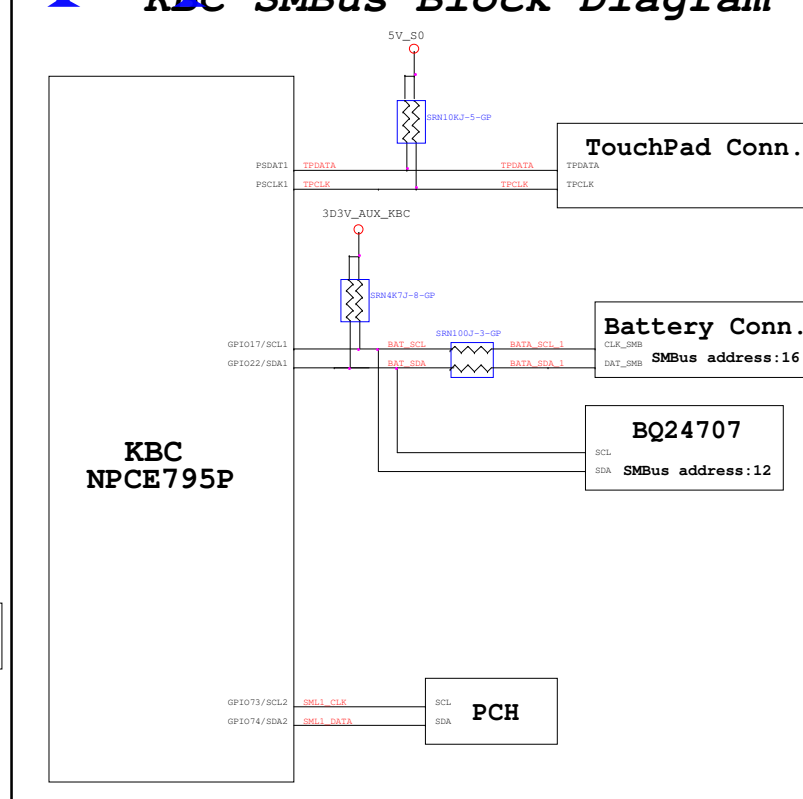
起点主板维修网 www.qdzbw.com

DV15 HR Vos GIGA HDMI NoSurge

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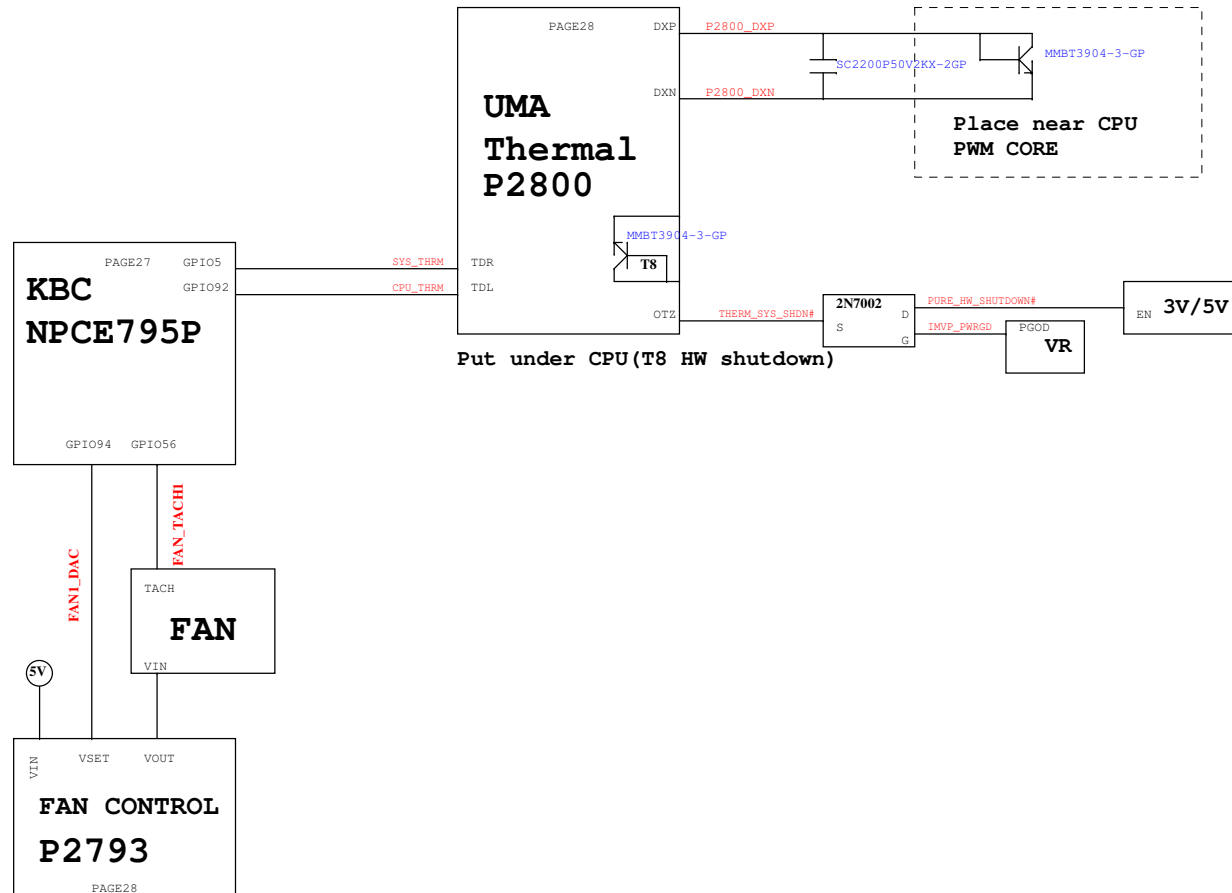
Power Block Diagram		
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KLC SMBus Block Diagram



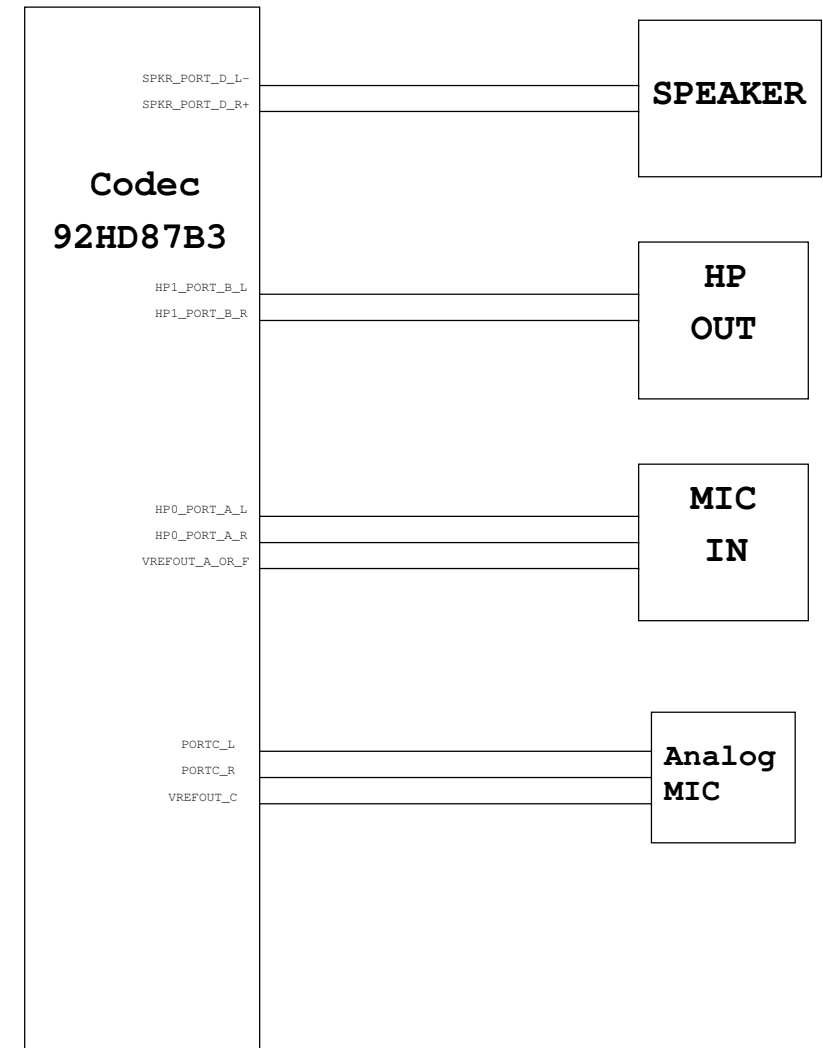
起点主板维修网 www.qdzbwx.com

Thermal Block Diagram



起点主板维修网 www.qdzbwx.com

Audio Block Diagram



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