

Compal confidential

Schematics Document

Mobile Merom uFCPGA with Satna Rosa Platform

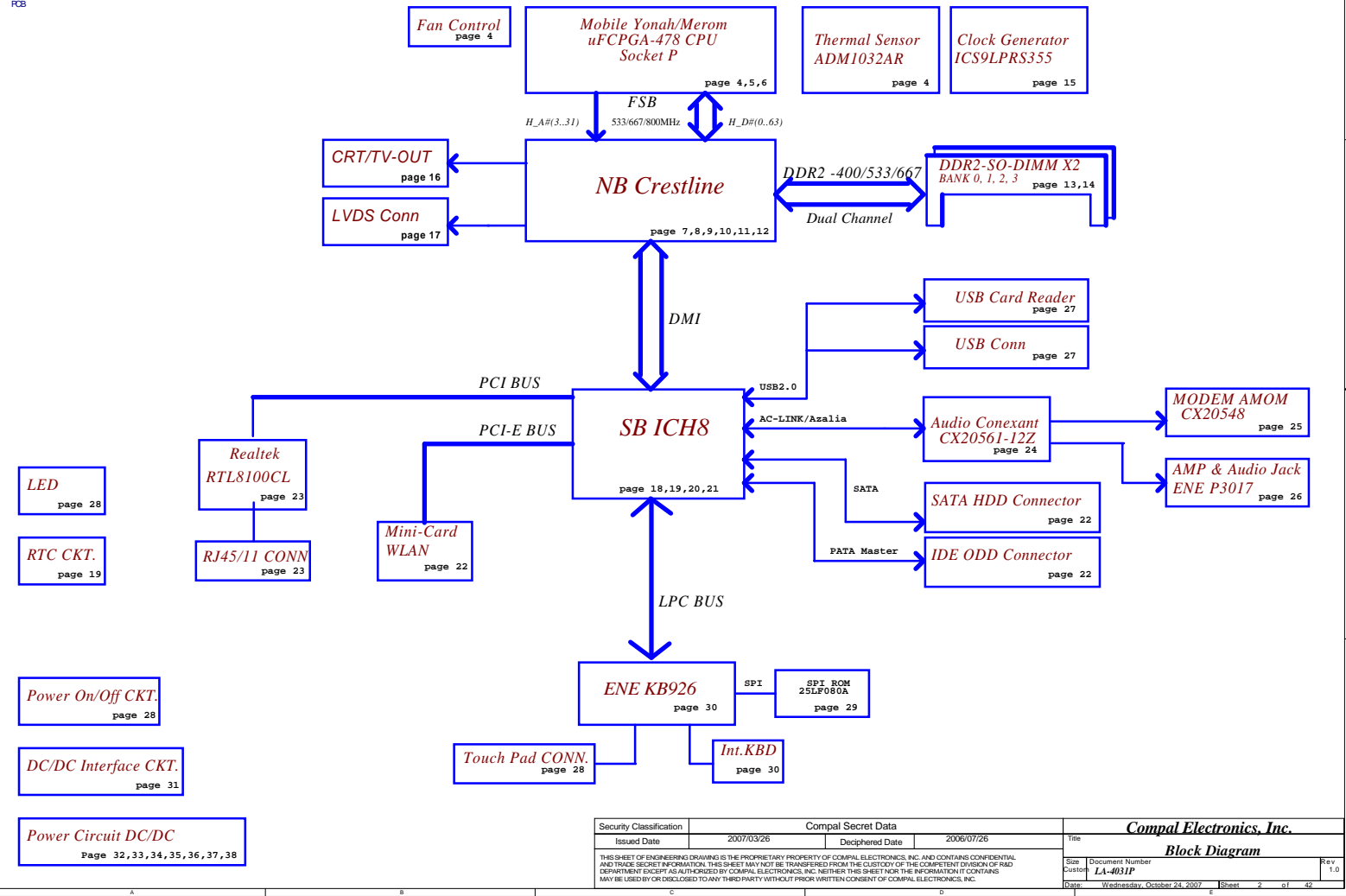
2007-07-30

REV:0.2

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Issued Date	2007/03/26	Deciphered Date	2006/07/26	
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				Document Number
				Customer
				LA-4031P
				Rev
				1.0
				Date
				Wednesday, October 24, 2007
				Sheet
				1 of 42



www.Laptopblue.vn
Spartan 1.1 (Merom +Crestline+ICH8)



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				Customer	LA-4031P
				Date	Wednesday, October 24, 2007
				Sheet	2 of 42
				Rev	1.0

Voltage Rails

power plane State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +1.25VS +0.9V +VCCP +CPU_CORE
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

 : means Digital Ground : means Analog Ground

@ : means just reserve , no build

DEBUG@ : means just reserve for debug.

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
LAN	AD17	0	A

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

SMBUS Control Table

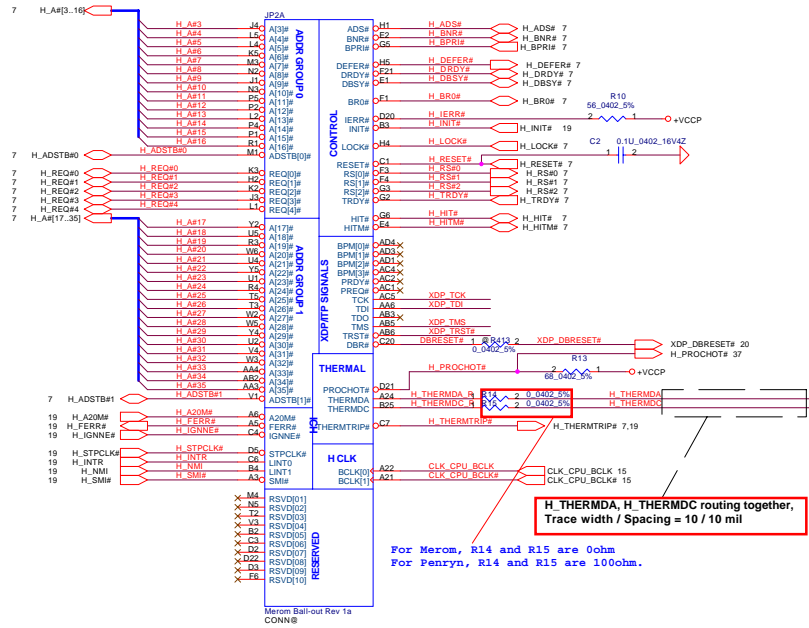
	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU) ADM1032	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB925	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB925	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH8	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Crestline	X	X	X	X	X	X	X	V

BOM: 43152432L03(965GM) & 43152432L04(960GML) with card reader

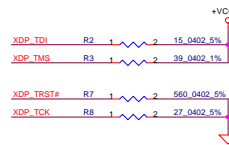
BOM: 43152432L01(965GM) & 43152432L02(960GML) without card reader

Jump-Short: PJP?

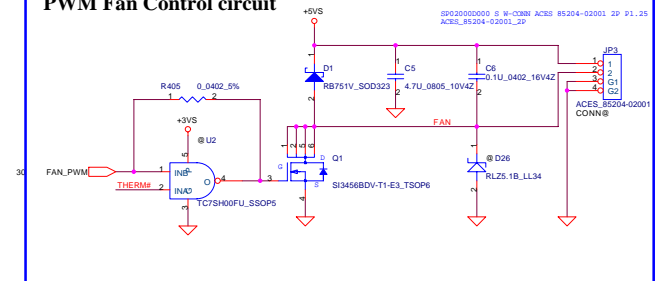
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				Size	Document Number	Rev
					LA-4031P	1.0
				Date	Wednesday, October 24, 2007	Sheet 3 of 42



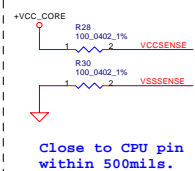
For Merom, R14 and R15 are 0ohm
For Penryn, R14 and R15 are 100ohm.



PWM Fan Control circuit

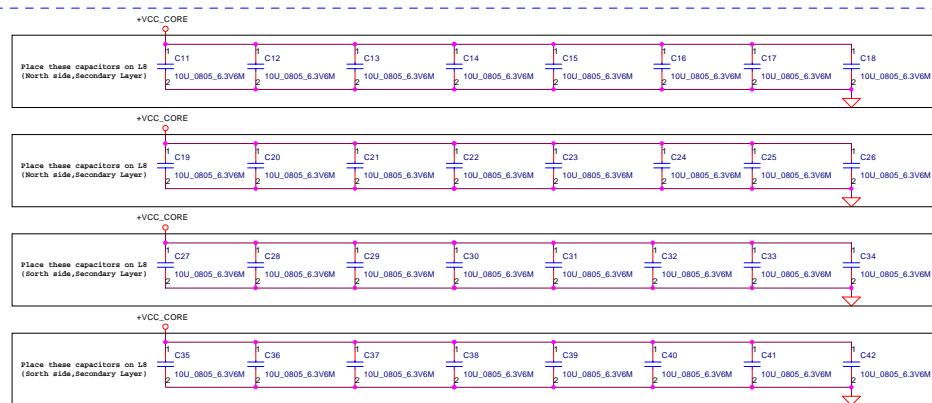


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				Customer	LA-4031P
				Date	Wednesday, October 24, 2007
				Sheet	4 of 42



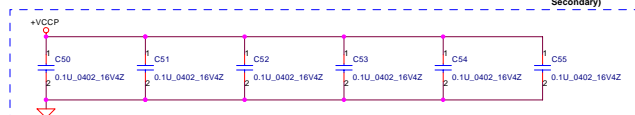
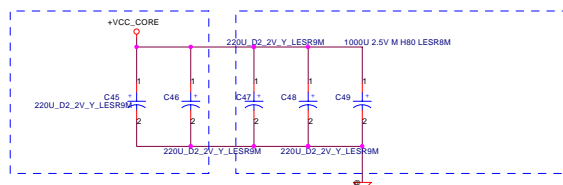
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			Created: 09/26/97	

JP20		
A4	VSS001	VSS082
A5	VSS002	VSS083
A6	VSS003	VSS084
A7	VSS004	VSS085
A8	VSS005	VSS086
A9	VSS006	VSS087
A10	VSS007	VSS088
A11	VSS008	VSS089
A12	VSS009	VSS090
A13	VSS010	VSS091
A14	VSS011	VSS092
A15	VSS012	VSS093
A16	VSS013	VSS094
A17	VSS014	VSS095
A18	VSS015	VSS096
A19	VSS016	VSS097
A20	VSS017	VSS098
A21	VSS018	VSS099
A22	VSS019	VSS100
A23	VSS020	VSS101
A24	VSS021	VSS102
A25	VSS022	VSS103
A26	VSS023	VSS104
A27	VSS024	VSS105
A28	VSS025	VSS106
A29	VSS026	VSS107
A30	VSS027	VSS108
A31	VSS028	VSS109
A32	VSS029	VSS110
A33	VSS030	VSS111
A34	VSS031	VSS112
A35	VSS032	VSS113
A36	VSS033	VSS114
A37	VSS034	VSS115
A38	VSS035	VSS116
A39	VSS036	VSS117
A40	VSS037	VSS118
A41	VSS038	VSS119
A42	VSS039	VSS120
A43	VSS040	VSS121
A44	VSS041	VSS122
A45	VSS042	VSS123
A46	VSS043	VSS124
A47	VSS044	VSS125
A48	VSS045	VSS126
A49	VSS046	VSS127
A50	VSS047	VSS128
A51	VSS048	VSS129
A52	VSS049	VSS130
A53	VSS050	VSS131
A54	VSS051	VSS132
A55	VSS052	VSS133
A56	VSS053	VSS134
A57	VSS054	VSS135
A58	VSS055	VSS136
A59	VSS056	VSS137
A60	VSS057	VSS138
A61	VSS058	VSS139
A62	VSS059	VSS140
A63	VSS060	VSS141
A64	VSS061	VSS142
A65	VSS062	VSS143
A66	VSS063	VSS144
A67	VSS064	VSS145
A68	VSS065	VSS146
A69	VSS066	VSS147
A70	VSS067	VSS148
A71	VSS068	VSS149
A72	VSS069	VSS150
A73	VSS070	VSS151
A74	VSS071	VSS152
A75	VSS072	VSS153
A76	VSS073	VSS154
A77	VSS074	VSS155
A78	VSS075	VSS156
A79	VSS076	VSS157
A80	VSS077	VSS158
A81	VSS078	VSS159
A82	VSS079	VSS160
A83	VSS080	VSS161
A84	VSS081	VSS162
A85	VSS082	VSS163

Merom Ball-out Rev 1a
CONN

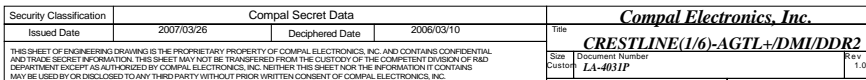
Mid Frequency Decoupling

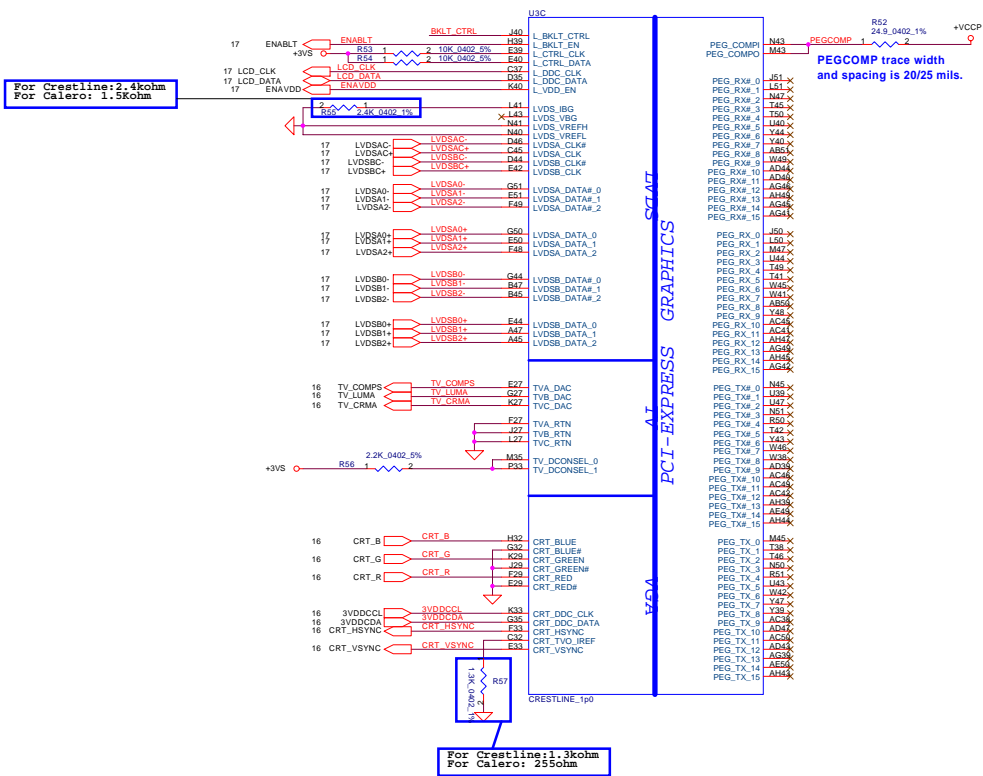
Near CPU CORE regulator

ESR <= 1.5m ohm
Capacitor > 1980uF

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				LA-4031P
				Rev
				1.0
				Date
				Wednesday, October 24, 2007
				Sheet
				6 of 42

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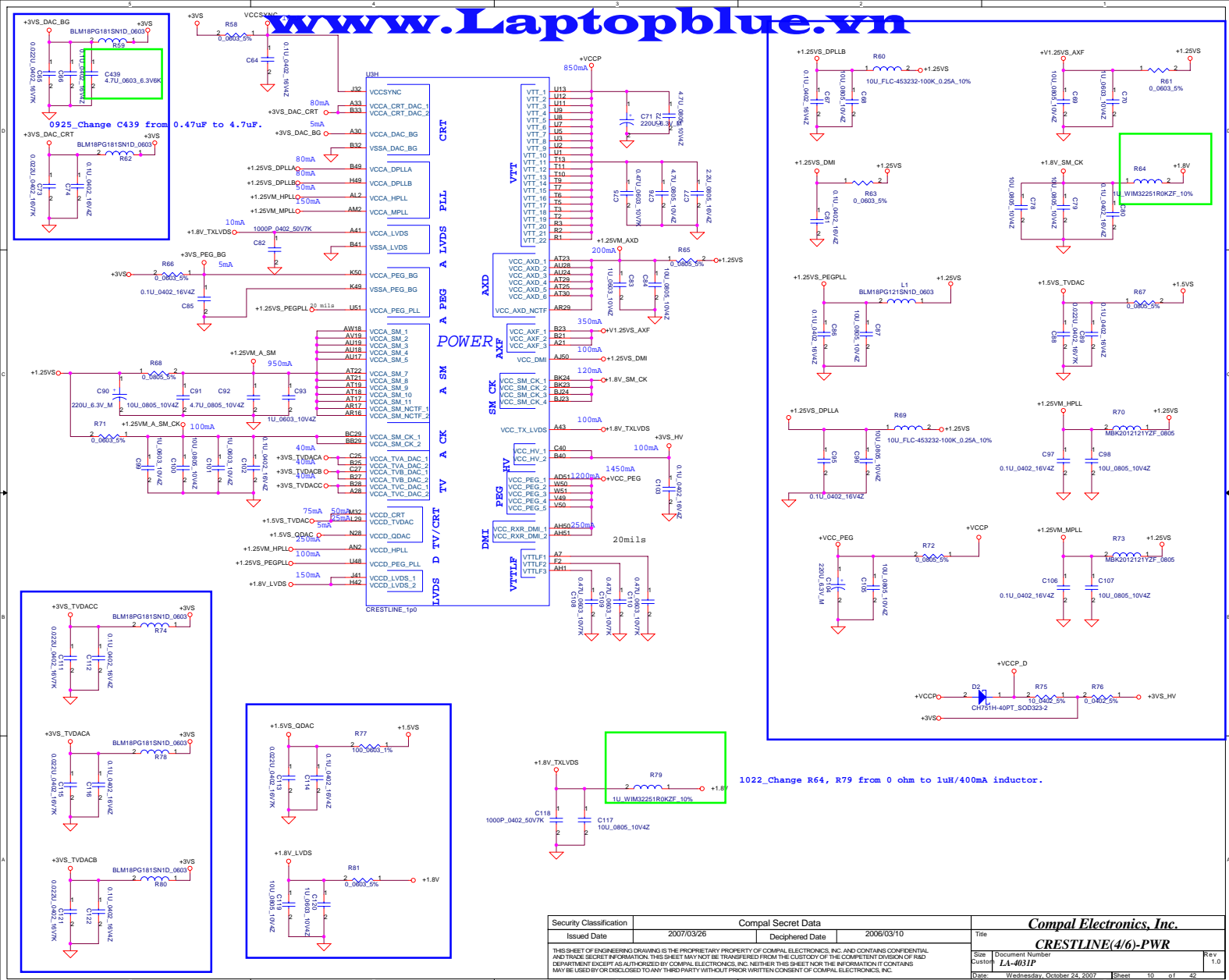


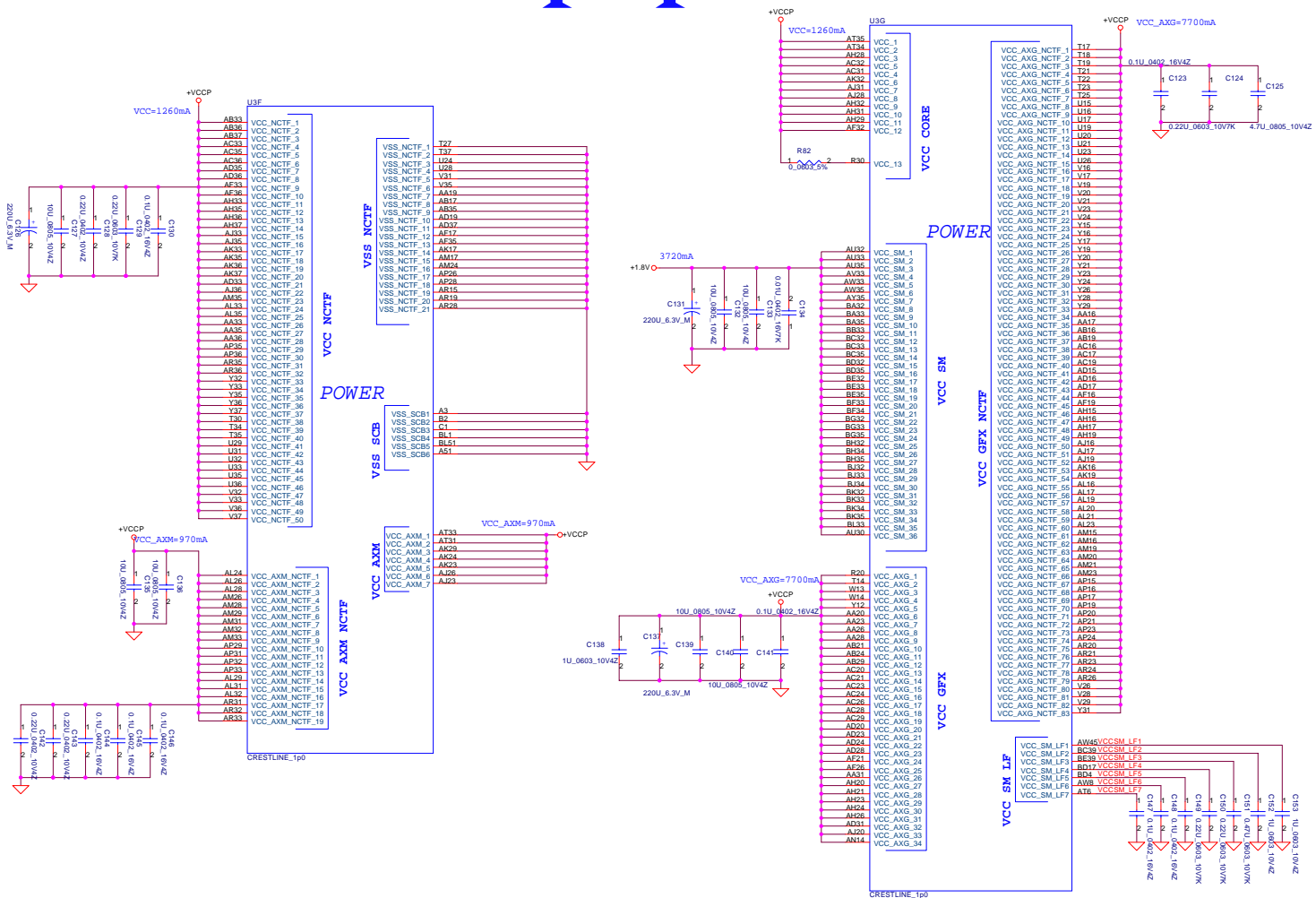


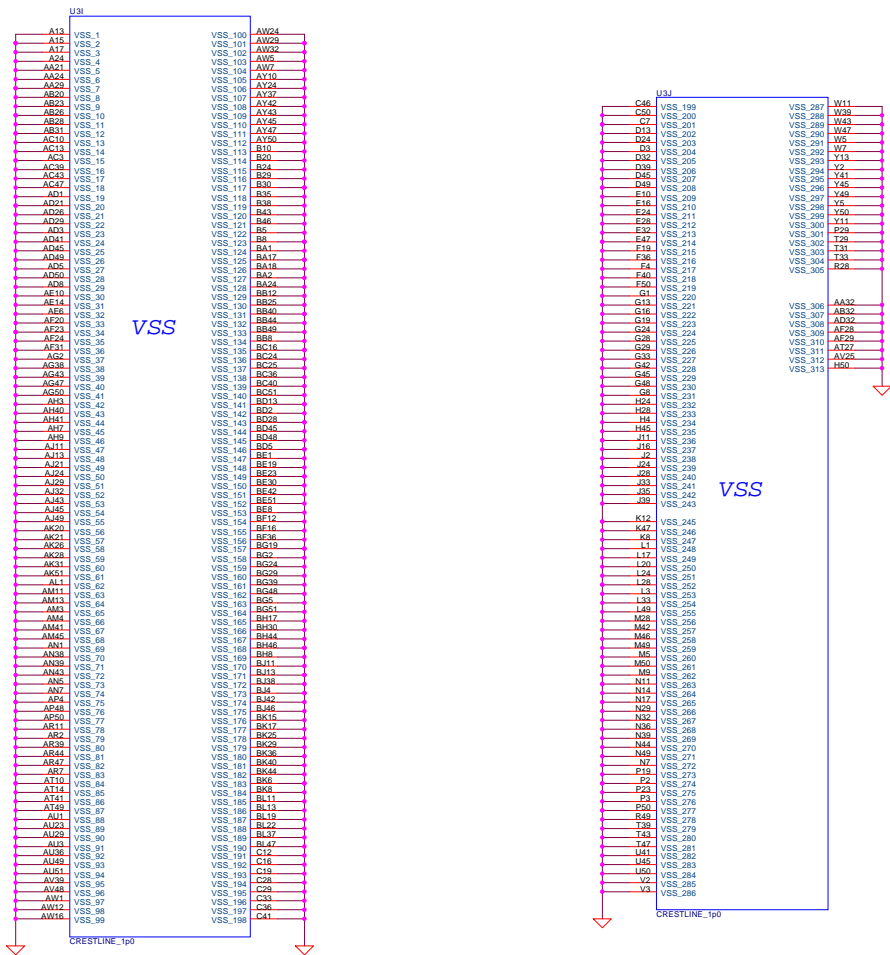
CFG[17:3] have internal pull up
CFG[19:18] have internal pull down

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIe)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved 00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[13:12] (XOR/ALLZ)	
CFG[15:14]	Reserved 0 = Disabled 1 = Enabled *
CFG16 (FSB Dynamic ODT)	
CFG[18:17]	Reserved
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.

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				Customer	LA-4031P
				Date	Wednesday, October 24, 2007
				Sheet	9 of 42
				Rev	1.0



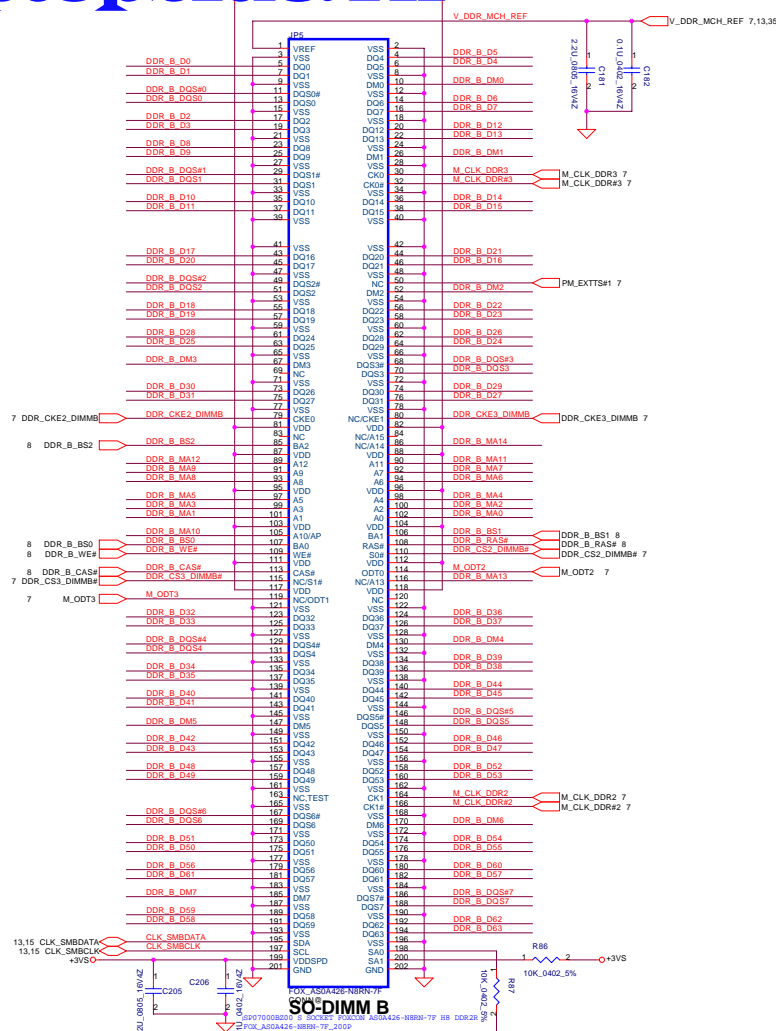





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				Date	Wednesday, October 24, 2007
				Sheet	12 of 42
				Rev	1.0

The diagram shows a transmission line model consisting of nine segments. Each segment is labeled with its length, 2.50,0005,1094Z. The segments are connected by nodes labeled C-1 through C-9. The input voltage at node C-1 is +18V. The output end of the cable is terminated with a load resistor R_L .

DDR Bank	Row	Col	Value	DDR Bank	Row	Col	Value
DDR_B_MA1	RP14	1	4	RP15	56_0A04	4P2R_5S	
DDR_B_MA2		1	4	RP16	56_0A04	4P2R_5S	
DDR_B_MA3		1	4	RP17	56_0A04	4P2R_5S	
DDR_B_MA4		1	4	RP18	56_0A04	4P2R_5S	
DDR_B_MA5		1	4	RP19	56_0A04	4P2R_5S	
DDR_B_MA6		1	4	RP20	56_0A04	4P2R_5S	
DDR_B_MA7		1	4	RP21	56_0A04	4P2R_5S	
DDR_B_MA8		1	4	RP22	56_0A04	4P2R_5S	
DDR_B_MA9		1	4	RP23	56_0A04	4P2R_5S	
DDR_B_MA10		1	4	RP24	56_0A04	4P2R_5S	
DDR_B_MA11		1	4	RP25	56_0A04	4P2R_5S	
DDR_B_MA12		1	4	RP26	56_0A04	4P2R_5S	
DDR_B_MA13		1	4	RP27	56_0A04	4P2R_5S	
DDR_B_MA14		1	4	RP28	56_0A04	4P2R_5S	
DDR_B_MA15		1	4	RP29	56_0A04	4P2R_5S	
DDR_B_MA16		1	4	RP30	56_0A04	4P2R_5S	
DDR_B_MA17		1	4	RP31	56_0A04	4P2R_5S	
DDR_B_MA18		1	4	RP32	56_0A04	4P2R_5S	
DDR_B_MA19		1	4	RP33	56_0A04	4P2R_5S	
DDR_B_MA20		1	4	RP34	56_0A04	4P2R_5S	
DDR_B_MA21		1	4	RP35	56_0A04	4P2R_5S	
DDR_B_MA22		1	4	RP36	56_0A04	4P2R_5S	
DDR_B_MA23		1	4	RP37	56_0A04	4P2R_5S	
DDR_B_MA24		1	4	RP38	56_0A04	4P2R_5S	
DDR_B_MA25		1	4	RP39	56_0A04	4P2R_5S	
DDR_B_MA26		1	4	RP40	56_0A04	4P2R_5S	
DDR_B_MA27		1	4	RP41	56_0A04	4P2R_5S	
DDR_B_MA28		1	4	RP42	56_0A04	4P2R_5S	
DDR_B_MA29		1	4	RP43	56_0A04	4P2R_5S	
DDR_B_MA30		1	4	RP44	56_0A04	4P2R_5S	
DDR_B_MA31		1	4	RP45	56_0A04	4P2R_5S	
DDR_B_MA32		1	4	RP46	56_0A04	4P2R_5S	
DDR_B_MA33		1	4	RP47	56_0A04	4P2R_5S	
DDR_B_MA34		1	4	RP48	56_0A04	4P2R_5S	
DDR_B_MA35		1	4	RP49	56_0A04	4P2R_5S	
DDR_B_MA36		1	4	RP50	56_0A04	4P2R_5S	
DDR_B_MA37		1	4	RP51	56_0A04	4P2R_5S	
DDR_B_MA38		1	4	RP52	56_0A04	4P2R_5S	
DDR_B_MA39		1	4	RP53	56_0A04	4P2R_5S	
DDR_B_MA40		1	4	RP54	56_0A04	4P2R_5S	
DDR_B_MA41		1	4	RP55	56_0A04	4P2R_5S	
DDR_B_MA42		1	4	RP56	56_0A04	4P2R_5S	
DDR_B_MA43		1	4	RP57	56_0A04	4P2R_5S	
DDR_B_MA44		1	4	RP58	56_0A04	4P2R_5S	
DDR_B_MA45		1	4	RP59	56_0A04	4P2R_5S	
DDR_B_MA46		1	4	RP60	56_0A04	4P2R_5S	
DDR_B_MA47		1	4	RP61	56_0A04	4P2R_5S	
DDR_B_MA48		1	4	RP62	56_0A04	4P2R_5S	
DDR_B_MA49		1	4	RP63	56_0A04	4P2R_5S	
DDR_B_MA50		1	4	RP64	56_0A04	4P2R_5S	
DDR_B_MA51		1	4	RP65	56_0A04	4P2R_5S	
DDR_B_MA52		1	4	RP66	56_0A04	4P2R_5S	
DDR_B_MA53	</						



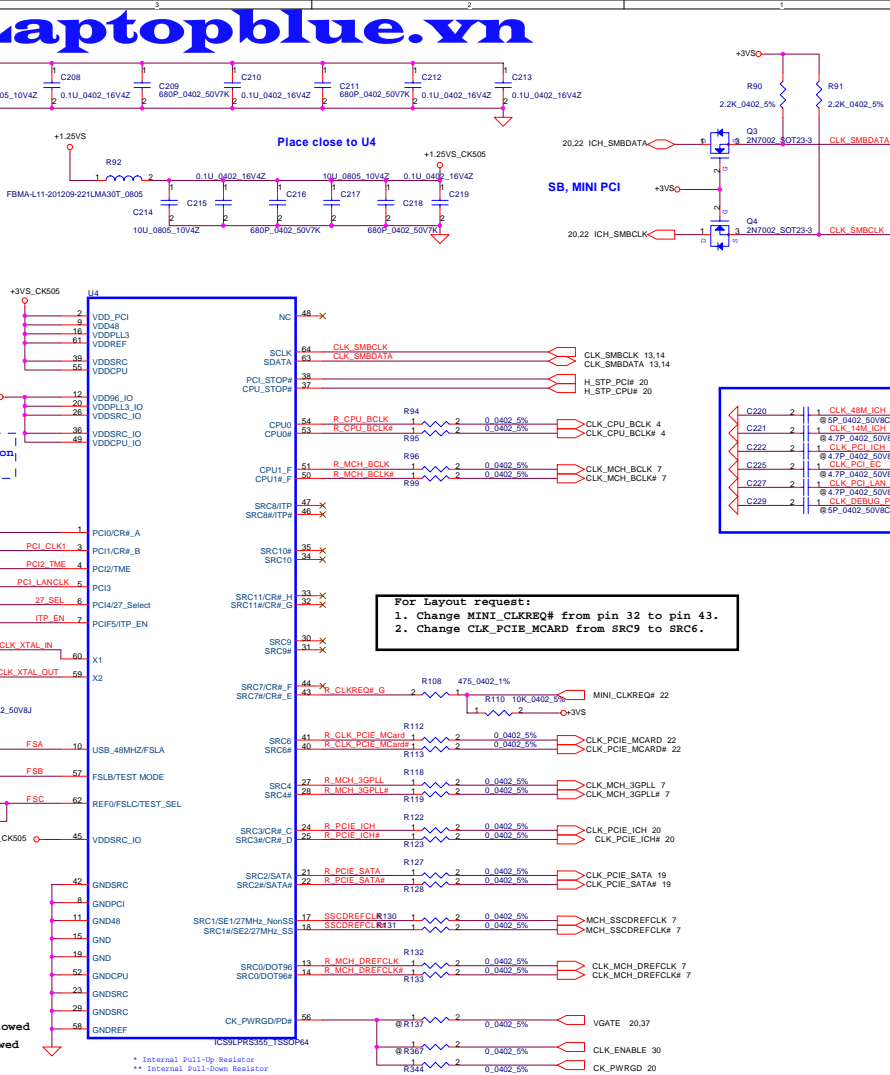
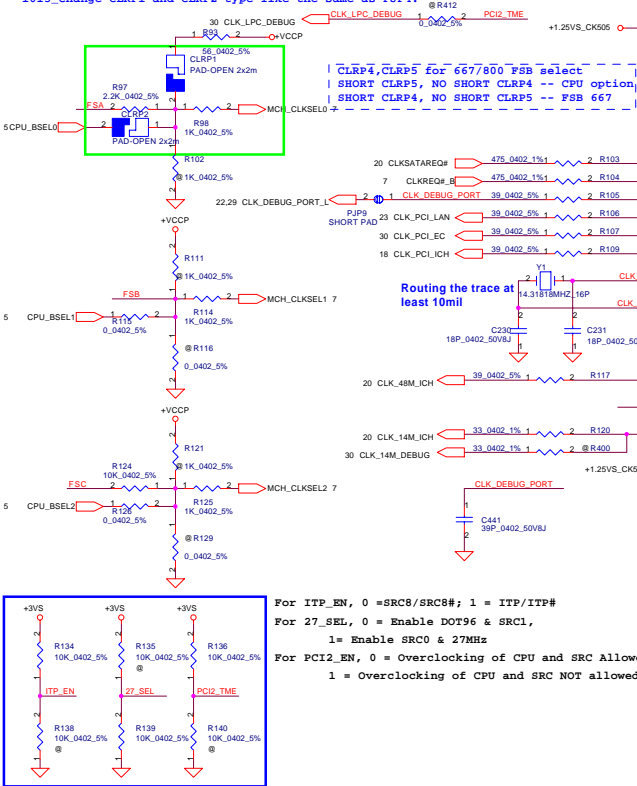
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					Date 14-001P	Rev 1.0
					Drawn 02/26/04	Issued 14-01-02

FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	1	133	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3

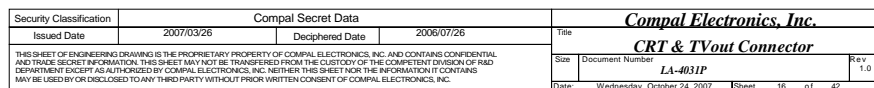
FSB Frequency Selet:

CPU Driven	Stuff	R107	R135	R1083
★(Default)	No stuff	R1074	R1086	R1098 R1113 R1128 R1139
667MHz	Stuff	R1086	R1139	R1135 R1074 R1139 R1135
	No stuff	R1083	R1107	R1128 R1113 R1098
800MHz	Stuff	R1135	R1139	
	No stuff	R1083	R1086	R1098 R1128 R1074 R1107 R1113

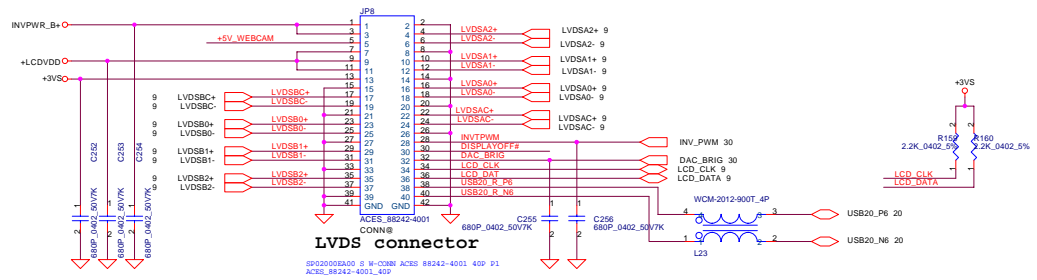
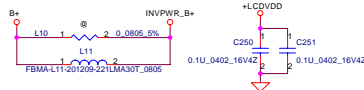
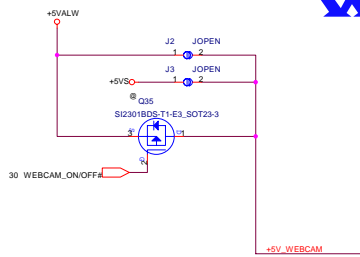
1015_Change CLR#1 and CLR#2 type like the same as RJP4.



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Date: Wednesday, October 24, 2007		Sheet 18 of 42

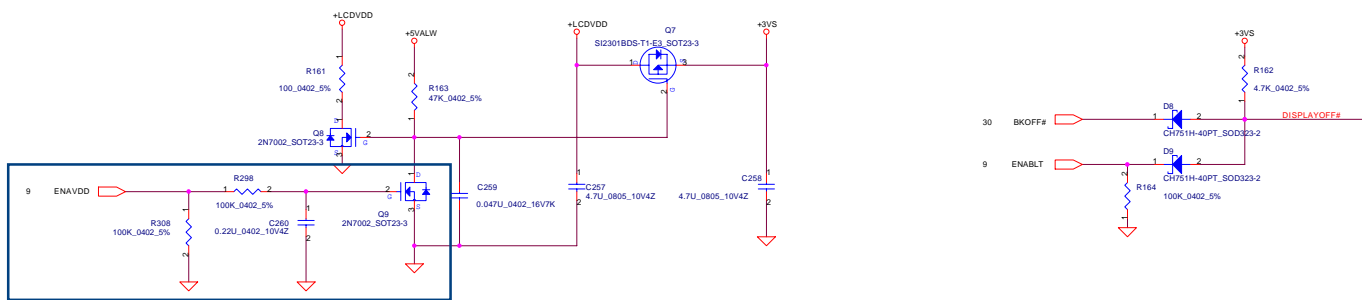


LVDS CONN



LVDS connector

SP020098A00 50 W-CONN ACES 88242-4001 40P P1
ACES_88242-4001_40P

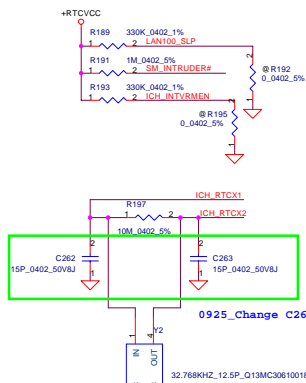


Avoid Panel display garbage after power on.

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				Date	Wednesday, October 24, 2007
				Sheet	17 of 42
				Rev	1.0

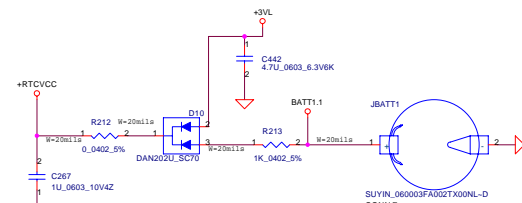
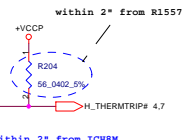
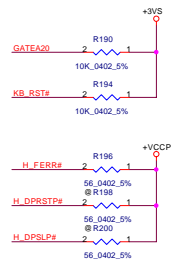
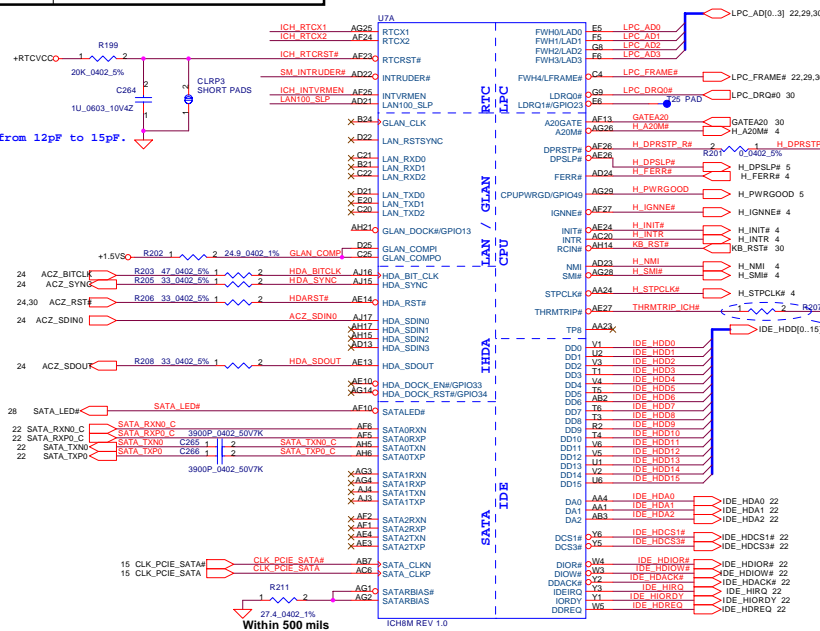
Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

A16 swap override Strap	
PCI_GNT3#	*Low= A16 swap override Enable High= Default

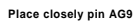


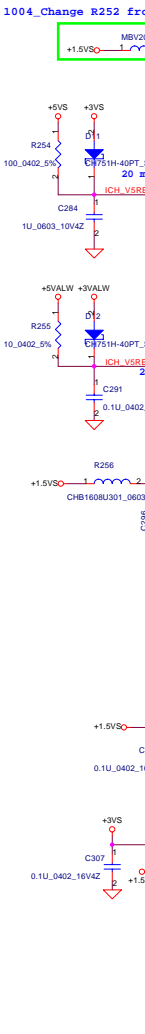
ICH8M internal VR Enable Strap
(Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)

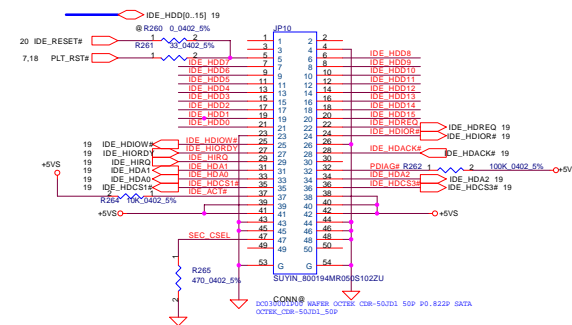
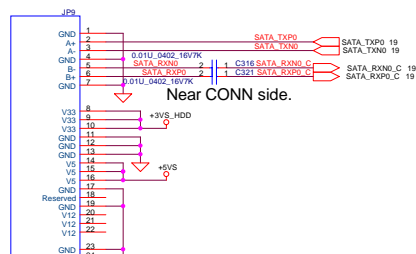
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)
ICH8M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)



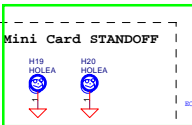
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Date	Wednesday, October 24, 2007	Sheet	19	of 42



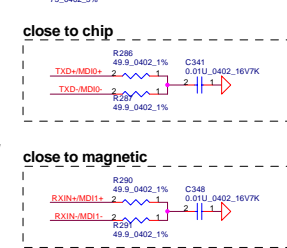




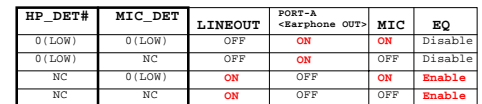
SP01000P700 S H-CONN ACES 88914-5204 52P P0.8



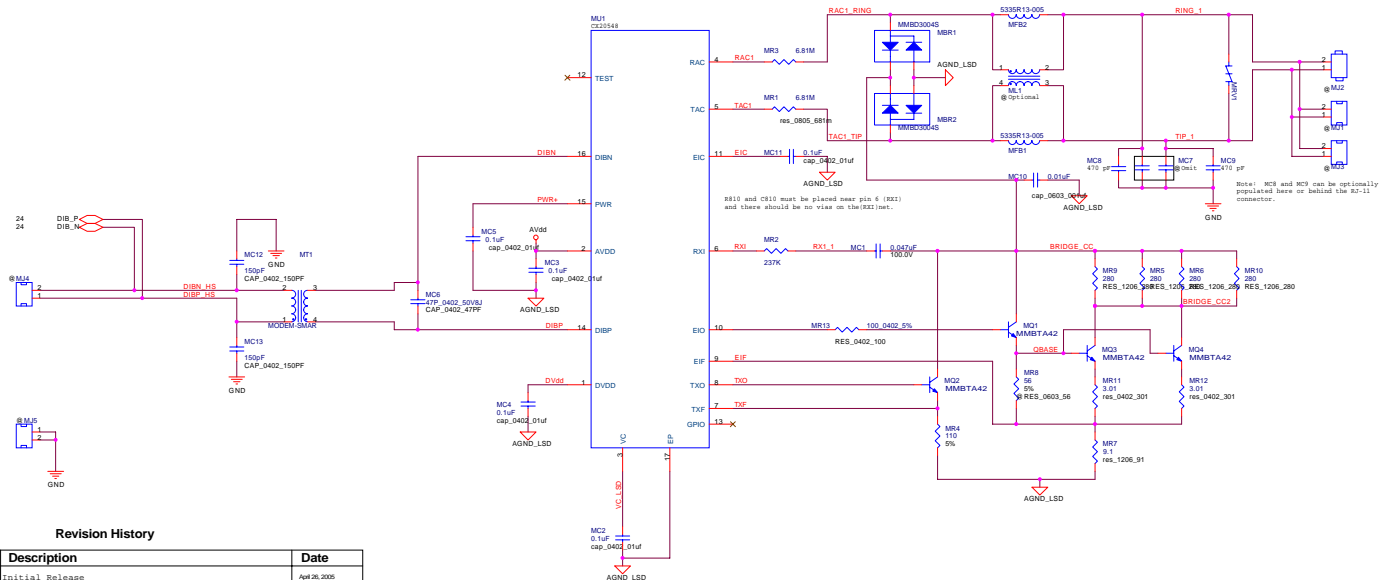
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			Date: Wednesday, October 24, 2007	Sheet 23 of 42



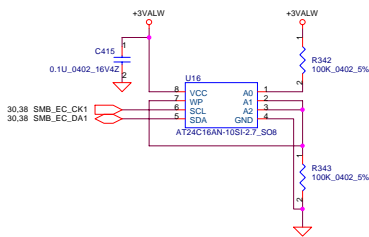
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Issued Date	2007/03/26	Deciphered Date	2006/03/10	
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			Sheet	21 of 42



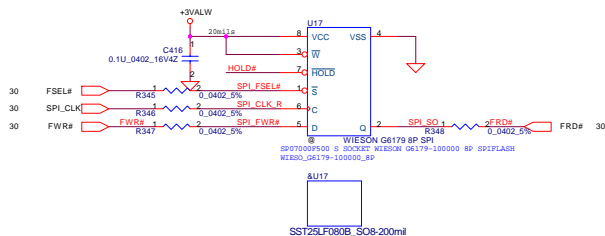
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Date: Wednesday, October 24, 2007				Sheet: 25 of 45

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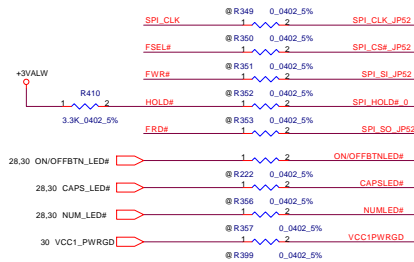
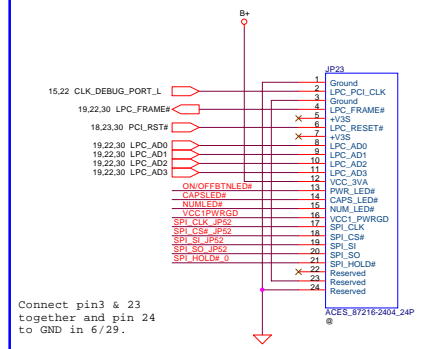
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Date:	Wednesday, Oct 24, 2007	Sheet	98	of	102	



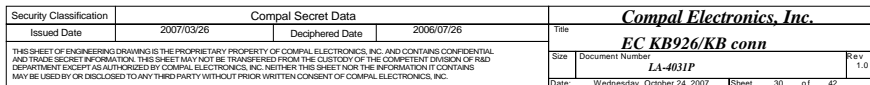
SPI ROM



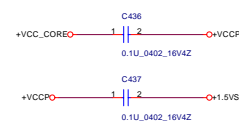
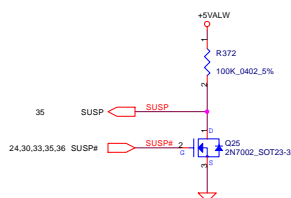
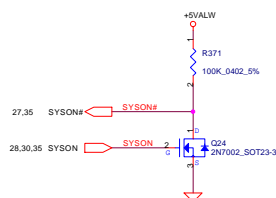
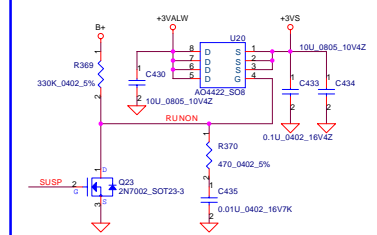
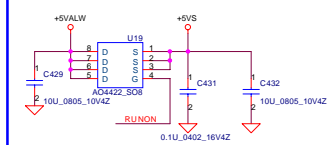
LPC Debug Port



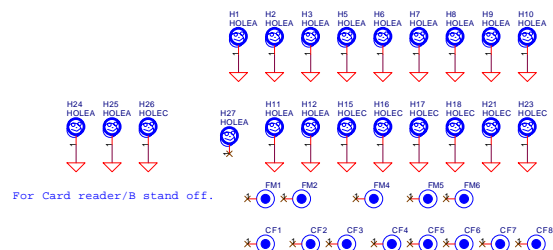
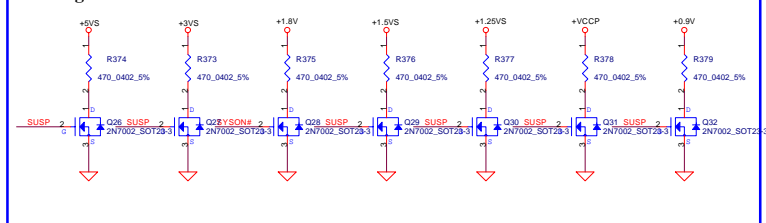
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
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				Date	Wednesday, October 24, 2007
				Sheet	29 of 42
				Rev	1.0




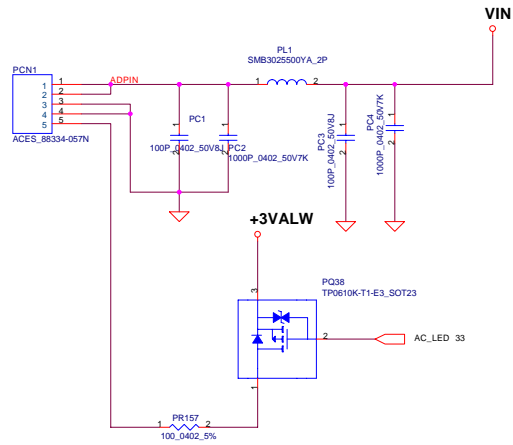
+3VALW to +3VS Transfer



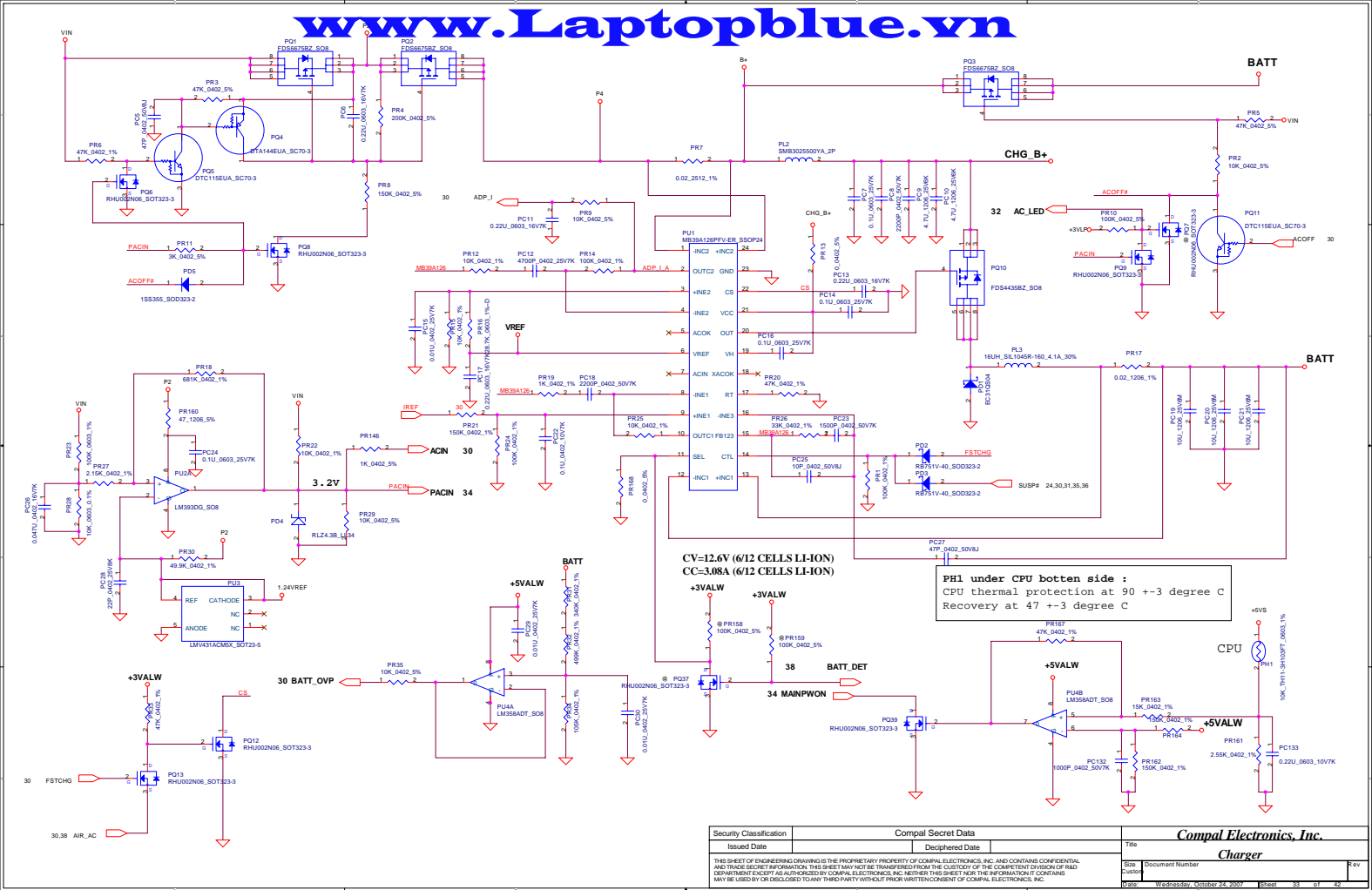
Discharge circuit

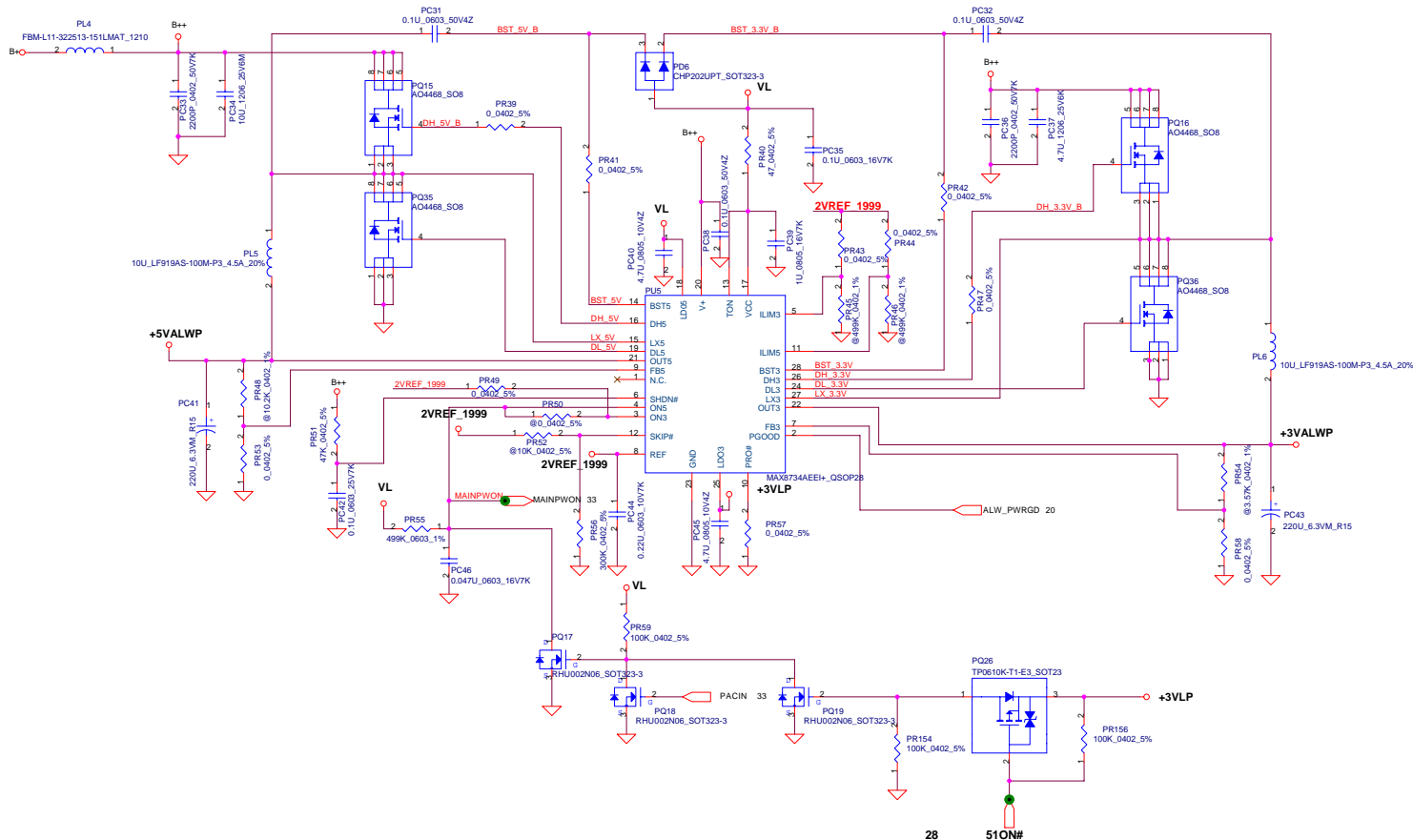


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Date	02/24/98	Date	02/24/98	Rev. 1.0

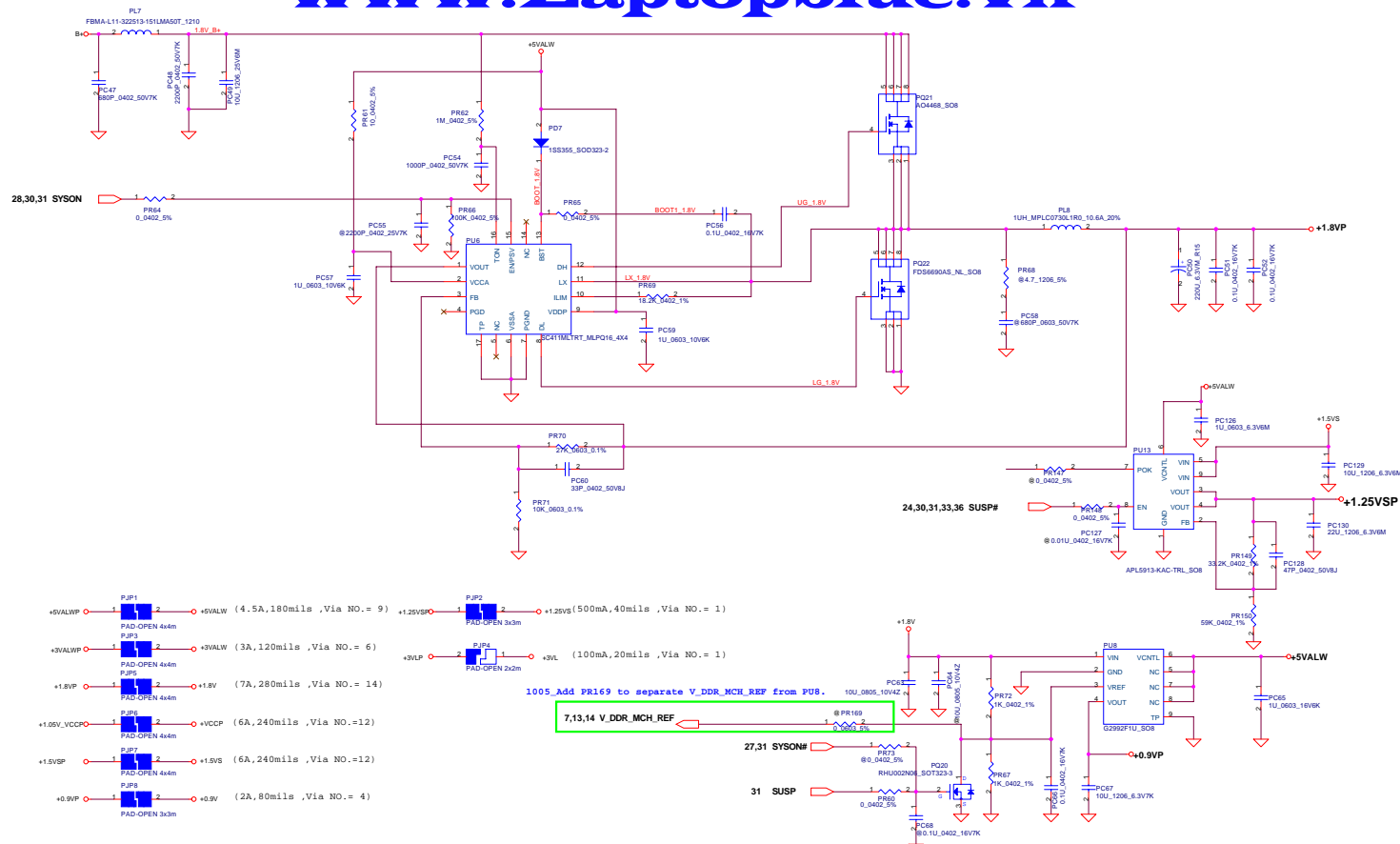


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				Date	Wednesday, October 24, 2007
				Sheet	32 of 42





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				Date	Wednesday, October 24, 2007
				Sheet	34 of 42

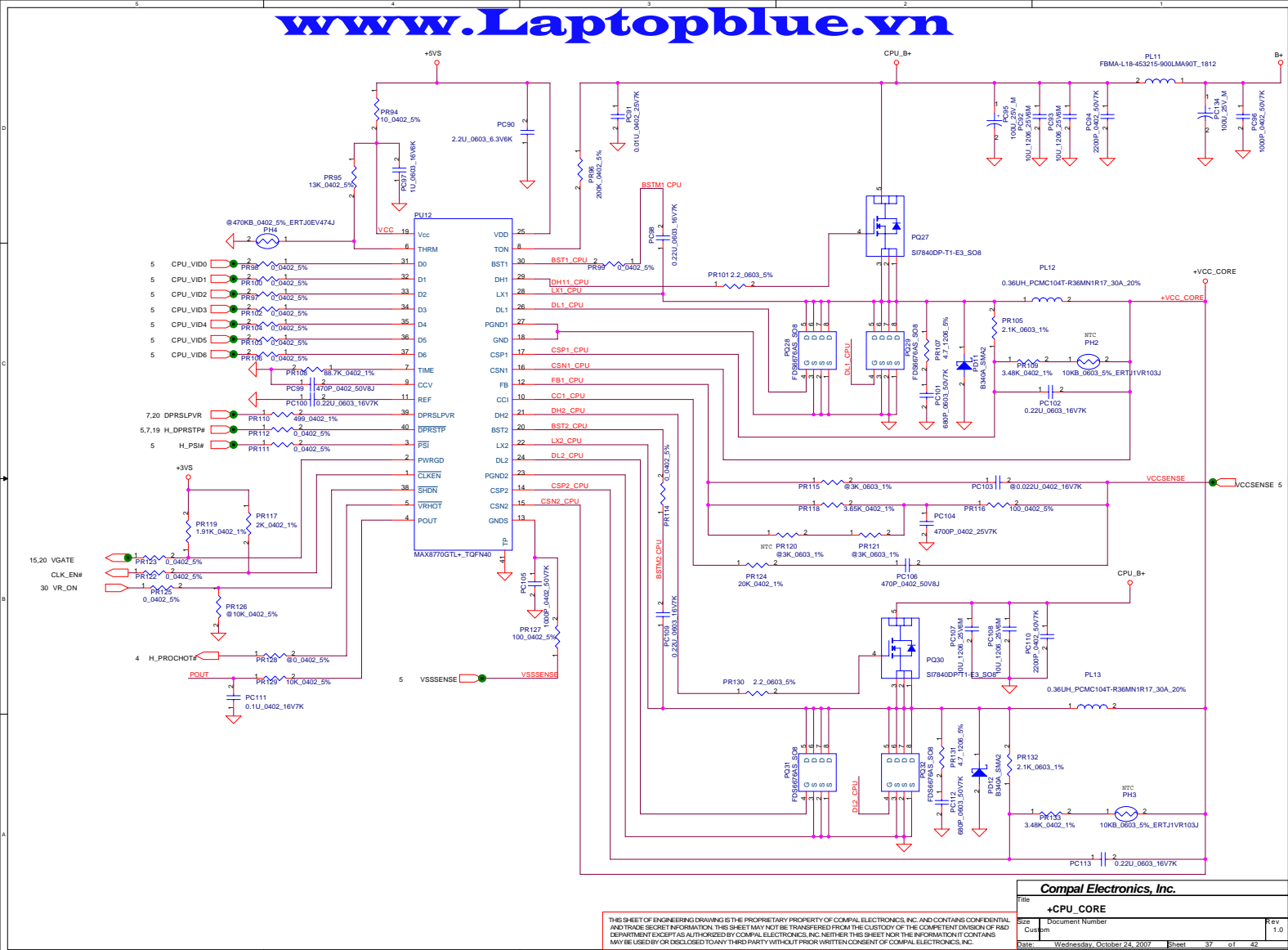


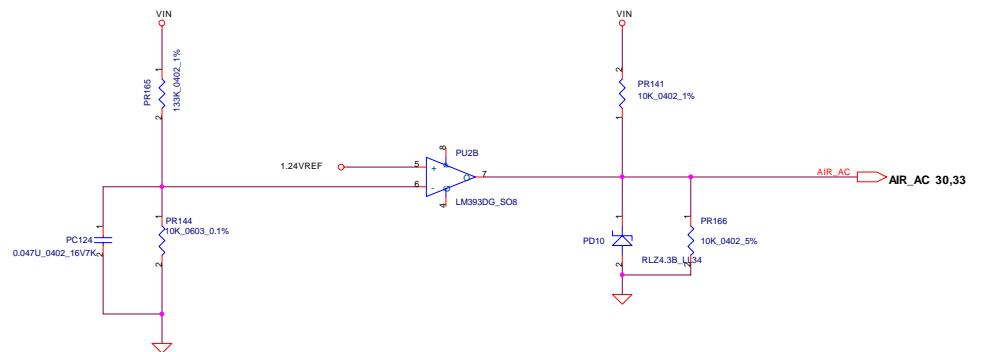
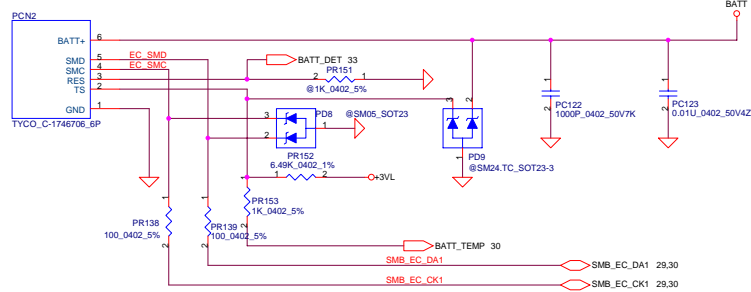
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				Date	Wednesday, October 24, 2007
				Sheet	42 of 38

Item	Change item	Page	Date	Phase
1	Change R296 2.2K to 4.7K and Reserved R303	24	8/6	SI-->PV
2	Add R424 R425 100ohm on MIC_EXT_R and MIC_EXT_L	26	8/6	SI-->PV
3	Fine tune R298 C260 value	17	8/6	SI-->PV
4	Change PIRQ from F to A	18	8/14	SI-->PV
5	Connect PCI_SERR# to EC GPIO pin.	18	8/31	SI-->PV
6	Modify PC BEEP circuit.	20	8/31	SI-->PV
7	For support Intel Penryn CPU.	04	9/3	SI-->PV
8	For ESD request.	28	9/3	SI-->PV
9	For EMI request.	26	9/5	SI-->PV
10	Change C391, C393, C395, C396 from 0.47uF to 0.047uF.	26	9/7	SI-->PV
11	Add R417 and R418 to fine-tune Vp-p.	26	9/7	SI-->PV
12	For ESD request.	20	9/7	SI-->PV
13				
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				Date:	Wednesday, October 24, 2007	Sheet 40 of 42

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Date	Wednesday, October 24, 2007	Sheet	42 of 42	Rev 1.0		