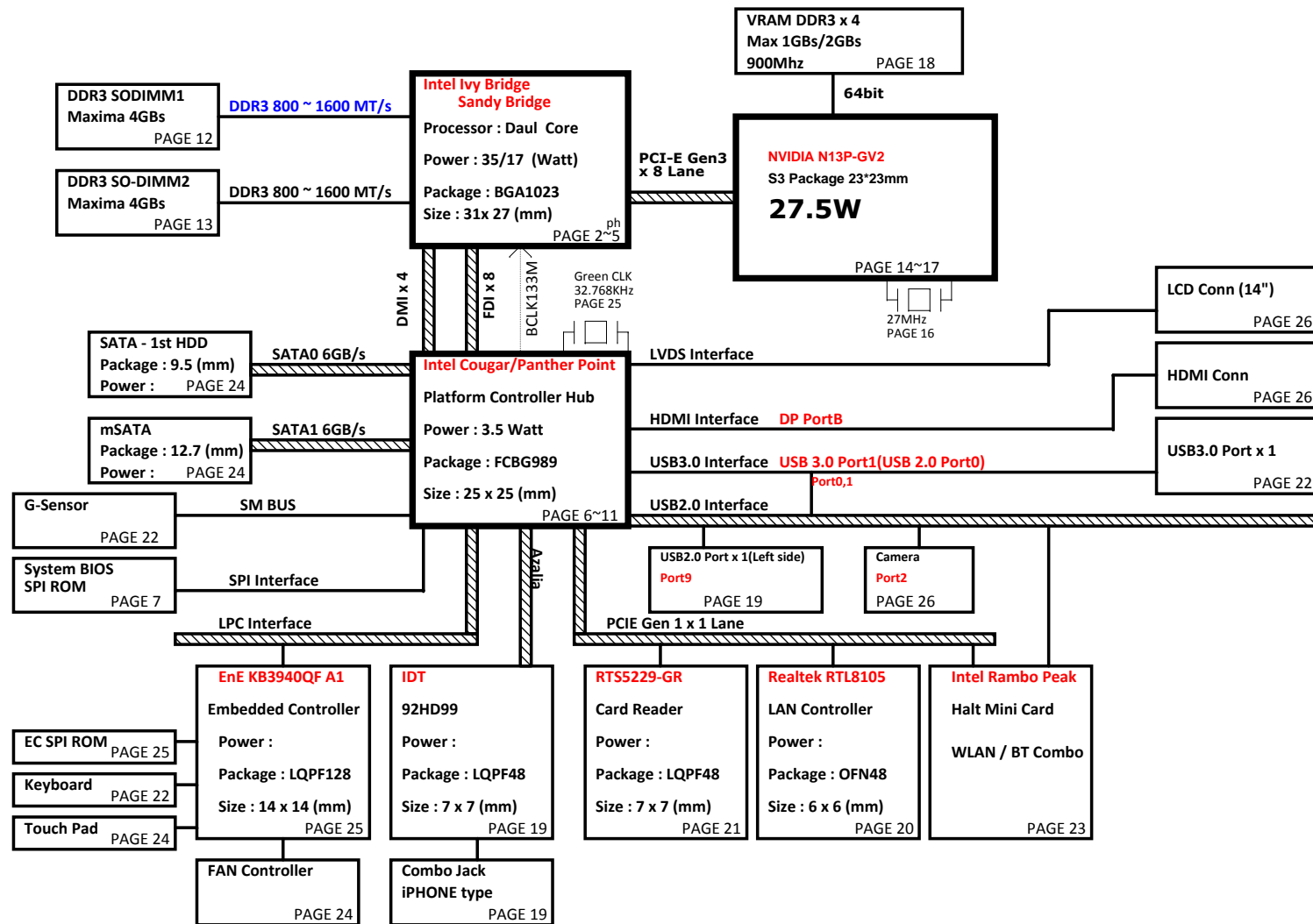


Volks DIS/UMA (14"/15.6") Ultra/Slim

Intel Chief River Platform Block Diagram



PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT

Power Source

BQ24738
System Charge Power (+BATCHG)

Ricktek RT8223P
System Power (+3VPCU/+5VPCU/
+3VS5/+5VS5)

**NCP6132/NCP5911/RT8240P/
TP551462RGER**
Processor Power (+VCC_CORE/
+1.05_VTT/+VCCSA)

SLG55448V
System Discharge Power
(+1.5V/+3V/+5V)

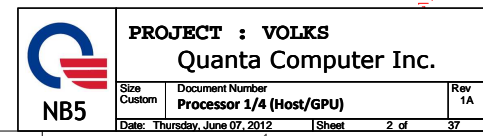
Richtek RT8207
System Memory Power (+1.5VSUS/
+0.75V_DDR_VTT)

NCP3218G
GPU core power(+VGACORE)

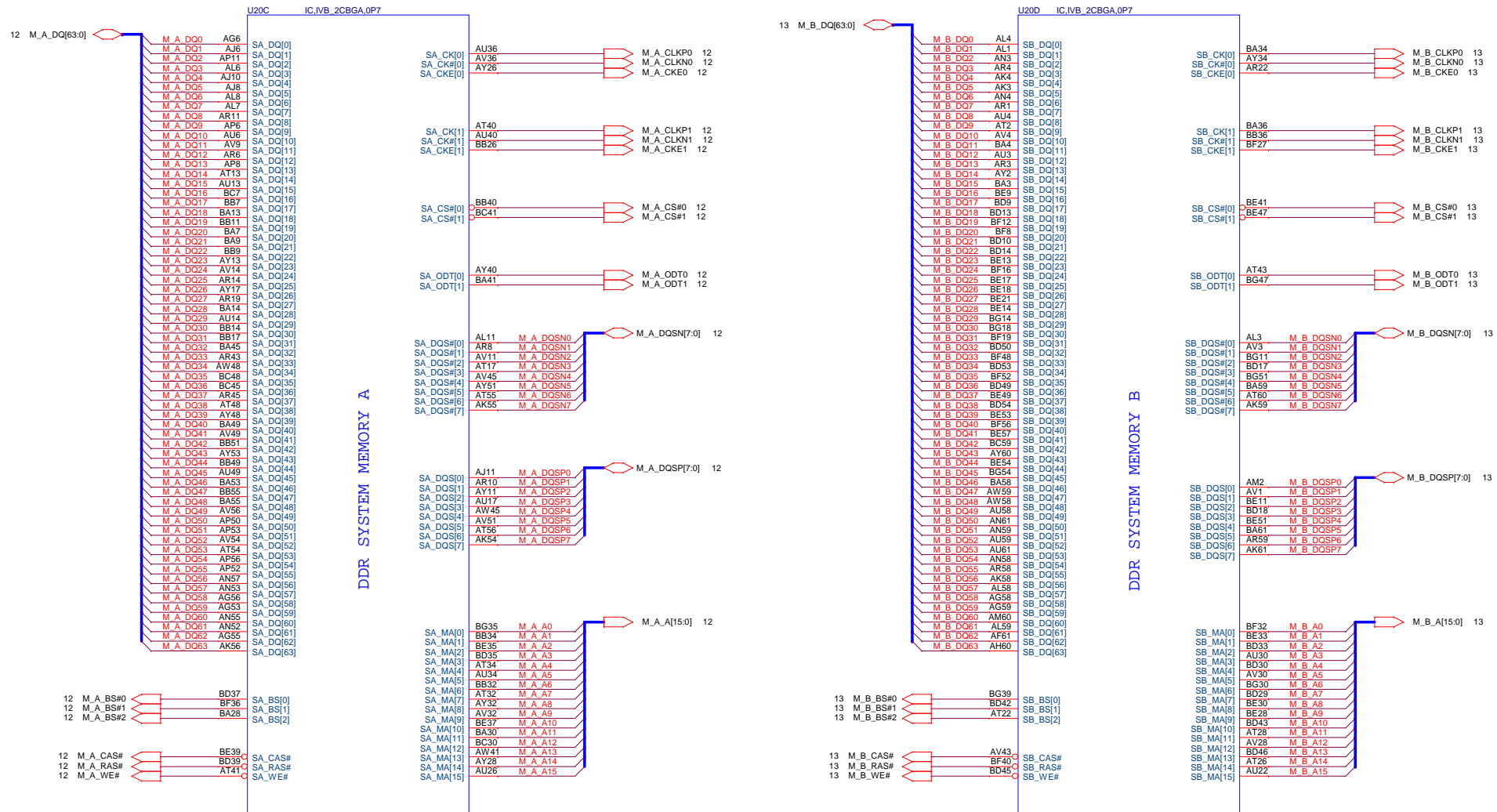


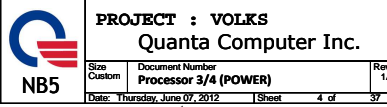
PROJECT : VOLKS
Quanta Computer Inc.

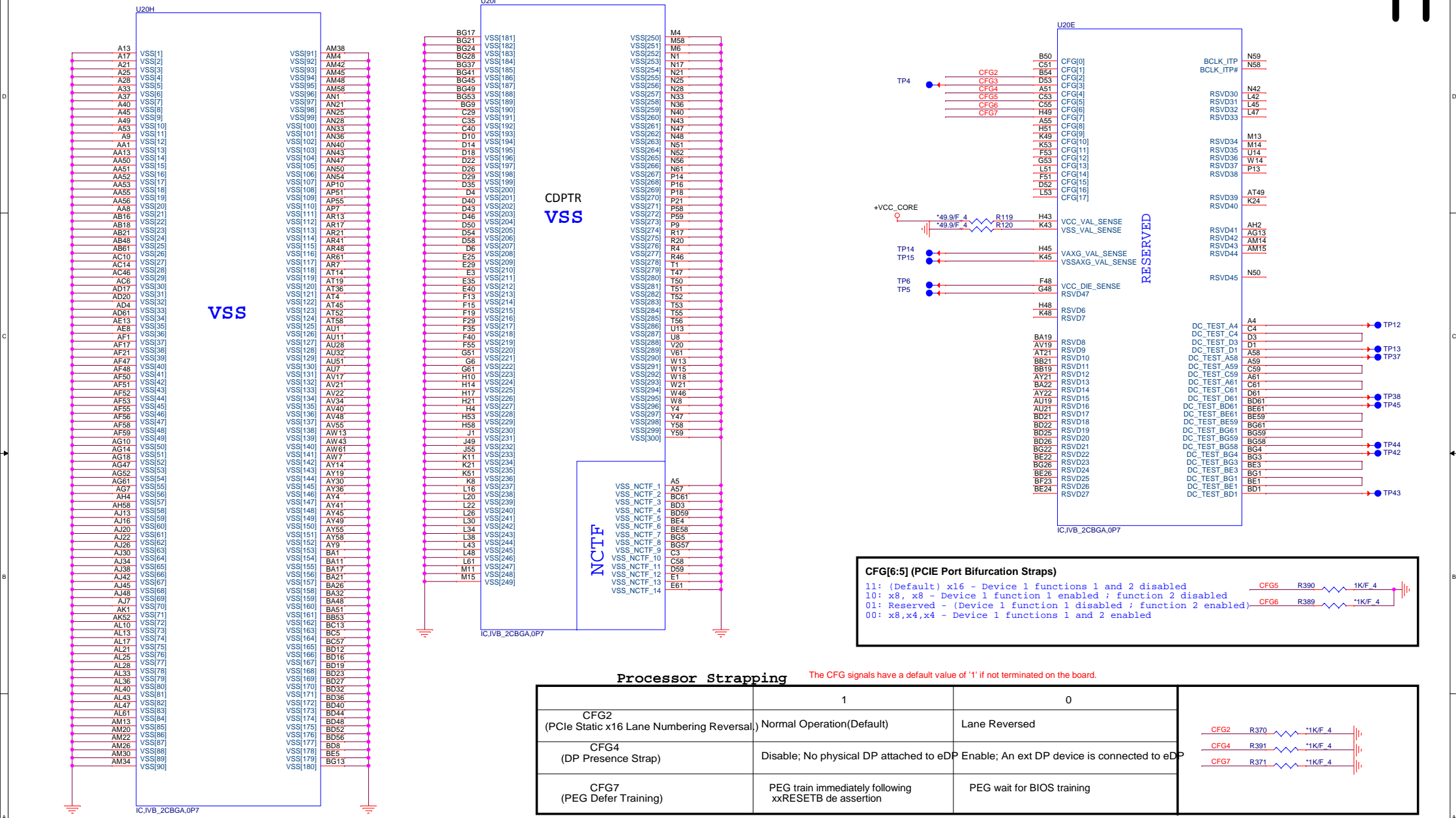
Size Custom	Document Number Block Diagram	Rev 1A
Date: Thursday, June 07, 2012	Sheet	1 of 37



Ivy Bridge Processor (DDR3)








CFG[6:5] (PCIe Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0	
CFG2 (PCIe Static x16 Lane Numbering Reversal)	Normal Operation(Default)	Lane Reversed	
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training	

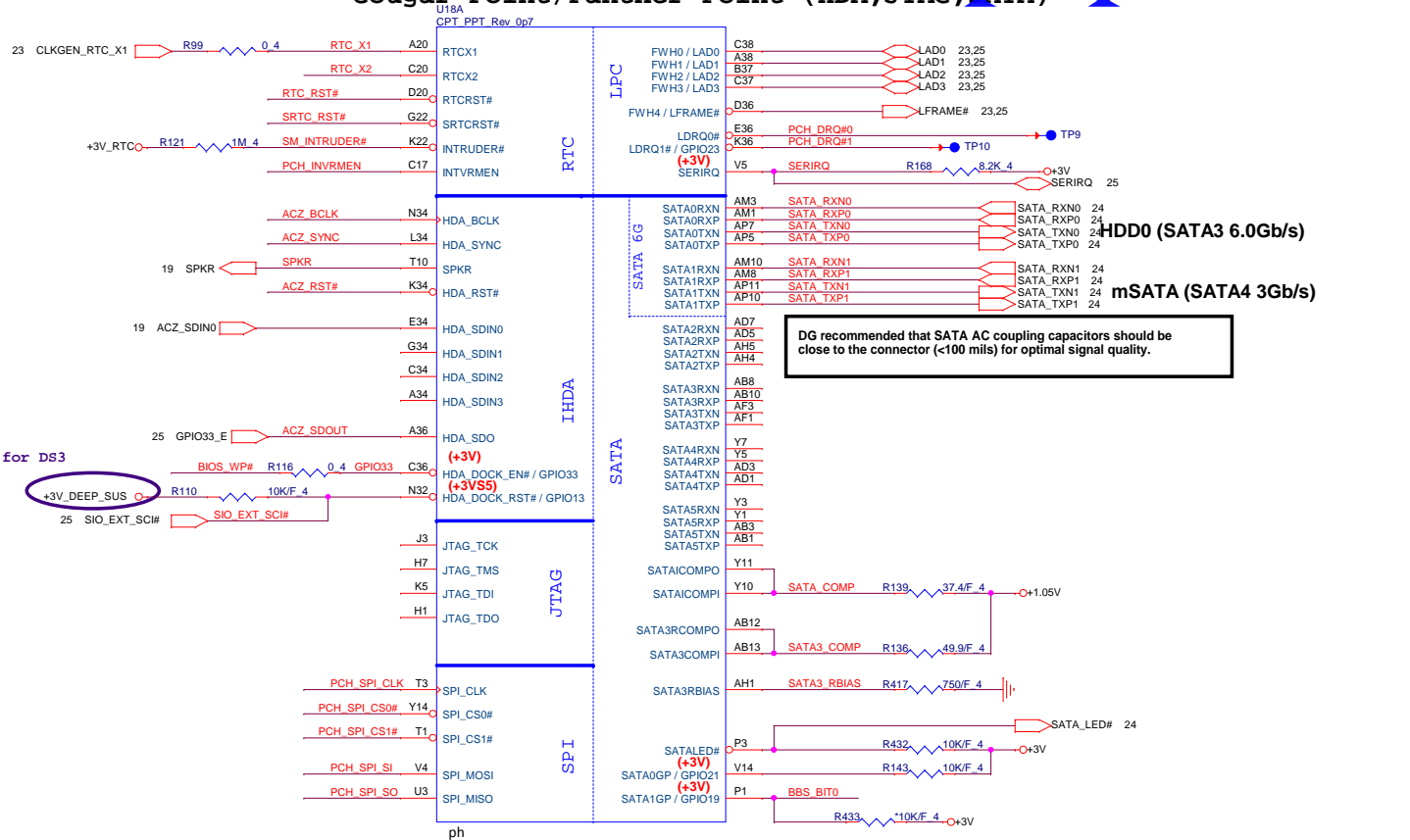


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Size Custom	Document Number Processor 4/4 (RSV,Ground)	Rev 1A
Date: Thursday, June 07, 2012	Sheet	5 of 37



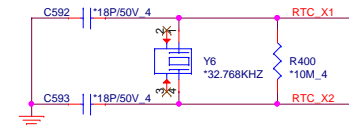
Size Custom	Document Number PCH 1/6 (Host/Display)	Rev 1A
Date: Thursday, June 07, 2012	Sheet 6 of	37



PCH Strap Table

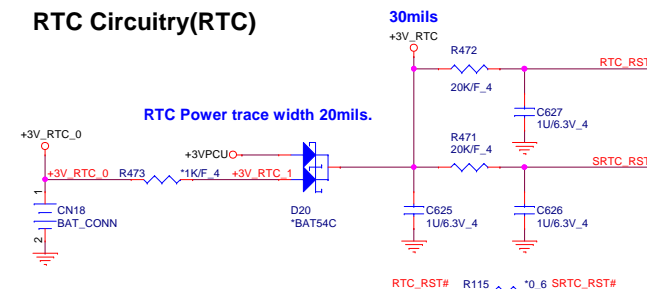
Pin Name	Strap description	Sampled	Configuration	Circuit									
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V ₀ R152 1K/F 4 SPKR									
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	+3V ₀ R363 1K/F 4 R364 10K/F 4 PCI_GNT3# 8									
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V _{RTC0} R122 330K 4 PCH_INVRMEN									
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R104 1K/F 4 ACZ_SDOOUT ACZ_SDOOUT 25									
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"><thead><tr><th>GNT1#</th><th>GNT0#</th><th>Boot Location</th></tr></thead><tbody><tr><td>1</td><td>0</td><td>SPI</td></tr><tr><td>0</td><td>1</td><td>LPC</td></tr></tbody></table>	GNT1#	GNT0#	Boot Location	1	0	SPI	0	1	LPC	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1# R419 1K/F 4 BBS_BIT0 R354 1K/F 4 BBS_BIT1 8
GNT1#	GNT0#	Boot Location											
1	0	SPI											
0	1	LPC											
GPIO19 Different from Calpella	Boot BIOS Selection 0 [bit-0]	PWROK											
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN									
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V ₀ R416 1K/F 4 NV_ALE 8									
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm	+1.8V ₀ R415 2.2K 4 R414 1K/F 4 NV_CLE 9 H_SNB_IVB# 2									
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	for DS3 +3V _{DEEP_SUS} R135 1K/F 4 ACZ_SYNC									
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	+3V _{DEEP_SUS} R405 1K/F 4 ACZ_SDOOUT									
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)										
GPIO28 Different from Calpella	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)										
SPI_MOSI	ITPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable										

RTC Clock 32.768KHz

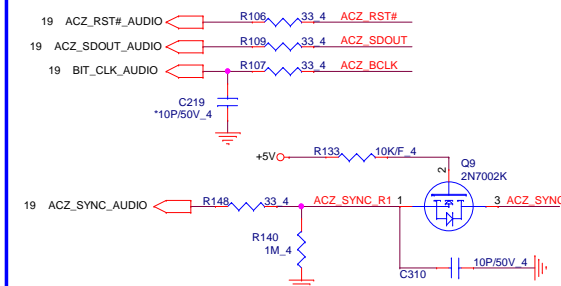


no stuff if use green Clock

RTC Circuitry(RTC)

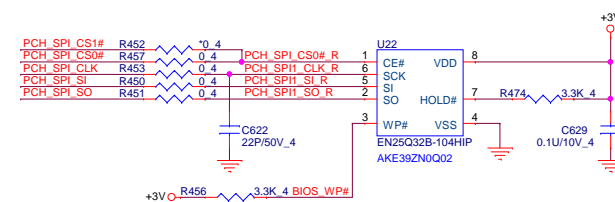


HDA Bus(CLG)



Vender	Size	P/N
EON	4MB	AKE392N0Q02 (EN25Q32B-104HIP)
MX	4MB	AKE39FP0Z02 (MX25L3206EM2I-12G)
AMIC	4MB	AKE39F-0800 (A25LQ32AM-F/Q)
Socket		DFHS08FS023

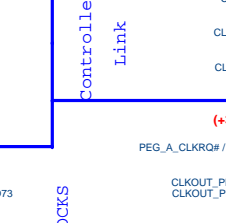
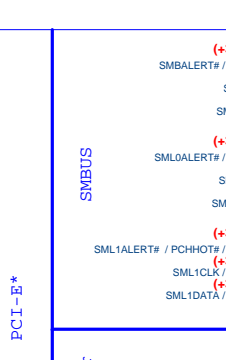
PCH SPI ROM(CLG)



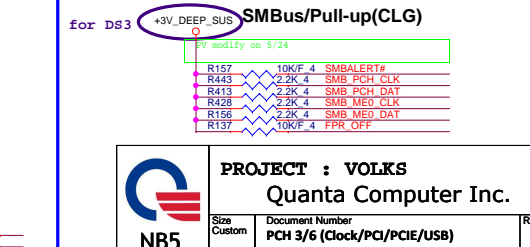
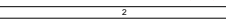
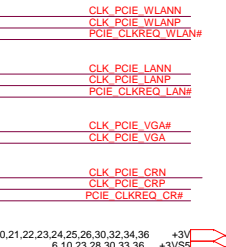
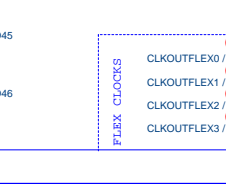
PROJECT : VOLKS
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Size	Document Number	Rev
Custom	PCH 2/6 (HDA/RTC/SATA/SPI)	1A
Date: Thursday, June 07, 2012	Sheet	7 of 37

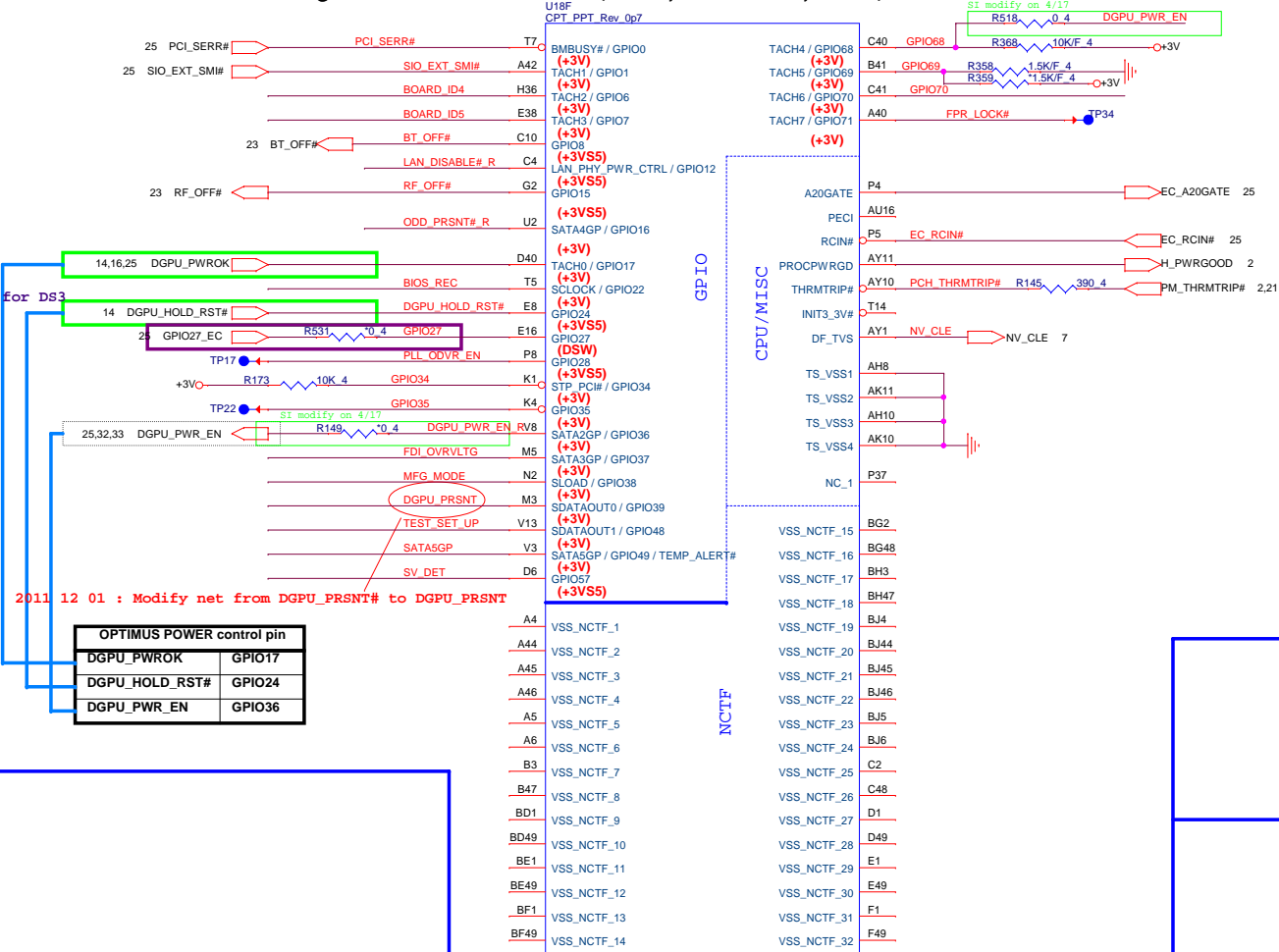
Cougar Point-M/Panther Point (PCI-E,SMBUS,CLK)



CLKOUT

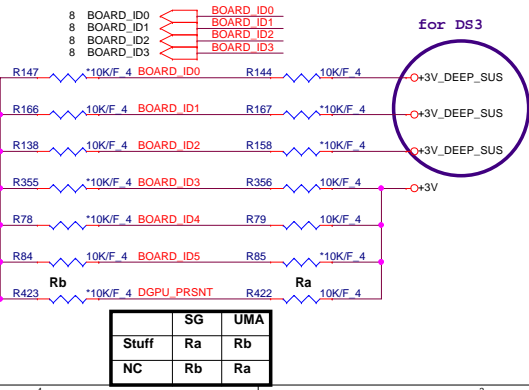


Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)



Chief River BOARD ID SETTING

Model	BOARD_ID5	BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
U33 UMA	0	0	0	0	0	0
U33 DIS 128*16 VRAM	0	0	0	0	0	1
U33 DIS 256X16 VRAM	0	0	0	0	1	1
	0	0	0	1	1	1
U33 HM77	0	0	1	X	X	X
U33 HM70	0	0	0	X	X	X



MFG-TEST

for D83

+3V_DEEP_SUS

RF_OFF# → R437 10K/F 4

BIOS_REC → R169 10K/F 4

TEST_SET_UP → R146 10K/F 4

SV_DET →

FDI_OVRVLTG → R171 10K/F 4

SATA2GP/GPIO36 → Reserved only

TEST DETECT → Low = Default

FDI TERMINATION VOLTAGE OVERRIDE → Reserved only

GPIO Pull-up/Pull-down(CLG)

for D83

+3V_DEEP_SUS

BT_OFF# → R408 10K/F 4

LAN_DISABLE# → R → R425 10K/F 4

DGPU_HOLD_RST# → R334 10K/F 4

SIO_EXT_SMI# → R357 10K/F 4

BT_OFF# → R409 10K/F 4

EC_A20GATE → R162 10K/F 4

EC_RCIN# → R163 10K/F 4

SATA5GP → R431 10K/F 4

GPIO70 → R365 1.5K/F 4

FPR_LOCK# → R360 1.5K/F 4

ODD_PRST# → R → R418 10K/F 4

DGPU_PWROK → R366 10K/F 4

GPIO27 → R129 10K/F 4

Intel ME Crypto Transport Layer Security (TLS) cipher suite

Low = Disable (Default)

High = Enable

BIOS RECOVERY

High = Disable (Default)

Low = Enable

TEST SET UP

High = Strong (Default)

TEST DETECT

Low = Default

SATA2GP/GPIO36

Reserved only

FDI TERMINATION VOLTAGE OVERRIDE

Reserved only

PROJECT : VOLKS

Quanta Computer Inc.

Size Custom

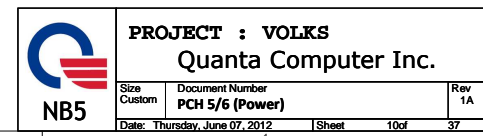
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Rev 1A

Date: Thursday, June 07, 2012

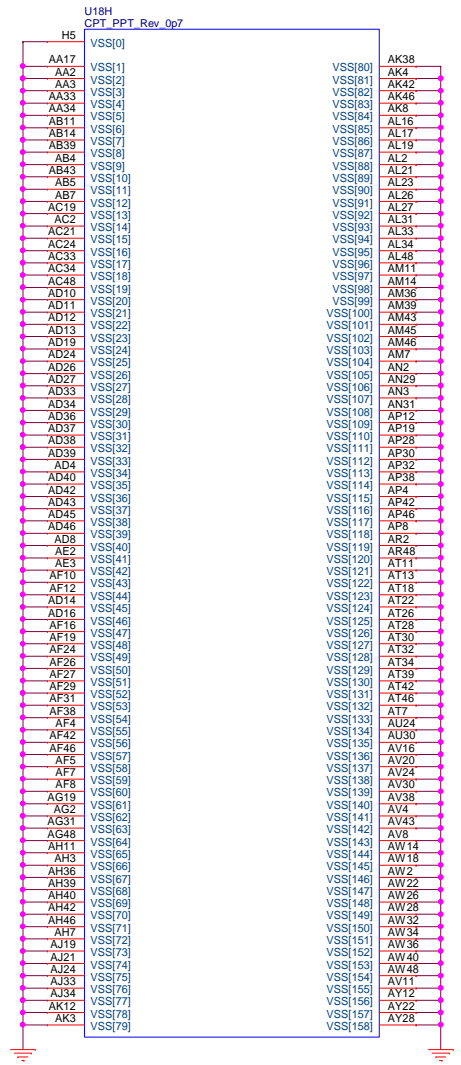
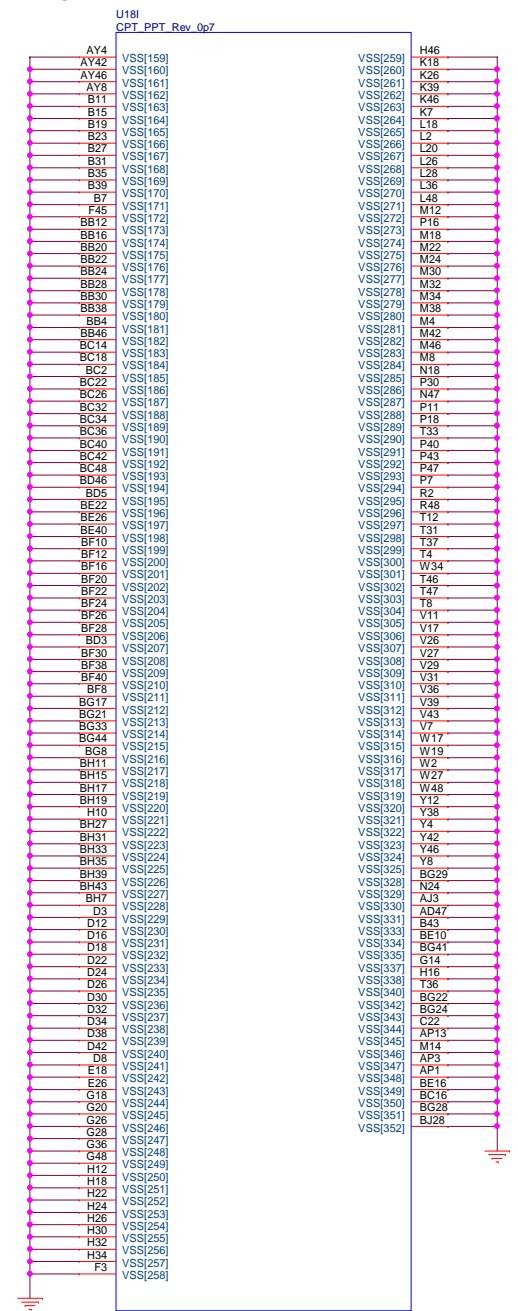
Sheet 9 of 37

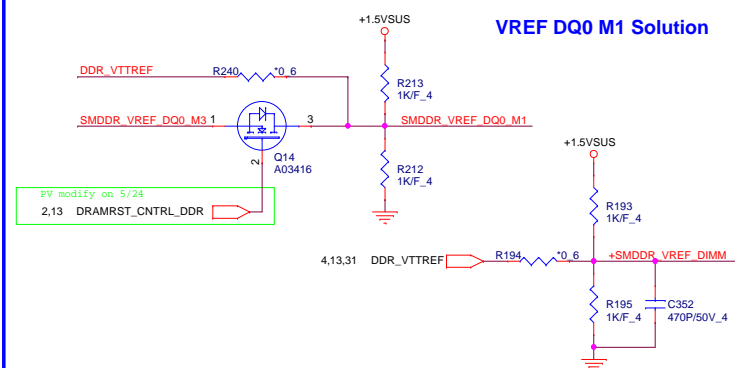
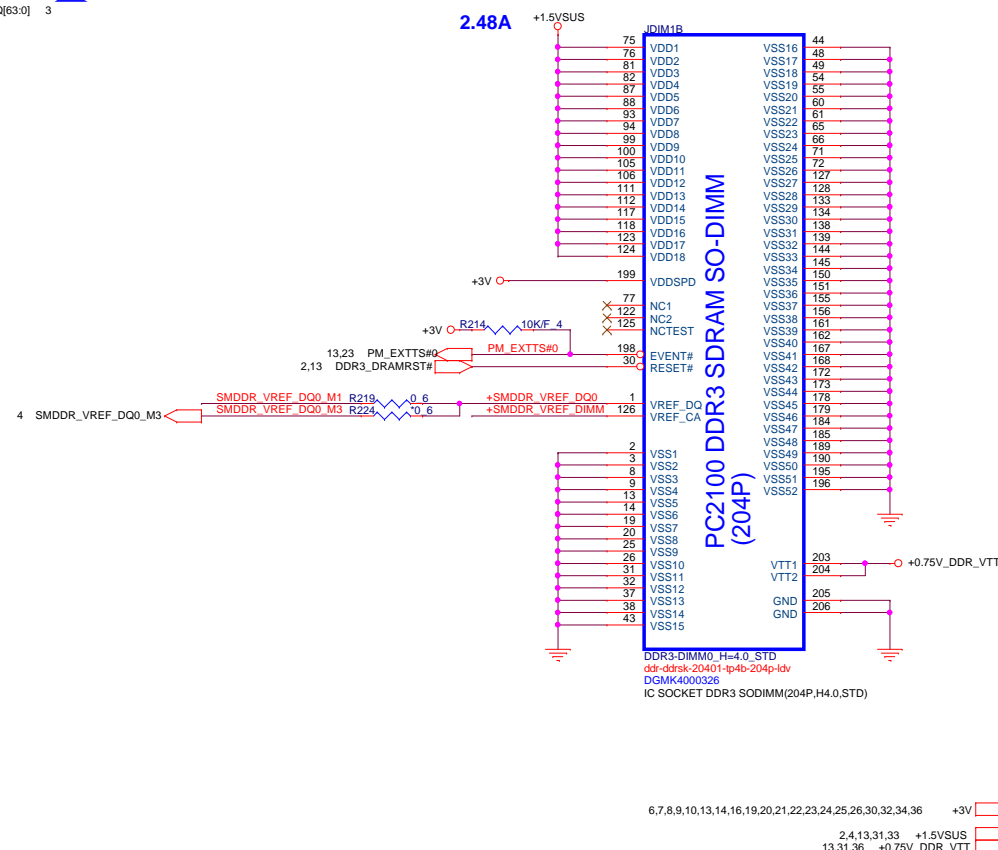
Cougar Point/Panther Point (POWER)

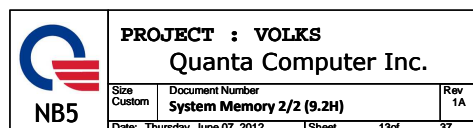


Cougar Point/Panther Point (GND)

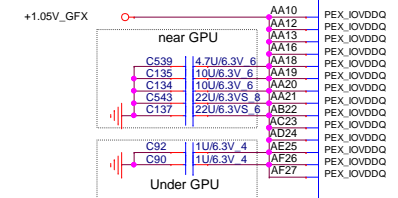
Cougar Point/Panther Point (GND)



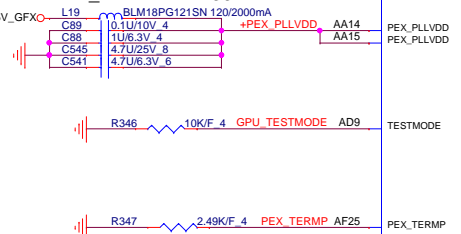
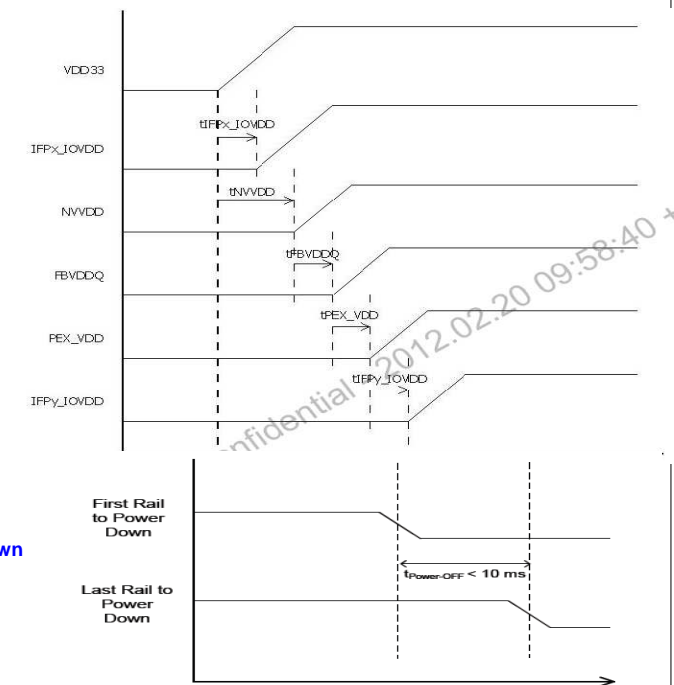
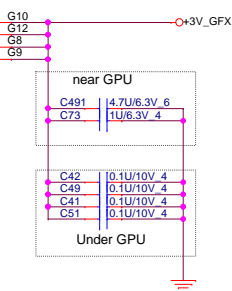
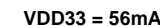
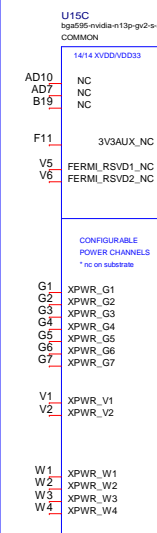
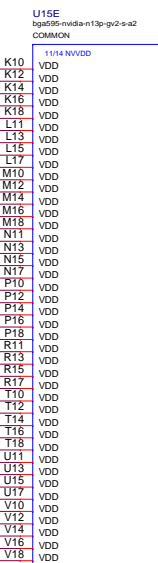
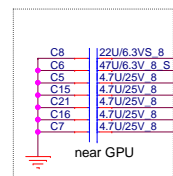
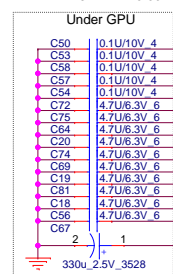
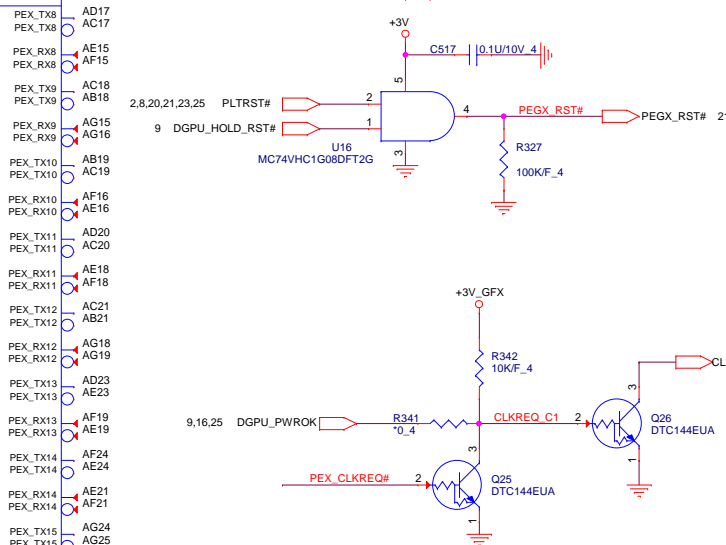
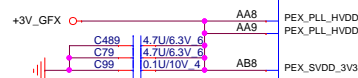




N13P-GV2-S-A2 (GB2-64)
Max point NVCLK = 937.5 , MCLK = 900
TDP point NVCLK = 800 , MCLK = 900

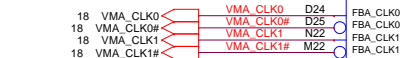
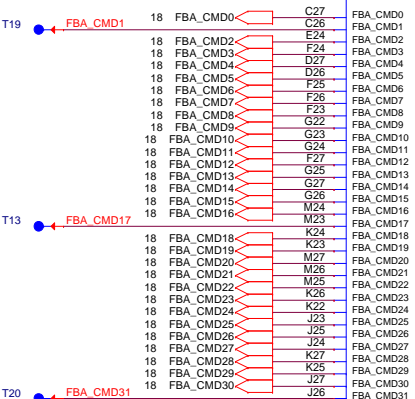
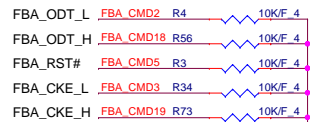


**PEX_PLL_HVDD +
PEX_SVDD 3V3 = 143mA**

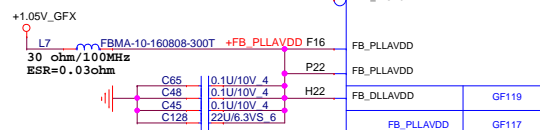


6,10,23,28,30,33,36 +3VS5
16,17,32,33 +3V_GFX
15,16,33 +1.05V_GFX
17,32,33 +VGACORE
23,24,25,26,30,32,34,36 +3V

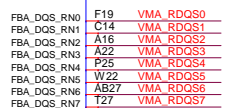
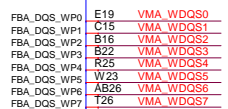
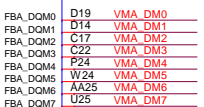
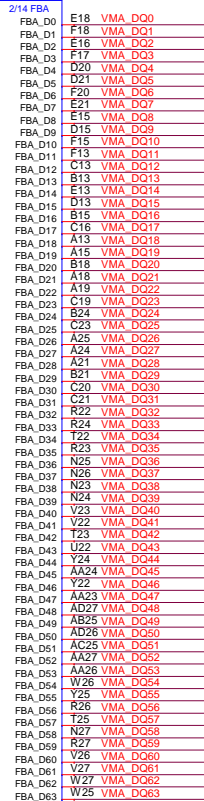
U15B
bga55-mida-n13p-g2-s-a2
COMMON



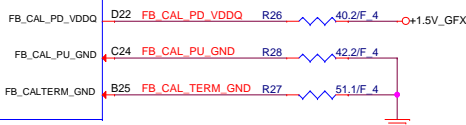
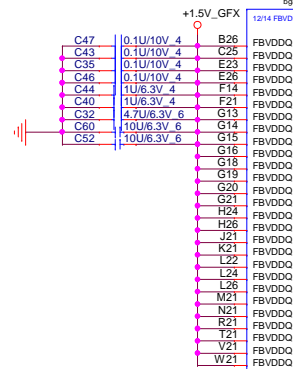
FB_PLLAVDD = 55mA



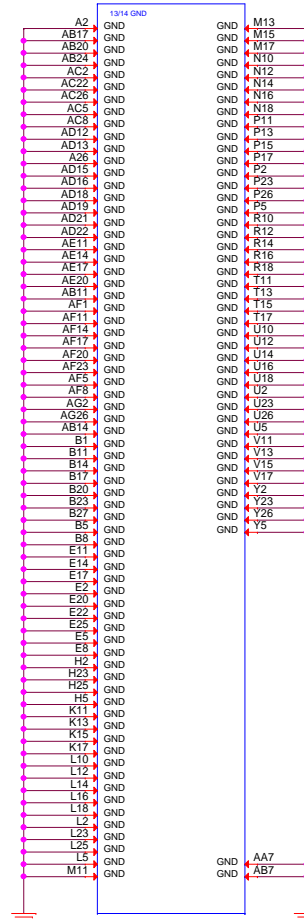
FB_DLLAVDD = 15mA



FBVDDQ + FBVDD = 3.116A

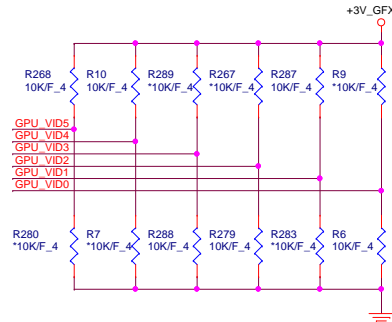


bga55-mida-n13p-g2-s-a2
COMMON U15F

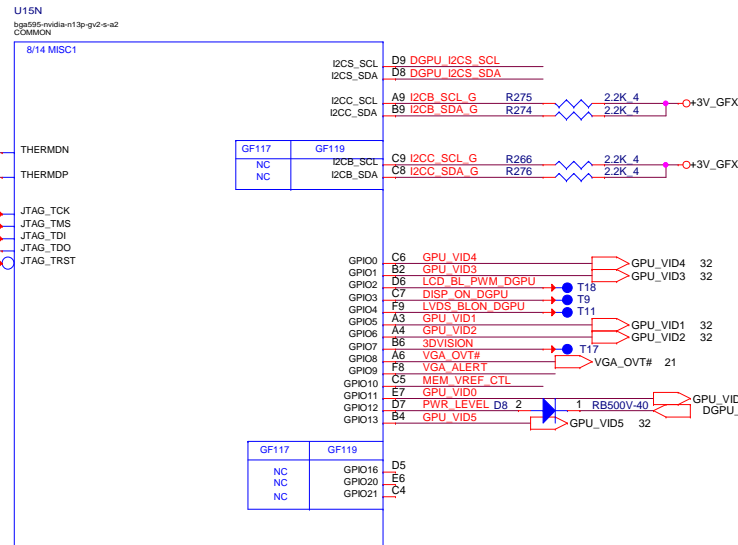
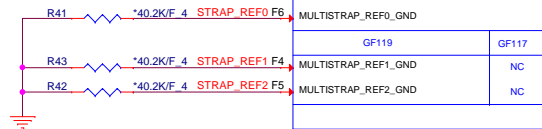


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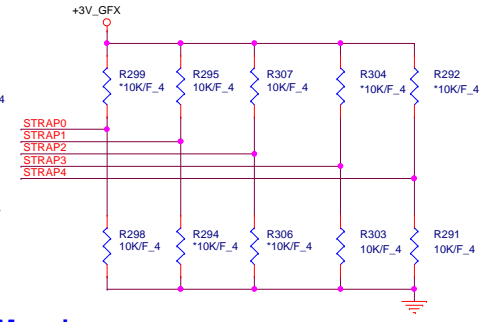
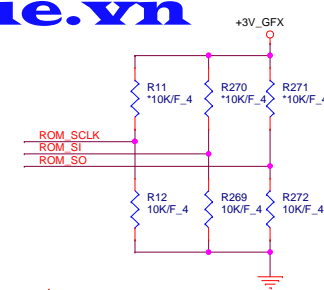
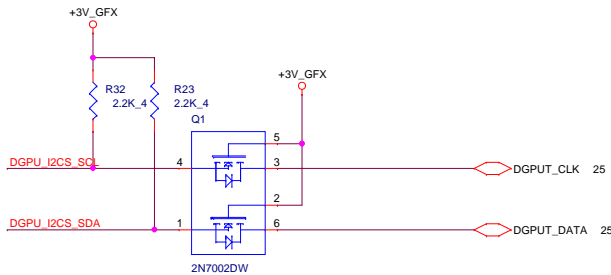
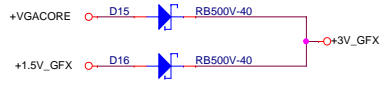
Size	Document Number	Rev
Custom	N11M-GE2(MEMORY/GND)	1A
Date: Thursday, June 07, 2012	Sheet 15 of 37	



N13P-GV2 NVDD HW BOOT Voltage = 0.875V
VID = 0110010



for meet Power down sequence.
Nvidia request for optimus



Binary Strap Mode Mapping

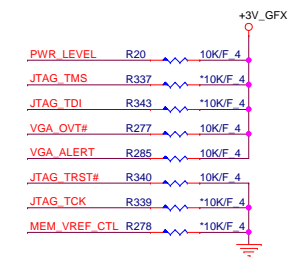
Strap Pin name	Strap Mapping	Resistance	Polarity
ROM_SCL	SMB_ALT_ADDR	10Kohm	Pull-down to GND
ROM_SI	SUB_VENDOR	10Kohm	Pull-UP to 3V3 if VBIOS ROM Exists Pull-down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10Kohm	Pull-down to GND (no dispaly)
STRAP0	RAMCFG[0]	10Kohm	USER defined
STRAP1	RAMCFG[1]	10Kohm	USER defined
STRAP2	RAMCFG[2]	10Kohm	USER defined
STRAP3	RAMCFG[3]	10Kohm	USER defined
STRAP4	PCIE_MAX_SPEED	10Kohm	Pull-down to GND

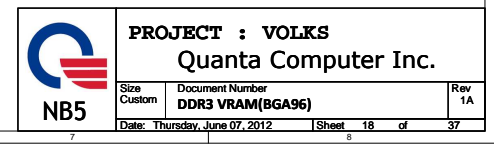
VRAM Configuration Table

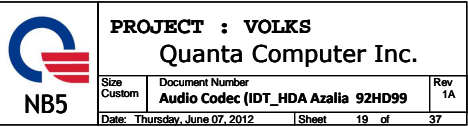
RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	QBCON P/N	HP P/N
0001 0101 1100 1001	(MP) DDR3 256Mx16x4, 64bit, 2Gb,900MHz DDR3 256Mx16x4, 64bit, 2Gb,900MHz DDR3 128Mx16x4, 64bit, 1Gb,900MHz DDR3 128Mx16x4, 64bit, 1Gb,900MHz	Reserved Hynix Micron Hynix Samsung	H5TQ4G63MFR-11C MT41K256M16HA-107G:E H5TQ2G63DFR-11C K4W2G1646C-HC11	AKD5PGWTW00 AKD5PGSTL01 AKD5MGWTW12 AKD5MGWT513	AKD5PGWTW01 AKD5PGSTL02 AKD5MGWTW13 AKD5MGWT508
0001 0100 1011	(OOC) DDR3 256Mx16x4, 64bit, 2Gb,900MHz DDR3 256Mx16x4, 64bit, 2Gb,900MHz DDR3 128Mx16x4, 64bit, 1Gb,900MHz	Samsung Hynix Samsung	K4W4G1646B-HC11 H5TQ4G63AFR-11C K4W2G1646E-BC11	AKD5MGWT518 AKD5MGWT521	AKD5MGWT517 AKD5MGWT522

GB2-64 and GB4-128 GPIO Description

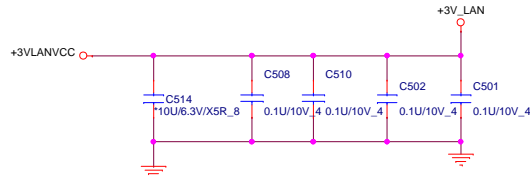
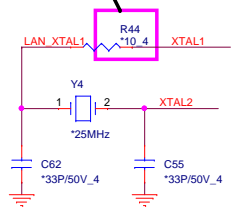
GPIO pin Name	Normal Function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	GPU_VID4	O	GPU Core VDD VID4	Strap to boot NVVDD
GPIO1	GPU_VID3	O	GPU Core VDD VID3	Strap to boot NVVDD
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control	100 K pull-down
GPIO3	LCD_VCC or PSI	O	Panel Power Enable or Phase Shedding	LCD_VCC: 100K pull-down PSI: 10K pull-up or pull-down; stuff as needed to disable phase shedding by default
GPIO4	LCD_BLEN	O	Panel Backlight Enable	100 K pull-down
GPIO5	GPU_VID1	O	GPU Core VDD VID1	Strap to boot NVVDD
GPIO6	GPU_VID2	O	GPU Core VDD VID2	Strap to boot NVVDD
GPIO7	3Dvision	O	3D Vision Left/Right signal	100 K pull-down
GPIO8	OVERT	I/O	Active Low Thermal Catastrophic Over Temperature	100 K pull-up
GPIO9	ALERT	I/O	Active Low Thermal Alert	100 K pull-up
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 K pull-down
GPIO11	GPU_VID0	O	GPU Core VDD VID0	Strap to boot NVVDD
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100 K pull-up
GPIO13	GPU_VID5	O	GPU Core VDD VID5	Strap to boot NVVDD
GPIO14	HPD_AB	I	Hot Plug Detect for IFPA	See Figure 76
GPIO15	HPD_C	I	Hot Plug Detect for IFPC	See Figure 76
GPIO16	PSI or MEM_VDD_CTL	O	Phase Shedding or Memory VDD VID	PSI: 10K pull-up or pull-down; stuff as needed to disable phase shedding by default MEM_VDD_CTL: Strap to boot FBVDD/Q
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	See Figure 76
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	See Figure 76
GPIO19	HPD_F	I	Hot Plug Detect for IFPF	See Figure 76
GPIO20	Reserved			
GPIO21	Reserved			





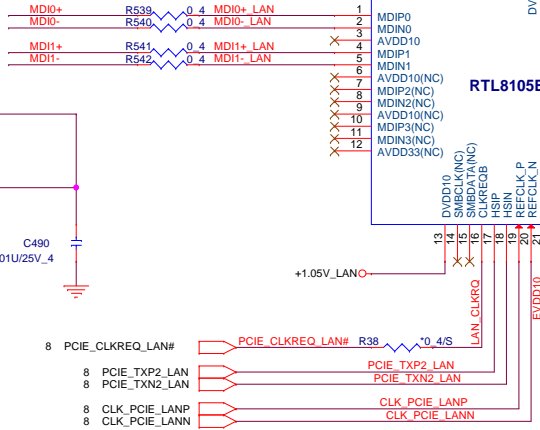
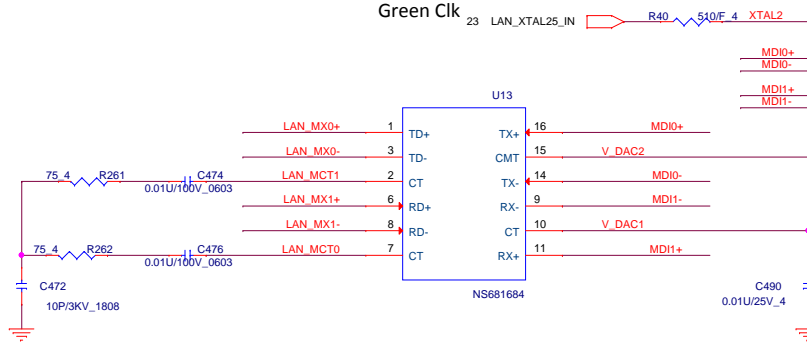


For EMI 0 ~ 22 ohm

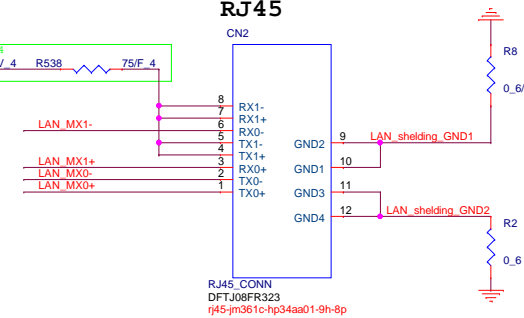
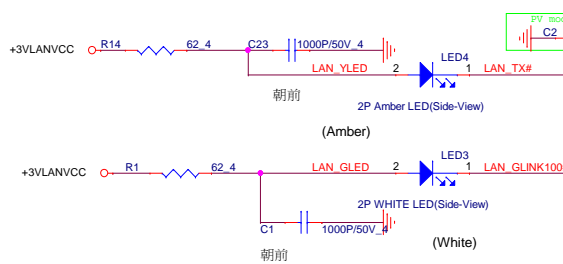
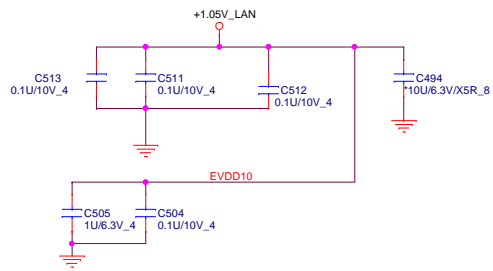
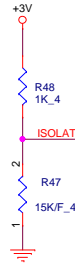


GND VIA x 9 Pcs

Green Clk

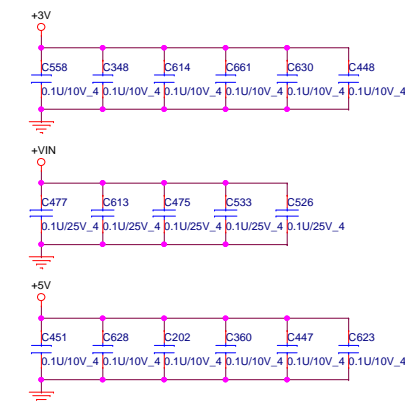
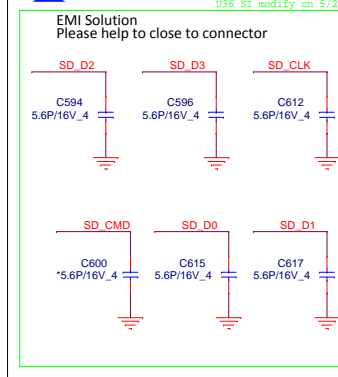
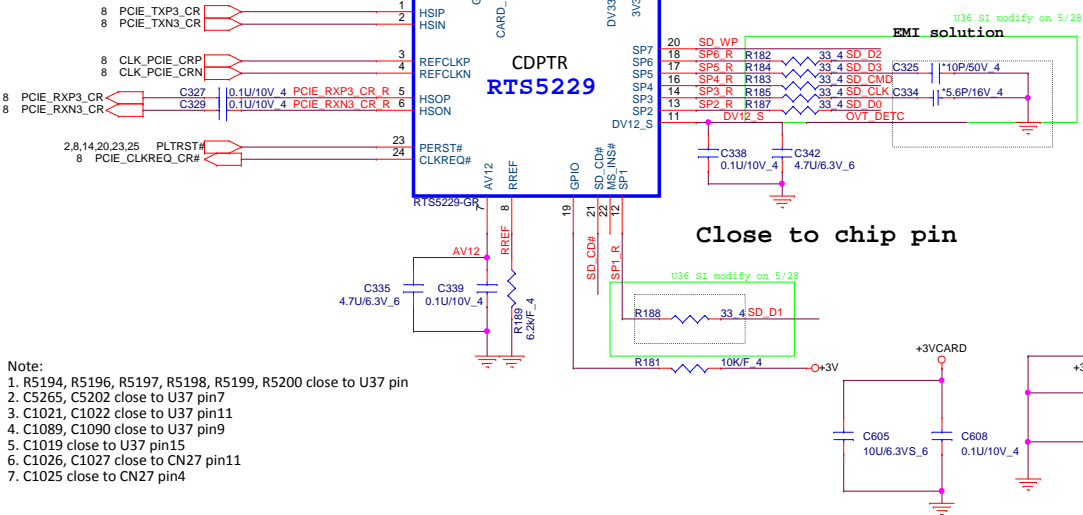


if ISOLATEB pin pull-low, the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

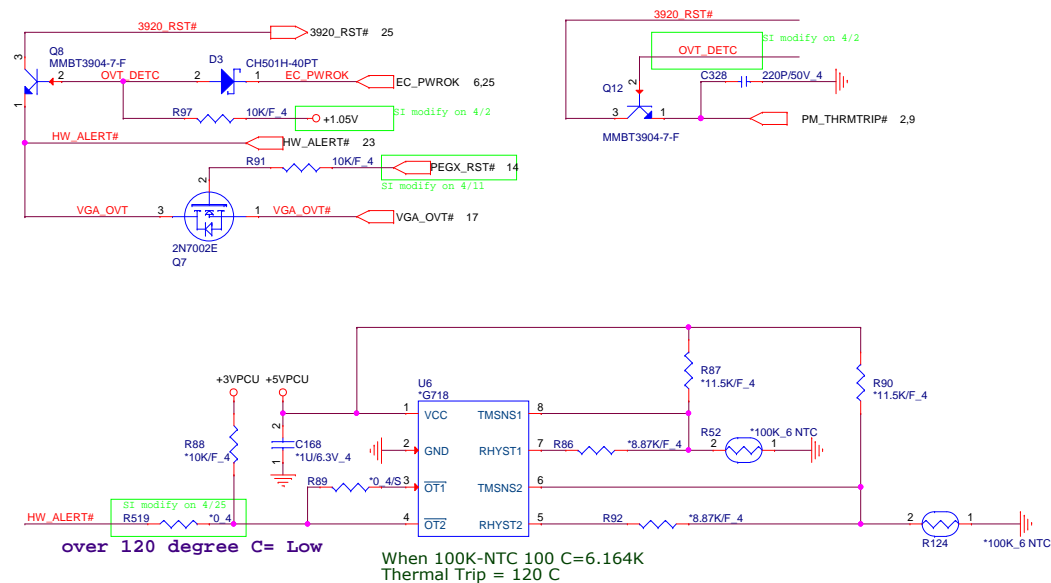


CARD READER

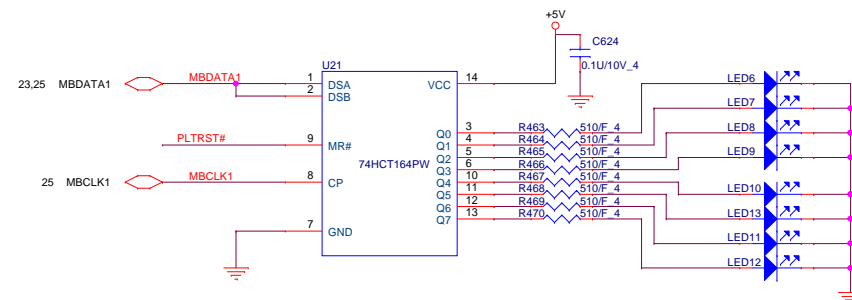
SD / MMC

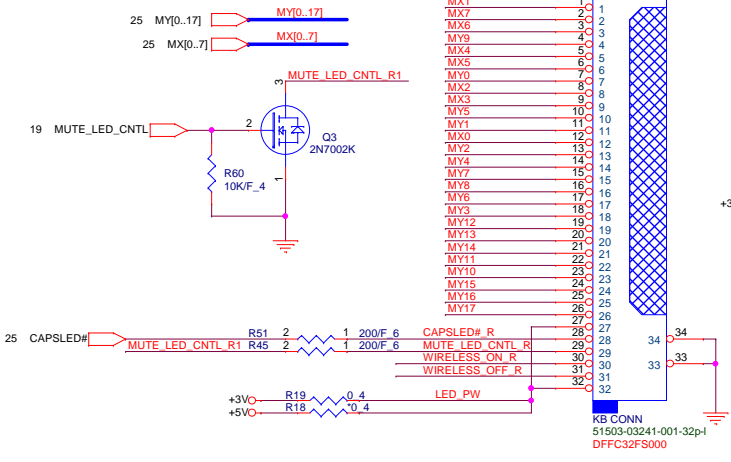


Thermal HW protect

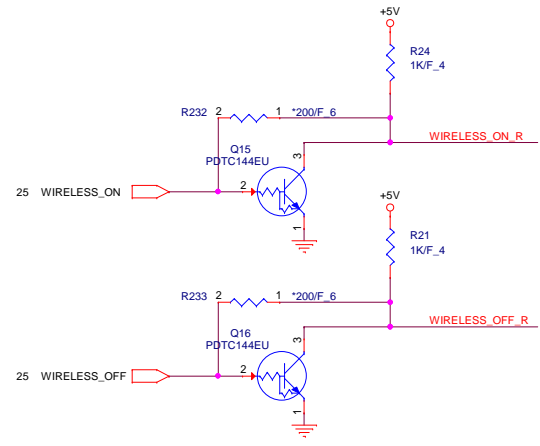
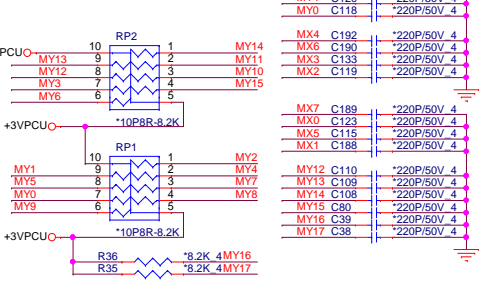


80 port

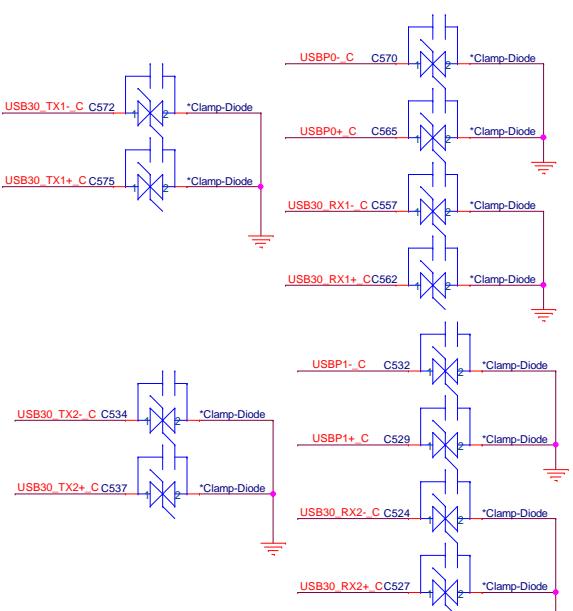




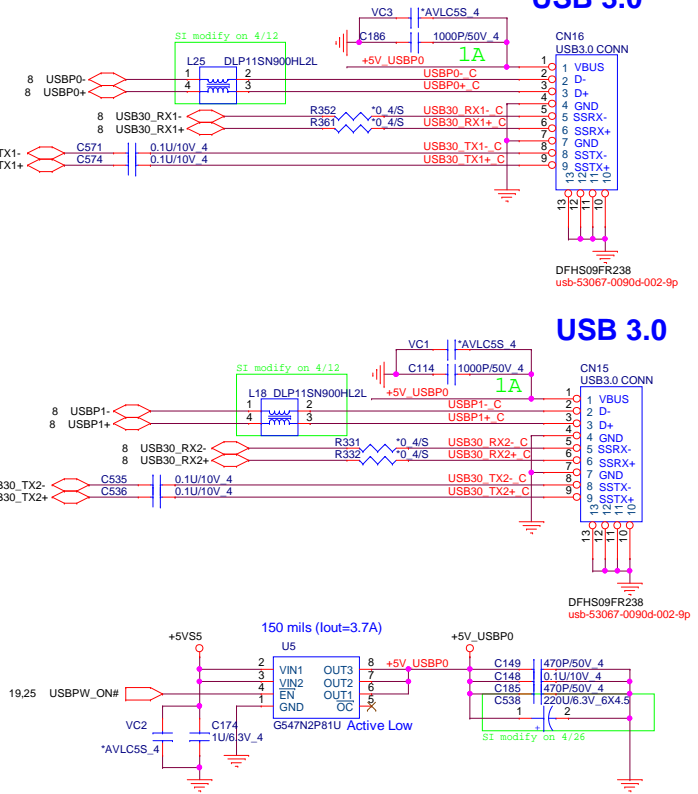
KEYBOARD PULL-UP



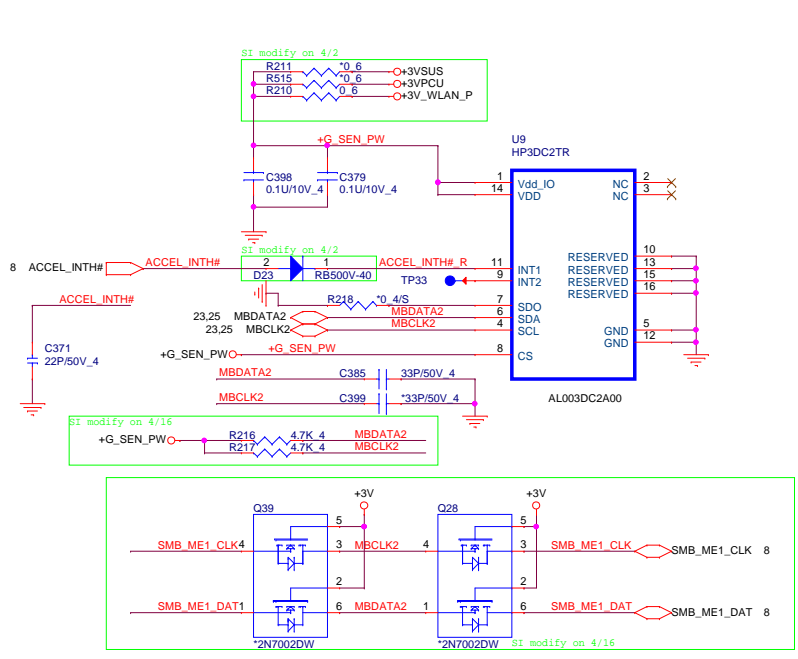
USB 2.0/3.0 Combo



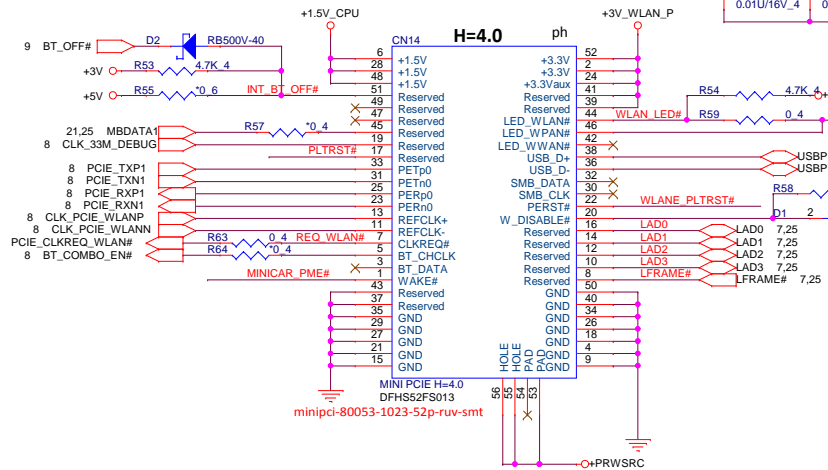
USB 3.0



Accelerometer Sensor

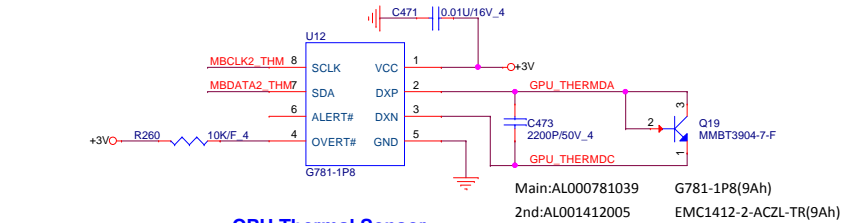


Mini Card WLAN/BT(Optional)

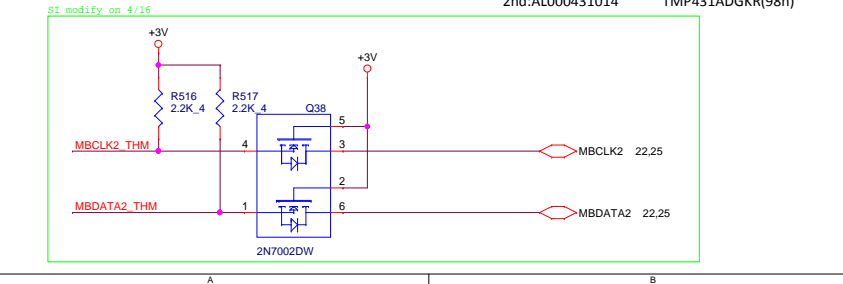
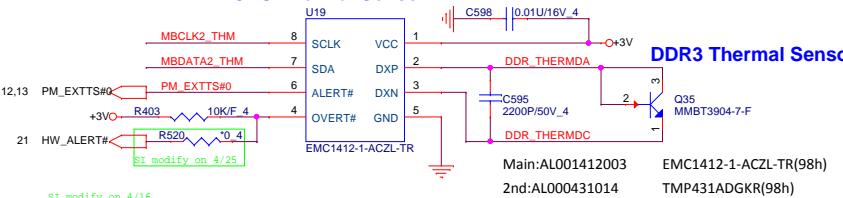


Local Thermal Sensor

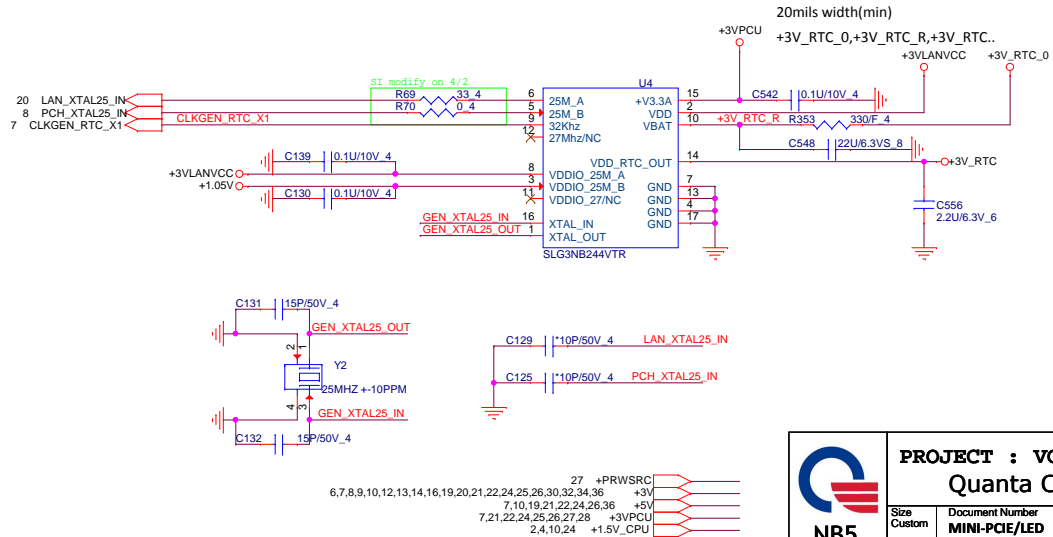
GPU Thermal Sensor



CPU Thermal Sensor



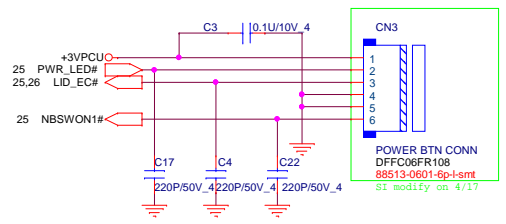
Green CLK Circuitry



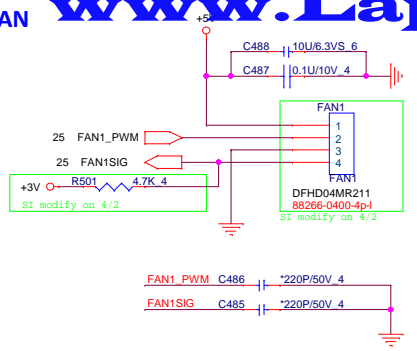
	PROJECT : VOLKS	
	Quanta Computer Inc.	
Size	Document Number	Rev
Custom	MINI-PCIE/LED	1A
Date: Thursday, June 07, 2012		Sheet 23 of 37

Power Button Connector

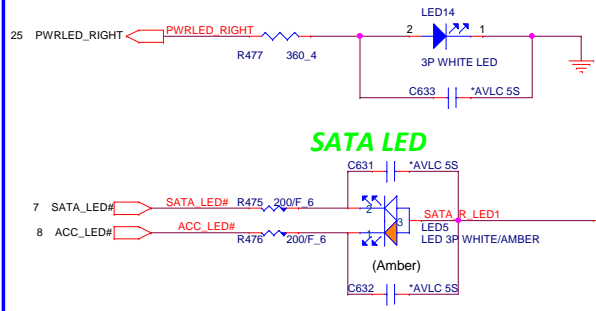
Pin1 : +3VPCU(LIDSWITCH PWR)
Pin2 : POWER LED
Pin3 : LIDSWITCH
Pin4 : GND
Pin5 : GND
Pin6 : POWERON#



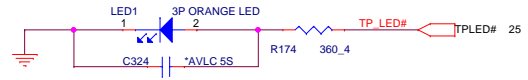
FAN



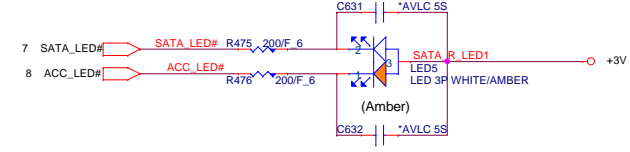
PWR LED



14" TP LED

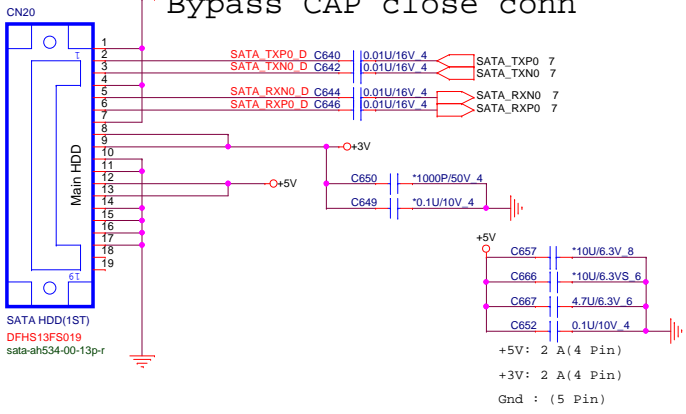


SATA LED

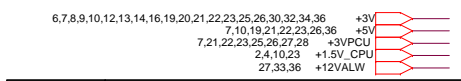
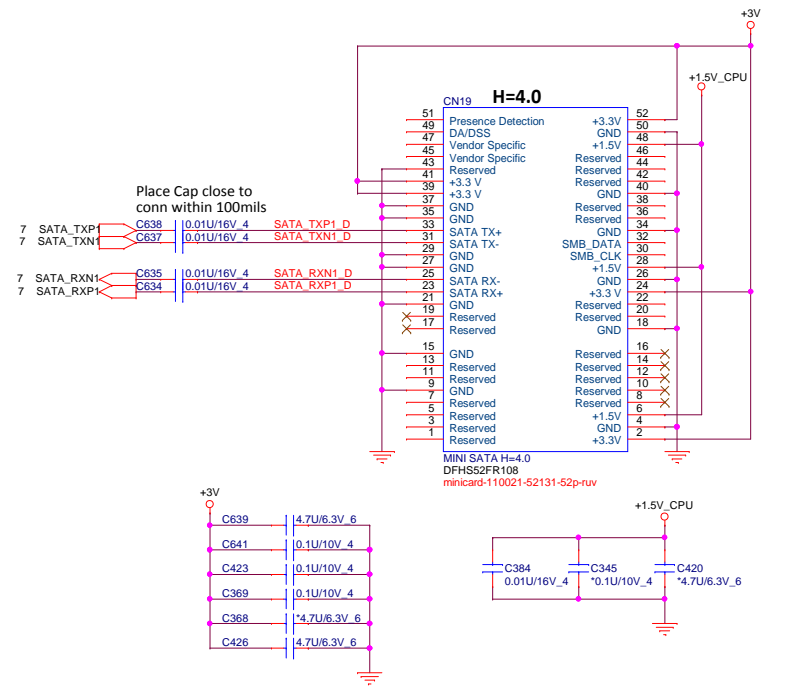


SATA HDD Connector(Cable type)

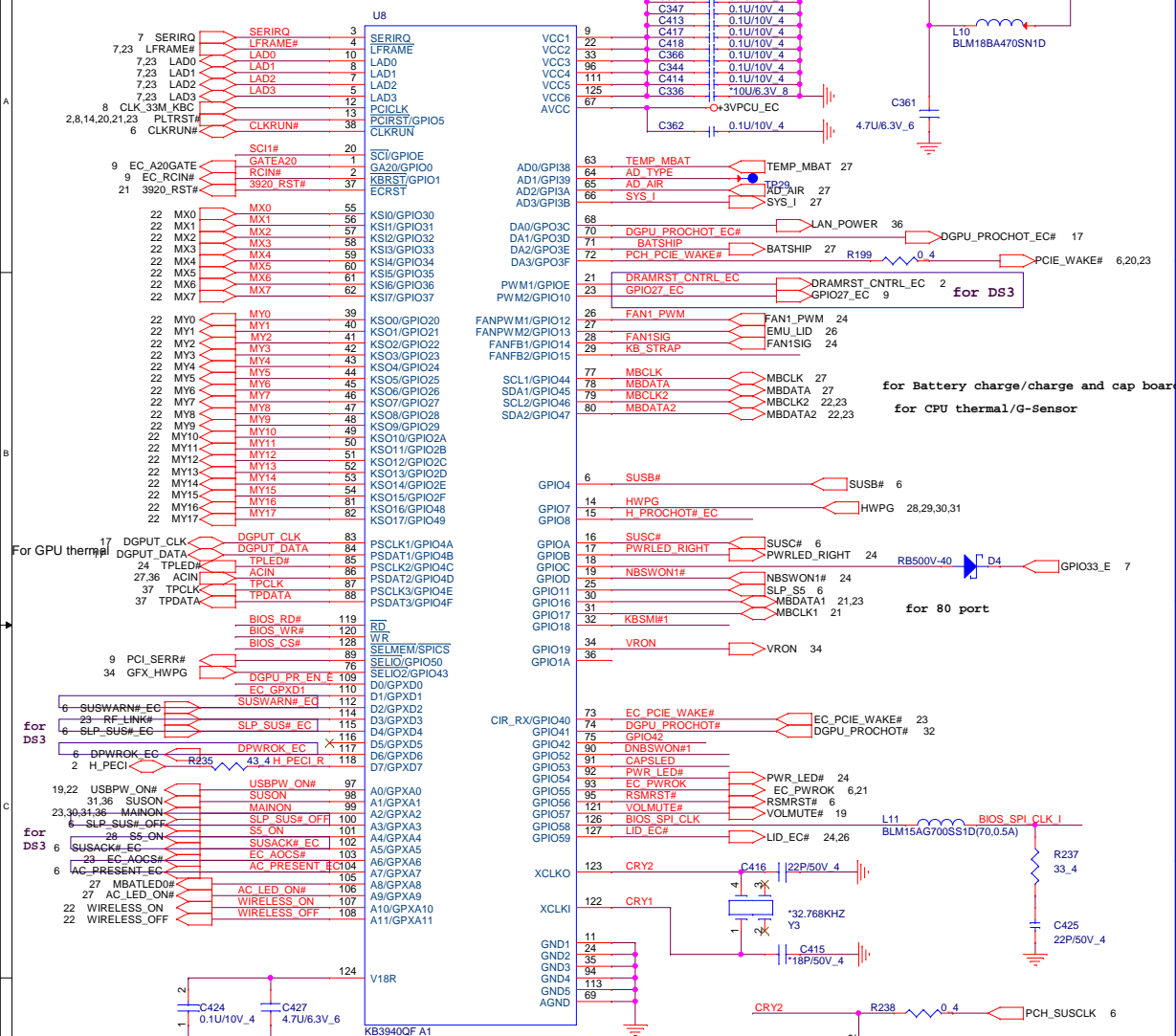
Bypass CAP close conn



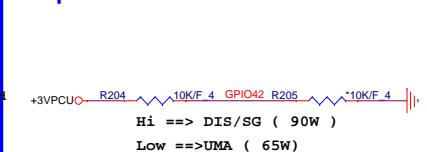
Mini PCI-E Card 2- Full size mSATA



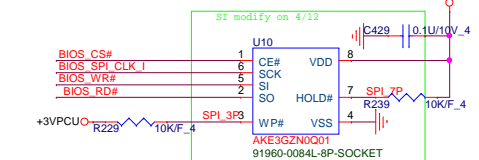
NB5		PROJECT : VOLKS	
		Quanta Computer Inc.	
Size Custom	Document Number	SATA HDD/ODD/MSATA CONN	
Date: Thursday, June 07, 2012	Sheet	24 of	37



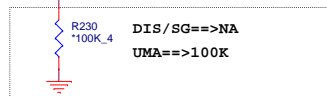
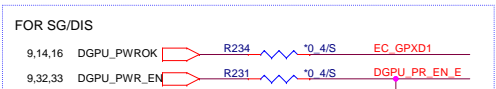
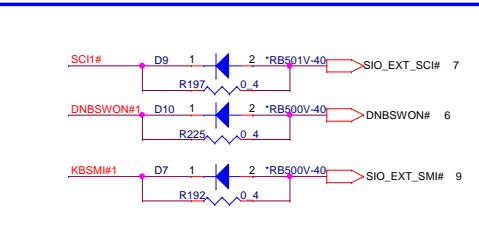
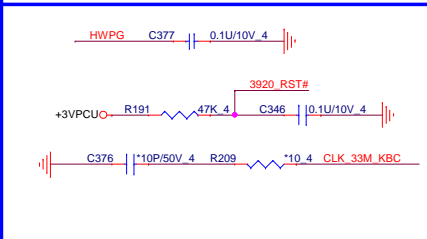
Adapter select for EC



Vender	Size	P/N
EON	1MB	AKE3G2N0Q01 (EON EN25Q80A-100HIP)
MX	1MB	AKE3GFP0Z00 (MX25L8006EM2I-12G)
AMIC	1MB	AKE3GZP0801 (A25L080M-F)
Socket		DFHS08FS023



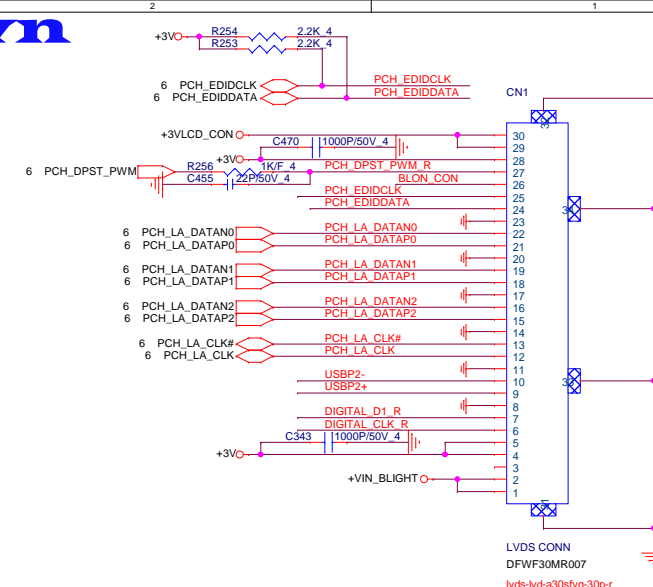
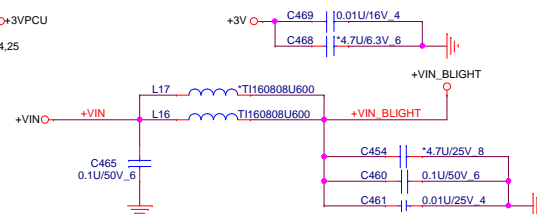
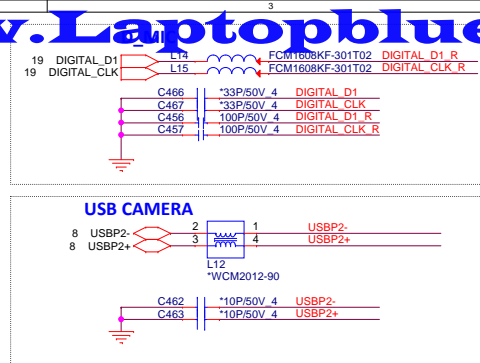
Reserve for ENE Hold time issue		
MBCLK2	C381	*10P/50V_4
MBDATA2	C380	*10P/50V_4
MBCLK	C373	*10P/50V_4
MBDATA	C375	*10P/50V_4
DGPU_CLK	C389	*10P/50V_4
DGPU_DATA	C388	*10P/50V_4



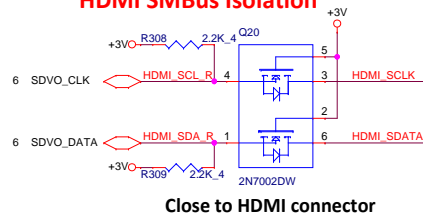
2,4,6,7,8,10,21,23,30,33,34
6,7,8,9,10,12,13,14,16,19,20,21,22,23,24,26,30,32,34,36
7,21,22,23,24,26,27,28

4 3

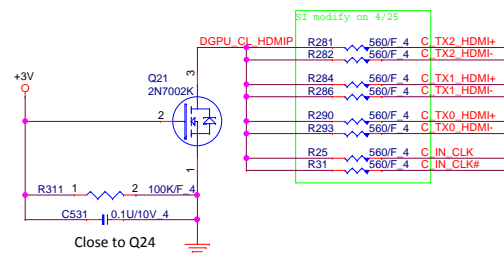
www.Laptopblue.vn



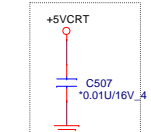
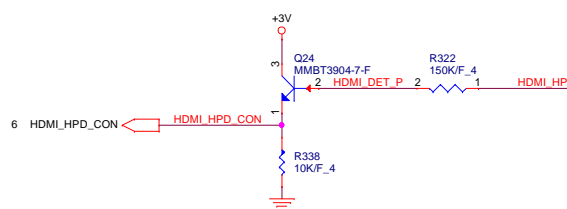
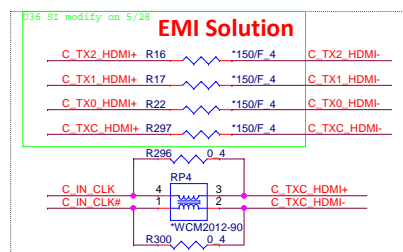
HDMI SMBus Isolation



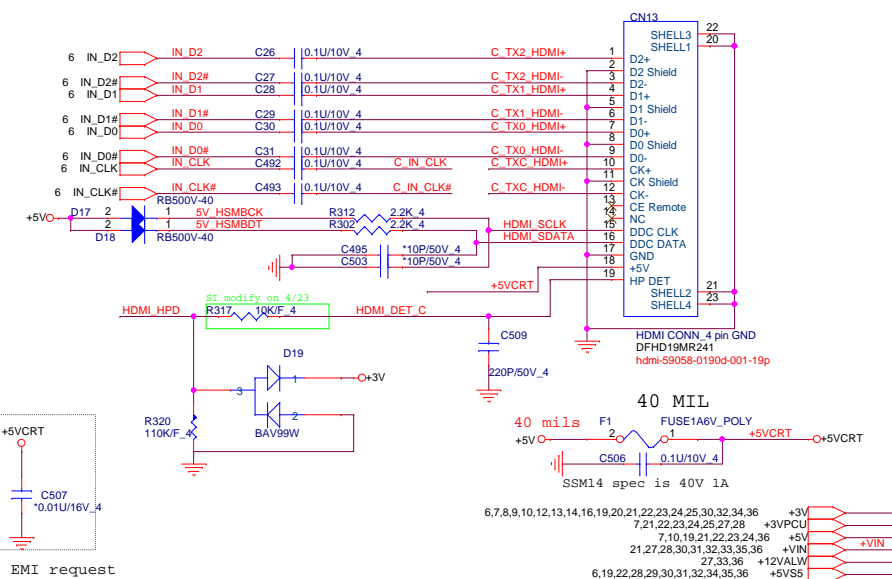
Close to HDMI connector

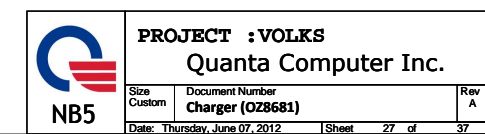


Close to Q24



for EMI request



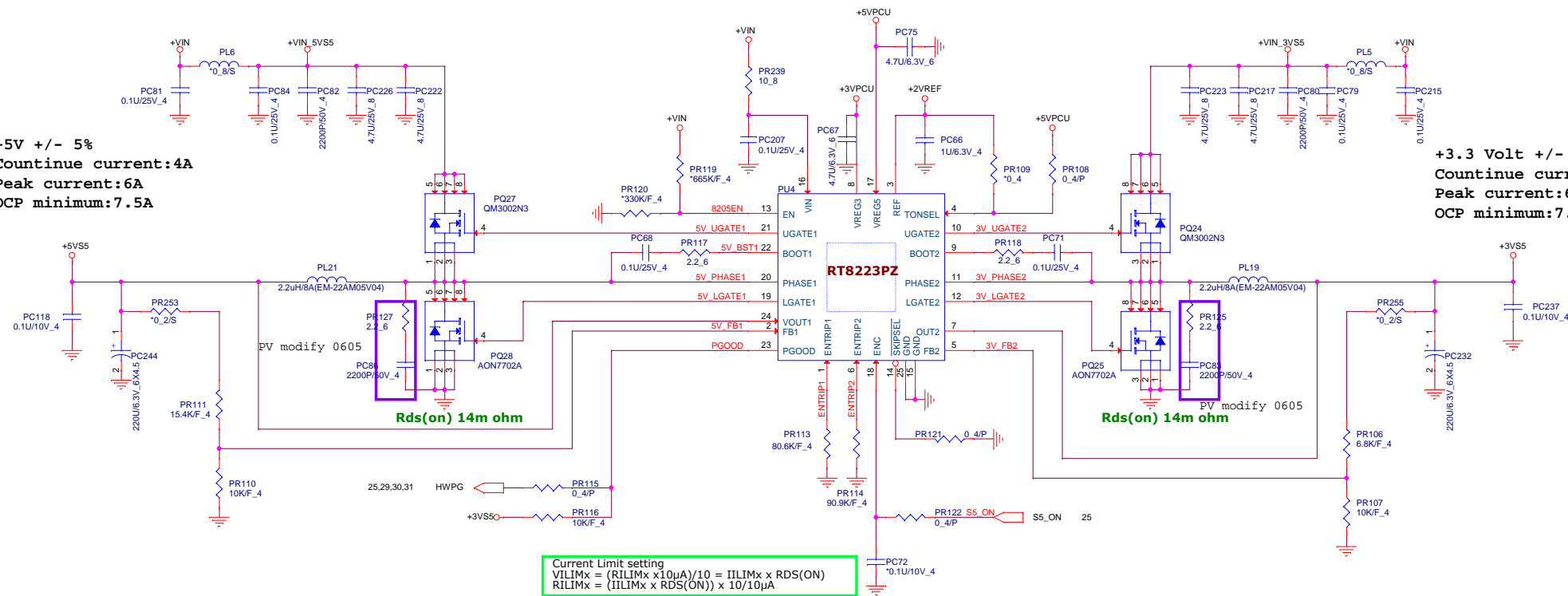


+5V +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A


+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

Current Limit setting
 $VILIMx = (RILIMx \times 10\mu A) / 10 = IILIMx \times RDS(ON)$
 $RILIMx = (IILIMx \times RDS(ON)) \times 10 / 10\mu A$

TONSEL= VREG5
 Vout1=400kHz/Vout2=500kHz



21,26,27,30,31,32,33,35,36 +VIN
 6,10,23,30,33,36 +3VS5
 7,21,22,23,24,25,26,27 +5VSS
 +3VPCU

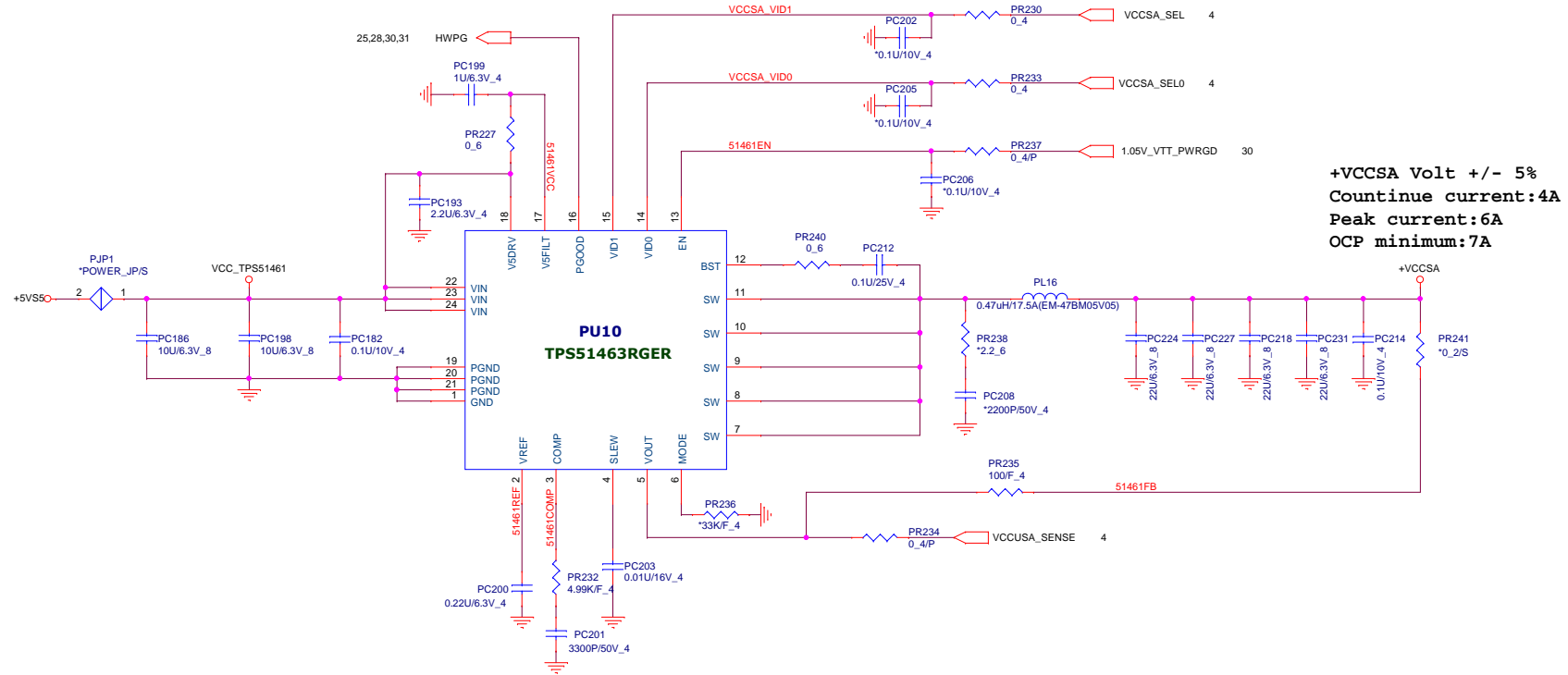
	PROJECT :VOLKS		
	Quanta Computer Inc.		
	Size	Document Number	Rev
	Custom	3/5VSS (RT8223P)	A
Date: Thursday, June 07, 2012 Sheet 28 of 37			

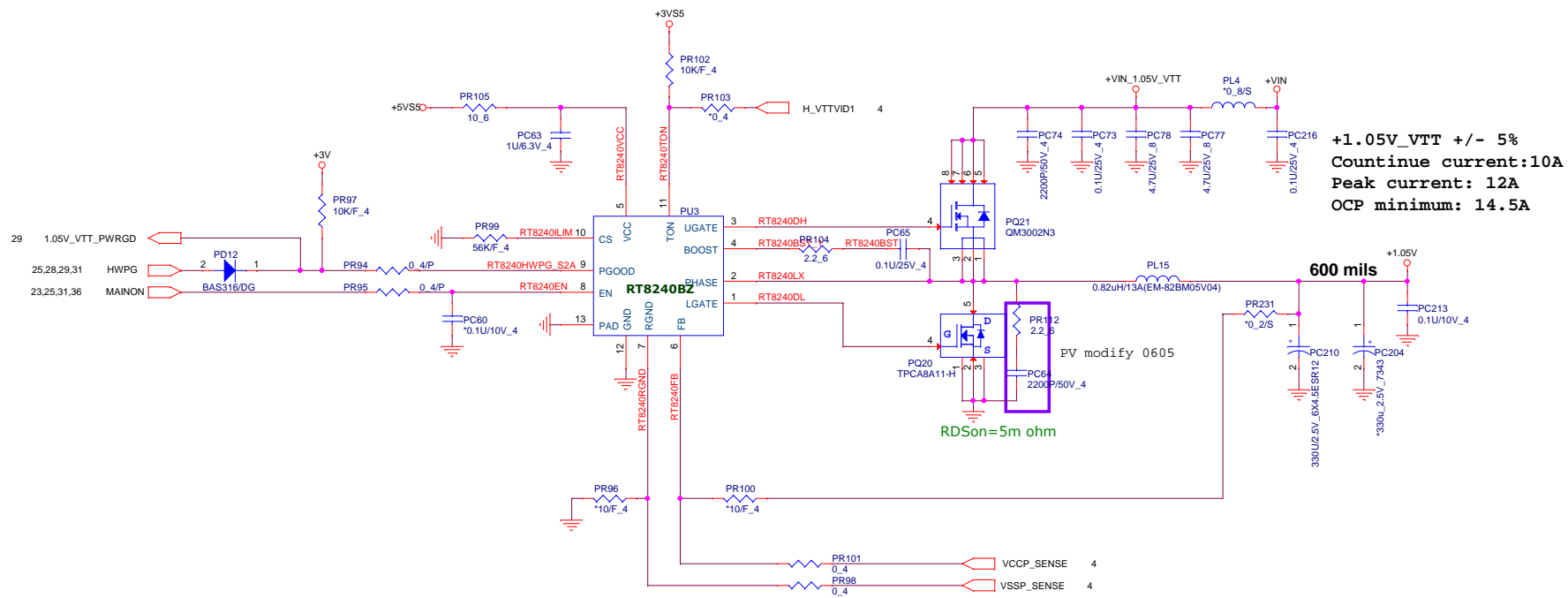
TPS51462RGER/AL051462000
For CPU SV system agent
voltage slew rate of 0.5 -10 mV/μs

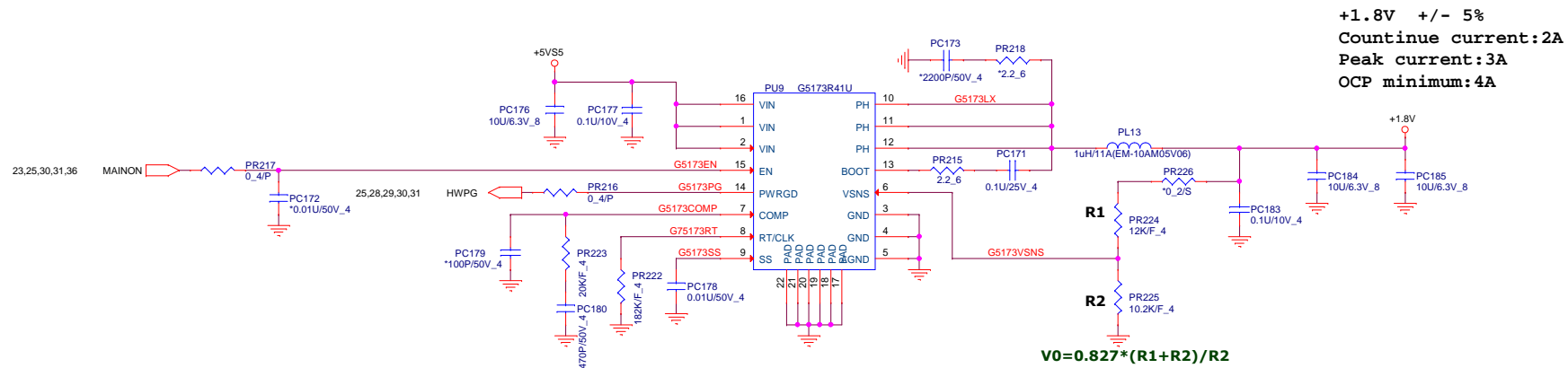
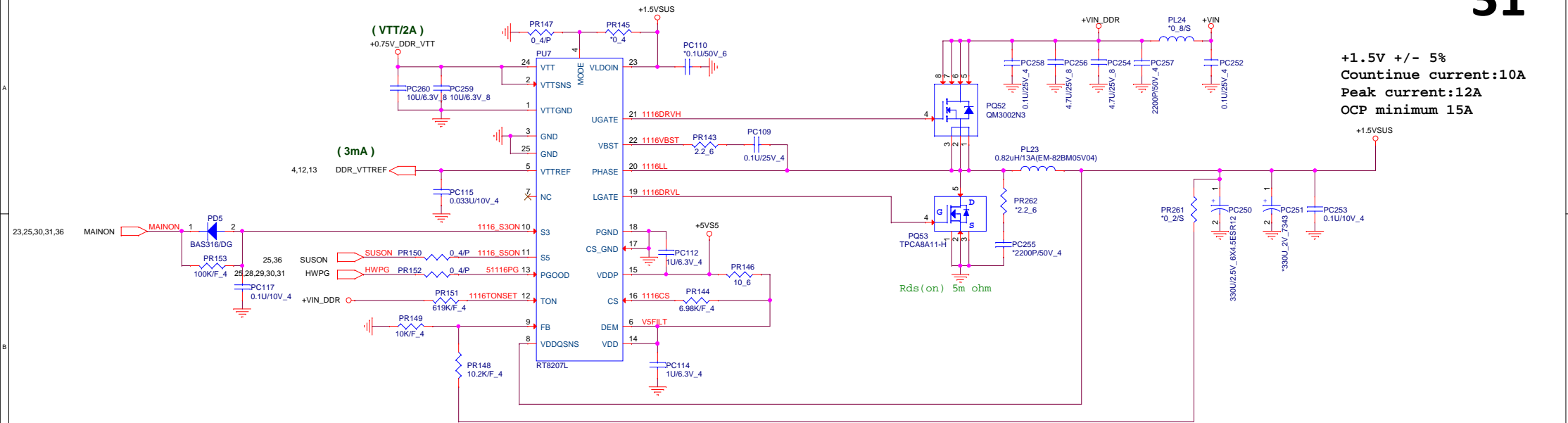
SEL0	SEL1	+VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

TPS51463RGER/AL051463000
For CPU ULV system agent
voltage slew rate of 0.5 -10 mV/μs

SEL0	SEL1	+VCCSA
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V



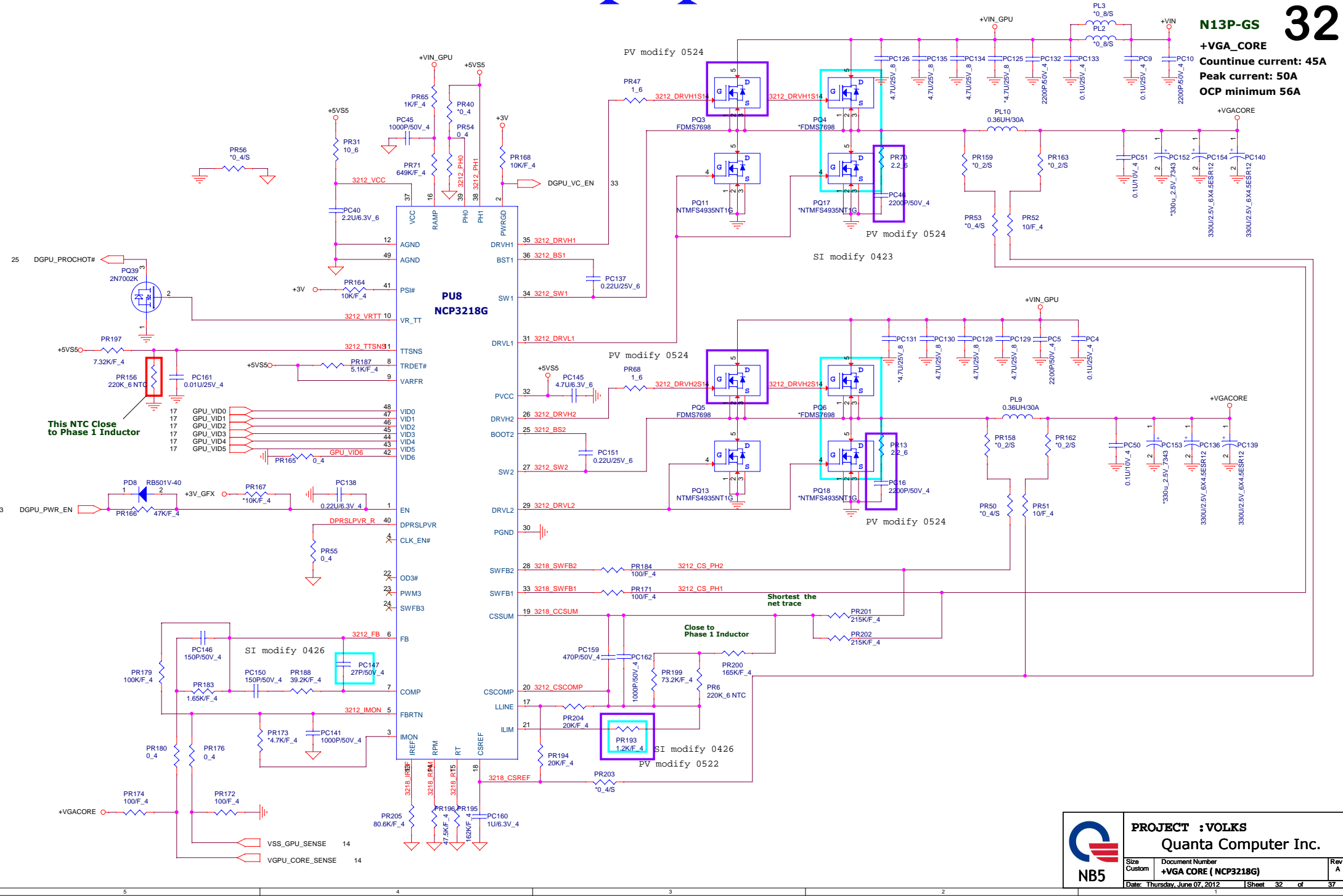




N13P-GS

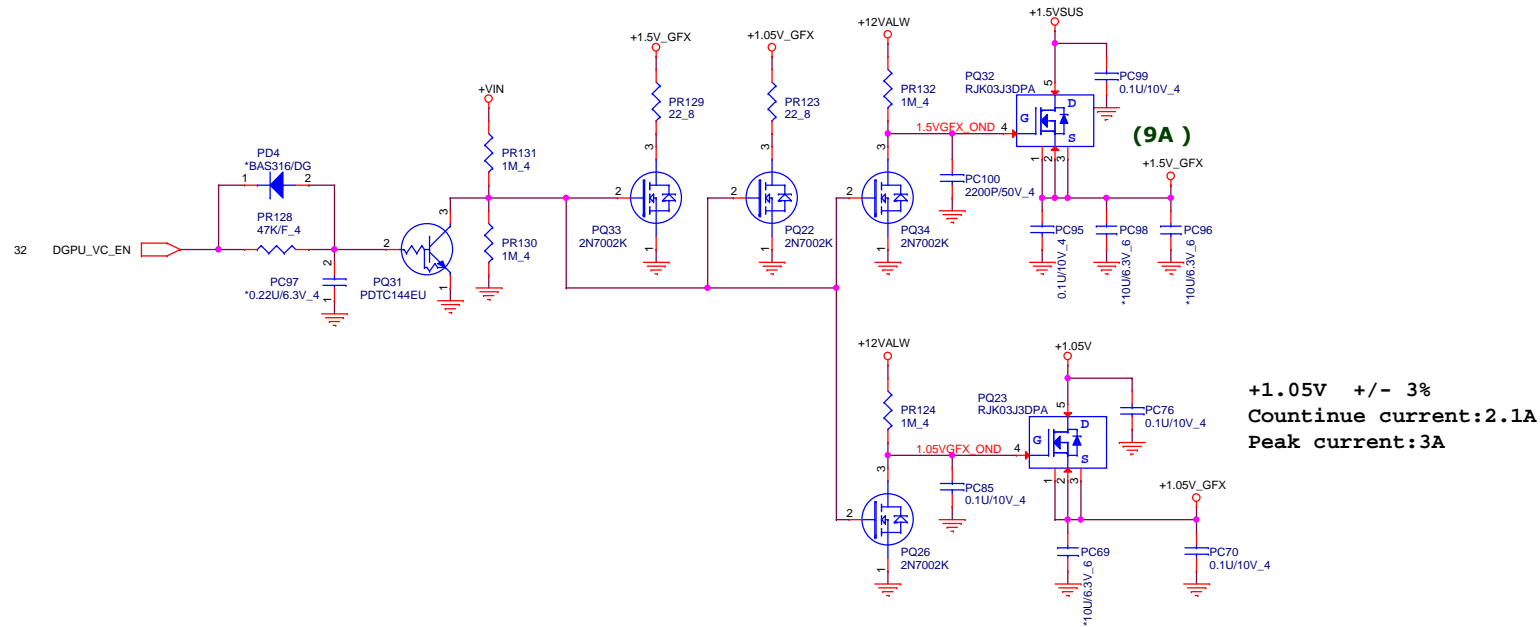
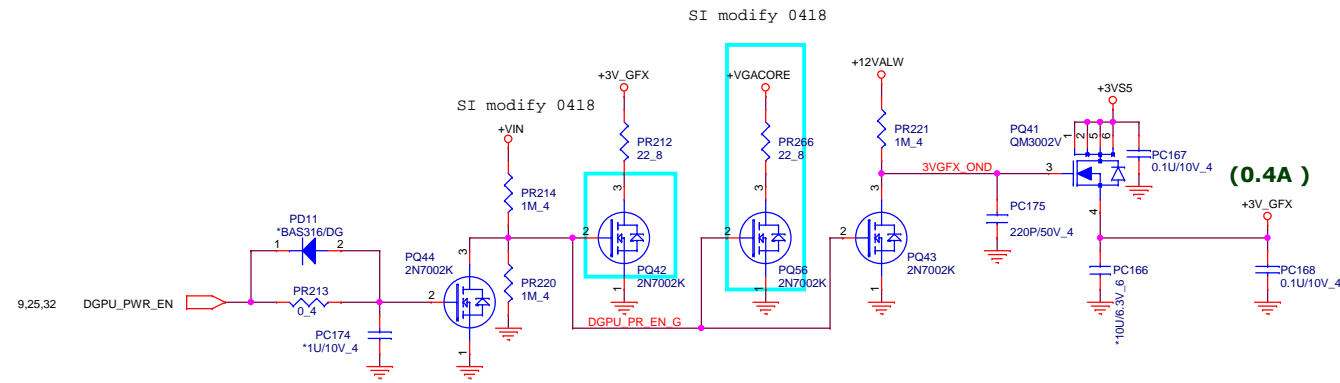
+VGA_CORE

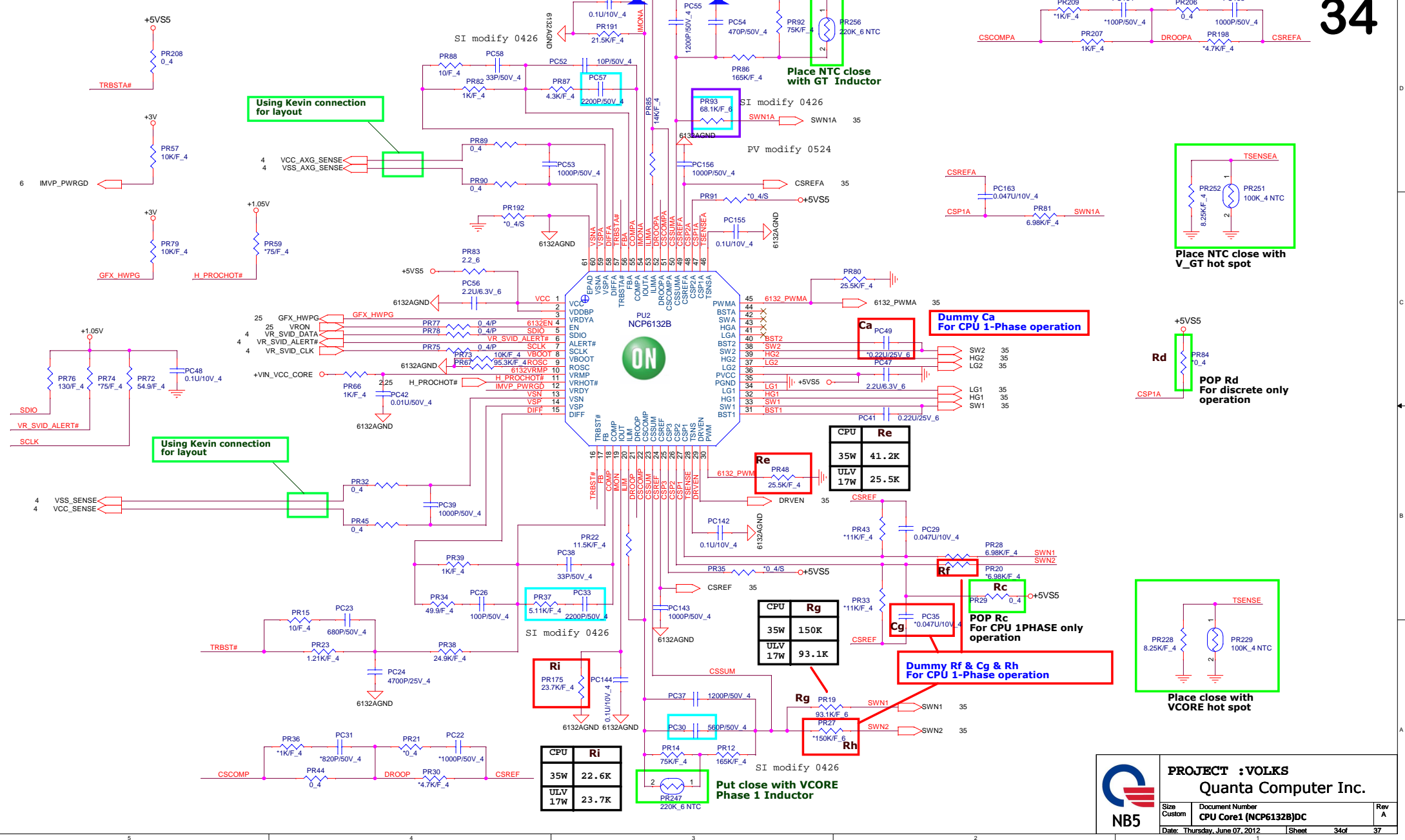
Countinue current: 45A
Peak current: 50A
OCP minimum 56A

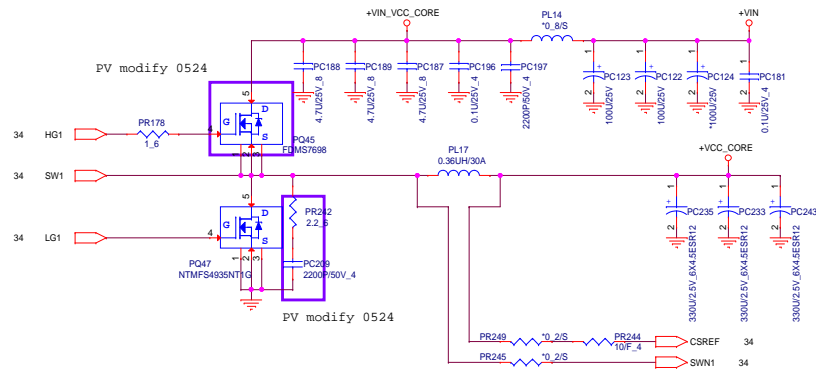


VGA

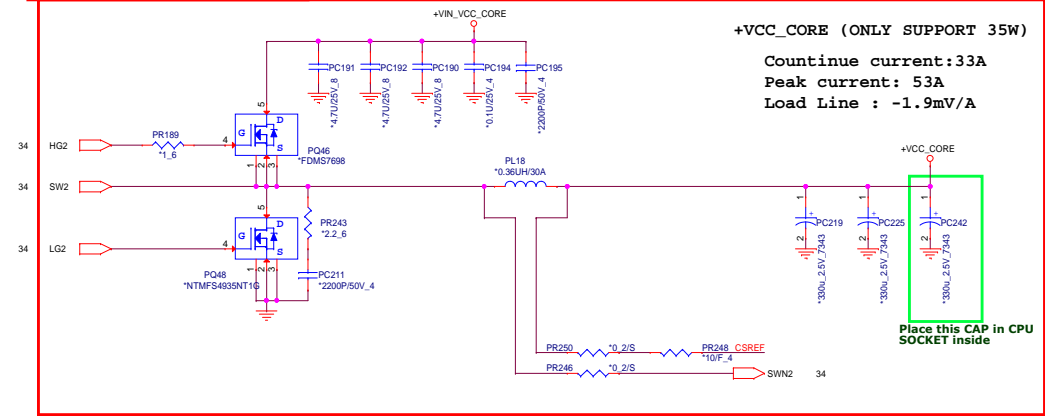
2,4,12,13,31	+1.5VSUS
6,10,23,28,30,36	+3VSS
14,16,17,32	+3V_GFX
15,16,17,18	+1.5V_GFX
14,15,16	+1.05V_GFX
27,36	+12VALW
2,4,6,7,8,10,21,23,30,34	+1.05V







Dummy This Schematic
For CPU 1-Phase operation

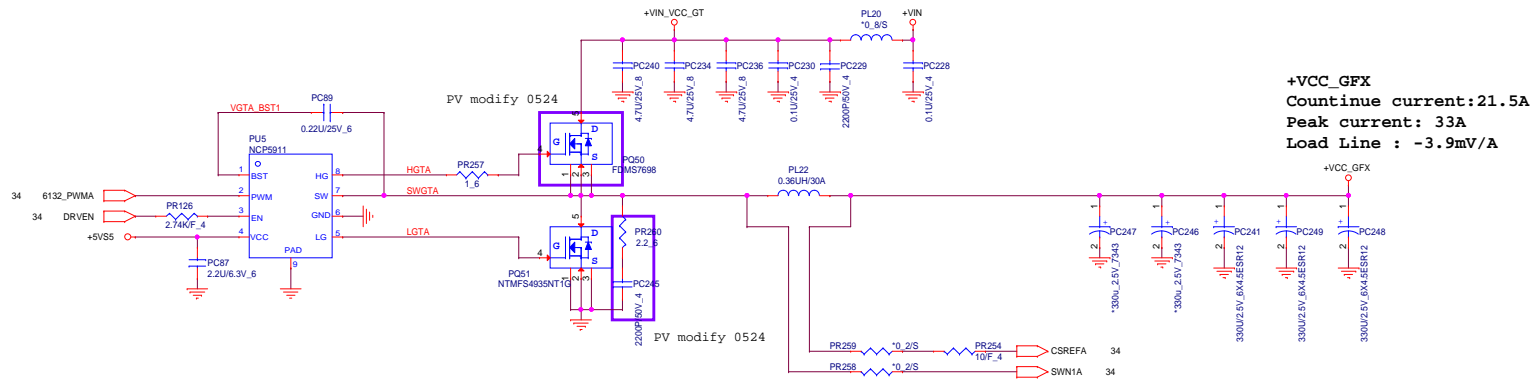


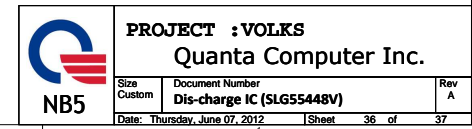
+VCC_CORE (ONLY SUPPORT 35W)

Countinue current:32A
Peak current: 53A
Load Line : -1.9mV/A

+VCC_CORE (ULV 17W)

Countinue current:16A
Peak current: 33A
Load Line : -2.9mV/A





+PRWSRC	C713	0.1U/25V 4
+PRWSRC	C714	0.1U/25V 4
+VIN	C715	0.1U/25V 4
+VIN	C716	0.1U/25V 4
+VIN	C717	0.1U/25V 4
+VIN	C710	150P/50V 4
+VIN	C711	150P/50V 4
+VIN	C712	150P/50V 4
BATT+	C718	0.1U/25V 4
BATT+	C719	0.1U/25V 4
BATT+	C720	150P/50V 4
BATT+	C721	150P/50V 4

