

Page	Title of Schematics Page	Rev.	Date	Page	Title of Schematics Page	Rev.	Date
01	Schematics Page Index	PV	10'11'22	36	VGA (PCI-E) 1/6	PV	10'11'22
02	Block Diagram	PV	10'11'22	37	VGA (STRAP) 2/6	PV	10'11'22
03	ARD (DMI,PEG,FDI)	PV	10'11'22	38	VGA (IO) 3/6	PV	10'11'22
04	ARD (CLK,MISC,JTAG)	PV	10'11'22	39	VGA (Memory BUS) 4/6	PV	10'11'22
05	ARD (DDR3)	PV	10'11'22	40	VGA (LVDS) 5/6	PV	10'11'22
06	ARD (POWER)	PV	10'11'22	41	VGA (POWER) 6/6	PV	10'11'22
07	ARD (GRAPHICS POWER)	PV	10'11'22	42	VRAM (DDR3) 1/4	PV	10'11'22
08	ARD (GND)	PV	10'11'22	43	VRAM (DDR3) 2/4	PV	10'11'22
09	ARD (RESERVED)	PV	10'11'22	44	VRAM (DDR3) 3/4	PV	10'11'22
10	PCH (HDA,JTAG,SAT)	PV	10'11'22	45	VRAM (DDR3) 4/4	PV	10'11'22
11	PCH (PCI-E,SMBUS,CLK)	PV	10'11'22	46	VRAM (BYPASS) 1/2	PV	10'11'22
12	PCH (DMI,FDI,GPIO)	PV	10'11'22	47	VRAM (BYPASS) 2/2	PV	10'11'22
13	PCH (LVDS,DDI)	PV	10'11'22	48	VGA (BACO)	PV	10'11'22
14	PCH (PCI,USB,NVRAM)	PV	10'11'22	49	Power History (1)	PV	10'11'22
15	PCH (GPIO,VSS NCTF,RSVD)	PV	10'11'22	50	PWR Power Design Diagram	PV	10'11'22
16	PCH (POWER) 1/2	PV	10'11'22	51	PWR DCIN	PV	10'11'22
17	PCH (POWER) 2/2	PV	10'11'22	52	PWR Battery Conn.	PV	10'11'22
18	PCH (VSS)	PV	10'11'22	53	PWR Charger	PV	10'11'22
19	CLOCK GEN	PV	10'11'22	54	PWR +5V/+3V/+12V	PV	10'11'22
20	DDR3(SO-DIMM 0) 1/2	PV	10'11'22	55	PWR +1 05V	PV	10'11'22
21	DDR3(SO-DIMM 1) 2/2	PV	10'11'22	56	PWR +1 5V/+0 75V/1.8V	PV	10'11'22
22	CRT	PV	10'11'22	57	PWR VHCORE	PV	10'11'22
23	LVDS	PV	10'11'22	58	PWR GFXCORE	PV	10'11'22
24	HDMI	PV	10'11'22	59	PWR AT VDD/PEX VDD	PV	10'11'22
25	EC+KBC(ITE8518)	PV	10'11'22	60	PWR Others power plane	PV	10'11'22
26	EC SPI ROM & DEBUG PORT	PV	10'11'22	61	History (1)	PV	10'11'22
27	REALTEK LAN	PV	10'11'22	62	History (2)	PV	10'11'22
28	Audio (CODEC)	PV	10'11'22	63	History (3)	PV	10'11'22
29	SATA HDD/ODD	PV	10'11'22	64	DB POWER BUTTON	PV	10'11'22
30	FAN/Accelerometer/Thermal	PV	10'11'22	65	BTB Conn& LED& Hole/Boss	PV	10'11'22
31	WLAN	PV	10'11'22	66	USB 3.0 Controller (1.1V)	PV	10'11'22
32	CARD READER	PV	10'11'22	67	USB3.0 PORT x2	PV	10'11'22
33	MB TO DB CONN	PV	10'11'22	68			
34	HOLE & BOSS	PV	10'11'22	69			
35	AUDIO (Jack Mute) 2/2	PV	10'11'22	70			


Project Code & Schematics Subject: Rains Main Board 10L

PCB P/N:

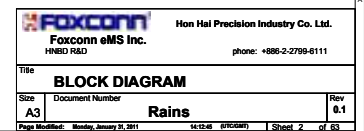
LED DB P/N:

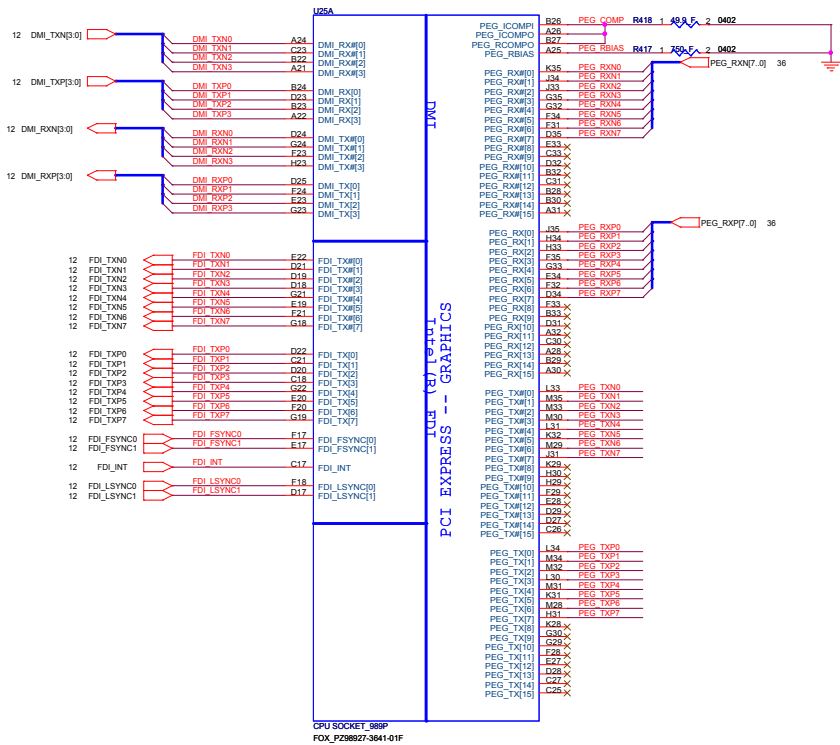
P/B DB P/N:

P. Leader	Check by	Design by

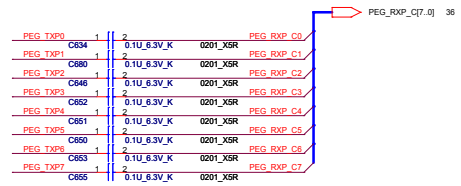
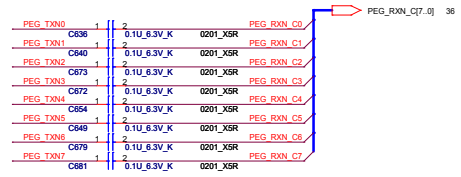
		Hon Hai Precision Industry Co. Ltd.	
Foxconn eMS Inc.		phone: +886-2-2799-6111	
HNEO R&D			
Title			
Index page			
Size		Document Number	
A3		Rains	
Page Modified: Monday, January 23, 2011		Rev 6.1	
14:24:46 (UTC+08:00)		Sheet 1 of 63	

Platform: AMD Winstler M2 Discrete Gra





If PCIe Graphics is not implemented, the TX/RX pairs can be left as No Connect.

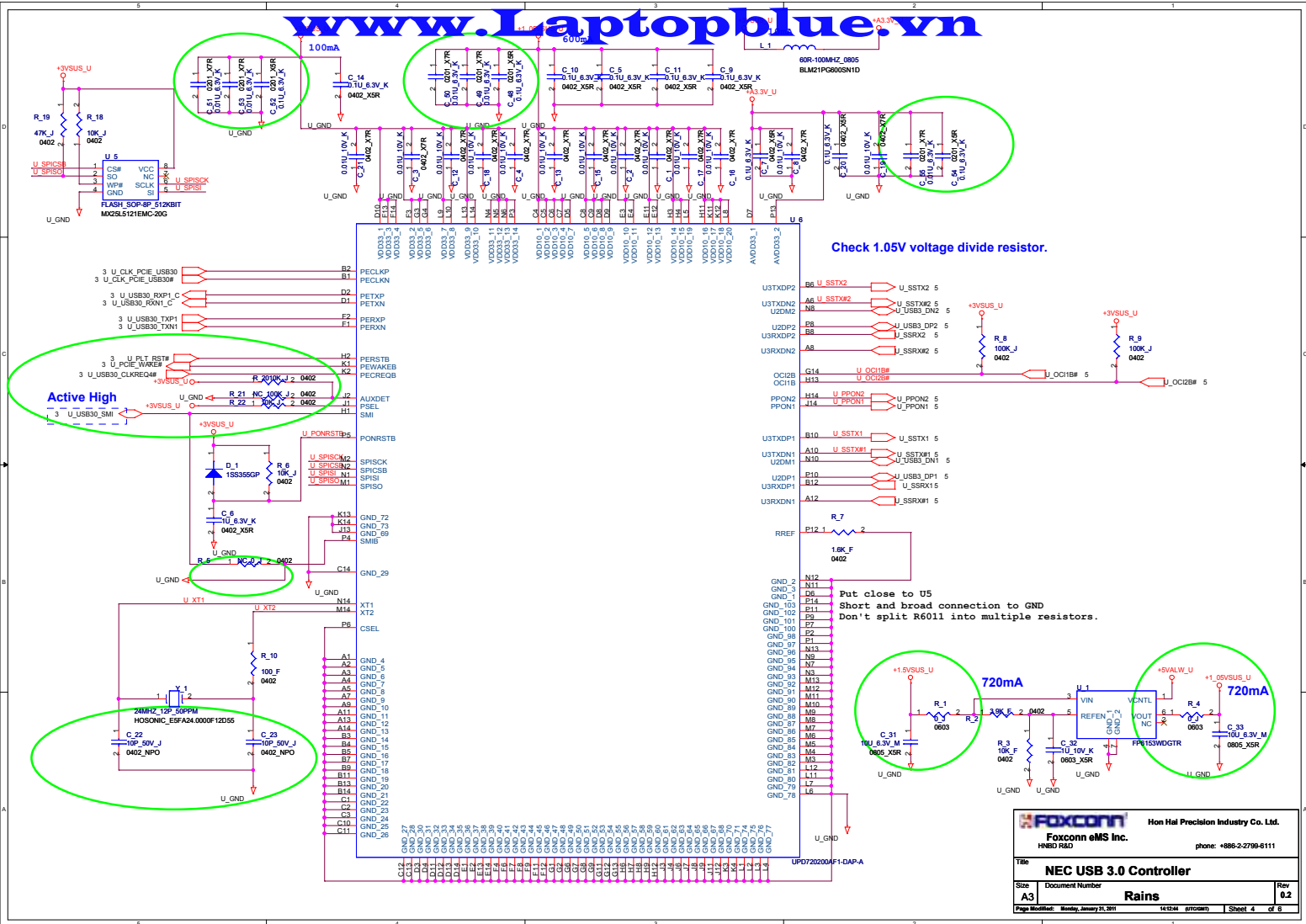


For Disable Arrandale Graphic

In addition, FDI_RXN_[7:0] and FDI_RXP_[7:0] can be left floating on the FCH.

FDI_TX[7:0] and FDI_TXP[7:0] can be left floating on the Arrandale. The OFX_IMON, FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT signals on the Arrandale side should be tied to GND (through 1-k Ω resistors). FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1] can be ganged together with one resistor.

		Hon Hai Precision Industry Co. Ltd. phone: +886-2-2799-6111	
Foxconn eMS Inc. HNEO R&D			
Title: ARD (DMI,PEG,FDI)			
Size: A3	Document Number: Rains		Rev: 6.1
Page Modified: Monday, January 21, 2011 14:24:00 (UTC+0800) Sheet 3 of 63			



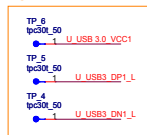


CPU SOCKET_989P
FOX_PZ98927-3641-01P

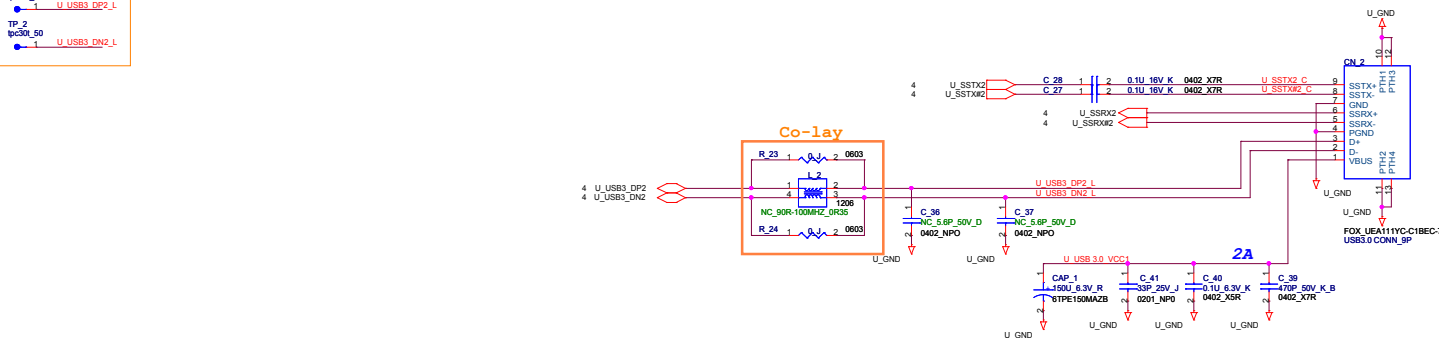
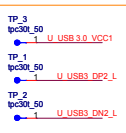


phone: +886-2-2799-6111

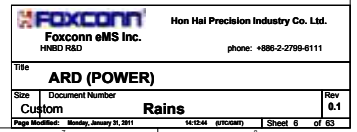
SI BFT Test Pad



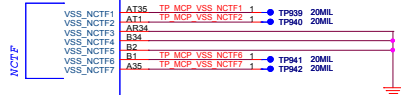
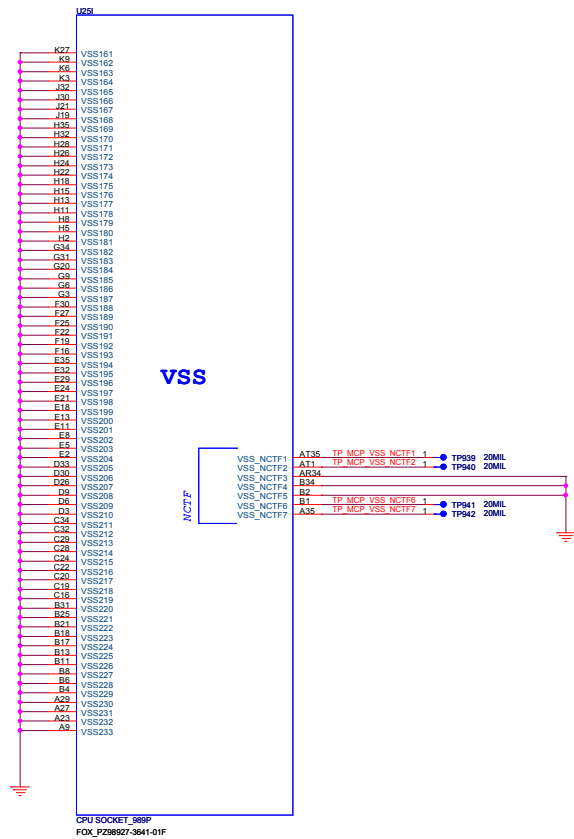
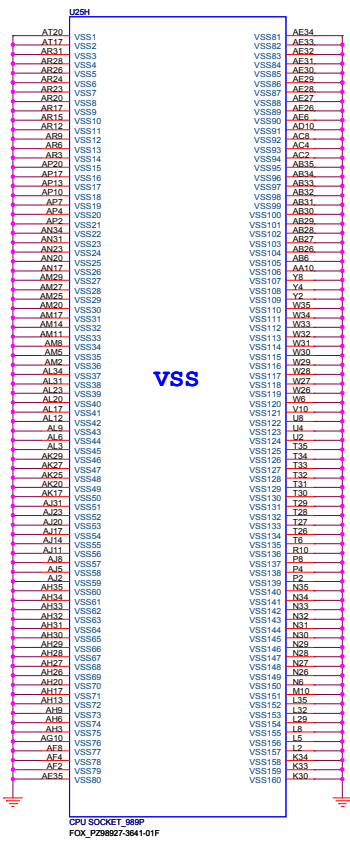
SI BFT Test Pad



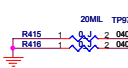
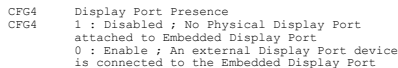
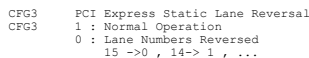
		Hon Hai Precision Industry Co. Ltd. phone: +886-2-2799-6111	
Foxconn eMS Inc. HNEO R&D			
Title USB3.0 PORT x2			
Size A3		Document Number Rains	
Page Modified: Monday, January 21, 2013		Rev 8.2	
		Sheet 5 of 8	



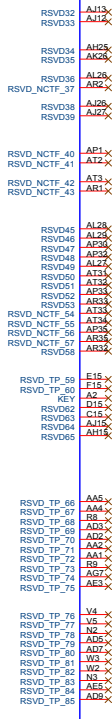




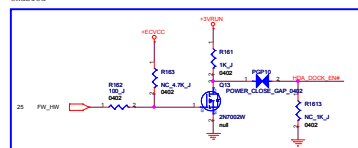
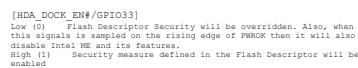
```
CFG[1:0] - PCI Express* Port Bifurcation:
    11 = 1 x16 PEG
    10 = 2 x8 PEG
```



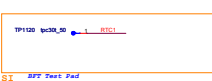
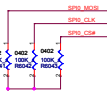
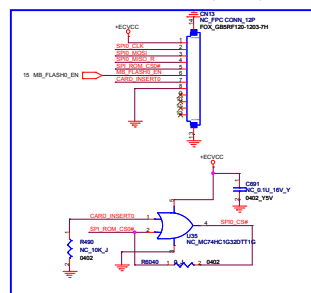
Intel has determined that the workaround (3.01K pull down to Vss on signal CFG[7]) is not robust. Intel recommends not implementing this workaround at this time (CFG[7] should not be pulled down). Intel recommends not to test for PCI-E Express 2.0 Jitter specification compliance for the affected steppings.



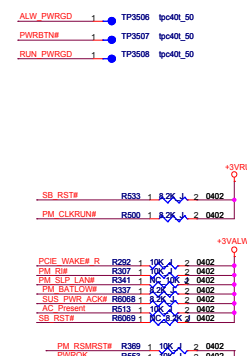
R18
0_J
0402

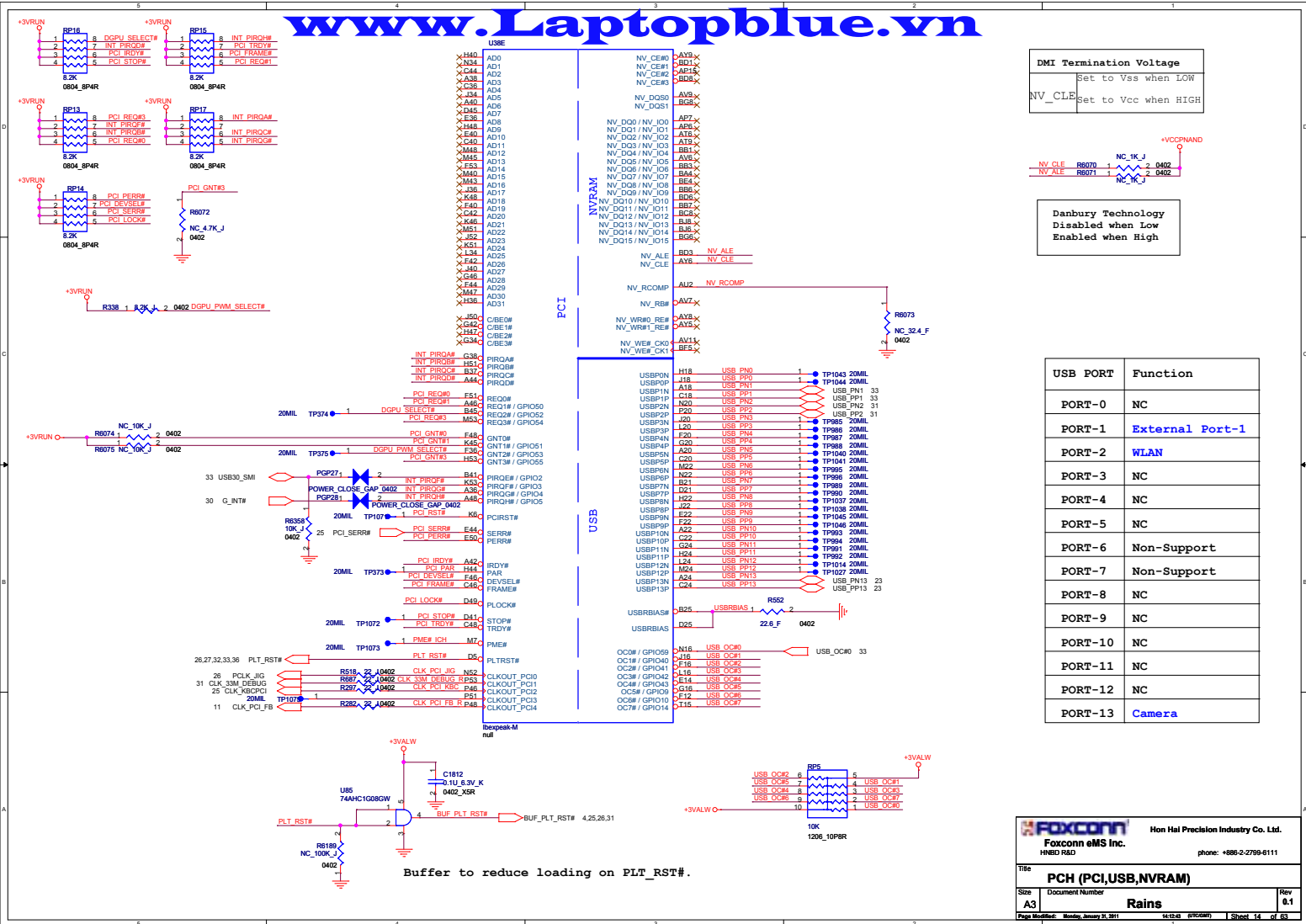


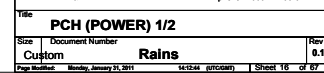
EXTERNAL SPI0 ROM INTERFACE (FOR U98)



 Foxconn eMS Inc. HNSD R&D		Hon Hai Precision Industry Co. Ltd. phone: +886-2-2799-6111	
Title: PCH (HDA,JTAG,SAT)			
Size	Document Number	Rev	0
Custom	Rains		



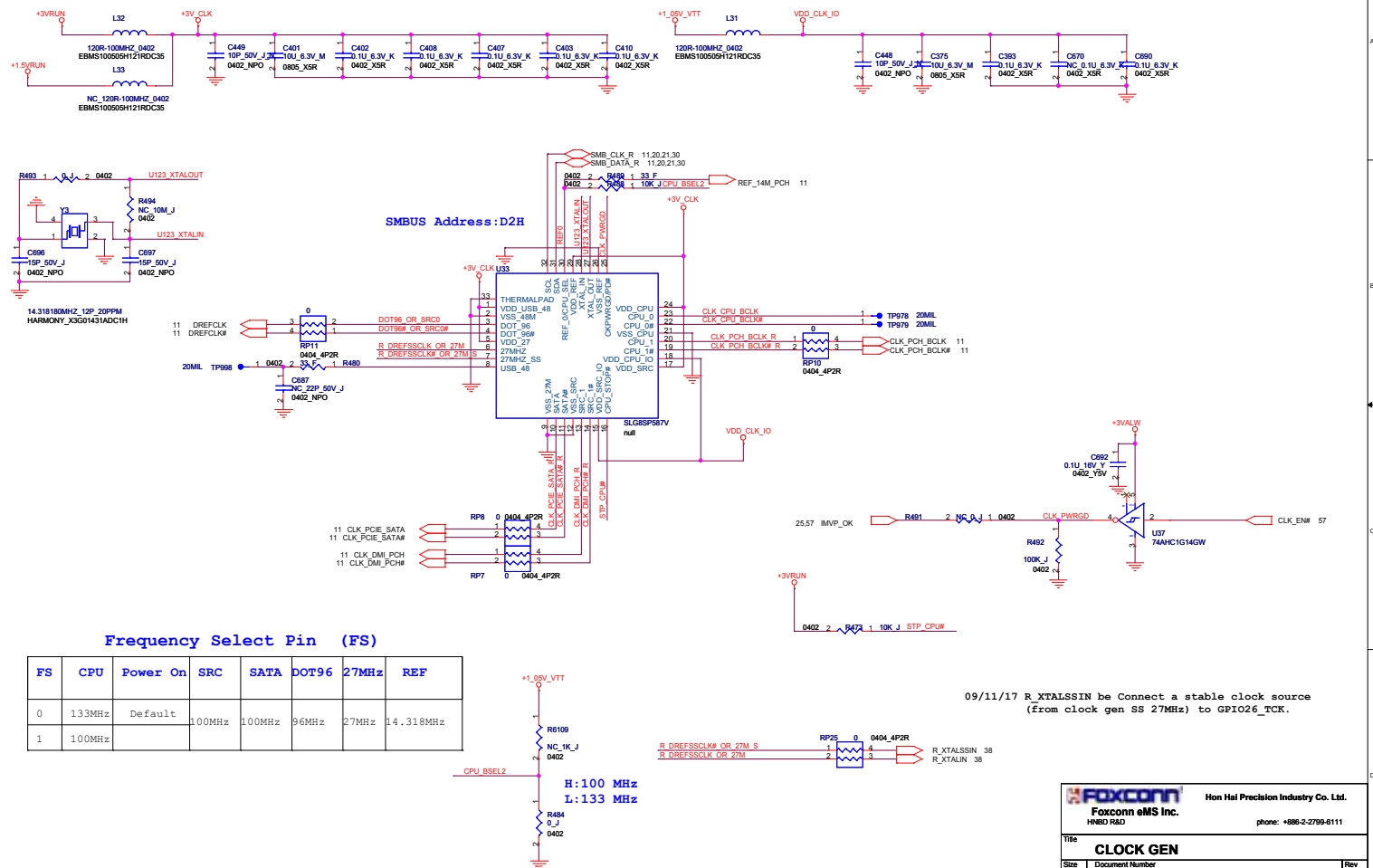




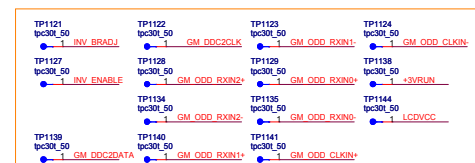
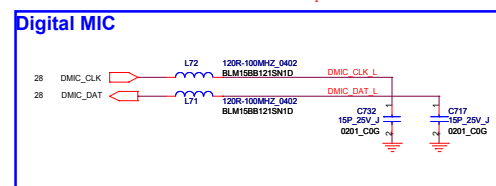
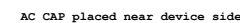
U38		
AV7	VSS159	H49
B11	VSS160	H5
B15	VSS161	J24
B19	VSS162	K11
B23	VSS163	K43
B27	VSS164	K47
B31	VSS165	K7
B35	VSS166	L14
B39	VSS167	L18
B43	VSS168	L2
B47	VSS169	L32
B51	VSS170	L36
B55	VSS171	L40
B59	VSS172	L52
B63	VSS173	M12
B67	VSS174	M16
B71	VSS175	M18
B75	VSS176	M32
B79	VSS177	M34
B83	VSS178	M38
B87	VSS179	M42
B91	VSS180	M46
B95	VSS181	M49
B99	VSS182	M5
C03	VSS183	M8
C07	VSS184	M9
C11	VSS185	N24
C15	VSS186	N24
C19	VSS187	AD15
C23	VSS188	P22
C27	VSS189	P30
C31	VSS190	P32
C35	VSS191	P34
C39	VSS192	P42
C43	VSS193	P45
C47	VSS194	P47
C51	VSS195	R2
C55	VSS196	R22
C59	VSS197	T12
C63	VSS198	T46
C67	VSS199	T46
C71	VSS200	T49
C75	VSS201	T5
C79	VSS202	T8
C83	VSS203	U31
C87	VSS204	U32
C91	VSS205	U34
C95	VSS206	U34
C99	VSS207	P38
D03	VSS208	V11
D07	VSS209	P16
D11	VSS210	V19
D15	VSS211	VSS210
D19	VSS212	V22
D23	VSS213	V30
D27	VSS214	V32
D31	VSS215	V34
D35	VSS216	V36
D39	VSS217	V38
D43	VSS218	V38
D47	VSS219	V43
D51	VSS220	V45
D55	VSS221	V46
D59	VSS222	V49
D63	VSS223	V52
D67	VSS224	V5
D71	VSS225	V7
D75	VSS226	V8
D79	VSS227	W2
D83	VSS228	W52
D87	VSS229	Y11
D91	VSS230	Y12
D95	VSS231	Y15
D99	VSS232	Y23
E03	VSS233	Y28
E07	VSS234	Y30
E11	VSS235	Y31
E15	VSS236	Y32
E19	VSS237	Y38
E23	VSS238	Y43
E27	VSS239	Y46
E31	VSS240	Y46
E35	VSS241	P46
E39	VSS242	Y5
E43	VSS243	Y8
E47	VSS244	P24
E51	VSS245	T43
E55	VSS246	AD51
E59	VSS247	AT8
E63	VSS248	AD47
E67	VSS249	Y47
E71	VSS250	AT12
E75	VSS251	AM6
E79	VSS252	AT13
E83	VSS253	AM5
E87	VSS254	VSS254
E91	VSS255	AK45
E95	VSS256	AK38
E99	VSS257	AV14
F03	VSS258	VSS258

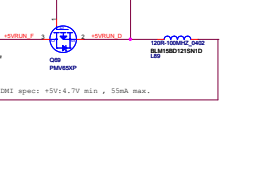
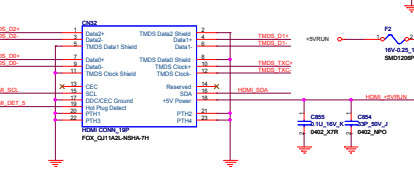
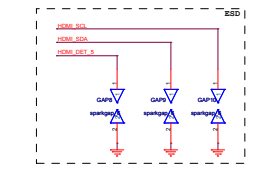
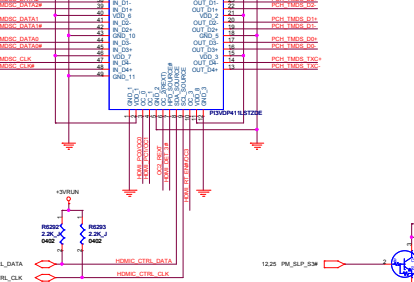
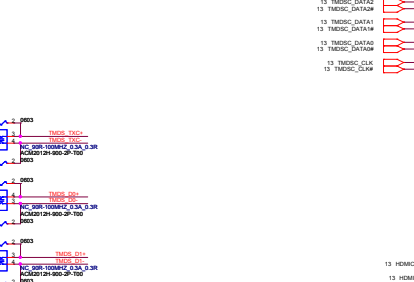
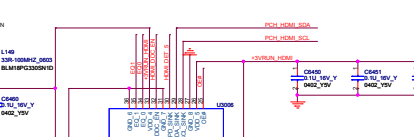
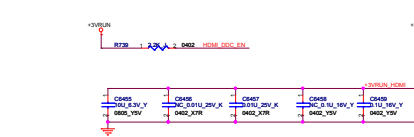
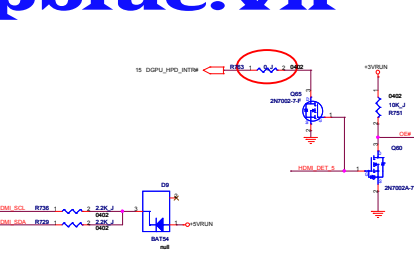
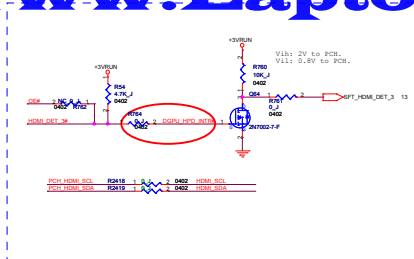
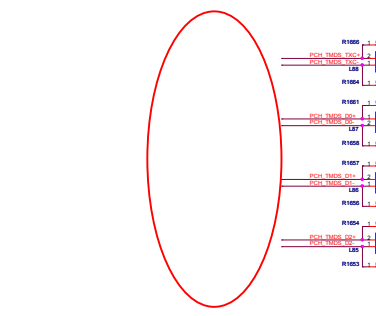
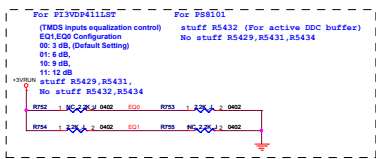
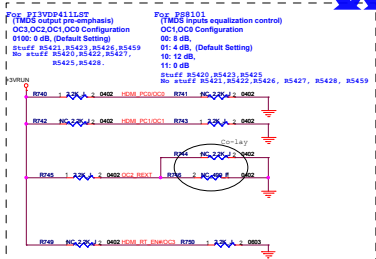
U39H		
AB16	VSS[0]	
AA19	VSS[1]	VSS80
AA20	VSS[2]	VSS81
AA22	VSS[3]	VSS82
AA23	VSS[4]	VSS83
AA24	VSS[5]	VSS84
AA28	VSS[6]	VSS85
AA30	VSS[7]	VSS86
AA31	VSS[8]	VSS87
AA32	VSS[9]	VSS88
AA33	VSS[10]	VSS89
AB11	VSS[11]	VSS90
AB15	VSS[12]	VSS91
AB23	VSS[13]	VSS92
AB32	VSS[14]	VSS93
AB31	VSS[15]	VSS94
AB39	VSS[16]	VSS95
AB43	VSS[17]	VSS96
AB47	VSS[18]	VSS97
AB5	VSS[19]	VSS98
AB6	VSS[20]	VSS99
AC2	VSS[21]	VSS100
AC22	VSS[22]	VSS101
AD11	VSS[23]	VSS102
AD12	VSS[24]	VSS103
AD16	VSS[25]	VSS104
AD23	VSS[26]	VSS105
AD31	VSS[27]	VSS106
AD32	VSS[28]	VSS107
AD34	VSS[29]	VSS108
AD35	VSS[30]	VSS109
AD36	VSS[31]	VSS110
AD37	VSS[32]	VSS111
AD38	VSS[33]	VSS112
AD39	VSS[34]	VSS113
AD7	VSS[35]	VSS114
AE2	VSS[36]	VSS115
AE4	VSS[37]	VSS116
AE12	VSS[38]	VSS117
Y13	VSS[39]	VSS118
Y19	VSS[40]	VSS119
Y20	VSS[41]	VSS120
Y22	VSS[42]	VSS121
Y28	VSS[43]	VSS122
Y30	VSS[44]	VSS123
Y32	VSS[45]	VSS124
Y34	VSS[46]	VSS125
Y36	VSS[47]	VSS126
Y38	VSS[48]	VSS127
Y43	VSS[49]	VSS128
Y45	VSS[50]	VSS129
Y46	VSS[51]	VSS130
Y49	VSS[52]	VSS131
Y52	VSS[53]	VSS132
V5	VSS[54]	VSS133
V7	VSS[55]	VSS134
V8	VSS[56]	VSS135
W2	VSS[57]	VSS136
W52	VSS[58]	VSS137
Y11	VSS[59]	VSS138
Y12	VSS[60]	VSS139
Y15	VSS[61]	VSS140
Y23	VSS[62]	VSS141
Y28	VSS[63]	VSS142
Y30	VSS[64]	VSS143
Y31	VSS[65]	VSS144
Y32	VSS[66]	VSS145
Y38	VSS[67]	VSS146
Y43	VSS[68]	VSS147
Y46	VSS[69]	VSS148
Y46	VSS[70]	VSS149
P46	VSS[71]	VSS150
Y5	VSS[72]	VSS151
Y8	VSS[73]	VSS152
P24	VSS[74]	VSS153
T43	VSS[75]	VSS154
AD51	VSS[76]	VSS155
AT8	VSS[77]	VSS156
AD47	VSS[78]	VSS157
Y47	VSS[79]	VSS158
AT12	VSS[80]	VSS159

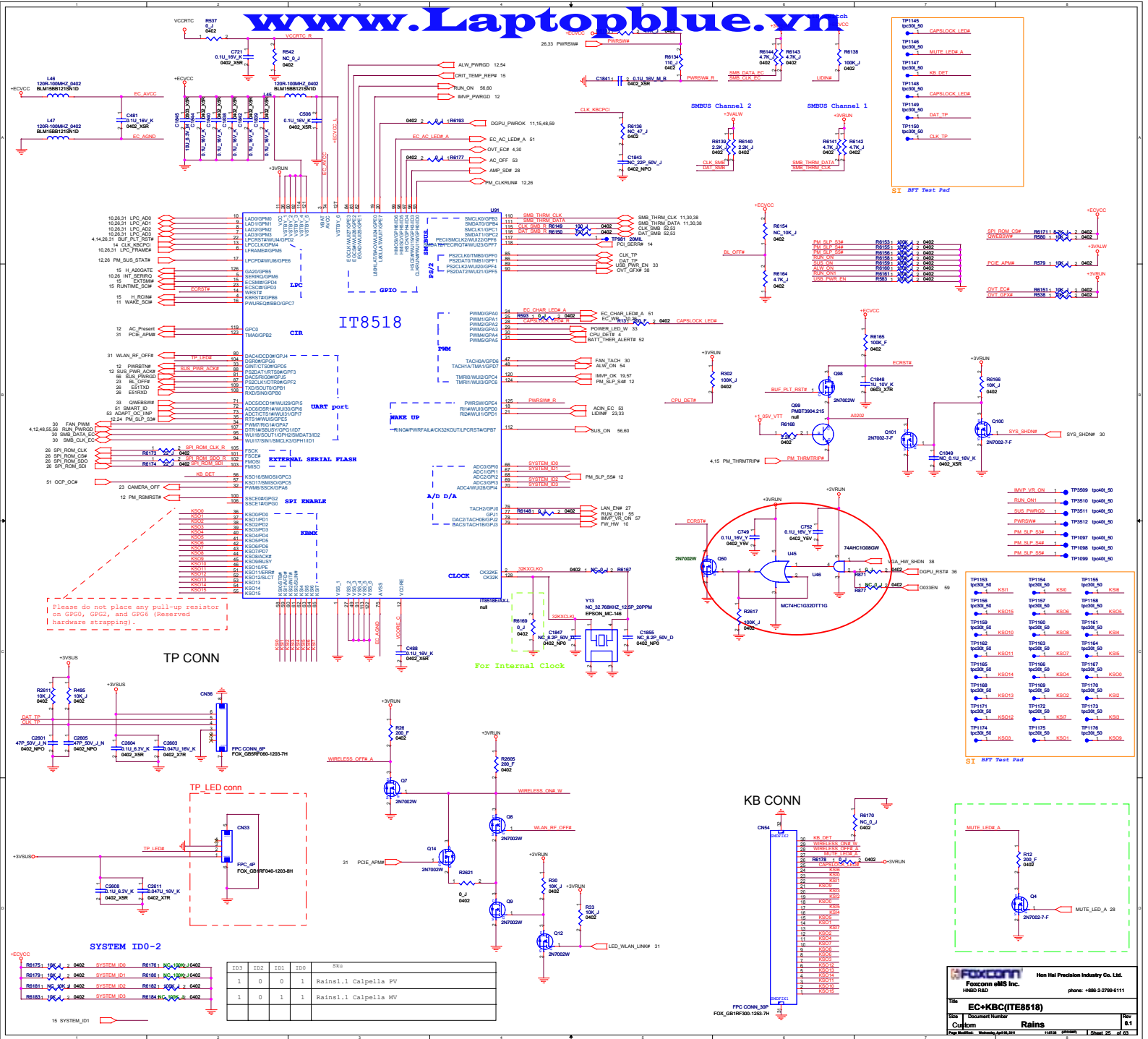
Foxconn		Hon Hai Precision Industry Co. Ltd.			
Foxconn eMS Inc.		phone: +886-2-2799-6111			
HNSD R&D					
Title					
PCH (VSS)					
Size		Document Number			
A3		Rains			
Page Modified: Monday, January 21, 2013		14:24:44 (UTC+0800)			
Sheet 18		of 63			
Rev		6.1			





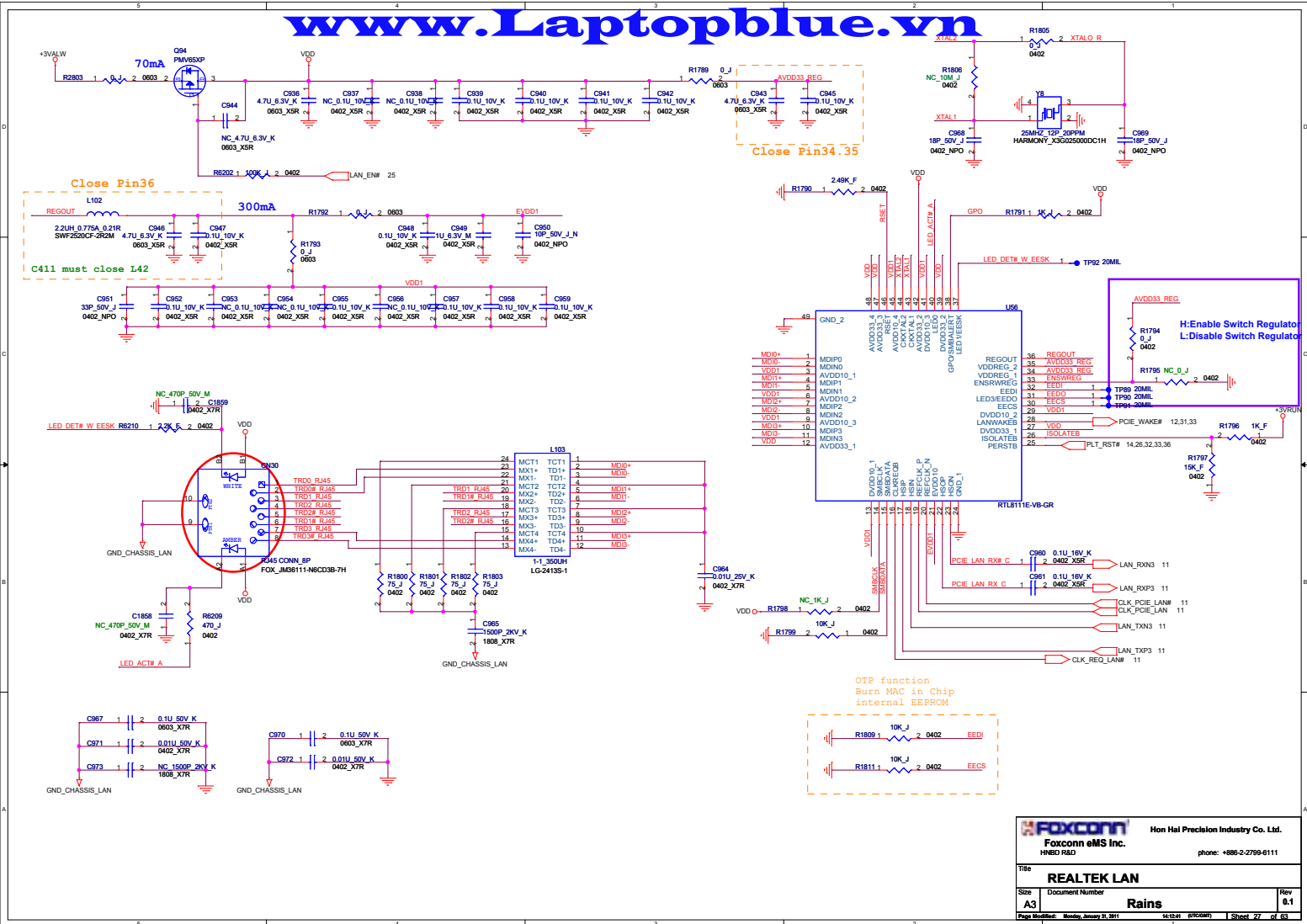


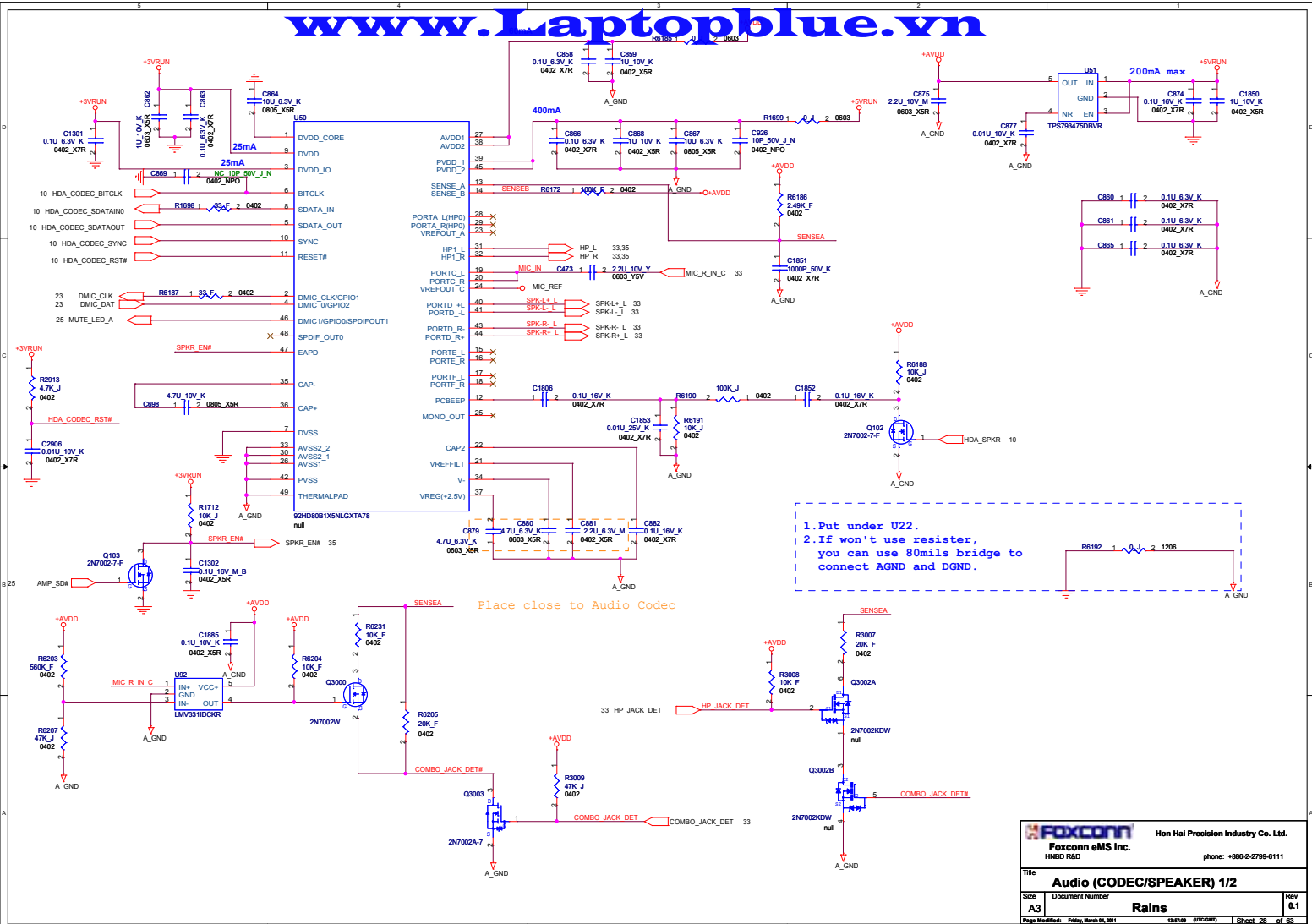




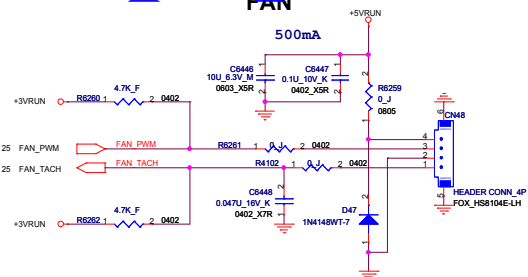
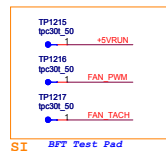
Please do not place any pull-up resistor on GPIOs, GPIOs, and GPIOs (reserved hardware strapping).

IO3	IO2	IO1	IO0	SKU
1	0	0	1	Rainell Calpella PV
1	0	1	1	Rainell Calpella MV

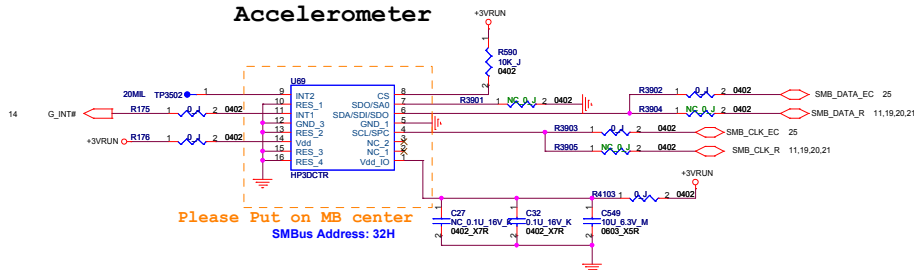




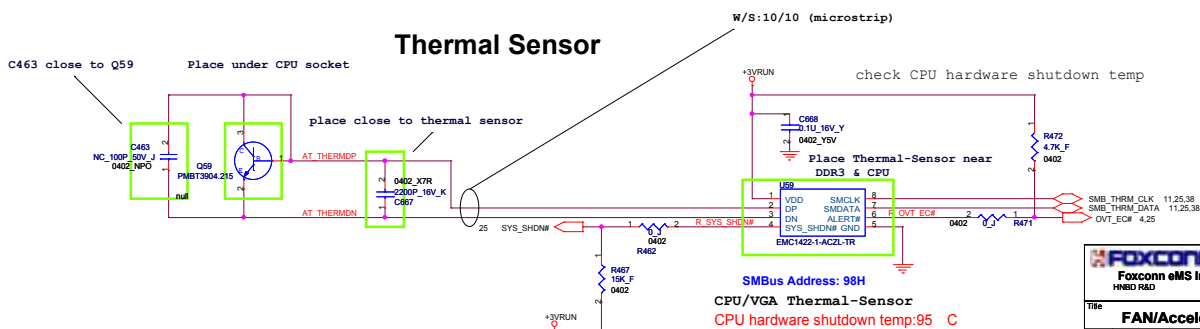
FAN



Accelerometer



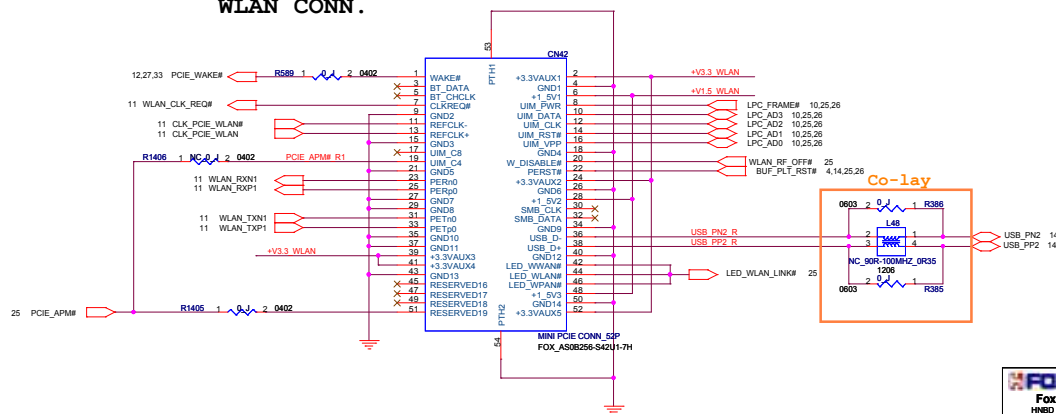
Thermal Sensor



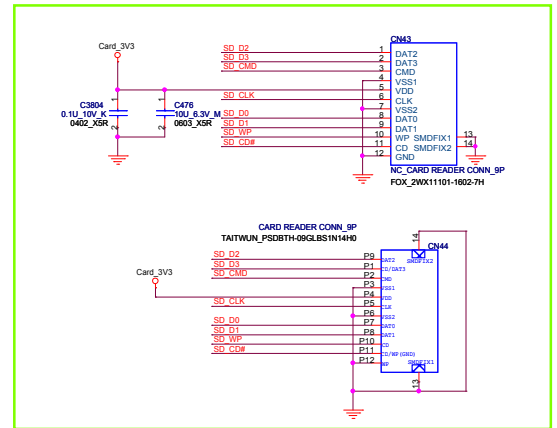
Foxconn Foxconn eMS Inc. HNEO R&D phone: +886-2-2799-6111	
Hon Hai Precision Industry Co. Ltd.	
Title FAN/Accelerometer	Rev 8.1
Size A3	Document Number Rains
Page Modified: Monday, January 25, 2011 14:24 0/10000 Sheet 30 of 53	



WLAN CONN.

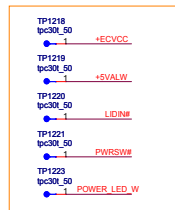


PCB layout for the RTSS5209-GR module. The layout includes a USB connector (U58) with pins for HSIP, HSIN, REFCLKP, REFCLKN, HSOP, HSON, GND_1, DV12, CARD1_3V3, 3V3_IN_1, CARD2_3V3, and SD pins. It also shows a 1.2A current source, a 1A current source, and a 1.2A current source. The layout is labeled with component values and pin numbers.

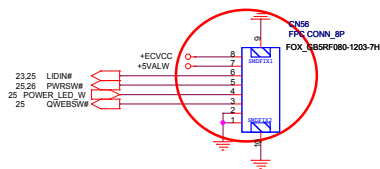


Please put close to U58

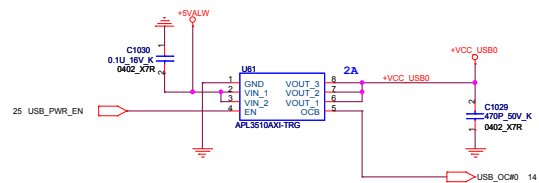
POWER BUTTON BOARD CONNECTOR



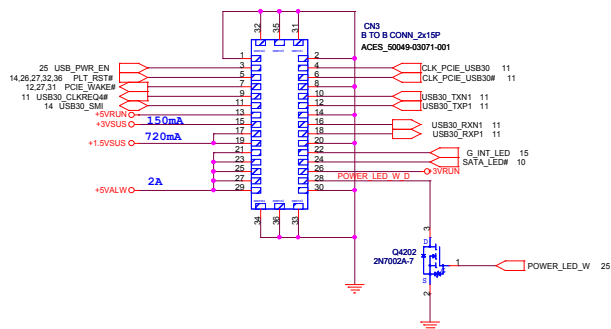
SI RFT Test Pad



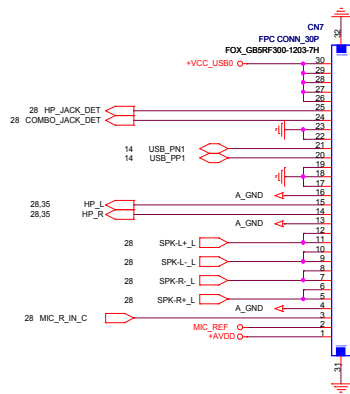
USB 2.0 POWER SWITCH



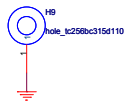
USB3.0 DB CONN



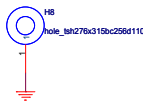
AUDIO jack + USB2.0 port X1



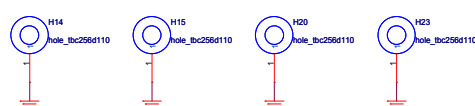
B+C Type



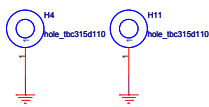
R+U Type



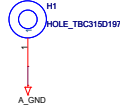
B+B Type



C+C Type



G Type



J Type



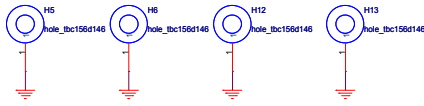
A+A Type



S+V Type



L Type



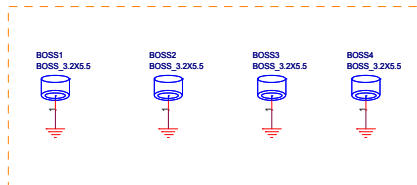
M Type



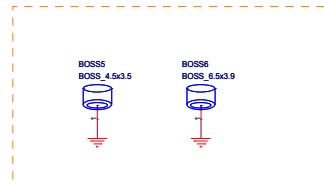
N Type



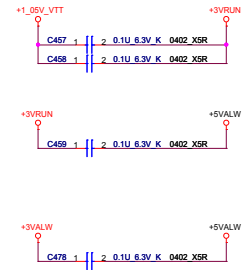
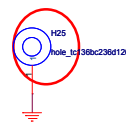
TOP SIDE BOSE




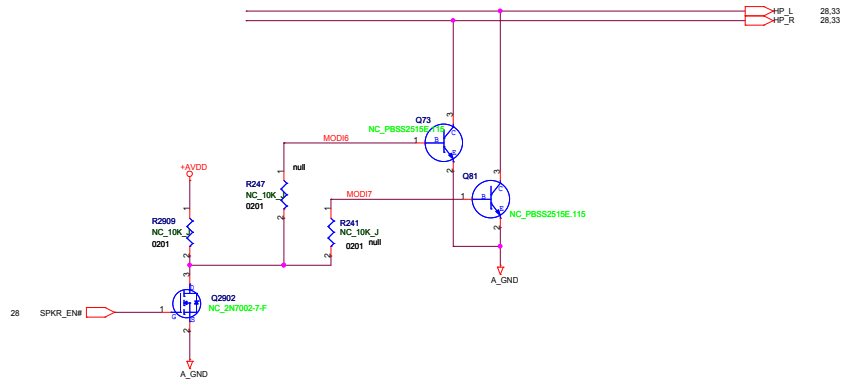
Bottom SIDE



Co-lay with BOSS5



		Hon Hai Precision Industry Co. Ltd.	
Foxconn eMS Inc.			
HNBD R&D		phone: +886-2-2799-6111	
Title			
Hole & BOSS			
Size	Document Number		Rev
A3	Rains		0.1
Page Modified: Monday, January 21, 2013 14:24:00 (UTC+0800)		Sheet 34	of 83



de-pop noise schematic

GPIO21 MUST BE LOW DURING POSTB WHEN ENHANCED BIOS OPTION IS ON

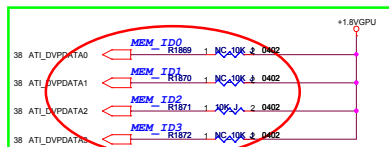
PIN STRAPS

Strap for DDR3 VRAM
ATI_DVPPDATA[3 : 0]

For Wistler-Pro

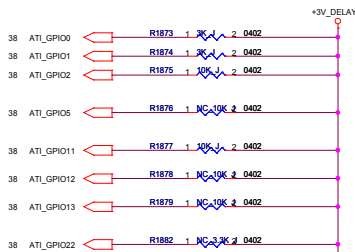
0001 64Mx16	Hynix (800MHz)	x8pcs
0010 64Mx16	Samsung (800MHz)	x8pcs
0100 64Mx16	Hynix (900MHz)*	x8pcs
1000 64Mx16	Samsung (900MHz)	x8pcs
0011 128Mx16	Hynix (800MHz)	x8pcs
0110 128Mx16	Samsung (800MHz)	x8pcs
1100 128Mx16	Hynix (900MHz)	x8pcs
1001 128Mx16	Samsung (900MHz)	x8pcs

*means the schematic implemented



If no ROM attached, GPIO[13:12:11]
CONFIG[2:0]
controls the memory aperture size.

64MB	010
128MB	000
256MB	001
512MB	001



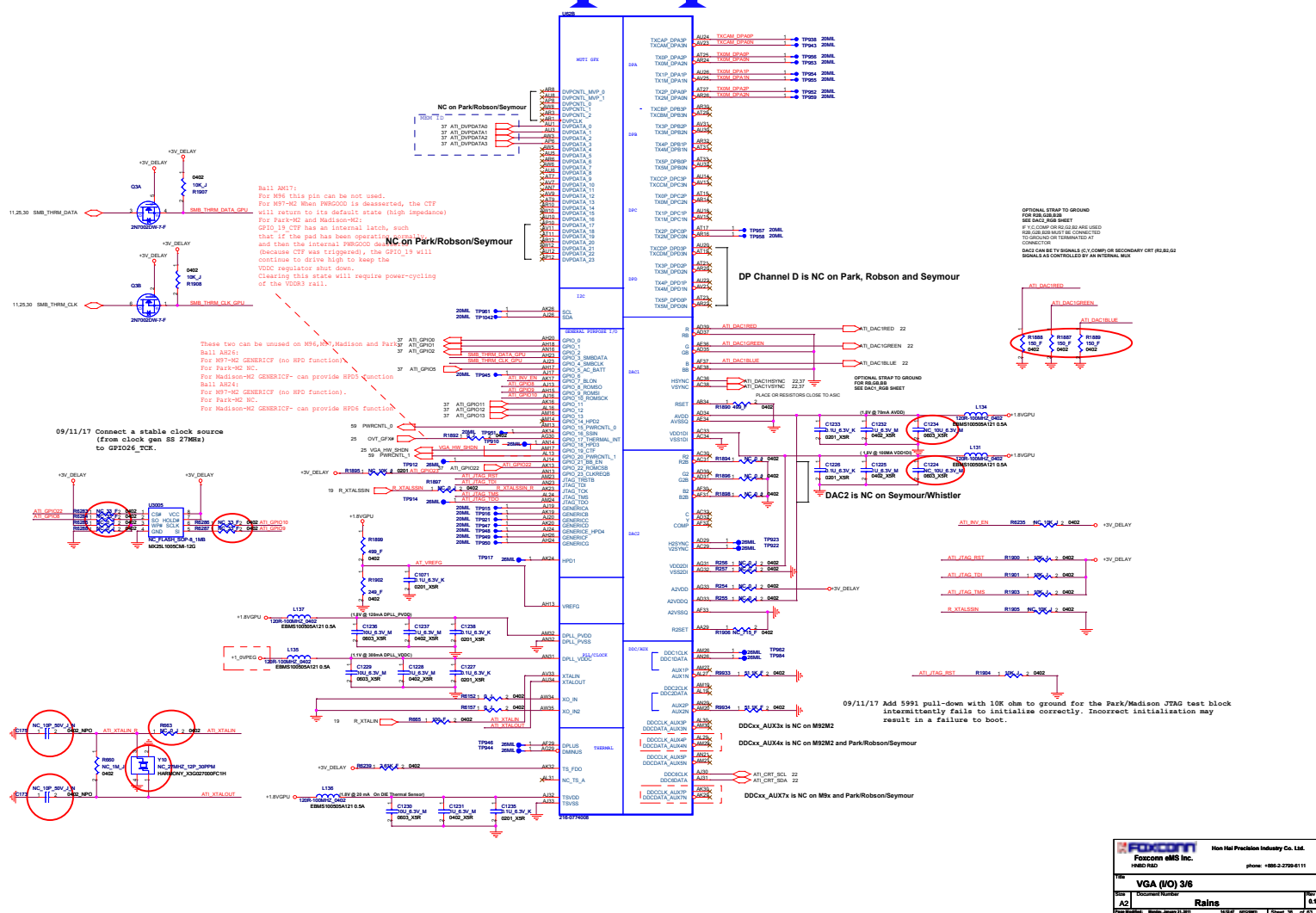
1 Enable HD Audio
0 Disable HD Audio

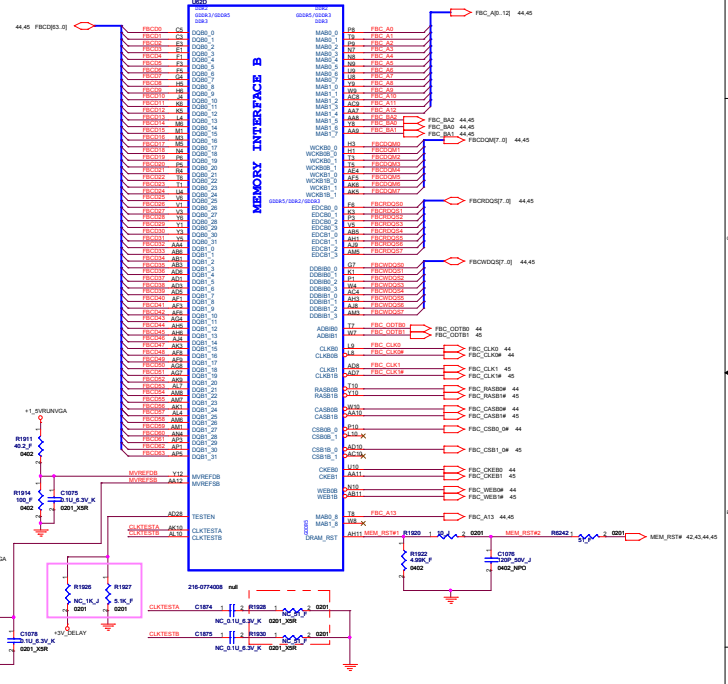
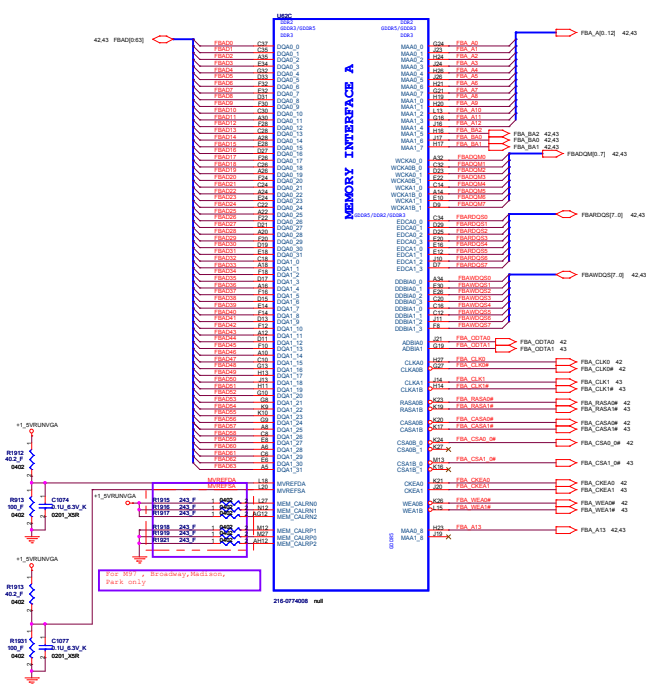


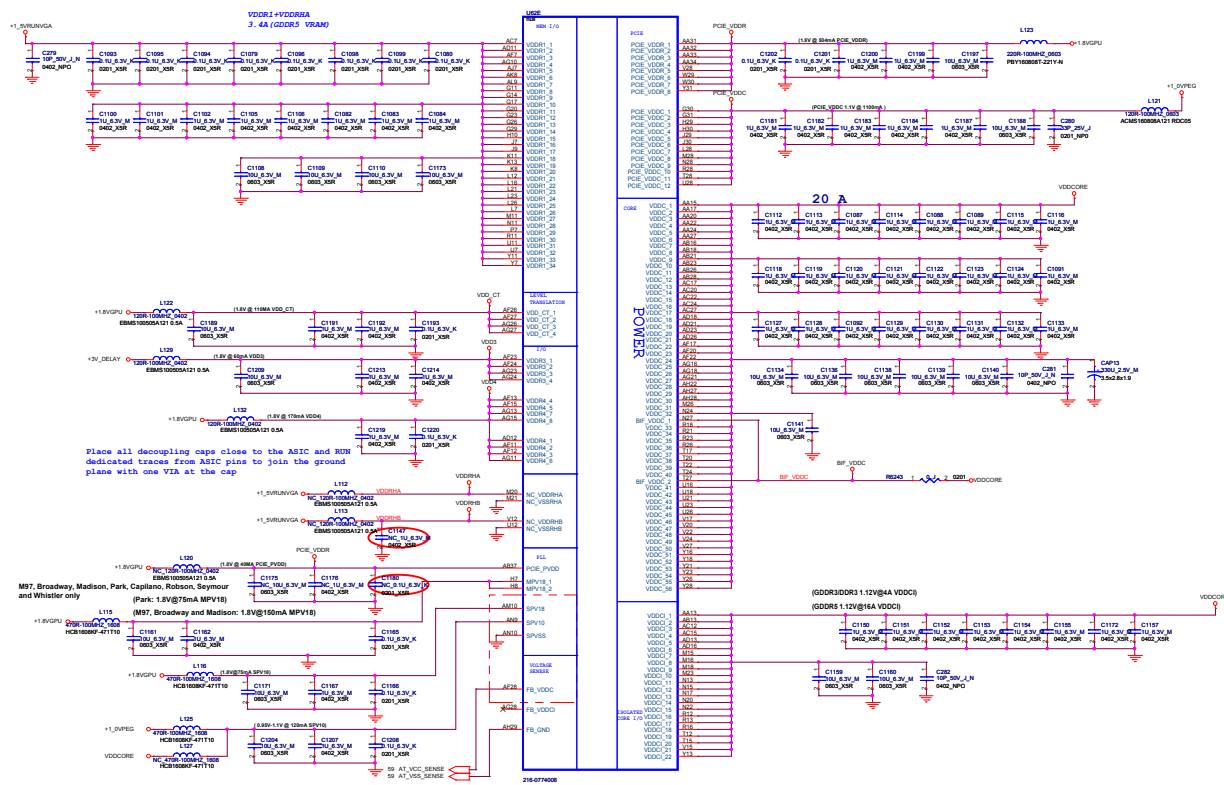
1 Enable HDMI
0 Disable HDMI

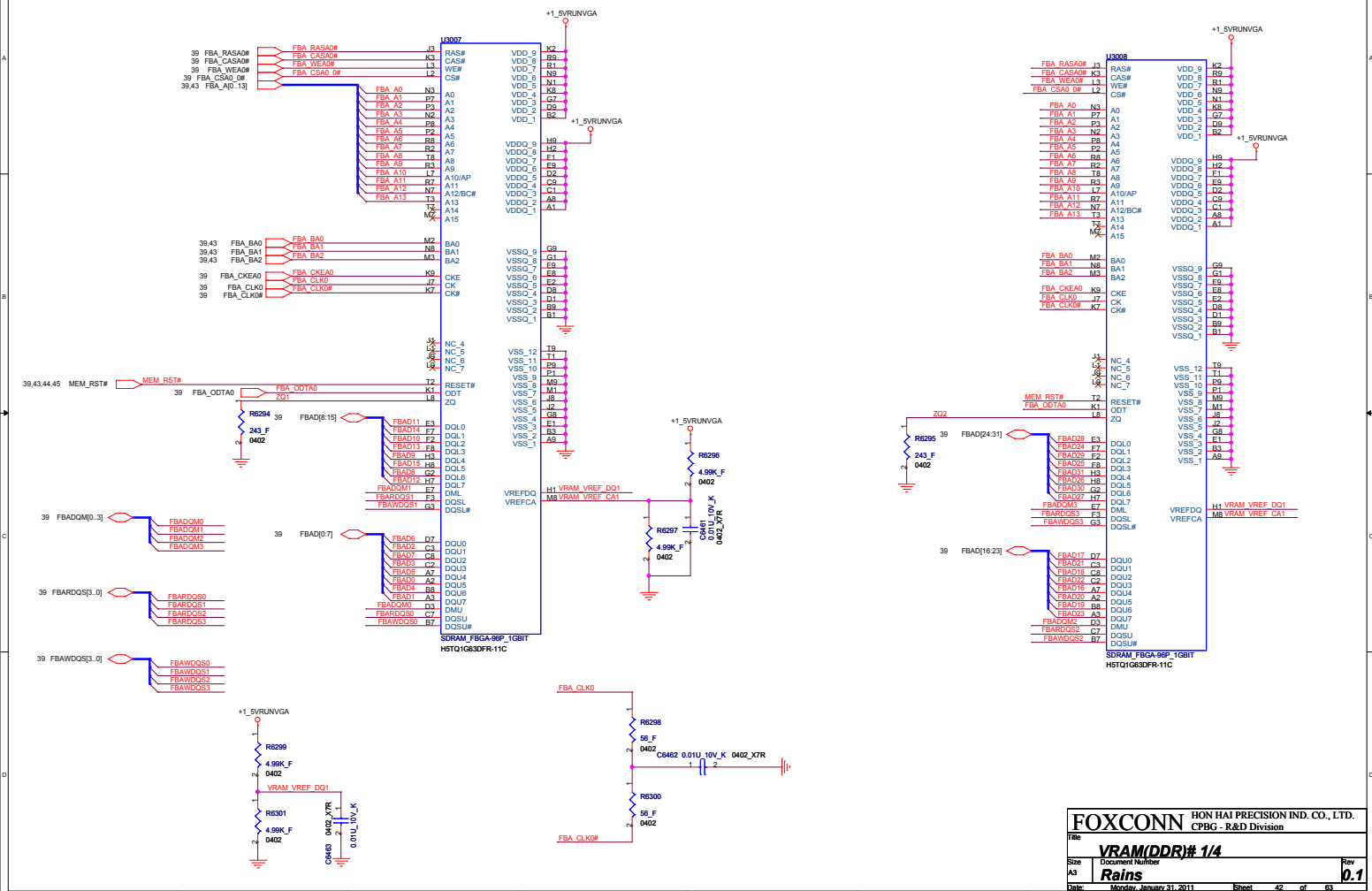


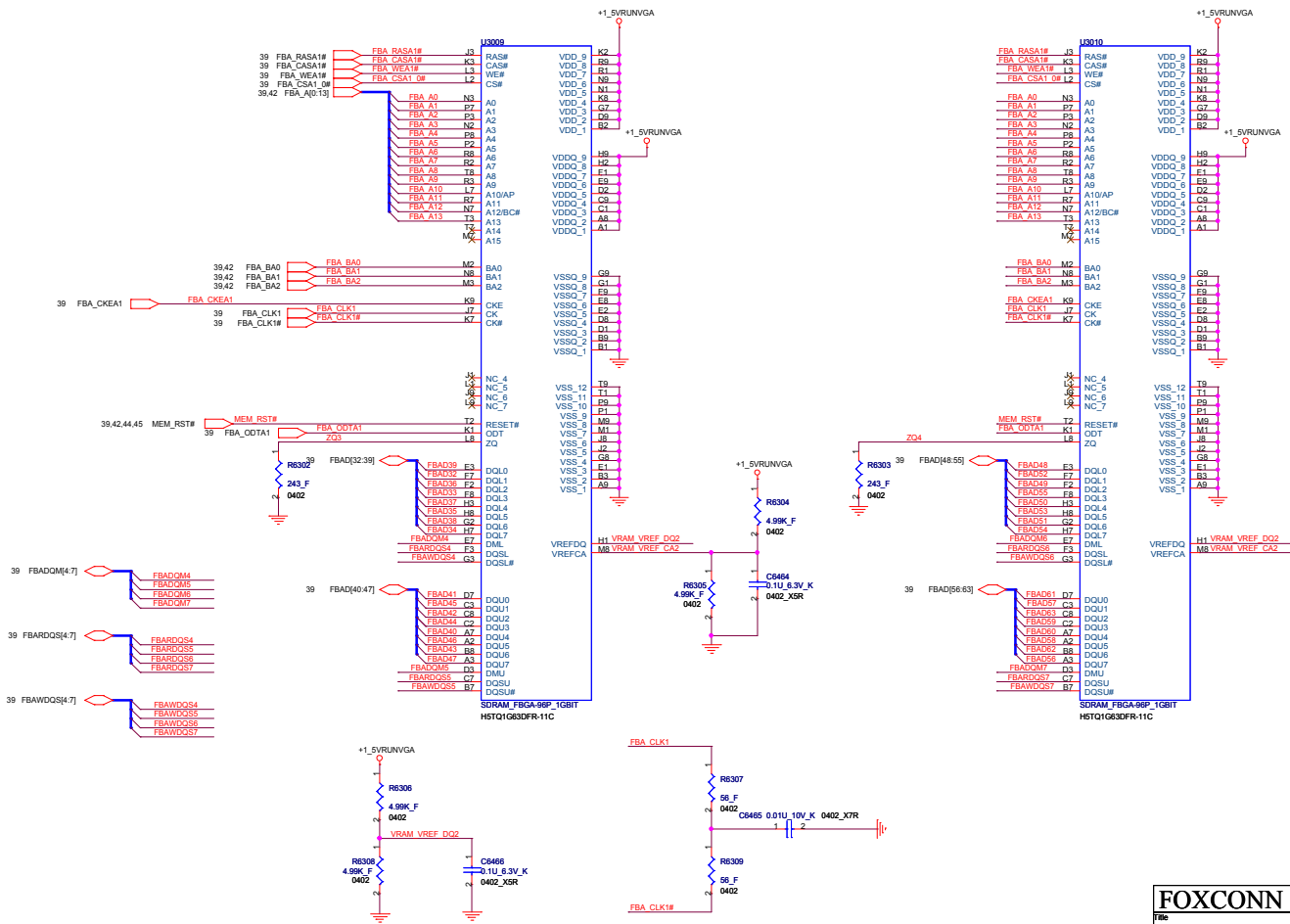
CONFIGURATION STRAPS		
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET		
STRAPS	PIN name	DESCRIPTION OF DEFAULT SETTINGS
TX_PWR5_ENB	GPIO_0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing
TX_DEEMPH_EN	GPIO_1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled
AC_BATT	GPIO_5	AC (Performance mode) = 3.3 V Battery saving mode = 0.0 V
PWRCNTL_0	GPIO_6	Power Control signals control the core voltage regulator.
PWRCNTL_1	GPIO_15	At Reset, these signals will be inputs with weak internal pull-down resistors.
BB_EN	GPIO_16	VBUS can define these signals to be either 3.3-V outputs or open drain outputs.
	GPIO_20	The output state (high/low) of these signals is programmable for each PowerPlay state.
	GPIO_21	Voltage control signal for memory voltage regulator.
BLON	GPIO_7	Controls Backlight On/Off. Active high. If not needed as the backlight enable signal, it can alternatively be used as a GPIO or an open drain type output. Note: External pull-down recommended
VGA_DIS	GPIO_9	0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller
CONFIG[0]	GPIO_11	If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size.
CONFIG[1]	GPIO_12	
CONFIG[2]	GPIO_13	
BIOS_ROM_EN	GPIO_22	Enable external BIOS ROM device 0: Disable external BIOS ROM device 1: Enable external BIOS ROM device
VIP_DEVICE_STRAP_ENA	VZSYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)
RSVD	HQSYNC	RESERVED
THERMAL_INT	GPIO_17	Thermal monitor interrupt 1) An input from an external temperature sensor (ALERTb)
CLKREQB	GPIO_23	Reserve
AUD[1]	HSYNC	AUD[1:0]: 00 - No audio function; 01 - Audio for DisplayPort only; 10 - Audio for DisplayPort and HDMI if dongle is detected; 11 - Audio for both DisplayPort and HDMI. HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.
AUD[0]	VSYNC	
RSVD	GENERICC	RESERVED

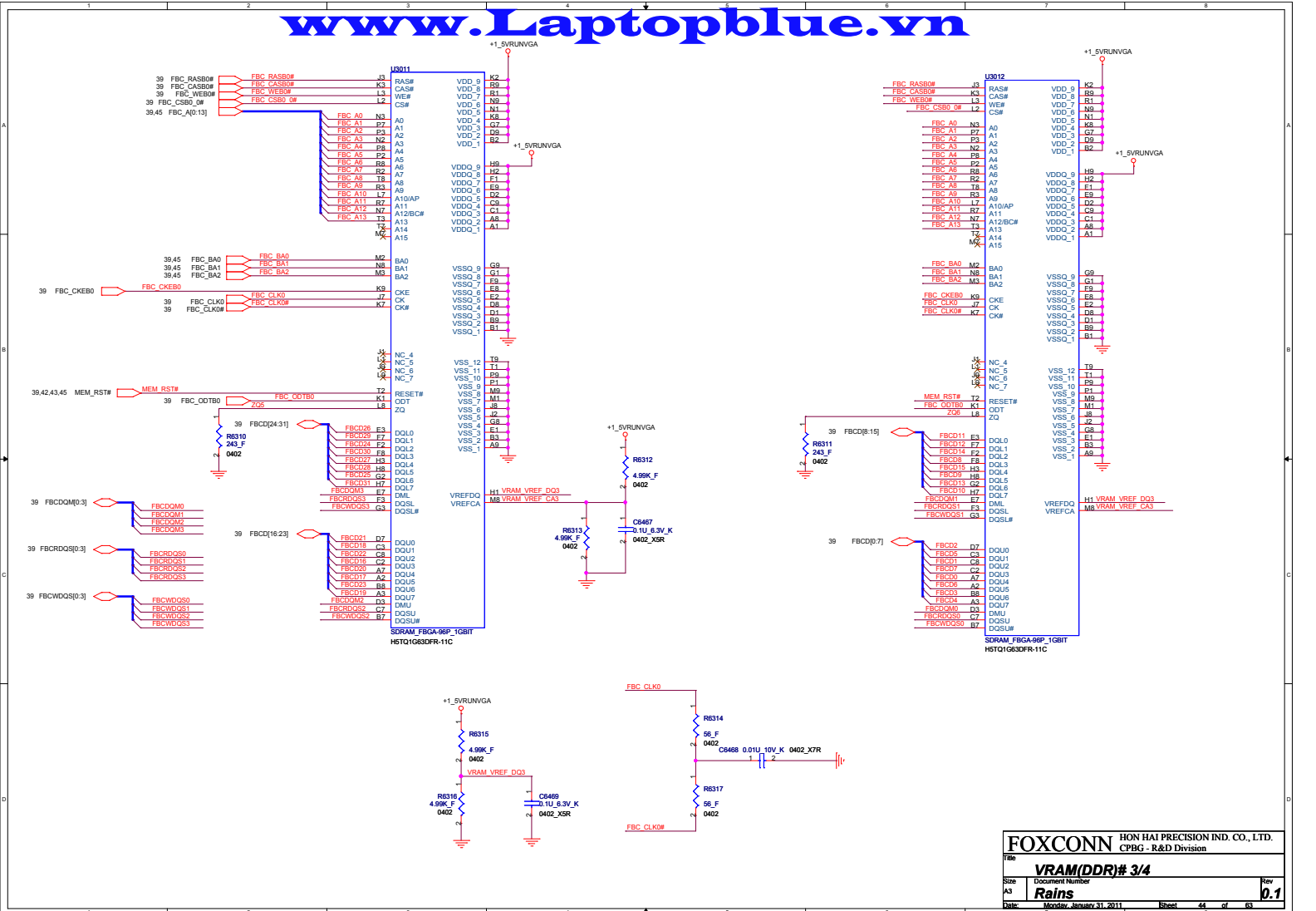


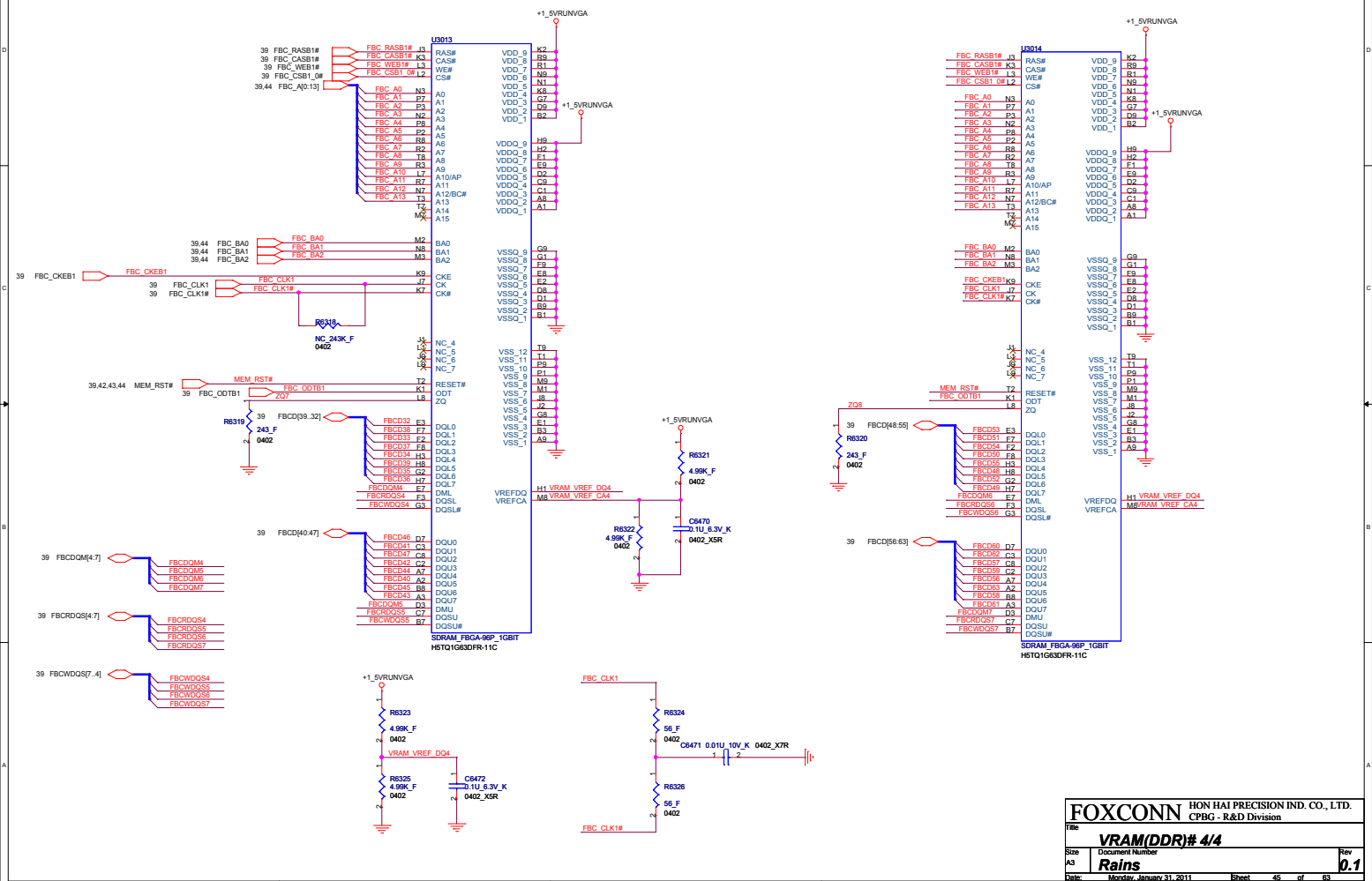








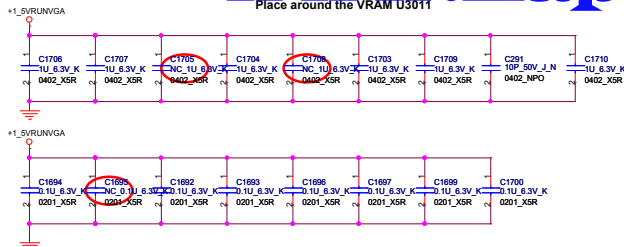




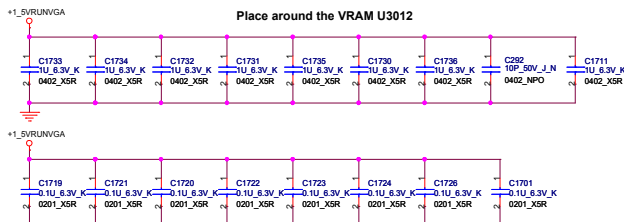


S
t
i
c
h
i
n
g
C
a
p
s

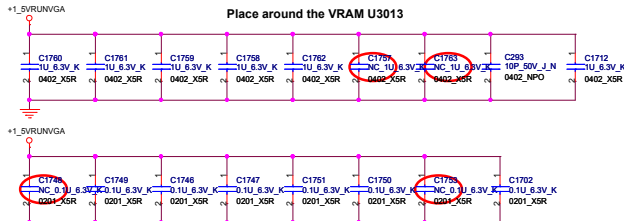
Place around the VRAM U3011



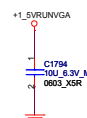
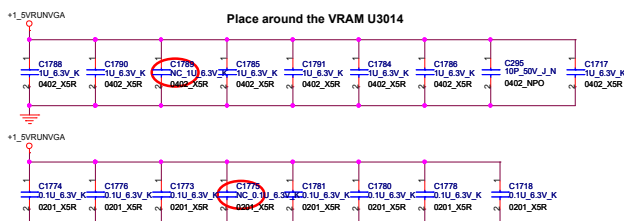
Place around the VRAM U3012



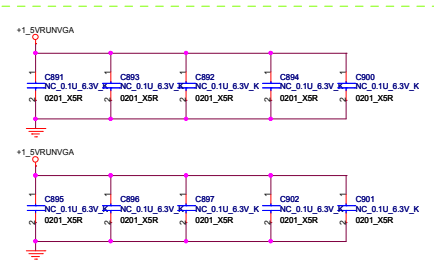
Place around the VRAM U3013



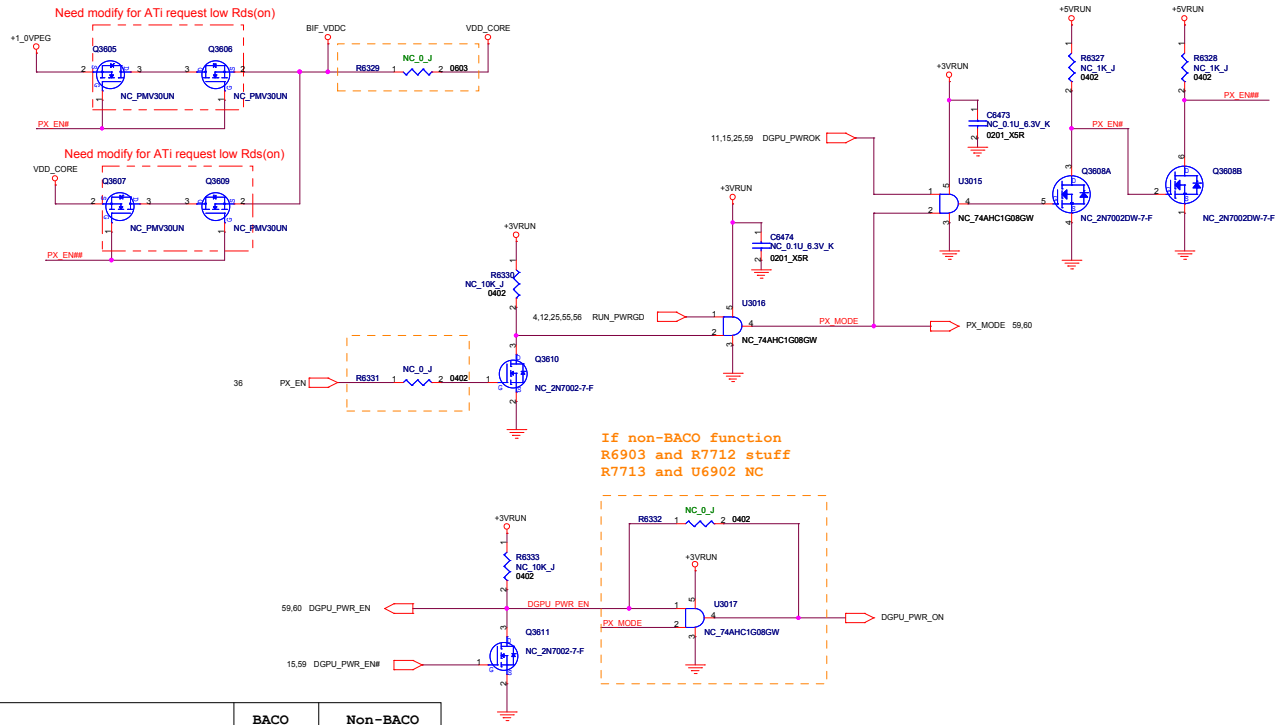
Place around the VRAM U3014



Switching Caps



BACO circuit



	BACO	Non-BACO
R6903, R7712, PR387, PR256	NC	Stuff
Q7703, Q6903, Q7705, Q7706, R7713, R27, Q7707, U7705, C7716, U7702, C7715, R7710, Q6801, R7711, U6902	Stuff	NC
U6902	NC	NC

S1 Stage Power Modify
9/9
P56. PU12 Footprint Change to QPW_11P_20_118X118_P862a95 for SMT issue
9/11
P59,P60 +5VSDS change to +5VALW for Quiescent current

9/13
P51. DC_1W connector FCN1 change to 1N-000400A-M8G2 G873071-10272-7H
9/15
P57. PL19 change to CTX17-18745-R

9/16
P60. PQ49 Footprint change to QPW_5P_26_130 X 130
9/23
P57. PR190,PR195,PR235,PR256 13.7K 0402 1% change to 19.1K 0402 1% for loadline
PR196 change to 8.06K 1% 0402 for SV(48A) IMCW
P54. PR301 change to 31.1K 1% 0402 for USB Voltage Drop

9/28
P59. Del RJ27 for space issue.

9/29
P59. PR184 change to 5.36K 1% 0402 for GFX_IMCW

10/4
P51. Add RJ20 close jump for test reserve
P52. Add RJ27 close jump for test reserve

10/6
P54. Add PR115,PR120,PC103,PC109 2.2ohm 6 680p for EMC request

10/8
P59. PR240 change to 100W F for sequence
P54. PR305 change to 232W for 3VALW OCP point
PR308 change to 301F for 3VALW OCP point

S12 Stage Power Modify
10/30
P53. Add RJ17,RJ32,RJ33,RJ34,RJ35 for IINP accuracy issue

PV Stage Power Modify
11/16
P59. PR241 change to 2.67K for output voltage drop

PV Stage Power Modify
11/17
P51. Del RJ20 close jump,PL1 F12 change to stuff for EMC request
P52. Del RJ27 close jump,PL3 F14 change to stuff for EMC request
P53. Add PC421 for acoustic issue

PV Stage Power Modify
11/19
P51. PR2 change to 1.47K ohm
PR3 change to 604 ohm for LED lighting issue
PR4,PR8,PL1A,PR6,PR7,PQ1 change to no stuff

MV Stage Power Modify
12/15
P59. PR240 From vendor YEAGO to TA-1 for buyer request
Add PD49 BA754 for abnormal waveform issue

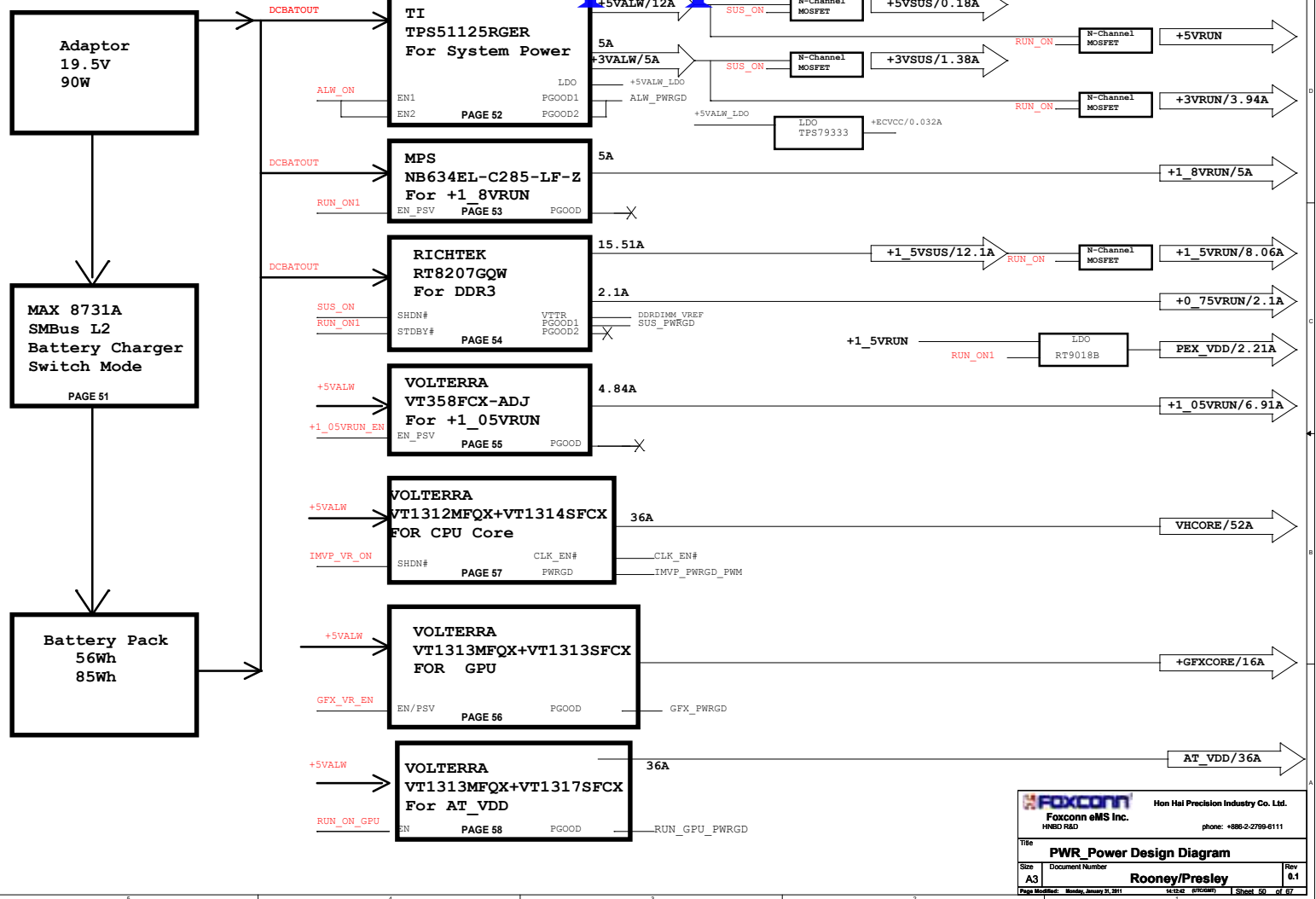
MV Stage Power Modify
12/20
Del P53.RJ2,P54.RJ18 RJ19, P56.RJ9, P59.RJ24 for L6 require

MV Stage Power Modify
12/30
P59. PC420 change to 2200/6.3V
P53. PC421 change to 470/25V

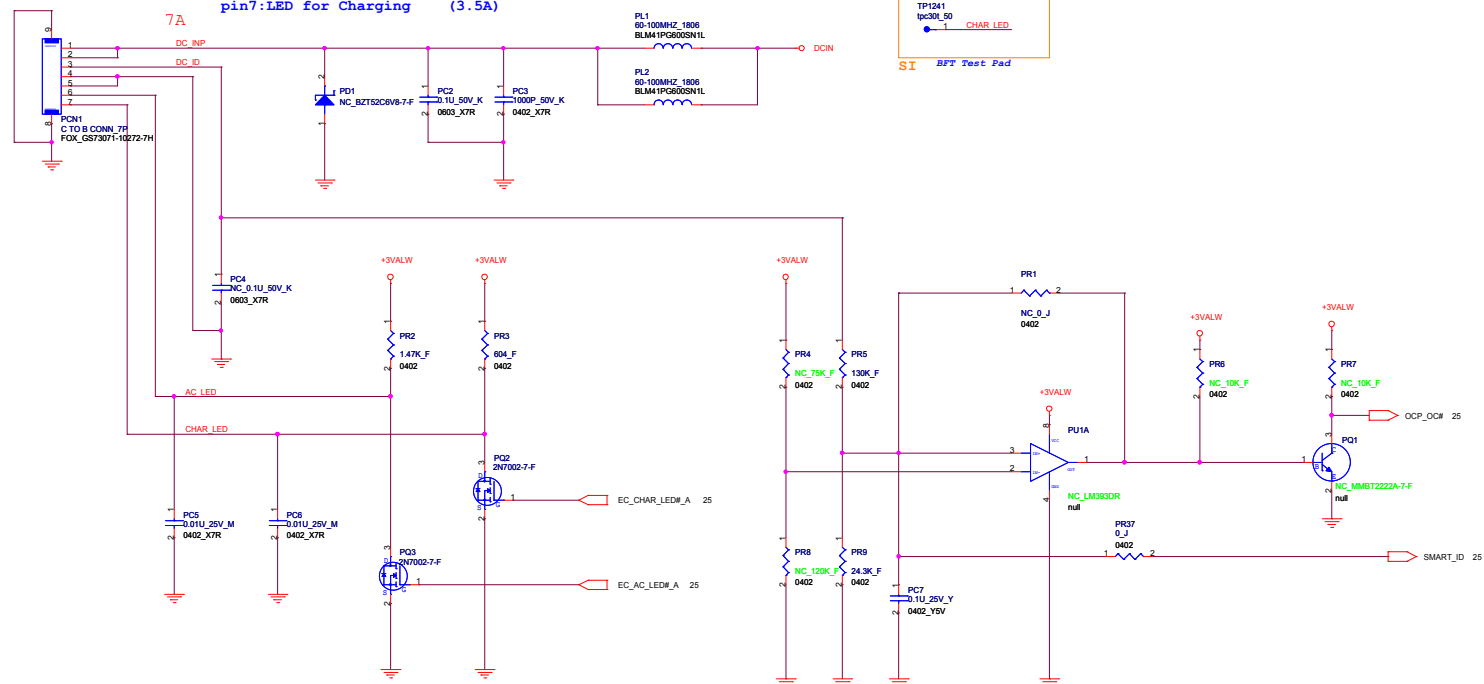
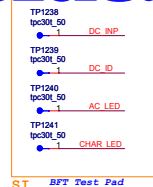


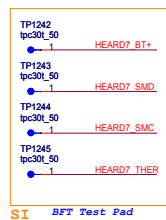
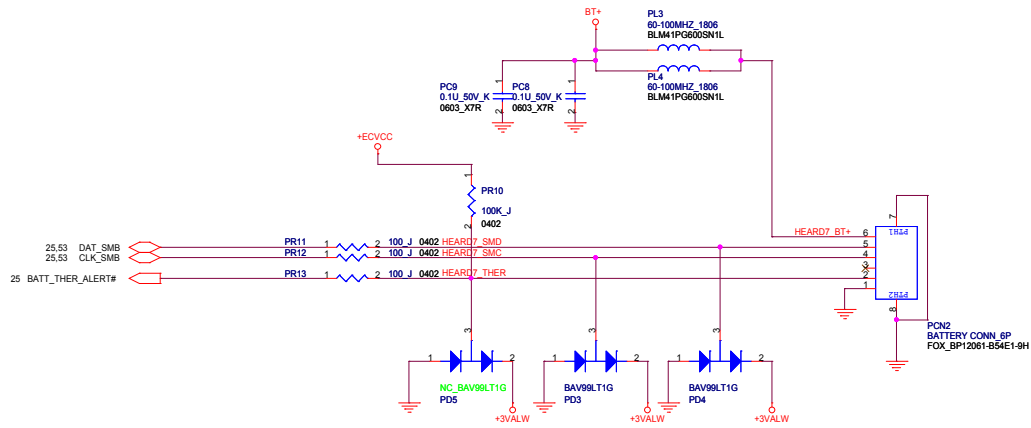
Hon Hai Precision Industry Co. Ltd.
Foxconn eMS Inc.
HNEO R&D
phone: +886-2-2799-6111

Title		Rev 6.1
Power History		
Size A3	Document Number Rains	
Page Modified: Monday, January 21, 2013 14:32:44 (UTC+0800)		Sheet 48 of 57

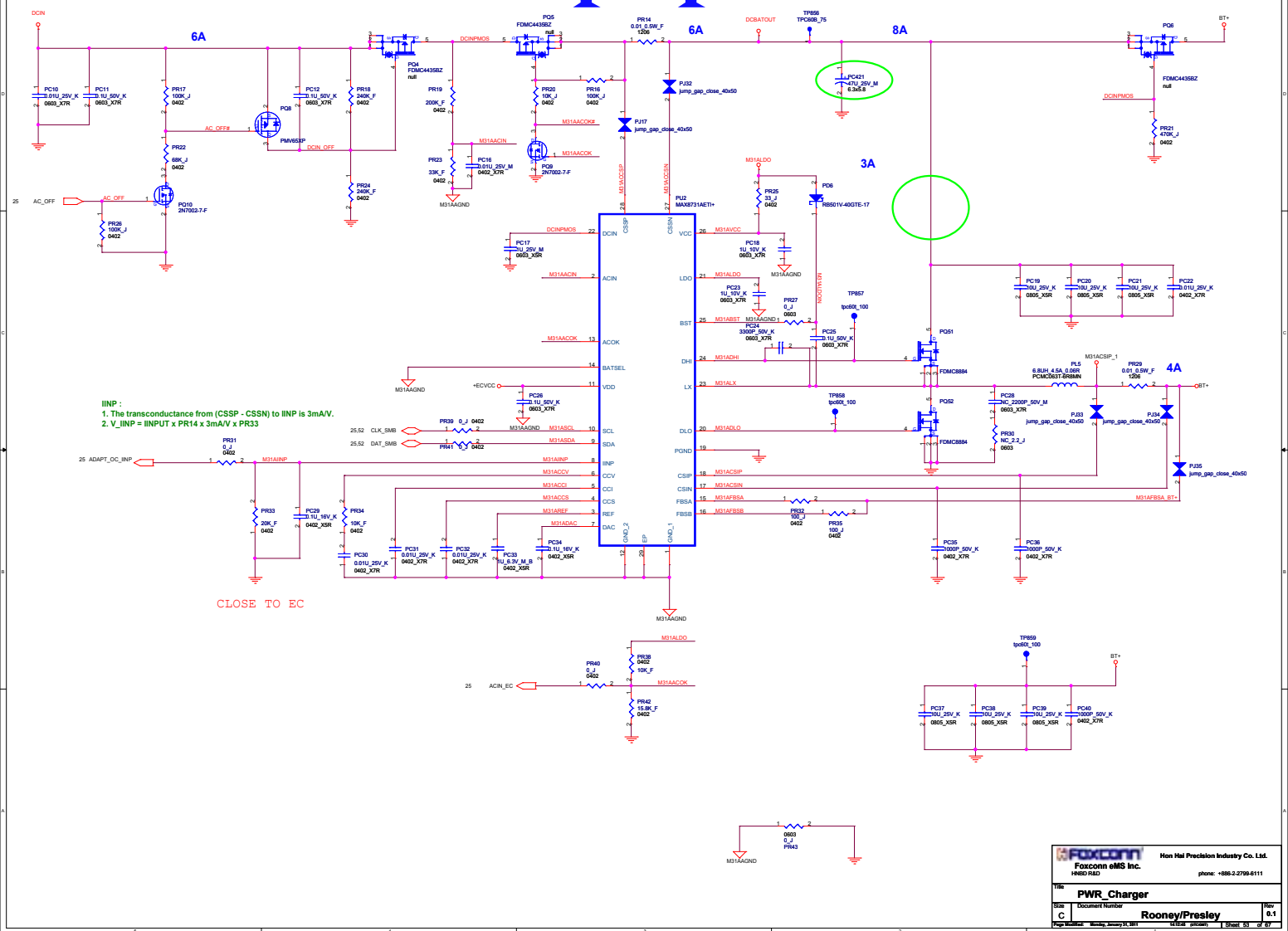



pin1:DC_INP	(3.5A)
pin2:DC_INP	(3.5A)
pin3:DC_ID	(3.5A)
pin4:GND	(3.5A)
pin5:GND	(3.5A)
pin6:LED for AC present	(3.5A)
pin7:LED for Charging	(3.5A)



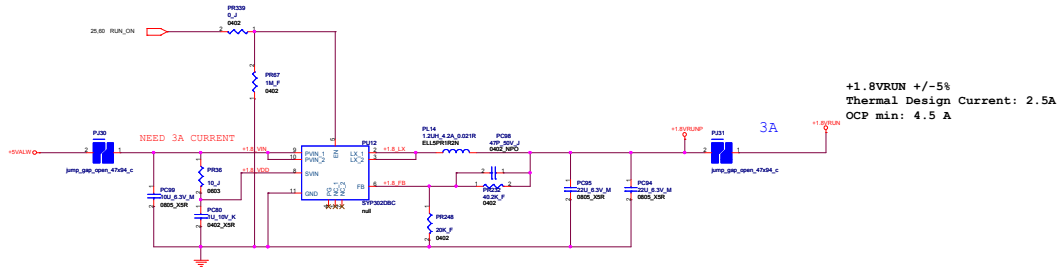
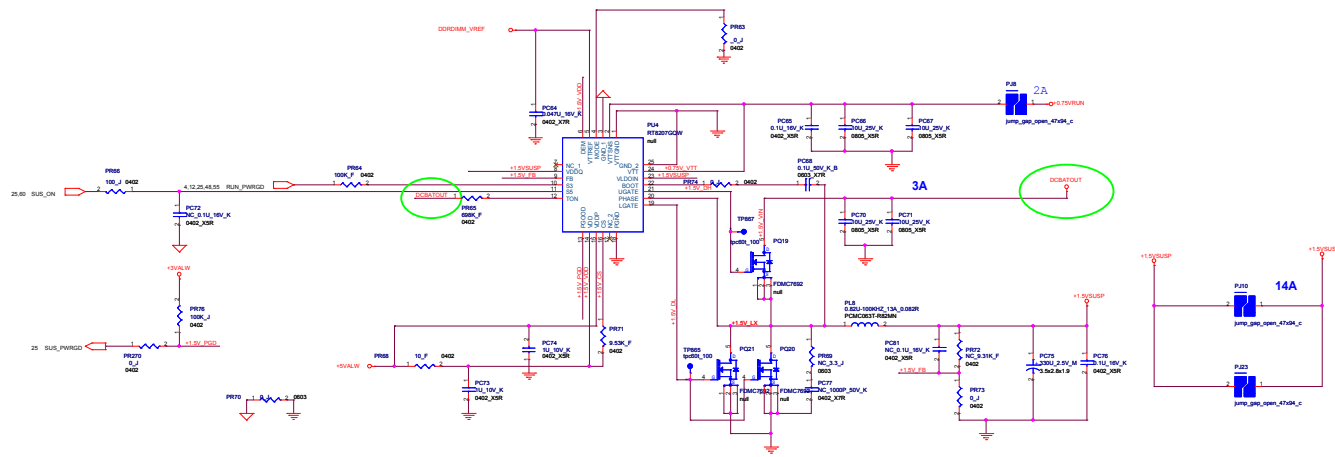


 Foxconn Foxconn eMS Inc. HNBD R&D		Hon Hai Precision Industry Co. Ltd. phone: +886-2-2799-6111	
Title PWR_Battery Conn.			
Size B	Document Number Rooney/Presley	Rev 0.1	
Page Modified: Monday, January 31, 2011 14:12:42 (UTC+0800) Sheet 52 of 67			

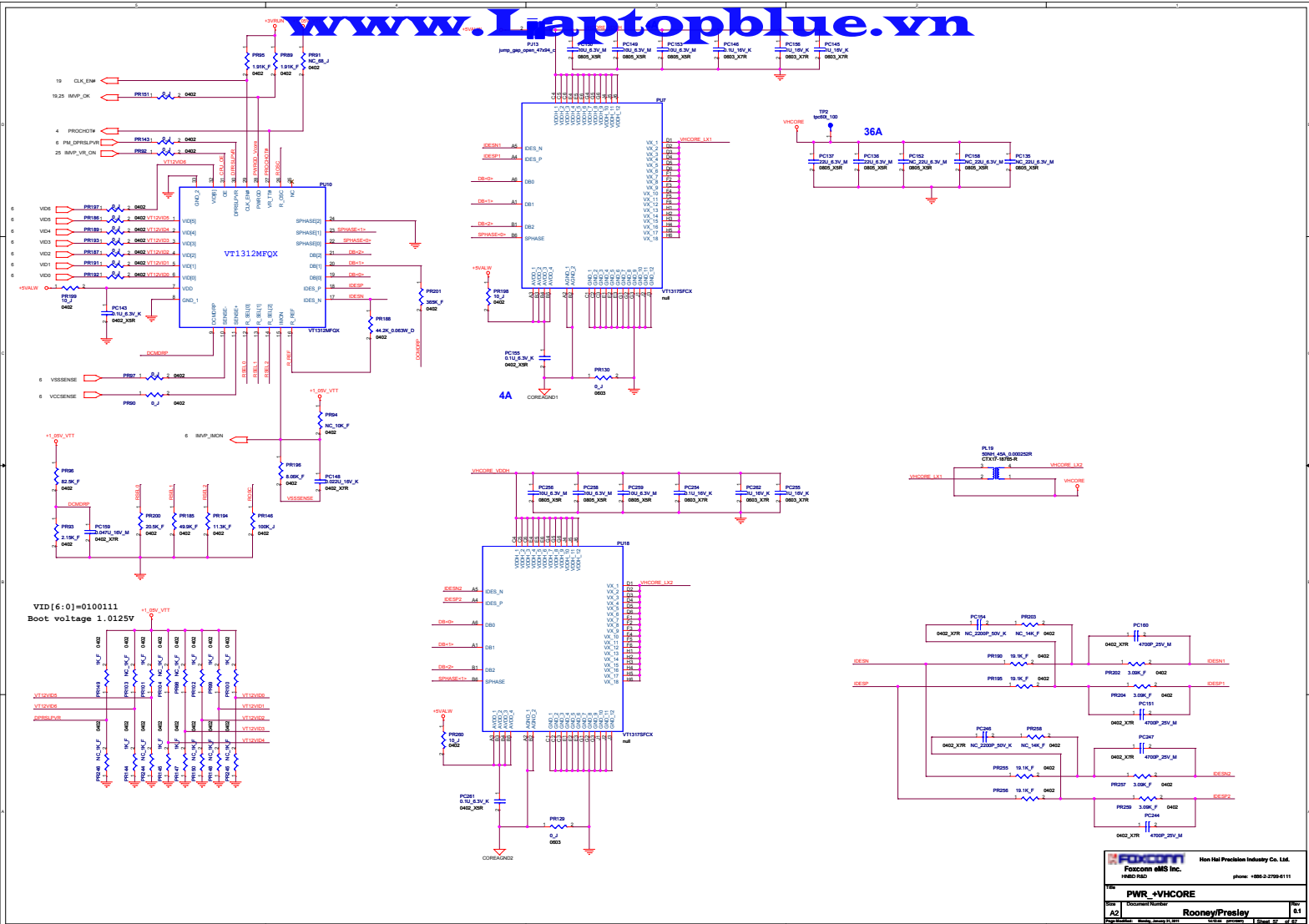


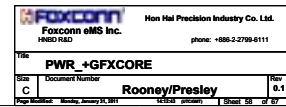
 Foxconn eMS Inc. HNEED R&D		Hon Hai Precision Industry Co. Ltd. phone: +886-3-2799-6111	
Title PWR_Charger			
Size C	Document Number Rooney/Presley		Rev 0.1
Page 1 of 1 Monday, January 31, 2011		1419246 (internal)	Sheet 53 of 67

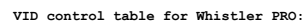




+1.8VRUN +/-5%
Thermal Design Current: 2.5A
OCP min: 4.5 A

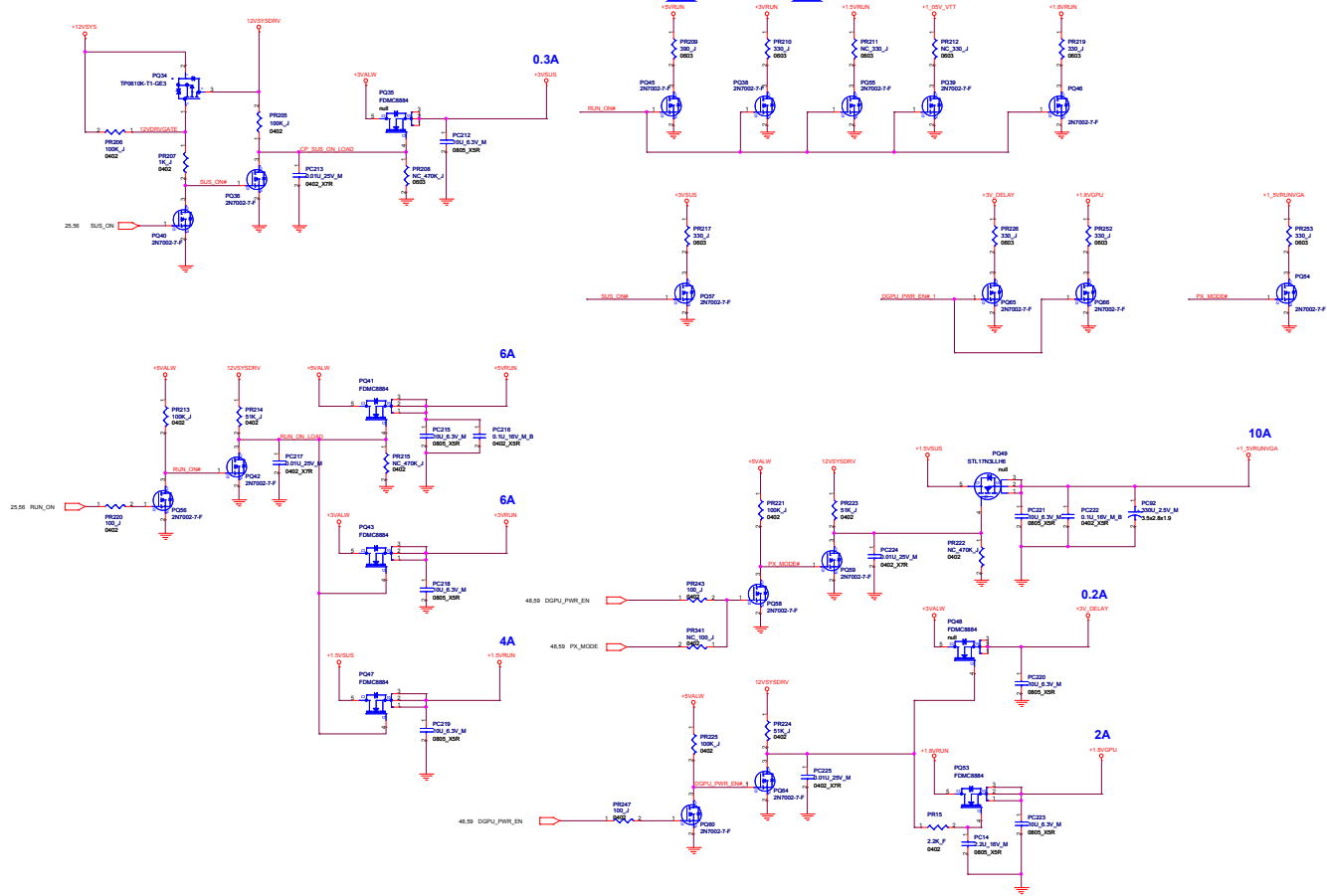






PWRMNTL_0	PWRMNTL_1	GPU Voltage
0	0	1.05V
1	0	1V
1	1	0.9V

$$V_o = (1 + (PR187/PR189)) * 0.8 = 1V$$



Rains DB

(2010/07/29)

- P.25, 28 Del WWAN and KB Backlit for Customer request.
- P.20,21 Swap CN27, CN28 DDR connector.
- P.74 Change Cardreader schematics for customer request.
- P.62 Del RF Solution for RF recommend.
- P.42,43,44,45 Swap VRAM data signals for layout request.

(2010/07/30)

- P.27 Del U57, C966 for unused EEPROM.
- P.61 Del PWR_RF Solution for RF request.
- P.11 Swap LAN & WLAN TX, RX for BIOS request.

(2010/08/02)

- P.29 Change input to SATA Re-Driver U71 net name to SATA_TXP0_R,SATA_TXN0_R, SATA_RXP0_R,SATA_RXN0_R
- P.42~45 Change +1.5VVRUN to +1.5VVRUNVGA for VRAM part.
- P.38 NC R1894, R1896, R1898, R254 and Reserve R255, R256, R257 for DAC2.
- P.36 NC U62.U13 and U62.V13 for AMD recommend.
- P.38 Add R9933, R9934 51.1K for AMD recommend.

(2010/08/03)

- P.28 Connect CN42(WLAN) pin 42, 44, 46 together for BIOS request.
- P.46 Add C1605, C1606, C1607, C1608, C1609, C1610, C1617, C1618 for AMD request.
- P.47 Add C1700, C1701, C1702, C1710, C1711, C1712, C1717, C1718 for AMD request.
- P.46 Del C1168, C1169, C1144, C1212, C1203, C1205, C1662, C1659, C1661, C1689, C1686, C1688, C1690, C1903 for AMD request.
- P.47 Del C1716, C1713, C1714, C1743, C1740, C1742, C1793, C1782, C1792, C1797, C1795, C1796 for AMD request.
- P.14 Add R687 to connect CLK_33M_Debug for customer debug card.
- P.28 Reserve R591 for customer debug card.
- P.27 Add R2803 to +3VALW for EE debug.
- P.23 Del R65, R67, R68, R75 for PDD drop.
- P.35 Del Bluetooth and LED board connector CN57 for customer drop.
- P.35 Add CN3 USB3.0 connector.
- P.25 Add PCIE_APM# in U91.123 and R579 for BIOS request.
- P.14 Del R397 for BIOS request.
- P.31 Del Bluetooth power Q85 and relative schematics for PDD drop.
- P.25 Del Q2602 and Add Q2601 for Bluetooth and wireless LED feature.

(2010/08/05)

- P.25 Add R583 and U91.89 to USB_PWR_EN for BIOS recommend.
- P.35 Change CN3.28 form SUS_ON to USB_PWR_EN.
- P.32 Add R31, R548, R563, R559, R561, R562, R564, C464 for vendor recommend.
- P.31 Add CN6 Camera connector for customer recommend.
- P.28 Add R589, LPC_AD0~3 and LPC FRAME# for HP debug card.
- P.30 Change C6447 & C6448 from 0201 to 0402.
- P.38 Add Q3 for SMBUS level shift.
- P.23 Change CN38 to 30pin and del camera relative schematics.

(2010/08/06)

- P.65 Change R6199 from 47K to 10K ohms
- P.33 Del R6193 for vondor suggestion

- P.32 Change C151 from 0.1u to 0.1 for vendor suggestion
- P.33 Change R6190 from 150k to 100k for vendor suggestion
- P.30 CN3 pin 30 connect to SUS_PWRGD

(2010/08/10)

- P.10 Add R349, R350, R351, R352 33 ohm for LPC_A0~3 debug.
- P.66 Modify U61 relative schematics and del U3200 and D3200.
- P.14 Del USB Port 0 & Port 9 NC for unused.
- P.66 Add CN7 Audio MB to DB connector.
- P.33 Change internal speaker net name to SPK-L+_L, SPK-L-_L, SPK-R+_L, SPK-R-_L.
- P.61 Del all of PWR RF solution for unused WWAN.

(2010/08/11)

- P.49 Add Screw Hole.
- P.23 Change C925 from 0402 to 0603 for derating issue.
- P.11 Del R622 for unused.
- P.7~47 Change C645, C264, C267, C266, C268, C269, C277, C273, C274, C1813, C1814, C447, C1818, C449, C448, C429, C356, C424, C308, C950, C984, C987, C1038, C1005, C926, C279, C282, C281, C284, C288, C289, C290, C291, C292, C293, C295 from 33p to 10p for RF recommend.
- P.32 Change CN43 cardreader connector for ME request.

(2010/08/12)

- P.15 Change Net Name LCDID1 to GPIO37, LCDID4 to GPIO48.
- P.15 Del R6105, R6103 and change R6113, R6100 to connect with +3VRUN.
- P.11 Change CLK_PCIE_CR and CR_CLK_REQ# to PCIECLKRQ4#.
- P.14 Del INT_PIRQ# and RP17.7, JP6, JP7.
- P.15 Del JP2, JP3, JP4 for unused.
- P.11 Del JP5 for unused.
- P.15 Change GPIO37 net name to DGPU_PRSENT# and Add R6116.
- P.25 Connect U91.118 to PCI_SERR# for Debug request.
- P.11 Add TP374, TP375 for reserve DGPU select.

(2010/08/13)

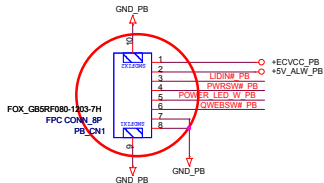
- P.25 Add R3, R4, R5, R6 for reserving TP power.
- P.25 Add R580, Net QWEBSW# and TP_LED_A for customer request.
- P.25 Add CN33, C2608, C2611 for TP LED.
- P.35 Change CN56, CN3 Power board and USB3.0 connector to DB.
- P.35 Add Q4202 for PWR LED.
- P.34 Change CN7 Audio DB connector for ME request.
- P.31 Change CN42 WLAN connector for ME request.
- P.24 Change CN32 HDMI connector.
- P.22 Change CN37 CRT connector.

(2010/08/16)

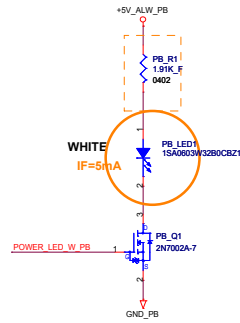
- P.34 Change CN7 pin define.
- P.10 Swap CN25 pin 1 & 2 for ME request.
- P.29 Change CN52 SATA HDD connector.
- P.06 Add R403, R404 for EE measurement.
- P.07 Add R400, R406, R407, R408 for EE measurement.
- P.16 Add R409, R265 for EE measurement.
- P.17 Add R410 for EE measurement.

 Foxconn eMS Inc. HNEO R&D		Hon Hai Precision Industry Co. Ltd. phone: +886-2-2799-6111	
Title		History	
Size	Document Number	Rev	
A3		8.1	
Page Modified: Monday, January 25, 2011		14:24:41 (UTC+08)	Sheet 61 of 67

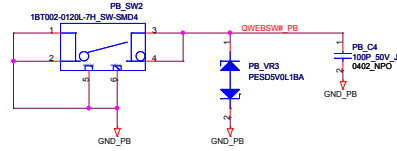
DB To MB Conn.



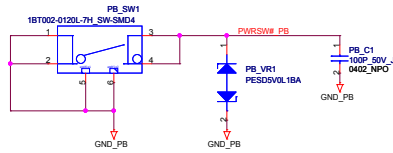
Power LED



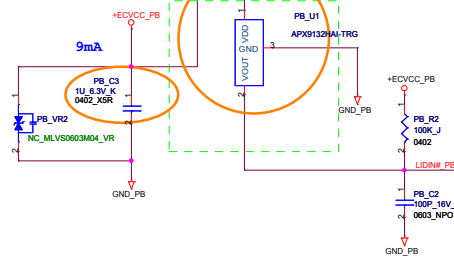
QuickWeb Button



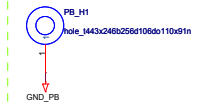
Power Button



LID SWITCH



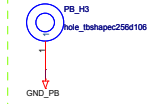
A +C + D Type



G Type



A + A Type



B Type



F + E Type



 Foxconn Foxconn eMS Inc. HNEO R&D		Hon Hai Precision Industry Co. Ltd. phone: +886-2-2799-6111	
Title DB_POWER BUTTON			
Size A3	Document Number Rains HR	Rev M1	
Page Modified: Monday, January 21, 2013 11:42:46 (UTC+08)		Sheet 61 of 66	

Rains DB

(2010/08/17)

- P.46 Add Stitching Caps C883~C890, C898, C899 for AMD request.
- P.47 Add Stitching Caps C891~C897, C900~C902 for AMD request.
- P.23 Modify CN38 LVDS pin dinfine.

(2010/08/18)

- P.32 Change cardreader GND Power to GND.
- P.25 Del R3, R4, R5, R6 for unused reserve.
- P.25 Add R2620, R2621 for Wireless LED debug.
- P.25 Change CN33 and EC pin name to TP_LED#.
- P.34 Change H1 GND to A_GND.
- P.27 Swap CN30 LAN connector A1, A2 and B1,B2 for vendor recommend.
- P.33 Add SW1 and C5 for Power button and change CN56.2 to +5VALW.
- P.23 Change CN38.27 to +5VRUN and add C608.
- P.34 Add Boss1~6 for ME request.

(2010/08/19)

- P.25 Del TP1151 for unused.
- P.07 Del R408 for release space.
- P.34 Connect H5, H6, H12, H13 to GND.
- P.20 Add C445, C453 for power plane.
- P.34 Add C457, C458, C459, C478 for power plane.
- P.29 Add R2~R9 for reserving remove SATA redriver.

(2010/08/20)

- P.34 Change H9, Boss1~7 for ME request.

Rains SI

(2010/09/03)

- P.11 Change CR_RXN8, CR_RXP8, CR_TXN8, CR_TXP8 to U38 PCIE port4 for EE debug.
- P.29 Change U71 power pin name to 1.5VRUN for EE debug.
- P.27 Change CN30 LAN connector pin define for EE debug.
- P.28 Change R3007 to connect with SENSEA and Q3002A.6 for EE debug.

(2010/09/09)

- P.33 Change CN3 pin 12 & 27 define to +3VRUN and USB30_SMI for EE request.

(2010/09/12)

- P.23 Change LVDS connector pin define for ME request.
- P.27 Change L103 LAN Transformer for EE debug.

(2010/09/13)

- P.23 Rotate LVDS connector pin define for ME request.
- P.28 Change SENSEA and COMBO_JACK_DET# in Q3000, R6205 for EE debug.

(2010/09/15)

- P.10 Change CN25 RTC pin define for ME request.
- P.25 Change CN52 HDD pin define for ME request.
- P.31 Del CN6, L73, L74, C733, C718 Camera connector for ME request.

(2010/09/20)

- P.33 Change CN3 USB3.0 connector pin define +3VRUN and USB30_SMI.

(2010/09/24)

- P.22 Change CRT connector CN37 for ME request.
- P.24 Change HDMI connector CN32 for ME request.
- P.25 Change KB connector CN54 for ME request.
- P.27 Change LAN connector CN30 for ME request.
- P.29 Change HDD connector CN52 for ME request.
- P.31 Add WLAN BTB connector CN17 for ME request.
- P.32 Change Cardreader connector CN43 for ME request.
- P.33 Change USB3.0 BTB connector CN3 for ME request.
- P.35 Add WLAN DB schematics for ME request.
- P.25 Change Y13 for cost down.

(2010/09/28)

- P.41 Add CAP13 in VDDCore for Power request.
- P.33 Change CN3.2 to GND for EE request.
- P.25 Add R12, Q4 for Mute LED debug.
- P.28 Change U50.46 net name to MUTE_LED_A.
- P.25 Add R13 for CAPSLOCK_LED# and CAPSLOCK_LED#_R.
- P.35 Change GND to W_GND for DB.
- P.23 Change C1006 from 0603 to 0402 1u and C1863 for EE debug.
- P.23 Change R12 to connect to MUTE_LED#_A.

(2010/09/29)

- P.28 Del D12 and Add Q103 for Audio Mute debug.

(2010/09/30)

- P.23 Del R67~R77 and chang the LVDS net name for EE recommend.

(2010/10/04)

- P.15 Change G_INT#_LED net name to G_INT_LED for high active.
- P.33 Change G_INT#_LED net name to G_INT_LED for high active.
- P.25 Del Q2601, Q3604, R2620 and Add Q7, Q8, Q9, Q12, Q14, R30, R33 for EE debug WLAN LED.
- P.17 Add C823 22uF for EE solve CRT water wave issue.

(2010/10/05)

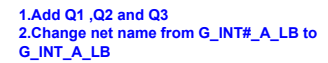
- P.31 Del CN17 WLAN DB BTB connector for ME request.
- P.35 Del W_CN1 & W_CN2 for ME request.
- P.17 Add C484 0.1uF for reserving CRT water wave issue.

(2010/10/07)

- P.32 Co-lay CN44 cardreader connector for introducing 2nd source
- P.34 Update all of the screw hole.

 Foxconn eMS Inc. HNEO R&D		Hon Hai Precision Industry Co. Ltd. phone: +886-2-2799-6111	
Title		History (2)	
Size	A3	Document Number	Rev 6.1
Page Modified: Monday, January 25, 2011 14:24 (UTC+8)		Rains Sheet 52 of 57	

HDD LED



Rains PV

(2010/10/28)

- P.4 Change R192, R180, R195, R63, R64, R708, R709, R969 to close gap.
- P.7 Change R407 to PGP9 for EE cost down.
- P.10 Change R160, R6039, R6052, R6065 to PGP10~13 for EE cost down.
- P.11 Change R623 to PGP15 for EE cost down.
- P.12 Change R279, R345, R280, R370, R368 to PGP16~20 for EE cost down.
- P.13 Change R628, R629, R657, R658, R669, R655 to PGP21~26 for EE cost down.
- P.14 Change R1403, R398 to PGP27~28 for EE cost down.
- P.15 Change R393 to PGP 29 for EE cost down.
- P.16 Change R258, R298 to PGP 30~31 for EE cost down.
- P.17 Change R227, R514, R735, R221, R498, R497 to PGP 32~37 for EE cost down.
- P.23 Change R527, R65, R62, R266 to PGP 38~41 for EE cost down.
- P.24 Del R2409~R2416 for EE cost down.
- P.33 Del R6229, R596 for EE cost down.

(2010/11/02)

- P.4 Add CPU_DET# for EC request.
- P.25 Add R6193, R302, DGPU_PWROK, CPU_DET# for EC request.

(2010/11/17)

- P.64 Change PB_CN1 pin define for ME request.
- P.24 Del R333,Q28, R334 for changing VGA HW_SD.
- P.24 Add U45, U46, Q50, C749, C752, R2617, R871, R877 for VGA HW Shut down.

(2010/11/18)

- P.24 Del TP997 and add R593 connect to EC_WP# for Flash Write Protect.
- P.10 Add R226 to connect EC_WP# for Flash Write Protect.

(2010/11/19)

- P.33 Swap CN56 Power board connector for ME request.
- P.64 Recover PB_CN1 pin define for ME request.
- P.10 Del R245 and add Q15, R107 for EC_WP#.
- P.26 Add Q17 and R108, R9902 for EC_WP#.
- P.35 Add Q73, Q81, R247, R241, R2909, Q2902 for Headphone jack mute.
- P.24 Del R6123~R6130 and Q97, R6132 for HDMI quality.

(2010/11/22)

- P.23 Add R73, R74, C19, C20, L63, Q28 for LVDS DCBATOUT.

Rains MV

(2010/12/3)

- P.24 Add R763,R764 and connect DGPU_HPD_INTR# to Q64.1 pin for HDMI debug.

(2010/12/16)

- P.33 Del SW1 & C5 for EE cost down.
- P.10 NC CN13, U35, R490, C691 and stuff R6040 for EE cost down.

(2010/12/17)

- P.29 Del R6357 for EE cost down.

(2010/12/28)

- P.29 Add TP960 for L6 request.

Rains1.1 PV

(2011/1/31)

- P.26 Change EC_WP# to EC_WP and add U12, C145, R108 latch for HP request.
- P.10 Change EC_WP# to SPI_PROTECT.

Rains1.1 PV

(2011/1/31)

- P.25 Change PCB ID to ID[3..0]:1001, stuff R6175 and no-stuff R6176.
- P.59 Change PR240 to 10K and PR342 to 33K for VGA loss issue

 Foxconn eMS Inc. HNEO R&D		Hon Hai Precision Industry Co. Ltd. phone: +886-2-2799-6111	
Title		History (3)	
Size	Document Number		Rev
A3	Rains		6.1
Page Modified: Monday, January 24, 2011		14:23:31 6/16/2011	Sheet 63 of 67