

Model : Calpella

PCB1
PCB
37GC42200-C0

Intel Calpella CPU + Intel PCH Chipset

C42IIX Main BD REV.C
P/N: 37GC42200-C0
Made in China

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16	Ibex Peak_Power1_g	
17	Ibex Peak_Power2_h	
18	Ibex Peak_M_GND	
19	CLOCK GEN (ICS9LRS3197)	
20	LCD	
21	CRT/TPM/G-SENSOR	
22	MINI CARD/ODD/HDD/MDC CON	
23	CCD/BT/USB CON/3G & LED	
24	LAN - RTL8111DL-GR	
25	DVI SHIFTER/HDMI	
26	Audio Codec ALC269	
27	EC-IT8502NX/BIOS/FAN	
28	POWER SWITCH	
29	DC IN & CHARGER (OZ8618)	
30	+CPU_CORE (OZ8291)	
31	+GFX_CORE (OZ8291)	
32	0.75_DDR/1.8VS/1.1VS	
33	+1.1VS_VTT (OZ8111)	
34	+1.5 (OZ8116)	
35		
36		

AOI	ICT	ATS	CHR	I/D	F/T	PCBA	T/Q

Revision History		
	8/2009	Initial RA
	10/2009	RB
	12/2009	RC



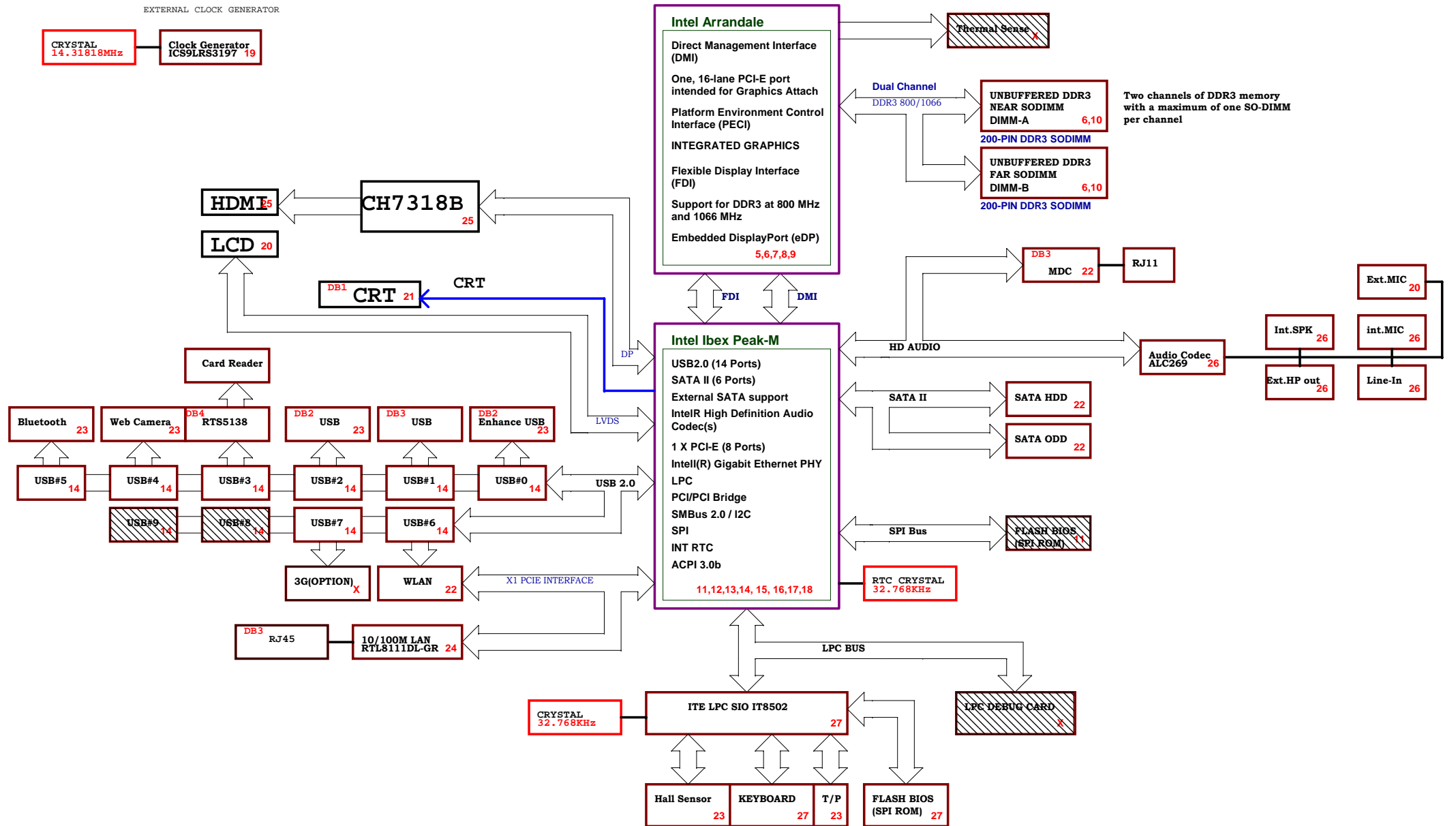
ECS COMPUTER CORP.

Title			COVER PAGE
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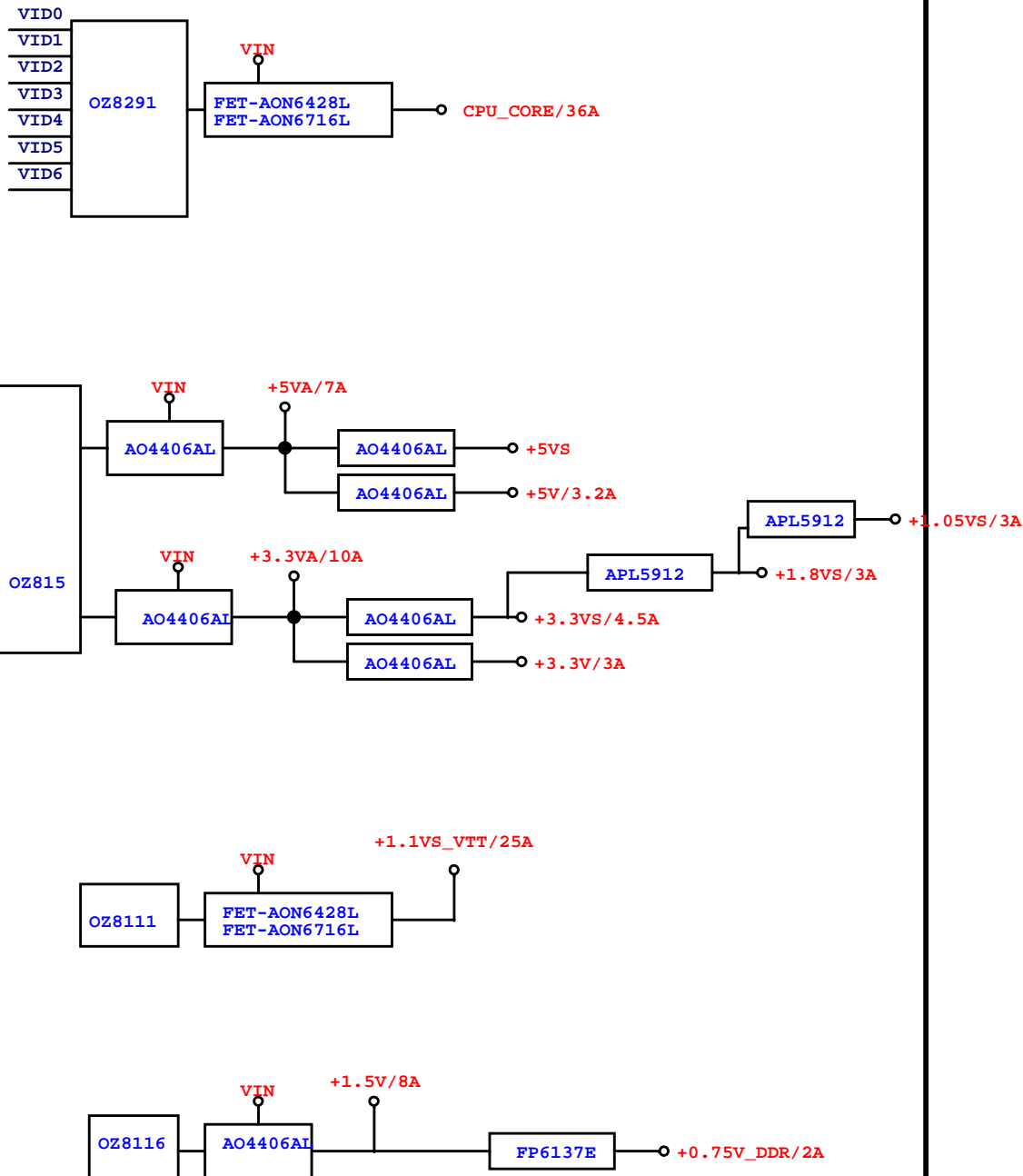
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C42IIX Calpella

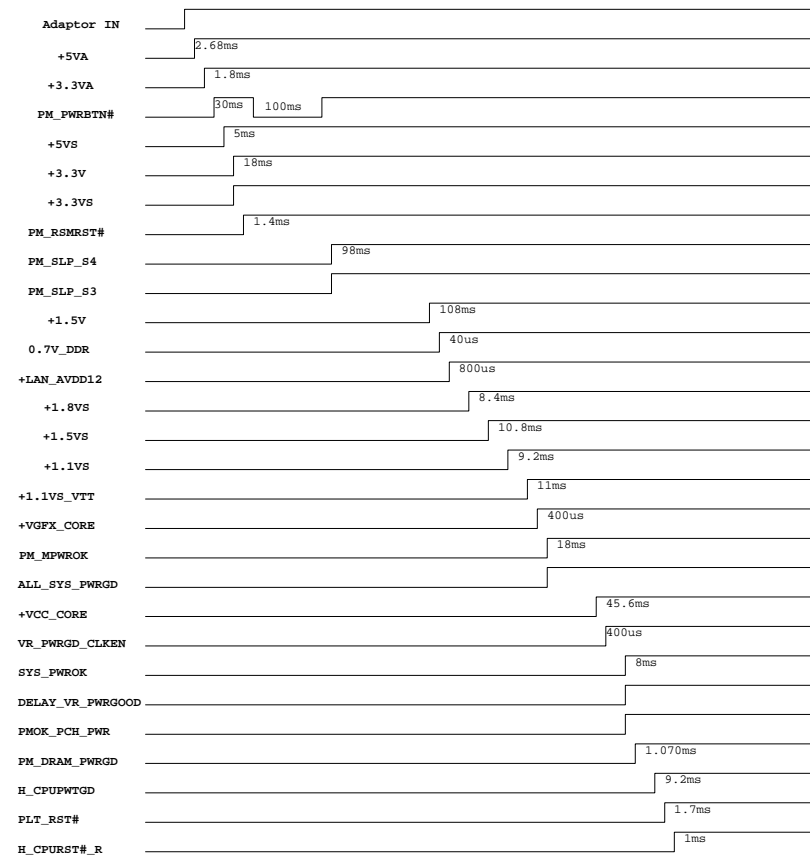
SYSTEM BLOCK DIAGRAM



POWER BLOCK DIAGRAM



Power up sequence



PCH GPIO	
GPIO0	S_GPIO
GPIO1	SMC_RUNTIME_SCI#
GPIO2	INT_PIRQ#
GPIO3	INT_PIRQ#
GPIO4	INT_PIRQ#
GPIO5	INT_PIRQ#
GPIO6	DGPU_HPD_INTR#
GPIO7	NC
GPIO8	HOST_ALERT#2
GPIO9	USB_OC#_10_11
GPIO10	USB_OC#_12_13
GPIO12	GPIO12
GPIO13	NC
GPIO14	USB_OC#_13_14
GPIO15	HOST_ALERT#1
GPIO16	DGPU_HOLD_RST#
GPIO17	DGPU_PWROK
GPIO18	CLK_MINI1_OE#
GPIO19	SATA_DET1#
GPIO20	CLK_PCIE_LAN_REQ#
GPIO21	SATA_DET0#
GPIO22	BIOS_REC
GPIO23	NC
GPIO24	NC
GPIO25	NC
GPIO26	NC
GPIO27	NC
GPIO28	SPI_CS#2
GPIO29	USB_OC#5
GPIO30	SUB_PWR_ACK
GPIO31	AC_PRESENT
GPIO32	PM_CLKRUN#
GPIO33	HDADOCKEN#_R
GPIO34	NC
GPIO35	NC
GPIO36	DGPU_PWR_EN#
GPIO37	DGPU_PRSENT#
GPIO38	MFG_MODE
GPIO39	CRB_SV_DET
GPIO40	USB_OC#_2_3
GPIO41	USB_OC#_4_5
GPIO42	USB_OC#_6_7
GPIO43	USB_OC#_8_9
GPIO50	PCI_REQ#1
GPIO51	PCI_GNT#1
GPIO52	DGPU_SELECT#
GPIO53	NC
GPIO54	PCI_REQ#3
GPIO55	PCI_GNT#3
GPIO44	NC
GPIO45	NC
GPIO46	RST_GATE
GPIO48	SV_SET_UP
GPIO49	CRIT_TEMP_REP#_R
GPIO56	NC
GPIO57	PCH_GPIO57
GPIO58	SMB1_CLK_EC
GPIO59	USB_OC#_0_1
GPIO61	PM_SUS_STAT#
GPIO72	PM_BATTLOW#
GPIO74	LPD_SPI_INTR#
GPIO75	SMB1_DAT_EC

ITE8502NX GPIO Pin Definition list	
GPA0	BTL_BEEP
GPA1	EC_BL_PWM
GPA2	LS_OFF#
GPA3	CCD_EN
GPA4	RF_LED_EC#
GPA5	Mini_Card_PWR_ON#
GPA6	MINI_RFON
GPA7	BT_ON
GPB0	SENBAT_V
GPB1	ALL_SYS_PWRGD
GPB2	+1.1VS_ON
GPB3	BAT_SMBCLK
GPB4	BAT_SMBDAT
GPB5	H_A20GATE
GPB6	H_RCIN#
GPB7	VCORE_ON
GPC0	+1.8VS_ON
GPC1	SMB_CLK_EC_CLK
GPC2	SMB_DATA_EC_CLK
GPC3	SAFETY
GPC4	+3.3VS_ON
GPC5	+5VS_ON
GPC6	+1.1VS_VTT_ON
GPC7	PM_PWRBTN#
GPD0	AC_IN
GPD1	INT1
GPD2	PLT_RST#
GPD3	ECSCI#
GPD4	
GPD5	AC_PRESENT
GPD6	+1.5V_ON
GPD7	+1.5VS_ON
GPE0	PM_RSMRST#
GPE1	VGA_CORE_ON
GPE2	PM_MPWROK
GPE3	+1.8VS_ON_ATI
GPE4	PWRON
GPE5	VDDR3_ON
GPE6	Low Voltage
GPE7	MUTE_AMP#
GPF0	EC_PROCHOT
GPF1	CHG_R_LED
GPF2	CHG_B_LED
GPF3	PWR_LED
GPF4	TP_CLK
GPF5	TP_DATA
GPF6	SMB_CLK_G
GPF7	SMB_DATA_G
GPH0	PWR_KEEP
GPH1	GPIO33
GPH2	
GPH3	PCH_SPI_CS
GPH4	PCH_SPI_CLK
GPH5	PCH_SPI_SO
GPH6	PCH_SPI_SI
GPG1	+3.3V_ON
ADC0/GPI0	BATT_TEMP
ADC1/GPI1	ADAPTOR_I
ADC2/GPI2	BAT_I
ADC3/GPI3	BAT_V
ADC4/GPI4	RF_SW
ADC5/GPI5	PM_SLP_S4#
ADC6/GPI6	PM_SLP_S3#
ADC7/GPI7	SUB_PWR_ACK

ITE8502NX I2C to	
DAC0/GPJ0	Fast-charge-EN
DAC0/GPJ1	CHG_I
DAC0/GPJ2	FAN_CTRL1
DAC0/GPJ3	CHG_ON
DAC0/GPJ4	USB0_EN#
DAC0/GPJ5	SET_V

ITE8502NX KB Matrlk interface	
KS10/STB#	KB_SIN0
KS11/AFD#	KB_SIN1
KS12/INIT#	KB_SIN2
KS13SLIN#	KB_SIN3
KS14	KB_SIN4
KS15	KB_SIN5
KS16	KB_SIN6
KS17	KB_SIN7
KS00/PD0	KB_SOUT0
KS01/PD1	KB_SOUT1
KS02/PD2	KB_SOUT2
KS03/PD3	KB_SOUT3
KS04/PD4	KB_SOUT4
KS05/PD5	KB_SOUT5
KS06/PD6	KB_SOUT6
KS07/PD7	KB_SOUT7
KS08/ACK#	KB_SOUT8
KS09/BUSY	KB_SOUT9
KS010/PE	KB_SOUT10
KS011/ERR#	KB_SOUT11
KS012/SLCT	KB_SOUT12
KS013	KB_SOUT13
KS014	KB_SOUT14
KS015	KB_SOUT15

ITE8502NX SPI Flash ROM interface	
FLFRAME#/GPG2	FLFRAME#
FLAD0/SCE#	EC_SPI_CS#
FLAD1/S1	EC_SPI_SI
FLAD2/S2	EC_SPI_SO
FLAD3/GPG6	LID#
FLCLK/SCK	EC_SPI_CLK
FLRST#/WU17 /GPG0 /TW	LCDSW

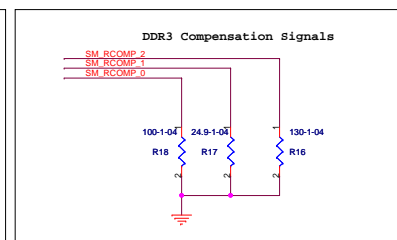
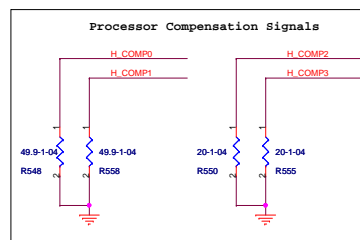
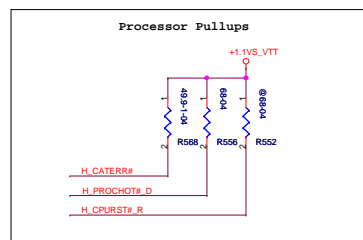
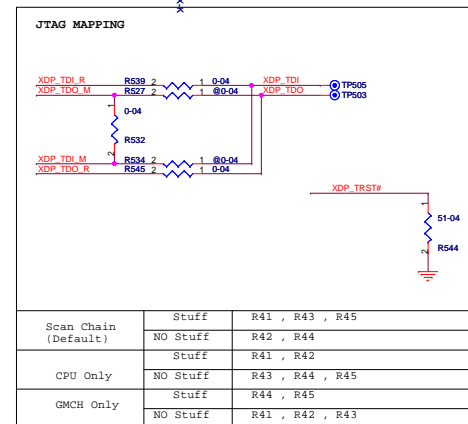
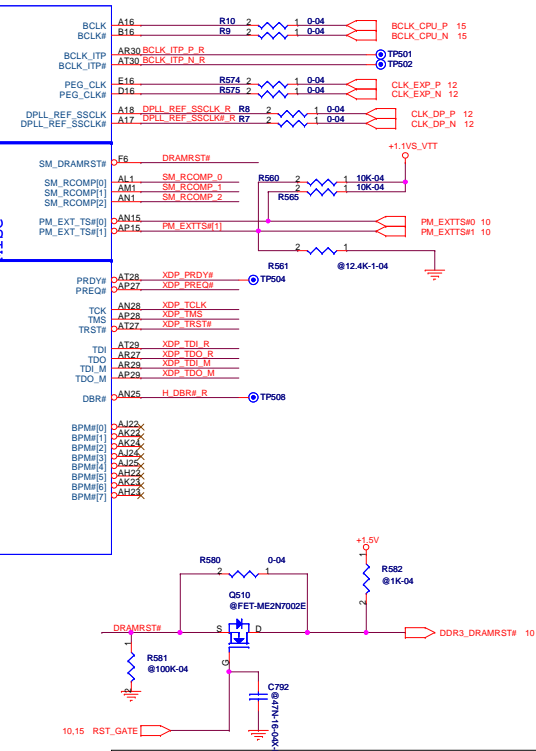
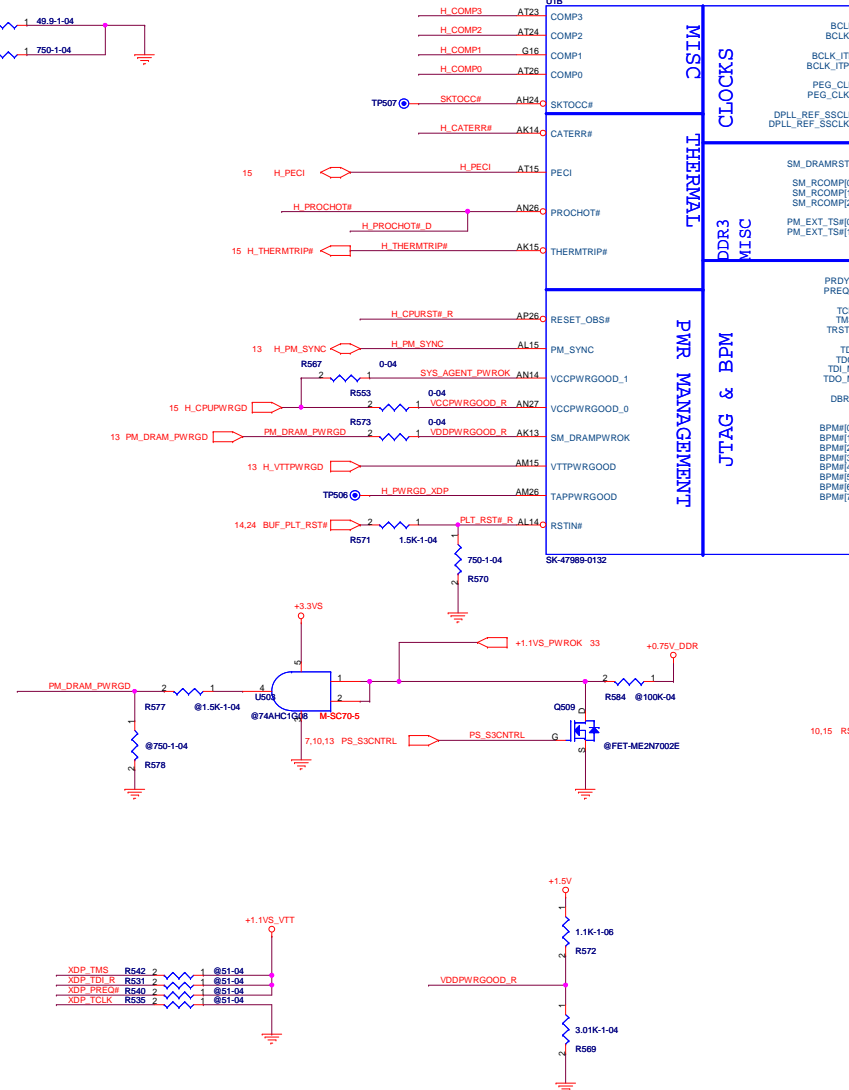
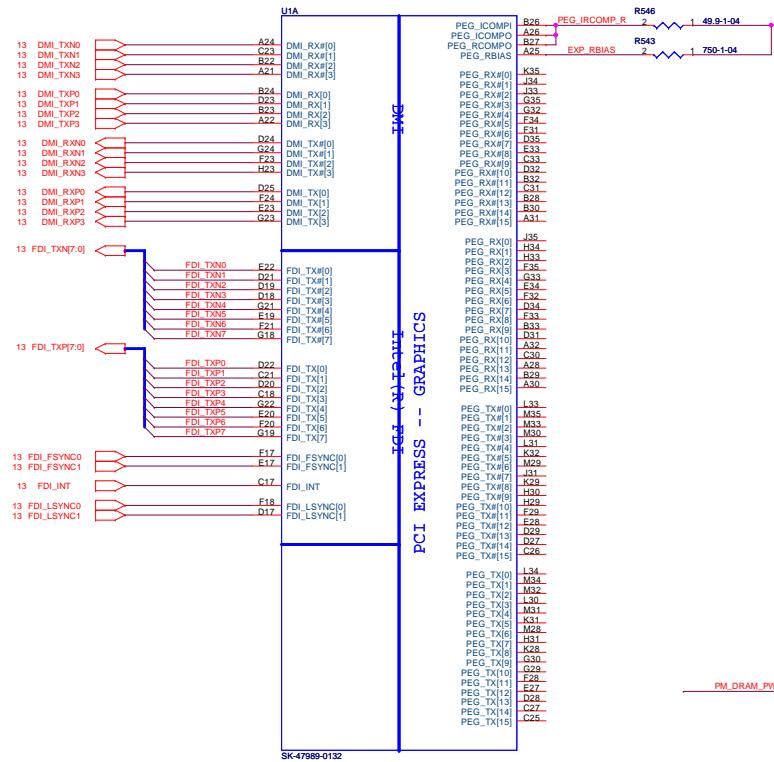
ITE8502NX System & LPC Bus	
LAD0	LPC_AD0
LAD1	LPC_AD1
LAD2	LPC_AD2
LAD3	LPC_AD3
SERIRQ	INT_SERIRQ
LFRAME#	LPC_FRAME#
LPCLK	CLK_PCI_KBC
WRST#	LRST1#

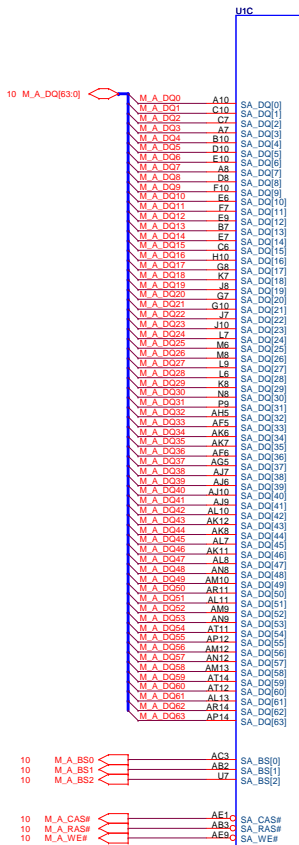
ITE8502NX Clock	
CLK32K	EC32KI
CK32KE	EC32KO

ITE8502NX Power	
VSTBY0	+3.3VA
VSTBY1	+3.3VA
VSTBY2	+3.3VA
VSTBY3	+3.3VA
VSTBY4	+3.3VA
VSTBY5	+3.3VA
VBAT	+3.3VA_RTC
AVCC	+3.3VA
VCC	+3.3VS

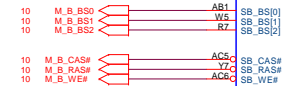
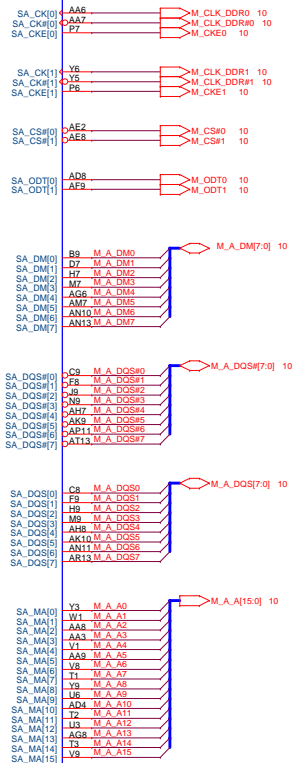
ITE8502NX GND	
AVSS	GND
VSS0	GND
VSS1	GND
VSS2	GND
VSS3	GND
VSS4	GND
VSS5	GND
VSS6	GND

ARRANDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)

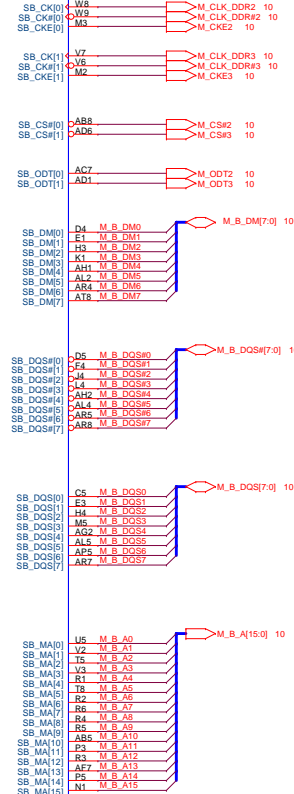




DDR SYSTEM MEMORY A



DDR SYSTEM MEMORY - B



ECS COMPUTER CORP.

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	SCHEMATIC1		
	Custom		
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ARRANDALE/CLARKSFIELD PROCESSOR (POWER)

Processor Core Power

Processor UNCore Power

CPU CORE
48000mA

+VCC_CORE

VTT

VTT0.1

VTT0.2

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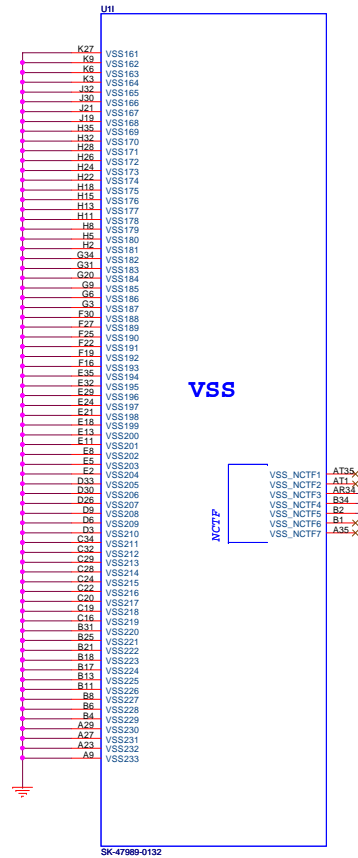
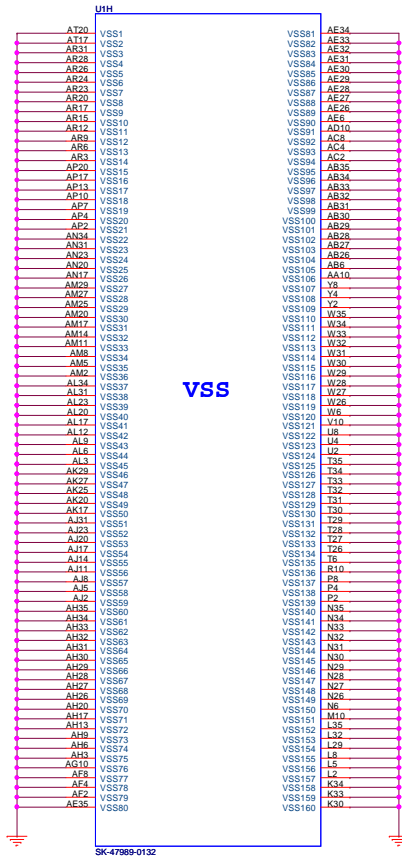
VTT0.285

VTT0.286

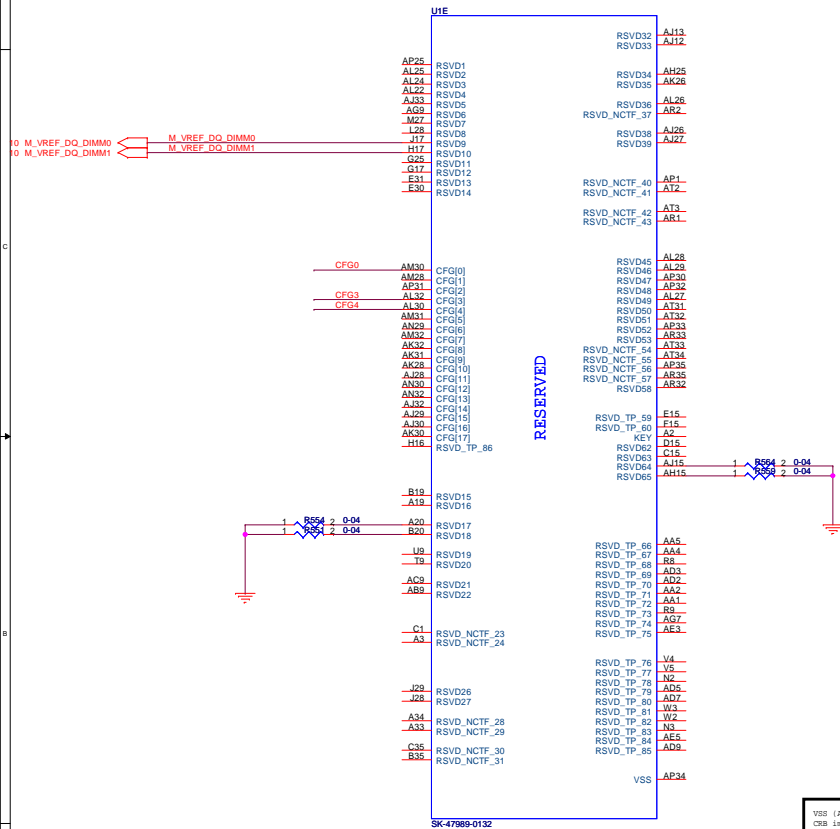
VTT0.287

VTT0.288

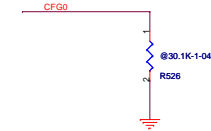
AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



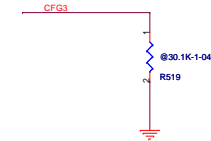
AUBURNDALE/CLARKSFIELD PROCESSOR (RESERVED)



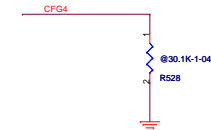
PCI-Express Configuration Select	
CFG0	1 : Single PEG 0 : Bifurcation enabled



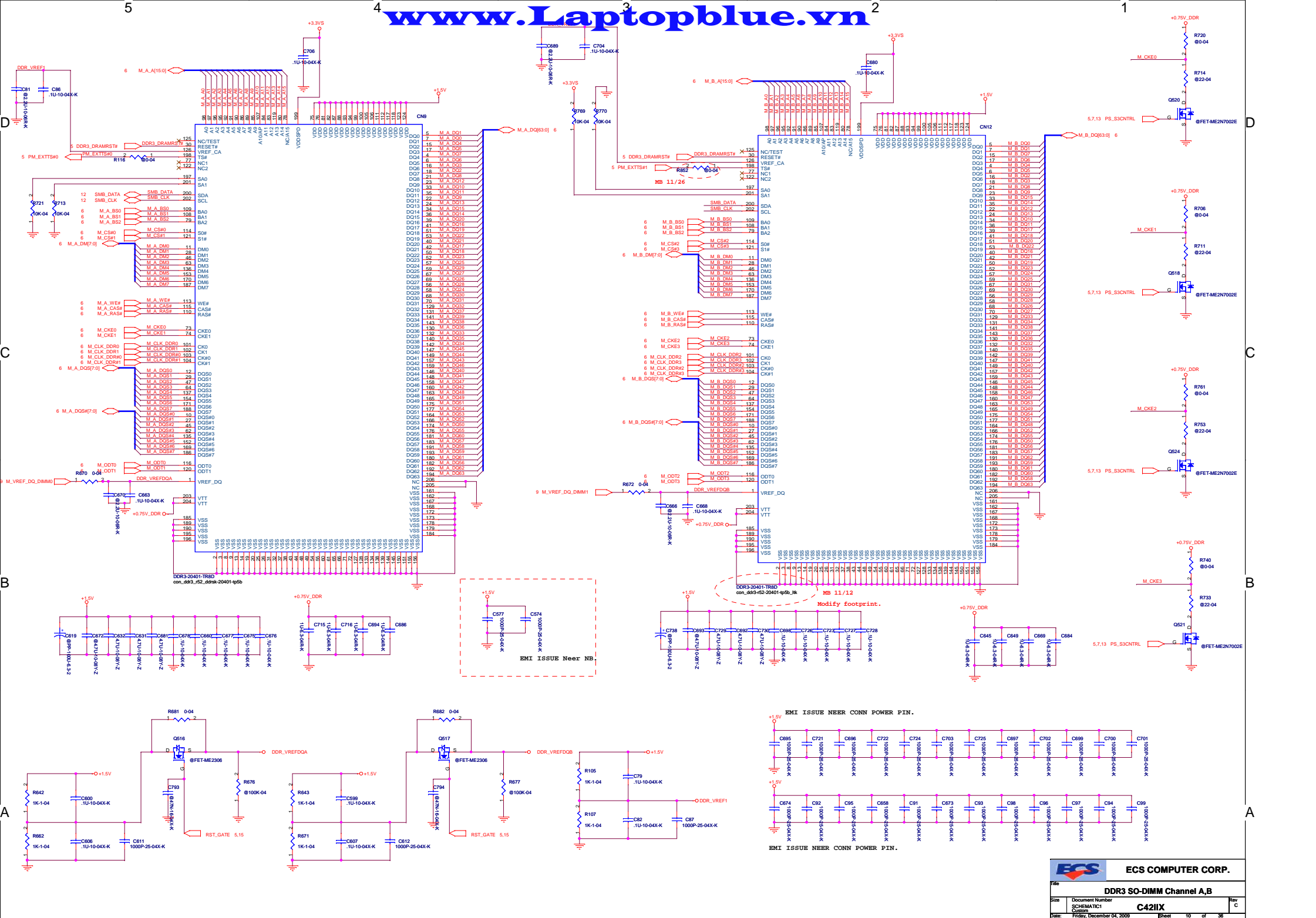
CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 : Normal Operation 0 : Lane Numbers Reversed



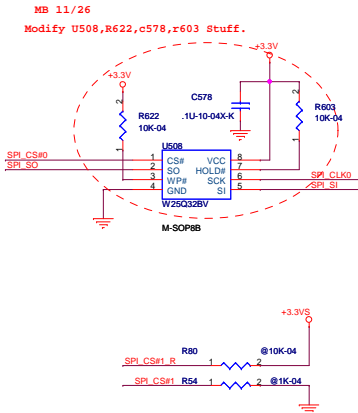
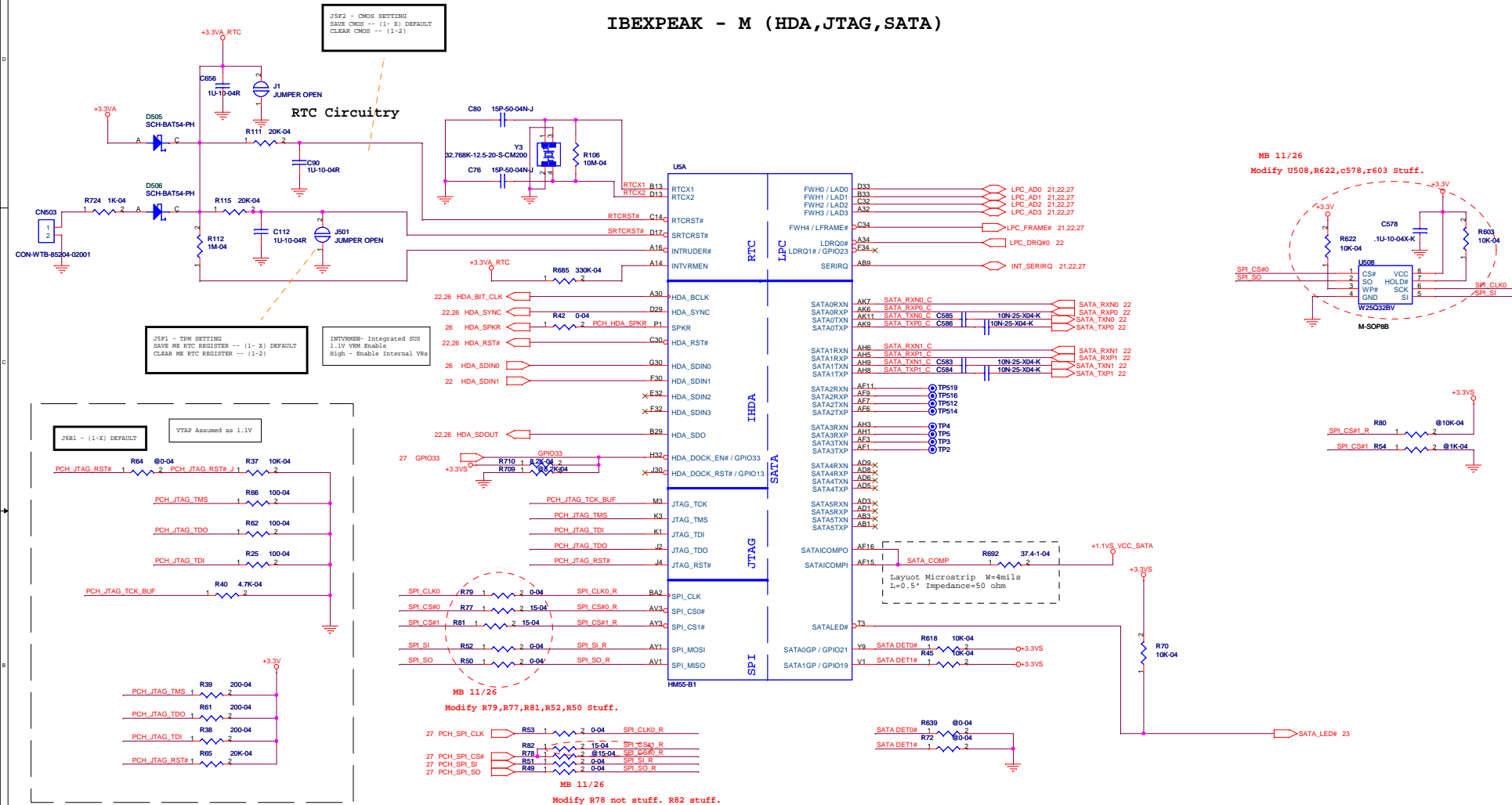
CFG4 - Display port presence	
CFG4	1 : Display , No physical display port attached to Embedded display port
	0 : Enabled , An external display port device is connected to the Embedded display port



VSS (AP34) can be left NC in CRB implementation; EDS/DG recommendation to GND

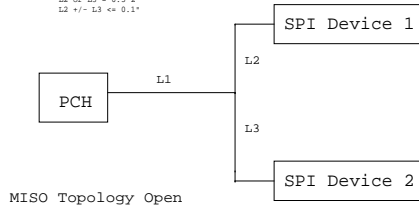


IBEXPEAK - M (HDA,JTAG,SATA)

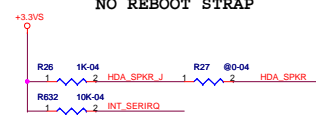


Layout Topology for SPI CLK and MOSI

L1 = 1-5"
L2 or L3 = 0.5-2"
L2 +/- L3 <= 0.1"

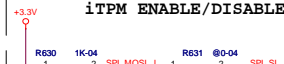


NO REBOOT STRAP

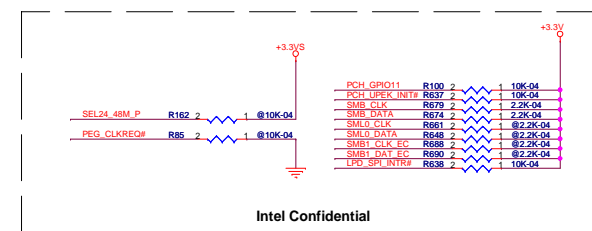
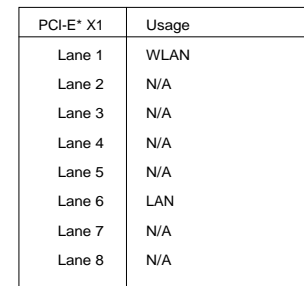


J9G4 - NO REBOOT
Disabled when LOW -- (1- X) DEFAULT
Enabled when HIGH -- (1-2)

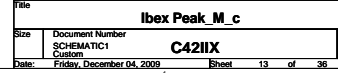
iTPM ENABLE/DISABLE

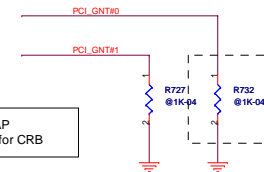
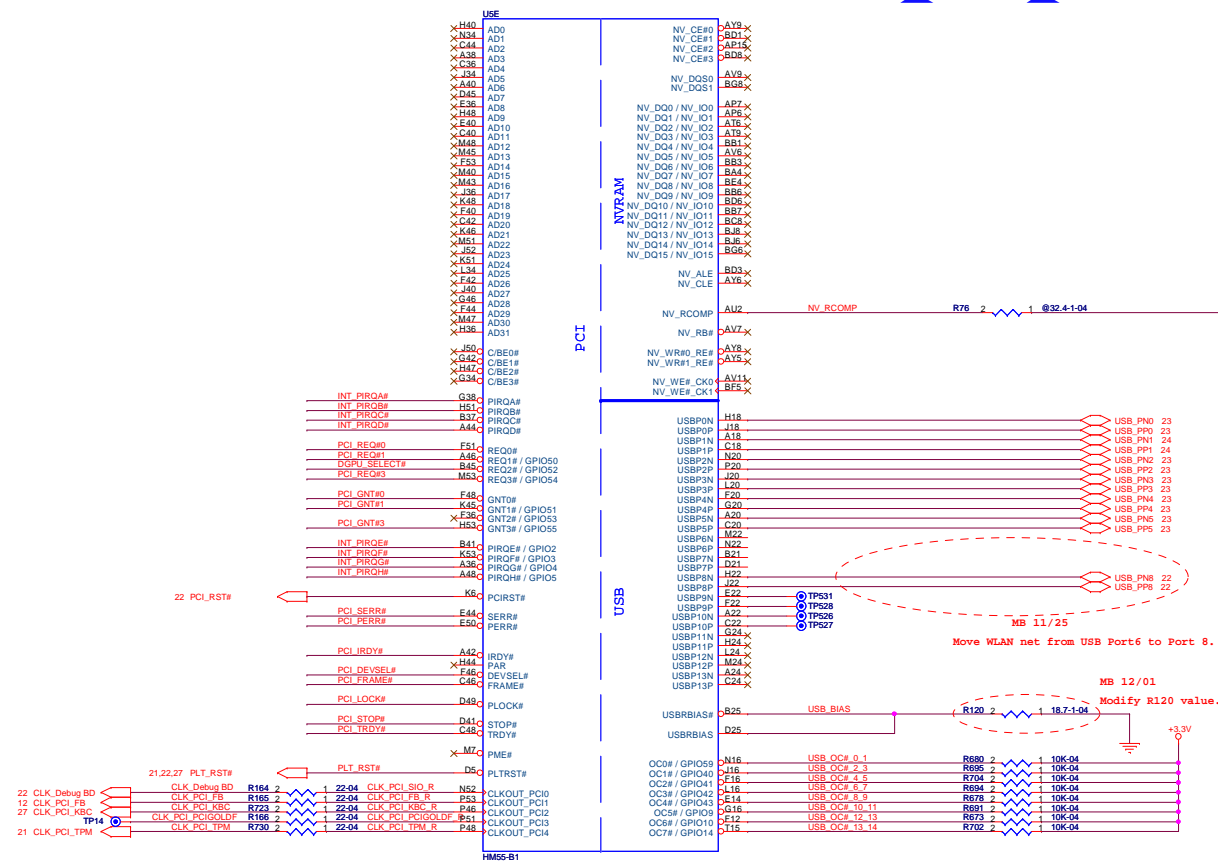


J9E1 - TPM FUNCTION
DISABLE -- (1- X) DEFAULT
ENABLE -- (1-2)



Port B not detected





R? --BBS STRAP
DEFAULT :1-X for CRB

BOOT BIOS STRAP		
PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

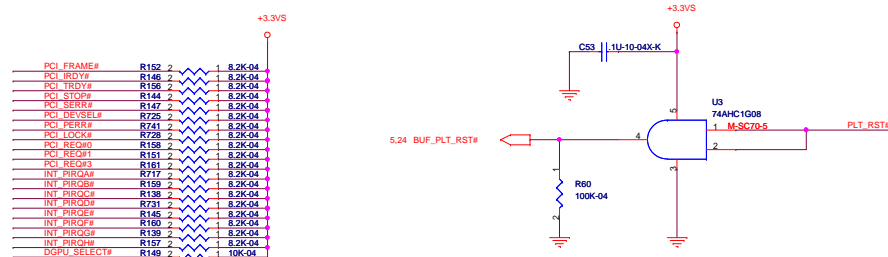
USB Ports Table

USBP0	Enhance USB
USBN0	USB_0
USBP1	USB BD
USBN1	USB_1
USBP2	USB BD
USBN2	USB_2
USBP3	Card Reader
USBN3	USB
USBP4	Web Camera
USBN4	USB
USBP5	Bluetooth
USBN5	USB
USBP6	
USBN6	
USBP7	
USBN7	
USBP8	WLAN
USBN8	USB
USBP9	
USBN9	
USBP10	
USBN10	
USBP11	
USBN11	

Move WLAN net from USB Port6 to Port 8.

Modify R120 value.

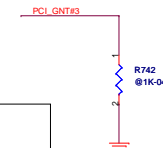
USB_OC#_0_1



Buffer to reduce loading on PLT_RST#

A16 swap override Strap/ Top-Block
Swap Override jumper

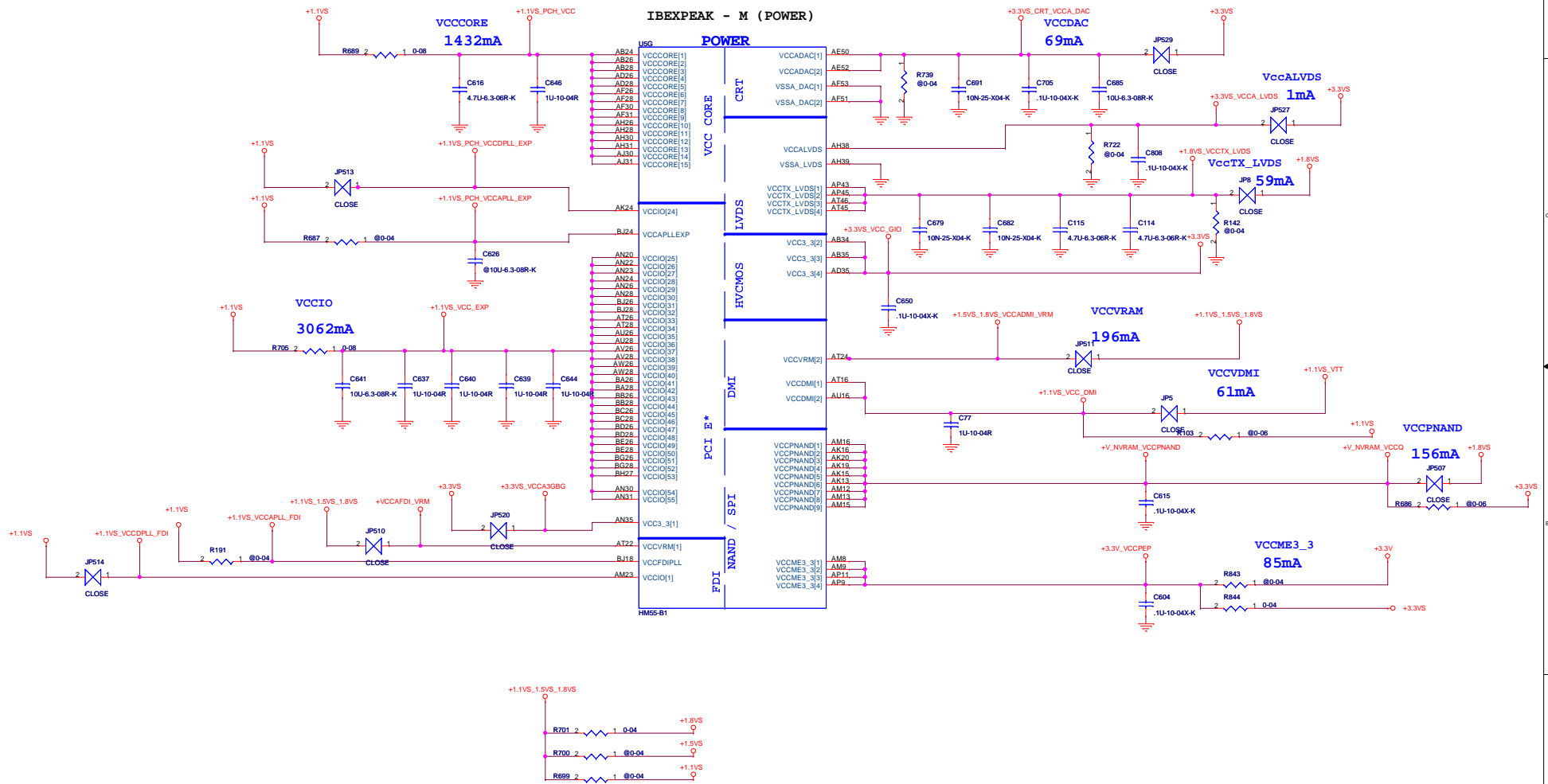
PCI_GNT#3	LOW = A16 swap override/Top -Block Swap Override enabled High = Default
-----------	----------------------------------------------------------------------------------



Danbury Technology
Disabled when LOW
Enabled when HIGH

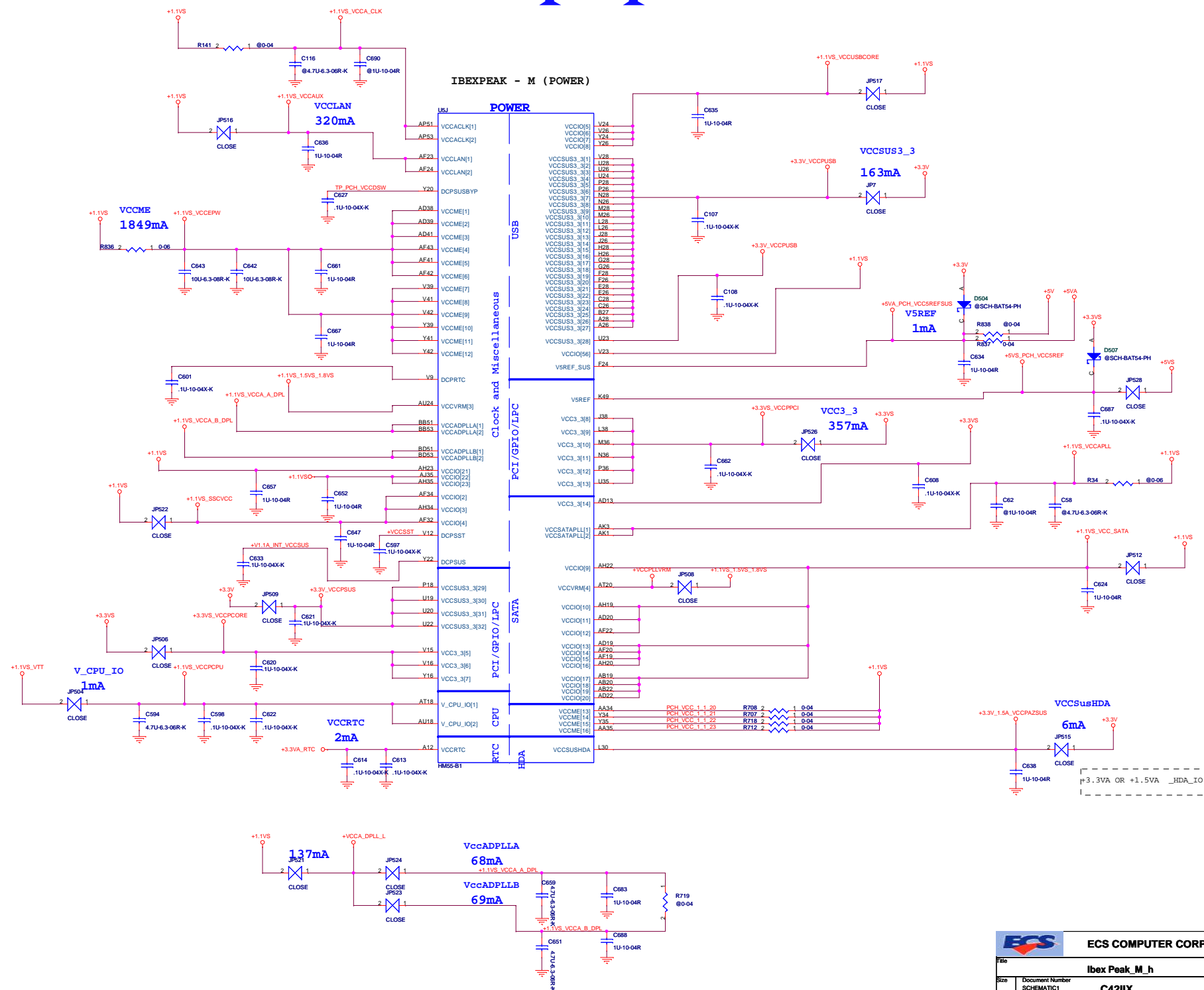
IBEXPEAK - M (POWER)

POWER

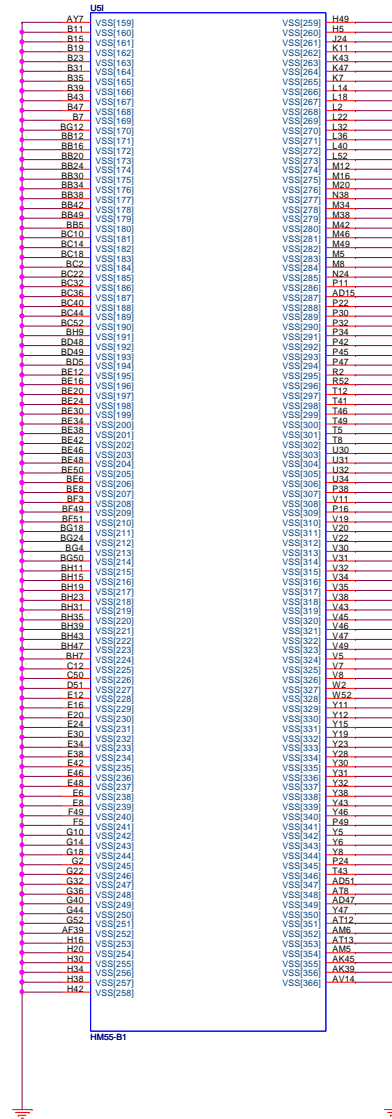
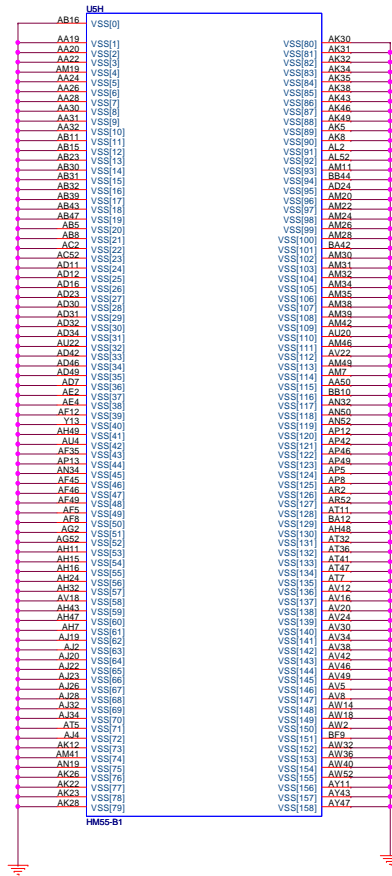


ECS COMPUTER CORP.

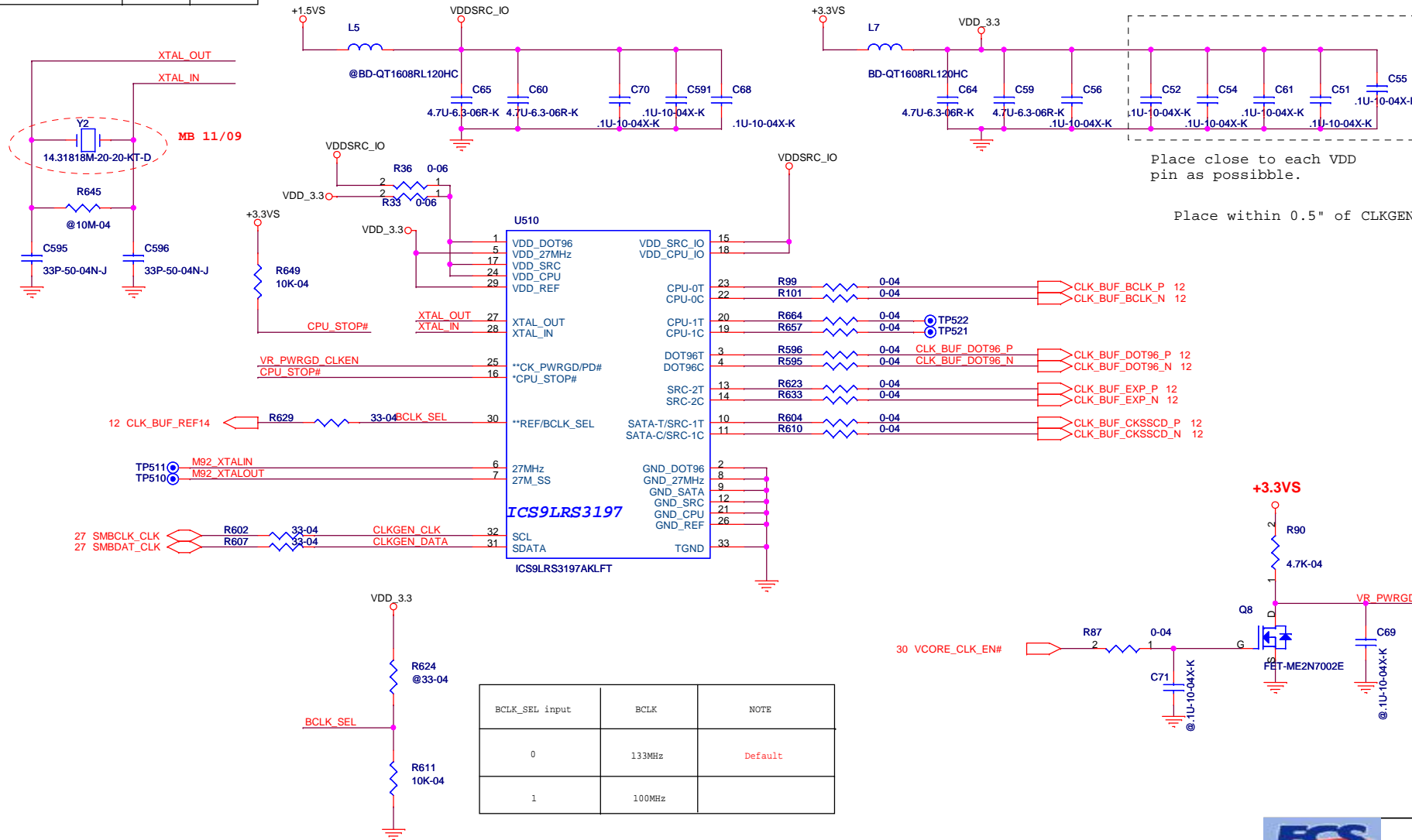
File	Ibex Peak_g		
Size	Document Number	Rev	
	SCHEMATIC1	C	
	Custom		
Date	Friday, December 04, 2009	Sheet	16 of 38



IBEX PEAK-M (GND)

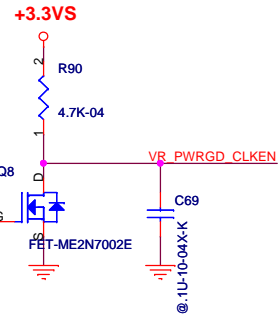


	L7	L5
ICS9LRS3197		
ICS9LVS3197		



Place close to each VDD pin as possible.

Place within 0.5" of CLKGEN



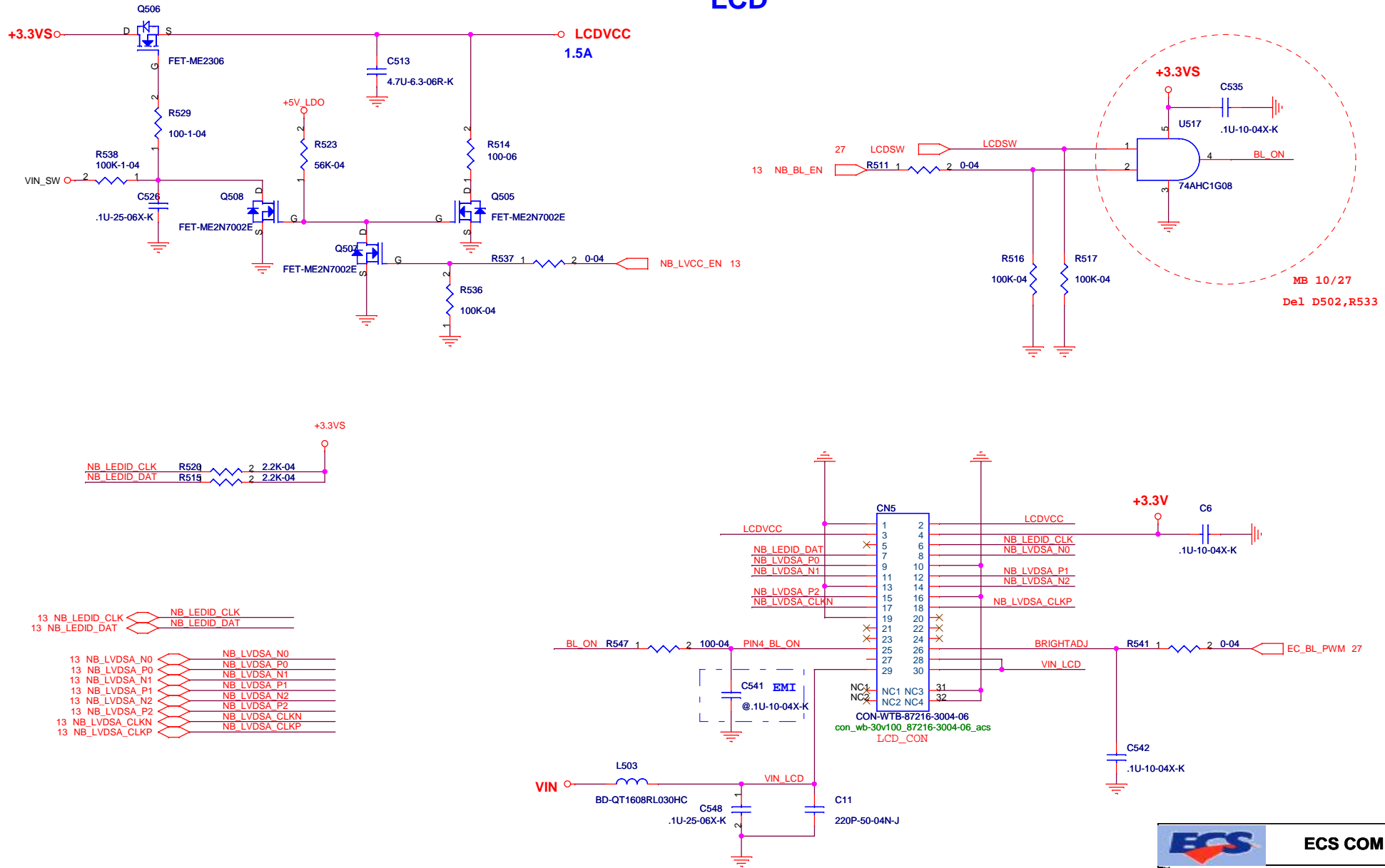
ECS COMPUTER CORP.

Title			CLOCK GEN (ICS9LRS3197)	
Size	Document Number	C42IIX		Rev
B	SCHEMATIC1			C
Date:	Friday, December 04, 2009	Sheet	19	of 36

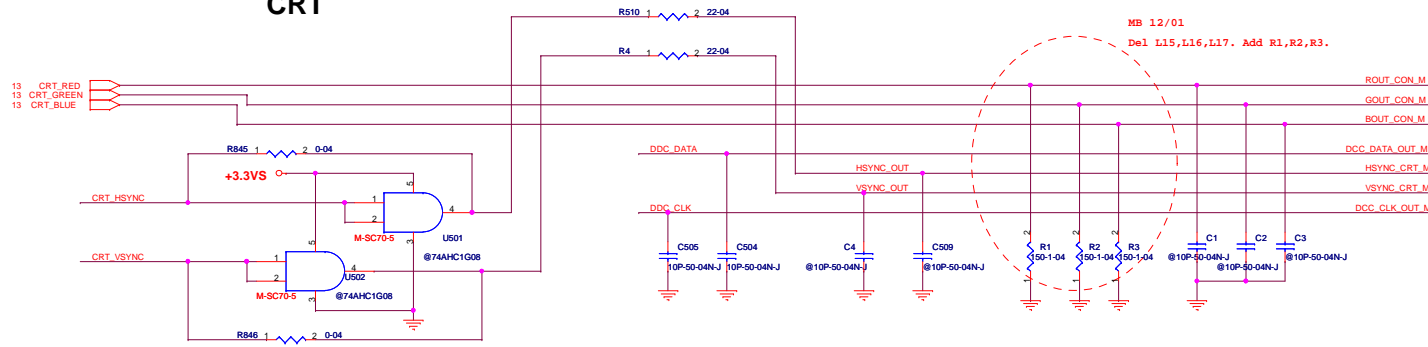
CLK_BUF_REF14 12

www.Laptopblue.vn

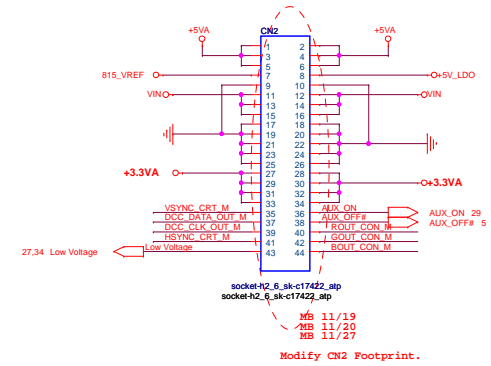
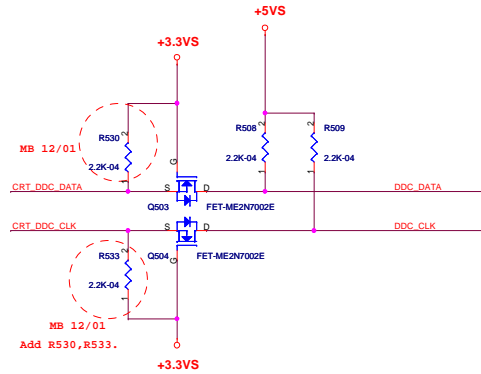
LCD



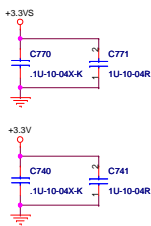
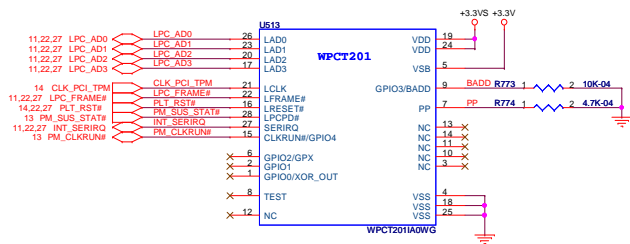
CRT



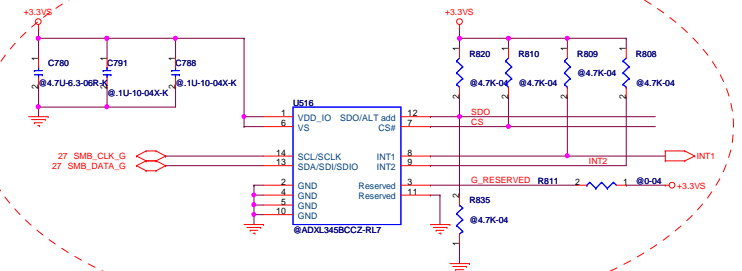
Connect to Power BD
CRT/+3.3VA/+5VA Conn

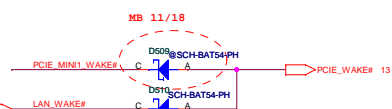
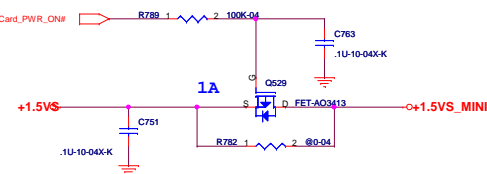


TPM



G-Sensor





SATA HDD

V_HDD1

11 SATA_TXP0
11 SATA_TXN0
11 SATA_RXN0
11 SATA_RXP0

C507 10N-25-X04-K
C506 10N-25-X04-K

NC4
S1
S2
S3
S4
S5
S6
S7
P1
P2
P3
P4
P5
P6
P7
P8
P9
P10
P11
P12
P13
P14
P15
NC2
NC1
GND1
GND2

1 R178 2 @9-04

con_hdd_s50r_c166bp-12205-l_atp
con_hdd_s50r_c166bp-12205-l_atp

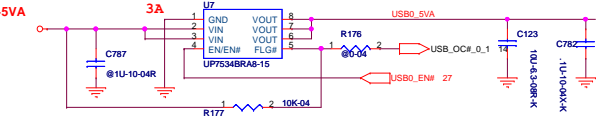
+5VS
1.5A
60MIL
L1
BD-QT1608RL0600C
C5 4.7uF±5%K
C7 4.7uF±5%K
C10 1U-10-04X-K
V_HDD1
1.5A
60MIL

[illegible]

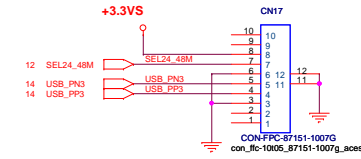
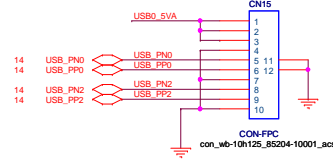
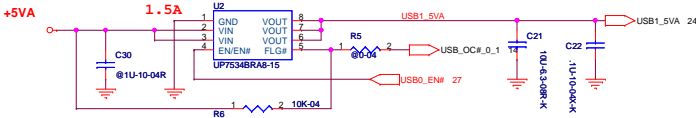
Connect to USB BD
USB CONN

Connect to Card Reader
Card Reader Conn

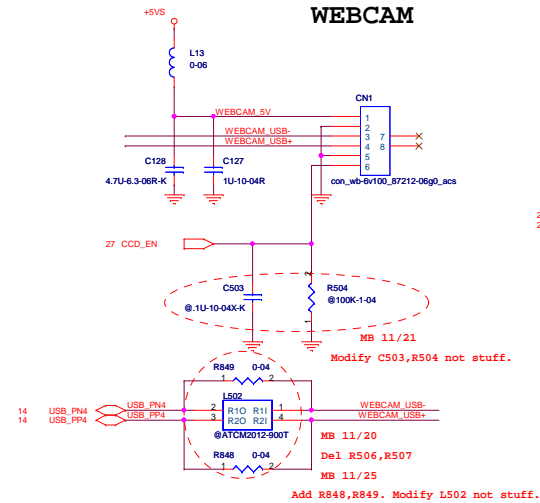
USB0/USB2



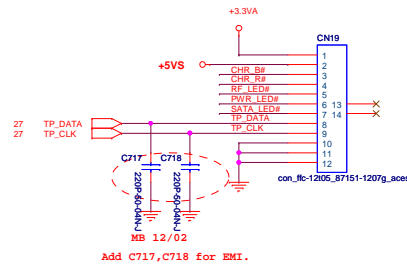
USB1



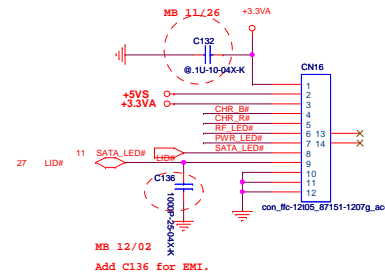
WEBCAM



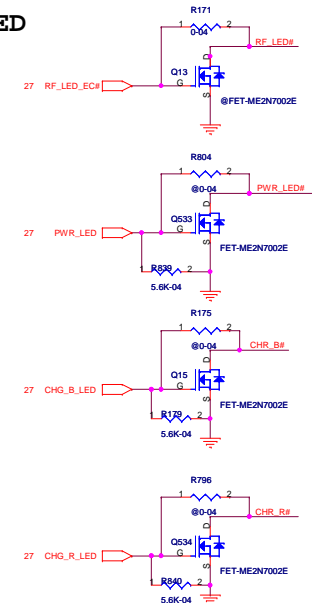
Connect to TP+LED BD
TP+LED Conn



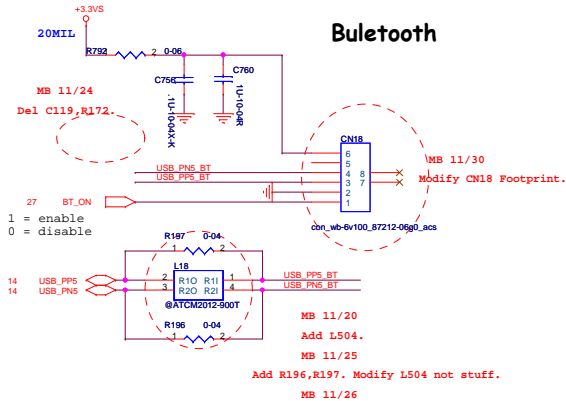
Connect to LED/LID BD
LED/LID CONN

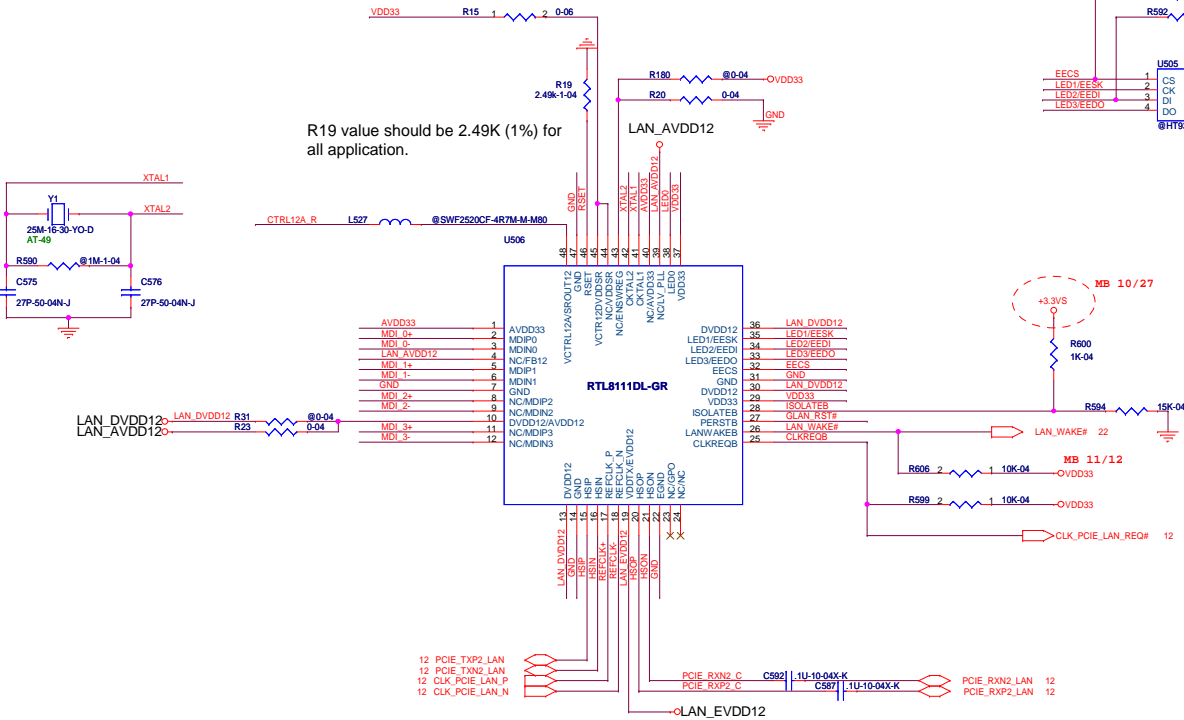
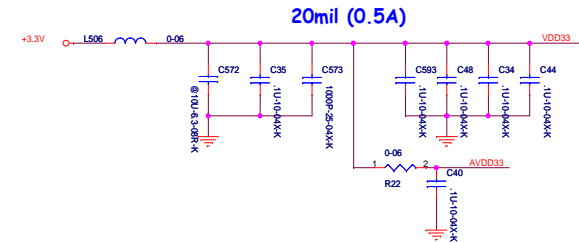
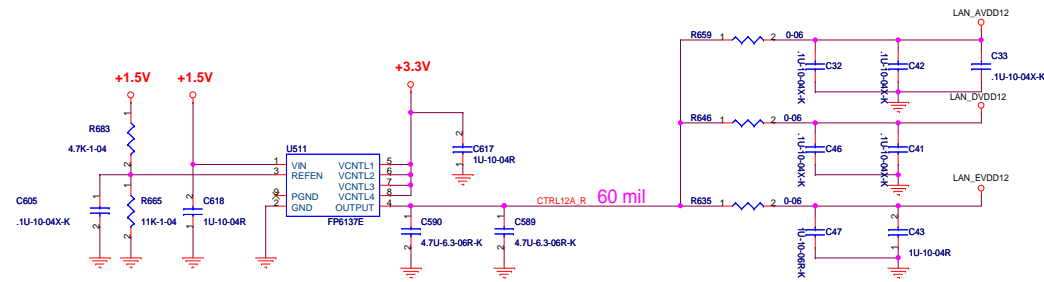


LED

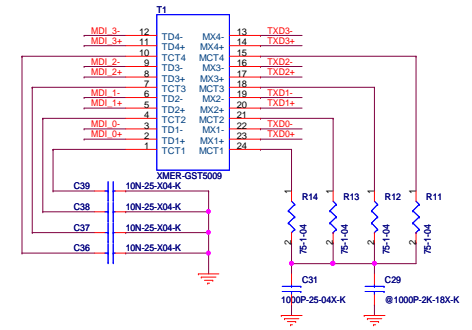
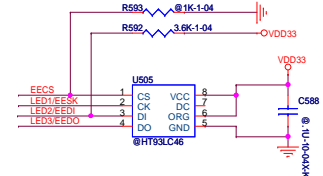


Buletooth

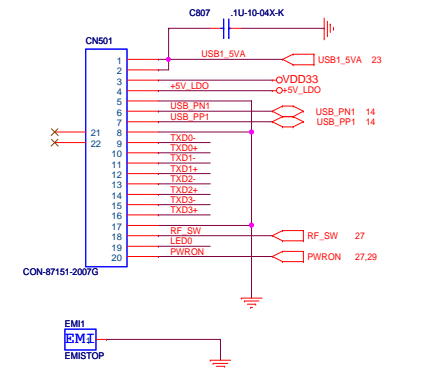




R509 is only required by RTL8102EL and RTL8103EL.



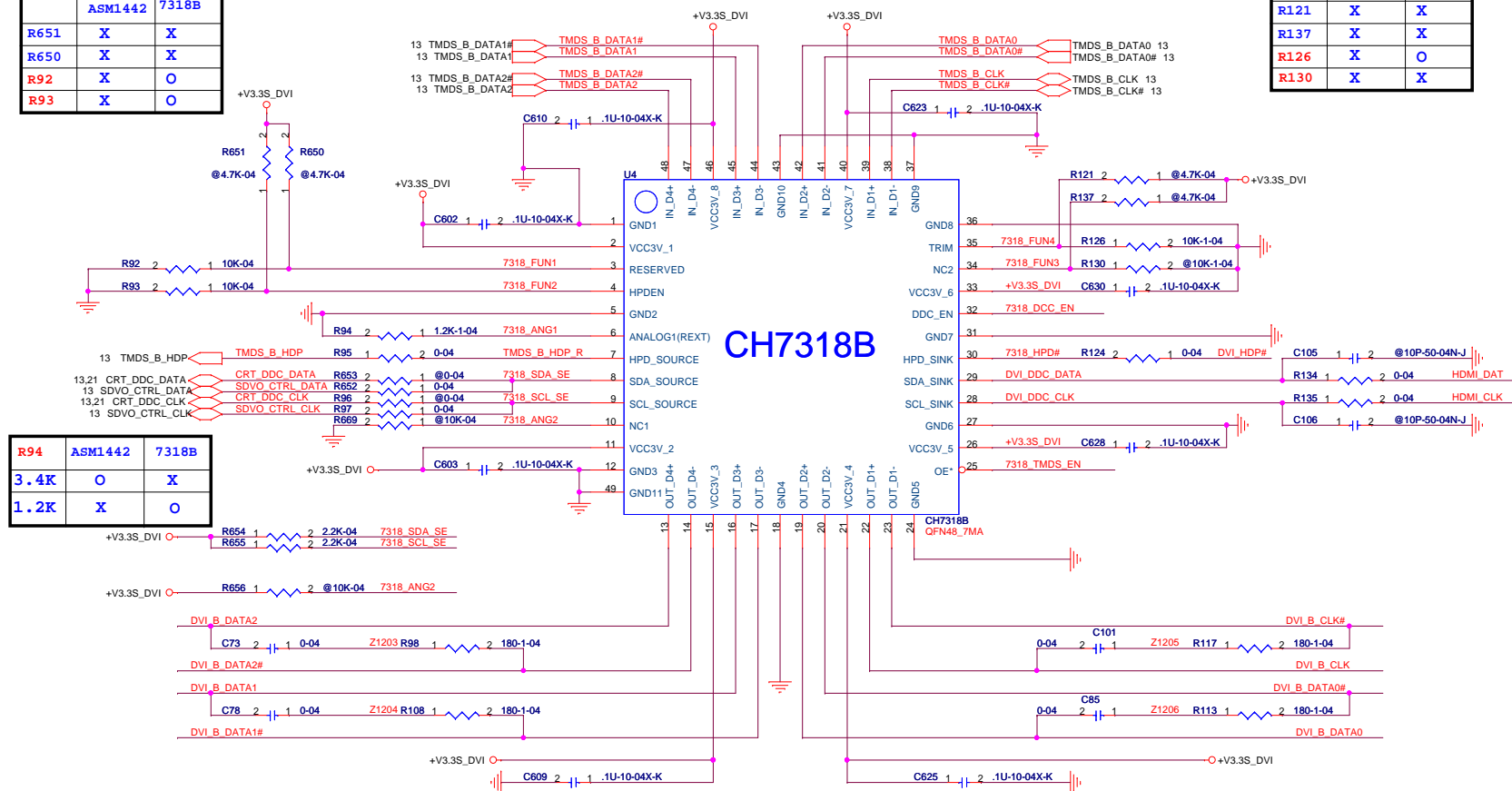
Connect to IO BD



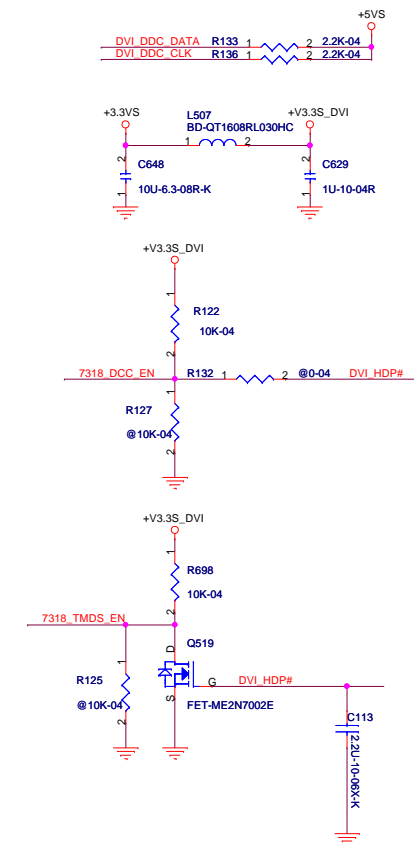
DVI SHIFTER

	ASM1442	7318B
R651	X	X
R650	X	X
R92	X	O
R93	X	O

	ASM1442	7318B
R121	X	X
R137	X	X
R126	X	O
R130	X	X

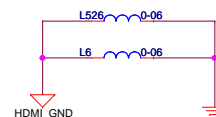
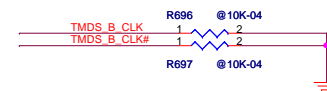
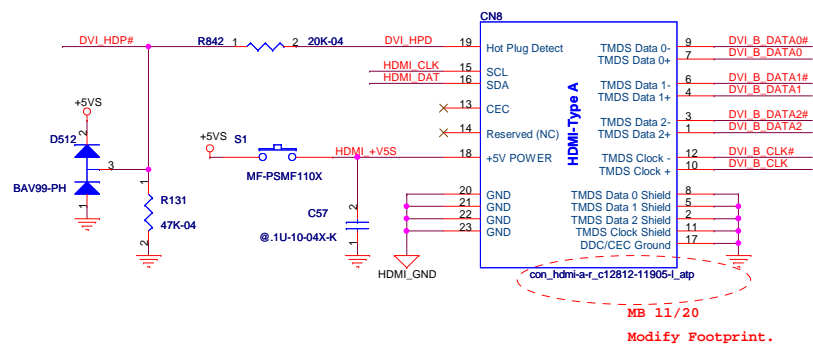


R94	ASM1442	7318B
3.4K	O	X
1.2K	X	O

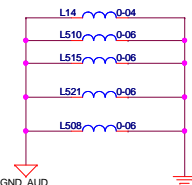
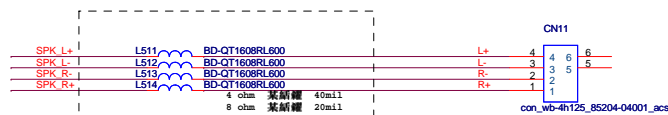
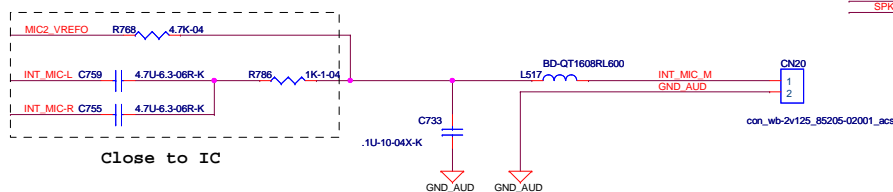
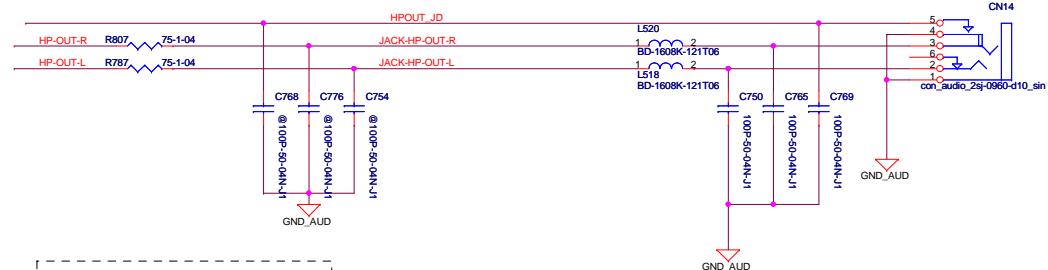
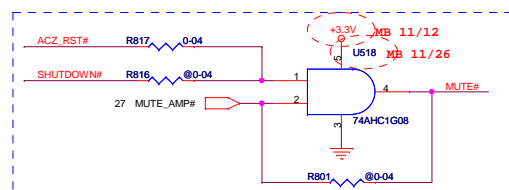
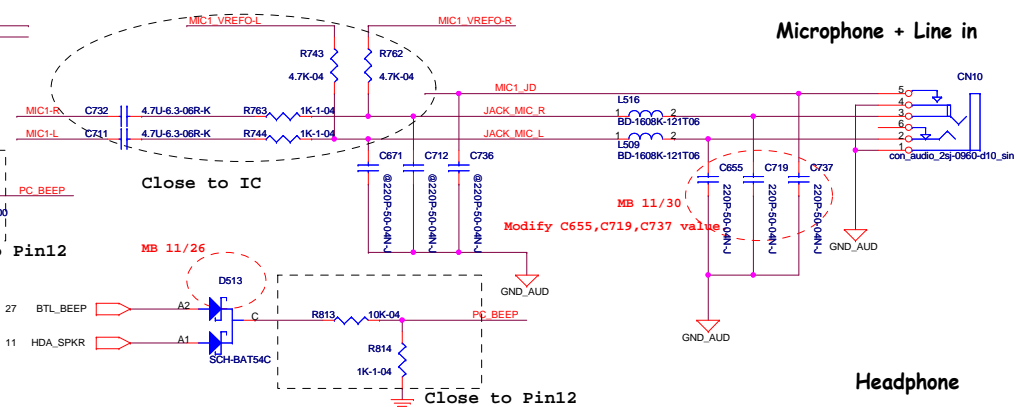
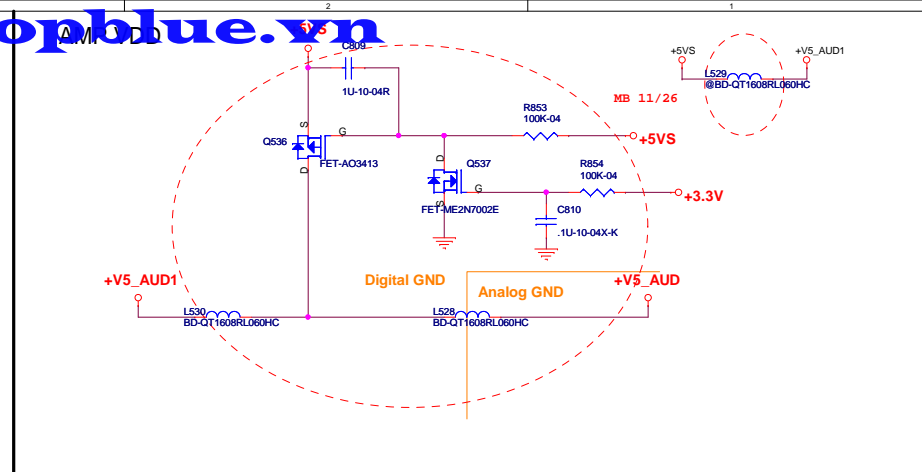
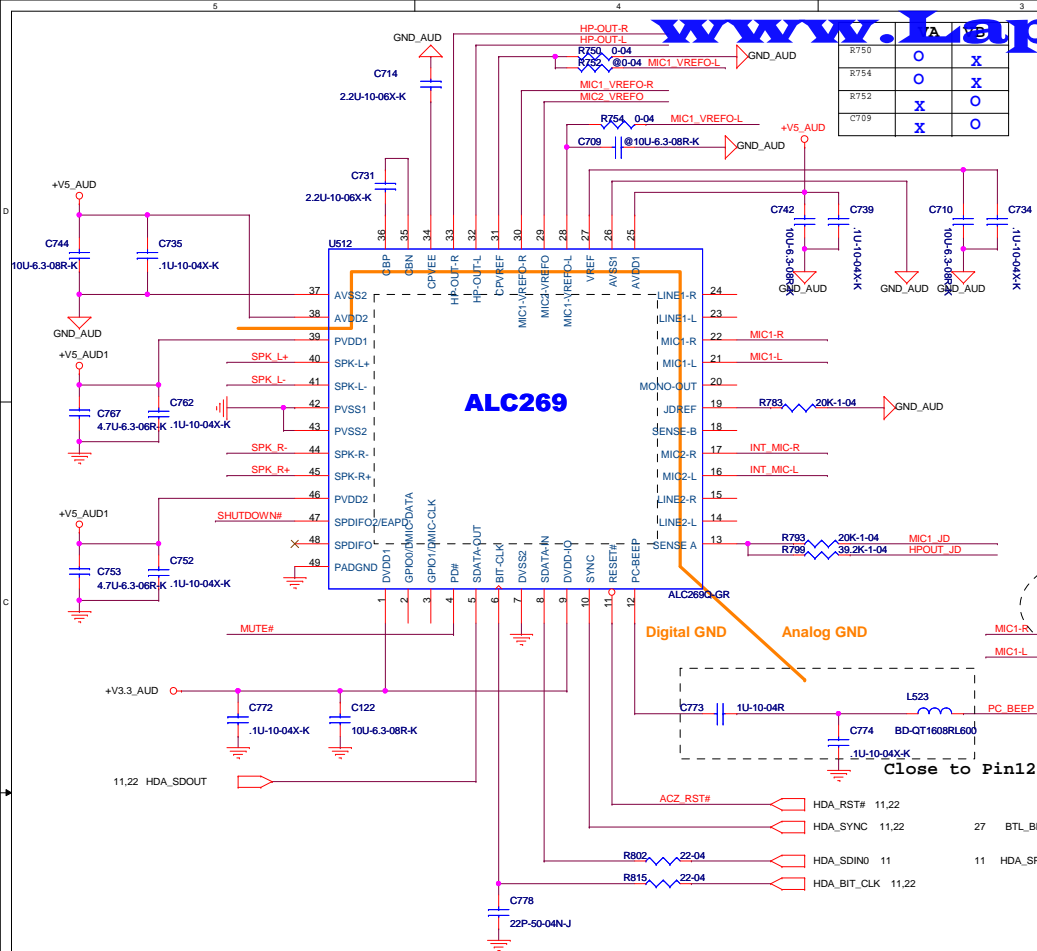


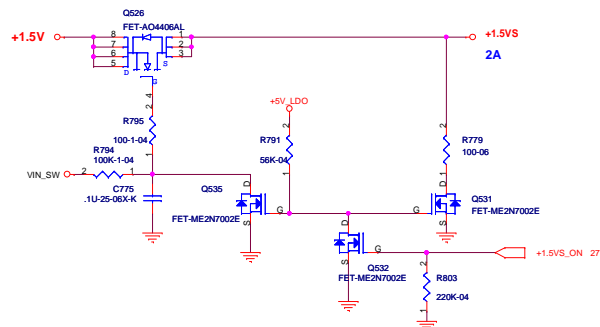
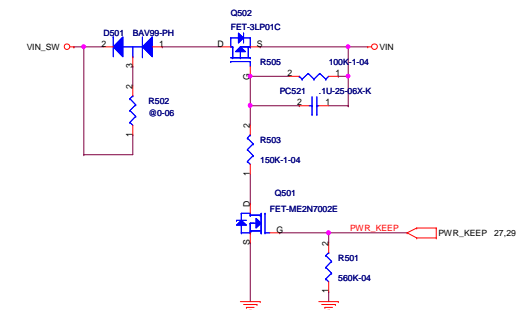
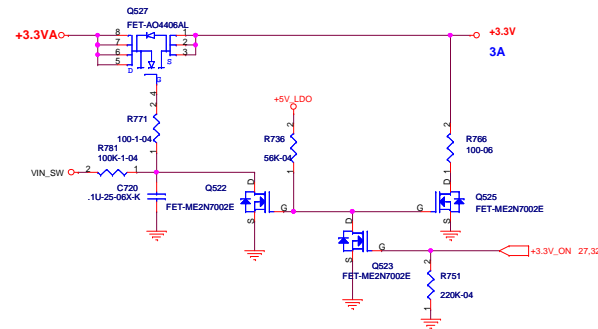
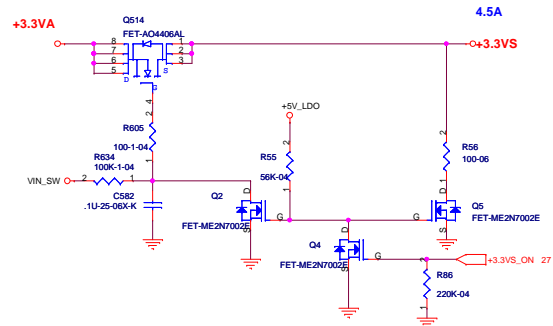
	ASML442	7318B
R117	X	O
C101	X	O
R113	X	O
C85	X	O
R108	X	O
C78	X	O
R98	X	O
C73	X	O

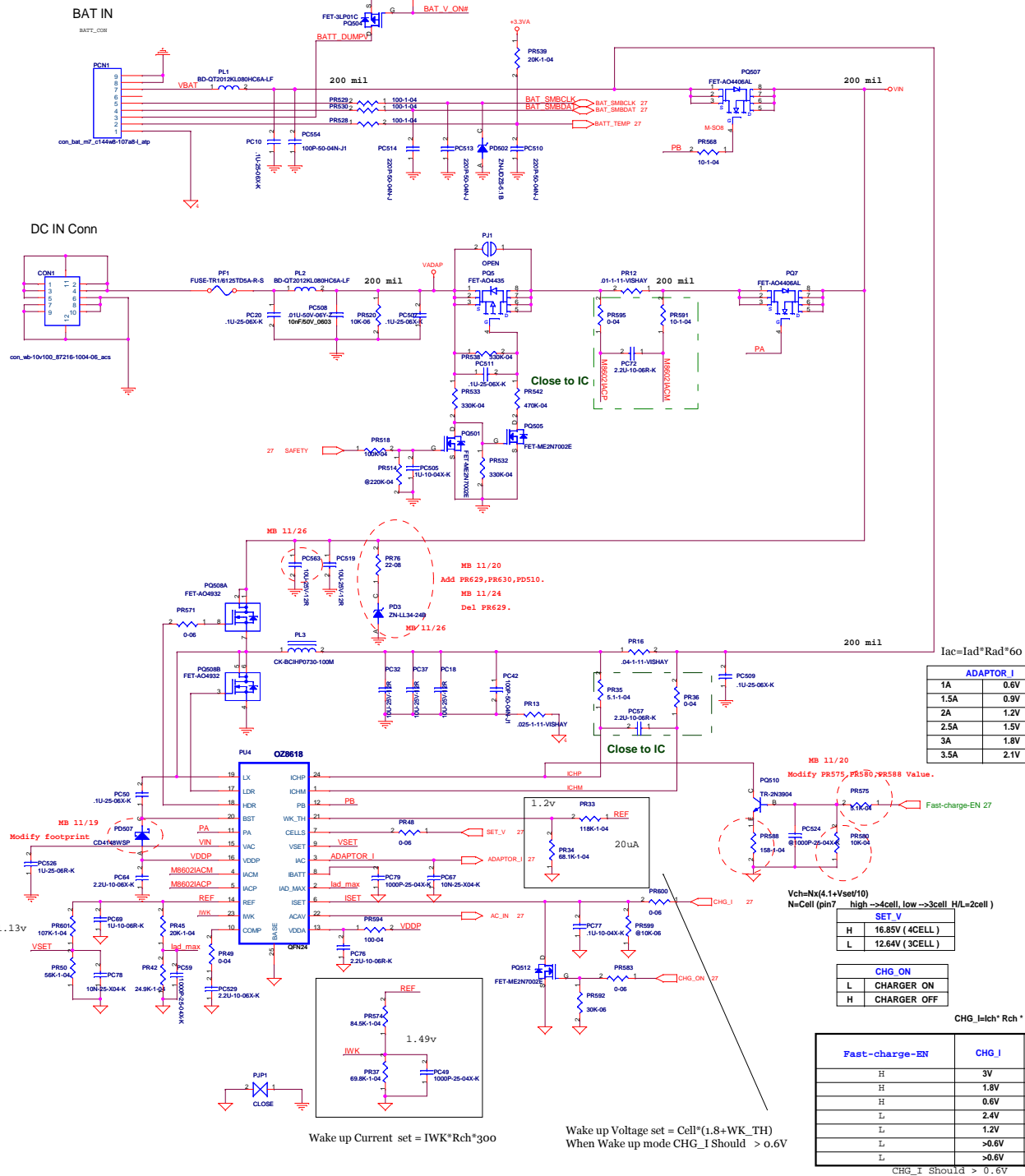
HDMI Conn.

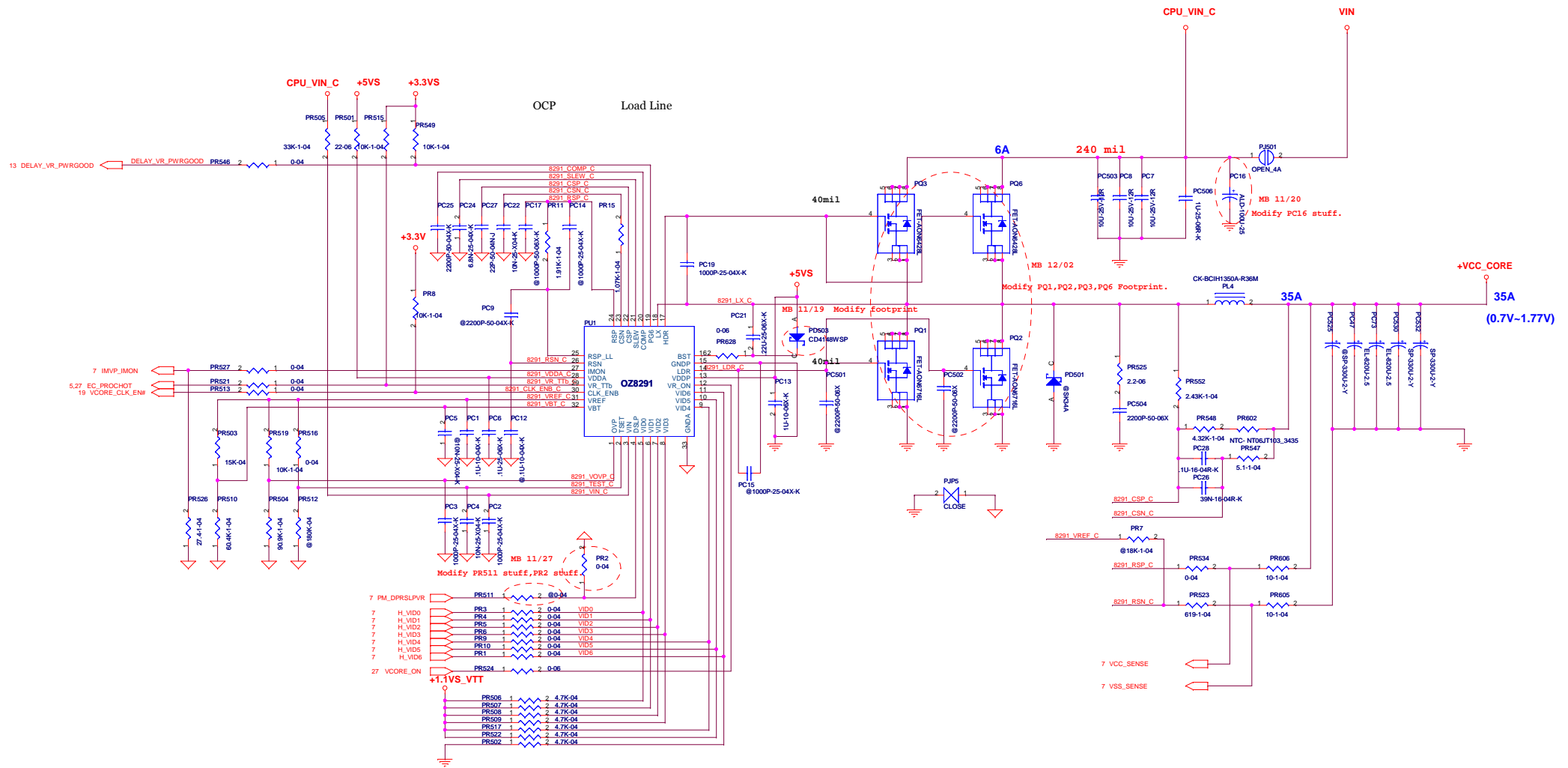


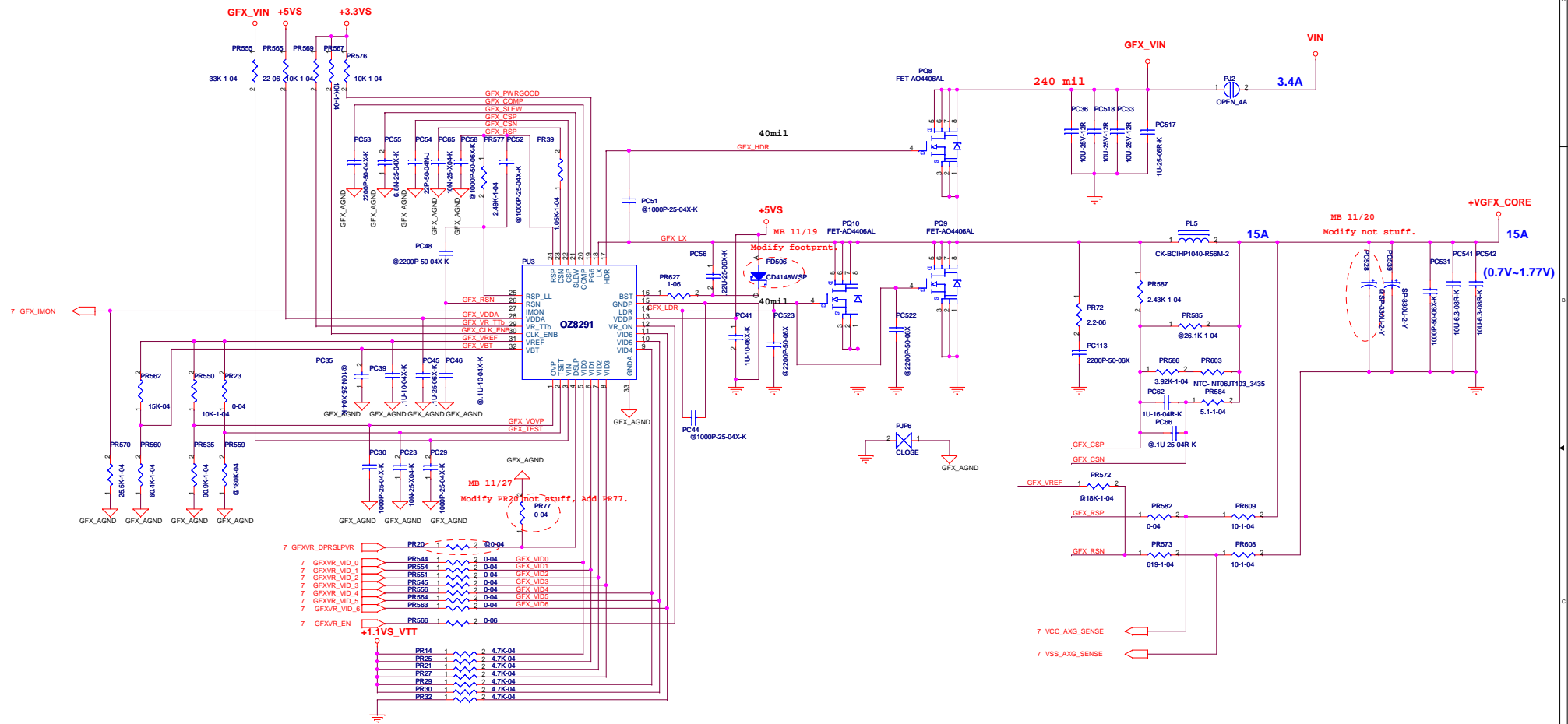
	VA	VB
R750	0	X
R754	0	X
R752	X	0
C709	X	0

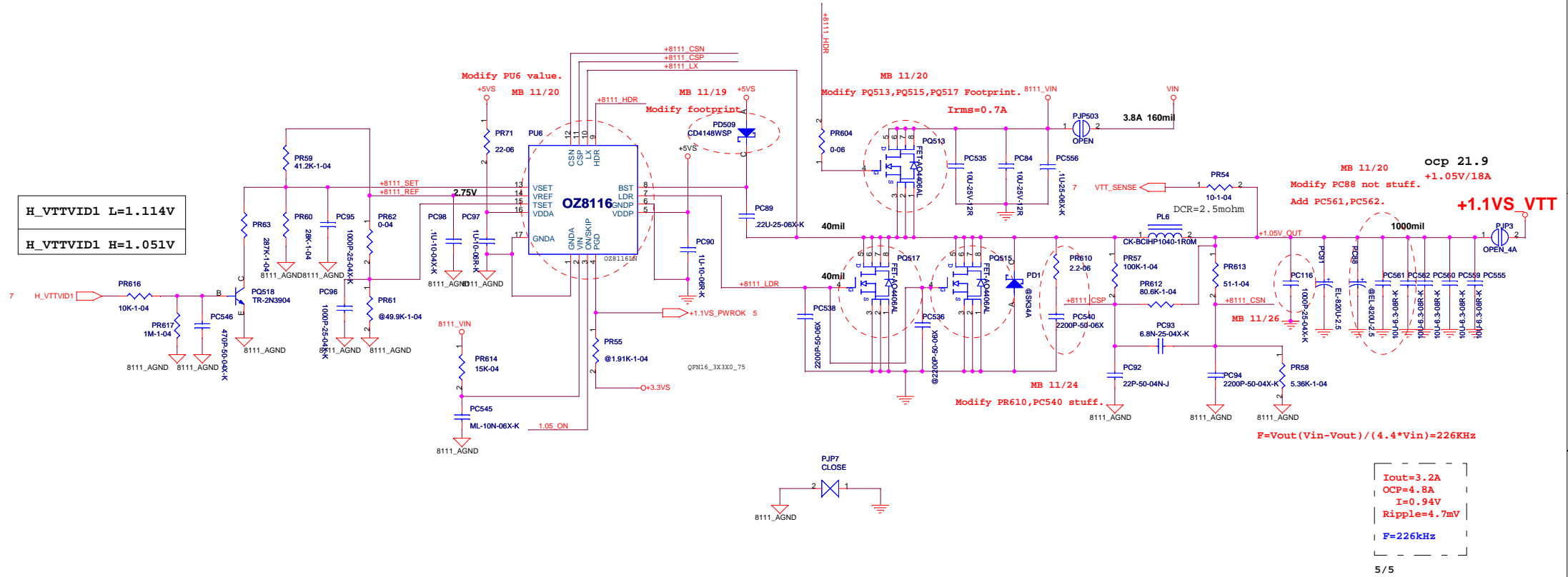






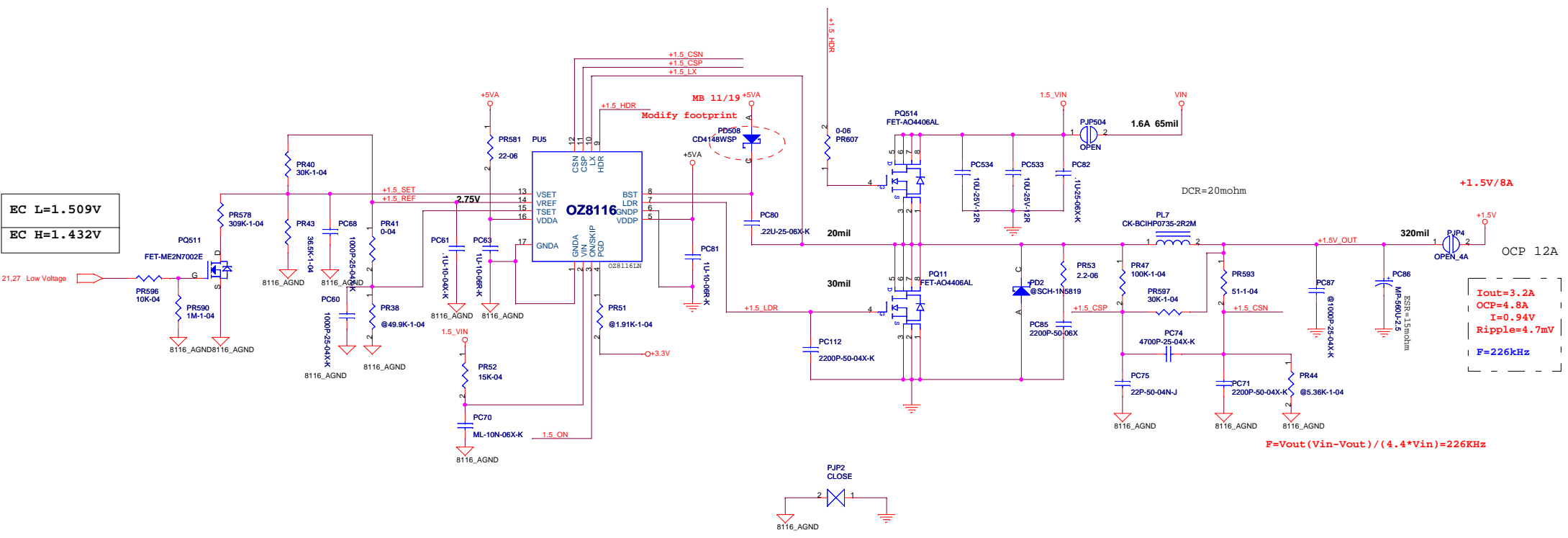






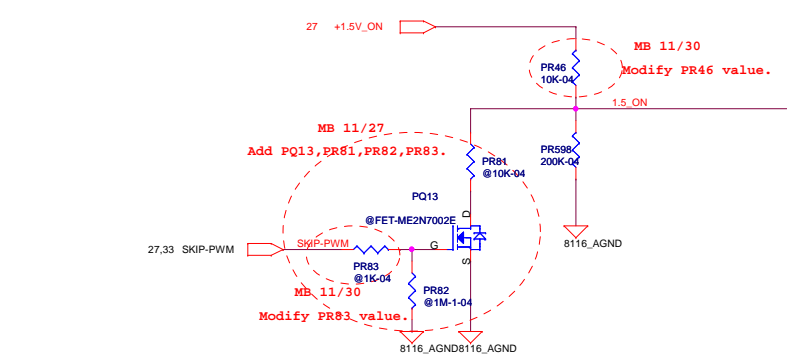
5/5

EC L=1.509V
EC H=1.432V



Iout=3.2A
OCP=4.8A
I=0.94V
Ripple=4.7mV
F=226kHz

$$F = \text{Vout}(\text{Vin} - \text{Vout}) / (4.4 * \text{Vin}) = 226\text{KHz}$$



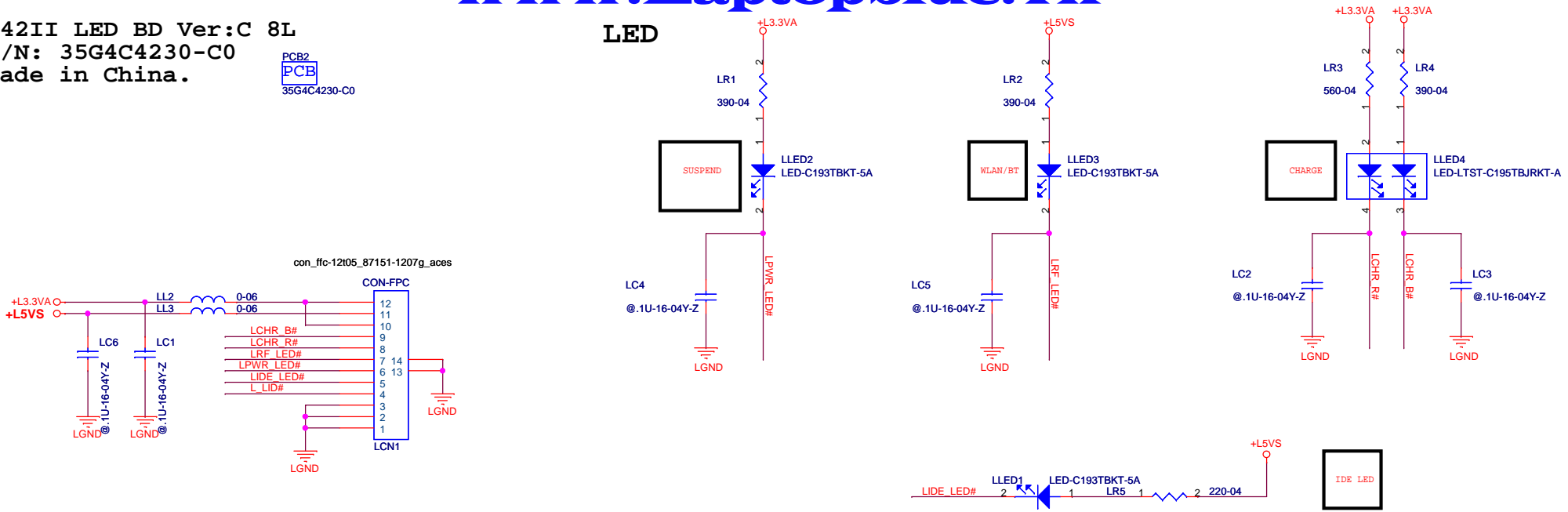
1. Page24 Modify R600 connect to "+3.3VS" net.	Milo	10/27	Vincent 12/04	Jack 12/04
2. Page20 Del D502,R533: Add U517.	Milo	10/27	Vincent 12/04	Jack 12/04
3. Page21 Modify C780,C791,C788,R820,R810,R809,R808,R835,U516,R835 not stuff.	Milo	10/27	Vincent 12/04	Jack 12/04
4. Page29 Modify PD504 Footprint.	Milo	11/03	Vincent 12/04	Jack 12/04
5. Page19 Modify Y2 Footprint.	Milo	11/09	Vincent 12/04	Jack 12/04
6. Page10 Modify CN12 Footprint.	Milo	11/12	Vincent 12/04	Jack 12/04
7. Page28 Modify H1 Footprint.	Milo	11/12	Vincent 12/04	Jack 12/04
8. Page22 Modify CN505 Footprint. Add R194,R195(@100K-04).	Milo	11/12	Vincent 12/04	Jack 12/04
9. Page26 Modify U6.5 connect to "+3.3V" net.	Milo	11/12	Vincent 12/04	Jack 12/04
10. Page22 Modify D509 not stuff.	Milo	11/18	Vincent 12/04	Jack 12/04
11. Page21 Modify CN2 Footprint.	Milo	11/19	Vincent 12/04	Jack 12/04
12. Page29,30,31,33,34 Modify PD503,PD505-PD509 Footprint.	Milo	11/19	Vincent 12/04	Jack 12/04
13. Page23 Del R506,R507. Add L504. Modify L502 Footprint.	Milo	11/20	Vincent 12/04	Jack 12/04
14. Page22 Add L505.	Milo	11/20	Vincent 12/04	Jack 12/04
15. Page21,25,28 Modify CN2,CN8,H10 footprint.	Milo	11/20	Vincent 12/04	Jack 12/04
16. Page29 Modify PR575,PR588 value. Modify PR580 stuff.	Milo	11/20	Vincent 12/04	Jack 12/04
17. Page29 Add PR629,PR630,PD510.	Milo	11/20	Vincent 12/04	Jack 12/04
18. Page30 Modify PC16 stuff.	Milo	11/20	Vincent 12/04	Jack 12/04
19. Page31 Modify PC528 not stuff.	Milo	11/20	Vincent 12/04	Jack 12/04
20. Page33 Modify PU6 value. Modify PQ513,PQ515,PQ517 footprint.	Milo	11/20	Vincent 12/04	Jack 12/04
21. Page33 Modify PC88 not stuff. Add PC561,PC562.	Milo	11/20	Vincent 12/04	Jack 12/04
22. Page23 Modify C503,R504 not stuff.	Milo	11/21	Vincent 12/04	Jack 12/04
23. Page29 Del PR629.	Milo	11/24	Vincent 12/04	Jack 12/04
24. Page33 Modify PR610,PC540 stuff.	Milo	11/24	Vincent 12/04	Jack 12/04
25. Page27 Del C45.	Milo	11/24	Vincent 12/04	Jack 12/04
26. Page11 Modify U508 stuff.	Milo	11/24	Vincent 12/04	Jack 12/04
27. Page23 Del CL19,R172.	Milo	11/24	Vincent 12/04	Jack 12/04
28. Page23 Add R196,R197,R848,R849. Modify L502,L504 not stuff.	Milo	11/25	Vincent 12/04	Jack 12/04
29. Page22 Add R850,R851. Modify L505 not stuff.	Milo	11/25	Vincent 12/04	Jack 12/04
30. Page14 Move WLAN net from USB Port6 to Port 8.	Milo	11/25	Vincent 12/04	Jack 12/04
31. Page11 Modify R622,C578,R603,R79,R77,R81,R52,R50,R82 stuff. Modify R78 not stuff.	Milo	11/26	Vincent 12/04	Jack 12/04
32. Rename, CN505-->CN13, PC547--> PC114, PC548--> PC115, PD510-->PD3, PR618--> PR73. PR619-->PR74, PR620-->PR75, PR630-->PR76, L504-->L18, PC544-->PC116, LC1-->CL132.	Milo	11/26	Vincent 12/04	Jack 12/04
33. Rename, CL120-->C809, CL121-->C810, CL124-->C811, CL125-->C812, D2-->D513, L10-->L528. L11-->L529, L12-->L530, PC111-->PC563, Q14-->Q536, Q16-->Q537, R150-->R852, R173-->R853. R174--> R854, R187-->R855, R188-->R856, R194-->R857, R195-->R858, U6--> U518.	Milo	11/26	Vincent 12/04	Jack 12/04
34. Page30 Modify PR2 stuff, PR511 not stuff.	Milo	11/27	Vincent 12/04	Jack 12/04
35. Page31 Modify PR20 not stuff, Add PR77(0-04).	Milo	11/27	Vincent 12/04	Jack 12/04
36. Page32 Modify PU7 value(OZ8033).	Milo	11/27	Vincent 12/04	Jack 12/04
37. Page33 Modify PR611 value(10K-04), Add PQ12,PR78,PR79,PR80.	Milo	11/27	Vincent 12/04	Jack 12/04
38. Page34 Add PQ13,PR81,PR82,PR83.	Milo	11/27	Vincent 12/04	Jack 12/04
39. Page29 U514.95 connect to "SKIP-PWM" net.	Milo	11/27	Vincent 12/04	Jack 12/04
40. Page21 Modify CN2 footprint.	Milo	11/27	Vincent 12/04	Jack 12/04
41. Page33,34 Modify PR80,PR83,PR46 value.	Milo	11/30	Vincent 12/04	Jack 12/04
42. Page12 Modify R163 Footprint, Add CL19.	Milo	11/30	Vincent 12/04	Jack 12/04
43. Page23 Modify CN18 Footprint.	Milo	11/30	Vincent 12/04	Jack 12/04
44. Page26 Modify C737,C719,C655 value.	Milo	11/30	Vincent 12/04	Jack 12/04
45. Page33 Modify PR78,PR79,PR80,PQ12 not stuff. Modify PR611 value.	Milo	12/01	Vincent 12/04	Jack 12/04
46. Page14 Modify R120 value.	Milo	12/01	Vincent 12/04	Jack 12/04
47. Page21 Del L15,L16,L17. Add R1,R2,R3.	Milo	12/01	Vincent 12/04	Jack 12/04
48. Page21 Add R530,R533.	Milo	12/01	Vincent 12/04	Jack 12/04
49. Page13 Add CL133,CL134,CL135.	Milo	12/02	Vincent 12/04	Jack 12/04
50. Page28 Add C803.	Milo	12/02	Vincent 12/04	Jack 12/04
51. Page23 Add C717,C718,CL136.	Milo	12/02	Vincent 12/04	Jack 12/04
52. Page12 Modify CL19 stuff.	Milo	12/02	Vincent 12/04	Jack 12/04
53. Page22 Modify R780 Footprint.	Milo	12/02	Vincent 12/04	Jack 12/04
54. Page30 Modify PQ1,PQ2,PQ3,PQ6 Footprint.	Milo	12/02	Vincent 12/04	Jack 12

[illegible]

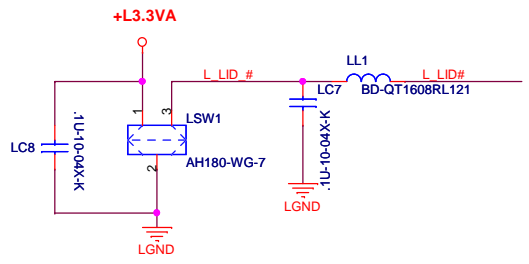
C42II LED BD Ver:C 8L
P/N: 35G4C4230-C0
Made in China.

PCB2
PCB
35G4C4230-C0

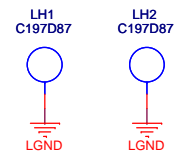
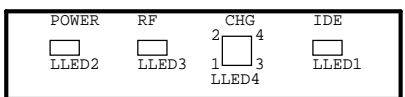
LED



LID



Color	Sus/Wireless	Charger	
	Blue	Blue	Red
5mA	390_1	390_1	560_1
20mA	90.9	100	140



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TitleLED/LID BD

SizeDocument NumberSCHEMATIC1RevC

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