

Berry DG15 Discrete/UMA Schematics Document

Arrandale

Intel PCH

2009-10-12

REV : X00

*DY :None Installed
UMA:UMA platform installed
DIS:DIS platform installed
Madisan:gDDR3 1GB platform installed
Colay :Manual modify BOM*

<Core Design>



Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Cover Page

Size
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AMD Graphic
Madison-LP / Park-XT
(Discrete only)


80, 81, 82, 83, 84

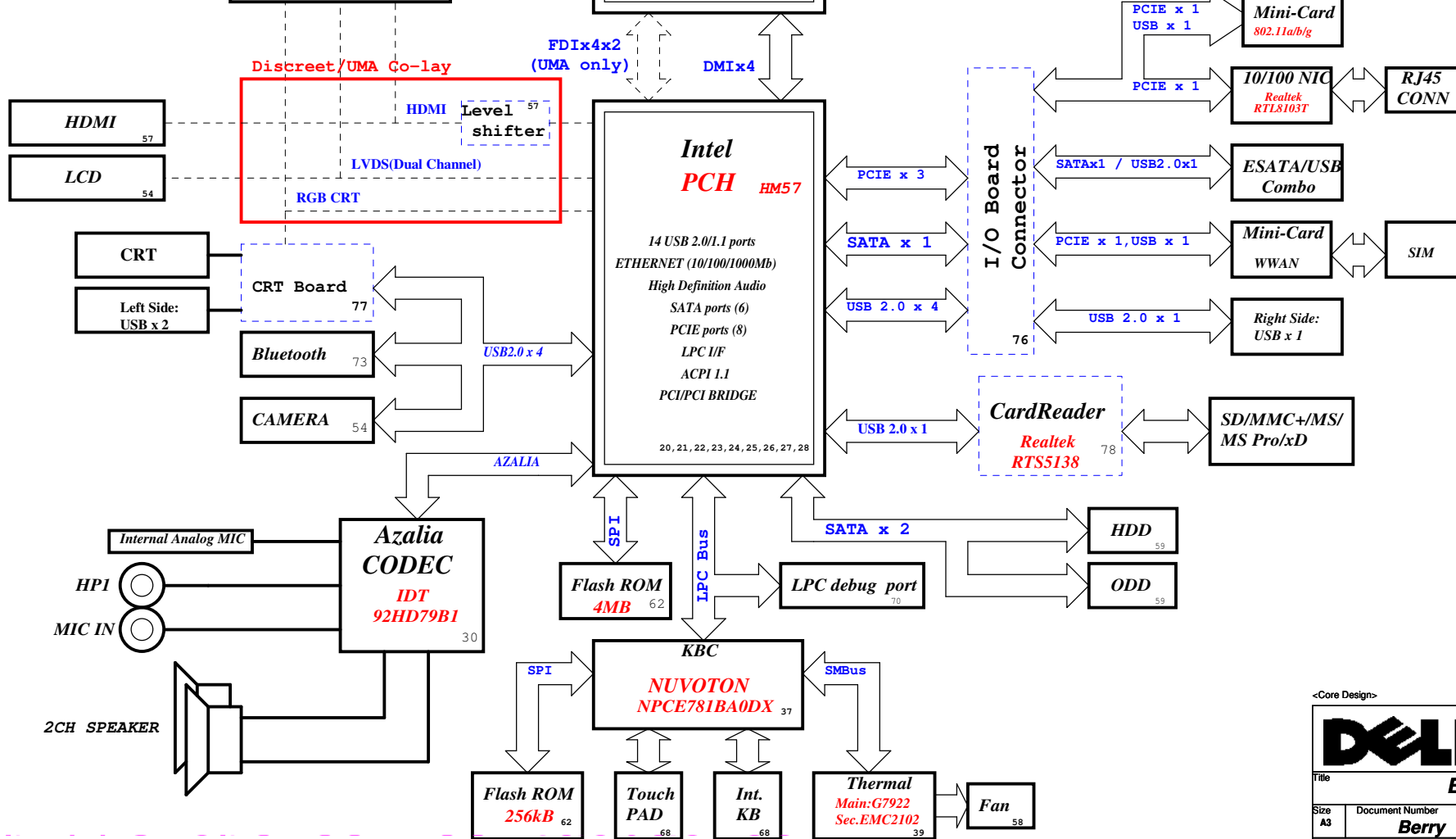
Clock Generator
SLG8SP585

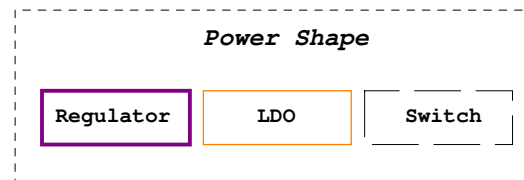
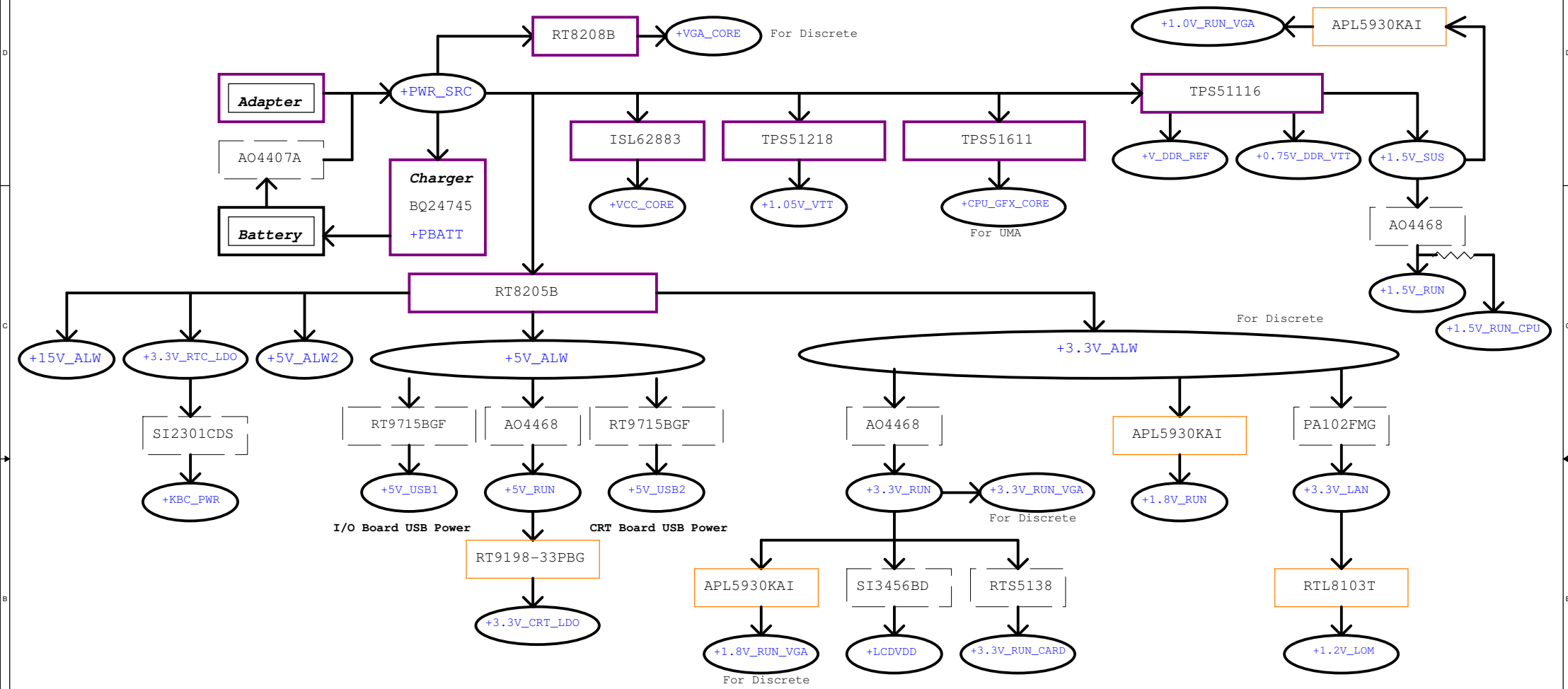
Intel CPU
Arrandale

Project code : 91.4HH01.001
PCB P/N : 48.4HH01.0SA
Revision : 09909-SA

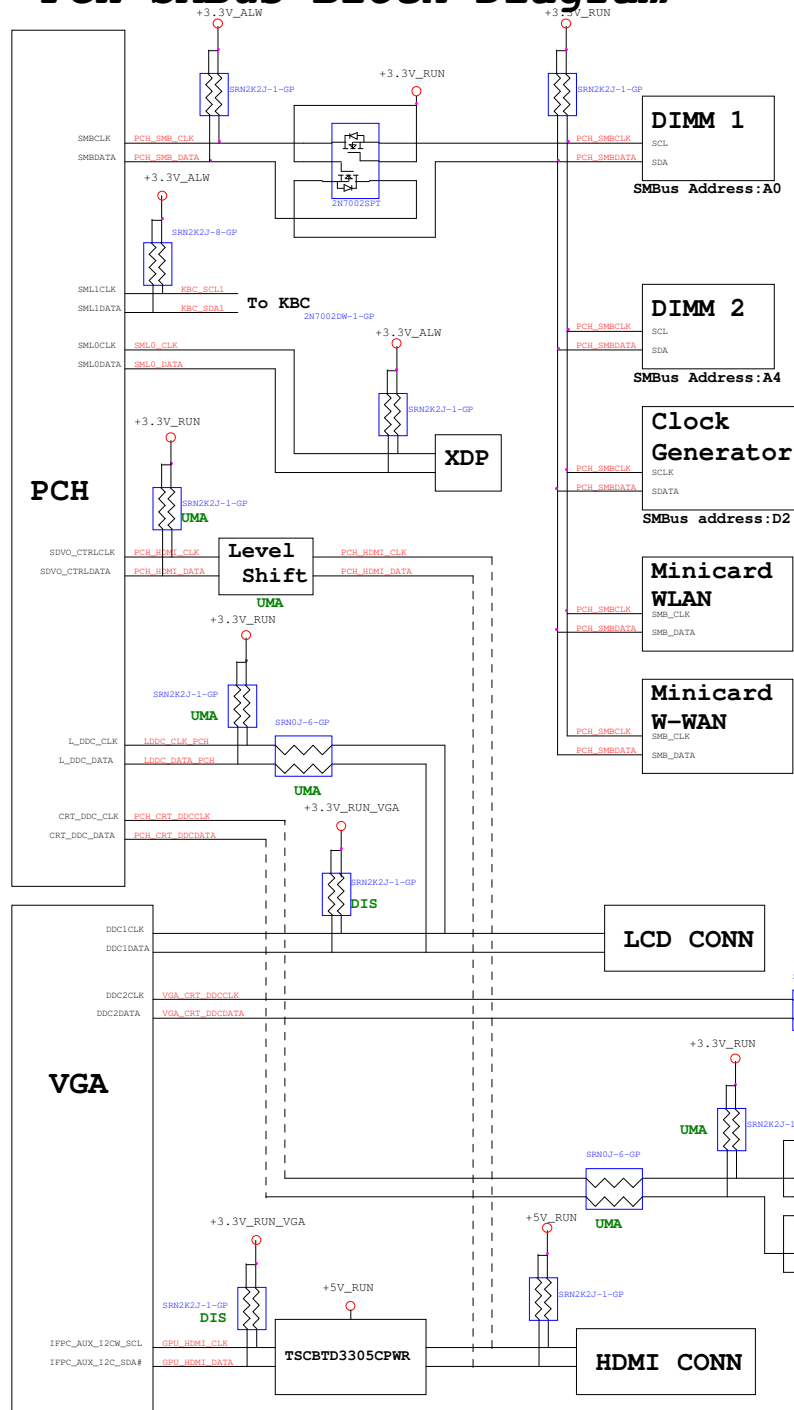
CPU DC/DC ISL62883		47
INPUTS	OUTPUTS	
+PWR_SRC	+VCC_CORE	
SYSTEM DC/DC TPS51218		48
INPUTS	OUTPUTS	
+PWR_SRC	+1.05V_VTT	
SYSTEM DC/DC RT8205B		49
INPUTS	OUTPUTS	
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +5V_ALW +3.3V_ALW +15V_ALW	
SYSTEM DC/DC TPS51116		50
INPUTS	OUTPUTS	
+PWR_SRC	+1.5V_SUS +0.75V_DDR_VTT +V_DDR_REF	
SYSTEM DC/DC TPS51611		51
INPUTS	OUTPUTS	
+PWR_SRC	+CPU_GFX_CORE	
VGA RT8208B		89
INPUTS	OUTPUTS	
+PWR_SRC	+VGA_CORE	
TI CHARGER BQ24745		45
INPUTS	OUTPUTS	
+DC_IN +PBATT	+PWR_SRC	
SYSTEM DC/DC APL5930		51
INPUTS	OUTPUTS	
+3.3V_ALW	+1.8V_RUN +1.8V_RUN_VGA	
SYSTEM DC/DC APL5930		90
INPUTS	OUTPUTS	
+1.5V_SUS +5V_ALW +3.3V_ALW	+1.0V_RUN_VGA +5V_RUN +3.3V_RUN	
Switches		
INPUTS	OUTPUTS	
+1.5V_SUS +5V_ALW +3.3V_ALW	+1.5V_RUN +5V_RUN +3.3V_RUN	
PCB LAYER		
L1:Top		
L2:VCC		
L3:Signal		
L4:Signal		
L5:GND		
L6:Bottom		

<Core Design>		L6: Bottom	
		Wistron Corporation 21F, B8, Sec.1, Hsin Tai Wu Rd., Hsieh, Taipei Hsien 221, Taiwan, R.O.C.	
Title		Block Diagram	
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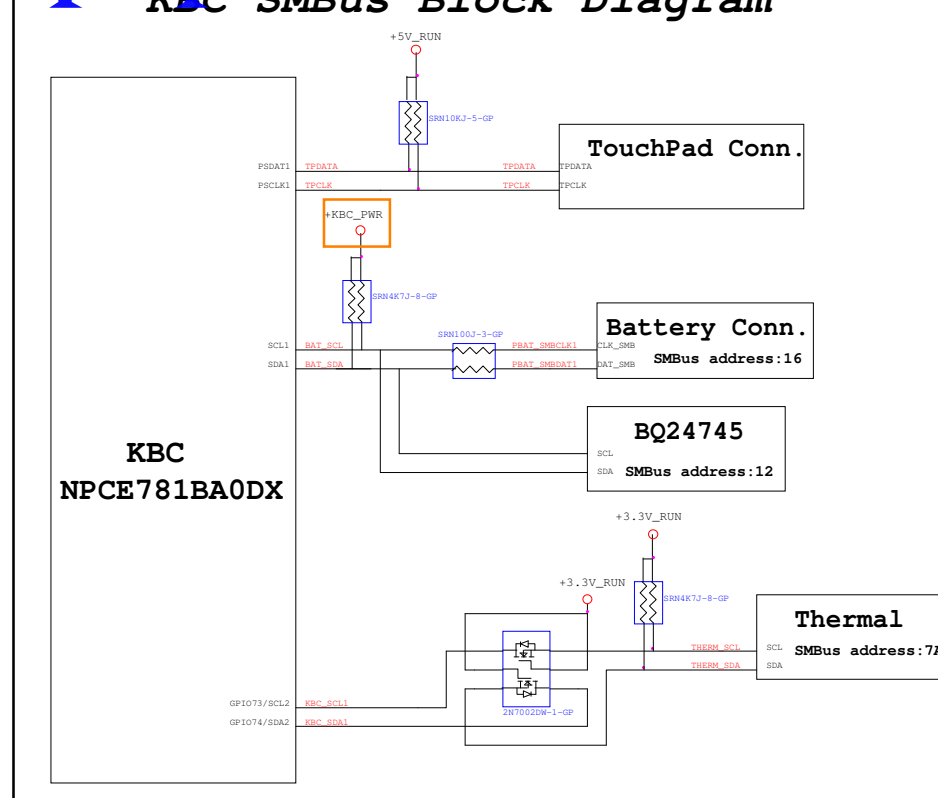




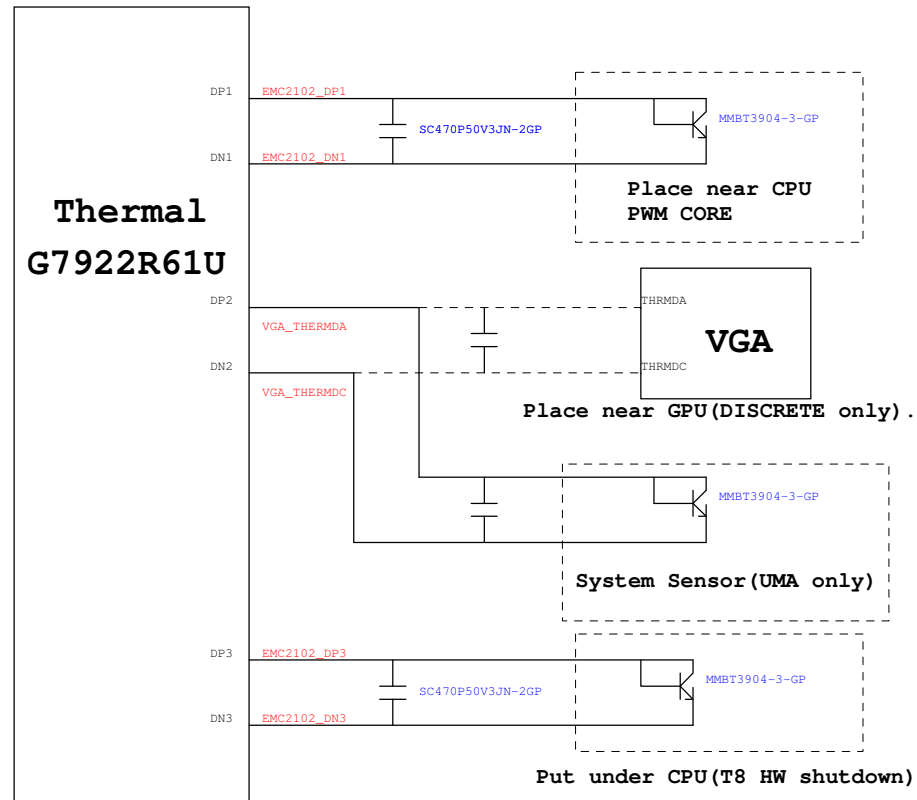
PCH SMBus Block Diagram



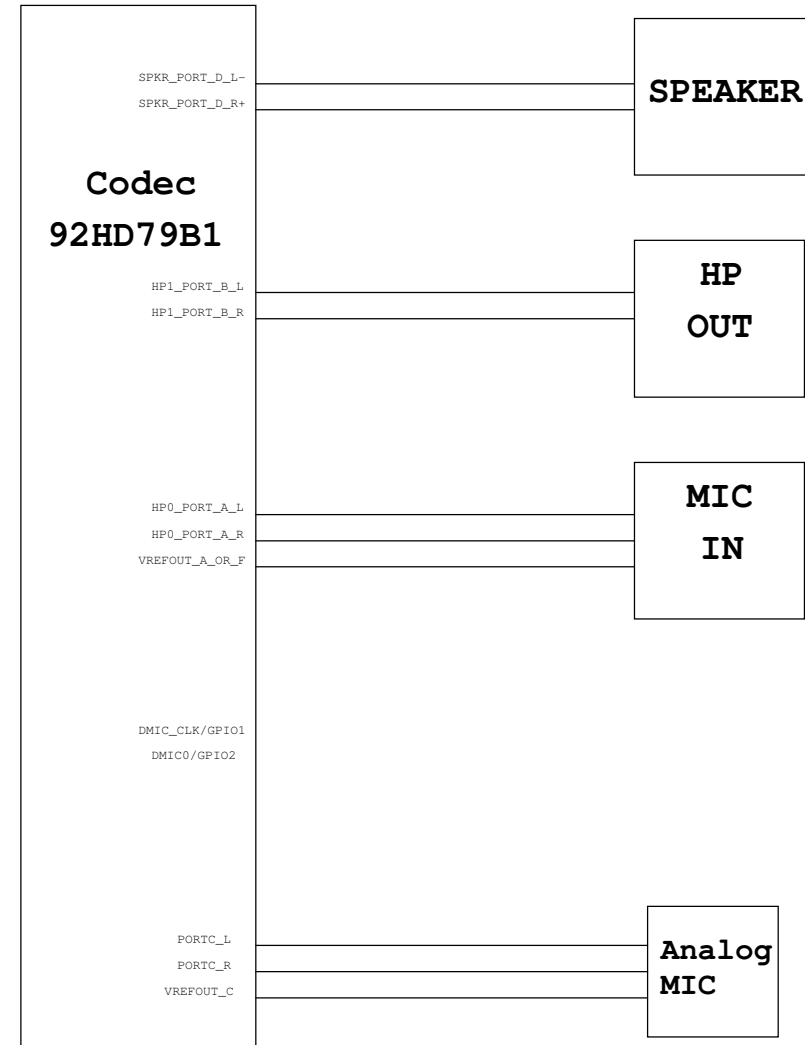
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



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PCH Strapping

Calpella Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap Mode (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled
GNT0#, GNT1#/GPIO51	Default (SPI): Left both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/GPIO53	Default - Internal pull-up. Low (0) = Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	Default: Do not pull low. Disable ME in Manufacturing Mode: Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable iTPM: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN#/GPIO[33]	Low (0): Flash Descriptor Security will be overridden. High (1) : Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

PCIE Routing

LANE1	RESERVED
LANE2	MiniCard WLAN
LANE3	LAN
LANE4	W-WAN
LANE5	RESERVED
LANE6	RESERVED
LANE7	H55/HM55 no support
LANE8	H55/HM55 no support

USB Table

USB	
Pair	Device
0	USB2 (CRT Board)
1	USB3 (CRT Board)
2	WLAN (I/O Board)
3	RESERVED
4	CARD READER
5	BLUETOOTH
6	HM55 no support
7	HM55 no support
8	USB1 (I/O Board)
9	USB0 (I/O Board ESATA)
10	RESERVED
11	W-WAN (I/O Board)
12	RESERVED
13	CAMERA

SATA Table


SATA	
Pair	Device
0	HDD
1	ODD
2	HM55 no support
3	HM55 no support
4	ESATA
5	RESERVED

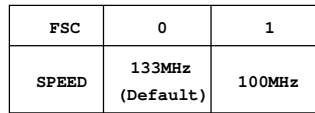
Processor Strapping

Calpella Schematic Checklist Rev.0_7

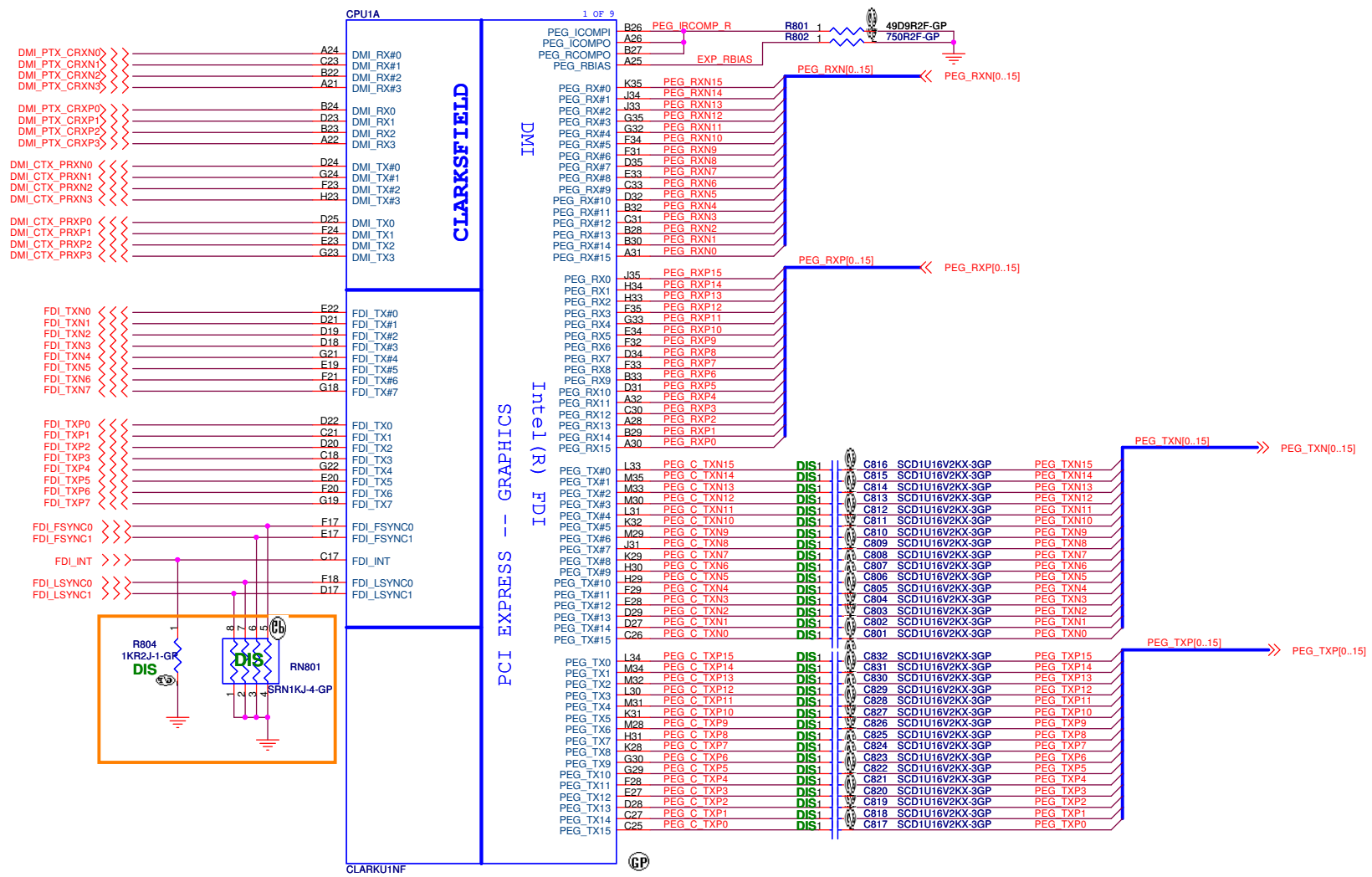
Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	Reserved - Temporarily used for early Clarksfield samples.	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor Note: Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

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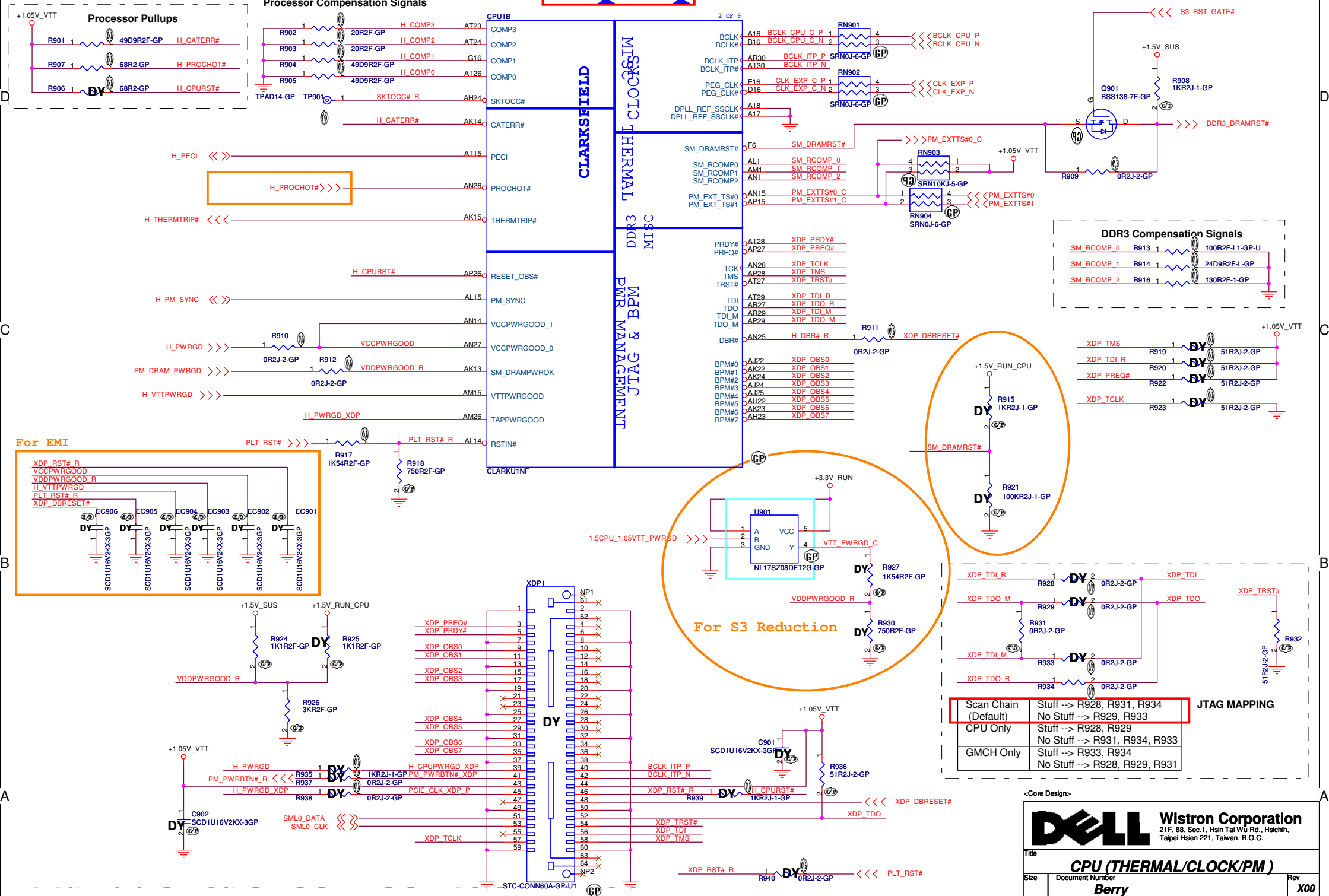
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Title			
<i>Table of Content</i>			
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SSID = CPU



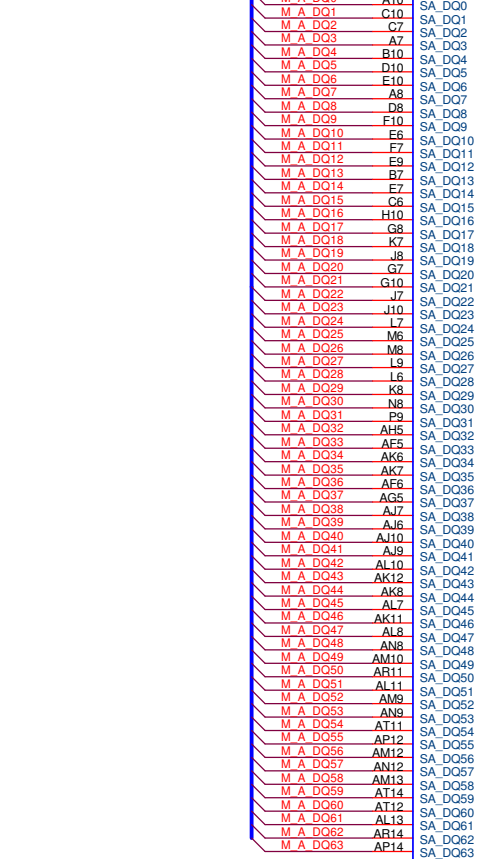
62.10055.341
SEC. 62.10053.561



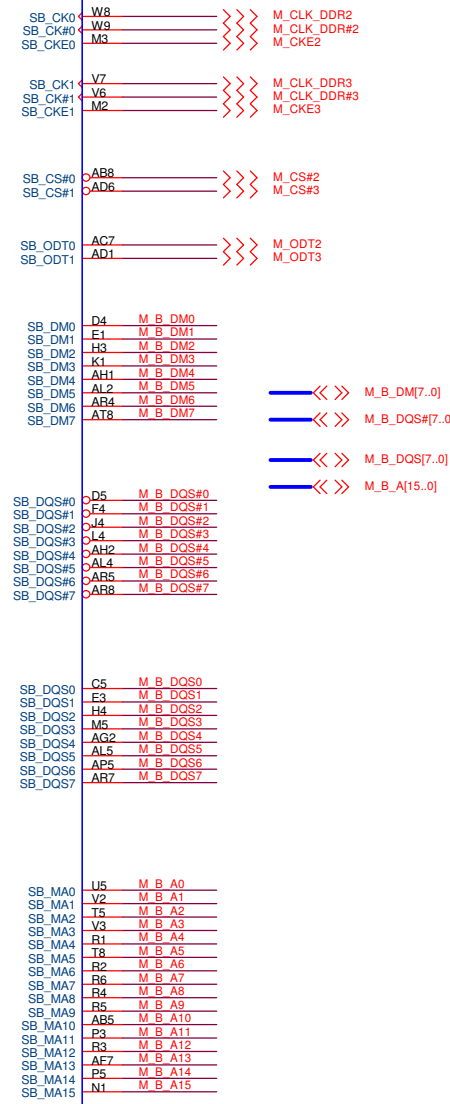
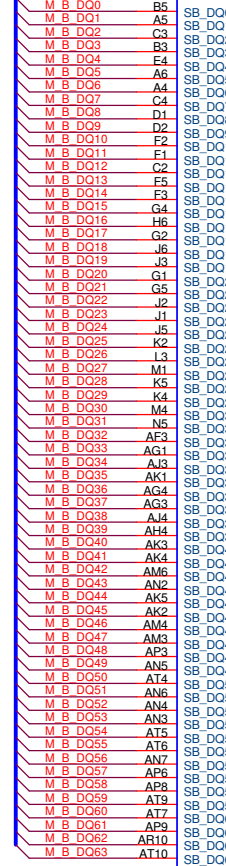
SSID = CPU

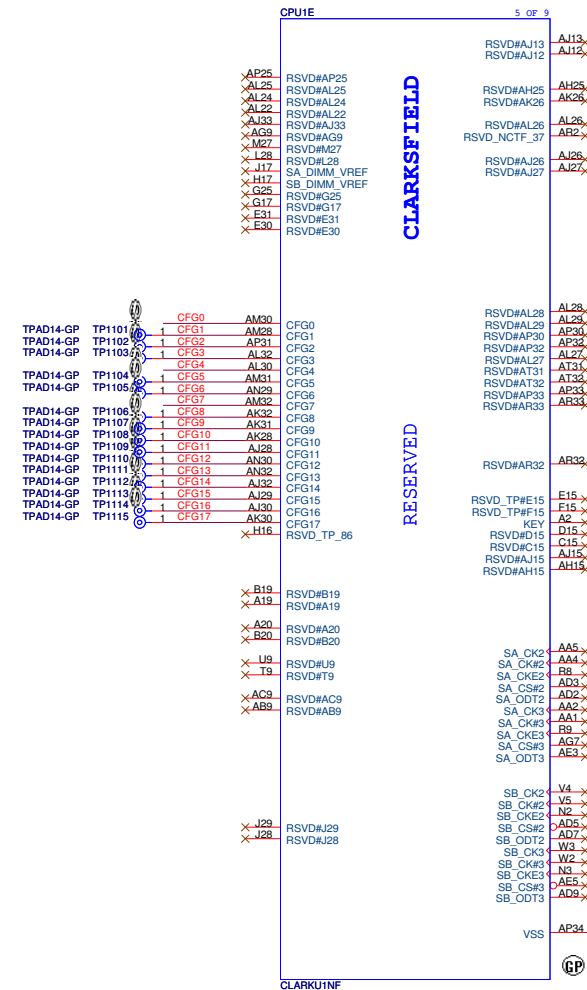
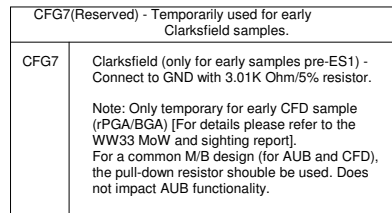
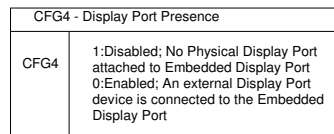
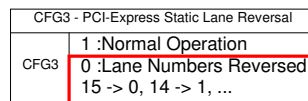
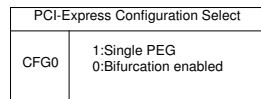
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M_A_DQ[63..0] <<>> M_A_DQ[63..0]

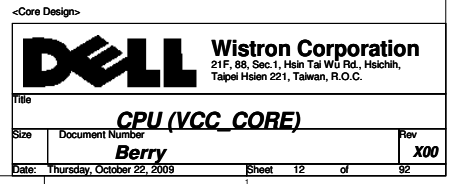


M_B_DQ[63..0] <<>> M_B_DQ[63..0]





VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.





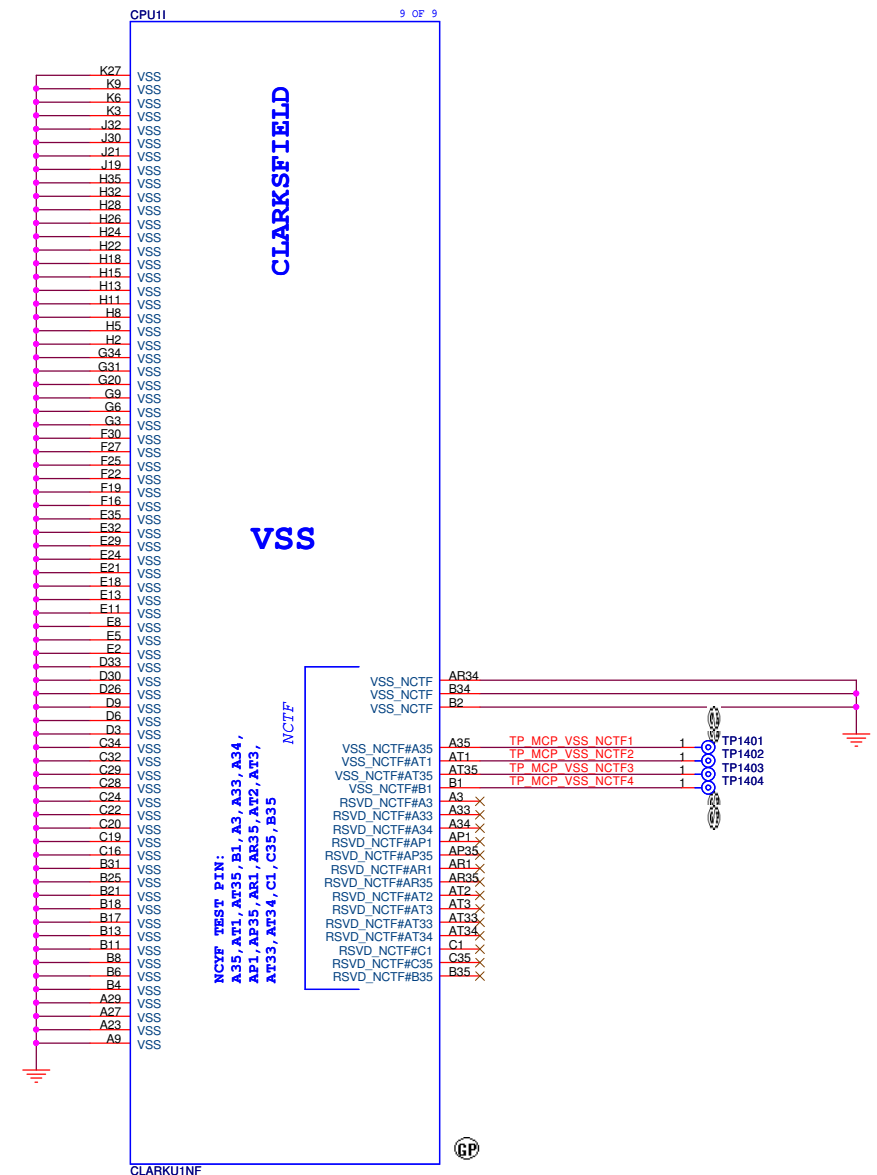
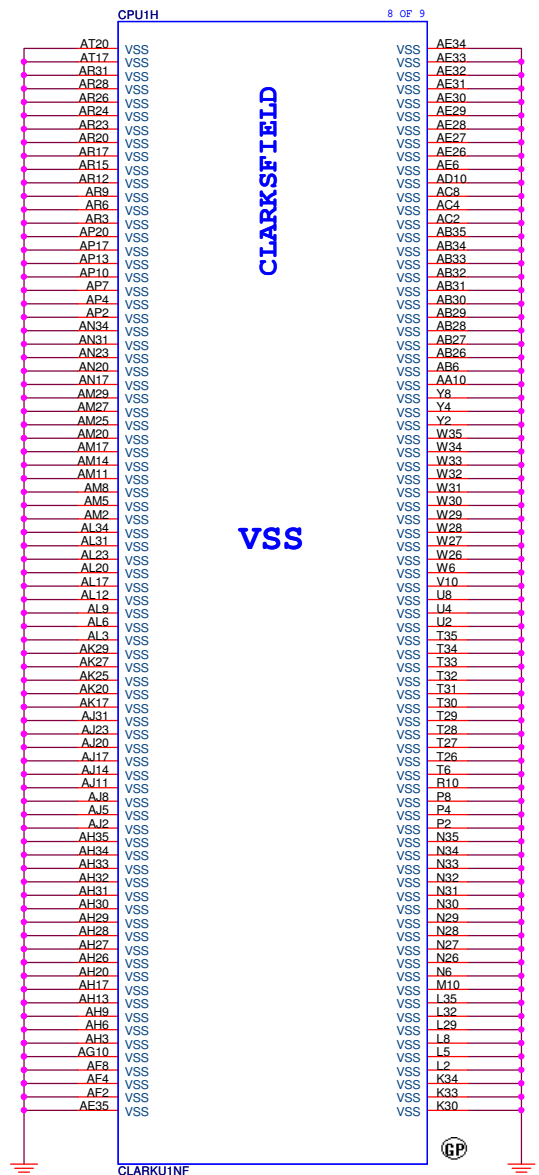
CPU (VCC GFXCORE)

Rev

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SSID = CPU



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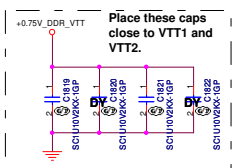
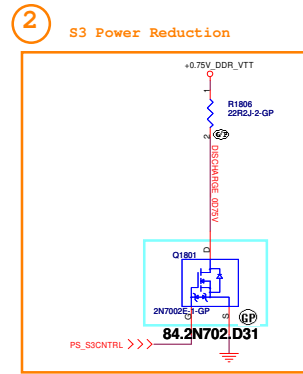
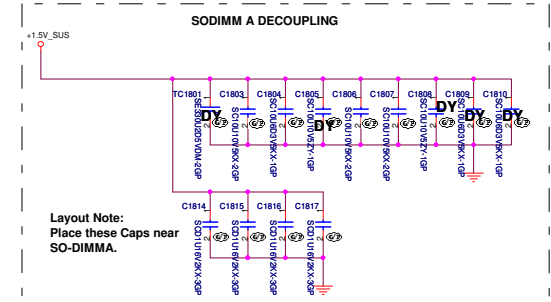
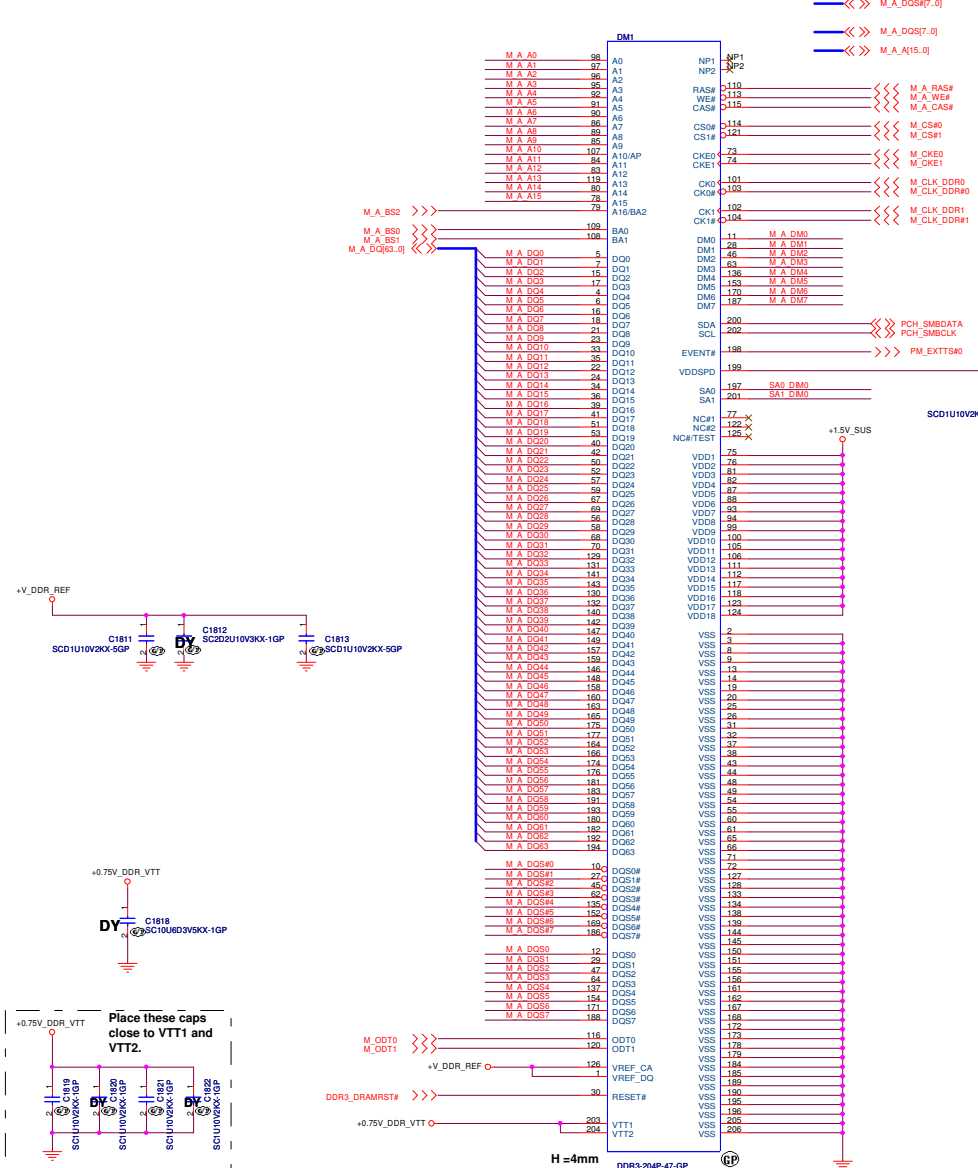
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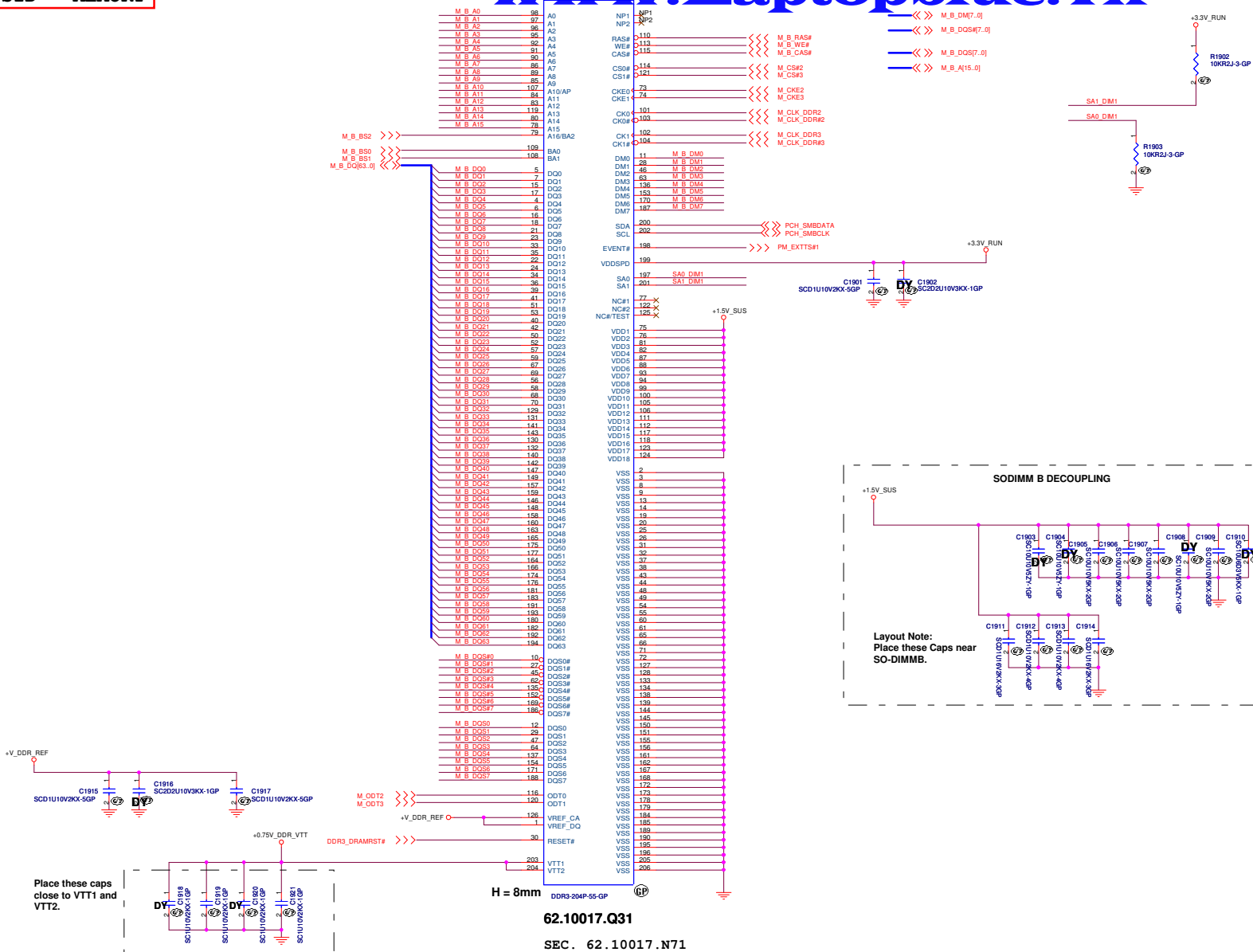
<<< M_A_CS#
<<< M_A_DQS#(7..0)
<<< M_A_DQS#(7..0)
<<< M_A_A[15..0]

Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

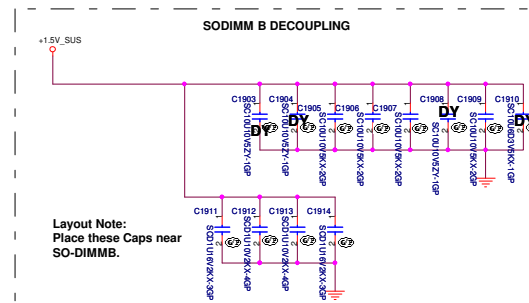


62.10017.P31
SEC. 62.10017.P11



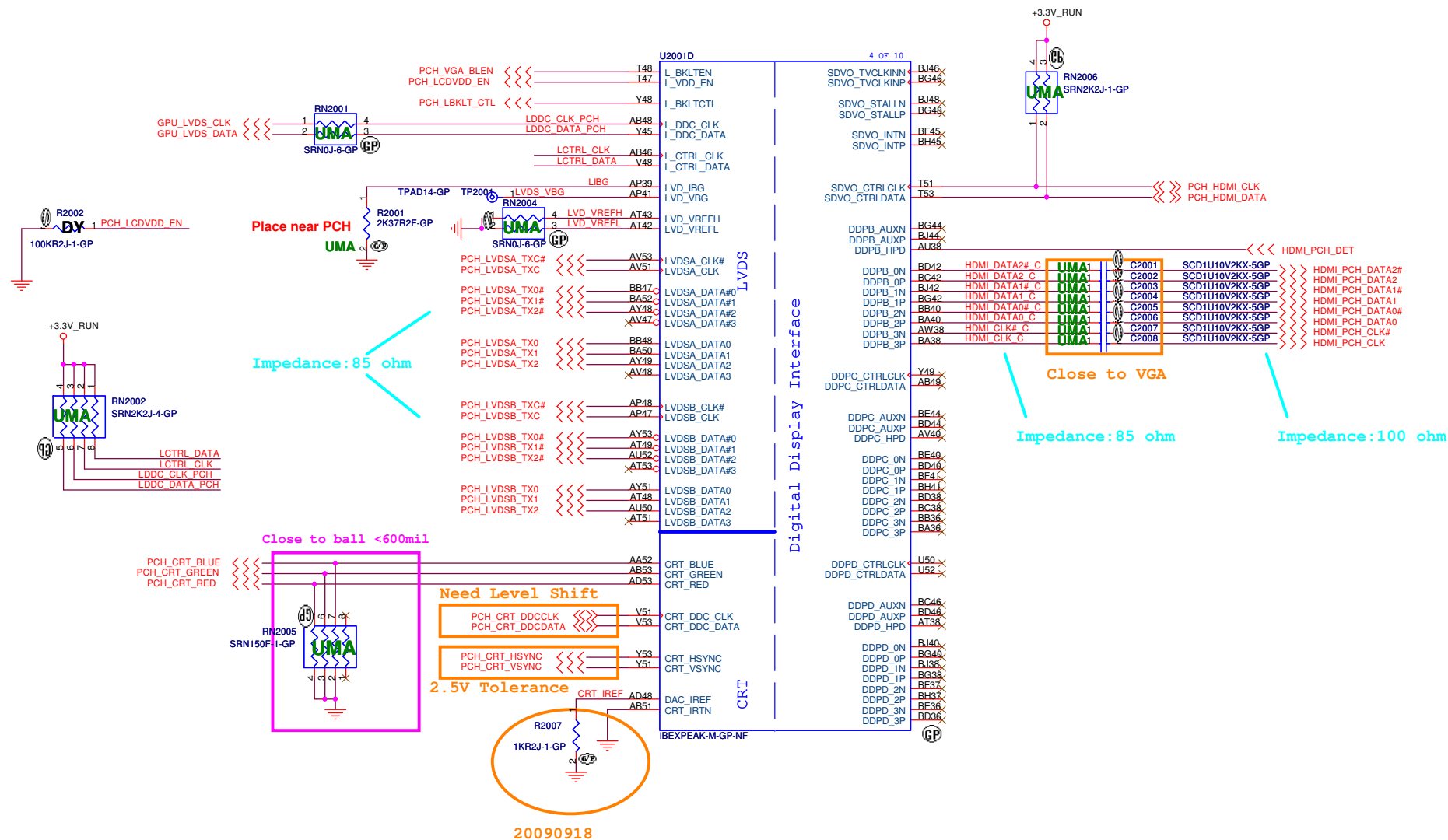
Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32



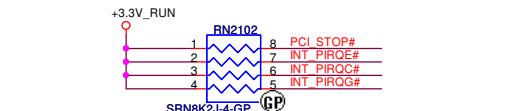
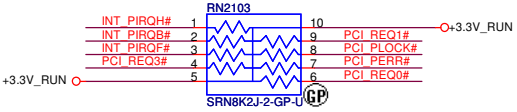
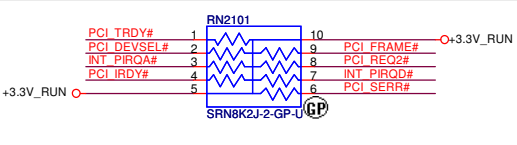
Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

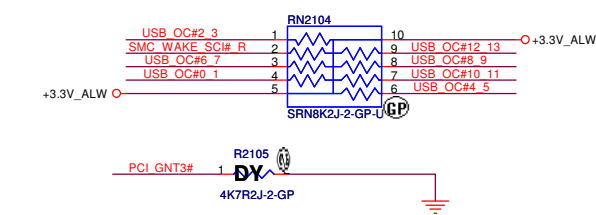


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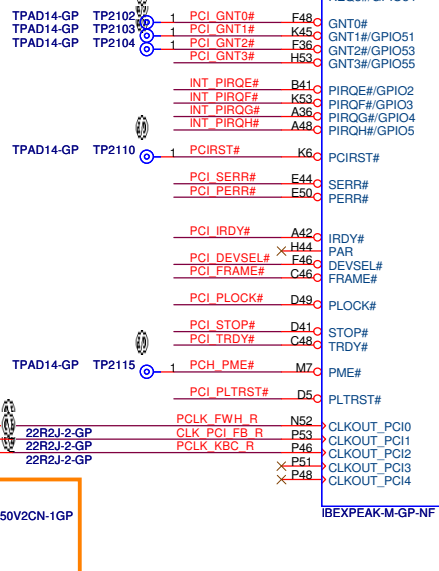
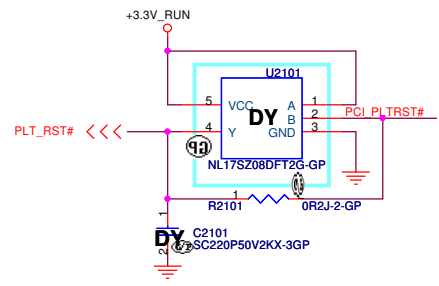
SSID = PCH



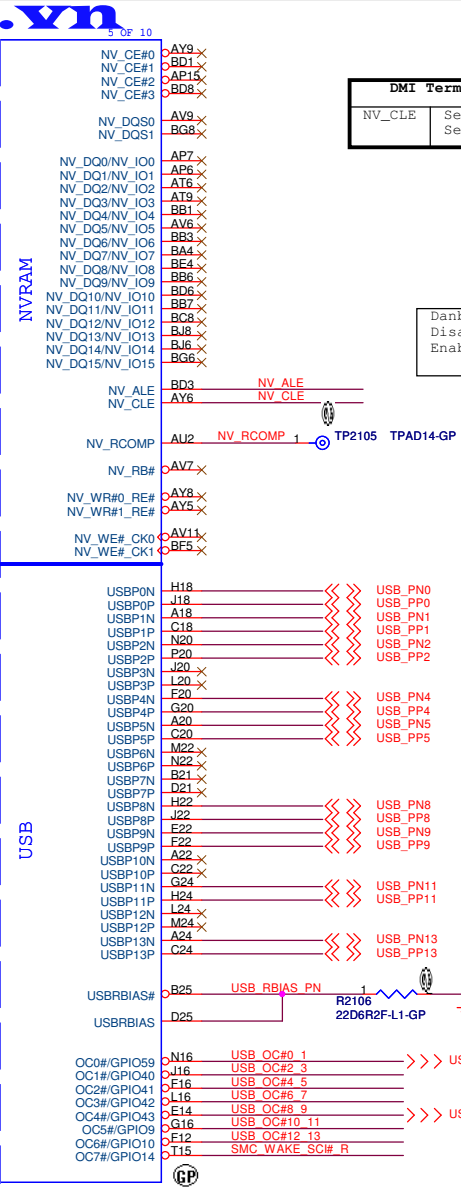
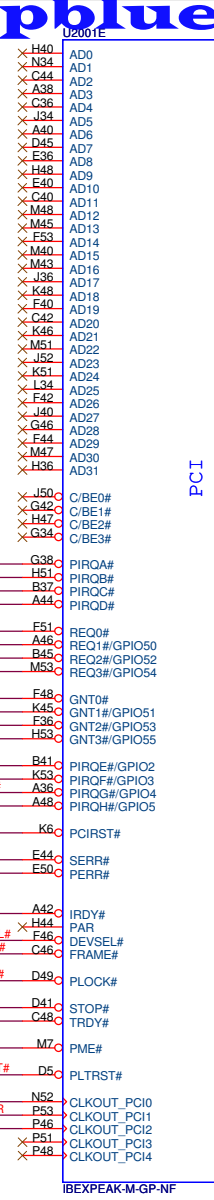
BOOT BIOS Strap		
PCI_GNT#1	PCI_GNT#0	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI (Default)



A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default



KBC CLK EMI



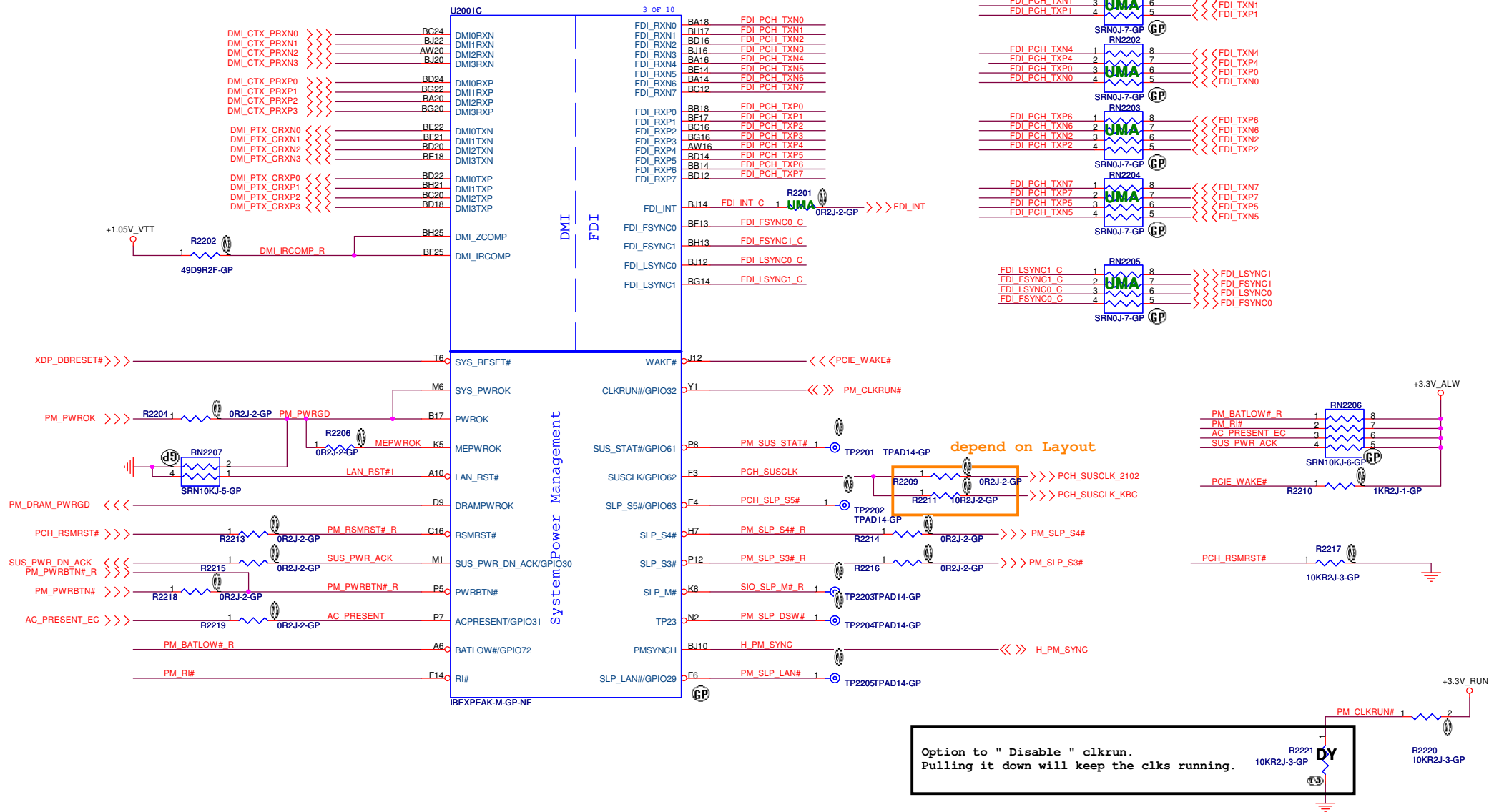
DMI Termination Voltage	
NV_CLE	Set to Vss when low. Set to Vcc when high.

Danbury Technology:
Disabled when Low.
Enable when High.

USB	
Pair	Device
0	USB2 (CRT Board)
1	USB3 (CRT Board)
2	WLAN (I/O Board)
3	X
4	CARD READER
5	BLUETOOTH
6	X
7	X
8	USB1 (I/O Board)
9	ESATA (I/O Board COMBO)
10	X
11	W-WAN (I/O Board)
12	X
13	CAMERA

SSID = PCH

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PCH (DM I/FDI/PM)

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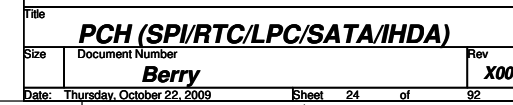
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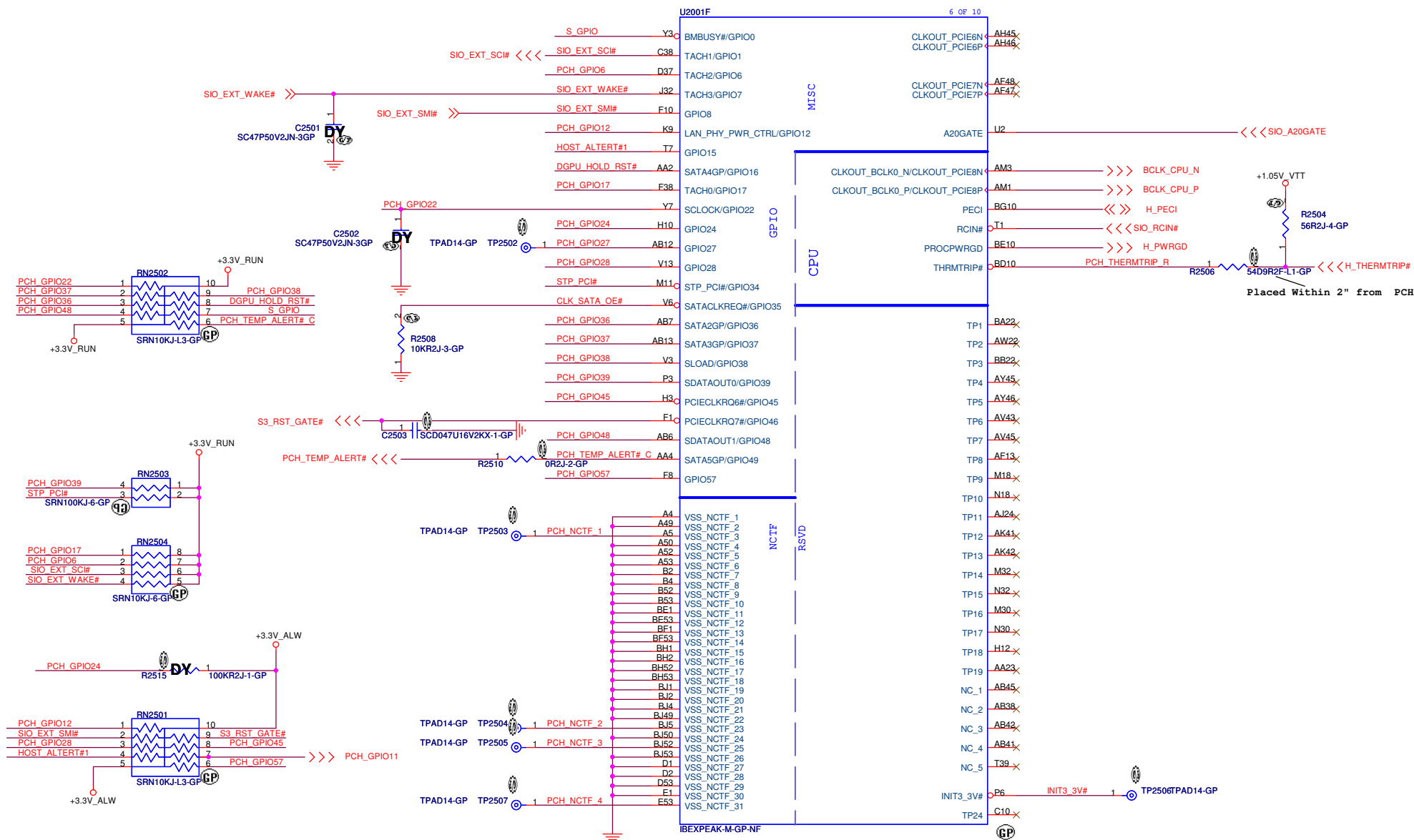
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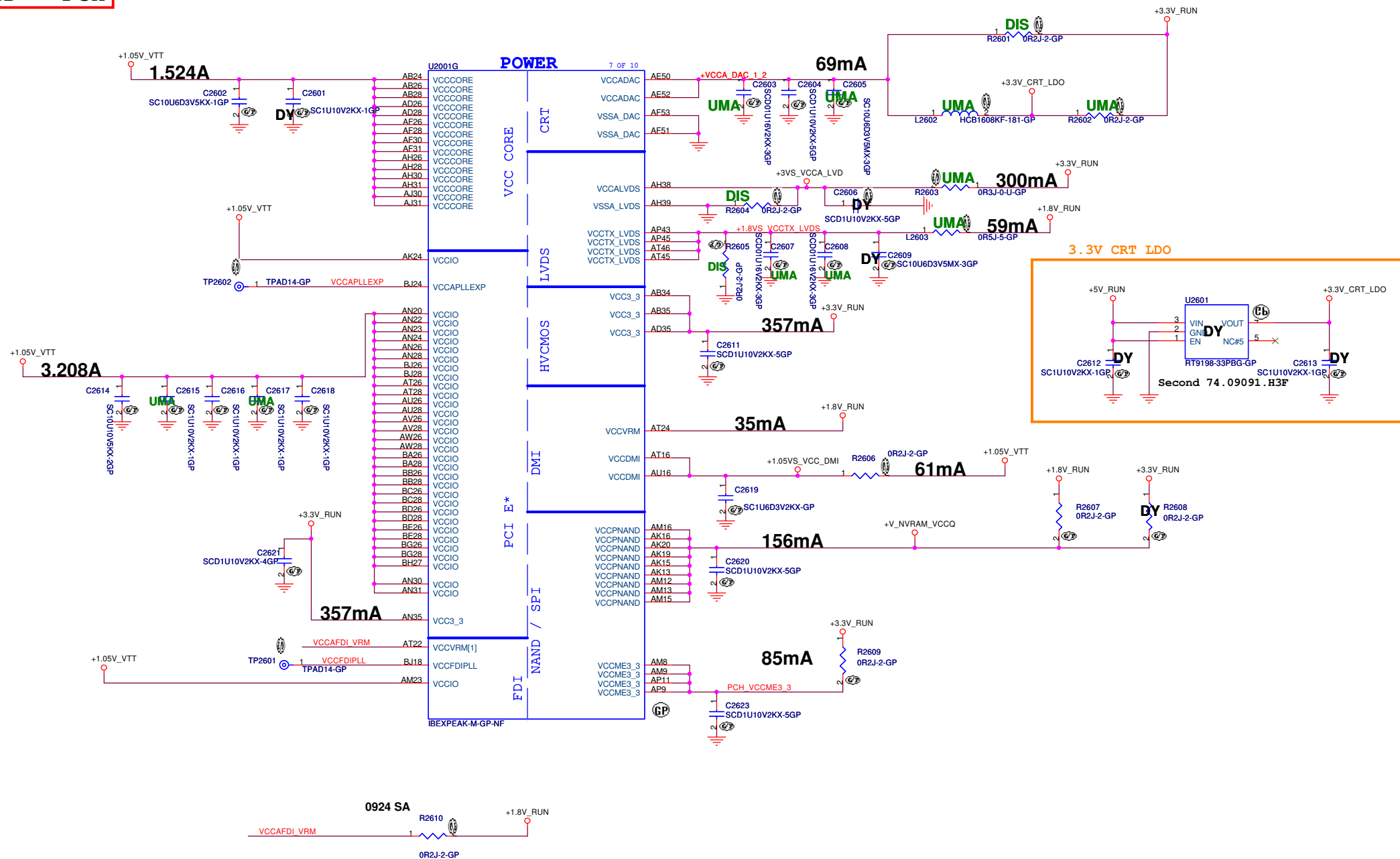
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SSID = PCH



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SSID = PCH



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Title: **PCH (VSS)**

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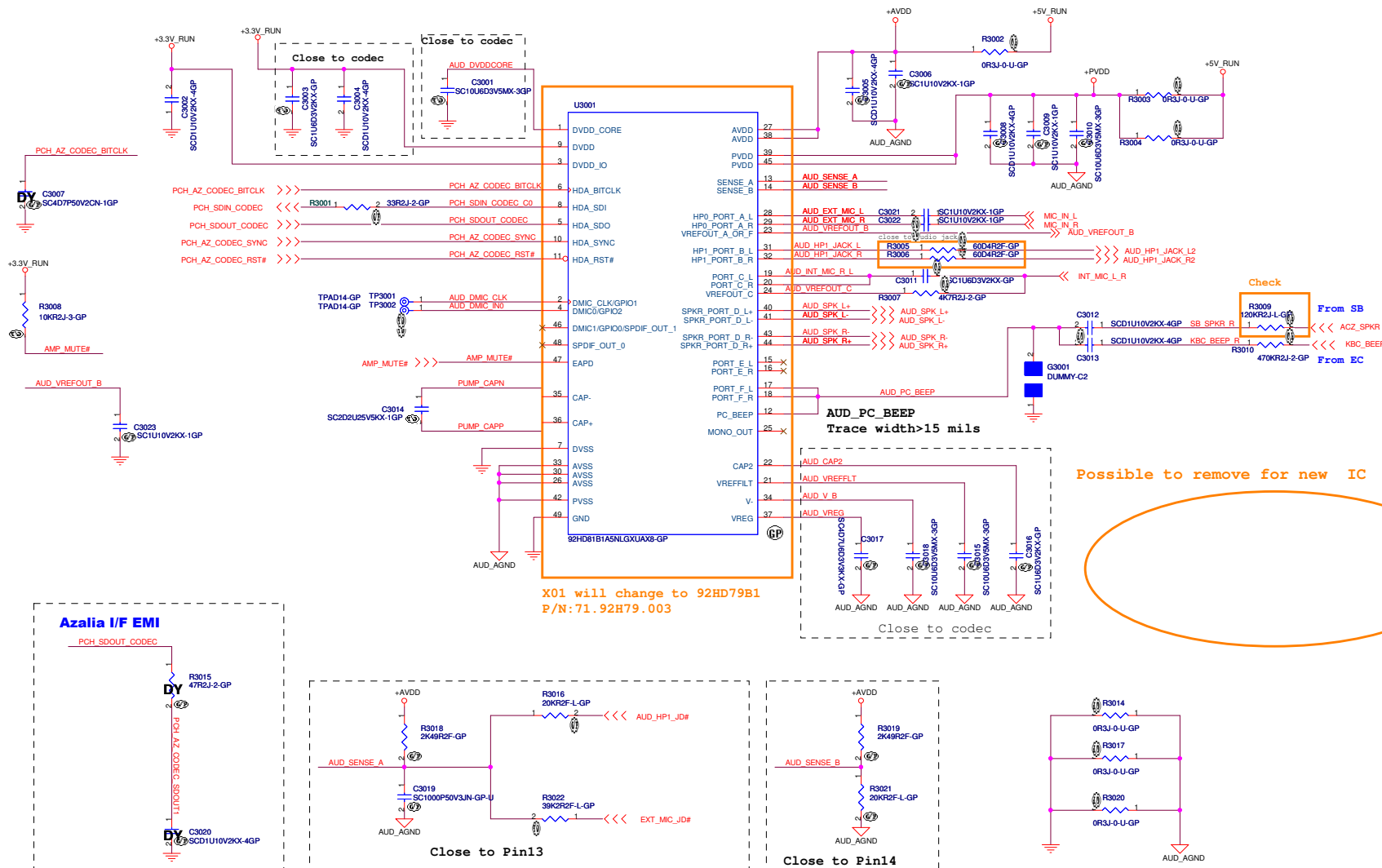
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SSID = AUDIO



Possible to remove for new IC

X01 will change to 92HD79B1
P/N:71.92H79.003

Close to codec

Azalia I/F EMI

Close to Pin13

Close to Pin14

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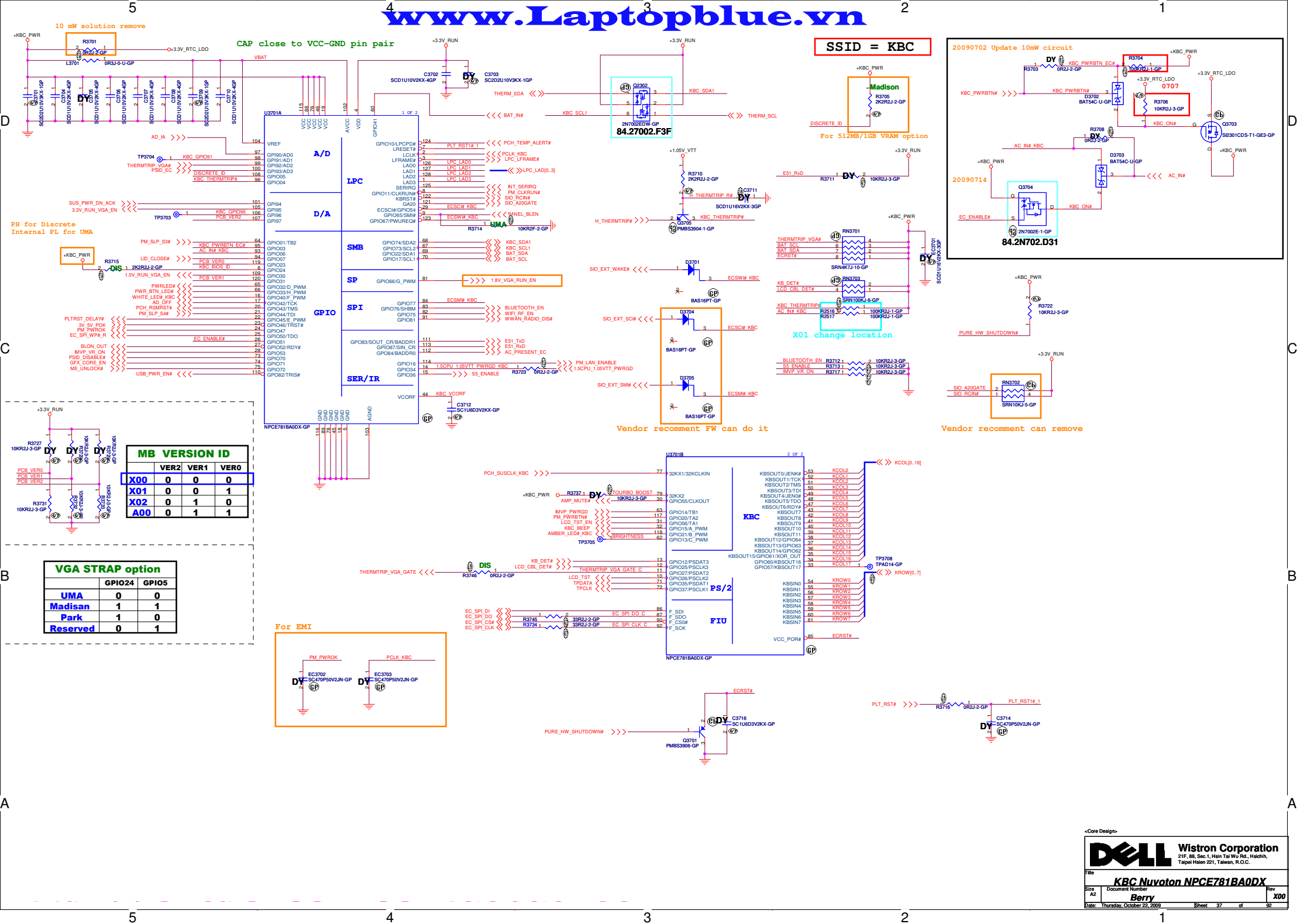
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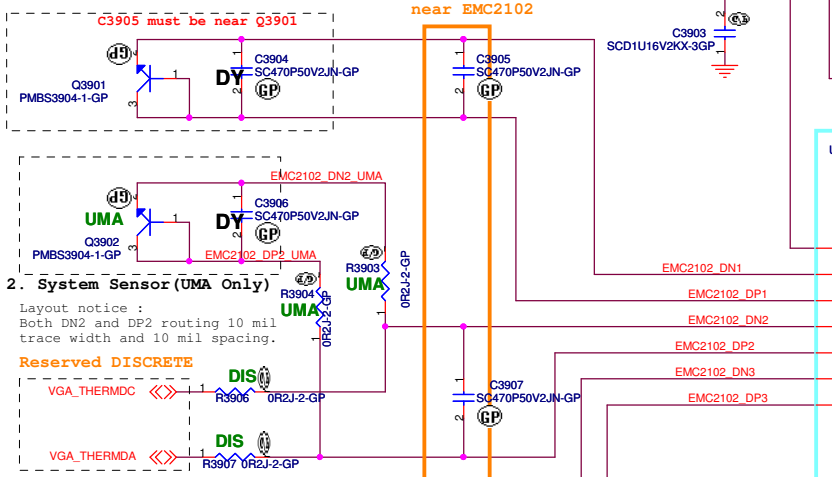
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SSID = Thermal

1. Place near CPU PWM CORE and PCH.

Layout notice :
Both DN1 and DP1 routing 10 mil
trace width and 10 mil spacing.



2. System Sensor (UMA Only)

Layout notice :
Both DN2 and DP2 routing 10 mil
trace width and 10 mil spacing.

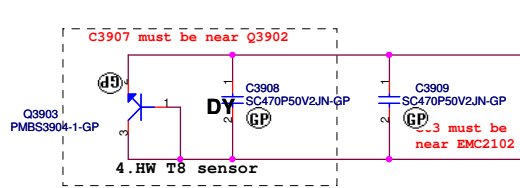
Reserved DISCRETE

VGA_THERMDC <<<

VGA_THERMDA <<<

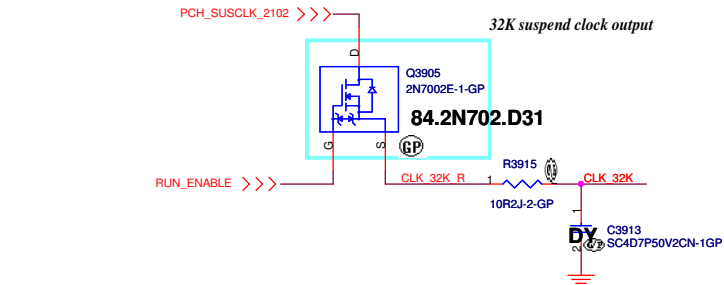
3. VGA Sensor (DISCRETE Only)

Layout notice :
Both VGA_THERMDA and VGA_THERMDC routing
10 mil trace width and 10 mil spacing.



4. HW T8 sensor

Layout notice :
Both DN3 and DP3 routing 10 mil
trace width and 10 mil spacing.



32K suspend clock output

84.2N702.D31

C3913 SC4D7P50V2CN-1GP

GND = Channel 1
OPEN = Channel 3
+3.3V = Disabled

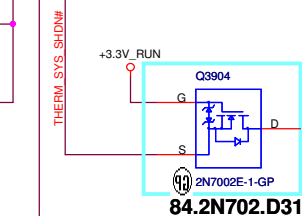
GND = Fan is OFF
OPEN = Fan is at 60% full-scale
+3.3V = Fan is at 75% full-scale

EMC2102_FAN_TACH <<< EMC2102_FAN_TACH
EMC2102_FAN_DRIVE >>> EMC2102_FAN_DRIVE

THERM_SCL
THERM_SDA

CLK_IN
CLK_SEL
RESET#
TP3901

EMC2102_DZK-GP
THERM_POWER_OK#
THERMTRIP#



84.2N702.D31

Main G7922R61U for GMT P/N:74.07922.0B3
SEC. EMC2102 for SMSC P/N:74.02102.A73

GND = Internal Oscillator Selected
+3.3V = External 32.768kHz Clock Selected

TRIP_SET Pin Voltage
 $V_DEGREE = ((Degree - 75) / 21)$

T8 shutdown is set 88 deg-C.

<Core Design>

DELL		Wistron Corporation	
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Title Thermal/Fan Controllor EMC2102			
Size	Document Number	Rev	X00
Custom	Berry		
Date:	Thursday, October 22, 2009	Sheet	39 of 92

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<Core Design>



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Title

Reserved

Size
A3

Document Number
Berry

Rev
X00

Date: Wednesday, October 14, 2009

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<Core Design>



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Title

Reserved

Size
A3

Document Number

Berry

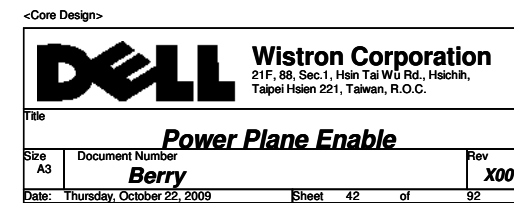
Rev

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<Core Design>



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Title

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Size
A3

Document Number

Berry

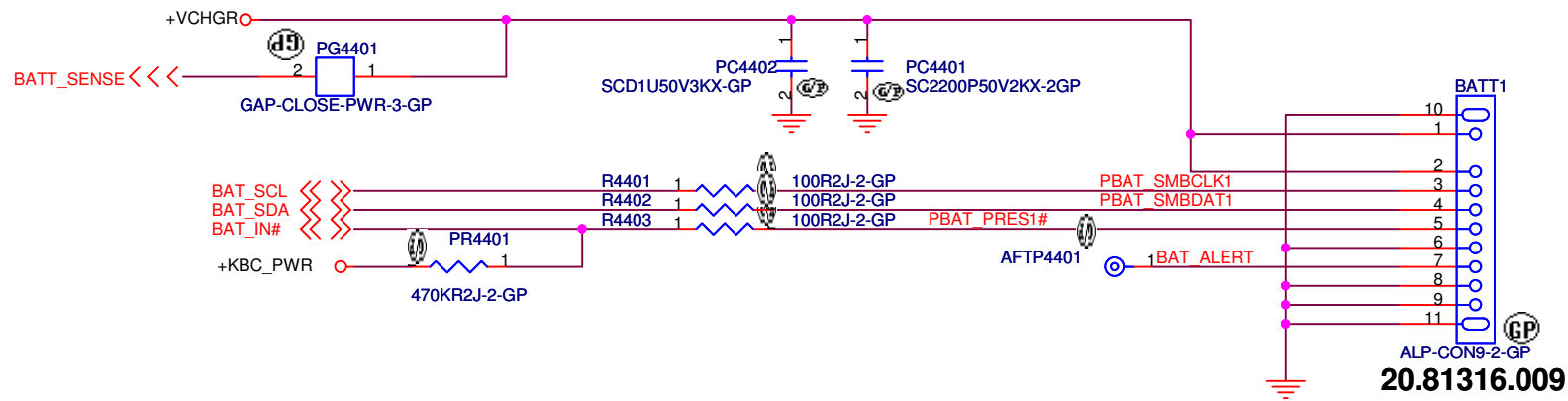
Rev

X00

Date: Wednesday, October 14, 2009

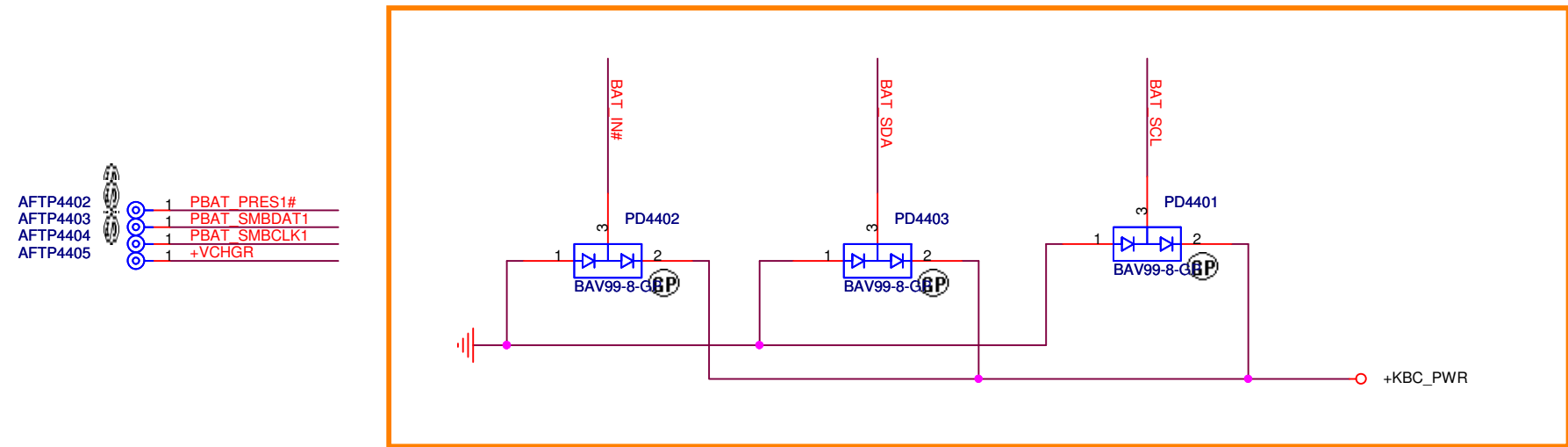
Sheet 43 of 92

Batt Connector




For actual location, need to be swap all pin

Close to Batt Connector



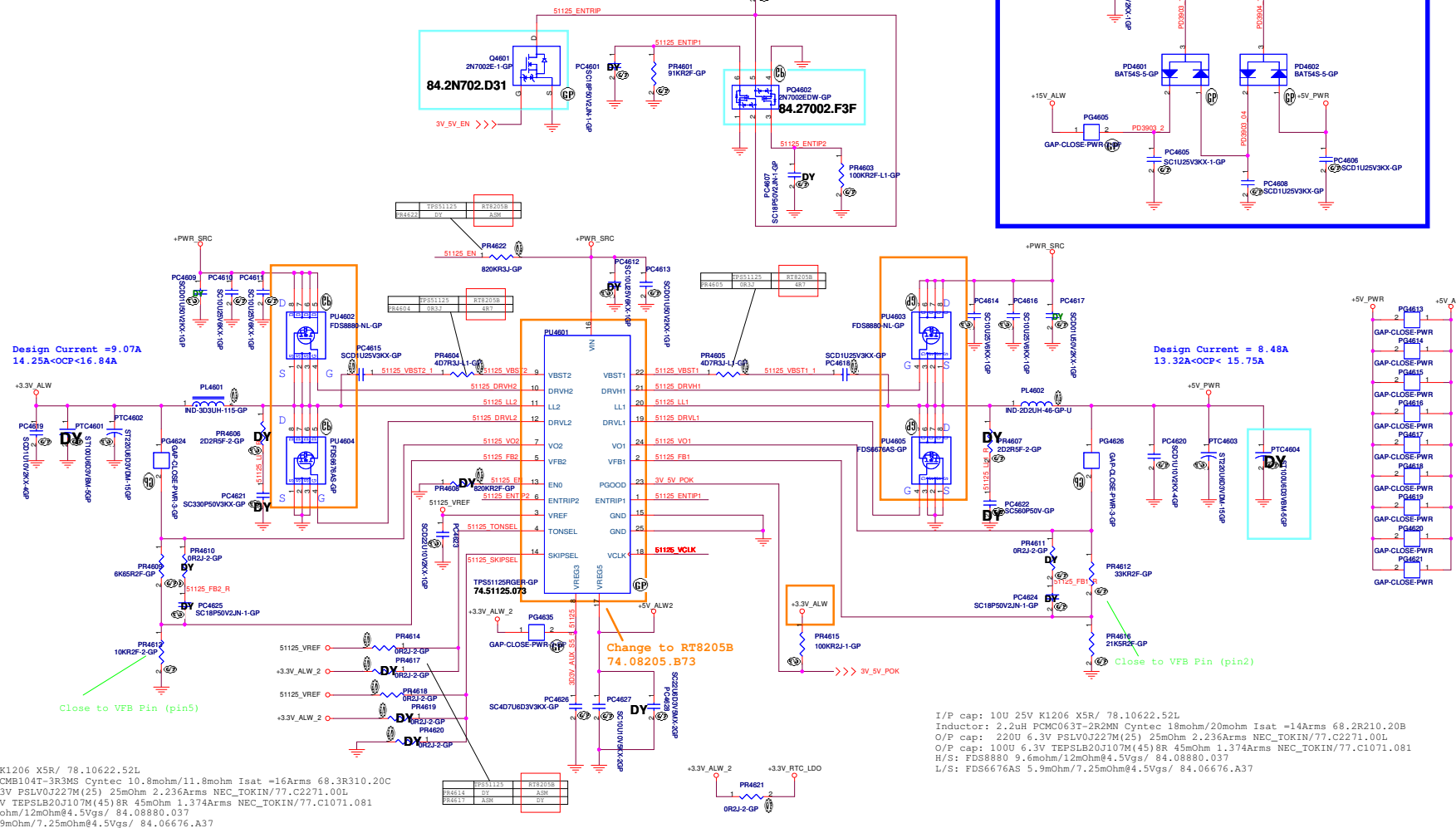
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: BATT CONN			
Size: A4	Document Number: Berry		Rev: X00
Date: Thursday, October 22, 2009		Sheet: 44	of: 92

**CHARGER BQ24745**

Rev	X00
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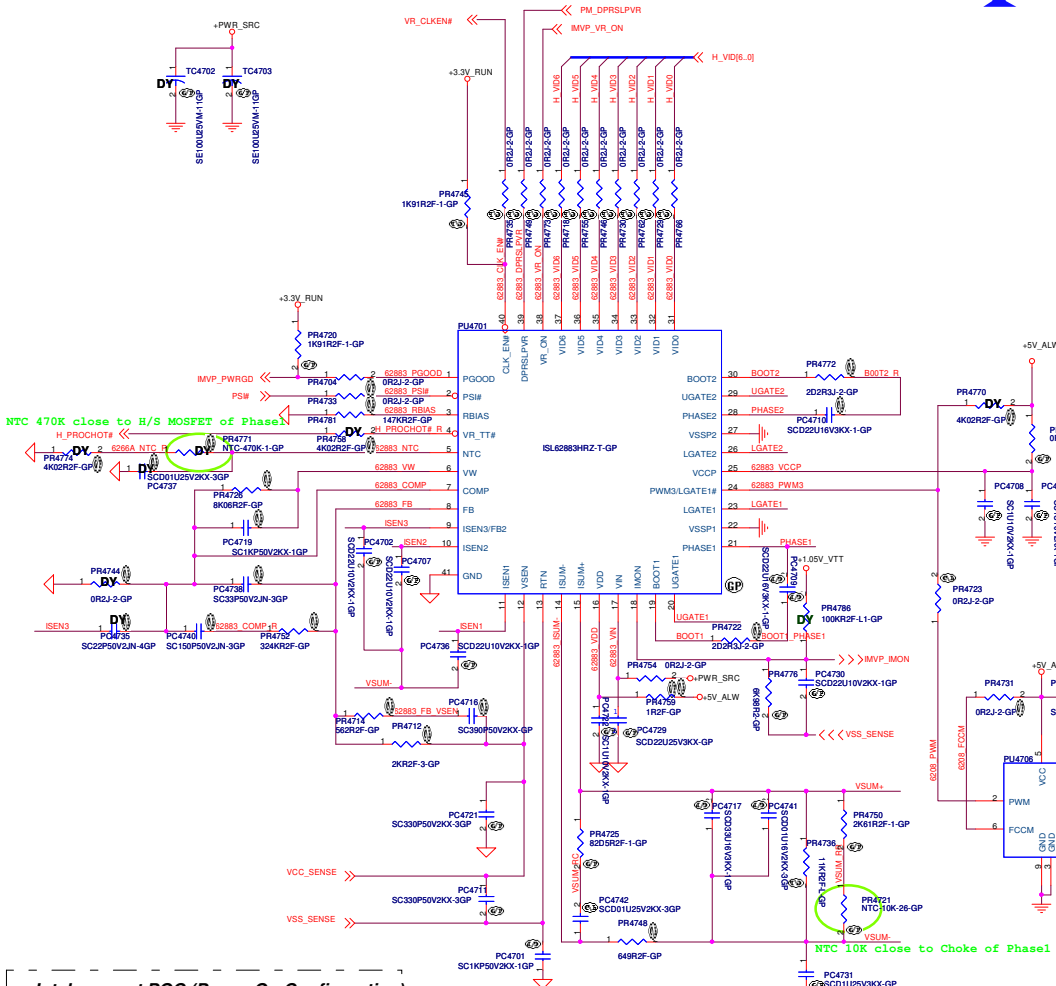
I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2uH PCMC063T-2R2NM (Cyntec 18mohm/20mohm Isat =14Arms 68R.2R10.20B
O/P cap: 220U 6.3V PSLV0J22J27M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V TEPSLB20J107M(45)58R 45mOhm 1.374Arms NEC_TOKIN/77.C1071.08R
H/S: FDS8880 9.6mohm/12mOhm@4.5Vgs/ 84.08880.037
L/S: FDS6676AS 5.9mOhm/7.25mOhm@4.5Vgs/ 84.06676.A37

TPS51123:

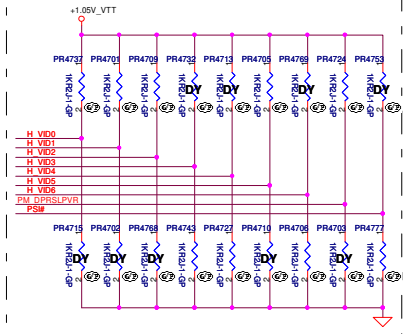
TONESEL	CH1	CH2	SKIPSEL	VREG3 or VREG5	VREF (2V)	GND
GND	200kHz	265kHz	Operating Mode	OOA Auto Skip	Auto Skip	PWM only
VREF	245kHz	305kHz				
VREG3	300kHz	375kHz				
VREG5	365kHz	460kHz				

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both IDOs, VCLK on and ready to turn on switcher channels	enable both IDOs, VCLK off and ready to turn on switcher channels	disable all circuit

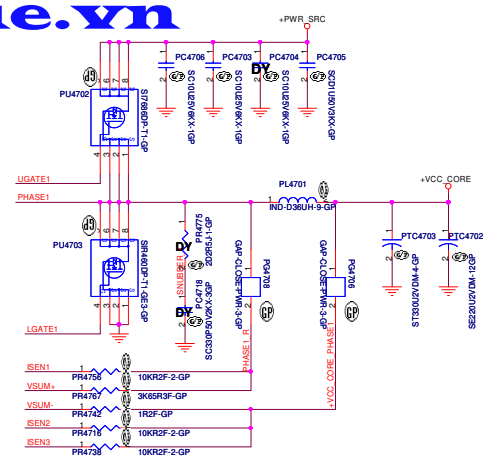
TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3	365kHz	460kHz
VREG5	365kHz	460kHz



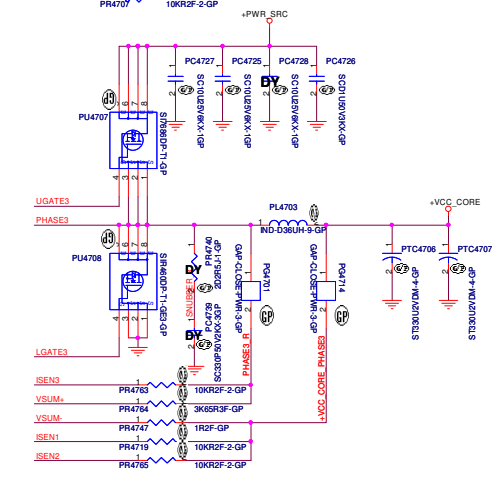
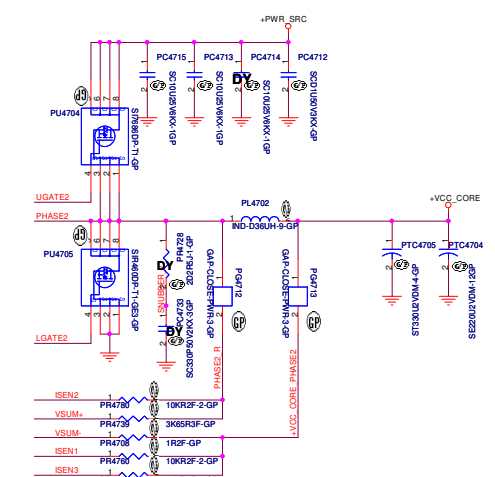
Intel support POC (Power On Configuration).



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
 Inductor: 0.36UH PCMC104T-R36NN1R05J Cyntec 1.05mohm/ 68.R3610.20C
 O/P cap: 330U 2V EEF5X0D221E7 6mOhm 3.0Arms Panasonic/79.33719.20L
 O/P cap: 220U 2V EEF5X0D331XE 7mOhm 3.4Arms Panasonic/79.22719.90L
 H/S: S17686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
 L/S: S1R460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037



Design Current = 48A
 52.8A < OCP < 67.2A



<Core Design>

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Title

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Size
A3

Document Number

Berry

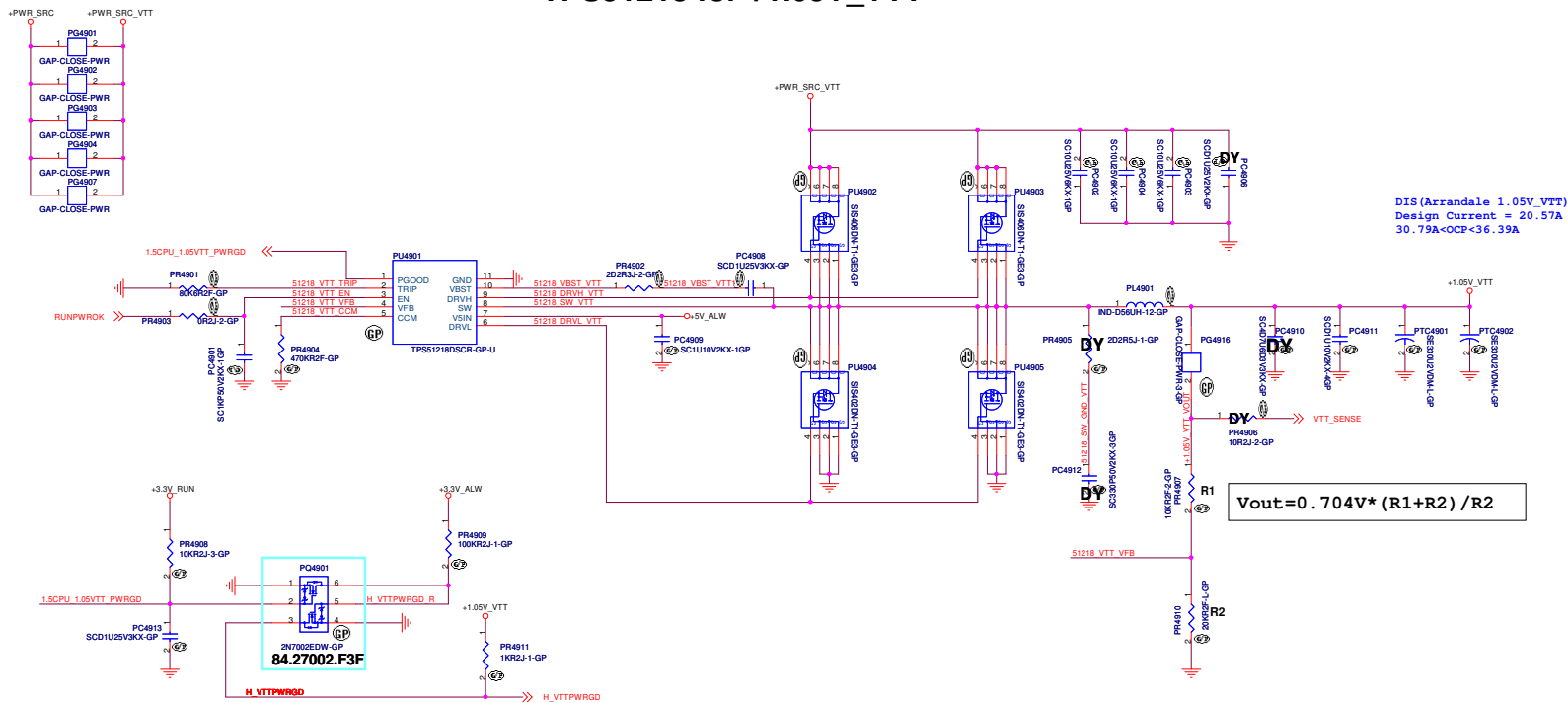
Rev

X00

Date: Wednesday, October 14, 2009

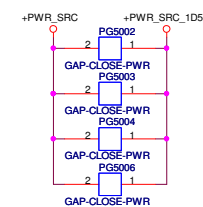
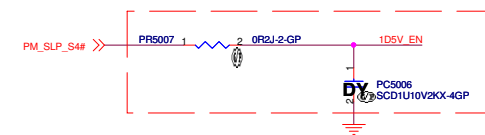
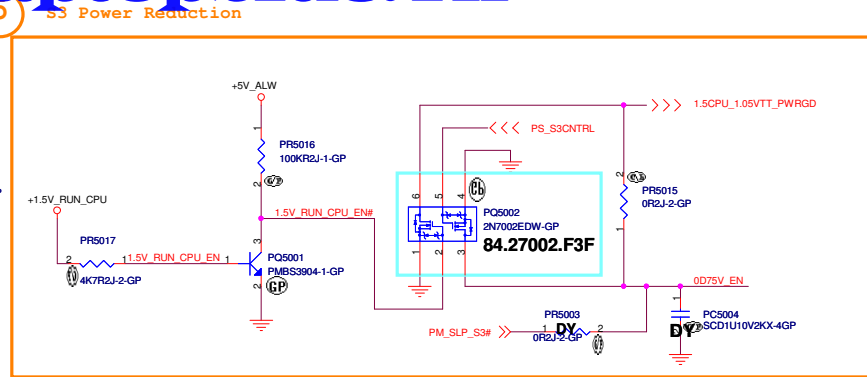
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TPS51218 for +1.05V_VTT

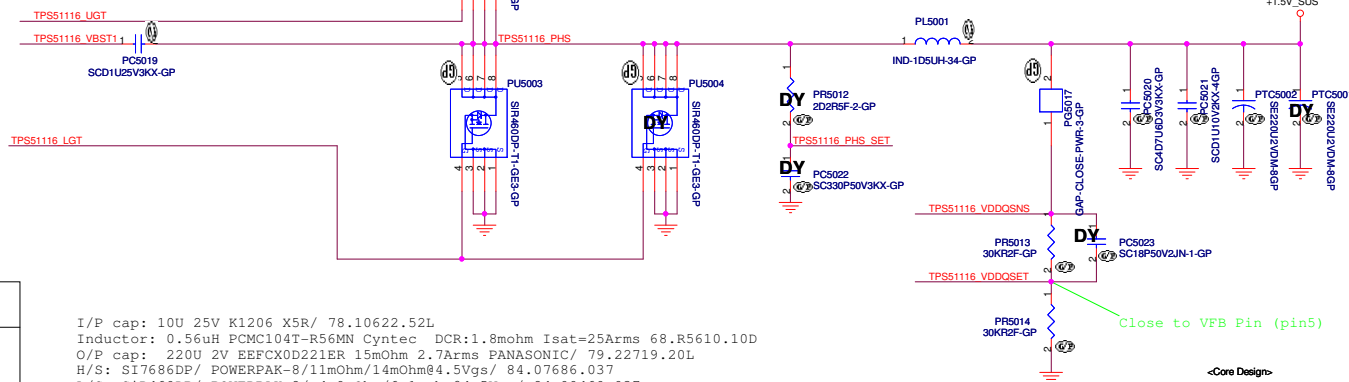


I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cynotec DCR:1.6mohm/1.8mohm Isat=25Arms 68.R5610.100
O/P cap: 330U 2.5V EEF5X0D331ER 9mOhm 3Arms PANASONIC/ 79.33719.L01
H/S: SIS406DN/ POWERPAK-8/ 11.5mOhm/14.5mOhm 84.5Vgs/ 84.00406.037
L/S: SIS402DN/ POWERPAK-8/ 6.4mOhm/8mohm@4.5Vgs/ 84.00402.037

<Core Design>



Design Current = 14.45A
22.71A < OCP < 26.84A

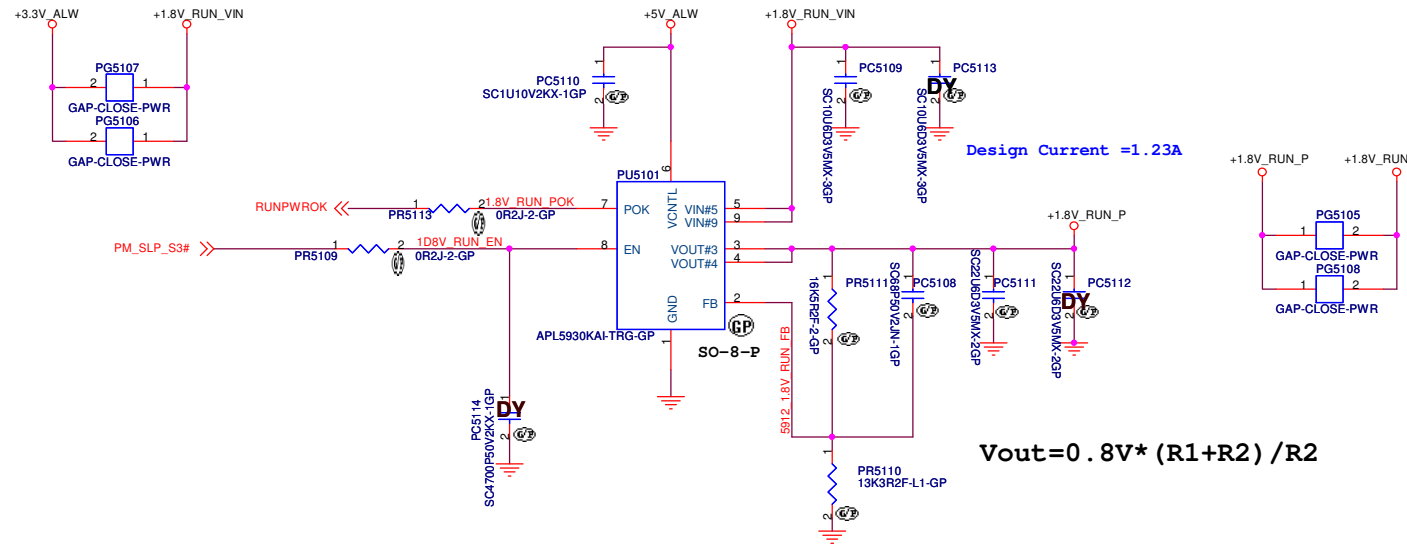


VDDQSET	VDDQ (V)	VTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 220U 2V EEFCK0221ER 15mohm 2.7Arms PANASONIC/ 79.22719.20L
H/S: SI7686DP/ POWERPAK-8/ 11mohm/14mohm@4.5Vgs/ 84.07686.037
L/S: SI7460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037
Switching freq-->400KHz

SSID = PWR.Plane.Regulator_1p8v

APL5930 for +1.8V_RUN



<Core Design>

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<Core Design>



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Title

Reserved

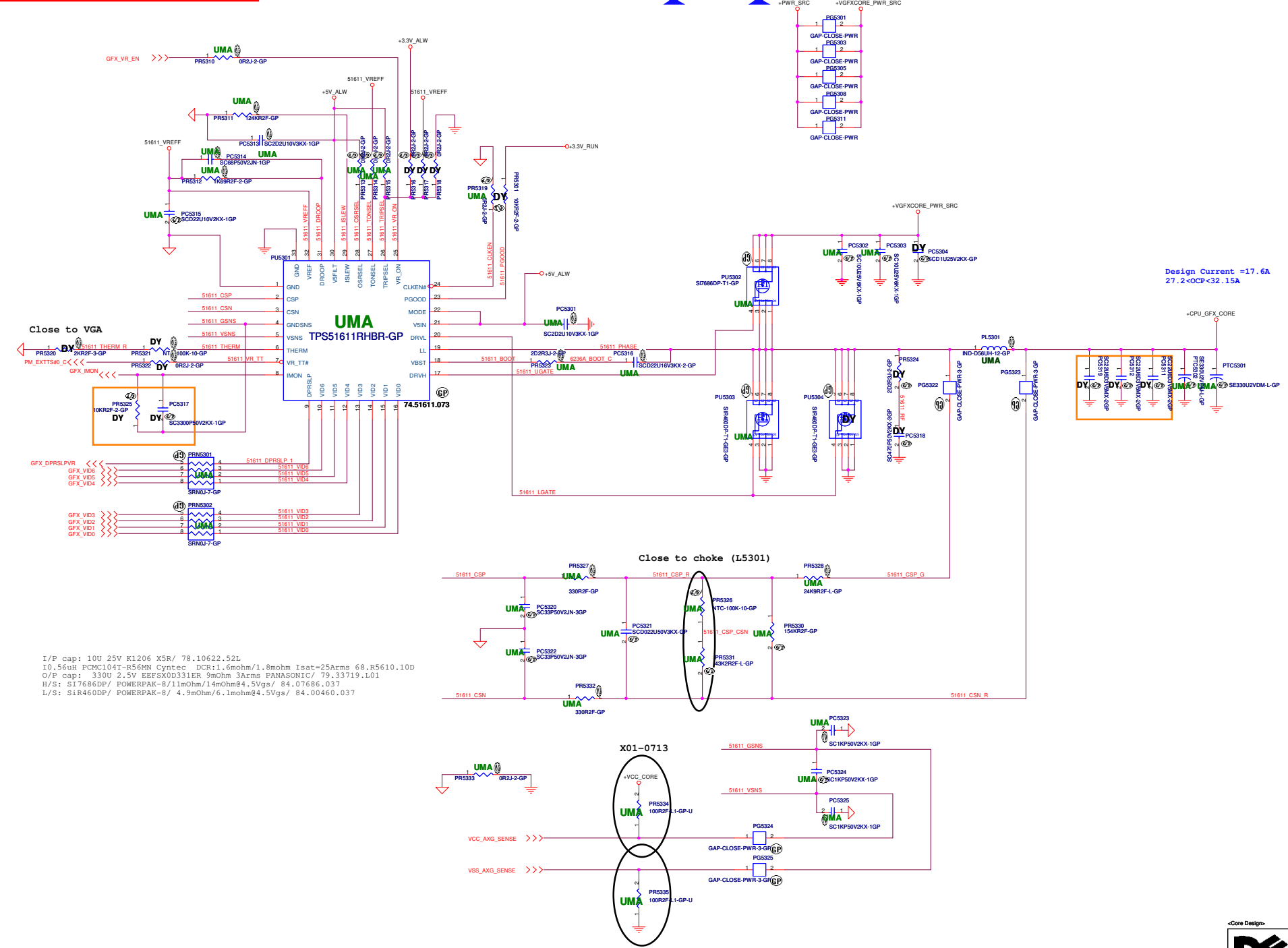
Size
A3

Document Number
Berry

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X00

Date: Wednesday, October 14, 2009

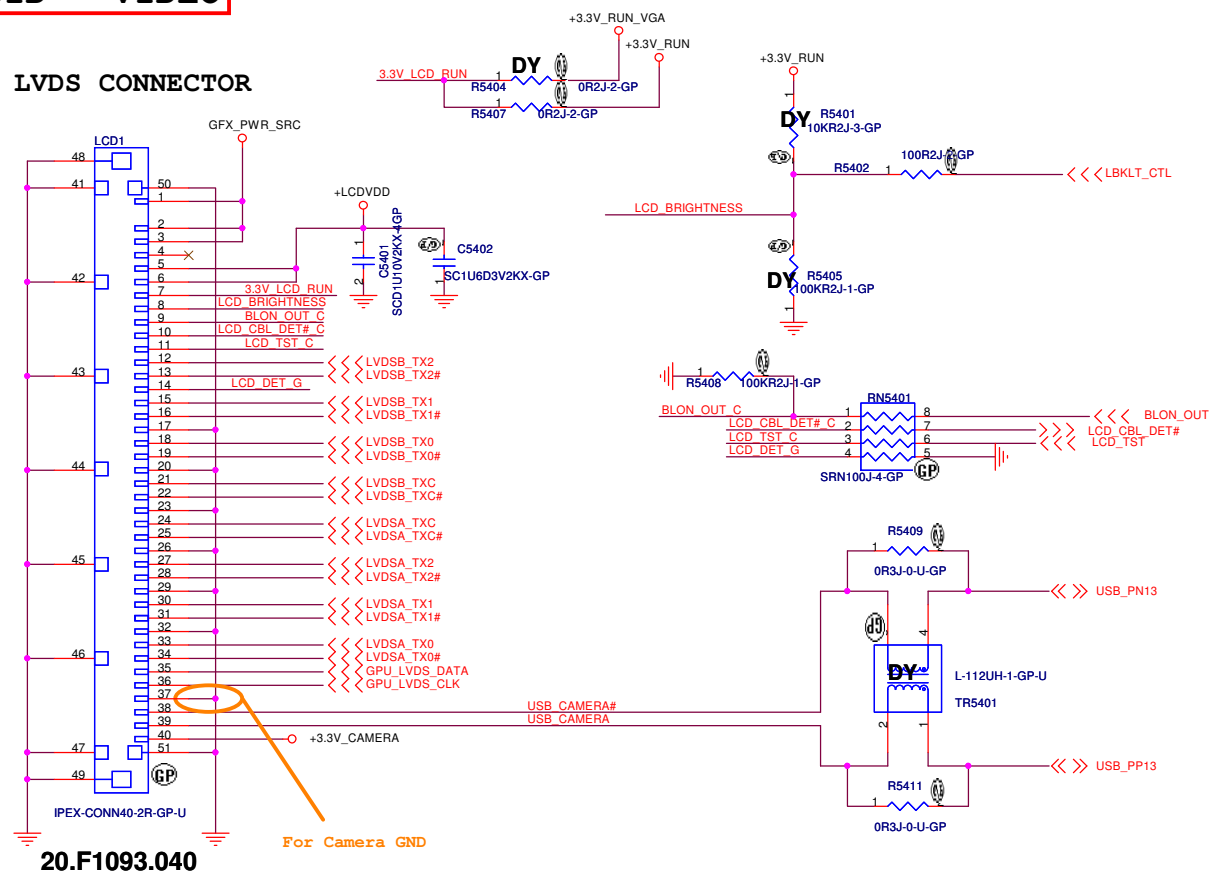
Sheet 52 of 92



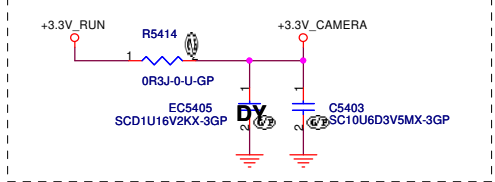
SSID = Inverter

SSID = VIDEO

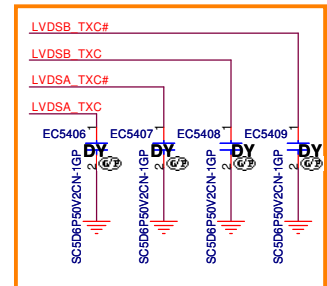
LVDS CONNECTOR



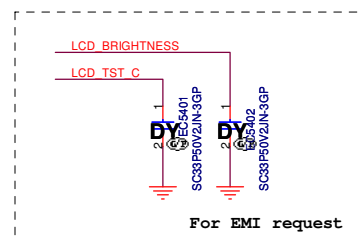
Camera Power



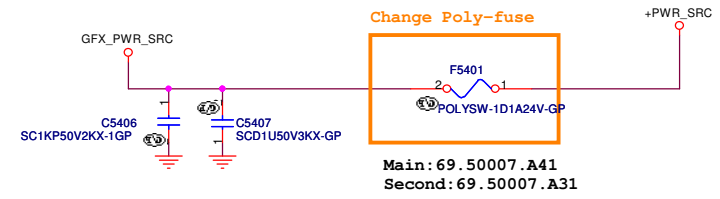
Close to LVDS connector



For EMI request

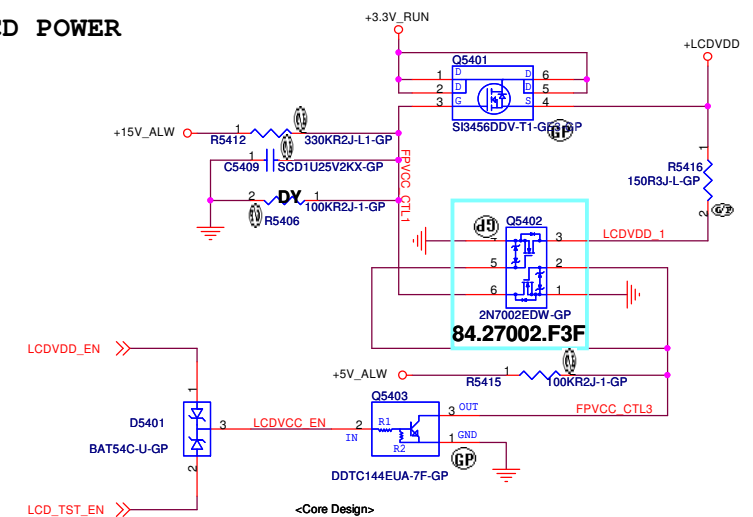


INVERTER POWER



SSID = VIDEO

LCD POWER



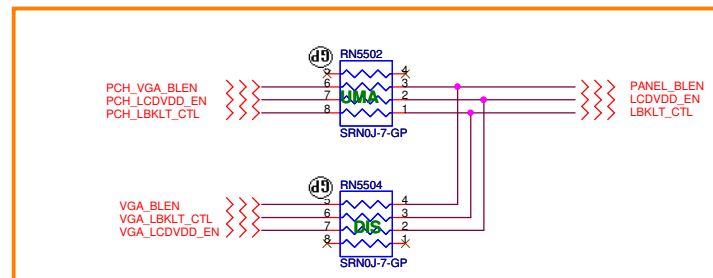
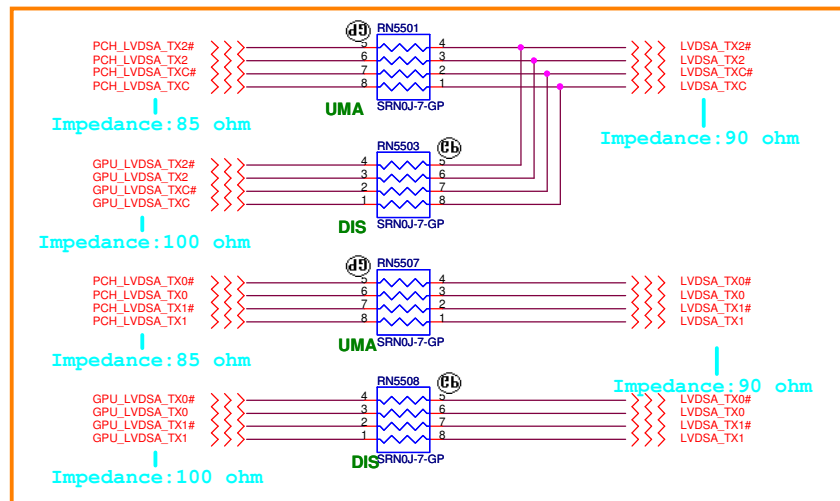
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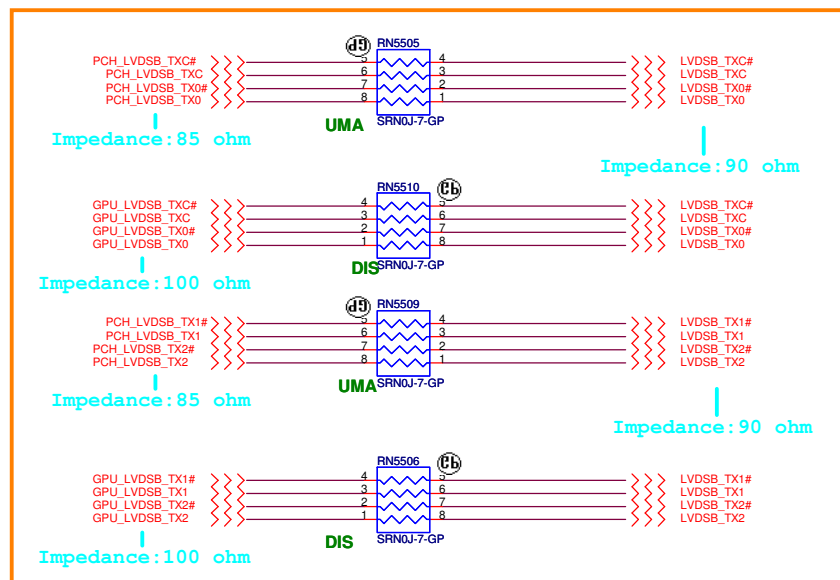
Title LCD/Inverter Connector			Rev X00
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LVDS Channel A

Panel BL brightness/Power En/BL En



LVDS Channel B



<Core Design>

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<Core Design>



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Title

LVDS Switch

Size
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Document Number

Berry

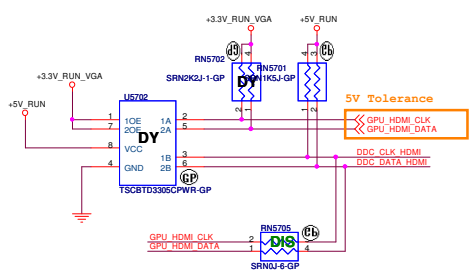
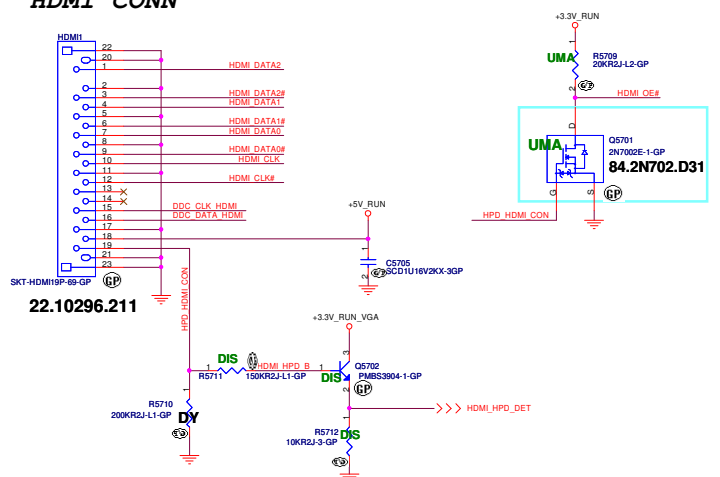
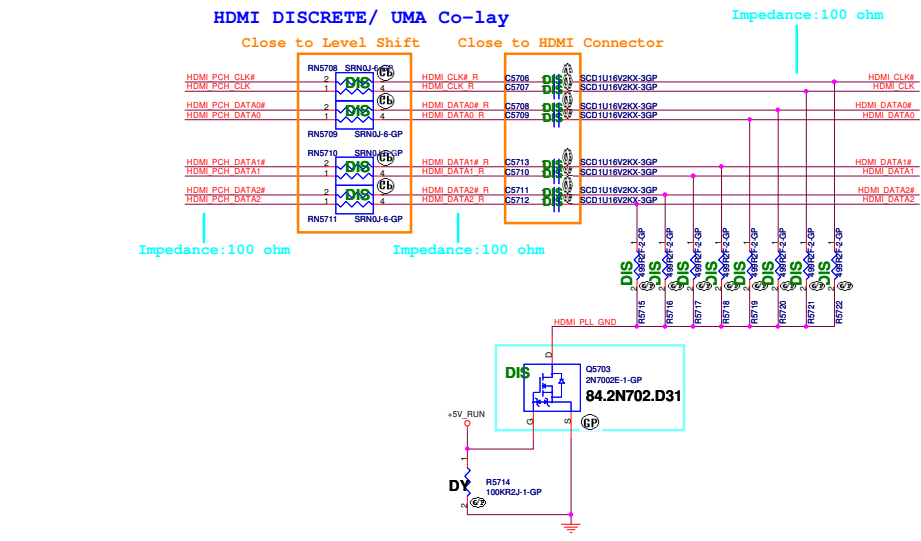
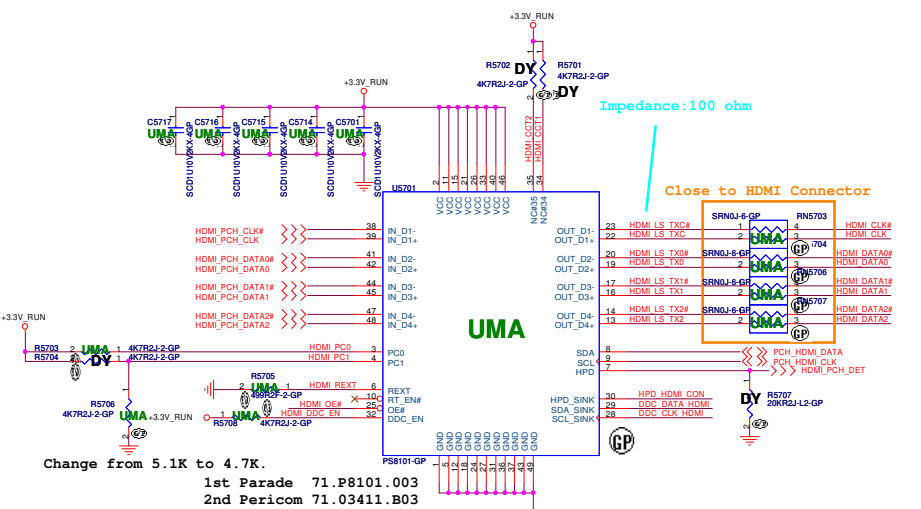
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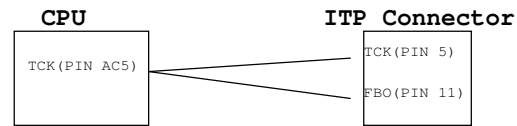
HDMI CONN



SSID = User.Interface

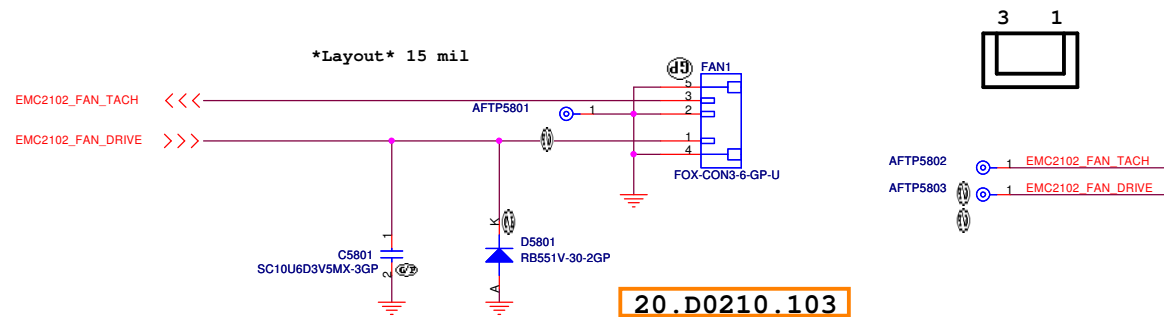
ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



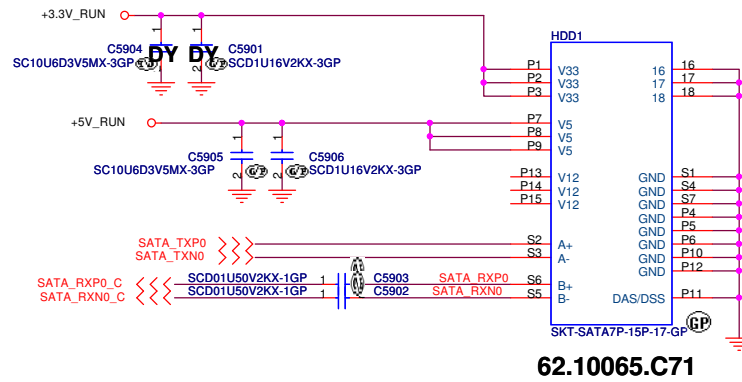
SSID = Thermal

Fan Connector

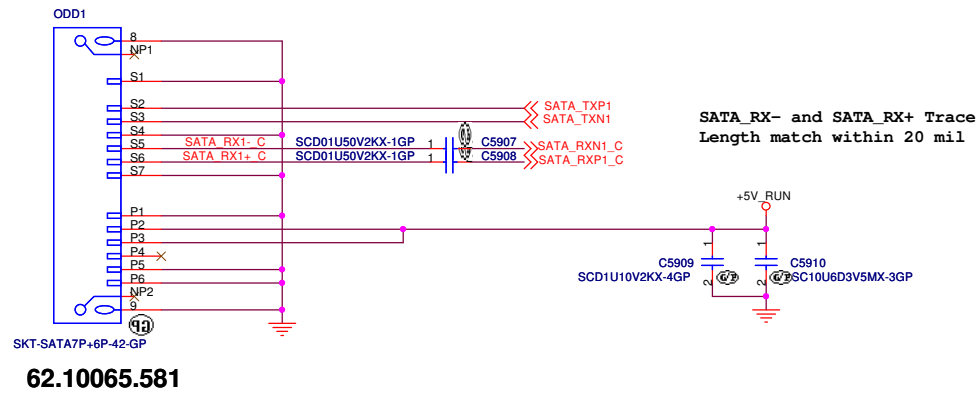


<Core Design>

SATA HDD Connector



ODD Connector



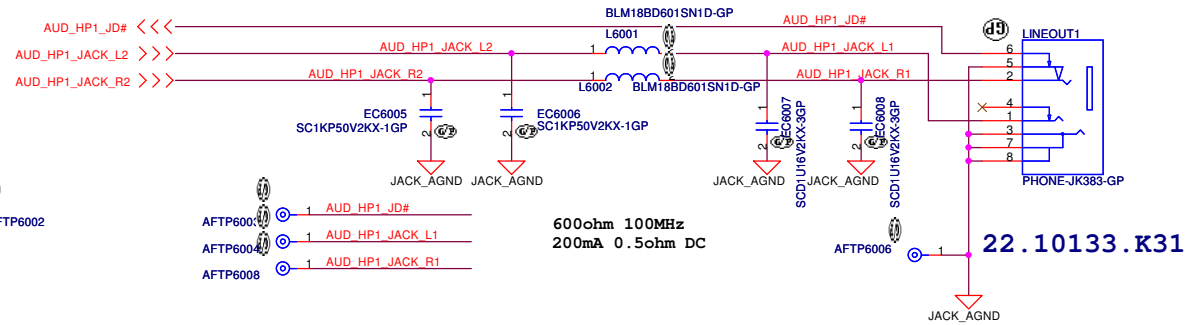
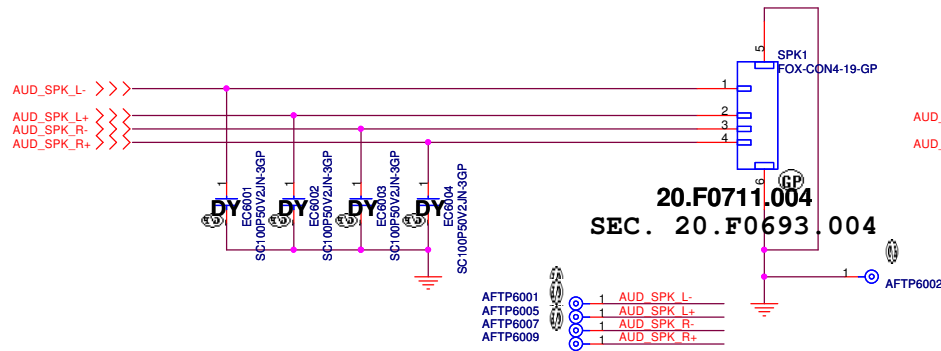
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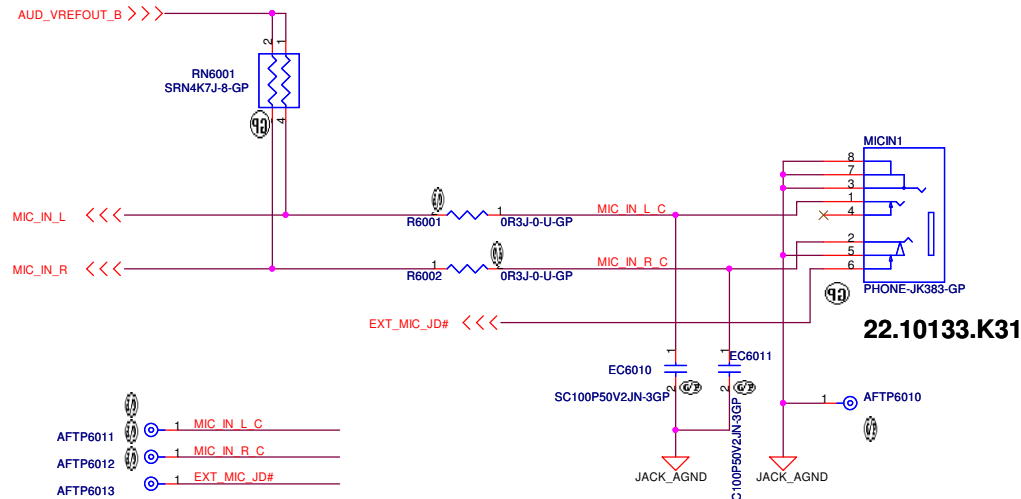
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Taipei Hsien 221, Taiwan, R.O.C.

Title			
HDD/ODD			
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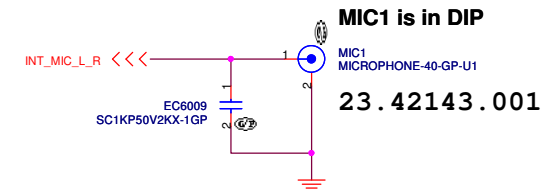
LINE1
OUT



MIC IN



Internal Microphone

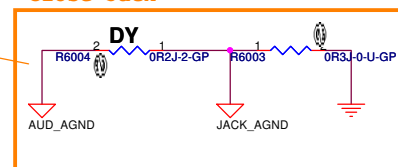


MIC1 is in DIP

23.42143.001

Close Jack

```
width 15mil
```



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<Core Design>



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Title

Reserved

Size
A3

Document Number

Berry

Rev

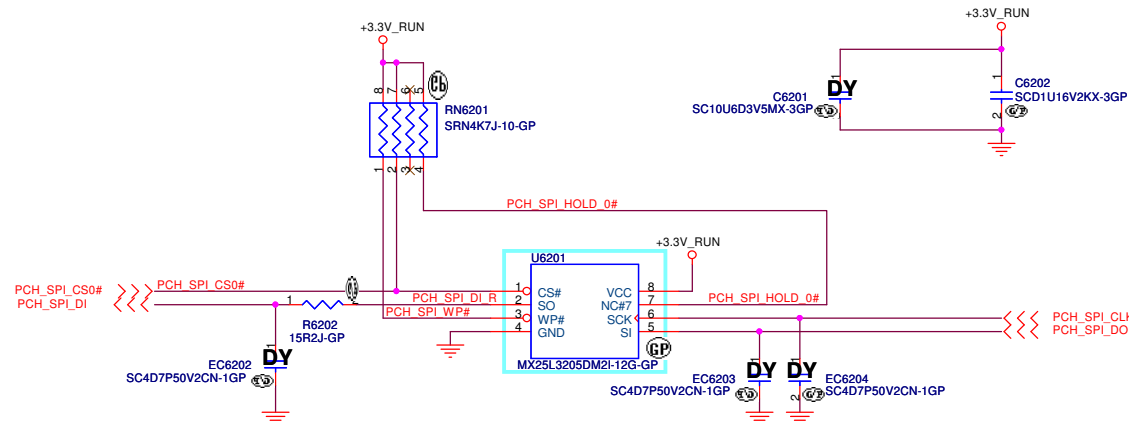
X00

Date: Wednesday, October 14, 2009

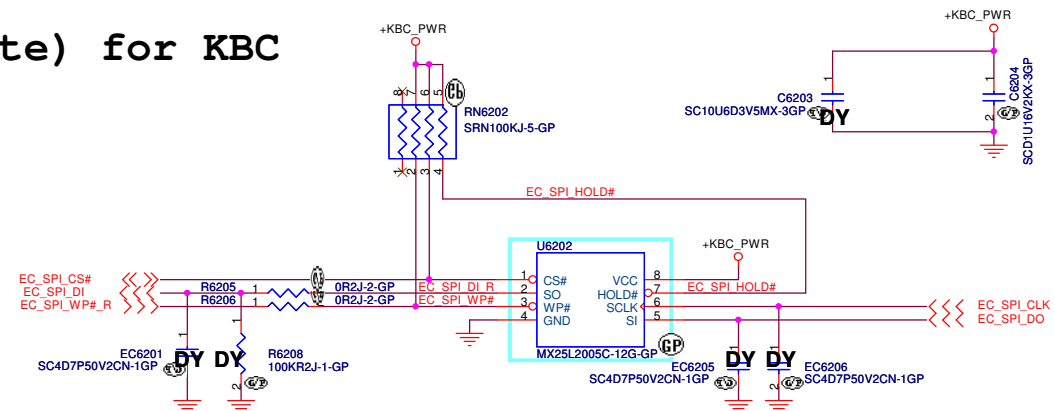
Sheet 61 of 92

SSID = Flash.ROM

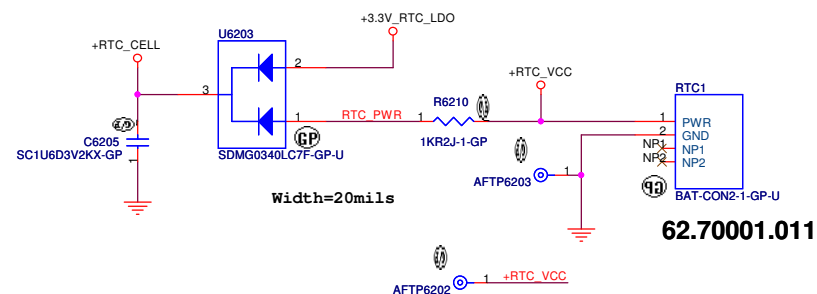
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SPI FLASH ROM (4M byte) for PCH



SPI FLASH ROM (256K byte) for KBC



SSID = RBATT



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Title	Author	Date	Page	Page	Page	Page	Page	Page	Page

Flash/RTC

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A3

Document Number	Boon
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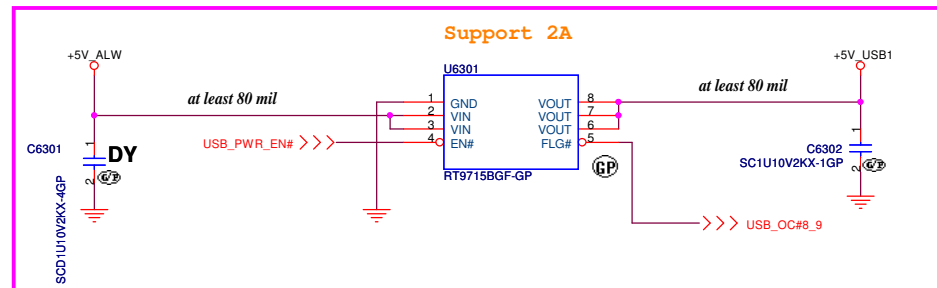
Rev	
X00	

SSID = USB

Close to I/O connector

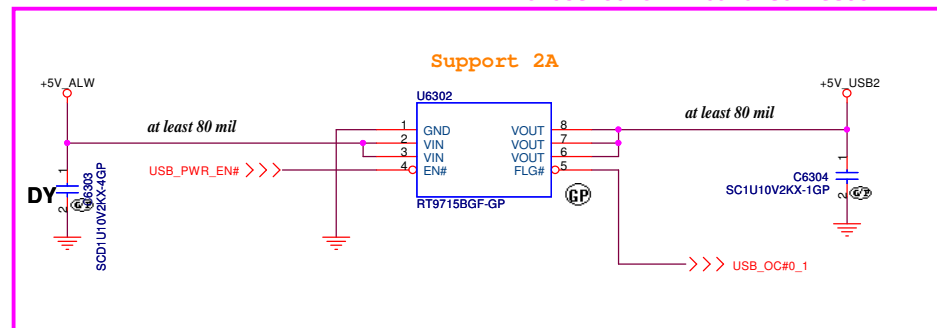
IO Board USB Power

Main RT9715BGF P/N:74.09715.B79
SEC G547F2P81U P/N: 74.00547.A79



CRT Board USB Power

Close to CRT Board connector



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<Core Design>



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Title

Reserved

Size
A4

Document Number
Berry


Rev
X00

Date: Wednesday, October 14, 2009

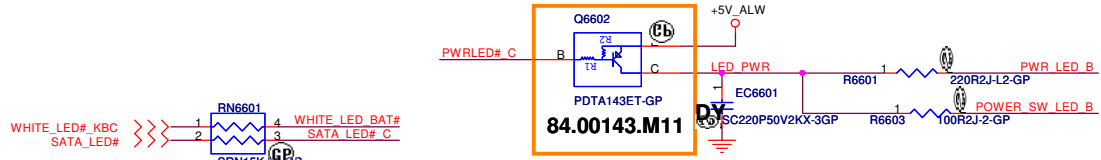
Sheet 64 of 92

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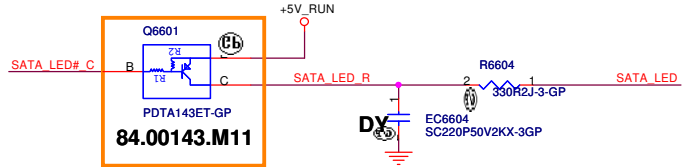
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		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
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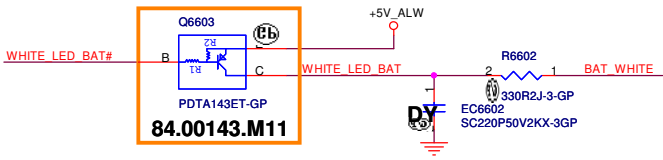
Power LED (White)



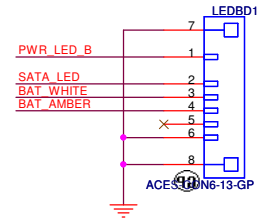
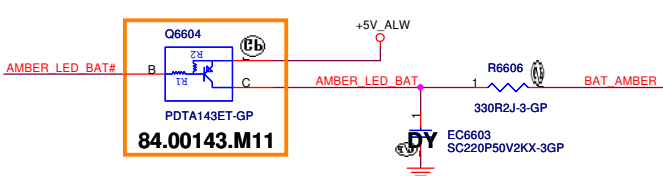
SATA HDD LED (White)



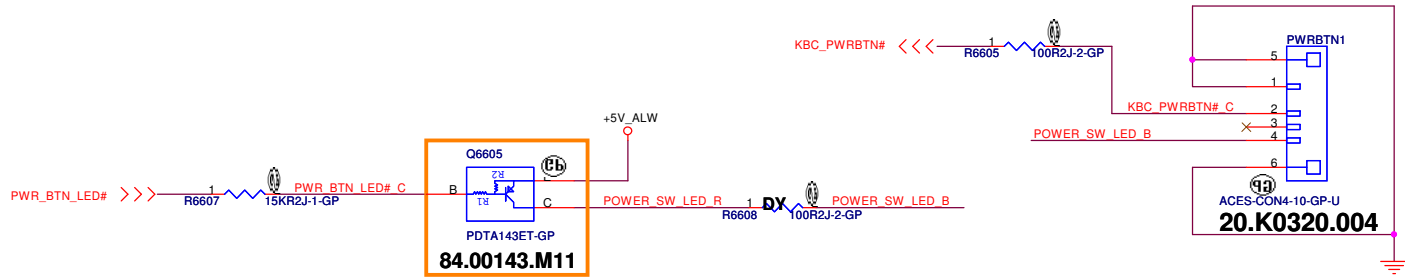
Battery LED1 (White)



Battery LED2 (Amber)



Power button LED (White)



(Blanking)

<Core Design>



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A3

Document Number

Berry

Rev

X00

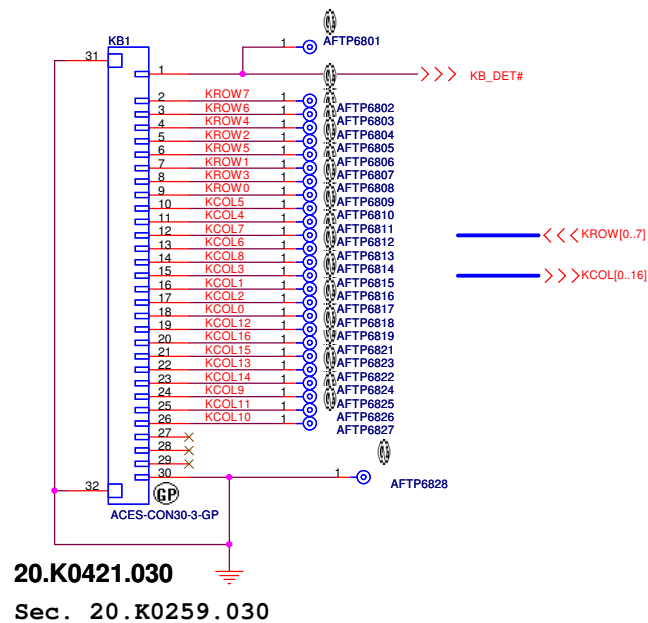
Date: Wednesday, October 14, 2009

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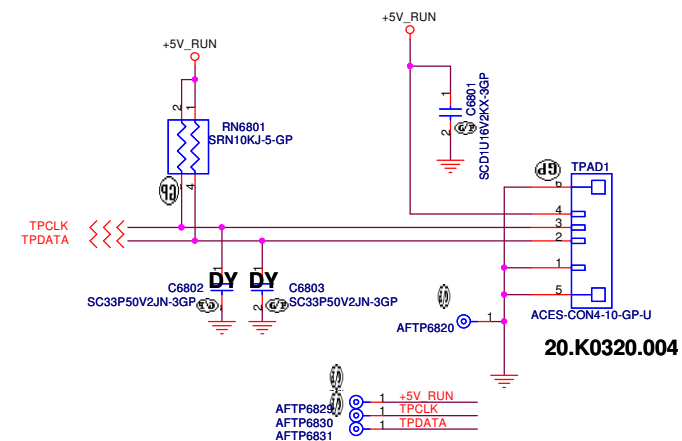
SSID = KBC

SSID = Touch.Pad

Internal KeyBoard Connector



TouchPad Connector

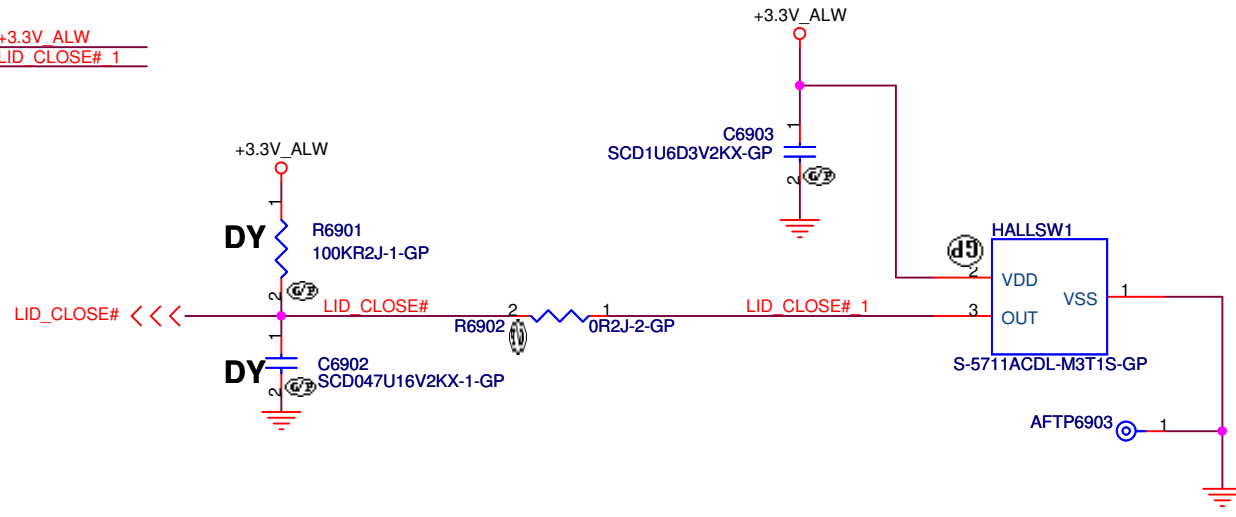


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Taipei Hsien 221, Taiwan, R.O.C.

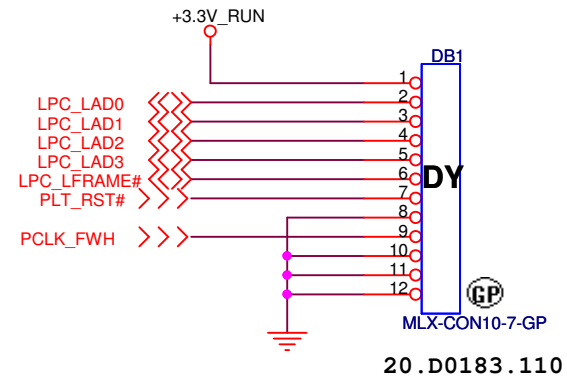
Title			Key Board/Touch Pad	
Size	Document Number	Rev		
A3	Berry	X00		
Date:	Thursday, October 22, 2009	Sheet	68	of 92

AFTP6901 1 +3.3V_ALW
AFTP6902 1 LID_CLOSE# 1



<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title Hall Sensor	
Size A4	Document Number Berry		Rev X00
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<Core Design>



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Title

Dubug connector

Size
A4

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<Core Design>



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<Core Design>



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Title

RESERVED

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Document Number

Berry

Rev

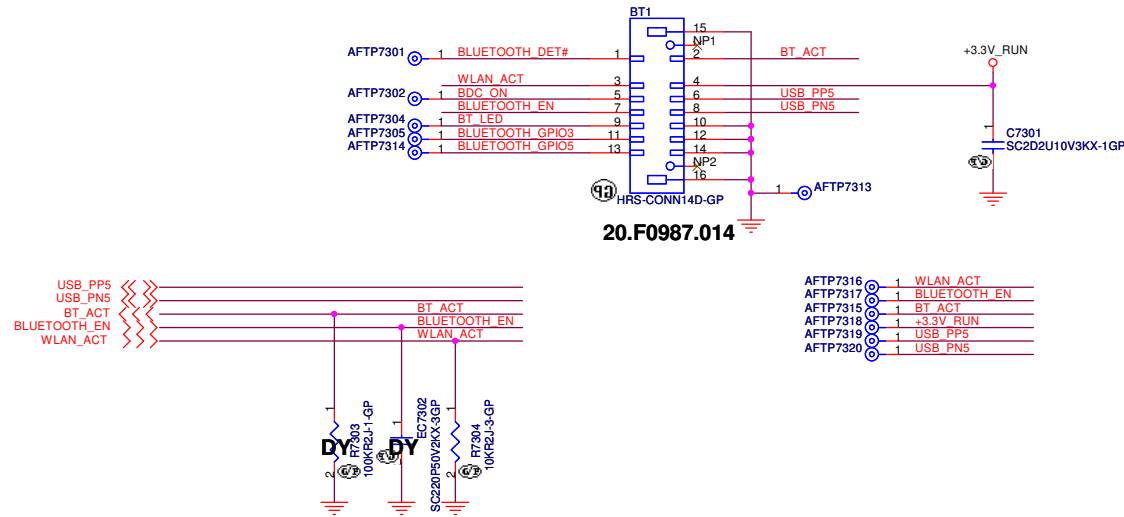
X00

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SSID = User.Interface

Bluetooth Module conn.



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<Core Design>



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Title

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Size
A4

Document Number

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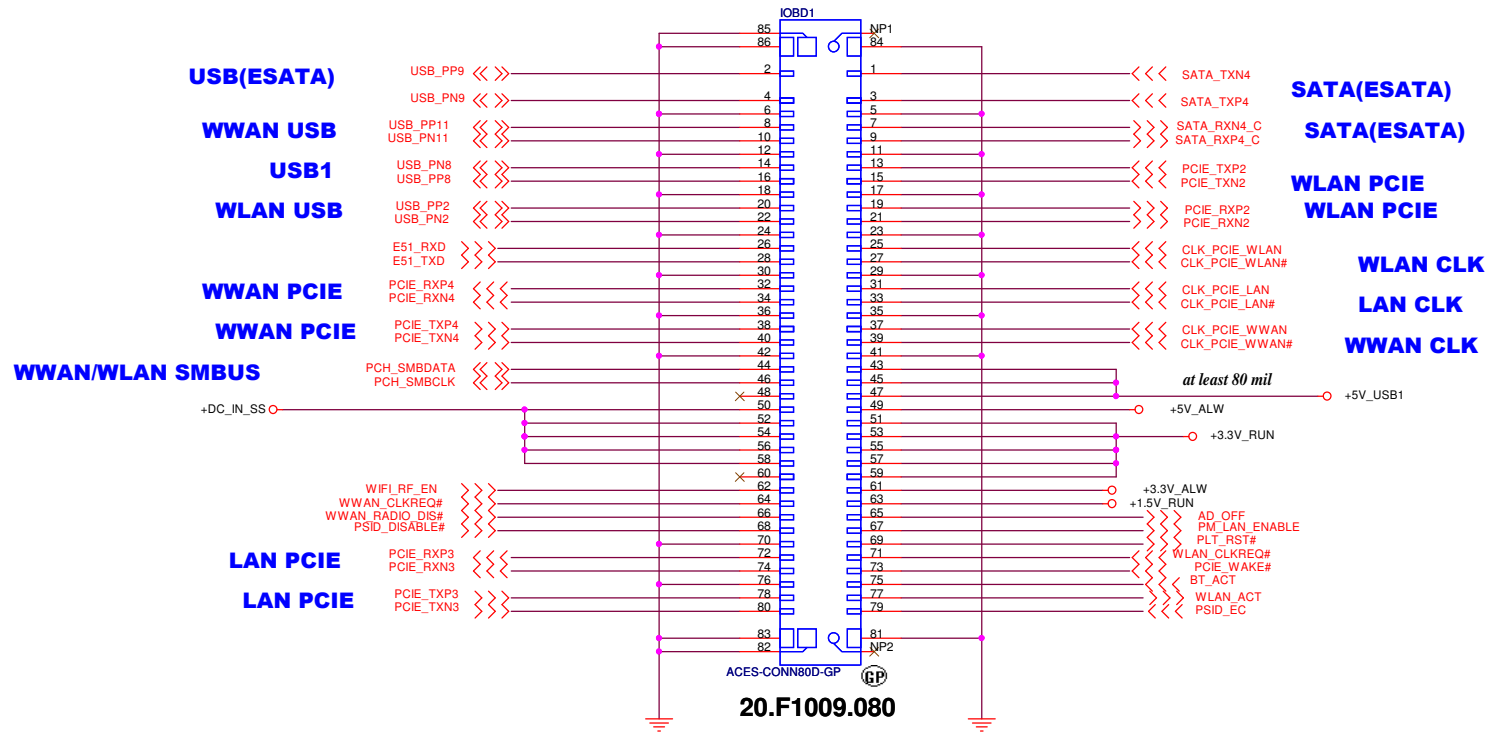
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X00

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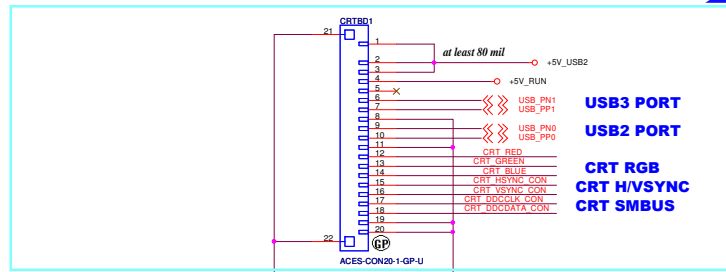
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IO Board CONN 80 pin



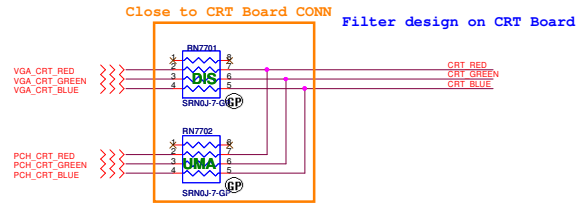
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CRT Board Connector

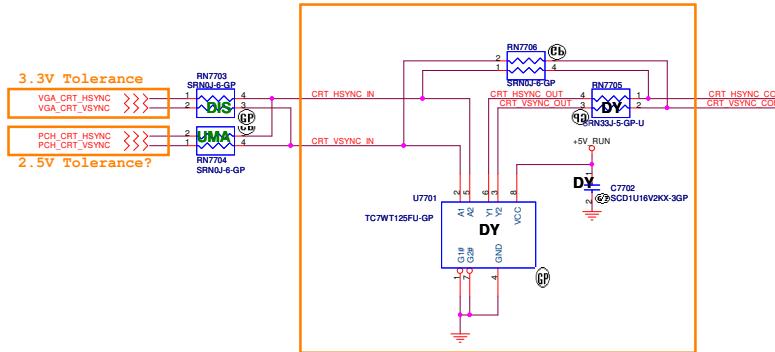


20.F0772.020
SEC. 20.F1035.020

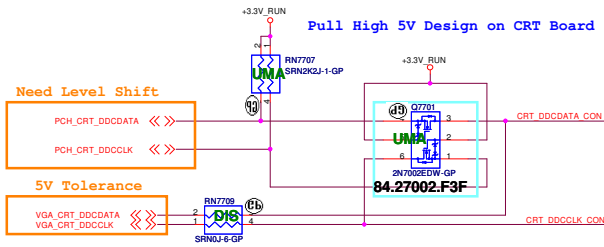
CRT RGB



CRT Hsync & Vsync level shift



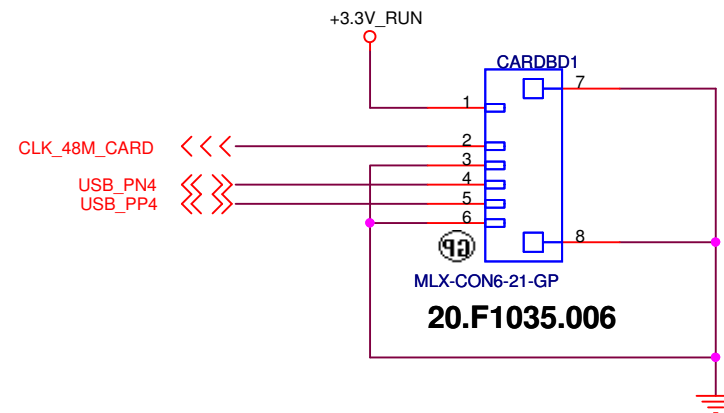
CRT DDCDATA & DDCCLK level shift



<Core Design>

SSID = SDIO

Card Reader connector



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Title

CARD Reader CONN

Size
A4

Document Number

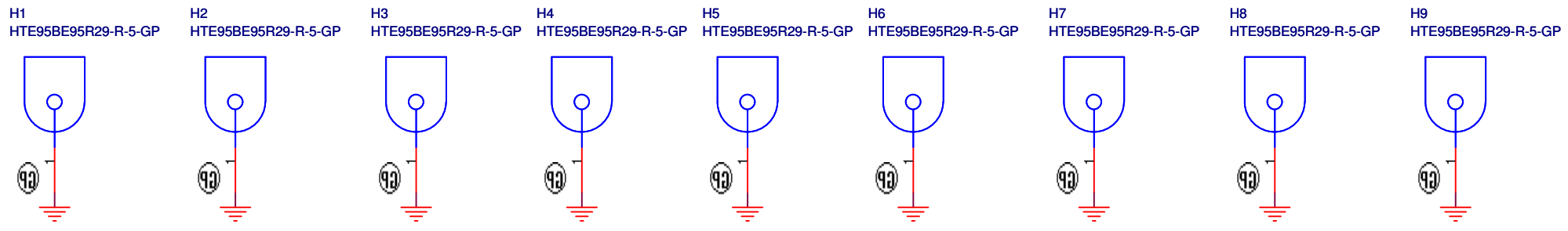
Berry

Rev

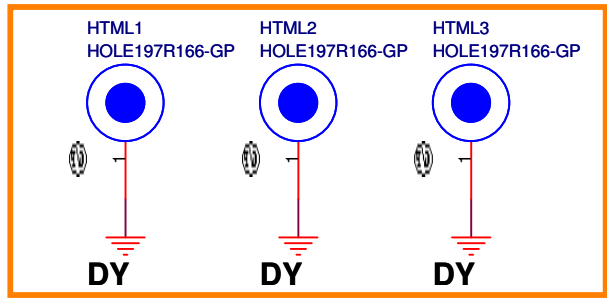
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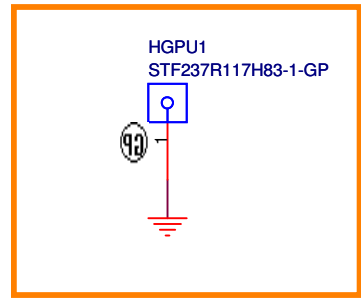
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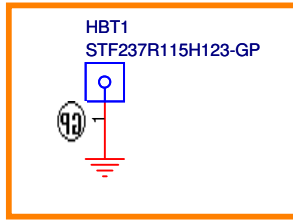
CPU Thermal module hole



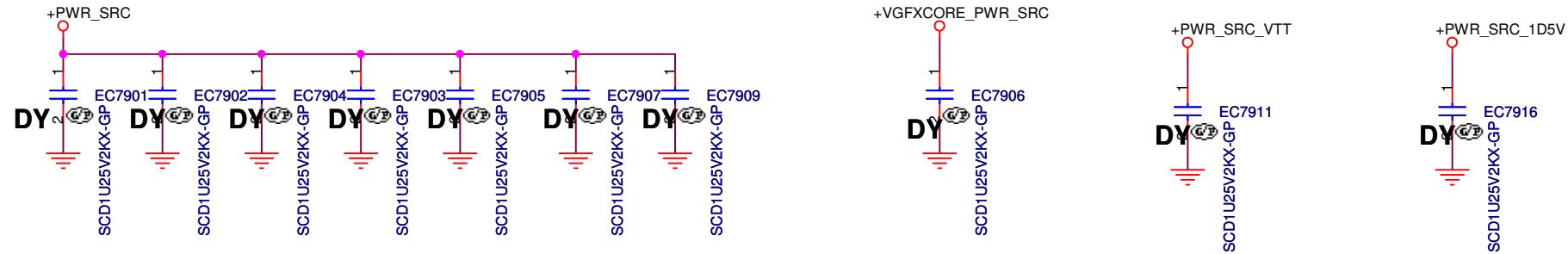
GPU Thermal module hole



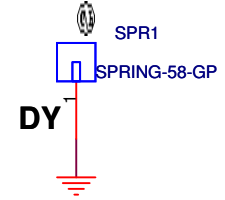
stand off



EMI Reserve





EMI Reserve



<Core Design>

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Title UNUSED PARTS/EMI Capacitors			
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PEG_TXP[0..15] >> 
PEG_TXN[0..15] >> 

VGA1A

1 OF 8

PEG_RXP[0..15] >> 
PEG_RXN[0..15] >> PEG_TXP0 AA38
PEG_TXN0 Y37PCIE_RX0P
PCIE_RX0NY33 PEG C RXP0 C8001 DIS SCD1U16V2KX-3GP PEG_RXP0
Y32 PEG C RXN0 C8002 DIS SCD1U16V2KX-3GP PEG_RXN0PEG_TXP1 Y35
PEG_TXN1 W36PCIE_RX1P
PCIE_RX1NW33 PEG C RXP1 C8003 DIS SCD1U16V2KX-3GP PEG_RXP1
W32 PEG C RXN1 C8004 DIS SCD1U16V2KX-3GP PEG_RXN1PEG_TXP2 W38
PEG_TXN2 V37PCIE_RX2P
PCIE_RX2NU33 PEG C RXP2 C8005 DIS SCD1U16V2KX-3GP PEG_RXP2
U32 PEG C RXN2 C8006 DIS SCD1U16V2KX-3GP PEG_RXN2PEG_TXP3 V35
PEG_TXN3 U36PCIE_RX3P
PCIE_RX3NU30 PEG C RXP3 C8008 DIS SCD1U16V2KX-3GP PEG_RXP3
U29 PEG C RXN3 C8007 DIS SCD1U16V2KX-3GP PEG_RXN3PEG_TXP4 U38
PEG_TXN4 T37PCIE_RX4P
PCIE_RX4NT33 PEG C RXP4 C8009 DIS SCD1U16V2KX-3GP PEG_RXP4
T32 PEG C RXN4 C8010 DIS SCD1U16V2KX-3GP PEG_RXN4PEG_TXP5 T35
PEG_TXN5 R36PCIE_RX5P
PCIE_RX5NT30 PEG C RXP5 C8011 DIS SCD1U16V2KX-3GP PEG_RXP5
T29 PEG C RXN5 C8012 DIS SCD1U16V2KX-3GP PEG_RXN5PEG_TXP6 R38
PEG_TXN6 P37PCIE_RX6P
PCIE_RX6NP33 PEG C RXP6 C8013 DIS SCD1U16V2KX-3GP PEG_RXP6
P32 PEG C RXN6 C8014 DIS SCD1U16V2KX-3GP PEG_RXN6PEG_TXP7 P35
PEG_TXN7 N36PCIE_RX7P
PCIE_RX7NP30 PEG C RXP7 C8016 DIS SCD1U16V2KX-3GP PEG_RXP7
P29 PEG C RXN7 C8015 DIS SCD1U16V2KX-3GP PEG_RXN7PEG_TXP8 N38
PEG_TXN8 M37PCIE_RX8P
PCIE_RX8NN33 PEG C RXP8 C8018 DIS SCD1U16V2KX-3GP PEG_RXP8
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PEG_TXN9 L36PCIE_RX9P
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PCIE_RX10NL33 PEG C RXP10 C8021 DIS SCD1U16V2KX-3GP PEG_RXP10
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H32 PEG C RXN15 C8031 DIS SCD1U16V2KX-3GP PEG_RXN15

PCI EXPRESS INTERFACE

DIS

CLK_PCIE_VGA >> AB35
CLK_PCIE_VGA# >> AA36

CLOCK



PCIE_REFCLKP
PCIE_REFCLKN

CALIBRATION

PCIE_CALRP
PCIE_CALRN

PERST#

MADISON-PRO-2-GP

PLT_RST# >> 
R8018 1 2 PWRGOOD 10KR2F-2-GP
R8020 1 2 VGA_RST# AA30C
R8021 1 2 PLTRST_DELAY# >> 
R8021 1 2 0R2J-2-GPY30 PCIE_CALRP 1 DIS 1K27R2F-2-GP +1.0V_RUN_VGA
Y29 PCIE_CALRN 1 DIS 2KR2F-3-GP

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED,
THEY MUST NOT CONFLICT DURING RESETRECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMEND	PLATFORM SETTING
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X	1
TX_DEEMPH_EN	GPIO1	PCIe TRANSMITTER DE-EMPHASIS ENABLED 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	X	1
BIF_GEN2_EN_A	GPIO2	0:Advertises the PCIe device as 2.5GT/s capable at power on. 1:Advertises the PCIe device as 5.0GT/s capable at power on.	0	0
GPIO5_AC_BATT	GPIO5	optional input allow the system to request a fast power reduction by setting GPIO5 to low.	?	0
RESERVED	GPIO8	RESERVED	0	0
VGA_DIS	GPIO9	0:VGA Controller capacity enabled 1:The device won't be recognized as the system's VGA controller	0	0
ROMIDCFG[2:0]	GPIO[13:11]	BIOS_ROM_EN=1, Config[2:0] defines the ROM type BIOS_ROM_EN=0, Config[2:0] defines the primary memory aperture size	X X X	0 0 1 (256MB)
RESERVED	GPIO21	RESERVED	0	0
BIOS_ROM_EN	GPIO_22_ROMCSB	0:Disable external BIOS ROM device 1:Enable external BIOS ROM device	X	0
VIP_DEVICE_STRAP_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver that it sense whether or not a VIP device is connected on the VIP Host interface.	X	0
RSVD	H2SYNC	RESERVED	0	0
RSVD	GENERICC	RESERVED	0	0
AUD[1]	HSYNC	AUD[1:0]:11-Audio for both DisplayPort and HDMI	X	1
AUD[0]	VSXNC		X	1

PIN STRAPS

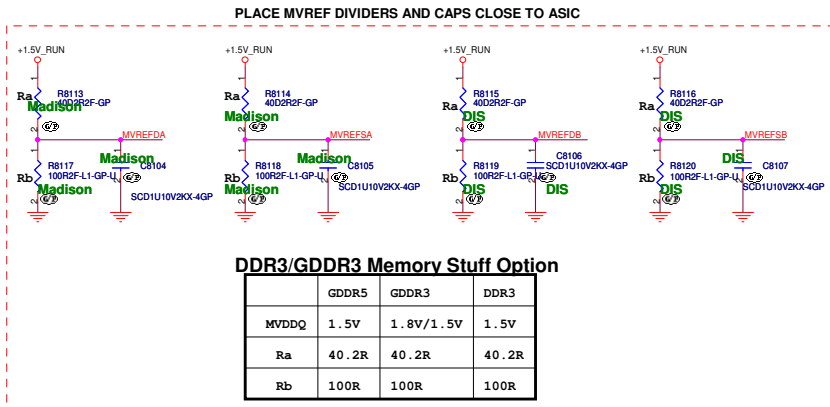
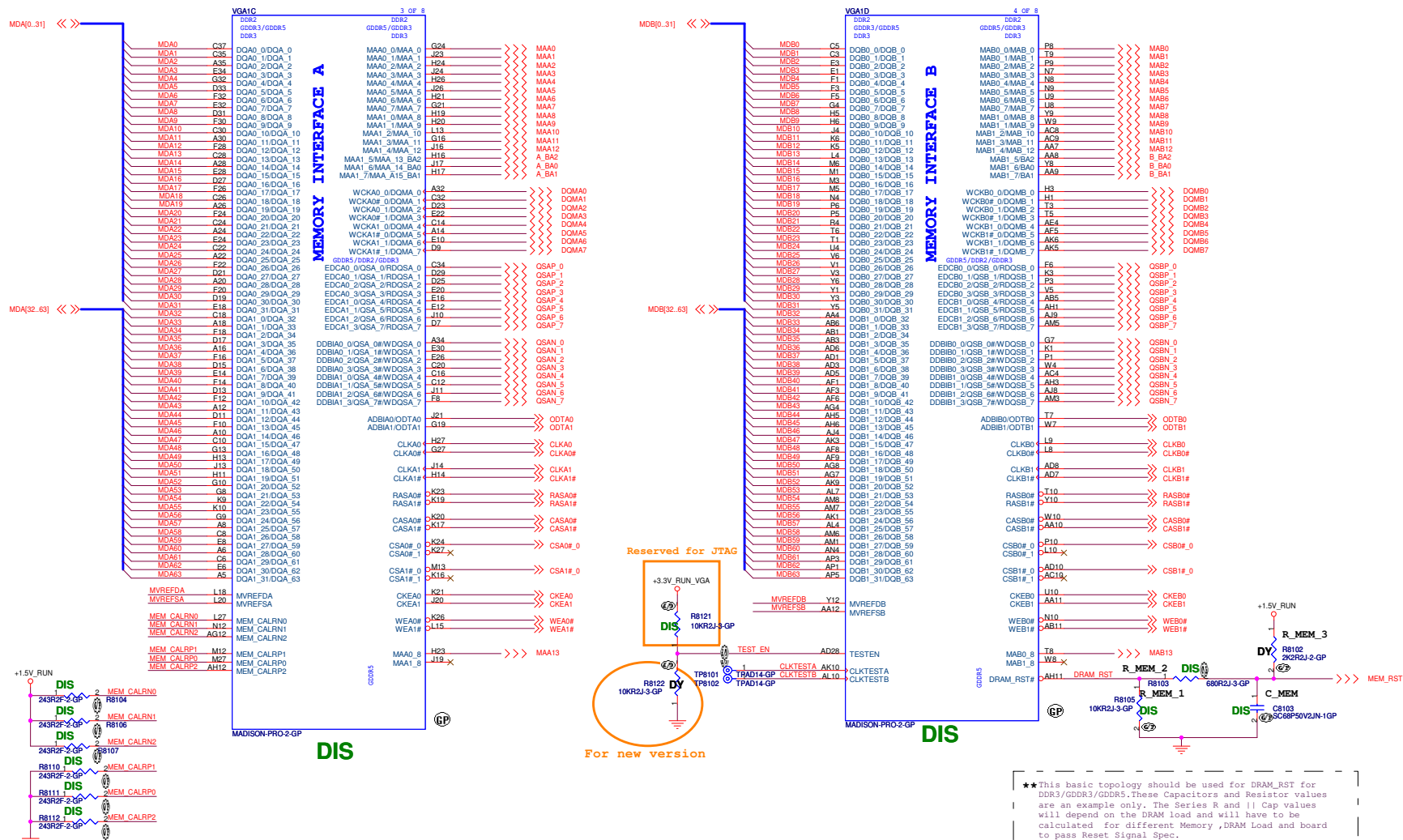
+3.3V_RUN_VGA

TX_PWRS_ENB <<	R8001	1	DY	3KR2J-2-GP
TX_DEEMPH_EN <<	R8002	1	DY	3KR2J-2-GP
BIF_GEN2_EN_A <<	R8003	1	DY	10KR2J-3-GP
GPIO8_ROMSO <<	R8004	1	DY	10KR2J-3-GP
VGA_DIS <<	R8005	1	DY	10KR2J-3-GP
CONFIG0 <<	R8006	1	DIS	10KR2J-3-GP
CONFIG1 <<	R8007	1	DY	10KR2J-3-GP
CONFIG2 <<	R8008	1	DY	10KR2J-3-GP
VGA_CRT_VSYNC >>	R8009	1	DIS	10KR2J-3-GP
VGA_CRT_HSYNC >>	R8010	1	DIS	10KR2J-3-GP
VSXNC_DAC2 >>	R8012	1	DY	10KR2J-3-GP
HSXNC_DAC2 >>	R8013	1	DY	10KR2J-3-GP
BIOS_ROM_EN <<	R8014	1	DY	10KR2J-3-GP
GPIO5_AC_BATT <<	R8015	1	DY	10KR2J-3-GP
GPIO21_BB_EN <<	R8016	1	DY	10KR2J-3-GP

<Core Design>

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Title		GPU PCIE/STRAPPING(1/5)	
Size	Document Number	Rev	
A3	Berry	X00	
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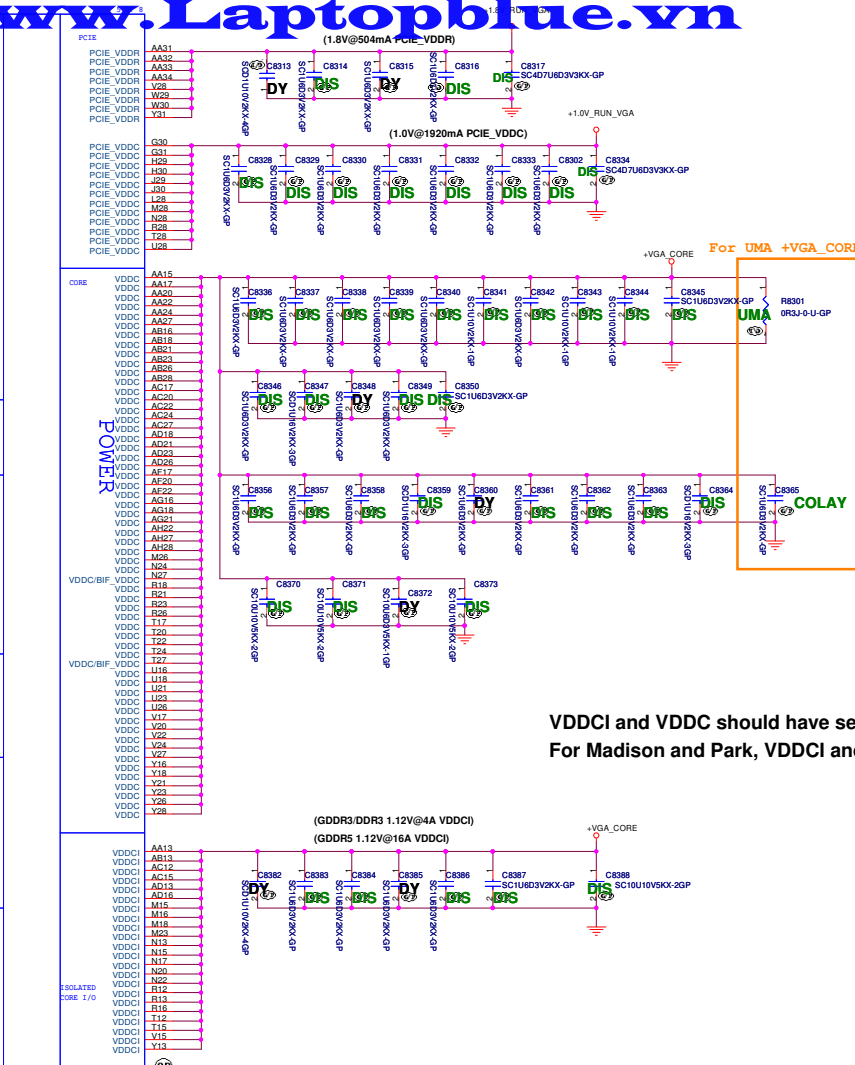
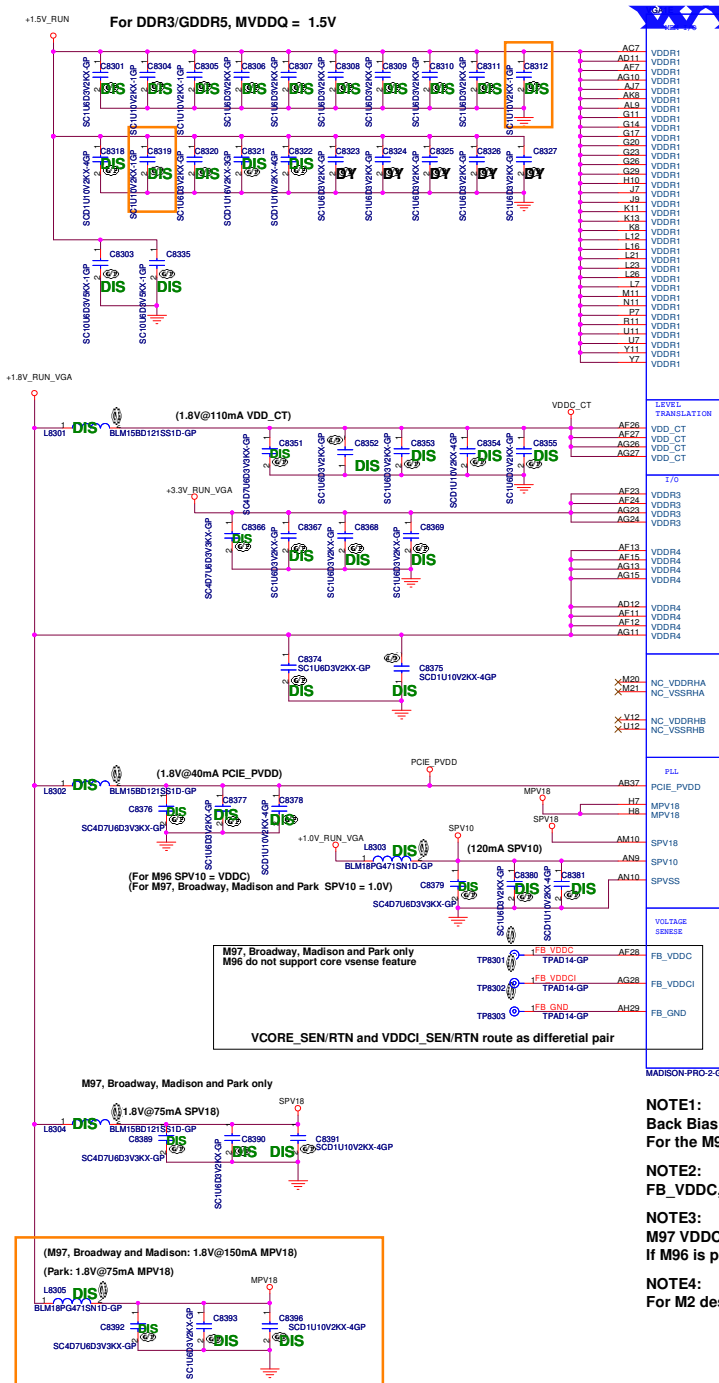


Designator	For M97-M2	For Mannheim
R_MEM_1	10K	10K
R_MEM_2	0R/Short	680R
R_MEM_3	DNI	DNI
C_MEM	2.2nF	68pF

<Core Design>

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Taippei Hsien 221, Taiwan, R.O.C.

File **GPU Memory(2/5)**
Size **C** Document Number **Berry** Rev **X00**
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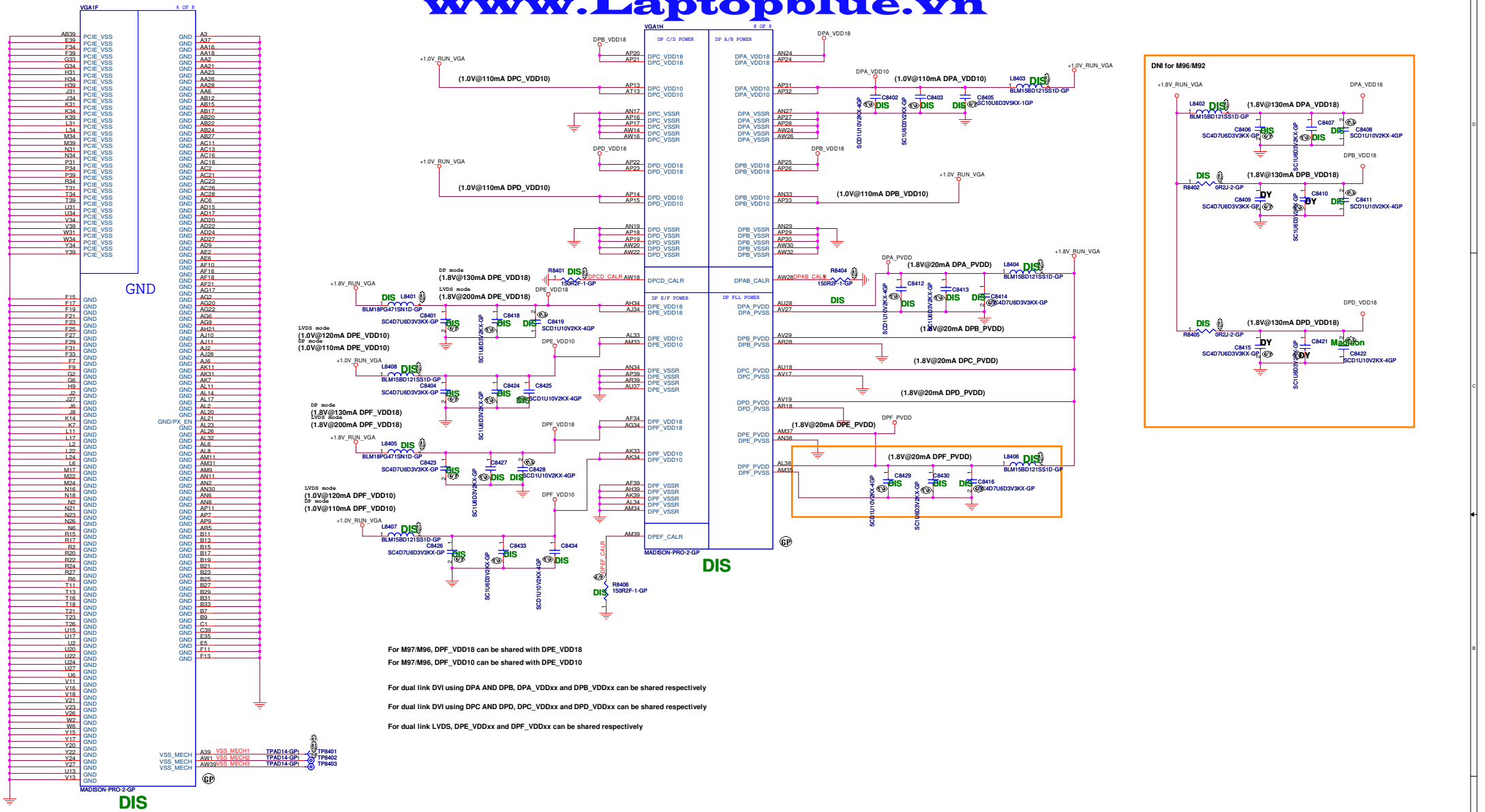


NOTE1:
Back Bias is not supported on M97, Broadway, Madison and Park
For the M96 Back Bias circuitry, refer to REF134

NOTE2:
FB_VDDC, FB_VDDCI and FB_GND are not support on M96

NOTE3:
M97 VDDC and VDDCI ball assignments are different from M96.
If M96 is populated on this design, VDDC and VDDCI will be shorted on the substrate.

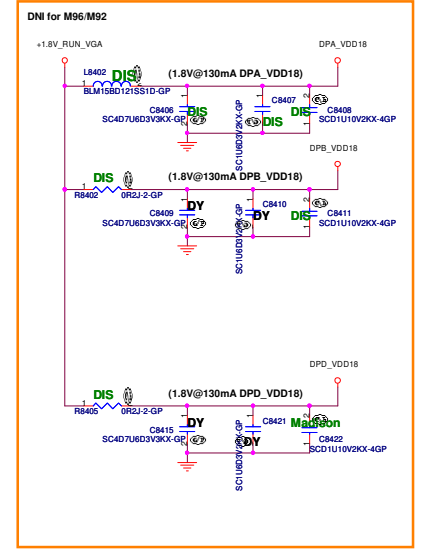
NOTE4:
For M2 design compatibility, refer to the document AN_M96_Ax and AN_M97_Ax

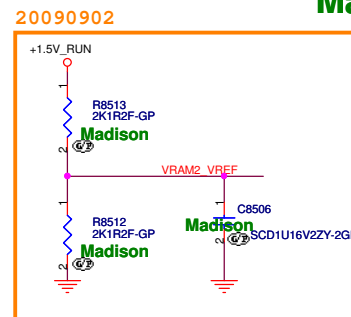
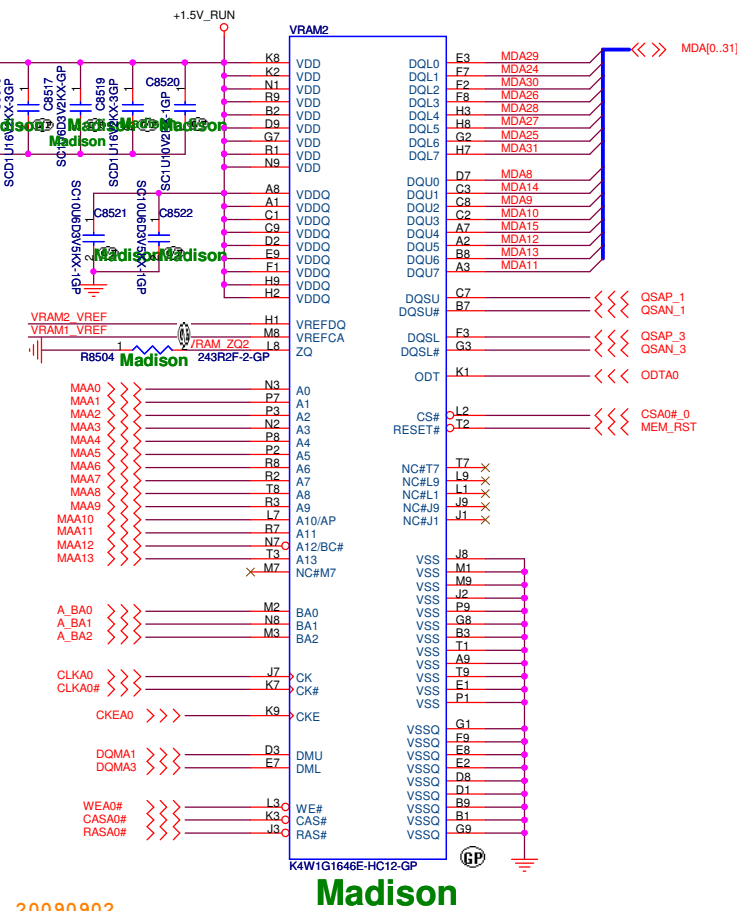


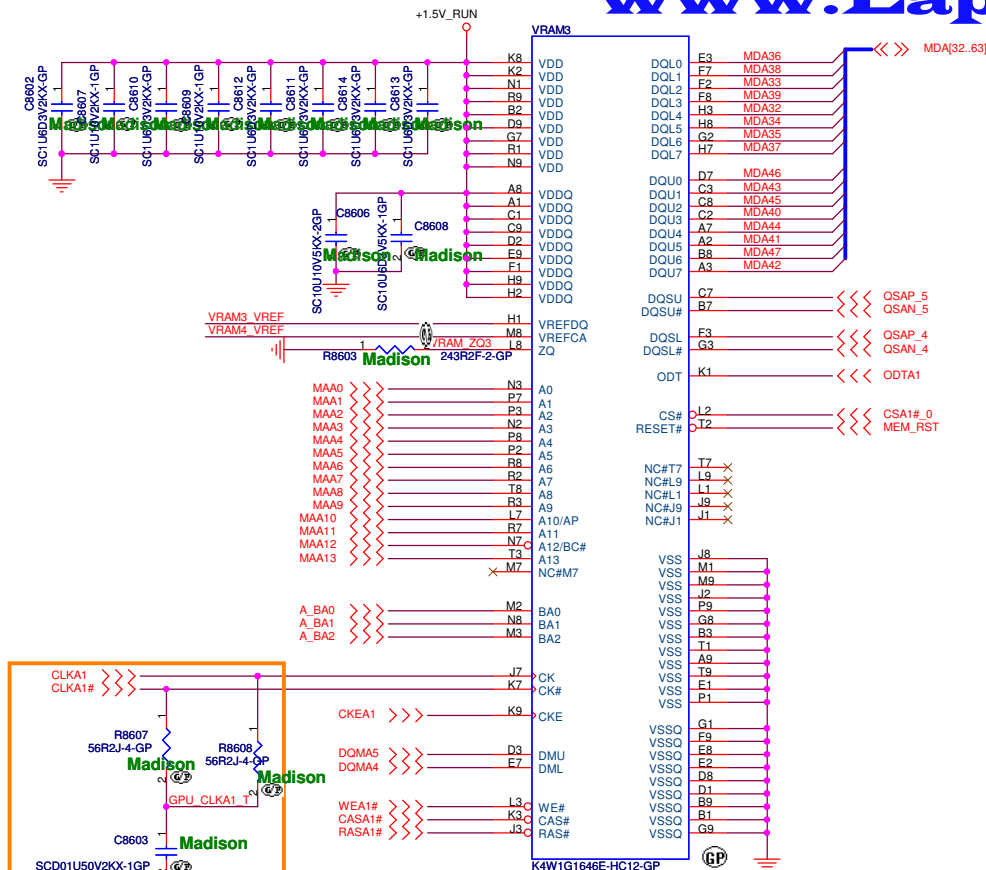
For M97/M96, DPF_VDD18 can be shared with DPE_VDD18
 For M97/M96, DPF_VDD10 can be shared with DPE_VDD10

For dual link DVI using DPA and DPB, DPA_VDDxx and DPB_VDDxx can be shared respectively
 For dual link DVI using DPC and DPD, DPC_VDDxx and DPD_VDDxx can be shared respectively

For dual link LVDS, DPE_VDDxx and DPF_VDDxx can be shared respectively



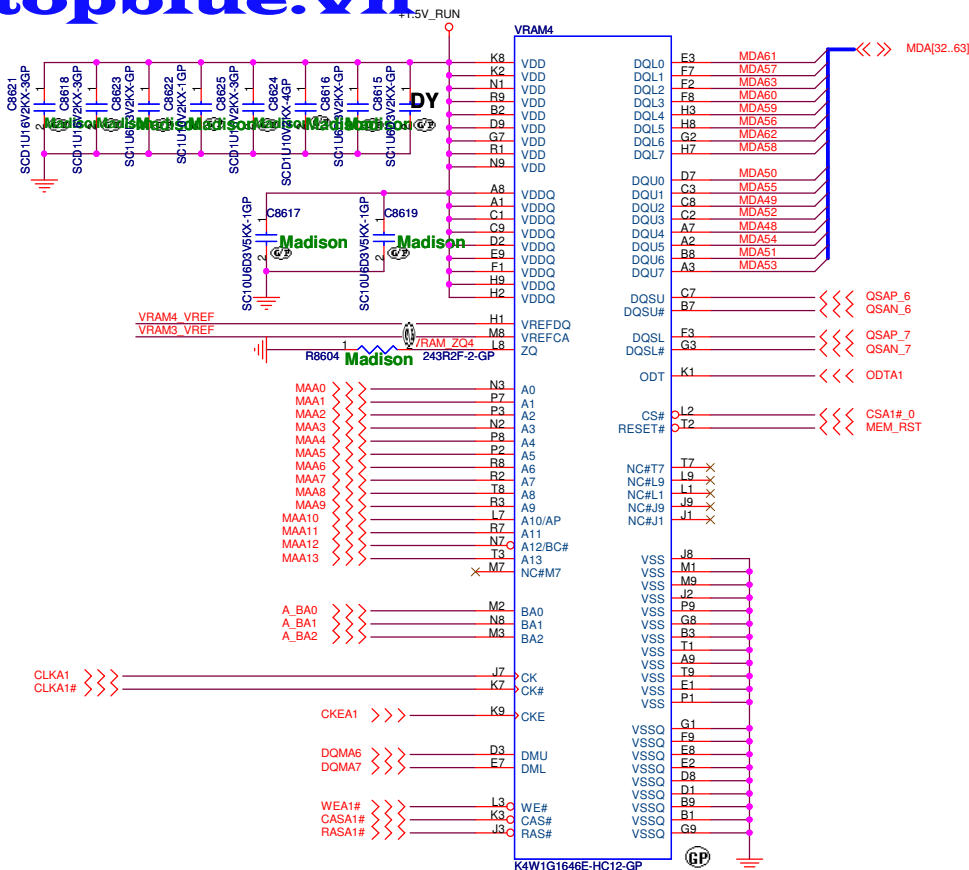
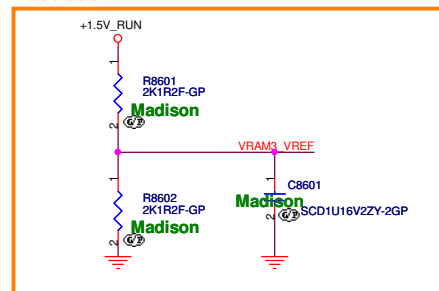




Madison

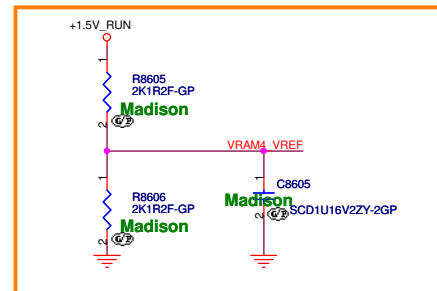
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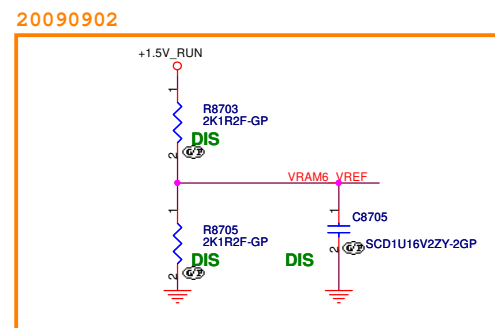
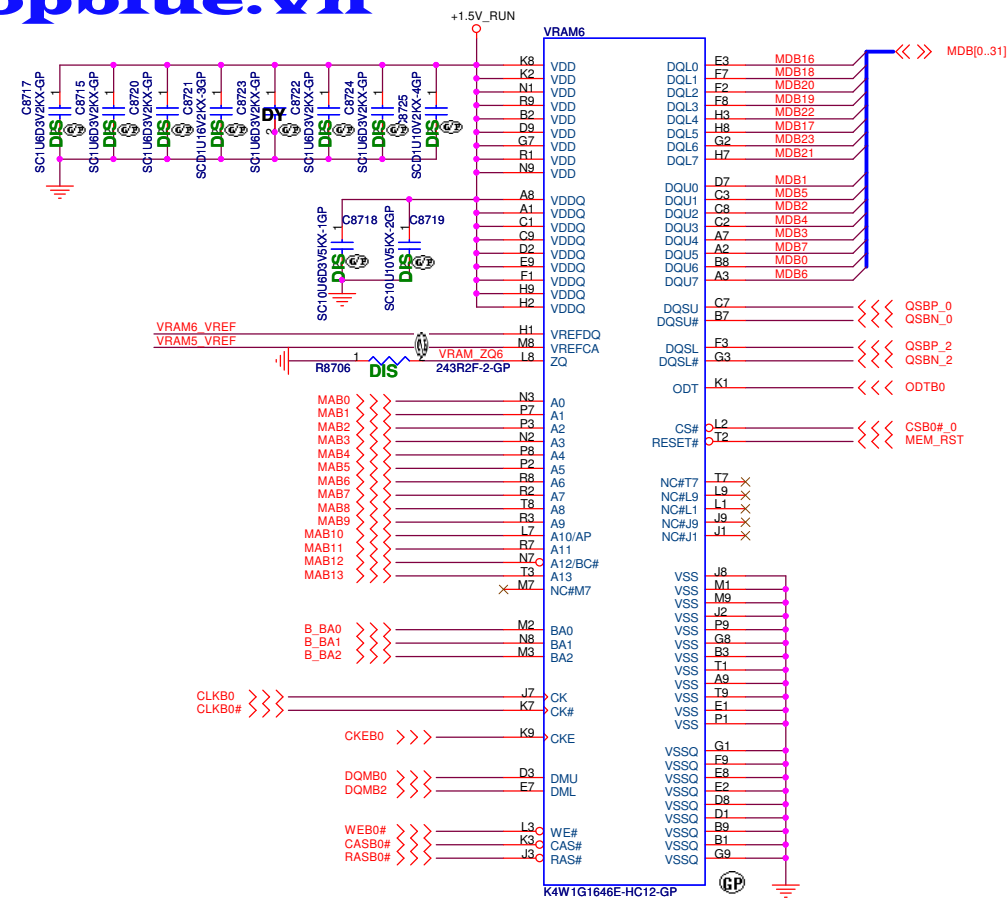
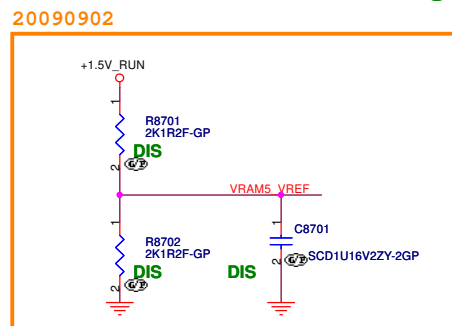
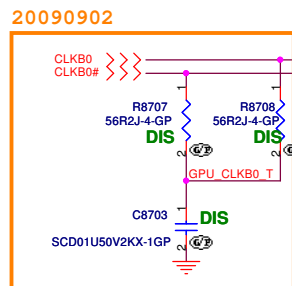
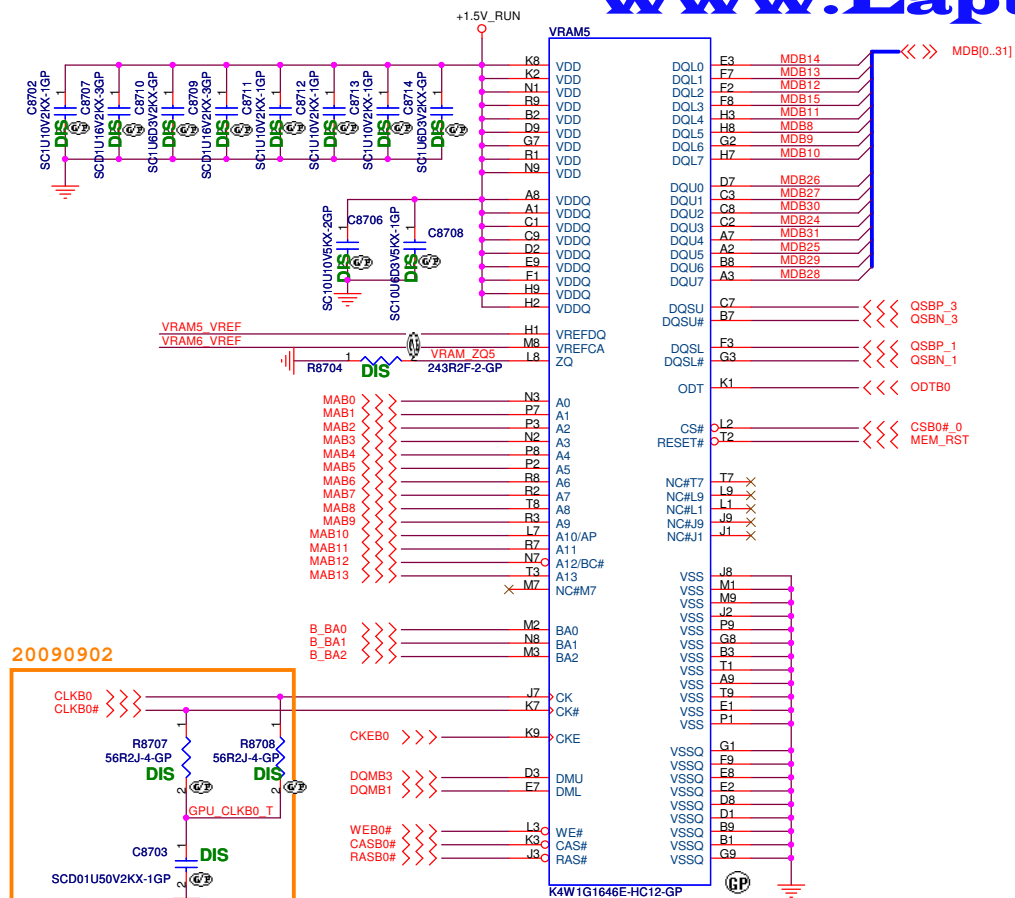
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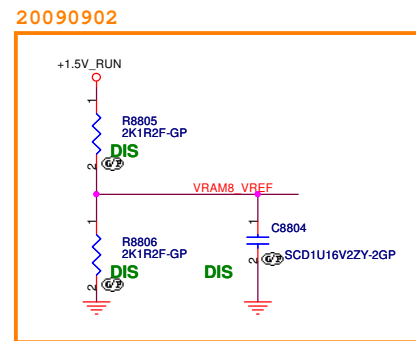
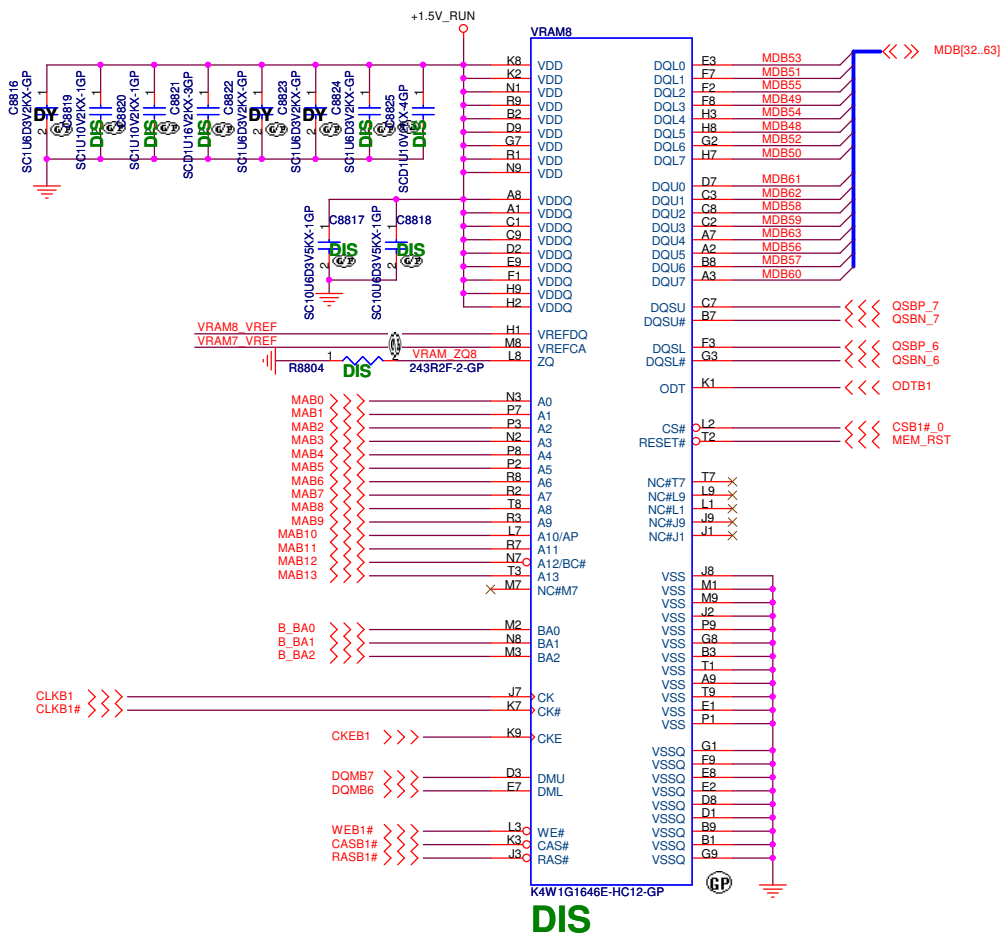
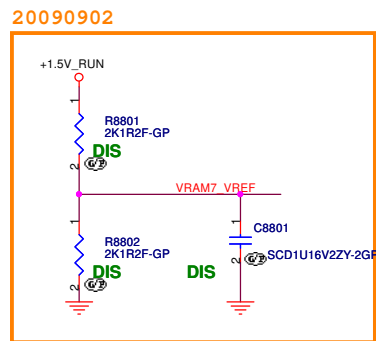
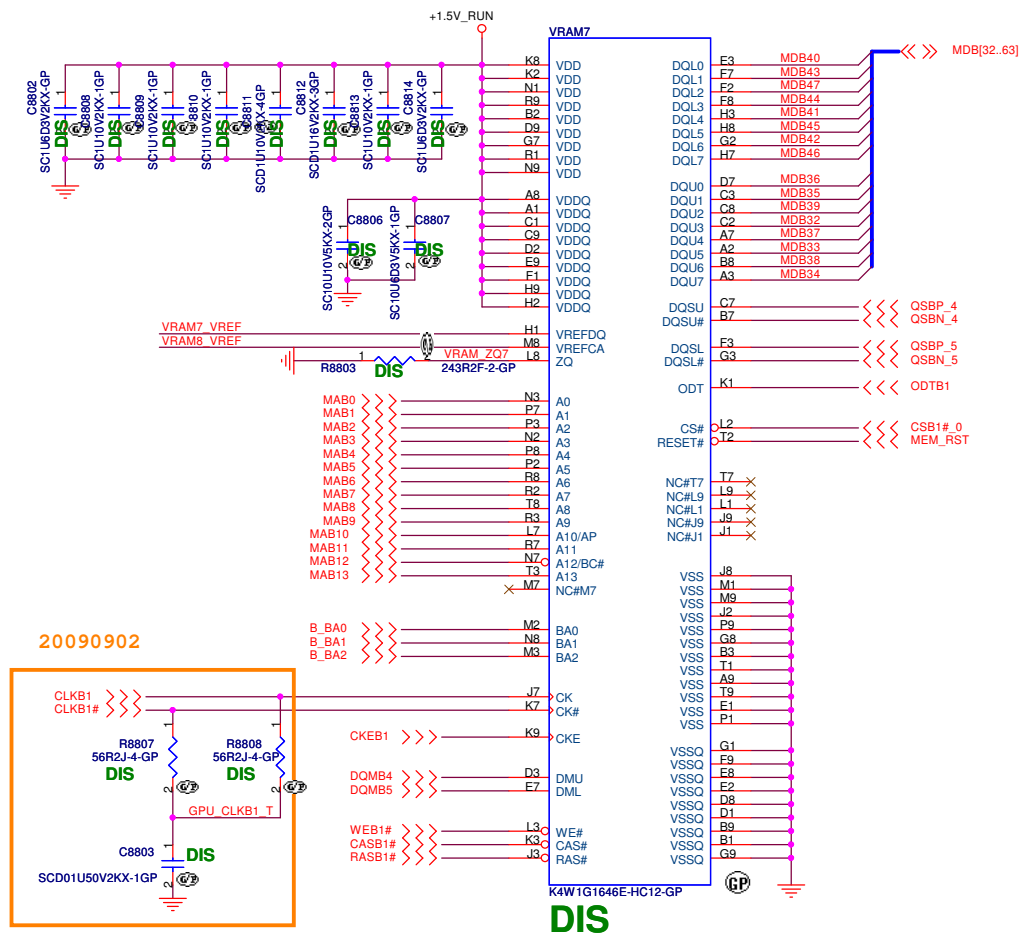


Madison

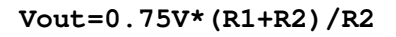
20090902







RT6208BQW 101 TVGA_CORE



RT8208B:74.08208.A73

PWRCNTL_0	PWRCNTL_1	+VGA_CORE
H	H	0.9V
L	H	0.95V
H	L	1.05V
L	L	1.1V

<Core Design>



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Title	Author	Year	Journal	Volume	Page
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RT8208B +VGA_CORESize
A3

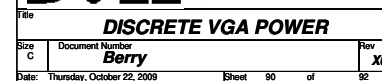
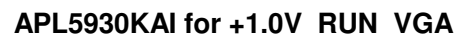
Document Number

Arsenal DJ1 Discrete

Date: Thursday, October 22, 2009

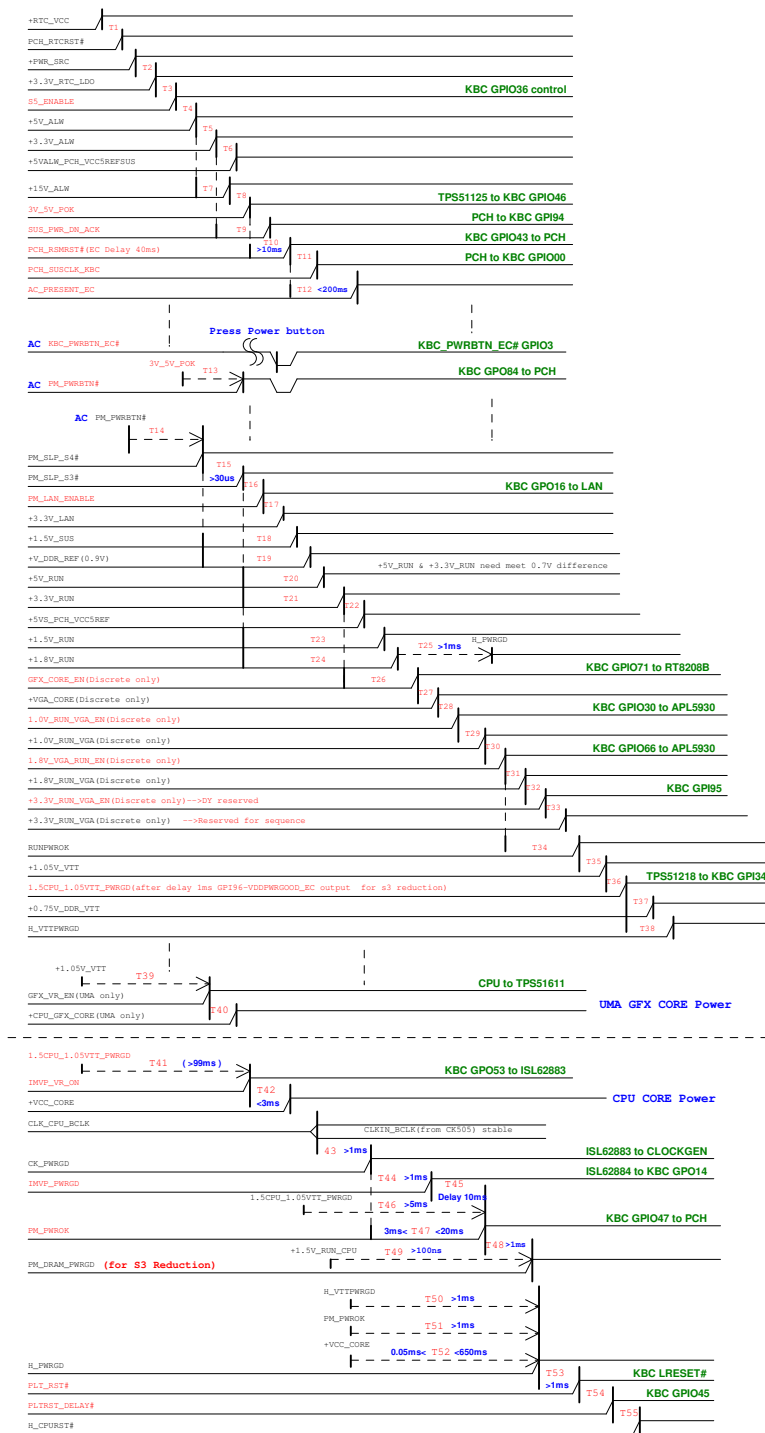
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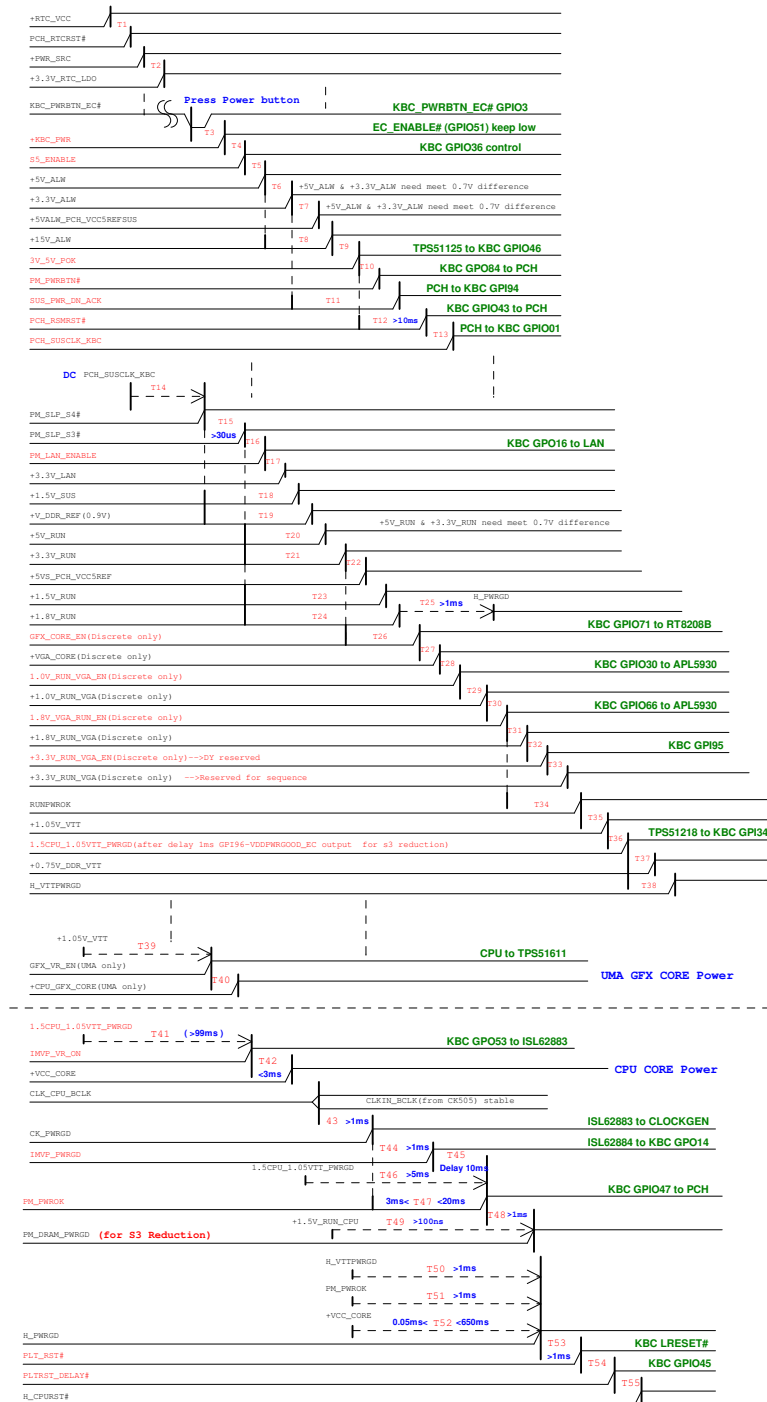
(AC mode)

red word: KBC GPIO



(DC mode)

red word: KBC GPIO



(Blanking)

<Core Design>



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Title

Change History

Size
A3

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