

MODEL NAME : VBW00  
PROJECT CODE : ANRVBW0100  
PCB NO : DA8000WK000 LA-9981P M/B  
DA40001FO00 LS-9101P POWER BUTTON/B  
DA40001FP00 LS-9102P USB/B  
DA40001FQ00 LS-9103P TP BUTTON/B

# Dell / Compal Confidential

## Schematic Document

Intel Shark Bay ULT  
OAK Value2  
UMA/DIS AMD Sun XT

2013-03-09

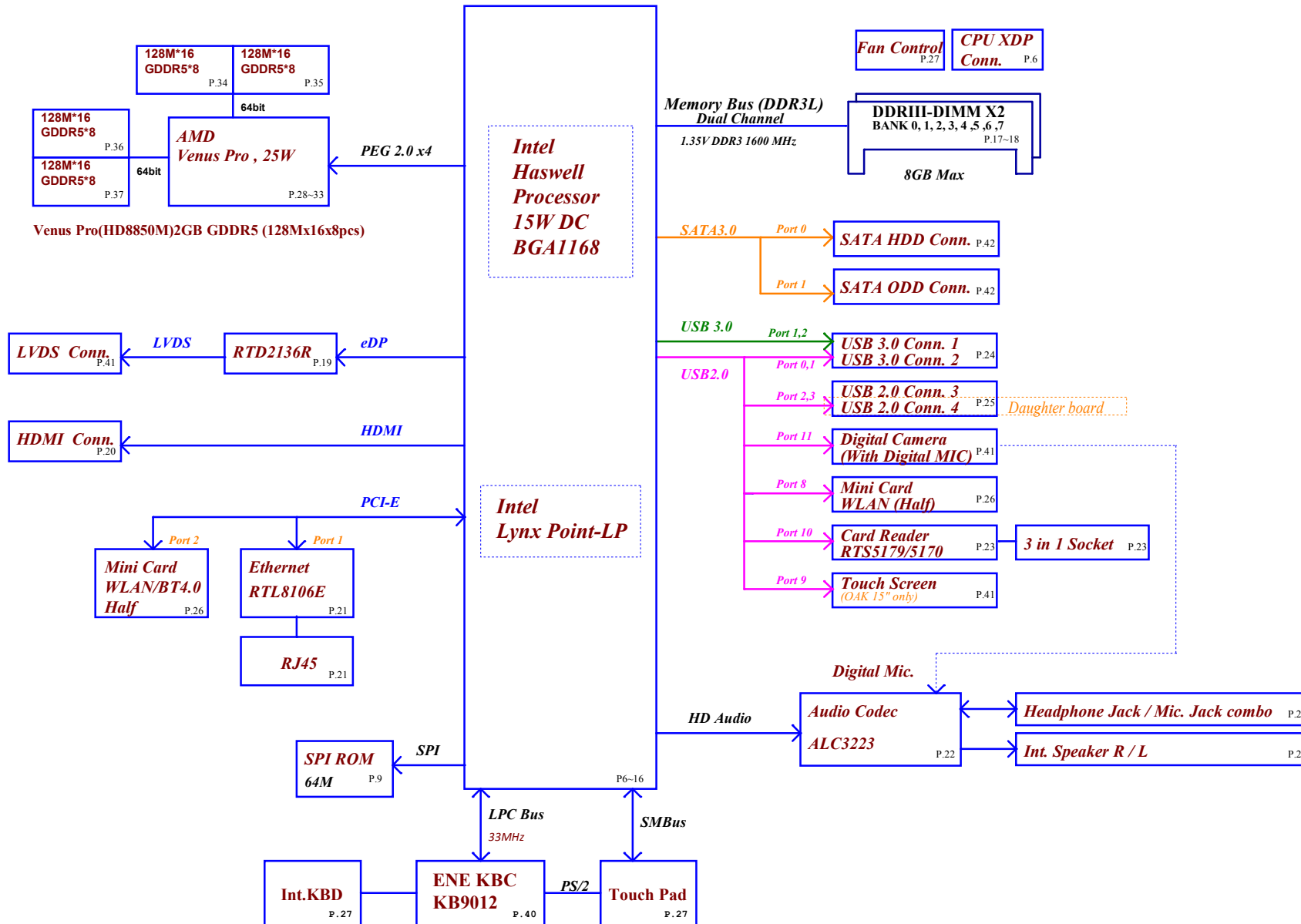
Rev: 0.2

X76@ : 76 level  
46@ : 46 level  
@ : Nopop component  
CONN@ : Connector component  
XDP@ : XDP function  
UMA@ : Only for UMA  
DIS@ : Only for Discrete  
SUN@ : SUN XT  
EMI@ : EMI parts  
@EMI@ : Reserve EMI parts  
ESD@ : ESD parts  
RF@ : RF parts

BOM config  
UMA : UMA@,EMI@,ESD@,RF@,XDP@  
DIS SUN : SUN@,DIS@,EMI@,ESD@,RF@,XDP@



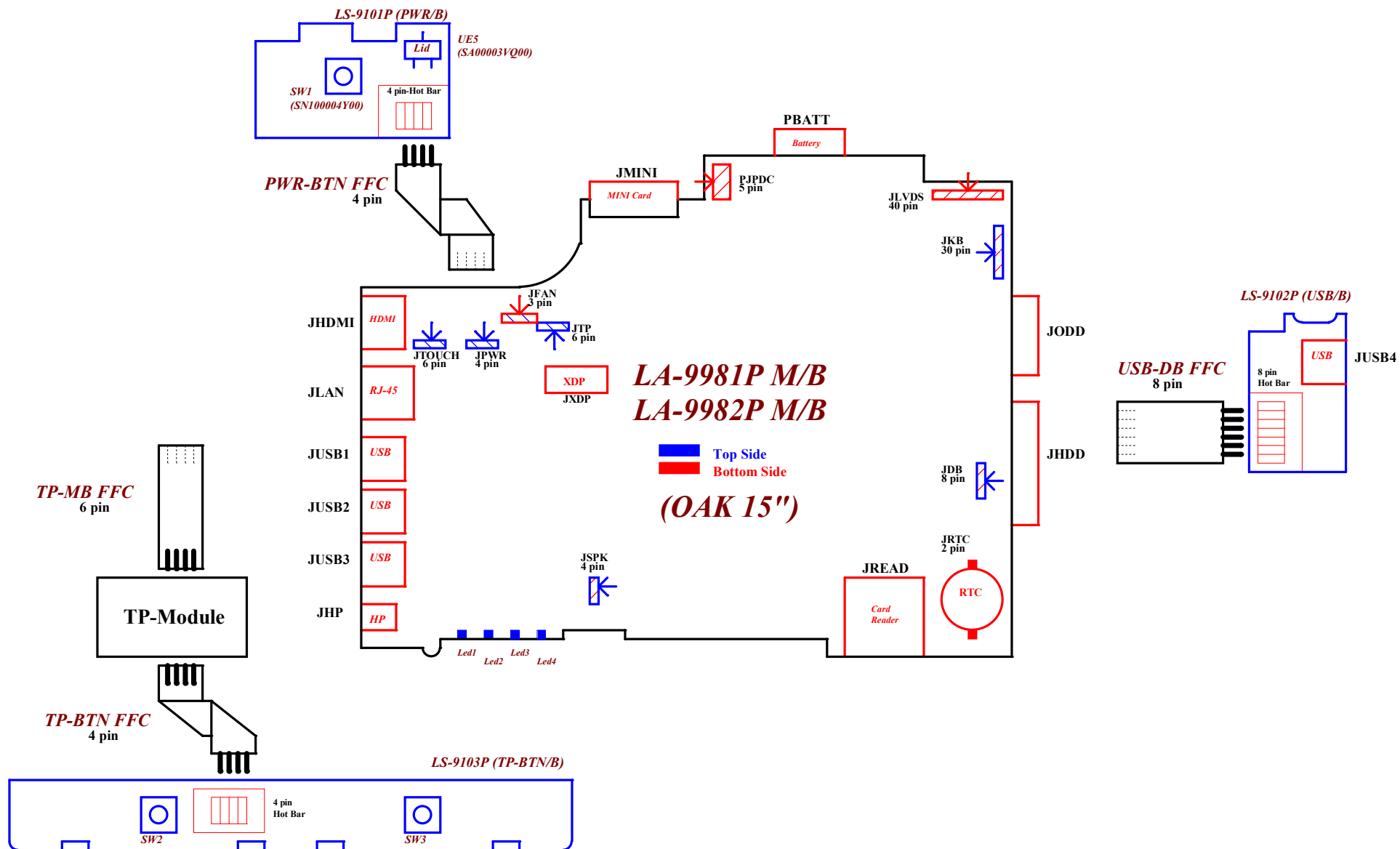
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Project Code : VAW00 / VAW01

File Name : LA-9981P / LA-9982P



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										DB block diagram	
										LA-9981P	
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Board ID Table for AD channel

Vcc	3.3V +/- 1%				
Ra	100K +/- 1%				
Board ID	Rb	V <sub>AD_BID</sub> min	V <sub>AD_BID</sub> typ	V <sub>AD_BID</sub> max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V	3.300V	0xE7 - 0xFF

SMBUS Control Table

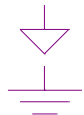
	SOURCE	BATT	Charger	RTD2136S	VGA	DDR3L	XDP	WLAN mini card	Touch pad
EC_SMB_CK1 EC_SMB_DA1	KB9012	V	V						
EC_SMB_CK2 EC_SMB_DA2	KB9012			V	V				
SMBCLK SMBDATA	ULT					V	V	V	V
SMLCLK SMLDATA	ULT								
SML1CLK SML1DATA	ULT								

Link

BOARD ID Table

ID	PCB Revision			
	UMA	Sun XT	Venus Pro	Venus XT
0	0.1			
1		0.1		
2			0.1	
3				0.1
4	0.2			
5		0.2		
6			0.2	
7				0.2
8	0.3			
9		0.3		
10			0.3	
11				0.3
12	1.0			
13		1.0		
14			1.0	
15				1.0

Symbol Note :



: means Digital Ground



: means Analog Ground

CLOCK SIGNAL	
CLKOUT_PCIE0	
CLKOUT_PCIE1	
CLKOUT_PCIE2	10/100 LAN
CLKOUT_PCIE3	MINI Card (WLAN)
CLKOUT_PCIE4	dGPU (N14P)
CLKOUT_PCIE5	

ULT

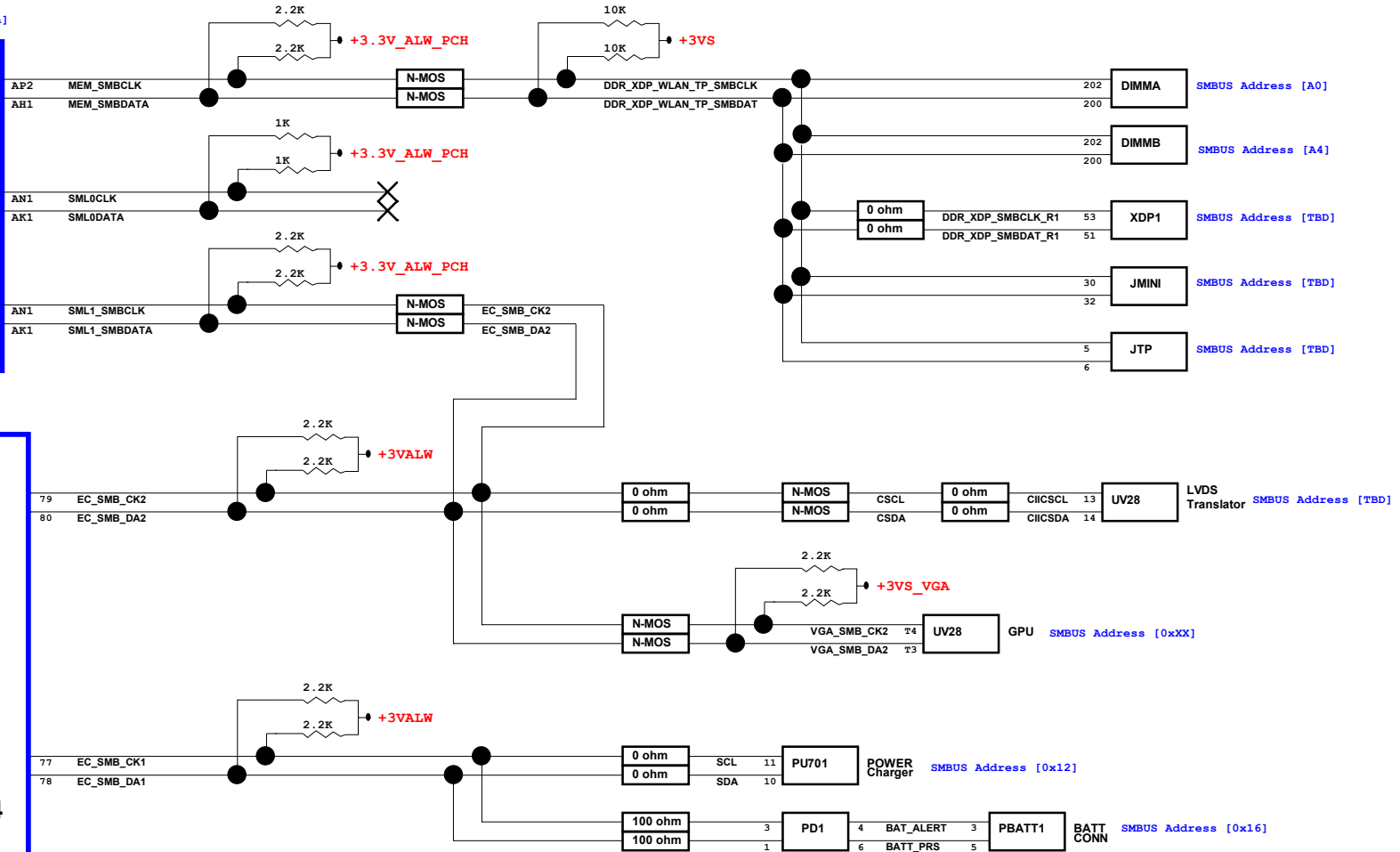
USB3.0	
Port1	USB connector 2
Port2	USB connector 1
Port3	
Port4	
USB2.0	
Port0	USB connector 2
Port1	USB connector 1
Port2	USB connector 3
Port3	USB connector 4 (DB)
Port4	MINI Card (WLAN)
Port5	Touch Screen Panel
Port6	Card Reader
Port7	Camera
PCI EXPRESS	
Lane 1	
Lane 2	
Lane 3	10/100 LAN
Lane 4	MINI Card (WLAN)
Lane 5	PEG (N14P)
Lane 6	PEG (N14P)
SATA	
SATA0	HDD
SATA1	ODD
SATA2	
SATA3	

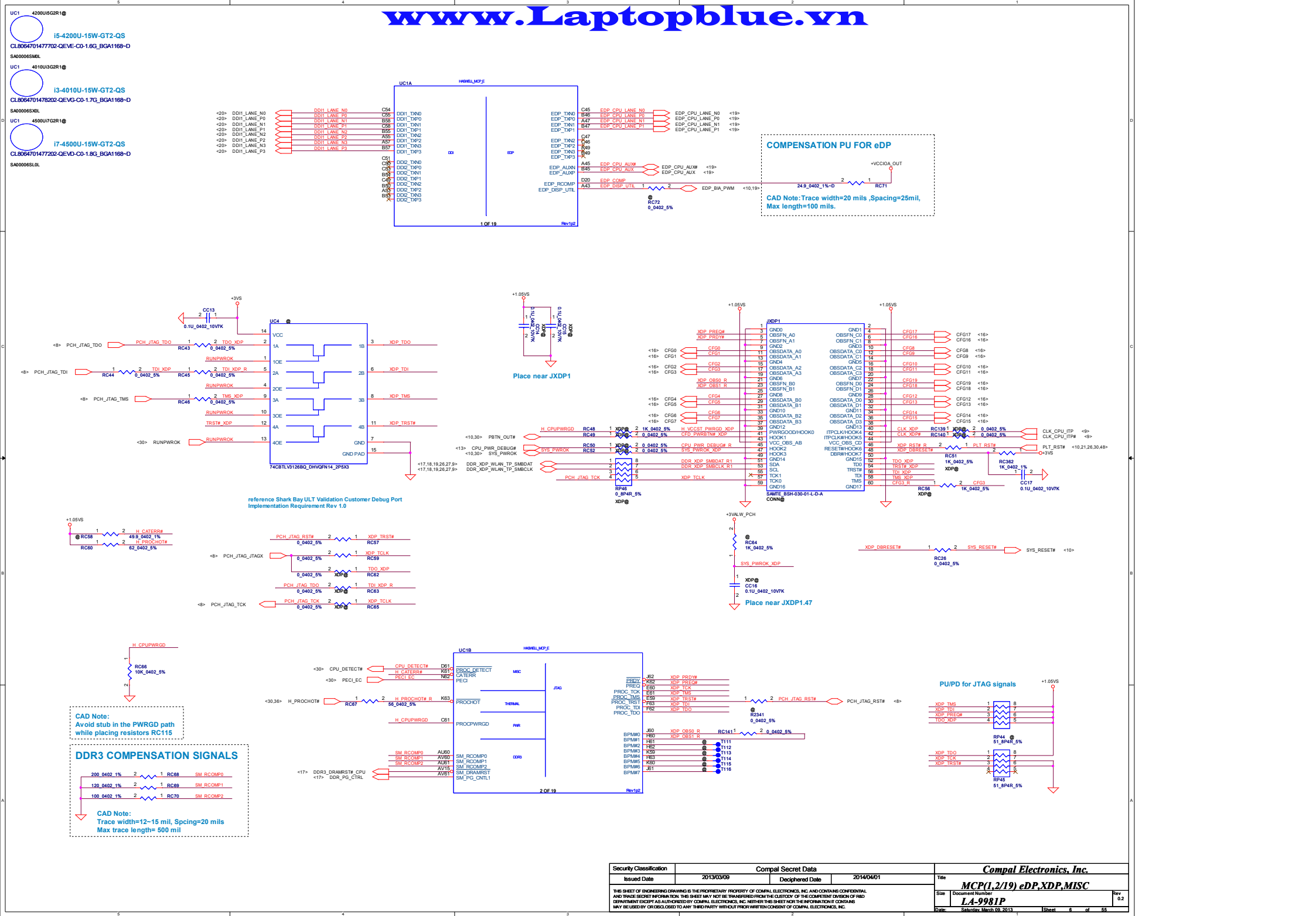
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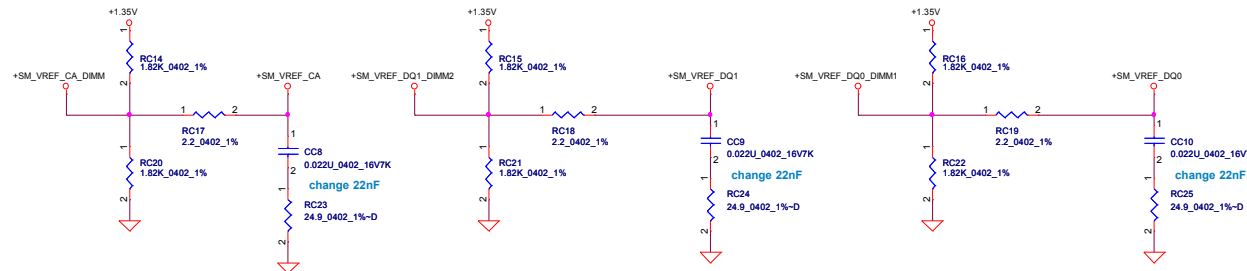
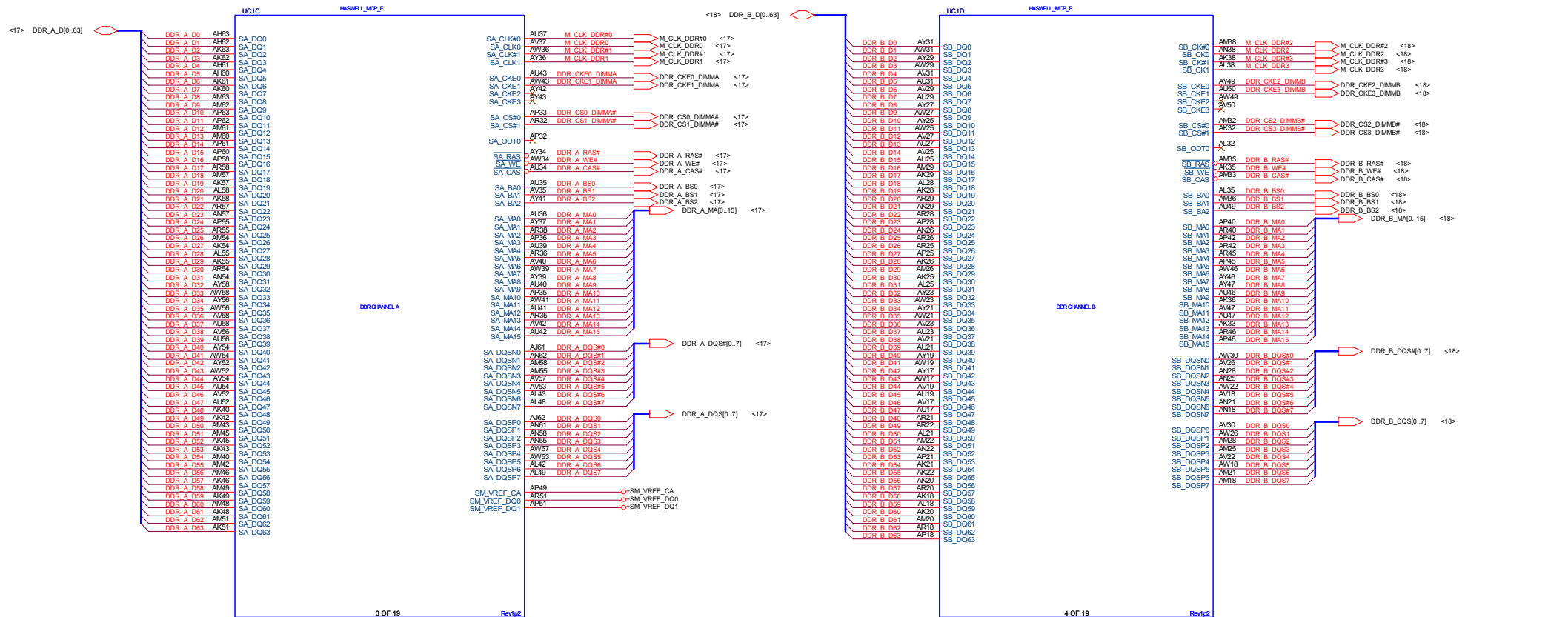
SMBUS Address [0x9a]

MCH  
Shark bay

KBC  
KB9012A4













confirm by intel request PDG P141

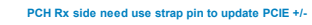
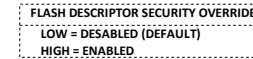
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<6>	PCH_JTAG_RST#		PCH_JTAG_RST#
<6>	PCH_JTAG_TCK		PCH_JTAG_TCK
<6>	PCH_JTAG_TDI		PCH_JTAG_TDI
<6>	PCH_JTAG_TDO		PCH_JTAG_TDO
<6>	PCH_JTAG_TMS		PCH_JTAG_TMS
<6>	PCH_JTAG_JTAGX		PCH_JTAG_JTAGX



ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers



A







+3VS



CS# 1 8  
VCC 2 7

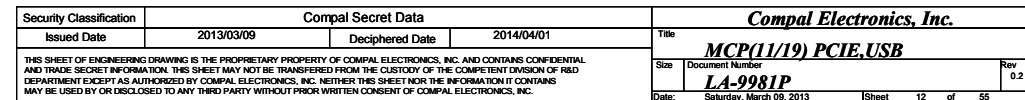


<29> XTAL24\_IN  XTAL24\_IN

[illegible]

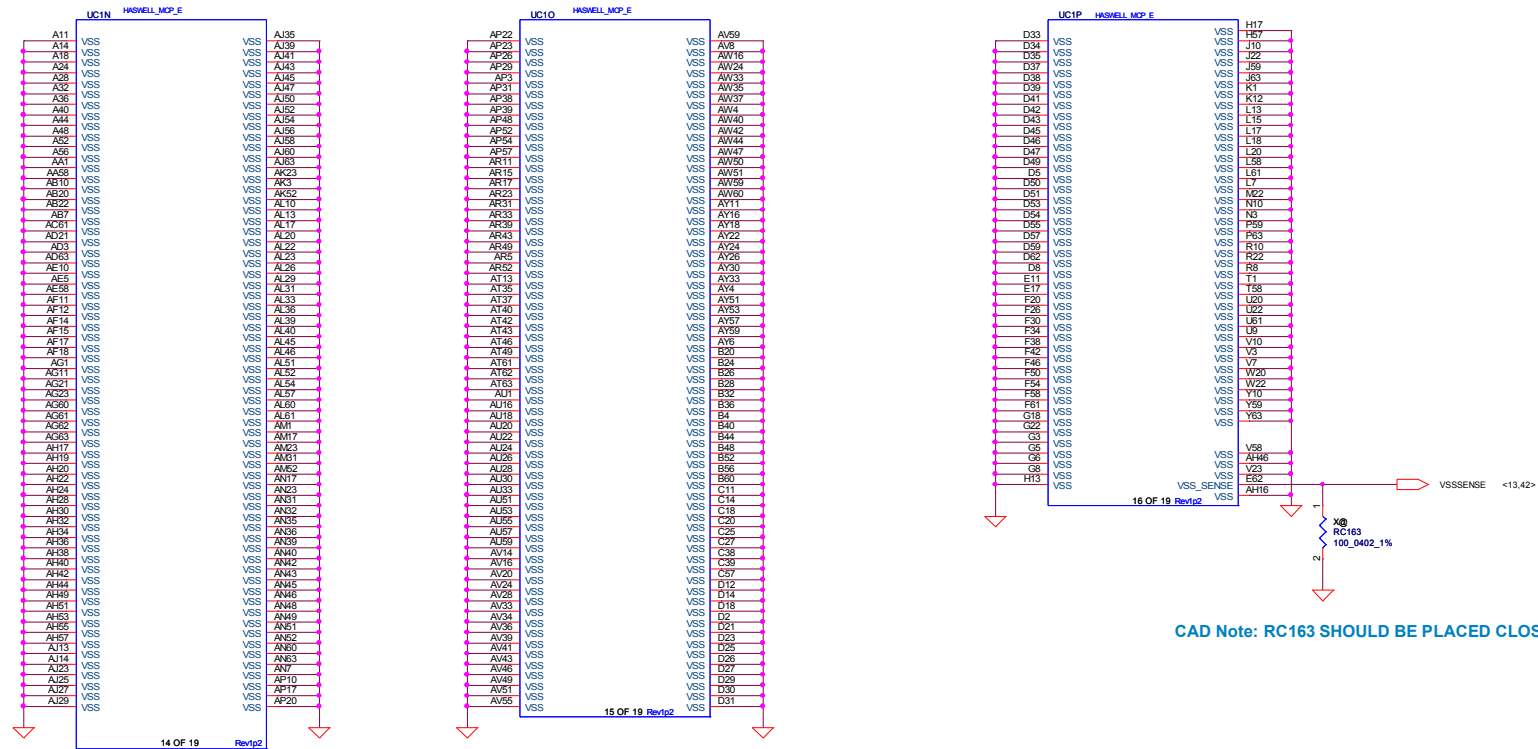












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H=4mm

2-3A to 1 DIMMs/channel

Populate RD1, De-Populate RD7 for Intel DDR3 VREFDQ multiple methods M1  
Populate RD7, De-Populate RD1 for Intel DDR3 VREFDQ multiple methods M3

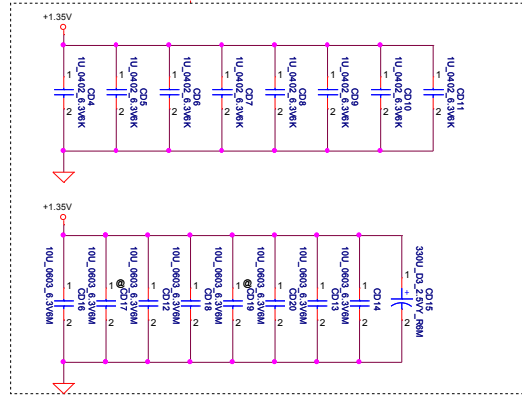
<7> DDR\_A\_DQS#(0..7)  
<7> DDR\_A\_DQ(0..63)  
<7> DDR\_A\_DQS(0..7)  
<7> DDR\_A\_MA(0..15)

All VREF traces should have 10 mil trace width

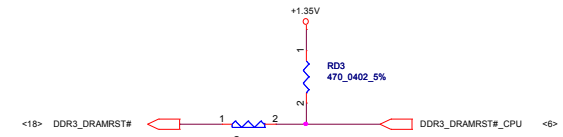
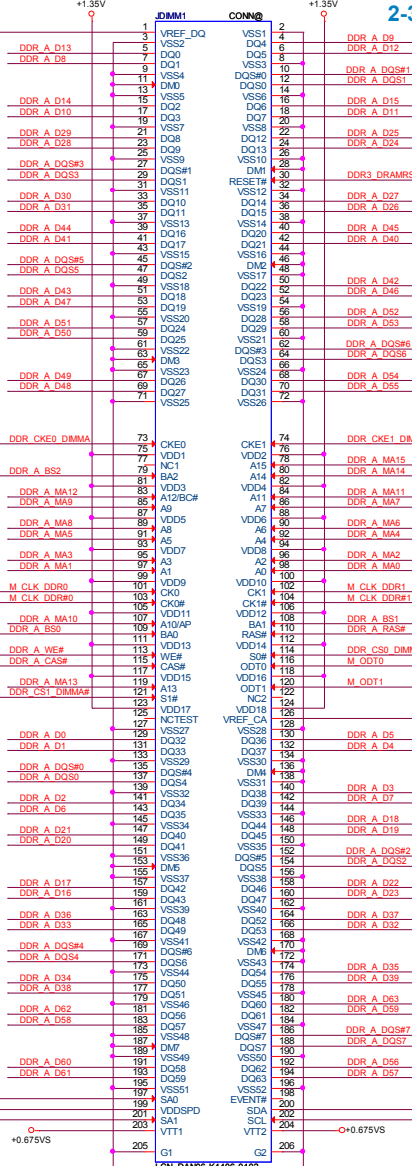
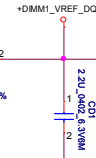
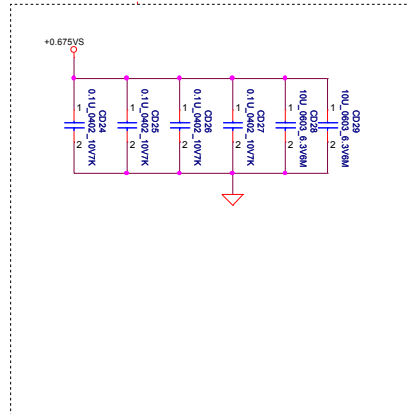
Layout Note:  
Place near JDIMM1

Note:  
Check voltage tolerance of VREF\_DQ at the DIMM socket

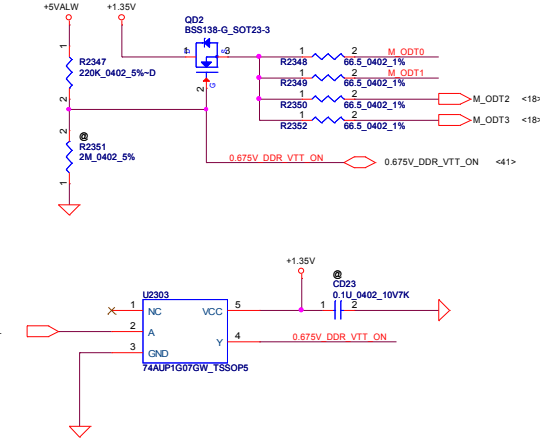
CAD NOTE  
PLACE THE CAP NEAR TO DIMM RESET PIN



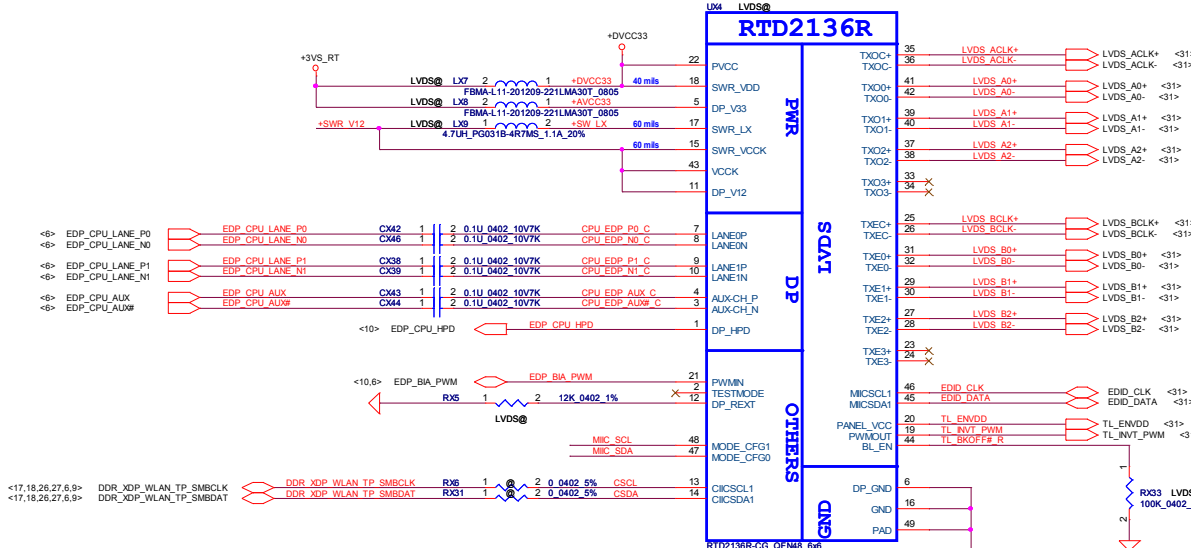
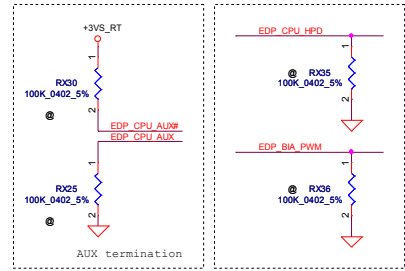
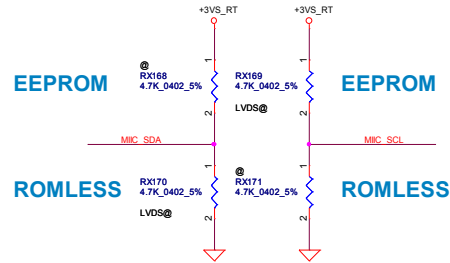
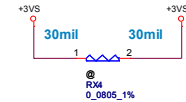
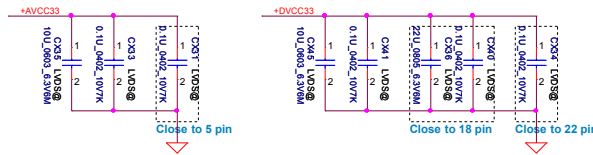
Layout Note:  
Place near JDIMM1.203,204



DDR3L SODIMM ODT GENERATION

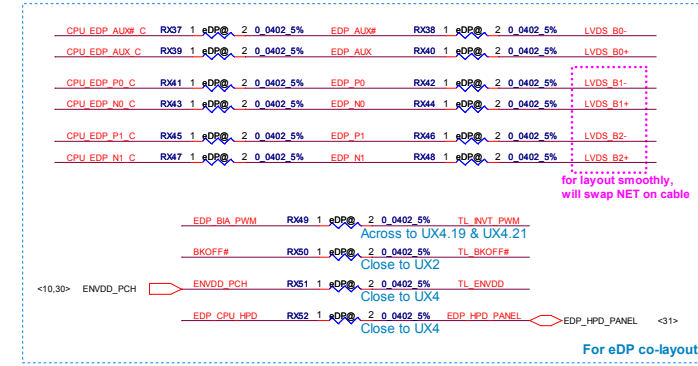
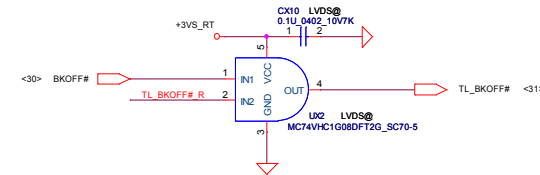




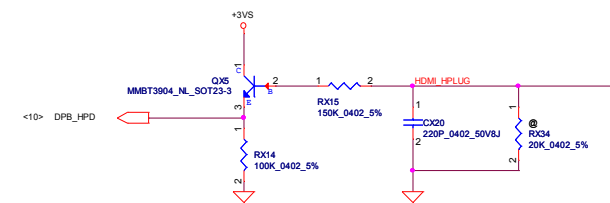
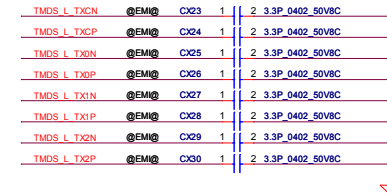
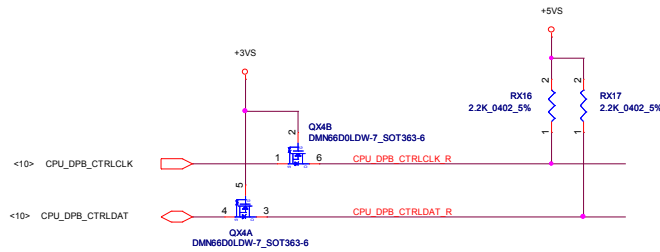
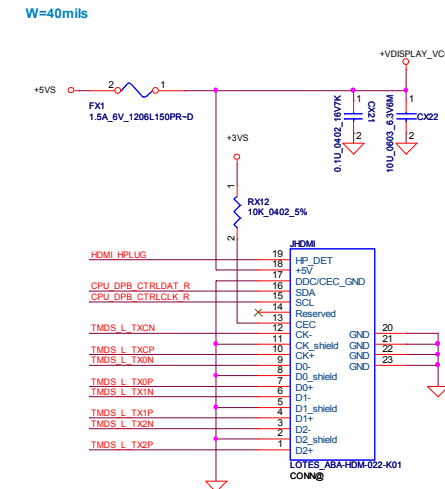
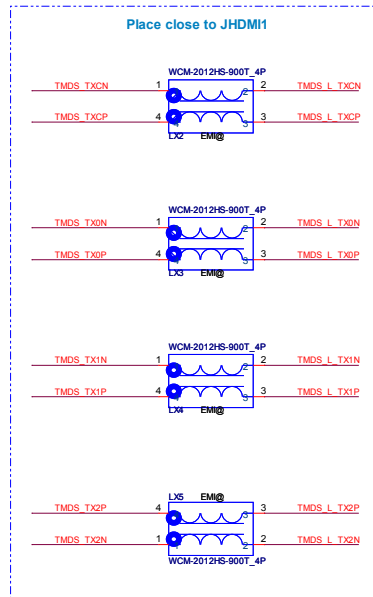
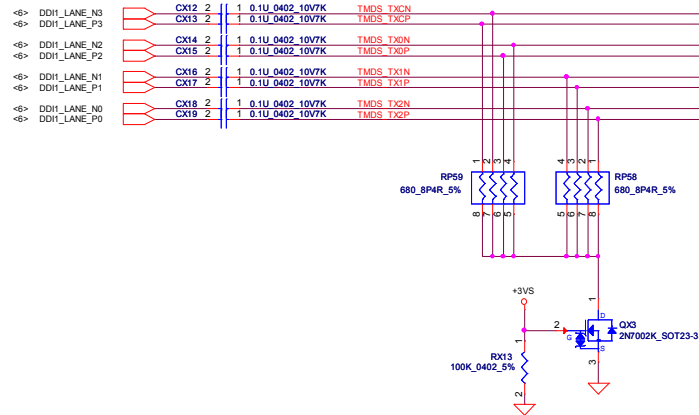


RTD2136S : SA00004NW10  
RTD2136R : SA000067100

Vendor advise reserve it



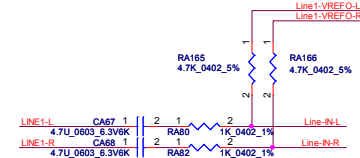
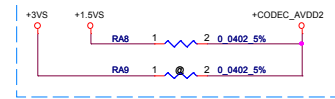
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Issued Date		Deciphered Date		2014/04/01	
2013/03/09		2014/04/01		eDP to LVDS converter	
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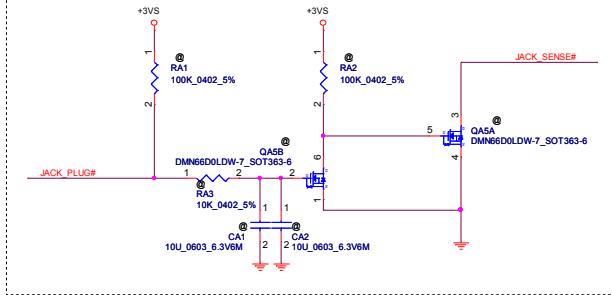


### CA71, CA51 place close to Pin 26

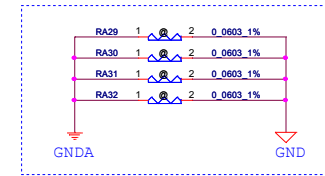
CA53, CA55 change Value from 10U\_0603\_6.3V6M~D to 4.7U\_0603\_6.3V6K



### JACK\_PLUG Delay circuitis



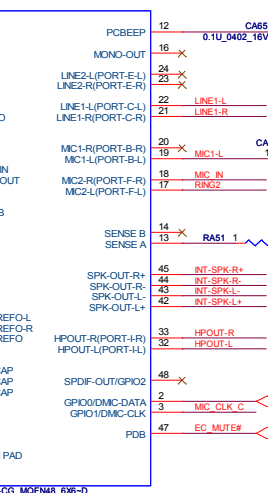
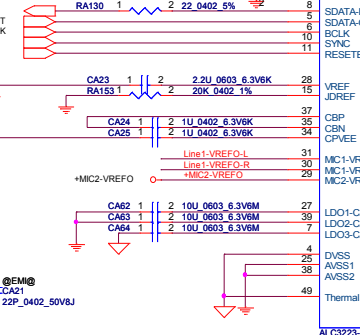
### Reserve for cancel Delay circuitis



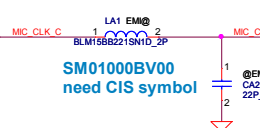
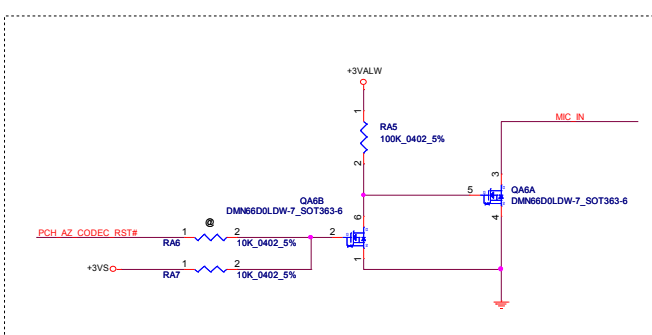
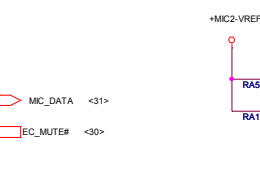
Place on the moat between GND & GNDA.

### CA57,CA58 close to UA1 pin1

- <8> PCH\_AZ\_CODEC\_SDINO
- <8> PCH\_AZ\_CODEC\_SDOOUT
- <8> PCH\_AZ\_CODEC\_BITCLK
- <8> PCH\_AZ\_CODEC\_SYNC
- <8> PCH\_AZ\_CODEC\_RST#



### RA51, RA33 place close to UA1

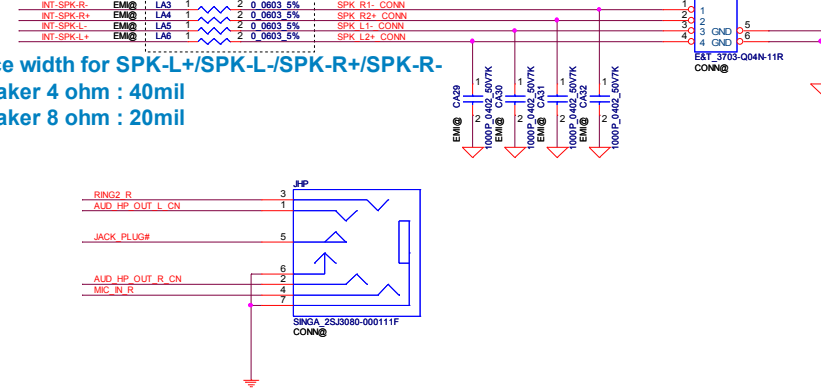


### Close to UA1 Pin11,13,14,16

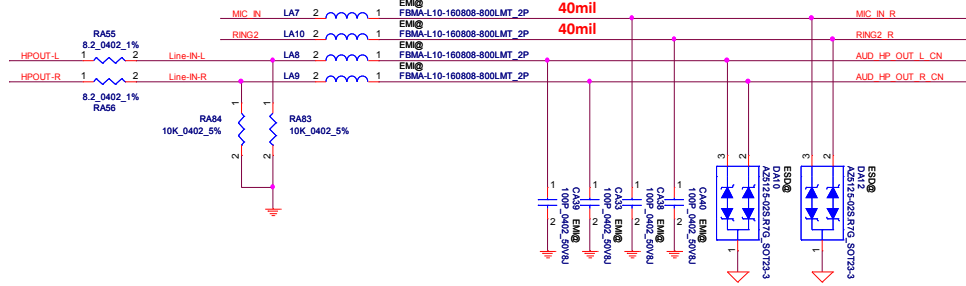


Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-  
Speaker 4 ohm : 40mil  
Speaker 8 ohm : 20mil

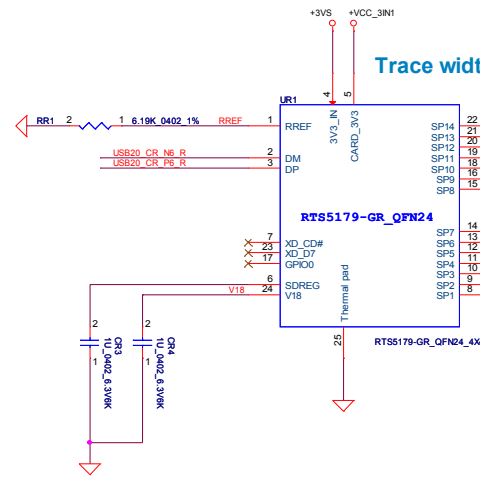
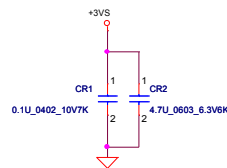
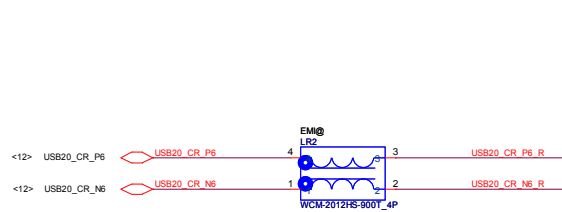
### close to Codec



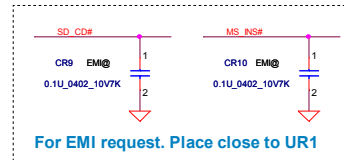
### iPhone and Nokia type Combo Jack



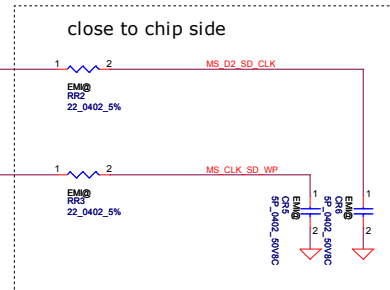
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Trace width:40mil

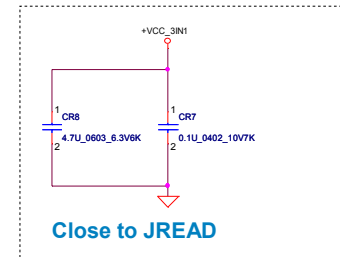


For EMI request. Place close to UR1

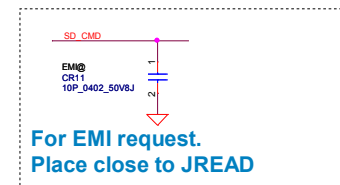


拉MS\_D2\_SD\_CLK到Conn pin 13 SD\_CLK  
再打Via拉到pin 10 MS\_D2

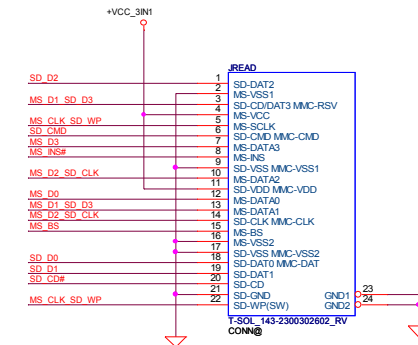
拉MS\_CLK\_SD\_WP到Conn pin 5 MS\_CLK  
再打Via拉到pin 20 SD\_W

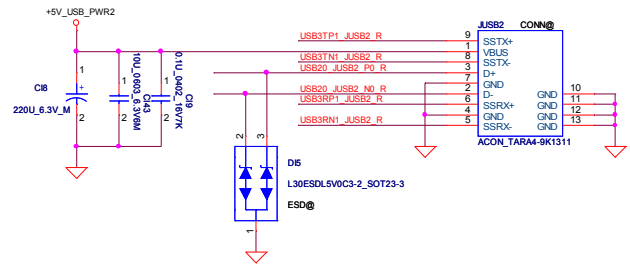
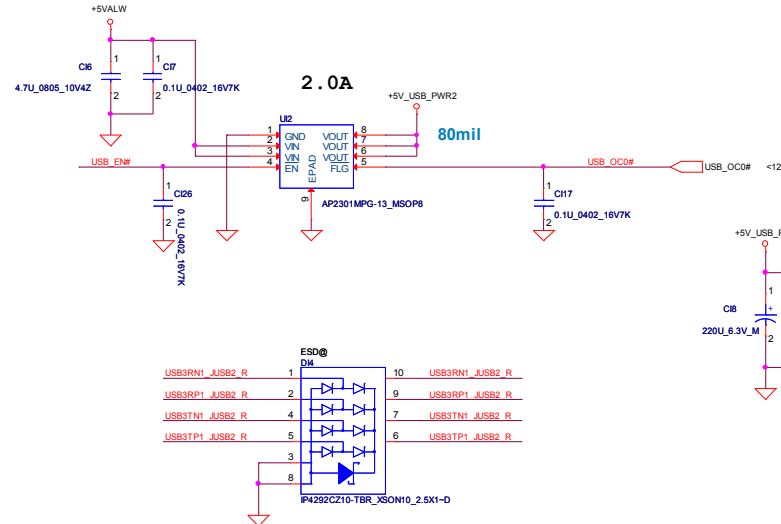
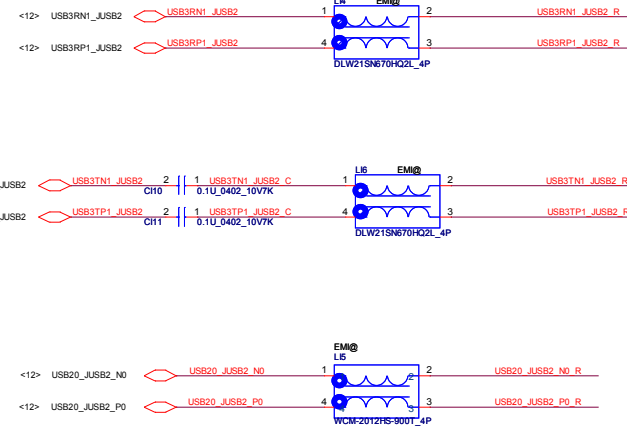
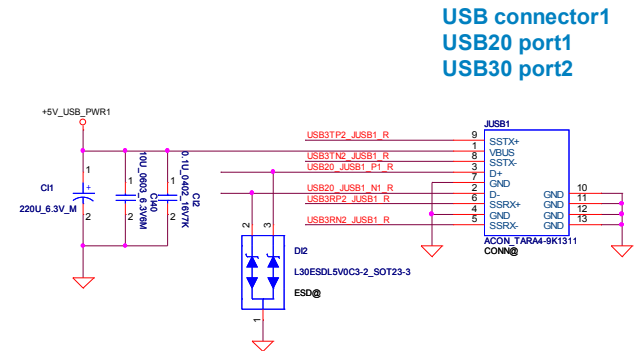
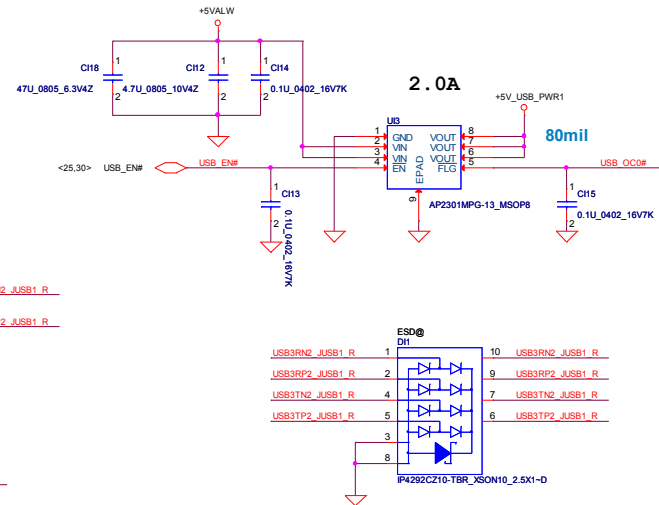
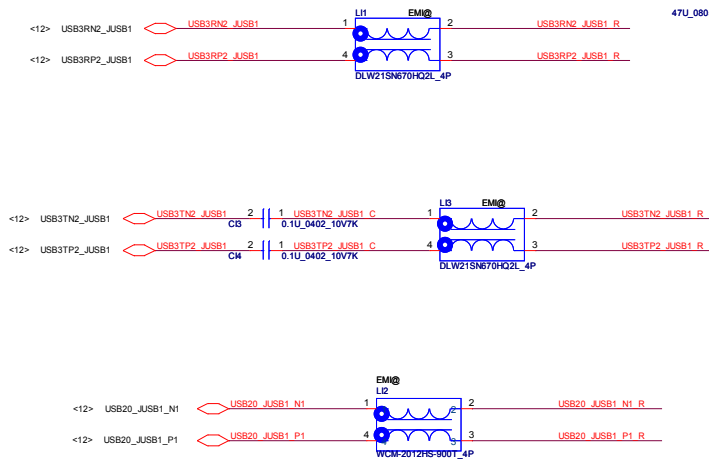


Close to JREAD

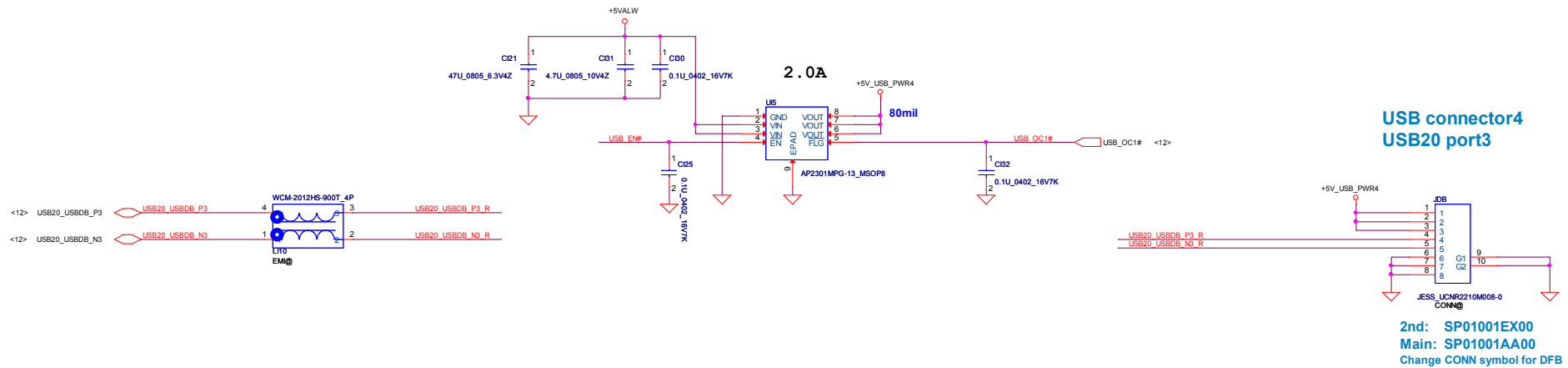
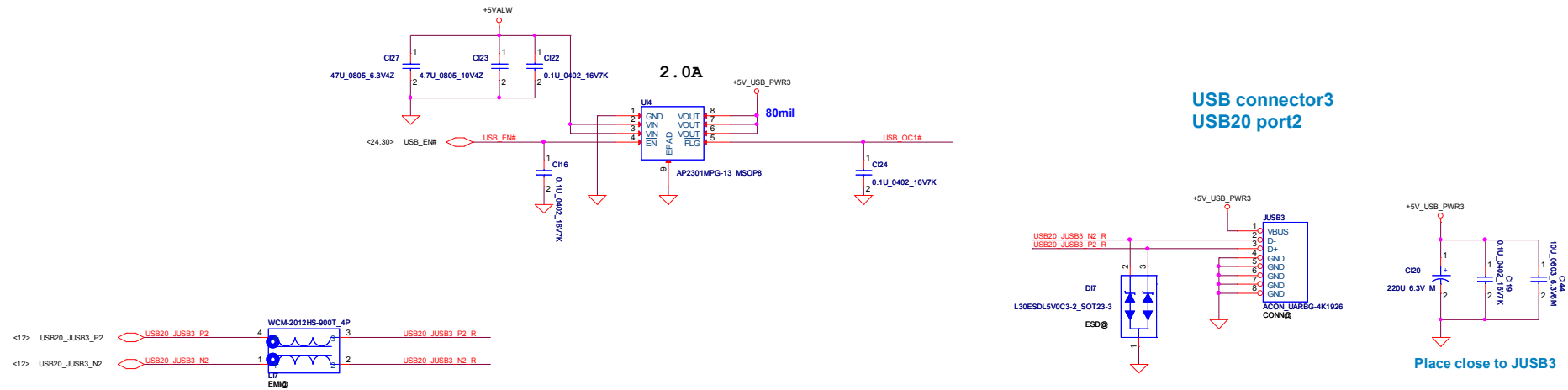


For EMI request.  
Place close to JREAD

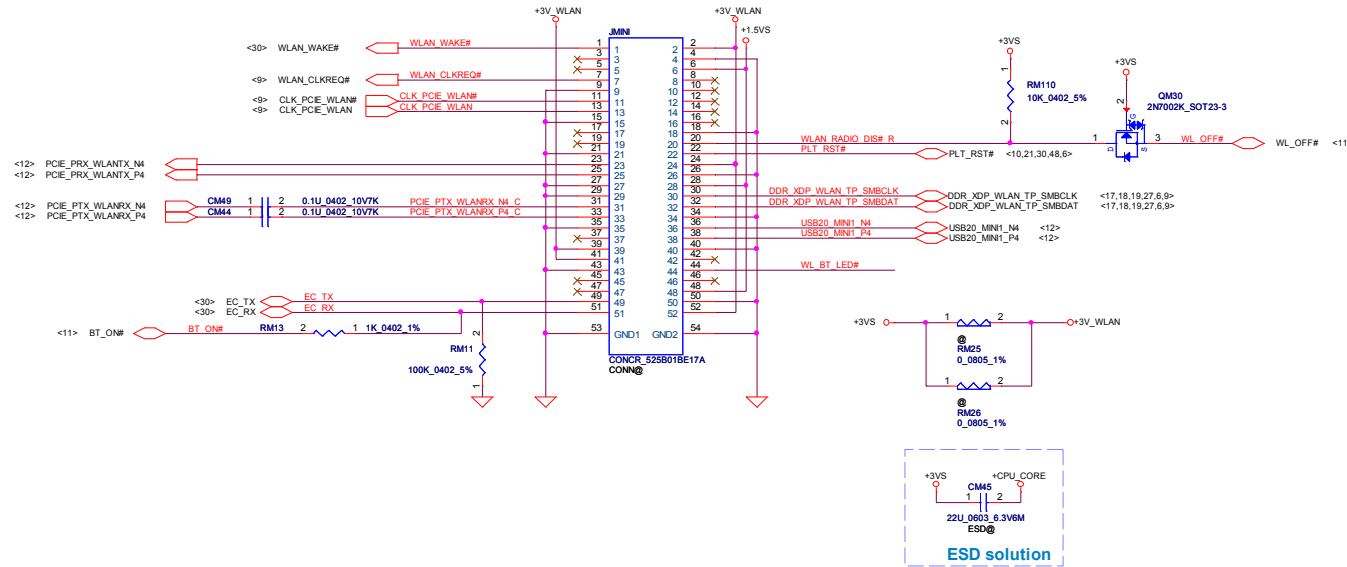




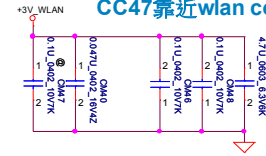




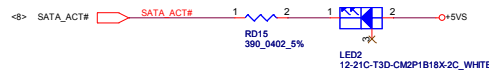
# Mini WLAN/WIMAX H=6.7



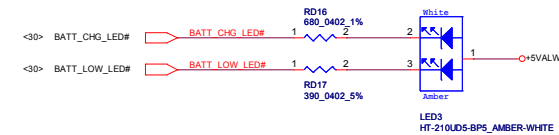
## CC47靠近wlan connector



## HDD LED



## Battery LED

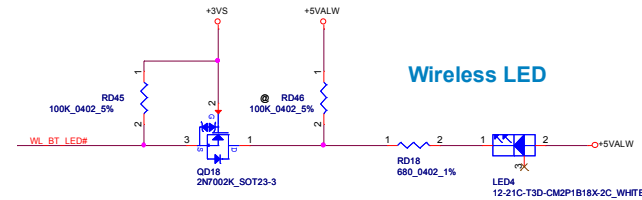


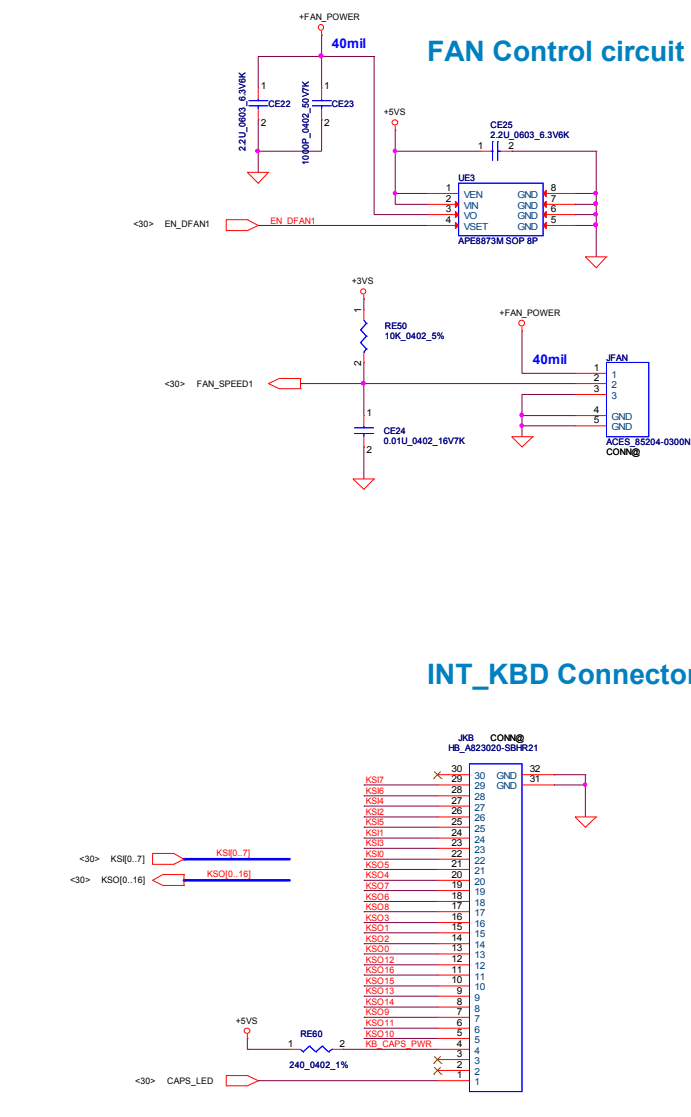
## Power LED



## 10mils, All pins

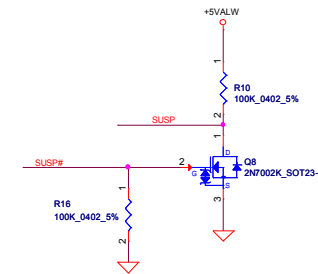
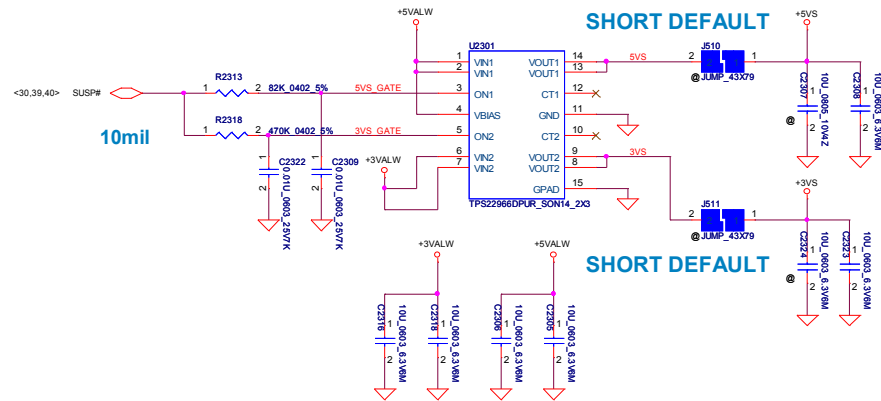
## Wireless LED



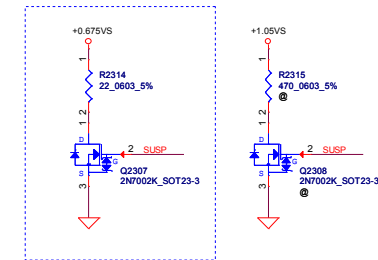
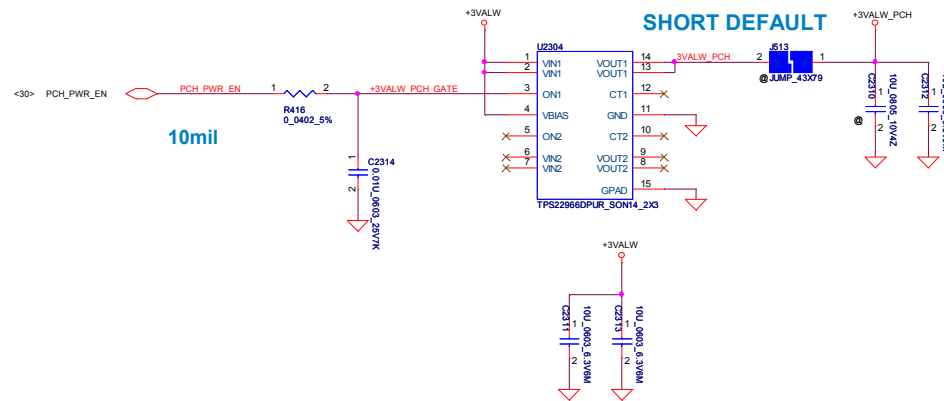


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## +5VS and +3VS switch

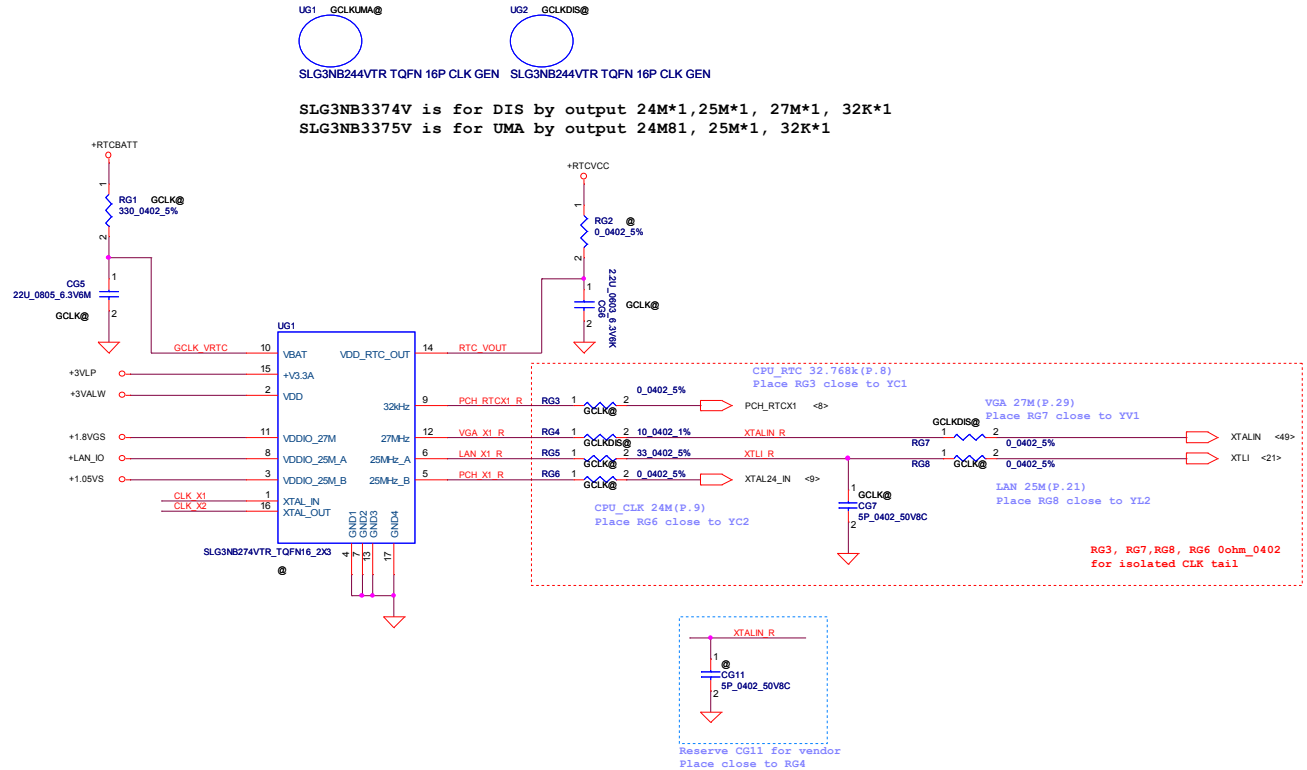
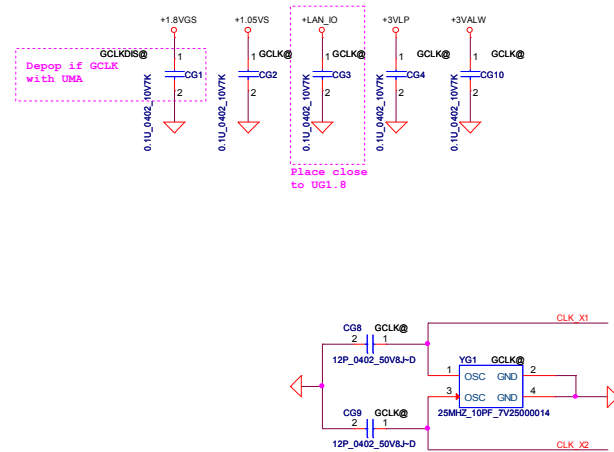


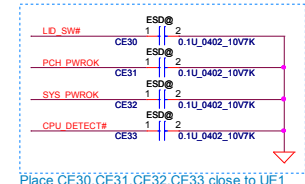
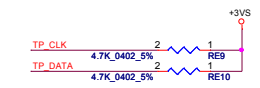
## +3VALW\_PCH switch



For Intel S3 Power Reduction

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				Date	Rev
				Saturday, March 09, 2013	0.2
				Sheet	28 of 55





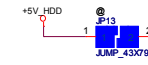
ME\_FWP PCH has internal 20K PD.  
(suspend power rail)

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Issued Date	2013/03/09	Deciphered Date	2014/04/01	Title	EC ENE-KB9012
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Date:				Saturday, March 09, 2013	Sheet 30 of 55

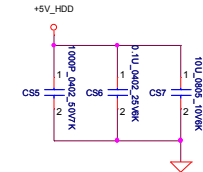
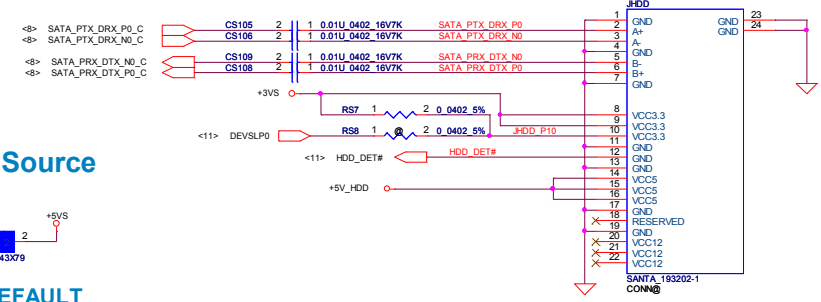


## SATA HDD Connector

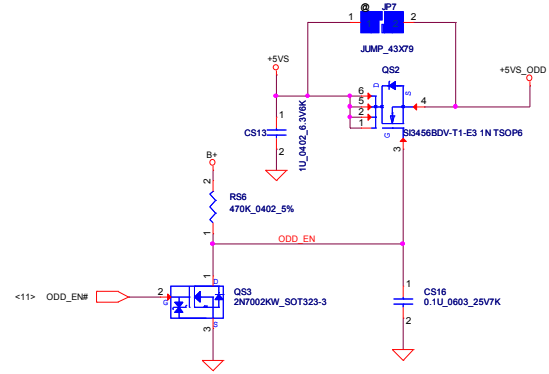
## +5V\_HDD Source



SHORT DEFAULT

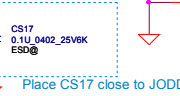
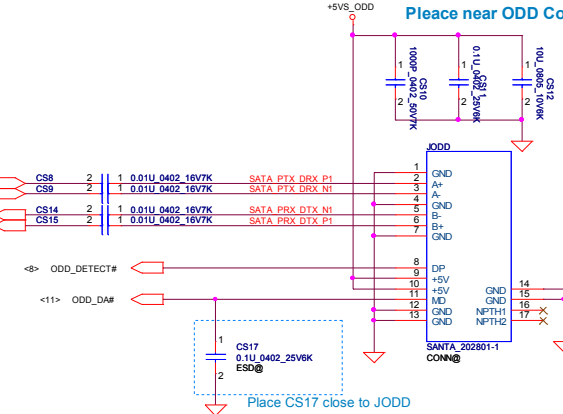


## ODD Power Control



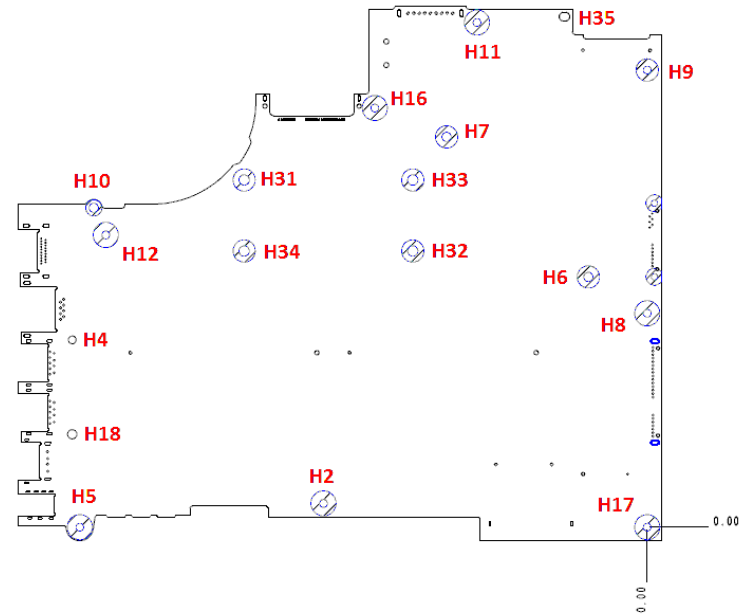
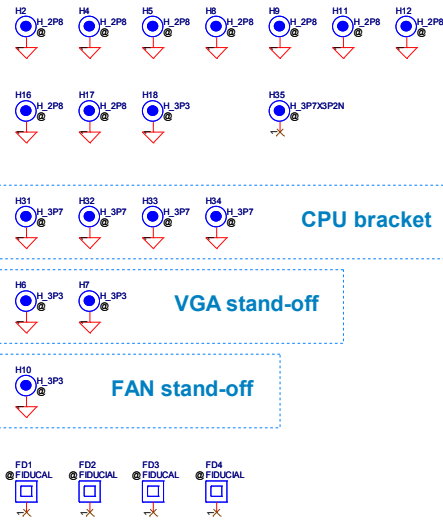
## SATA ODD Connector

Please near ODD Connector





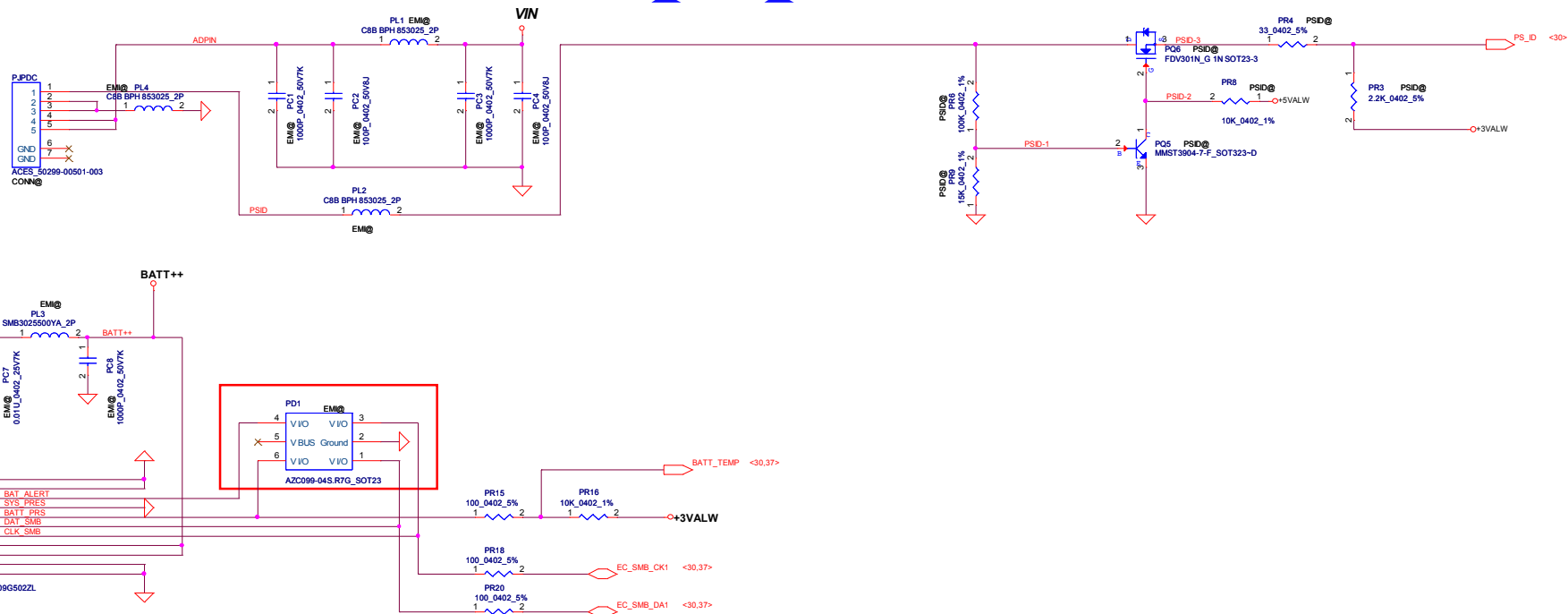
## Screw Hole



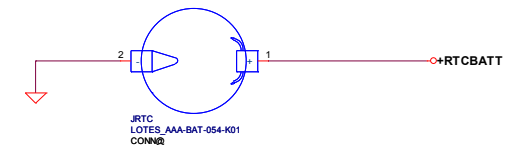
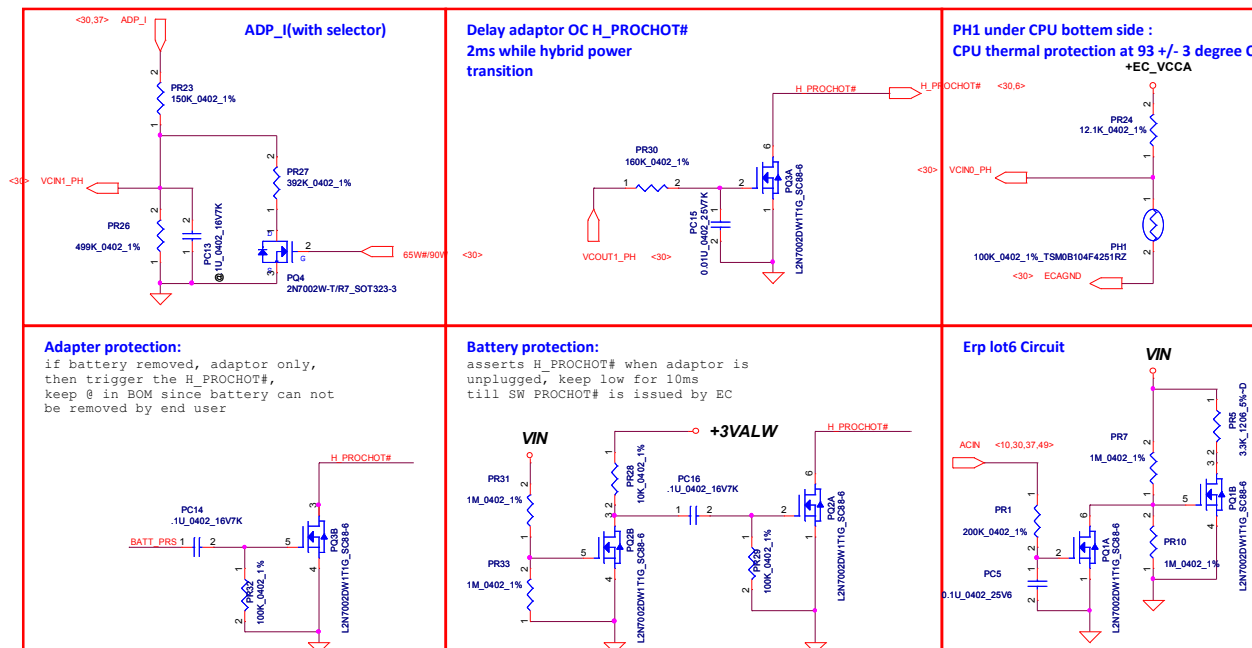
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Issued Date	2013/03/09	Deciphered Date	2014/04/01	Title	<b>Screw Hole</b>
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Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	34	Card Reader	2012/04/27	HW	The Card reader USB signal is incorrect.	SWAP UR1 USB signal P/N	0.2
2							
3							
4							
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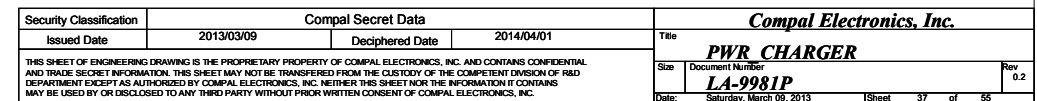
Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
40							
41							
42							
43							
44							
45							
46							
47							
48							
49							
50							
51							
52							
53							
54							

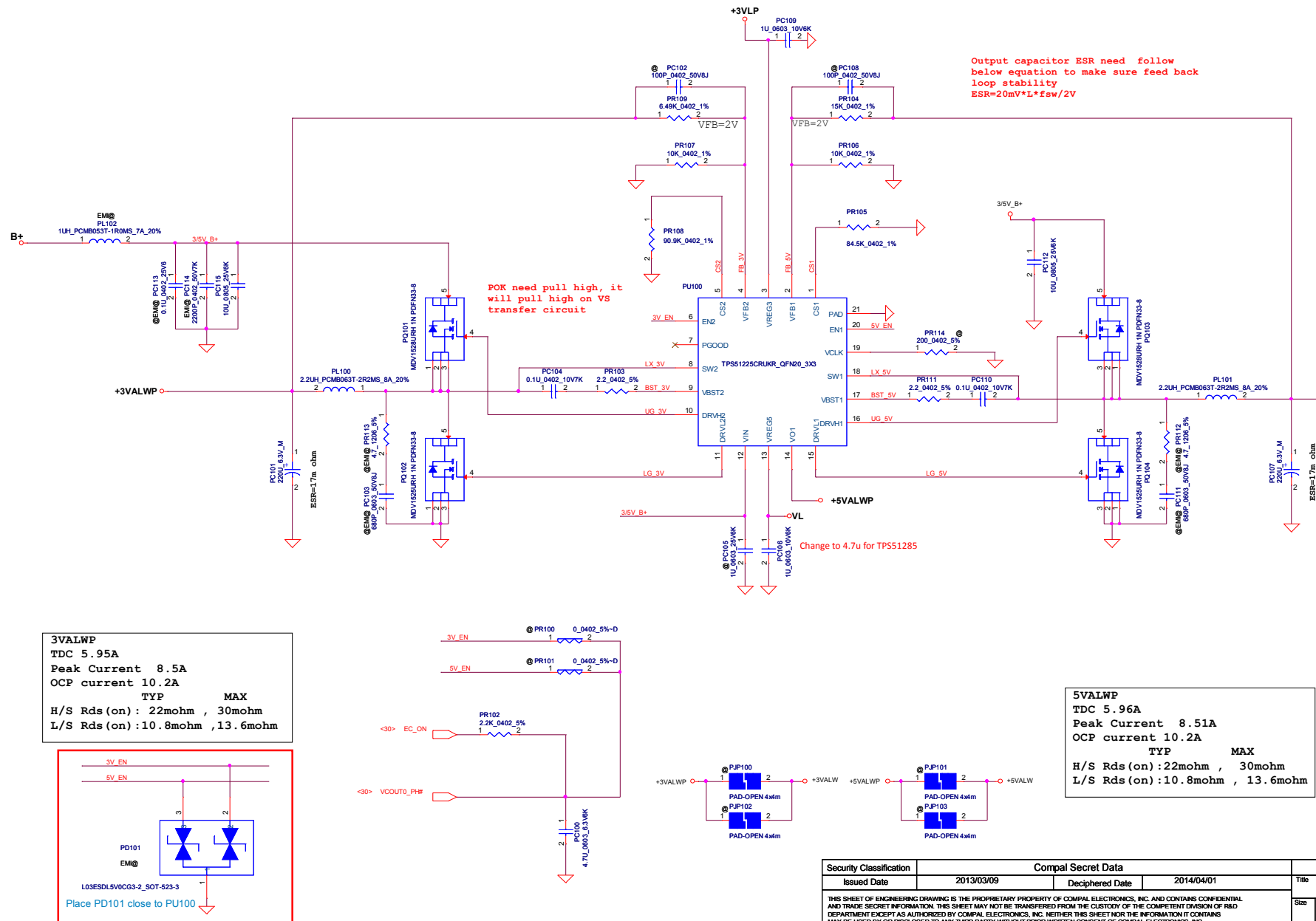


Other component (37.1)

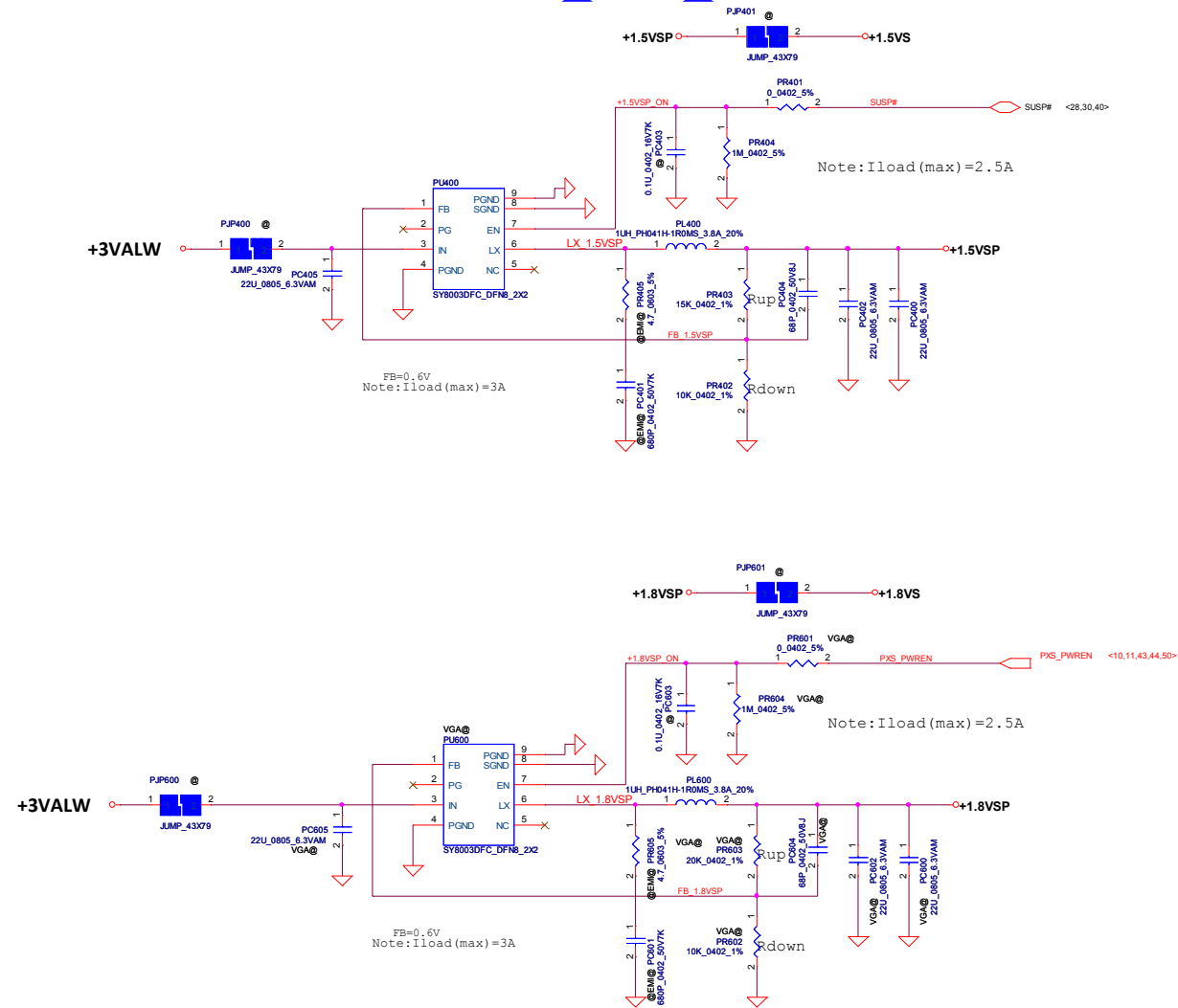


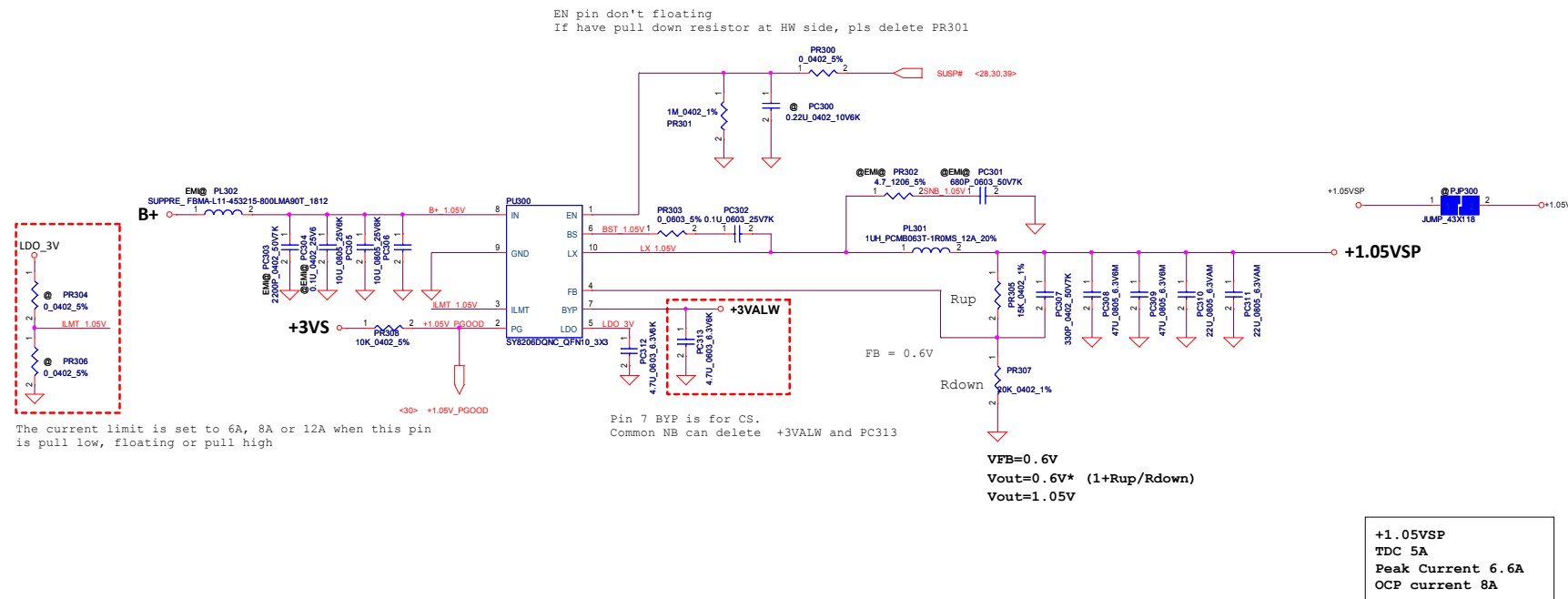
Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>PWR DCIN/BATT CONN/OTP</b>	
Issued Date	2013/03/09	Deciphered Date	2014/04/01	Title	
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					<b>LA-9981P</b>	0.2
Date:	Saturday, March 09, 2013	Sheet	38	of	55	



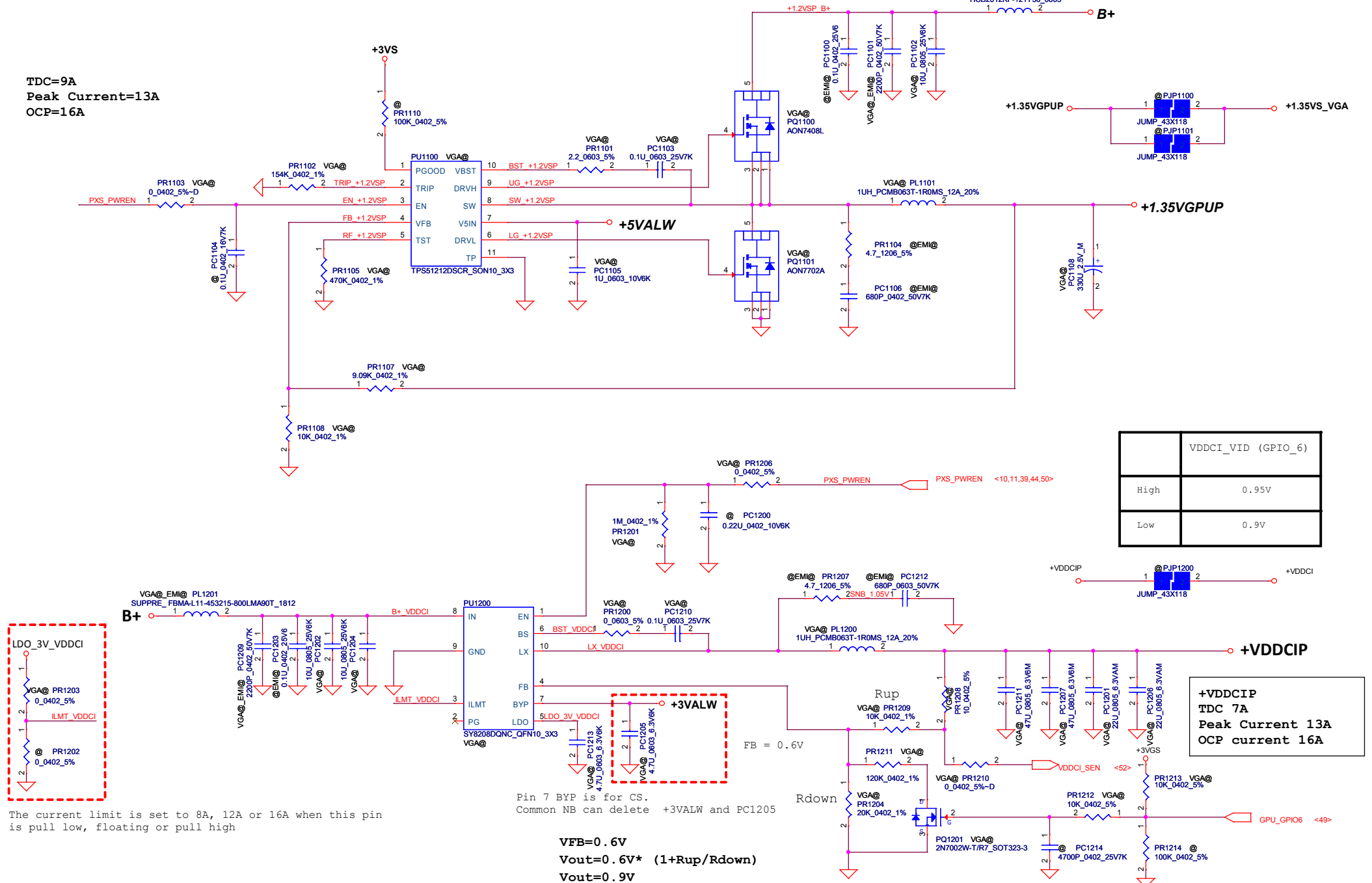








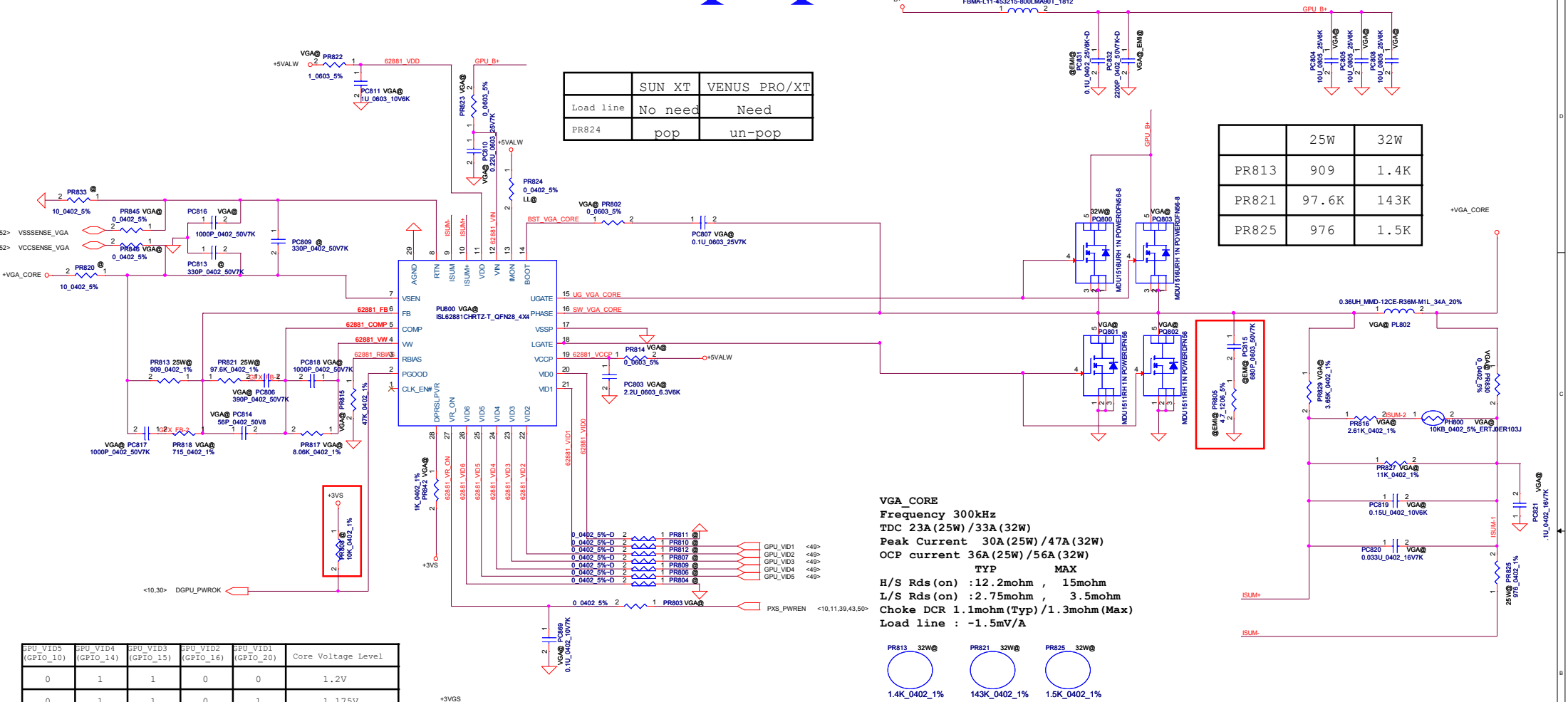
TDC=9A  
Peak Current=13A  
OCP=16A



	VDDCI_VID (GPIO_6)
High	0.95V
Low	0.9V

+VDDCIP  
TDC 7A  
Peak Current 13A  
OCP current 16A

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				Document Number
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				0.2
				Date
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				43 of 55



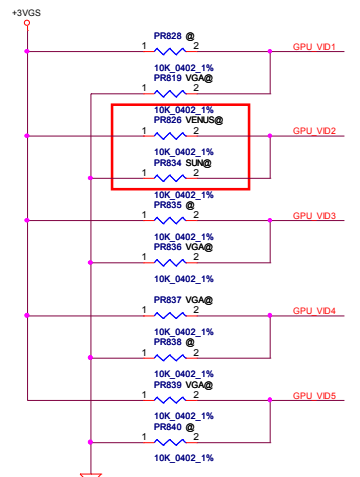
	SUN XT	VENUS PRO/XT
Load line	No need	Need
PR824	pop	un-pop

	25W	32W
PR813	909	1.4K
PR821	97.6K	143K
PR825	976	1.5K

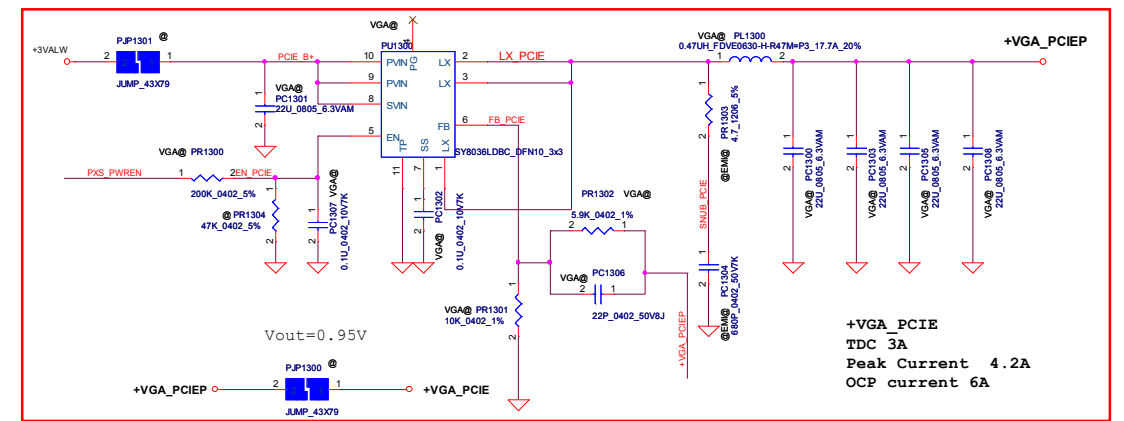
VGA\_CORE  
Frequency 300kHz  
TDC 23A (25W) / 33A (32W)  
Peak Current 30A (25W) / 47A (32W)  
OCP current 36A (25W) / 56A (32W)  
TYP MAX  
H/S Rds(on) : 12.2mohm , 15mohm  
L/S Rds(on) : 2.75mohm , 3.5mohm  
Choke DCR 1.1mohm (Typ) / 1.3mohm (Max)  
Load line : -1.5mV/A



SPU_VID5 (GPIO_10)	SPU_VID4 (GPIO_14)	SPU_VID3 (GPIO_15)	SPU_VID2 (GPIO_16)	SPU_VID1 (GPIO_20)	Core Voltage Level
0	1	1	0	0	1.2V
0	1	1	0	1	1.175V
0	1	1	1	0	1.15V
0	1	1	1	1	1.125V
1	0	0	0	0	1.1V
1	0	0	0	1	1.075V
1	0	0	1	0	1.05V
1	0	0	1	1	1.025V
1	0	1	0	0	1V
1	0	1	0	1	0.975V
1	0	1	1	0	0.95V
1	0	1	1	1	0.925V
1	1	0	0	0	0.9V
1	1	0	0	1	0.875V
1	1	0	1	0	0.85V
1	1	0	1	1	0.825V
1	1	1	0	0	0.8V
1	1	1	1	1	0.775V

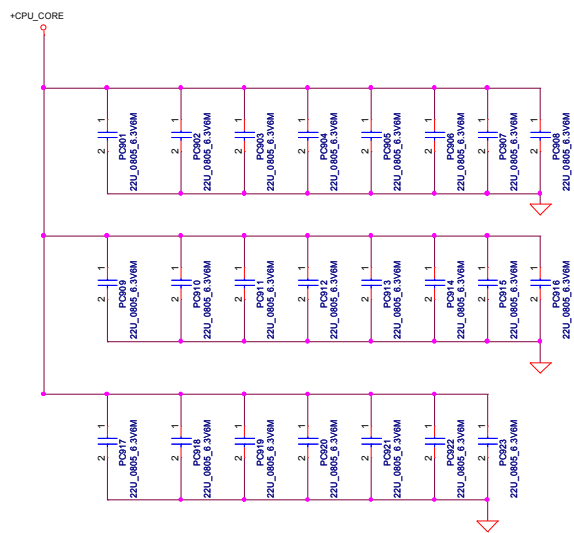


Initial voltage: 0.85V (Venus)  
0.9V (Sun)

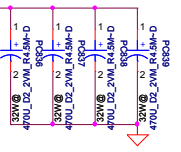
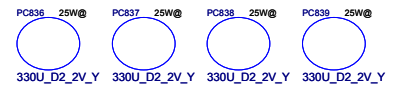
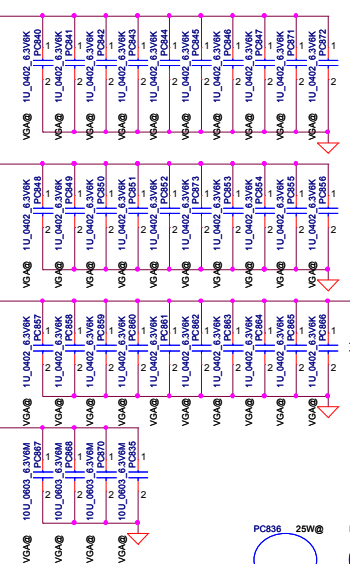


+VGA\_PCIE  
TDC 3A  
Peak Current 4.2A  
OCP current 6A

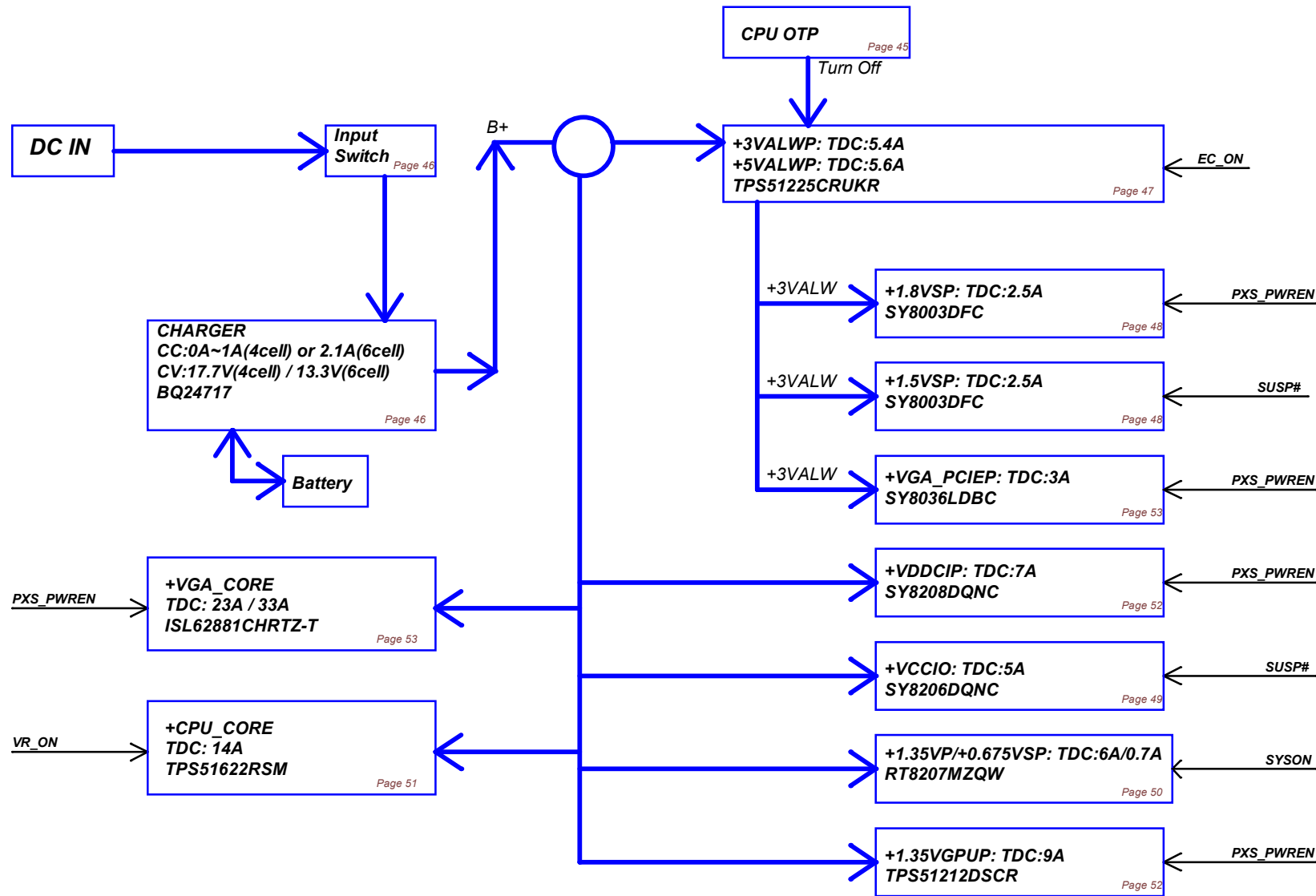
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+VGA\_CORE



## Power block

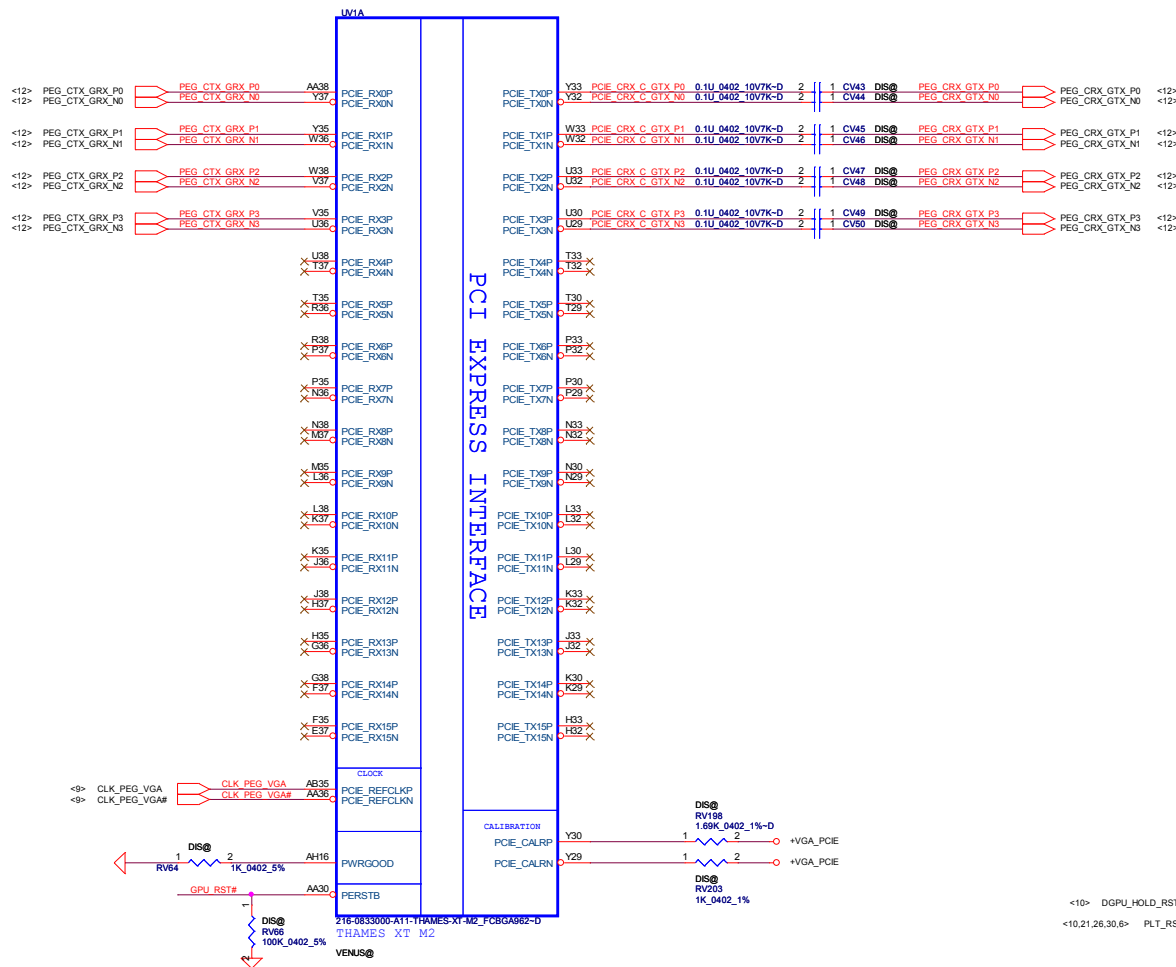


## Page 1

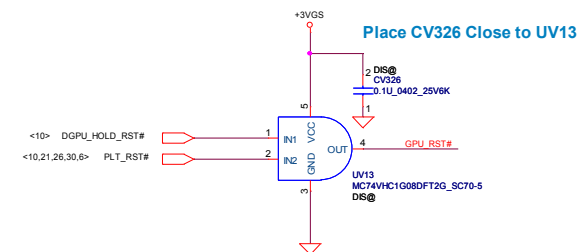
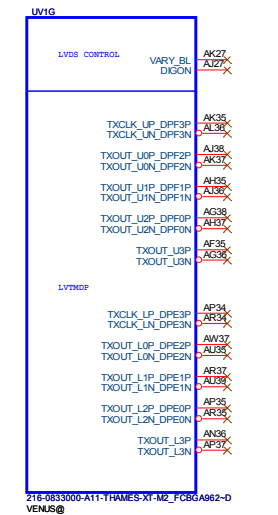
Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	45	CHARGER	13/01/30	Morris	adjust design parameter from vendor recommend	delete PD702 change PC712 to unpop change PQ704 to unpop change PC707 from 0.1uF_0402 to 1uF_0603 change PC720 from 0.1uF to 100pF change PC711 from 1000pF to 0.01uF change PQ705 from SB00000USD00 to SB00000WY00	0.2
2	50	VCORE	13/01/30	Morris	adjust design parameter from vendor recommend	change PC509 from 0.1uF to 1000pF change PR529 from 3.83K to 5.76K change PR504 from 523K to 499K	0.2
3	44	DCIN/BATT CONN/OTP	13/01/30	Morris	change from ESD request	change PD1 from SC300002E00 to SC300001G00	0.2
4	46	3.3VALWP/5VALWP	13/02/01	Morris	add ESD diode from ESD request	add PD101(SCA00002A00)	0.2
5	50	VCORE	13/02/21	Morris	adjust design parameter from fine tune result	change PR501 from 422K to 523K change PR503 from 56K to 75K	0.2
6	52	VGA_CORE/PCIE	13/02/21	Morris	unpop from EE request	unpop PR808	0.2
7	52	VGA_CORE/PCIE	13/03/05	Morris	adjust output voltage from vender request	unpop PR826 and pop PR834 (only for Sun XT)	0.2

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## GFX PCIE LANE REVERSAL



## LVDS Interface

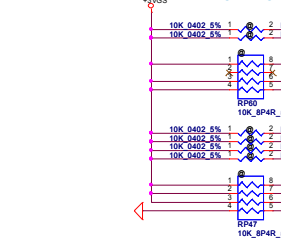




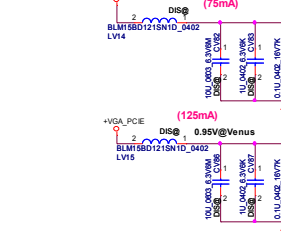
SUN GPIO N.C. PIN

- GPIO1 GPU\_GPIO1
- GPIO2 GPU\_GPIO2
- GPIO7 N.C
- GPIO11 GPU\_GPIO11
- GPIO12 GPU\_GPIO12
- GPIO13 GPU\_GPIO13
- GPIO14 N.C
- GPIO18 N.C

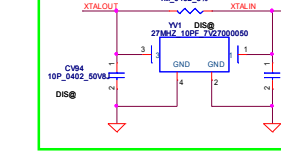
STRAPS



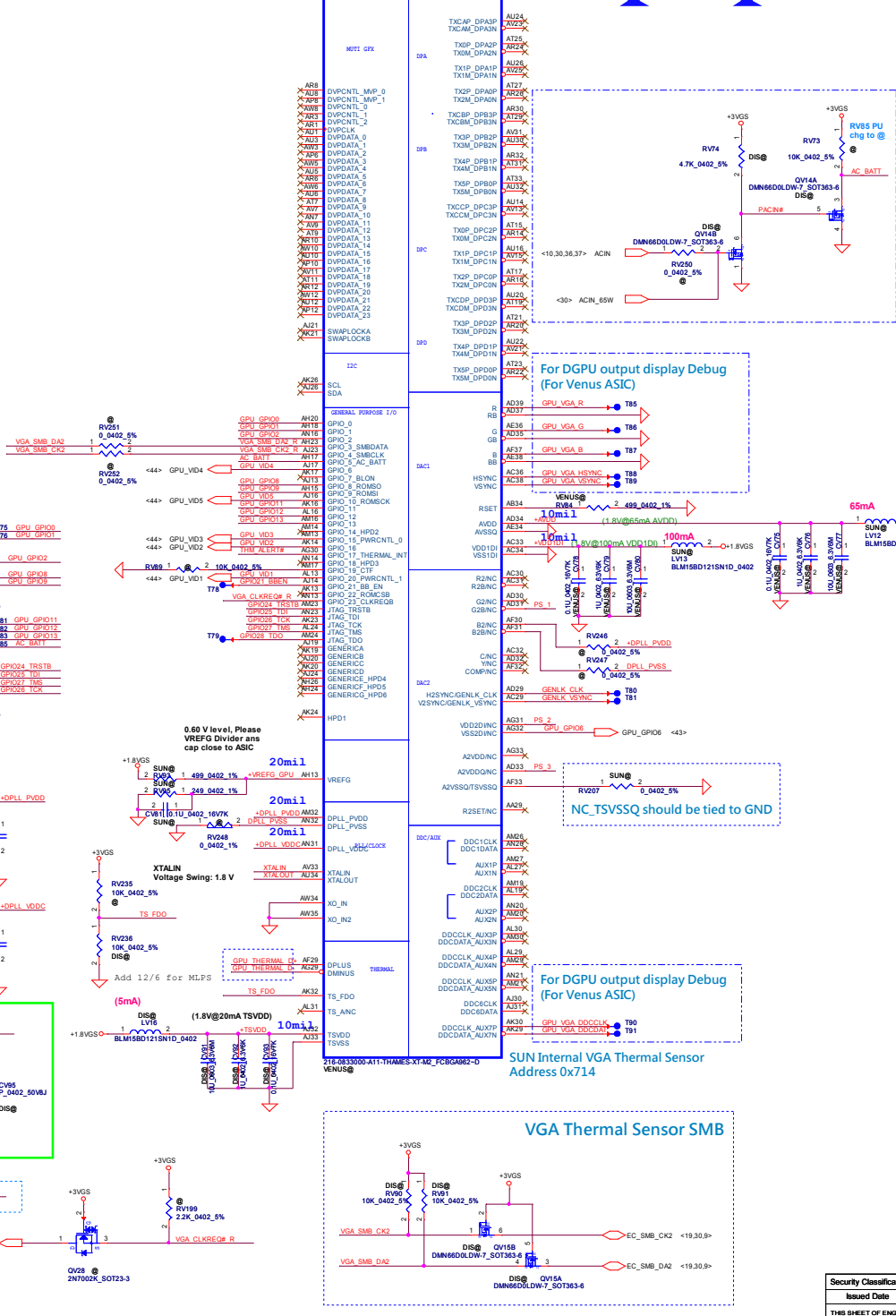
0.80 V level, Please VREFS Divider and cap close to ASIC



For GCLK

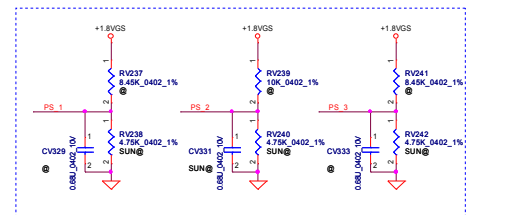


VGA Thermal Sensor SMB



RECOMMENDED SETTINGS			
0= DO NOT INSTALL RESISTOR 1= INSTALL 10K RESISTOR X= DESIGN DEPENDANT NA= NOT APPLICABLE			
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCI FULL TX OUTPUT SWING 0: 50% swing 1: full swing	X
TX_DEEMPH_EN	GPIO1	PCI TRANSMITTER DE-EMPHASIS 0: disable 1: enable	X
RSVD	GPIO2	Advertises PCIe speed when compliance test	0
RSVD	GPIO8	RESERVED	0
BF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	X
ROMCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XXX
WP_DEVICE_STRAP_ENA	V2SYN	IGNORE WP DEVICE STRAPS	0
RSVD	H2SYN		0
RSVD	GENERIC		0
AUD[1]	HSYN	AUD[1] AUD[0] 0: No audio function 1: Audio for DisplayPort and HDMI if dongle is detected	11
AUD[0]	VSYN	1: Audio for DisplayPort only 1: Audio for both DisplayPort and HDMI	
AMD RESERVED CONFIGURATION STRAPS ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET			
GPIO21	H2SYN	GENERIC	GPIO2 GPIO8

TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)

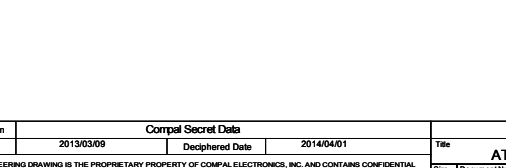


Vendor	RV241	RV242	Bits [3:1]
1280X16 (1GB) DDR3	Hynix 2Gb SA00006H40L(R1)	NC	4.75K 000
1280X16 (1GB) DDR3	Samsung 2Gb SA00006H41L(R3)	8.45K 2K	001
1280X16 (1GB) DDR3	Samsung 2Gb SA00005SH0L(R1)	4.75K NC	111
1280X16 (1GB) DDR3	Micron 2Gb SA00005X80L(R1)		
1280X16 (1GB) DDR3	Micron 2Gb SA00005XB1L(R3)		

For DGPU output display Debug (For Venus ASIC)

SUN Internal VGA Thermal Sensor Address 0x714

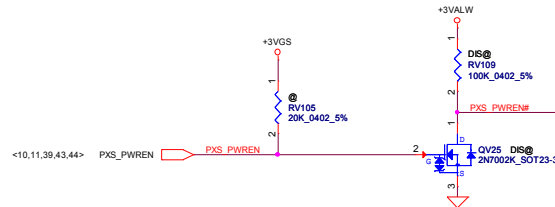
VGA Thermal Sensor SMB



PX\_MODE=1 for Normal Operation  
PX\_MODE=0 for BACO mode to shut down power rails except VDDR3, PCIE\_VDDC and 1.8V rail

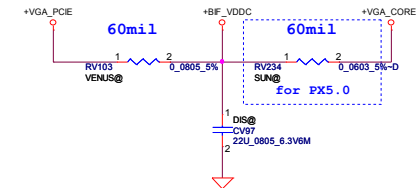
**Note:**

PX4.0 +VGA\_CORE, VDDCI, +1.5VGS ON  
PX4.0 +3VGS, +1.0VGS, +1.8VGS OFF  
PX5.0 +3VGS, +VGA\_CORE, VDDCI, +1.5VGV, +1.0VGS, +1.8VGS OFF

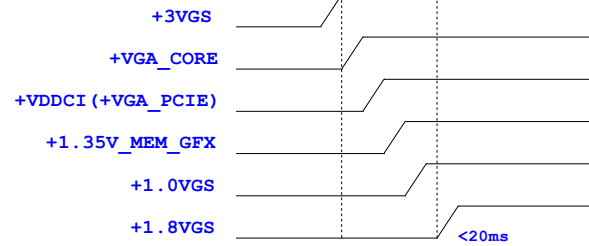


for PX4.0 and PX5.0

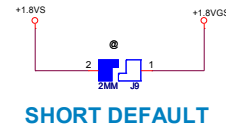
Switch circuits in BACO desings for Thames/Seymour only  
55mA@1.0V, in BACO mode



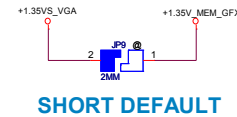
**Power sequence of Sun XT, Venus Pro, Venus XT**



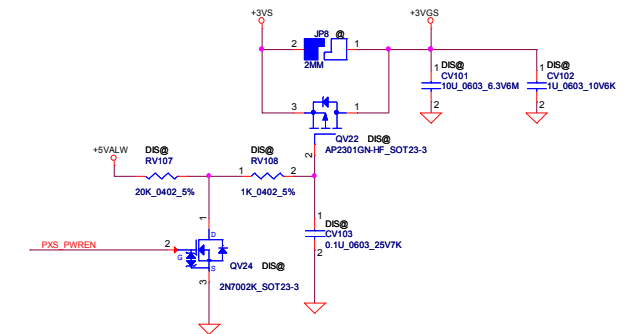
**+1.8VS TO +1.8VGS**



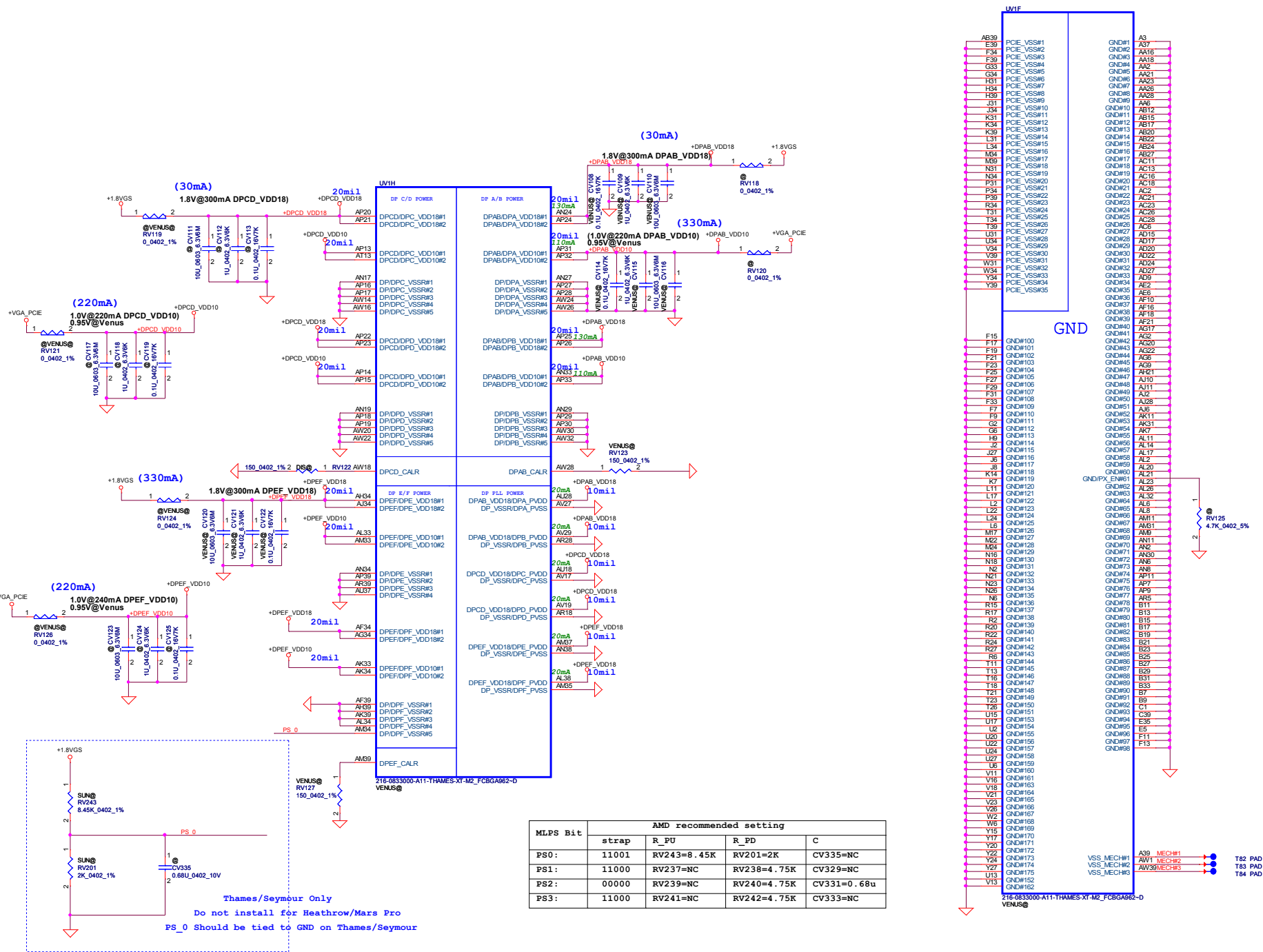
**+1.35VS\_VGA TO +1.35V\_MEM\_GFX**



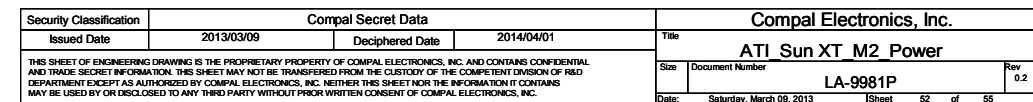
**+3VS TO +3VGS**

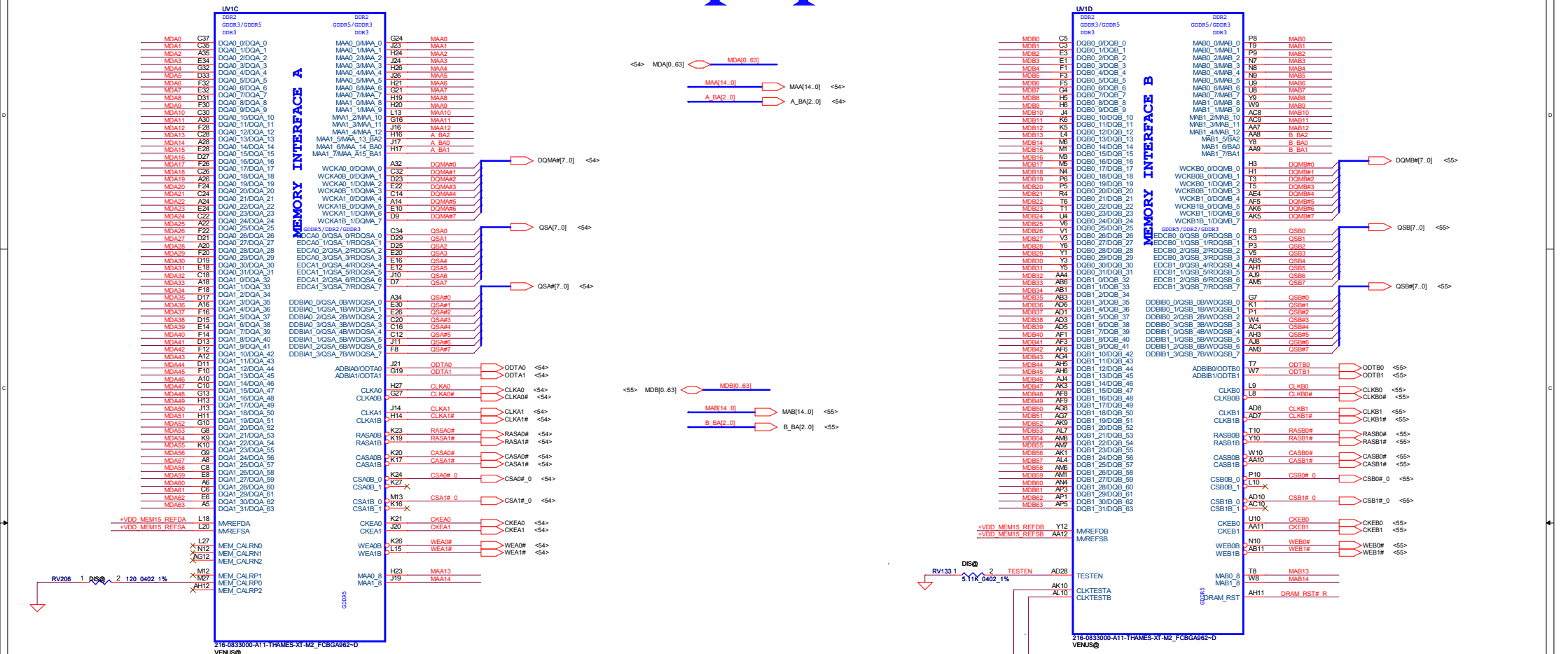


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/03/09	Deciphered Date	2014/04/01	Title	ATI Sun XT M2 BACO POWER
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				Sheet	50 of 55

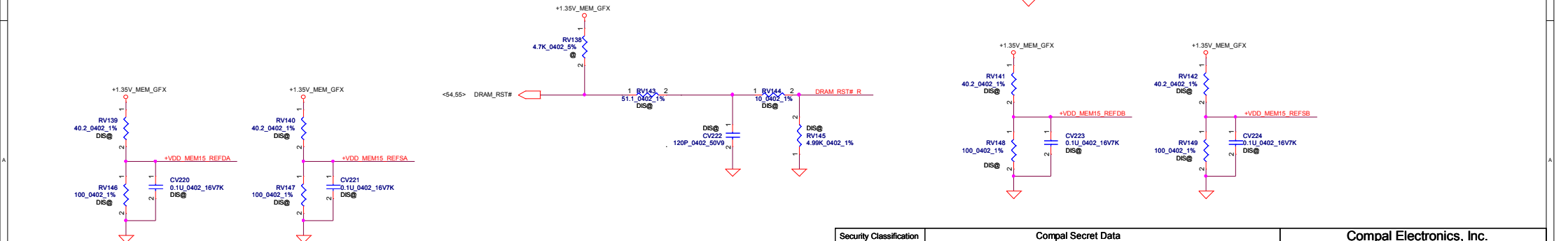


MLPS Bit	AMD recommended setting			
	strap	R_PU	R_PD	C
PS0:	11001	RV243=8.45K	RV201=2K	CV335=NC
PS1:	11000	RV237=NC	RV238=4.75K	CV329=NC
PS2:	00000	RV239=NC	RV240=4.75K	CV331=0.68u
PS3:	11000	RV241=NC	RV242=4.75K	CV333=NC

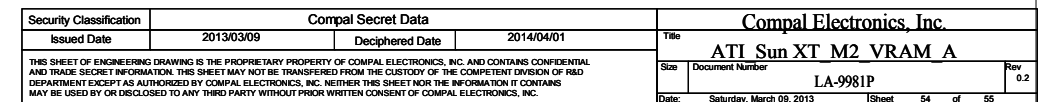




This basic topology should be used for DRAM\_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and | Cap values will depend on the DRAM load and will have to be calculated for different Memory, DRAM load and board to pass Reset Signal Spec. Place all these components very close to GPU (Within 25mm) and keep all component close to each other (within 5mm) except Rser2



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/03/09	Deciphered Date	2014/04/01	Title	ATI Sun XT M2 MEM IF
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CHANNEL B : 256MB DDR3

