

**DJ1 Calpella UMA Schematics Document**

**Arrandale**

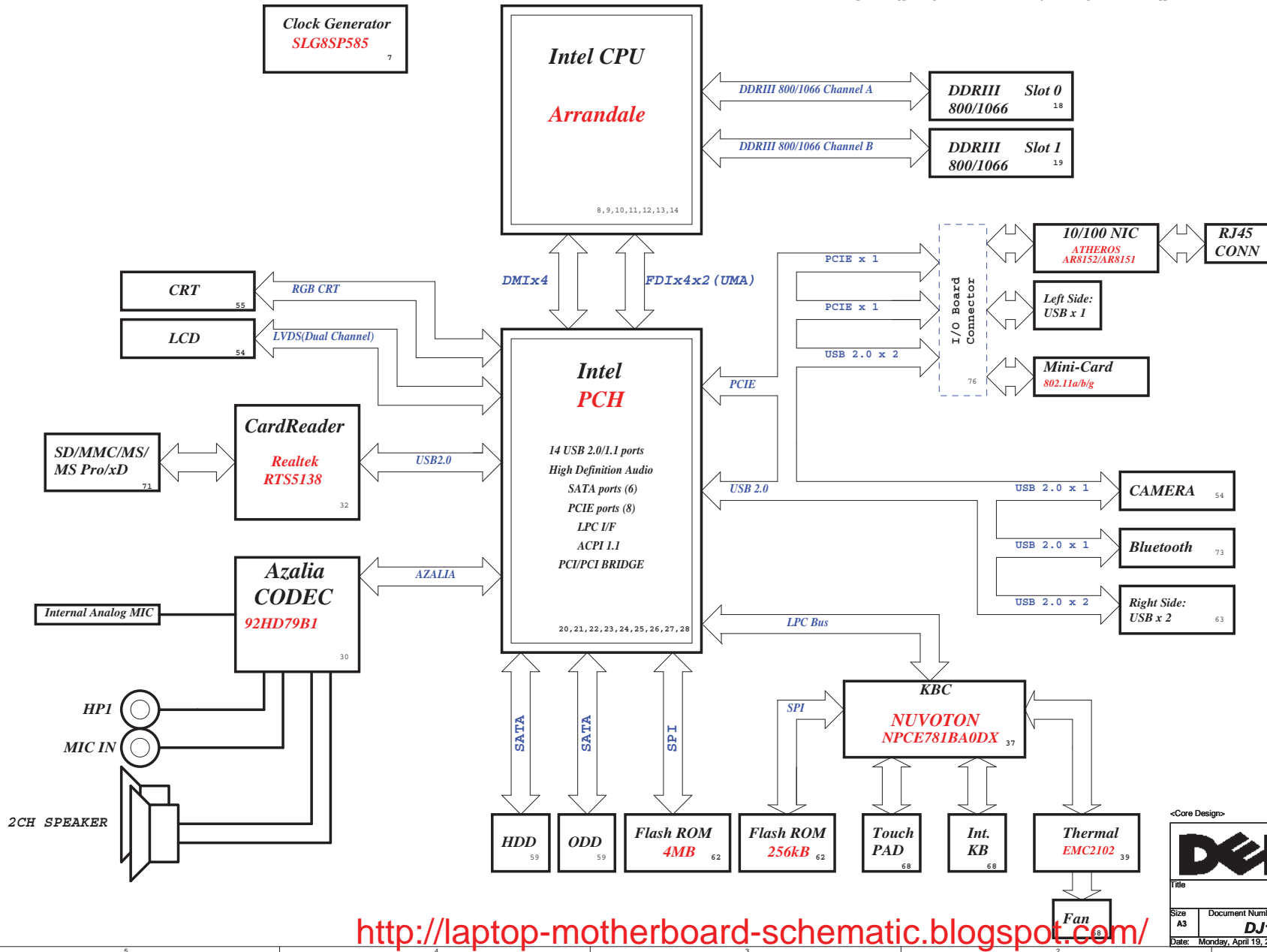
**Intel PCH**

**2010-04-23**

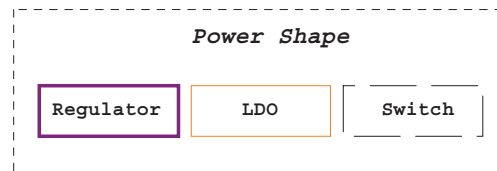
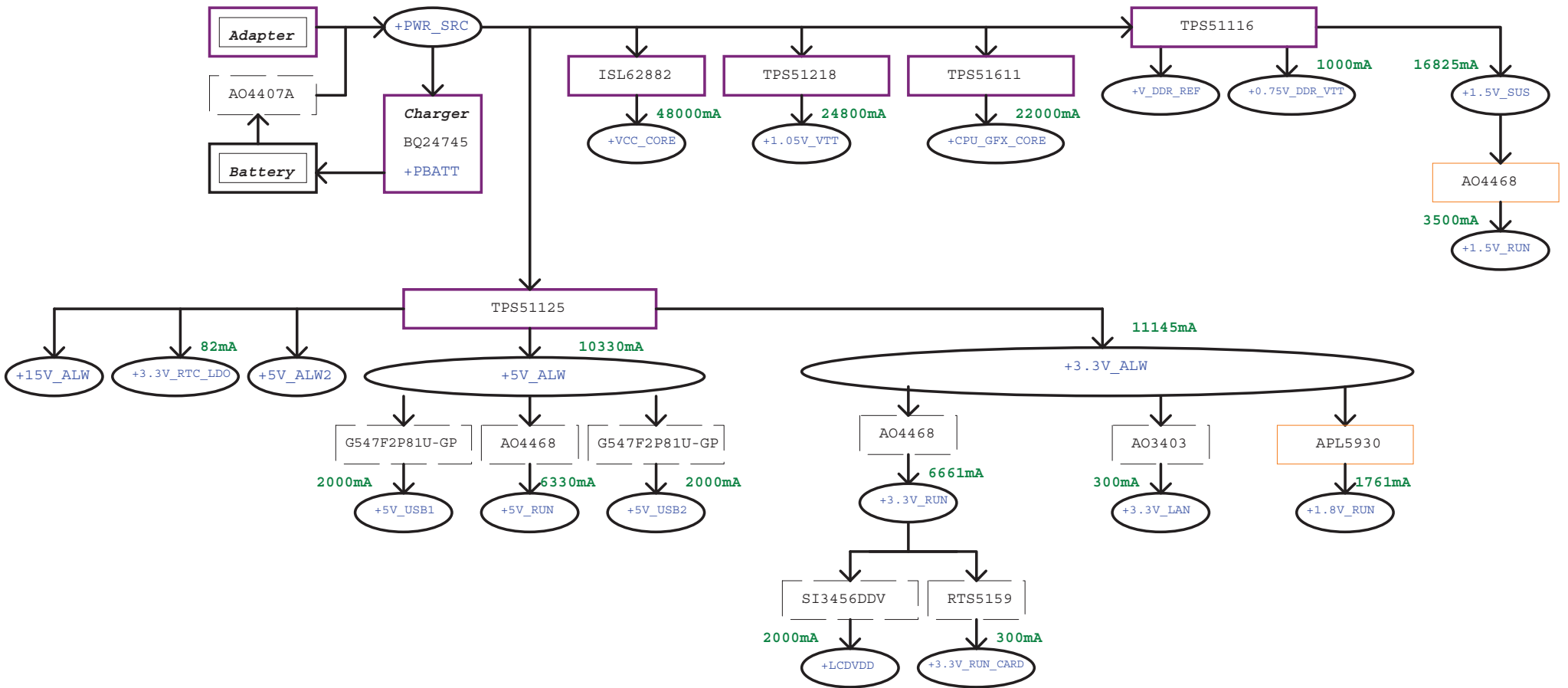
**REV : X01**

*DY : Nopop Component*

Project code : 91.4EK01.001  
PCB P/N : 48.4EK19.0SB  
Revision : 10212-SB

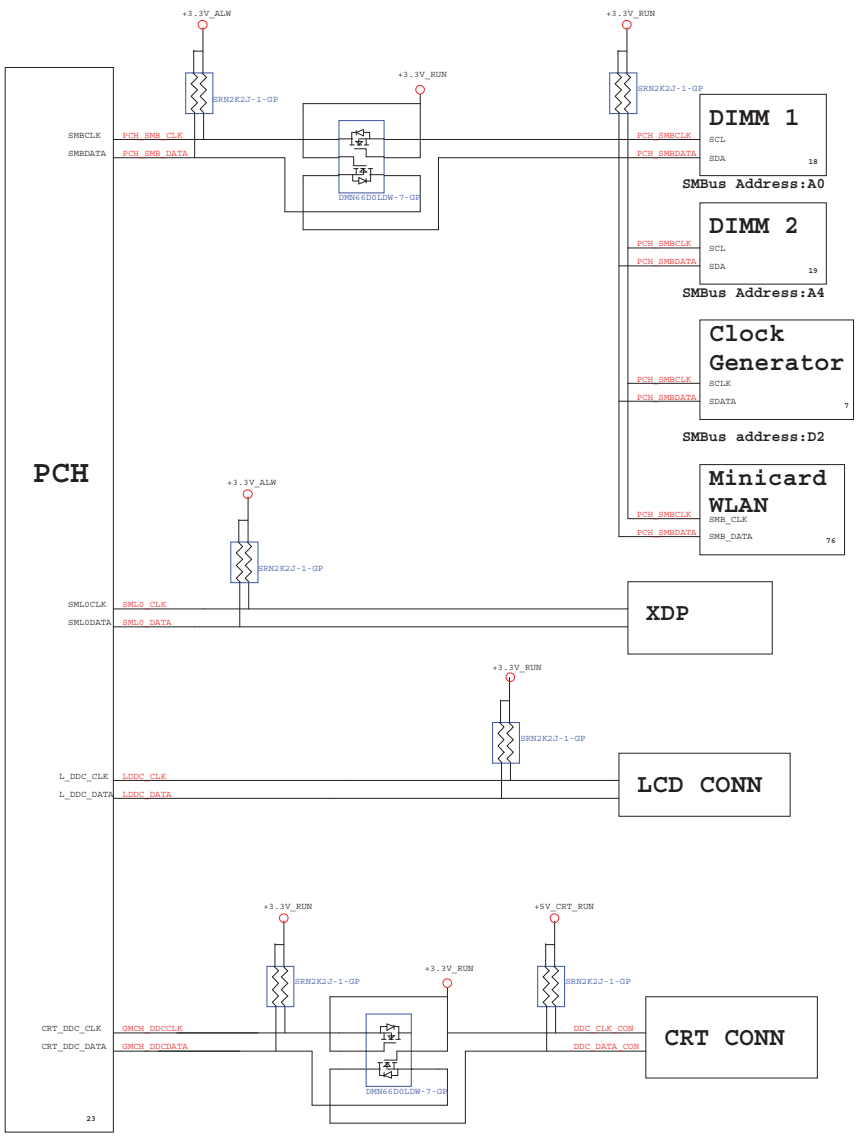


CPU DC/DC	
ISL62882 47,48	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE
SYSTEM DC/DC	
TPS51218 49	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VTT
SYSTEM DC/DC	
RT8205BGQW 46	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +5V_ALW +3.3V_ALW +15V_ALW
SYSTEM DC/DC	
RT8207GQW 50	
INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS +0.75V_DDR_VTT +V_DDR_REF
SYSTEM DC/DC	
TPS51611 53	
INPUTS	OUTPUTS
+PWR_SRC	+CPU_GFX_CORE
MAXIM CHARGER	
BQ24745	
INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC
SYSTEM DC/DC	
APL5930 51	
INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN
SYSTEM DC/DC	
Switches 42	
INPUTS	OUTPUTS
+1.5V_SUS +5V_ALW +3.3V_ALW	+1.5V_RUN +5V_RUN +3.3V_RUN
PCB LAYER	
L1: Top	
L2: VCC	
L3: Signal	
L4: Signal	
L5: GND	
L6: Bottom	

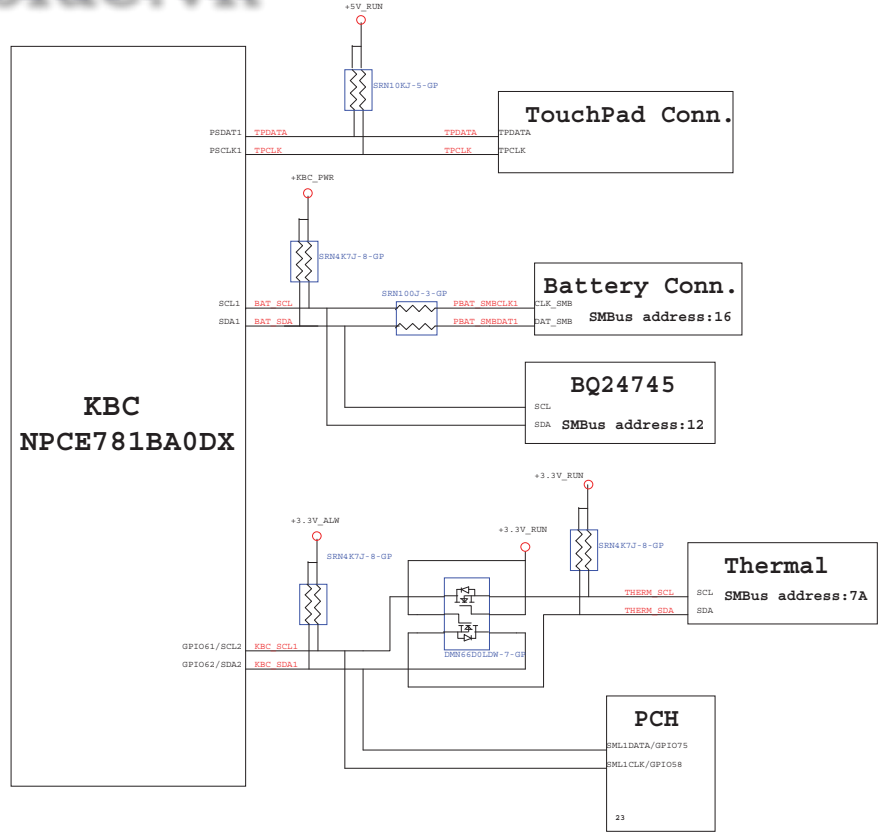


PCH SMBus Block Diagram

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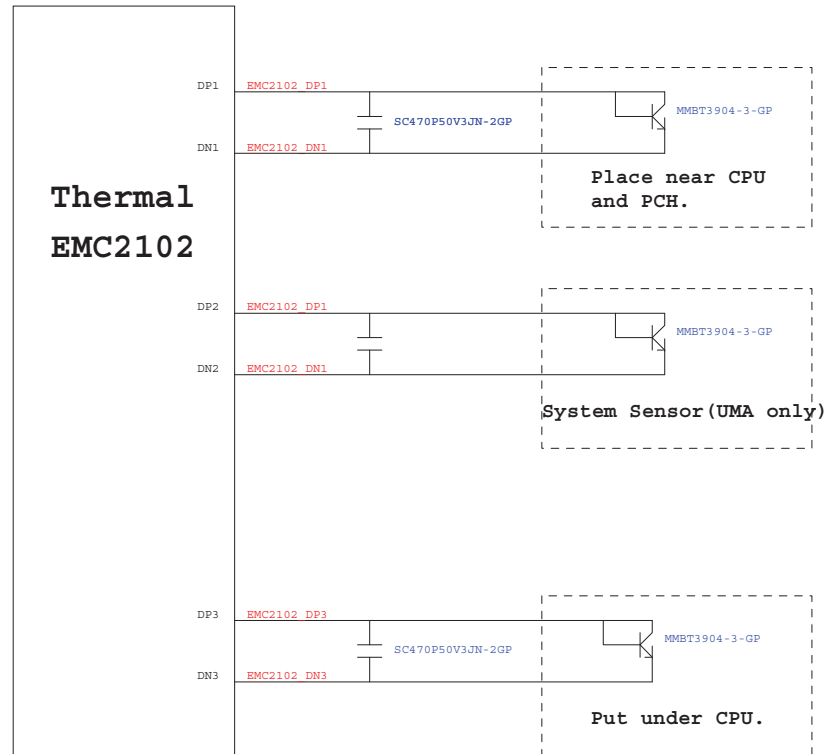


KBC SMBus Block Diagram

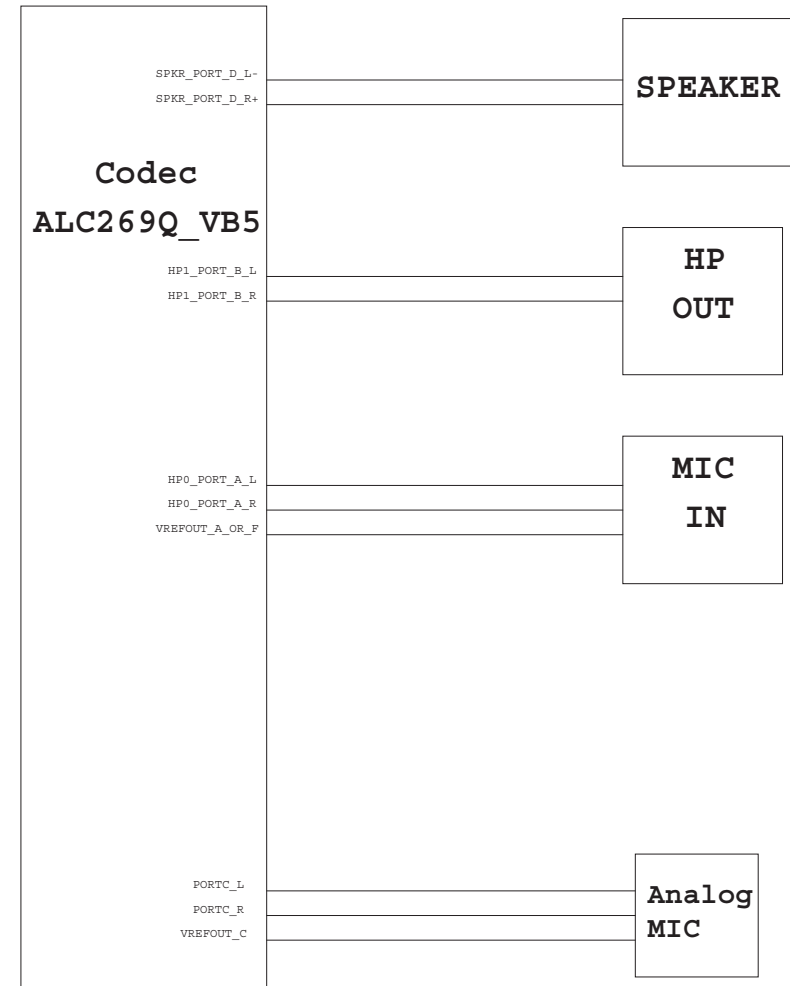


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## Thermal Block Diagram



## Audio Block Diagram



## PCB Strapping

Calpella Schematic Checklist Rev.0\_7

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-k- 10-k weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap Mode (Connect to ground with 4.7-k weak pull-down resistor).
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled
GNT0#, GNT1#/GPIO51	Default (SPI): Left both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Connect GNT1# to ground with 1-k pull-down resistor. Leave GNT0# Floating. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-k pull-down resistor.
GNT2#/GPIO53	Default - Internal pull-up. Low (0) = Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	Default: Do not pull low. Disable ME in Manufacturing Mode: Connect to ground with 1-k pull-down resistor.
SPI_MOSI	Enable iTPM: Connect to Vcc3_3 with 8.2-k weak pull- up resistor. Disable iTPM: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to Vcc3_3 with 8.2-k weak pull-up resistor. Disable Danbury: Connect to ground with 4.7-k weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD DOCK_EN# /GPIO[33]	Low (0): Flash Descriptor Security will be overridden. High (1) : Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

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## PCB Schematic Strapping

Calpella Schematic Checklist Rev.0\_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	Reserved - Temporarily used for early Clarksfield samples.	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor Note: Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

## PCIE Routing

LANE2	MiniCard WLAN
LANE3	LAN

## USB Table

USB	
Pair	Device
0	USB0 (I/O Board)
1	X
2	USB2
3	USB3
4	X
5	WLAN (I/O Board)
6	X
7	X
8	X
9	BLUETOOTH
10	CARD READER
11	CAMERA
12	X
13	X

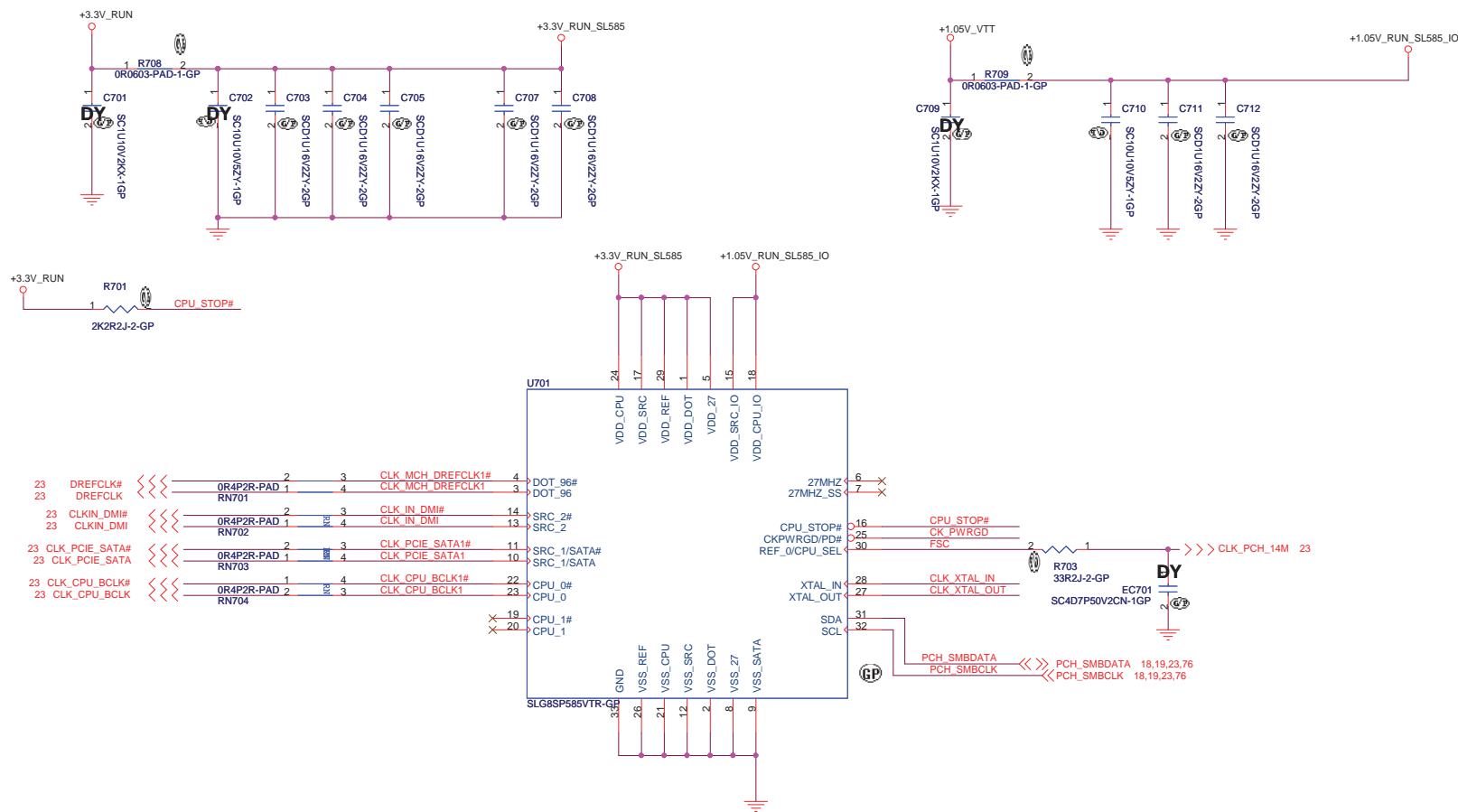
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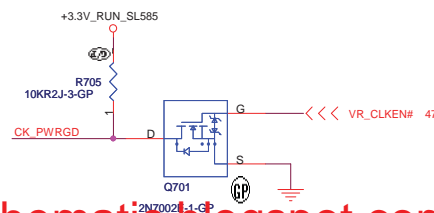
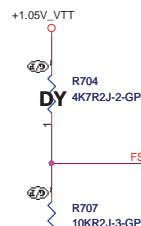
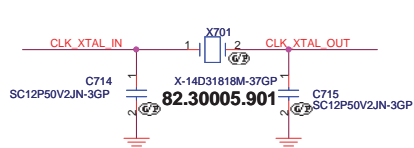
<b>DELL</b>		<b>Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
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SSID = CLOCK

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FSC	0	1
SPEED	133MHz (Default)	100MHz



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3rd : 62.10055.321

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**CPU1A**

**DMI**

**PCI EXPRESS - - GRAPHICS**

**PCI EXPRESS - - AUDIO**

**AUBURNDALE**

**EXP. RBIAS**

**PEG\_IROMP\_R**

**R801**

**R802**

**4909R2F-GP**

**22** **DMI\_PTX\_CRXN0** **>>>** **A24** **DMI\_RX0#**

**22** **DMI\_PTX\_CRXN1** **>>>** **C23** **DMI\_RX1#**

**22** **DMI\_PTX\_CRXN2** **>>>** **B22** **DMI\_RX2#**

**22** **DMI\_PTX\_CRXN3** **>>>** **A21** **DMI\_RX3#**

**22** **DMI\_PTX\_CRXP0** **>>>** **B24** **DMI\_RX0**

**22** **DMI\_PTX\_CRXP1** **>>>** **D23** **DMI\_RX1**

**22** **DMI\_PTX\_CRXP2** **>>>** **B23** **DMI\_RX2**

**22** **DMI\_PTX\_CRXP3** **>>>** **A22** **DMI\_RX3**

**22** **DMI\_CTX\_PRXN0** **<<<** **D24** **DMI\_TX0#**

**22** **DMI\_CTX\_PRXN1** **<<<** **G24** **DMI\_TX1#**

**22** **DMI\_CTX\_PRXN2** **<<<** **F23** **DMI\_TX2#**

**22** **DMI\_CTX\_PRXN3** **<<<** **H23** **DMI\_TX3#**

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**22** **DMI\_CTX\_PRPX1** **<<<** **F24** **DMI\_TX1**

**22** **DMI\_CTX\_PRPX2** **<<<** **E23** **DMI\_TX2**

**22** **DMI\_CTX\_PRPX3** **<<<** **G23** **DMI\_TX3**

**22** **FDI\_TXN0** **<<<** **E22** **FDI\_TX0#**

**22** **FDI\_TXN1** **<<<** **D21** **FDI\_TX1#**

**22** **FDI\_TXN2** **<<<** **D19** **FDI\_TX2#**

**22** **FDI\_TXN3** **<<<** **D18** **FDI\_TX3#**

**22** **FDI\_TXN4** **<<<** **G21** **FDI\_TX4#**

**22** **FDI\_TXN5** **<<<** **E19** **FDI\_TX5#**

**22** **FDI\_TXN6** **<<<** **F21** **FDI\_TX6#**

**22** **FDI\_TXN7** **<<<** **G18** **FDI\_TX7#**

**22** **FDI\_TXP0** **<<<** **D22** **FDI\_TX0**

**22** **FDI\_TXP1** **<<<** **C21** **FDI\_TX1**

**22** **FDI\_TXP2** **<<<** **D20** **FDI\_TX2**

**22** **FDI\_TXP3** **<<<** **C18** **FDI\_TX3**

**22** **FDI\_TXP4** **<<<** **G22** **FDI\_TX4**

**22** **FDI\_TXP5** **<<<** **E20** **FDI\_TX5**

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**22** **FDI\_TXP7** **<<<** **G19** **FDI\_TX7**

**22** **FDI\_FSYNC0** **<<<** **F17** **FDI\_FSYNC0**

**22** **FDI\_FSYNC1** **<<<** **E17** **FDI\_FSYNC1**

**22** **FDI\_INT** **<<<** **C17** **FDI\_INT**

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**22** **FDI\_LSYNC1** **<<<** **D17** **FDI\_LSYNC1**

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**PEG\_RCOMP0** **B27** **PEG\_RBIAS** **A25**

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**PEG\_RX2#** **J33** **PEG\_RX3#** **G35**

**PEG\_RX4#** **G32** **PEG\_RX5#** **F34**

**PEG\_RX6#** **F31** **PEG\_RX7#** **D35**

**PEG\_RX8#** **E33** **PEG\_RX9#** **C33**

**PEG\_RX10#** **D32** **PEG\_RX11#** **B32**

**PEG\_RX12#** **C31** **PEG\_RX13#** **B28**

**PEG\_RX14#** **B30** **PEG\_RX15#** **A31**

**PEG\_RX0** **J35** **PEG\_RX1** **H34**

**PEG\_RX2** **H33** **PEG\_RX3** **F35**

**PEG\_RX4** **G33** **PEG\_RX5** **F32**

**PEG\_RX6** **D34** **PEG\_RX7** **F33**

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**PEG\_RX12** **A28** **PEG\_RX13** **B29**

**PEG\_RX14** **A30** **PEG\_RX15** **L33**

**PEG\_TX0#** **M35** **PEG\_TX1#** **M33**

**PEG\_TX2#** **M30** **PEG\_TX3#** **L31**

**PEG\_TX4#** **K32** **PEG\_TX5#** **M29**

**PEG\_TX6#** **J31** **PEG\_TX7#** **K29**

**PEG\_TX8#** **H30** **PEG\_TX9#** **H29**

**PEG\_TX10#** **F29** **PEG\_TX11#** **E28**

**PEG\_TX12#** **D29** **PEG\_TX13#** **D27**

**PEG\_TX14#** **C26** **PEG\_TX15#** **L34**

**PEG\_TX0** **M34** **PEG\_TX1** **L30**

**PEG\_TX2** **M31** **PEG\_TX3** **K31**

**PEG\_TX4** **M28** **PEG\_TX5** **H31**

**PEG\_TX6** **K28** **PEG\_TX7** **G30**

**PEG\_TX8** **G29** **PEG\_TX9** **F28**

**PEG\_TX10** **E27** **PEG\_TX11** **D28**

**PEG\_TX12** **C27** **PEG\_TX13** **C25**

**PEG\_TX14** **C25** **PEG\_TX15** **C25**

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Title	Author	Year	Journal	Volume	Page
...	...	...	...	...	...

**CPU (PCIe/DMI/FDI)**

Size

Document Number
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**X01**

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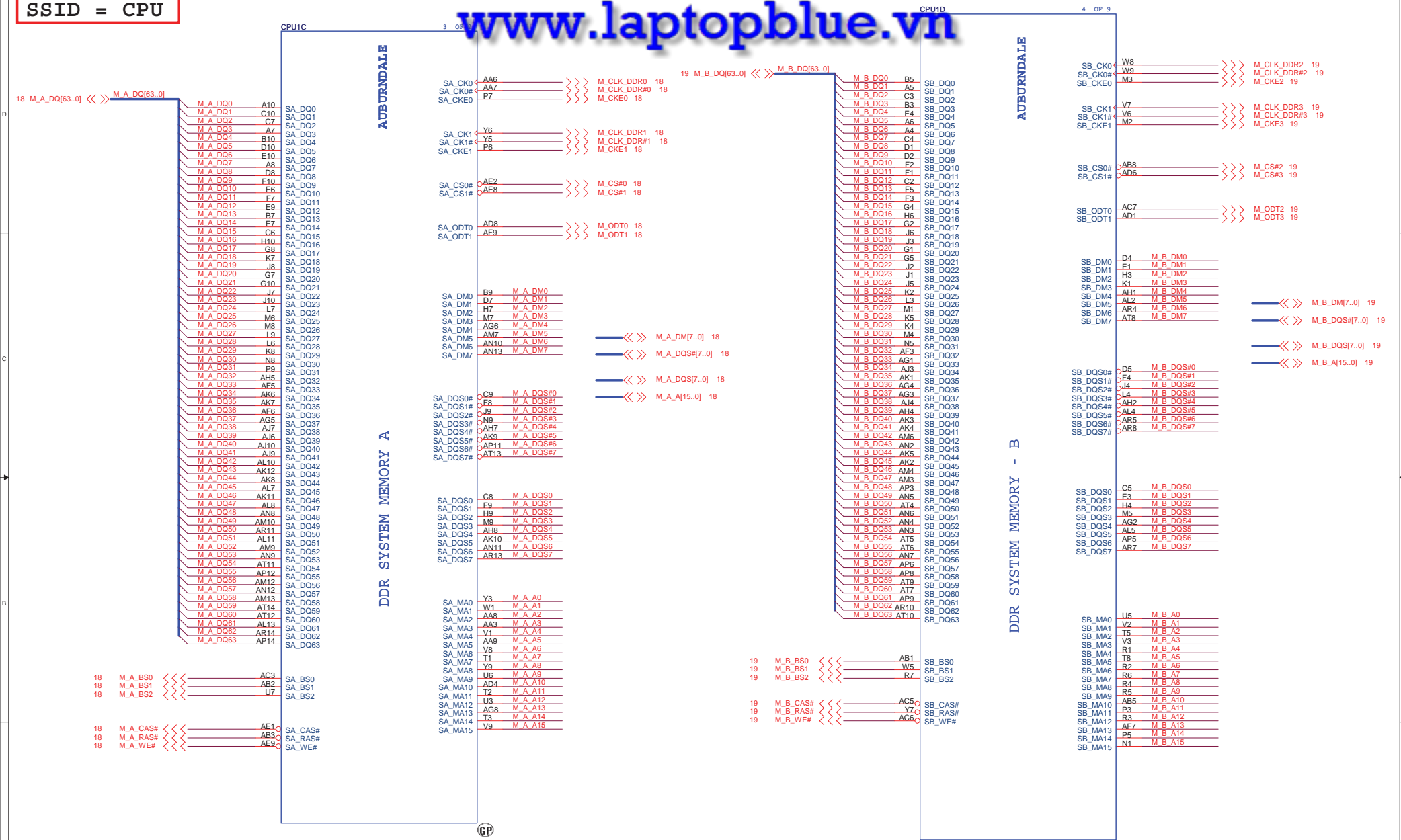
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SSID = CPU

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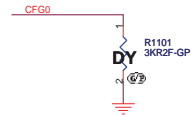
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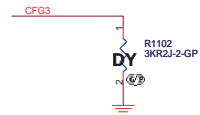
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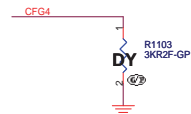
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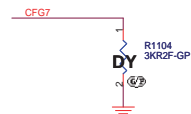
PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled



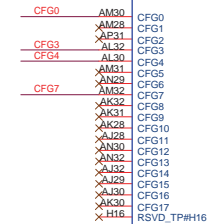
CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...



CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port



CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor.  Note: Only temporary for early CFD sample (rPGA/BGA) (For details please refer to the WW33 Mo/W and sighting report). For a common M/B design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.



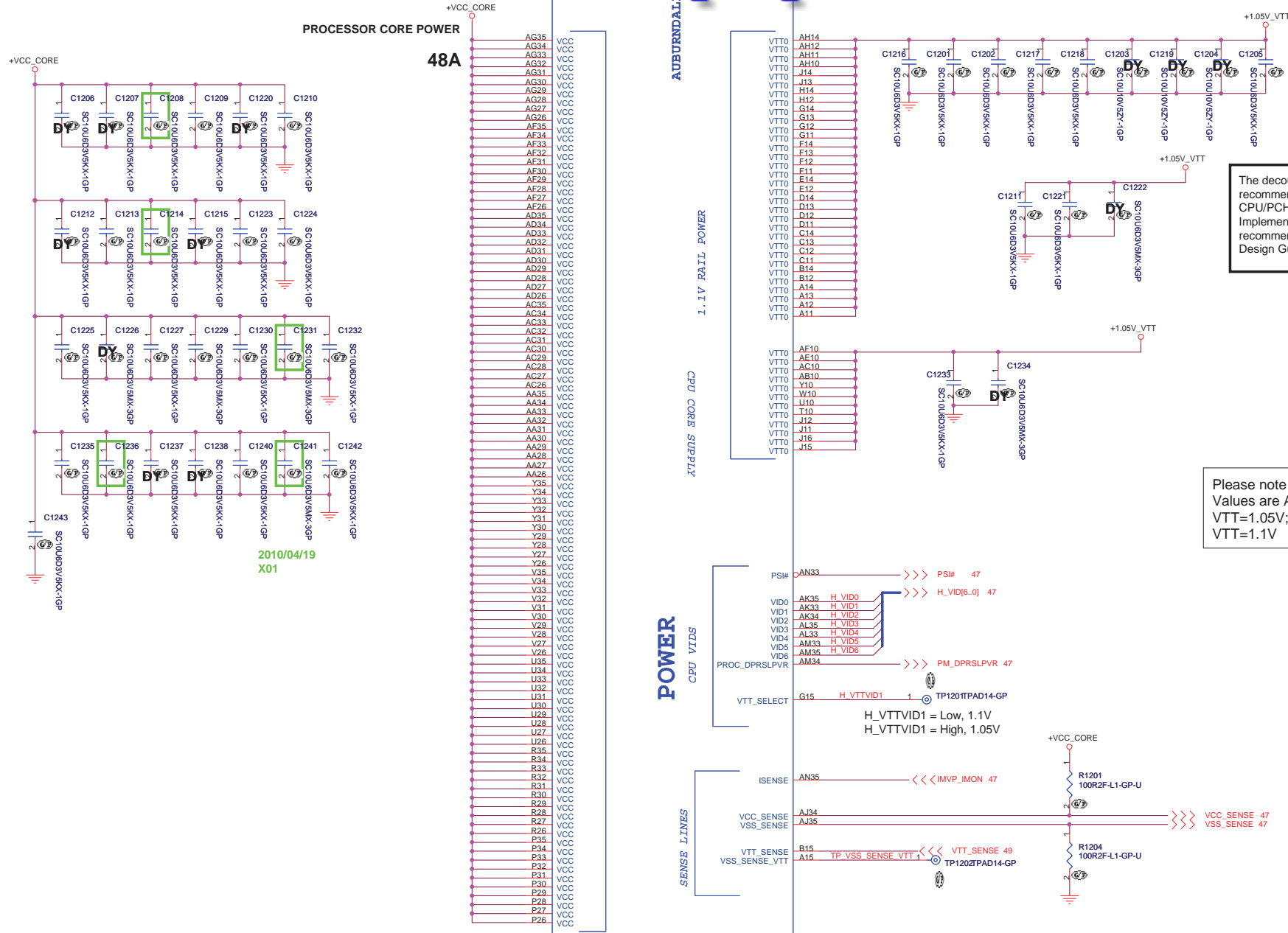
VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.

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The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail Values are Auburndale  
VTT=1.05V; Clarksfield  
VTT=1.1V

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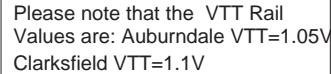
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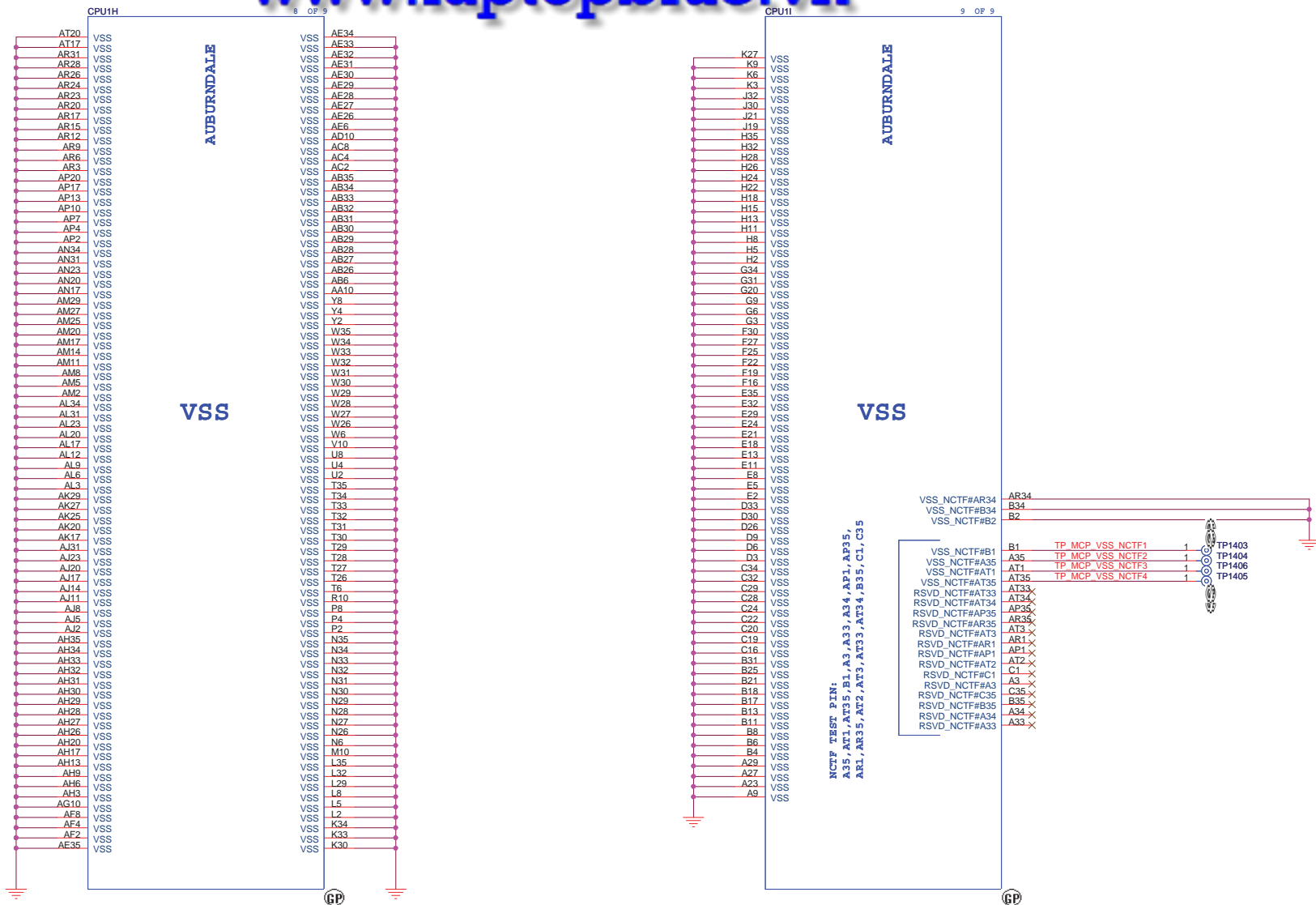
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Title			
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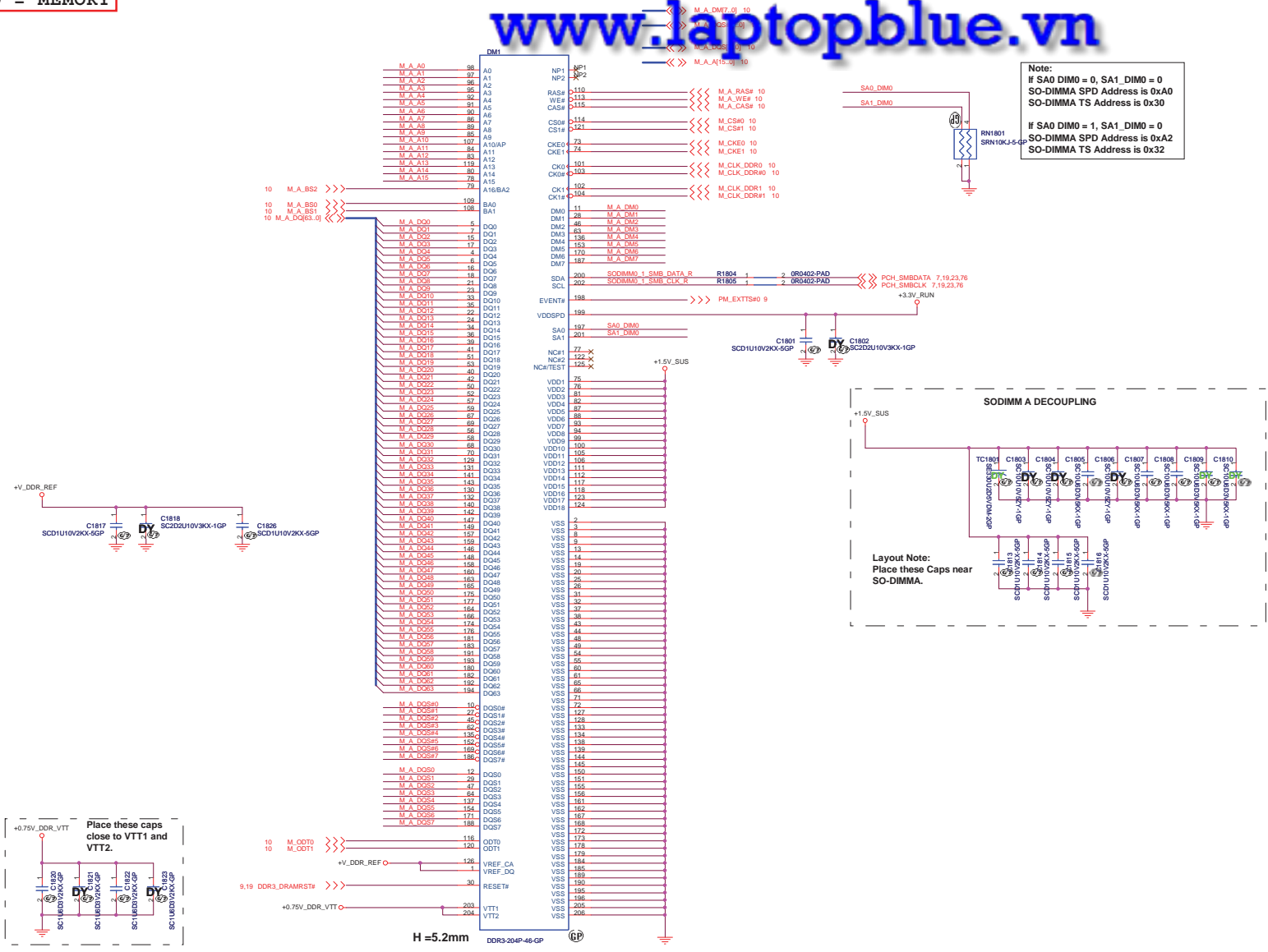
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SSID = MEMORY

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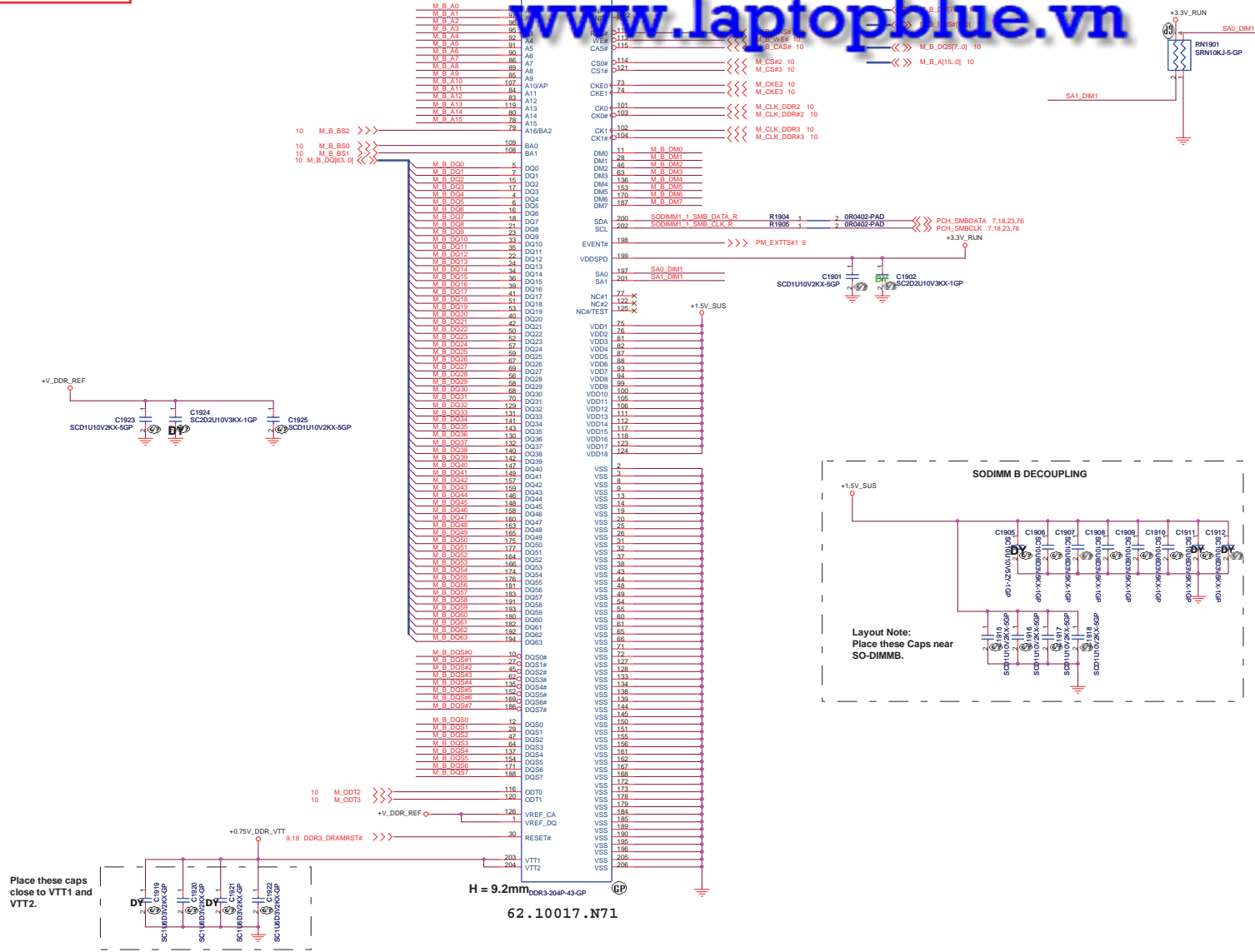


Note:  
If SA0\_DIM0 = 0, SA1\_DIM0 = 0  
SO-DIMMA SPD Address is 0xA0  
SO-DIMMA TS Address is 0x30  
  
If SA0\_DIM0 = 1, SA1\_DIM0 = 0  
SO-DIMMA SPD Address is 0xA2  
SO-DIMMA TS Address is 0x32

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SSID = MEMORY

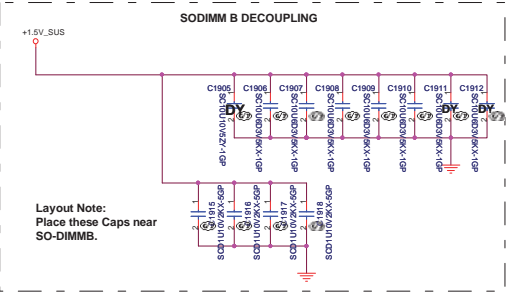
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Place these caps close to VTT1 and VTT2.

Note:  
SO-DIMMB SPD Address is 0xA4  
SO-DIMMB TS Address is 0x34

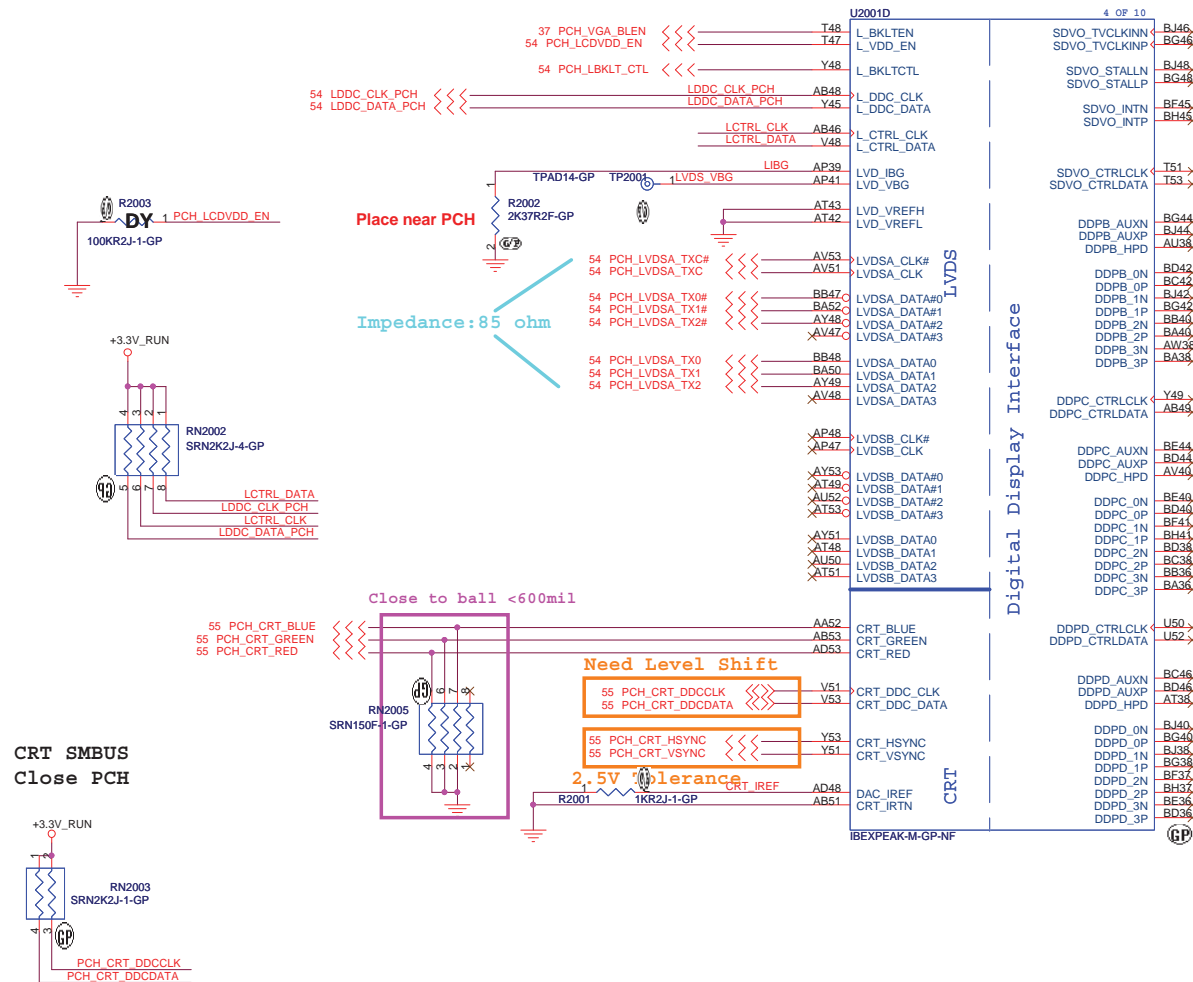
SO-DIMMB is placed farther from the Processor than SO-DIMMA



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SSID = PCH

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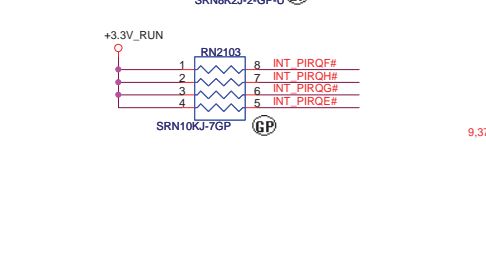
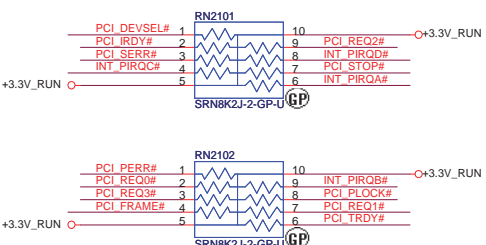


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Title		
PCH (LVDS/CRT/DDI)		
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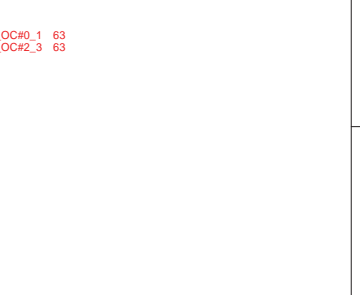
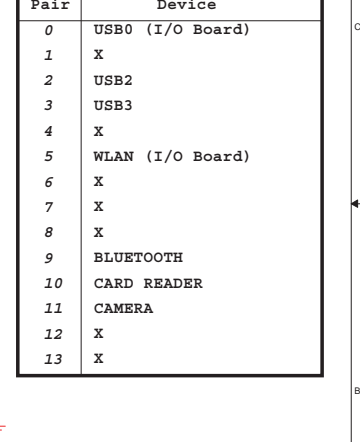
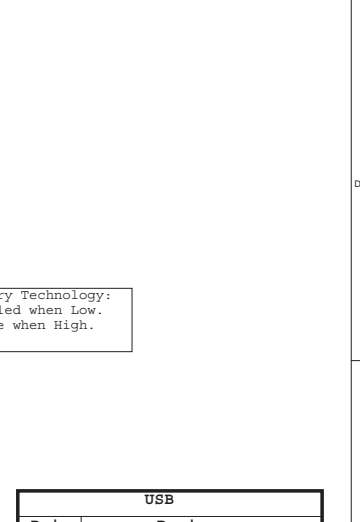
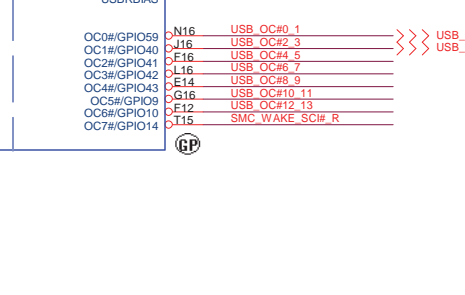
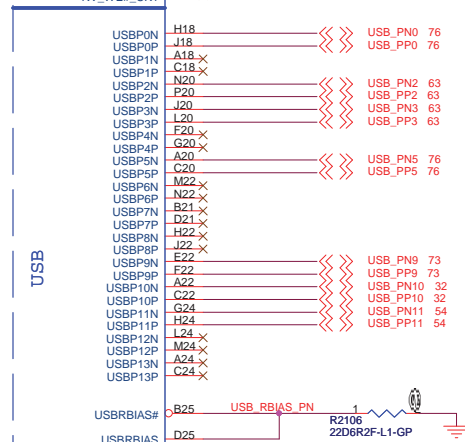
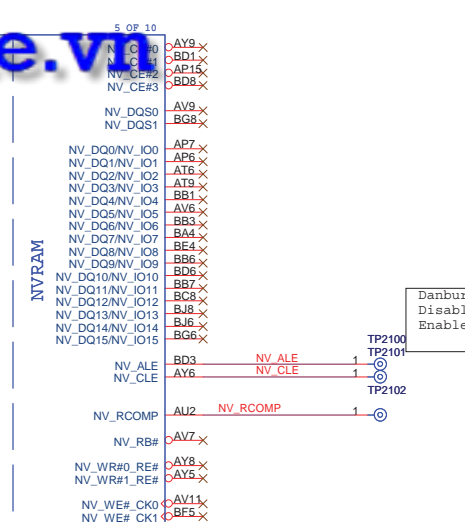
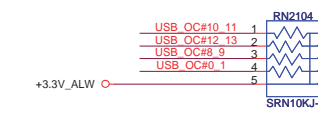
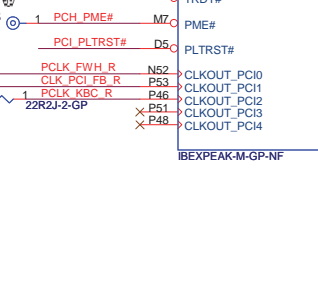
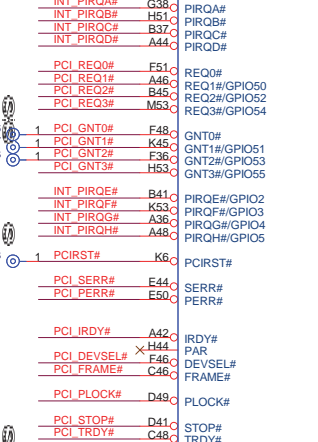
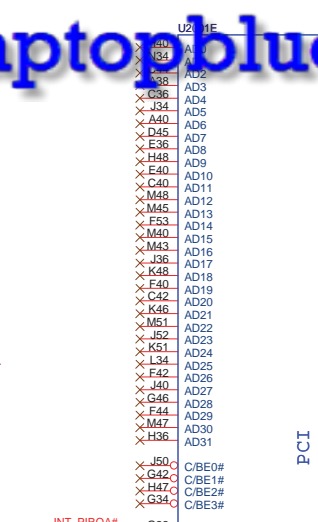
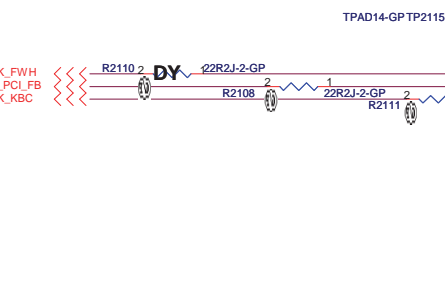
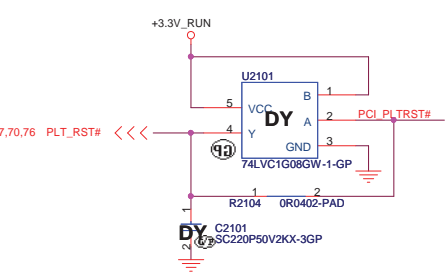
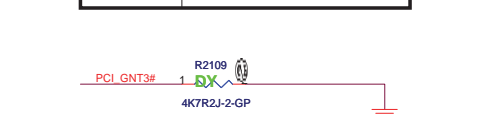
SSID = PCH  
www.laptopblue.vn



BOOT BIOS Strap		
PCI_GNT#1	PCI_GNT#0	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI (Default)



A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default



<Core Design>

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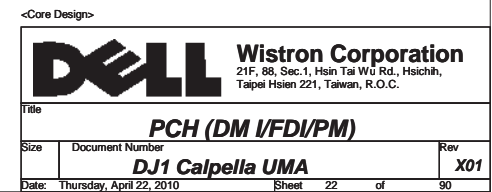
Title: **PCH (PCI/USB/NVRAM)**

Size: Document Number: **DJ1 Calpella UMA** Rev: **X01**

Date: Thursday, April 22, 2010 Sheet: 21 of 90

<http://laptop-motherboard-schematic.blogspot.com/>

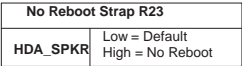
www.laptopblue.vn




<http://laptop-motherboard-schematic.blogspot.com/>

[www.laptopblue.vn](http://www.laptopblue.vn)





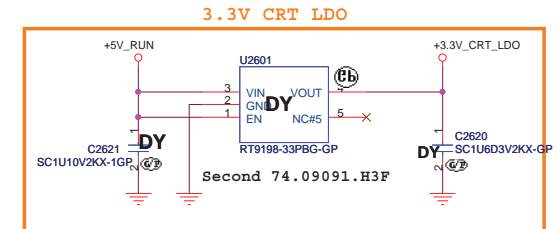
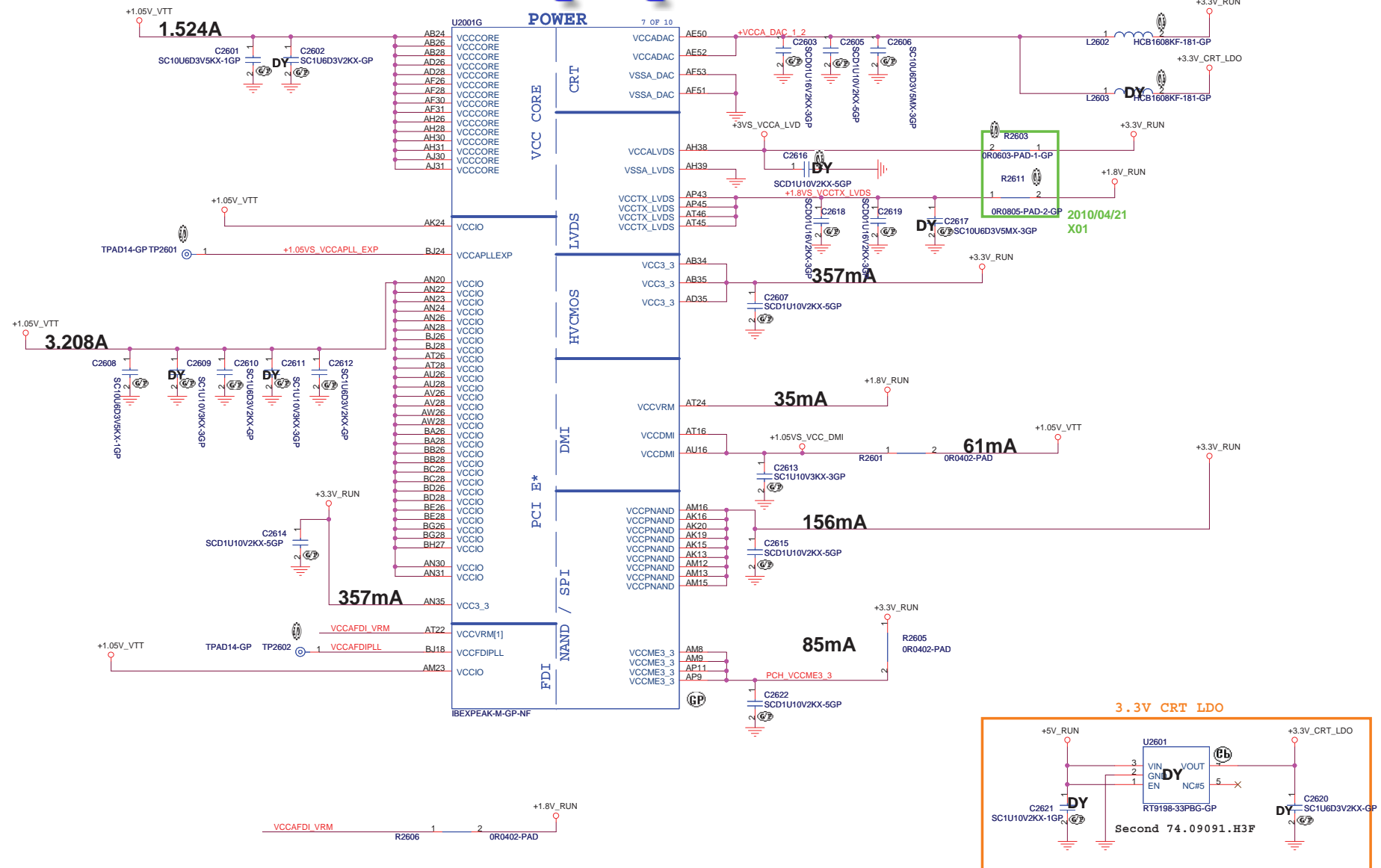
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Title			
<b><i>PCH (SPI/RTC/LPC/SATA/IHDA)</i></b>			
Size	Document Number	Rev	
	<b><i>DJ1 Calpella UMA</i></b>	<b><i>X01</i></b>	
Date:	Thursday, April 22, 2010	Sheet	24 of 90





SSID = PCH

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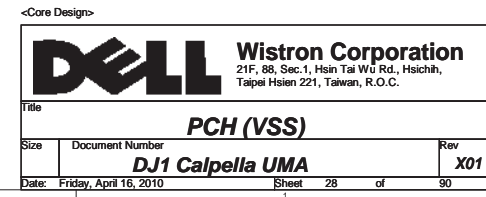
Title: **PCH (POWER1)**

Size	Document Number	Rev
	<b>DJ1 Calpella UMA</b>	<b>X01</b>

Date: Wednesday, April 21, 2010 Sheet 26 of 90

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Taipei Hsien 221, Taiwan, R.O.C.

Title

**Reserved**

Size  
A3

Document Number

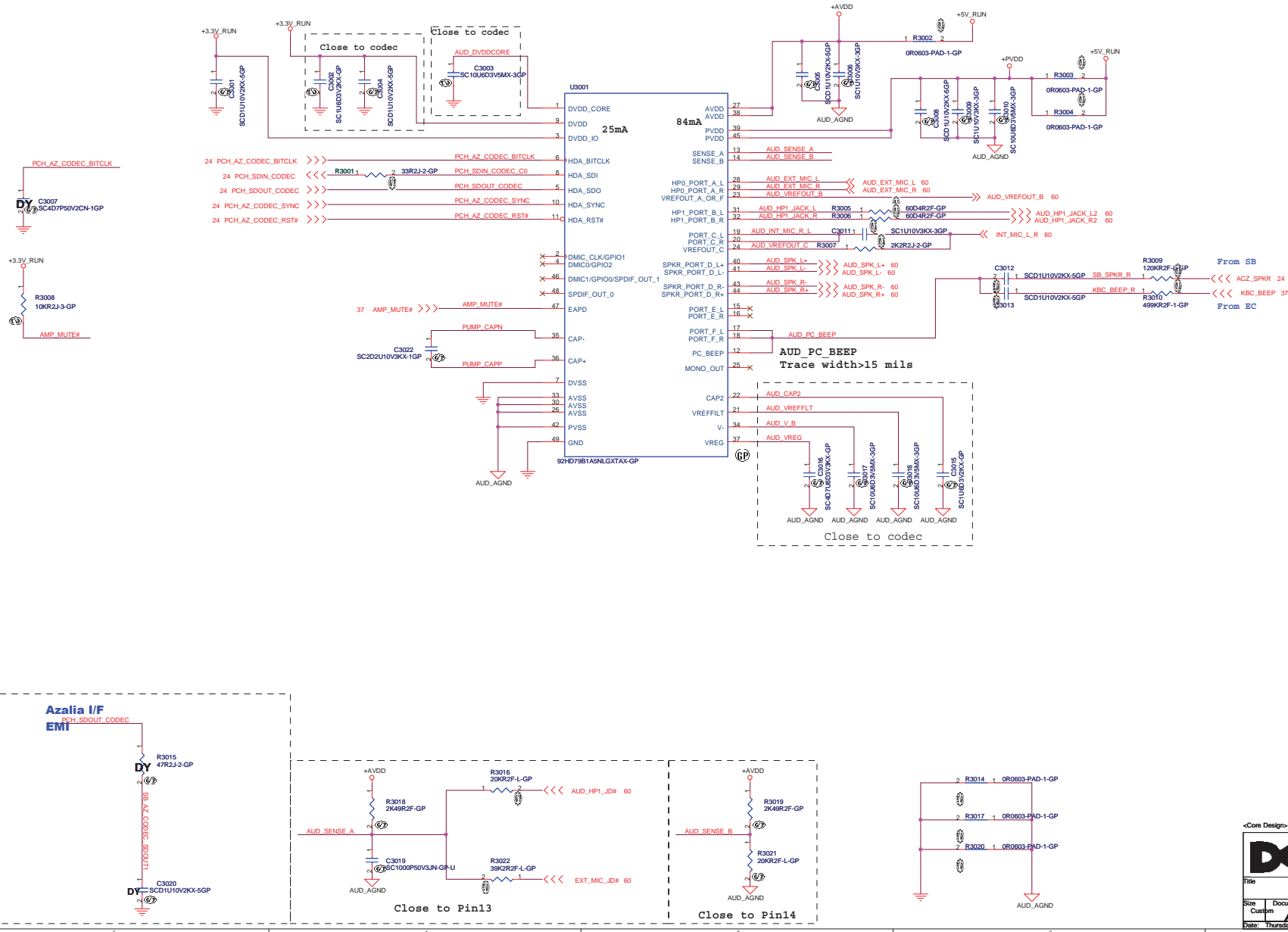
**DJ1 Calpella UMA**

Rev

**X01**

Date: Friday, April 16, 2010

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<Core Design>

<b>DELL</b>		<b>Wistron Corporation</b>	
		21F, 8B, Sec 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.	
Title		<b>Audio Codec 92HD79B1</b>	
Size	Document Number	Rev	
Custom		<b>Arsenal D11 Discrete</b>	
Date	Thursday, April 22, 2010	Sheet	30 of 90

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Taipei Hsien 221, Taiwan, R.O.C.

Title

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Size  
A3

Document Number

**DJ1 Calpella UMA**

Rev

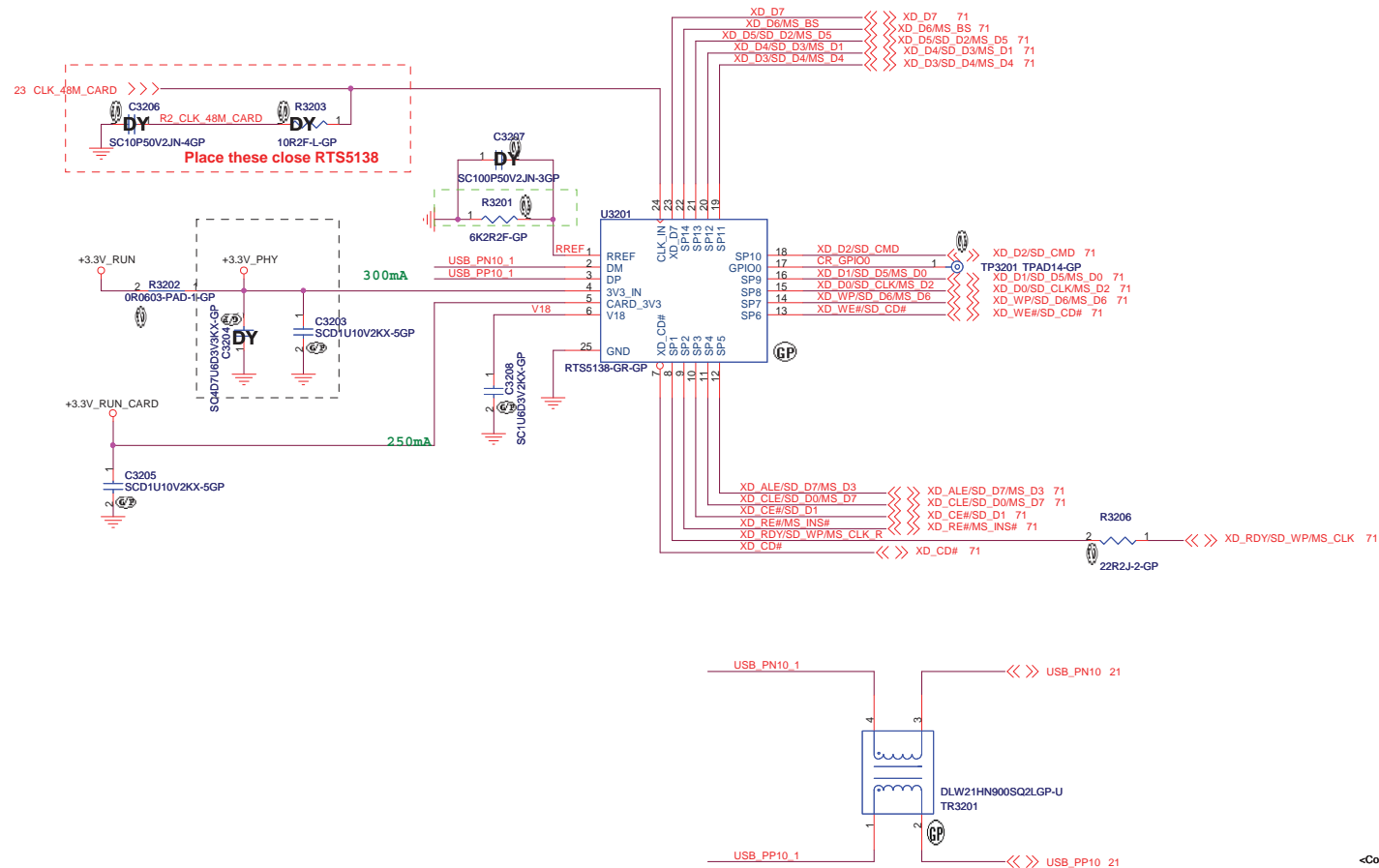
**X01**

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SSID = SDIO

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Title

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A3

Document Number

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Rev

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Document Number

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Rev

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Title

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Size  
A3

Document Number

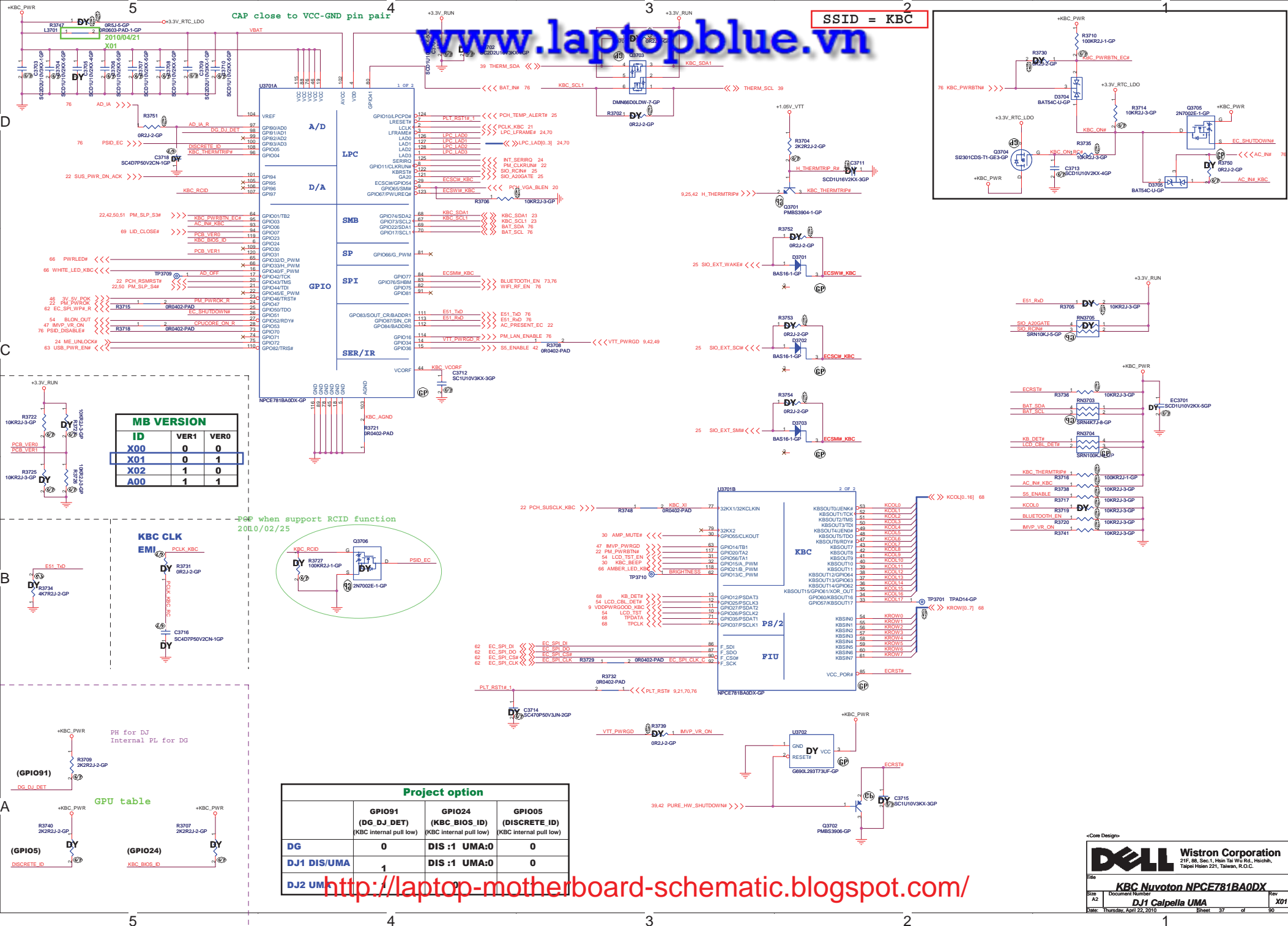
**DJ1 Calpella UMA**

Rev

**X01**

Date: Friday, April 16, 2010

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Title

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Size  
A3

Document Number

**DJ1 Calpella UMA**

Rev

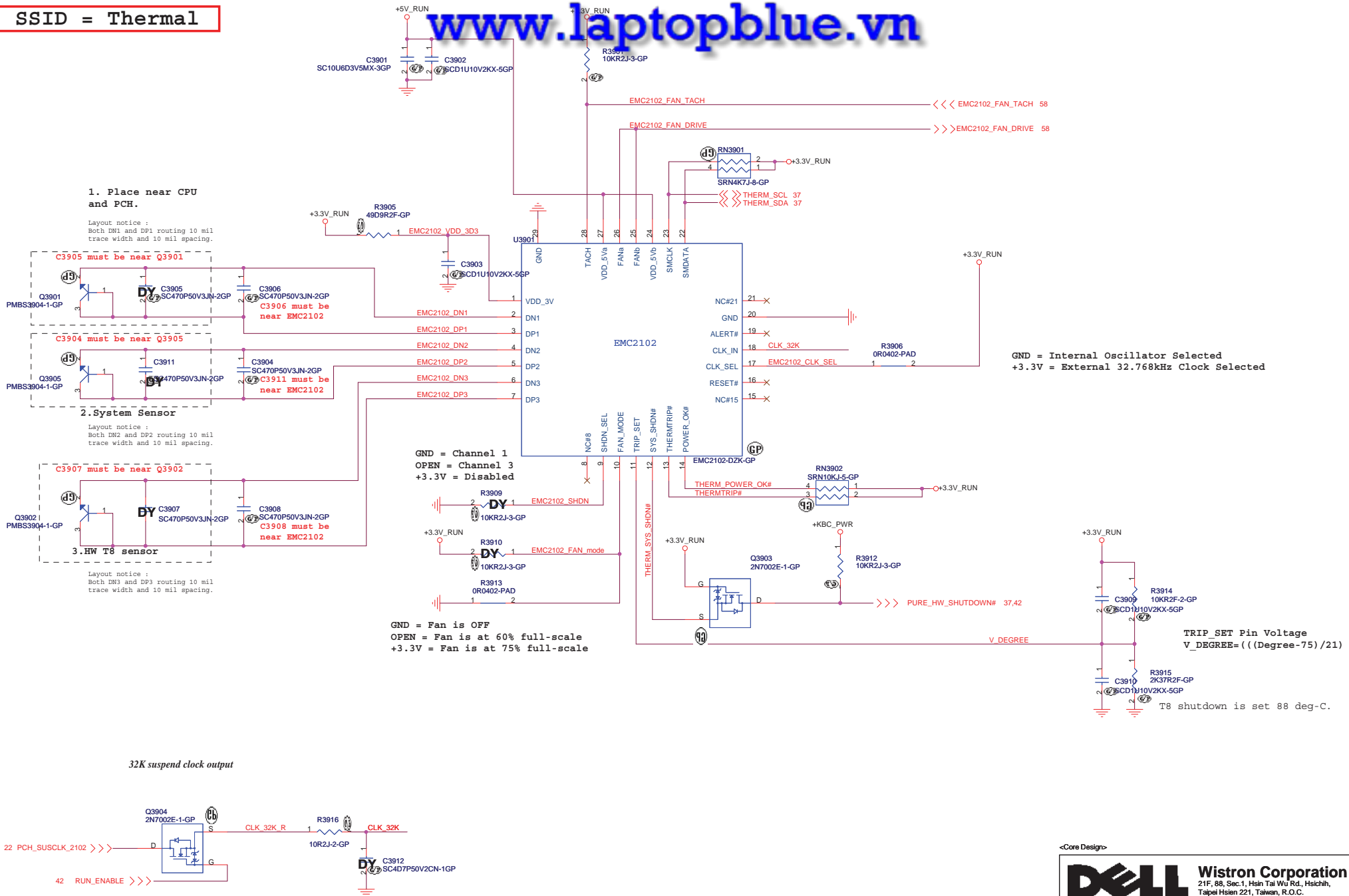
**X01**

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SSID = Thermal

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Title

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Size  
A3

Document Number

**DJ1 Calpella UMA**

Rev

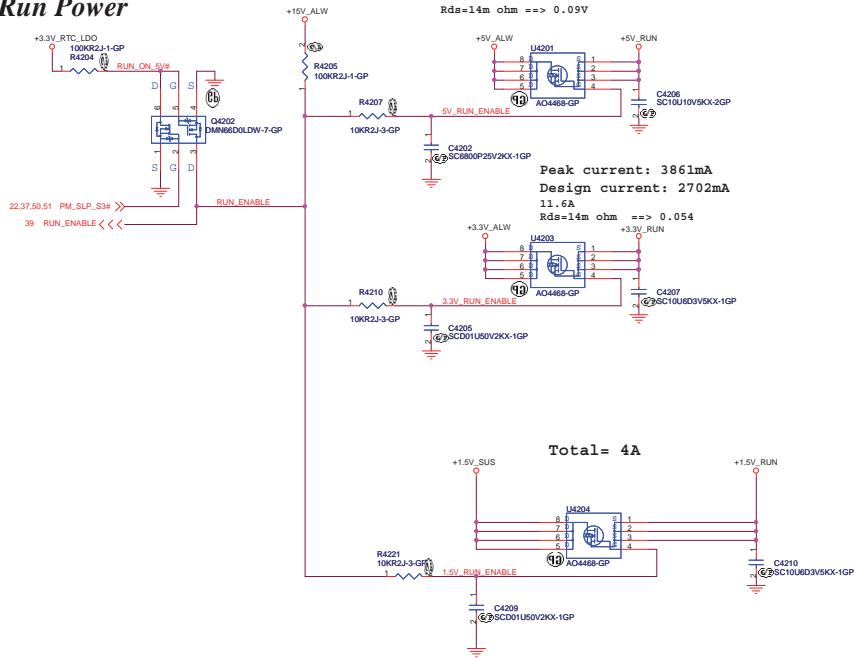
**X01**

Date: Friday, April 16, 2010

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### Run Power

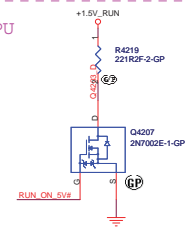


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Peak current: 6370mA ( HD:1100 ODD:2500 )
Design current: 4459 mA
11.6A
Rds=14m ohm ==> 0.09V
```

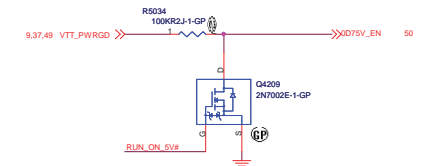
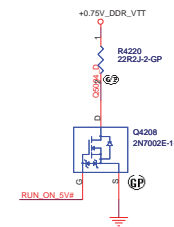
```
Peak current: 3861mA
Design current: 2702mA
11.6A
Rds=14m ohm ==> 0.054
```

$$\text{Total} = 4A$$

For



425302\_425302\_Calpella\_S3PowerReduction\_WhitePape  
Revision 0.7



&amp;ltCore Design&gt;



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Title			
<b>Power Plane Enable</b>			
Size	Document Number	Rev	
A2	<b>DJ1 Calpella UMA</b>	X0	
Date:	Thursday, April 22, 2010	Sheet	42 of 90

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Title

**Reserved**

Size  
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Document Number

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Rev

**X01**

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Title

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Size  
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Document Number

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Rev

**X01**

Date: Friday, April 16, 2010

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Title

**Reserved**

Size  
A3

Document Number

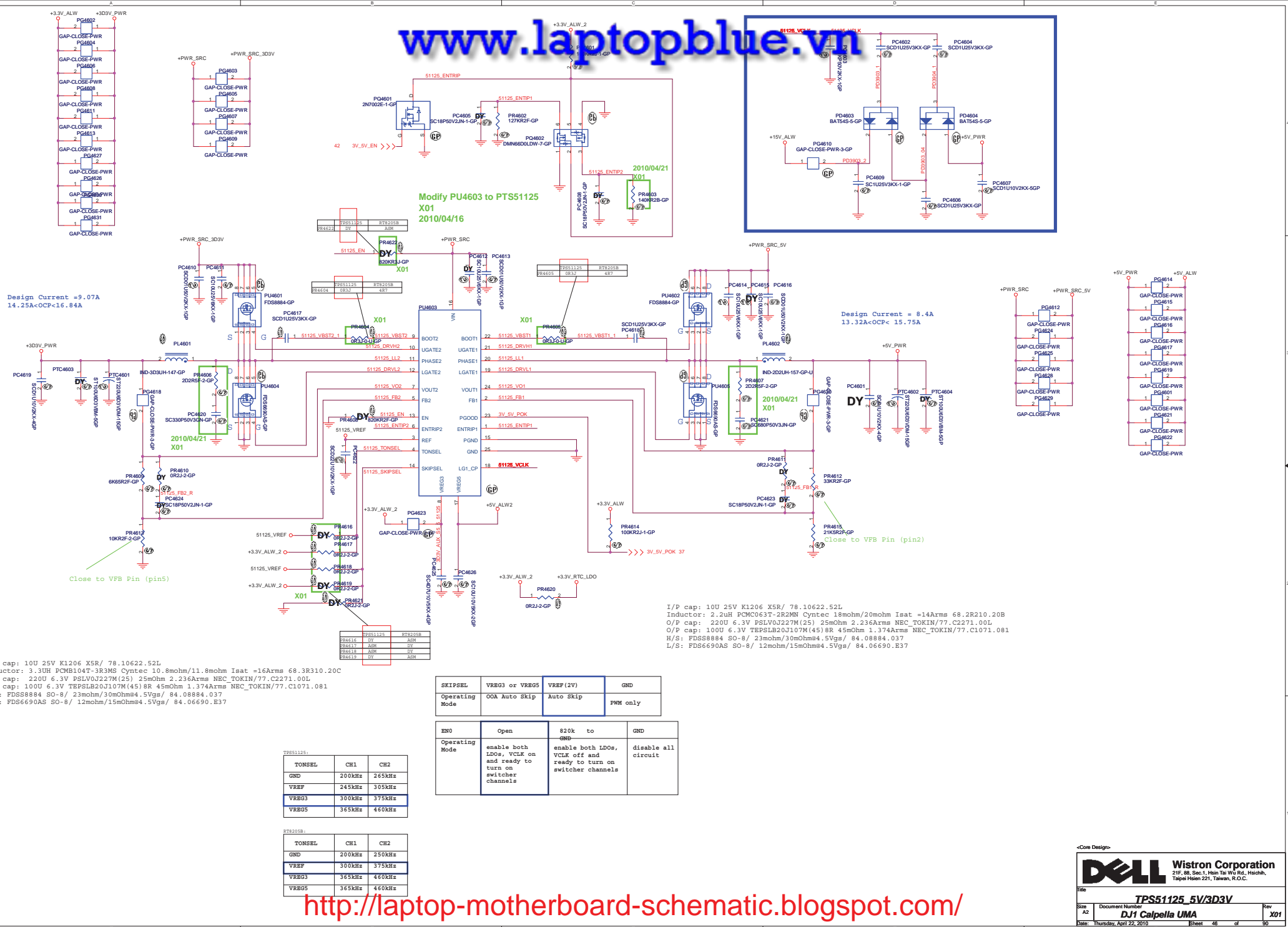
**DJ1 Calpella UMA**

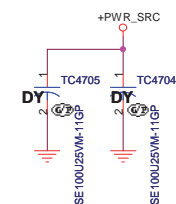
Rev

**X01**

Date: Friday, April 16, 2010

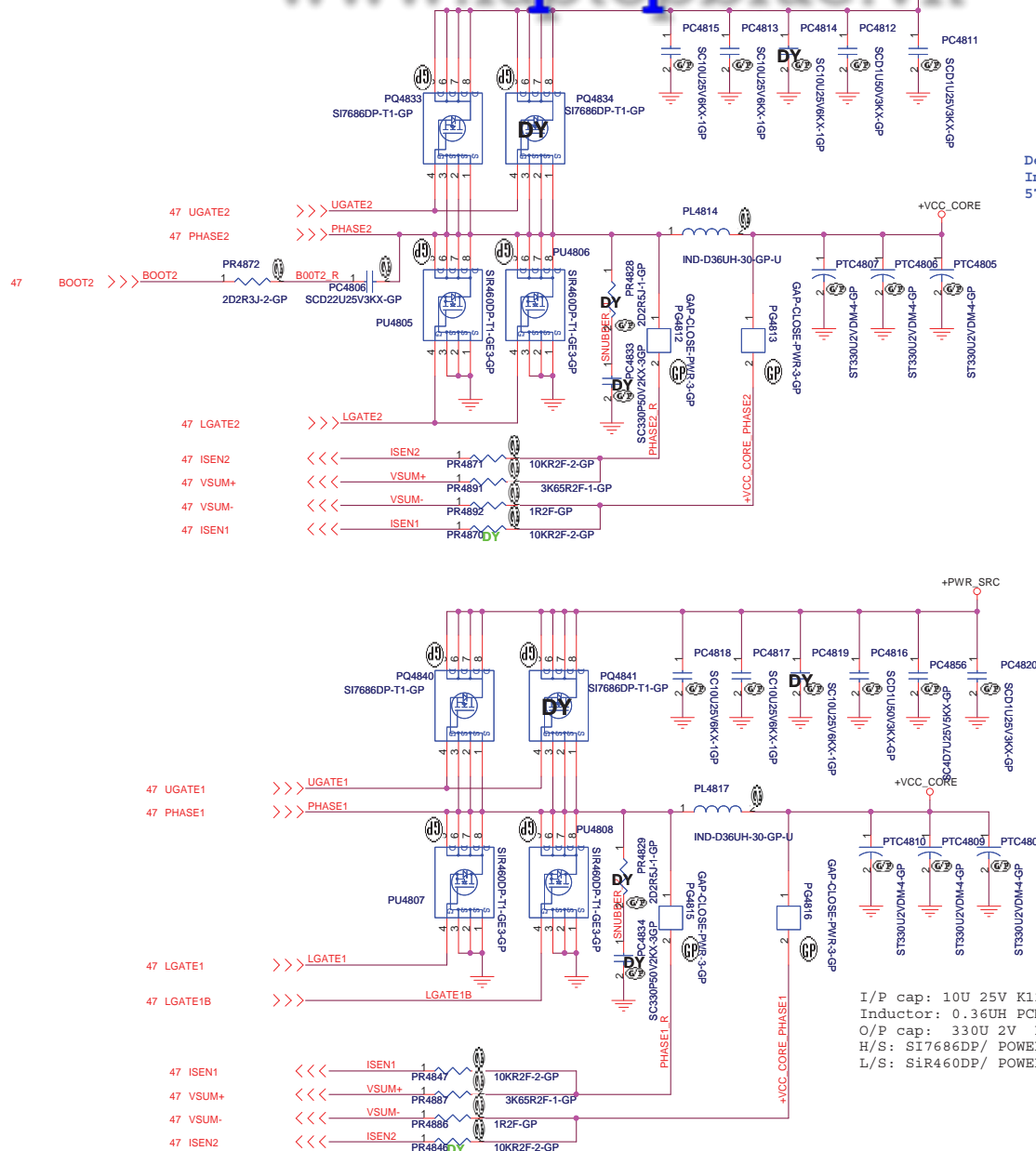
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Title			
<b>ISL62883 CPU CORE</b>			
Size A3	Document Number <b>Berry</b>	Rev <b>X0</b>	
Date: Monday, April 26, 2010	Sheet 47	of 90	



Design Current = 34A  
Imax=48A  
57.6A<OCP<67.2A

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L  
Inductor: 0.36UH PCMC104T-R36MN1R05J Cyntec 1.05mohm/ 68.R3610.20C  
O/P cap: 330U 2V EEF5X0D331XE 6mOhm 3.4Arms Panasonic/79.33719.20L  
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037  
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

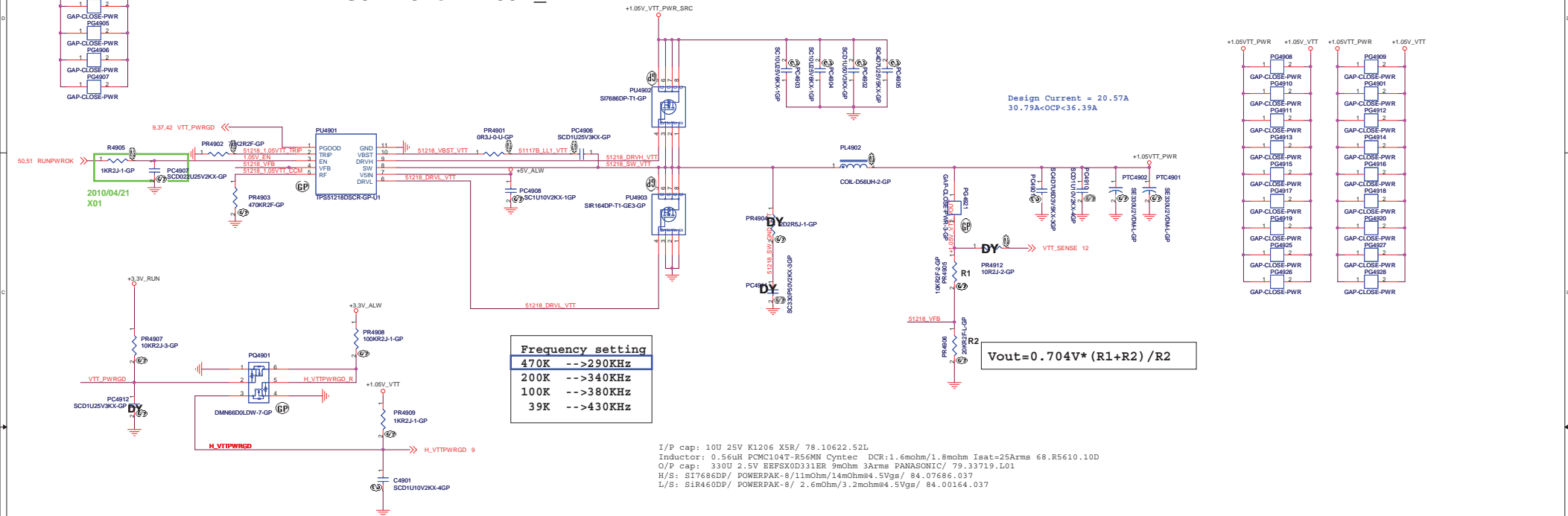
<Core Design>

**DELL** Wistron Corporation  
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Title			
ISL62883 CPU CORE			
Size	Document Number	Rev	
A3	Berry	X01	
Date: Thursday, April 22, 2010		Sheet 48	of 90



## +1.05V\_VTT\_PWR\_SRC



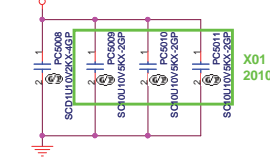
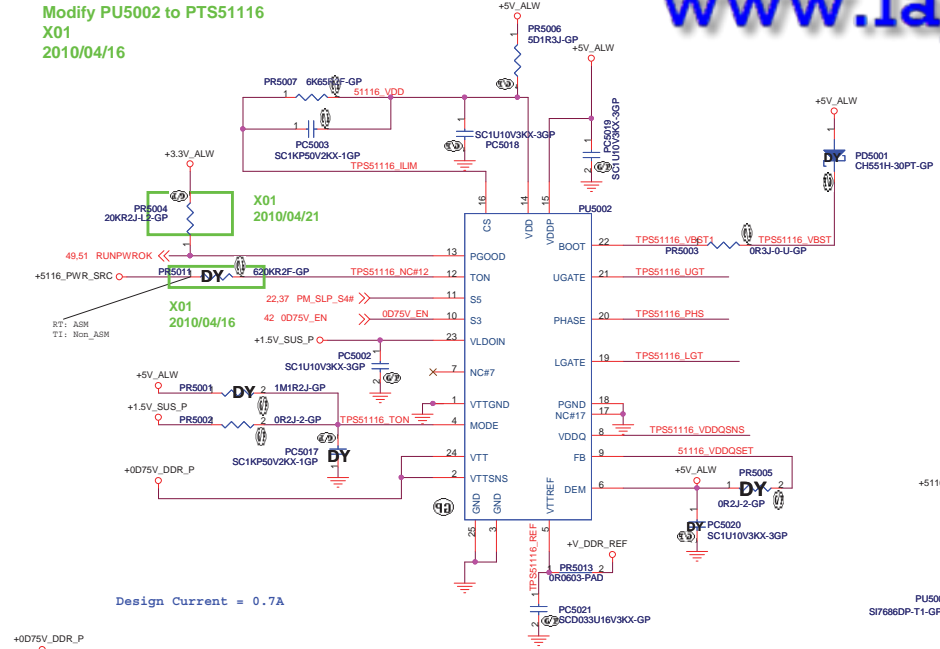
«Core Design»



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Title			
<b>TPS51218 +1.05V VTT</b>			
Size	Document Number	Rev	
A2	<b>DJ1 Calpella UMA</b>	<b>X01</b>	
Date:	Thursday, April 22, 2010	Sheet	49 of 90

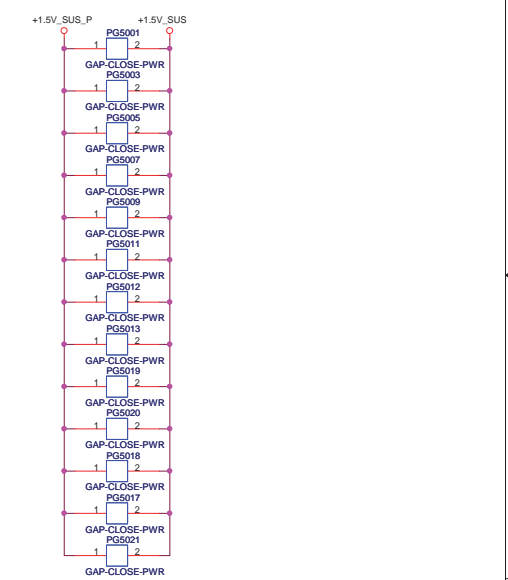
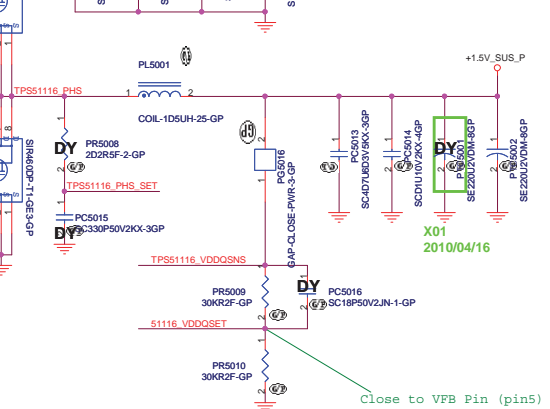
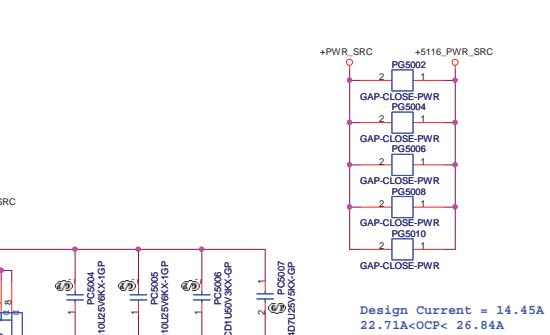
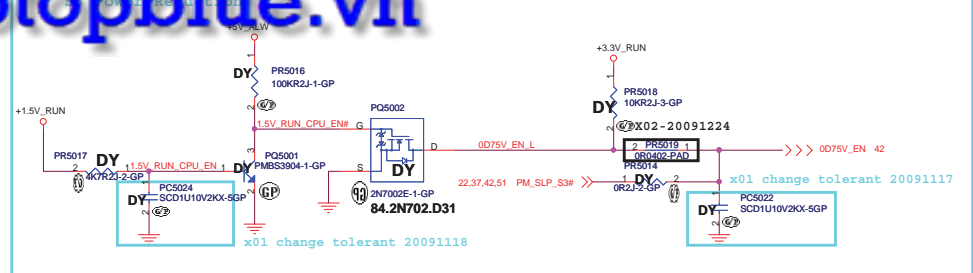
Modify PU5002 to PTS51116  
X01  
2010/04/16



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L  
Inductor: 1.5uH PCMC104T-1R5 Cyntec DCR:3.8mohm Isat=33Arms 68.1R510.10J  
O/P cap: 220U 2V EEPCK0D221ER 15mOhm 2.7Arms PANASONIC/ 79.22719.20L  
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037  
L/S: SI7460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037  
Switching freq-->400KHz



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Title: **TPS51116 +1.5V SUS**

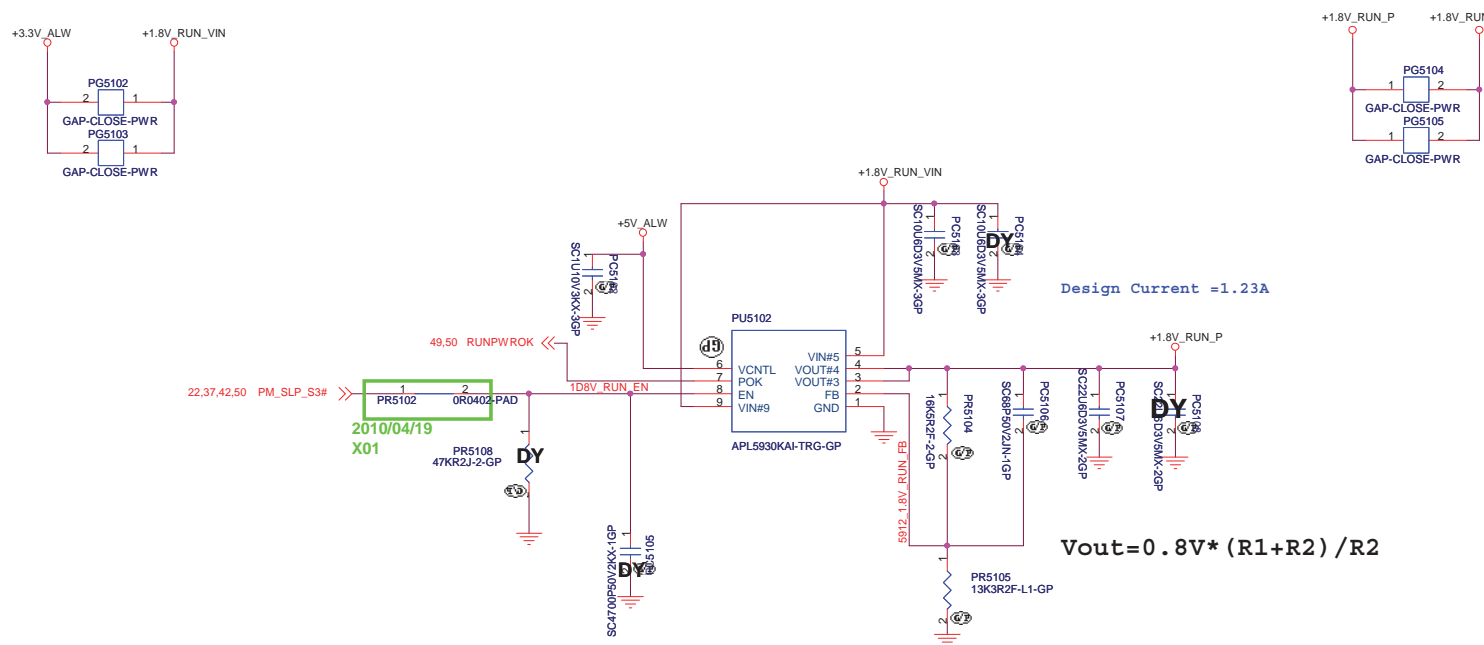
Doc Number: **DJ1 Calpella UMA**

Date: Thursday, April 22, 2010 Sheet 50 of 90

Rev: **X01**

SSID = PWR.Plane.Regulator\_1p8v

## APL5930 for +1.8V\_RUN



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Title

**Reserved**

Size  
A3

Document Number

**DJ1 Calpella UMA**

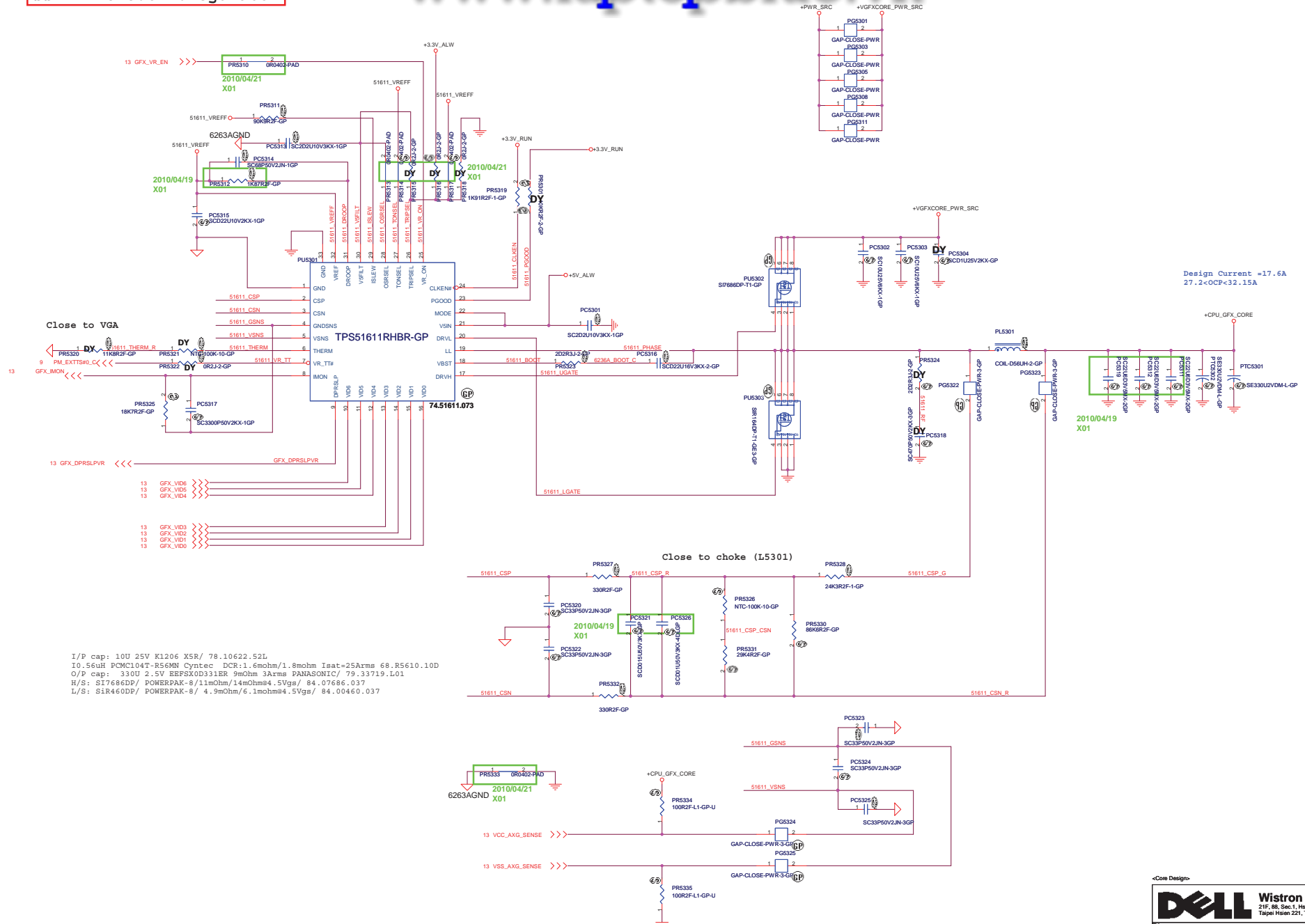
Rev

**X01**

Date: Friday, April 16, 2010

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SSID = CPU.GFX.Regulator



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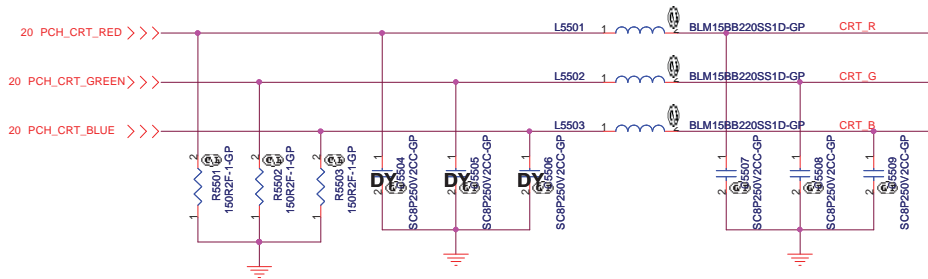
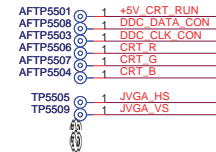
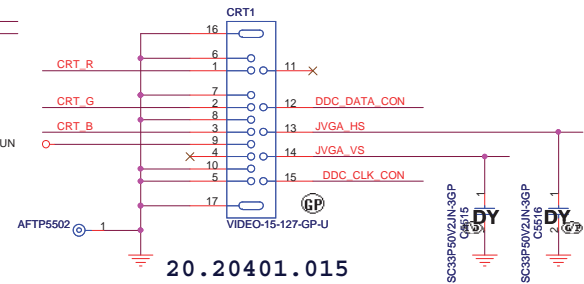
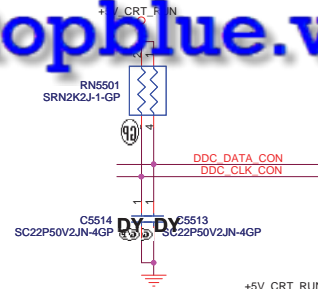
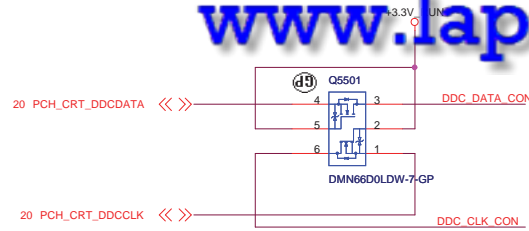
SSID = Inverter

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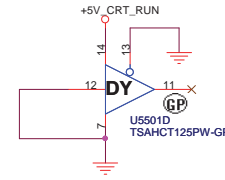
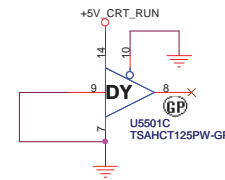
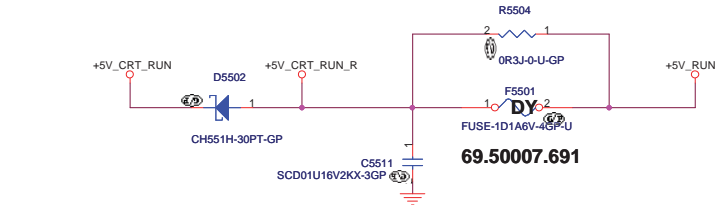
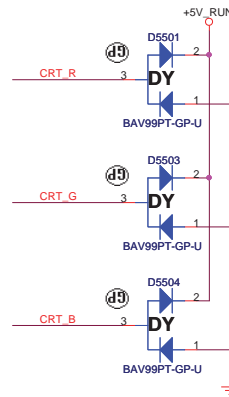
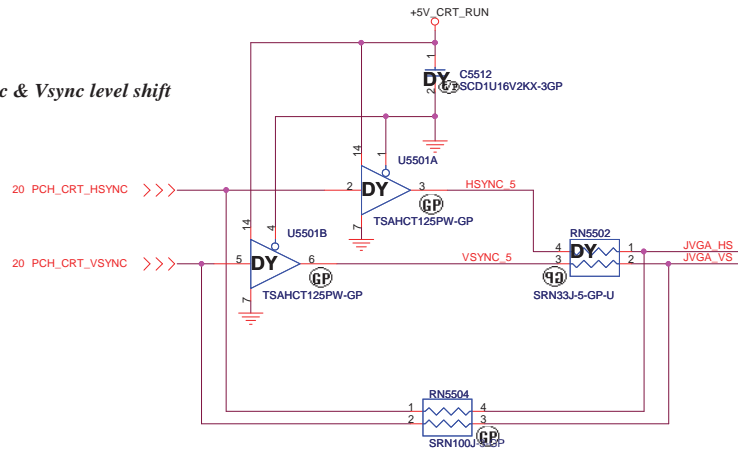
SSID = VIDEO

Layout Note:

- \*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
- \* RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.



Hsync & Vsync level shift



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CLOSE TO TRANSFORMER

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Title: **CRT Connector**

Size: Document Number: **DJ1 Calpella UMA** Rev: **X01**

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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

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**HDMI**

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Rev

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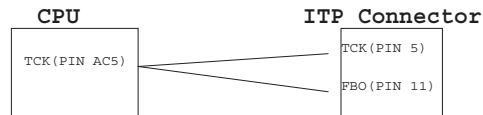
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SSID = User.Interface
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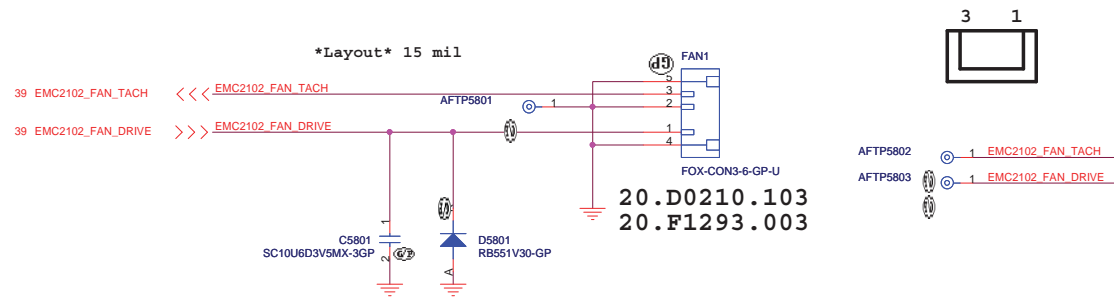
## ITP Connector

H\_CPURST# use pull-up Resistor close  
ITP connector 500 mil ( max ),  
others place near CPU side.



SSID = Thermal

## Fan Connector



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### ITP/Fan Connector

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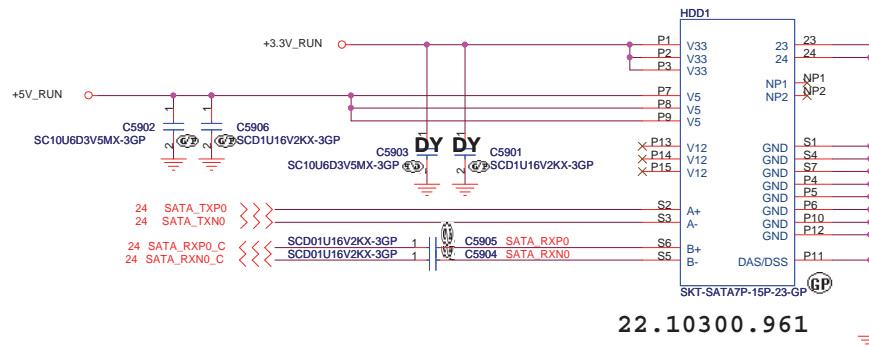
**DJ1 Calpella UMA**

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**X01**

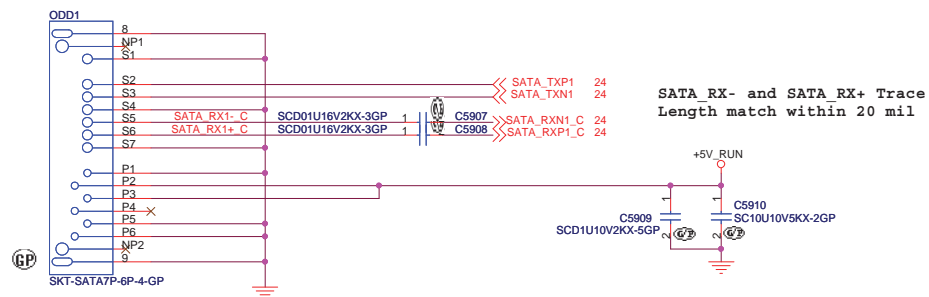
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## ODD Connector



22.10300.811  
22.10300.421  
22.10300.471

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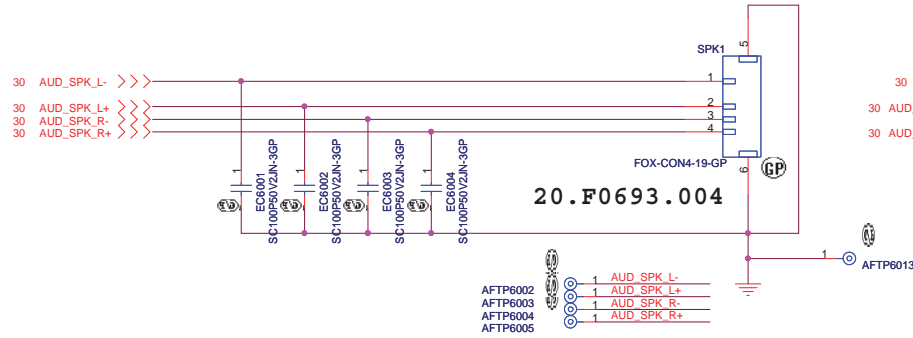
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SSID = AUDIO

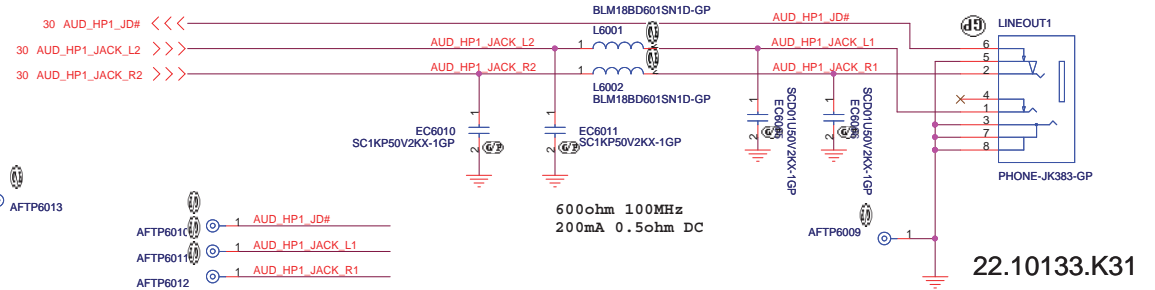
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## Speaker Connector

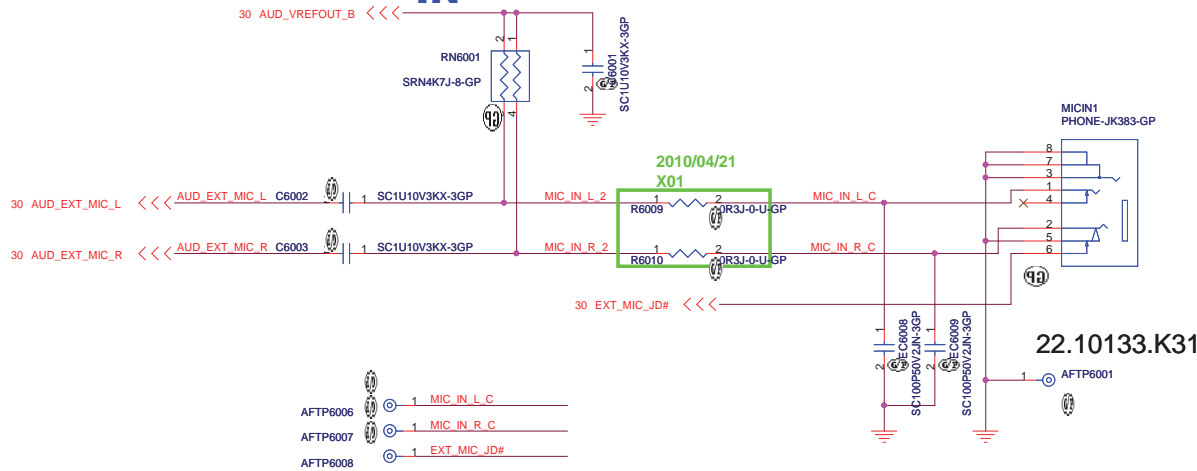
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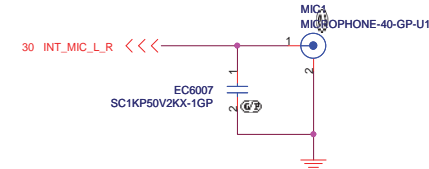
## LINE1 OUT



## MIC IN



## Internal Microphone



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**Audio Jack**

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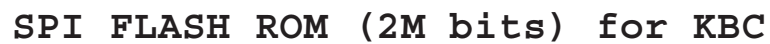
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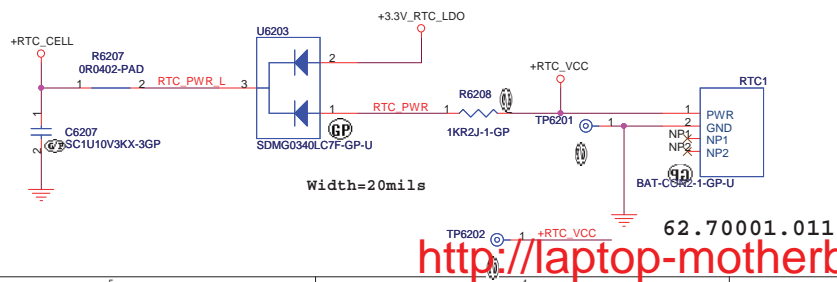
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SPI FLASH ROM (32M bits, 241 pins)



## RTC Connector



TP6202  1  +RTC\_VCC 62.70001.011

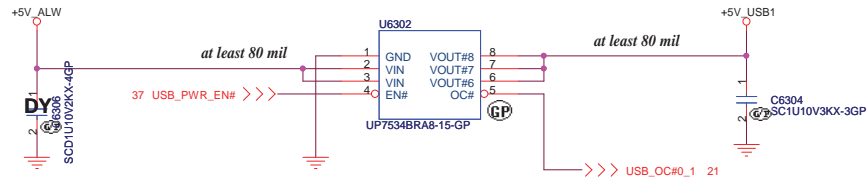
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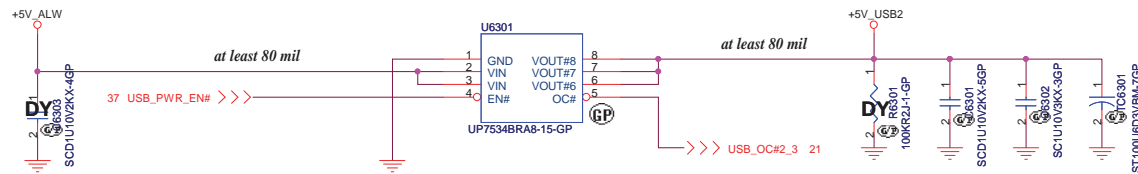
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## IO Board USB Power

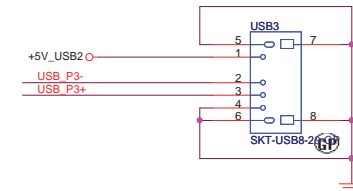
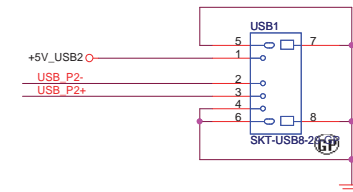
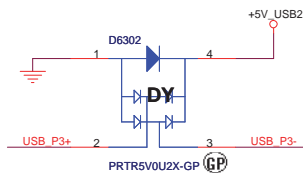
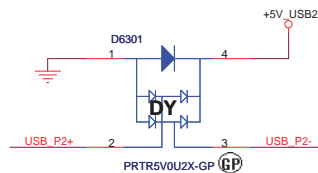
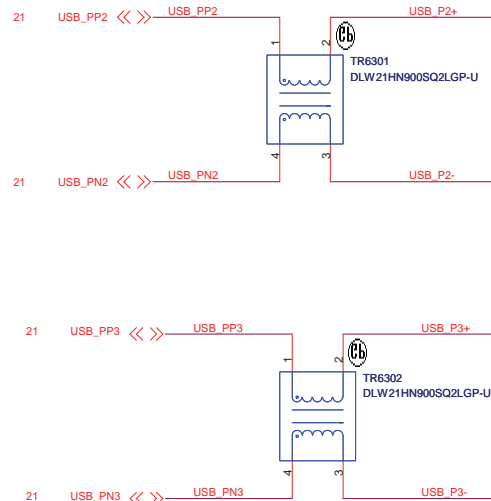
UP7534BRA8-15 P/N:74.07534.079  
SEC AP2101MPG-13 P/N: 74.02101.079



## Right USB Power



AFTP6304 1 +5V\_USB2  
AFTP6302 1 USB\_P2-  
AFTP6301 1 USB\_P2+  
AFTP6306 1 USB\_P3-  
AFTP6305 1 USB\_P3+



22.10254.451

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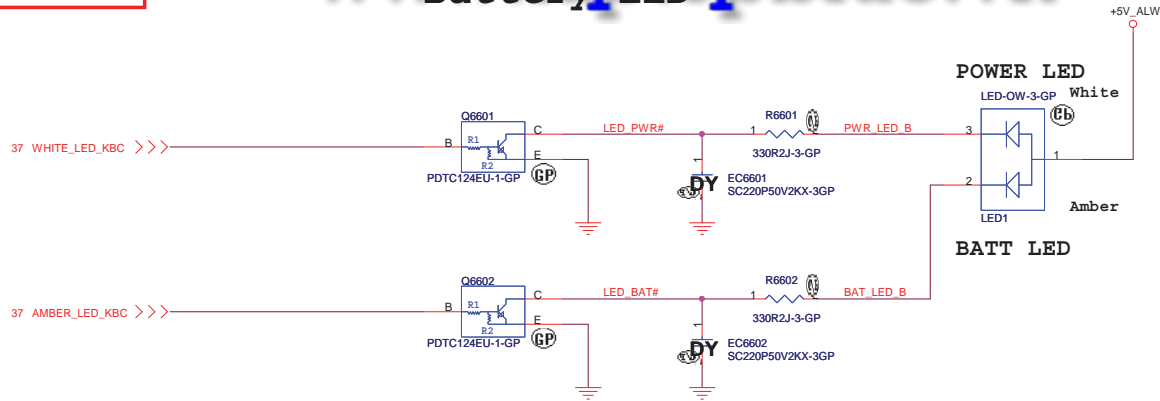
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SSID = User.Interface

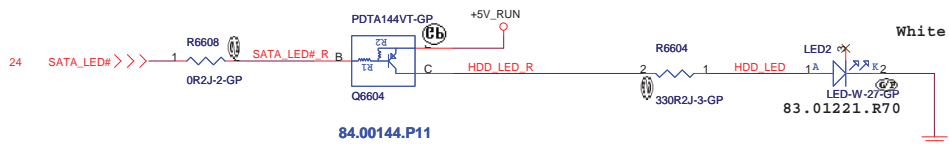
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Battery LED



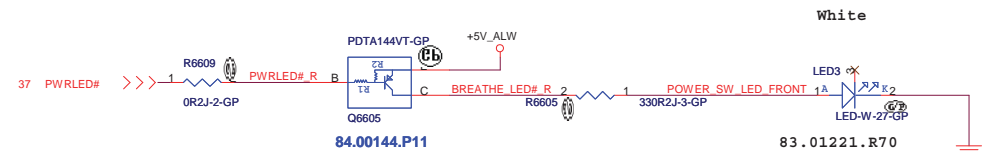
83.00326.G70  
83.01222.K70

## HDD LED



84.00144.P11

## BREATHE PWR LED (Front)



84.00144.P11

83.01221.R70

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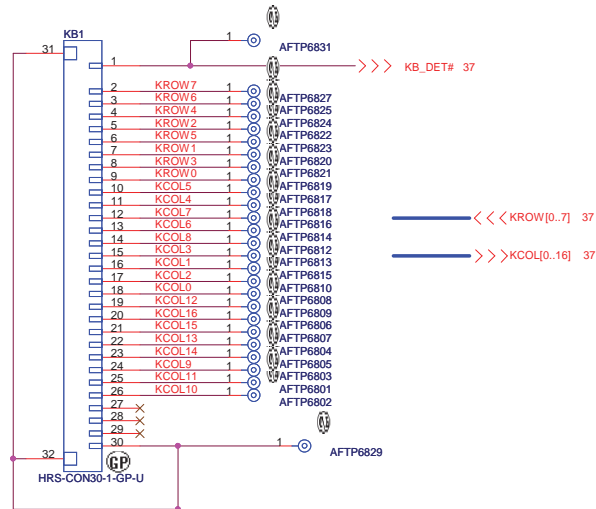
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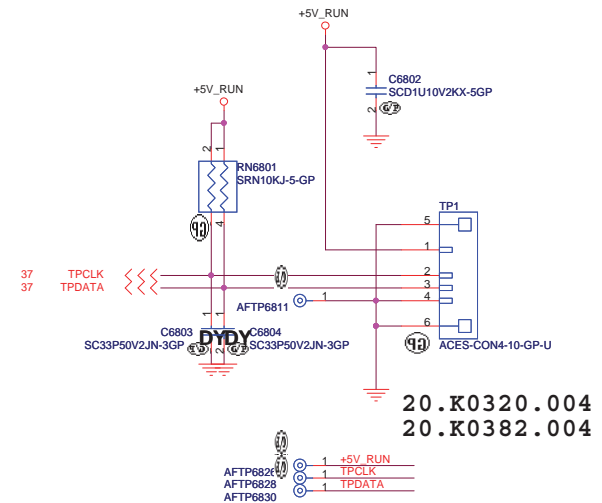
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## TouchPad Connector



```
Main 20.K0259.030
      20.K0461.030
      20.K0421.030
```



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### Key Board/Touch Pad

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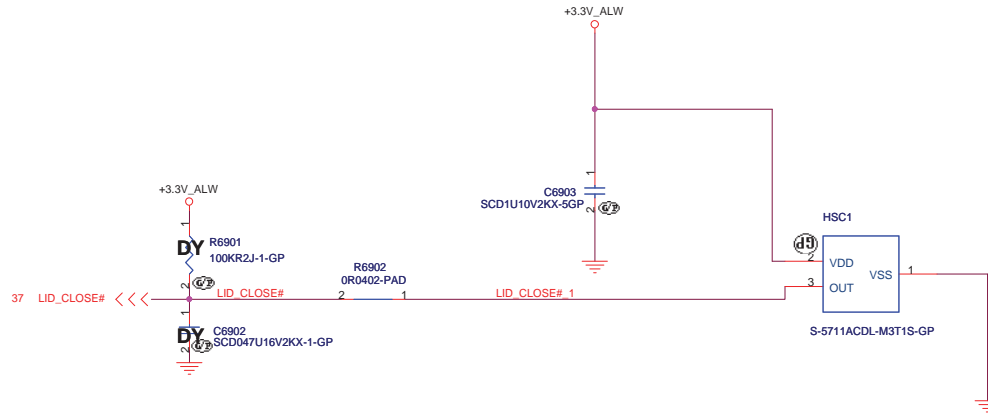
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**Hall Sensor**

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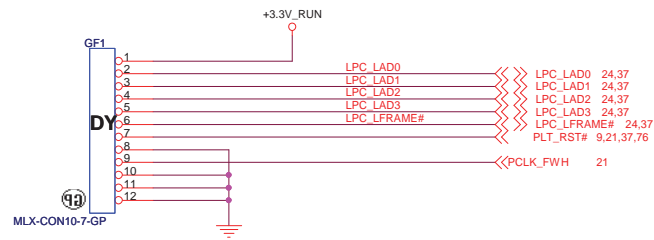
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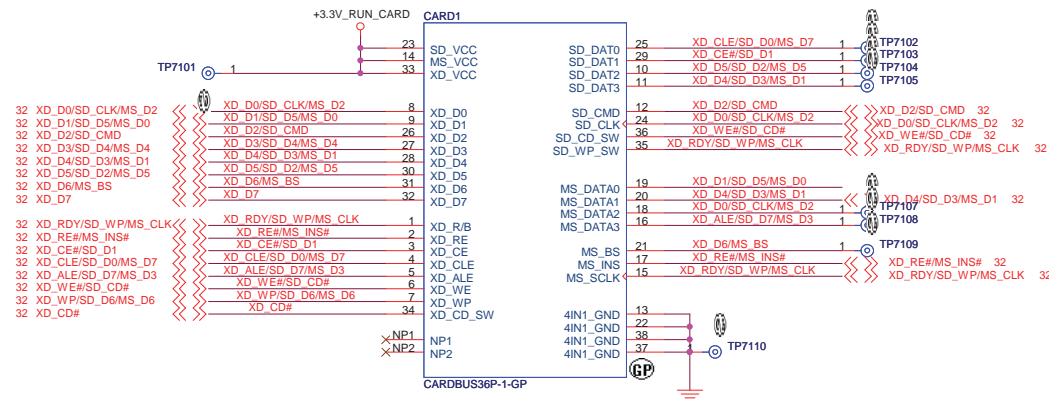
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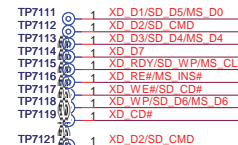
*SD/XD/Micro Reader* [www.laptopblue.vn](http://www.laptopblue.vn)




XD\_CLE/SD\_D0/MS D7  
 XD\_CE#/SD\_D1  
 XD\_D5/SD\_D3/MS D5  
 XD\_D4/SD\_D2/MS D1  
 XD\_D2/SD\_CMD  
 XD\_D0/SD\_CLK/MS D2  
 XD\_WE#/SD\_CD#  
 XD\_RDY/SD\_WP/MS\_CLK

E710  
 SC220P8P8VXX-3GP  
 E709  
 SC220P8P8VXX-3GP  
 E708  
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For EMI



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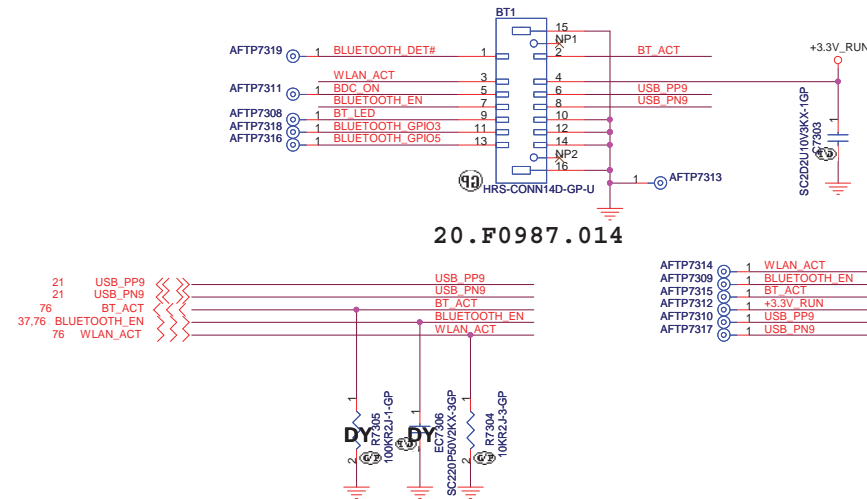
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SSID = User.Interface

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### Bluetooth Module conn.



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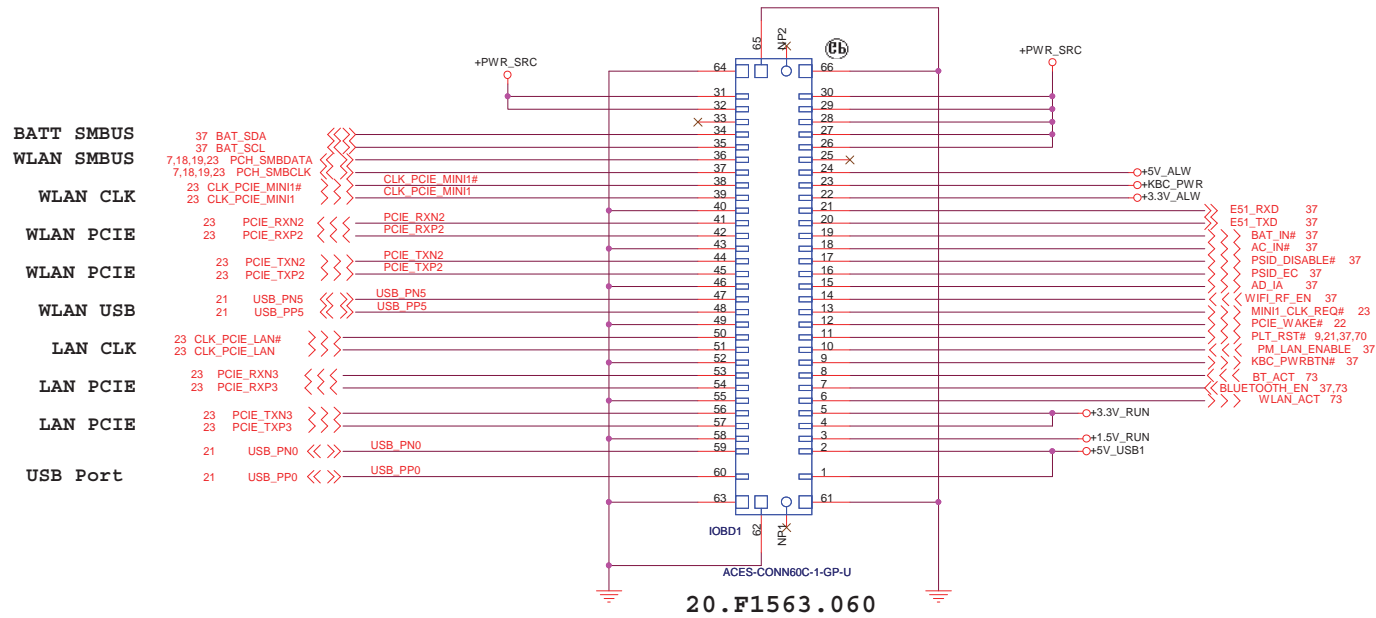
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SSID = PWR.Support

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<b>IO Board Connector</b>			
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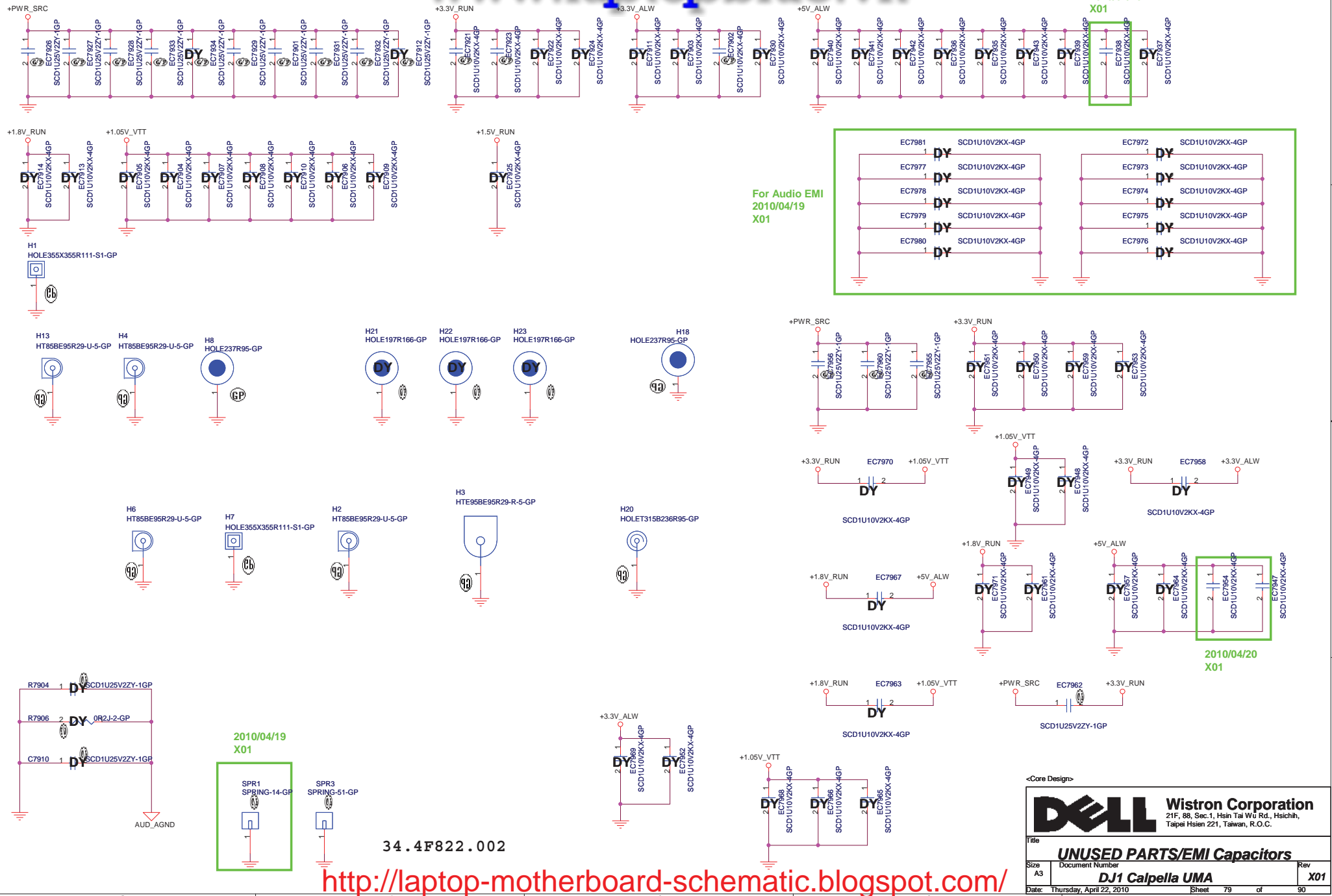
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SSID = VIDEO

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Reserved**

Size  
A3

Document Number

**DJ1 Calpella UMA**

Rev

**X01**


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Item	Page#	Date	Request By	Issue description	Solution Description	Rev
1	46	2010/04/16	Power team	PU4603 (RT8205) shortage risk	Change to TPS51125	X01
2	50	2010/04/16	Power team	PU5002 (RT8207) shortage risk	Change to TPS51116, DY PR5011	X01
3	49	2010/04/16	EE	PM_PWROK to +1.05V_VTT power down sequence out of SPEC	Modify PC4907=0.022U, PR5004, add R4905=1K	X01
4	55	2010/04/16	EE	For SIV CRT test fail item	Modify RN5504=100 Ohm	X01
5	50	2010/04/16	Power team	Cost down	DY PTC5001	X01
6	53/13	2010/04/19	Power team	Power team request	Change PC5321=0.015U, PC5326=0.01U, PR5312 Mount PC5319, PC5312, PC5311, C1325, C1328, C1323	X01
7	47/12	2010/04/19	Power team	Power team request	Modify PR4705=2,8K, PR4727=1.4K Mount C1214=C1236=C1241=C1208=C1231=10U	X01
8	79	2010/04/19	ME	For EMI	Add SPR1	X01
9	79	2010/04/21-22	EMC	For EMI	Add EC7972-EC7981 (DY) Mount EC7938, EC7947, EC7954	X01
10	26/37/47/51/53/	2010/04/21	EE	Cost down	Change 0 Ohm resistance to 0 Ohm pad: R2611, R2603, L3701, PR4706, PR4708, PR4713, PR4718, PR4722, PR4732, PR4738, PR4744, PR4755, PR4764, PR4707, PR4711, PR4776, PR4784, PR4703, PR4704, PR4790, PR5102, PR5310, PR5313, PR5314, PR5317, PR5333	X01
11	60	2010/04/21	EE	for audio vender's seggust	Modify R6009, R6010 to 0 Ohm resistances	X01
12	37	2010/04/21	EE	For version ID	Mount R3722, DY R3725	X01
13	46	2010/04/22	Power team	For power snubber	Mount PR4606=PR4607=2R2, PC4620=330P, PC4621=680P	X01
14	46	2010/04/22	Power team	For OCP	Modify PR4603=140K	X01
15	47	2010/04/23	Power team	For power snubber	Modify PR4717=10K	X01

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**Change History**

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(AC mode)

red word: KBC GPIO

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DC mod

re word: KBC, GPIO

