TUCANA Block Diagram

PROJECT CODE : 91.4KK01.001
PCB P/N : 48.4KK01.0SB
REVISION : S0201-SB

Clock Generator
ICS9LVS3197BKLFT
3

Thermal Sensor
GMT G787
37

DDRIII 800 Slot 0 21 — DDRIII Channel A
DDRIII 800 Slot 1 22 — DDRIII Channel B

Intel CPU
SFF
4,5,..,10,11

FDIx8 / DMIx4

Int MIC
Line Out
MIC In
SPKR 1.5W

Codec Realtek ALC269 31~33 — AZALIA

INTEL
PCH
14 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
6 SATA ports
8 PCIE ports
ACPI 1.1
LPC I/F
PCI/PCI BRIDGE
12,13,...,19,20

LVDS — LCD 23
RGB — CRT 24
PCIe — HDMI 25

USB
9 — CAMERA 23
0,1,4 — USB Port x 3 28
12 — Blue Tooth 27
2 — Cardreader Realtek RTS5186 34 — MS Pro Duo /SD(SDHC) 34
8 — Mini 1 Card WLAN/ WIMAX 35

PCIe
1 — Giga LAN Atheros AR8131M 29 — TXFM 30 — RJ45 30
3

HDD 26 — 0 — SATA
Flash ROM 4MB 39 — SPI

LPC
KBC Winbond NPCE781L 38 — SPI — Flash ROM 128KB 39
LPC DEBUG CONN. 39
Touch Pad 40
INT. KB 38

PCB STACKUP

TOP		L1
VCC		L2
S		L3
S		L4
GND		L5
BOTTOM		L6

SMbus ADDRESS

DIMM 1	1010 000x b
DIMM 2	1010 001x b
CLK GEN	1110 001x b
Thermal Sensor	0101 110x b
CHARGER	0001 001x b
BATTERY	0001 110x b

SYSTEM DC/DC RT8223 47

INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(5A) 5V_AUX_S5 3D3V_AUX_S5

RT8209 49

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(20A)

RT8209 48

INPUTS	OUTPUTS
DCBATOUT	1D5V_S3(9.4A)

RT9026 51

INPUTS	OUTPUTS
5V_S5	DDR_VREF_S3 1.2A

CHARGER BQ24751 52

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A

CPU DC/DC ADP3211 46

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 27A

GFX Core ADP3211 50

INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE 11A

DVT 1ST

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Title: BLOCK DIAGRAM
Size: A3 | Document Number: TUCANA | Rev: SB
Date: Wednesday, July 07, 2010 | Sheet 1 of 56

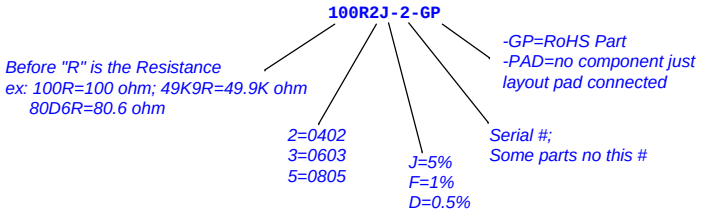
PCH Strapping

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#	**Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default - Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	**Enable iTPM:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable iTPM:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Danbury:** Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :** Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

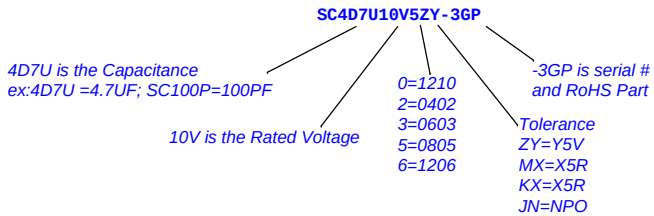
Processor Strapping

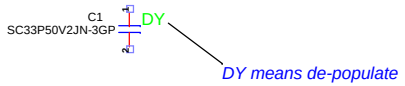
Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connected to the Embedded Display Port.	**1**
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	**1**
CFG[7]	**Reserved - Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** - Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	**0**

Resistor



Capacitor





DVT 1ST

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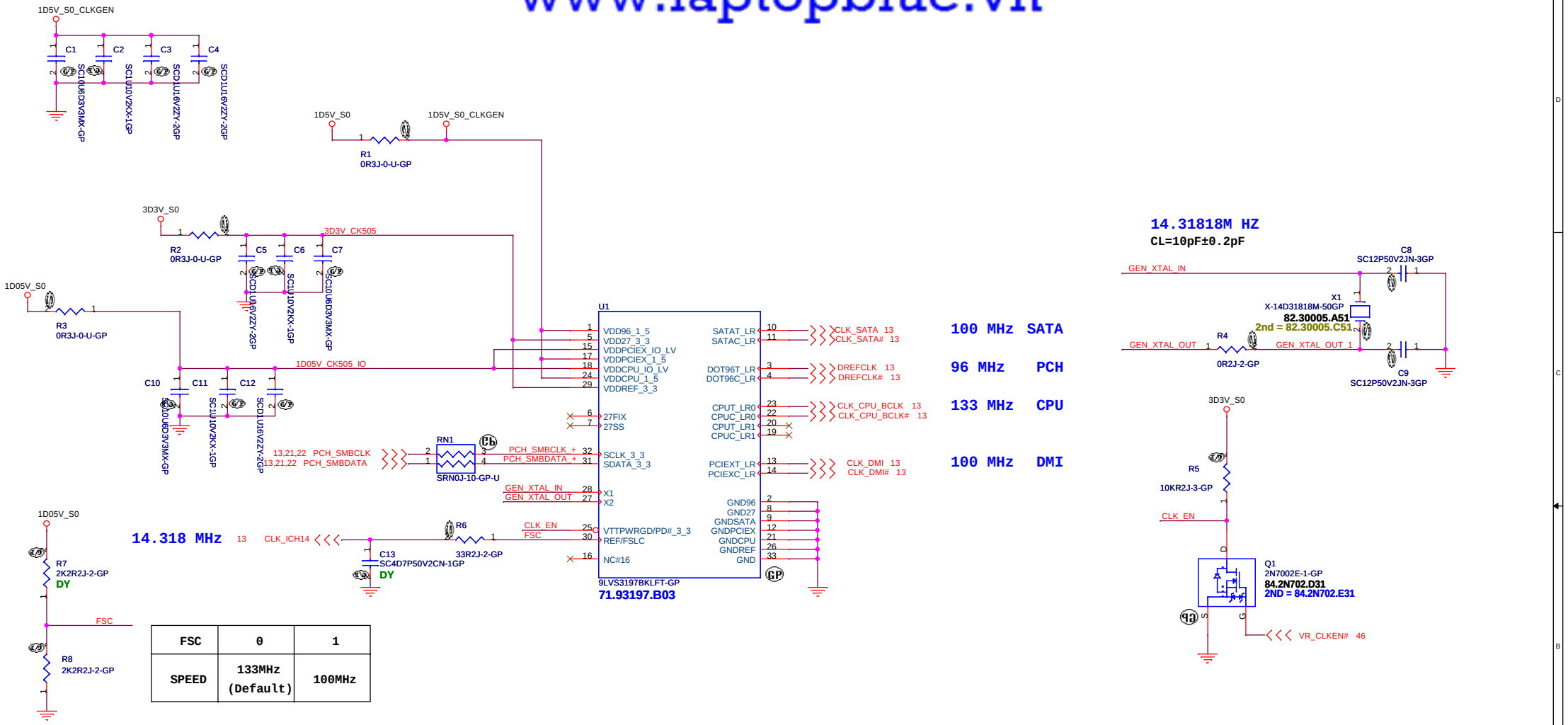
Title: Reference	
Size: A3	Document Number: TUCANA — Rev: SB
Date: Wednesday, July 07, 2010	Sheet 2 of 56



FSC	0	1
SPEED	133MHz (Default)	100MHz

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Clock Generator

Size	Document Number	Rev
A3	TUCANA	SB

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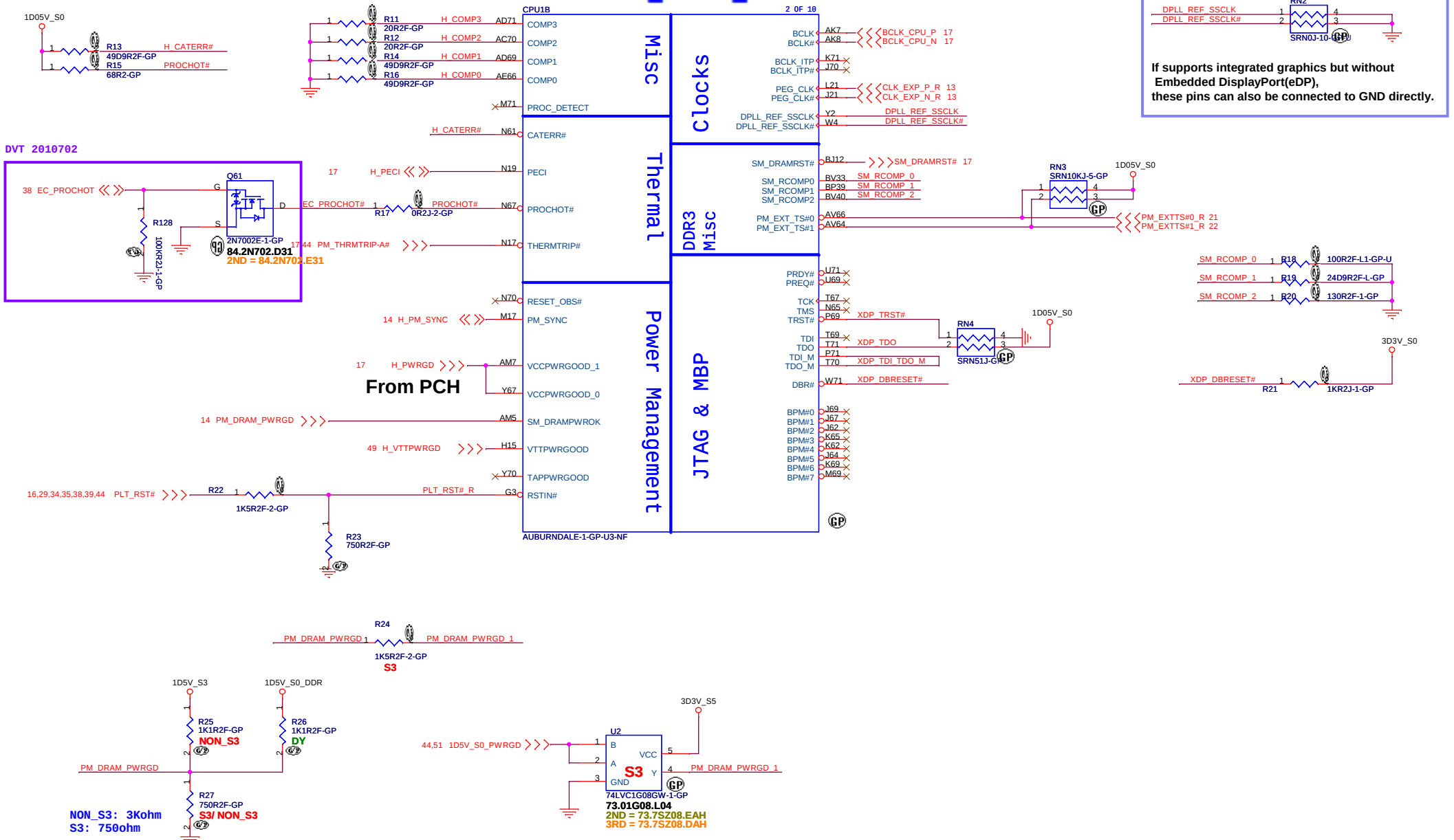
Title	CPU SFF 1 of 8(DMI/FDI/PEG)		
Size A3	Document Number TUCANA		Rev SB
Date: Wednesday, July 07, 2010	Sheet 4	of	56



DVT 1ST

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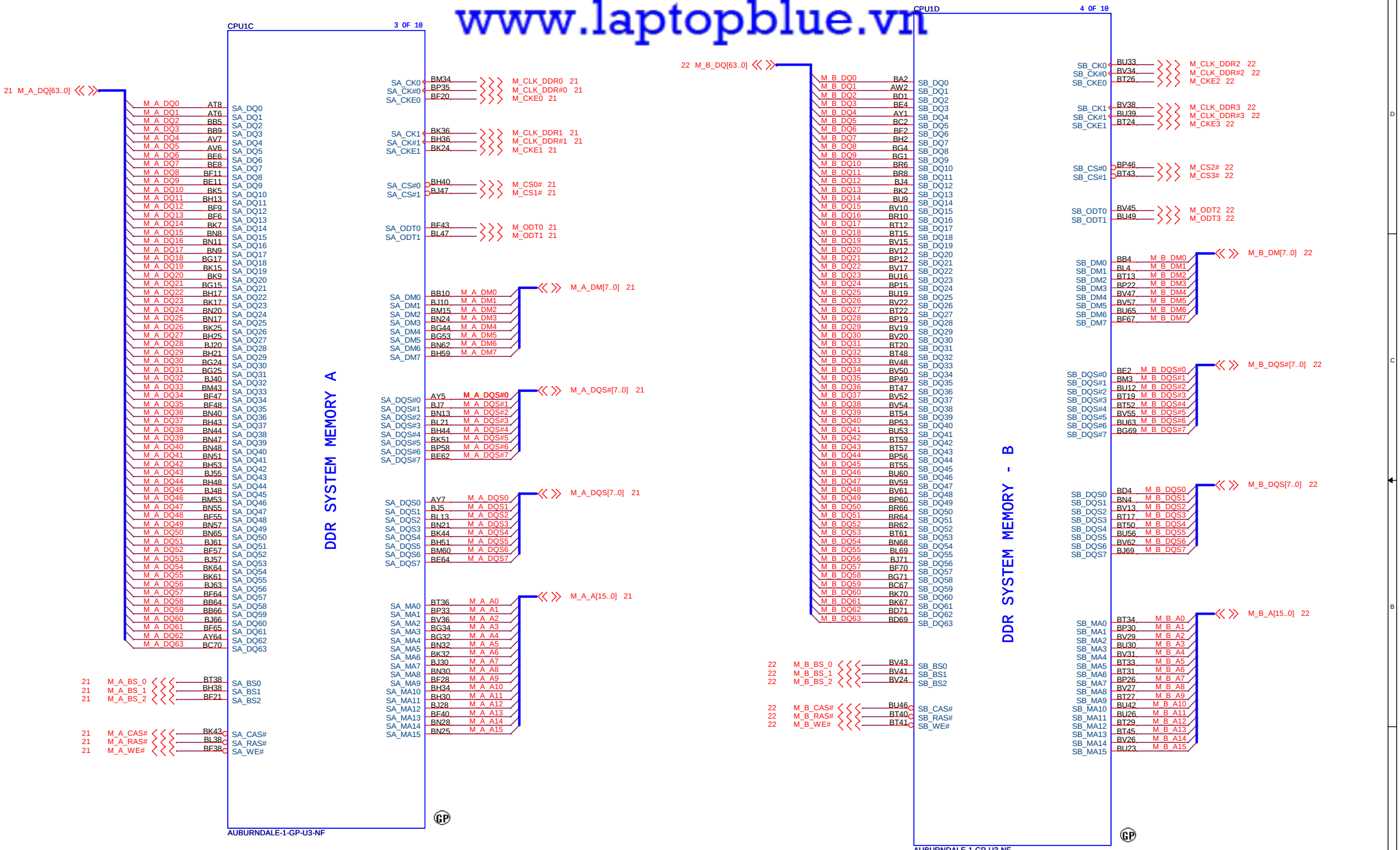
Title	**CPU SFF 2 of 8(CLK/Thermal)**	
Size A3	Document Number **TUCANA**	Rev **SB**
Date: Wednesday, July 07, 2010	Sheet 5 of 56	



緯創資通 Wistron Corporation
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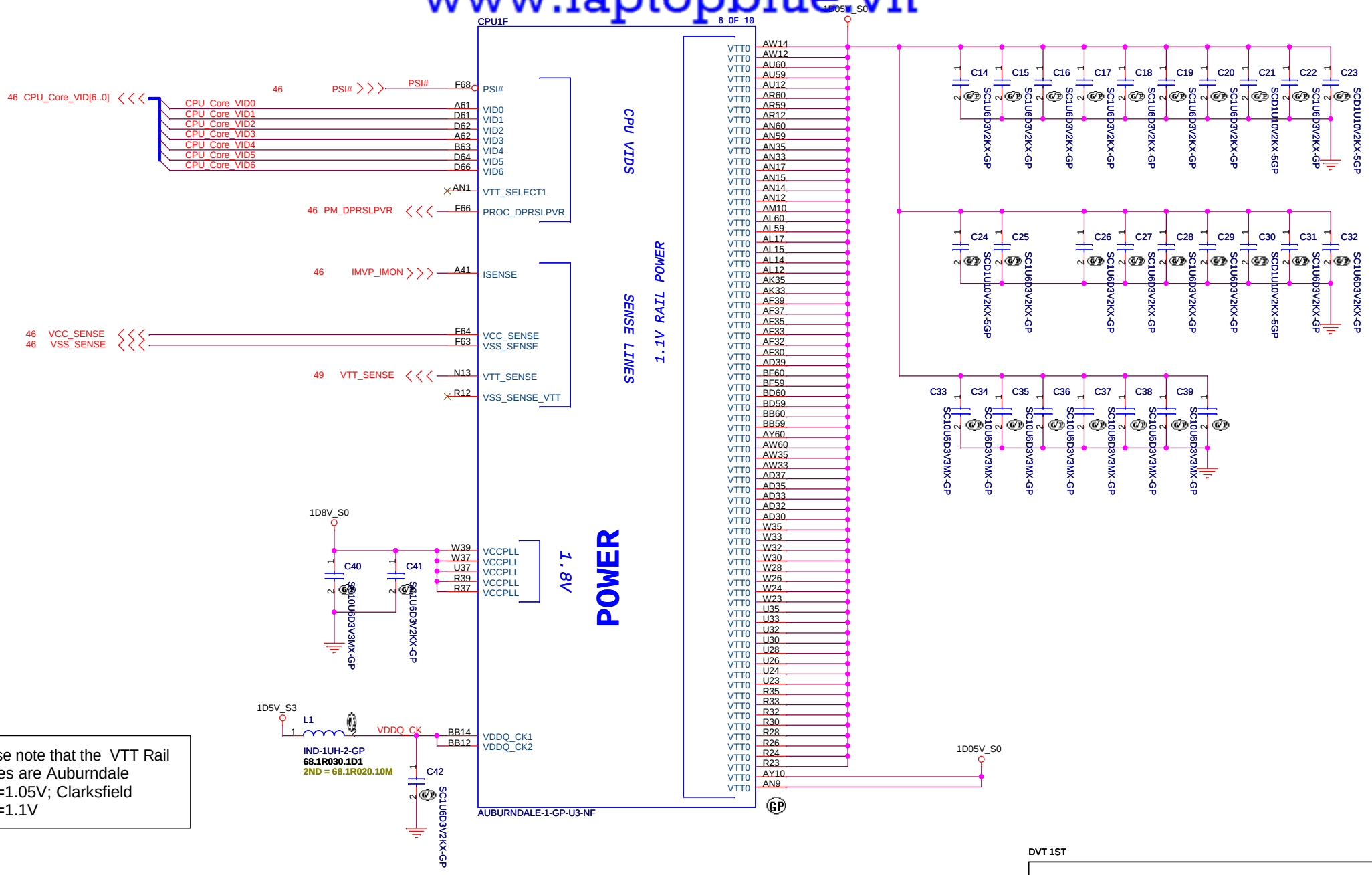
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU SFF 3 of 8(DDR)		
Size A3	Document Number TUCANA		Rev SB
Date: Wednesday, July 07, 2010	Sheet 6	of	56



Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V

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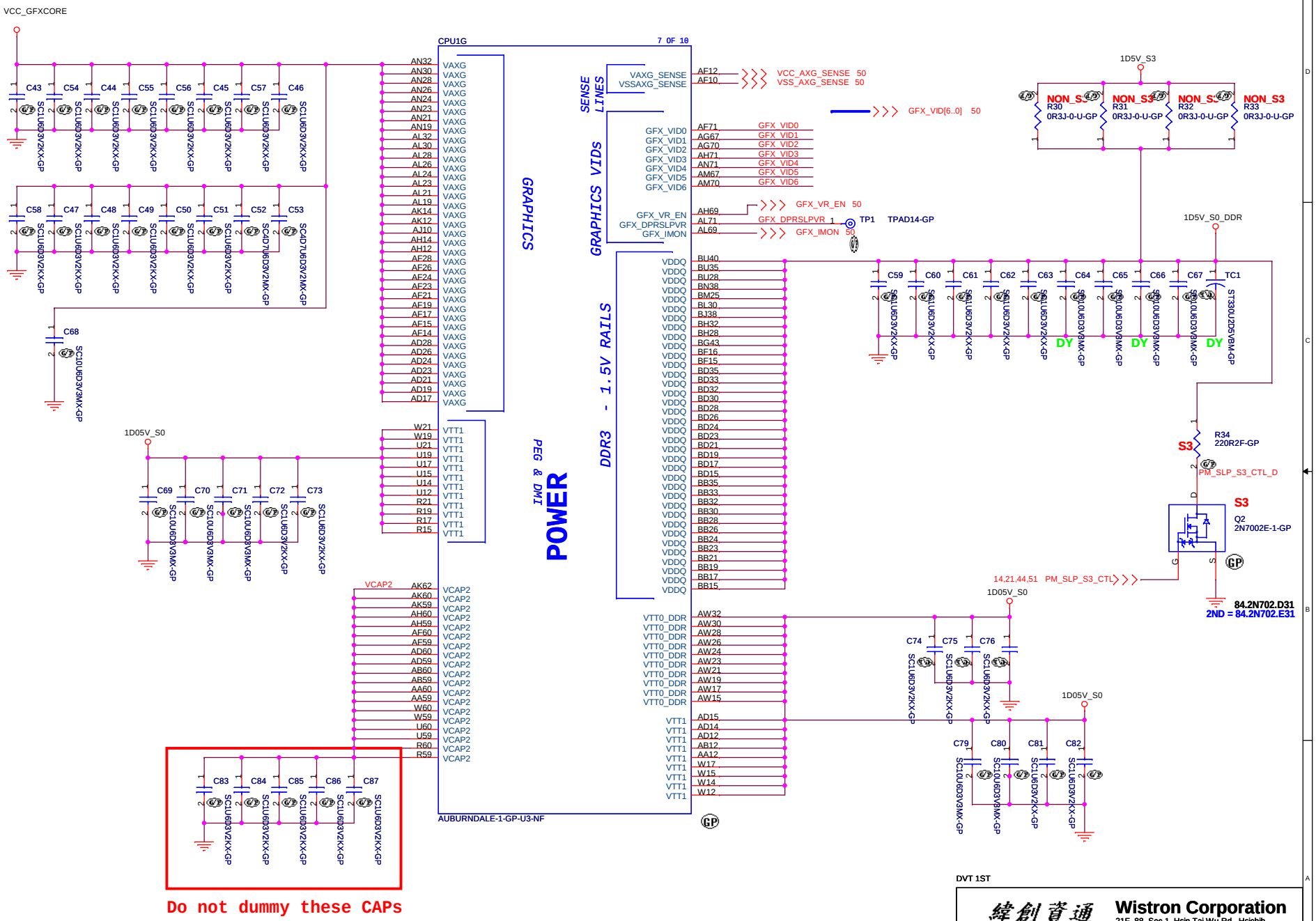
Title	CPU SFF 4 of 8(POWER/VTT)	
Size: Custom	Document Number: TUCANA	Rev: SB
Date: Wednesday, July 07, 2010	Sheet 7 of 56	



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緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	CPU SFF 5 of 8(PWR/DDR/GFX/)
Size A3	Document Number TUCANA Rev SB
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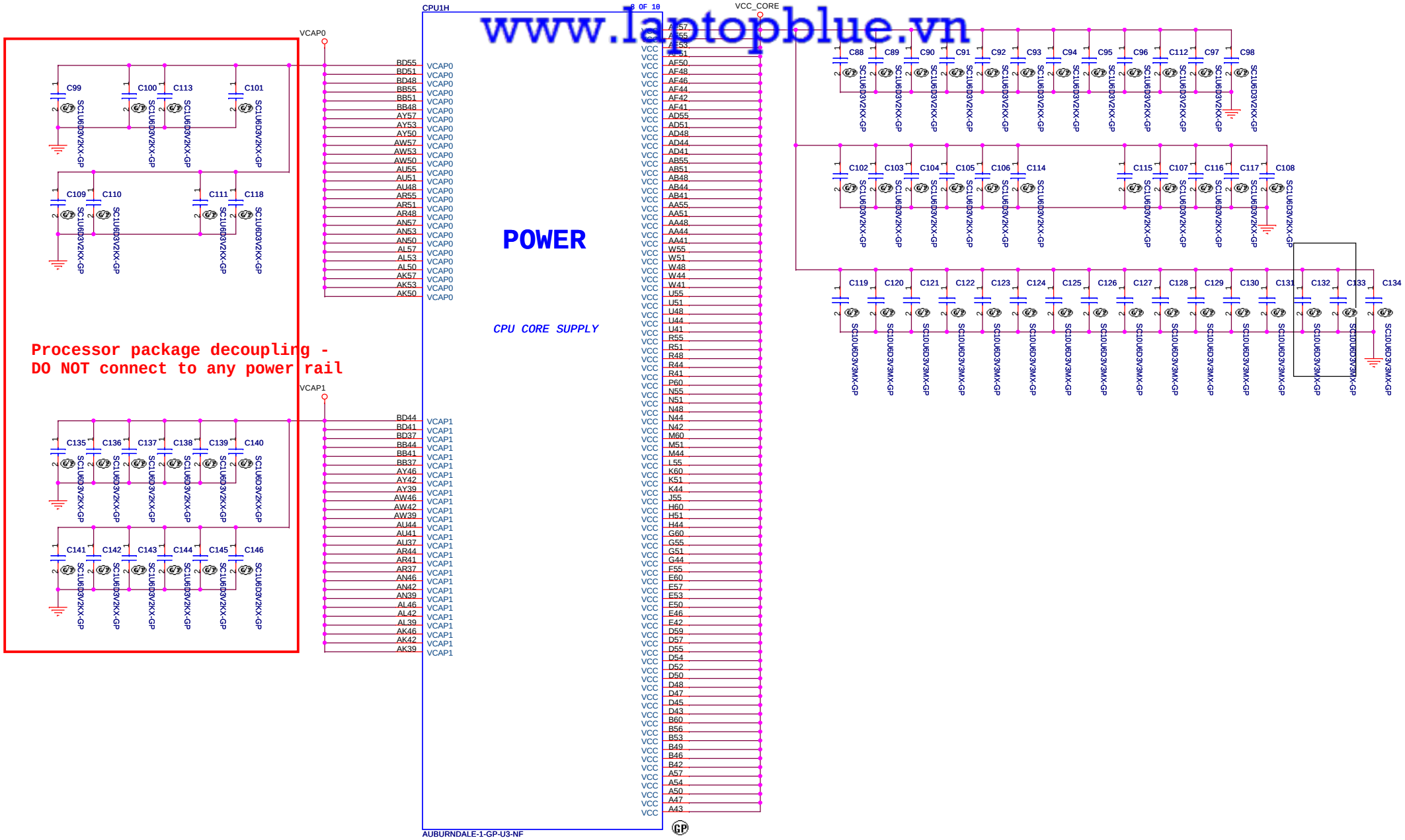

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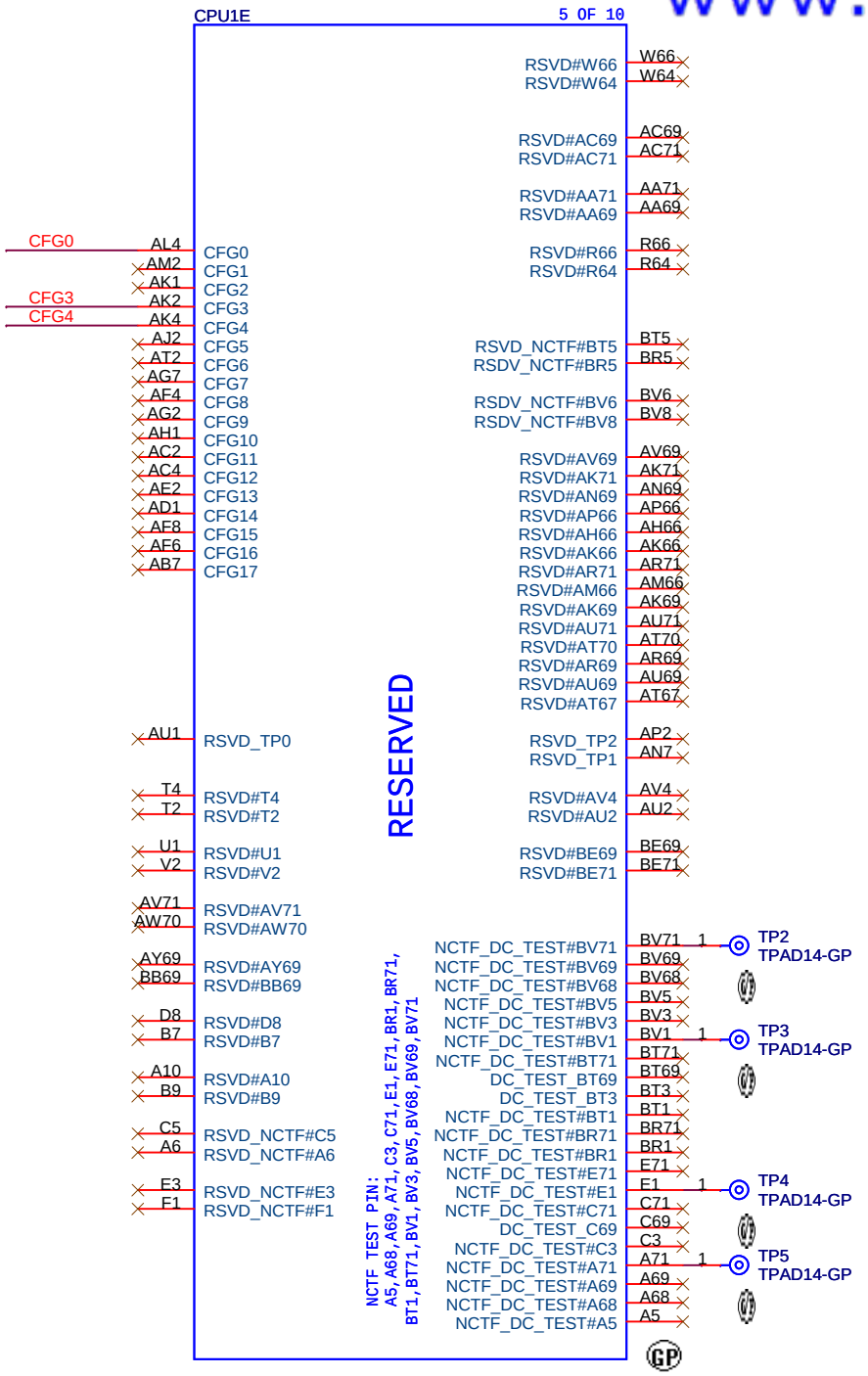
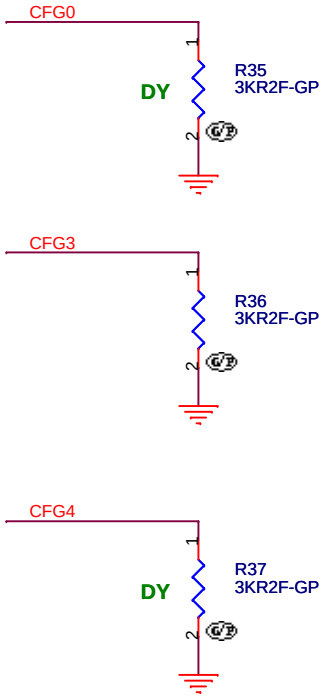
Title	CPU SFF 6 of 8(CPUCORE)	
Size A3	Document Number TUCANA	Rev SB
Date: Wednesday, July 07, 2010	Sheet 9 of 56	





PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

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Title: **CPU SFF 7 of 8(RESERVED)**

Size	Document Number	Rev
A4	TUCANA	SB

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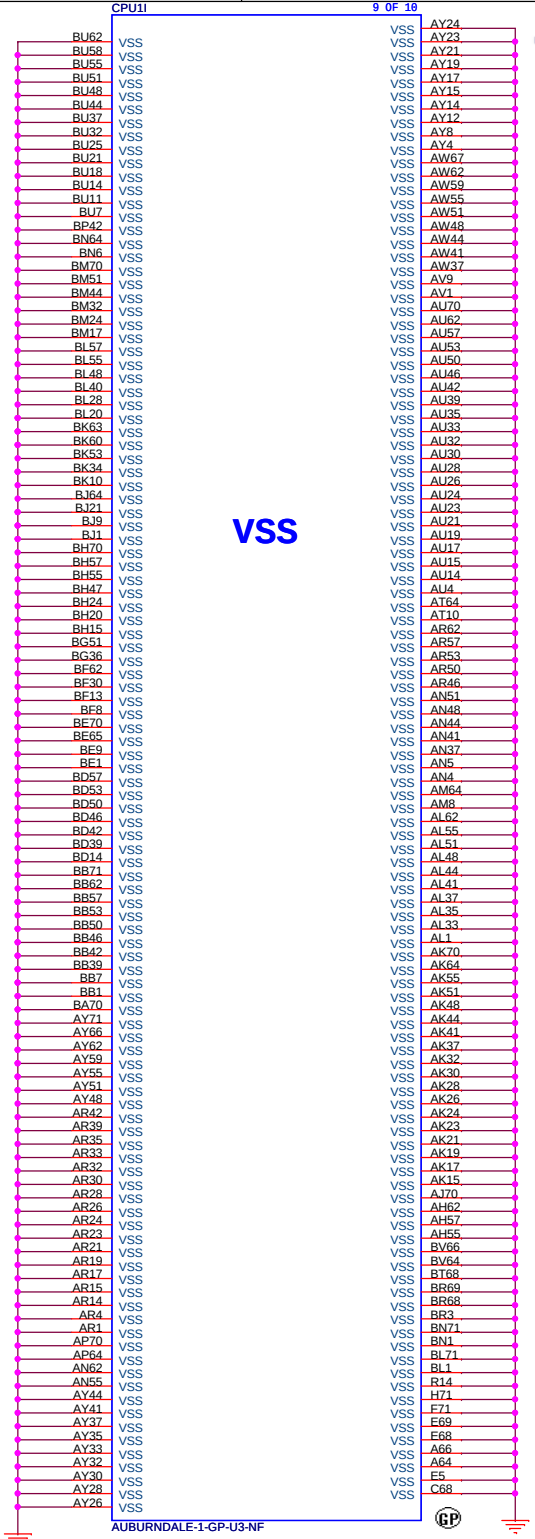

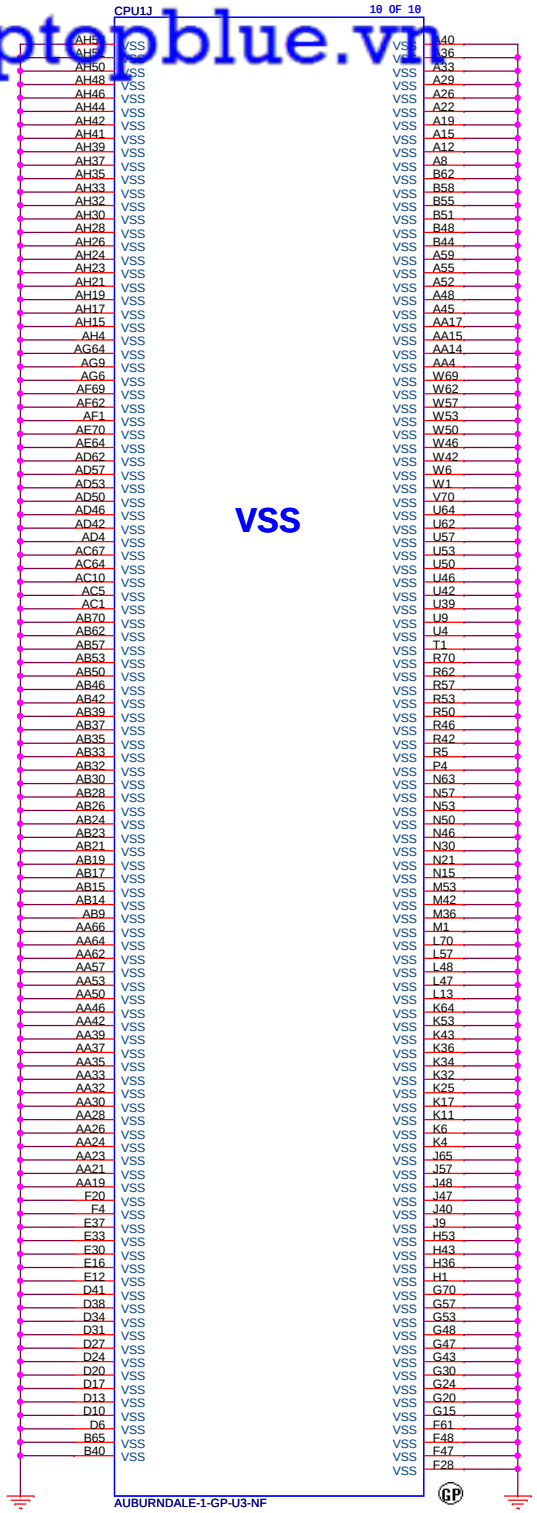

DVT 1ST

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Title	CPU SFF 8 of 8(VSS)	
Size A3	Document Number TUCANA	Rev SB
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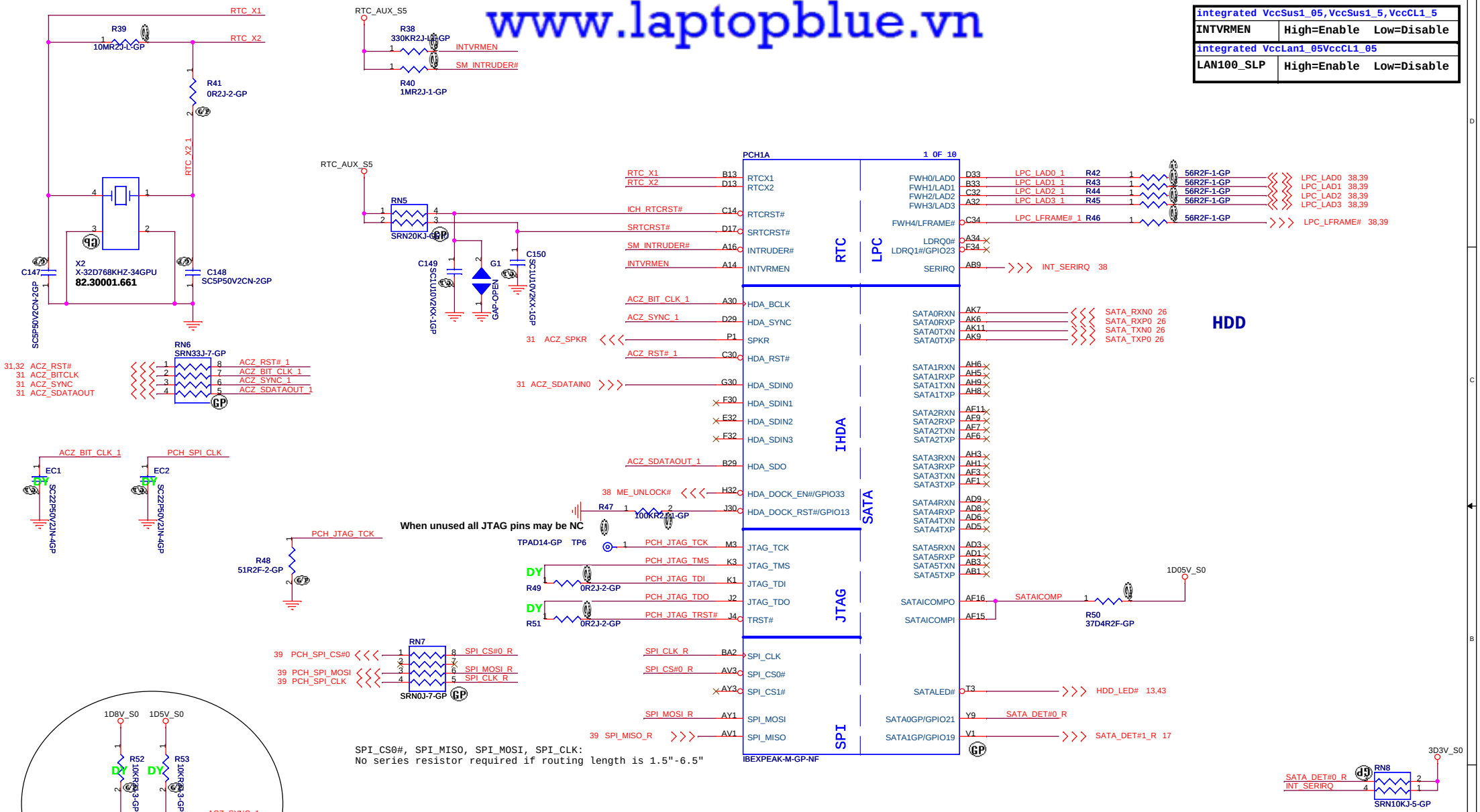
integrated VccSus1_05,VccSus1_5,VccCL1_5	
INTVRMEN	High=Enable Low=Disable
integrated VccLan1_05VccCL1_05	
LAN100_SLP	High=Enable Low=Disable



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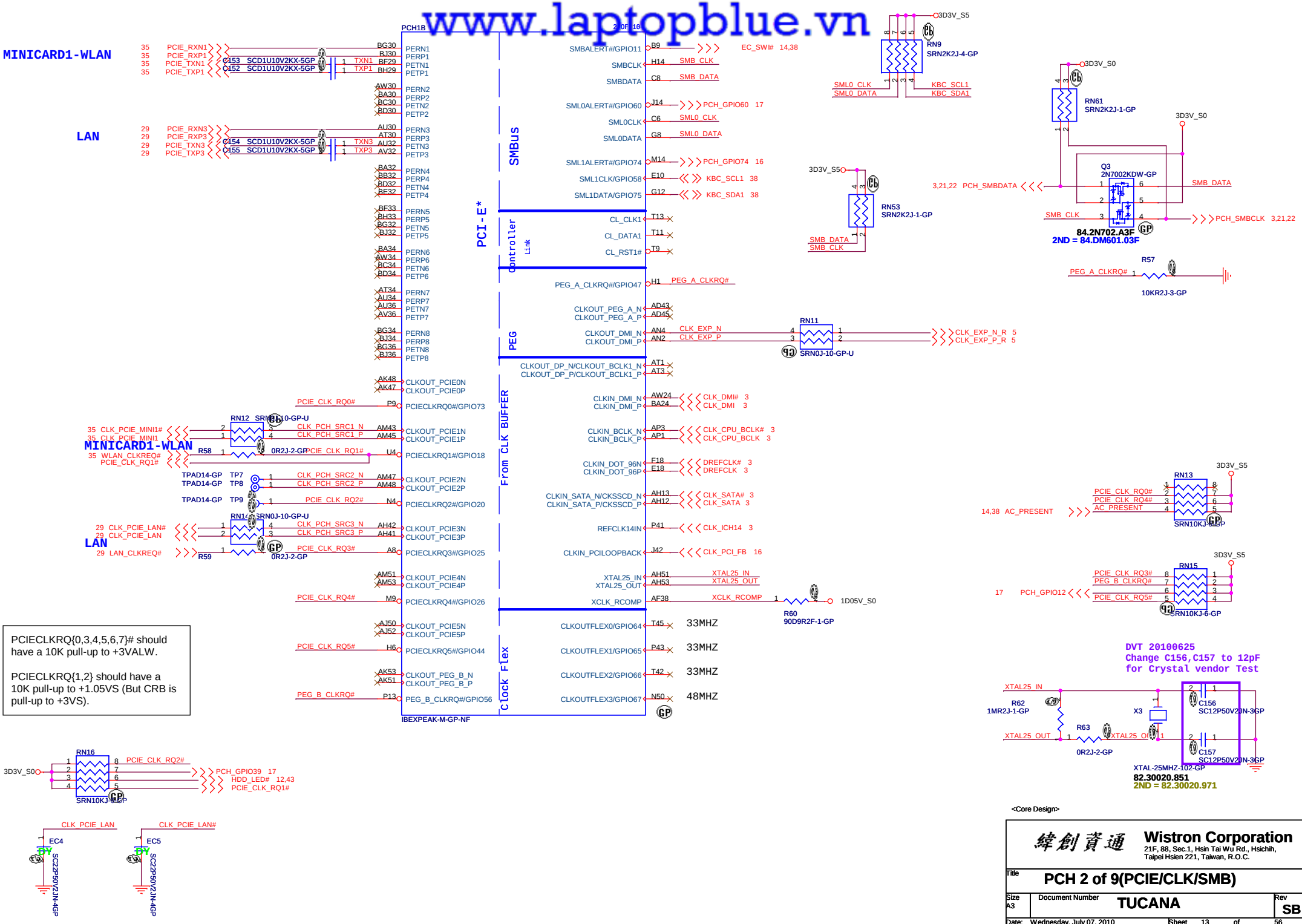
Title: PCH 1 of 9(SATA/RTC/HDA)

Size	Document Number	Rev
A3	TUCANA	SB

Date: Wednesday, July 07, 2010 Sheet 12 of 56



PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3VALW.

PCIECLKRQ{1,2} should have a 10K pull-up to +1.05VS (But CRB is pull-up to +3VS).

<Core Design>

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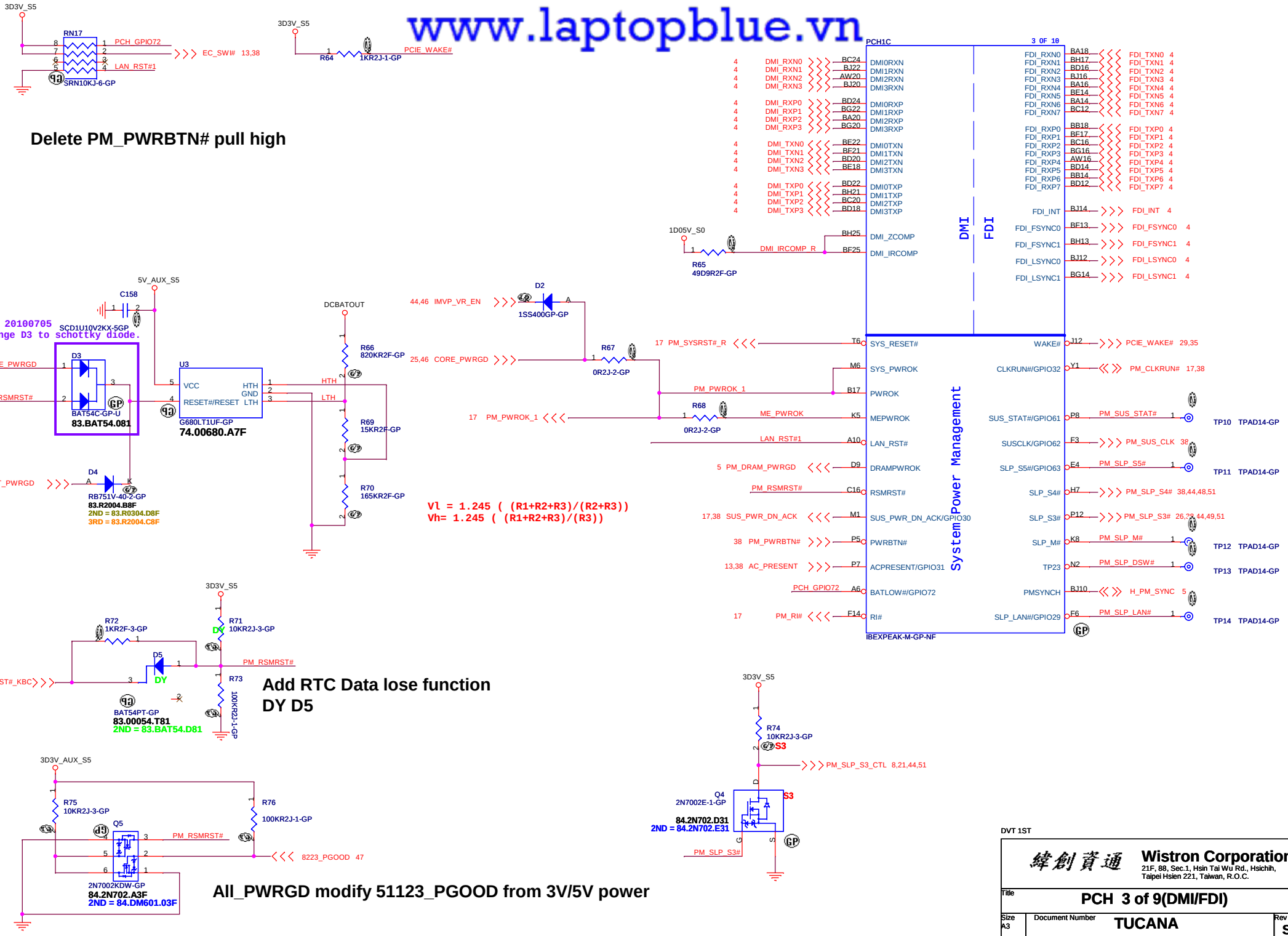
Title	PCH 2 of 9(PCIE/CLK/SMB)		
Size A3	Document Number TUCANA		Rev SB
Date: Wednesday, July 07, 2010	Sheet 13 of 56		



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Title	PCH 3 of 9(DMI/FDI)	
Size A3	Document Number TUCANA	Rev SB
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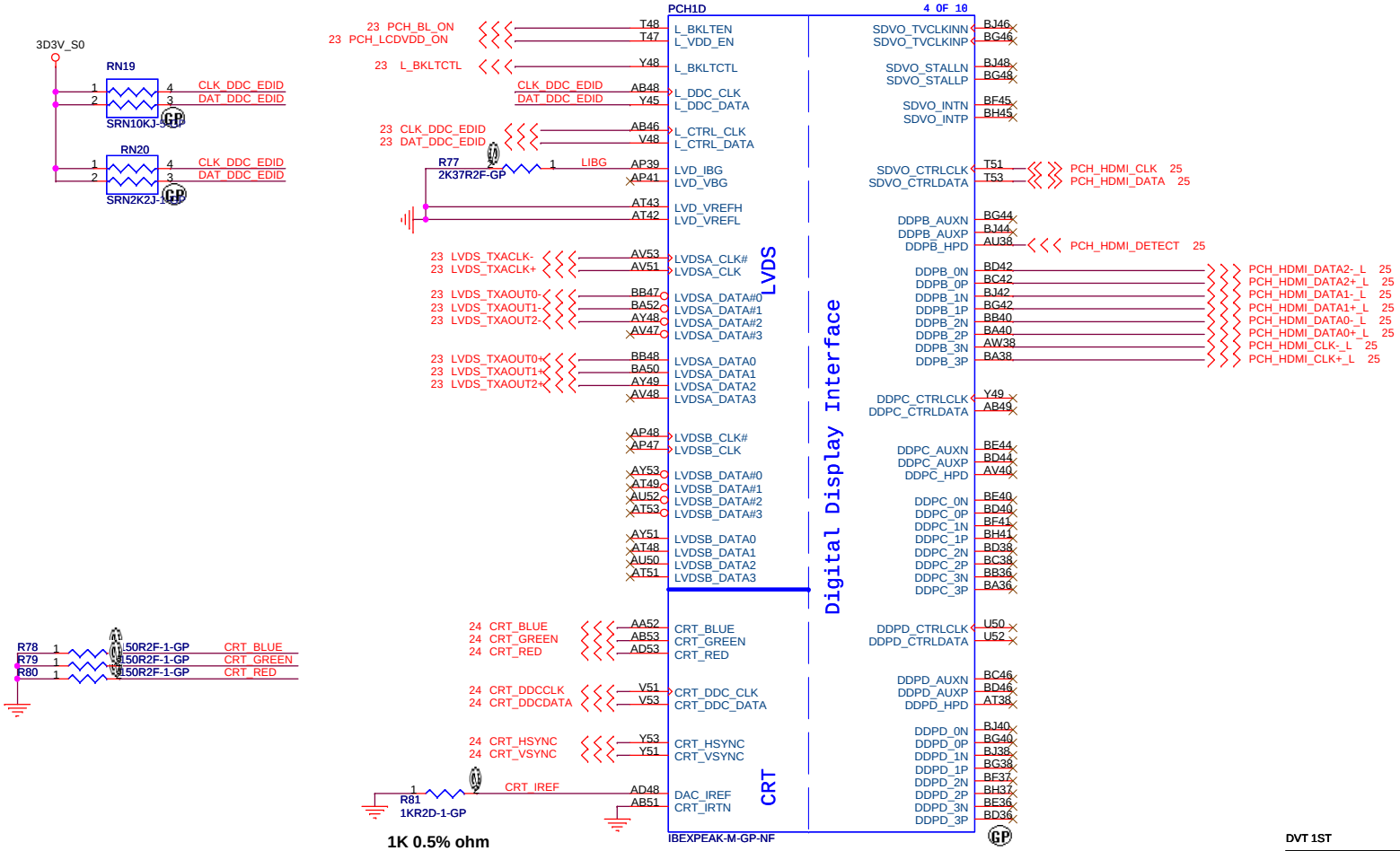
Panel backlight enable control for LVDS -
used to gate power into the backlight circuit



DVT 1ST

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Title: PCH 4 of 9(LVDS/CRT/DP)		
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3D3V_S0

RN21 SRN8K2J-4-GP
- PCI_PERR#
- PCI_PLOCK#
- PCI_DEVSEL#
- PCI_SERR#

RN22 SRN8K2J-4-GP
- INT_PIRQD#
- PCI_IRDY#
- PCI_STOP#
- INT_PIRQE#

RN23 SRN8K2J-4-GP
- PCI_REQ3#
- INT_PIRQF#
- INT_PIRQB#
- PCI_REQ0#

RN24 SRN8K2J-4-GP
- INT_PIRQH#
- PCI_TRDY#
- PCI_FRAME#
- PCI_REQ1#

RN25 SRN8K2J-4-GP
- PCI_REQ2#
- INT_PIRQC#
- INT_PIRQA#
- INT_PIRQG#

PCI_GNT0# — R82 1KR2J-1-GP (DY)
PCI_GNT1# — R83 1KR2J-1-GP (DY)
USE SPI

DVT 20100621
Add PCI_REQ2# Pull-High to 3D3V_S0
by hang-up issue

These pins are left as NC, because the function is disable.

These pins are left as NC, because the function is disable.

PCH1E — 5 OF 10

PCI: AD0–AD31, C/BE0#–C/BE3#, PIRQA#–PIRQD#, REQ0#–REQ3#, GNT0#–GNT3#, PIRQE#/GPIO2–PIRQH#/GPIO5, PCIRST#, SERR#, PERR#, IRDY#, PAR, DEVSEL#, FRAME#, PLOCK#, STOP#, TRDY#, PME#, PLTRST#, CLKOUT_PCI0–CLKOUT_PCI4

NVRAM: NV_CE#0–NV_CE#3, NV_DQS0, NV_DQS1, NV_DQ0/NV_IO0–NV_DQ15/NV_IO15, NV_ALE, NV_CLE, NV_RCOMP, NV_RB#, NV_WR#0_RE#, NV_WR#1_RE#, NV_WE#_CK0, NV_WE#_CK1

USB: USBP0N–USBP13N, USBP0P–USBP13P, USBRBIAS#, USBRBIAS, OC0#/GPIO59–OC7#/GPIO14

IBEXPEAK-M-GP-NF

PCI_SERR# — R84 22D6R2F-L1-GP

PLT_RST# — R85 100KR2J-1-GP (DY)

PCLK_FWH — R259 22R2F-1-GP — CLK_PCI_SIO_R
CLK_PCI_FB — R260 22R2F-1-GP — CLK_PCI_FB_R
CLK_PCI_KBC — R86 47R2J-2-GP — CLK_PCI_KBC_R

PCLK_FWH — EC6 (DY) SC22P50V2JN-4GP

RN28 SRN10KJ-6-GP: USB_OC#1, USB_OC#3, USB_OC#7, USB_OC#0

RN27 SRN10KJ-6-GP: USB_OC#4, USB_OC#2, USB_OC#5

USB Table

Pair	Device
0	External #0
1	External #1
2	CardReader
3	NC
4	External #2
5	NC
6	NC
7	NC
8	WLAN/WiMAX
9	CAMERA(HS)
10	NC
11	NC
12	BLUETOOTH(FS)
13	NC

BOOT BIOS Strap

PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC(Default)
1	0	Reserved
0	1	PCI
1	1	SPI

DVT 1ST

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Title: PCH 5 of 9(PCI/USB)
Size: A3 | Document Number: TUCANA | Rev: SB
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GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.

PCH1F 6 OF 10

IBEXPEAK-M-GP-NF

NCTF TEST PIN:
A4, A49, A5, A50, A52, A53, B2, B53, BE1,
BE53, BF1, BF53, BH1, BH53, BJ1, BJ2, BJ4,
BJ49, BJ5, BJ50, BJ52, BJ53, D1, D53, E1, E53

DVT 20100629

To CPU

DVT 1ST

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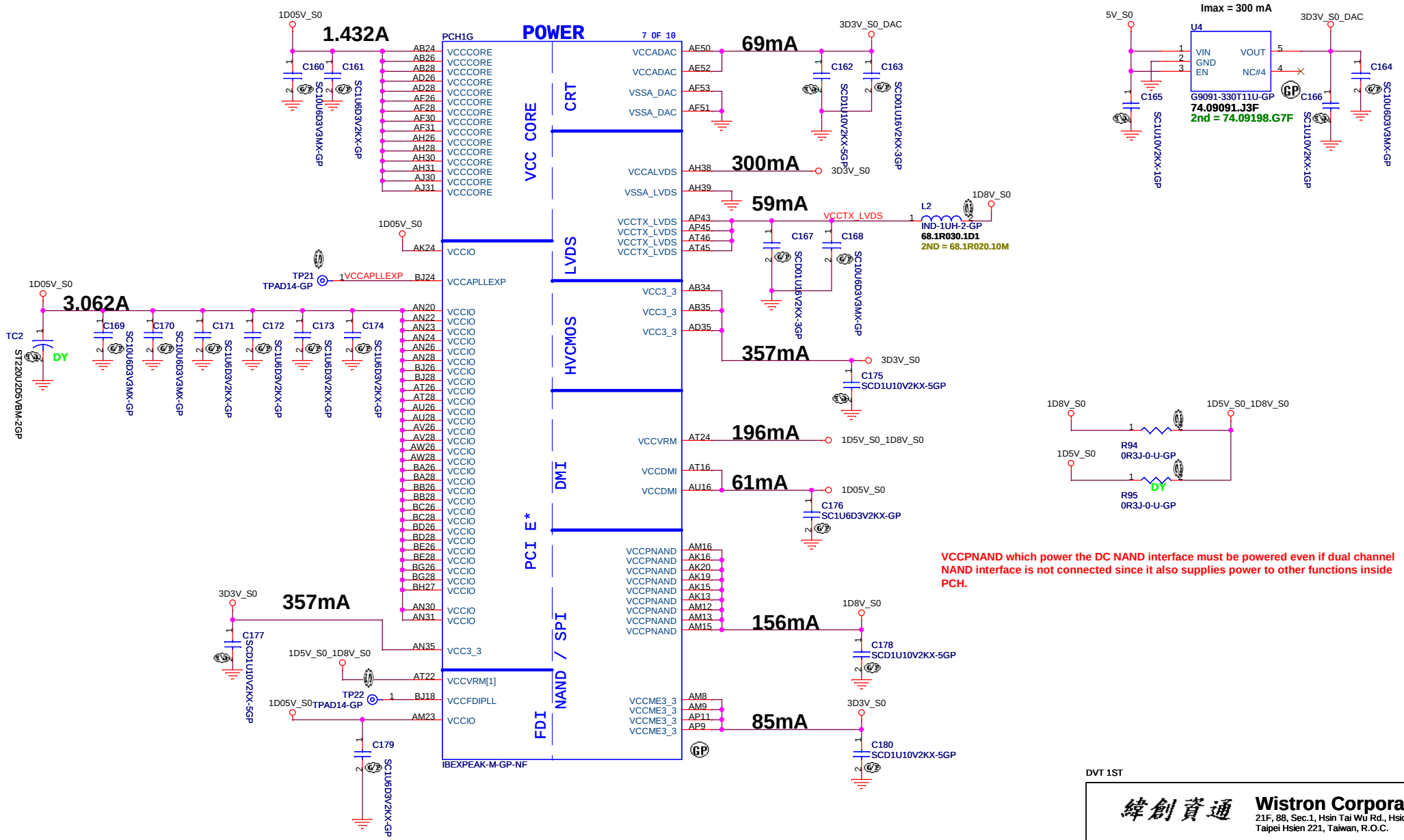
Title: PCH 6 of 9(GPIO/RSVD)		
Size: A3	Document Number: TUCANA	Rev: SB
Date: Wednesday, July 07, 2010	Sheet 17 of 56	



VCCPNAND which power the DC NAND interface must be powered even if dual channel NAND interface is not connected since it also supplies power to other functions inside PCH.

DVT 1ST

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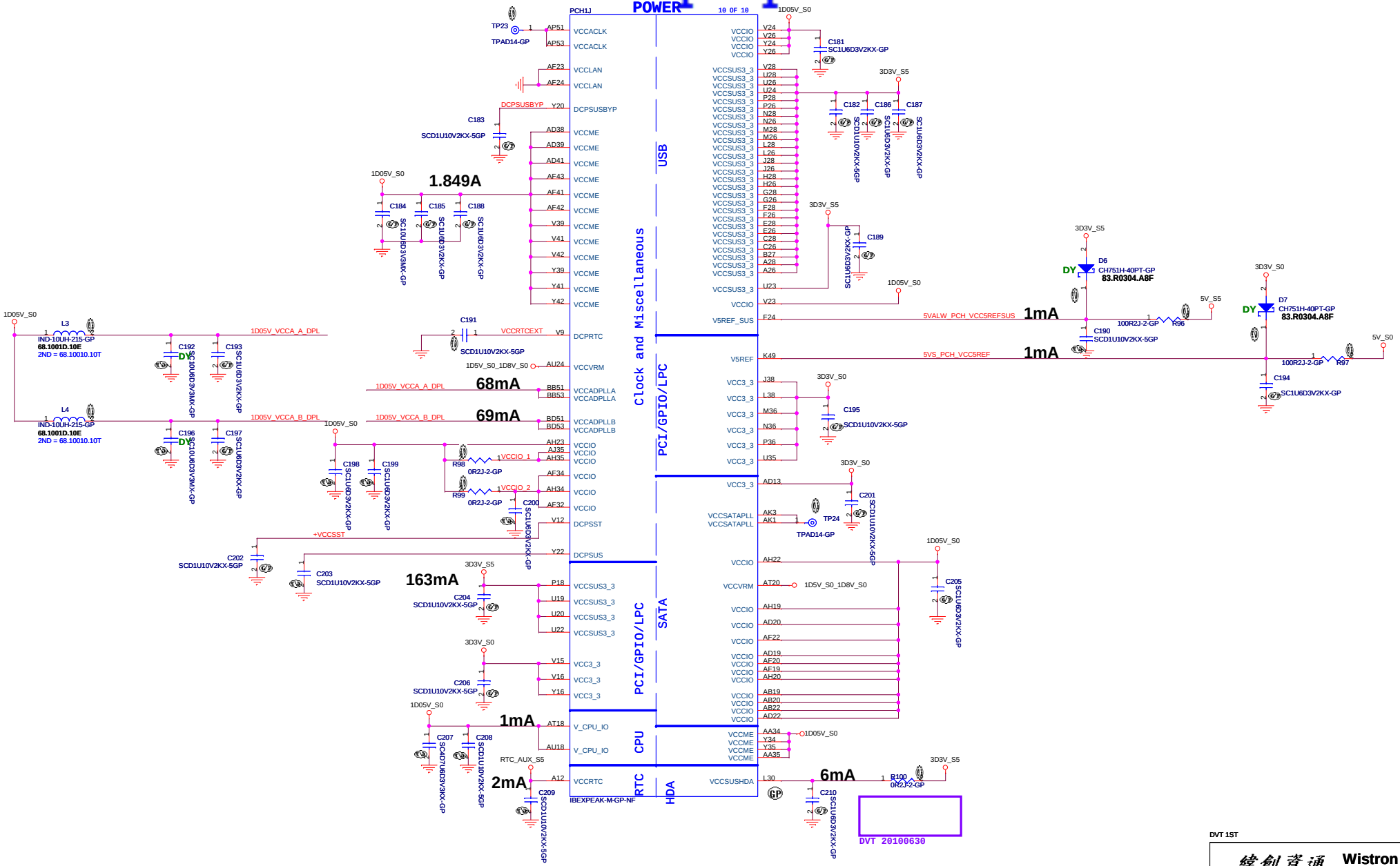
Title	**PCH 7 of 9(PWR/VCORE/LVDS)**
Size: Custom	Document Number: **TUCANA**
Rev	**SB**
Date: Wednesday, July 07, 2010	Sheet 18 of 56



DVT 1ST

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	PCH 8 of 9(PWR\SATA\USB)	
Size: Custom	Document Number: TUCANA	Rev: SB
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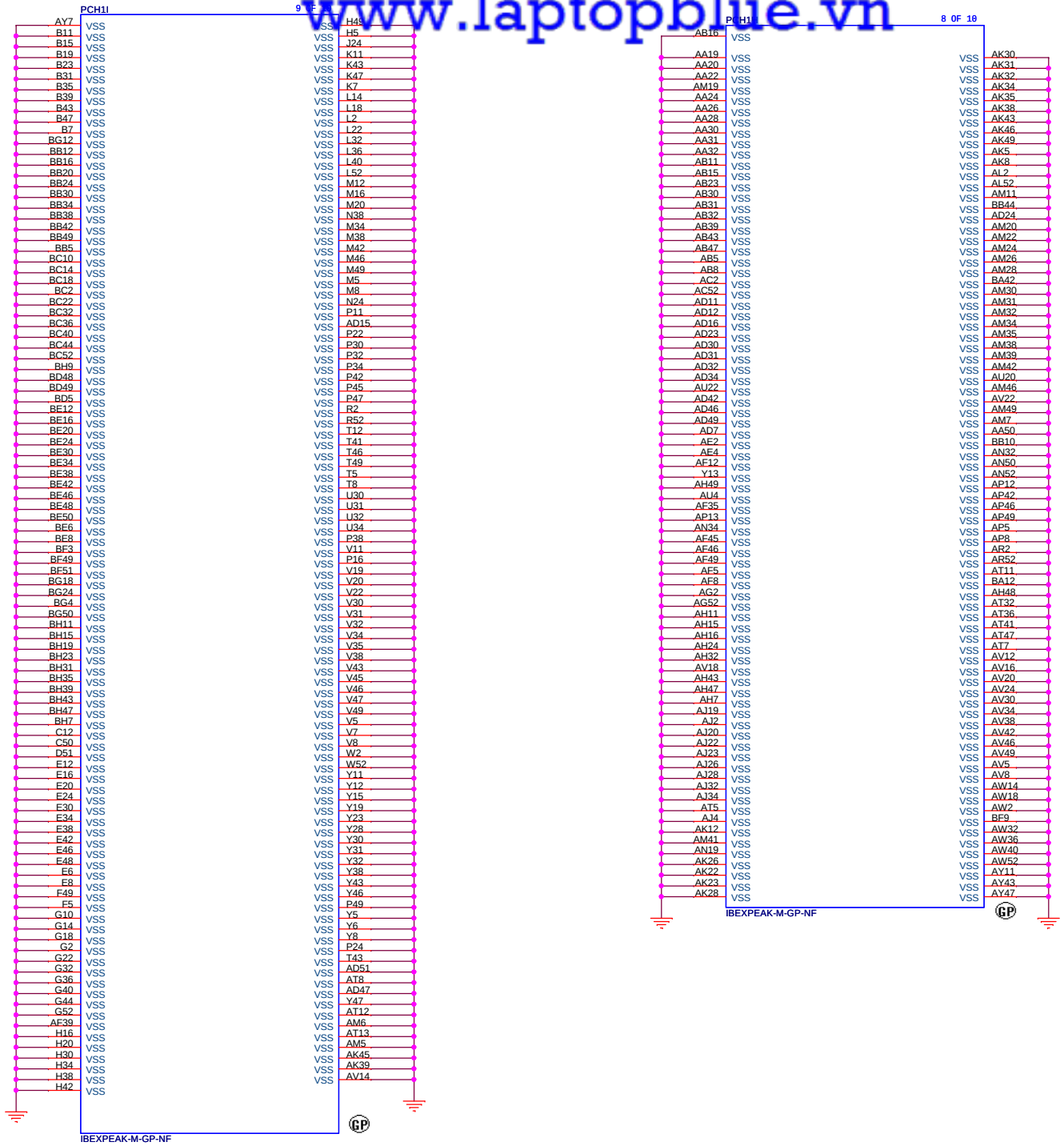

DVT 1ST

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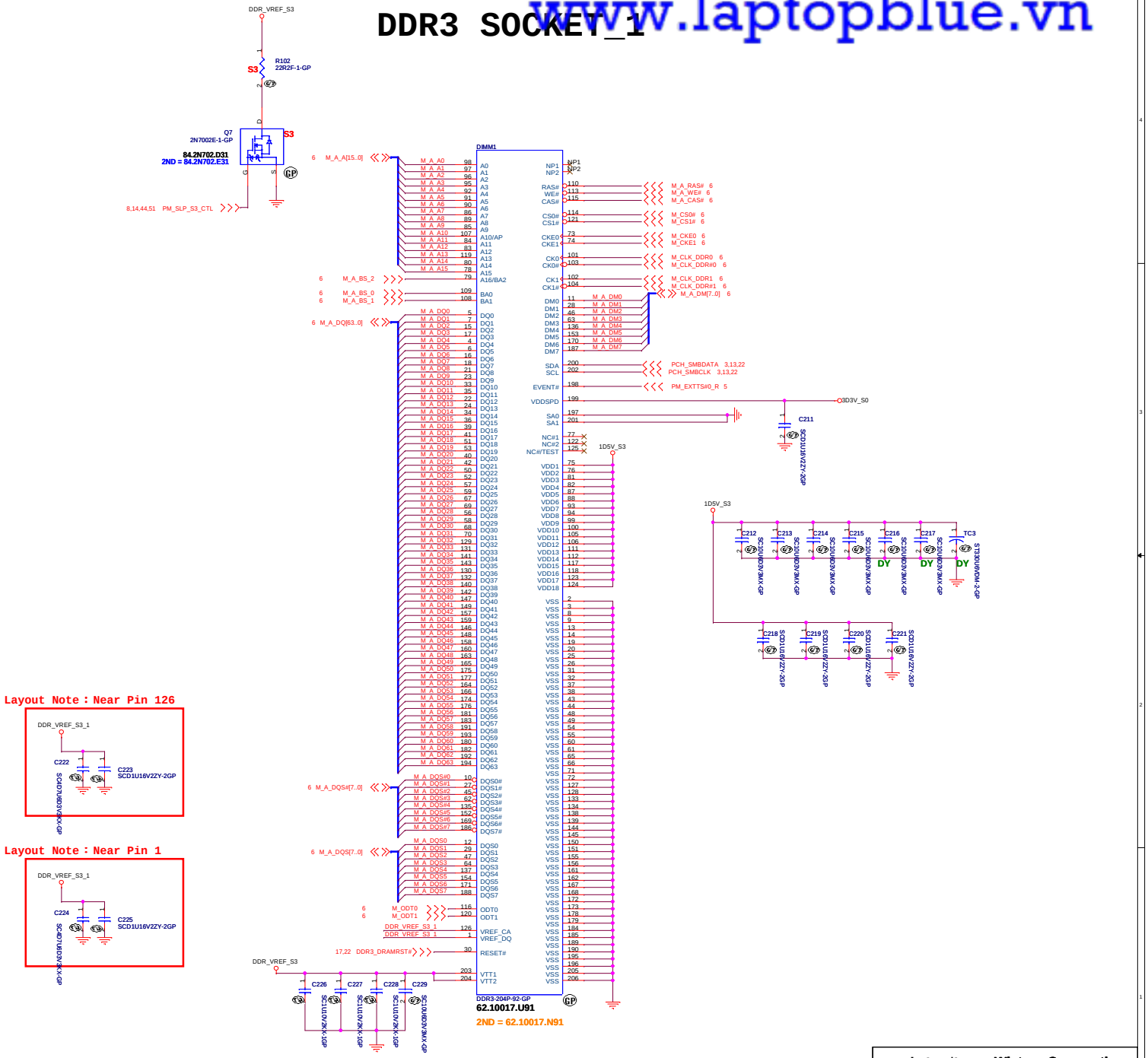
Title: **PCH 9 of 9(VSS)**

Size	Document Number	Rev
A3	TUCANA	SB

Date: Wednesday, July 07, 2010 Sheet 20 of 56

DDR3 SOCKET_1

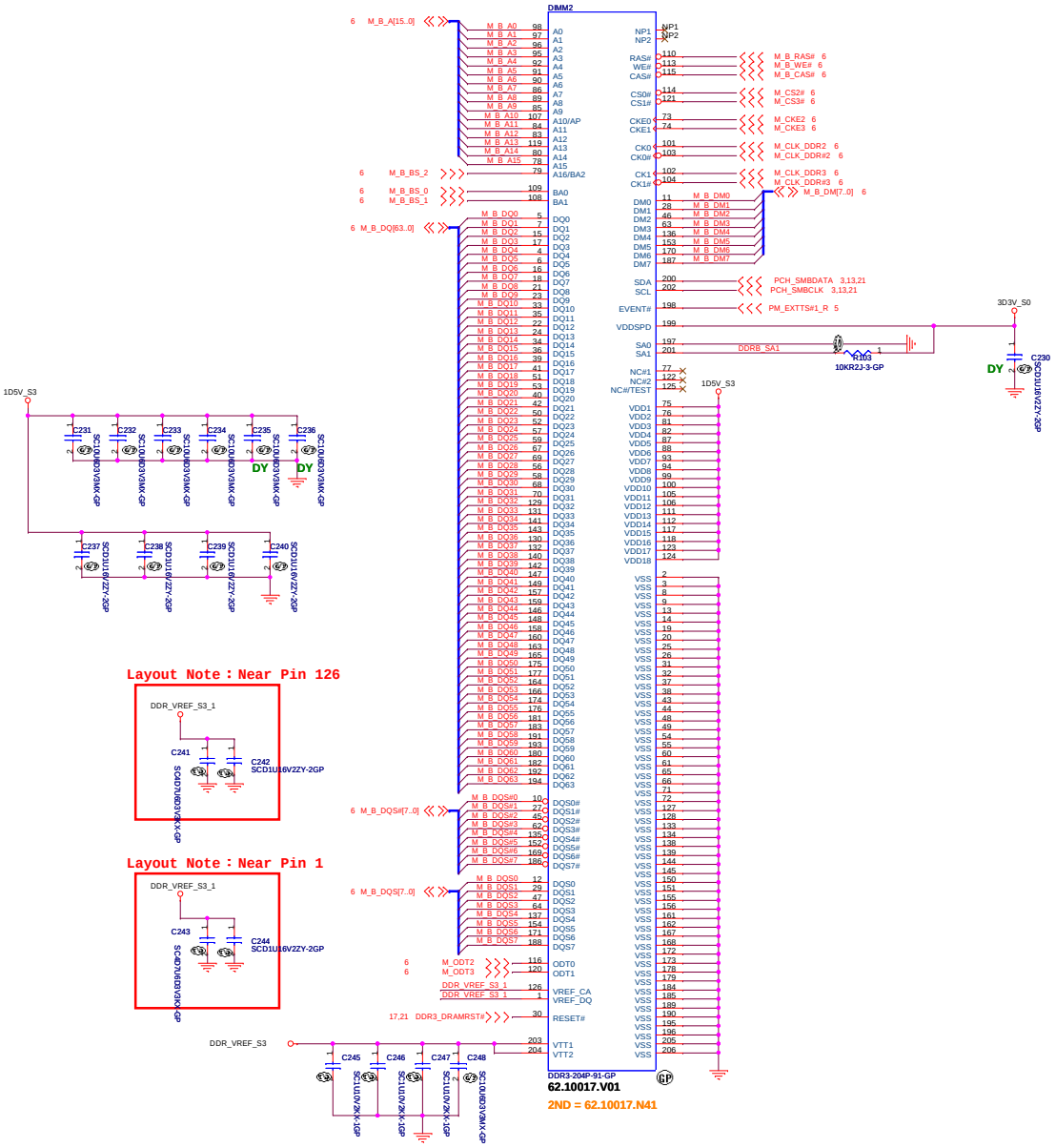


Layout Note : Near Pin 126

Layout Note : Near Pin 1

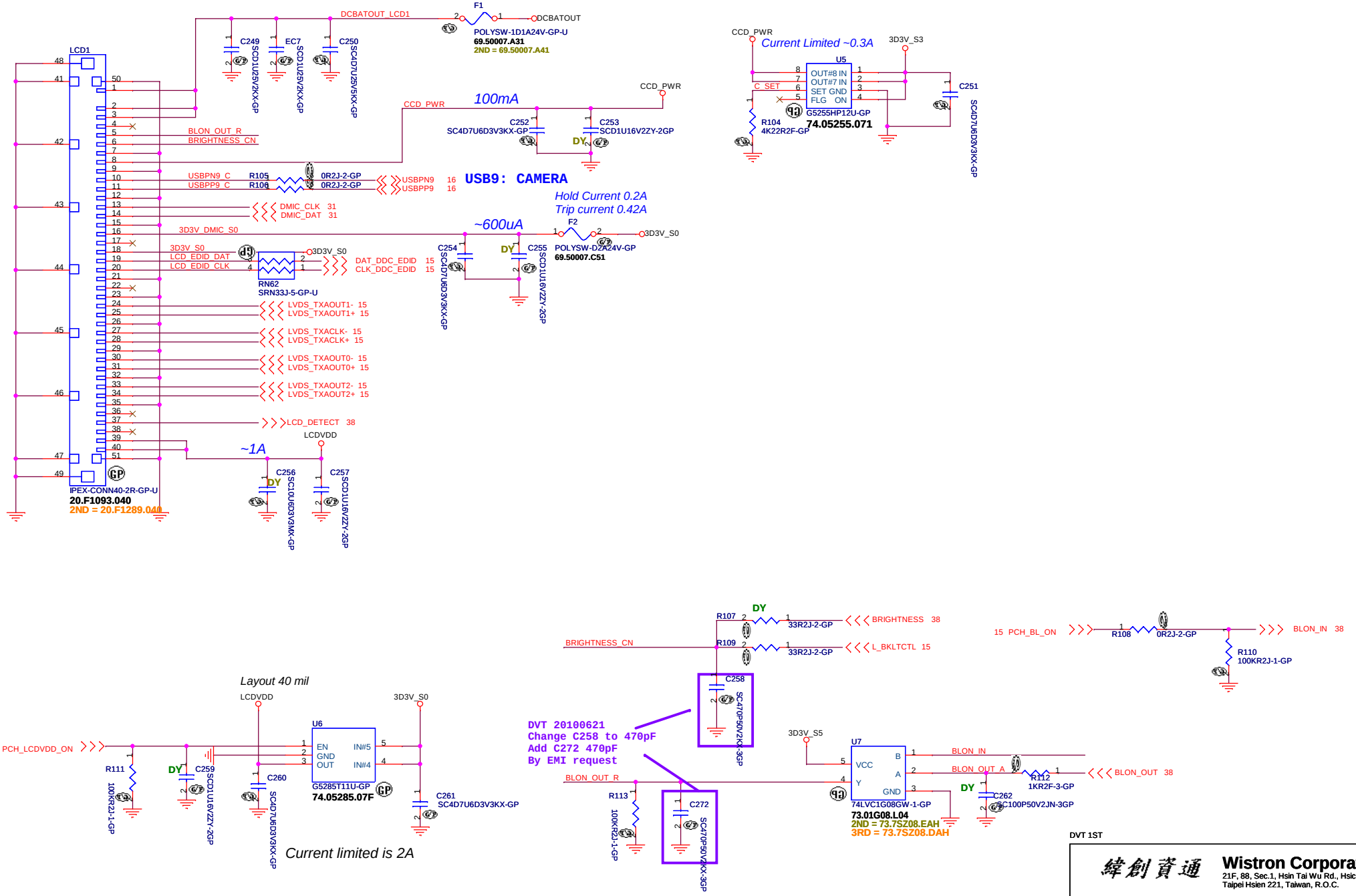
緯創資通 Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DDR3 Socket1		
Size	Document Number: TUCANA	Rev: SB
Date: Wednesday, July 07, 2010	Sheet 21 of 56	

DDR3 SOCKET_2



緯創資通	Wistron Corporation		
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	DDR3 Socket2		
Size	Document Number	Rev	
	TUCANA	SB	
Date: Wednesday, July 07, 2010	Sheet 22 of 56		

LCD/CCD CONN



DVT 1ST

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**LCD CONN**
Size	Document Number: **TUCANA** — Rev: SB
Date: Wednesday, July 07, 2010	Sheet 23 of 56

Layout Note:
Place these resistors close to the CRT-out connector

Ferrite bead impedance: 40 ohm@100MHz

15 CRT_RED
15 CRT_GREEN
15 CRT_BLUE

CRT_RED
CRT_GREEN
CRT_BLUE

L5 SBK160808T-4[DY]-N-GP
L6 SBK160808T-4[DY]-N-GP
L7 SBK160808T-4[DY]-N-GP
68.00119.241
2ND = 68.00909.151

CRT_R
CRT_G
CRT_B

R116 150R2F-1-GP
R117 150R2F-1-GP
R118 150R2F-1-GP

C264 C265 C266 C267 C268 C269
SC5P50V2CN-2GP

3D3V_S0
5V_S0
5V_CRT_S0

C263 SCD1U16V2ZY-2GP
U8
CM2009-02QR-GP
83.02009.BA0

VCC_SYNC
VCC_VIDEO
VCC_DDC
VIDEO_1
VIDEO_2
VIDEO_3
BYP
DDC_IN1
DDC_IN2
DDC_OUT1
DDC_OUT2
SYNC_IN1
SYNC_IN2
SYNC_OUT1
SYNC_OUT2
GND

C270 SCD22U10V2KX-1GP

R114 R115 2K7R2J-GP

DVT 20100621
Change R114,R115,R119,R120 to 2.7K ohm for CRT VEVS report

CRT_DDCCLK 15
CRT_DDCDATA 15
CLK_DDC1_5
DAT_DDC1_5
CRT_HSYNC 15
CRT_VSYNC 15
CRT_HSYNC_R
CRT_VSYNC_R
CRT_HSYNC1
CRT_VSYNC1

RN35 SRN33J-5-GP-U

R119 2K7R2J-GP
R120 2K7R2J-GP

EC122 EC123 SCD01U50V2KX-1GP

Layout Note:
** Must be a ground return path between this ground and the ground on the VGA connector.*
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

CRT I/F & CONNECTOR

6 1 7 2 8 3 9 4 10 5

EC8 EC9 SCD1U16V2ZY-2GP

CRT1
D-SUB-15-76-GP
20.20891.015
2ND = 20.20886.015

NC#4
NC#11
VCC_CRT
DDCDATA_ID1
DDCCLK_ID3
CRT_RED
CRT_GREEN
CRT_BLUE
VSYNC
HSYNC
GND

~300mA

D8 CH551H-30PT-GP
83.R5003.C8F
2ND = 83.5R003.08F
3RD = 83.R5003.H8H

F6 POLYSW-40A60V-GP
69.44002.001

DVT 20100601
Change F6 to 69.44002.001, for Cadiz use

C273 SCD01U50V2KX-1GP

C274 C275 C276 C277 DY
SC18P50V2JN-1-GP

DVT 1ST

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Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT CONN
Size:
Document Number: TUCANA
Rev: SB
Date: Wednesday, July 07, 2010
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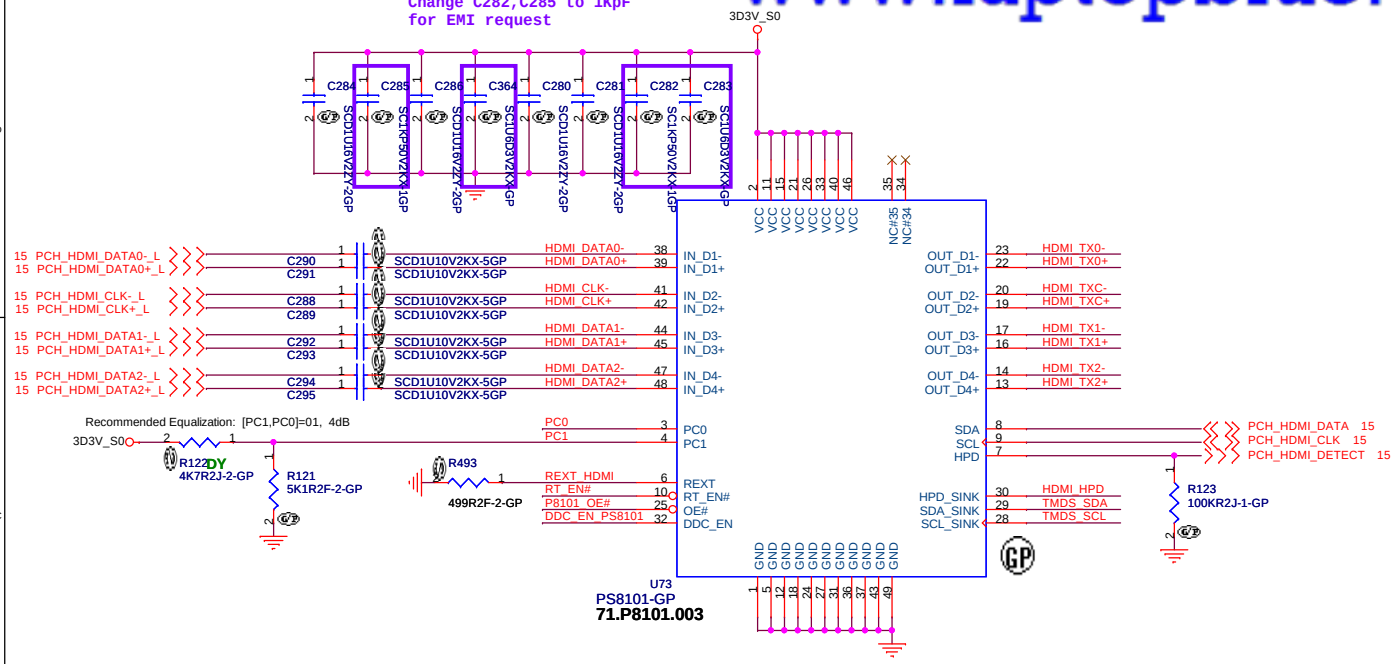
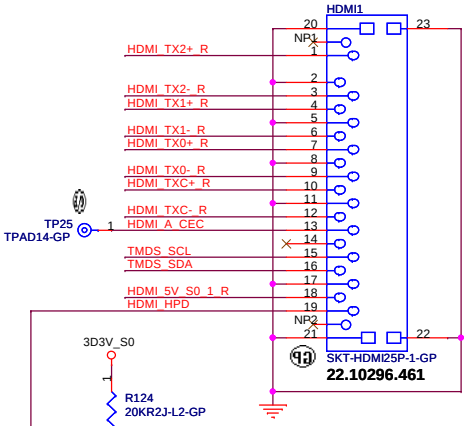
DVT 20100611
Change C283,C364 to 1uF
Change C282,C285 to 1KpF
for EMI request

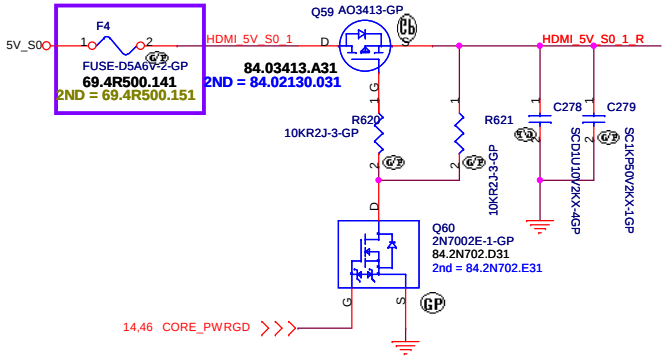


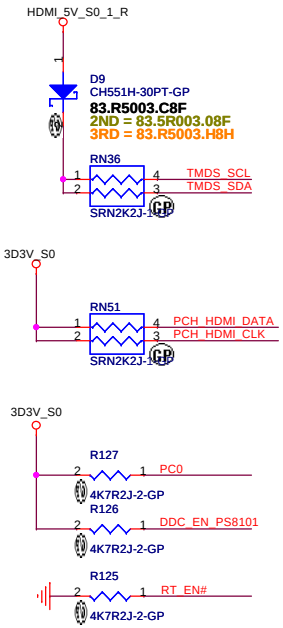


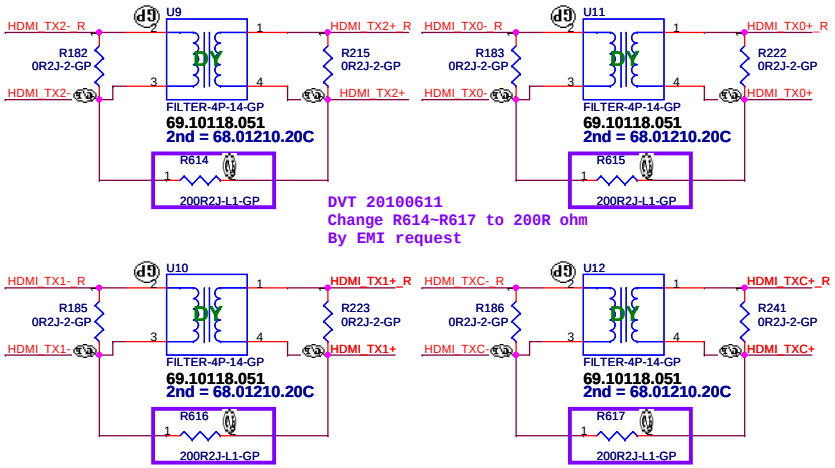
HDMI in : Hi
HDMI out : Low

DVT 20100630
Change Q12 to 84.2N702.D31
(ESD Protected 1.0KV)

DVT 20100517
change 2nd source to 69.4R500.151







DVT 20100611
Change R614~R617 to 200R ohm
By EMI request

DVT 1ST

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI CONN
Size: | Document Number: TUCANA | Rev: SB
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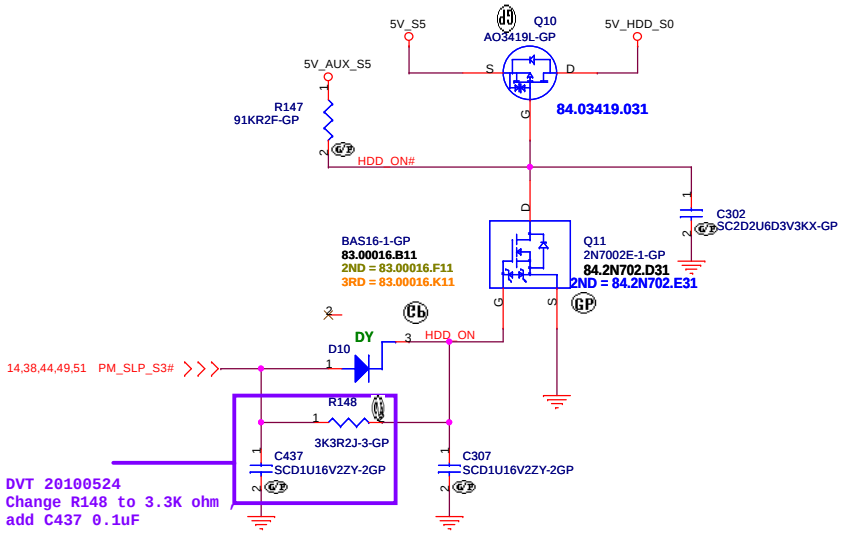
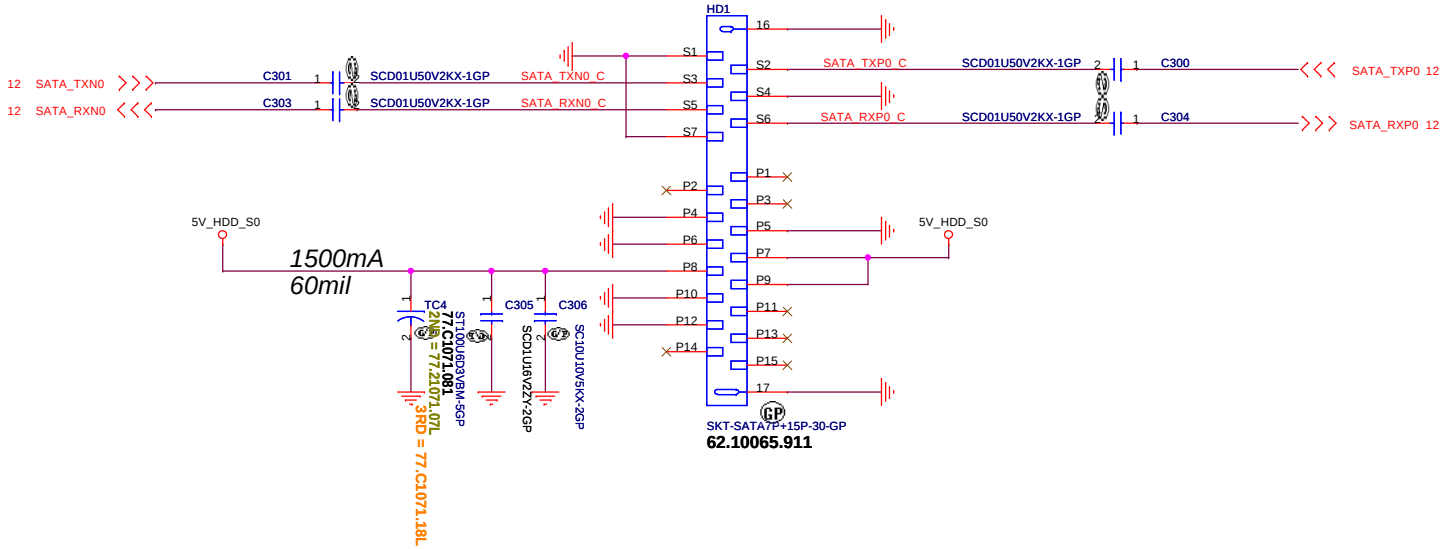


Delay HDD power off timing for 400ms after SATA controller shut down. Control the C307 and R148 to finally tune delay timing between 500ms and 400ms.

SSD SATA Connector



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD Connector

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	TUCANA	SB

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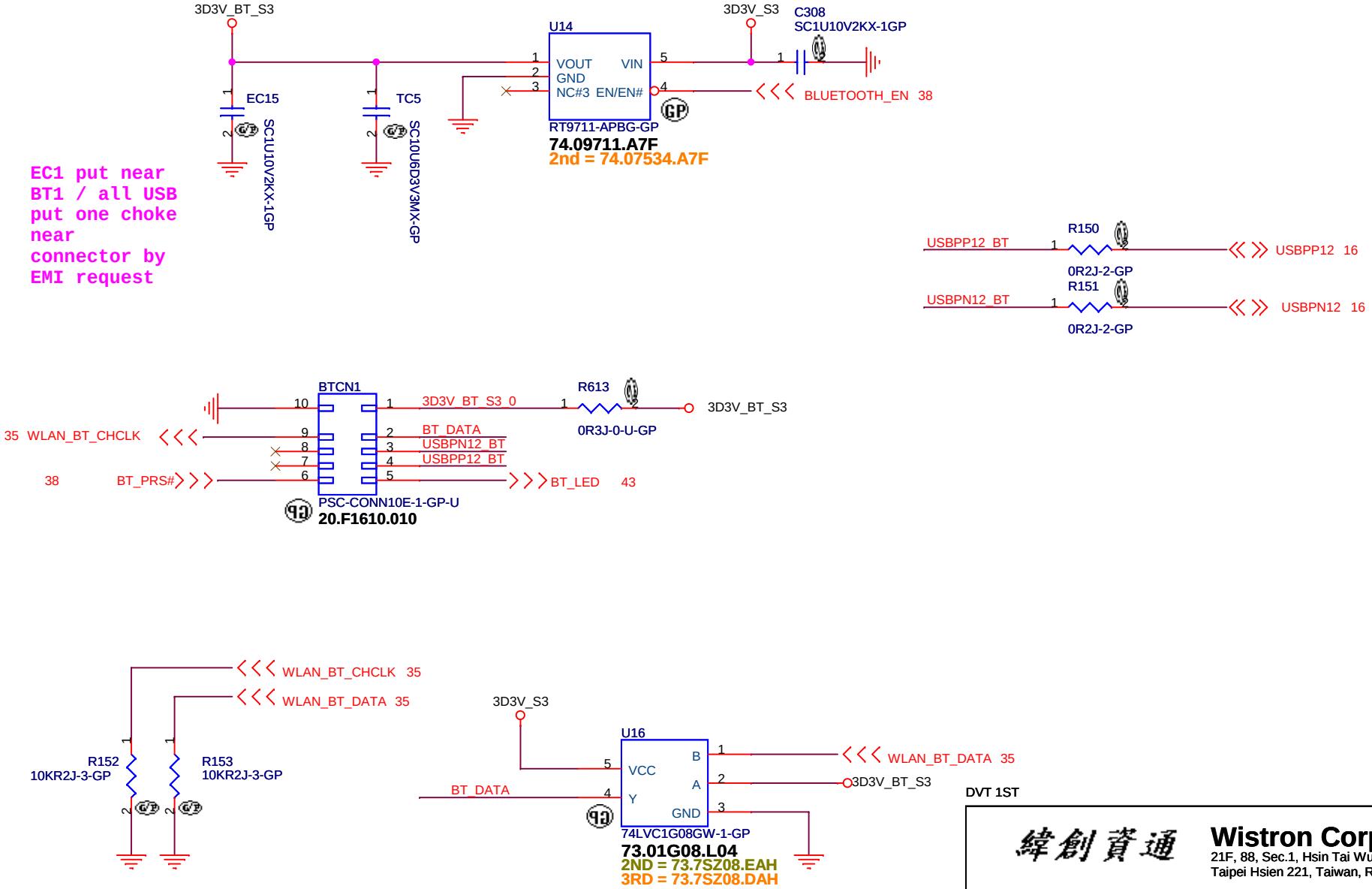
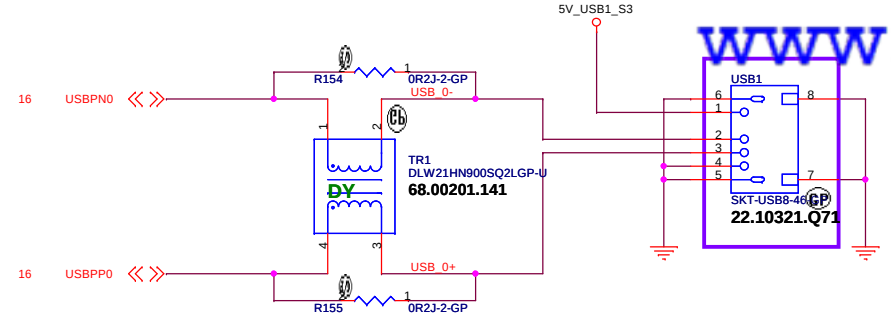
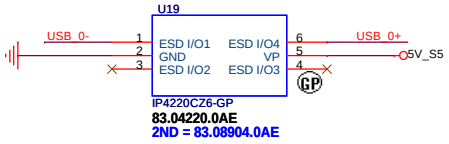
Bluetooth

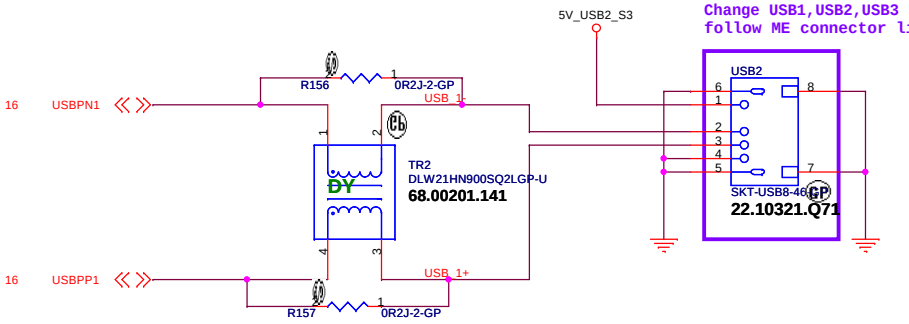


DVT 1ST

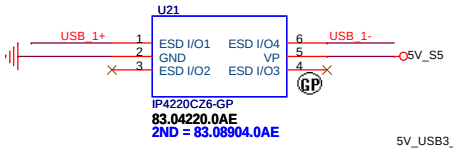
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Bluetooth*		
Size	Document Number: TUCANA	Rev: SB
Date: Wednesday, July 07, 2010	Sheet 27 of 56	

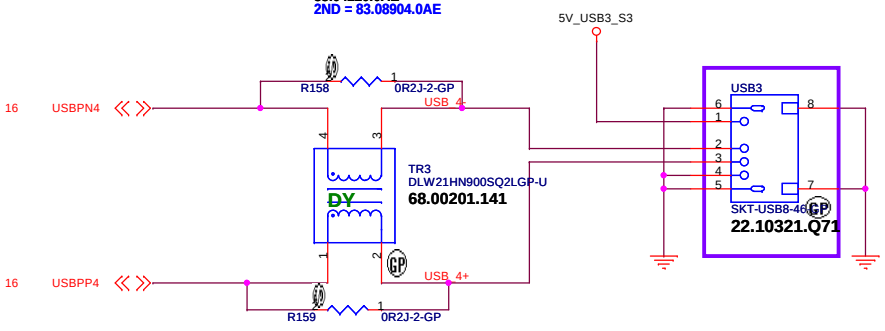


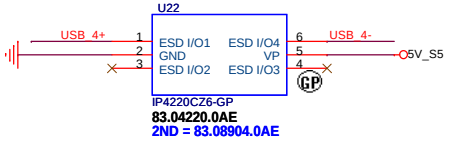


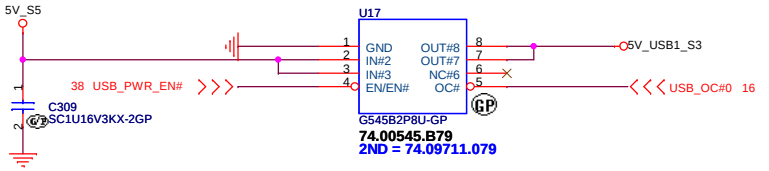


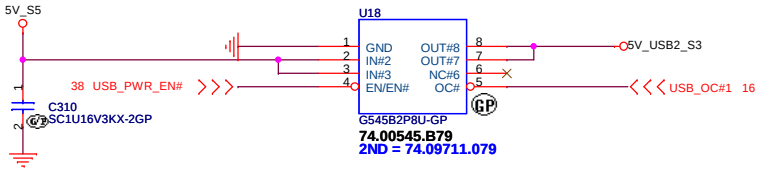
DVT 20100604
Change USB1,USB2,USB3 to 22.10321.Q71
follow ME connector list.

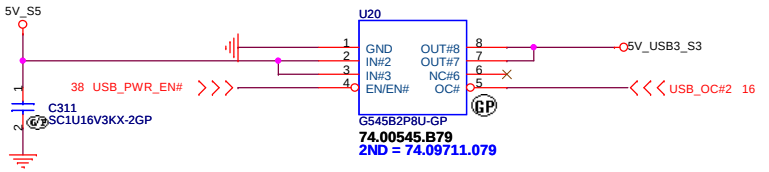




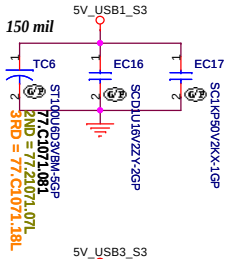


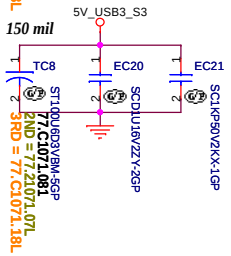


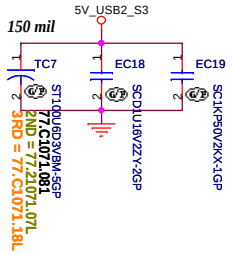




U17,U18,U20 Current Limit 1.5A

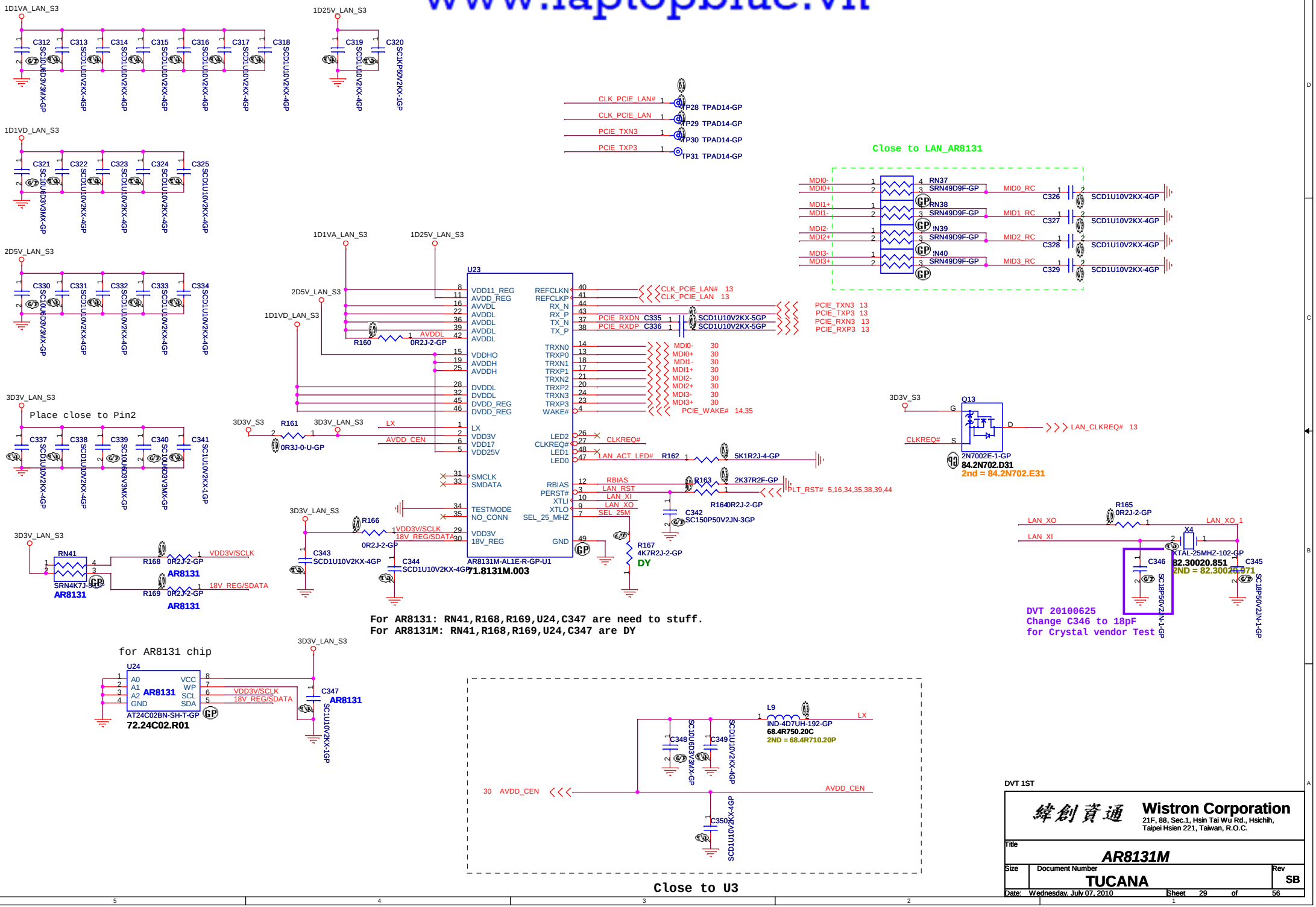






DVT 1ST

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: USB CONN		
Size	Document Number: TUCANA	Rev: SB
Date: Wednesday, July 07, 2010	Sheet 28 of 56	



For AR8131: RN41,R168,R169,U24,C347 are need to stuff.
For AR8131M: RN41,R168,R169,U24,C347 are DY

DVT 1ST

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: AR8131M

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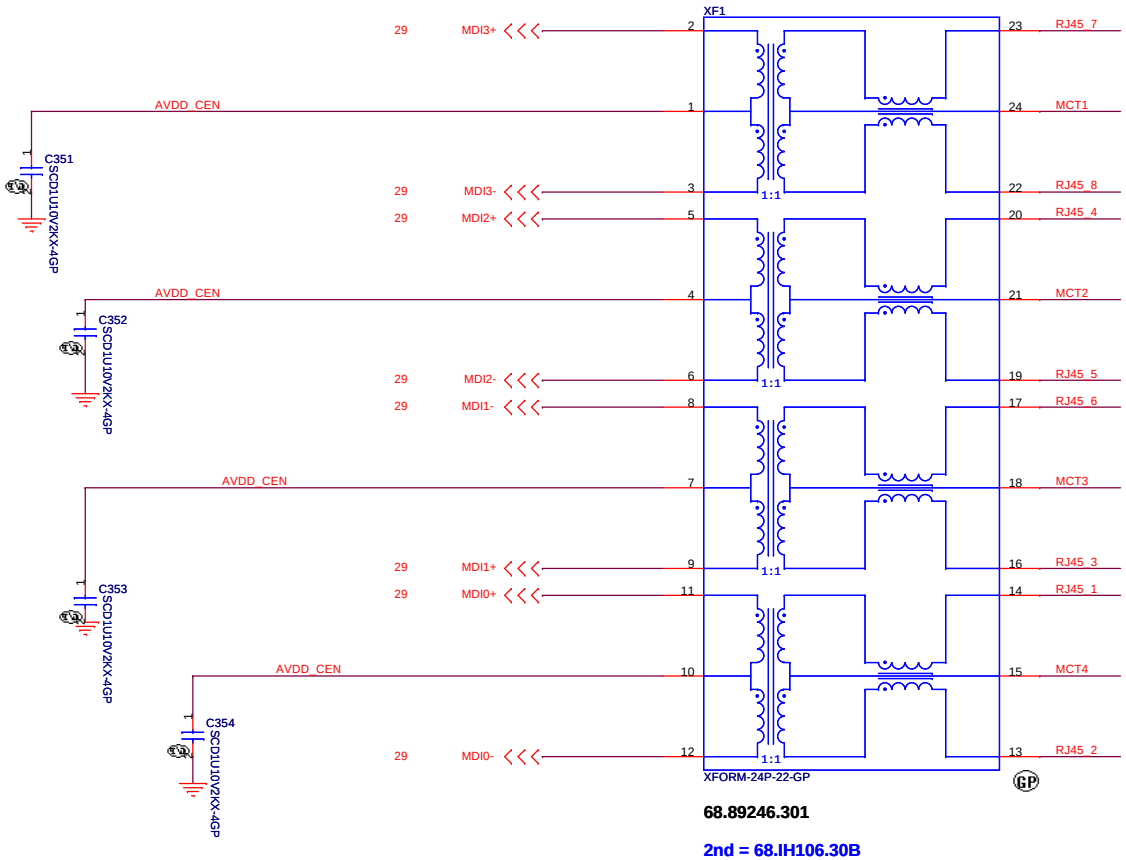
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

LAN Transformer

AVDD_CEN 29

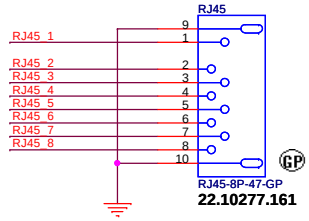
GIGA Lan Transformer



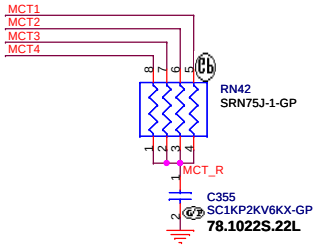
68.89246.301

2nd = 68.IH106.30B

LAN Connector



22.10277.161



78.1022S.22L

DVT 1ST

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
LAN CONN		
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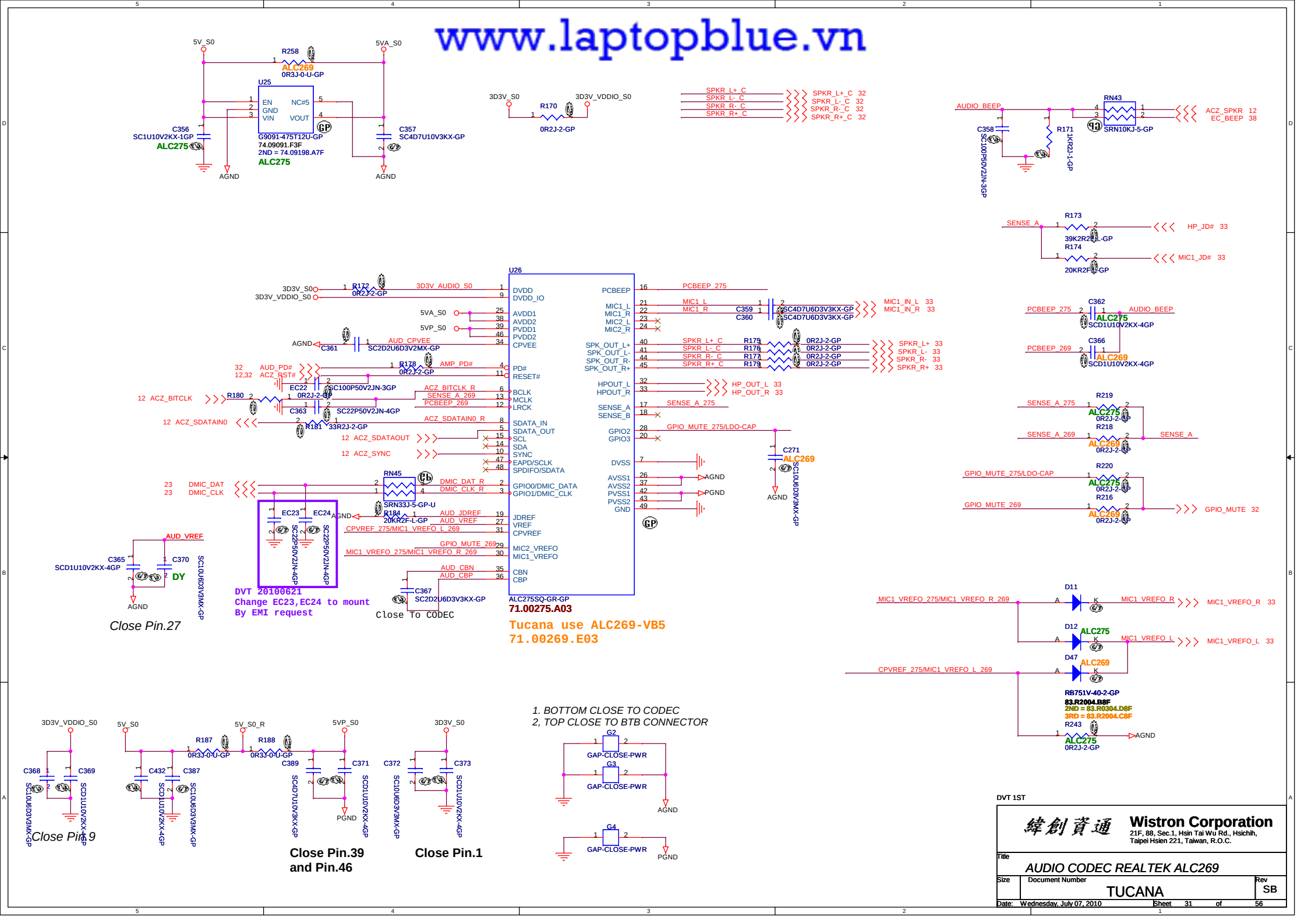

DVT 1ST

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *AUDIO CODEC REALTEK ALC269*

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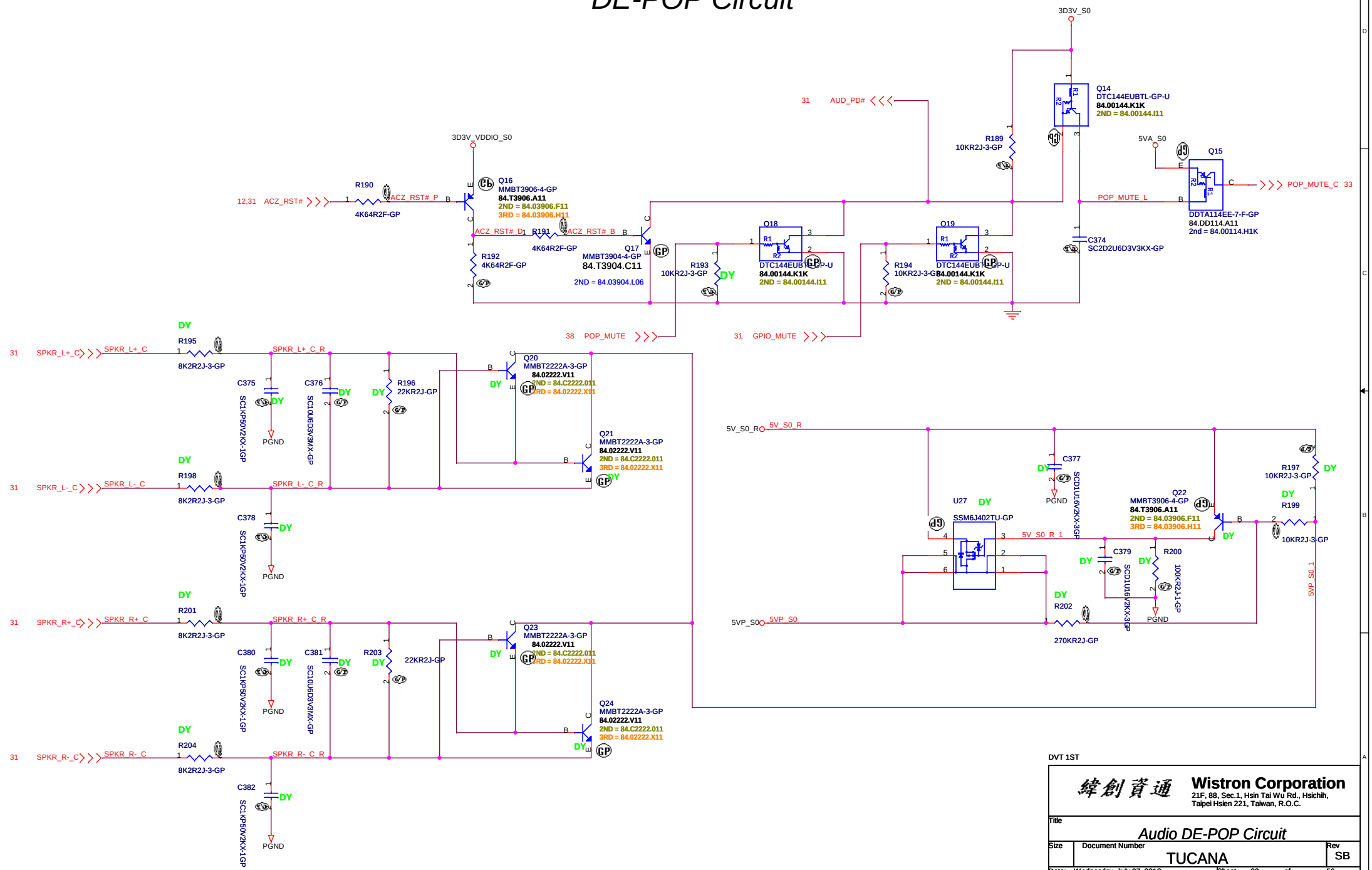
DE-POP Circuit



DVT 1ST

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Audio DE-POP Circuit		
Size	Document Number: TUCANA	Rev: SB
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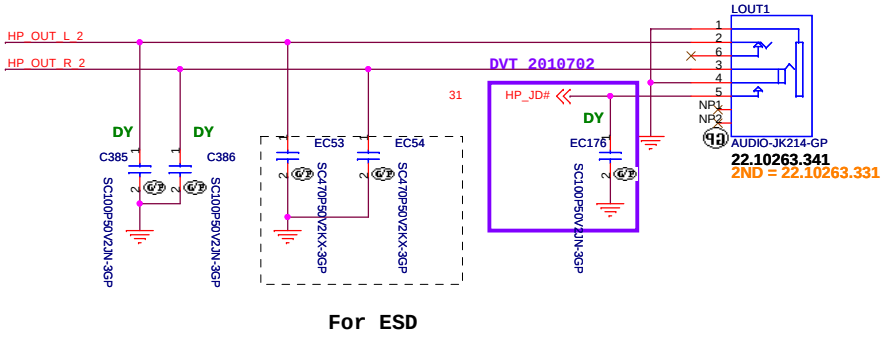
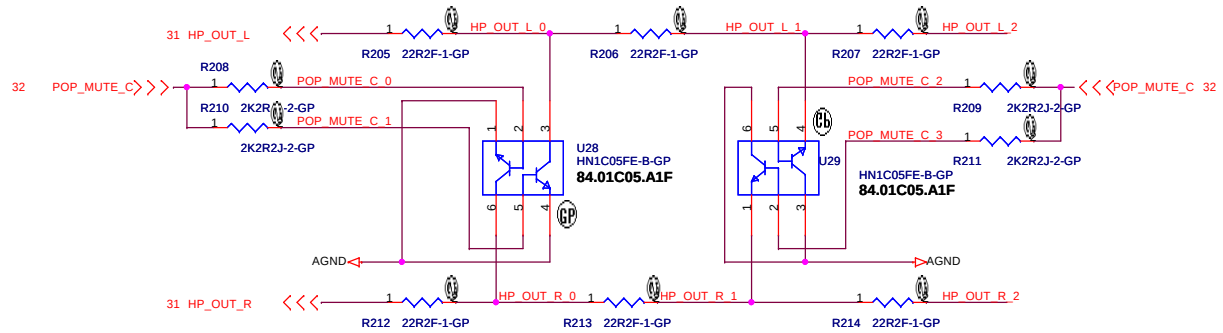
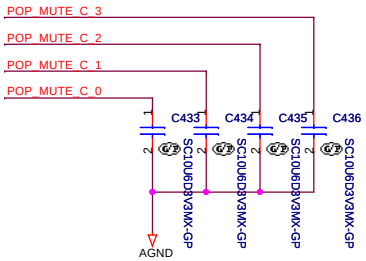
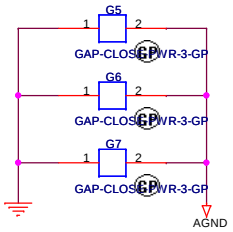
LINE OUT



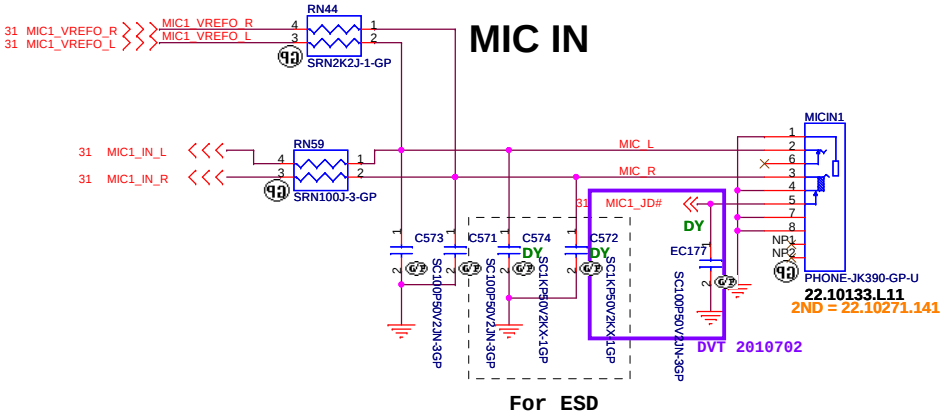
For ESD





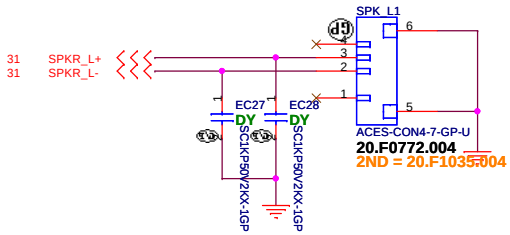


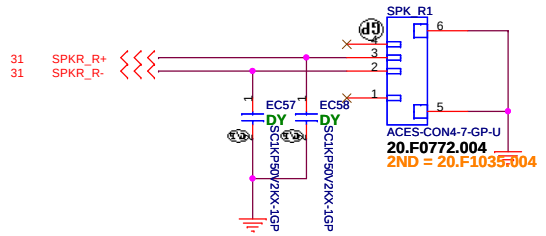
MIC IN



For ESD

Internal Speaker CONN





DVT 1ST

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Jack & Speaker

Size	Document Number	Rev
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DVT 20100625
Change C384,C388 to 15P
for Crystal vendor Test

DVT 20100621
Add 0.1uF between MS_INS# and GND
for CardReader VEVS Test

DVT 20100621
Change C576~C580, C589 to 5pF
for CardReader VEVS Test

For EMI

For EMI

Low Active

SD/MS LED
Orange
~20mA

U75
RTS5186-GR-GP
71.05186.00G

SD1
SKT-SDCARD-24-GP-U1
62.10051.891

MS1
MSCARD-14P-GP-U
62.10051.951

U76
AT93C46DN-SH-B-GP
72.93C46.T01
Serial EEPROM

Q25
NDS0610-NL-GP
2ND = 84.00610.E31
84.S0610.B31

CRLED1
LED-Y-98-GP
83.00191.H70
2ND = 83.19217.E70

DVT 1ST

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CardReader RTS5138
Size: TUCANA
Document Number
Rev: SB
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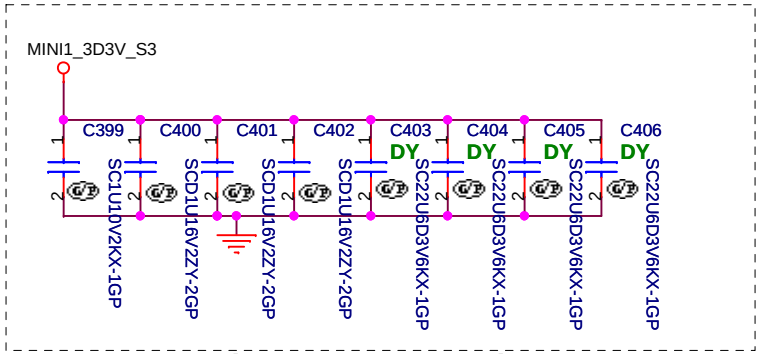
Mini Card Connector(WLAN)

WLAN_EN:
Low: disable the radio
High: enable the radio



C50,C68 bypass MINI1 pin2
C51,C69 bypass MINI1 pin39
C52,C70 bypass MINI1 pin41
C53,C71 bypass MINI1 pin52
Place near MINI1

MINI1
PTWO-CONN52A-8-GP
20.F1518.052
2ND = 62.10043.981

3D3V_S3
L62
0R3J-0-U-GP
MINI1_3D3V_S3

WAKE#
27 WLAN_BT_DATA
27 WLAN_BT_CHCLK
13 WLAN_CLKREQ#
13 CLK_PCIE_MINI1#
13 CLK_PCIE_MINI1
38 E51_RxD
38 E51_TxD
R611 0R2J-2-GP
R612 0R2J-2-GP
E51_RxD_1
E51_TxD_1
13 PCIE_RXN1
13 PCIE_RXP1
13 PCIE_TXN1
13 PCIE_TXP1
MINI1_3D3V_S3
5V_S5
R289 0R2J-2-GP
MINI_5V_S5

C569 SC100P50V2JN-3GP DY
PLT_RST1#_MINI1
R489 0R2J-2-GP
WLAN_EN 38
PLT_RST# 5,16,29,34,38,39,44

USBPN8_MINI
R491 0R2J-2-GP
USBPN8 16
USBPP8_MINI
R492 0R2J-2-GP
USBPP8 16

WLAN_LED# 1
WLAN_LED# 43
Q27
2N7002EW-1-GP
84.2N702.C3K
2ND = 84.2N702.B3K

3D3V_S3
R221 10KR2J-3-GP
Q26
WAKE#
PCIE_WAKE# 14,29
2N7002EW-1-GP
84.2N702.C3K
2ND = 84.2N702.B3K

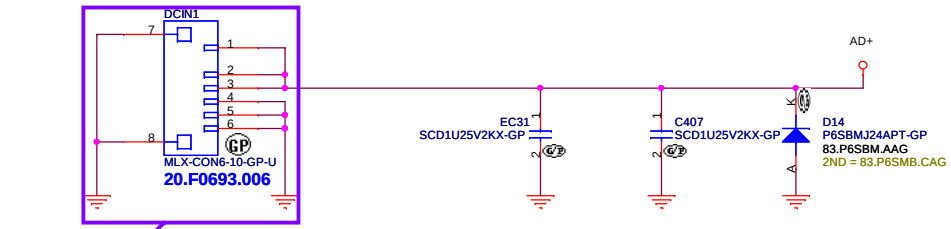
DVT 1ST

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINI CARD CONN
Size: Document Number: TUCANA
Rev: SB
Date: Wednesday, July 07, 2010
Sheet 35 of 56

DC IN Connector

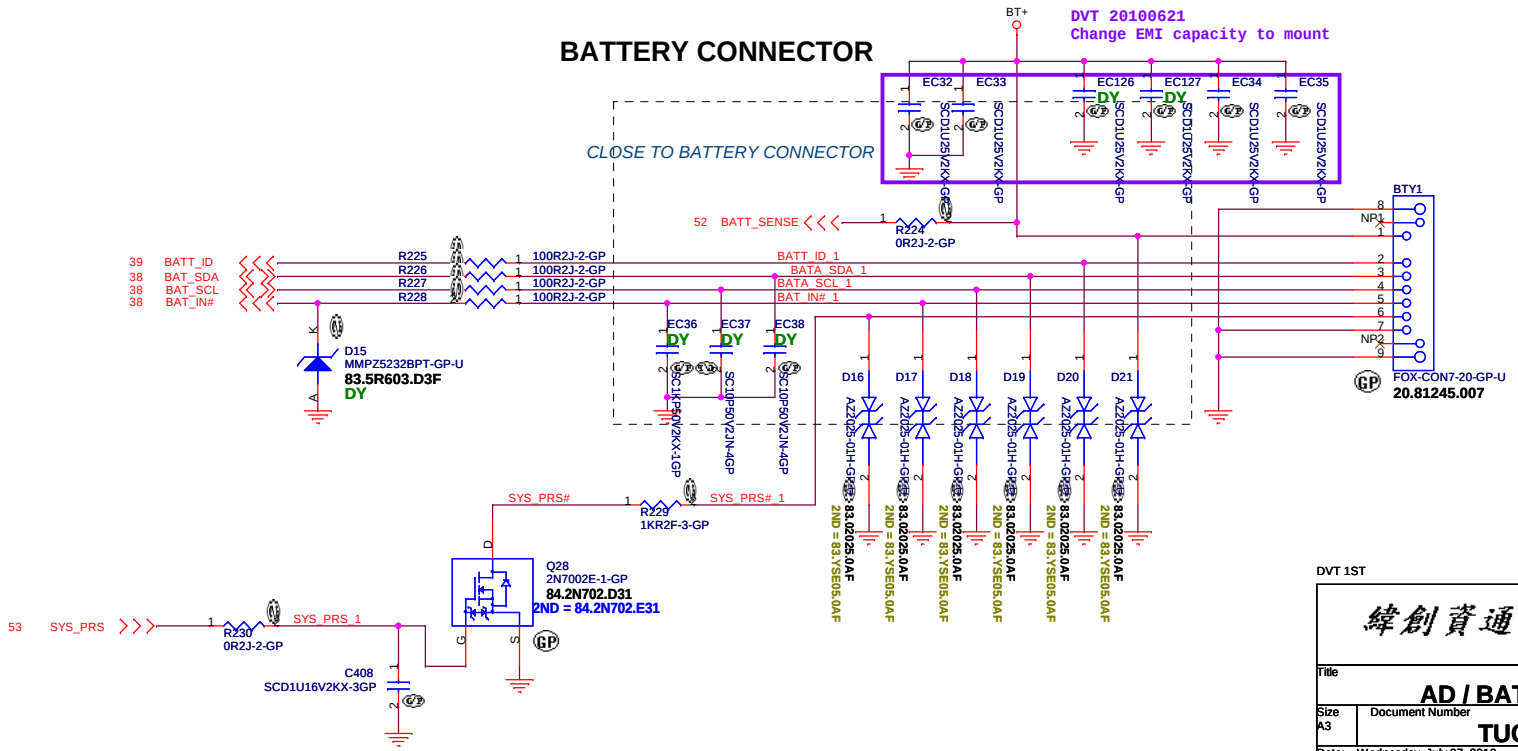
1 pin 1A



DVT 20100610
Change DCIN1 to 20.F0693.006
(follow connector list)

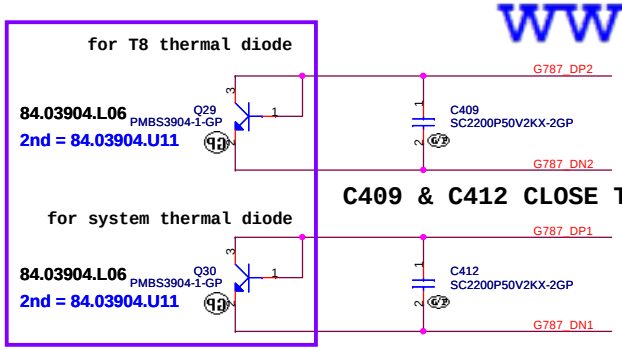
Adaptor in to generate DCBATOUT

BATTERY CONNECTOR



DVT 1ST

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**AD / BATT CONN**
Size A3	Document Number **TUCANA** Rev SB
Date: Wednesday, July 07, 2010	Sheet 36 of 56

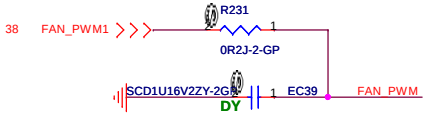


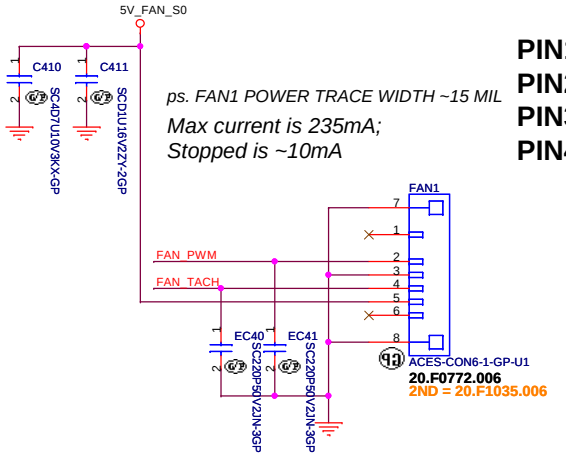
C409 & C412 CLOSE TO G787

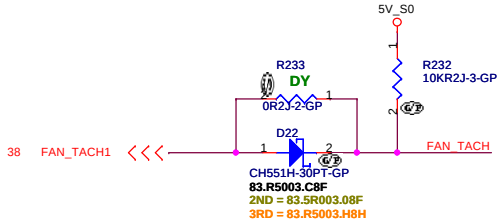
DVT 20100705
Delelte Q29,Q30 main source 84.T3904.C11, follow CARAVEL-CP design

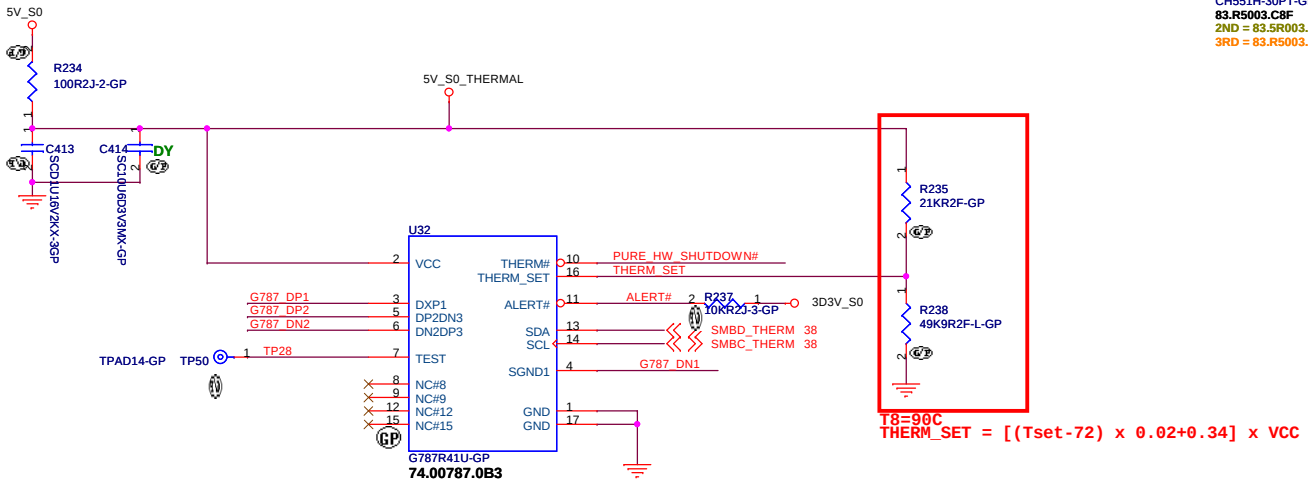
PWM FAN

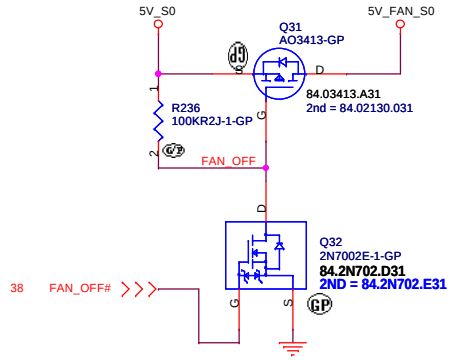
PIN1	PWM
PIN2	GND
PIN3	FG
PIN4	VCC

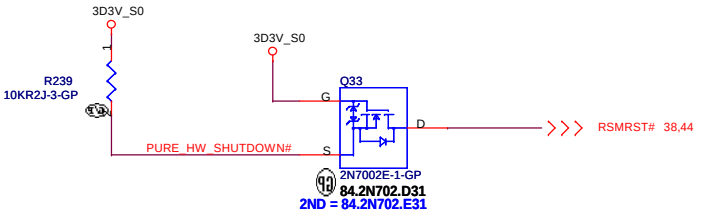












DVT 1ST

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Thermal/Fan Controllor*

Size	Document Number	Rev
	TUCANA	SB

Date: Wednesday, July 07, 2010 Sheet 37 of 56

PCB Version A/D (Pin 98)	Pull-Low Resistor	Pull-High Resistor (3D3V_S5)	Voltage
SA	100.0K	10.0 K	3.0 V
SB	100.0K	20.0 K	2.75V
SC	100.0K	33.0 K	2.54V
-1	100.0K	47.0 K	2.24V
-2	100.0K	64.9 K	1.94V
-3	100.0K	76.8 K	1.81V
-4	100.0K	100.0K	1.65V

DVT 20100611
Change R240 to 20K ohm
SB version.

These two caps close to Pin VDD

THERMAL ----->
BATTERY ----->

DVT 20100527
Add LCD_DETECT pull-high to 3D3V_S5

For BIOS data lose

Internal KeyBoard Connector

FOR KBC DEBUG

DVT 1ST

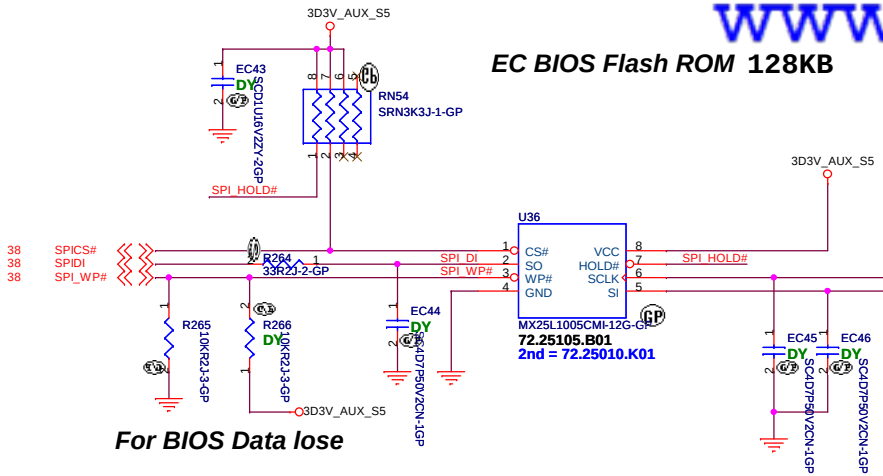
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC WPC775L

Size: A2 | Document Number: TUCANA | Rev: SB

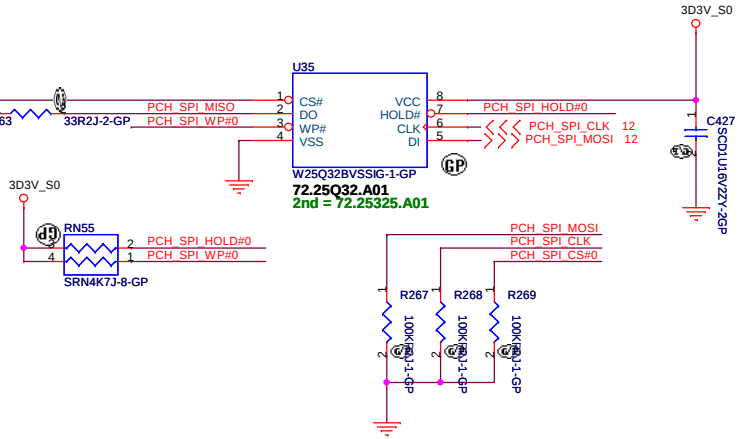
Date: Thursday, July 08, 2010 | Sheet 38 of 56

EC BIOS Flash ROM 128KB

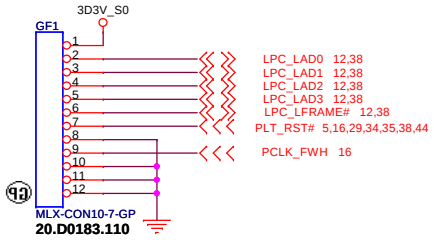


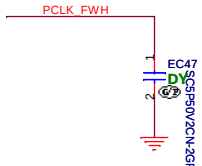
For BIOS Data lose

System BIOS Flash ROM (4MB)

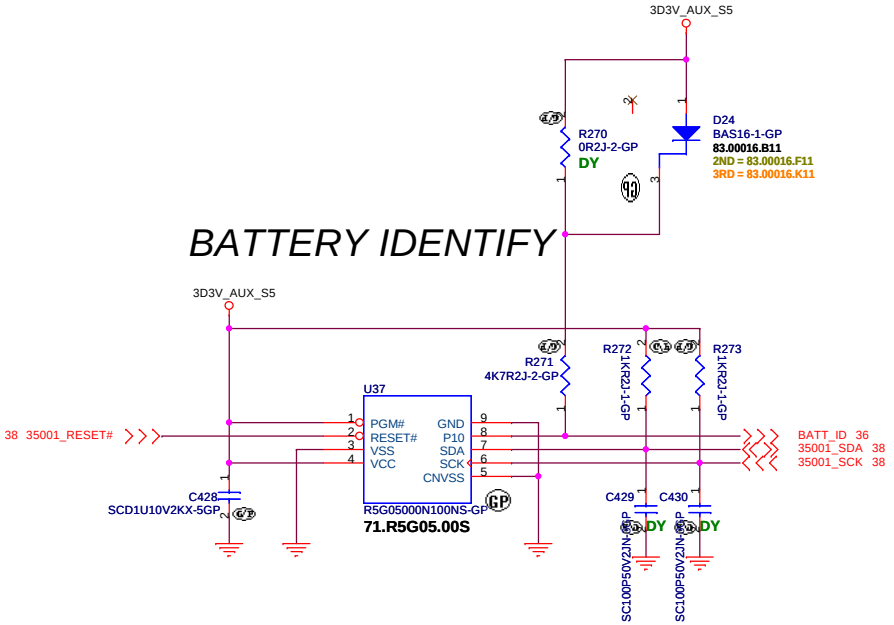


GOLDEN FINGER FOR DEBUG BOARD CONNECTOR (only install it on EVT)



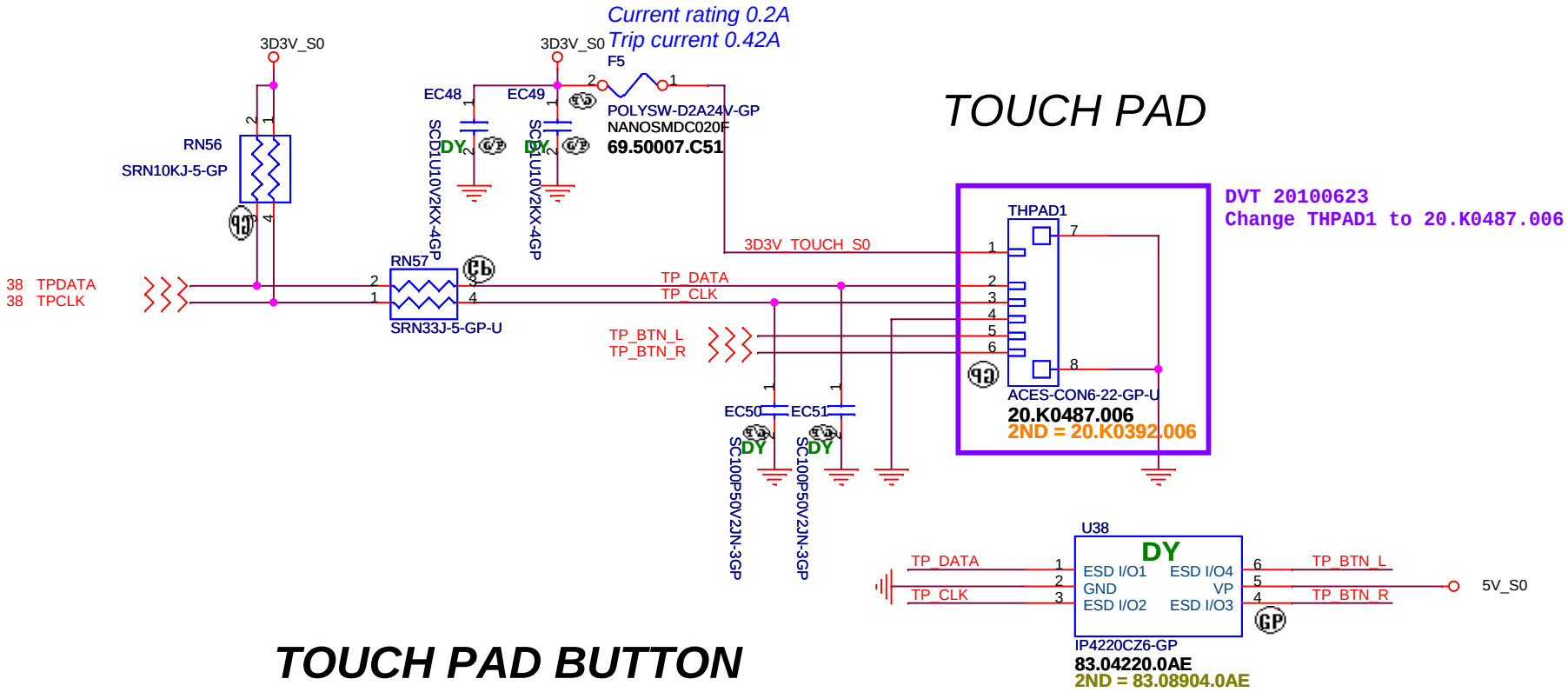


BATTERY IDENTIFY



DVT 1ST

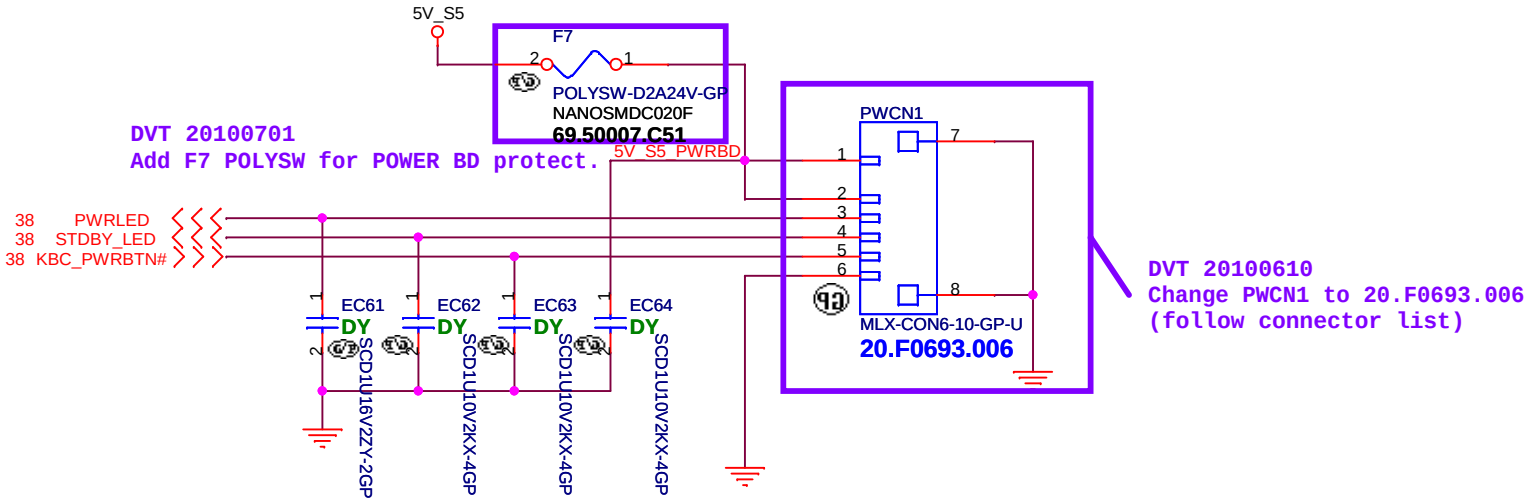
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***BIOS & SW/C & BAT ID***
Size	Document Number: **TUCANA** — Rev: SB
Date: Wednesday, July 07, 2010	Sheet 39 of 56



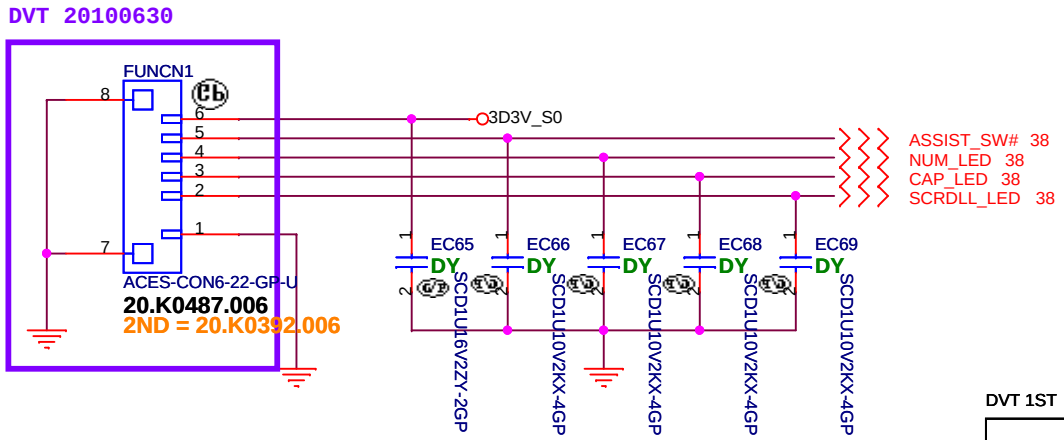
DVT 1ST

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: TouchPad		
Size: A4	Document Number: TUCANA	Rev: SB
Date: Wednesday, July 07, 2010	Sheet 40 of 56	

POWER BUTTON BD CONN



FUNCTION BD CONN

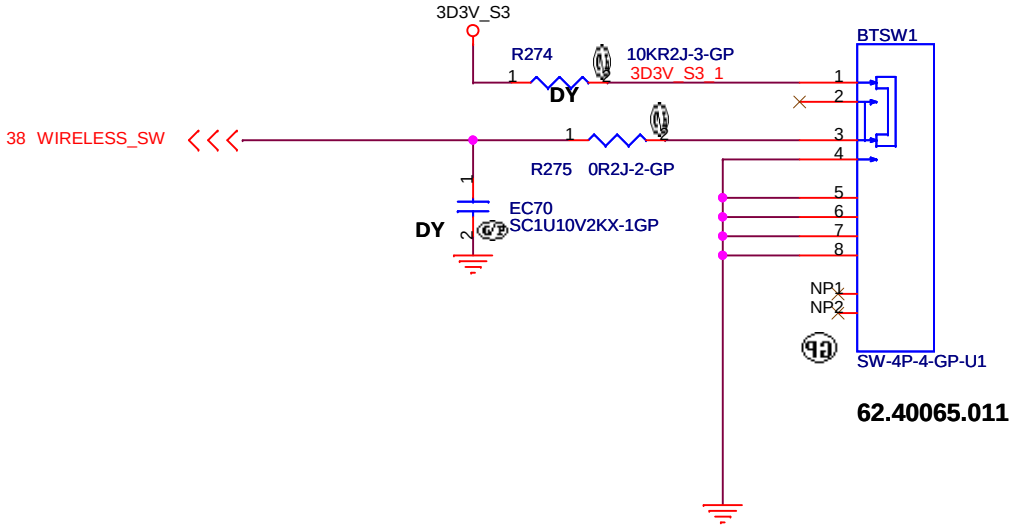


DVT 1ST

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	FUNCTION BD & POWER BD	
Size	Document Number: TUCANA	Rev: SB
Date: Wednesday, July 07, 2010	Sheet 41 of 56	

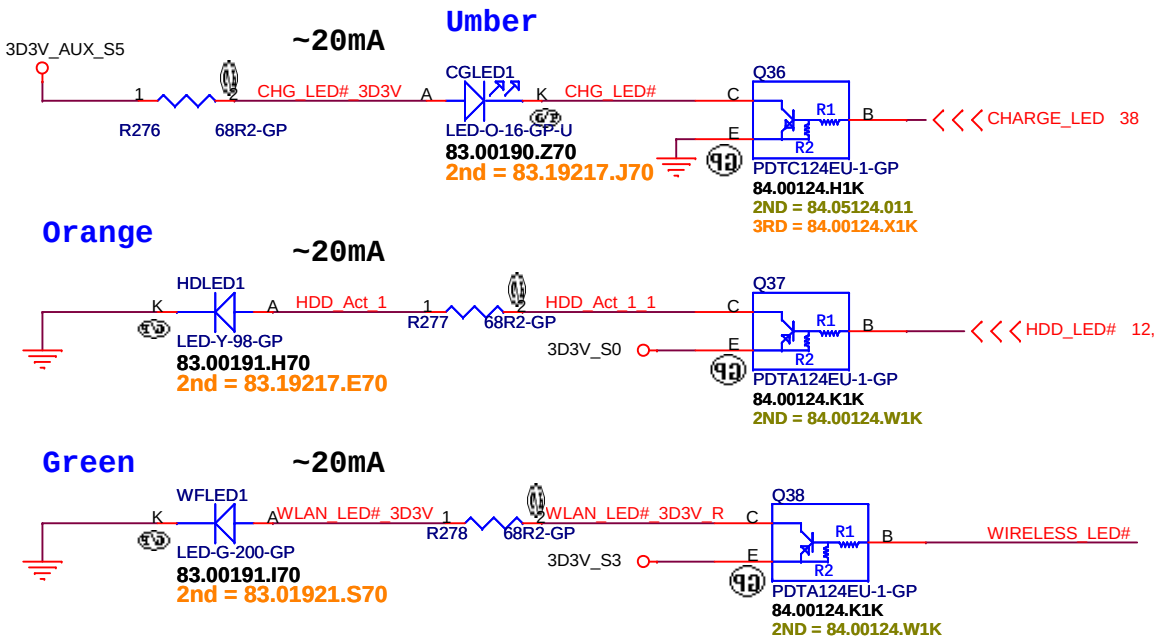
WLAN SWITCH



DVT 1ST

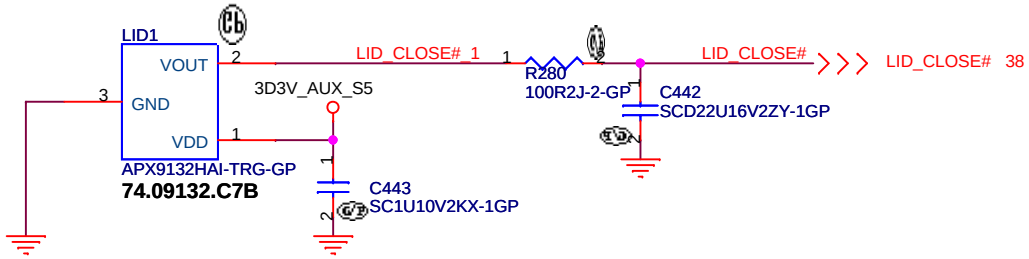
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Switch*		
Size	Document Number: TUCANA	Rev: SB
Date: Wednesday, July 07, 2010	Sheet 42 of 56	

LED



active	High	Low
WWAN(W_DISABLE#)	ON	OFF
WLAN(WLAN_LED#)	OFF	ON
Bluetooth(BT_LED)	ON	OFF

Cover Up Switch



Common wireless SW(mechanical)	ON							
WLAN SW(software)	ON	OFF	ON	OFF	ON	OFF	ON	OFF
WWAN SW(software)	ON	ON	OFF	OFF	ON	ON	OFF	OFF
Bluetooth SW(software)	ON	ON	ON	ON	OFF	OFF	OFF	OFF
LED	TURN ON							OFF

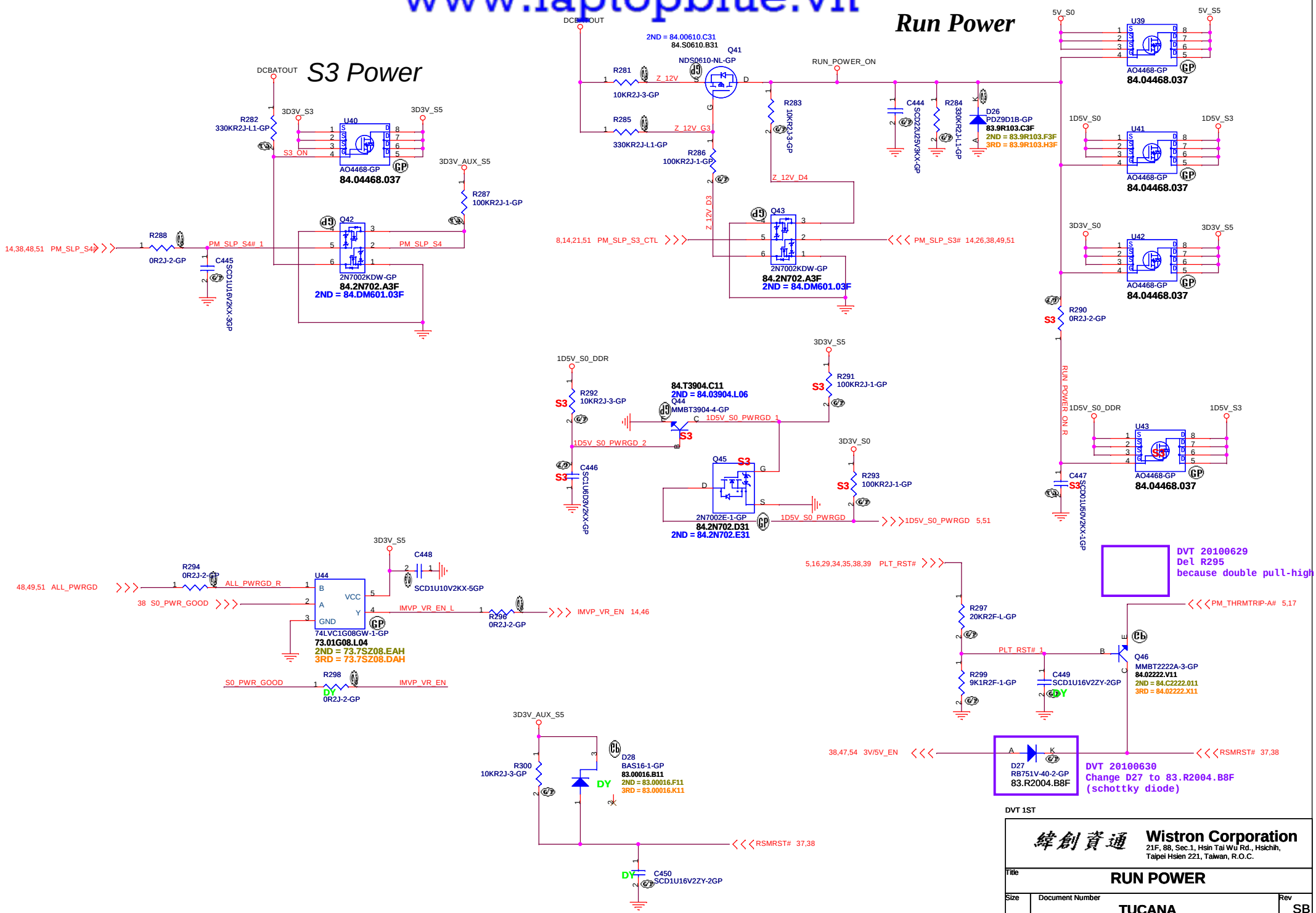
DVT 1ST

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

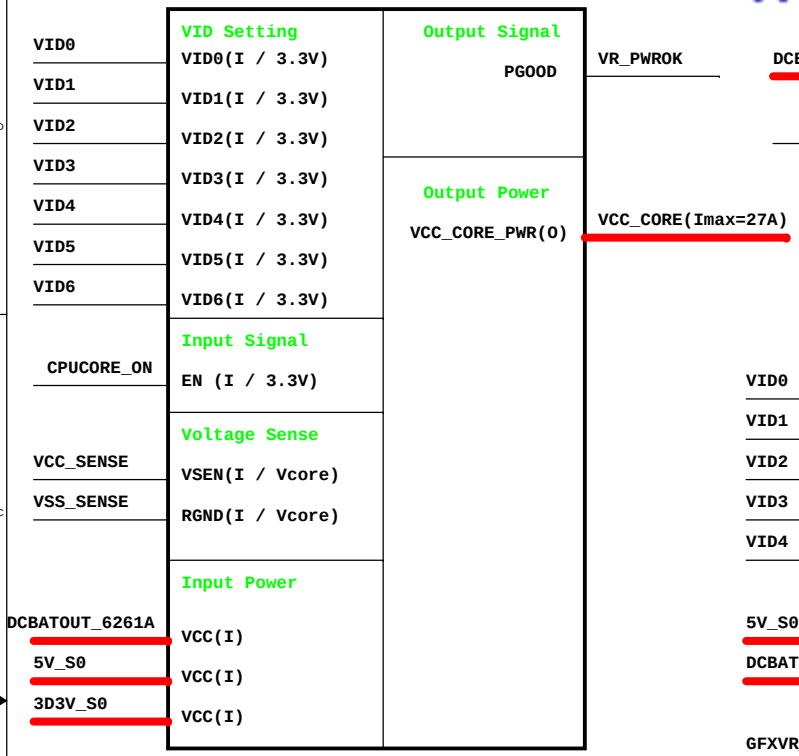
Title: ***Lid Switch & LED***

Size	Document Number	Rev
	TUCANA	SB

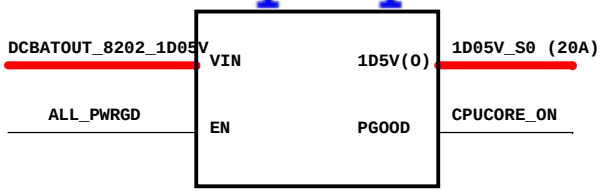
Date: Wednesday, July 07, 2010 Sheet 43 of 56



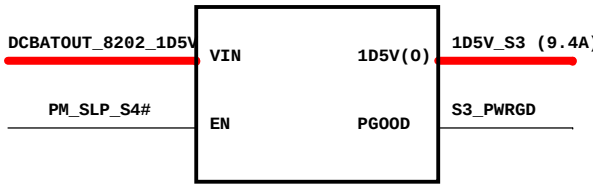
CPU_CORE
ADP3211



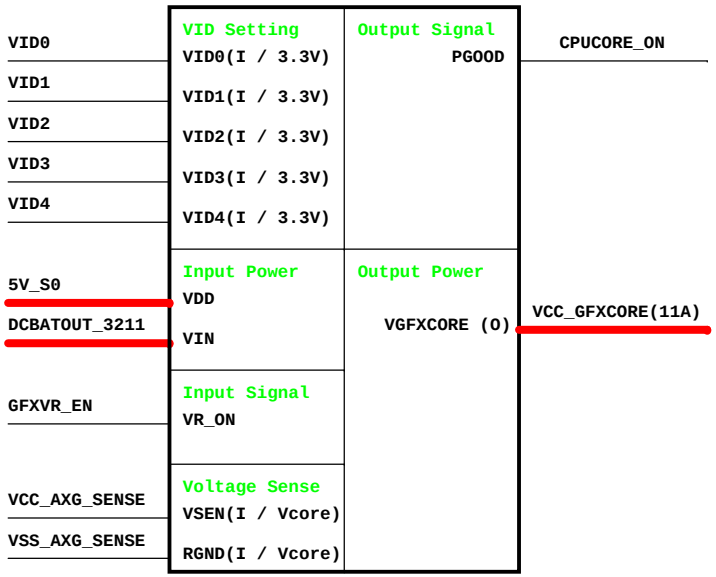
RT8209 1D05V_S0



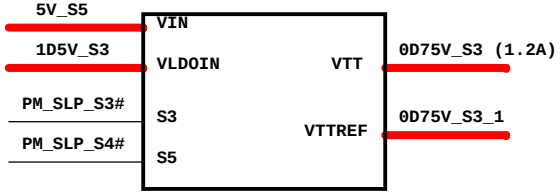
RT8209 1D5V_S3



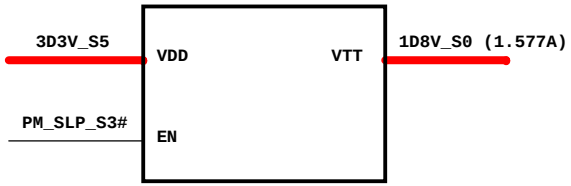
GFX_CORE/ VGA_CORE
ADP3211



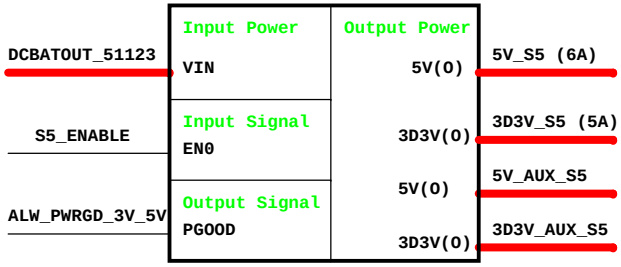
RT9026 0D75V_S0



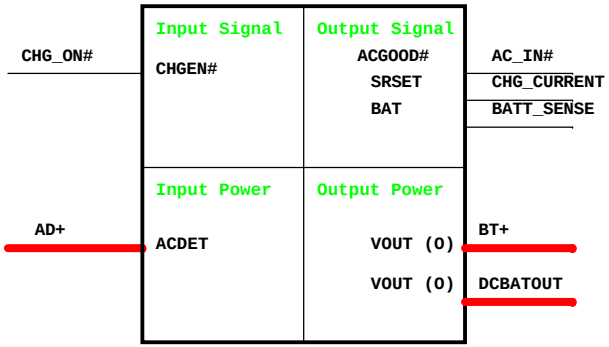
RT8015 1D8V_S0



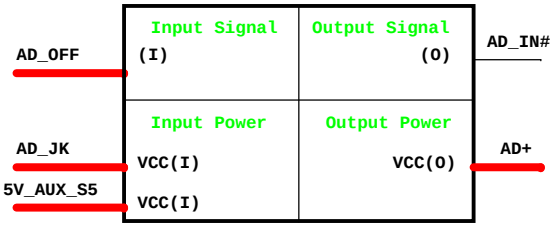
5V/3D3V
RT8223



Charger BQ24751



Adapter



DVT 1ST

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Sequence Logic**

Size	Document Number	Rev
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DVT 20100701
Change OPEN-GAP to CLOSE-GAP

DVT 20100623

DVT 20100623

DVT 20100623

Id=24A
Qg=11nC
Rdson=9.6~13.4mohm

Id=50A
Qg=46nC
Rdson=2.3~3.6mohm

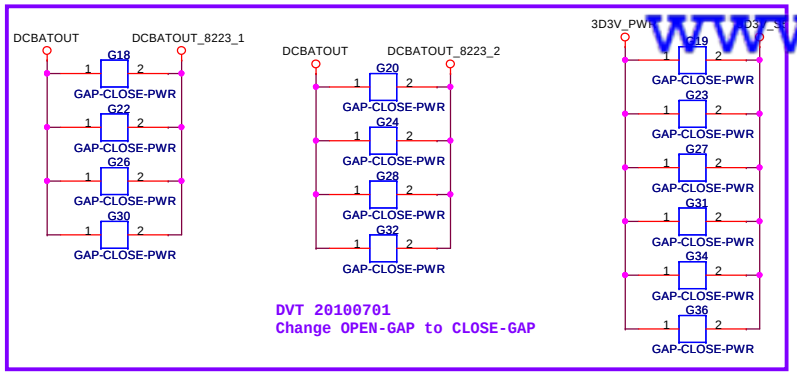
Iomax=27A
OCP>40.5A

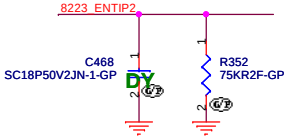
Mag. 0.36uH
DCR=1.05~1.2mohm
Idc=30A, Isat=60A

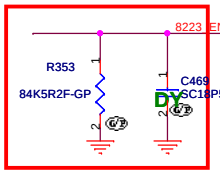
Panasonic 330uF
2V, ESR=9mohm

Intel support POC (power on current).

DVT 1ST			
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: ADP3211 CPU CORE			
Size	Document Number: TUCANA		Rev: SB
Date: Wednesday, July 07, 2010	Sheet 46 of 56		

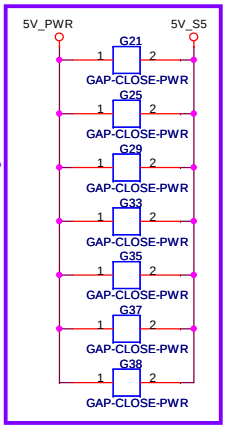


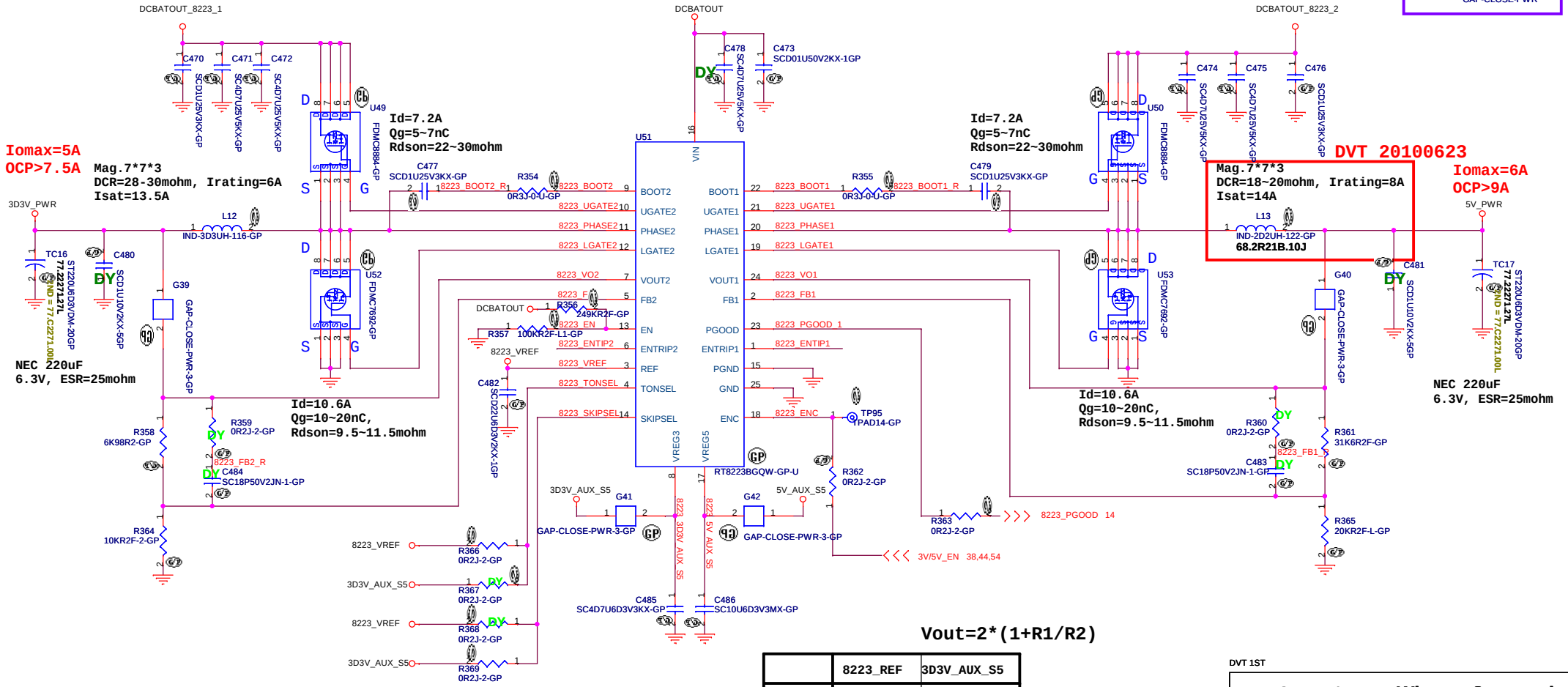




DVT 20100623

DVT 20100701
Change OPEN-GAP
to CLOSE-GAP





Vout=2*(1+R1/R2)

	8223_REF	3D3V_AUX_S5
SKIPSEL	PWM	00A AUTOSKIP
TONSEL	245k/CH1 305k/CH2	300k/CH1 375k/CH2

DVT 1ST

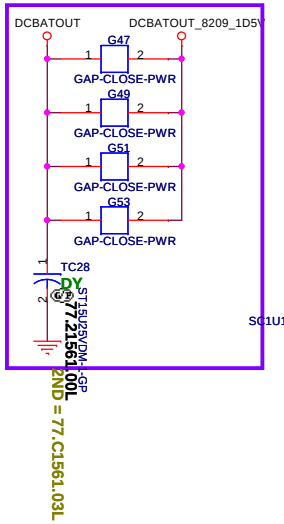
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8223_5V/3D3V

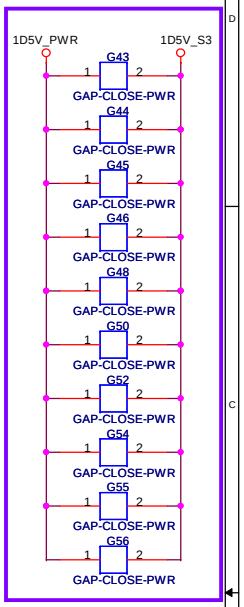
Size | Document Number: TUCANA | Rev: SA

Date: Wednesday, July 07, 2010 | Sheet 47 of 56

DVT 20100701
Change OPEN-GAP to
CLOSE-GAP



DVT 20100701
Change OPEN-GAP to
CLOSE-GAP



RT8209 for 1D5V

DVT 1ST

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: RT8209_1D5V		
Size	Document Number: TUCANA	Rev: SB
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RT8209 1D05V

DCBATOUT
DCBATOUT_RT8209_1D05V
G57 GAP-CLOSE-PWR
G58 GAP-CLOSE-PWR
G60 GAP-CLOSE-PWR
G62 GAP-CLOSE-PWR
TC19 ST15U25VDM-1-GP
DY
77.21561.00L
2ND = 77.C1561.03L

DVT 20100701
Change OPEN-GAP to
CLOSE-GAP

5V_S5
C500 SC1U10V2KX-1GP
C503 SC1U10V2KX-1GP
R382 2D2R3-1-U-GP
8209_1D05_V5FILT
R383 0R3J-0-U-GP
8209_1D05_BOOT
8209_1D05_BOOT_1
C501 SCD1U25V3KX-GP
U59
VDD
VDDP
FB
BOOT
EN/DEM
TON
CS
UGATE
LGATE
PHASE
VOUT
PGOOD
GND
PGND
NC#15
RT8209EGQW-GP
74.08209.B73
8209_1D05_UGATE
8209_1D05_LGATE
8209_1D05_PHASE
1D05V_PWR
VTT_PWRGD 14,38
8209_1D05_FB
8209_1D05_EN
8209_1D05_TON
8209_1D05_CS
44,48,51 ALL_PWRGD
R386 0R2J-2-GP
R387 200KR2F-L-GP
R388 100KR2F-L1-GP
R389 14K3R2F-GP
DVT 20100623

DCBATOUT_RT8209_1D05V
U57 SI7686DP-T1-GE3-GP
84.07686.A37
C496 SC4D7U25V5KX-GP
C497 SC4D7U25V5KX-GP
C498 SC4D7U25V5KX-GP
C499 SCD1U25V3KX-GP
Id=24A
Qg=11nC
Rdson=9.4~13.5mohm
DVT 20100622
Mag. 0.56uH
DCR=1.6~1.8mohm
Idc=25A, Isat=40A
Iomax=20A
OCP>30A
R381 0R3J-0-U-GP
8209_1D05_UGATE_R
L15 IND-D56UH-27-GP
68.R5610.10P
20100428
U58 SIR164DP-T1-GE3-GP
84.00164.037
Id=50A
Qg=46nC,
Rdson=2.3~3.6mohm
1D05V_PWR
C502 SC18P50V2JN-1-GP
DY
TC21 ST330U2D5VBM-1-GP
80.337V1.A2L
2ND = 77.23371.31L
TC20 ST330U2D5VBM-1-GP
80.337V1.A2L
2ND = 77.23371.31L
R384 10KR2F-2-GP
8209_1D05_FB
R385 24KR2F-GP
Vout=0.75*(1+R1/R2)
8209_1D05_FB
R390 0R2J-2-GP
VTT_SENSE 7

1D05V_PWR
1D05V_S0
G59 GAP-CLOSE-PWR
G61 GAP-CLOSE-PWR
G63 GAP-CLOSE-PWR
G64 GAP-CLOSE-PWR
G65 GAP-CLOSE-PWR
G66 GAP-CLOSE-PWR
G67 GAP-CLOSE-PWR
G68 GAP-CLOSE-PWR
G69 GAP-CLOSE-PWR
G70 GAP-CLOSE-PWR
G71 GAP-CLOSE-PWR
G72 GAP-CLOSE-PWR
G73 GAP-CLOSE-PWR
G74 GAP-CLOSE-PWR
G75 GAP-CLOSE-PWR
G76 GAP-CLOSE-PWR
G77 GAP-CLOSE-PWR
G78 GAP-CLOSE-PWR
G79 GAP-CLOSE-PWR
G80 GAP-CLOSE-PWR

3D3V_S5
R391 10KR2J-3-GP
Q47 2N7002KDW-GP
84.2N702.A3F
2ND = 84.DM601.03F
VTT_PWRGD
H_VTTPWRGD_R
3D3V_S5
R392 100KR2J-1-GP
1D05V_S0
R394 1KR2J-1-GP
H_VTTPWRGD 5

The processor needs to be warned about the VTT rails shutdown at least 100 ns before the VTT rail falls to -5% of nominal value.

3D3V_S5
R393 100KR2J-1-GP
DY
Q48 2N7002KDW-GP
H_VTTPWRGD
PM_SLP_S3# 14,26,38,44,51
H_VTTPWRGD_1
DY
84.2N702.A3F
2ND = 84.DM601.03F

DVT 1ST

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DVT 20100701
Change OPEN-GAP to
CLOSE-GAP

DCBATOUT
DCBATOUT_3211_GFX
G81 GAP-CLOSE-PWR
G82 GAP-CLOSE-PWR
G83 GAP-CLOSE-PWR
G84 GAP-CLOSE-PWR
G85 GAP-CLOSE-PWR
G86 GAP-CLOSE-PWR
TC22 ST15U25VDM-1-GP
DY
77.21561.00L
2ND = 77.C1561.03L

8 GFX_VID[6..0]
GFX_VID6 R395 0R2J-2-GP GFX_R_VID6
GFX_VID5 R396 0R2J-2-GP GFX_R_VID5
GFX_VID4 R397 0R2J-2-GP GFX_R_VID4
GFX_VID3 R398 0R2J-2-GP GFX_R_VID3
GFX_VID2 R399 0R2J-2-GP GFX_R_VID2
GFX_VID1 R401 0R2J-2-GP GFX_R_VID1
GFX_VID0 R402 0R2J-2-GP GFX_R_VID0
8 GFX_VR_EN R403 0R2J-2-GP GFX_IMVP_VR_EN
R405 470R2F-GP
3D3V_S5 R404 10KR2J-3-GP GFX_PWRGD
8 GFX_IMON R406 0R2J-2-GP
R407 8K66R2D-GP
C509 SCD056U16V2KX-GP
GFX_PWRGD
GFX_FBRTN
GFX_FB
GFX_COMP
GFX_ILIM
5V_S5 R409 6K65R2F-GP
GFX_CSCOMP
C511 SC220P50V2JN-3GP
C512 SC1P5V2JN-3GP
R410 1KR2F-1-GP
C514 SC470P50V2KX-3GP
GFX_COMP_L
R411 20KR2F-1-GP
GFX_AGND
C515 SC1KP50V2KX-1GP
GFX_IREF R412 80K6R2F-GP
GFX_RPM R413 160KR2F-GP
GFX_RT R414 261KR2F-GP
GFX_RAMP
GFX_CSREF
GFX_CSISB
GFX_CSCOMP
DCBATOUT_3211_GFX
GFX_RAMP_1 R415 1KR2F-3-GP
R416 422KR2F-1-GP
C516 SC1KP50V2KX-1GP
GFX_AGND
GFX_FB_1
R421 100R2F-L1-GP-U VCC_GFXCORE
R422 0R2J-2-GP VCC_AXG_SENSE 8
R423 0R2J-2-GP VSS_AXG_SENSE 8
R424 100R2F-L1-GP-U
G89 GAP-CLOSE-PWR-3-GP
GFX_AGND

U61 ADP3211MNR2G-GP
74.03211.033
EN VID0 VID1 VID2 VID3 VID4 VID5 VID6
PWRGD IMON CLKEN# FBRTN FB COMP GPU ILIM
VCC BST DRVH SW PVCC DRVL PGND GND
IREF RPM RT RAMP ILINE CSREF CSISB CSCOMP

5V_S5 R400 10R3F-GP
C507 SC1U10V2KX-1GP
GFX_AGND
R408 1R3J-L1-GP GFX_BST_1
C510 SCD22U16V3KX-2-GP
C513 SC3D3U10V5KX-2GP
O5V_S5
GFX_VCC GFX_BST GFX_DRVH GFX_SW GFX_DRVL

DCBATOUT_3211_GFX
U60 SI7686DP-T1-GE3-GP
C508 SCD47U25V5KX-GP
C504 SCD47U25V5KX-GP
C505 SCD47U25V5KX-GP
C506 SCD10U25V3KX-3GP
Id=14.3A
Qg=9.2~14nC
Rdson=11~14mohm
Iomax=12A
OCP>18A
Mag. 0.56uH
DCR=1.6~1.8mohm
Idc=25A, Isat=40A
L16 IND-D56UH-27-GP
U62 SI7164DP-T1-GE3-GP
Id=26.5A
Qg=40.6~61nC
Rdson=2.6~3.2mohm
G87 GAP-CLOSE-PWR-3-GP
G88 GAP-CLOSE-PWR-3-GP
VCC_GFXCORE
C23 ST330U2D5VBM-1-GP
C24 ST330U2D5VBM-1-GP
C26 ST330U2D5VBM-1-GP
Panasonic 330uF
2V, ESR=9mohm
DVT 20100623

R417 71K5R2F-1-GP GFX_CSCOMP_1
R418 165KR2F-GP
R419 56K2R3F-GP GFX_SW_L
DVT 20100623
R420 NTC-220K-5-GP
C517 SC82P50V2KX-1GP
C518 SC1KP50V2KX-1GP
C519 SC1KP50V2KX-1GP

DVT 1ST

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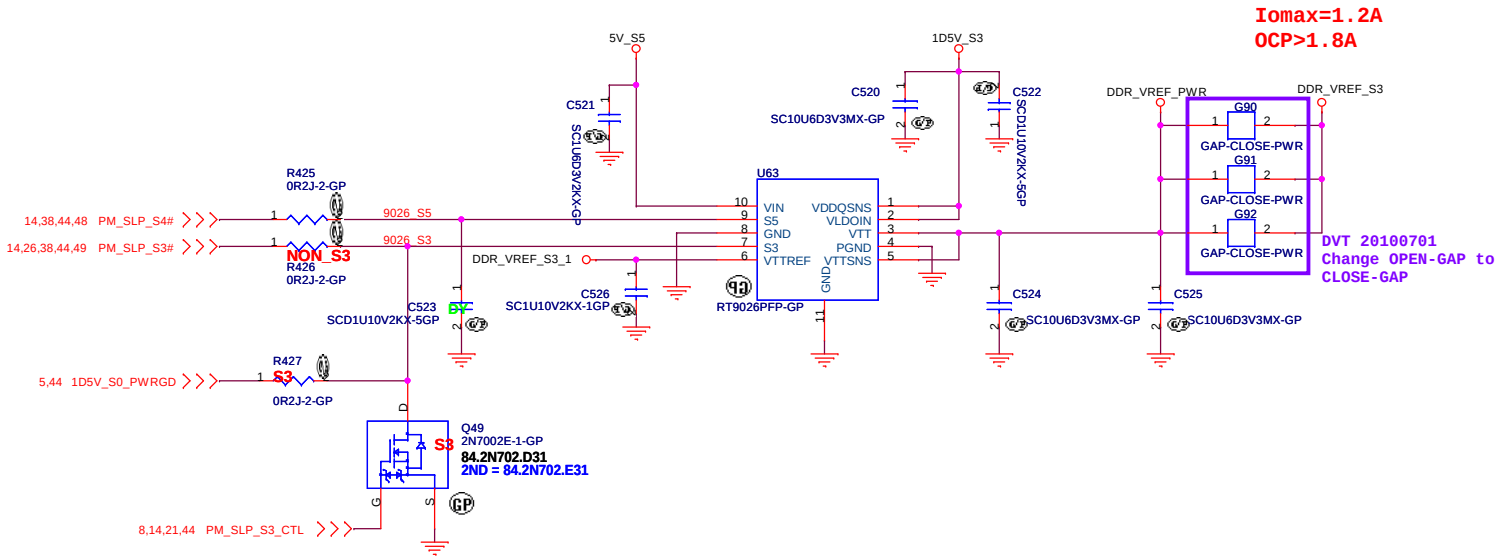
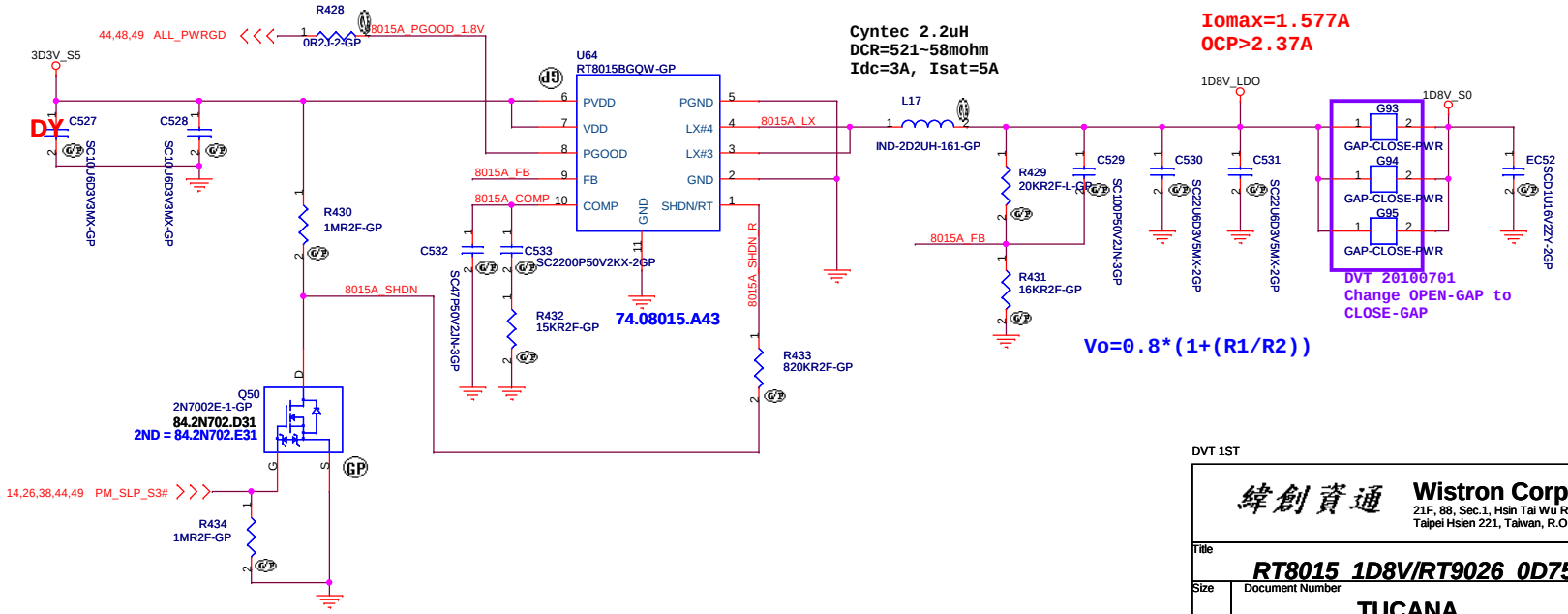
RT9026 for 0D75V_S3



RT8015 for 1D8V_S0



DVT 1ST

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Title: RT8015_1D8V/RT9026_0D75

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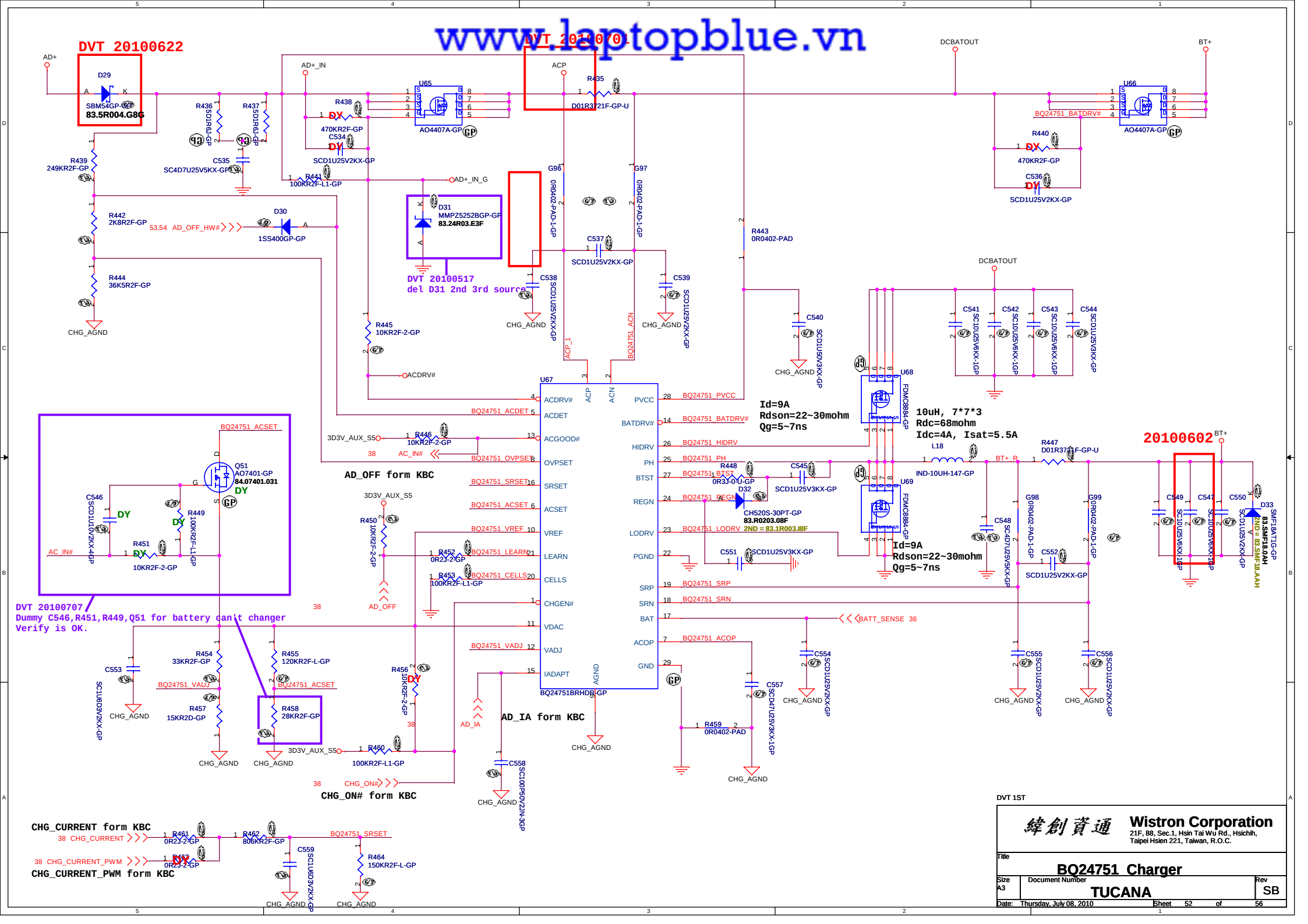

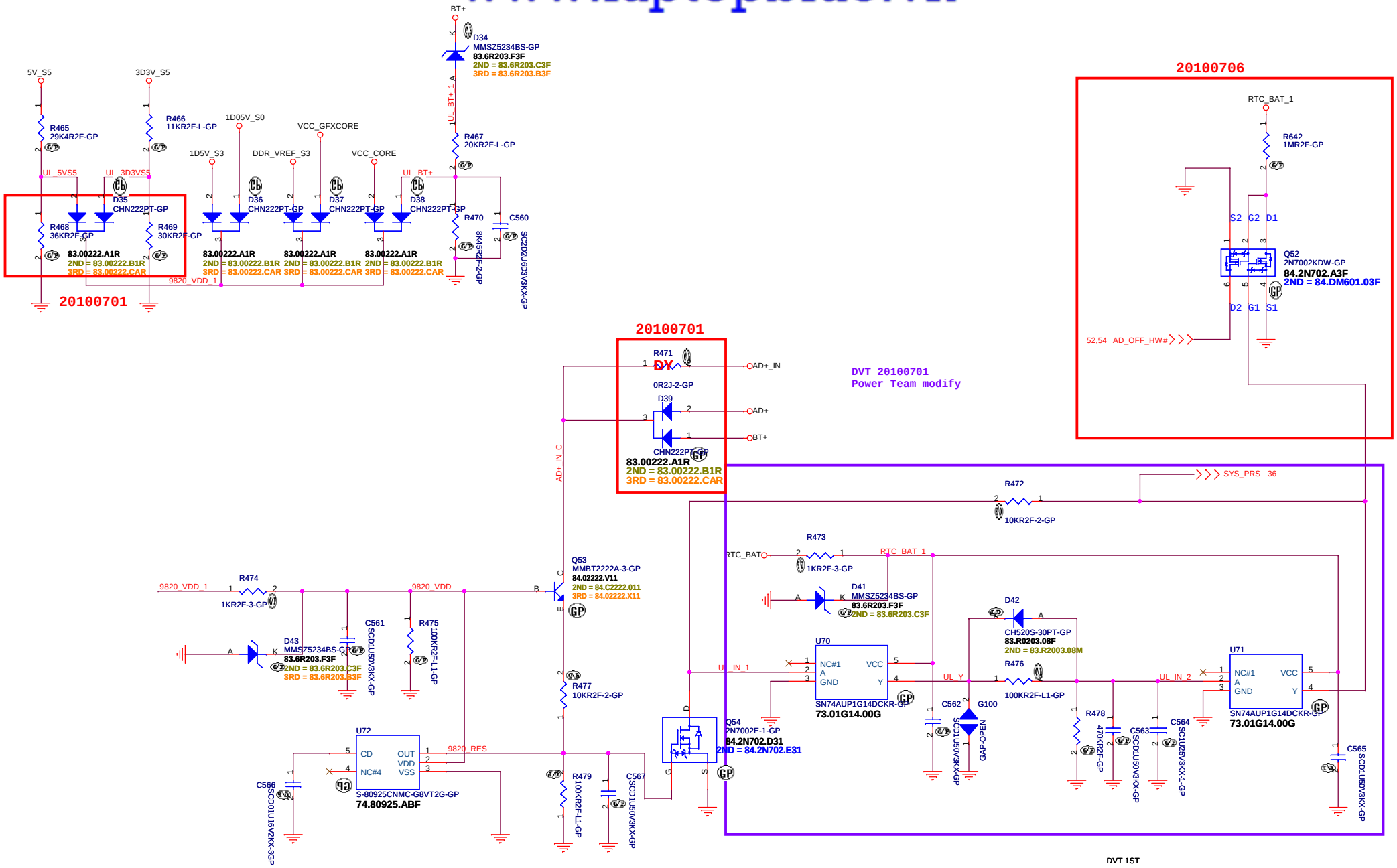

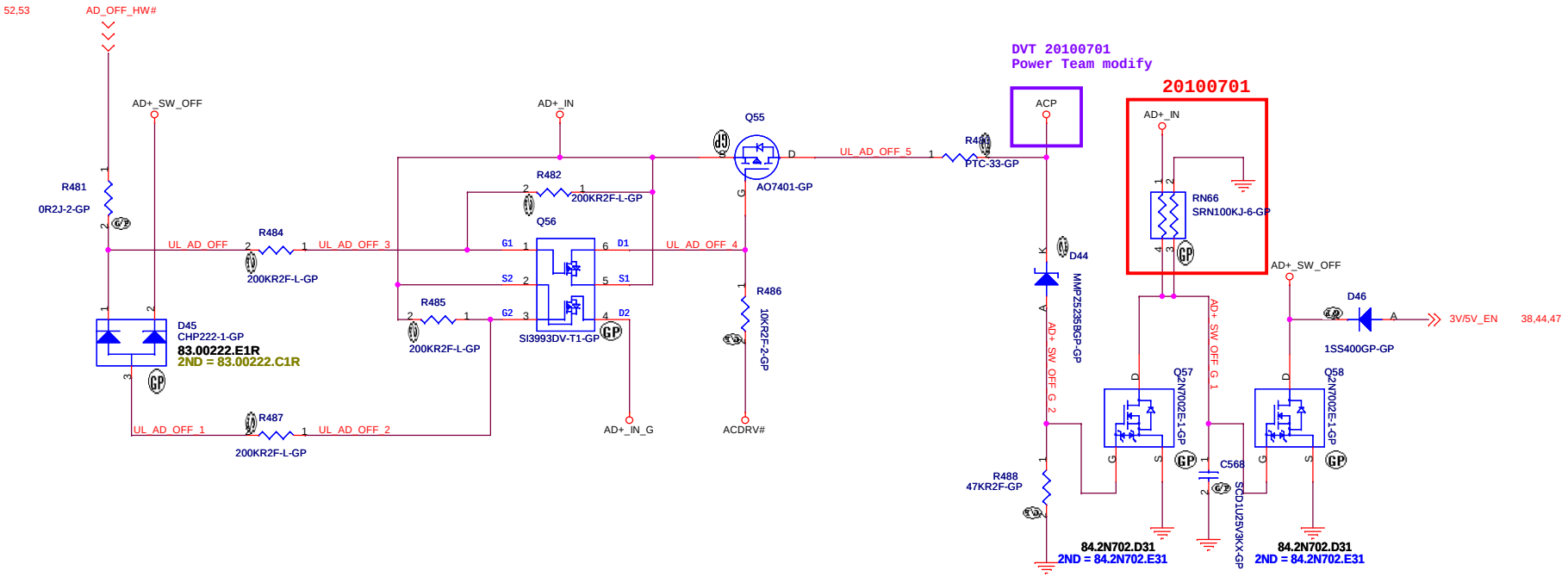

DVT 1ST

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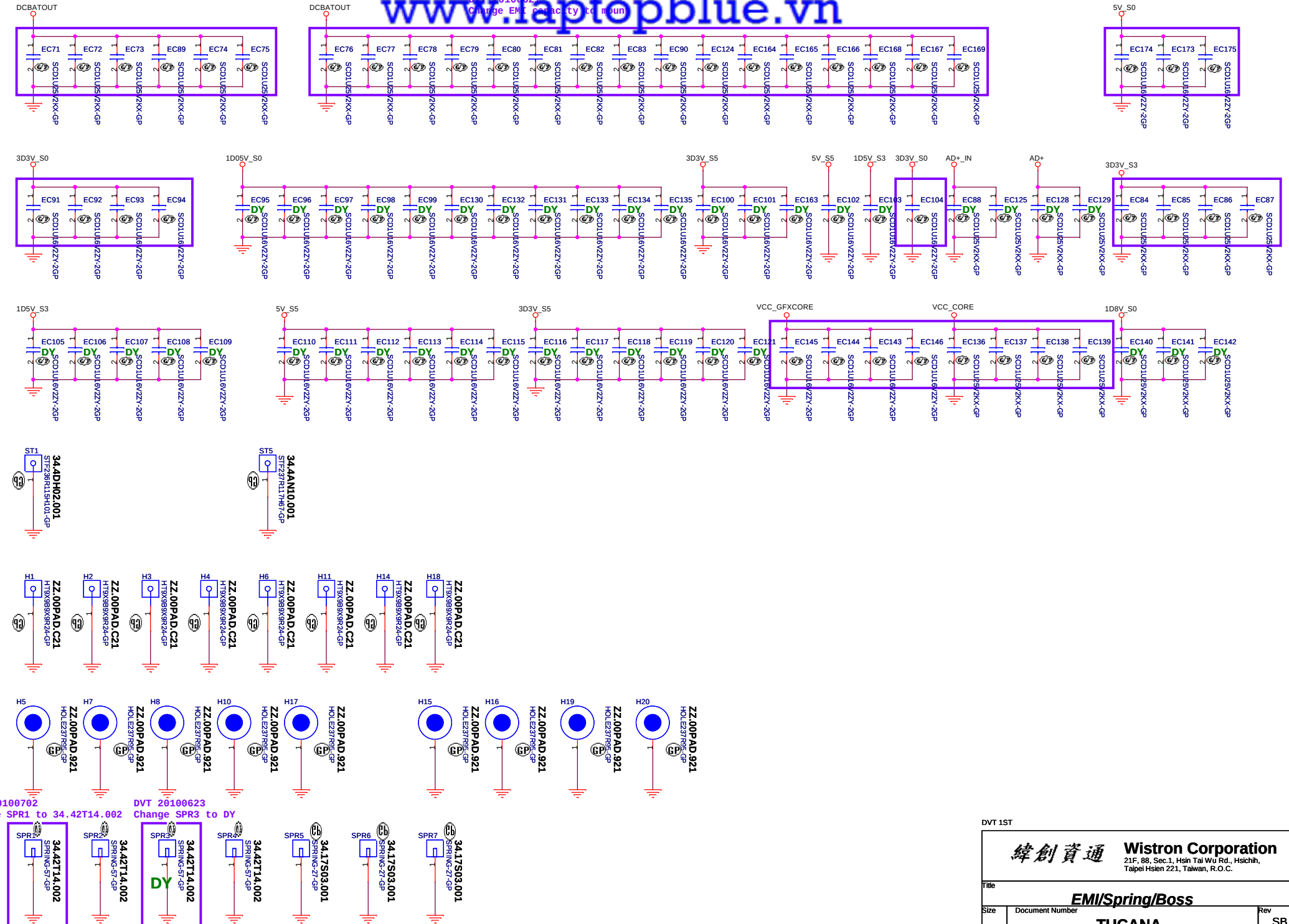
DVT 20100621
Change EMI capacity to mount



DVT 20100702
Change SPR1 to 34.42T14.002

DVT 20100623
Change SPR3 to DY

DVT 1ST

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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EVT

2010/5/17	P.52[BQ24751_Charger]	Del D31 2nd 3rd source
2010/5/17	P.25[HDMI CONN_PS8101]	Change 2nd source to 69.4R500.151
2010/5/24	P.26[HDD Connector]	Change R148 to 3.3K ohm ,add C437 for PM_SLP_S3# Delay
2010/5/27	P.38[KBC_NPCE781L / KB]	Add LCD_DETECT pull-high to 3D3V_S5
2010/5/31	P.52[BQ24751_Charger]	Mount C546,R451,R449,Q51 for battery can't Changer
2010/6/1	P.24[CRT CONN]	Change F6 to 69.44002.001, for Cadiz use
2010/6/4	P.33[Audio Jack]	Change MICIN1 to 20.10133.L11 , follow connector list
	P.28[USB]	Change USB1,USB2,USB3 connector to 22.10321.Q71 [follow ME connector list]
2010/6/10	P.36[AD / BATT CONN]	Change DCIN1 to 20.F0693.006 (follow connector list)
	P.41[FUNCTION BD & POWER BD]	Change PWCN1 to 20.F0693.006 (follow connector list)
2010/6/11	P.41[FUNCTION BD & POWER BD]	Del FUNCN2 connector by ME request
	P.38[KBC_NPCE781L / KB]	Change R240 to 20K ohm SB version.
	P.25[HDMI CONN_PS8101]	Change R614~R617 to 200R2J , Set mount. [for EMI request]
	P.25[HDMI CONN_PS8101]	Change C283,C364 to 1uF [for EMI request]
	P.25[HDMI CONN_PS8101]	Change C282,C285 to 1KpF [for EMI request]
2010/6/21	P.16[PCH (5 of 9)-PCI/USB]	Add PCI_REQ2# Pull-High to 3D3V_S0 by hang-up issue
	P.31[Audio Codec ALC269]	Change EC23,EC24 to mount [for EMI request]
	P.55[EMI/Spring/Boss]	Change DCBATOUT capacity to mount (EC71~83,EC89,EC90,EC124,EC164~169) [for EMI request]
		Change 5V_S0 capacity to mount (EC173~EC175) [for EMI request]
		Change 3D3V_S0 capacity to mount (EC91~94,EC104) [for EMI request]
		Change 3D3V_S3 capacity to mount (EC84~87) [for EMI request]
		Change VCC_GFXCORE capacity to mount (EC142~146) [for EMI request]
		Change VCC_CORE capacity to mount (EC136~139) [for EMI request]
	P.36[AD / BATT CONN]	Change BT+ capacity to mount (EC32~35) [for EMI request]
	P.23[LCD CONN]	Change C258 to 470pF (BRIGHTNESS_CN) [for EMI request]
		Add C272 between BLON_OUT_R and Gnd [for EMI request]
	P.34[CardReader RTS5186]	Change C576~580,C589 to 5pF [CardReader VEVS test]
		Add 0.1uF between MS_INS# and GND [CardReader VEVS test]
	P.24[CRT CONN]	Change R114,R115,R119,R120 to 2.7K ohm [CRT VEVS report]
2010/6/22	P.53[UL CIRCUIT]	UL Circuit modify. [Prevent the RTC_BAT keep protecting.]
2010/6/23	P.40[TouchPad]	Change THPAD1 to 20.K0487.006 [Follow ME connector list]
	P.55[EMI/Spring/Boss]	Change SPR3 to DY [for EMI request]
	P.53[UL CIRCUIT]	Add D42(83.00400.D1F), D41(83.00400.D1F) components. [Reduce the RTC_BAT discharge]
		connect R467 pin1 to D41 and D42 pin k. [Reduce the RTC_BAT discharge]
		connect D42 pin A to AD+_in. [Reduce the RTC_BAT discharge]
		connect D41 pin A to ACP_UVP [Reduce the RTC_BAT discharge]
	P.46[ADP3211_CPU CORE]	Change U45 to 84.08030.037 [Improve High side Vgs induce voltage]
		Change U47 to 84.08028.037 [Improve High side Vgs induce voltage]
		Change U48 to 84.08028.037 [Improve High side Vgs induce voltage]
		add these statements. [follow Power Team design]
		Change R316 to 7.87K ohm (old use 7.32K ohm) [Tune CPU Imon value]
		Change C465 to 680pF (old use 560pF) [Tune CPU load line value]
	P.47[RT8223_5V/3D3V]	Change R353 to 84.5K ohm (old use 97.6K ohm) [Adjust OCP value]
		Change L13 to 2.2uH (old use 3.3uH) [IC needs highter sensing voltage to detect it.]
	P.48[RT8209_1D5V]	Change R377 to 7.5K ohm (old use 11.5K ohm) [Adjust OCP value]
	P.49[RT8209_1D05V]	Change R389 to 14.3K ohm (old use 10.2K ohm) [Adjust OCP value]
		Change L15 to 0.56uH (old use 0.45uH) [Reduce the output ripple voltage]
	P.50[ADP3211_GFX_CORE]	Change R419 to 56.2K ohm (old use 53.6K ohm) [Tune GFX load line value]
		Change TC26 to mount.(old Dummy) [Improve under-shoot voltage phenomenon]
2010/6/25	P.13[PCH (2 of 9)-PCIE/CLK/SMB]	Change C156,C157 to 12pF [for Crystal vendor Test]
	P.29[LAN AR8131M]	Change C346 to 18pF [for Crystal vendor Test]
	P.34[CardReader RTS5186]	Change C384,C388 to 15pF [for Crystal vendor Test]
2010/6/29	P.17[PCH (6 of 9)-GPIO/RSVD]	Change RN31 to R648,R649 (56 ohm) for pull-high 1.05V_S0
		Del R295 , because double pull-high
2010/6/30	P.41[FUNCTION BD & POWER BD]	Change pin define of the FUNCN1 connector [follow the way of FFC folder for ME]
	P.19[PCH (8 of 9)-PWR\SATA\USB]	Del R101 , only use 3D3V_S5
	P.12[PCH (1 of 9)-SATA/RTC/HDA]	Change D1 to 83.R2003.I81 (SCHOTTKY DIODE)
	P.25[HDMI CONN_PS8101]	Change Q12 to 84.2N702.D31 (ESD Protected 1.0KV)
	P.44[RUN POWER]	Change D27 to 83.R2004.B8F (schottky diode)
2010/7/1	P.46[ADP3211_CPU CORE]	Change OPEN-GAP to CLOSE-GAP (G9~14)
	P.47[RT8223_5V/3D3V]	Change OPEN-GAP to CLOSE-GAP (G18,G22,G26,G30,G20,G24,G28,G32)
		Change OPEN-GAP to CLOSE-GAP (G19,G23,G27,G31,G34,G36)
		Change OPEN-GAP to CLOSE-GAP (G21,G25,G29,G33,G35,G37,G38)
	P.48[RT8209_1D5V]	Change OPEN-GAP to CLOSE-GAP (G47,G49,G51,G53)
		Change OPEN-GAP to CLOSE-GAP (G43~46,G48,G50,G52,G54~56)
	P.49[RT8209_1D05V]	Change OPEN-GAP to CLOSE-GAP (G57,G58,G60,G62)
		Change OPEN-GAP to CLOSE-GAP (G59,G61,G63~80)
	P.50[ADP3211_GFX_CORE]	Change OPEN-GAP to CLOSE-GAP (G81~86)
	P.51[RT8015_1D8V/ RT9026_0D75]	Change OPEN-GAP to CLOSE-GAP (G90~95)
	P.41[FUNCTION BD & POWER BD]	Add F7 POLYSW for POWER BD 5V_S5 protect.
	P.54[UVP Protect]	Delete R483 and add RN66. (RN66 part number is 66.10436.04L)
		Connect AD+_IN to RN66 pin 1.
		Connect RN66 pin2 to GND.
		Connect RN66 pin3 and pin4 to AD+_SW_OFF_G_1
	P.53[UL CIRCUIT]	Change R468 part number to the 64.36025.6DL
		Change R469 to the part number 64.30025.6DL
		Cummy R471 and mount D39.
		Delete D40 and RN58.
		Add R642. (Part number is 64.10045.6DL)
		Connect R642 pin 1 to RTC_BAT.
		Connect R642 pin2 to Q52 pin 2 and pin3.
	P.52[BQ24751_Charger]	Connect ACP to R435 pin 1.
	P.27[Bluetooth]	UPDATE BTCN1 PCB LAYOUT (REMOVE THE NPTH)

2010/7/2	P.38[KBC_NPCE781L / KB]	Rename H_PROCHOT# to EC_PROCHOT
	P.5[CPU SFF(2 of 8)-CLK/Thermal]	Add R128 for EC_PROCHOT pull-low to Gnd
	P.5[CPU SFF(2 of 8)-CLK/Thermal]	Add Q61 for EC_PROCHOT to PROCHOT#
	P.33[Audio Jack]	Add EC176 for HP_JD# to GND , Set Dummy for ESD.
		Add EC177 for MIC1_JD# to GND , Set Dummy for ESD.
	P.55[EMI/Spring/Boss]	Change SPR1 to 34.42T14.002
2010/7/5	P.14[PCH (3 of 9)-DMI/FDI]	Change D3 to schottky diode.
	P.37[Thermal / Fan Controllor]	Delelte Q29,Q30 main source 84.T3904.C11, follow CARAVEL-CP design
2010/7/6	P.53[UL CIRCUIT]	Rename R642 Pin1 contact to RTC_BAT_1 (Old use RTC_BAT),follow CARAVEL-CP

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HISTORY_EVT

Size: A2 | Document Number: TUCANA | Rev: SB

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