

HOUSTON14/15_Optimus

CPU : Arrandale BGA
Chip Set : Intel Ibex Peak
GFX : N11P / N11M / INT.GFX
Remarks : Calpella Platform

Model Name : Houston14/15 Optimus
PBA Name : MAIN
PCB Code : BA41-01386A (GCE)
BA41-01387A (NY)
BA41-01388A (HST)
BA41-01389A (GBM)
Dev. Step : PV
Revision : 1.0
T.R. Date : 2010.08.13

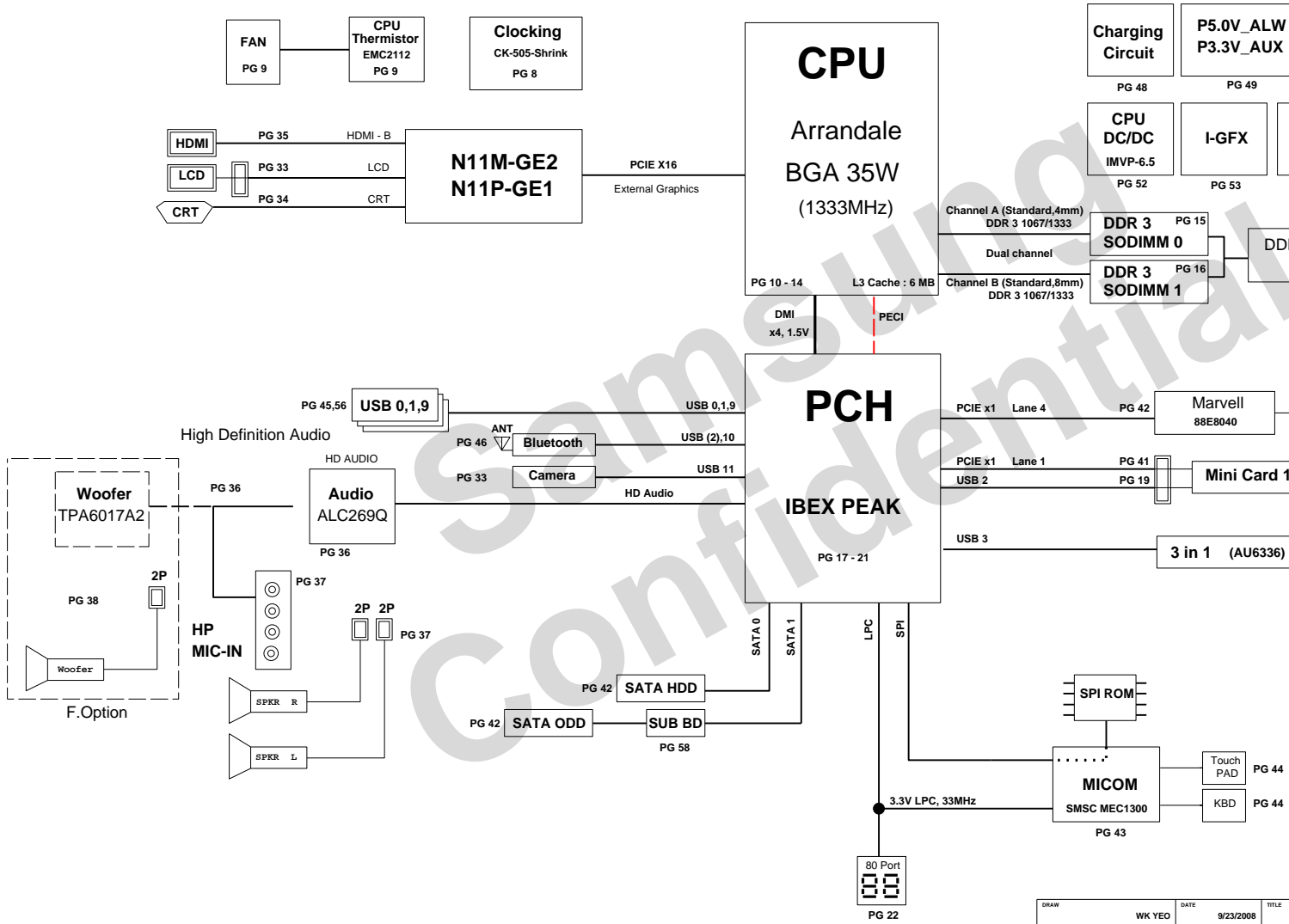
Design	CHECK	APPROVAL

Owner : SEC Mobile R & D Signature : X

sheet01 : Cover
sheet02 : BLOCK DIAGRAM
sheet03 : BOARD INFORMATION
sheet04 : POWER DIAGRAM
sheet05 : POWER RAILS
sheet06 : POWER SEQUENCE
sheet07 : CLOCK DISTRIBUTION
sheet08 : CK505-SHRINK
sheet09 : Thermal Sensor
sheet10 : CPU
sheet11 : CPU
sheet12 : CPU
sheet13 : CPU
sheet14 : CPU
sheet15 : DDR3 SODIMM #0
sheet16 : DDR3 SODIMM #1
sheet17 : PCH-IbexPeak
sheet18 : PCH-IbexPeak
sheet19 : PCH-IbexPeak
sheet20 : PCH-IbexPeak
sheet21 : PCH-IbexPeak
sheet22 : 80 port
sheet23 : N11X-GE2/GE1
sheet24 : N11X-GE2/GE1
sheet25 : N11X-GE2/GE1
sheet26 : N11X-GE2/GE1
sheet27 : N11X-GE2/GE1
sheet28 : GFX memory
sheet29 : GFX memory
sheet30 : GFX memory
sheet31 : GFX
sheet32 : N11X
sheet33 : LVDS
sheet34 : CRT
sheet35 : HDMI
sheet36 : Audio
sheet37 : Audio
sheet38 : WOO
sheet39 : LAN
sheet40 : 3-in-1
sheet41 : WLAN
sheet42 : SATA
sheet43 : MICC
sheet44 : MICC
sheet45 : LED
sheet46 : USB
sheet47 : Blueto
sheet48 : Powe
sheet49 : Powe
sheet50 : Powe
sheet51 : Powe
sheet52 : Powe
sheet53 : Powe
sheet54 : Powe
sheet55 : Powe
sheet56 : Powe
sheet57 : Powe
sheet58 : USB/
sheet59 : ODD
sheet60 : ICT F

DRAW	WK YEO	DATE	10/10/2008	TITLE
CHECK	BW YOO	DEV. STEP	PR	
APPROVAL	SH LEE	REV	REV 1.0	
MODULE CODE		LAST EDIT		

BLOCK DIAGRAM



DRAW	WK YEO	DATE	9/23/2008	TITLE
CHECK	BW YOO	DEV. STEP	PR	
APPROVAL	SH LEE	REV	REV 1.0	
MODULE CODE	undefined	LAST EDIT		

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails		Active in
VDC P3.3V_MICOM P5.0V_ALW P5.0V_STB	Primary DC system power supply (7 to 21V) 3.3V always power rail (for Micom) 5.0V always power rail 5.0V always power rail	S4 - S5
P5.0V_AUX P3.3V_AUX P1.5V_AUX	5.0V switched on power rail (off in S4-S5) 3.3V switched on power rail (off in S4-S5) 1.5V power rail for DDR (off in S4-S5)	S3
P5.0V P3.3V P1.8V P1.5V P0.75V	5.0V switched power rail (off in S3-S5) 3.3V switched power rail (off in S3-S5) 1.8V switched power rail (off in S3-S5) 1.5V switched power rail (off in S3-S5) 0.9V power rail for DDR (off in S3-S5)	S0
VCC_CORE EGFX_CORE P1.05V (VCCP) P1.1V_VTT	Core Voltage for CPU Core Voltage for GPU VCC for Clarksfield & IBEX Peak VTT for CLARDSFIELD & IBEX Peak	S0

USB PORT Assign		PCI Express Assign	
PORT #	ASSIGNED TO	PORT #	ASSIGNED TO
0	SYSTEM PORT 0	1	Mini Card 1 (WLAN)
1	SYSTEM PORT 1	2	NC
2	Mini PCI Express	3	NC
3	Multi Memory Card Controller	4	LAN CONTROLLER
4	NC	5	NC
5	NC	6	NC
6	NC (N/A WITH HM55)	7	NC (N/A WITH HM55)
7	NC (N/A WITH HM55)	8	NC (N/A WITH HM55)
8	NC		
9	SYSTEM PORT 2		
10	Bluetooth		
11	Camera		
12	NC		
13	NC		

SATA PORT Assign	
PORT #	ASSIGNED TO
0	HDD
1	ODD
2	(N/A WITH HM55)
3	(N/A WITH HM55)
4	
5	

Crystal / Oscillator			
TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	IBEX-PEAK	Real Time Clock
Crystal	10MHz	MICOM	HD64F2169/21
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	25MHz	LAN	Intel LAN
Crystal	25MHz	IBEX PEAK	

LCD Pannel Detect (TBD)		
Devices	Resolution	PANNEL_DETECT_0

I ² C / SMB Address			
Devices	Address	Hex	Bus
IBEX PEAK	Master	-	SMBUS Master
CPU Thermal Sensor	0111 101x	7Ah	Thermal Sensor
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M Shrink(Clock Generator)	1101 001x	D2h	Clock, Unused Clock
Thermal Sensor on board	1101 100x	98h	
Power thermal management TS	1101 011x	96h	

DRAW	WK YEO	DATE	9/23/2008	TITLE
CHECK	BW YOO	DEV. STEP	PR	
APPROVAL	SH LEE	REV	REV 1.0	
MODULE CODE	undefined	LAST EDIT		

KBC3_SUSPWR

KBC3_PWRON

AC Adapter

Battery DC

VDC

P1.05V

ARD
IBEX PEAK

IGFX_CORE

INT GFX

EGFX_CORE

EXT GFX
Nvidia N11P

P1.5V_AUX

DDR3 MEMORY
PCH

P1.5V

gDDR-3 for EGF

P0.75V

DDR3 MEMORY

USB CONN

P5.0V_ALW

When USB Charge Enable

P5.0V_AUX

P5.0V

HDD CRT M
FAN PEG H

P3.3V_AUX

PCH
LAN

P3.3V

IBEX PEAK
MICOM
HD AUDIO M

P3.3V_MICOM

SPI ROM
MICOM

P5.0V_STB

P12.0V_ALW

P2.5V_LAN

LAN

P1.8V

IBEX PEAK
Nvidia n11P

Power On/Off Table by S-state

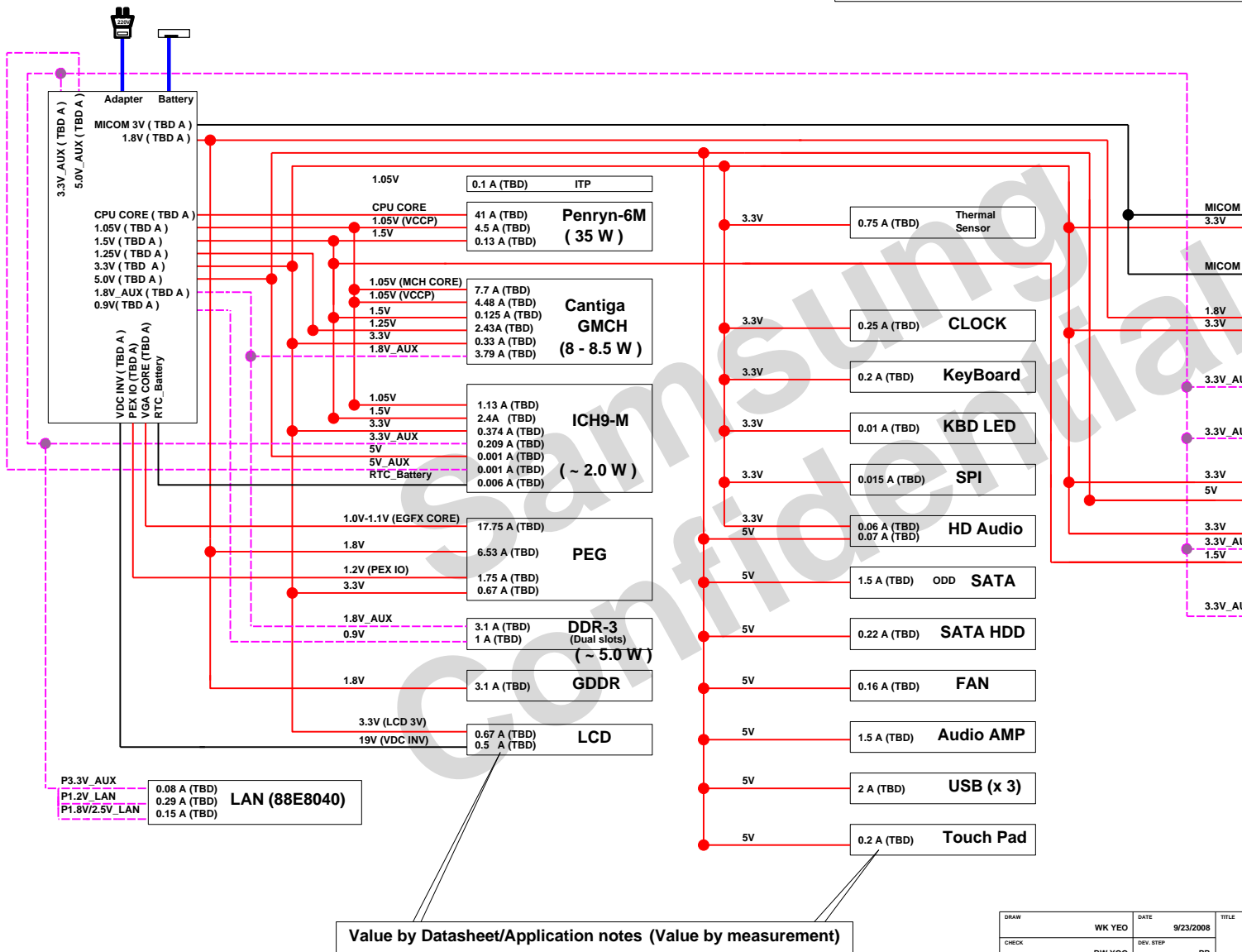
Rail State	S0	S3	S4	S5
+V*A(LWS) +V*LAN	ON	ON	ON	ON
+1.8V_AUX +0.9V	ON	ON	—	—
+V*AUX	ON	ON	—	—
+V	ON	—	—	—
+V* (CORE)	ON	—	—	—

S5-S4

S3

DRAW	WK YEO	DATE	9/23/2008	TITLE
CHECK	BW YOO	DEV. STEP	PR	
APPROVAL	SH LEE	REV	REV 1.0	
MODULE CODE	undefined	LAST EDIT		

POWER RAILS ANALYSIS



DRAW	WK YEO	DATE	9/23/2008	TITLE
CHECK	BW YOO	DEV. STEP	PR	
APPROVAL	SH LEE	REV	REV 1.0	
MODULE CODE	undefined	LAST EDIT		