

DRAWING

TITLE=K62

ABBREV=DRAWING

LAST_MODIFIED=

Tue Feb 8 15:20:30 2011

DRAWING TITLE

SCH, K62, MLB

Apple Inc.

051-8442

10.1.0

1 OF 110

1 OF 101

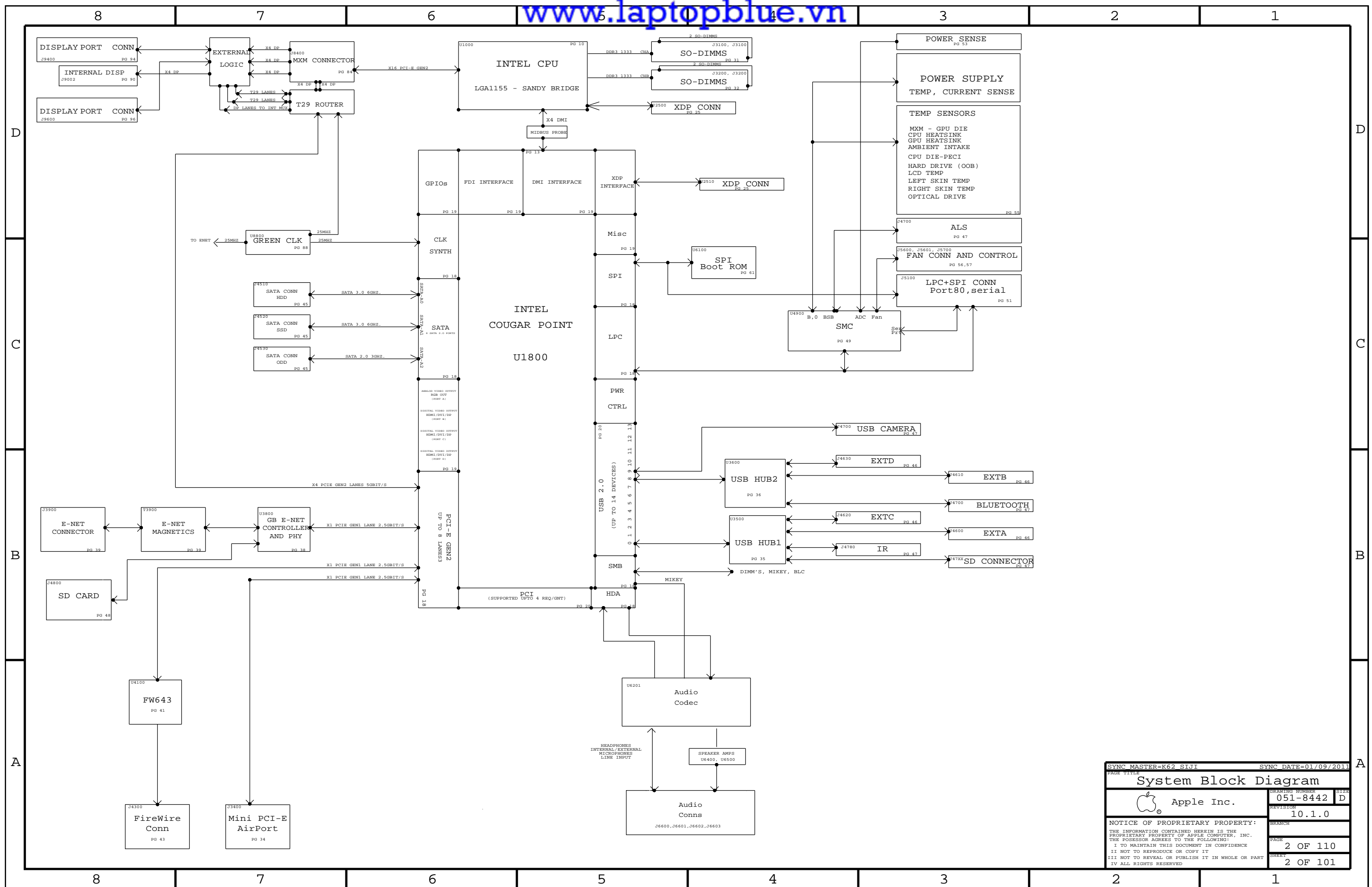
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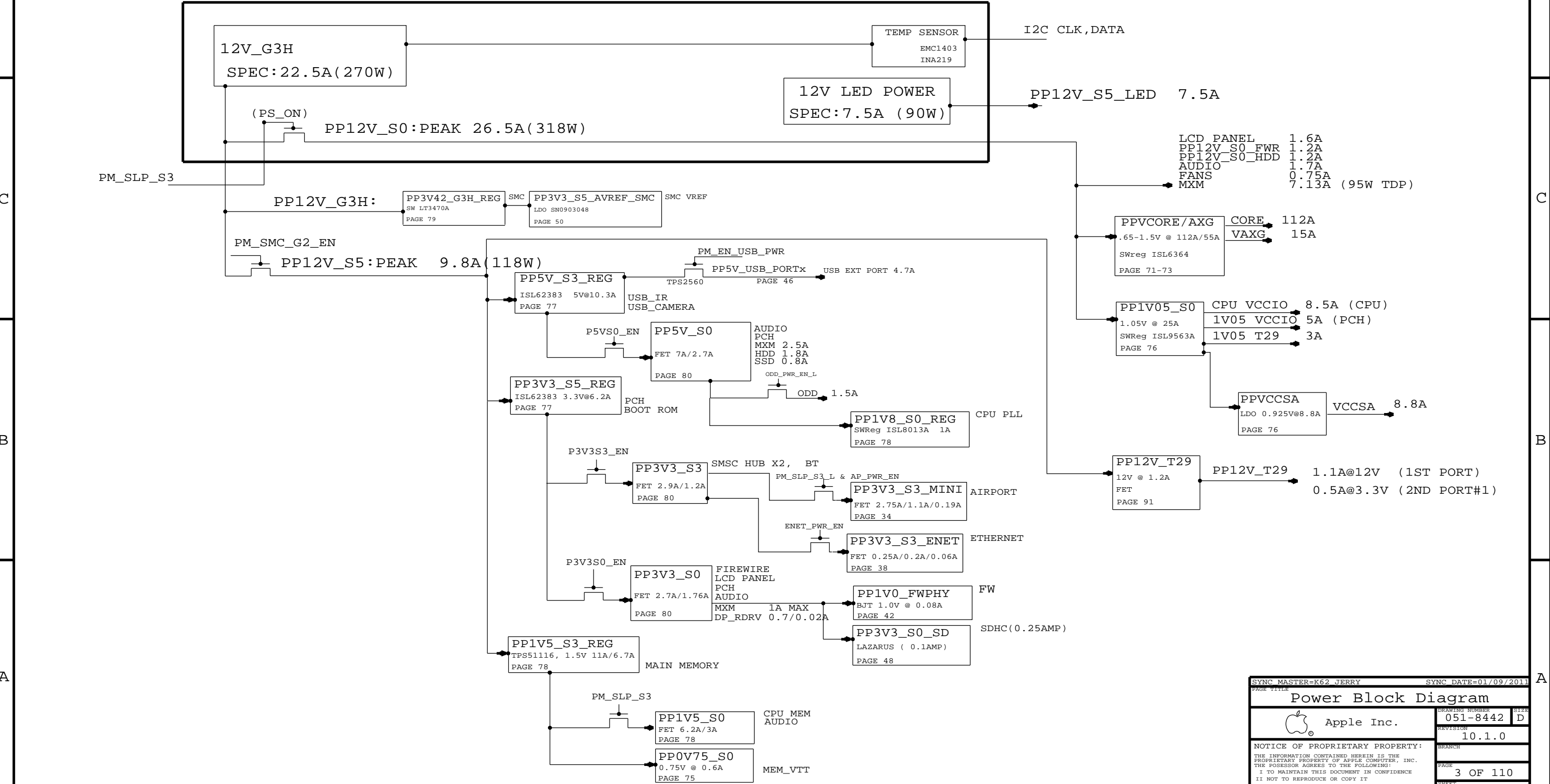
C

B

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A



PAGE TITLE		PAGE TITLE	
Power Block Diagram		Power Block Diagram	
Apple Inc.		DRAWING NUMBER	051-8442
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D

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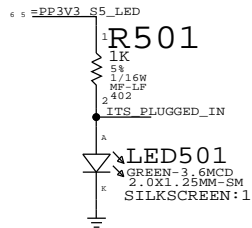
BOARD STACK-UP

BOTTOM

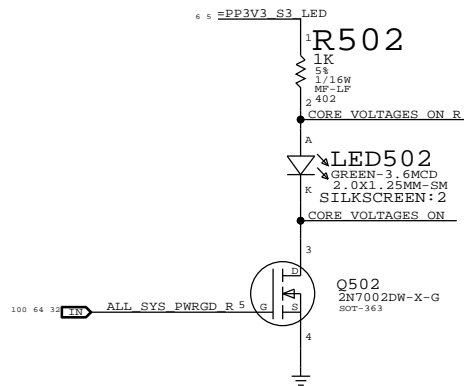
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RAW: 335S0539RAW: 335S0550RAW: 337S3997RAW: 338S0878CPUSK62 PARTSK62 ALTERNATE PARTS

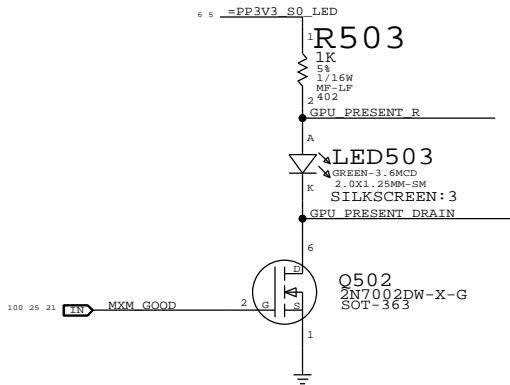
S5 Led



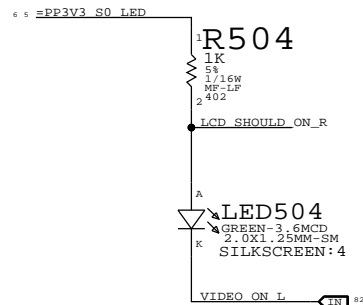
ALL_SYS_PWRGD Led



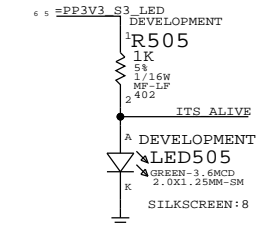
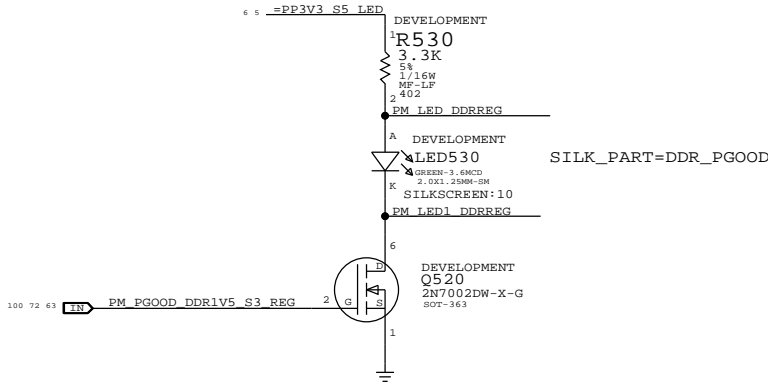
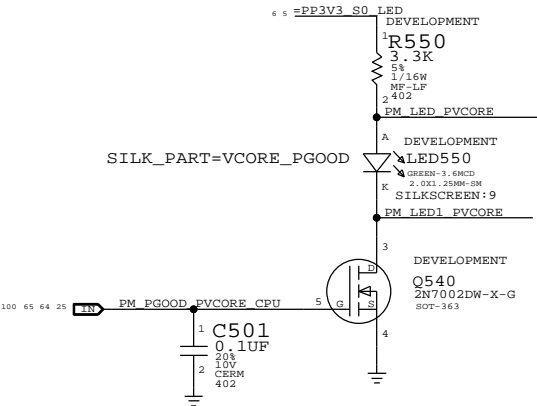
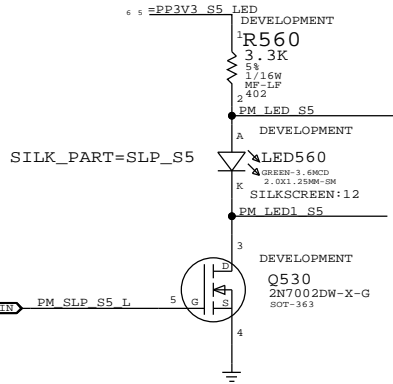
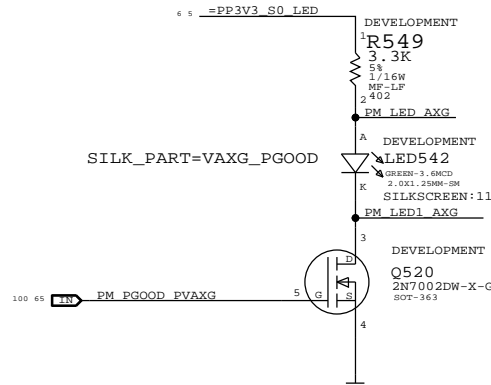
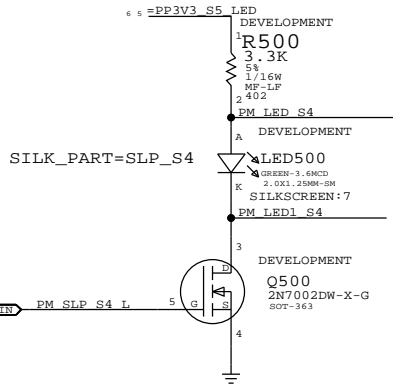
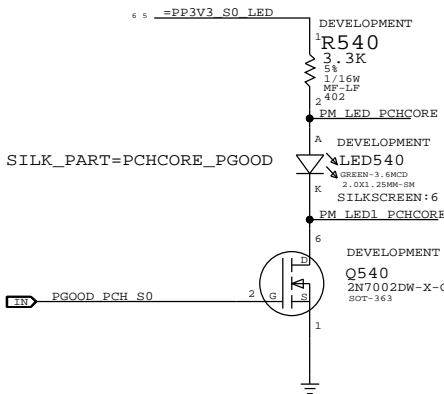
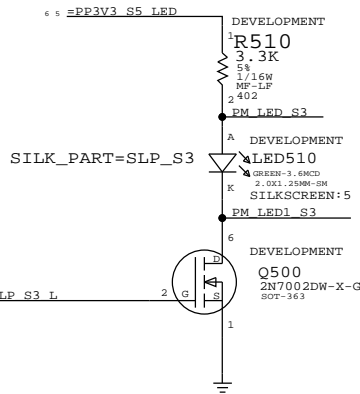
MXM PWR GOOD Led



VIDEO ON Led

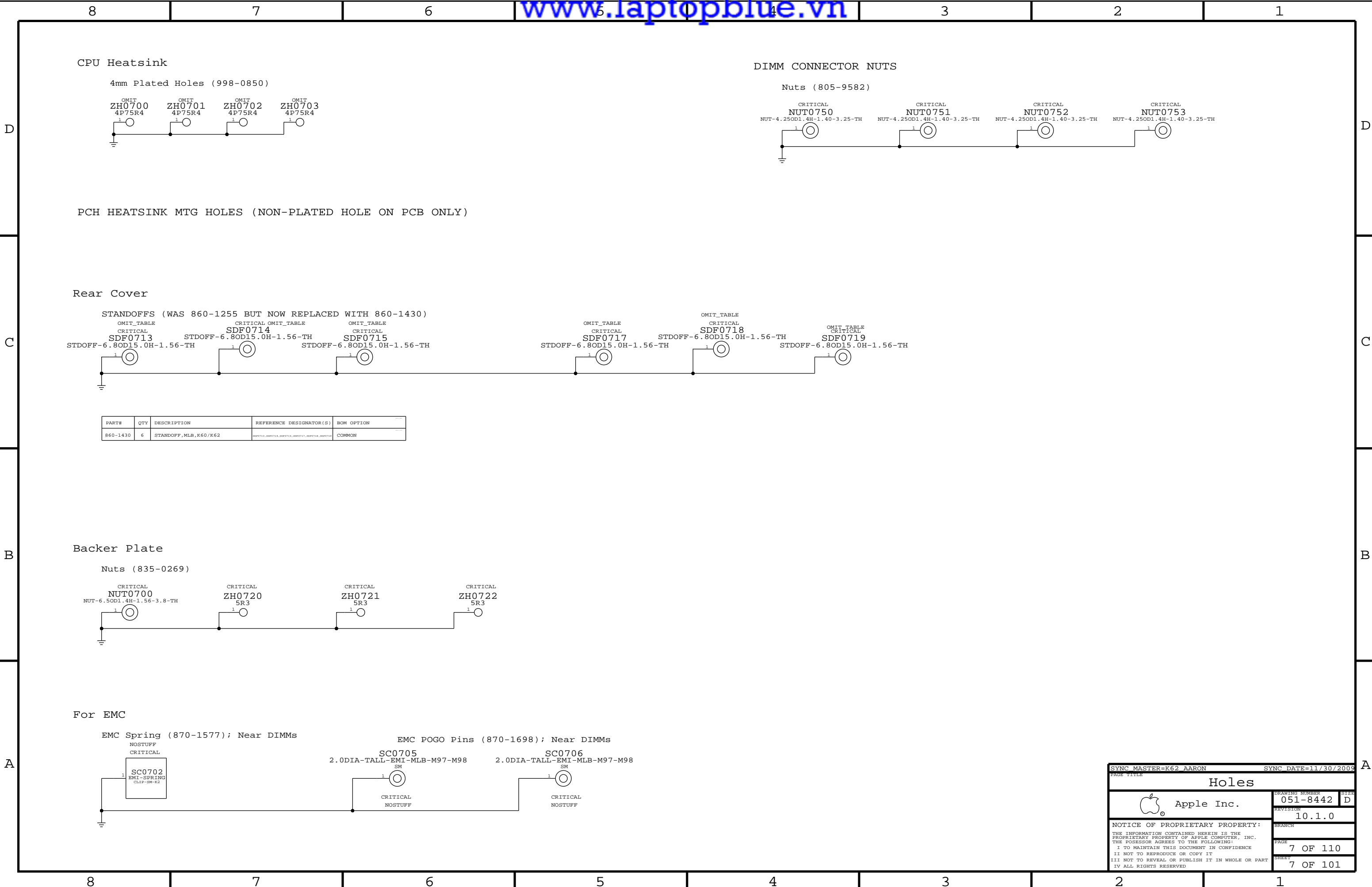


PROTO DEBUG LEDS ARE SHOWN BELOW



PAGE TITLE		SYNC MASTER=K62 AARON		SYNC DATE=07/01/2009	
DEBUG LEDS		DRAWING NUMBER		SIZE	
Apple Inc.		051-8442		D	
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8		7		6		5		4		3		2		1					
UNUSED CPU SIGNALS		NC ON UNUSED PCIE ALIASES		NC ON UNUSED DISPLAY ALIASES		NC ON UNUSED FDI ALIASES													
<div><div>10</div><div>TP CPU RSVD<16..1> == NC CPU RSVD<16..1> MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP CPU RSVD<46..19> == NC CPU RSVD<46..19> MAKE_BASE=TRUE NO_TEST=TRUE</div></div>		<div><div>18</div><div>TP PCIE CLK100M PE5P == NC PCIE CLK100M PE5P MAKE_BASE=TRUE NO_TEST=TRUE</div><div>18</div><div>TP PCIE CLK100M PE5N == NC PCIE CLK100M PE5N MAKE_BASE=TRUE NO_TEST=TRUE</div><div>21</div><div>TP PCIE CLK100M PE6P == NC PCIE CLK100M PE6P MAKE_BASE=TRUE NO_TEST=TRUE</div><div>21</div><div>TP PCIE CLK100M PE6N == NC PCIE CLK100M PE6N MAKE_BASE=TRUE NO_TEST=TRUE</div><div>21</div><div>TP PCIE CLK100M PE7P == NC PCIE CLK100M PE7P MAKE_BASE=TRUE NO_TEST=TRUE</div><div>21</div><div>TP PCIE CLK100M PE7N == NC PCIE CLK100M PE7N MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP PE RX N<3..0> == NC PE RXN<3..0> MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP PE RX P<3..0> == NC PE RXP<3..0> MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP PE TX N<3..0> == NC PE TXN<3..0> MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP PE TX P<3..0> == NC PE TXP<3..0> MAKE_BASE=TRUE NO_TEST=TRUE</div><div>18</div><div>TP PCIE D2R PERN4 == NC PCIE D2R PERN4 MAKE_BASE=TRUE NO_TEST=TRUE</div><div>18</div><div>TP PCIE D2R PERP4 == NC PCIE D2R PERP4 MAKE_BASE=TRUE NO_TEST=TRUE</div><div>18</div><div>TP PCIE R2D PETN4 == NC PCIE R2D PETN4 MAKE_BASE=TRUE NO_TEST=TRUE</div><div>18</div><div>TP PCIE R2D PETP4 == NC PCIE R2D PETP4 MAKE_BASE=TRUE NO_TEST=TRUE</div><div>18</div><div>TP PCIE CLK100M PE4P == NC PCIE CLK100M PE4P MAKE_BASE=TRUE NO_TEST=TRUE</div><div>18</div><div>TP PCIE CLK100M PE4N == NC PCIE CLK100M PE4N MAKE_BASE=TRUE NO_TEST=TRUE</div><div>18</div><div>TP LPC DREQ0 L == NC LPC DREQ0 L MAKE_BASE=TRUE NO_TEST=TRUE</div></div>		<div><div>10</div><div>TP CRT IG DDC CLK == NC CRT IG DDC CLK MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP CRT IG DDC DATA == NC CRT IG DDC DATA MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP CRT IG RED == NC CRT IG RED MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP CRT IG GREEN == NC CRT IG GREEN MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP CRT IG BLUE == NC CRT IG BLUE MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP CRT IG HSYNC == NC CRT IG HSYNC MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP CRT IG VSYNC == NC CRT IG VSYNC MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP DP IG B MLN<3..0> == NC DP IG B MLN<3..0> MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP DP IG B MLP<3..0> == NC DP IG B MLP<3..0> MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP DP IG B AUX N == NC DP IG B AUXN MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP DP IG B AUX P == NC DP IG B AUXP MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP DP IG B HPD == NC DP IG B HPD MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP DP IG B DDC CLK == NC DP IG B CTRL CLK MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP DP IG B DDC DATA == NC DP IG B CTRL DATA MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP DP IG C MLN<3..0> == NC DP IG C MLN<3..0> MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP DP IG C MLP<3..0> == NC DP IG C MLP<3..0> MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP DP IG C AUX N == NC DP IG C AUXN MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP DP IG C AUX P == NC DP IG C AUXP MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP DP IG C HPD == NC DP IG C HPD MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP DP IG C CTRL CLK == NC DP IG C CTRL CLK MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP DP IG C CTRL DATA == NC DP IG C CTRL DATA MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP DP IG D MLN<3..0> == NC DP IG D MLN<3..0> MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP DP IG D MLP<3..0> == NC DP IG D MLP<3..0> MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP DP IG D AUXN == NC DP IG D AUXN MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP DP IG D AUXP == NC DP IG D AUXP MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP DP IG D HPD == NC DP IG D HPD MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP DP IG D CTRL CLK == NC DP IG D CTRL CLK MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP DP IG D CTRL DATA == NC DP IG D CTRL DATA MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP SDVO TVCLKINN == NC SDVO TVCLKINN MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP SDVO TVCLKINP == NC SDVO TVCLKINP MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP SDVO STALLN == NC SDVO STALLN MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP SDVO STALLP == NC SDVO STALLP MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP SDVO INTN == NC SDVO INTN MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP SDVO INTP == NC SDVO INTP MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP PCH L BKLCTL == NC PCH L BKLCTL MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP PCH L BKLTEN == NC PCH L BKLTEN MAKE_BASE=TRUE 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MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP SATA E D2RN == NC SATA E D2RN MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP SATA E D2RP == NC SATA E D2RP MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP SATA E R2D CN == NC SATA E R2D CN MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP SATA E R2D CP == NC SATA E R2D CP MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP SATA F D2RN == NC SATA F D2RN MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP SATA F D2RP == NC SATA F D2RP MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP SATA F R2D CN == NC SATA F R2D CN MAKE_BASE=TRUE NO_TEST=TRUE</div><div>10</div><div>TP SATA F R2D CP == NC SATA F R2D CP MAKE_BASE=TRUE NO_TEST=TRUE</div></div>													
NC ON UNUSED PCI ALIASES						NC ON UNUSED SATA ALIASES													
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NC ON UNUSED MEM ALIASES		NC ON UNUSED USB ALIASES																	
<div><div>12</div><div>TP MEM A DQ CB<7..0> == NC MEM A DQ CB<7..0> MAKE_BASE=TRUE NO_TEST=TRUE</div><div>12</div><div>TP MEM A DOS N<8> == NC MEM A DOSN<8> MAKE_BASE=TRUE NO_TEST=TRUE</div><div>12</div><div>TP MEM A DOS P<8> == NC MEM A DOSP<8> MAKE_BASE=TRUE NO_TEST=TRUE</div><div>12</div><div>TP MEM B DQ CB<7..0> == NC MEM B DQ CB<7..0> MAKE_BASE=TRUE NO_TEST=TRUE</div><div>12</div><div>TP MEM B DOS N<8> == NC MEM B DOSN<8> MAKE_BASE=TRUE NO_TEST=TRUE</div><div>12</div><div>TP MEM B DOS P<8> == NC MEM B DOSP<8> MAKE_BASE=TRUE NO_TEST=TRUE</div></div>		<div><div>20</div><div>TP USB 1N == NC USB 1N MAKE_BASE=TRUE NO_TEST=TRUE</div><div>20</div><div>TP USB 1P == NC USB 1P MAKE_BASE=TRUE NO_TEST=TRUE</div><div>20</div><div>TP USB 2N == NC USB 2N MAKE_BASE=TRUE NO_TEST=TRUE</div><div>20</div><div>TP USB 2P == NC USB 2P MAKE_BASE=TRUE NO_TEST=TRUE</div><div>20</div><div>TP USB 3N == NC USB 3N MAKE_BASE=TRUE NO_TEST=TRUE</div><div>20</div><div>TP USB 3P == NC USB 3P MAKE_BASE=TRUE NO_TEST=TRUE</div><div>20</div><div>TP USB 4N == NC USB 4N MAKE_BASE=TRUE NO_TEST=TRUE</div><div>20</div><div>TP USB 4P == NC USB 4P MAKE_BASE=TRUE NO_TEST=TRUE</div><div>20</div><div>TP USB 5N == NC USB 5N MAKE_BASE=TRUE NO_TEST=TRUE</div><div>20</div><div>TP USB 5P == NC USB 5P MAKE_BASE=TRUE NO_TEST=TRUE</div><div>20</div><div>TP USB 6N == NC USB 6N MAKE_BASE=TRUE NO_TEST=TRUE</div><div>20</div><div>TP USB 6P == NC USB 6P MAKE_BASE=TRUE NO_TEST=TRUE</div><div>20</div><div>TP USB 7N == NC USB 7N MAKE_BASE=TRUE NO_TEST=TRUE</div><div>20</div><div>TP USB 7P == NC USB 7P MAKE_BASE=TRUE NO_TEST=TRUE</div><div>20</div><div>TP USB 10N == NC USB 10N MAKE_BASE=TRUE NO_TEST=TRUE</div><div>20</div><div>TP USB 10P == NC USB 10P MAKE_BASE=TRUE NO_TEST=TRUE</div><div>20</div><div>TP USB 11N == NC USB 11N MAKE_BASE=TRUE NO_TEST=TRUE</div><div>20</div><div>TP USB 11P == NC USB 11P MAKE_BASE=TRUE NO_TEST=TRUE</div><div>20</div><div>TP USB 12N == NC USB 12N MAKE_BASE=TRUE NO_TEST=TRUE</div><div>20</div><div>TP USB 12P == NC USB 12P MAKE_BASE=TRUE NO_TEST=TRUE</div><div>20</div><div>TP USB 13N == NC USB 13N MAKE_BASE=TRUE NO_TEST=TRUE</div><div>20</div><div>TP USB 13P == NC USB 13P MAKE_BASE=TRUE NO_TEST=TRUE</div></div>																	
NC ON UNUSED MISC ALIASES																			
<div><div>18</div><div>TP HDA SDIN1 == NC HDA SDIN1 MAKE_BASE=TRUE NO_TEST=TRUE</div><div>18</div><div>TP HDA SDIN2 == NC HDA SDIN2 MAKE_BASE=TRUE NO_TEST=TRUE</div><div>18</div><div>TP HDA SDIN3 == NC HDA SDIN3 MAKE_BASE=TRUE NO_TEST=TRUE</div><div>21</div><div>TP PCH PWM0 == NC PCH PWM0 MAKE_BASE=TRUE NO_TEST=TRUE</div><div>21</div><div>TP PCH PWM1 == NC PCH PWM1 MAKE_BASE=TRUE NO_TEST=TRUE</div><div>21</div><div>TP PCH PWM2 == NC PCH PWM2 MAKE_BASE=TRUE NO_TEST=TRUE</div><div>21</div><div>TP PCH PWM3 == NC PCH PWM3 MAKE_BASE=TRUE NO_TEST=TRUE</div><div>21</div><div>TP PCH SST == NC PCH SST MAKE_BASE=TRUE NO_TEST=TRUE</div><div>18</div><div>TP PCH CL CLK1 == NC PCH CL CLK1 MAKE_BASE=TRUE NO_TEST=TRUE</div><div>18</div><div>TP PCH CL DATA1 == NC PCH CL DATA1 MAKE_BASE=TRUE NO_TEST=TRUE</div><div>18</div><div>TP PCH CL RST1 == NC PCH CL RST1 MAKE_BASE=TRUE NO_TEST=TRUE</div></div>																			
8		7		6		5		4		3		2		1					

SYNC_MASTER=K62_S1J1

SYNC_DATE=01/09/2011

UNUSED SIGNAL ALIAS

Apple Inc.


051-8442

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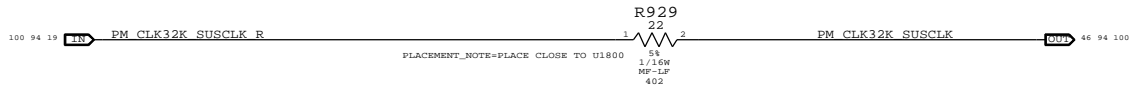
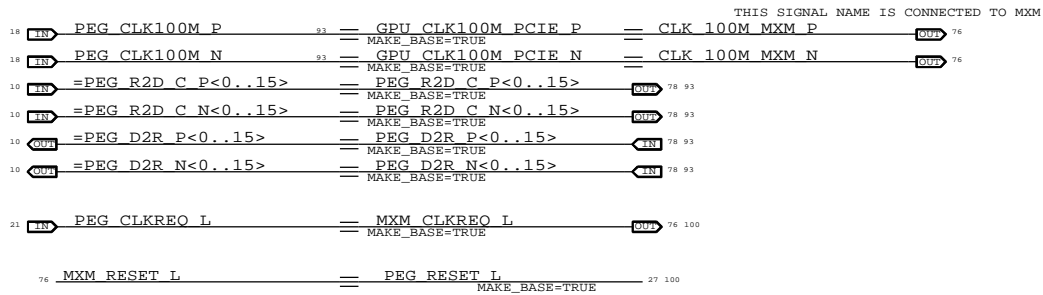
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SYNC MASTER=K62 SIJI		SYNC DATE=01/09/2011	
PAGE TITLE			
UNUSED SIGNAL ALIAS			
 Apple Inc.		DRAWING NUMBER	051-8442
		SIZE	D
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PEG Slot Support



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PAGE TITLE			
Signal Aliases			
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		REVISION	10.1.0
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SHORT B4 & C4 TOGETHER, ROUTE AS A SINGLE 4 MIL TRACE TO R1010.1
ROUTE B5 TO R1010.1 AS A SEPARATE 10 MIL TRACE.

PLACEMENT_NOTE=Place within 12.7MM of CPU

=PEVCCIO S0 CPU 6 11 13 16 65

R1010
24.9
1 2
1/16W
MF-LP
402

MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPER=CPU_RCOMP

MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPER=CPU_RCOMP

OMIT
U1000
SANDYBRIDGE
LGA1155-SKT
(5 OF 10)

RESERVED

TP CPU RSVD<1>	C38	RSVD_C38	RSVD_P35	P35	TP CPU RSVD<20>
TP CPU RSVD<2>	C39	RSVD_C39	RSVD_P37	P37	TP CPU RSVD<21>
TP CPU RSVD<3>	D38	RSVD_D38	RSVD_P39	P39	TP CPU RSVD<22>
TP CPU RSVD<4>	H7	RSVD_H7	RSVD_R34	R34	TP CPU RSVD<23>
TP CPU RSVD<5>	H8	RSVD_H8	RSVD_R36	R36	TP CPU RSVD<24>
TP CPU RSVD<6>	J9	RSVD_J9	RSVD_R38	R38	TP CPU RSVD<25>
TP CPU RSVD<7>	J31	RSVD_J31	RSVD_R40	R40	TP CPU RSVD<26>
TP CPU RSVD<8>	J33	RSVD_J33	RSVD_AB6	AB6	TP CPU RSVD<27>
TP CPU RSVD<9>	J34	RSVD_J34	RSVD_AB7	AB7	TP CPU RSVD<28>
TP CPU RSVD<10>	K9	RSVD_K9	RSVD_AD34	AD34	TP CPU RSVD<29>
TP CPU RSVD<11>	K31	RSVD_K31	RSVD_AD35	AD35	TP CPU RSVD<30>
TP CPU RSVD<12>	K34	RSVD_K34	RSVD_AD37	AD37	TP CPU RSVD<31>
TP CPU RSVD<13>	L9	RSVD_L9	RSVD_AE6	AE6	TP CPU RSVD<32>
TP CPU RSVD<14>	L31	RSVD_L31	RSVD_AF4	AF4	TP CPU RSVD<33>
TP CPU RSVD<15>	L33	RSVD_L33	RSVD_AG4	AG4	TP CPU RSVD<34>
TP CPU RSVD<16>	L34	RSVD_L34	RSVD_AJ11	AJ11	TP CPU RSVD<35>
SNS CPU THERMD N	M34	RSVD_M34 ThermDC	RSVD_AJ29	AJ29	TP CPU RSVD<36>
SNS CPU THERMD P	N33	RSVD_N33 ThermDA	RSVD_AJ30	AJ30	TP CPU RSVD<37>
TP CPU RSVD<19>	N34	RSVD_N34	RSVD_AJ31	AJ31	TP CPU RSVD<38>
CPU CFG<0>	H36	CFG_0	RSVD_AN20	AN20	TP CPU RSVD<39>
CPU CFG<1>	J36	CFG_1	RSVD_AP20	AP20	TP CPU RSVD<40>
CPU CFG<2>	J37	CFG_2	RSVD_AT11	AT11	TP CPU RSVD<41>
CPU CFG<3>	K36	CFG_3	RSVD_AT14	AT14	TP CPU RSVD<42>
CPU CFG<4>	L36	CFG_4	RSVD_AU10	AU10	TP CPU RSVD<43>
CPU CFG<5>	N35	CFG_5	RSVD_AV34	AV34	TP CPU RSVD<44>
CPU CFG<6>	L37	CFG_6	RSVD_AW34	AW34	TP CPU RSVD<45>
CPU CFG<7>	M36	CFG_7	RSVD_AY10	AY10	TP CPU RSVD<46>
CPU CFG<8>	J38	CFG_8	RSVD_NCTF_AV1	AV1	TP CPU RSVD NCTF<1>
CPU CFG<9>	L35	CFG_9	RSVD_NCTF_AW2	AW2	TP CPU RSVD NCTF<2>
CPU CFG<10>	M38	CFG_10	RSVD_NCTF_AY3	AY3	TP CPU RSVD NCTF<3>
CPU CFG<11>	N36	CFG_11	RSVD_NCTF_B39	B39	TP CPU RSVD NCTF<4>
CPU CFG<12>	N38	CFG_12	NCTF_A38	A38	TP CPU NCTF<1>
CPU CFG<13>	N39	CFG_13	NCTF_C2	C2	TP CPU NCTF<2>
CPU CFG<14>	N37	CFG_14	NCTF_D1	D1	TP CPU NCTF<3>
CPU CFG<15>	N40	CFG_15	NCTF_AU40	AU40	TP CPU NCTF<4>
CPU CFG<16>	G37	CFG_16	NCTF_AW38	AW38	TP CPU NCTF<5>
CPU CFG<17>	G36	CFG_17			

FOR SANDYBRIDGE PROCESSOR

CFG [6:5] :PCIE CONFIGURATION SELECT 11 = 1 X16 (DEFAULT) 10 = 2 X8 01 = RSVD 00 = X8, X4, X4
CFG [2] :PCIE LANE REVERSAL 1 = NORMAL OPERATION 0 = LANES REVERSED

OMIT
U1000
SANDYBRIDGE
LGA1155-SKT
(1 OF 10)

DMI

FLEXIBLE DISPLAY INTERFACE
(Unused)

PCI EXPRESS -- GRAPHICS

PCI EXPRESS
(Available for Workstation only)

(Available for Workstation only)

DMI_S2N N<0>	W4	DMI_RX_0*
DMI_S2N N<1>	V4	DMI_RX_1*
DMI_S2N N<2>	Y4	DMI_RX_2*
DMI_S2N N<3>	AA4	DMI_RX_3*
DMI_S2N P<0>	W5	DMI_RX_0
DMI_S2N P<1>	V5	DMI_RX_1
DMI_S2N P<2>	Y5	DMI_RX_2
DMI_S2N P<3>	AA5	DMI_RX_3
DMI_N2S N<0>	V6	DMI_TX_0*
DMI_N2S N<1>	W6	DMI_TX_1*
DMI_N2S N<2>	Y6	DMI_TX_2*
DMI_N2S N<3>	AA6	DMI_TX_3*
DMI_N2S P<0>	V7	DMI_TX_0
DMI_N2S P<1>	W7	DMI_TX_1
DMI_N2S P<2>	Y7	DMI_TX_2
DMI_N2S P<3>	AA7	DMI_TX_3

TP CPU FDI TX N<0>	AC7	FDI_TX_0*
TP CPU FDI TX N<1>	AC3	FDI_TX_1*
TP CPU FDI TX N<2>	AD1	FDI_TX_2*
TP CPU FDI TX N<3>	AD3	FDI_TX_3*
TP CPU FDI TX N<4>	AD6	FDI_TX_4*
TP CPU FDI TX N<5>	AE8	FDI_TX_5*
TP CPU FDI TX N<6>	AF2	FDI_TX_6*
TP CPU FDI TX N<7>	AG1	FDI_TX_7*
TP CPU FDI TX P<0>	AC8	FDI_TX_0
TP CPU FDI TX P<1>	AC2	FDI_TX_1
TP CPU FDI TX P<2>	AD2	FDI_TX_2
TP CPU FDI TX P<3>	AD4	FDI_TX_3
TP CPU FDI TX P<4>	AD7	FDI_TX_4
TP CPU FDI TX P<5>	AE7	FDI_TX_5
TP CPU FDI TX P<6>	AF3	FDI_TX_6
TP CPU FDI TX P<7>	AG2	FDI_TX_7

CPU FDI PSYNC<0>	AC5	FDI_PSYNC_0
CPU FDI PSYNC<1>	AE5	FDI_PSYNC_1
CPU FDI INT	AG3	FDI_INT
CPU FDI LSYNC<0>	AC4	FDI_LSYNC_0
CPU FDI LSYNC<1>	AE4	FDI_LSYNC_1

PLACEMENT_NOTE=Place within 12.7MM of CPU
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPER=CPU_RCOMP

R1011
5%
1/16W
MF-LP
402

TP PE RX N<0>	P4	PE_RX_0*
TP PE RX N<1>	R1	PE_RX_1*
TP PE RX N<2>	T3	PE_RX_2*
TP PE RX N<3>	U1	PE_RX_3*
TP PE RX P<0>	P3	PE_RX_0
TP PE RX P<1>	R2	PE_RX_1
TP PE RX P<2>	T4	PE_RX_2
TP PE RX P<3>	U2	PE_RX_3

TP PE TX N<0>	P7	PE_TX_0*
TP PE TX N<1>	T8	PE_TX_1*
TP PE TX N<2>	R5	PE_TX_2*
TP PE TX N<3>	U6	PE_TX_3*

TP PE TX P<0>	P8	PE_TX_0
TP PE TX P<1>	T7	PE_TX_1
TP PE TX P<2>	R6	PE_TX_2
TP PE TX P<3>	U5	PE_TX_3

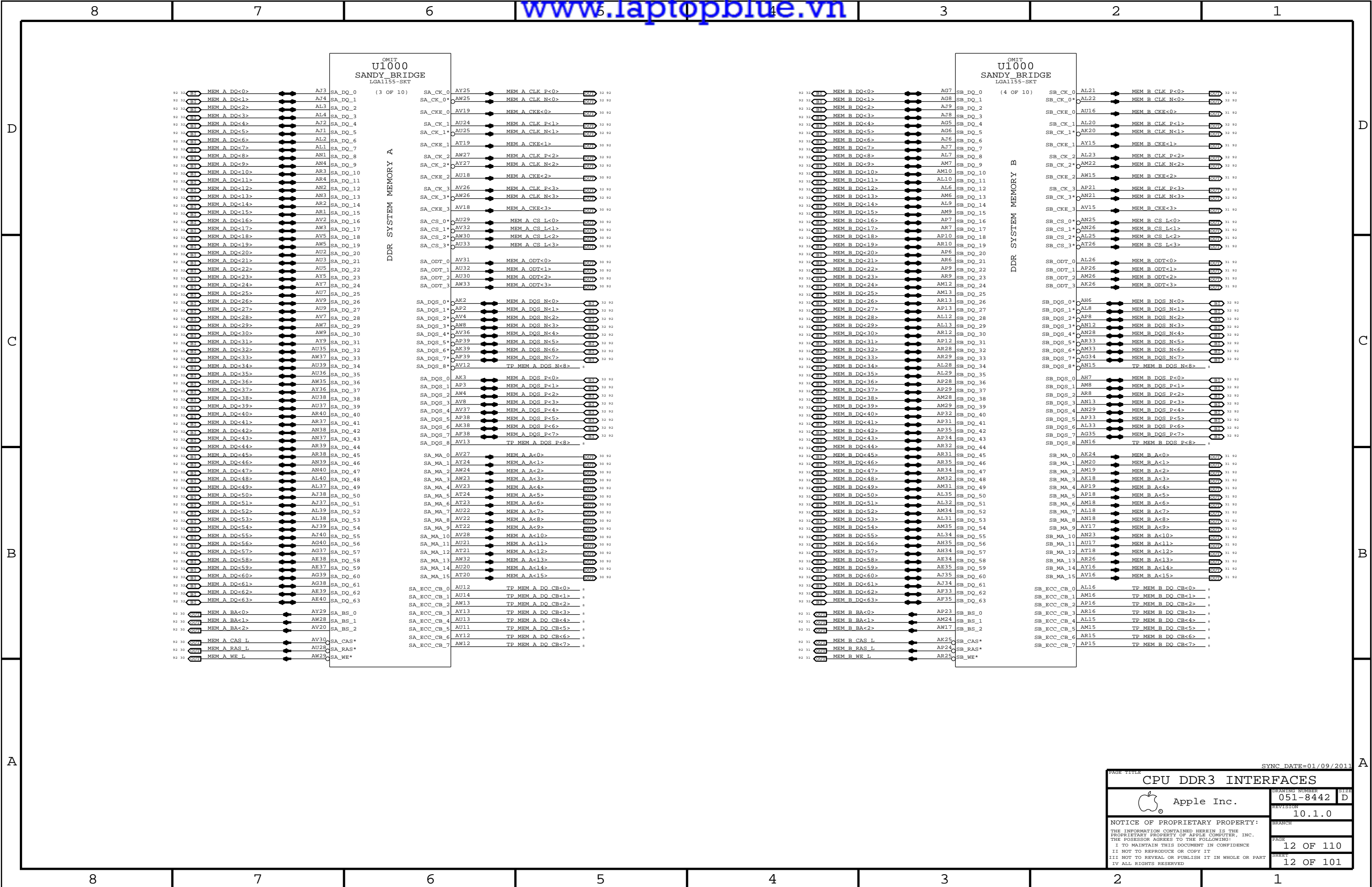
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PEG_ICOMPO	B5	
PEG_RCOMP1	C4	
PEG_RX_0*	B12	=PEG D2R N<0>
PEG_RX_1*	D11	=PEG D2R N<1>
PEG_RX_2*	C9	=PEG D2R N<2>
PEG_RX_3*	E9	=PEG D2R N<3>
PEG_RX_4*	B7	=PEG D2R N<4>
PEG_RX_5*	C5	=PEG D2R N<5>
PEG_RX_6*	A6	=PEG D2R N<6>
PEG_RX_7*	E1	=PEG D2R N<7>
PEG_RX_8*	F3	=PEG D2R N<8>
PEG_RX_9*	G1	=PEG D2R N<9>
PEG_RX_10*	H4	=PEG D2R N<10>
PEG_RX_11*	J2	=PEG D2R N<11>
PEG_RX_12*	K4	=PEG D2R N<12>
PEG_RX_13*	L2	=PEG D2R N<13>
PEG_RX_14*	M4	=PEG D2R N<14>
PEG_RX_15*	N2	=PEG D2R N<15>

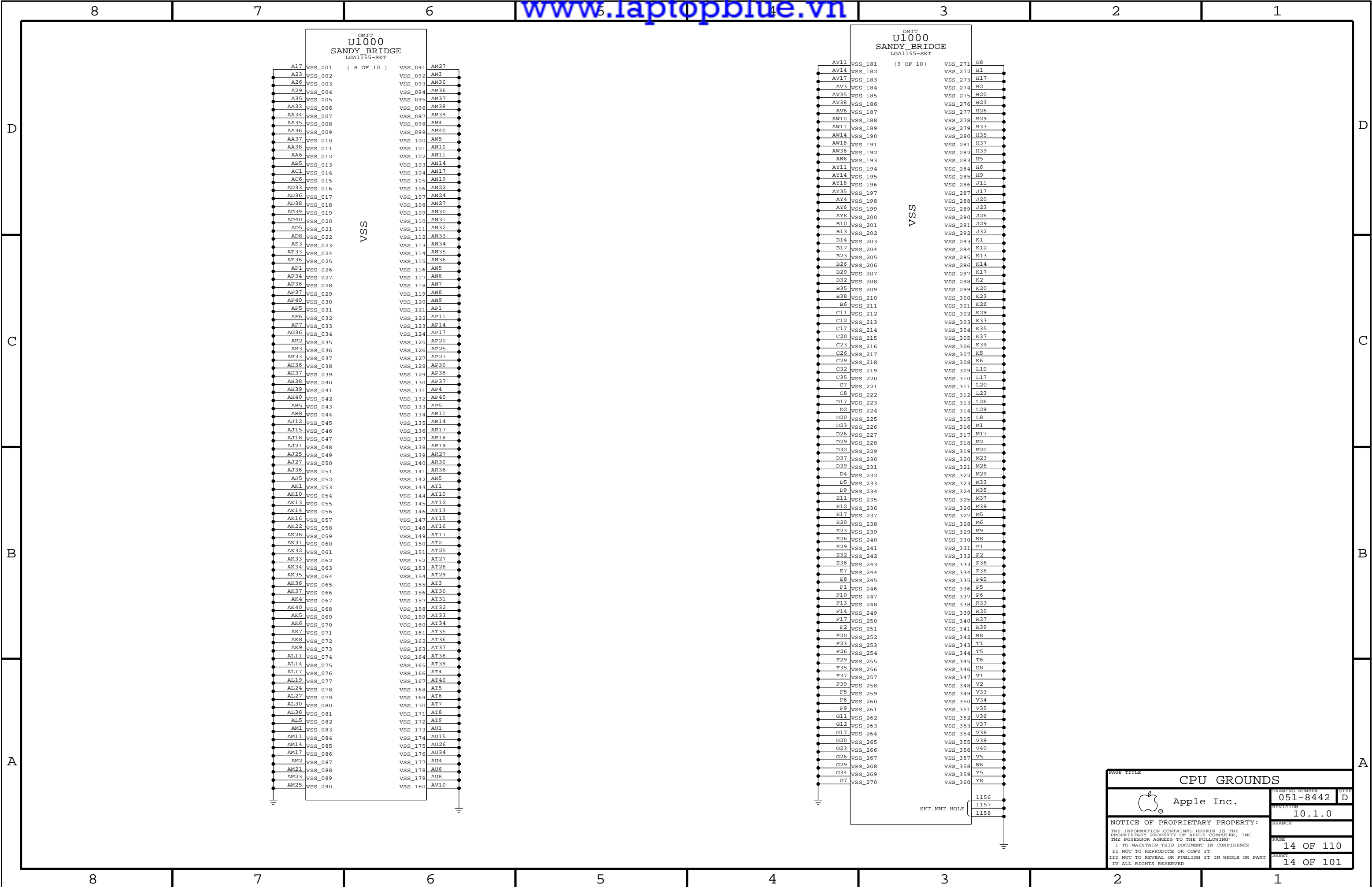
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PEG_RX_1	D12	=PEG D2R P<1>
PEG_RX_2	C10	=PEG D2R P<2>
PEG_RX_3	E10	=PEG D2R P<3>
PEG_RX_4	B8	=PEG D2R P<4>
PEG_RX_5	C6	=PEG D2R P<5>
PEG_RX_6	A5	=PEG D2R P<6>
PEG_RX_7	E2	=PEG D2R P<7>
PEG_RX_8	F4	=PEG D2R P<8>
PEG_RX_9	G2	=PEG D2R P<9>
PEG_RX_10	H3	=PEG D2R P<10>
PEG_RX_11	J1	=PEG D2R P<11>
PEG_RX_12	K3	=PEG D2R P<12>
PEG_RX_13	L1	=PEG D2R P<13>
PEG_RX_14	M3	=PEG D2R P<14>
PEG_RX_15	N1	=PEG D2R P<15>


PEG_TX_0*	C14	=PEG R2D C N<0>
PEG_TX_1*	E13	=PEG R2D C N<1>
PEG_TX_2*	G13	=PEG R2D C N<2>
PEG_TX_3*	F11	=PEG R2D C N<3>
PEG_TX_4*	J13	=PEG R2D C N<4>
PEG_TX_5*	D7	=PEG R2D C N<5>
PEG_TX_6*	C3	=PEG R2D C N<6>
PEG_TX_7*	E5	=PEG R2D C N<7>
PEG_TX_8*	F7	=PEG R2D C N<8>
PEG_TX_9*	G6	=PEG R2D C N<9>
PEG_TX_10*	K8	=PEG R2D C N<10>
PEG_TX_11*	J6	=PEG R2D C N<11>
PEG_TX_12*	M7	=PEG R2D C N<13>
PEG_TX_13*	L5	=PEG R2D C N<14>
PEG_TX_14*	N6	=PEG R2D C N<15>

PEG_TX_0	C13	=PEG R2D C P<0>
PEG_TX_1	E14	=PEG R2D C P<1>
PEG_TX_2	G14	=PEG R2D C P<2>
PEG_TX_3	F12	=PEG R2D C P<3>
PEG_TX_4	J14	=PEG R2D C P<4>
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PEG_TX_6	D3	=PEG R2D C P<6>
PEG_TX_7	E6	=PEG R2D C P<7>
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PEG_TX_9	G10	=PEG R2D C P<9>
PEG_TX_10	G5	=PEG R2D C P<10>
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PEG_TX_12	J5	=PEG R2D C P<12>
PEG_TX_13	M8	=PEG R2D C P<13>
PEG_TX_14	L6	=PEG R2D C P<14>
PEG_TX_15	N5	=PEG R2D C P<15>

A |





PAGE TITLE			
CPU GROUNDS			
 Apple Inc.	DRAWING NUMBER	051-8442	SIZE D
	REVISION	10.1.0	
	BRANCH		
	PAGE	14 OF 110	
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SHEET 14 OF 101			

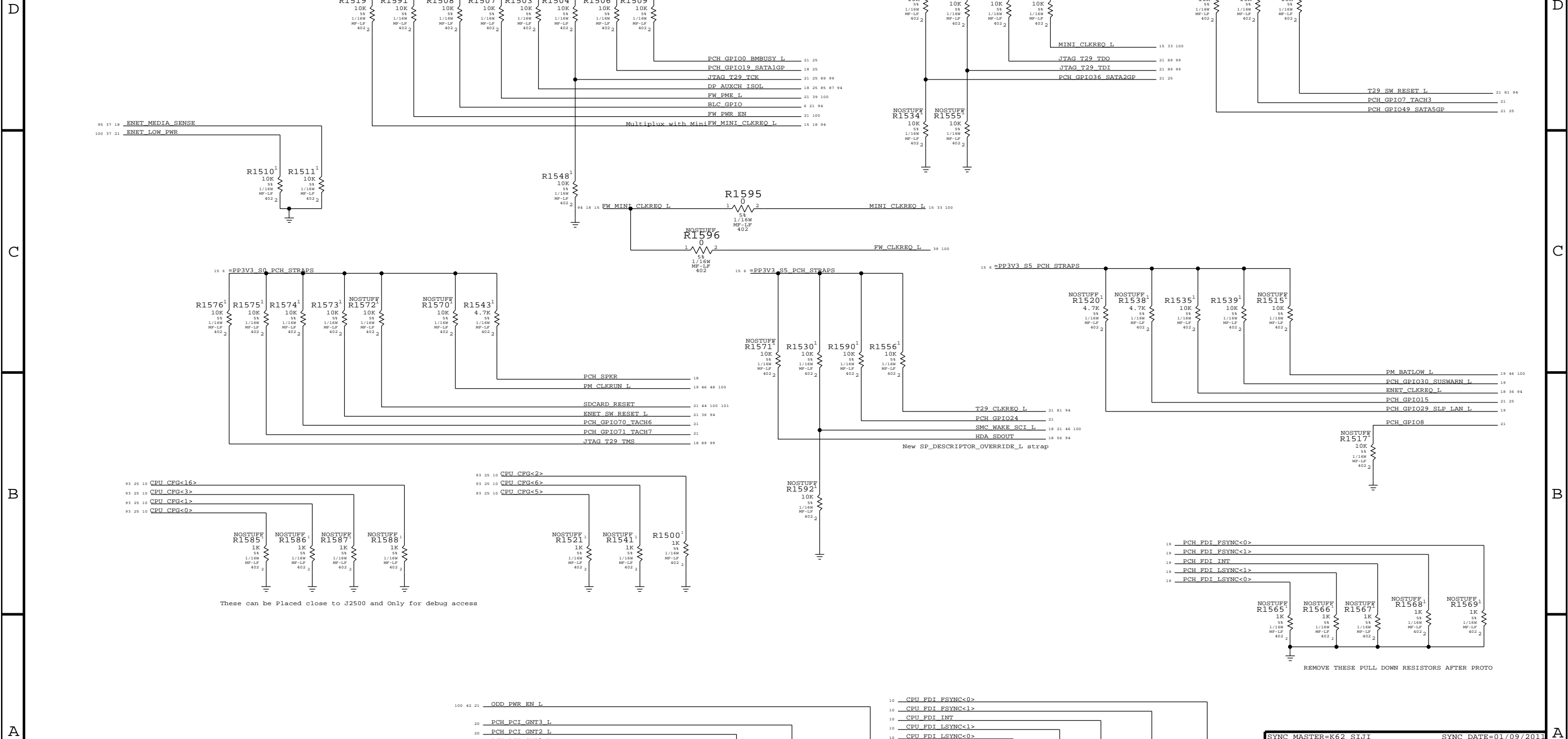


Diagram illustrating the pull-down resistors for various signals on the Apple K62 SiJ1 board. The diagram is divided into sections 1 through 8.

Section 1: Signals PCH_PCI_GNT2_L, PCH_PCI_GNT1_L, PCH_PCI_GNT0_L, and PCH_INIT3V3_L are connected to ground through resistors R1550, R1551, R1552, R1553, R1554, and R1512. The resistors are labeled with their values and tolerances: R1550 (1K, 5%, 1/16W, NP-LP, 402), R1551 (10K, 5%, 1/16W, NP-LP, 402), R1552 (10K, 5%, 1/16W, NP-LP, 402), R1553 (10K, 5%, 1/16W, NP-LP, 402), R1554 (10K, 5%, 1/16W, NP-LP, 402), and R1512 (10K, 5%, 1/16W, NP-LP, 402).

Section 2: Signals CPU_FDI_L<SYNC<1> and CPU_FDI_L<SYNC<0> are connected to ground through resistors R1560, R1561, R1562, R1563, and R1564. The resistors are labeled with their values and tolerances: R1560 (1K, 5%, 1/16W, NP-LP, 402), R1561 (1K, 5%, 1/16W, NP-LP, 402), R1562 (1K, 5%, 1/16W, NP-LP, 402), R1563 (1K, 5%, 1/16W, NP-LP, 402), and R1564 (1K, 5%, 1/16W, NP-LP, 402).

Section 3: A table containing drawing information and a notice of proprietary property.

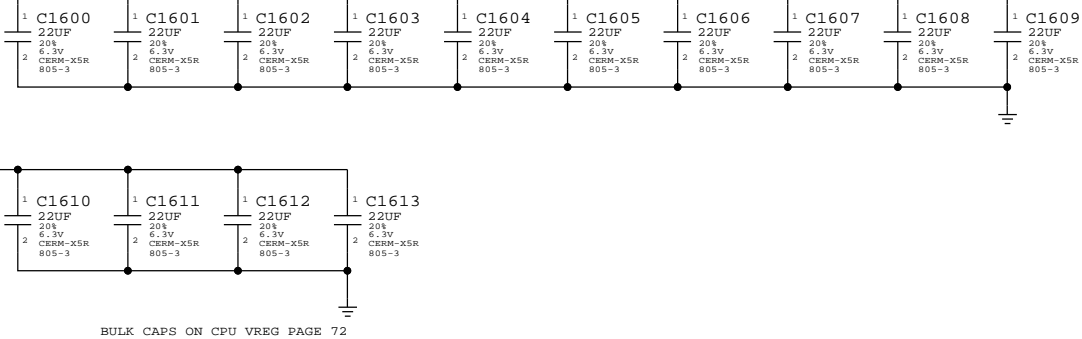
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SYNCH MASTER=K62 SiJ1	SYNCH DATE=01/09/2011
PAGE TITLE	
STRAPS,PULL UPS,PULL DOWNS FOR PCH AND CPU	
Apple Inc.	DRAWING NUMBER: 051-8442
REVISION: 10.1.0	SIZE: D
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CPU VCORE DECOUPLING

14x 22UF,0805 INTEL RECOMMENDATION 18X 22UF 0805 (14 Inside cavity and 4 North of processor)

PLACEMENT_NOTE (C1600-C1613):

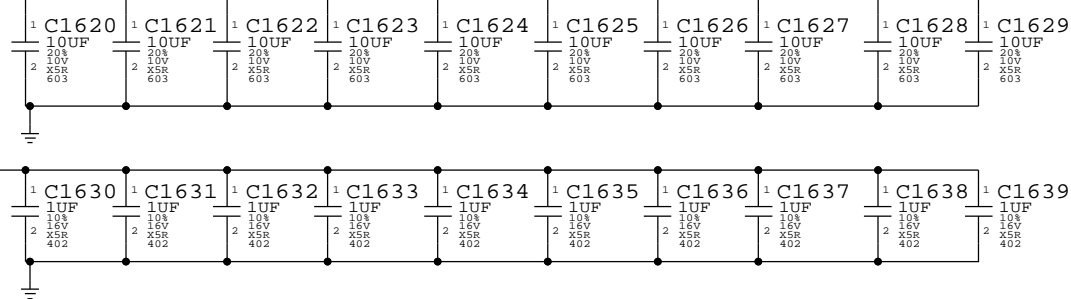
Place inside socket cavity



=PPVCORE_S0_CPU

10x 10UF and 10x 1UF CAPACITORS

Place inside socket cavity

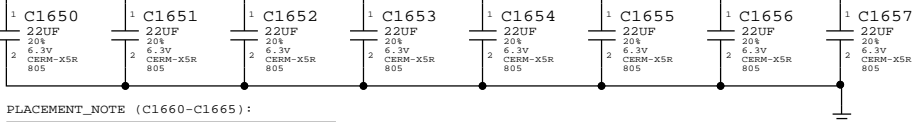


CPU VCCIO DECOUPLING

8X 22UF 0805, 6X 10UF 0805 INTEL RECOMMENDATION 9X22UF 0805,16X 0805 placeholders

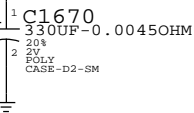
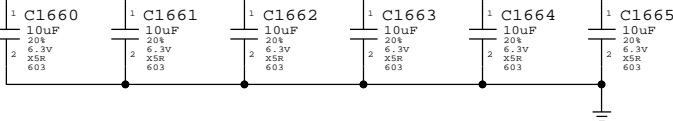
PLACEMENT_NOTE (C1650-C1657):

Place under socket cavity on secondary side.



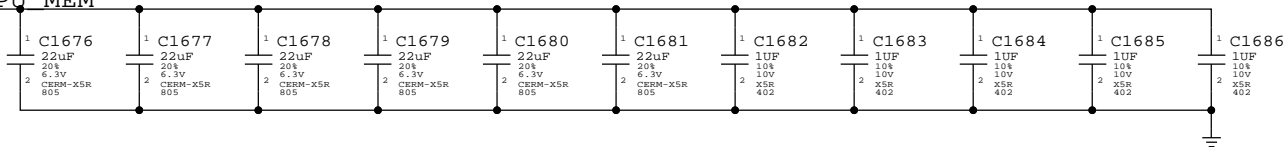
PLACEMENT_NOTE (C1660-C1665):

Place at edge of socket.



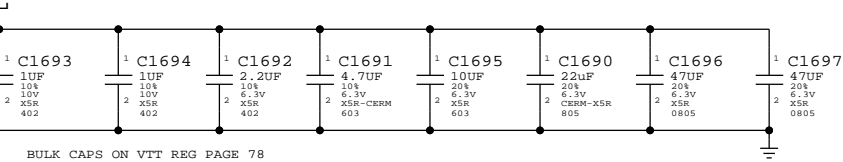
Memory (CPU VCCDDR) DECOUPLING

6x 22uF 0805, 5x 1uF 0402. INTEL RECOMMENDATION 9X 22uF 0805




PLL (CPU VCCSFR) DECOUPLING

2x 47uF, 1x 22uF 0805, 1x 10uF 0603, 1x 4.7uF 0603, 1x 2.2uF 0402, 2x 1uF 0402. INTEL RECOMMENDATION 10x 10uF 0805



Note: VCCSA decoupling is on regulator page

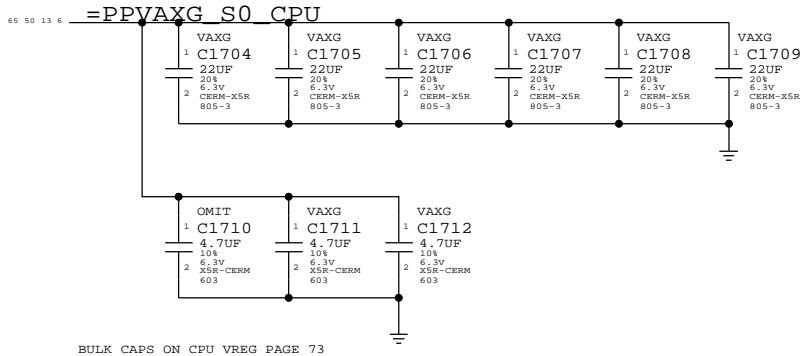
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CPU NON-GFX DECOUPLING				DRAWING NUMBER	
 Apple Inc.				051-8442	
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VAXG DECOUPLING

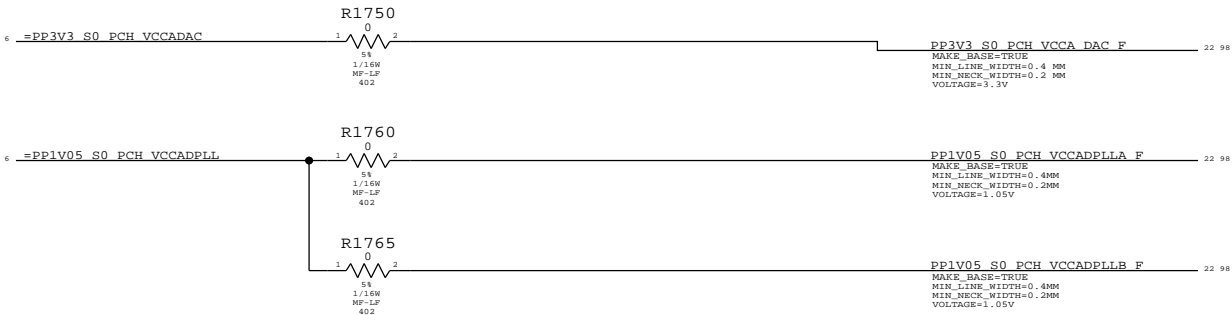
INTEL RECOMMENDATION 6X22UF 0805,3X 4.7UF

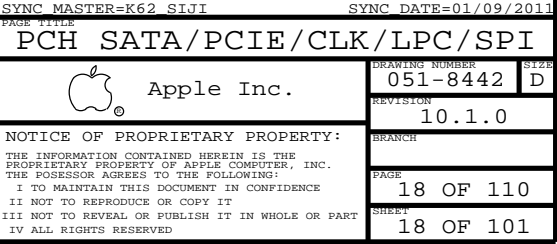
PLACEMENT_NOTE (C1704-C1709):

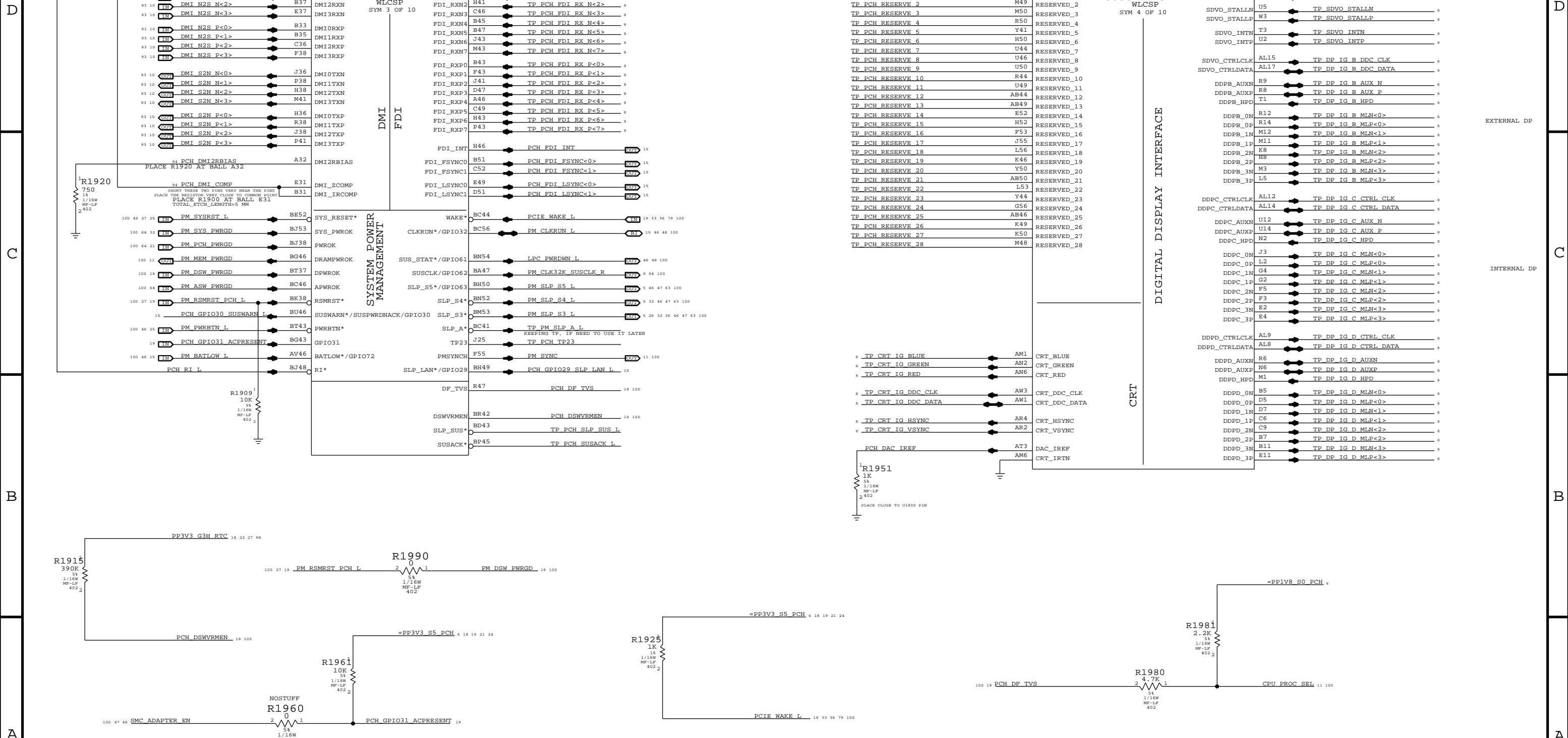
Place inside socket cavity

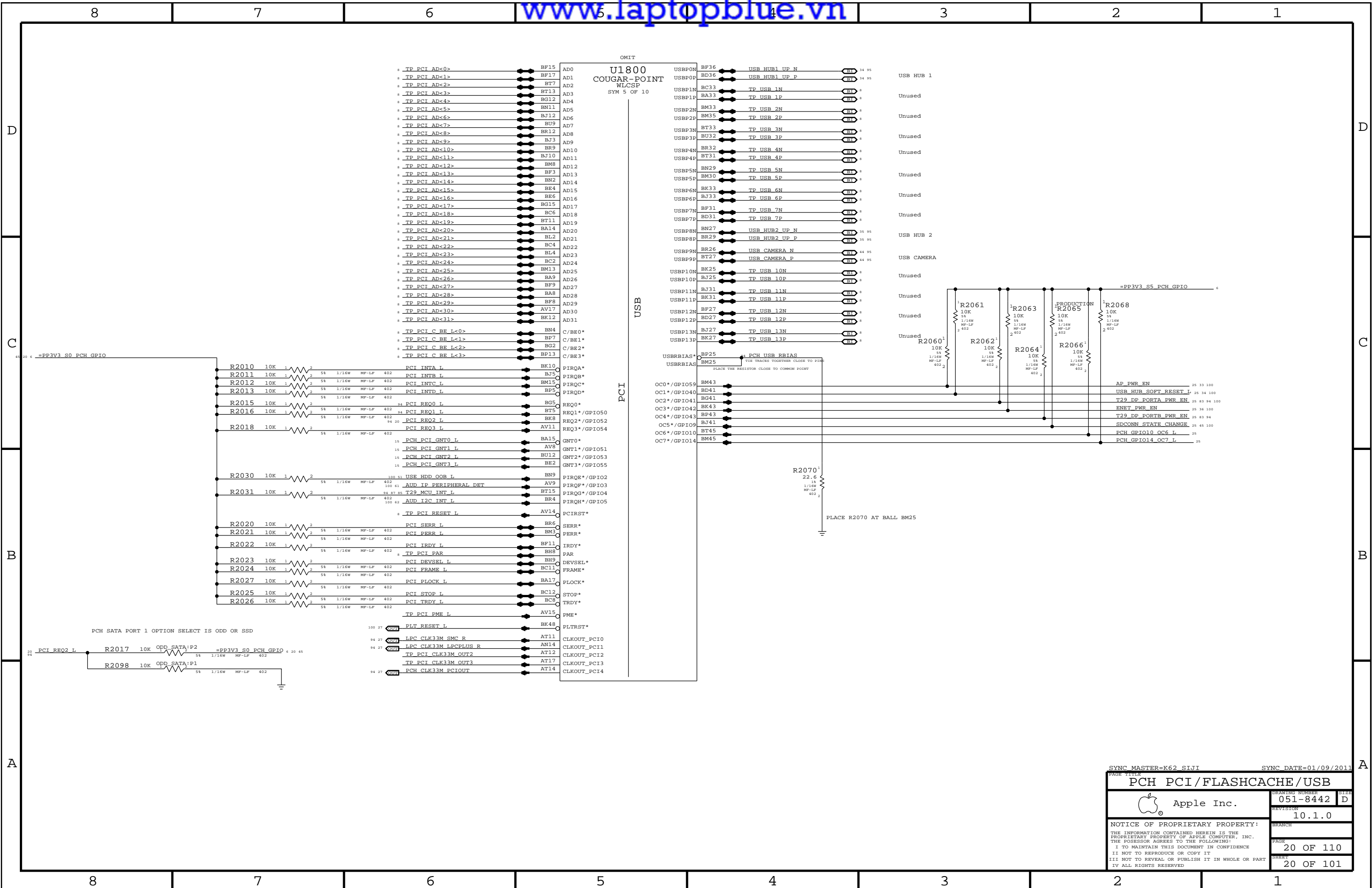


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
138S0586	1	CAP,4.7UF,10%,6.3V,0603	C1710	VAXG
113S0022	1	RES,0 OHM,5%,0603	C1710	NO_VAXG




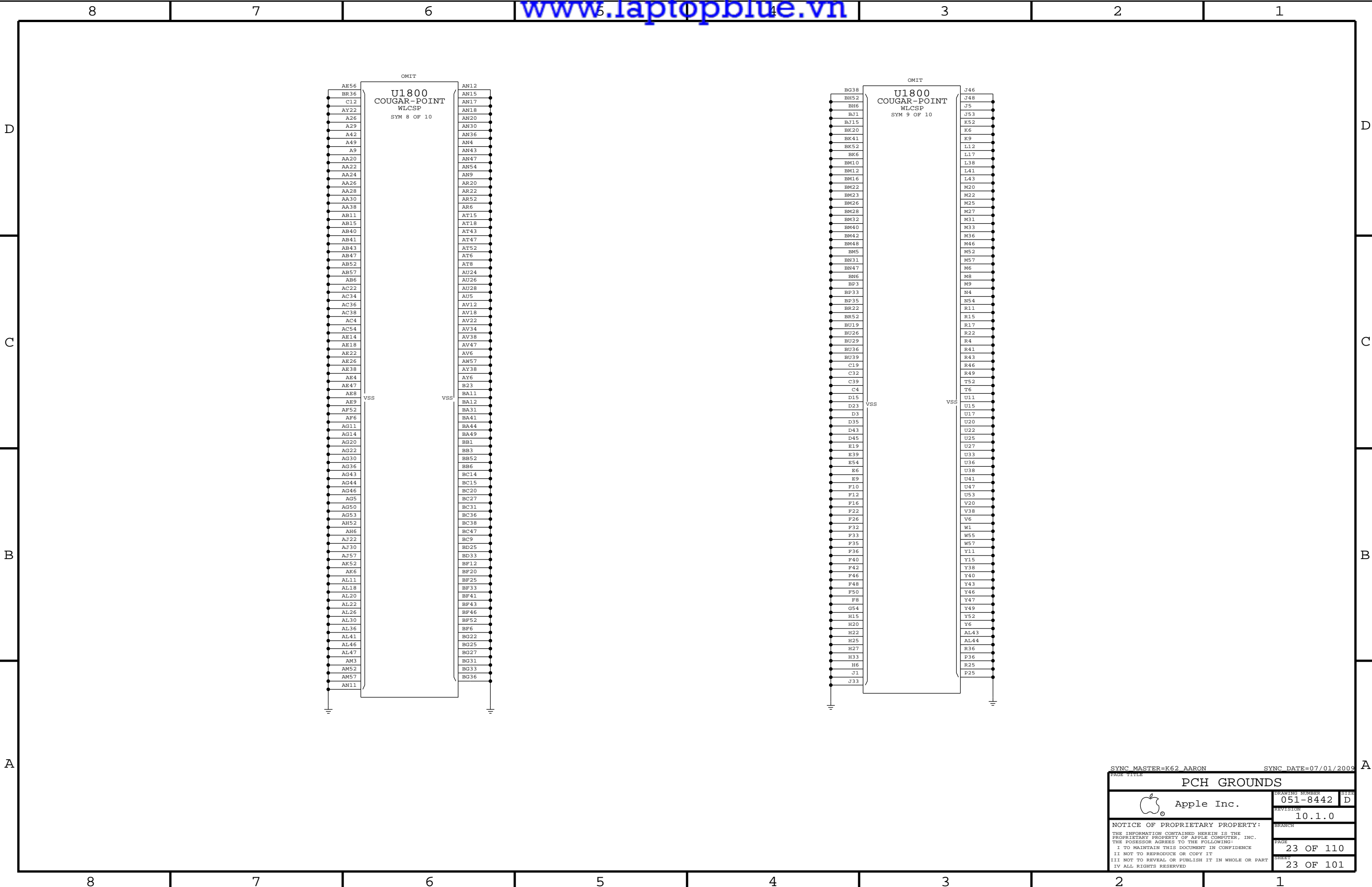








SYNC MASTER=K62 SIJI		SYNC DATE=01/09/2011	
PAGE TITLE			
PCH MISC			
 Apple Inc.	DRAWING NUMBER		SHEET
	051-8442		D
REVISION		10.1.0	
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D

C

B

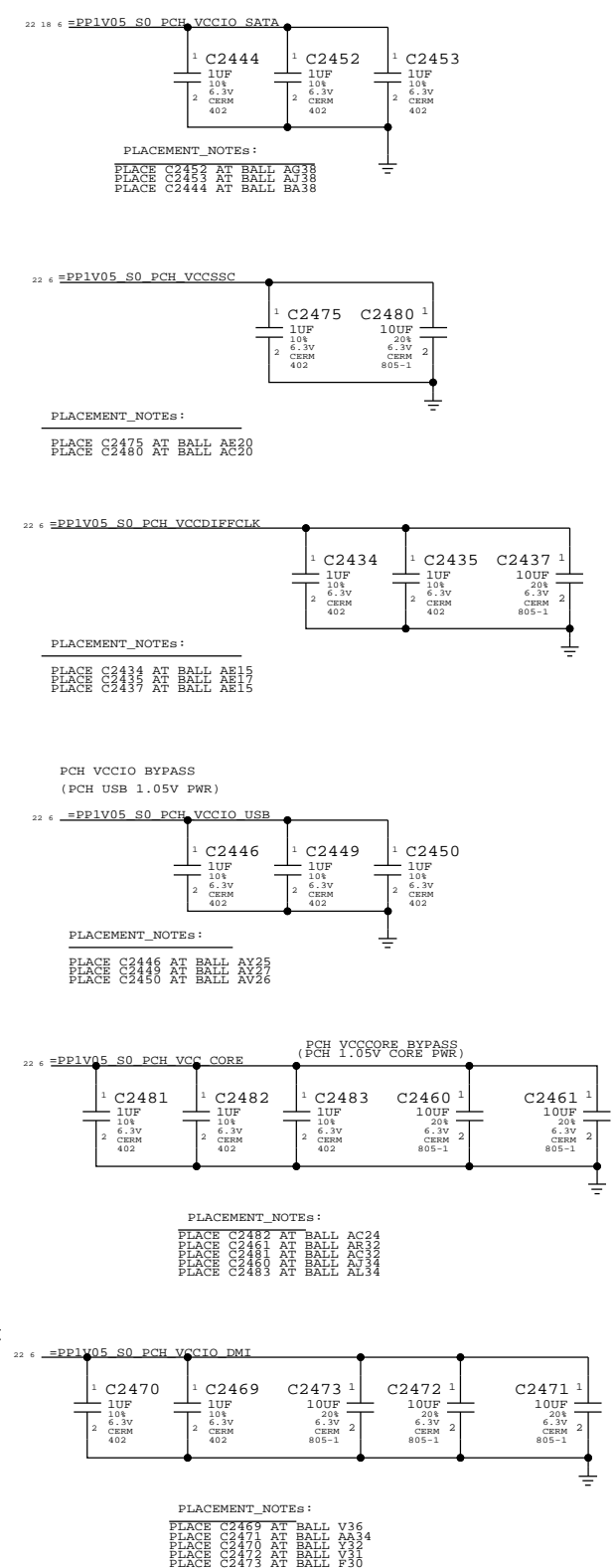
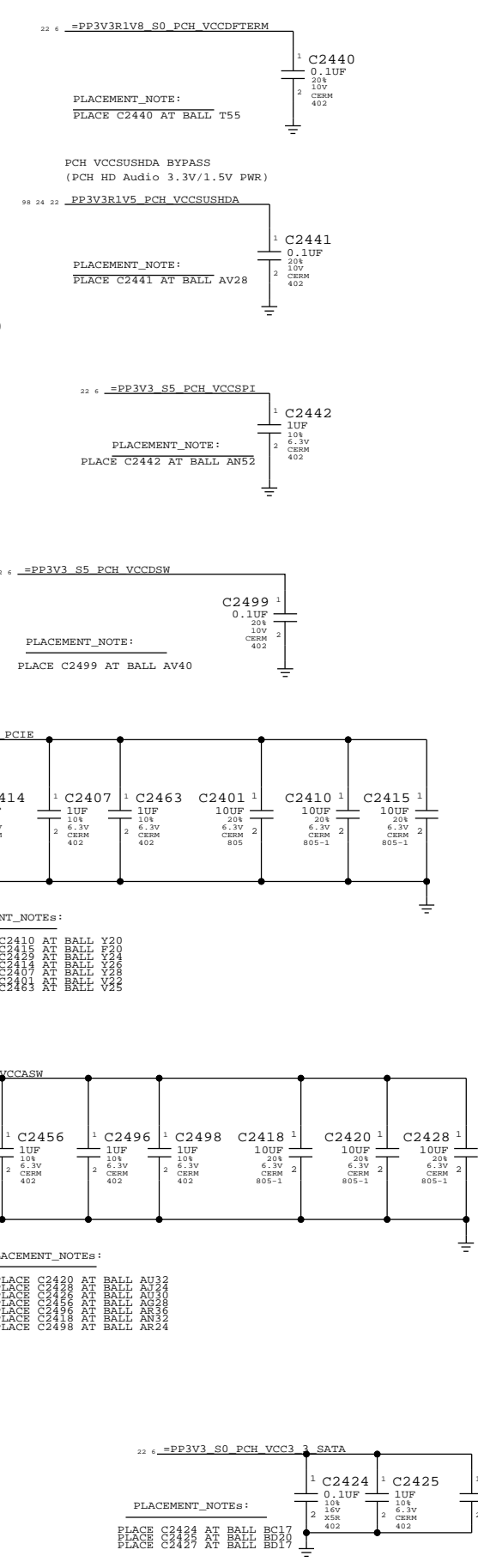
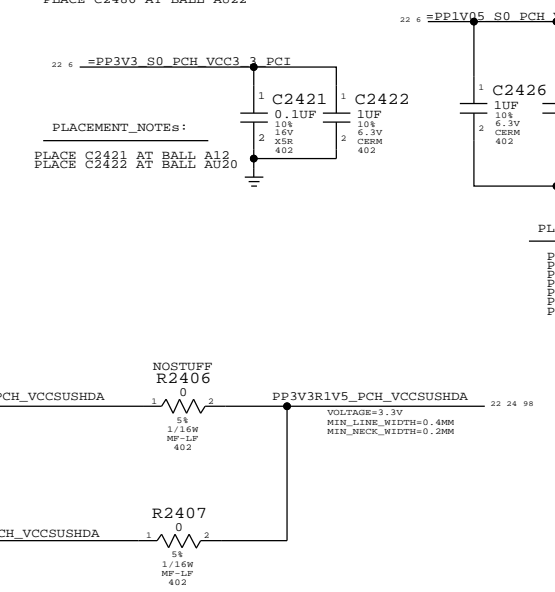
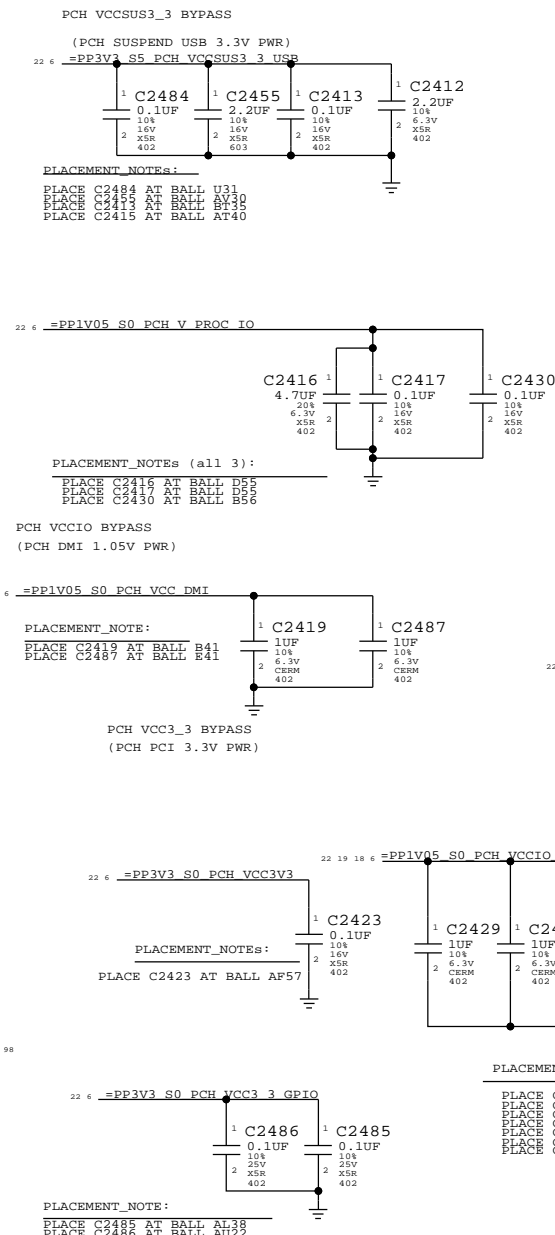
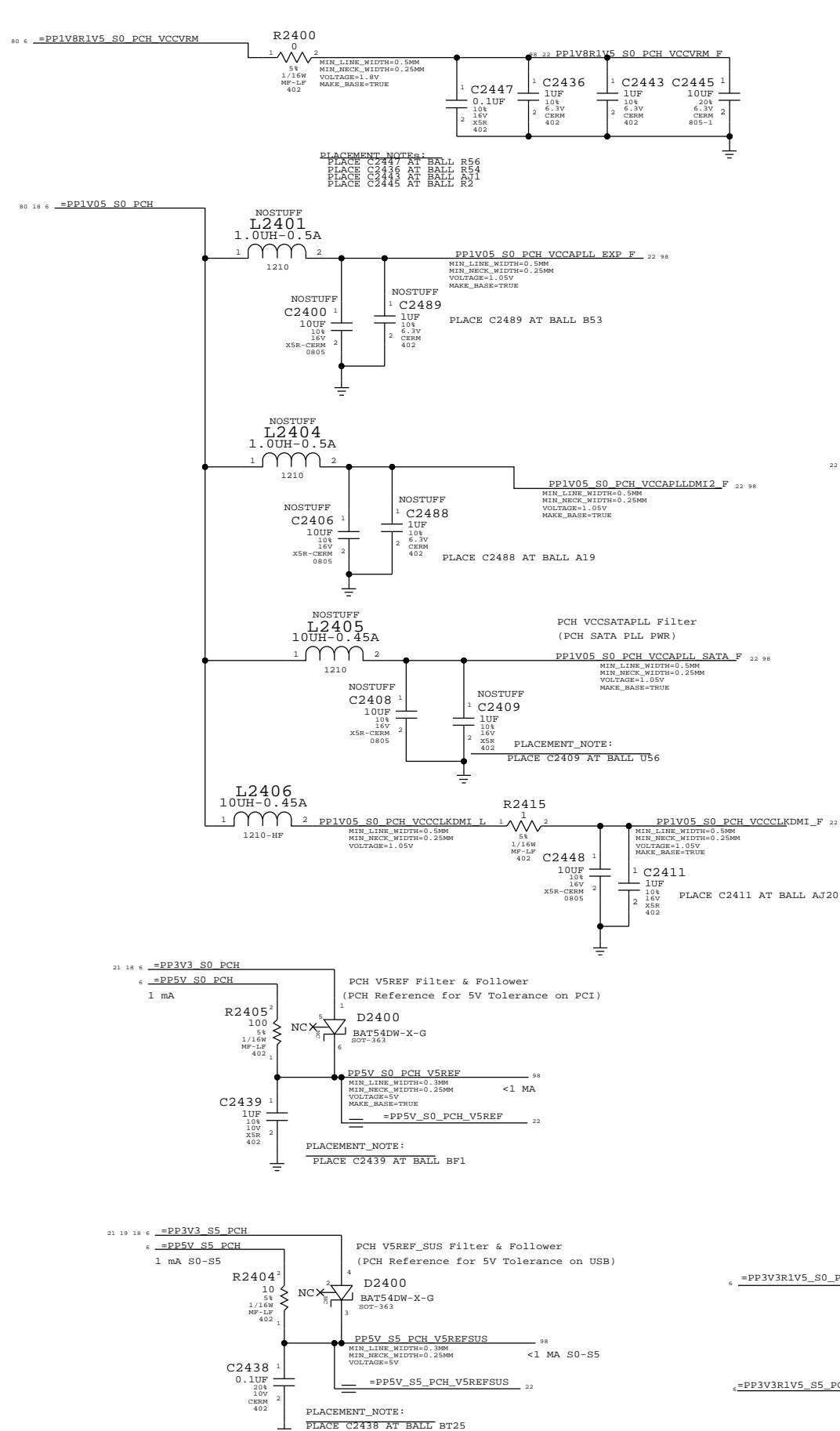
A

D

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B

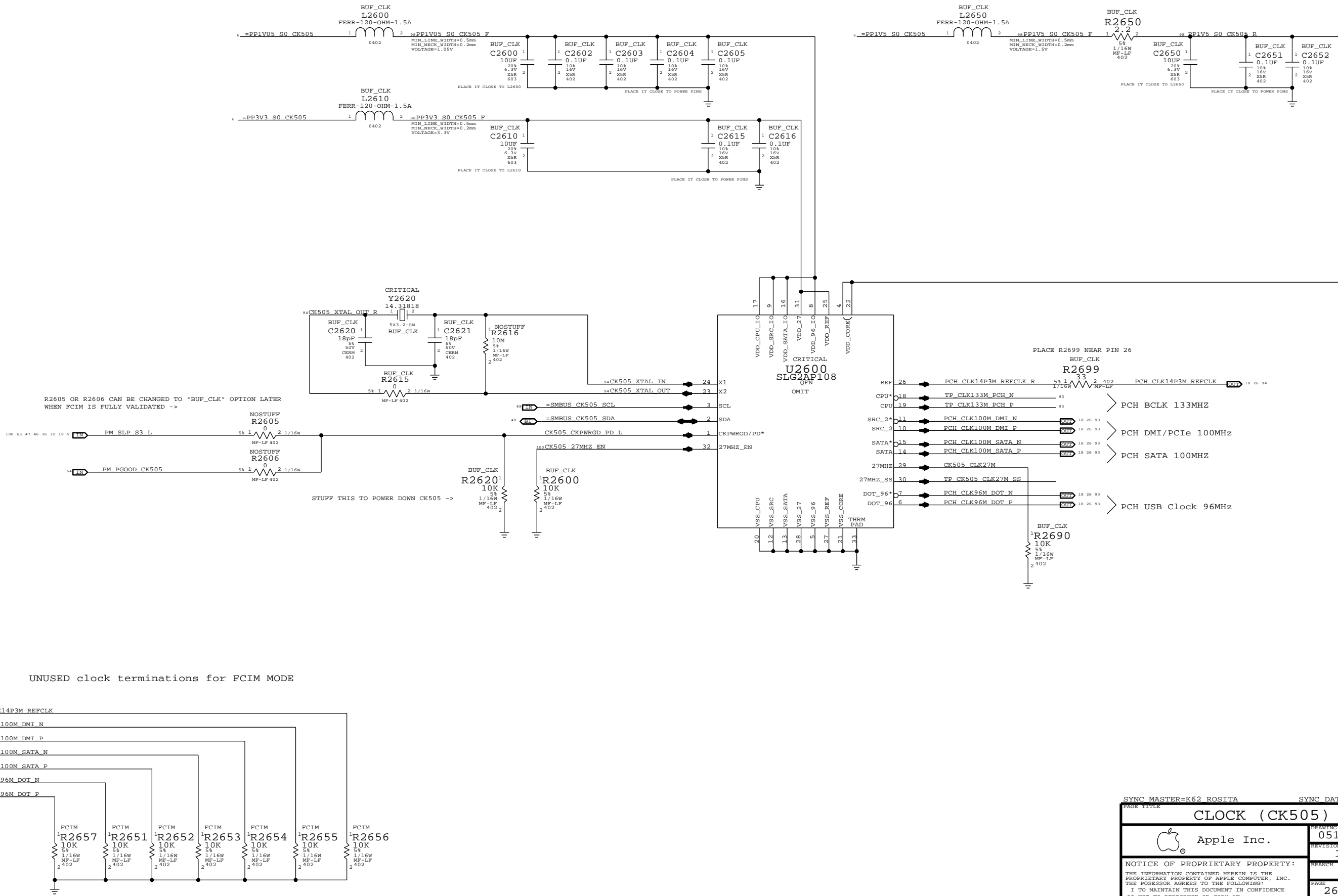
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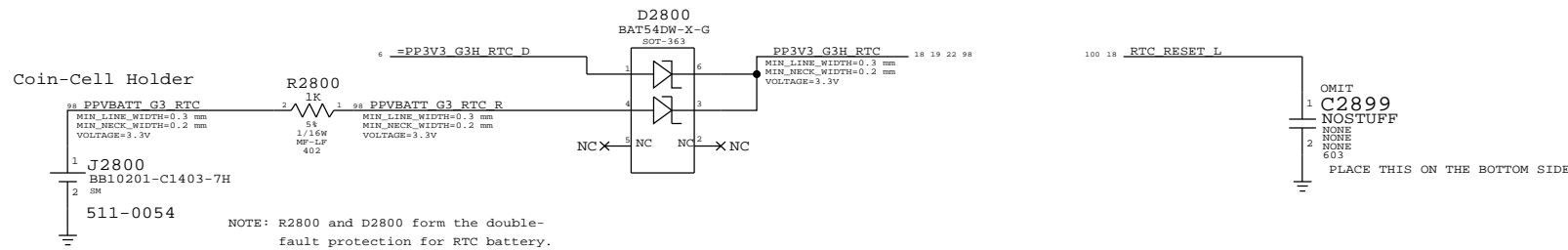
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PCH DECOUPLING					
Apple Inc.		DRAWING NUMBER		SIZE	
		051-8442		D	
		REVISION		10.1.0	
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				24 OF 101	

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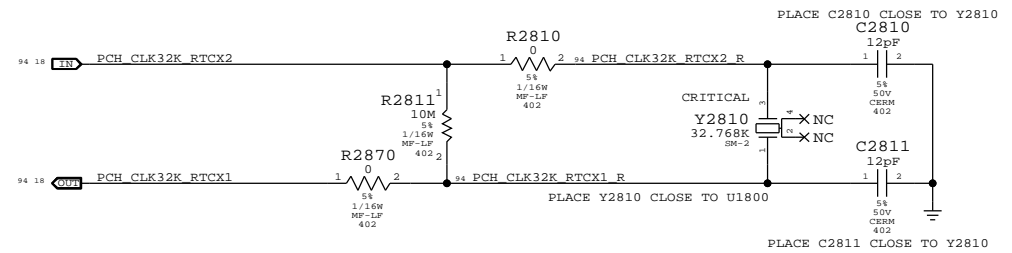




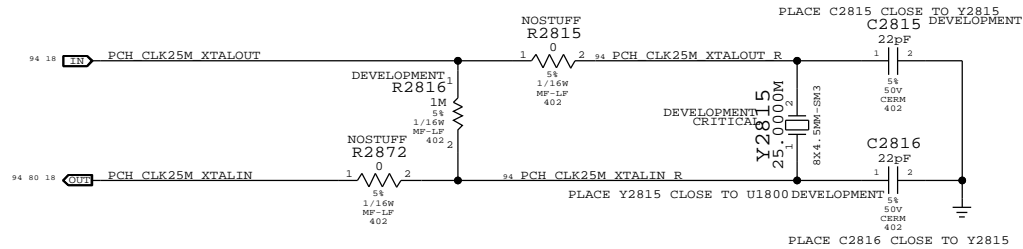
RTC Power Sources



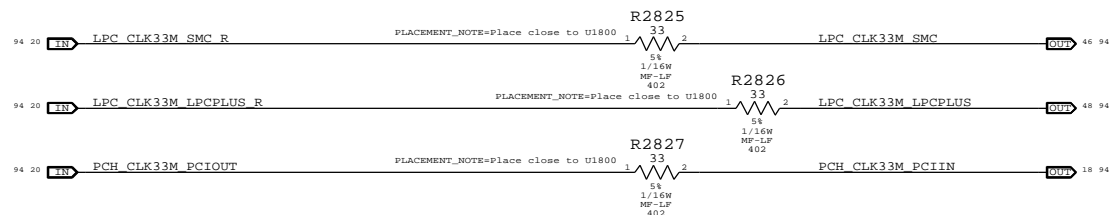
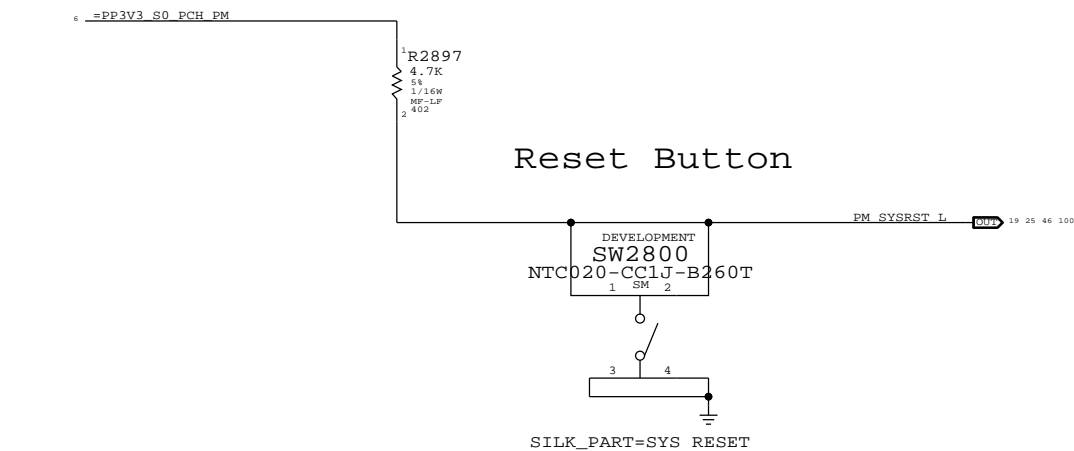
PCH RTC Crystal



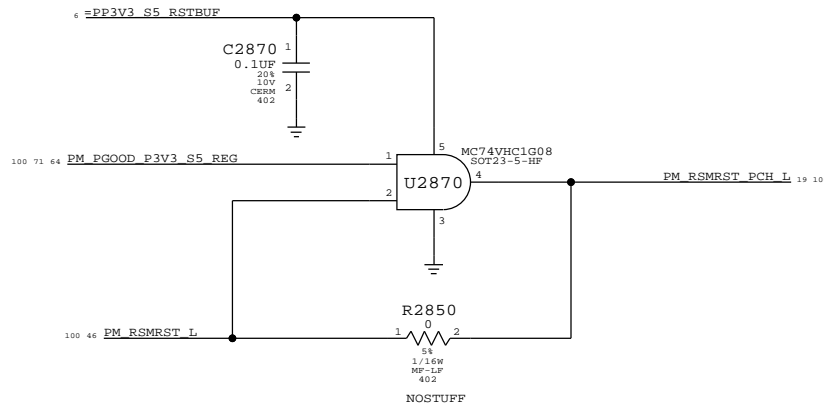
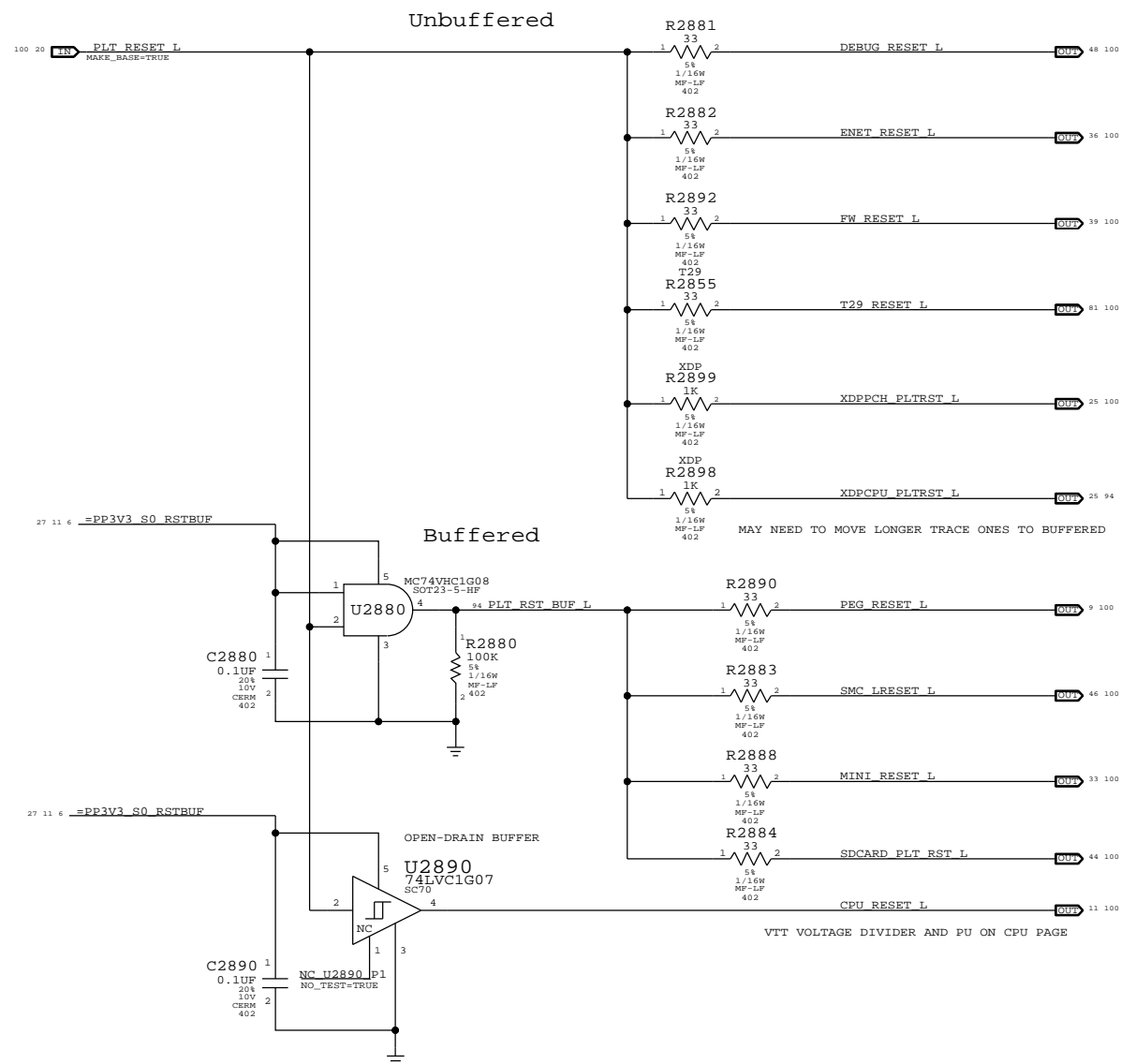
PCH 25MHZ CRYSTAL




Reset Button

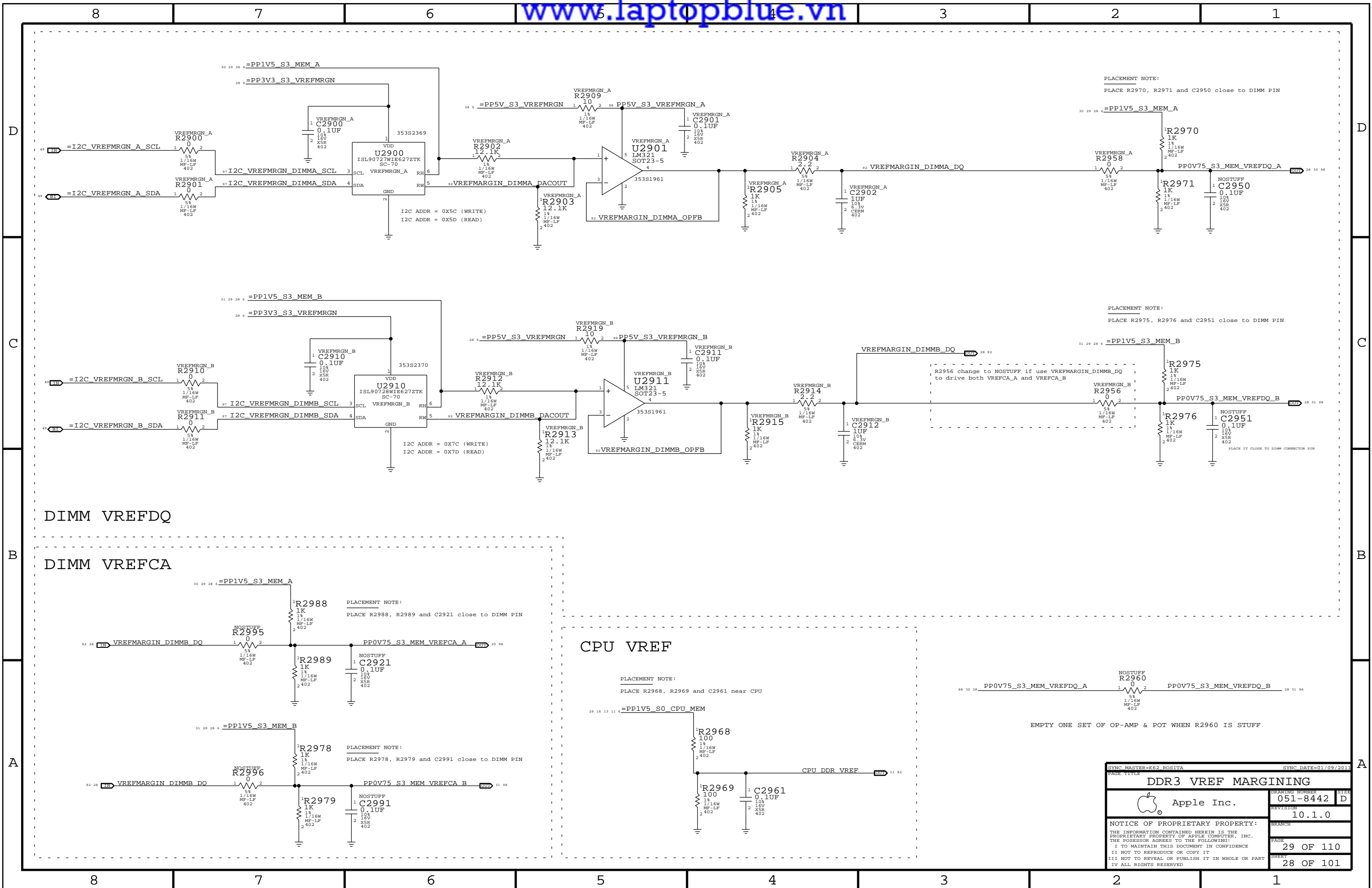


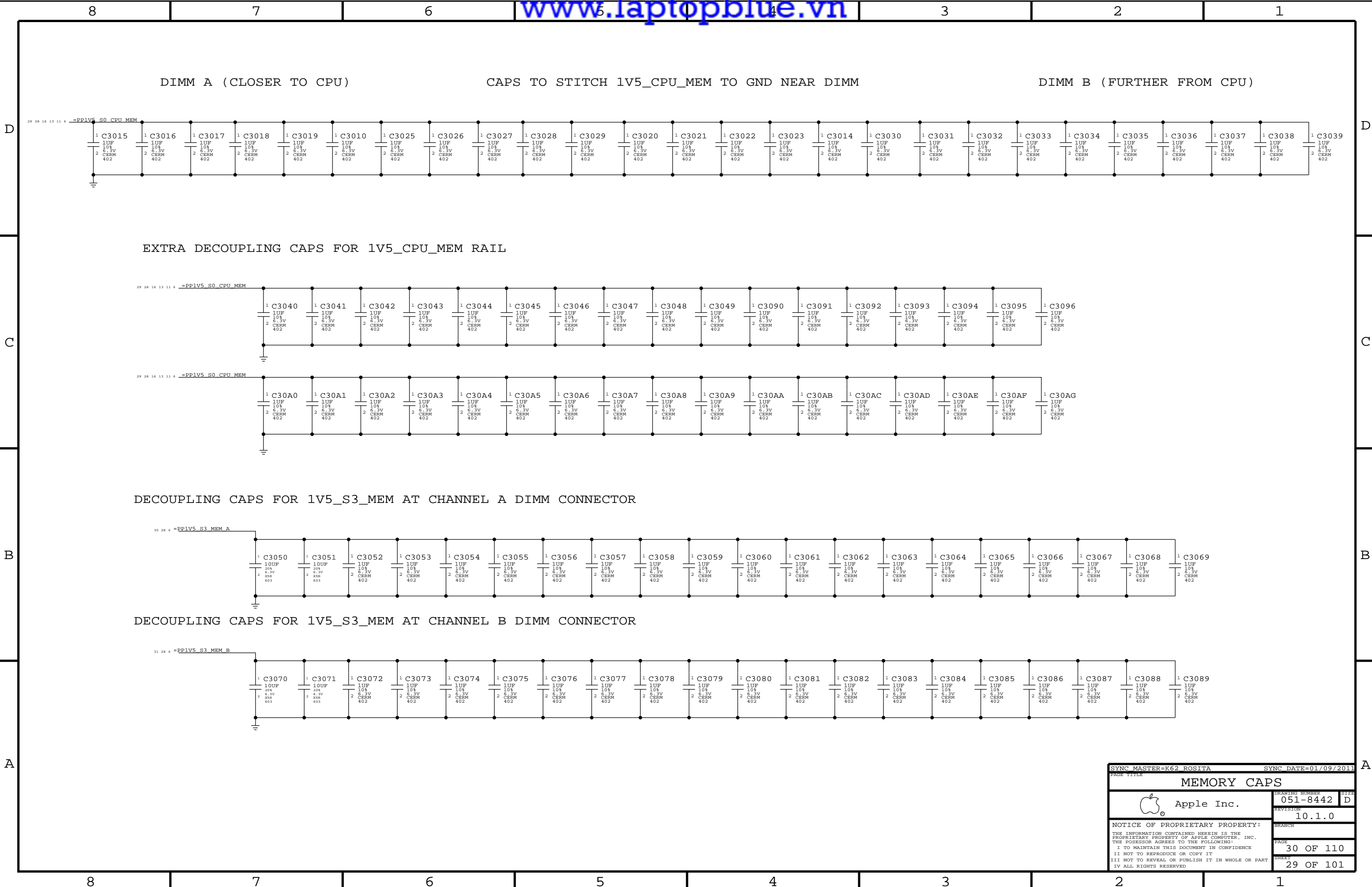
Platform Reset Connections




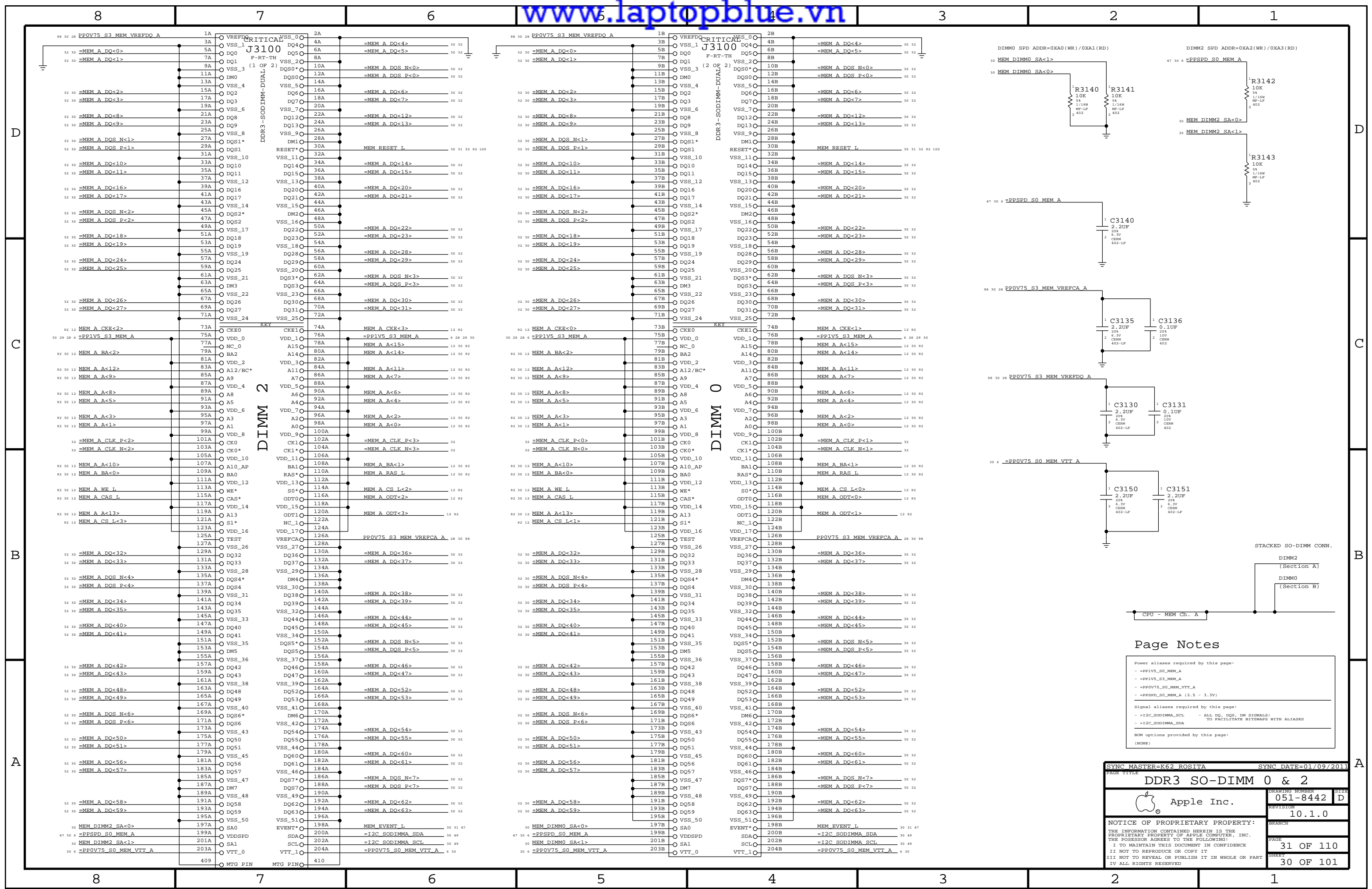
SMC PROVIDES RSMRST_L DE-ASSERTION DELAY UPON ENTRY TO S5
SMC PROVIDES RSMRST_L ASSERTION TIMING REQUIREMENTS UPON EXPECTED EXIT FROM S5
SMC MAY FORCE A RSMRST_L ASSERTION WITHOUT AN S5 POWER TRANSITION IN SOME ERROR CASES
PGOOD PROVIDES RSMRST_L ASSERTION TIMING REQUIREMENTS UPON AN UN-EXPECTED EXIT FROM S5 (POWER LOSS)

SYNC MASTER=K62 SIJI		SYNC DATE=01/09/2011	
PAGE TITLE			
CHIPSET SUPPORT			
		DRAWING NUMBER	051-8442
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MEMORY CAPS			
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SNB? CANNOT CONTROL THIS SIGNAL DIRECTLY SINCE IT MUST BE HIGH IN SLEEP AND CPU MEM RAILS ARE NOT POWERED IN SLEEP.



92	12	<u>MEM A CLK P<0></u>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM A CLK P<0>	30
92	12	<u>MEM A CLK N<0></u>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM A CLK N<0>	30
92	12	<u>MEM A CLK P<1></u>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM A CLK P<1>	30
92	12	<u>MEM A CLK N<1></u>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM A CLK N<1>	30
92	12	<u>MEM A CLK P<2></u>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM A CLK P<2>	30
92	12	<u>MEM A CLK N<2></u>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM A CLK N<2>	30
92	12	<u>MEM A CLK P<3></u>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM A CLK P<3>	30
92	12	<u>MEM A CLK N<3></u>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM A CLK N<3>	30
<hr/>						
92	12	<u>MEM B CLK P<0></u>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM B CLK P<0>	31
92	12	<u>MEM B CLK N<0></u>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM B CLK N<0>	31
92	12	<u>MEM B CLK P<1></u>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM B CLK P<1>	31
92	12	<u>MEM B CLK N<1></u>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM B CLK N<1>	31
92	12	<u>MEM B CLK P<2></u>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM B CLK P<2>	31
92	12	<u>MEM B CLK N<2></u>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM B CLK N<2>	31
92	12	<u>MEM B CLK P<3></u>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM B CLK P<3>	31
92	12	<u>MEM B CLK N<3></u>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM B CLK N<3>	31

S	R	CLK	D	Q	QB
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	POSEDGE	L	L	H
H	H	POSEDGE	H	H	L

MASTER=K62 ROSITA SYNC DATE=01/09/2011

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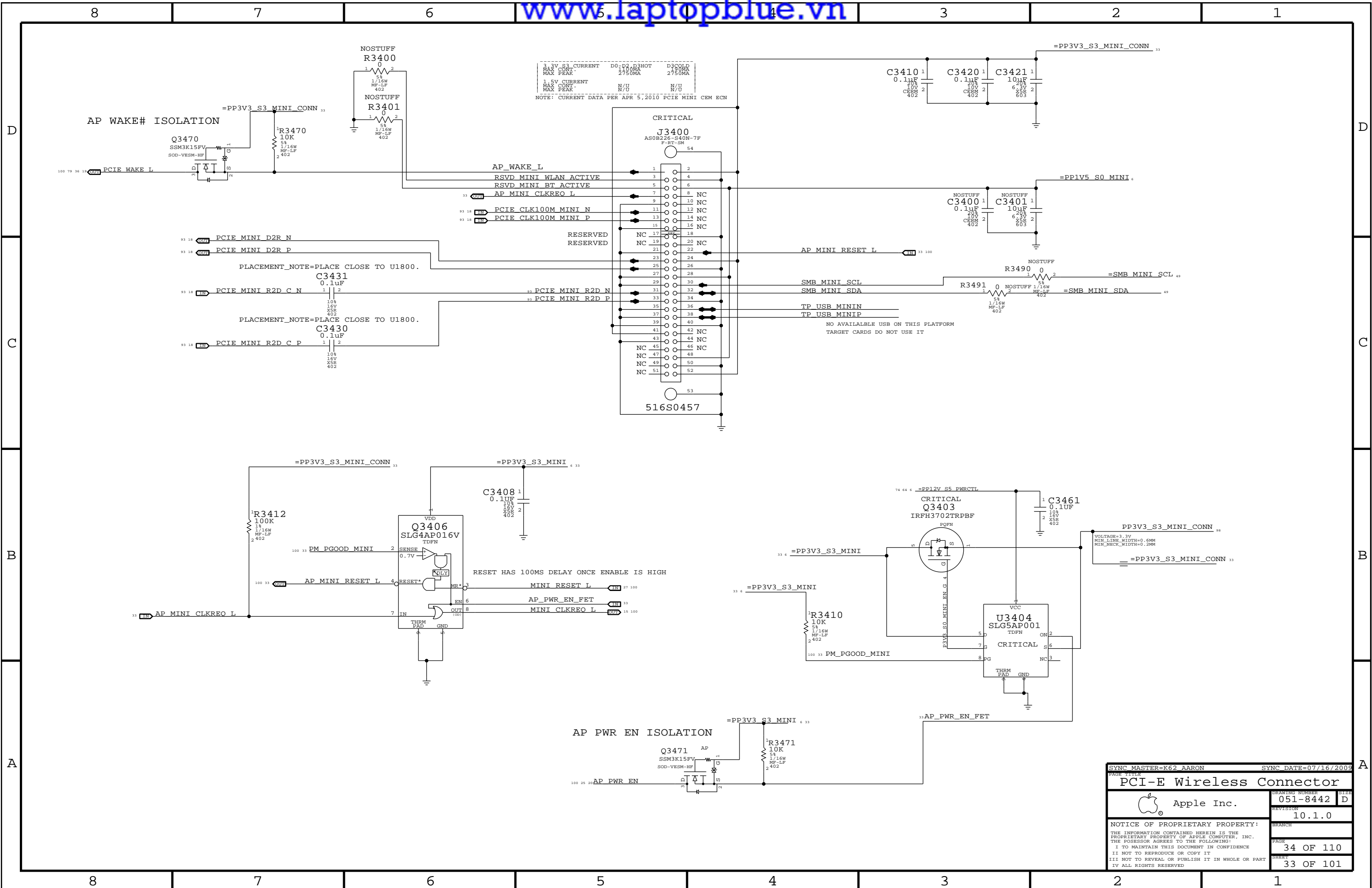
DRAWING NUMBER	SYMBOL
051-8442	D

REVISION
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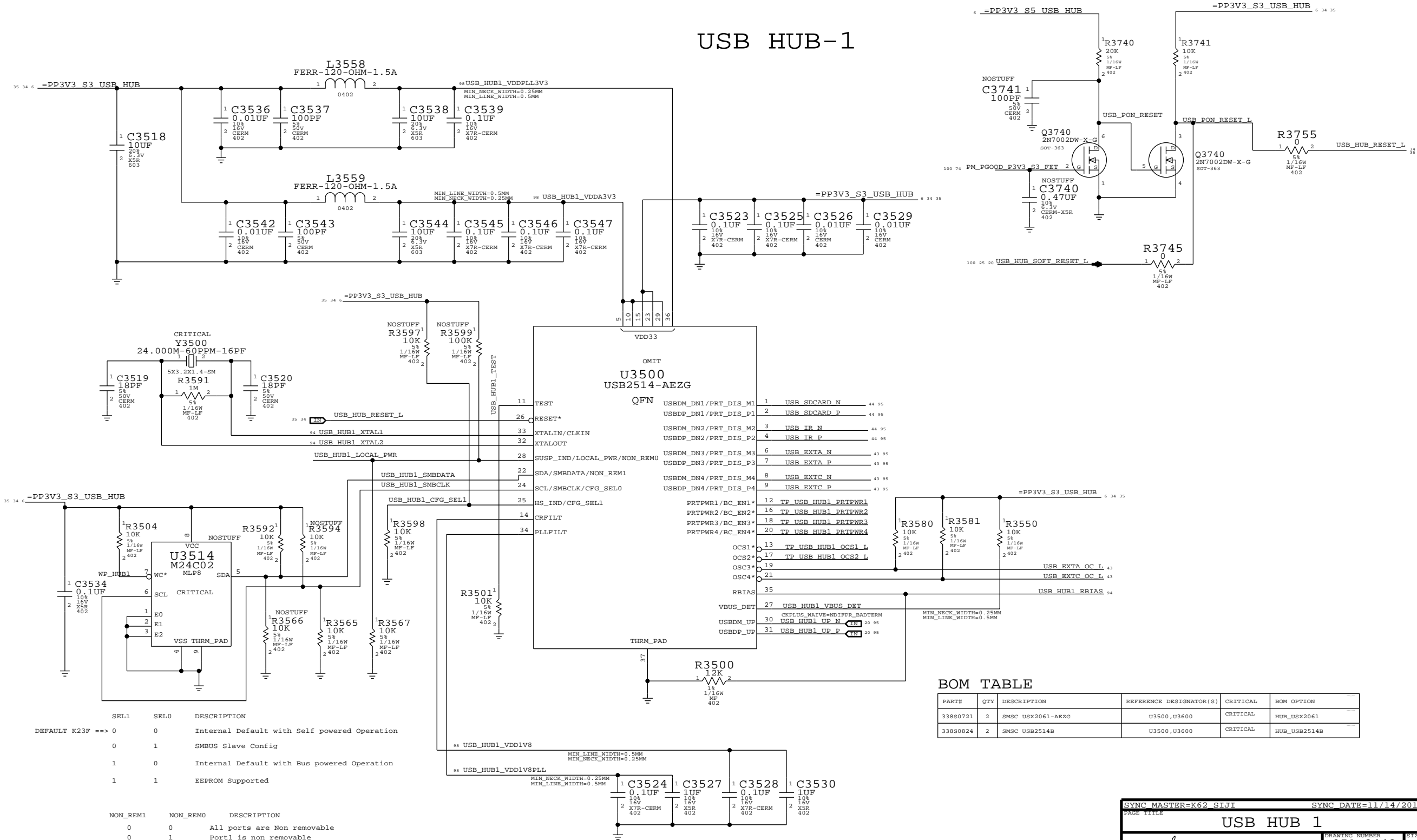
BRANCH

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SHEET
32 OF 101



USB HUB-1



SEL1	SEL0	DESCRIPTION
DEFAULT K23F ==> 0	0	Internal Default with Self powered Operation
0	1	SMBUS Slave Config
1	0	Internal Default with Bus powered Operation
1	1	EEPROM Supported

NON_REM1	NON_REMO	DESCRIPTION
0	0	All ports are Non removable
0	1	Port1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port1,2 and 3 are non Removable

SYNC MASTER=K62_S1J1

SYNC DATE=11/14/2010

USB HUB 1

Apple Inc.

DRAWING NUMBER

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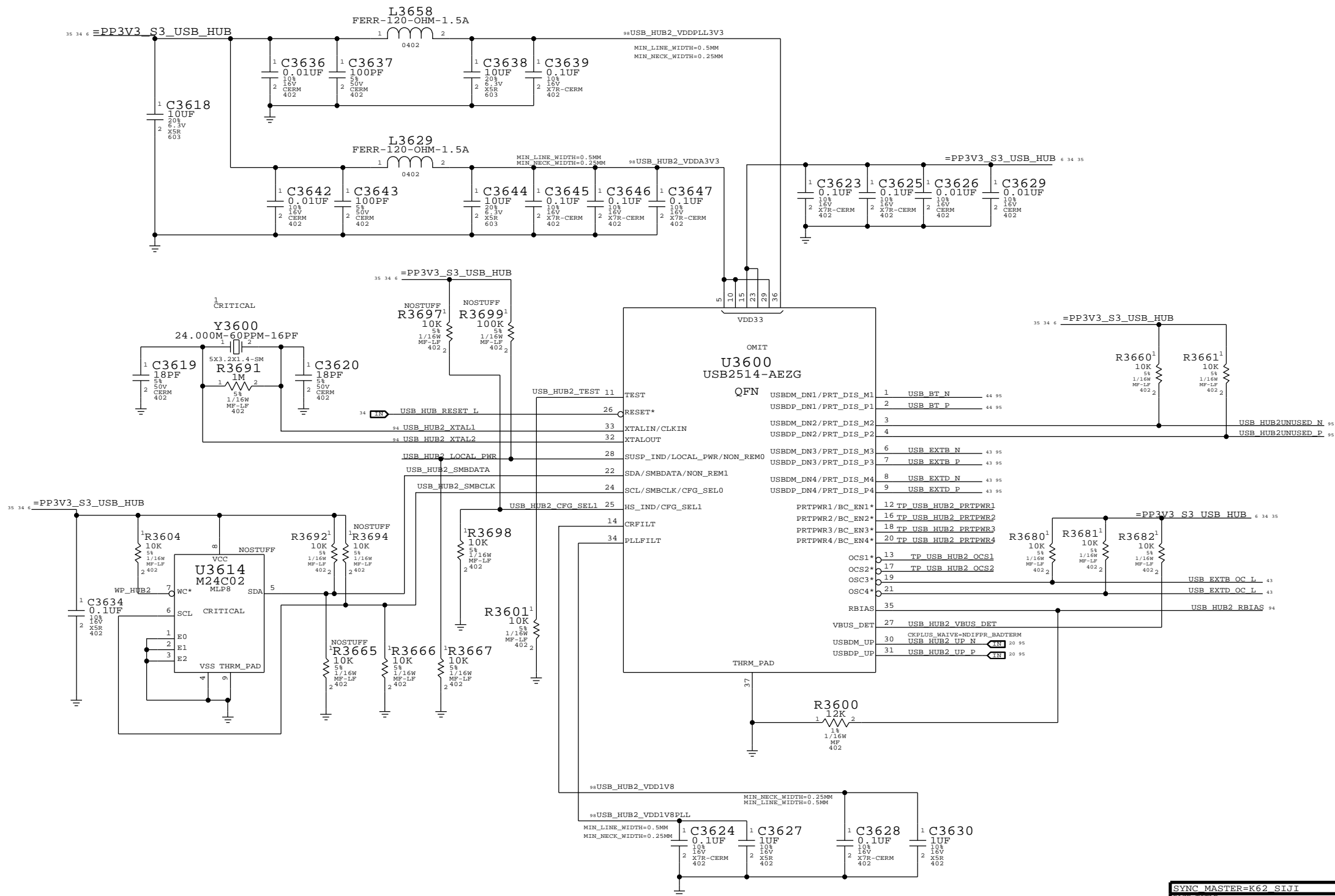
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SHEET

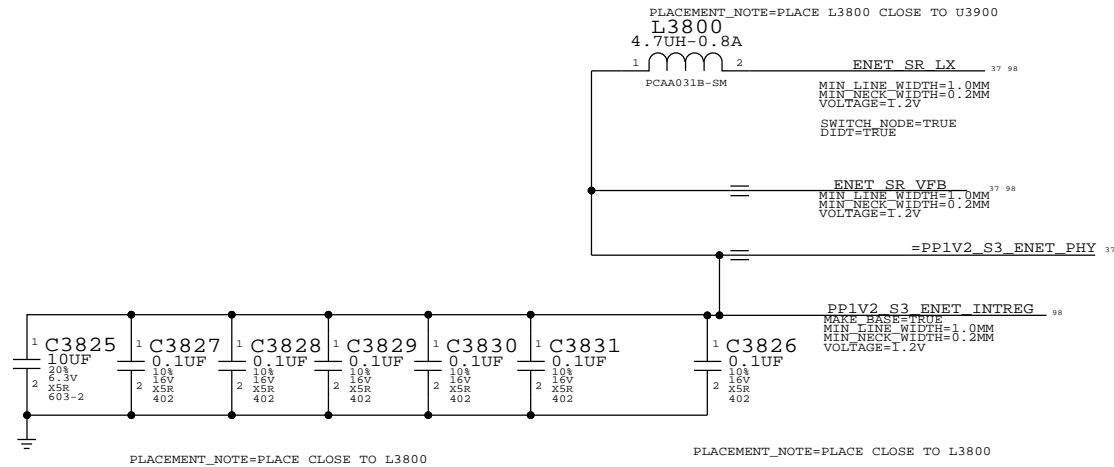
34 OF 101

USB HUB-2

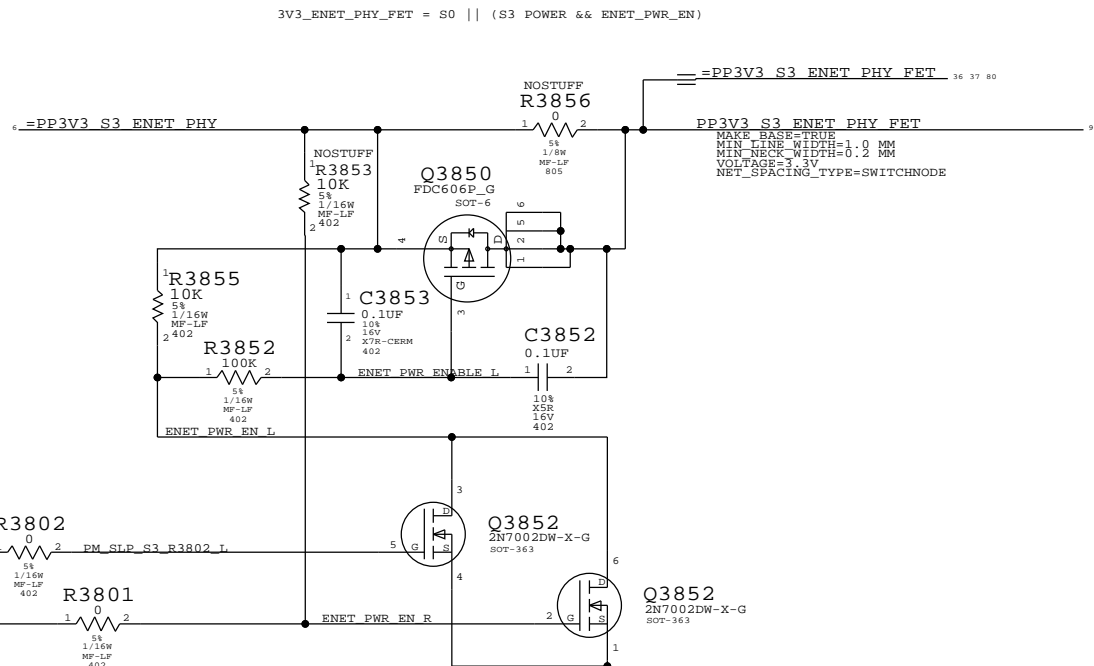


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PAGE TITLE			
USB HUB 2			
 Apple Inc.	DRAWING NUMBER	051-8442	SIZE
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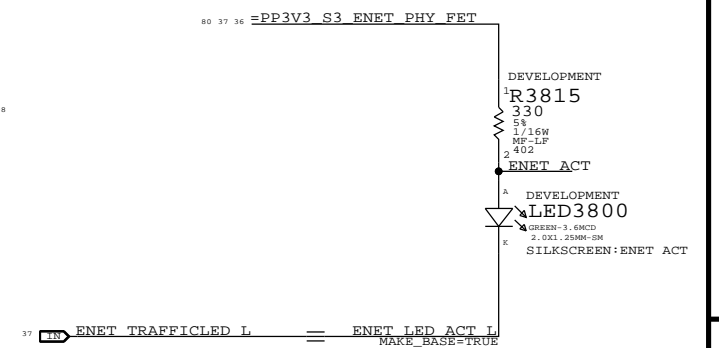
CAESAR IV 1.2V INT.VR CMPTS



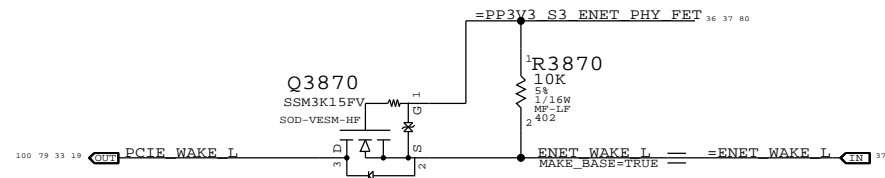
CAESAR IV POWER ENABLE CIRCUIT



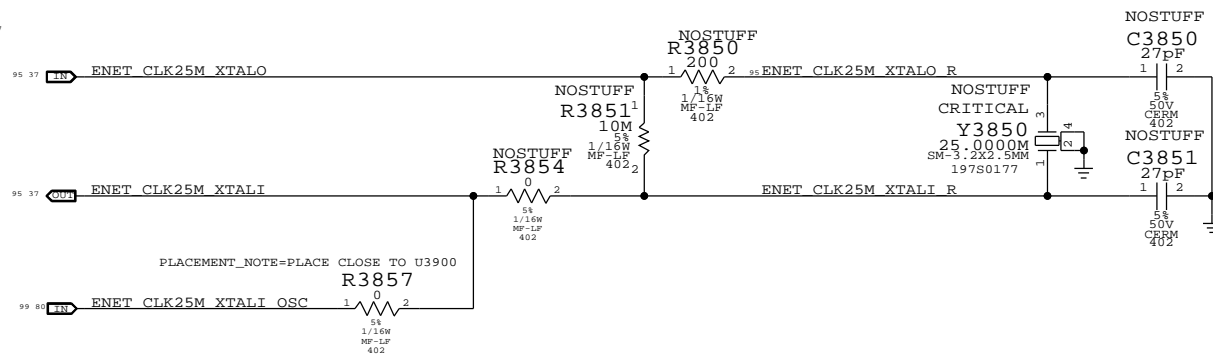
CAESAR IV ACTIVITY LED



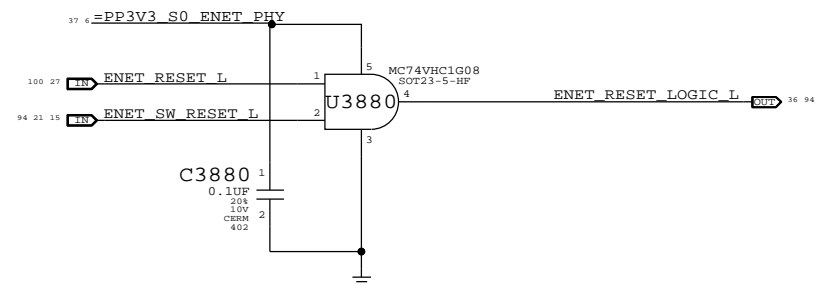
CAESAR IV WAKE# ISOLATION



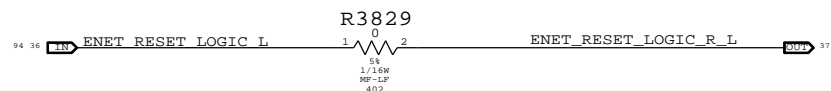
CAESAR IV 25MHZ XTAL



CAESAR IV SW RESET GATING

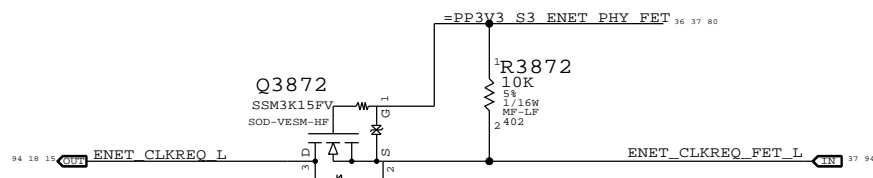



CAESAR IV RESET CONNECTION



CAESAR IV STRAPS (NONE)

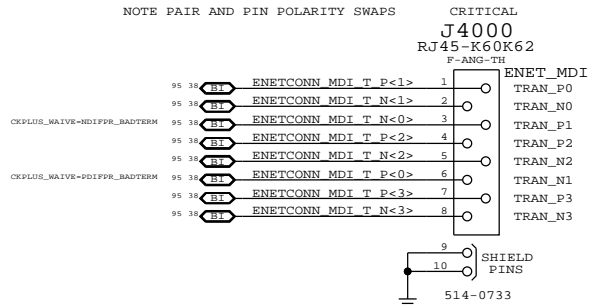
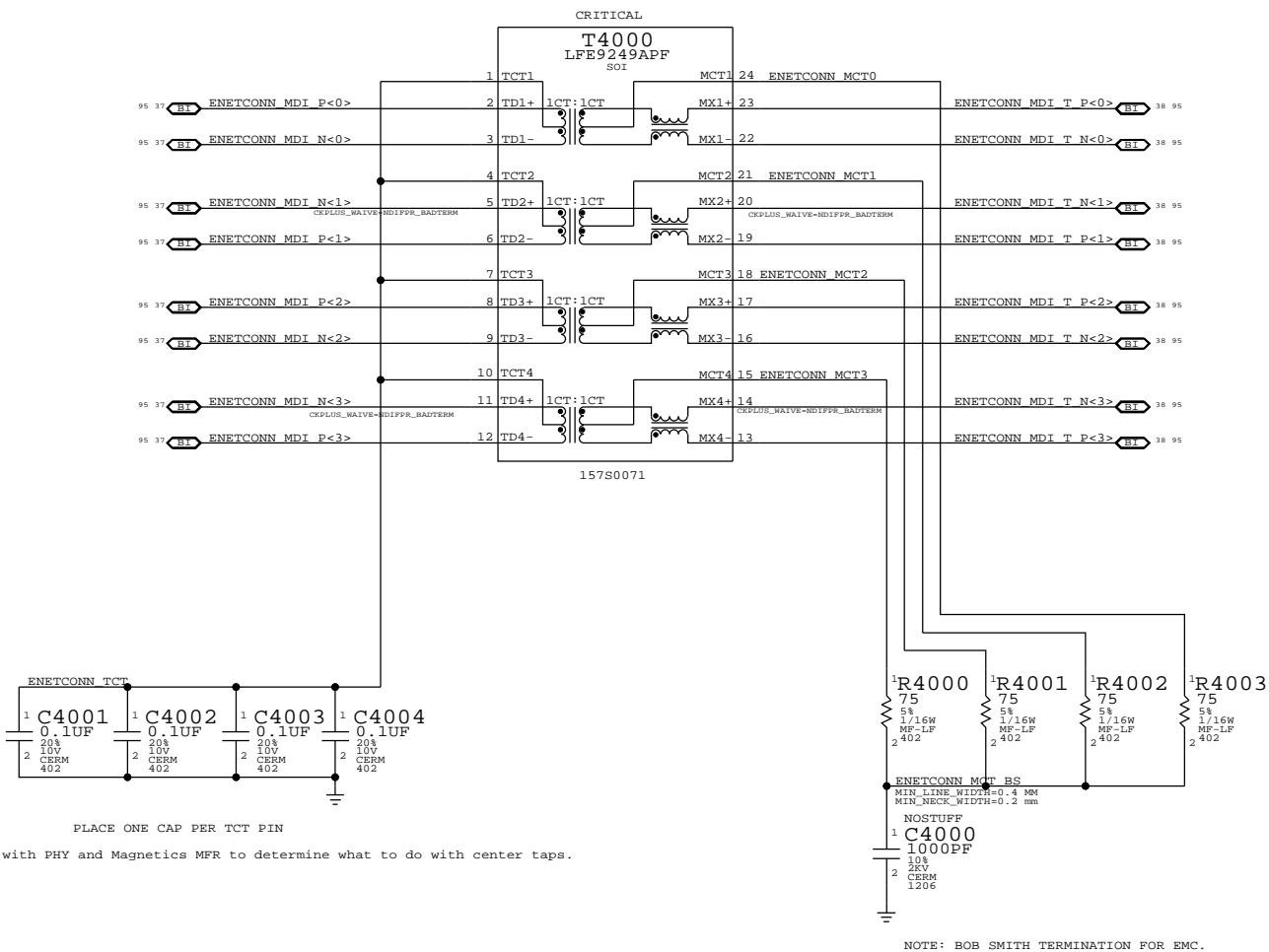
CAESAR IV CLKREQ ISOLATION



SYNC MASTER=K62 MARK		SYNC DATE=01/09/2011	
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CAESAR IV SUPPORT			
 Apple Inc.		DRAWING NUMBER	051-8442
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D

D

C

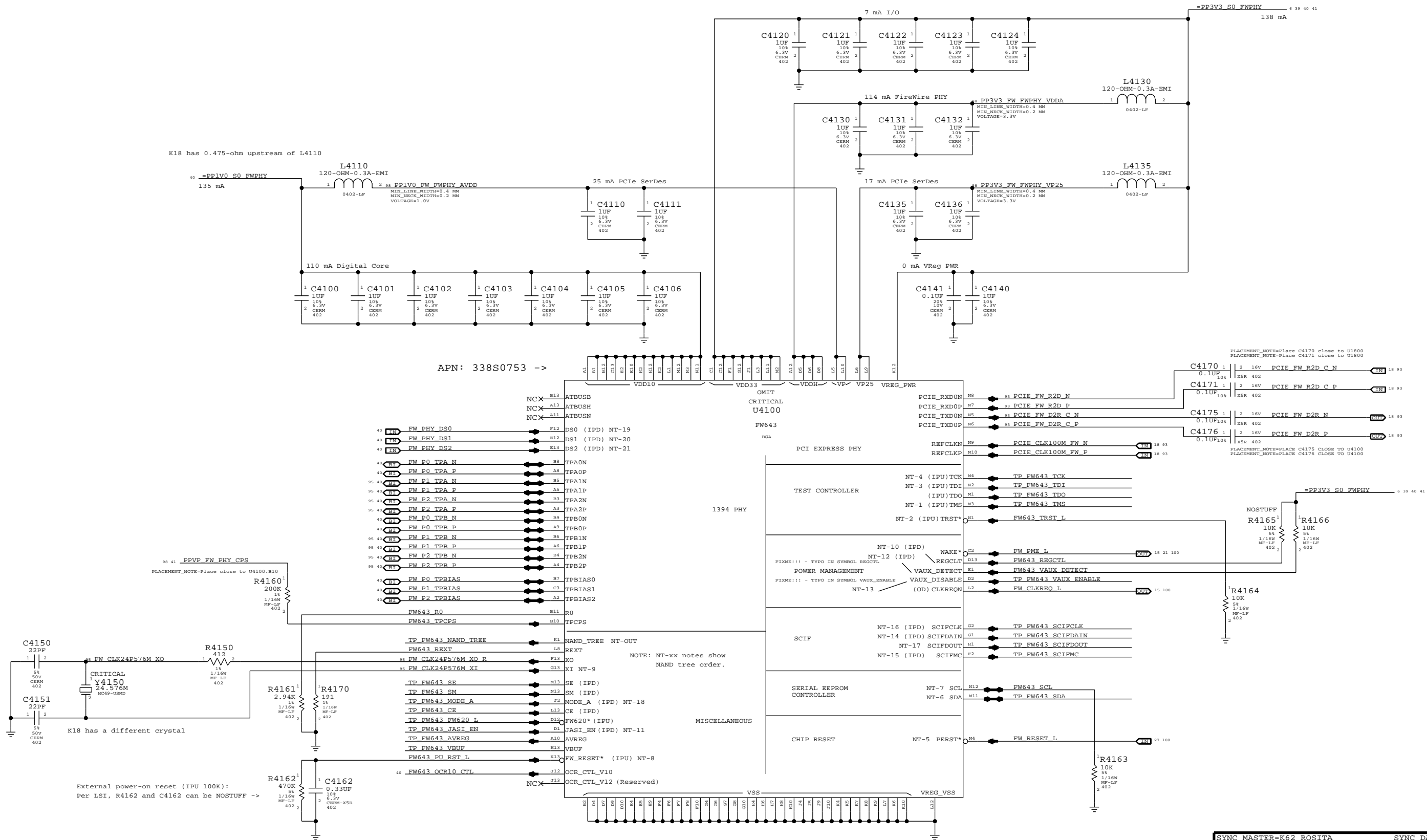
C


B

B

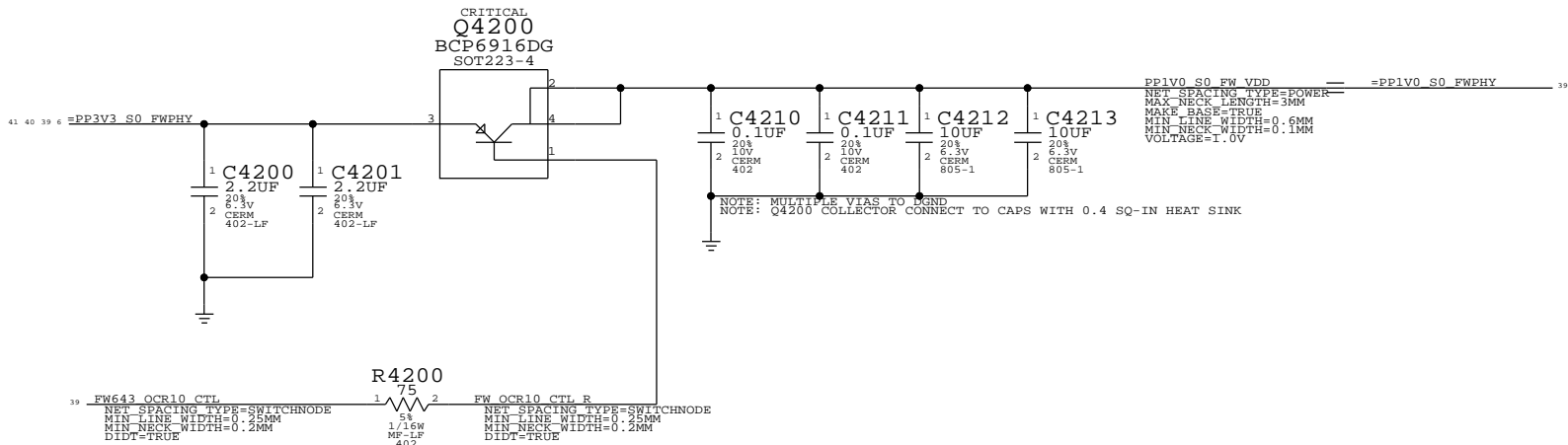
A

A

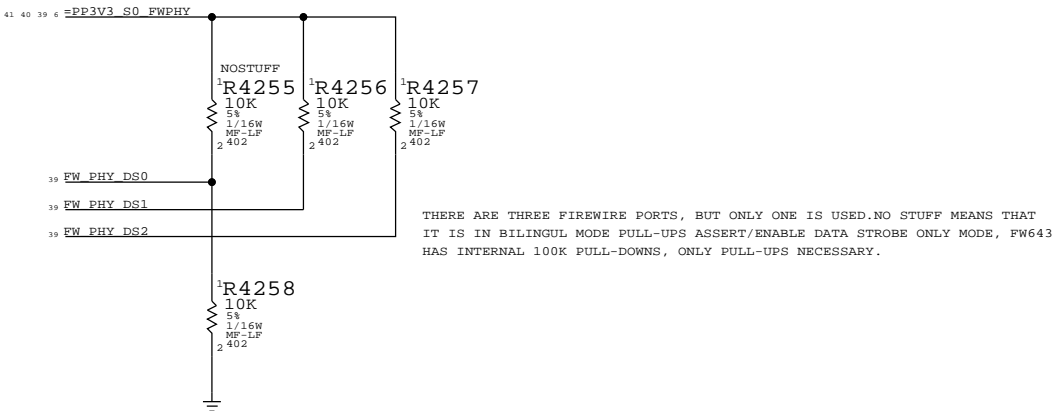


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PAGE TITLE			
FireWire LLC/PHY (FW643)			
 Apple Inc.		DRAWING NUMBER	051-8442
		REVISION	10.1.0
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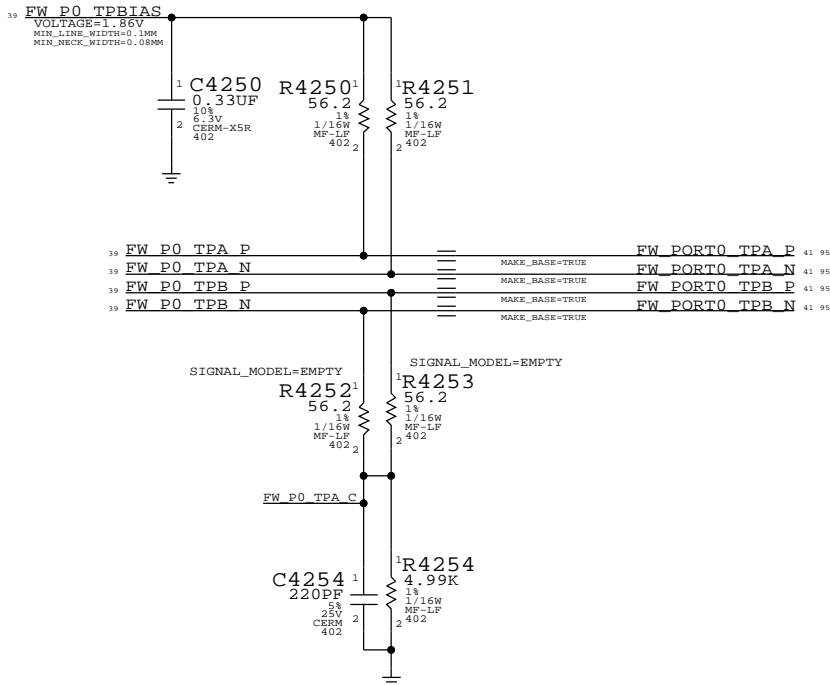
FW643 1.0V GENERATION



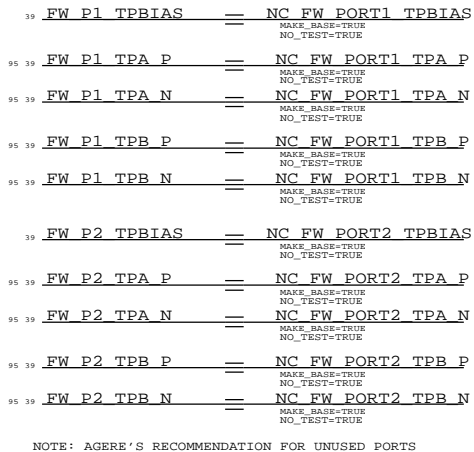
1394 PHY DATA/STROBE OPTIONS

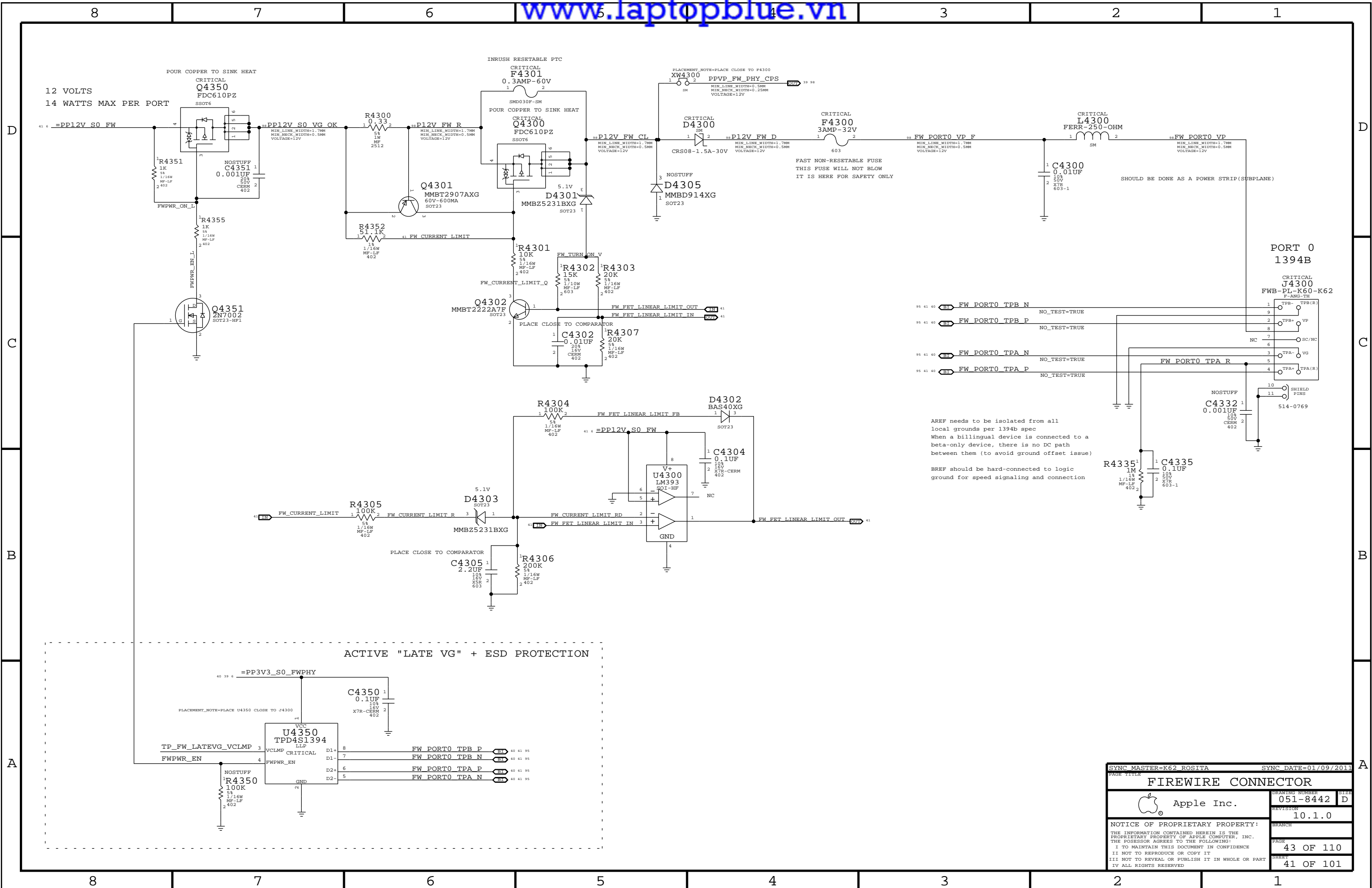


Termination
Place close to FireWire PHY



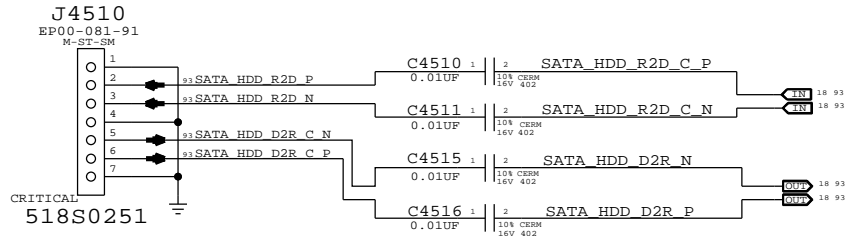
2ND & 3RD TPA/TPB PAIR UNUSED





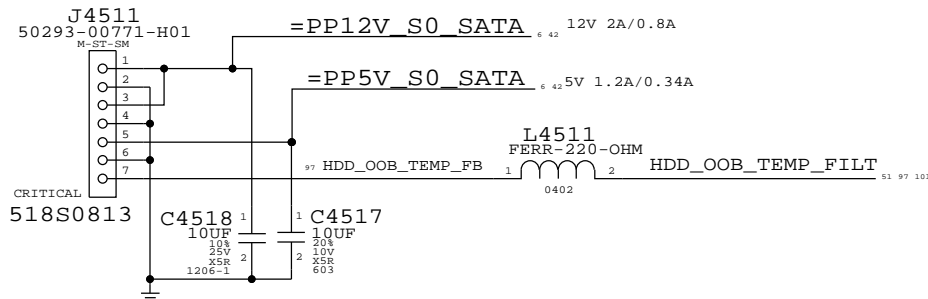
SILKSCREEN:SATA0

SATA PORT A0 FOR HDD



SILKSCREEN:HDD PWR

HDD Power

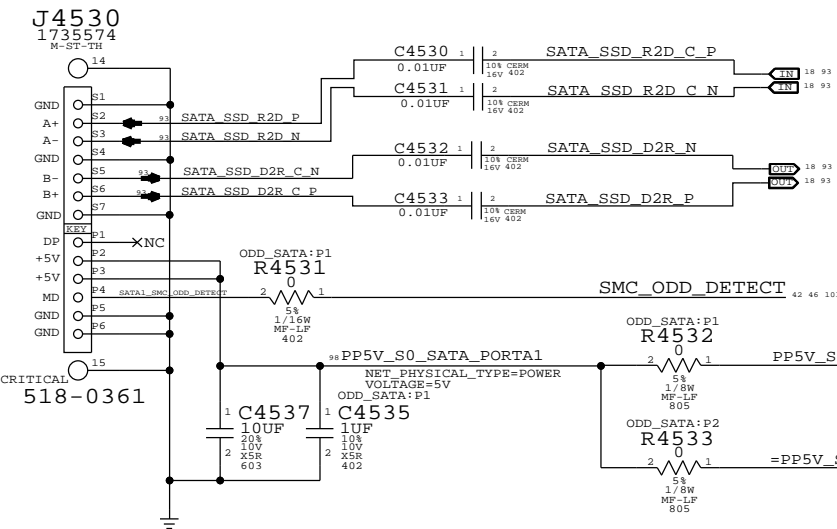


BOMOPTION OPTIONS FOR SATA PORT A1 AND A2

A1	A2	ODD_SATA:P1	ODD_SATA:P2
SSD	ODD		X
ODD		X	

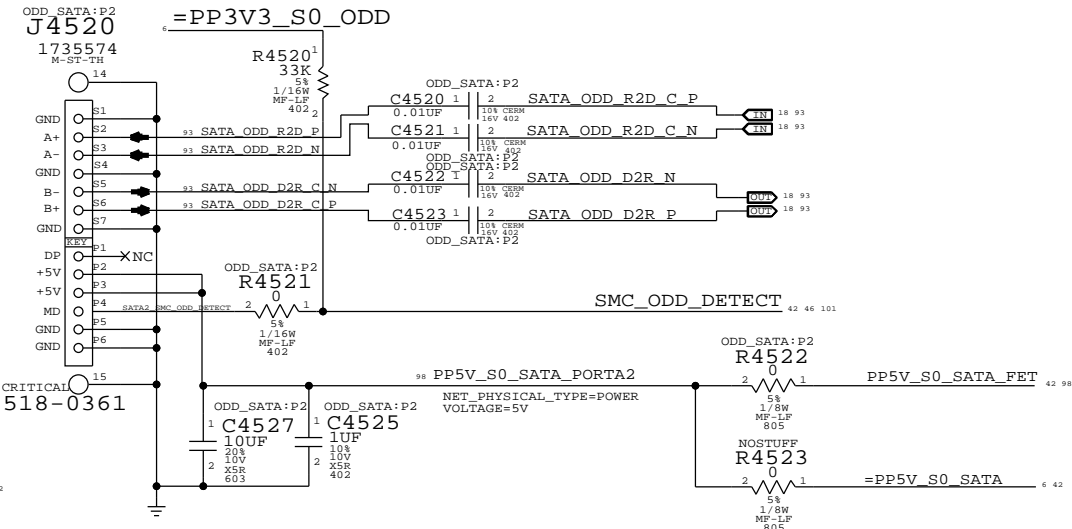
SATA PORT A1 FOR SSD/ODD

SILKSCREEN:SATA1

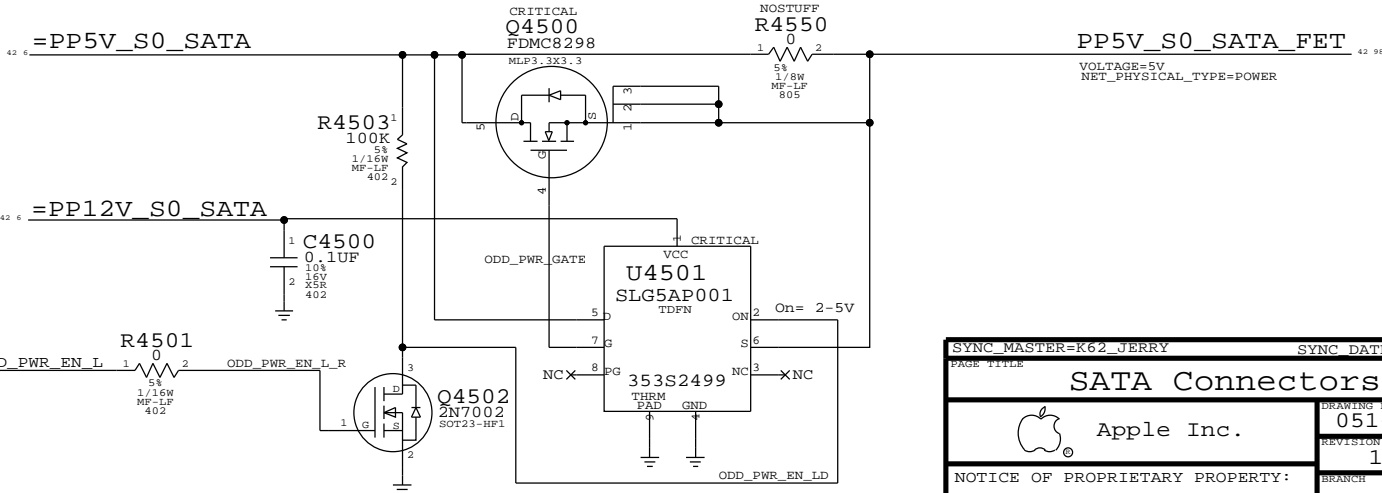
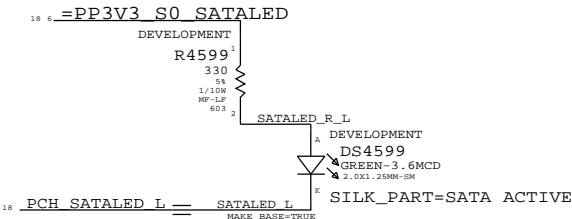


SILKSCREEN:SATA2

SATA PORT A2 FOR ODD



SATA Activity LED





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SATA Connectors		DRAWING NUMBER	
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Current Limit at 2.1Amp (@ S3 & S0)



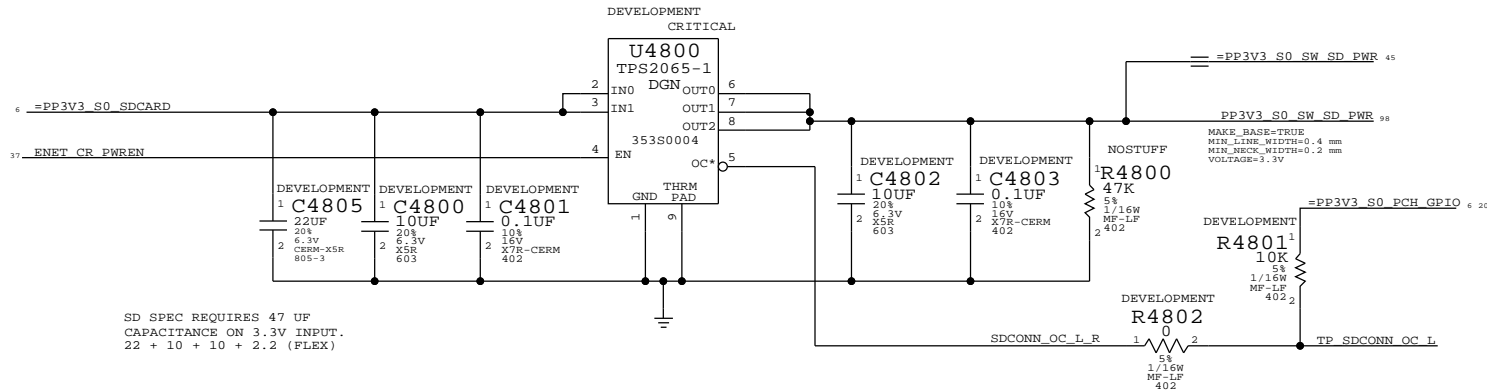
EXAMPLE: Port 1 - iPad fast charging = 2100mA
 Port 2 - Wired Keyboard = 1100mA
 Port 3 - iPhone fast charging = 1000mA
 PORT 4 - USB 2.0 500MA = 500MA
 TOTAL: 4700MA

SYNCH MASTER=K62 JERRY		SYNCH DATE=01/09/2011	
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EXTERNAL USB CONNECTORS			
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		REVISION 10.1.0	
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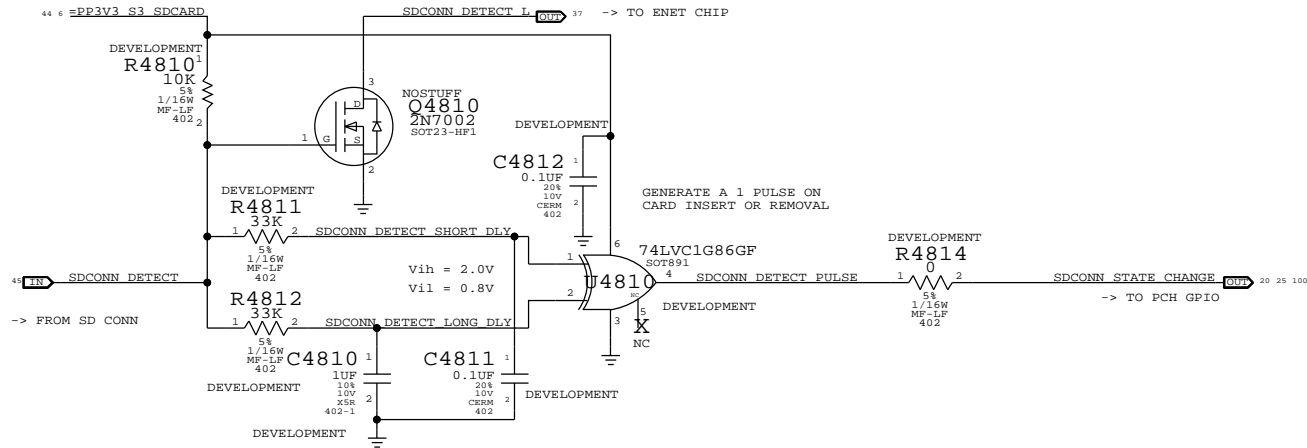
SYNC MASTER=K62 JERRY		SYNC DATE=01/09/2011	
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Internal USB Connections			
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SD CARD 3.3V OVERCURRENT PROTECTION CHIP WITH ACTIVE LOAD DISCHARGE

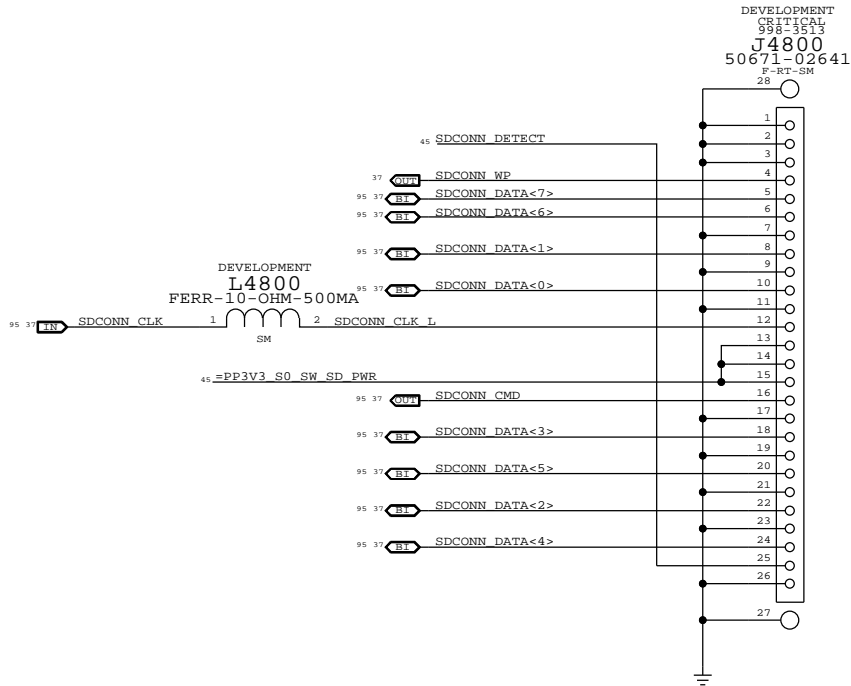
TPS2065-1 (1.0A LIMIT) HAS ACTIVE LOAD DISCHARGE SO R4800 IS NOSTUFF.



SDCONN DETECT DEBOUNCE, INVERSION, AND DETECT-CHANGED PCH GPIO CIRCUIT



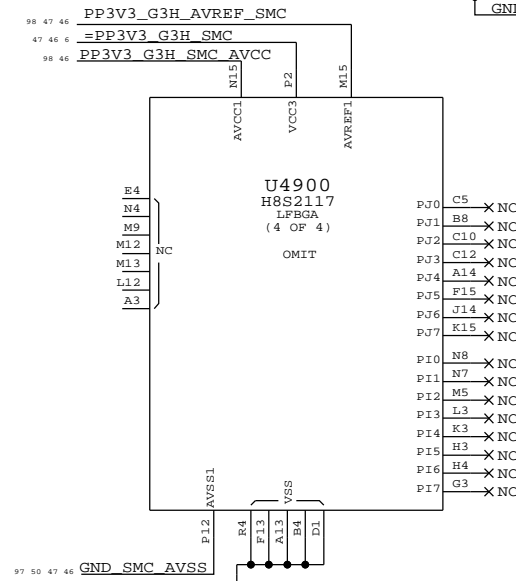
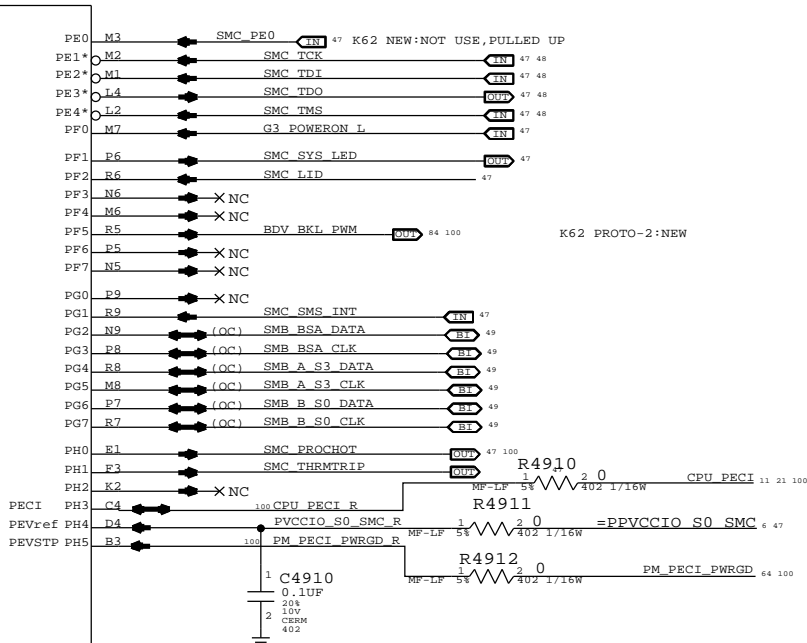
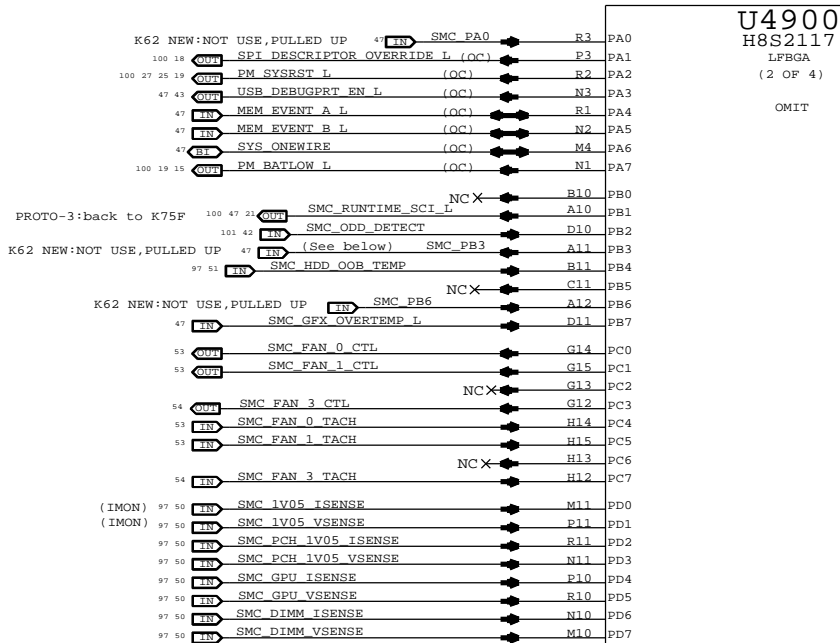
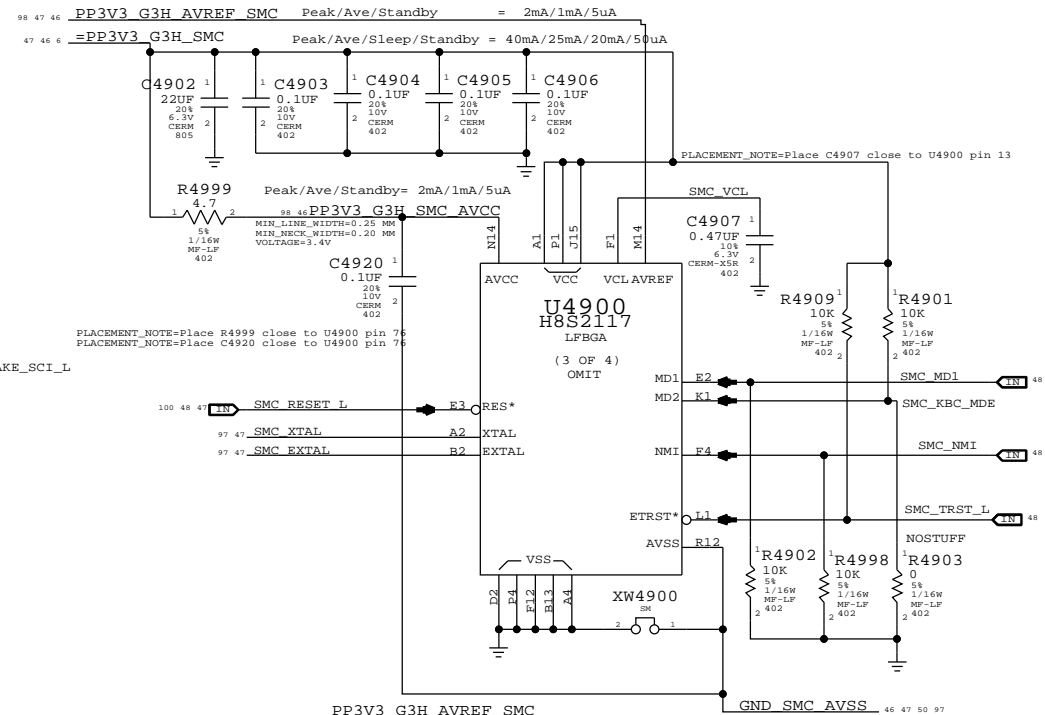
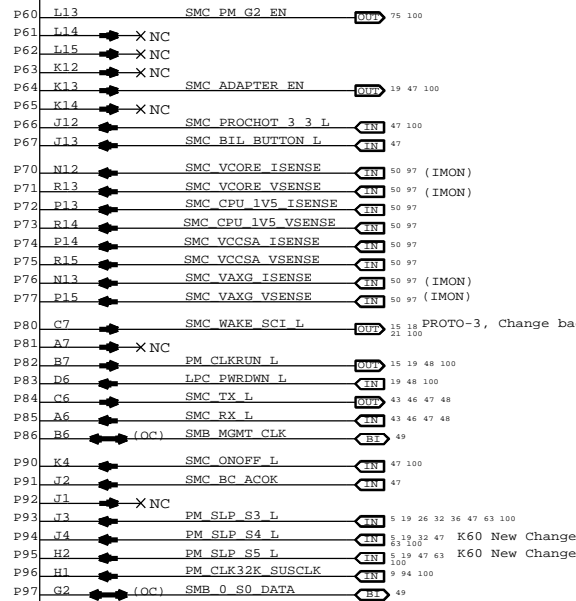
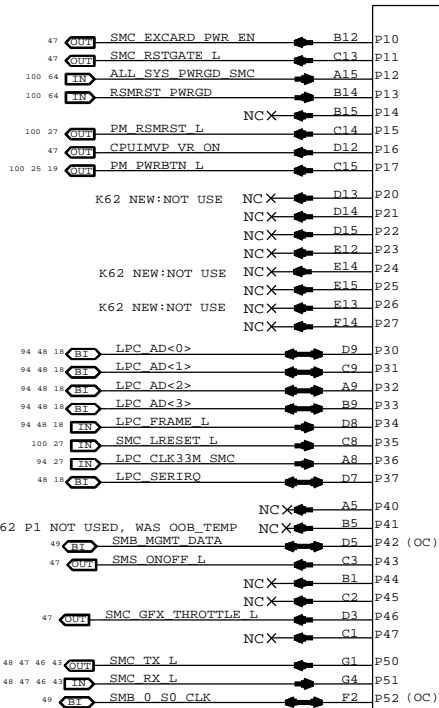
SD CARD CONNECTOR



PAGE TITLE		PAGE TITLE	
SD READER CONNECTOR		SD READER CONNECTOR	
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NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

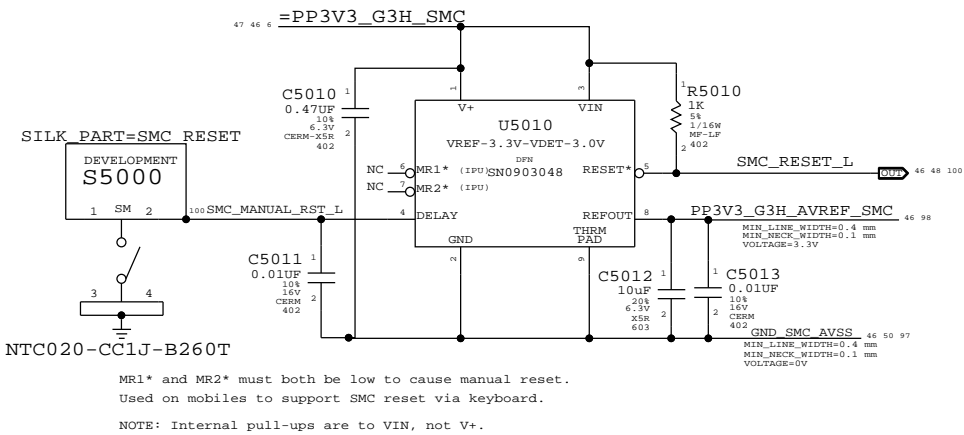
338S0878



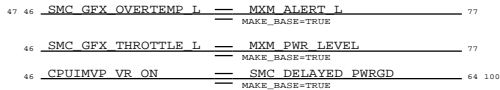
SMC PB3: SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)
SMC PG1: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

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SMC		DRAWING NUMBER	051-8442
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SMC Reset "Button", Supervisor & AVREF Supply

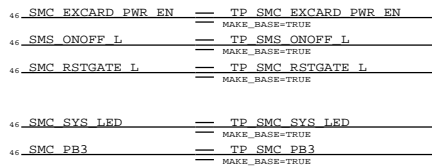


MISC. SIGNAL ALIASES

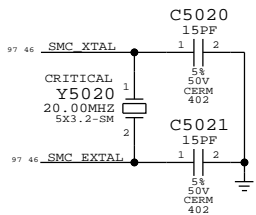


UNUSED PORT 7 ANALOG SENSORS

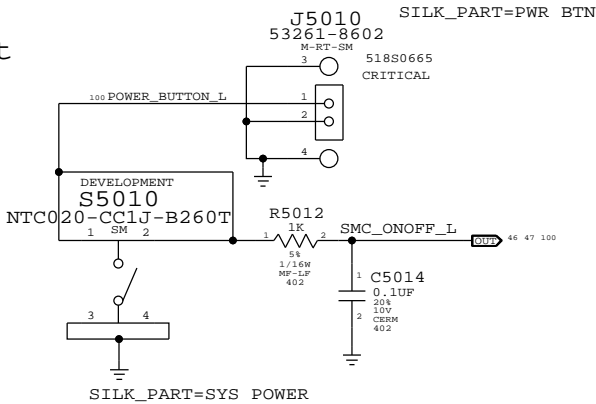
UNUSED TP/NC ALIASES



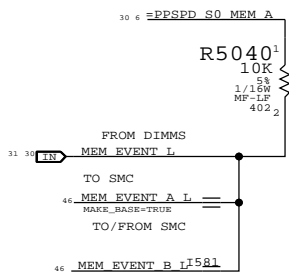
SMC Crystal Circuit



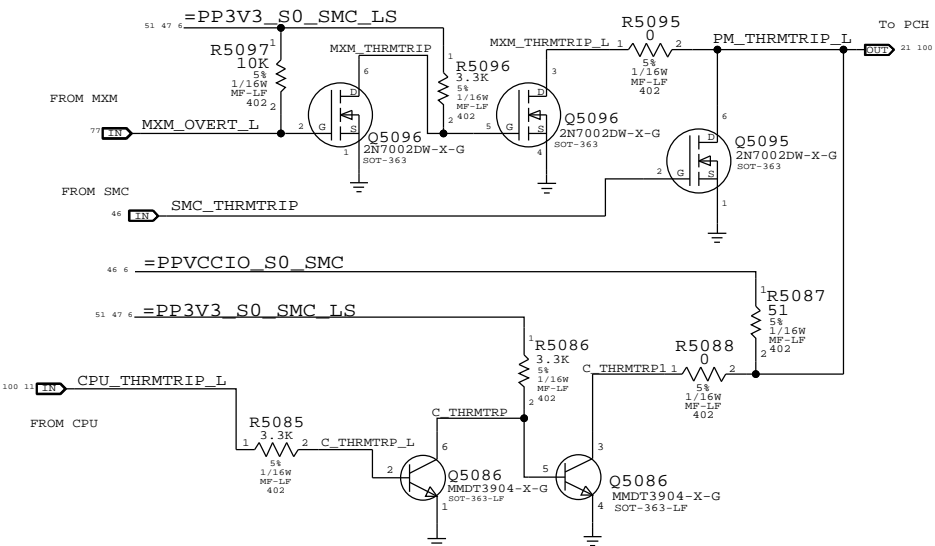
POWER BUTTON



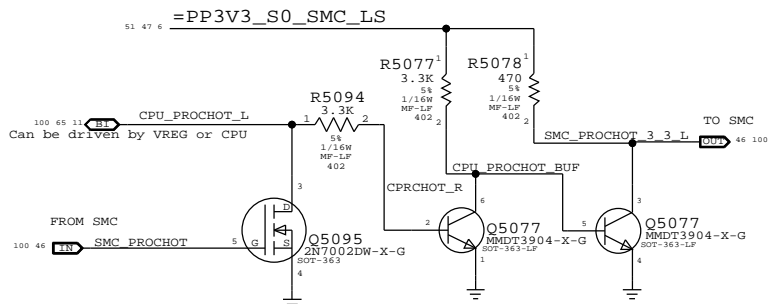
MEM_EVENT



SMC & MXM THERMTRIP LEVEL SHIFTING

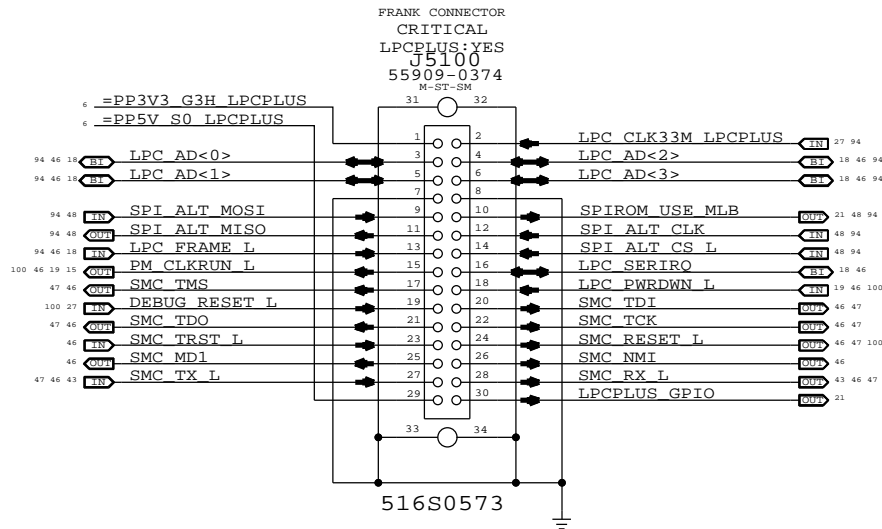


SMC PROCHOT 3.3V LEVEL SHIFTING

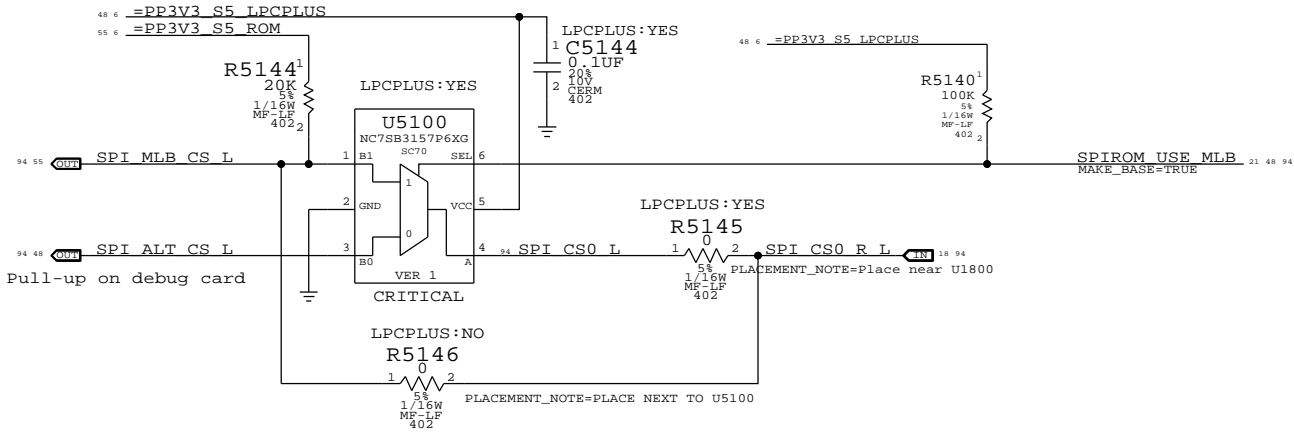


SYNC MASTER=K62 JERRY		SYNC DATE=01/09/2011	
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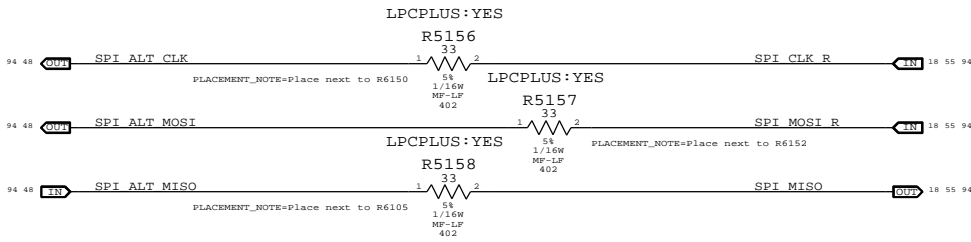
LPC+SPI Connector



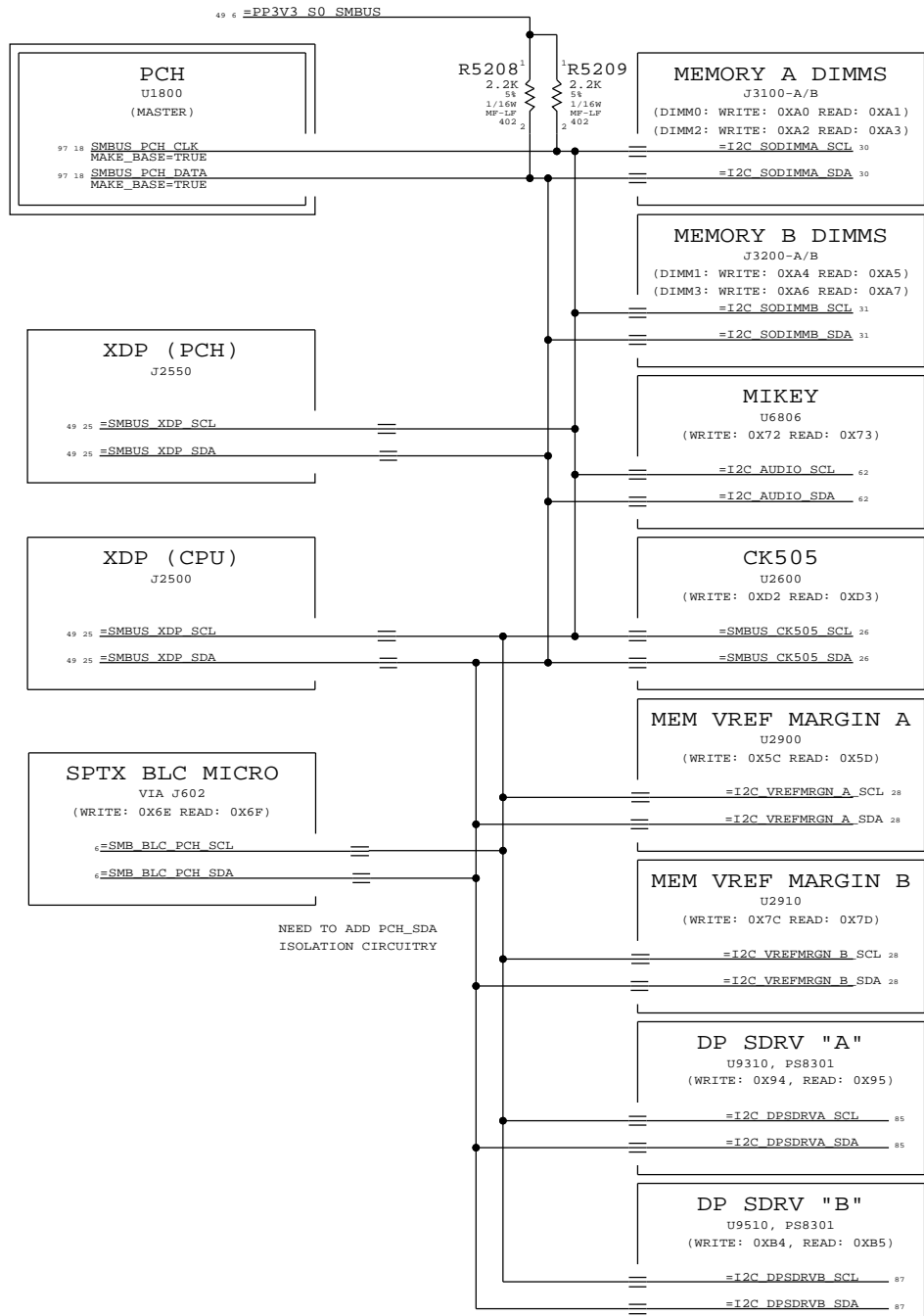
Alternate SPI ROM Support



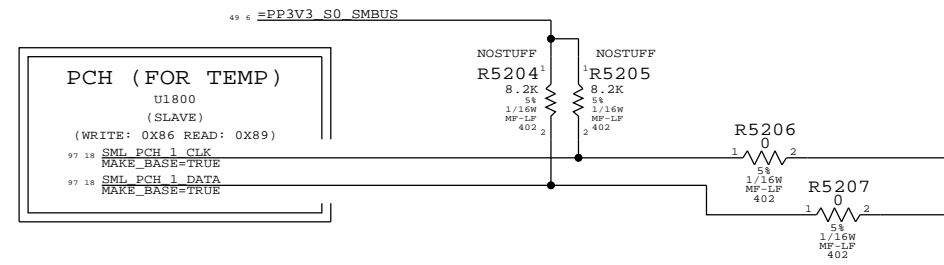
SPI Bus Series Resistance Option



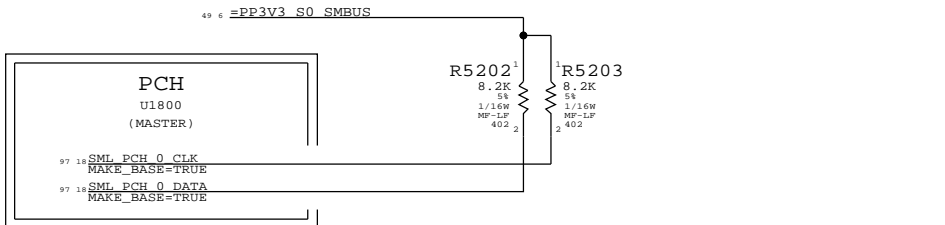
PCH "SMBUS" CONNECTIONS



PCH "SML 1" CONNECTIONS



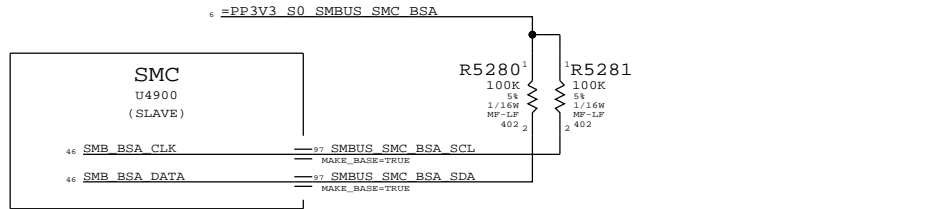
PCH "SML 0" CONNECTIONS



THIS PAGE DIFFERENT BETWEEN K60 AND K62.

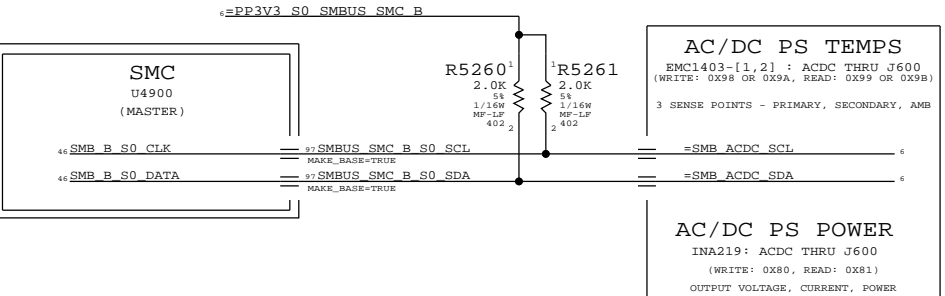
SMC SLAVE SMBUS "2" CONNECTIONS

USES INTERNAL SMC CONTROLLER CHANNEL 2 ONLY (NO CONNECTIONS, JUST PULLUP)



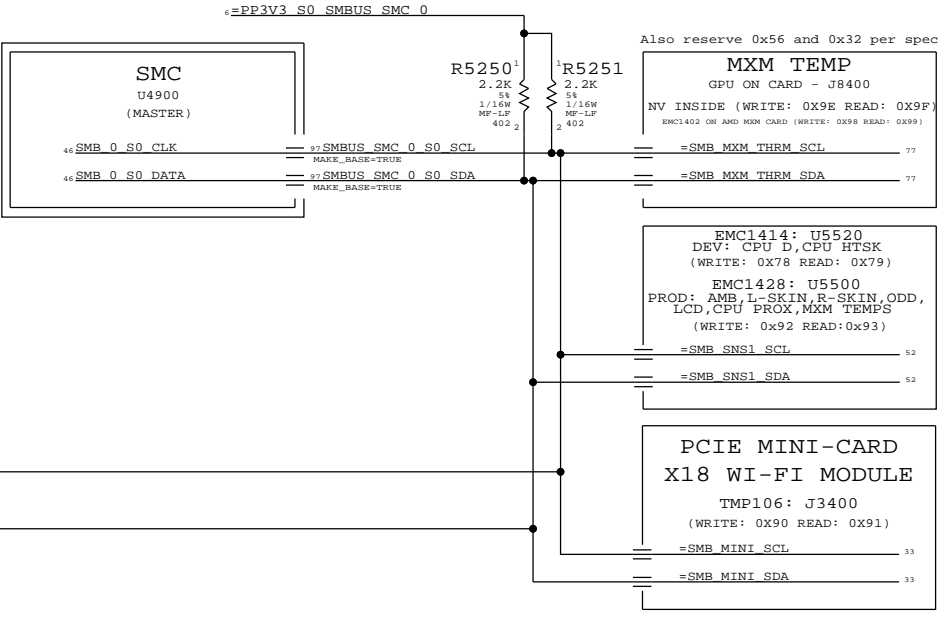
SMC "B" SMBUS CONNECTIONS

BUS B CAN USE EITHER INTERNAL SMC CHANNEL 0 OR 1, K60/62 CHOOSES 0



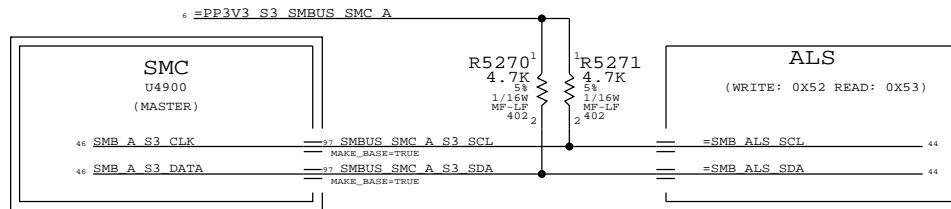
SMC "0" SMBUS CONNECTIONS

USES INTERNAL SMC CONTROLLER CHANNEL 0 ONLY



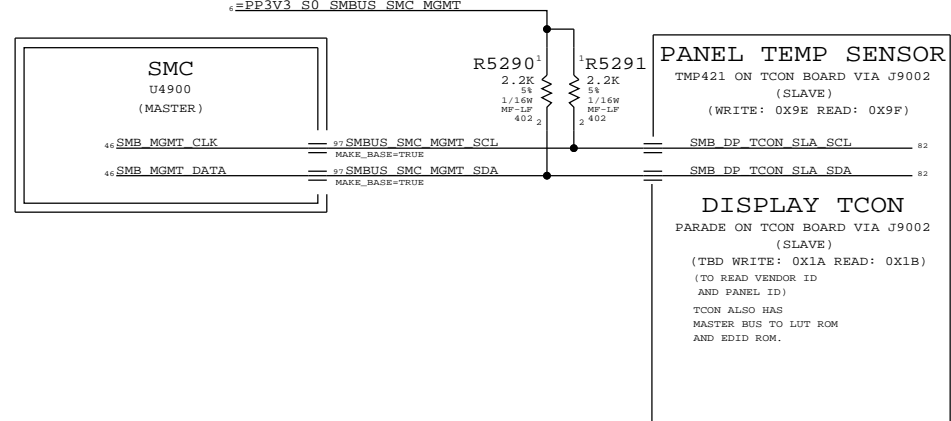
SMC "A" SMBUS CONNECTIONS

NOTE: SMC RMT BUS REMAINS POWERED AND MAY BE ACTIVE IN S3 STATE
BUS A CAN USE EITHER INTERNAL SMC CHANNEL 0 OR 1, K74 CHOOSES 1

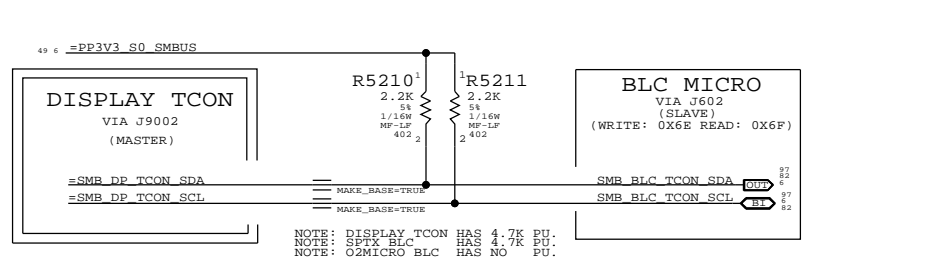


SMC "MANAGEMENT" SMBUS (BUS 1)

USES INTERNAL SMC CONTROLLER CHANNEL 1 ONLY

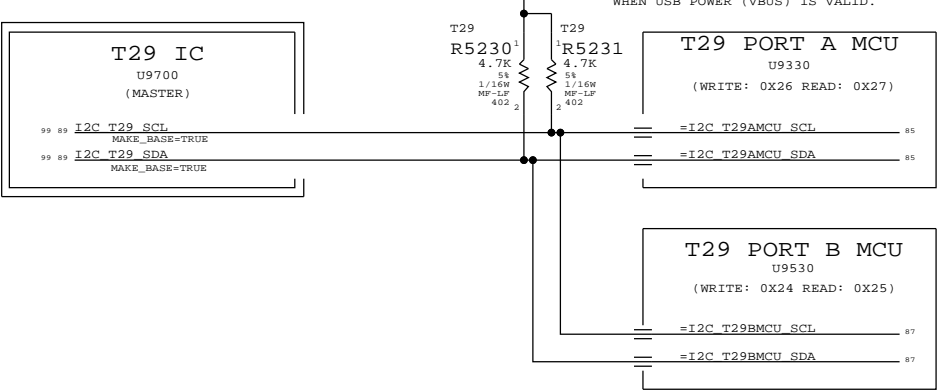


DISPLAY TCON TO SPTX OR O2M BLC




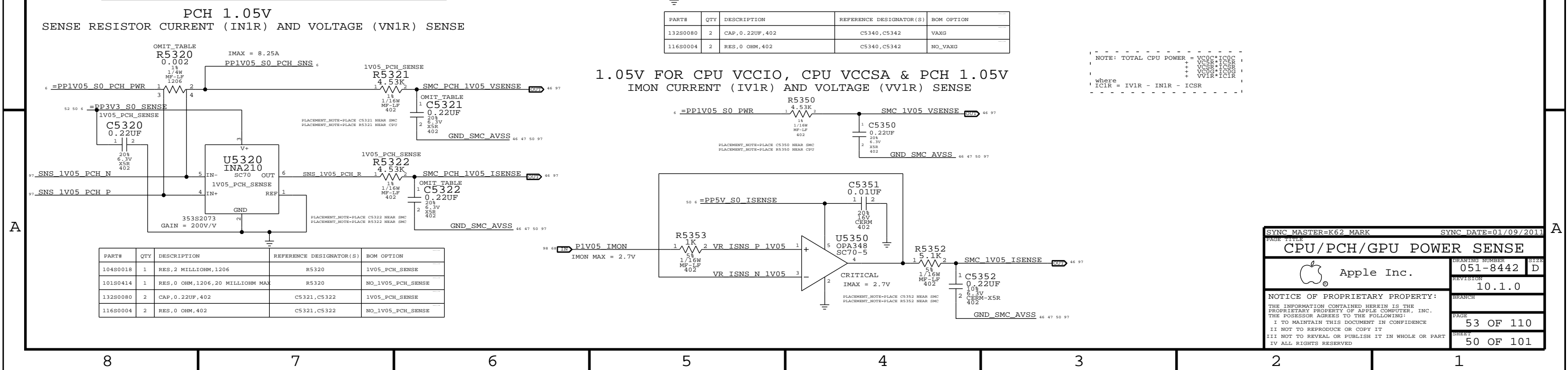
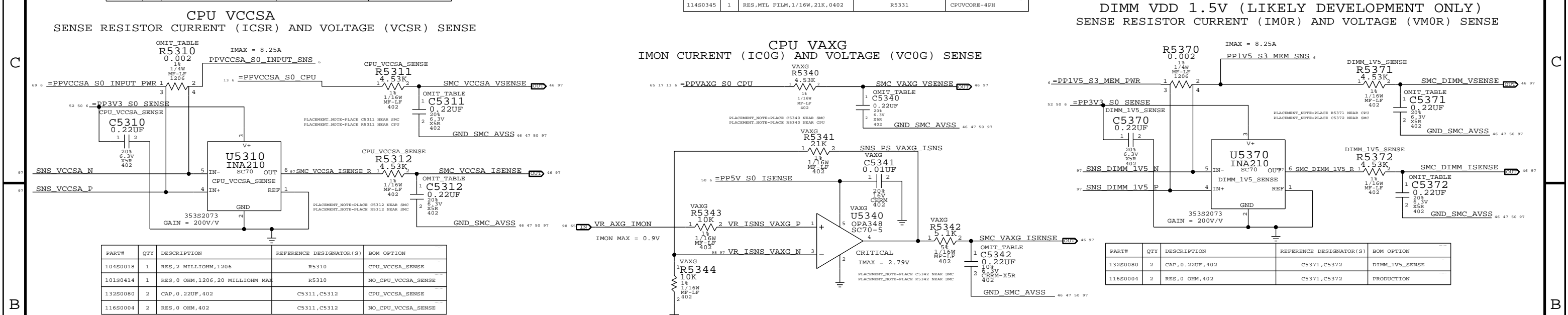
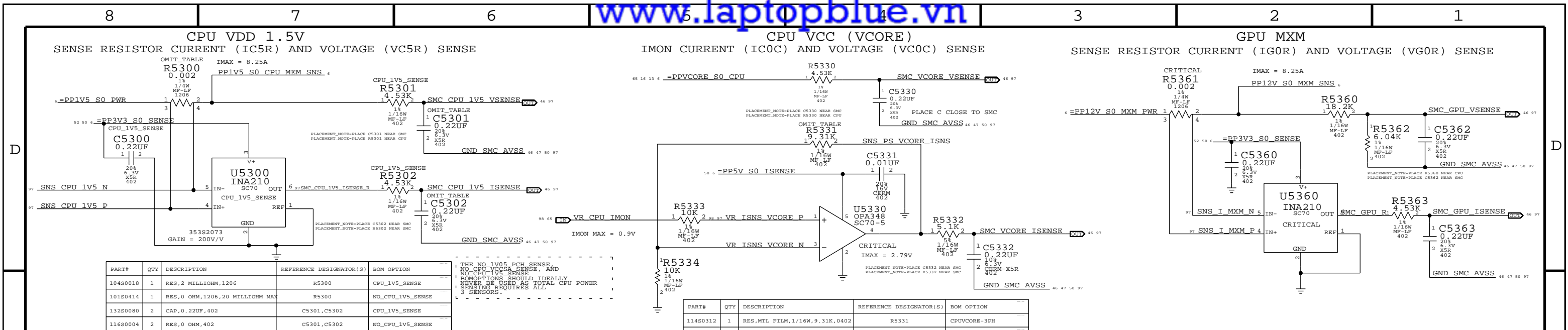
T29 I2C CONNECTIONS

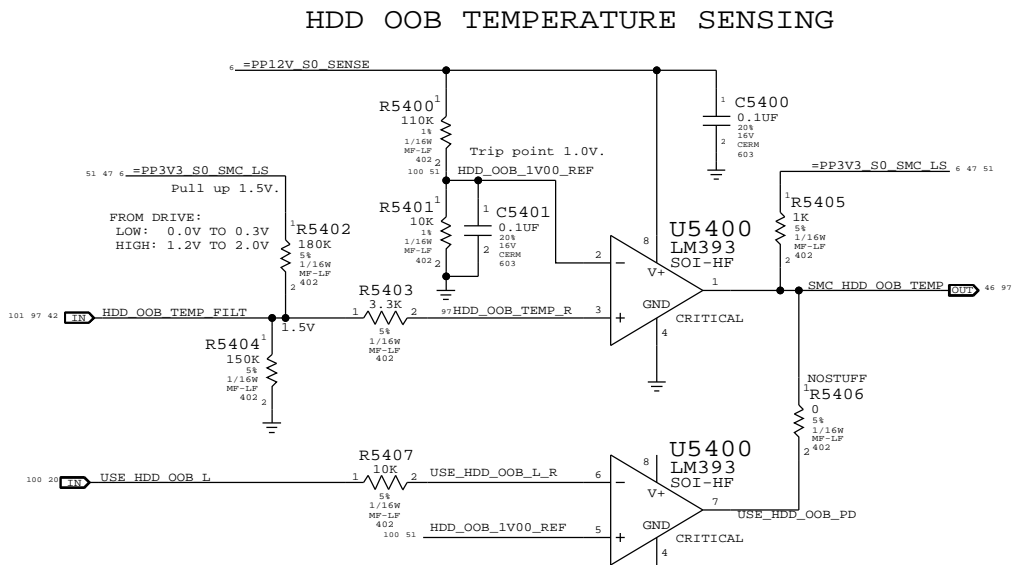
49 6 =PP3V3 S0 T29I2C



THE PCH address is user programmable by SPI ROM


SYNC MASTER=K62 MARK		SYNC DATE=01/09/2011	
PAGE TITLE			
SMBUS CONNECTIONS			
 Apple Inc.	DRAWING NUMBER	051-8442	SIZE D
	REVISION	10.1.0	
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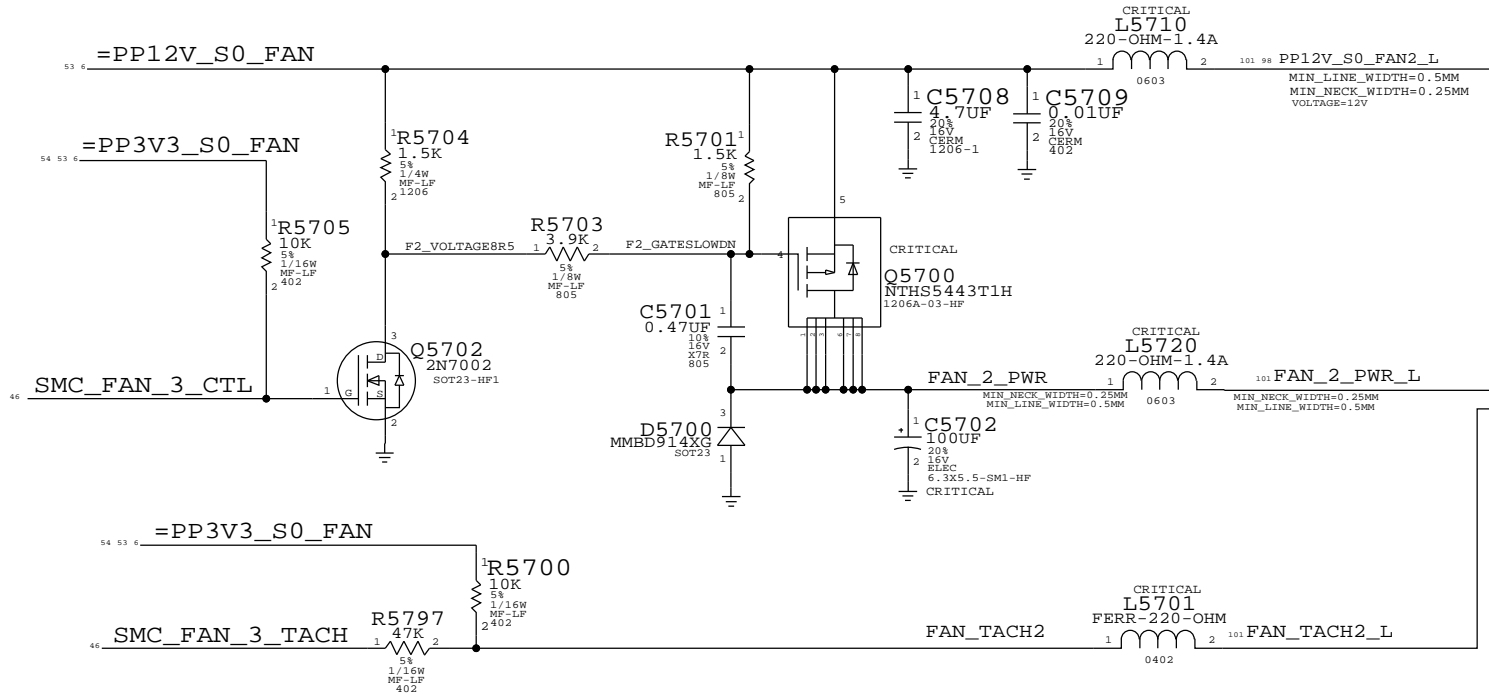


DRIVE ACTIVE = VALID SIGNAL, PROTOCOL BETWEEN 0-2.0V.
DRIVE ASLEEP = HDD DRIVES HDD_OOB_TEMP LOW
DRIVE ABSENT = OOB IS PULLED HIGH UNLESS PCH DETERMINES SSD PRESENT AND DRIVES USE_HDD_OOB_L LOW WHICH THEN PULLS HDD_OOB_TEMP LOW.

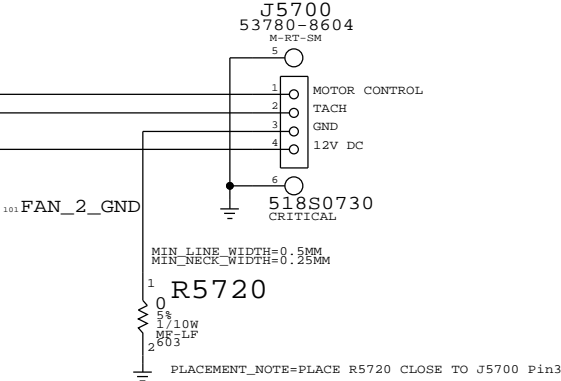
NOTE: WILL BE CONNECTED TO SATA PWR CONNECTOR PIN 11
THIS PIN IS ORIGINALLY INTENDED FOR HDD LED OUTPUT,
AND ALSO FOR HDD STAGGERED PIN UP (FLOATING) OR IMMEDIATE SPIN-UP (GROUND).
BOTH FUNCTIONS NOT USED.

SYNC MASTER=K62 MARK		SYNC DATE=01/09/2011	
PAGE TITLE			
TEMP SENSORS			
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		REVISION 10.1.0	
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SMC'S FAN3 OUTPUT CONTROL FAN 2

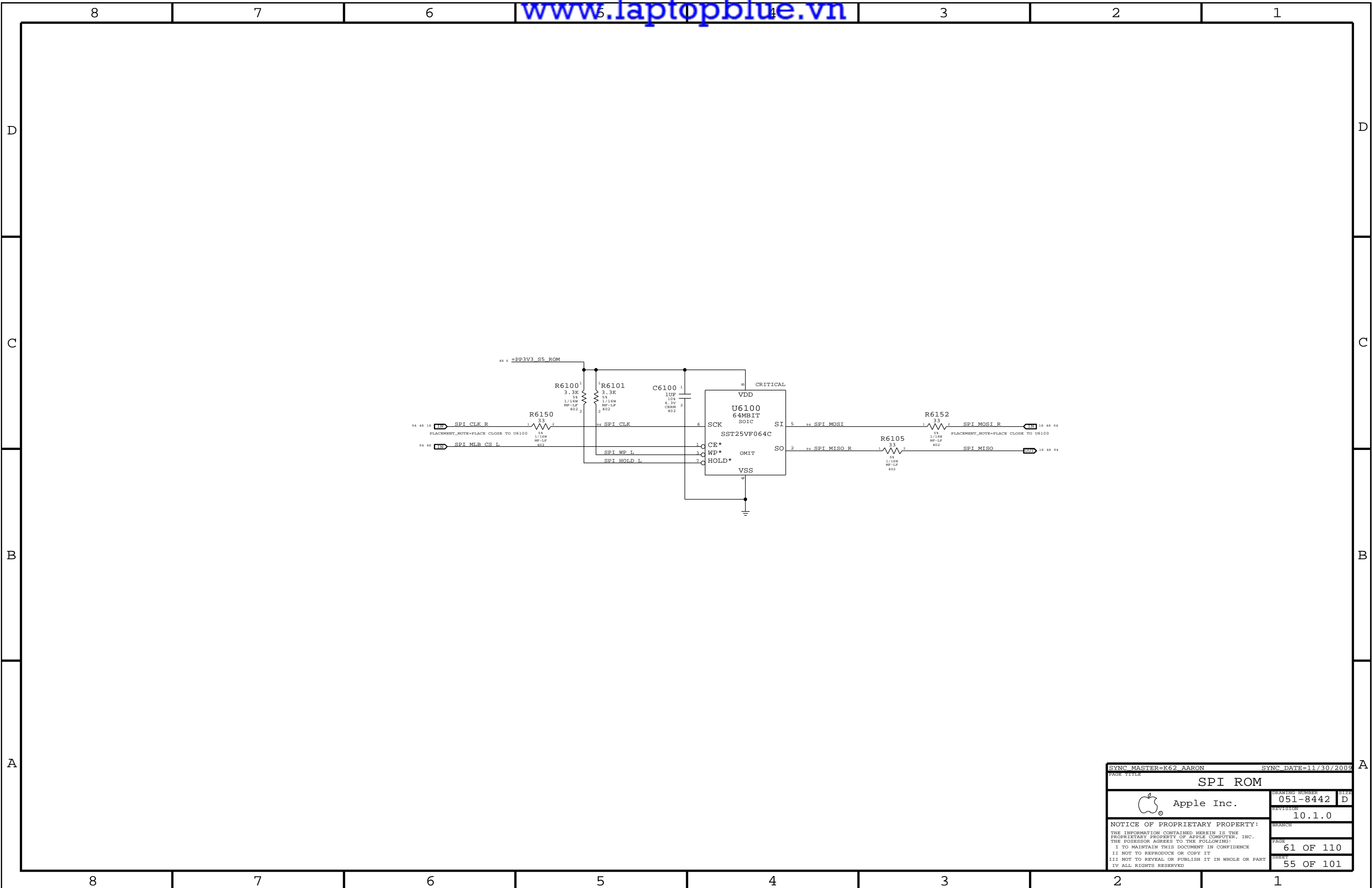


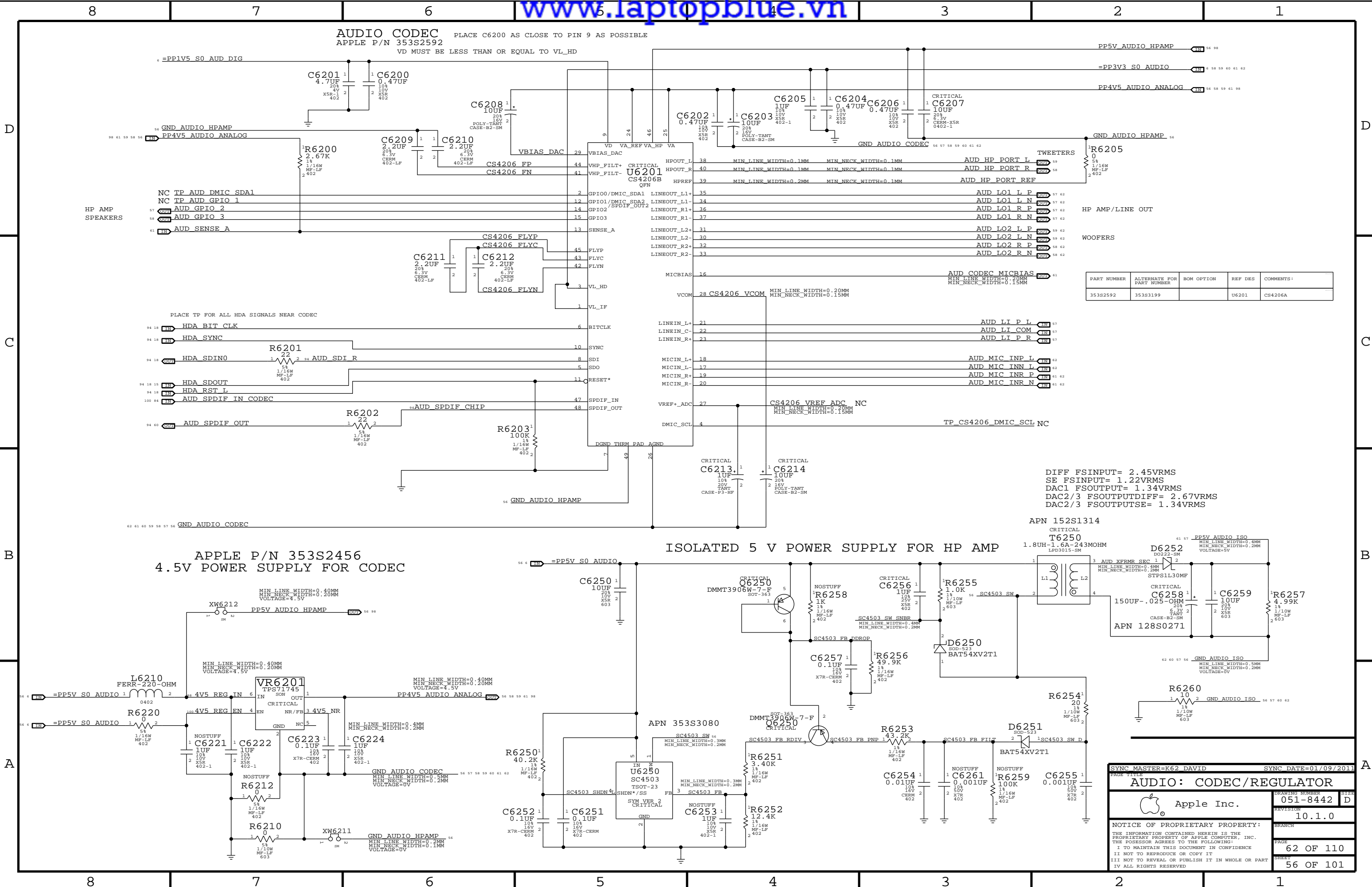
CPU FAN

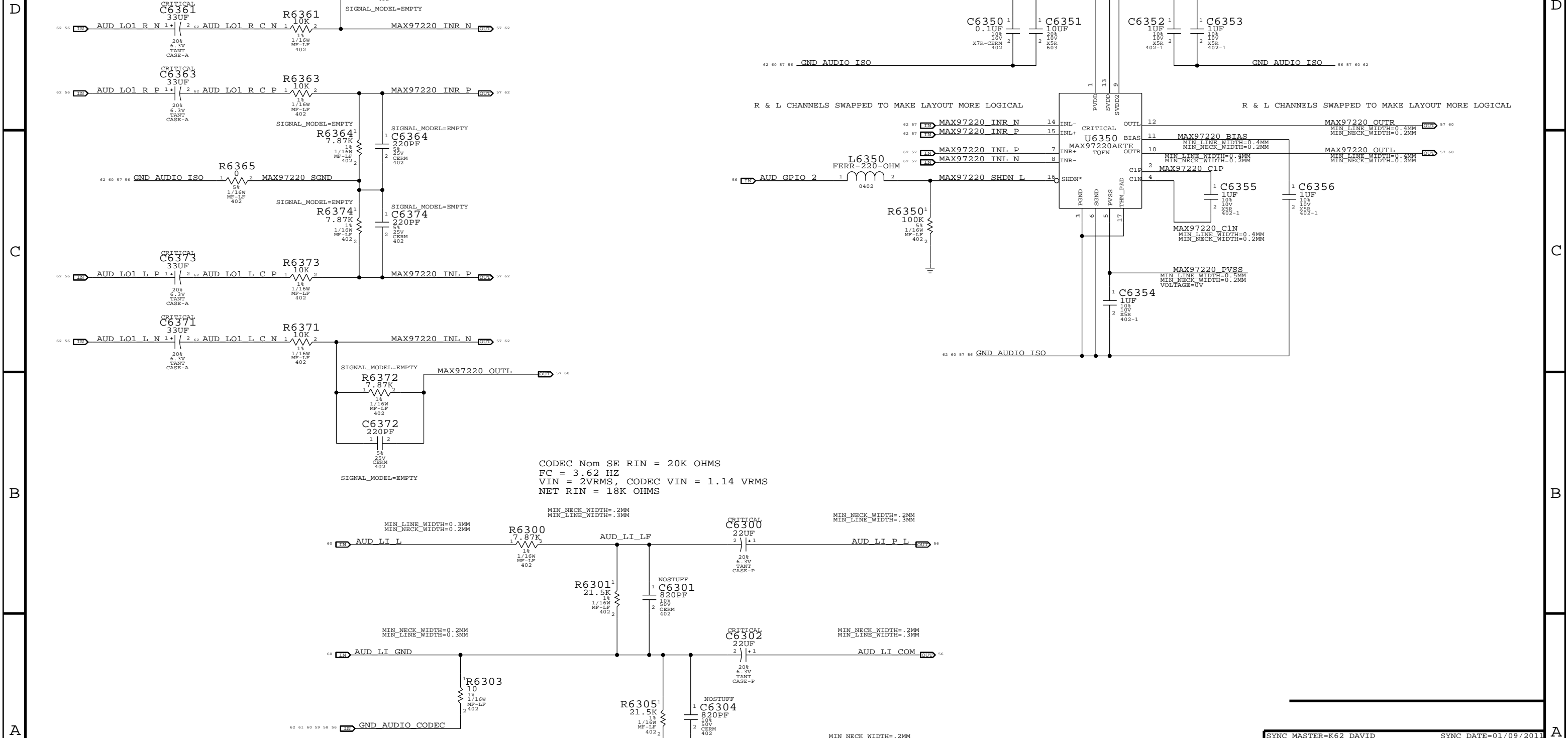



FAN 3 SMC CONTROL (UNUSED)

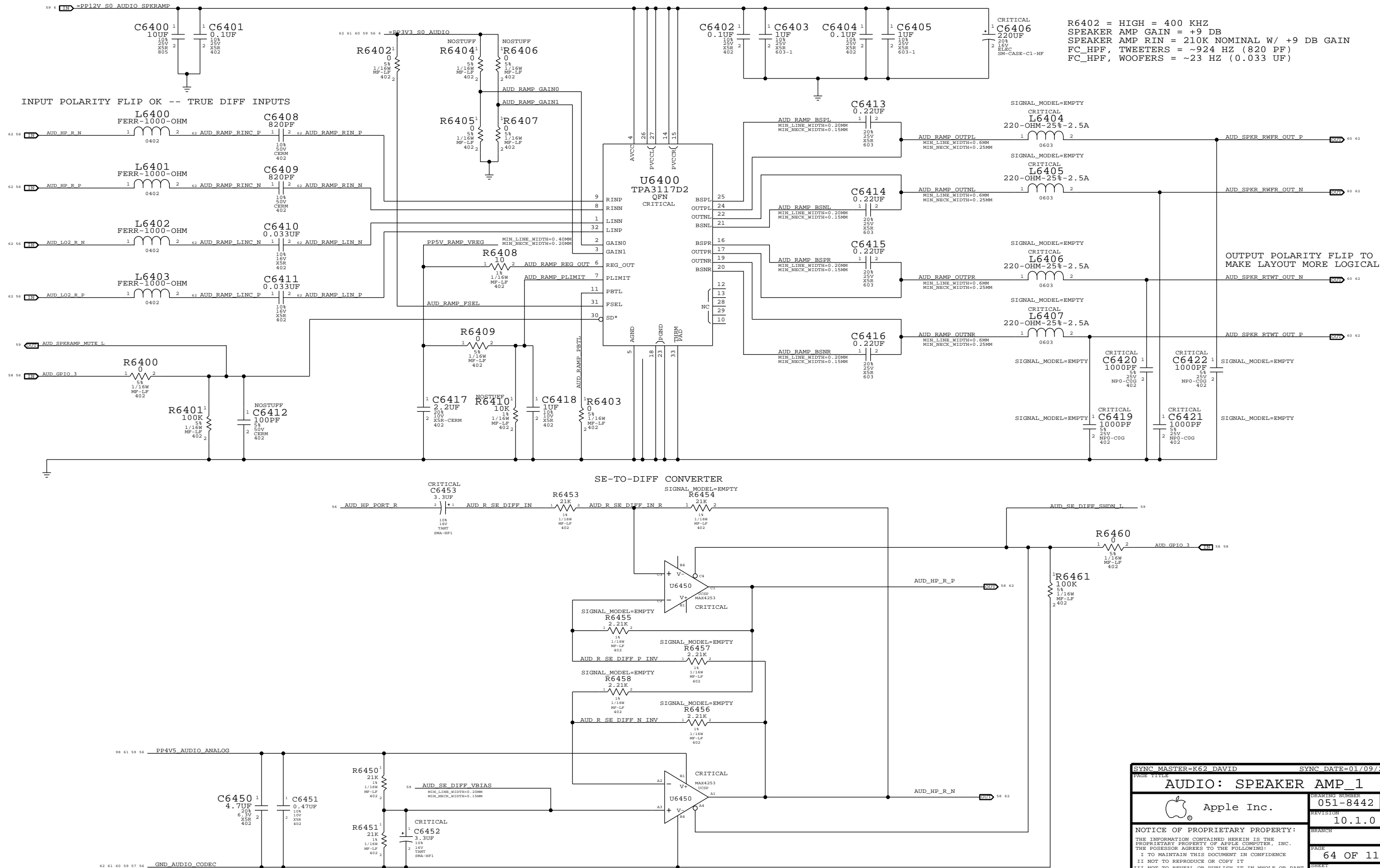
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PAGE TITLE			
CPU FAN			
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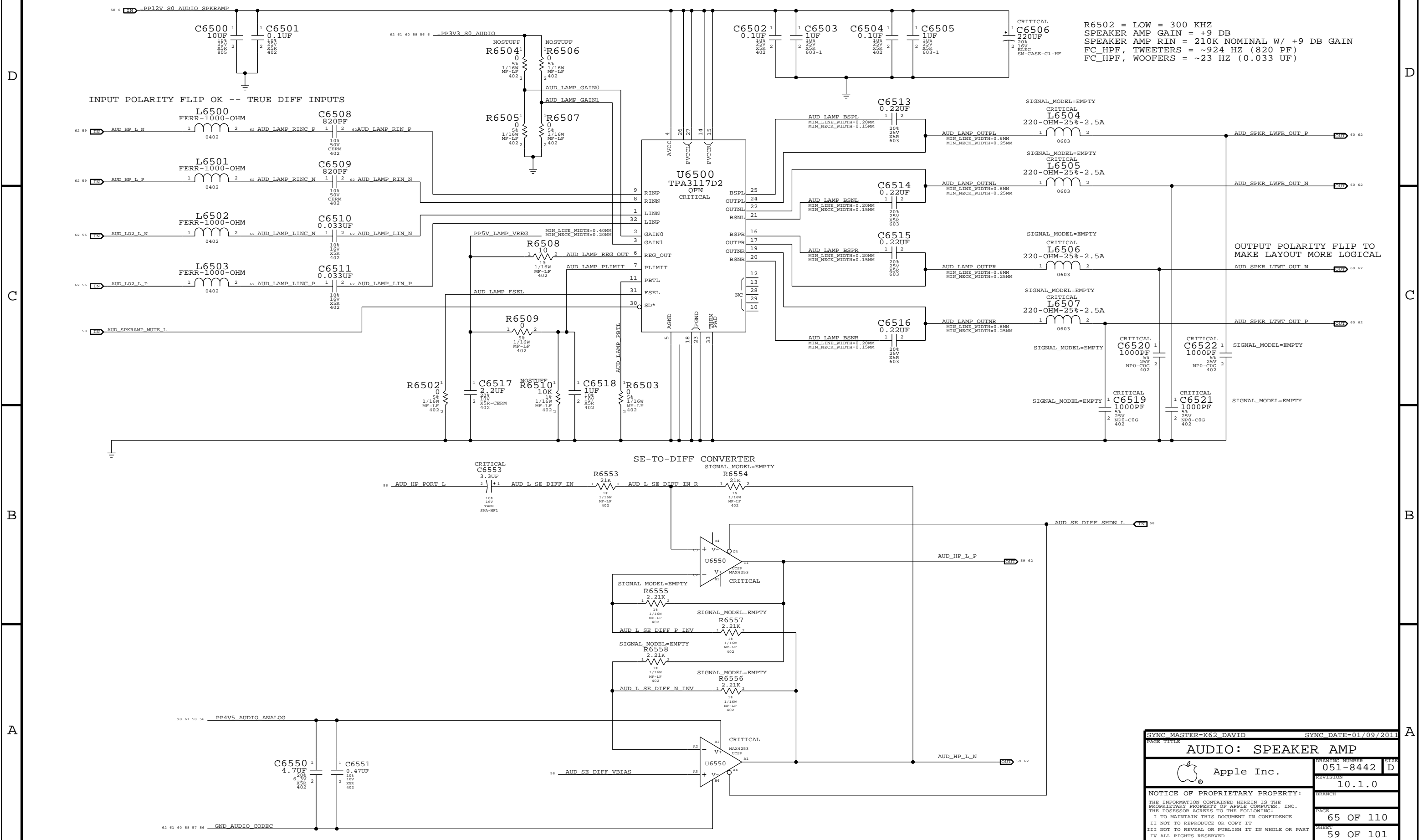


SYNC MASTER=K62 DAVID		SYNC DATE=01/09/2011	
PAGE TITLE			
AUDIO: FILTER/BUFFER			
 Apple Inc.		DRAWING NUMBER	
		051-8442	
		SIZE	
		D	
		REVISION	
		10.1.0	
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RIGHT CH SPEAKER AMP
APPLE P/N 353S3069

PAGE TITLE		PAGE NUMBER	
AUDIO: SPEAKER AMP_1		051-8442	
Apple Inc.		10.1.0	
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LEFT CH SPEAKER AMP
APPLE P/N 353S3069



INTERNAL MIC CON
APPLE P/N 518S0677

SPEAKER CABLE CONNECTORS

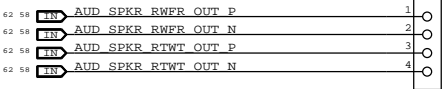
APPLE P/N 518S0748
APPLE P/N 518S0656

PROPERTIES FOR ALL SPKR NETS

CRITICAL

J6602
78048-0473
M-RT-SM

WOOFER (BR)
TWEETER (FR)

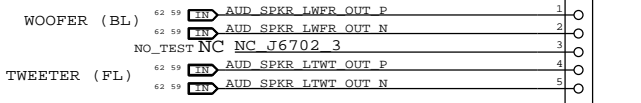


PROPERTIES FOR ALL SPKR NETS

CRITICAL

J6603
78048-0573
M-RT-SM

WOOFER (BL)
TWEETER (FL)



REMOTE I/O CONNECTOR

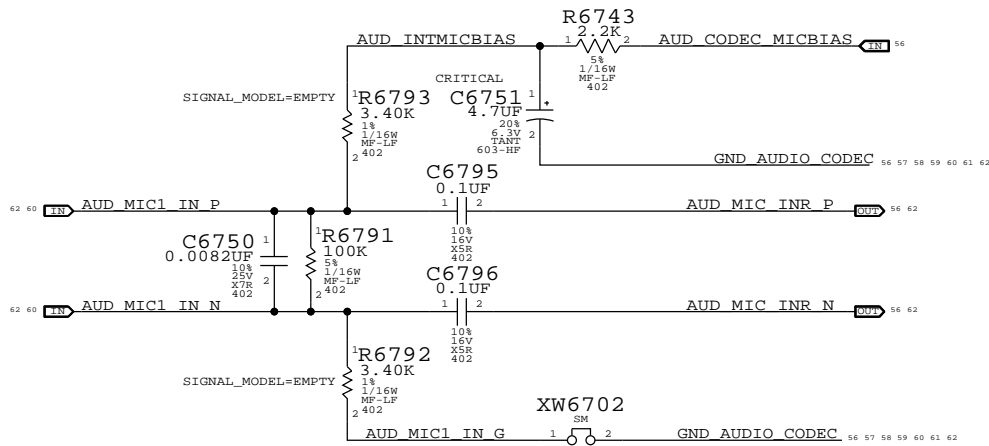
APPLE P/N 518S0723

CRITICAL
J6600
20143-020E-20F
P-RT-SM

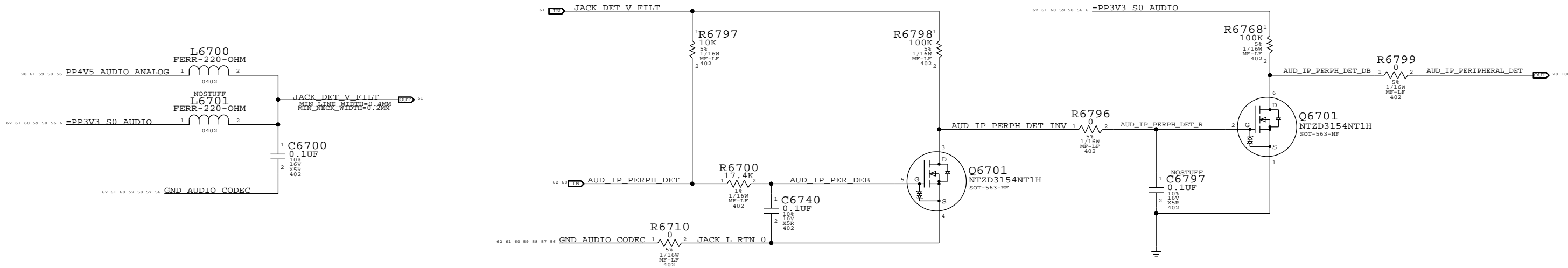
AUD SPDIFIN JACK
PP3V3 AUDIO SPDIF JACK
AUD LI_DET JACK
AUD LI GND JACK
AUD LI R JACK
AUD LI L JACK
AUD GND_DET JACK
HS MIC HI JACK
AUD HP GND JACK
AUD HP L JACK
AUD HP GND JACK
AUD HP R JACK
AUD HP TYPEDET JACK
AUD IP PERPH JACK
AUD HP TIPDET JACK
PP3V3 AUDIO SPDIF JACK

PAGE TITLE		SYNC DATE=01/09/2011	
Audio: MLB to I/O Conn.		Drawing NUMBER	
Apple Inc.		051-8442	
REVISION		SIZE	
10.1.0		D	
BRANCH		PAGE	
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Internal Microphone Impedance Matching



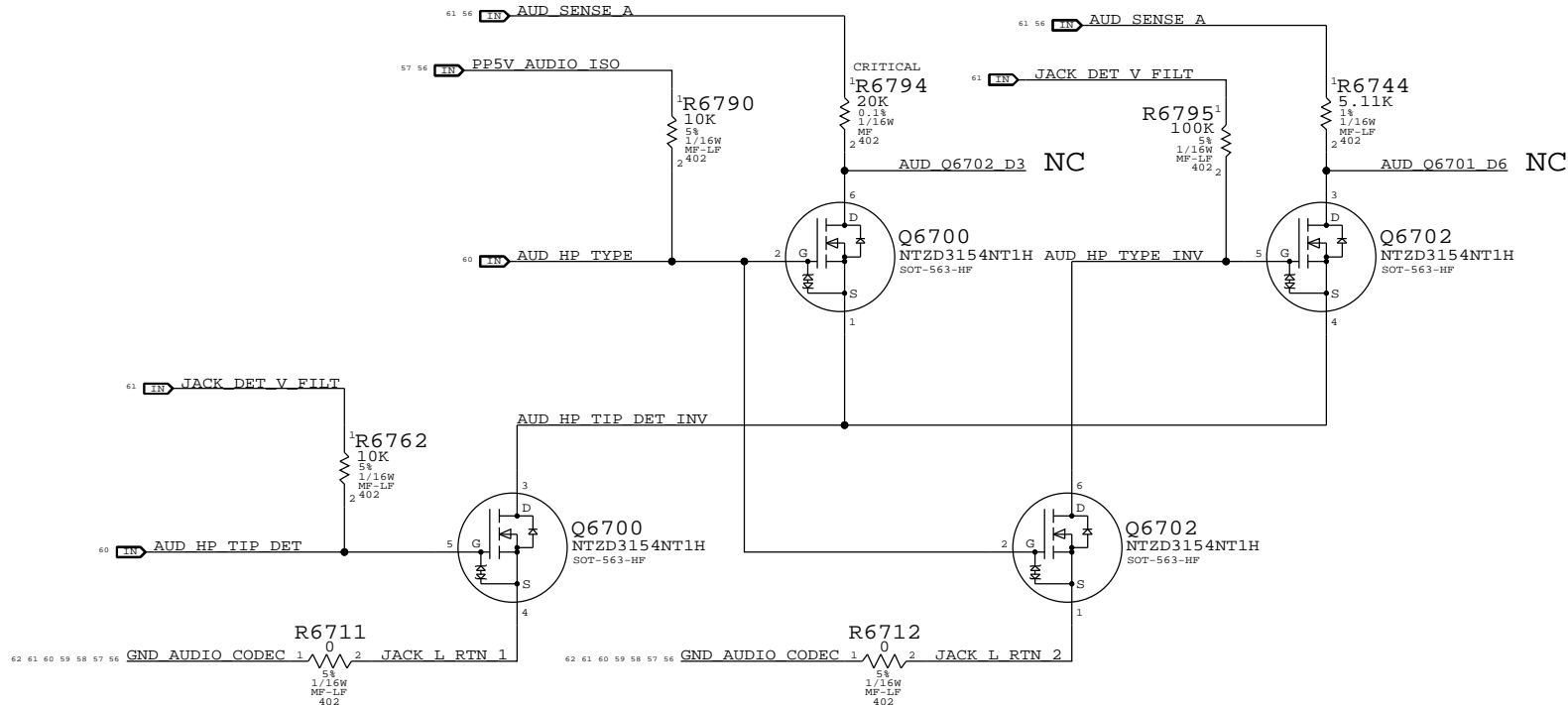
IPHS HS Detect Debounce CKT



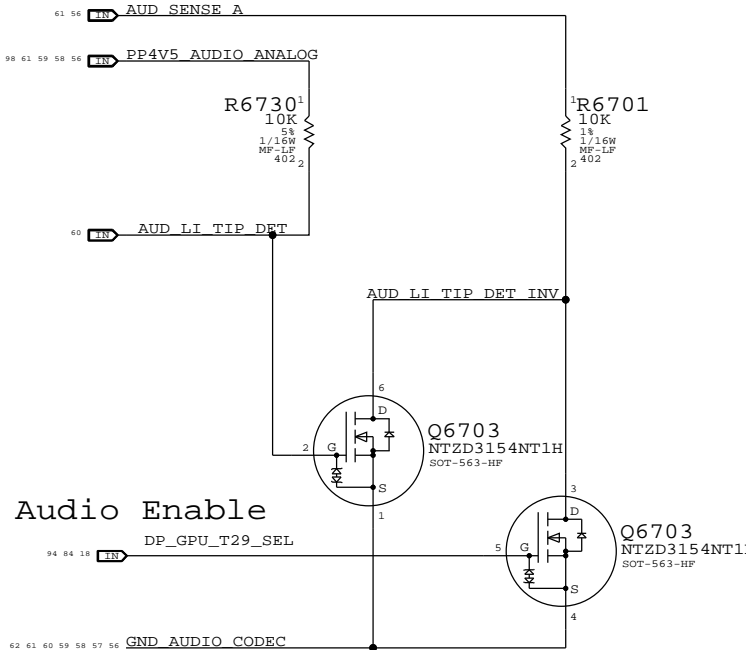
Digital Out (DETECT B)


Headphone Out (DETECT D)

LI Insert Detect (DETECT C)



DP Audio Enable



SYNC MASTER=K62 DAVID		SYNC DATE=01/09/2011	
PAGE TITLE			
AUDIO: Detects/Grounding			
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		SIZE	D
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		BRANCH	
		PAGE	67 OF 110
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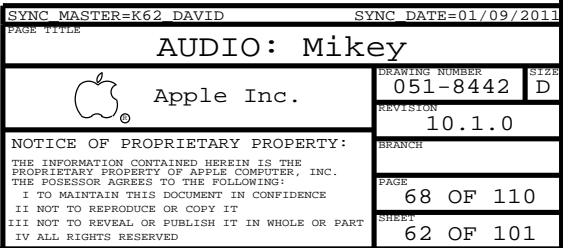
FUNCTION	VOLUME/MUTE	CONVERTER	PIN	COMPLEX	SHDN	DET ASSIGNMENT
HP/LINE OUT	0X03 (3)	0X03 (3)	0X0A (10,D)		GPIO_2	0X0A (D)
PRIMARY SPKRS (WFR)	0X04 (4)	0X04 (4)	0X0B (11)		GPIO_3	N/A
SECONDARY SPKRS (TWT)	0X02 (2)	0X02 (2)	0X09 (09)		GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0x10 (16)		N/A	0X0D (B)

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIODIFF	*	Y	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
SPKROUTDIFF	*	Y	0.6 MM	0.25 MM	10 MM	0.2 MM	0.2 MM

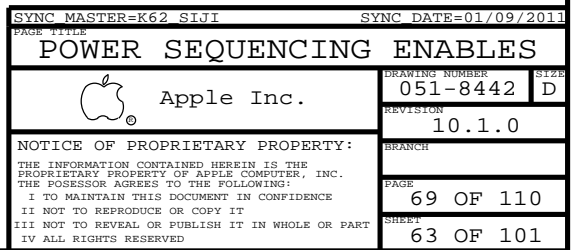
ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
E219	AUDIO DIFFERENTIAL	AUDIO	AUD_HP_L_P
E220	AUDIO DIFFERENTIAL	AUDIO	AUD_HP_L_N
E221	AUDIO DIFFERENTIAL	AUDIO	AUD_HP_R_P
E222	AUDIO DIFFERENTIAL	AUDIO	AUD_HP_R_N
E223	AUDIO DIFFERENTIAL	AUDIO	AUD_LO1_L_P
E224	AUDIO DIFFERENTIAL	AUDIO	AUD_LO1_L_N
E225	AUDIO DIFFERENTIAL	AUDIO	AUD_LO1_R_P
E226	AUDIO DIFFERENTIAL	AUDIO	AUD_LO1_R_N
E227	AUDIO DIFFERENTIAL	AUDIO	AUD_LO2_L_P
E228	AUDIO DIFFERENTIAL	AUDIO	AUD_LO2_L_N
E229	AUDIO DIFFERENTIAL	AUDIO	AUD_LO2_R_P
E230	AUDIO DIFFERENTIAL	AUDIO	AUD_LO2_R_N
E231	AUDIO DIFFERENTIAL	AUDIO	AUD_RAMP_LINC_P
E232	AUDIO DIFFERENTIAL	AUDIO	AUD_RAMP_LINC_N
E233	AUDIO DIFFERENTIAL	AUDIO	AUD_RAMP_RINC_P
E234	AUDIO DIFFERENTIAL	AUDIO	AUD_RAMP_RINC_N
E235	AUDIO DIFFERENTIAL	AUDIO	AUD_RAMP_LIN_P
E236	AUDIO DIFFERENTIAL	AUDIO	AUD_RAMP_LIN_N
E237	AUDIO DIFFERENTIAL	AUDIO	AUD_RAMP_RIN_P
E238	AUDIO DIFFERENTIAL	AUDIO	AUD_RAMP_RIN_N
E239	AUDIO DIFFERENTIAL	AUDIO	AUD_LAMP_LINC_P
E240	AUDIO DIFFERENTIAL	AUDIO	AUD_LAMP_LINC_N
E241	AUDIO DIFFERENTIAL	AUDIO	AUD_LAMP_RINC_P
E242	AUDIO DIFFERENTIAL	AUDIO	AUD_LAMP_RINC_N
E243	AUDIO DIFFERENTIAL	AUDIO	AUD_LAMP_LIN_P
E244	AUDIO DIFFERENTIAL	AUDIO	AUD_LAMP_LIN_N
E245	AUDIO DIFFERENTIAL	AUDIO	AUD_LAMP_RIN_P
E246	AUDIO DIFFERENTIAL	AUDIO	AUD_LAMP_RIN_N
E247	AUDIO DIFFERENTIAL	AUDIO	AUD_LO1_L_C_P
E248	AUDIO DIFFERENTIAL	AUDIO	AUD_LO1_L_C_N
E249	AUDIO DIFFERENTIAL	AUDIO	AUD_LO1_R_C_P
E250	AUDIO DIFFERENTIAL	AUDIO	AUD_LO1_R_C_N
E251	AUDIO DIFFERENTIAL	AUDIO	MAX97220_INL_P
E252	AUDIO DIFFERENTIAL	AUDIO	MAX97220_INL_N
E253	AUDIO DIFFERENTIAL	AUDIO	MAX97220_INR_P
E254	AUDIO DIFFERENTIAL	AUDIO	MAX97220_INR_N
E255	SERVOOUT DIFFERENTIAL	SERVOOUT	AUD_SPKR_RWFR_OUT_P
E256	SERVOOUT DIFFERENTIAL	SERVOOUT	AUD_SPKR_RWFR_OUT_N
E257	SERVOOUT DIFFERENTIAL	SERVOOUT	AUD_SPKR_STWT_OUT_P
E258	SERVOOUT DIFFERENTIAL	SERVOOUT	AUD_SPKR_STWT_OUT_N
E259	SERVOOUT DIFFERENTIAL	SERVOOUT	AUD_SPKR_LMFR_OUT_P
E260	SERVOOUT DIFFERENTIAL	SERVOOUT	AUD_SPKR_LMFR_OUT_N
E261	SERVOOUT DIFFERENTIAL	SERVOOUT	AUD_SPKR_LTWY_OUT_P
E262	SERVOOUT DIFFERENTIAL	SERVOOUT	AUD_SPKR_LTWY_OUT_N
E263	AUDIO DIFFERENTIAL	AUDIO	AUD_MIC1_IN_P
E264	AUDIO DIFFERENTIAL	AUDIO	AUD_MIC1_IN_N
E265	AUDIO DIFFERENTIAL	AUDIO	AUD_MIC_INR_P
E266	AUDIO DIFFERENTIAL	AUDIO	AUD_MIC_INR_N
E267	AUDIO DIFFERENTIAL	AUDIO	AUD_MIC_IN1_CONN_P
E268	AUDIO DIFFERENTIAL	AUDIO	AUD_MIC_IN1_CONN_N

FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
LINE IN	0X05 (5)	0X12 (12,C)	N/A	0X12 (C)
SPDIF IN	0X07 (7)	0x0F (15)	N/A	N/A
INTERNAL MIC	0X06 (6)	0X0E (14,LEFT & RIGHT)	N/A	N/A
EXTERNAL MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	COUGAR POINT GPIO 16	COUGAR POINT GPIO 5 (RCVR INT), COUGAR POINT GPIO 3 (PERIPH DET)

WRITE: 0X72 READ: 0X73 APN 353S2640



A



D

C

B

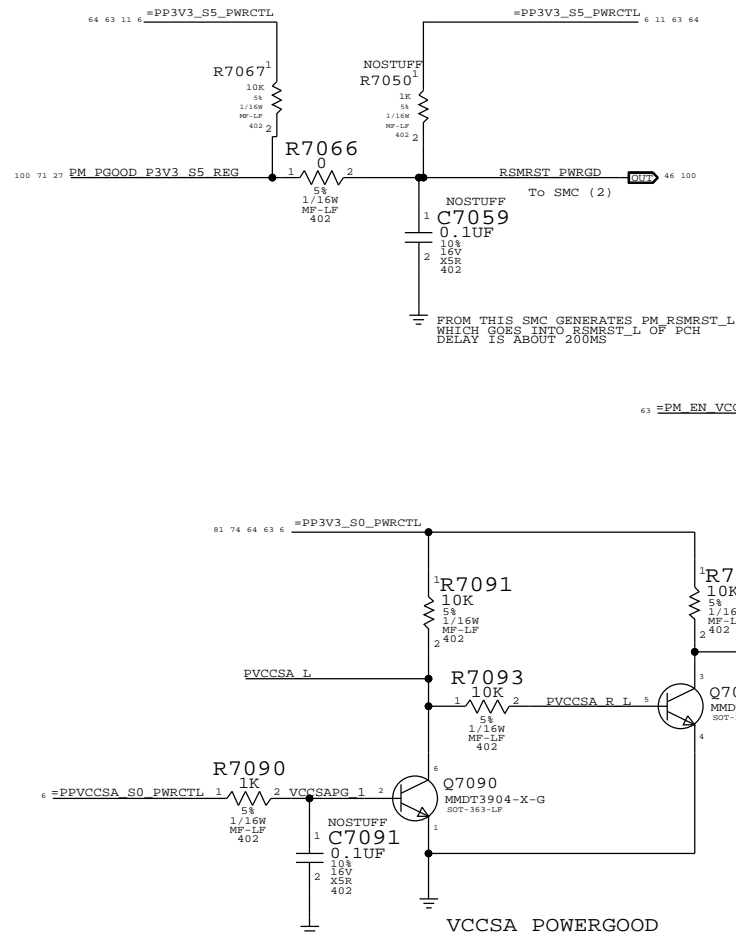
A

D

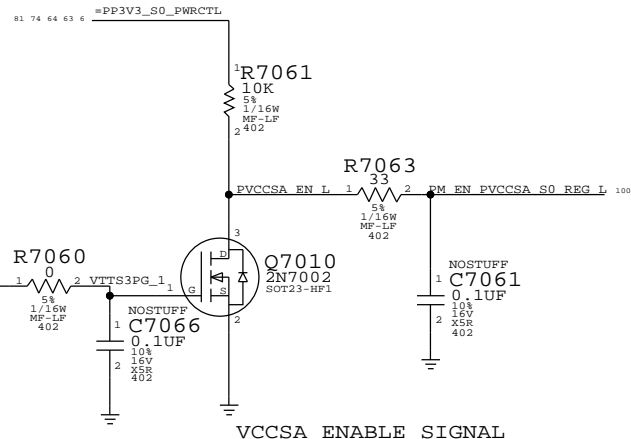
C

B

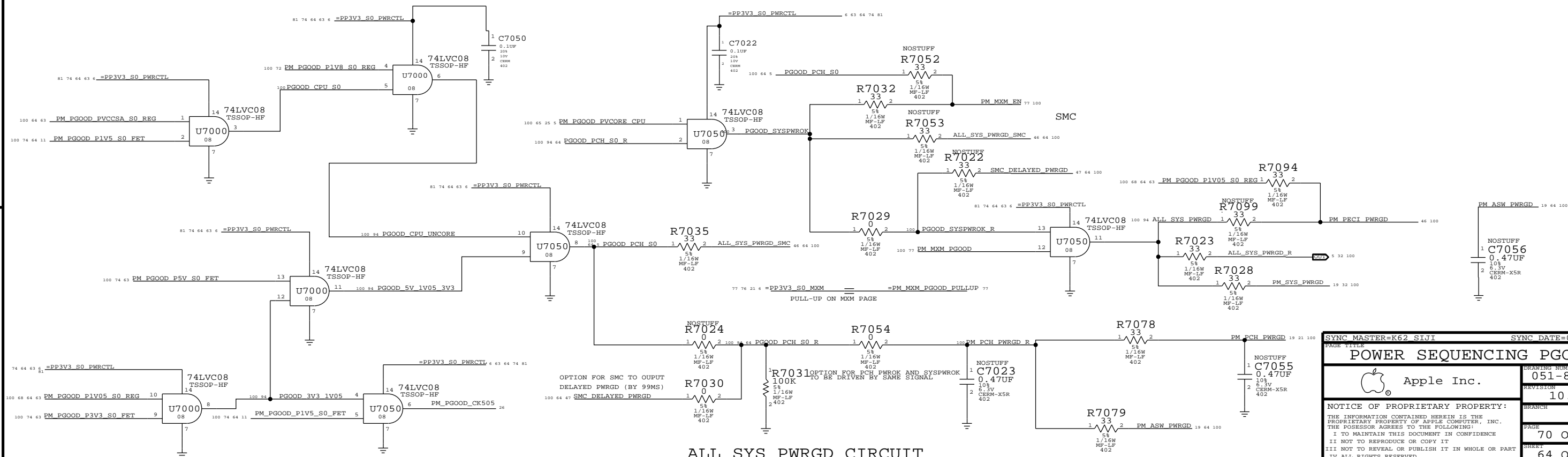
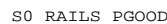
A |




VCCSA_POWERGOOD

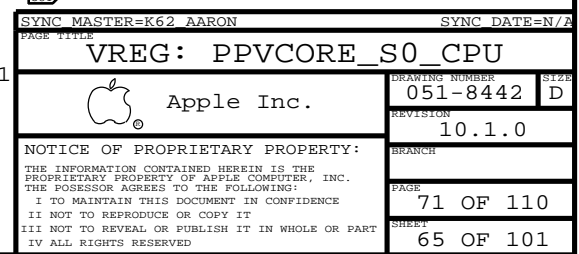


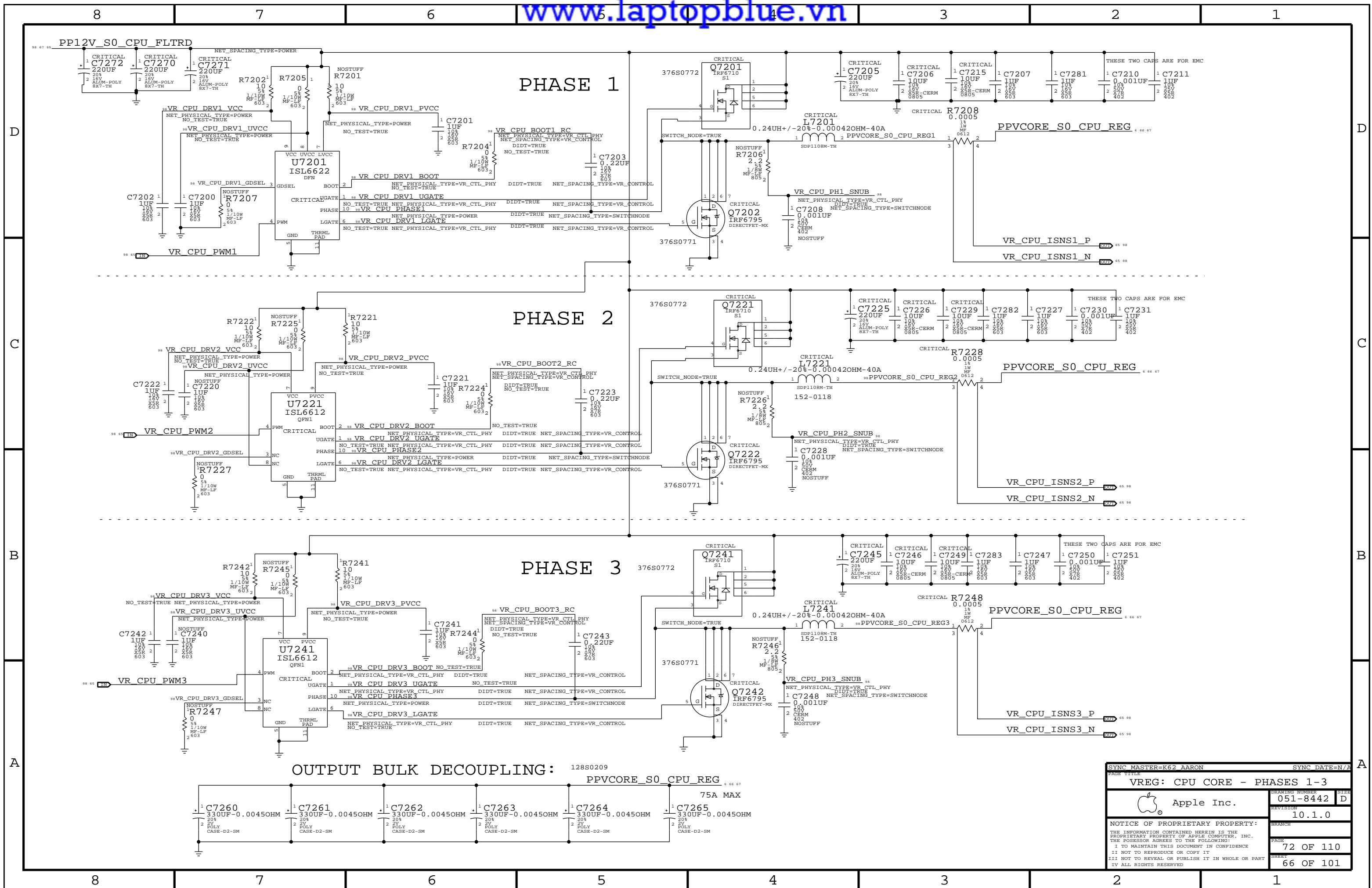
VCCSA ENABLE SIGNAL




ALL_SYS_PWRGD CIRCUIT

SYNCH MASTER-K62 SIJI		SYNCH DATE=01/09/2011	
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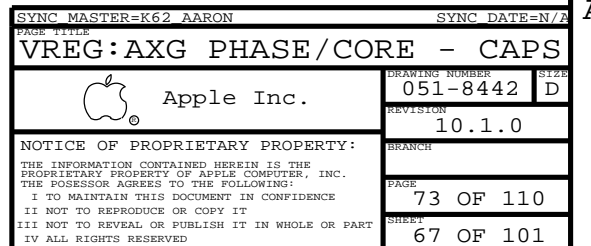


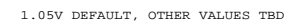


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PAGE TITLE			
VREG: CPU CORE - PHASES 1-3			
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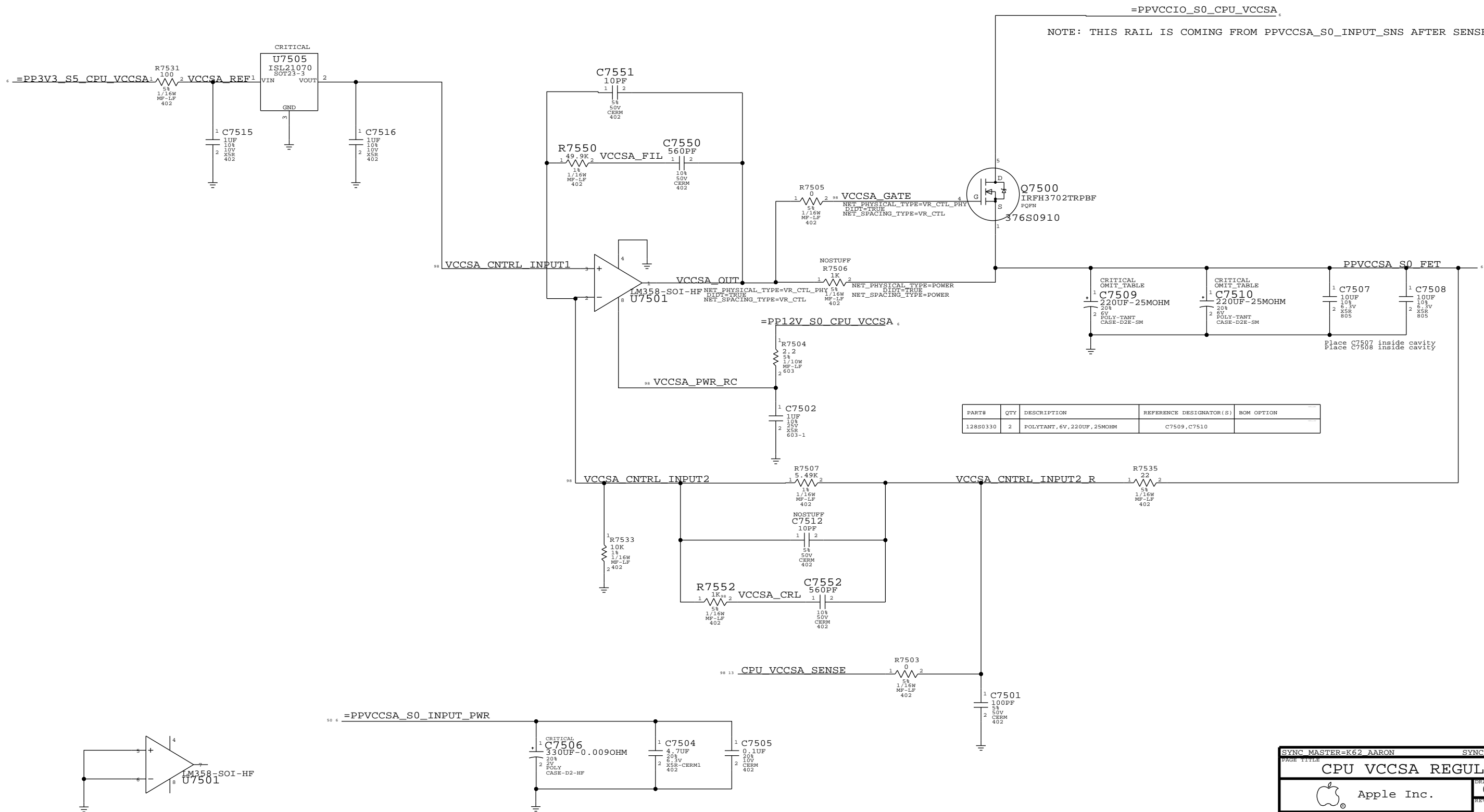
AXG PHASE (MAX 15A)






VID<3:0>	Voltage
0000	+1.100V
0011	+1.050V

CPU VCCSA 0.925V (8.8A MAX)



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
128S0330	2	POLYTANT, 6V, 220UF, 25MOHM	C7509, C7510	

SYNC MASTER=K62 AARON		SYNC DATE=12/08/2009	
PAGE TITLE			
CPU VCCSA REGULATOR			
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3V3 S5 REGULATOR


5V S3 REGULATOR

Power Rating ?

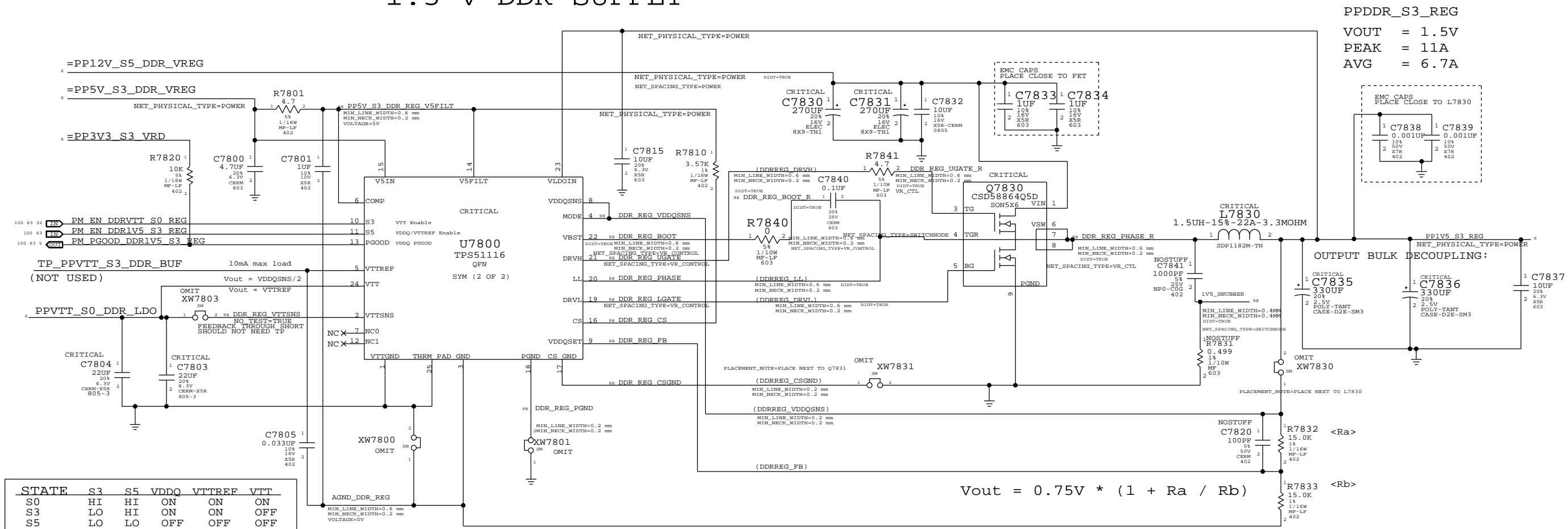
5V OUTPUT

OUTPUT BULK DECOUPLING:

$$V_{out} = 0.6V * (1 + R_a / R_b)$$

SYNC MASTER=K62 AARON		SYNC DATE=12/08/2009	
PAGE TITLE			
5V_S3 / 3V3_S5 VREGS			
 Apple Inc.		DRAWING NUMBER	051-8442
		SIZE	D
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1.5 V DDR SUPPLY

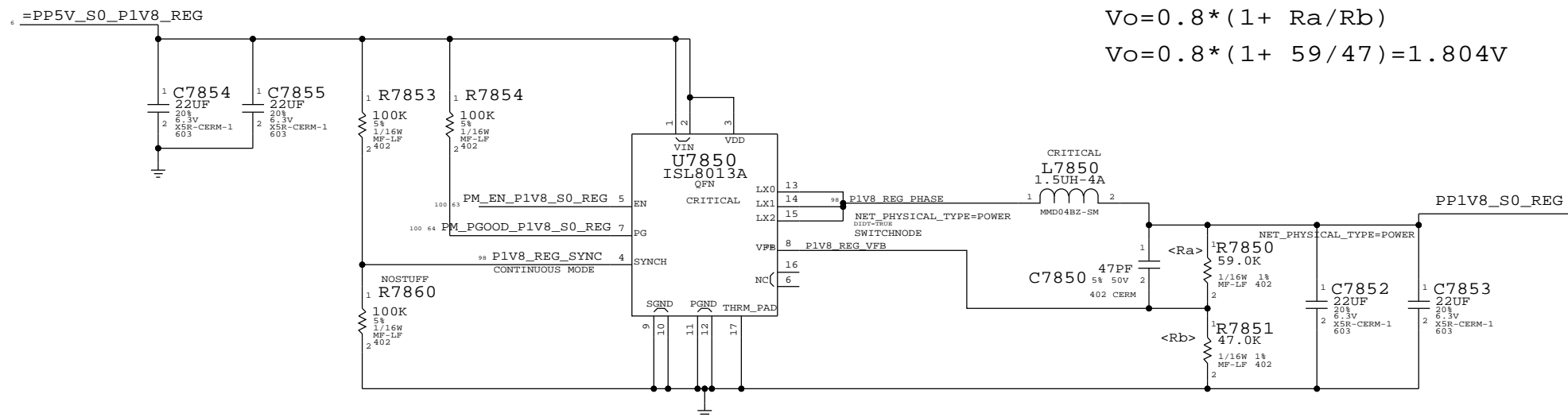



1.8 V SUPPLY

1A Average current

$$V_o = 0.8 * (1 + R_a / R_b)$$

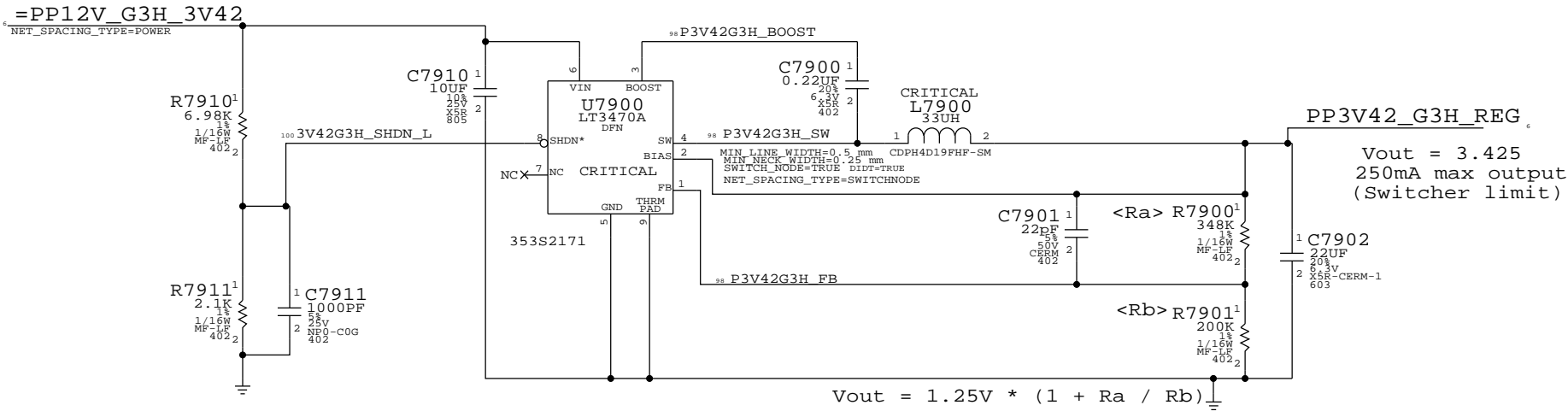
$$V_o = 0.8 * (1 + 59 / 47) = 1.804V$$

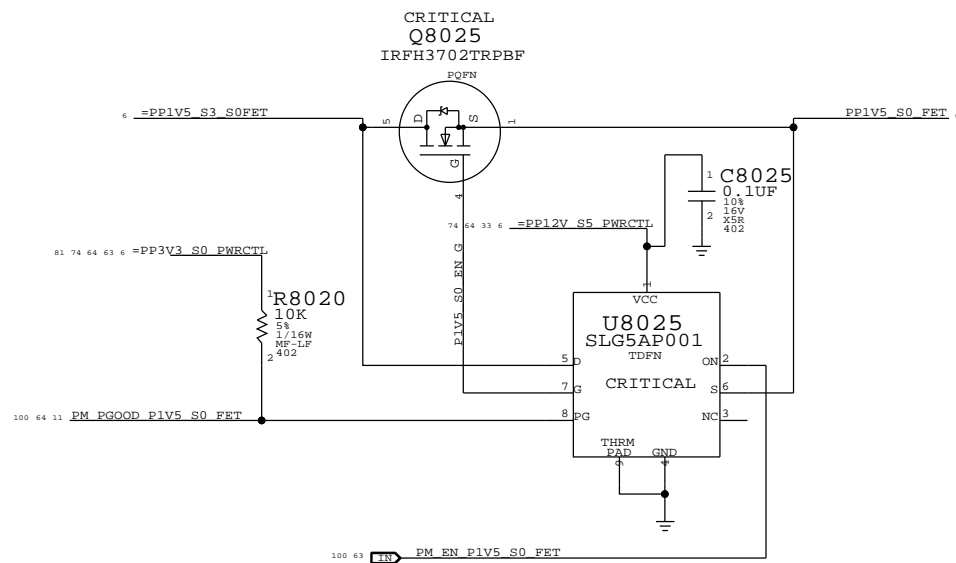
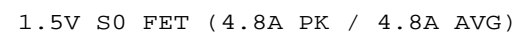
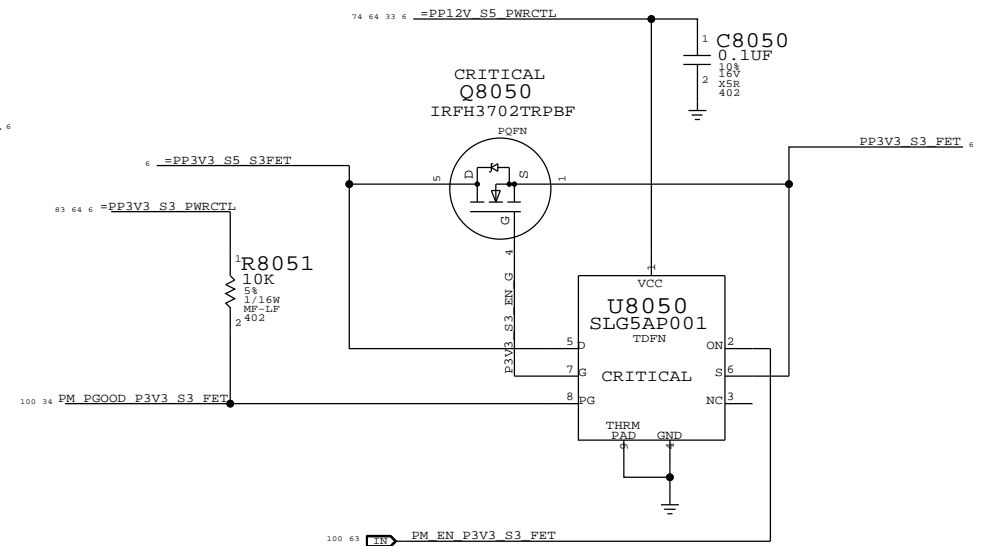
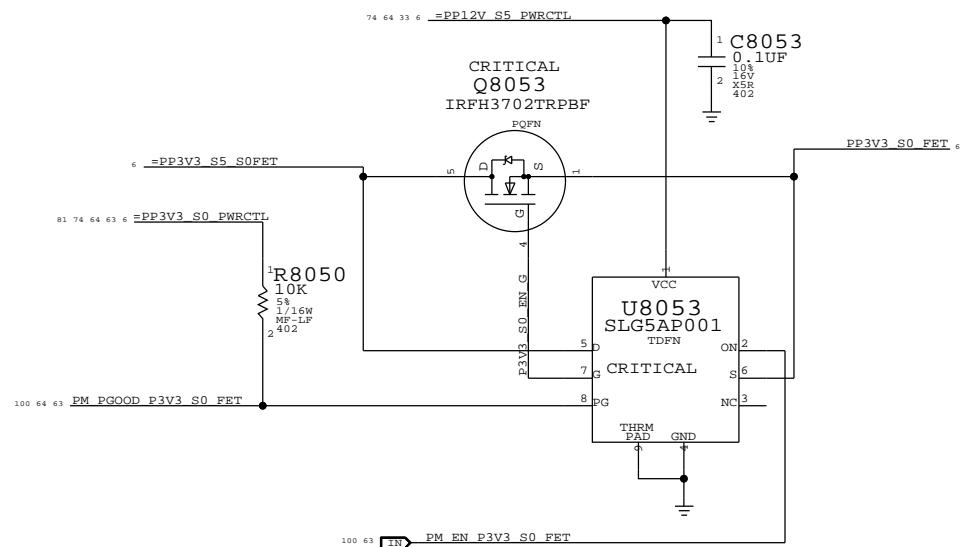
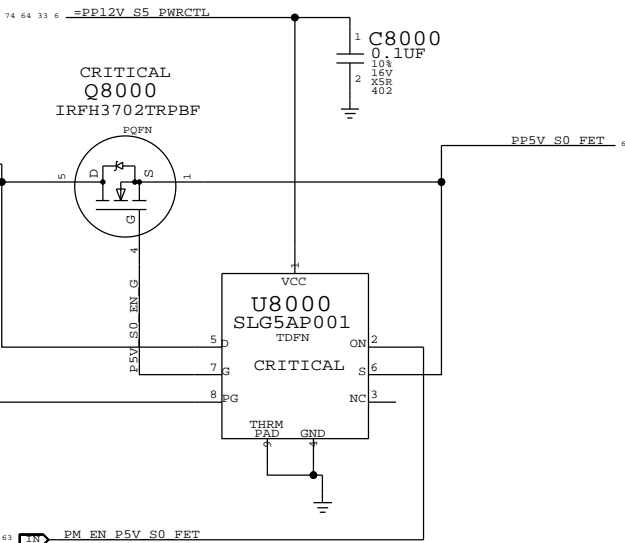
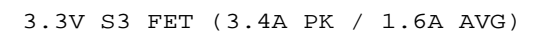
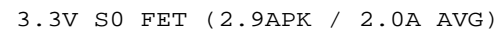
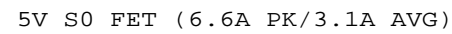


SYNC MASTER=K62 AARON		SYNC DATE=11/30/2009	
PAGE TITLE			
1.5V / 1.8V VREGS			
 Apple Inc.	DRAWING NUMBER	051-8442	SIZE
	REVISION	10.1.0	
	BRANCH		
	PAGE	78 OF 110	
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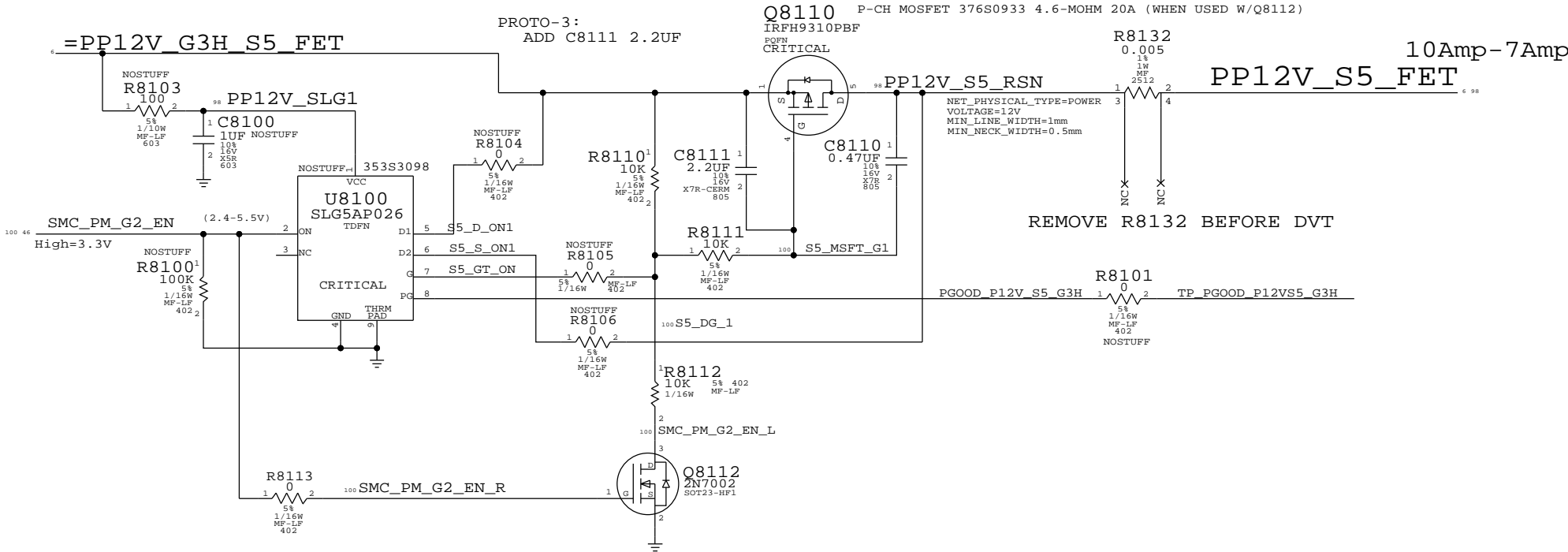
3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator





THE NMOS PMOS SHARING FOOTPRINT WILL NOT WORK DUE TO THE REVERSE POLARITY OF BODY DIODE.

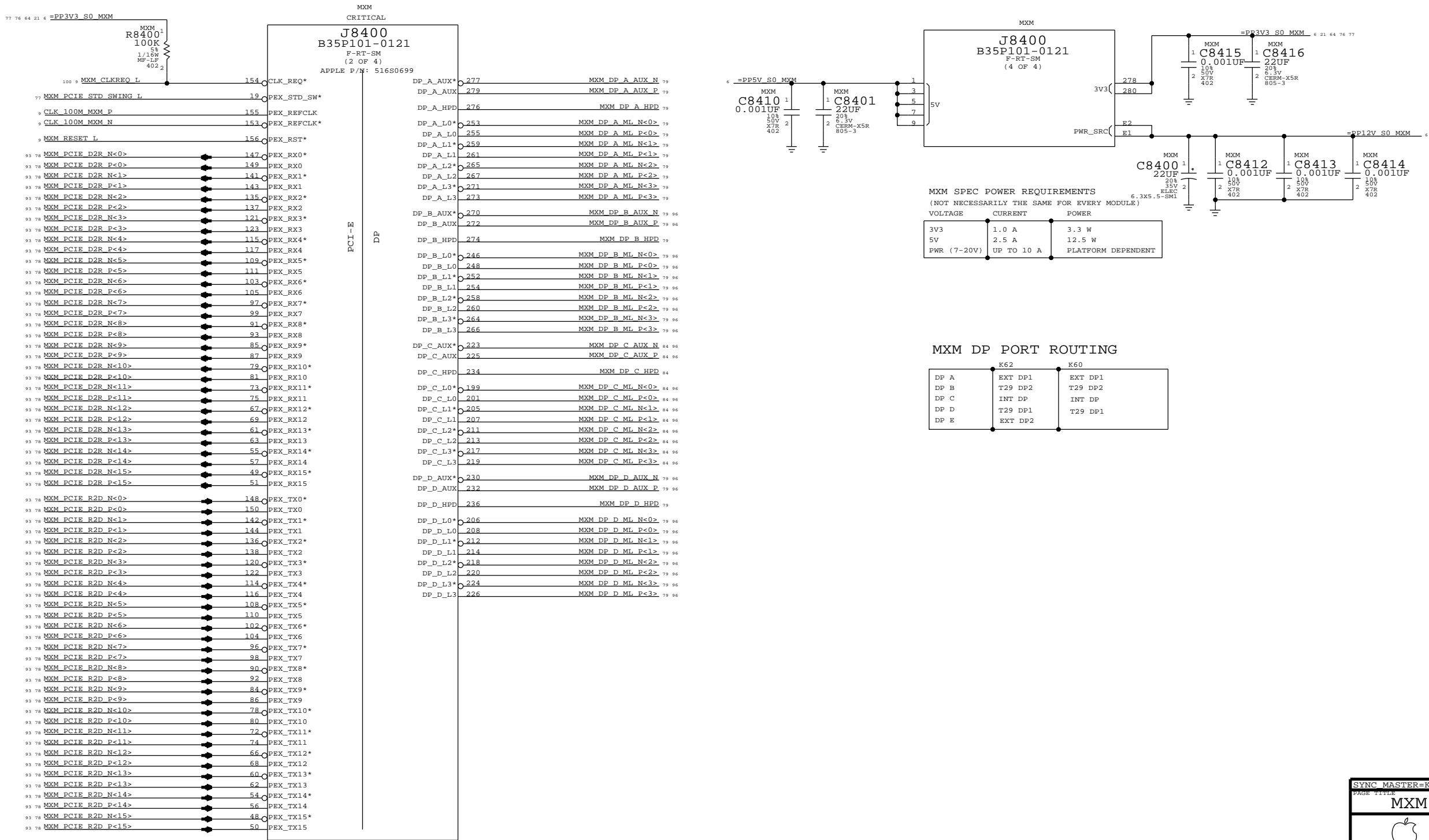


Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM
- =PP5V_S0_MXM
- =PPV_S0_MXM_PWRSRC


Signal aliases required by this page:
(NONE)


BOM options provided by this page:
- MXM



BOM options provided by this page:



8	7	6	5	4	3	2	1		
MXM TX CAPS				MXM RX CAPS					
D	93	9	15	PEG_R2D_C_P<0>	MXM C8600 0.1UF 1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<15>	93 76 93	
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	PAGE TITLE MXM PCIE CAPS								
	 Apple Inc.				DRAWING NUMBER 051-8442		SIZE D		
					REVISION 10.1.0				
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8	7	6	5	4	3	2	1		

SYNC MASTER=K62		SYNC DATE=N/A	
PAGE TITLE			
MXM PCIE CAPS			
 Apple Inc.		DRAWING NUMBER	051-8442
		REVISION	10.1.0
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		PAGE	86 OF 110
		SHEET	78 OF 101

Power aliases required by this page:

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

76	<u>MXM DP A ML P<0..3></u>	==	DP EXTA ML C P<0..3>	85	96
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76	<u>MXM DP A ML N<0..3></u>	==	DP EXTA ML C N<0..3>	85	96
			MAKE_BASE=TRUE NO_TEST=TRUE		
76	<u>MXM DP A AUX P</u>	==	DP EXTA AUXCH C P	79	85 96
			MAKE_BASE=TRUE NO_TEST=TRUE		
76	<u>MXM DP A AUX N</u>	==	DP EXTA AUXCH C N	79	85 96
			MAKE_BASE=TRUE NO_TEST=TRUE		
76	<u>MXM DP A HPD</u>	==	DP EXTA HPD	85	
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77	<u>MXM DP E ML P<0..3></u>	==	DP EXTB ML C P<0..3>	87	96
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			MAKE_BASE=TRUE NO_TEST=TRUE		
77	<u>MXM DP E AUX P</u>	==	DP EXTB AUXCH C P	79	87 96
			MAKE_BASE=TRUE NO_TEST=TRUE		
77	<u>MXM DP E AUX N</u>	==	DP EXTB AUXCH C N	79	87 96
			MAKE_BASE=TRUE NO_TEST=TRUE		
77	<u>MXM DP E HPD</u>	==	DP EXTB HPD	87	
			MAKE_BASE=TRUE NO_TEST=TRUE		

95	65	79	<u>DP_EXTA_AUXCH_C_P</u>	<u>==</u>	<u>DP_EXTA_DDC_CLK</u>	85
			MAKE_BASE=TRUE			
95	65	79	<u>DP_EXTA_AUXCH_C_N</u>	<u>==</u>	<u>DP_EXTA_DDC_DATA</u>	85
			MAKE_BASE=TRUE			
96	67	79	<u>DP_EXTB_AUXCH_C_P</u>	<u>==</u>	<u>DP_EXTB_DDC_CLK</u>	87
			MAKE_BASE=TRUE			
96	67	79	<u>DP_EXTB_AUXCH_C_N</u>	<u>==</u>	<u>DP_EXTB_DDC_DATA</u>	87
			MAKE_BASE=TRUE			


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182	T29 A BIAS R2D N0	85.86	1802	T29 B BIAS R2D N2	87.88
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187	NO TEST=TRUE		1807	NO TEST=TRUE	
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189	NO TEST=TRUE		1809	T29 B BIAS P3	88
190	T29 A BIAS N0	86	1810	T29 B BIAS N2	88
191	NO TEST=TRUE		1811	T29 B BIAS N3	88
192	DP A BIAS P 0	85.86	1812	NO TEST=TRUE	
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194	DP A BIAS N 0	85.86	1814	DP B BIAS N 0	87.88
195	NO TEST=TRUE		1815	DP B BIAS P 2	87.88
196	DP A BIAS P 2	85.86	1816	DP B BIAS P 3	87.88
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200	DP A BIAS P 3	85.89	1820	DP B BIAS P 3	87
201	NO TEST=TRUE		1821	NO TEST=TRUE	

	=PP3V3 SW DPAPWR	==	PP3V3 SW DPAPWR	98	98
	=PP3V3 SW DPBPWR	==	PP3V3 SW DPBPWR	97	98
100	PCIE WAKE L	==	T29 WAKE L	95	97
96	MXM DP B ML P<0..3>	==	DP T29SNK1 ML C P<0..3> MAKE_BASE=TRUE NO_TEST=TRUE	99	99
96	MXM DP B ML N<0..3>	==	DP T29SNK1 ML C N<0..3> MAKE_BASE=TRUE NO_TEST=TRUE	99	99
96	MXM DP A AUX P	==	DP T29SNK1 AUXCH C P MAKE_BASE=TRUE NO_TEST=TRUE	99	99
96	MXM DP A AUX N	==	DP T29SNK1 AUXCH C N MAKE_BASE=TRUE NO_TEST=TRUE	99	99
76	MXM DP B HPD	==	DP T29SNK1 HPD MAKE_BASE=TRUE NO_TEST=TRUE	99	
96	MXM DP D ML P<0..3>	==	DP T29SNK0 ML C P<0..3> MAKE_BASE=TRUE NO_TEST=TRUE	99	99
96	MXM DP D ML N<0..3>	==	DP T29SNK0 ML C N<0..3> MAKE_BASE=TRUE NO_TEST=TRUE	99	99
96	MXM DP D AUX P	==	DP T29SNK0 AUXCH C P MAKE_BASE=TRUE NO_TEST=TRUE	99	99
96	MXM DP D AUX N	==	DP T29SNK0 AUXCH C N MAKE_BASE=TRUE NO_TEST=TRUE	99	99
76	MXM DP D HPD	==	DP T29SNK0 HPD MAKE_BASE=TRUE NO_TEST=TRUE	99	

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77. MXM_PNL_PWR_EN     == NC MXM_PNL_PWR_EN
    MAKE_BASE=TRUE    NO_TEST=TRUE
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96 77	<u>MMX LVDS B CLK N</u>	==	NC MMX LVDS B CLK N	==	MAKE BASE=TRUE	NO TEST=TRUE
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96 77	<u>MMX LVDS B DATA P<1></u>	==	NC MMX LVDS B DATA P<1>	==	MAKE BASE=TRUE	NO TEST=TRUE
96 77	<u>MMX LVDS B DATA N<2></u>	==	NC MMX LVDS B DATA N<2>	==	MAKE BASE=TRUE	NO TEST=TRUE
96 77	<u>MMX LVDS B DATA P<2></u>	==	NC MMX LVDS B DATA P<2>	==	MAKE BASE=TRUE	NO TEST=TRUE
96 77	<u>MMX LVDS B DATA N<3></u>	==	NC MMX LVDS B DATA N<3>	==	MAKE BASE=TRUE	NO TEST=TRUE
96 77	<u>MMX LVDS B DATA P<3></u>	==	NC MMX LVDS B DATA P<3>	==	MAKE BASE=TRUE	NO TEST=TRUE

SYNC MASTER=K62 AARON		SYNC DATE=N/A	
PAGE TITLE			
DP ALIAS			
	Apple Inc.		DRAWING NUMBER 051-8442
			SIZE D
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GreenCLK Implementation Notes:

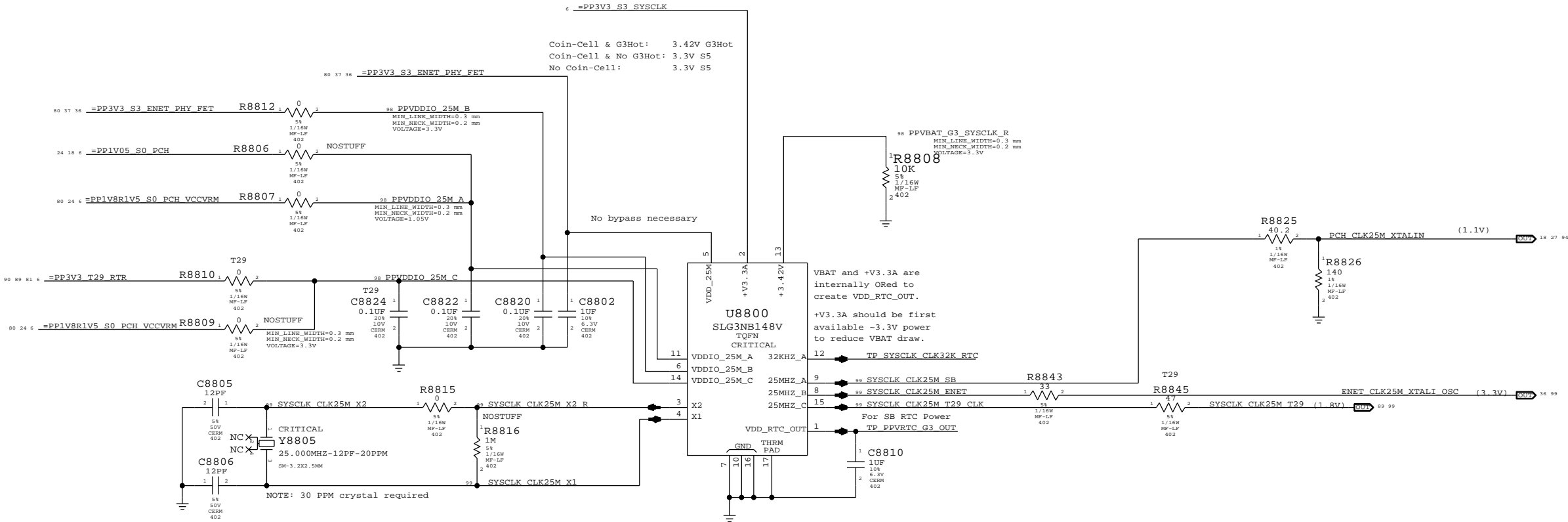
VBAT: Alias as appropriate (see note below & Desktop Example)
+V3.3A: Alias as appropriate (see note below)
VDD_25M: 3.3V matching 'highest' VDDIO power state (ENET)

VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Ethernet power rail for XTAL circuit.
VDDIO_25M_C: T29 power rail for XTAL circuit.

NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.

For Cougar Point Desktop: VDDIO = VCCVRM (1.8V), Vclk = 1.1V Max, Divider: 604 / 1000
For Cougar Point Mobile: VDDIO = VCCVRM (1.5V), Vclk = 1.1V Max, Divider: 332 / 1000
For Caesar-IV (BCM57765): VDDIO = XTALVDDH (3.3V), Vclk = 3.3V Max. No Divider Necessary

System RTC Power Source & 32kHz / 25MHz Clock Generator



Page Notes

Power aliases required by this page:

- =PP3V3_T29_P3V3T29FET (3.3V FET Input)
- =PP3V3_T29_FET (3.3V FET Output)
- =PP3V3_S0_T29PWRCTL
- =PP1V05_T29_P1V05T29FET (1.05V FET Input)
- =PP1V05_T29_FET (1.05V FET Output)

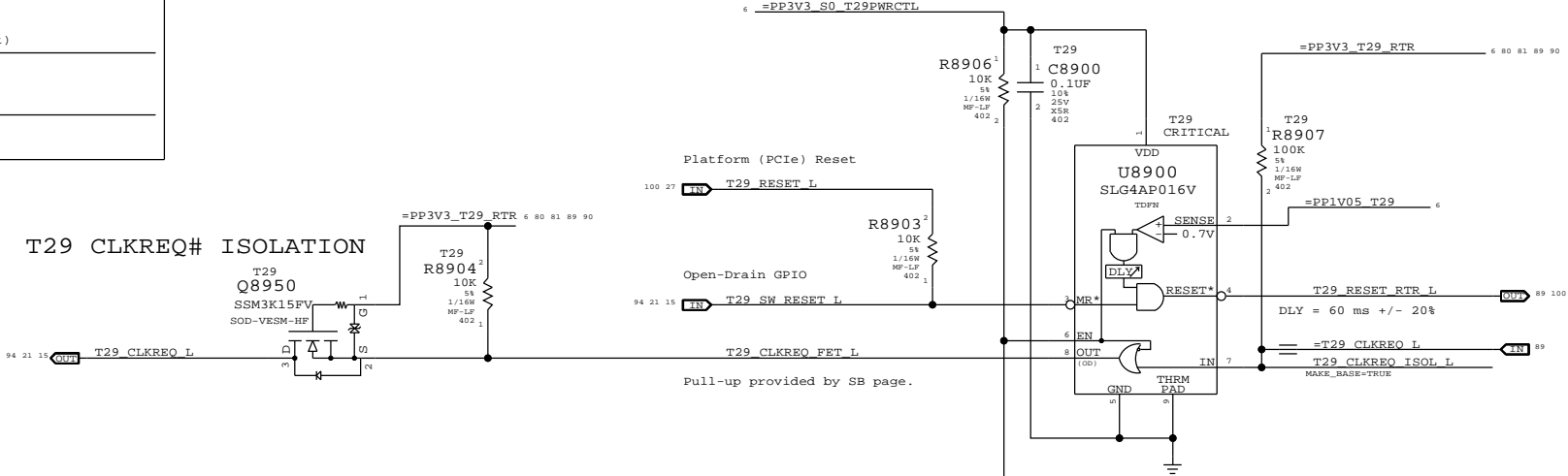
Signal aliases required by this page:

- =T29_CLKREQ_L
- T29_RESET_L

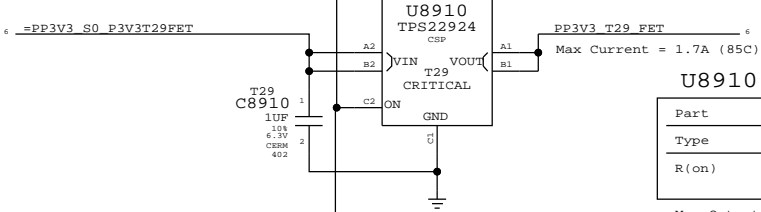
BOM options provided by this page:

(NONE)

Supervisor & CLKREQ# Isolation

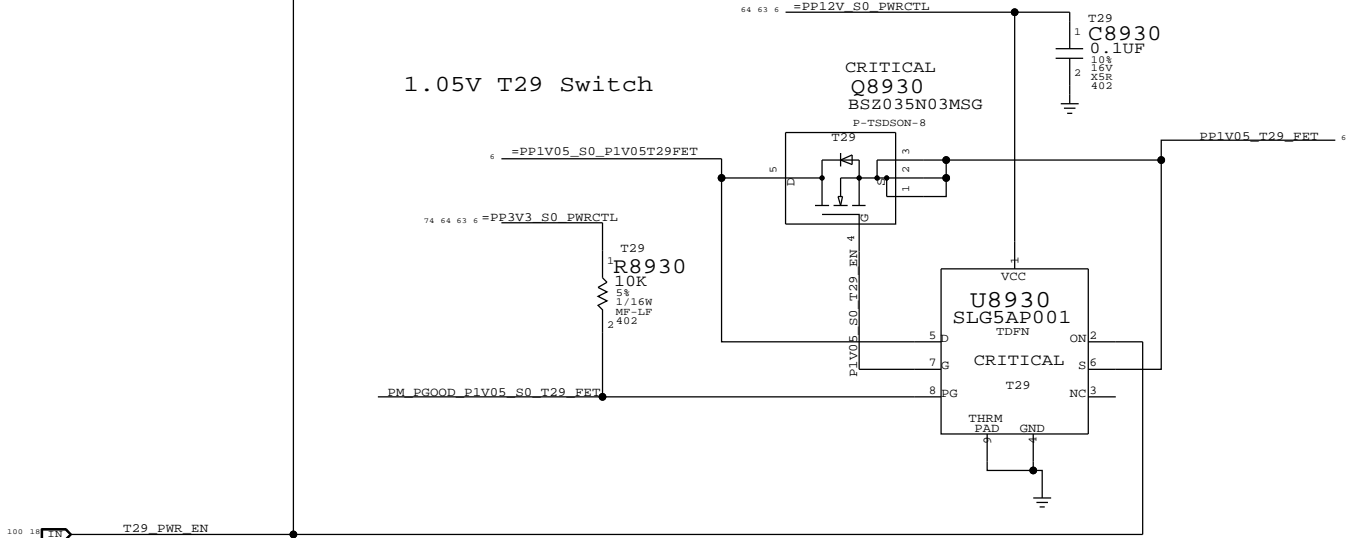


3.3V T29 Switch



Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ
	50 mOhm Max

1.05V T29 Switch



Page Notes

Power aliases required by this page:

- =PP12V_S0_LCD
- =PP3V3_S0_VIDEO

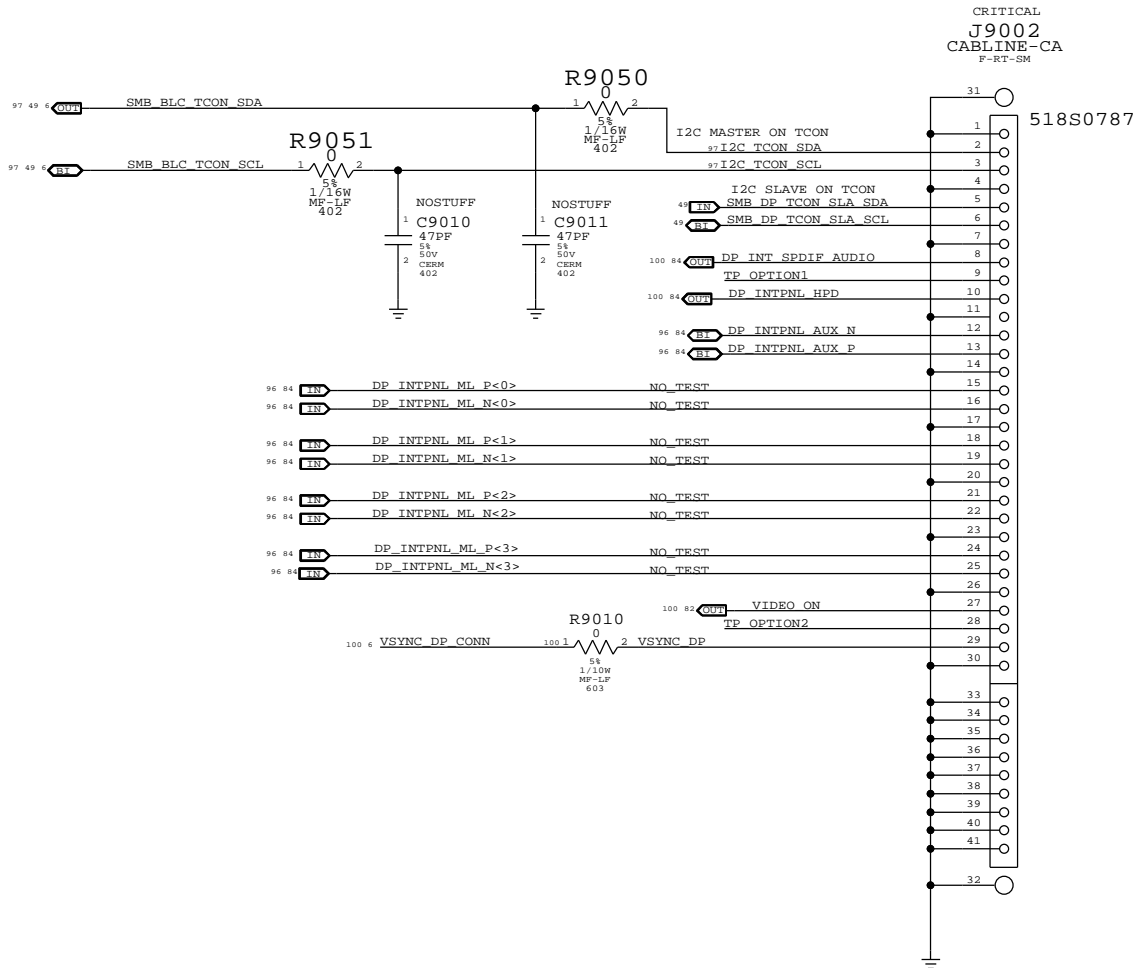
Signal aliases required by this page:

(NONE)

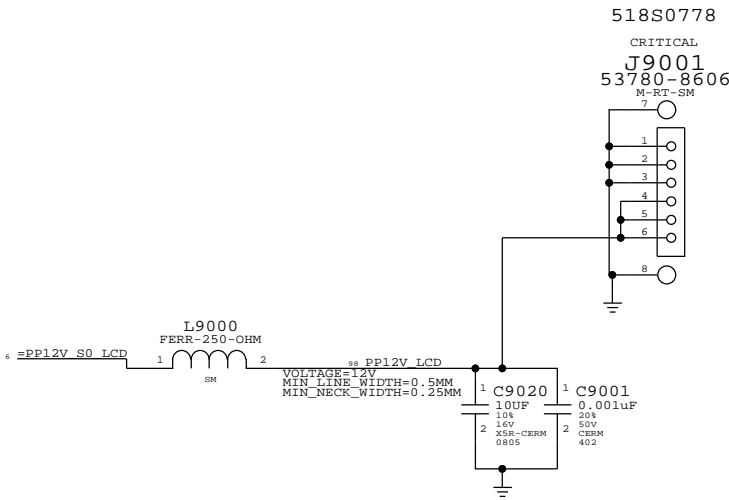
BOM options provided by this page:

IG, MXM, MLB_PNL_PWR, LCD_PNL_PWR

INTERNAL DP INTERFACE

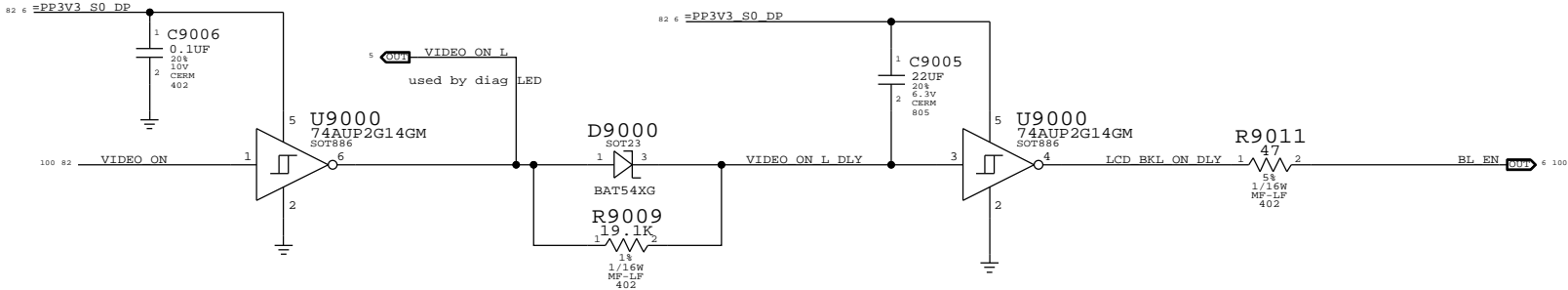



INTERNAL DP POWER



BACKLIGHT CONTROL SUPPORT

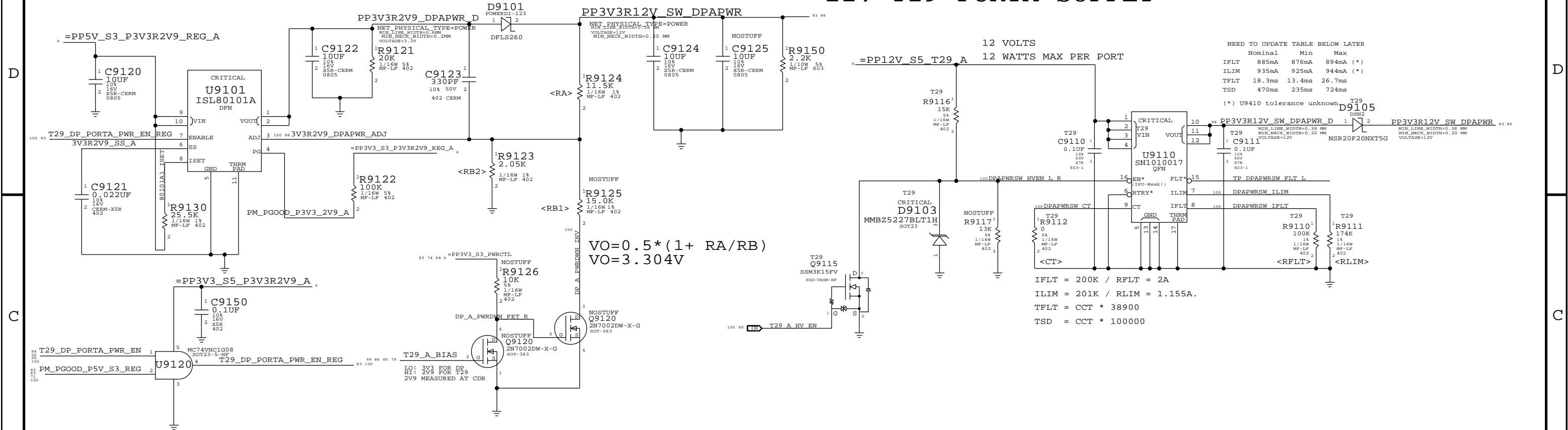
guarantee backlight is
only on when Panel has valid video



SYNC MASTER=K62 AARON		SYNC DATE=N/A	
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Display: Int DP Connector			
 Apple Inc.		DRAWING NUMBER	051-8442
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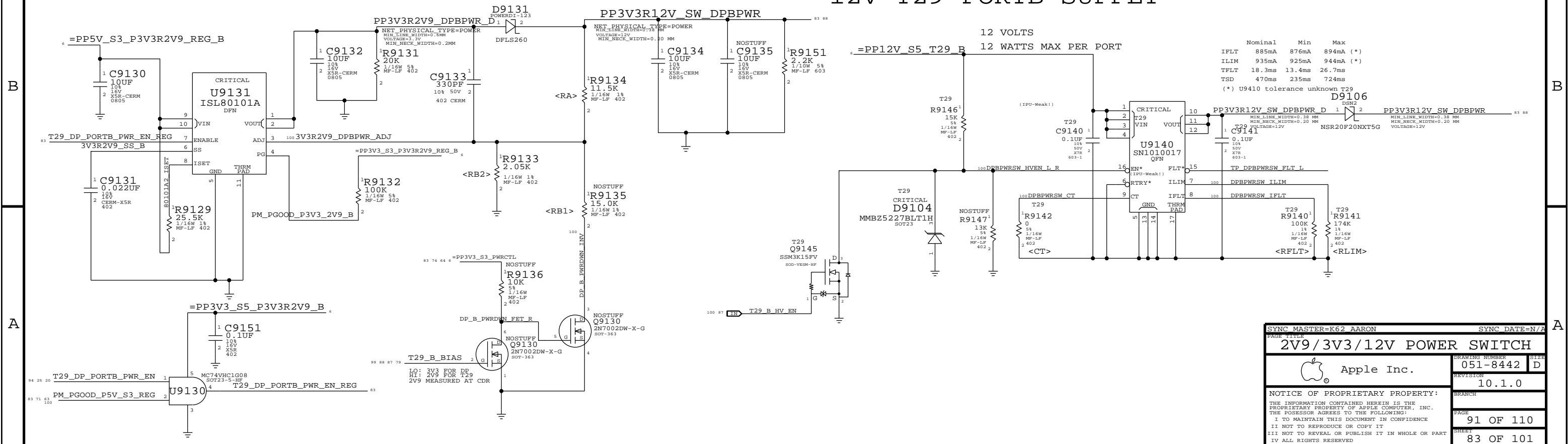
3V3 (DP) / 2V9 (T29) PORTA SUPPLY

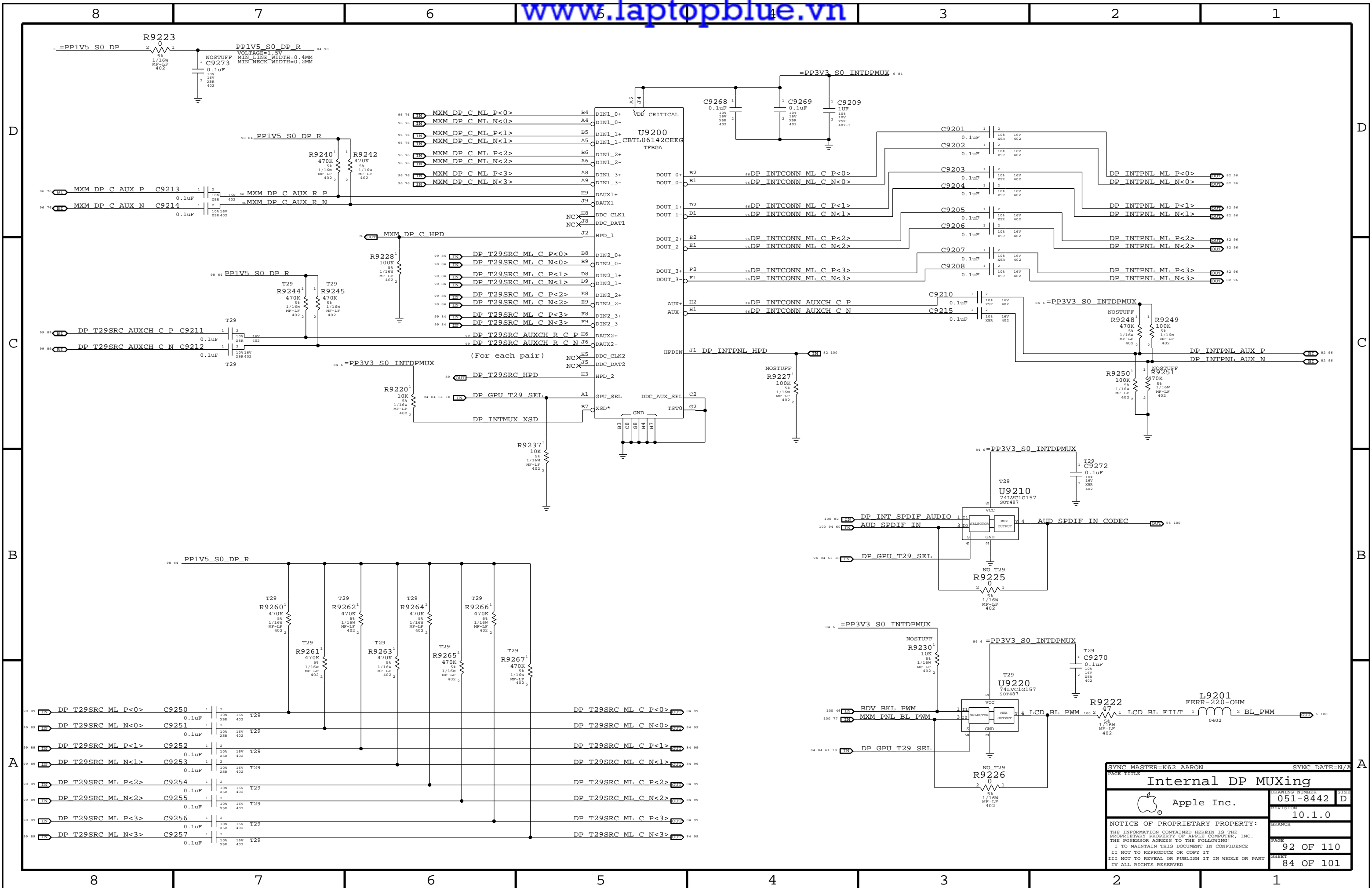
12V T29 PORTA SUPPLY

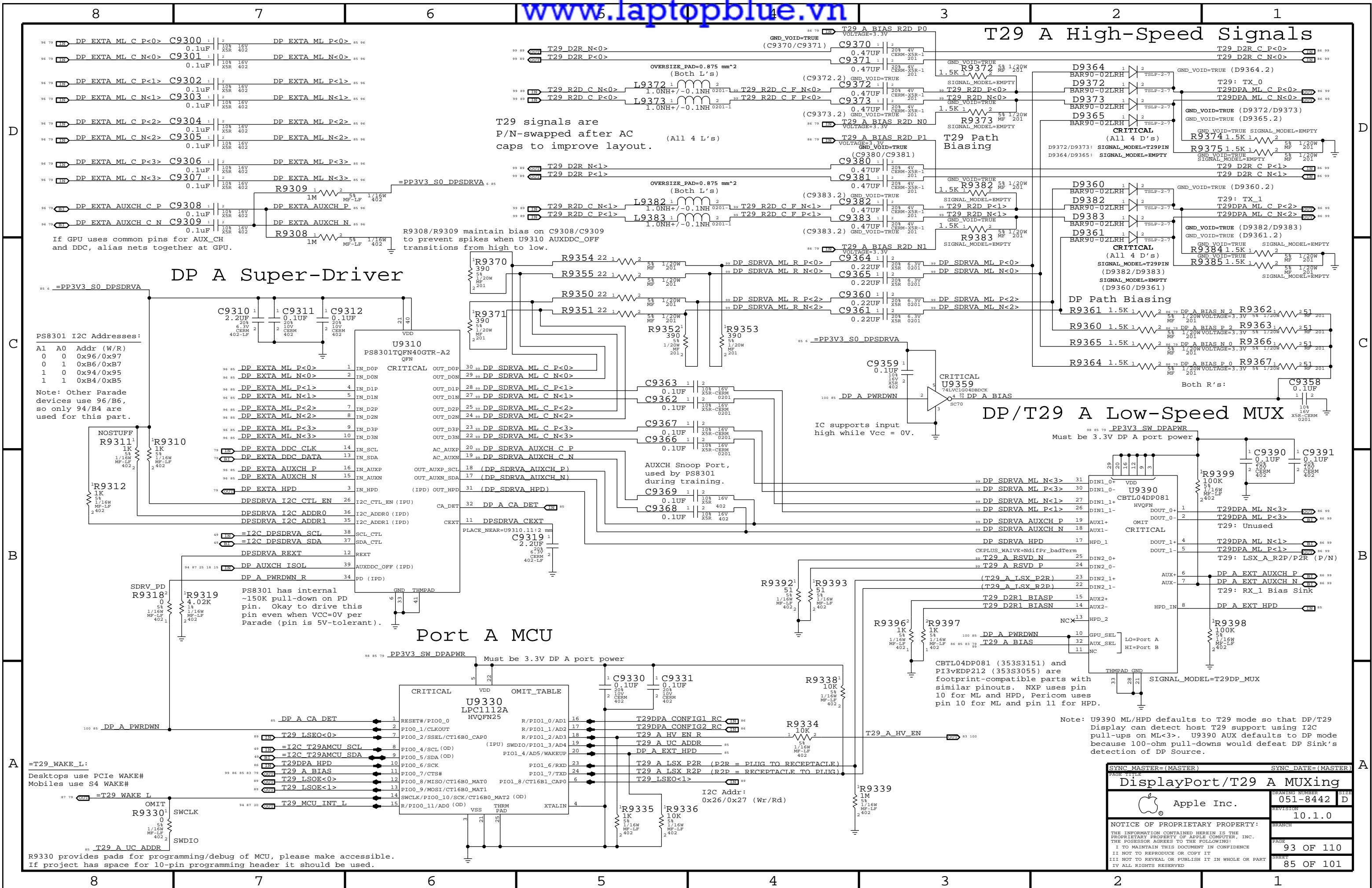


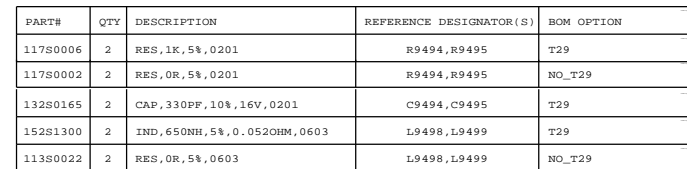
3V3 (DP) / 2V9 (T29) PORTB SUPPLY

12V T29 PORTB SUPPLY

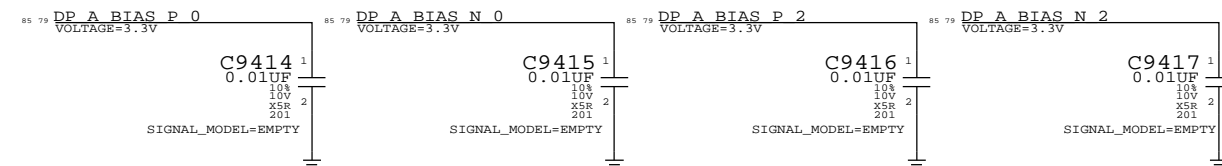









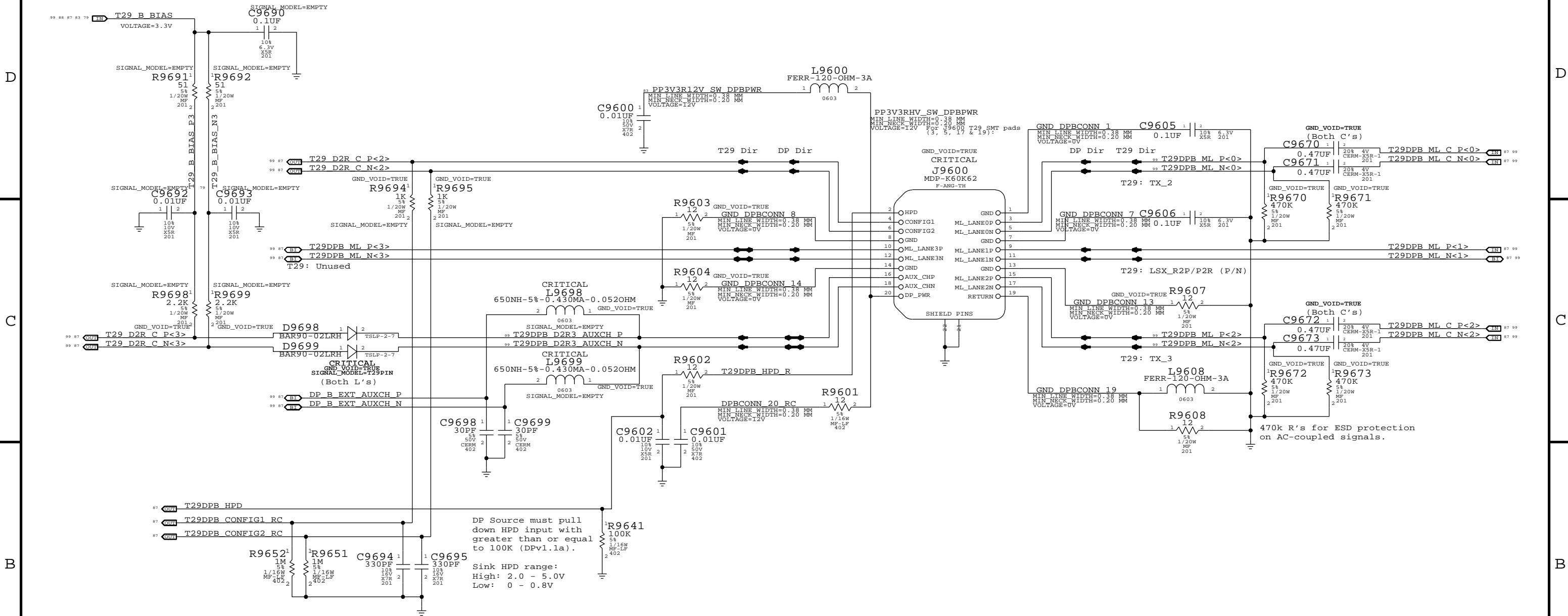
DP BIAS CAPS



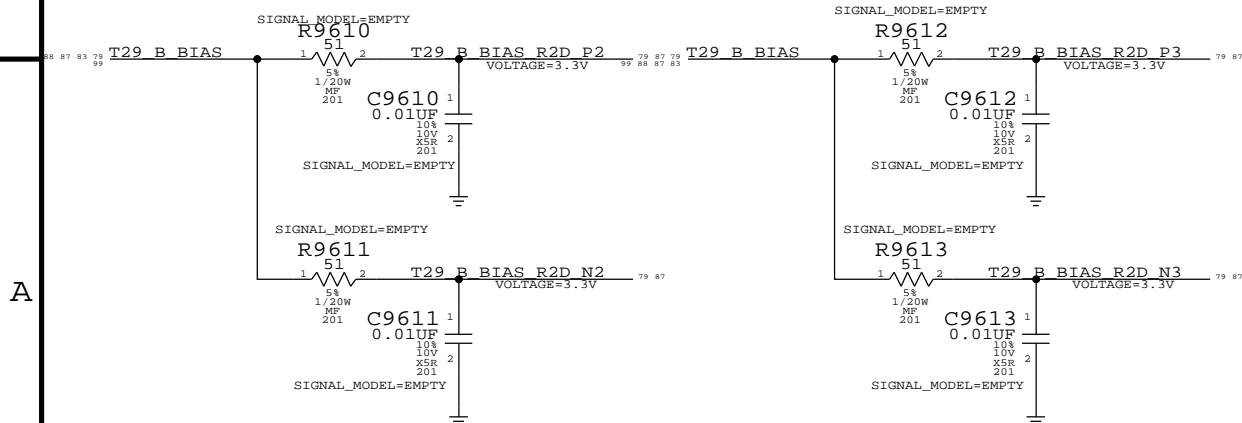
SYNC_MASTER=(MASTER) PAGE 11111		SYNC_DATE=(MASTER) PAGE 11111	
DisplayPort/T29 A Connector			
 Apple Inc.		DRAWING NUMBER 051-8442	
		SIZE D	
		REVISION 10.1.0	
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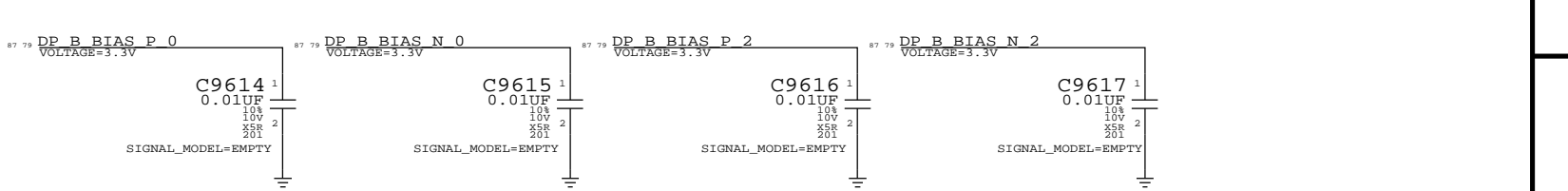
DisplayPort/T29 B Connector



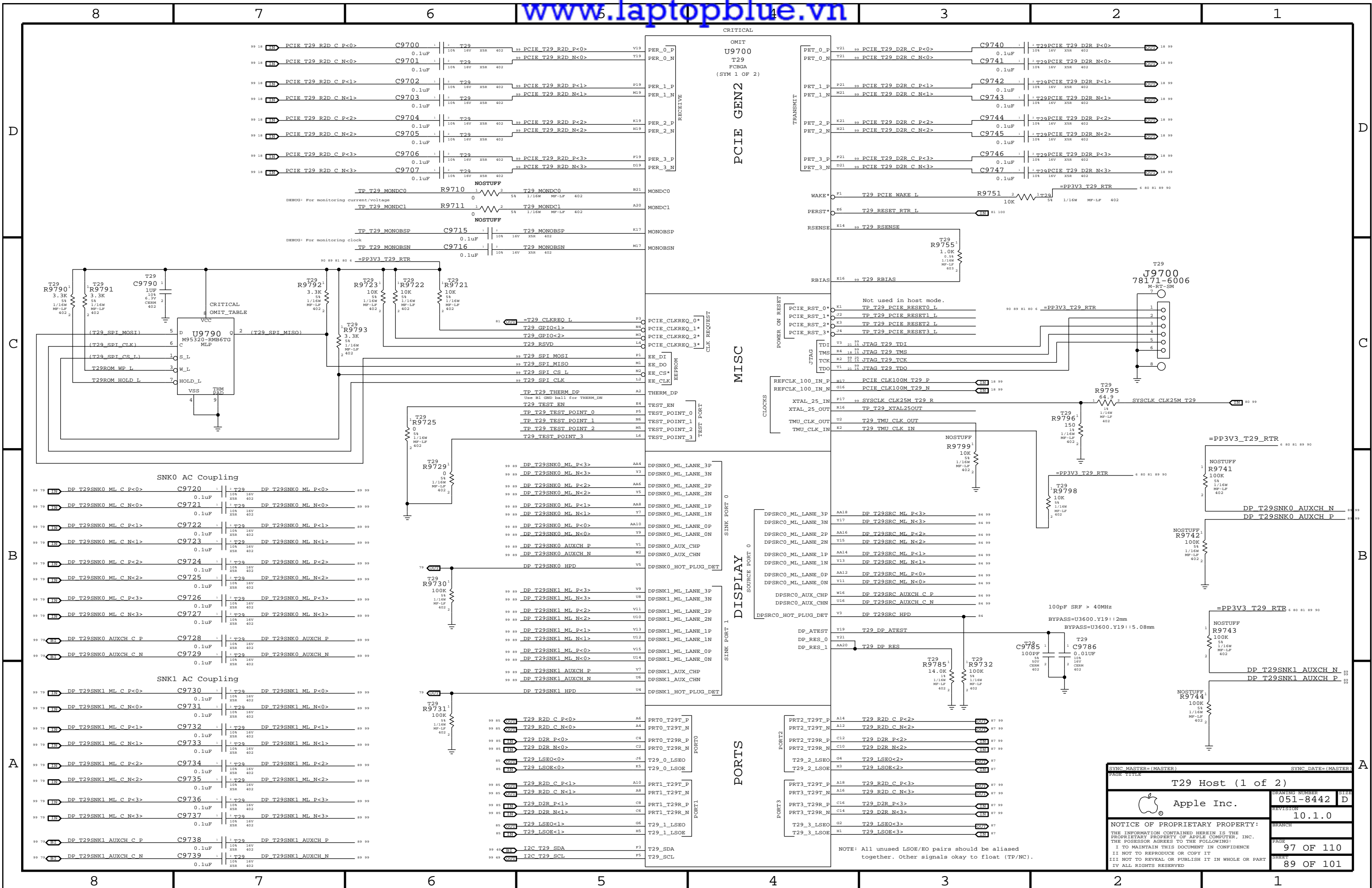
T29 BIAS RC



DP BIAS CAPS



SYNC MASTER=(MASTER)		SYNC DATE=(MASTER)	
PAGE TITLE		DisplayPort/T29 B Connector	
Apple Inc.		DRAWING NUMBER	051-8442
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DCBA

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SYNC MASTER=K62 ROSITA		SYNC DATE=01/09/2011	
PAGE TITLE			
Memory Constraints			
 Apple Inc.	DRAWING NUMBER		SIZE
	051-8442		D
	REVISION		
	10.1.0		
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PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=4X_DIELECTRIC	?	PCIE	TOP,BOTTOM	=4:1_SPACING	?
CLK_PCIE	*	0.5 MM	?				

CPU

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_RCOMP_PHY	*	Y	0.254 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_ITP	*	0.2 MM	?	CPU_RCOMP	*	0.2 MM	?

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=6:1_SPACING	?	SATA	TOP,BOTTOM	=6:1_SPACING	?

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
PCIE GRAPHICS	PCIE_85D	PCIE	PEG R2D C P<15..0>	9 78
	PCIE_85D	PCIE	PEG R2D C N<15..0>	9 78
	PCIE_85D	PCIE	PEG D2R P<15..0>	9 78
	PCIE_85D	PCIE	PEG D2R N<15..0>	9 78
	PCIE_85D	PCIE	MXM PCIE R2D P<7..0>	76 78
	PCIE_85D	PCIE	MXM PCIE R2D N<7..0>	76 78
	PCIE_85D	PCIE	MXM PCIE D2R P<7..0>	76 78
	PCIE_85D	PCIE	MXM PCIE D2R N<7..0>	76 78
	PCIE_85D	PCIE		
	PCIE_85D	PCIE		
PCIE I/O	PCIE_85D	PCIE	PCIE_MINI_R2D_P	33
	PCIE_85D	PCIE	PCIE_MINI_R2D_N	33
	PCIE_85D	PCIE	PCIE_MINI_R2D_C_P	18 33
	PCIE_85D	PCIE	PCIE_MINI_R2D_C_N	18 33
	PCIE_85D	PCIE	PCIE_MINI_D2R_P	18 33
	PCIE_85D	PCIE	PCIE_MINI_D2R_N	18 33
	PCIE_85D	PCIE		
	PCIE_85D	PCIE		
	PCIE_85D	PCIE		
	PCIE_85D	PCIE		
	PCIE_85D	PCIE	PCIE_FW_R2D_P	39
	PCIE_85D	PCIE	PCIE_FW_R2D_N	39
	PCIE_85D	PCIE	PCIE_FW_R2D_C_P	18 39
	PCIE_85D	PCIE	PCIE_FW_R2D_C_N	18 39
	PCIE_85D	PCIE	PCIE_FW_D2R_P	18 39
	PCIE_85D	PCIE	PCIE_FW_D2R_N	18 39
	PCIE_85D	PCIE	PCIE_FW_D2R_C_P	39
	PCIE_85D	PCIE	PCIE_FW_D2R_C_N	39
	PCIE_85D	PCIE		
	PCIE_85D	PCIE		
DMI	CLK_PCIE_90D	CLK_PCIE	DMI_MIDBUS_CLK100M_N	
	CLK_PCIE_90D	CLK_PCIE	DMI_MIDBUS_CLK100M_P	
	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_N	11 18
	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_P	11 18
	PCIE_85D	PCIE	DMI_S2N_P<3..0>	10 19
	PCIE_85D	PCIE	DMI_S2N_N<3..0>	10 19
	PCIE_85D	PCIE	DMI_N2S_P<3..0>	10 19
	PCIE_85D	PCIE	DMI_N2S_N<3..0>	10 19
	PCIE_85D	PCIE		
	PCIE_85D	PCIE		
PCIE REF CLOCKS	CLK_PCIE_90D	CLK_PCIE	GPU_CLK100M_PCIE_P	9
	CLK_PCIE_90D	CLK_PCIE	GPU_CLK100M_PCIE_N	9
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_MINI_P	18 33
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_MINI_N	18 33
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_P	18 39
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_N	18 39
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_P	18 37
	ENET_100D	ENET_MII	PCIE_CLK100M_ENET_P	18 37
	ENET_100D	ENET_MII	PCIE_CLK100M_ENET_N	18 37
	ENET_100D	ENET_MII		
SATA	SATA_90D	SATA	SATA_HDD_R2D_C_P	18 42
	SATA_90D	SATA	SATA_HDD_R2D_C_N	18 42
	SATA_90D	SATA	SATA_HDD_R2D_P	42
	SATA_90D	SATA	SATA_HDD_R2D_N	42
	SATA_90D	SATA	SATA_HDD_D2R_P	18 42
	SATA_90D	SATA	SATA_HDD_D2R_N	18 42
	SATA_90D	SATA	SATA_HDD_D2R_C_P	42
	SATA_90D	SATA	SATA_HDD_D2R_C_N	42
	SATA_90D	SATA	SATA_ODD_R2D_C_P	18 42
	SATA_90D	SATA	SATA_ODD_R2D_C_N	18 42
CLOCKS	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_DMI_P	18 26
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_DMI_N	18 26
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_P	18 26
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_N	18 26
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_P	18 26
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_N	18 26
	CLK_PCIE_90D	CLK_PCIE	ITP_XDP_CLK100M_N	18 25
	CLK_PCIE_90D	CLK_PCIE	ITP_XDP_CLK100M_P	18 25
	CLK_PCIE_90D	CLK_PCIE	ITP_CPU_CLK100M_N	11 18
	CLK_PCIE_90D	CLK_PCIE	ITP_CPU_CLK100M_P	11 18
UNUSED CLOCKS	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_P	25
	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_N	25
UNUSED PCIE	PCIE_85D	PCIE	MXM_PCIE_R2D_P<8..15>	76 78
	PCIE_85D	PCIE	MXM_PCIE_R2D_N<8..15>	76 78
	PCIE_85D	PCIE	MXM_PCIE_D2R_P<8..15>	76 78
	PCIE_85D	PCIE	MXM_PCIE_D2R_N<8..15>	76 78

ANY OTHER LYNNFIELD CONSTRAINTS NOT COVERED ON PAGES 101 AND 107 SHOULD GO ON THIS PAGE TOO

SYNC MASTER=K62 ROSITA

SYNC DATE=01/09/2011

PCIE/DMI/FDI/SATA CONSTRAINTS

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PCH CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCH	*	=4:1_SPACING	?
COMP_PCH	*	0.2 MM	?
ITP_PCH	*	0.2 MM	?

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	0.2 MM	?

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	0.15 MM	?
CLK_LPC	*	0.2 MM	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2X_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2X_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	0.2 MM	?

XTAL Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_XTAL	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XTAL	*	=4X_DIELECTRIC	?

NET_TYPE	PHYSICAL	SPACING
PM	T29 CLKREQ L	15 21 81
PM	FW MINI CLKREQ L	15 18
PM	BLC GPIO	6 15 21
PM	T29_SW RESET L	15 21 81
PM	ENET CLKREQ L	15 18 36
PM	DP GPU T29_SEL	18 61 84
PM	T29 MCU INT L	20 85 87
PM	T29_DP PORTA_PWR_EN	20 25 83 100
PM	T29_DP PORTB_PWR_EN	20 25 83
PM	DP AUXCH ISOL	15 18 25 85 87
PM	PLT_RST_BUF L	27
PM	XDP CPU_PLTTEST L	26 27
PM	PCH_PEG_CLKREQ L	21
PM	ENET_SW RESET L	15 21 36
PM	CPU_SKTOCC	63
PM	PM_EN_USB_PWR	43 63

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
	PCI_55S	PCI	PCI REQ0 L
	PCI_55S	PCI	PCI REQ1 L
	PCI_55S	PCI	PCI REQ2 L
	CLK_PCI_55S	CLK_PCI	PCH_CLK33M_PCIOUT
	CLK_PCI_55S	CLK_PCI	PCH_CLK33M_PCIIN
	LPC_55S	LPC	LPC_AD<3..0>
	LPC_55S	LPC	LPC_FRAME L
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS
	CLK_LPC_55S	PM	PM_CLK32K_SUSCLK_R
	CLK_LPC_55S	PM	PM_CLK32K_SUSCLK
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS_R
	LPC_55S	LPC	LPC_R_AD<3..0>
	LPC_55S	LPC	LPC_FRAME_R_L
	SPI_55S	SPI	SPI_CLK_1_R
	SPI_55S	SPI	SPI_MOSI_1_R
	CLK_XTAL	XTAL	USB_HUB2_XTAL1
	CLK_XTAL	XTAL	USB_HUB2_XTAL2
	CLK_XTAL	XTAL	PCH_CLK32K_RTCX1_R
	CLK_XTAL	XTAL	PCH_CLK32K_RTCX2_R
	CLK_XTAL	XTAL	PCH_CLK32K_RTCX1
	CLK_XTAL	XTAL	PCH_CLK32K_RTCX2
	CLK_XTAL	XTAL	PCH_CLK32K_RTCX1
	CLK_XTAL	XTAL	PCH_CLK32K_RTCX2
	CLK_XTAL	XTAL	CK505_XTAL_IN
	CLK_XTAL	XTAL	CK505_XTAL_OUT
	CLK_XTAL	XTAL	CK505_XTAL_OUT_R
	CLK_PCH_55S	CLK_PCH	PCH_CLK14P3M_REFCLK

NET_TYPE	PHYSICAL	SPACING
PM	ENET RESET LOGIC L	36
PM	ENET RESET FET L	
PM	ENET CLKREQ_FET L	36 37
PM	PGOOD_5V_1V05_3V3	64 100
PM	PGOOD_CPU_UNCORE	64 100
PM	ALL_SYS_PWRGD	64 100
PM	PGOOD_3V3_1V05	64 100
PM	PGOOD_PCH_S0_R	64 100
PM	AUD_IPHS_SWITCH_EN_PCH	21 25

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
	SPI_55S	SPI	SPI_CLK_R
	SPI_55S	SPI	SPI_CLK
	SPI_55S	SPI	SPI_MOSI_R
	SPI_55S	SPI	SPI_MOSI
	SPI_55S	SPI	SPI_MISO
	SPI_55S	SPI	SPI_MISO_R
	SPI_55S	SPI	SPI_CS0_R_L
	SPI_55S	SPI	SPI_CS0_L
	SPI_55S	SPI	SPI_MLB_CS_L
	SPI_55S	SPI	SPI_ALT_CS_L
	SPI_55S	SPI	SPIROM_USE_MLB
	SPI_55S	SPI	SPI_ALT_MOSI
	SPI_55S	SPI	SPI_ALT_MISO
	SPI_55S	SPI	SPI_ALT_CLK
	HDA_55S	HDA	HDA_BIT_CLK
	HDA_55S	HDA	HDA_BIT_CLK_R
	HDA_55S	HDA	HDA_RST_L
	HDA_55S	HDA	HDA_RST_R_L
	HDA_55S	HDA	HDA_SDOVT
	HDA_55S	HDA	HDA_SDOVT_R
	HDA_55S	HDA	HDA_SYNC
	HDA_55S	HDA	HDA_SYNC_R
	HDA_55S	HDA	HDA_SDINO
	HDA_55S	HDA	AUD_SDI_R
		PM	AUD_SPDIF_IN
		HDA	AUD_SPDIF_OUT
		HDA	AUD_SPDIF_CHIP
	HDA_55S	HDA	AUD_SPKR_OUTLO1L_NOUT
	HDA_55S	HDA	AUD_SPKR_OUTLO1L_POUT
	HDA_55S	HDA	AUD_SPKR_OUTLO1R_NOUT
	HDA_55S	HDA	AUD_SPKR_OUTLO1R_POUT
	HDA_55S	HDA	AUD_SPKR_OUTLO2L_NOUT
	HDA_55S	HDA	AUD_SPKR_OUTLO2L_POUT
	HDA_55S	HDA	AUD_SPKR_OUTLO2R_NOUT
	HDA_55S	HDA	AUD_SPKR_OUTLO2R_POUT
	CLK_XTAL	XTAL	PCH_CLK25M_XTALOUT_R
	CLK_XTAL	XTAL	PCH_CLK25M_XTALIN_R
	CLK_XTAL	XTAL	PCH_CLK25M_XTALOUT
	CLK_XTAL	XTAL	PCH_CLK25M_XTALIN
	PCH_55S	COMP_PCH	PCH_USB_RB1AS
	PCH_55S	COMP_PCH	PCH_SATA3COMP
	PCH_55S	COMP_PCH	PCH_XCLK_RCOMP
	PCH_55S	COMP_PCH	PCH_DMI_COMP
	PCH_55S	COMP_PCH	PCH_SATA1COMP
	CLK_XTAL	XTAL	USB_HUB1_XTAL1
	CLK_XTAL	XTAL	USB_HUB1_XTAL2
	PCH_55S	COMP_PCH	USB_HUB1_RB1AS
	PCH_55S	ITP_PCH	XDP_PCH_TCK
	PCH_55S	ITP_PCH	XDP_PCH_TMS
	PCH_55S	ITP_PCH	XDP_PCH_TDI
	PCH_55S	ITP_PCH	XDP_PCH_TDO
	PCH_55S	COMP_PCH	PCH_DMI2RB1AS
	PCH_55S	COMP_PCH	PCH_SATA3RB1AS
	PCH_55S	COMP_PCH	USB_HUB2_RB1AS

SYNC MASTER=K62_S1J1

SYNC DATE=01/09/2011

IBEX PEAK CONSTRAINTS

Apple Inc.

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SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

CB

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8	7	6	5	4	3	2	1
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VR CTRL NET PROPERTIES

VR CTRL NET PROPERTIES

NET_TYPE				
PHYSICAL		SPACING		
	VR_CTL_PHY	VR_CTL	DDR REG CS	72
REG	VR_CTL_PHY	VR_CTL	DDR REG FB	72
REG	VR_CTL_PHY	VR_CONTROL	DDR REG LGATE	72
REG	VR_CTL_PHY	VR_CONTROL	DDR REG UGATE	72
REG	VR_CTL_PHY	VR_CONTROL	DDR REG BOOT	72
REG	VR_CTL_PHY	VR_CONTROL	DDR REG BOOT R	72
REG	VR_CTL_PHY	VR_CTL	DDR REG VDDQSN	72
REG	VR_CTL_PHY	VR_CTL	DDR REG VITSNS	72
REG	VR_CTL_PHY	VR_CTL	DDR REG PHASE R	72
REG	VR_CTL_PHY	VR_CTL	DDR REG UGATE R	72
	VR_CTL_PHY	SWITCHMODE	I1V5_SNUBBER	72
REG	VR_CTL_PHY	VR_CTL	P1V8 REG VEB	72
REG	VR_CTL_PHY	VR_CTL	P1V8 REG SYNC	72
	VR_CTL_PHY	VR_CONTROL	P3V3S5 REG BOOT	71
REG	VR_CTL_PHY	VR_CONTROL	P3V3S5 REG BOOT R	71
REG	VR_CTL_PHY	VR_CTL	P3V3S5 REG FB	71
REG	VR_CTL_PHY	VR_CTL	P3V3S5 REG ISEN	71
REG	VR_CTL_PHY	VR_CONTROL	P3V3S5 REG LGATE	71
REG	VR_CTL_PHY	VR_CTL	P3V3S5 REG OCSET	71
REG	VR_CTL_PHY	VR_CONTROL	P3V3S5 REG VOUT1	71
REG	VR_CTL_PHY	VR_CONTROL	P3V3S5 REG FSET1	71
REG	VR_CTL_PHY	VR_CONTROL	P3V3S5 REG UGATE	71
REG	VR_CTL_PHY	VR_CTL	P3V3S5 REG SNUB	71
	VR_CTL_PHY	VR_CONTROL	P5V33 REG BOOT	71
REG	VR_CTL_PHY	VR_CTL	P5V33 REG FB	71
	VR_CTL_PHY	VR_CTL	P5V33 REG ISEN	71
REG	VR_CTL_PHY	VR_CONTROL	P5V33 REG LGATE	71
REG	VR_CTL_PHY	VR_CTL	P5V33 REG OCSET	71
REG	VR_CTL_PHY	VR_CONTROL	P5V33 REG FSET2	71
REG	VR_CTL_PHY	VR_CONTROL	P5V33 REG UGATE	71
REG	VR_CTL_PHY	VR_CONTROL	P5V33 REG VOUT2	71
	VR_CTL_PHY	VR_CTL	VCCSA_CNTRL_INPUT1	69
REG	VR_CTL_PHY	VR_CTL	VCCSA_CNTRL_INPUT2	69
REG	VR_CTL_PHY	VR_CTL	VCCSA_CNTRL_INPUT2	R 69 98
	VR_CTL_PHY	VR_CTL	VCCSA_OUT	69
REG	VR_CTL_PHY	VR_CTL	VCCSA_GATE	69
REG	VR_CTL_PHY	VR_CTL	VCCSA_REF	69
REG	VR_CTL_PHY	VR_CTL	VCCSA_CTL	69
	VR_CTL_PHY	VR_CTL	CPU_VCCSA_SENSE	13 69
	VR_CTL_PHY	VR_CTL	VR_CPU_TM	65
REG	VR_CTL_PHY	PM	3V3R2V9_DPAVWR_ADJ	83 100

NET_TYPE			
PHYSICAL	SPACING		
		PULL-UP STUB	< 1-INCH
		VID LENGTH SWRM	< 1-INCH
		VID LENGTH RANGE	1 TO 15-INCH
VR00	VID_PHY	VR_CTL_VIDS	CPU VIDSLCK R 13
VR01	VID_PHY	VR_CTL_VIDS	CPU VIDALERT L R 13
VR02	VID_PHY	VR_CTL_VIDS	CPU VIDSORT R 13
VR03	VID_PHY	VR_CTL_VIDS	CPU VIDSLCK 13 65
VR04	VID_PHY	VR_CTL_VIDS	CPU VIDALERT L 13 65
VR05	VID_PHY	VR_CTL_VIDS	CPU VIDSORT 13 65

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
VR_CTL_VIDS	*	= 4X_DIELECTRIC	?

SYNC MASTER-K62 JERRY		SYNC DATE-01/09/2011	
PAGE TITLE			
POWER CONSTRAINTS			
 Apple Inc.		DRAWING NUMBER	051-8442
		SIZE	D
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T29 ELECTRICAL ROUTES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29	*	=5X_DIELECTRIC	?	T29	TOP,BOTTOM	=7X_DIELECTRIC	?

T29 PCI-EXPRESS (SAME RULE AS PCIE)

T29 SPI INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SPI	*	0.2 MM	?

T29 XTAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_XTAL_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_XTAL	*	=4X_DIELECTRIC	?

T29 SMBUS INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SMB	*	=2x_DIELECTRIC	?

GREEN CLOCK CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_25M_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_25M	*	=5X_DIELECTRIC	?

T29 BIAS CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_COMP	*	0.2 MM	?

T29 NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		SPACING	
		PHYSICAL			
NO_TEST=TRUE	T29_90D	T29	T29_R2D C P<3..0>	85	89
NO_TEST=TRUE	T29_90D	T29	T29_R2D C N<3..0>	85	87
NO_TEST=TRUE	T29_90D	T29	T29_D2R C P<3..0>	85	87
NO_TEST=TRUE	T29_90D	T29	T29_D2R C N<3..0>	85	87
NO_TEST=TRUE	T29_90D	T29	T29_R2D P<3..0>	85	87
NO_TEST=TRUE	T29_90D	T29	T29_R2D N<3..0>	85	87
NO_TEST=TRUE	T29_90D	T29	T29_D2R P<3..0>	85	87
NO_TEST=TRUE	T29_90D	T29	T29_D2R N<3..0>	85	87
NO_TEST=TRUE	T29_90D	T29	T29_R2D C F P<3..0>	85	87
NO_TEST=TRUE	T29_90D	T29	T29_R2D C F N<3..0>	85	87
NO_TEST=TRUE	T29_90D	T29	T29DPA ML P<3..0>	85	86
NO_TEST=TRUE	T29_90D	T29	T29DPA ML N<3..0>	85	86
NO_TEST=TRUE	T29_90D	T29	T29DPB ML P<3..0>	87	88
NO_TEST=TRUE	T29_90D	T29	T29DPB ML N<3..0>	87	88
NO_TEST=TRUE	T29_90D	T29	DP A EXT AUXCH P	85	86
NO_TEST=TRUE	T29_90D	T29	DP A EXT AUXCH N	85	86
NO_TEST=TRUE	T29_90D	T29	DP SDRVA AUXCH C P	85	86
NO_TEST=TRUE	T29_90D	T29	DP SDRVA AUXCH C N	85	86
NO_TEST=TRUE	T29_90D	T29	DP SDRVB AUXCH C P	87	87
NO_TEST=TRUE	T29_90D	T29	DP SDRVB AUXCH C N	87	87
NO_TEST=TRUE	T29_90D	T29	DP B EXT AUXCH P	87	88
NO_TEST=TRUE	T29_90D	T29	DP B EXT AUXCH N	87	88
NO_TEST=TRUE	T29_90D	T29	T29DPA D2R1 AUXCH N	86	86
NO_TEST=TRUE	T29_90D	T29	T29DPB D2R3 AUXCH P	88	88
NO_TEST=TRUE	T29_90D	T29	T29DPB D2R3 AUXCH N	88	88
NO_TEST=TRUE	T29_90D	T29	T29DPA ML C N<0>	85	86
NO_TEST=TRUE	T29_90D	T29	T29DPA ML C P<0>	85	86
NO_TEST=TRUE	T29_90D	T29	T29DPA ML C N<2>	85	86
NO_TEST=TRUE	T29_90D	T29	T29DPA ML C P<2>	85	86
NO_TEST=TRUE	T29_90D	T29	T29DPB ML C N<0>	87	88
NO_TEST=TRUE	T29_90D	T29	T29DPB ML C P<0>	87	88
NO_TEST=TRUE	T29_90D	T29	T29DPB ML C N<2>	87	88
NO_TEST=TRUE	T29_90D	T29	T29DPB ML C P<2>	87	88
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE T29_R2D P<3..0>	89	
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE T29_R2D N<3..0>	89	
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE T29_R2D C P<3..0>	18	89
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE T29_R2D C N<3..0>	18	89
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE T29_D2R P<3..0>	18	89
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE T29_D2R N<3..0>	18	89
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE T29_D2R C P<3..0>	89	
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE T29_D2R C N<3..0>	89	
NO_TEST=TRUE	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M T29 P	18	89
NO_TEST=TRUE	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M T29 N	18	89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SRC ML C P<3..0>	84	
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SRC ML C N<3..0>	84	
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SRC ML P<3..0>	84	89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SRC ML N<3..0>	84	89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SNK0 ML P<3..0>	89	
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SNK0 ML N<3..0>	89	
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SNK0 AUXCH P	79	89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SNK0 AUXCH N	89	
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SNK0 ML C P<3..0>	79	89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SNK0 ML C N<3..0>	79	89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SNK0 AUXCH C P	79	89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SNK0 AUXCH C N	79	89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SNK1 ML P<3..0>	89	
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SNK1 ML N<3..0>	89	
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SNK1 AUXCH P	89	
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SNK1 AUXCH N	89	
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SNK1 ML C P<3..0>	79	89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SNK1 ML C N<3..0>	79	89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SNK1 AUXCH C P	79	89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SNK1 AUXCH C N	79	89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SRC AUXCH R C P	84	
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SRC AUXCH R C N	84	
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SRC AUXCH C P	84	89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SRC AUXCH C N	84	89
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP SDRVA AUXCH P	85	
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP SDRVA AUXCH N	85	
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP SDRVB AUXCH P	87	
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP SDRVB AUXCH N	87	
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP SDRVA ML C P<3..0>	85	
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP SDRVA ML C N<3..0>	85	
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP SDRVA ML P<3..0>	85	
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP SDRVA ML N<3..0>	85	
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP SDRVA ML R P<3..0>	85	
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP SDRVA ML R N<3..0>	85	
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP SDRVB ML C P<3..0>	87	
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP SDRVB ML C N<3..0>	87	
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP SDRVB ML P<3..0>	87	
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP SDRVB ML N<3..0>	87	
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP SDRVB ML R P<3..0>	87	
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP SDRVB ML R N<3..0>	87	
NO_TEST=TRUE	T29_90D	DISPLAYPORT	T29 A RSVD N	85	
NO_TEST=TRUE	T29_90D	DISPLAYPORT	T29 A RSVD P	85	
NO_TEST=TRUE	T29_90D	DISPLAYPORT	T29 B RSVD N	87	
NO_TEST=TRUE	T29_90D	DISPLAYPORT	T29 B RSVD P	87	

T29 NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		SPACING	
		PHYSICAL			
	T29_SBT_55S	T29_SBT	JTAG T29 TDI	18	21
	T29_SBT_55S	T29_SBT	JTAG T29 TMS	18	18
	T29_SBT_55S	T29_SBT	JTAG T29 TCK	18	21
	T29_SBT_55S	T29_SBT	JTAG T29 TDO	15	21
	T29_SBT_55S	T29_SBT	T29_SPI MOSI	89	
	T29_SBT_55S	T29_SBT	T29_SPI MISO	89	
	T29_SBT_55S	T29_SBT	T29_SPI CS L	89	
	T29_SBT_55S	T29_SBT	T29_SPI CLK	89	
	CLK_25M_55S	CLK_25M	SYSCLK CLK25M T29	80	89
	CLK_25M_55S	CLK_25M	SYSCLK CLK25M T29 R	89	89
	T29_SMB_55S	T29_SMB	I2C T29_SDA	49	89
	T29_SMB_55S	T29_SMB	I2C T29_SCL	49	89
	CLK_25M_55S	CLK_25M	SYSCLK CLK25M_SB	80	
	CLK_25M_55S	CLK_25M	SYSCLK CLK25M_ENET	80	
	CLK_25M_55S	CLK_25M	ENET CLK25M_XTALI OSC	16	80
	CLK_25M_55S	CLK_25M	SYSCLK CLK25M T29_CLK	80	
	CLK_25M_55S	CLK_25M	SYSCLK CLK25M T29	80	89
	CLK_25M_55S	CLK_25M	SYSCLK CLK25M T29_R	89	89
	T29_XTAL_100D	T29_XTAL	SYSCLK CLK25M_X2	80	
	T29_XTAL_100D	T29_XTAL	SYSCLK CLK25M_X2_R	80	
	T29_XTAL_100D	T29_XTAL	SYSCLK CLK25M_X1	80	
	T29_55S	T29_COMP	T29_RSENSE	89	
	T29_55S	T29_COMP	T29_RBIAS	89	
	T29_COMP	T29_COMP	T29_A_BIAS	79	83
	T29_COMP	T29_COMP	T29_B_BIAS	79	83
	T29_COMP	T29_COMP	DP_A_BIAS	79	85

D

C

B

A

PM NET PROPERTIES
(PM, RESET, EN, PGOOD)

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PM	*	*	2:1_SPACING
PM_VTT	PM_VTT	*	2:1_SPACING
PM_VTT	*	*	3:1_SPACING
PM_VTT	GND	*	DEFAULT
PM	GND	*	DEFAULT

NET_TYPE		PHYSICAL	SPACING
PHYSICAL	SPACING		
PM	4V5 REG EN	56	
PM	3V42Q3H SHDN L	73	
PM	ALL SYS PWRGD R	5	32 64
PM	ALL SYS PWRGD SMC	46	64
PM	AP PWR EN	20	25 33
PM	AP MINI RESET L	33	
PM	AUD I2C INT L	20	62
PM	AUD IP PERIPHERAL DET	20	61
PM	AUD IPHS SWITCH EN	21	62
PM	AUD SPDIF IN	60	84 94
PM	AUD SPDIF IN CODEC	56	84
PM	BDV_BKL_PWM	46	84 100
PM	BL_PWM	6	84
PM	BL_EN	6	82
PM	BDV_BKL_PWM	46	84 100
PM	CK505 27MHZ EN	26	
PM	CPUVTT REG EN	63	
PM_VTT	CPUVTT REG PGOOD R	63	
PM	CPU MEM RESET L	11	32
PM	CPU Peci R	46	
PM_VTT	CPU PWRGD	11	21 25
PM	CPU RESET L	11	27
PM	CPU SKTOCC L	11	63
PM	CPU CATERR L	11	
PM	CPU Peci	11	21 46
PM	CPU PROCHOT L	11	47 65
PM	CPU THRMTrip L	11	47
PM	CPU PROC_SEL	11	19
PM	DEBUG RESET L	27	48
PM	DDRVT EN	82	84
PM	DP INT SPDIF AUDIO	82	84
PM	DP INTFNL HPD	82	84
PM	3V3R2V9 DPAPWR ADJ	83	98
PM	DP A PWRDWN	83	
PM	DP A PWRDWN FET R	83	
PM	DP A PWRDWN INV	83	
PM	DPAPWRSW HVEN L R	83	
PM	DPAPWRSW CT	83	
PM	DPAPWRSW_ILIM	83	
PM	DPAPWRSW_ILIT	83	
PM	T29 A HV EN	83	85
PM	3V3R2V9 DPBPWR ADJ	83	
PM	DP B PWRDWN	83	
PM	DP B PWRDWN FET R	83	
PM	DP B PWRDWN INV	83	
PM	DPBPWRSW HVEN L R	83	
PM	DPBPWRSW CT	83	
PM	DPBPWRSW_ILIM	83	
PM	DPBPWRSW_ILIT	83	
PM	T29 B HV EN	83	87
PM	T29 PWR EN	18	81 100
PM	T29 RESET RTR L	81	89
PM	LCD_BL_FILT	84	
PM	LCD_BLK_ON_DLY	84	
PM	LCD_BL_PWM	84	
PM	MXM_PNL_BL_PWM	77	84

NET_TYPE		PHYSICAL	SPACING
PHYSICAL	SPACING		
PM	ENET PWR EN	20	25 36
PM	ENET LOW PWR	15	21 37
PM	FW RESET L	27	39
PM	ENET RESET L	27	36
PM	FW PME L	15	21 39
PM	FW PWR EN	15	21
PM	FW CLKREQ L	15	39
PM	ISOLATE CPU MEM L	21	25 32
PM	LPC PWRDWN L	19	46 48
PM	MEM RESET L	30	31 32 92
PM	MINI_CLKREQ L	15	33
PM	MINI_RESET L	27	33
PM	MXM_CLKREQ L	9	76
PM	MXM_GOOD	5	21 25
PM	ODD PWR EN L	15	21 42
PM	RTC RESET L	18	27 100
PM	RSRST PWRGD	46	64
PM	RTC RESET L	18	27 100
PM	S4_ENABLES	63	
PM	SDCONN_STATE_RST_L	95	
PM	SDCONN_DETECT_BUF_L	20	25 46
PM	SDCONN_STATE_CHANGE	15	21 44 101
PM	SDCARD RESET	44	
PM	SDCARD_PLT_RST_L	27	44
PM	SDCARD_PLT_RST_L_R	46	75
PM	SMC PM G2 EN	75	
PM	SMC PM G2 EN R	75	
PM	SMC PM G2 EN L	75	
PM	S5 DG 1	75	
PM	S5 MSFT G1	75	
PM	USE HDD OOB L	20	51
PM	HDD OOB 1V00 REF	51	
PM	SMC ADAPTER EN	19	46 47
PM	SMC RUNTIME SCI L	21	46 47
PM	SMC WAKE SCI L	15	18 21 46
PM	SMC DELAYED_PWRGD	27	64
PM	SMC LRESET L	27	46
PM	SMC RESET L	46	47 48
PM	SMC PROCHOT	46	47
PM	SMC PROCHOT 3 3 L	46	47
PM	SMC ONOFF L	46	47
PM	SMC MANUAL_RST_L	47	
PM	SPI_DESCRIPTOR_OVERRIDE_L	18	46
PM	T29 PWR EN	18	81 100
PM	T29 RESET L	27	81
PM	T29 DP PORTA_PWR_EN	20	25 83 94
PM	T29 DP PORTA_PWR_EN_REG	83	
PM_VTT	XDP_CPUPWRGD	11	25
PM_VTT	XDP_DBRESET L	11	25
PM_VTT	XDP_PWRGD	25	27
PM	XDPPCH_PLTRST L	20	25 34
PM	USB_HUB_SOFT_RESET_L	20	25 34
PM	VSYNC_DP_CONN	6	82
PM	VSYNC_DP	62	
PM	VIDEO_ON	62	
PM	VTT_REG_PGOOD_L	63	

NET_TYPE		PHYSICAL	SPACING
PHYSICAL	SPACING		
PM	PLT RESET L	20	27
PM_VTT	PLT RESET LS1V05 L	11	
PM	PM BATLOW L	15	19 46
PM	PM CLK32K_SUSCLK	9	46 94
PM	PM CLK32K_SUSCLK_R	9	19 94
PM	PM CLKRUN L	15	19 46 48
PM	PM PWRBTN L	19	25 46
PM	PM RSMRST L	27	46
PM	PM RSMRST_PCH_L	19	27
PM	PCH_SRTCST L	18	
PM	PCH_INTVRMEN L	18	
PM	PCH_DSMVRMEN	19	
PM	PCH_DF_TVS	19	
PM	PCH_PROCPWRGD	21	
PM	PCIE_WAKE_L	19	33 36 79
PM	PM_DSW_PWRGD	19	
PM	PM_ASW_PWRGD	19	64
PM	PM_MEM_PWRGD_R	11	
PM	PM_EN_DDR1V5_S3_REG	63	72
PM	PM_EN_DDRVTT_S0_REG	32	63 72
PM	PM_EN_P12V_S0_FET	6	63
PM	PM_EN_P1V05_S0_REG	63	68
PM	PM_EN_P1V05_S3_REG	63	74
PM	PM_EN_P1V5_S0_FET	63	74
PM	PM_EN_P1V8_S0_REG	63	72
PM	PM_EN_P3V3_S0_FET	63	74
PM	PM_EN_P3V3_S3_FET	63	74
PM	PM_EN_P3V3_S5_REG	71	
PM	PM_EN_P5V_S0_FET	63	74
PM	PM_EN_P5V_S3_REG	63	71
PM	PM_EN_PVCCSA_S0_REG_L	64	
PM	PM_EN_VCCSA_S0_CPU	63	65
PM	PM_EN_PVCORE_CPU	63	65
PM_VTT	PM_MEM_PWRGD	11	19 100
PM	PM_MXM_EN	64	77
PM	PM_PCH_PWRGD_R	64	
PM	PM_PECI_PWRGD	46	64
PM	PM_PECI_PWRGD_R	46	
PM	PM_PGOOD_DDR1V5_S3_REG	6	63 72
PM	PM_PGOOD_P1V05_S0_REG	63	64 68
PM	PM_PGOOD_P1V5_S0_FET	11	64 74
PM	PM_PGOOD_P1V8_S0_REG	64	72
PM	PM_PGOOD_P3V3_S0_FET	63	64 74
PM	PM_PGOOD_P3V3_S3_FET	34	74
PM	PM_PGOOD_P3V3_S5_REG	27	64 71
PM	PM_PGOOD_P5V_S0_FET	63	64 74
PM	PM_PGOOD_MINI	33	
PM	PM_PGOOD_PVCORE_CPU	5	25 64 65
PM	PM_PGOOD_PVCCSA_S0_REG	63	64
PM	PM_PGOOD_P5V_S3_REG	63	71 83
PM	PM_PGOOD_PVAXG	5	65
PM_VTT	PM_MEM_PWRGD	11	19 100
PM	PM_MEM_PWRGD_L	11	
PM	PM_MXM_PGOOD	64	77
PM	PM_PCH_PWRGD	19	21 64
PM	PM_SLP_S3_5V	32	
PM	PM_SLP_S3_5V_L	32	
PM	PM_SLP_S3_5V_R2	32	
PM	PM_SLP_S3_L	5	19 26 32 36 46 47 63
PM	PM_SLP_S4_L	5	19 32 46 47 63 100
PM	PM_SLP_S5_L	5	19 46 47 63
PM_VTT	PM_SYNC	11	19
PM	PM_SYSRST_L	19	25 27 46
PM	PM_SYS_PWRGD	19	32 64
PM_VTT	PM_THRMTrip_L	21	47
PM	PM_SLP_S3_BUF_L	63	
PM	PM_SLP_S4_1_L_R	63	
PM	PM_SLP_S4_D_L	32	
PM	PM_SLP_S4_L	5	19 32 46 47 63 100
PM	PGOOD_P1V5_S0_DLY	11	
PM	PGOOD_1V8_S0_G1	64	
PM	PGOOD_1V8_S0_G2	64	
PM	PGOOD_P12V_S0	63	64
PM	PGOOD_P1V8_S0	64	
PM	PGOOD_PCH_S0	5	64
PM	PGOOD_PCH_S0_R	64	94
PM	PGOOD_SYSPWR0K	64	
PM	PGOOD_SYSPWR0K_R	64	
PM	POWER_BUTTON_L	47	
PM	PEG_RESET_L	9	27
PM	PGOOD_CPU_S0	64	
PM	PGOOD_CPU_UNCORE	64	94
PM	PGOOD_5V_1V05_3V3	64	94
PM	PGOOD_3V3_1V05	64	94
PM	PGOOD_12V_S0_G1	64	
PM	PGOOD_12V_S0_G2	64	
PM	9V_COMP_REF	64	
PM	12V_COMP_REF	64	
PM	ALL_SYS_PWRGD	64	94

SYNC MASTER=K62_JERRY

SYNC DATE=01/09/2011

PM RESETS ENABLES PGOOD CONST

Apple Inc.

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