

MODEL NAME : VBW01
PROJECT CODE : ANRVBW0100
PCB NO : DA8000WL000 LA-9982P M/B
DA40001FO00 LS-9101P POWER BUTTON/B
DA40001FP00 LS-9102P USB/B
DA40001FQ00 LS-9103P TP BUTTON/B

Dell / Compal Confidential

Schematic Document

Intel Shark Bay ULT
OAK Mainstream2
UMA/DIS AMD Venus Pro

2013-05-29

Rev: 3.0

X76@ : 76 level
46@ : 46 level
@ : Nopop component
CONN@ : Connector component
XDP@ : XDP function
UMA@ : Only for UMA
DIS@ : Only for Discrete
VENUS@ : VENUS Pro,VENUS XT
VENUSXT@ : VENUS XT
VENUSPRO@ : VENUS Pro
@VENUS@ : VENUS nopop component
EMI@ : EMI parts
@EMI@ : Reserve EMI parts
ESD@ : ESD parts
RF@ : RF parts

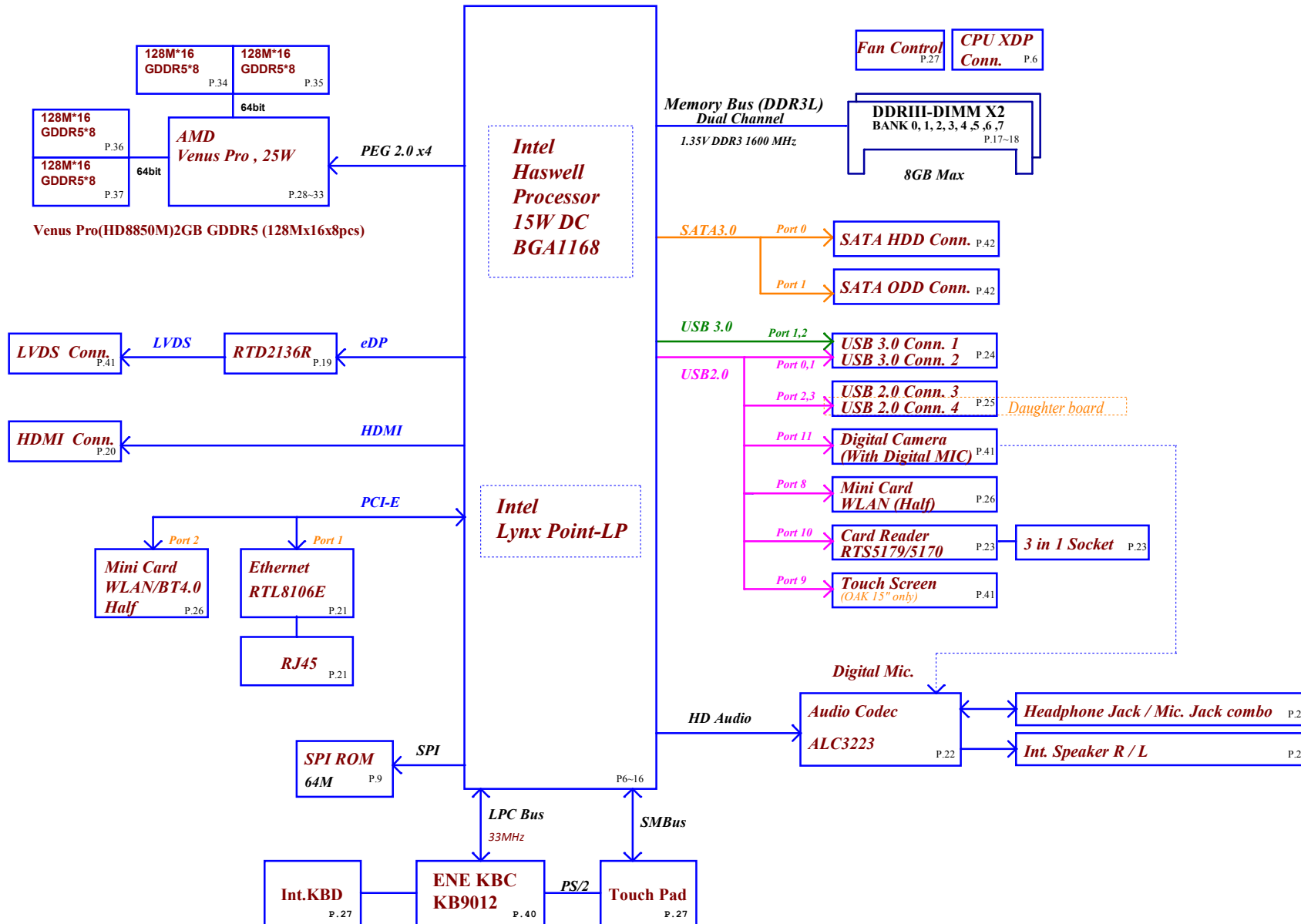
BOM config
UMA : UMA@,EMI@,ESD@,RF@
DIS VENUS : VENUS@,VENUSPRO@,DIS@,EMI@,ESD@,RF

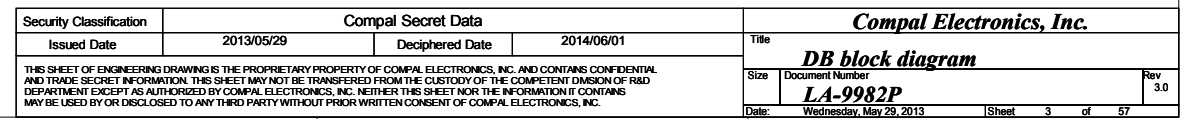
ZZZ R1@



PCB VBW01 LA9982P/LS9101P/LS9102P/LS9103P
DA20ZG00120

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/05/29	Deciphered Date	2014/06/01	Title	Cover Page
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Board ID Table for AD channel

Vcc	3.3V +/- 1%				
Ra	100K +/- 1%				
Board ID	Rb	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V	3.300V	0xE7 - 0xFF

SMBUS Control Table

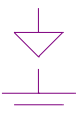
	SOURCE	BATT	Charger	RTD2136S	VGA	DDR3L	XDP	WLAN mini card	Touch pad
EC_SMB_CK1 EC_SMB_DA1	KB9012	V	V						
EC_SMB_CK2 EC_SMB_DA2	KB9012			V	V				
SMBCLK SMBDATA	ULT					V	V	V	V
SML0CLK SML0DATA	ULT								
SML1CLK SML1DATA	ULT								

Link

Board ID TABLE

ID	PCB Revision			
	UMA	Sun XT	VenusPro	VenusXT
0	SSI&A02			
1		SSI&A02		
2			SSI&A02	
3				SSI&A02
4	PT			
5		PT		
6			PT	
7				PT
8	ST			
9		ST		
10			ST	
11				ST
12	XB			
13		XB		
14			XB	
15				XB
16	A01			
17		A01		
18			A01	
19				A01

Symbol Note :



: means Digital Ground



: means Analog Ground

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ULT

USB3.0	
Port1	USB connector 2
Port2	USB connector 1
Port3	
Port4	
USB2.0	
Port0	USB connector 2
Port1	USB connector 1
Port2	USB connector 3
Port3	USB connector 4 (DB)
Port4	MINI Card (WLAN)
Port5	Touch Screen Panel
Port6	Card Reader
Port7	Camera
PCI EXPRESS	
Lane 1	
Lane 2	
Lane 3	10/100 LAN
Lane 4	MINI Card (WLAN)
Lane 5	PEG (N14P)
Lane 6	PEG (N14P)
SATA	
SATA0	HDD
SATA1	ODD
SATA2	
SATA3	

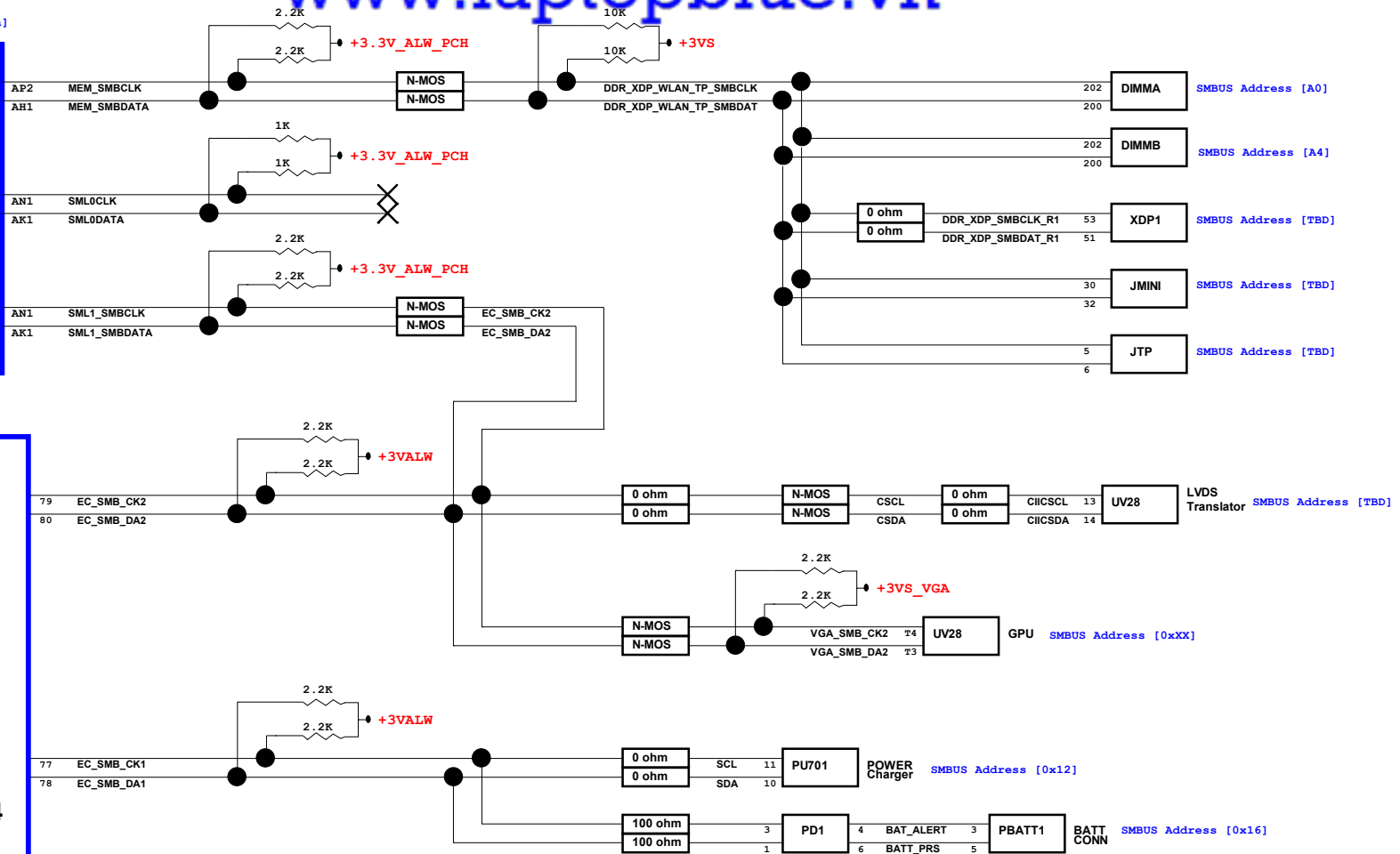
CLOCK SIGNAL	
CLKOUT_PCIE0	
CLKOUT_PCIE1	
CLKOUT_PCIE2	10/100 LAN
CLKOUT_PCIE3	MINI Card (WLAN)
CLKOUT_PCIE4	dGPU
CLKOUT_PCIE5	

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SMBUS Address [0x9a]

MCH
Shark bay

KBC
KB9012A4



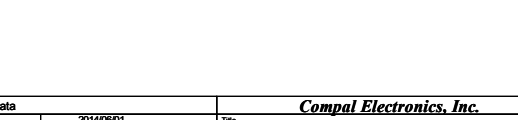
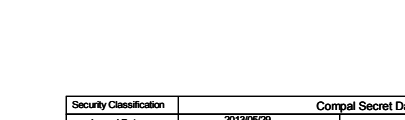
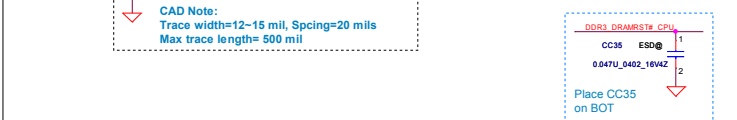
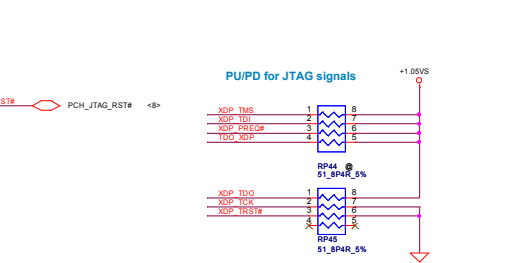
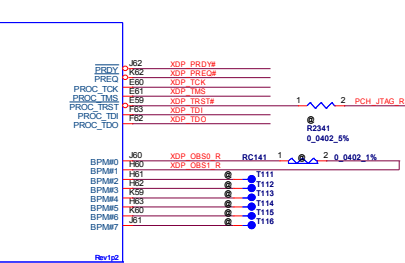
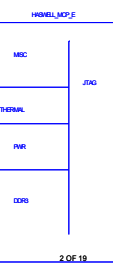
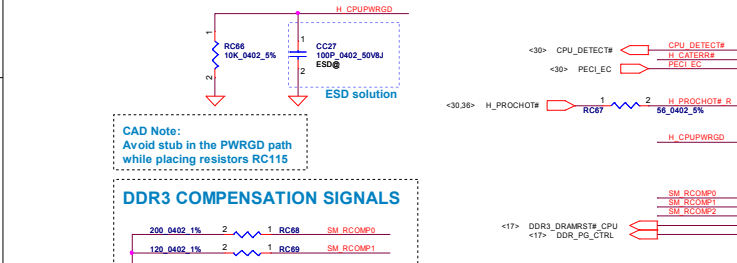
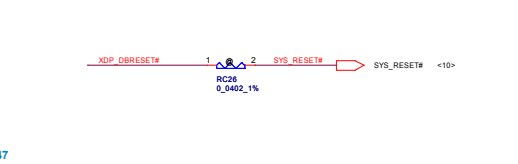
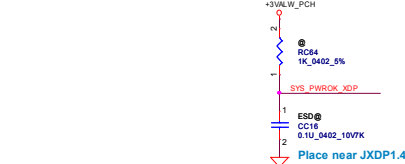
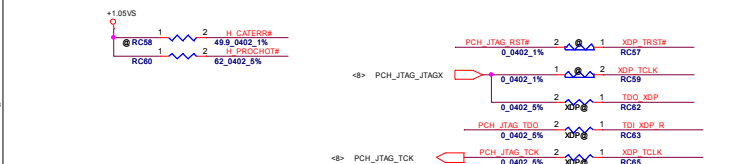
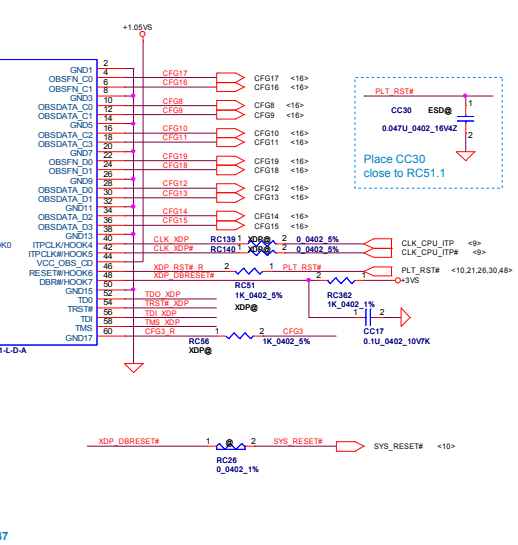
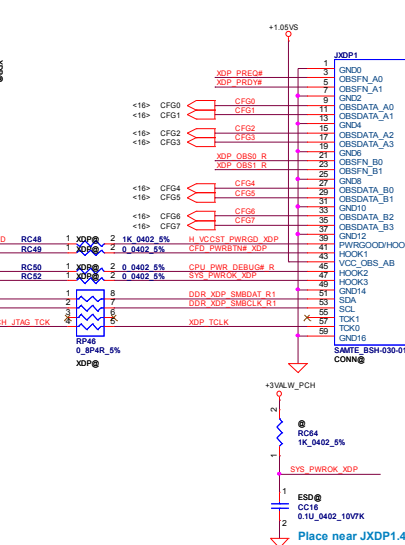
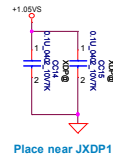
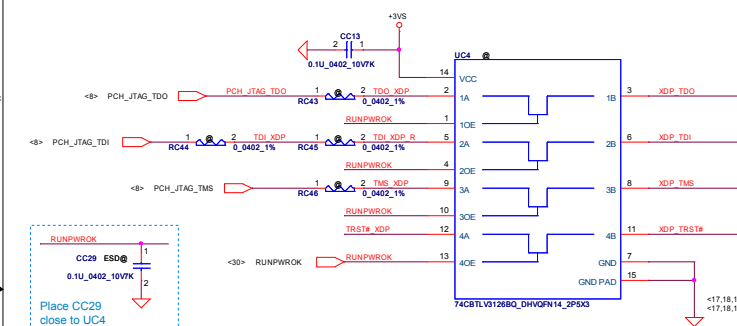
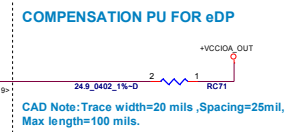
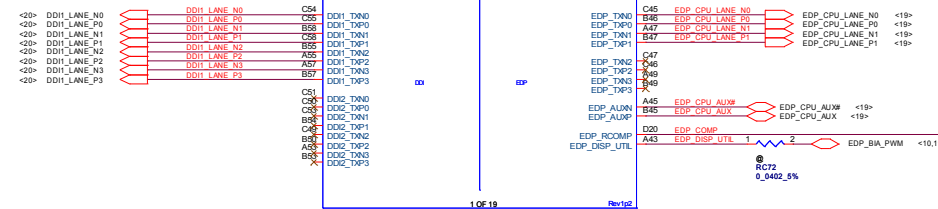
i3-4010U-15W-GT2-MP



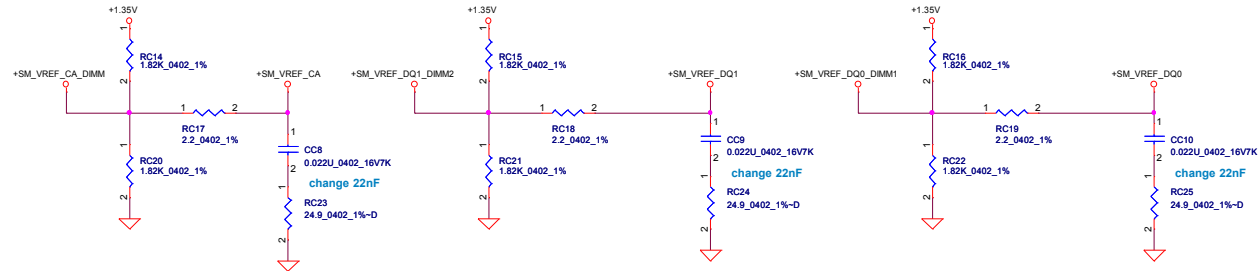
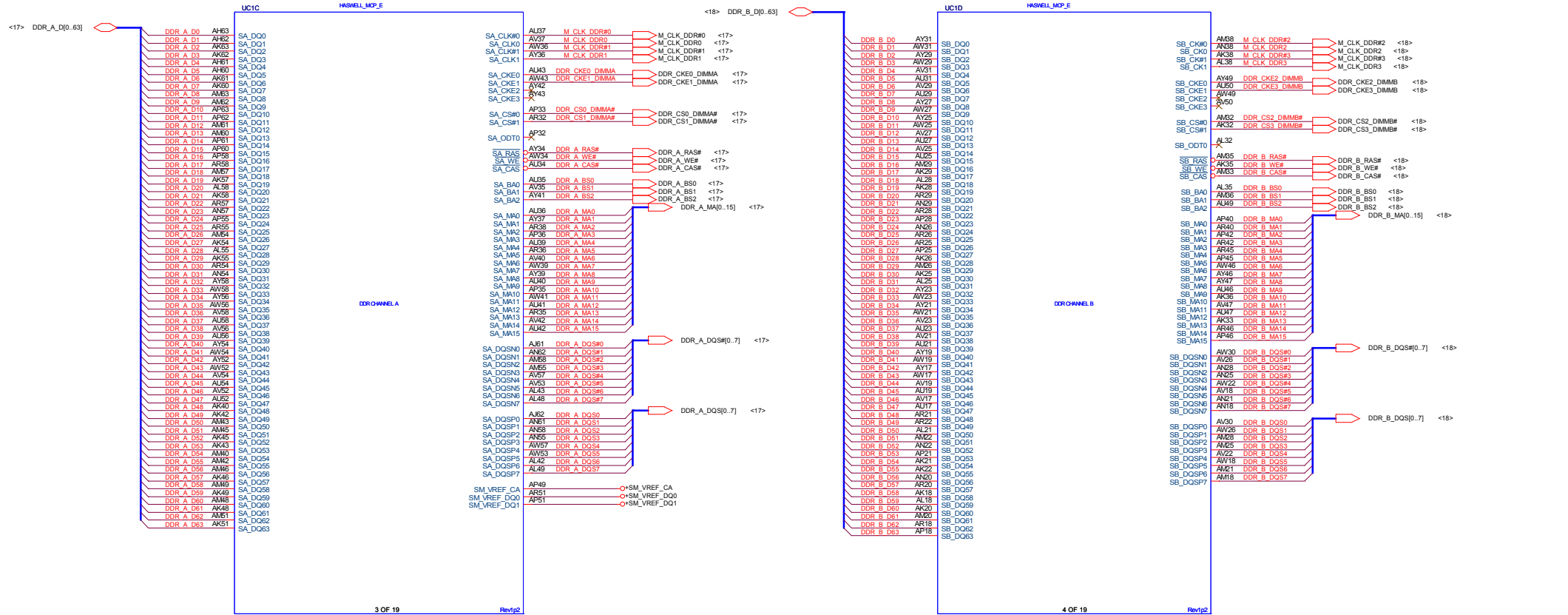
i5-4200U-15W-GT2-MP



i7-4500U-15W-GT2-MP

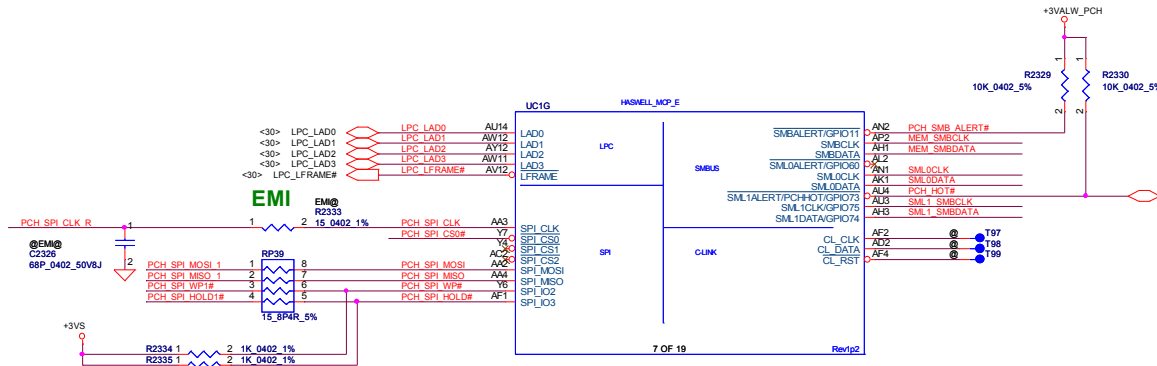


Security Classification	2013/05/29	Compal Secret Data	Deciphered Date	2014/06/01
Issued Date	2013/05/29	Deciphered Date	2014/06/01	
Title				
MCP(1,2/19) eDP.XDP.MISC				
Site				
I/A-9982P				
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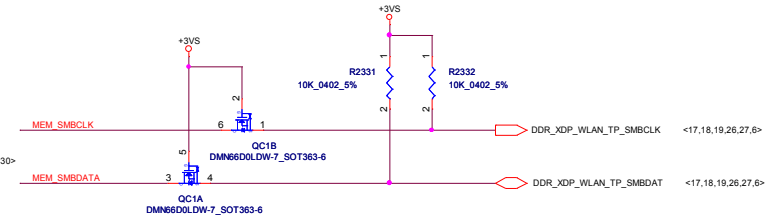


confirm by intel request PDG P141

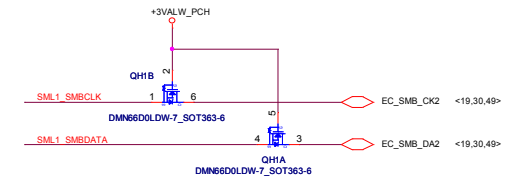
Security Classification		Compal Secret Data		Title	
Issued Date	2013/05/29	Deciphered Date	2014/06/01	MCP(3,4/19) DDR3	
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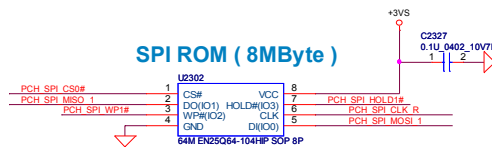
MEM Bus : DDR/XDP/WLAN/TP



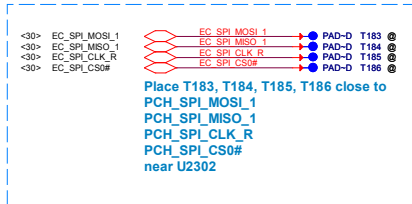
SML1 Bus : EC/Sensors



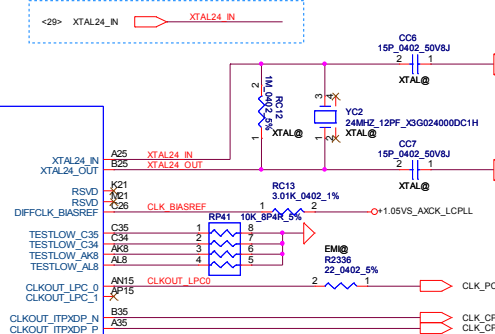
SPI ROM (8MByte)



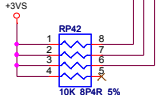
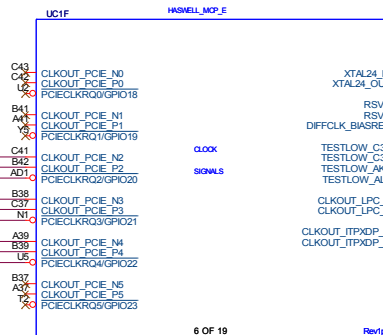
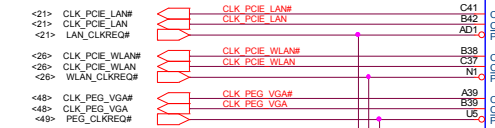
PN : SA000046400 ,64M,EN25Q64-104HIP



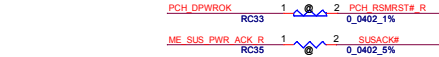
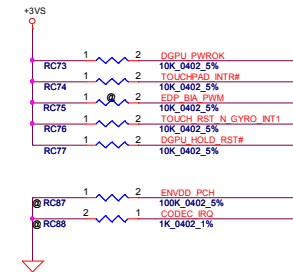
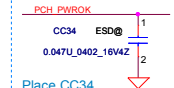
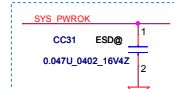
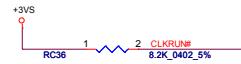
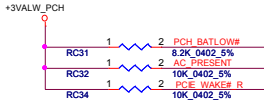
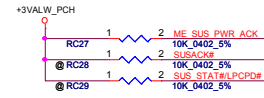
For GCLK



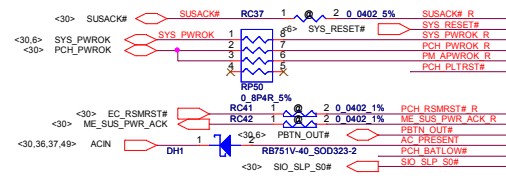
10/100 LAN ----->
WLAN (Mini Card) ---->
dGPU ---->



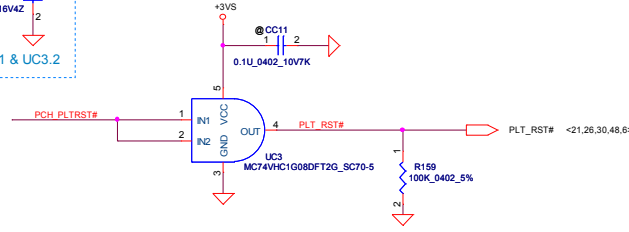
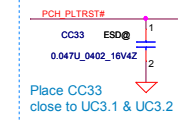
Security Classification		Compal Secret Data		Title	
Issued Date	2013/05/29	Deciphered Date	2014/06/01	MCP(6,7/19) CLK,SMB,SPI,LPC	
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Note: SUSACK# and SUSWARN# can be tied together if EC does not want to involve in the handshake mechanism for the Deep Sleep state entry and exit CAN be NC ,if not support Deep Sx

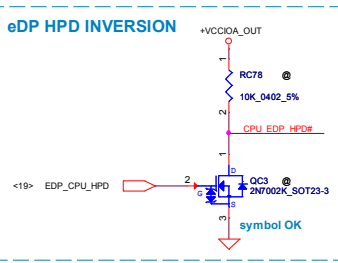
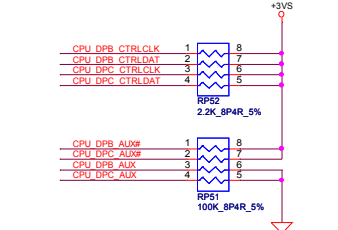
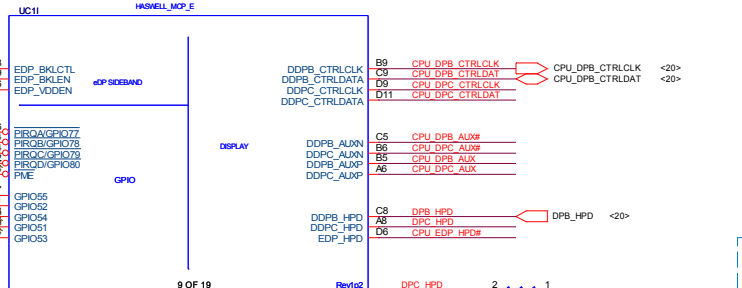
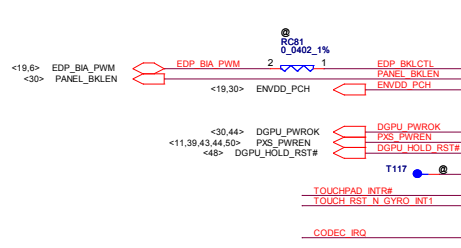
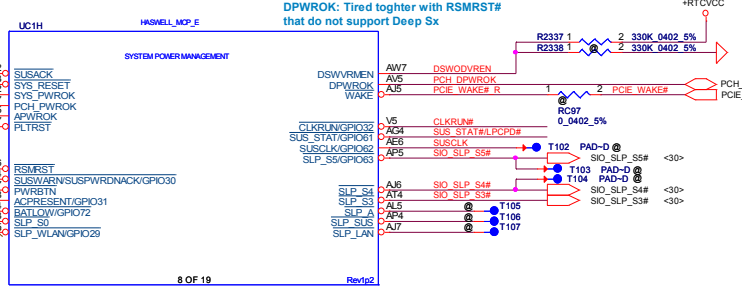


PCH_BATLOW# Need pull high to VCCDSW3_3 (If no deep Sx , connect to VCCSUS3_3)



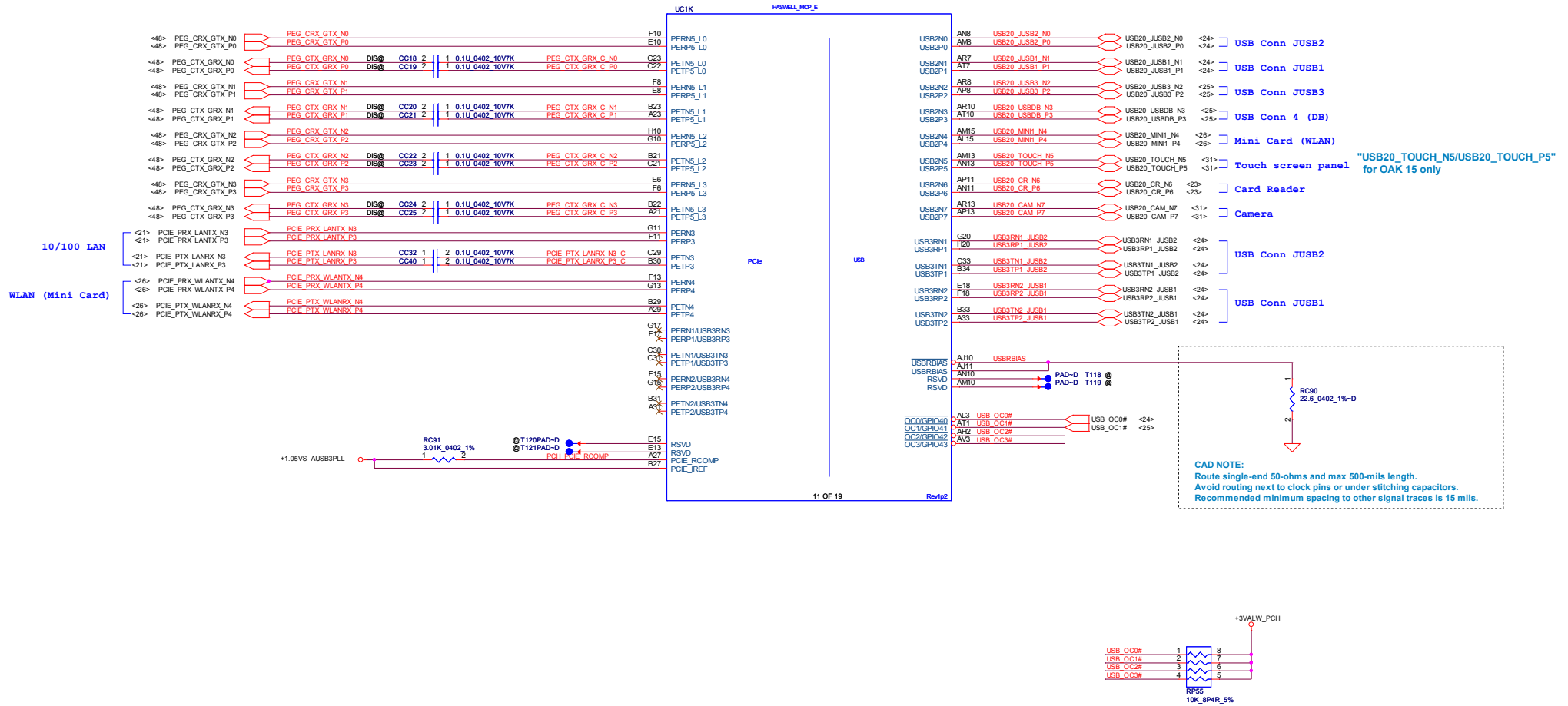
DSWODVREN - On Die DSW VR Enable
* H : Enable(DEFAULT)
L : Disable

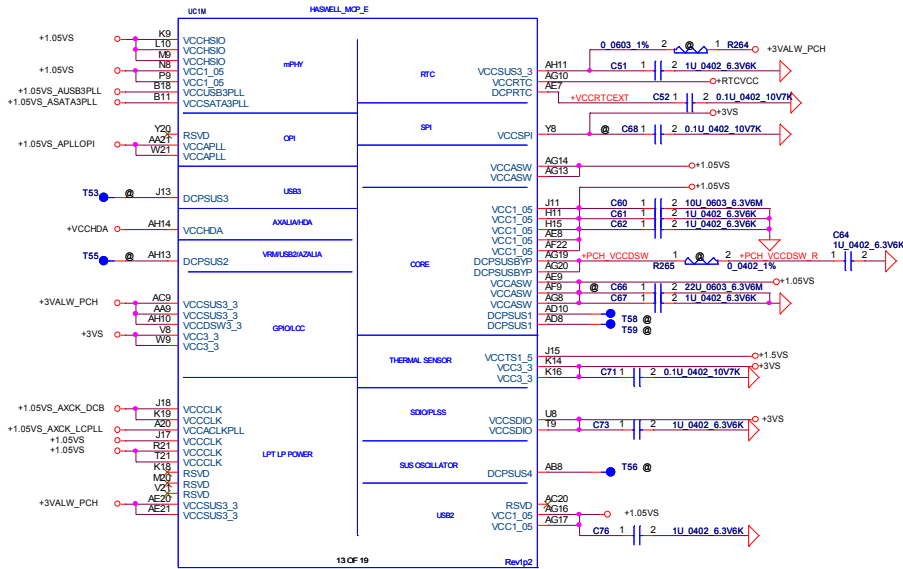
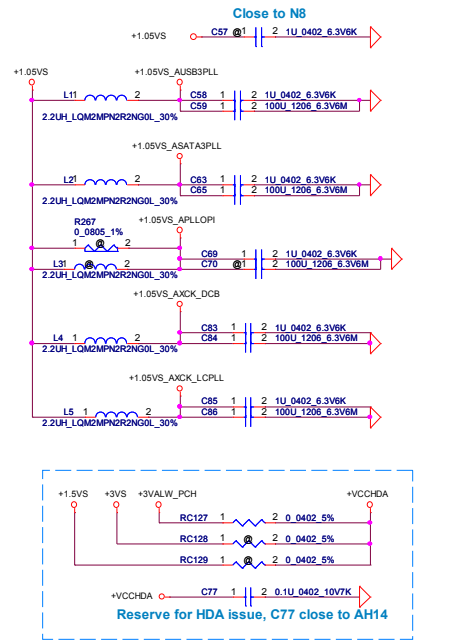
DSWODVREN - ON DIE DSW VR ENABLE
HIGH = ENABLED (DEFAULT)
LOW = DISABLED

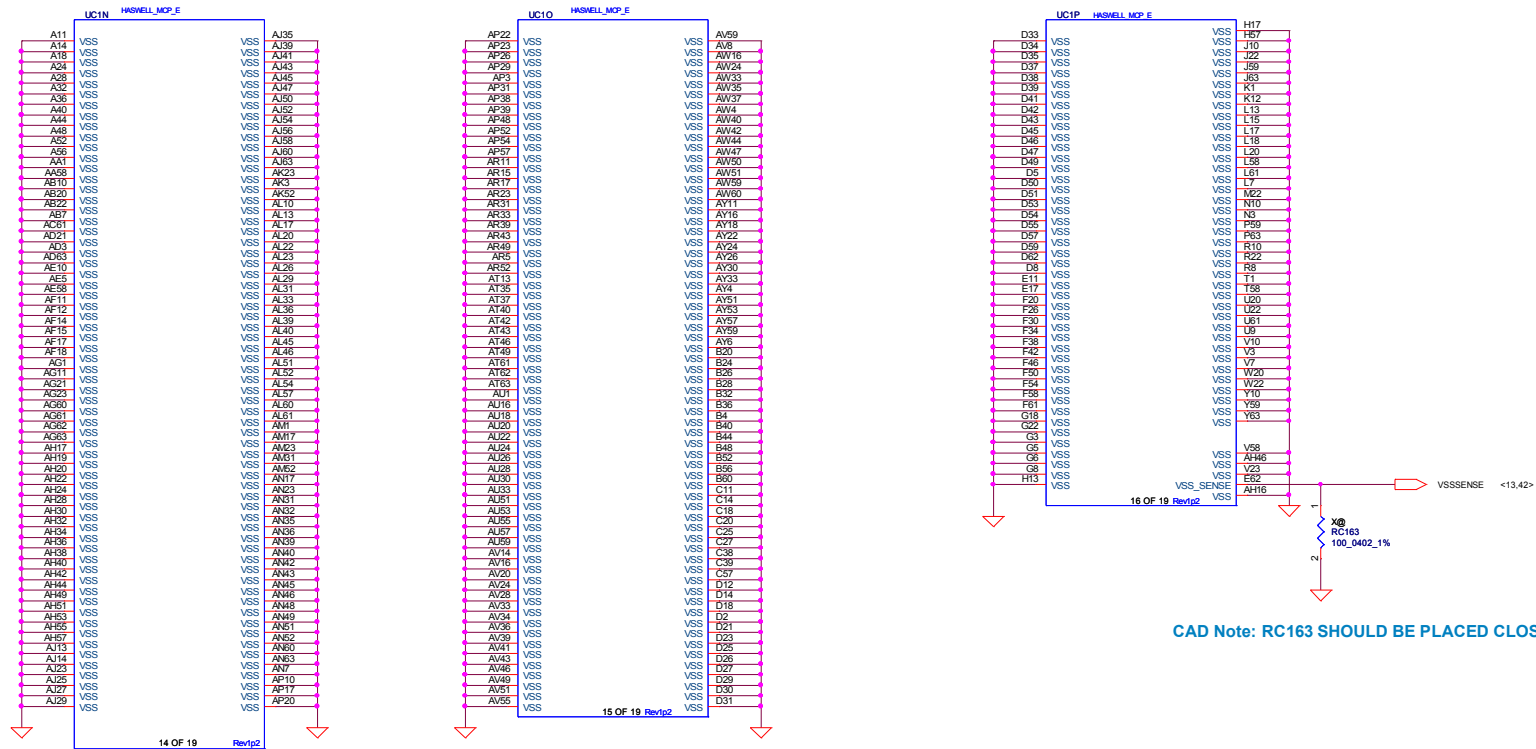


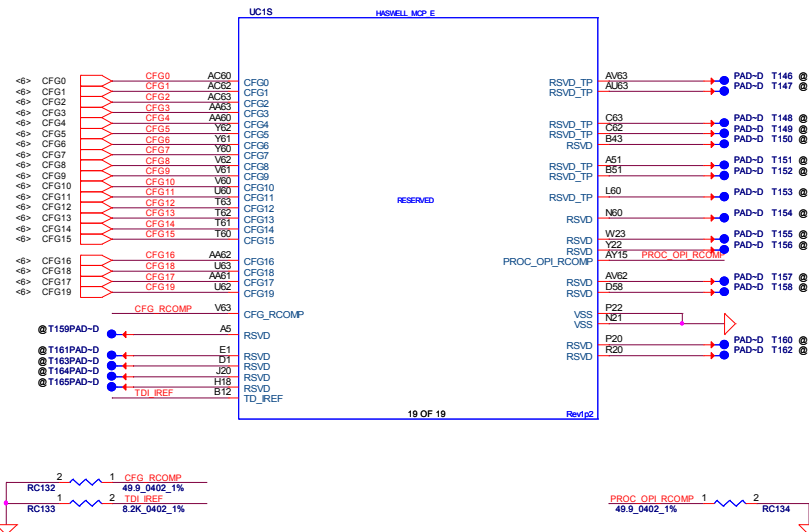
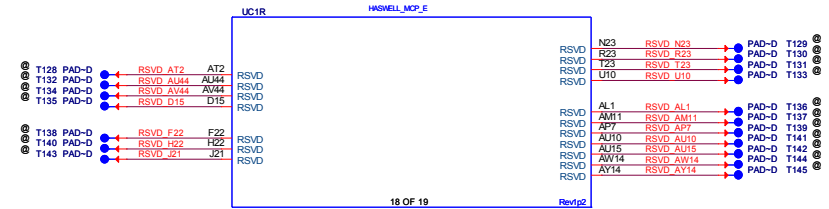
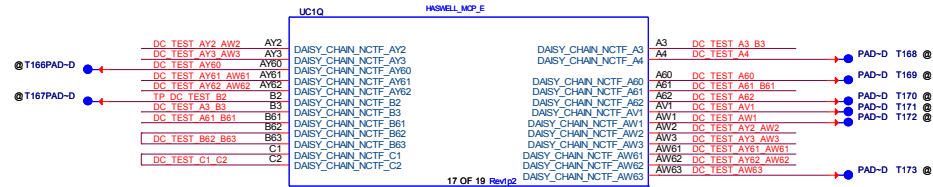
EDP_CPU_HPD 1 2 CPU_EDP_HPD#
0_0402_5% Reserve for eDP

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Issued Date		Deciphered Date		MCP(8,9/19) DDLEDP.GPIO	
2013/05/29		2014/06/01		Size	
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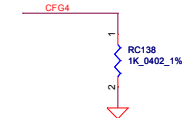








CFG STRAPS for CPU



Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port
	0: Enabled; An external Display Port device is connected to the Embedded Display Port

H=4mm

2-3A to 1 DIMMs/channel

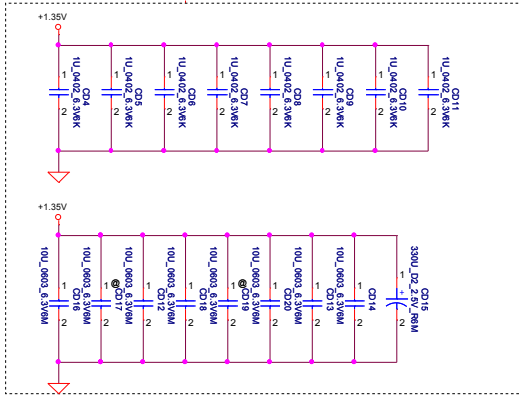
Populate RD1, De-Populate RD7 for Intel DDR3 VREFDQ multiple methods M1
Populate RD7, De-Populate RD1 for Intel DDR3 VREFDQ multiple methods M3

<7> DDR_A_DQS#(0..7)
<7> DDR_A_DQ(0..63)
<7> DDR_A_DQS(0..7)
<7> DDR_A_MA(0..15)

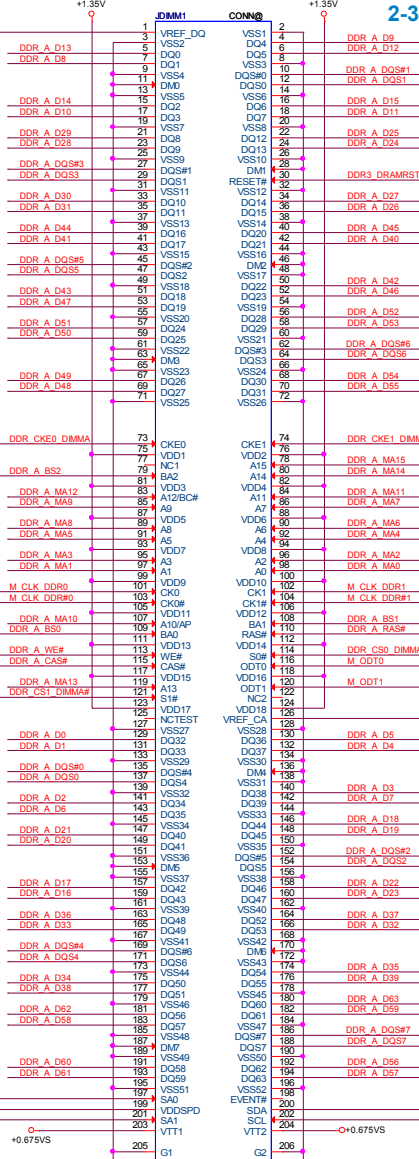
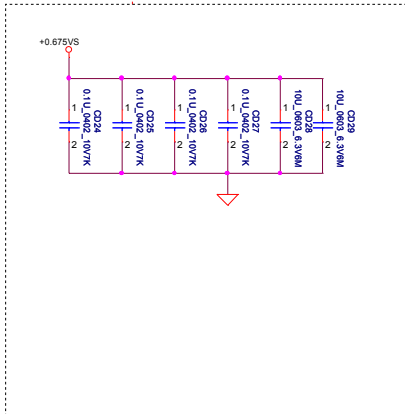
All VREF traces should have 10 mil trace width

Layout Note:
Place near JDIMM1

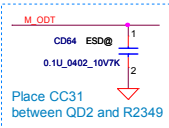
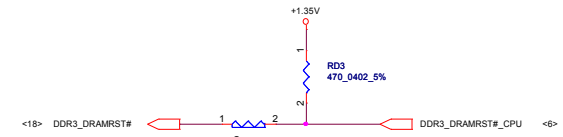
Note:
Check voltage tolerance of VREF_DQ at the DIMM socket



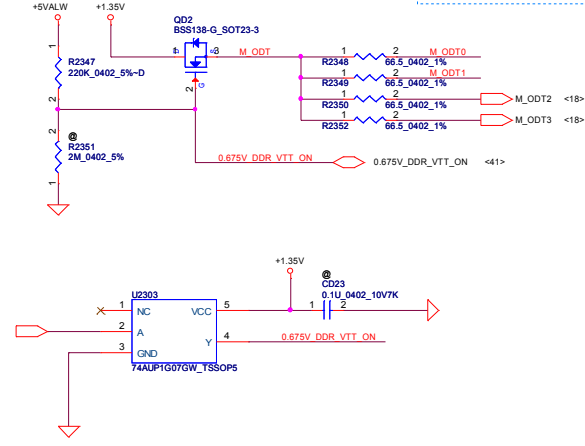
Layout Note:
Place near JDIMM1.203,204



CAD NOTE
PLACE THE CAP NEAR TO DIMM RESET PIN



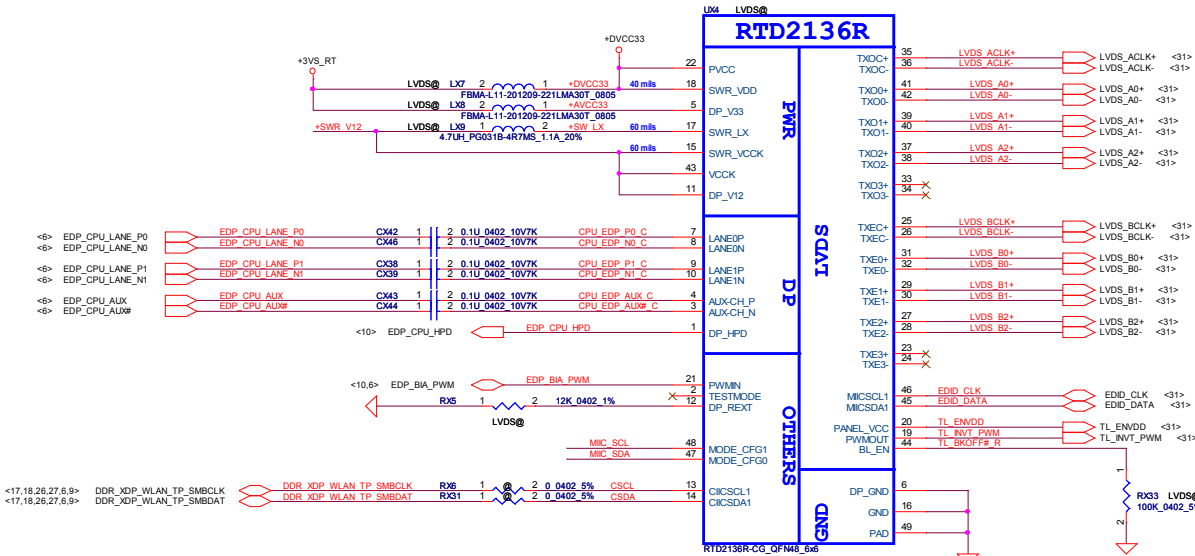
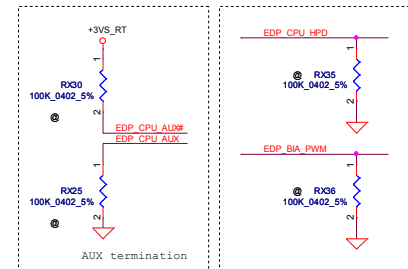
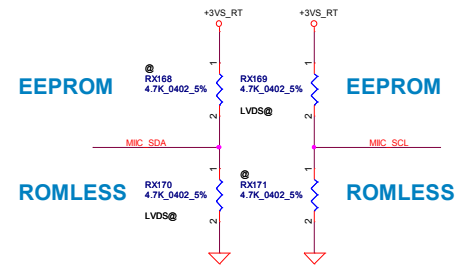
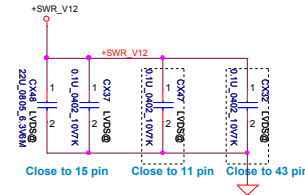
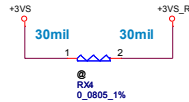
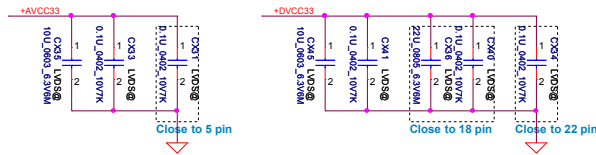
DDR3L SODIMM ODT GENERATION



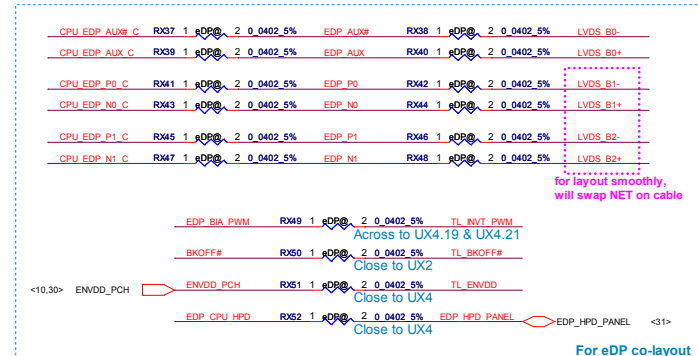
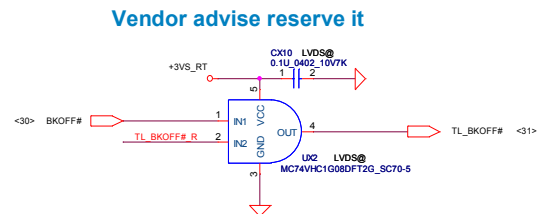
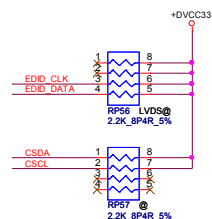
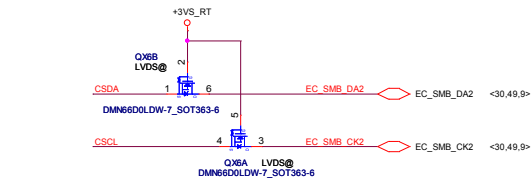
Security Classification		Compal Secret Data		Title	
Issued Date	2013/05/29	Deciphered Date	2014/06/01	DDR3L DIMM	
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				17	LA-9982P
				Date	Wednesday, May 29, 2013
				Sheet	17 of 57

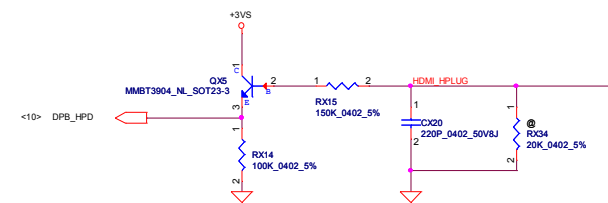
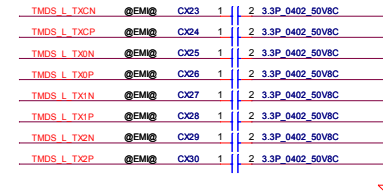
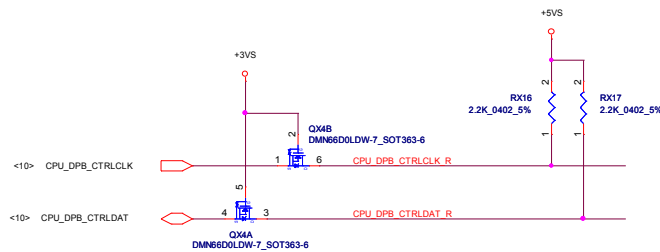
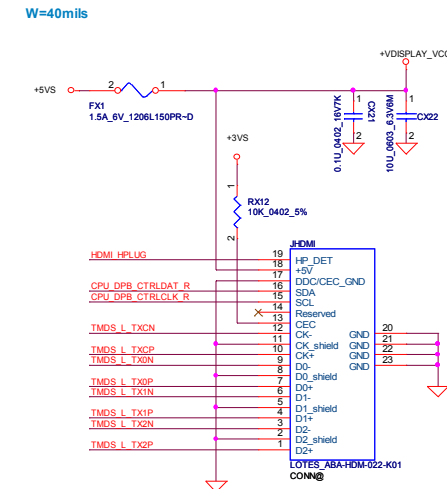
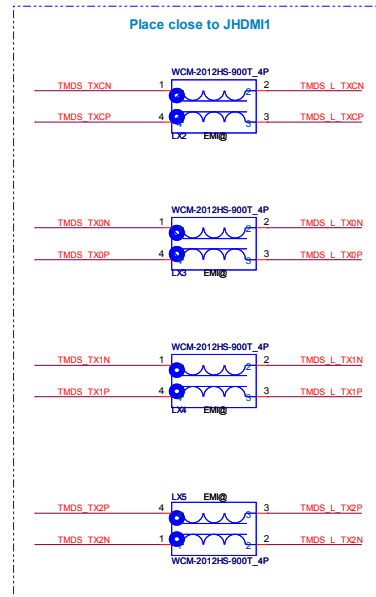
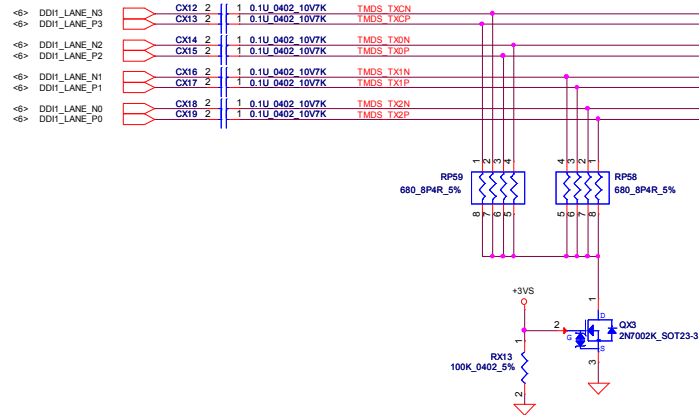


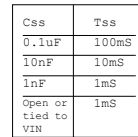
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RTD2136S : SA00004NW10
RTD2136R : SA000067100







TL1

16 MDI4- MDI4+

15 MCT2- MCT2+

14 MDI3- MDI3+

13 MCT1- MCT1+

12 MDI2- MDI2+

11 MDI1- MDI1+

10 NC NC

9 NC NC

8 TD+ TX

7 TD- TX

6 NC NC

5 NC NC

4 MDI1- MDI1+


3 MDI1+ MDI1-

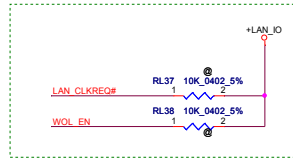
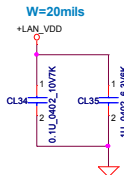
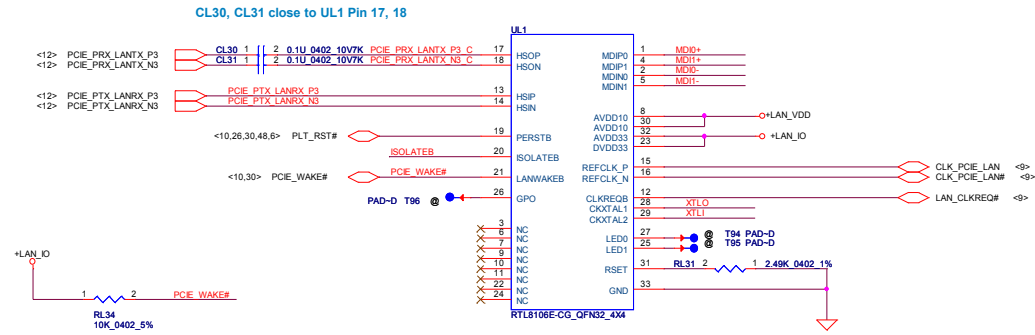
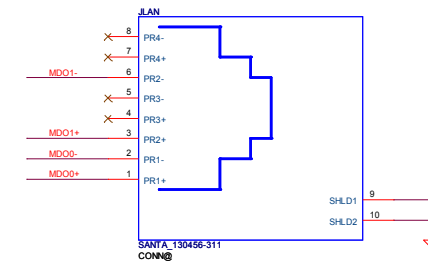
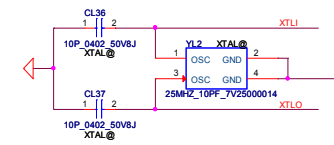
2 CL41 0.01uF 16V7K

1

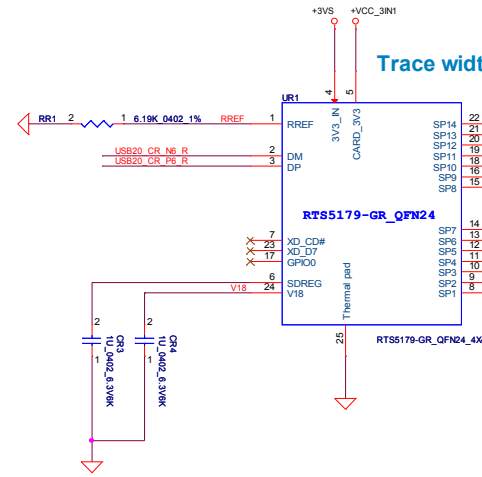
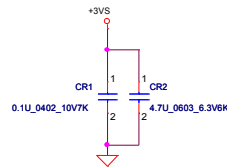
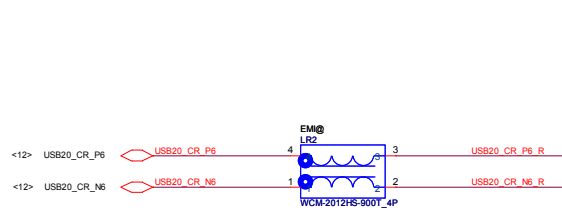
XFORM_NS0014

Change CPN to SP050
Need CIS symbol

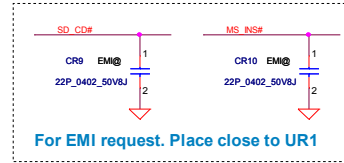
<29> XTLI  XTLI



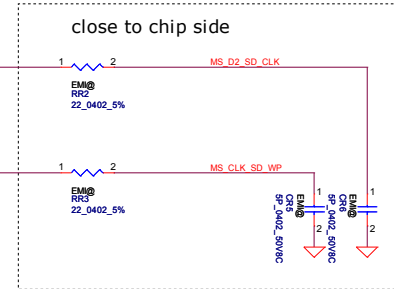
Reserve 10K pull LAN_IO



Trace width:40mil

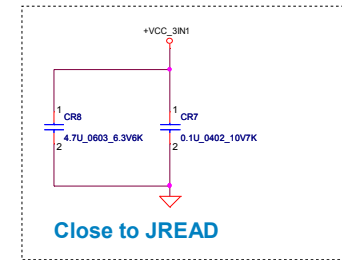


For EMI request. Place close to UR1

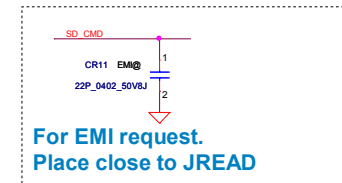


拉MS_D2_SD_CLK到Conn pin 13 SD_CLK
再打Via拉到pin 10 MS_D2

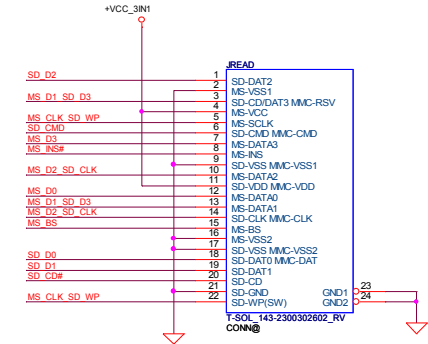
拉MS_CLK_SD_WP到Conn pin 5 MS_CLK
再打Via拉到pin 20 SD_W

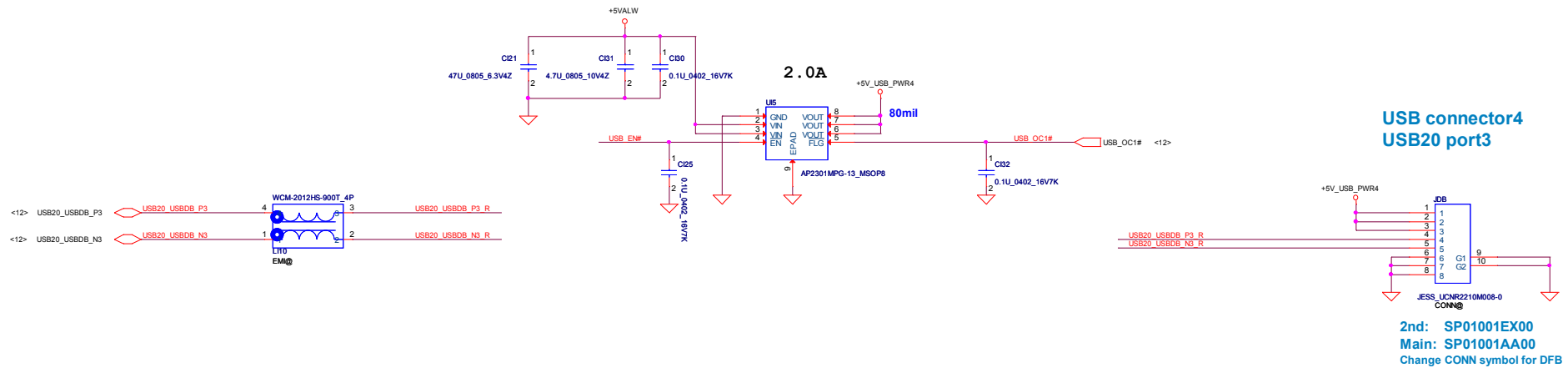
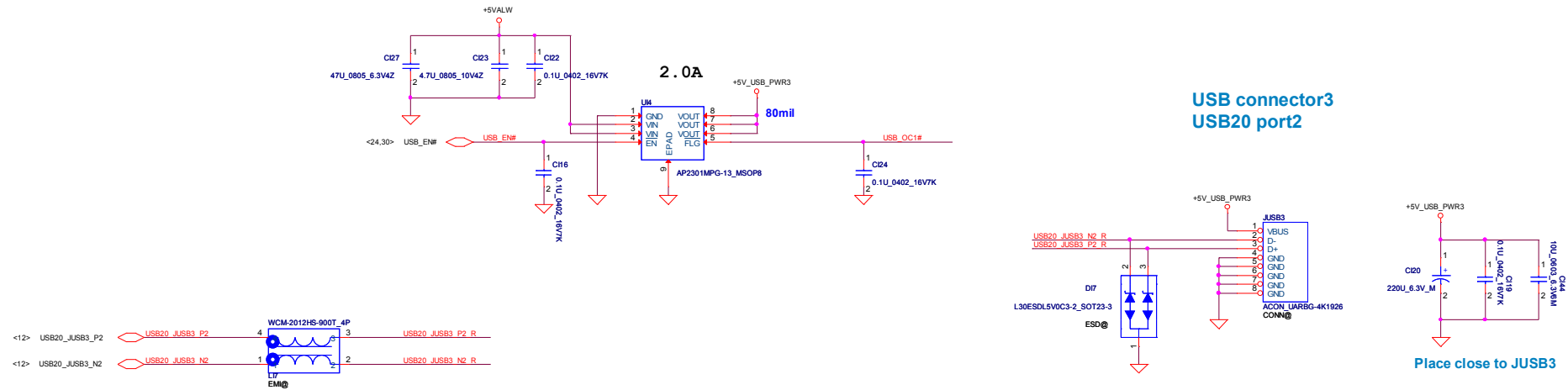


Close to JREAD

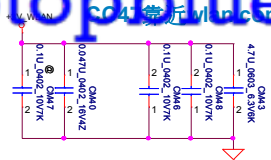


For EMI request.
Place close to JREAD

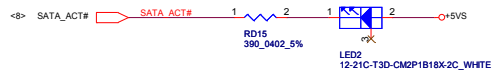




Mini WLAN/WIMAX H=6.7



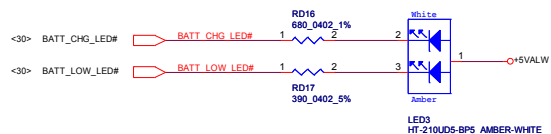
HDD LED



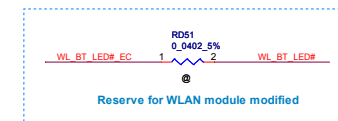
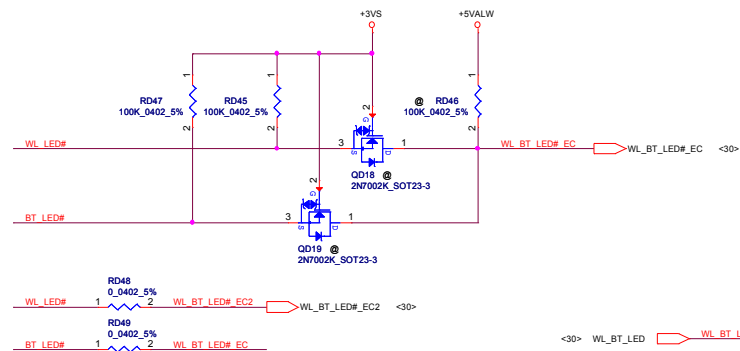
Power LED



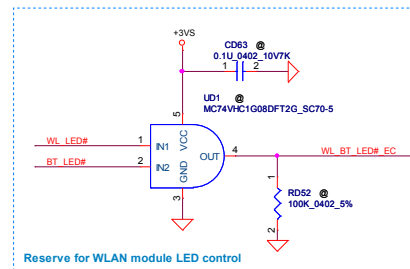
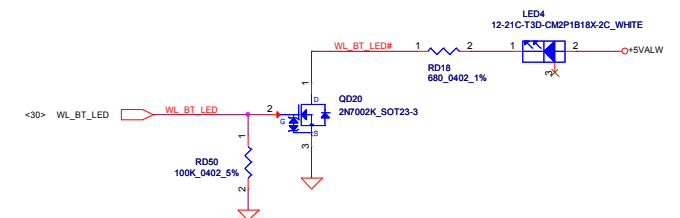
Battery LED



10mils, All pins

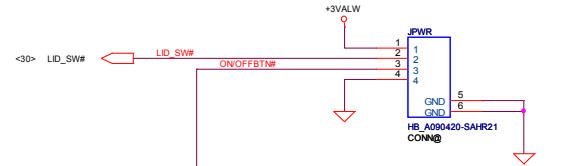


Wireless LED



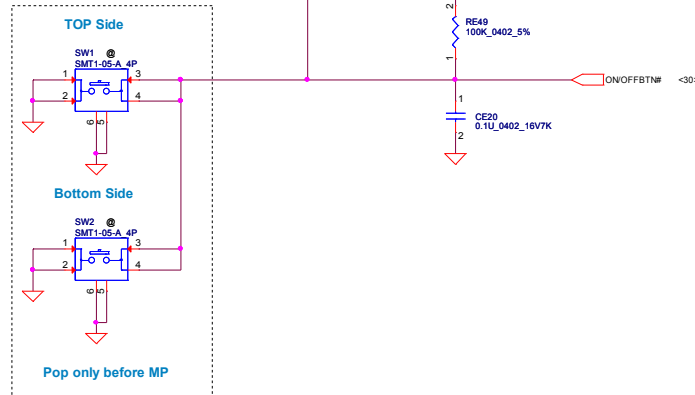
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/05/29	Deciphered Date	2014/06/01	Title	Mini Card/LED
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Date: Wednesday, May 29, 2013				Sheet	26 of 57

POWER/B



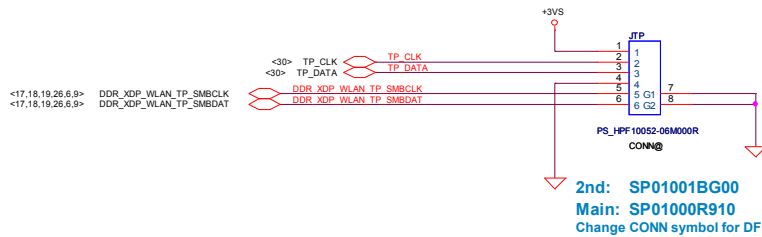
Power ON Circuit

ON/OFF switch

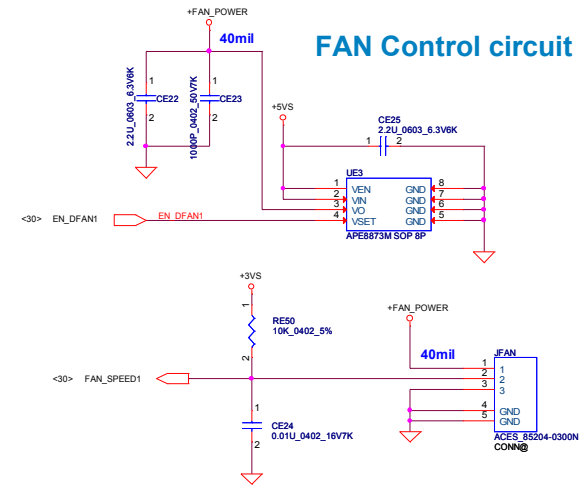


Pop only before MP

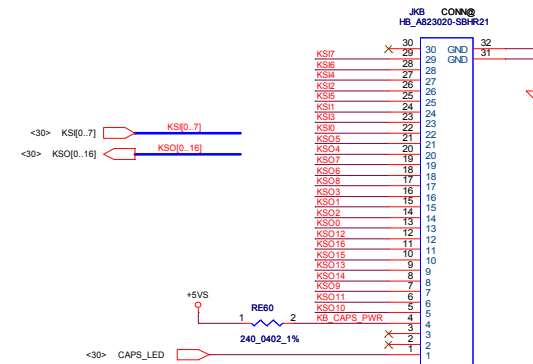
Touch pad



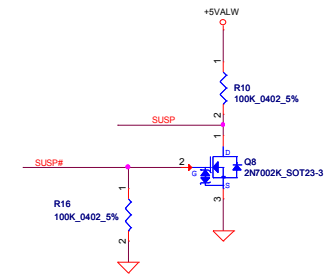
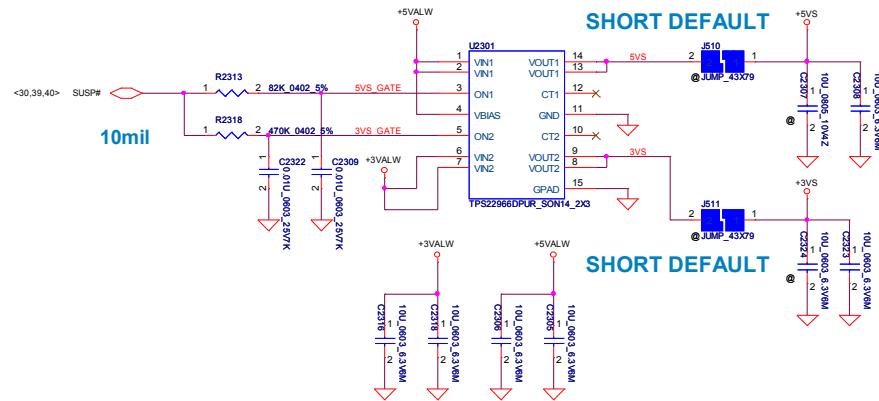
FAN Control circuit



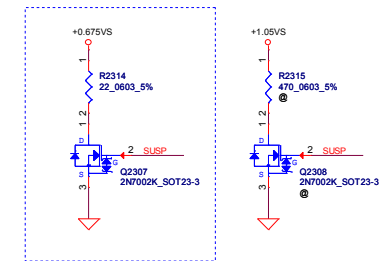
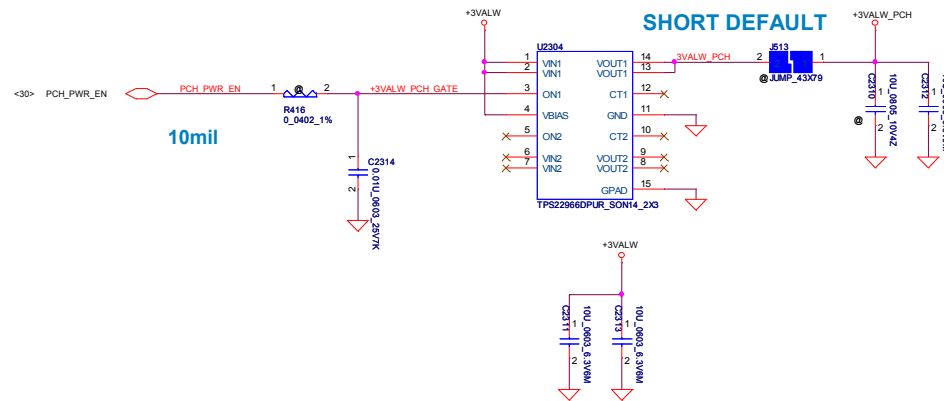
INT_KBD Connector



+5VS and +3VS switch

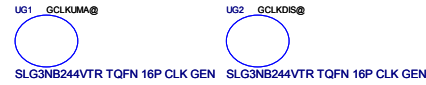
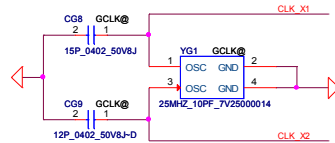
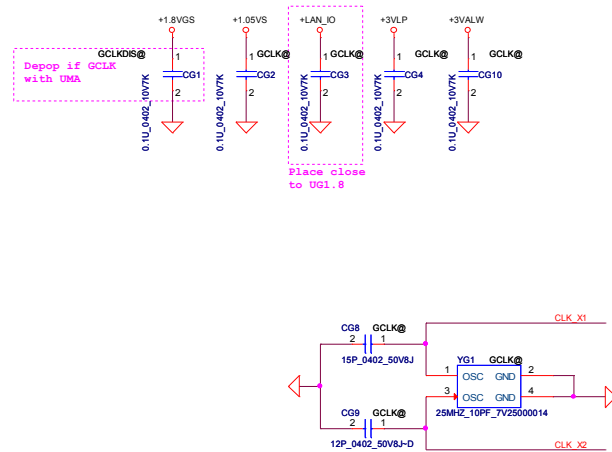


+3VALW_PCH switch

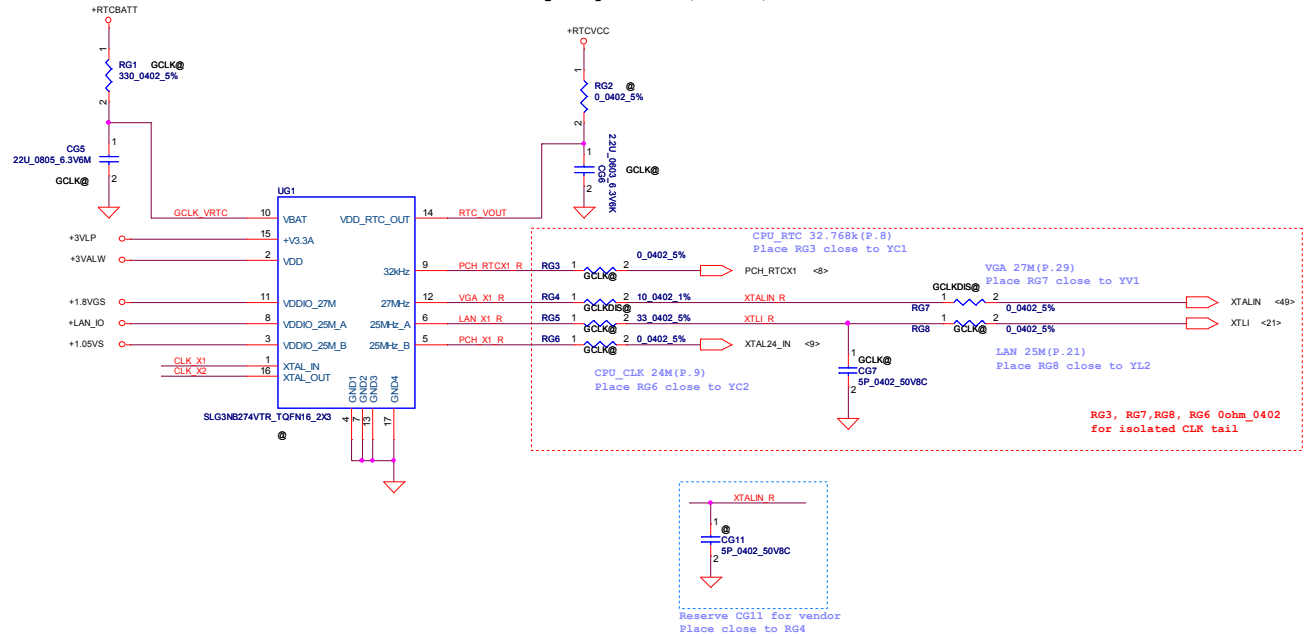


For Intel S3 Power Reduction

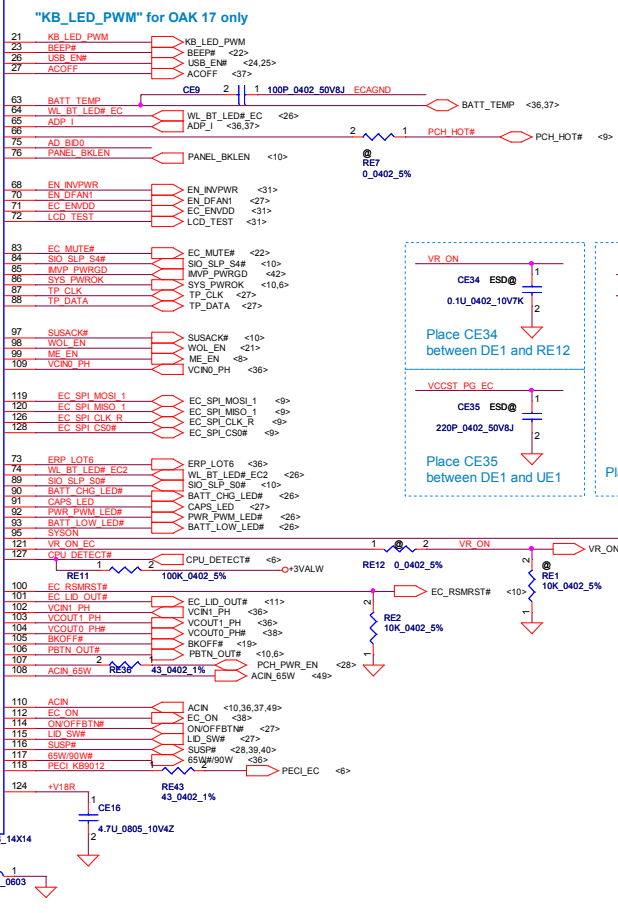
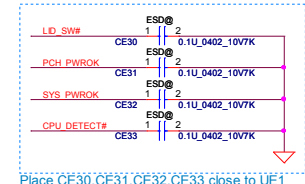
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/05/29	Deciphered Date	2014/06/01	Title	DC/DC Interface
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SLG3NB3374V is for DIS by output 24M*1, 25M*1, 27M*1, 32K*1
SLG3NB3375V is for UMA by output 24M81, 25M*1, 32K*1



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Issued Date	2013/05/29	Deciphered Date	2014/06/01	Title	GCLK
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				Date	Wednesday, May 29, 2013
				Sheet	23 of 57
				Rev	3.0



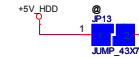
**KB9012A3 change to
KB9012A4 SA00004OB30**

Security Classification		Compal Secret Data		<i>Compal Electronics, Inc.</i> EC ENE-KB9012	
Issued Date	2013/05/29	Deciphered Date	2014/06/01	Title	LA-9982P
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				Date:	Wednesday, May 29, 2013
				Sheet	30 of 57

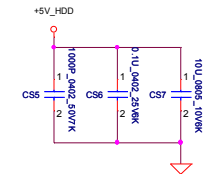
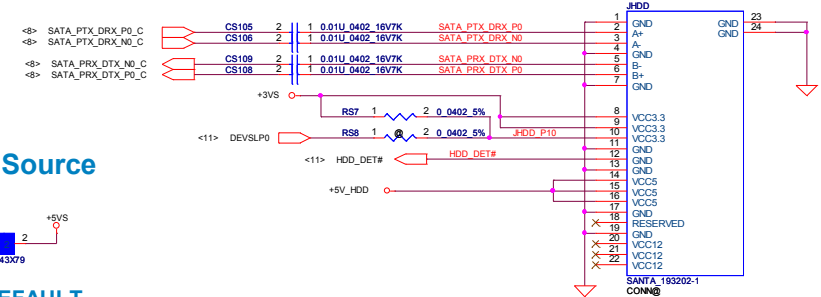
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/05/29	Deciphered Date	2014/06/01	Title	<i>LVDS/webcam/touch</i>
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					<i>LA-9982P</i>
Date:		Wednesday, May 29, 2013		Sheet	31 of 57

SATA HDD Connector

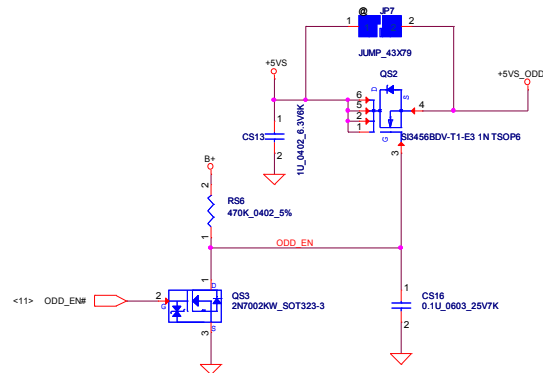
+5V_HDD Source



SHORT DEFAULT

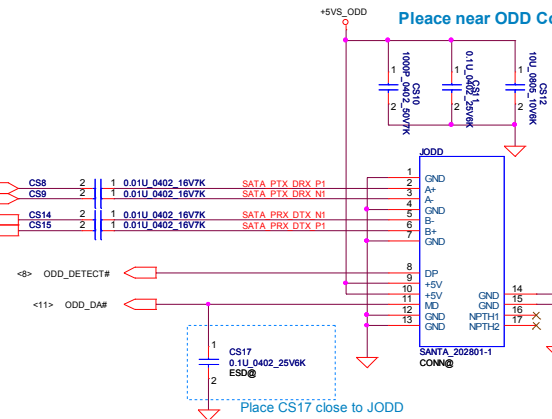


ODD Power Control

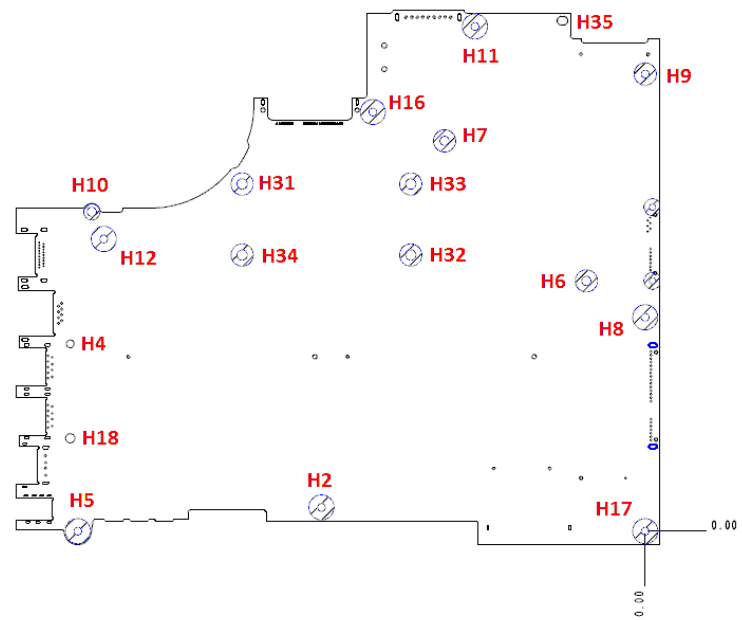
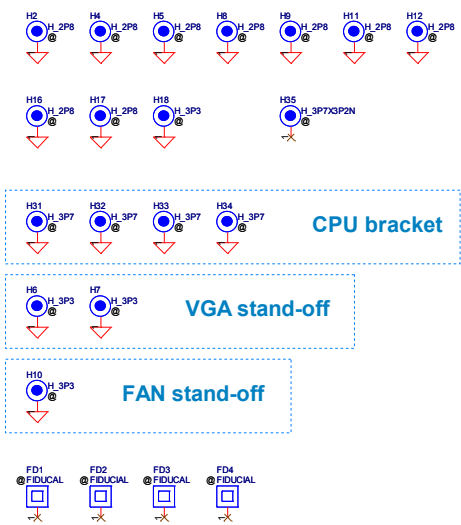


SATA ODD Connector

Please near ODD Connector

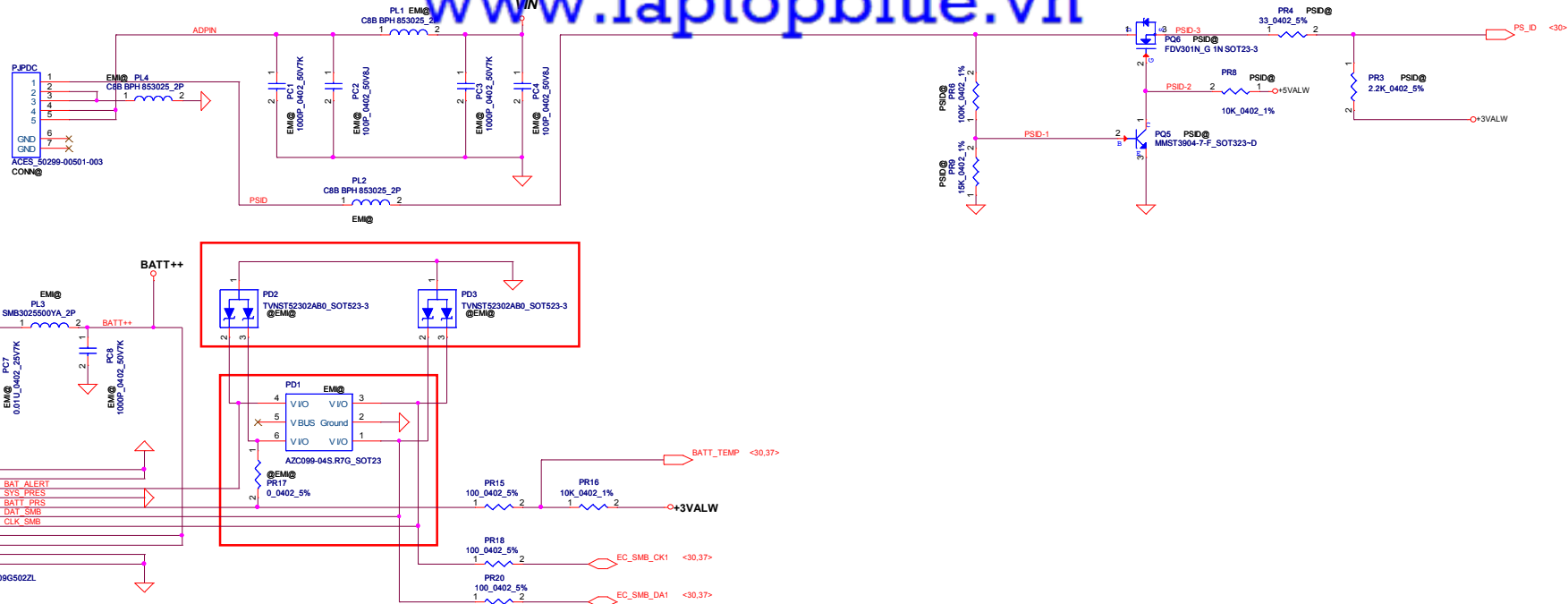


Screw Hole



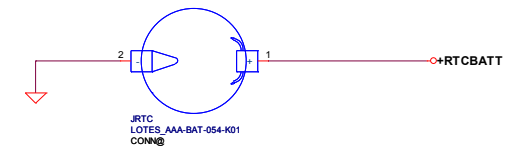
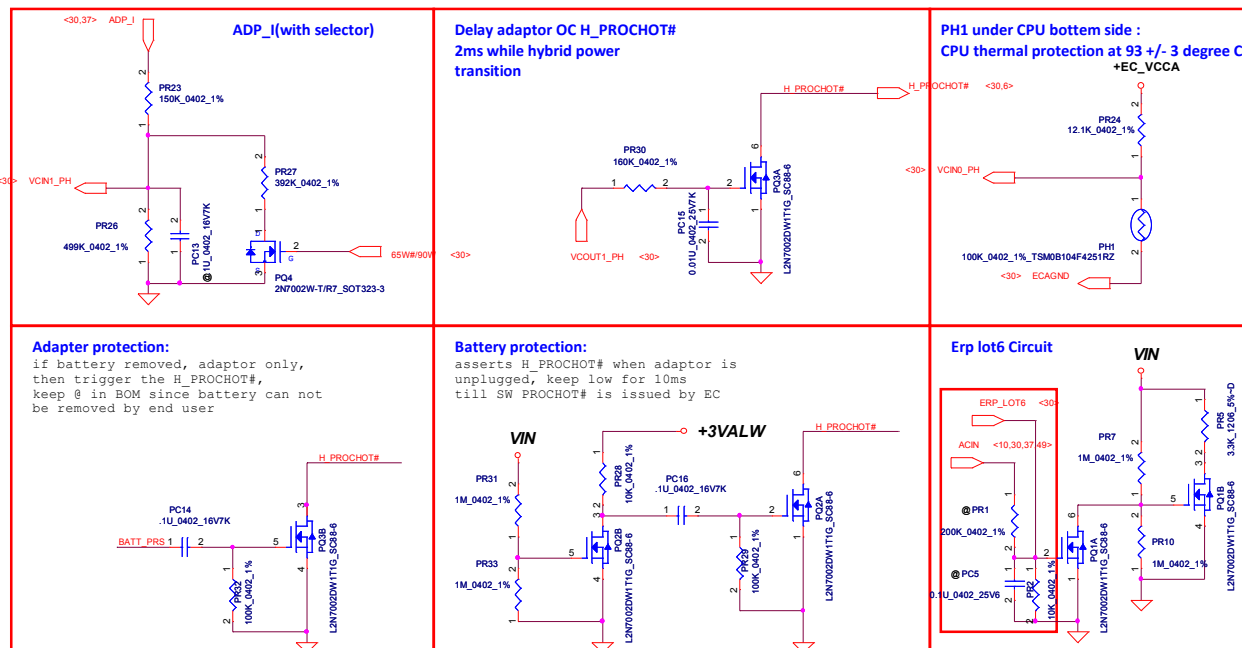
Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	34	Card Reader	2012/04/27	HW	The Card reader USB signal is incorrect.	SWAP UR1 USB signal P/N	0.2
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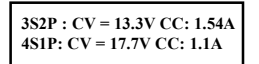
Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
40							
41							
42							
43							
44							
45							
46							
47							
48							
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50							
51							
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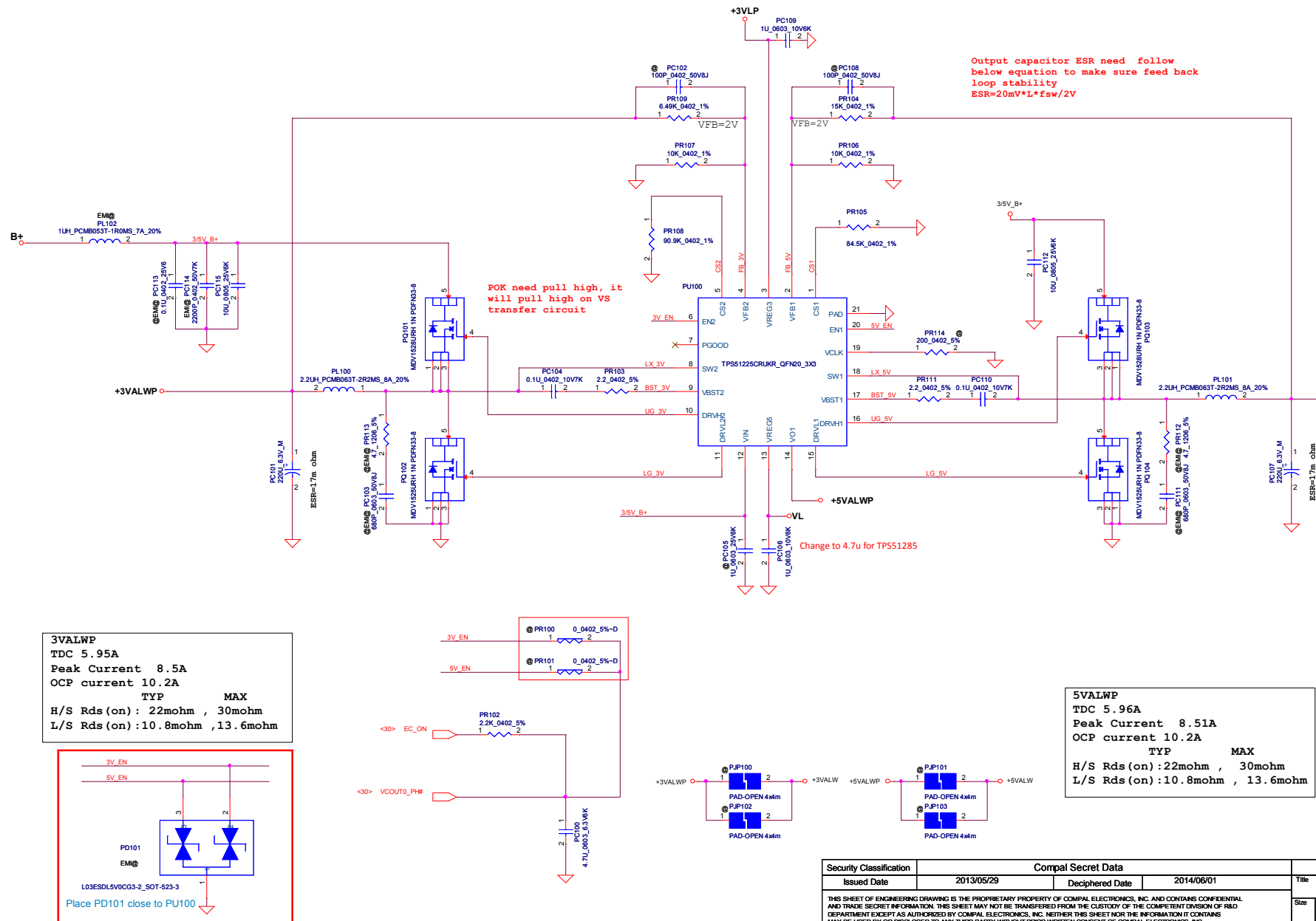
SMART
Battery:
01.GND1
02.GND2
03.BAT_ALERT
04.SYS_PRES
05.BATT_PRS
06.DAT_SMB
07.CLK_SMB
08.BATT1+
09.BATT2+

Other component (37.1)

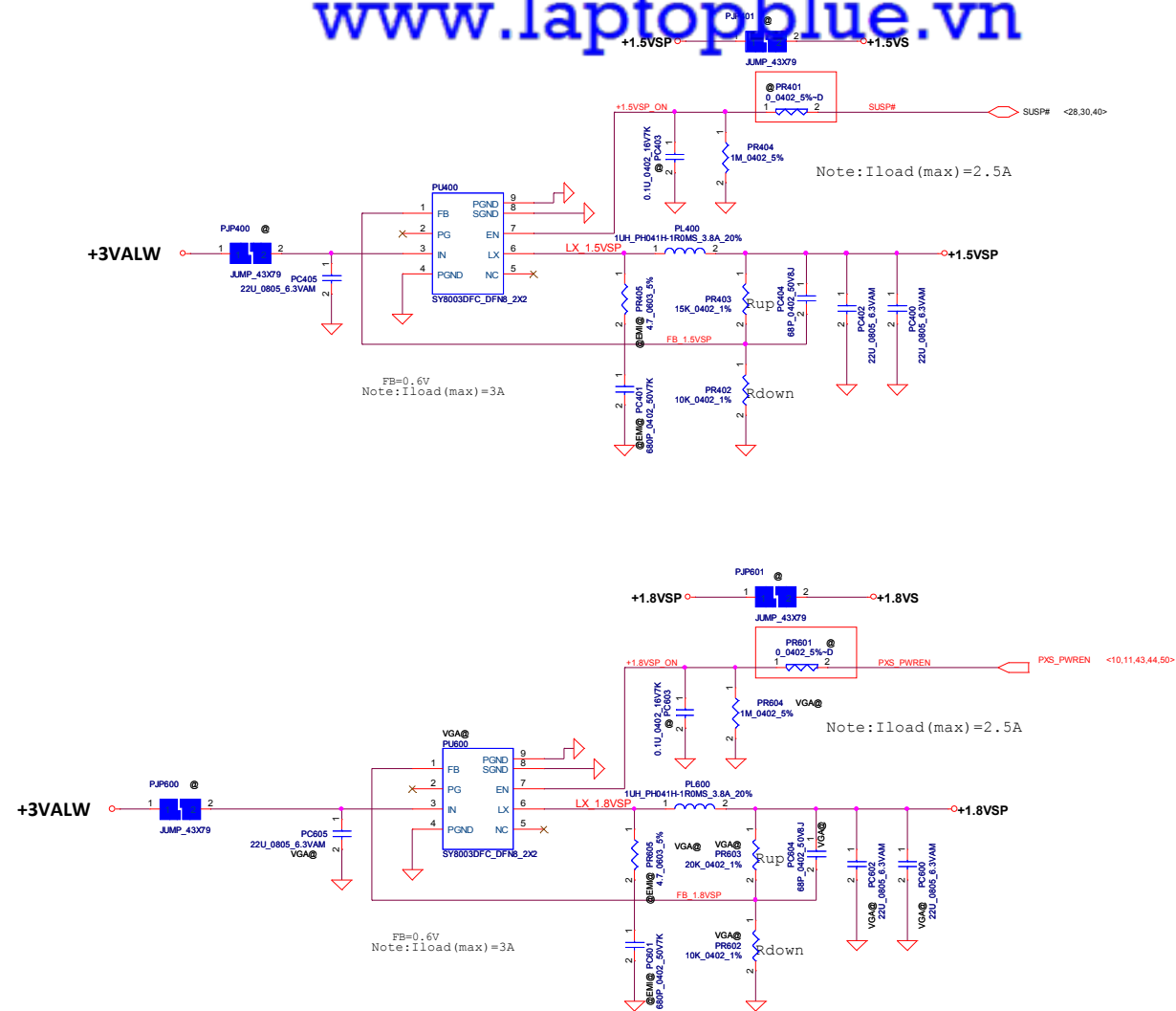




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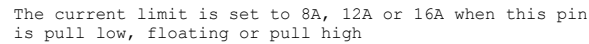
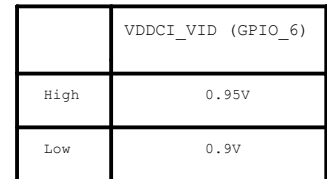


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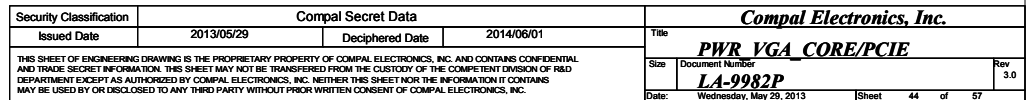
+3VS

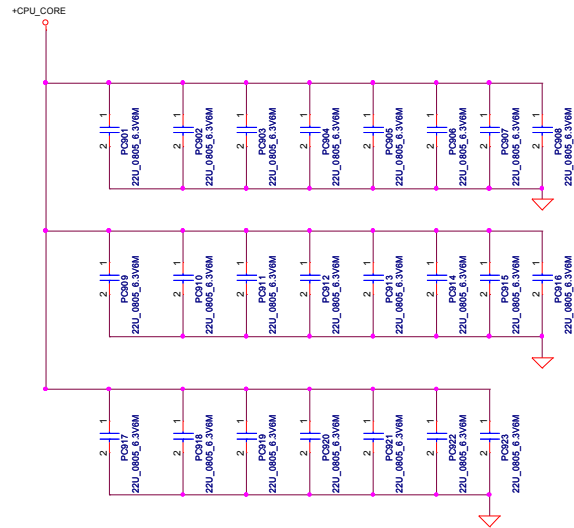
PR1110
100K_0402_5%



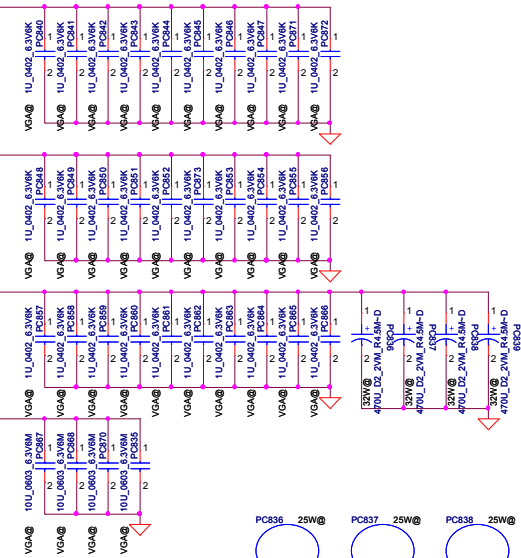
```
+VDDCIP
TDC 7A
Peak Current 13A
OCP current 16A
```

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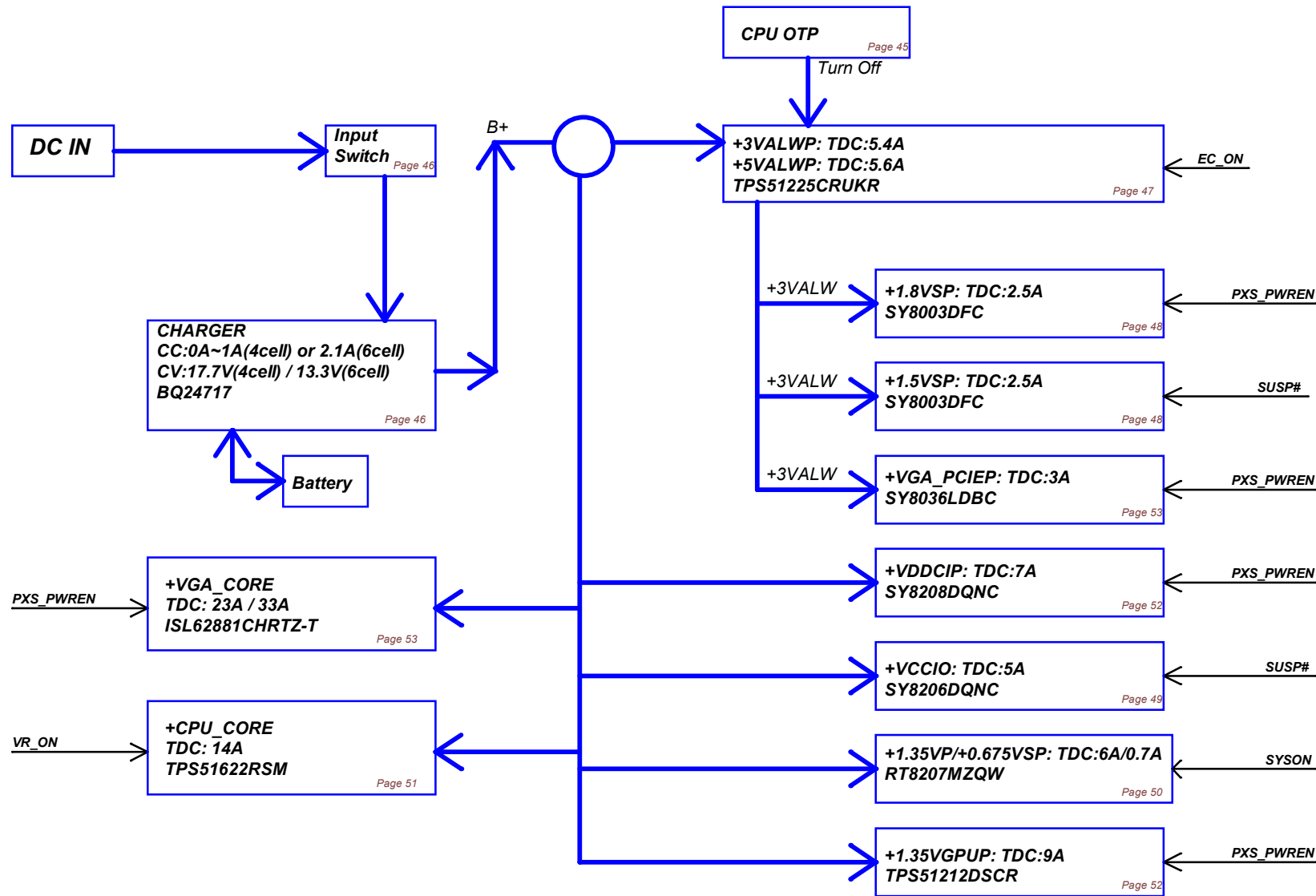




+VGA_CORE

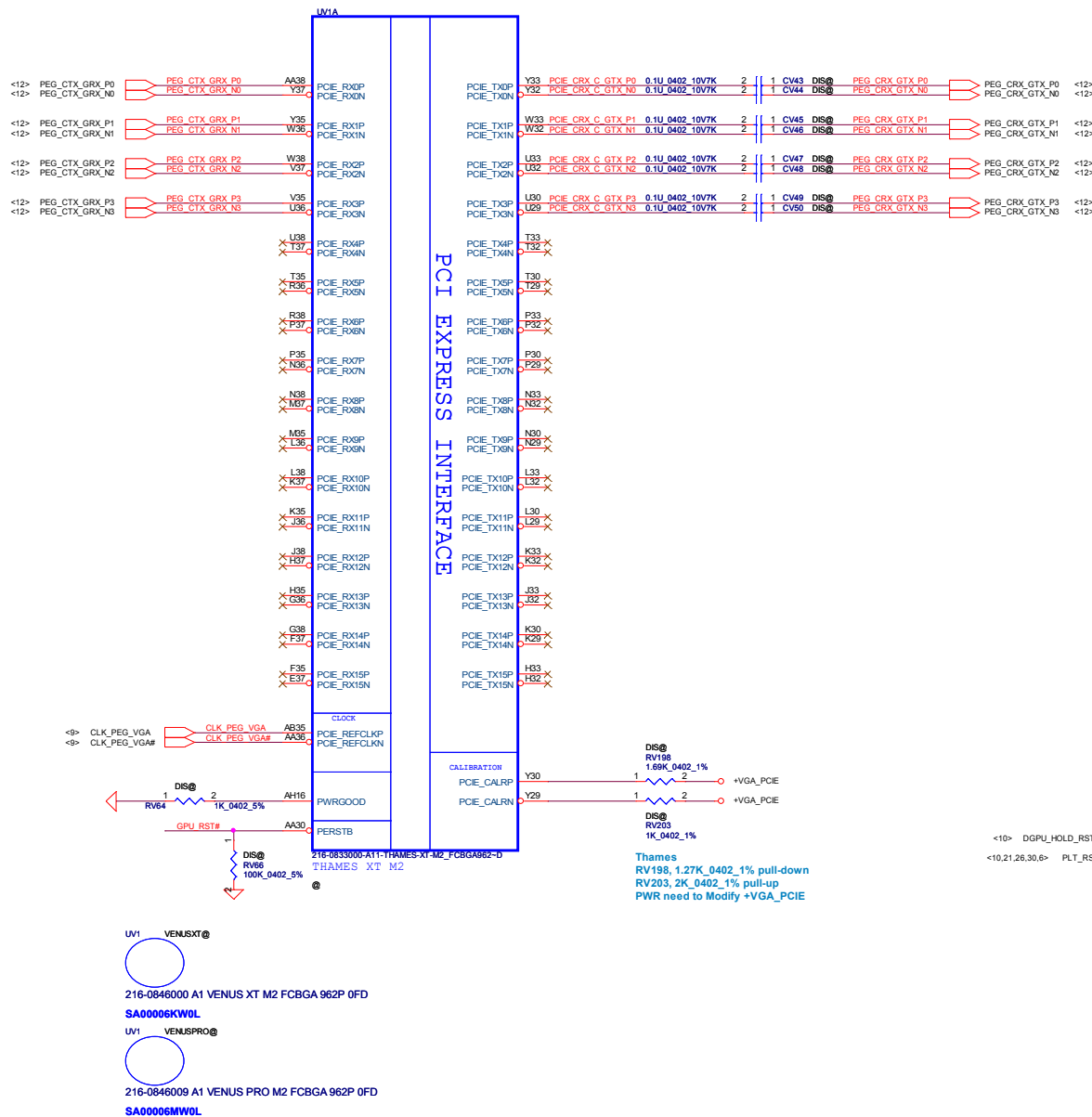


Power block

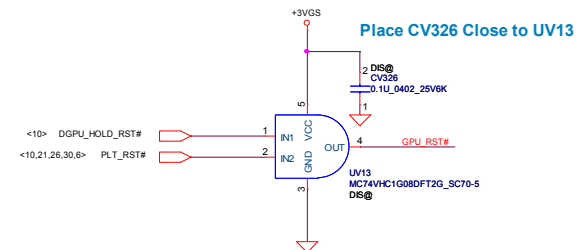
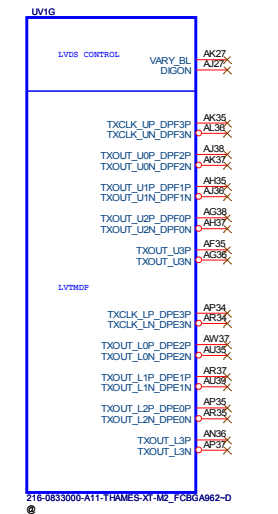


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GFX PCIE LANE REVERSAL



LVDS Interface

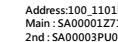


STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING 0: 50% swing 1: Full swing	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS Advertises PCIe speed when compliance test	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0: disable 1: enable	X
ROMCFGQ(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XXX
VP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VP DEVICE STRAPS	0
RSVD	H2SYNC		0
RSVD	GENERICC		0
AUD[0]	HSYNC	AUD[0] AUD[0] 0: No audio function 0: 1 Audio for DisplayPort and HDMI if dongle is detected	11
AUD[0]	VSYN	1: Audio for DisplayPort only 1: 1 Audio for both DisplayPort and HDMI	

GPI021	H2SYNC	GENERICC	GPI02	GPI0
--------	--------	----------	-------	------

VENUS MLPs
PS_3 used default

Closed to GP

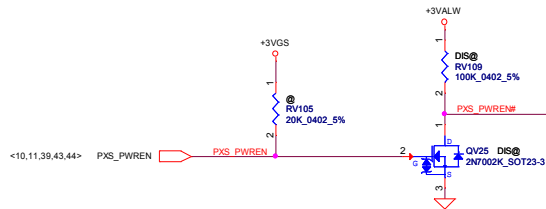


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PX_MODE=1 for Normal Operation
PX_MODE=0 for BACO mode to shut down power rails except VDDR3, PCIE_VDDC and 1.8V rail

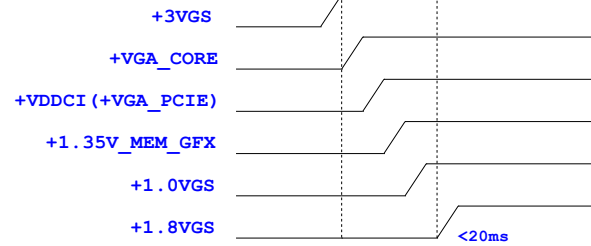
Note:

PX4.0 +VGA_CORE, VDDCI, +1.5VGS ON
PX4.0 +3VGS, +1.0VGS, +1.8VGS OFF
PX5.0 +3VGS, +VGA_CORE, VDDCI, +1.5VGV, +1.0VGS, +1.8VGS OFF

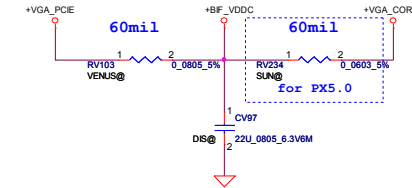


for PX4.0 and PX5.0

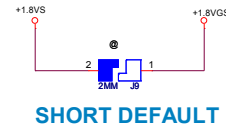
Power sequence of Sun XT, Venus Pro, Venus XT



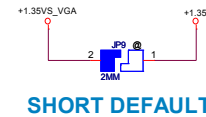
Switch circuits in BACO desings for Thames/Seymour only
55mA@1.0V, in BACO mode



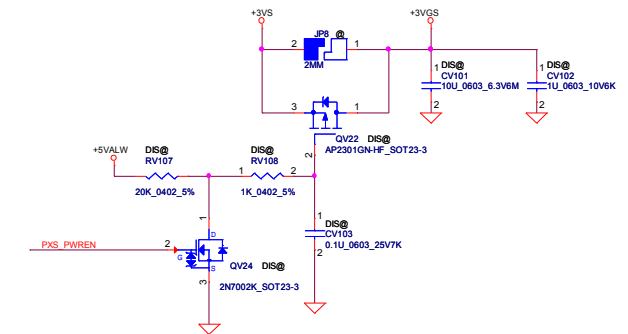
+1.8VS TO +1.8VGS

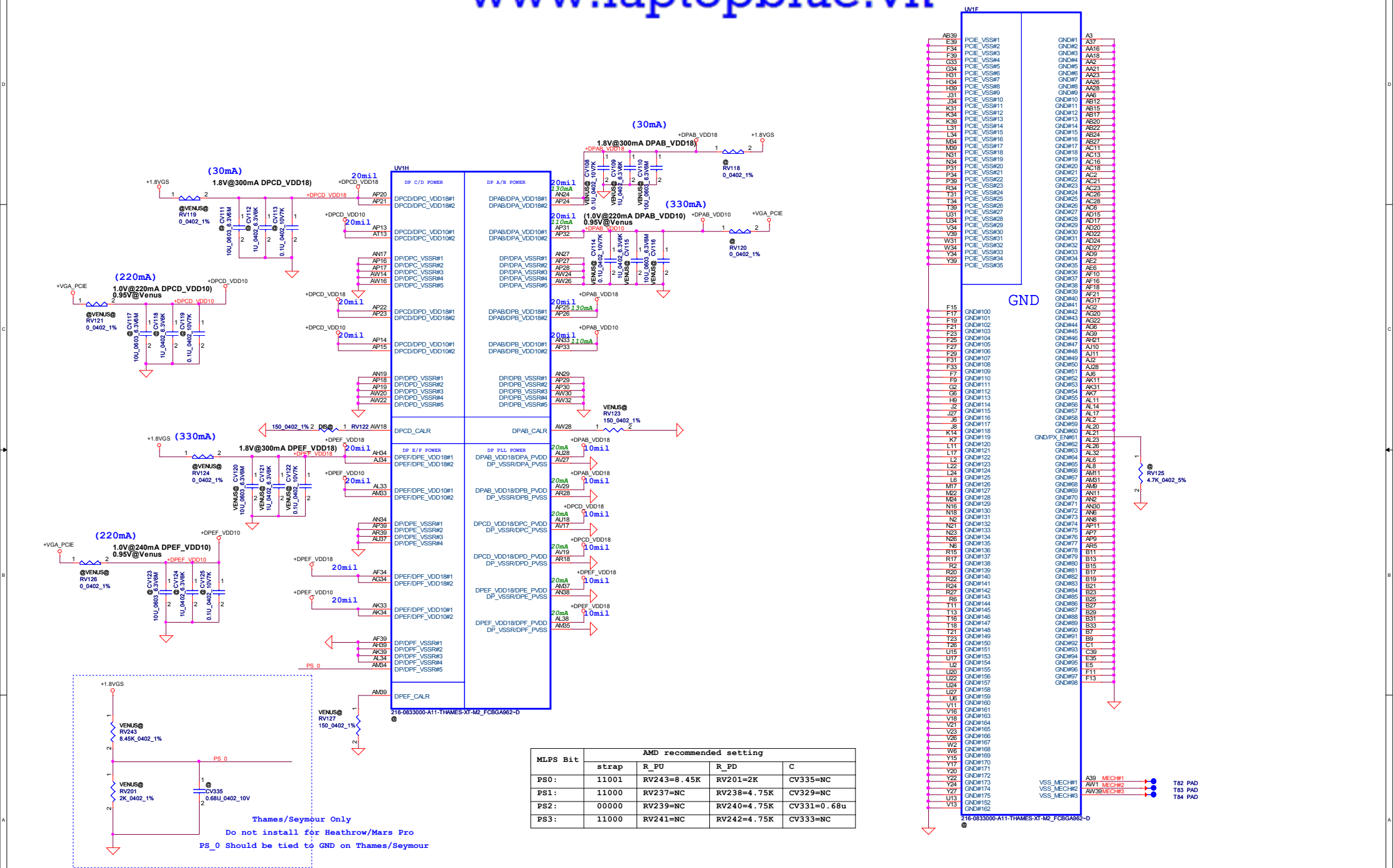


+1.35VS_VGA TO +1.35V_MEM_GFX



+3VS TO +3VGS



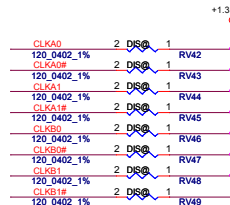




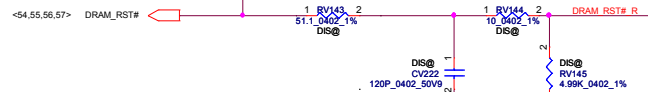
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GDDR5 CMD Mapping Table

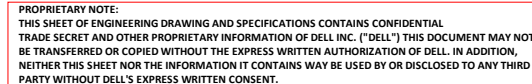
<0..31>	<32..63>	Memory
CMD12	CMD28	RAS#
CMD15	CMD31	CAS#
CMD5	CMD21	WE#
CMD0	CMD16	CS#
CMD8	CMD24	ABIT#
CMD10	CMD26	A0 A10
CMD11	CMD27	A1 A9
CMD2	CMD18	D2 BA0
CMD1	CMD17	A3 BA3
CMD4	CMD20	A5 BA1
CMD7	CMD23	A6 A11
CMD9	CMD25	A1Z FRU
CMD14	CMD30	CKEY
CMD13	CMD29	RESET#




This basic topology should be used for DRAM_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and | Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec. Place all these components very close to GPU (Within 25mm) and keep all component close to each other (within 5mm) except Rser2



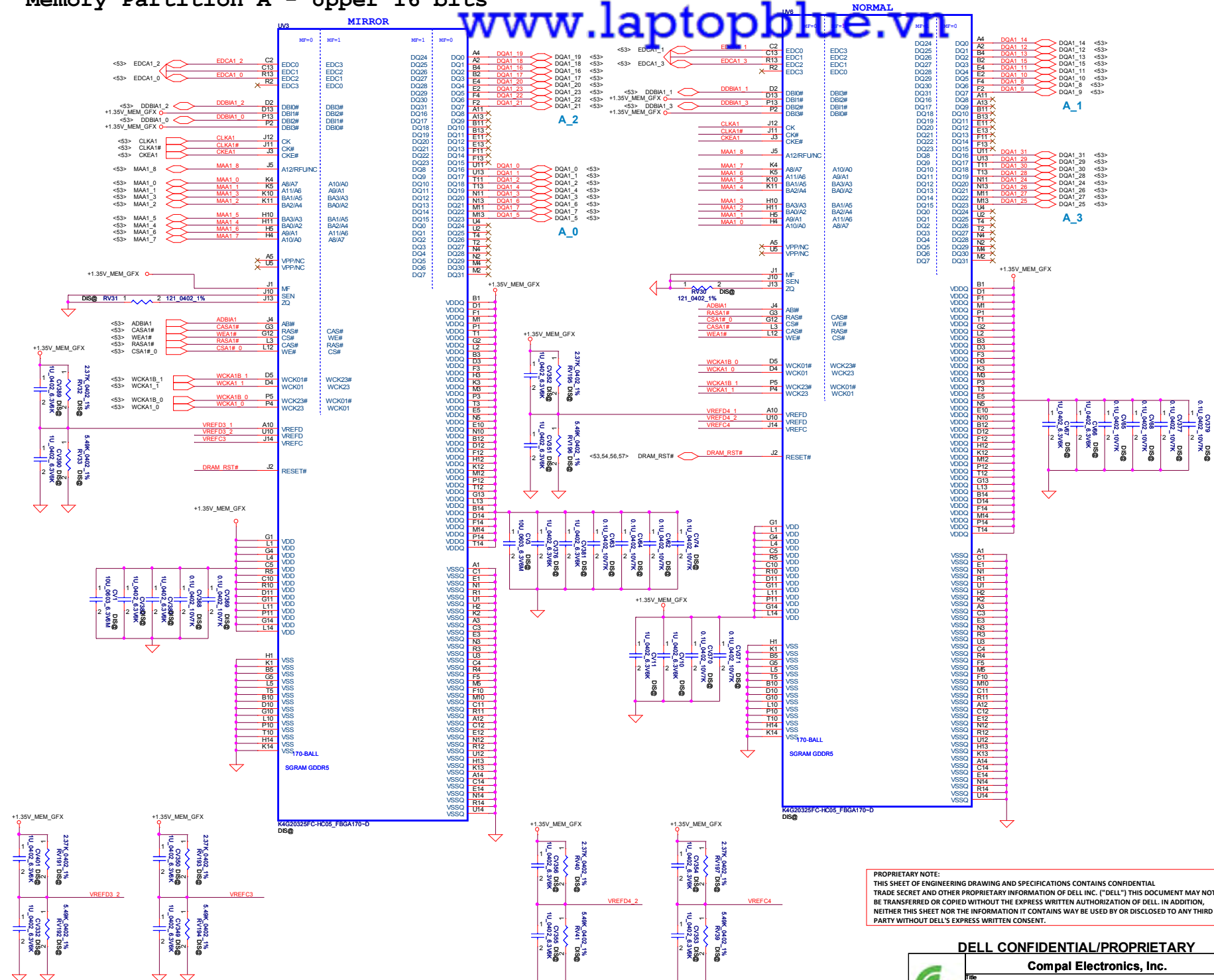
64X32 GDDR5



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		Title	
		VRAM A Lower UV4,UV5	
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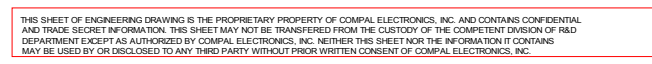
Memory Partition A - Upper 16 bits

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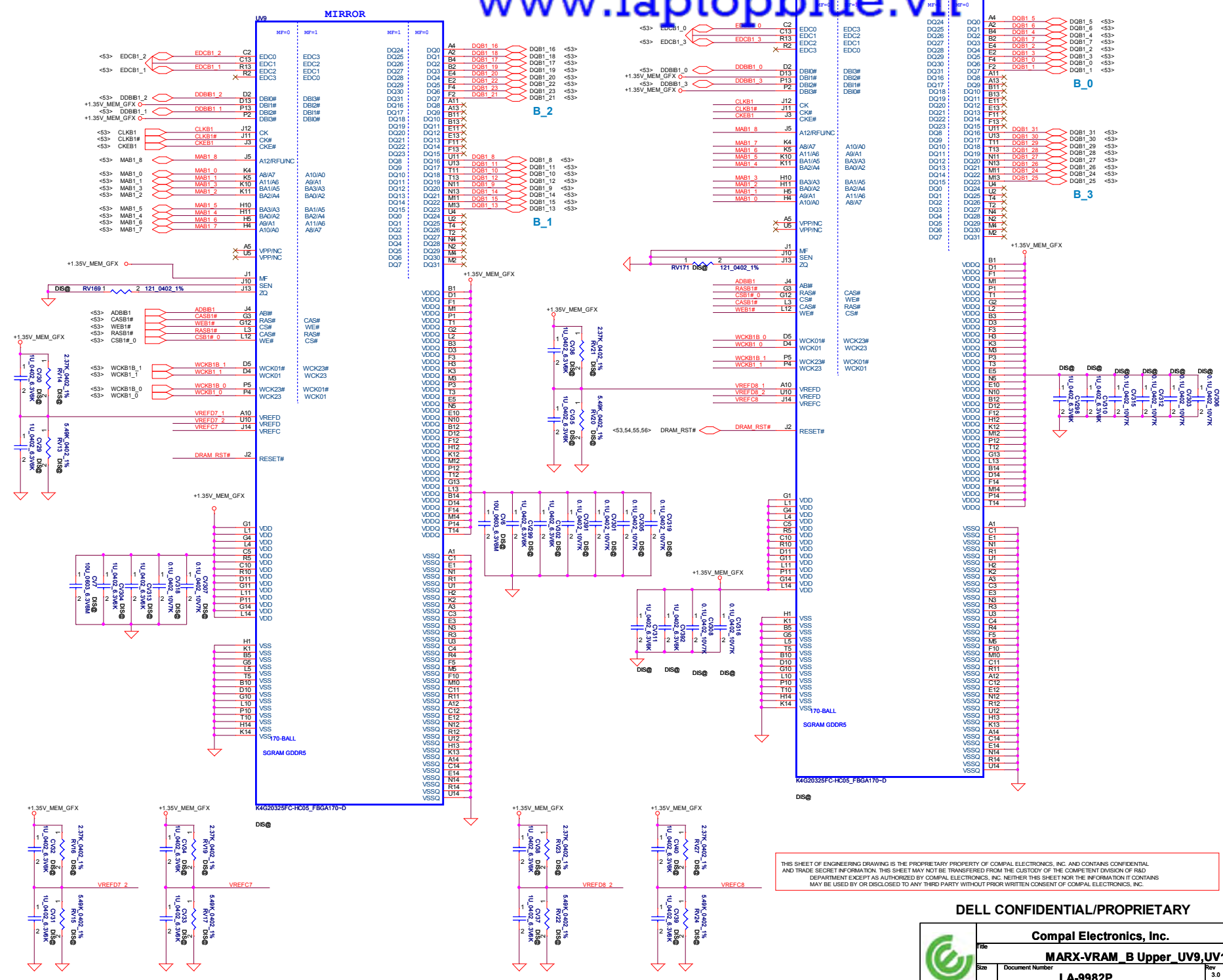
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Memory Partition B - Upper 16 bits

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