

# Berry DG15 Discrete/UMA Schematics Document

Arrandale

Intel PCH

2010-02-03

REV : A00

*DY :None Installed  
UMA:UMA platform installed  
PARK:DIS PARK platform installed  
M96:DIS M96 platform installed  
VRAM\_1G:VRAM 128M\*16 installed  
Colay :Manual modify BOM*

<Core Design>



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Title

**Cover Page**

Size  
A3

Document Number

**Berry**

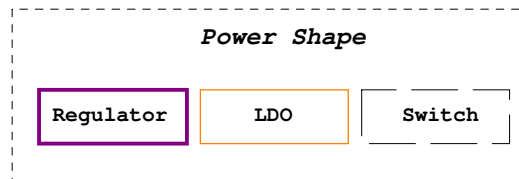
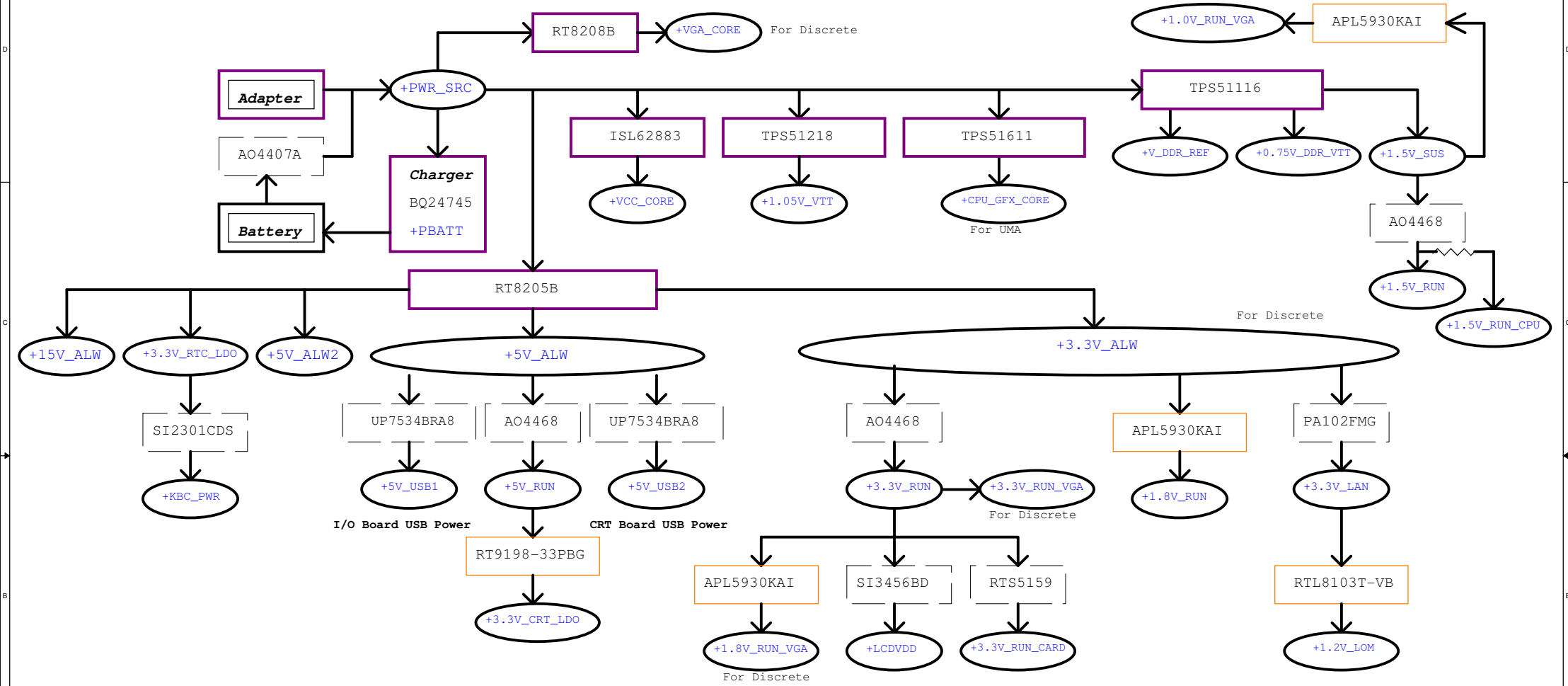
Rev

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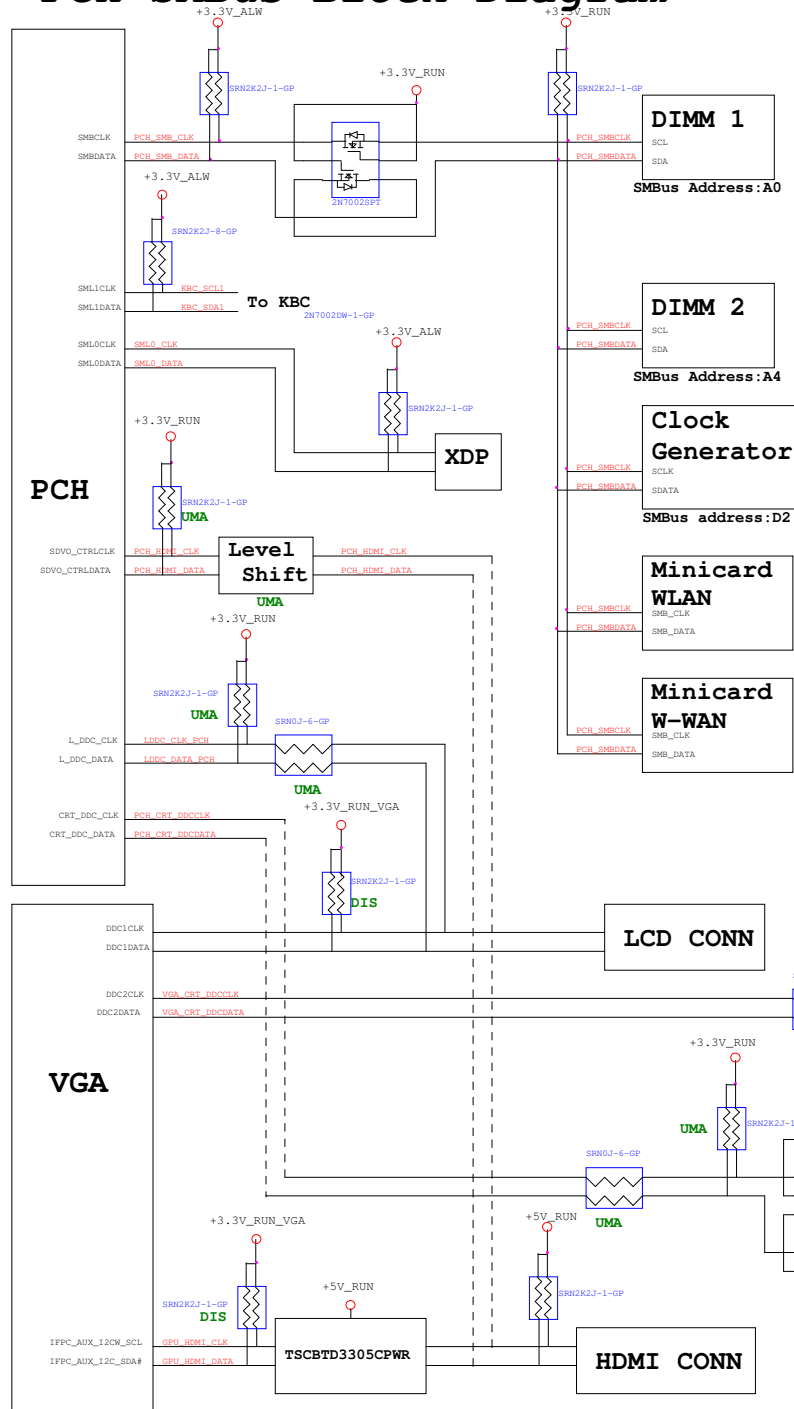
Date: Wednesday, February 10, 2010

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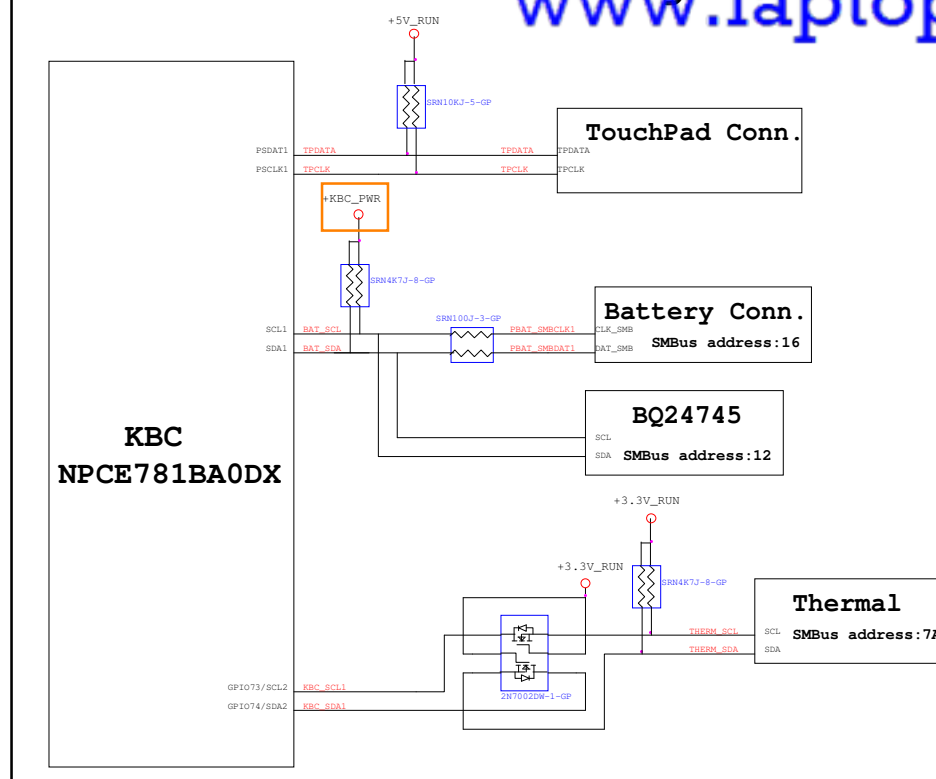




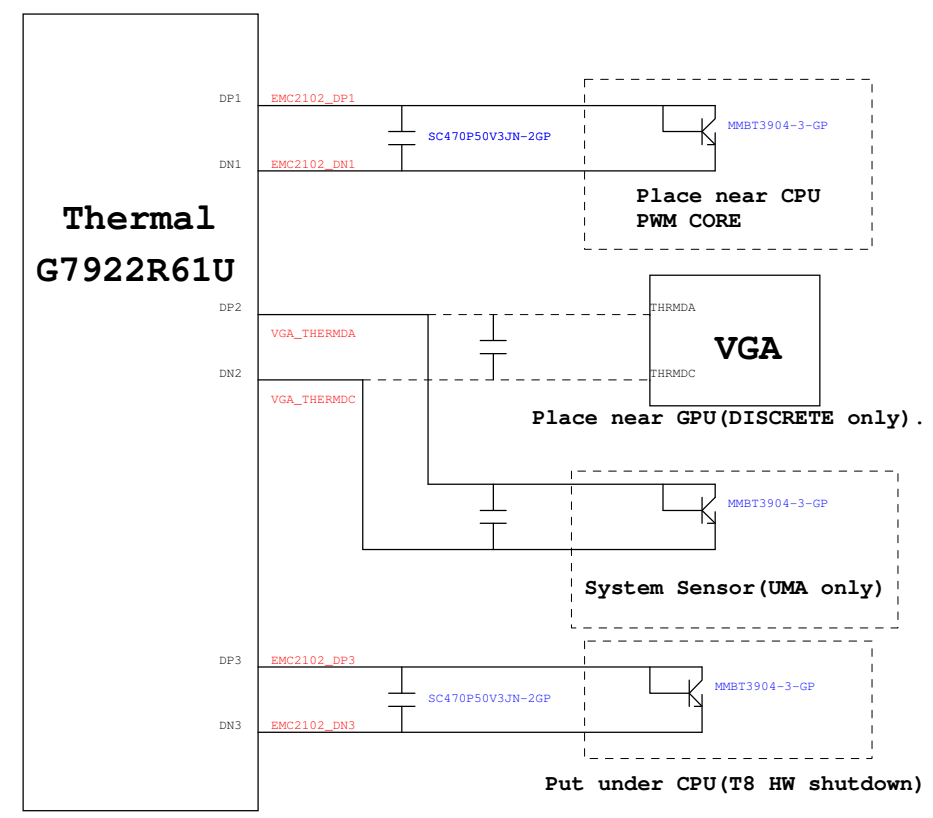
### PCH SMBus Block Diagram



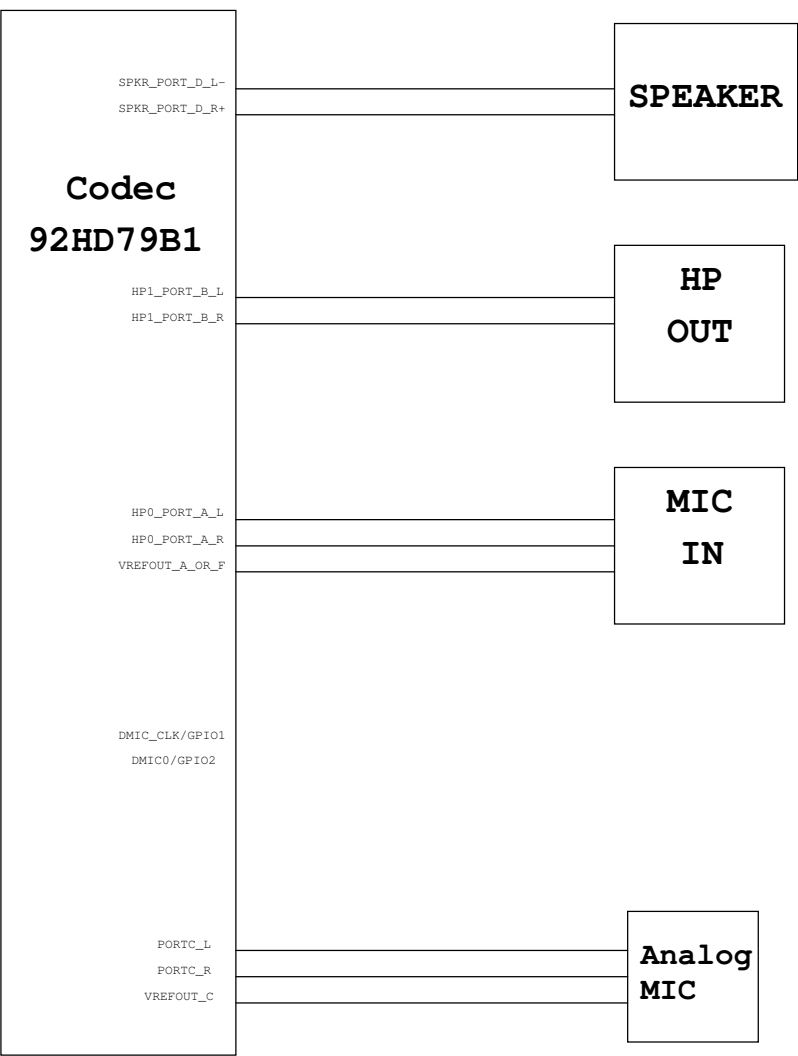
## KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



## PCH Strapping

Calpella Schematic Checklist Rev.0\_7

Name	Schematics Notes
SPKR	<b>Reboot option at power-up</b> Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/GPIO55	<b>Default Mode:</b> Internal pull-up. <b>Low (0) = Top Block Swap Mode</b> (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	<b>High (1) = Integrated VRM is enabled</b> <b>Low (0) = Integrated VRM is disabled</b>
GNT0#, GNT1#/GPIO51	<b>Default (SPI):</b> Left both GNT0# and GNT1# floating. No pull up required. <b>Boot from PCI:</b> Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. <b>Boot from LPC:</b> Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/GPIO53	<b>Default - Internal pull-up.</b> <b>Low (0)</b> = Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	<b>Default:</b> Do not pull low. <b>Disable ME in Manufacturing Mode:</b> Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	<b>Enable iTPM:</b> Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. <b>Disable iTPM:</b> Left floating, no pull-down required.
NV_ALE	<b>Enable Danbury:</b> Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. <b>Disable Danbury:</b> Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN#/GPIO[33]	<b>Low (0):</b> Flash Descriptor Security will be overridden. <b>High (1):</b> Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	<b>Default = Do not connect (floating)</b> <b>High(1)</b> = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. <b>Low (0)</b> = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

## PCIE Routing

LANE1	RESERVED
LANE2	MiniCard WLAN
LANE3	LAN
LANE4	W-WAN
LANE5	RESERVED
LANE6	RESERVED
LANE7	H55/HM55 no support
LANE8	H55/HM55 no support

## USB Table

USB	
Pair	Device
0	USB2 (CRT Board)
1	USB3 (CRT Board)
2	WLAN (I/O Board)
3	RESERVED
4	CARD READER
5	BLUETOOTH
6	HM55 no support
7	HM55 no support
8	USB1 (I/O Board)
9	USB0 (I/O Board ESATA)
10	RESERVED
11	W-WAN (I/O Board)
12	RESERVED
13	CAMERA

## SATA Table

SATA	
Pair	Device
0	HDD
1	ODD
2	HM55 no support
3	HM55 no support
4	ESATA
5	RESERVED

## Processor Strapping

Calpella Schematic Checklist Rev.0\_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	<b>Embedded DisplayPort Presence</b>	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	<b>PCI-Express Static Lane Reversal</b>	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	<b>PCI-Express Configuration Select</b>	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	<b>Reserved - Temporarily used for early Clarksfield samples.</b>	<b>Clarksfield (only for early samples pre-ES1)</b> - Connect to GND with 3.01K Ohm/5% resistor <b>Note:</b> Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

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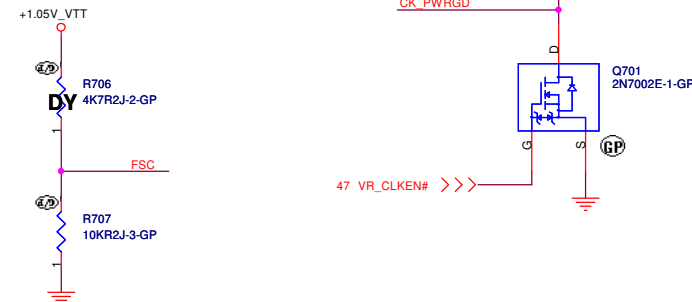
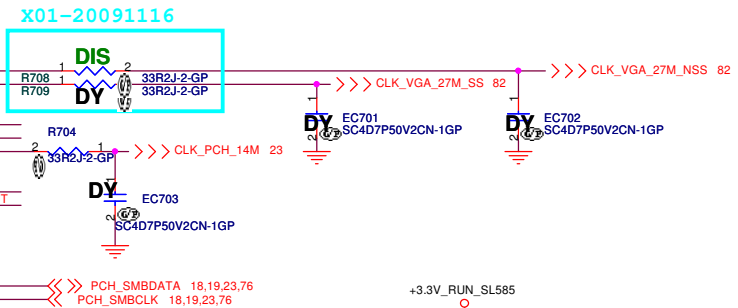
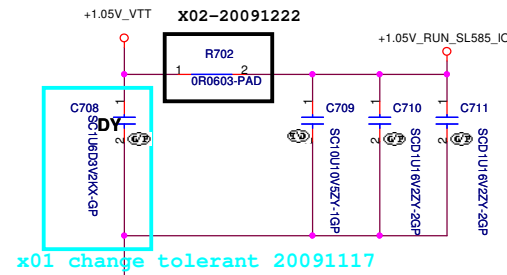


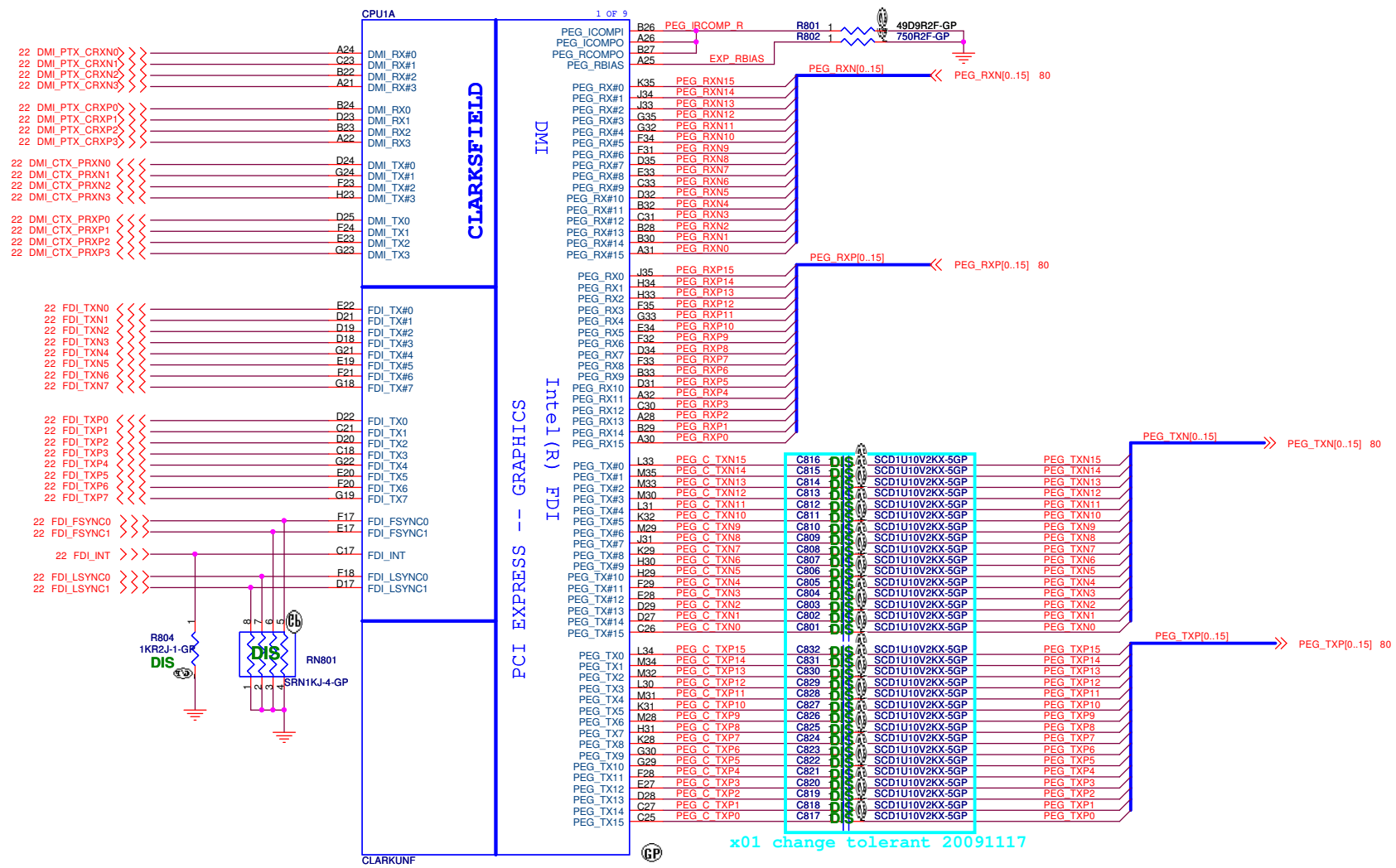
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SEC. 62.10053.561

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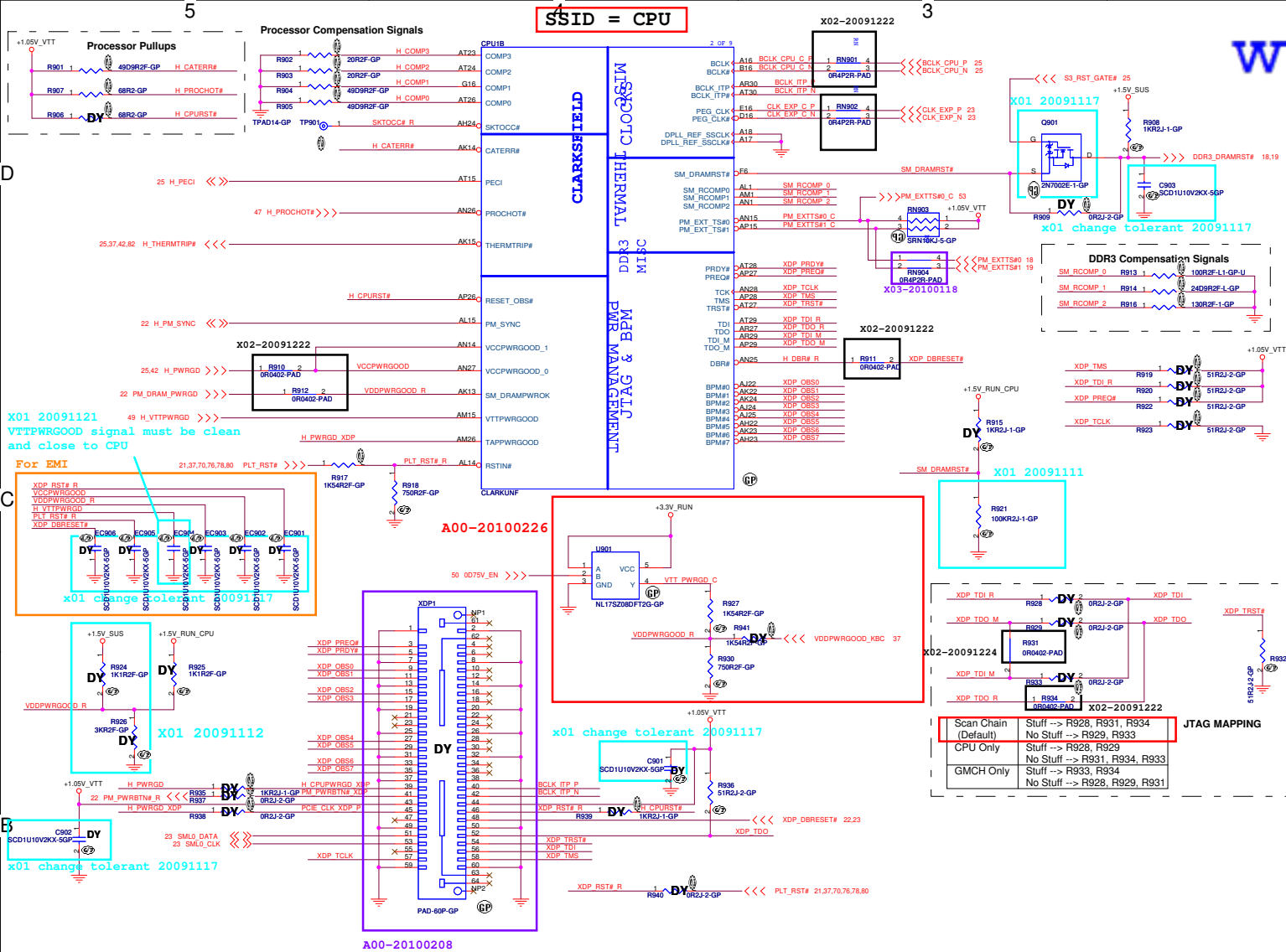
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Title: **CPU (PCIE/DMI/FDI)**

Size: Document Number **Berry** Rev **A00**

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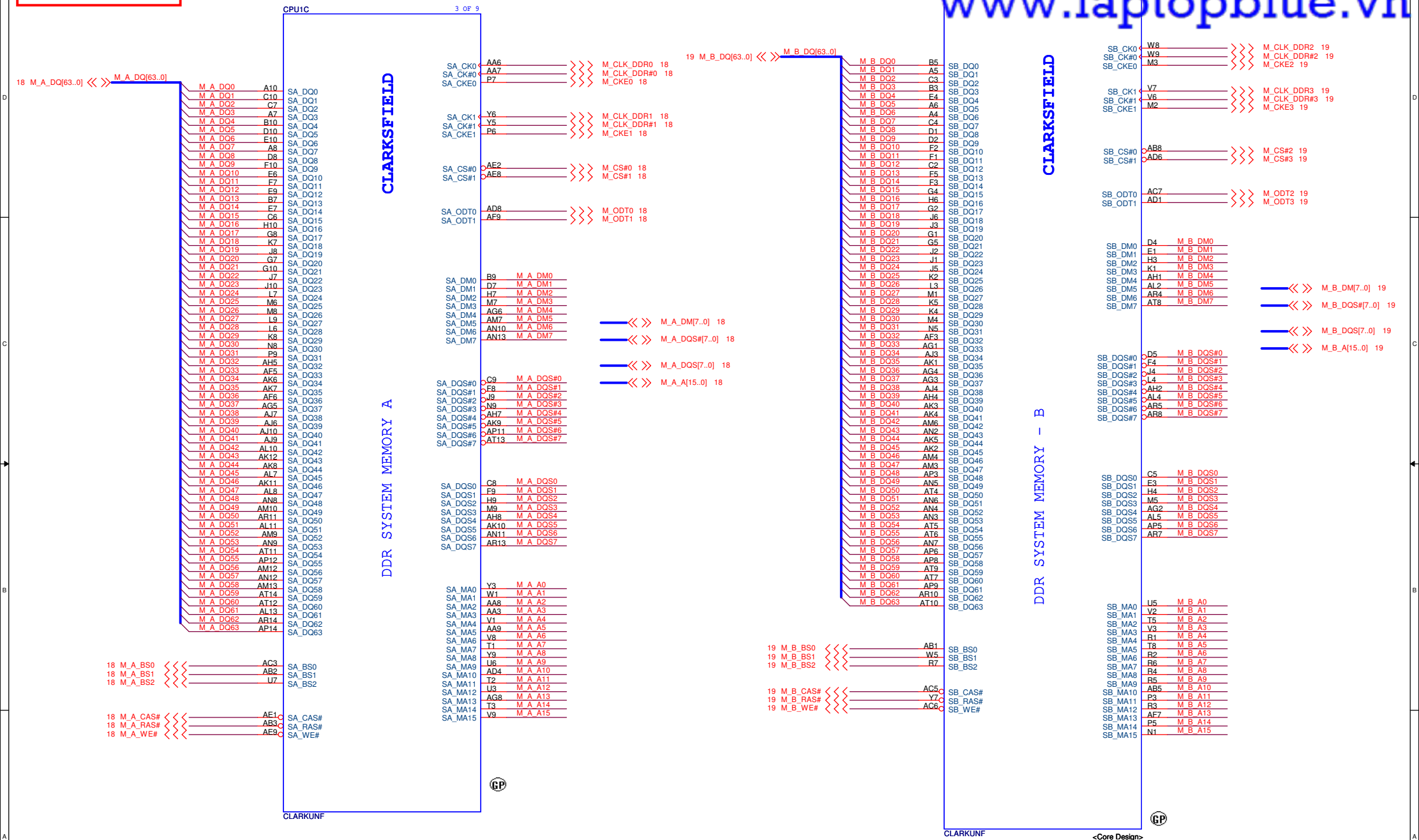




JTAG MAPPING	
Scan Chain (Default)	Stuff --> R928, R931, R934 No Stuff --> R929, R933
CPU Only	Stuff --> R928, R929 No Stuff --> R931, R934, R933
GMCC Only	Stuff --> R933, R934 No Stuff --> R928, R929, R931

SSID = CPU

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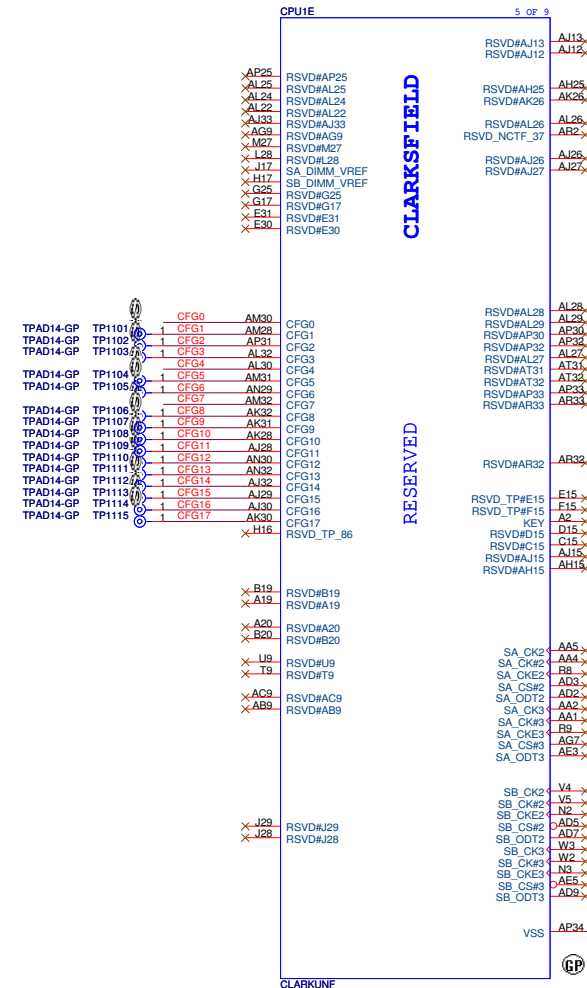
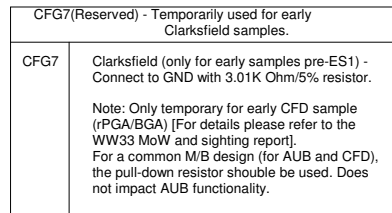
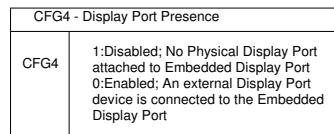
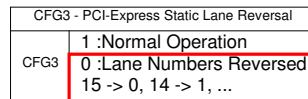
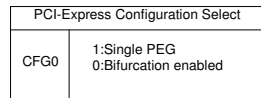
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (DDR)**

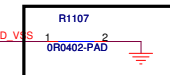
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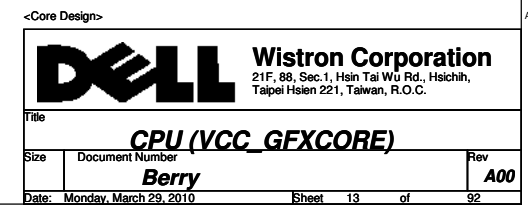


VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.

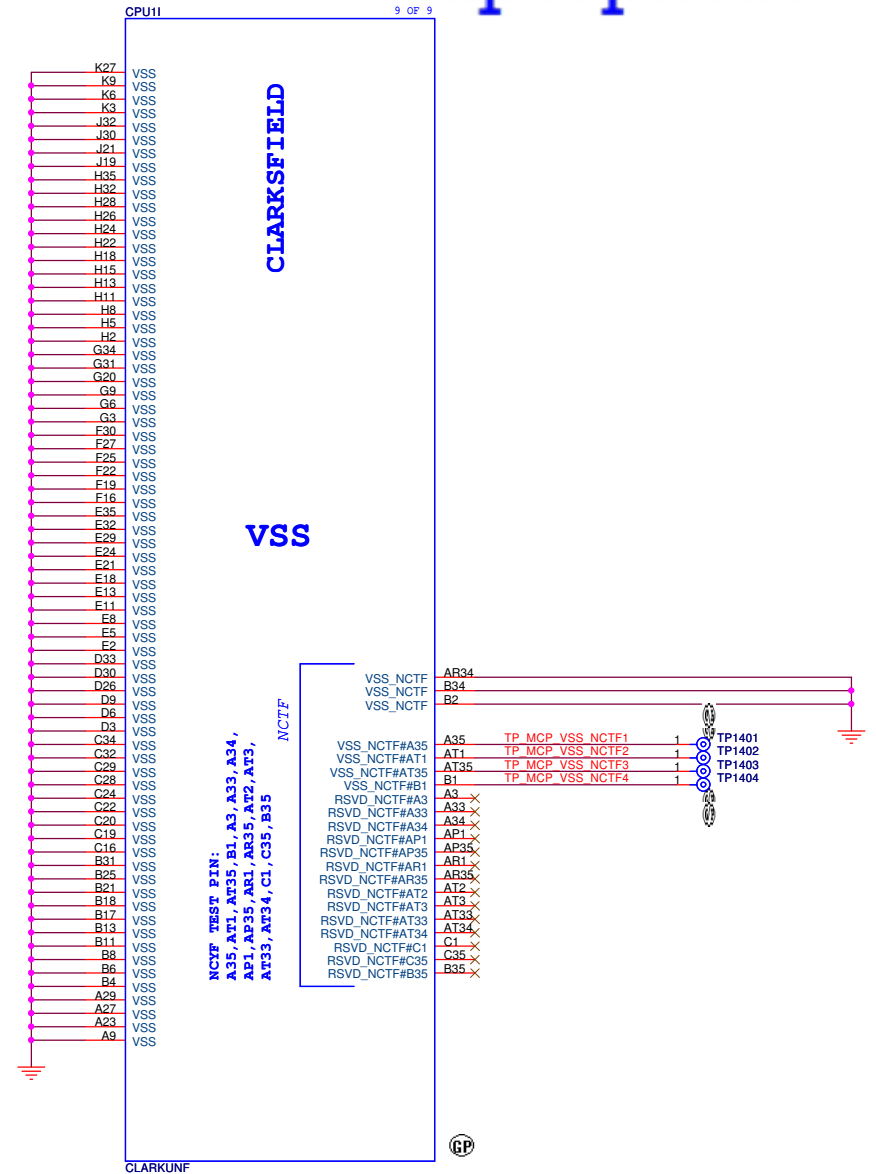
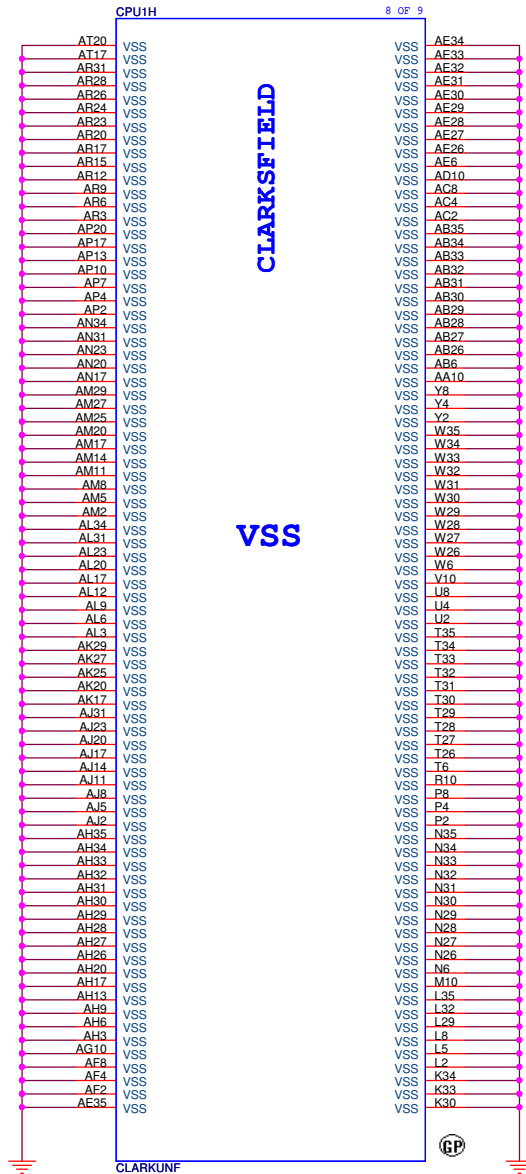


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Title			<b>CPU (VSS)</b>	
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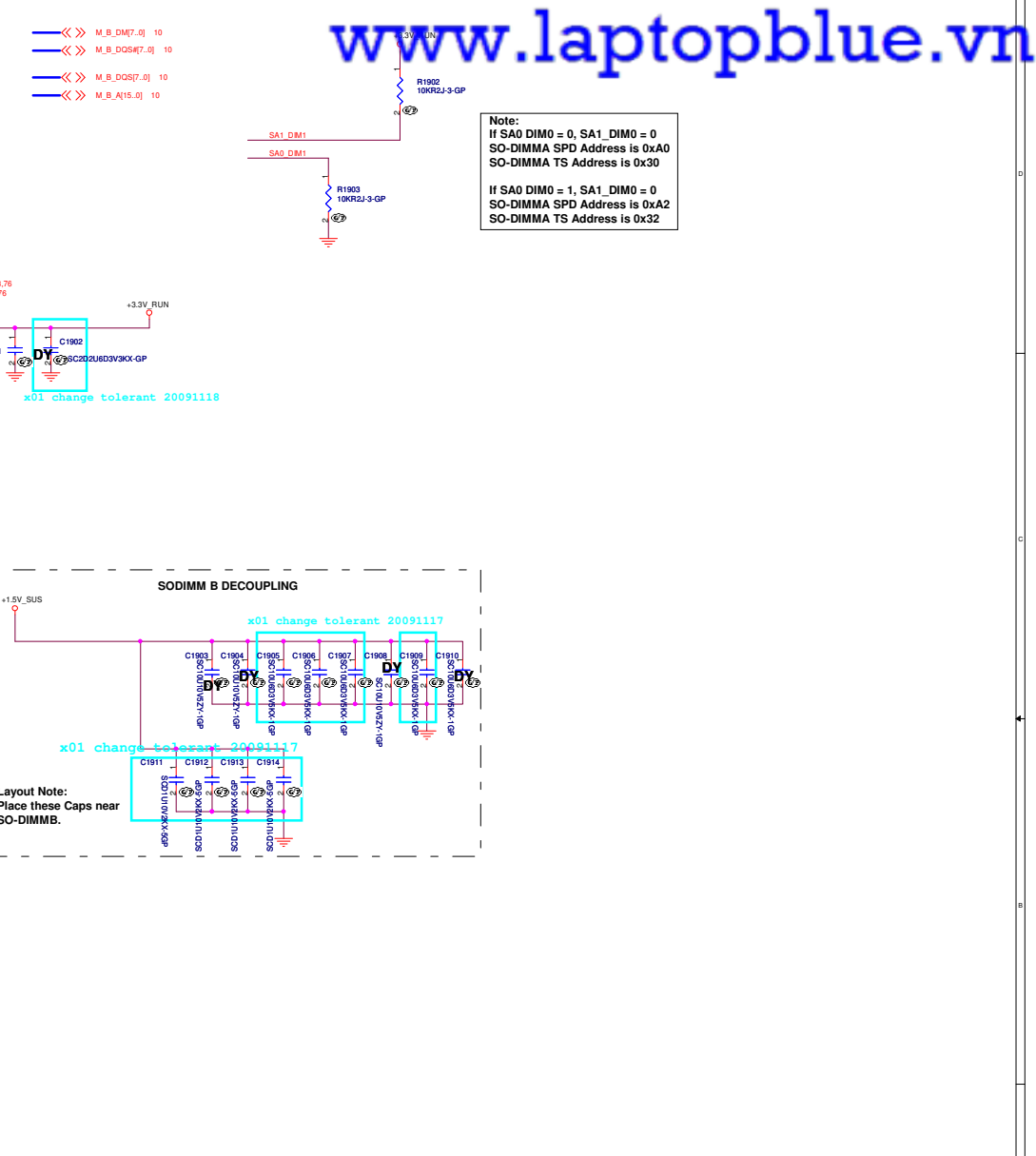
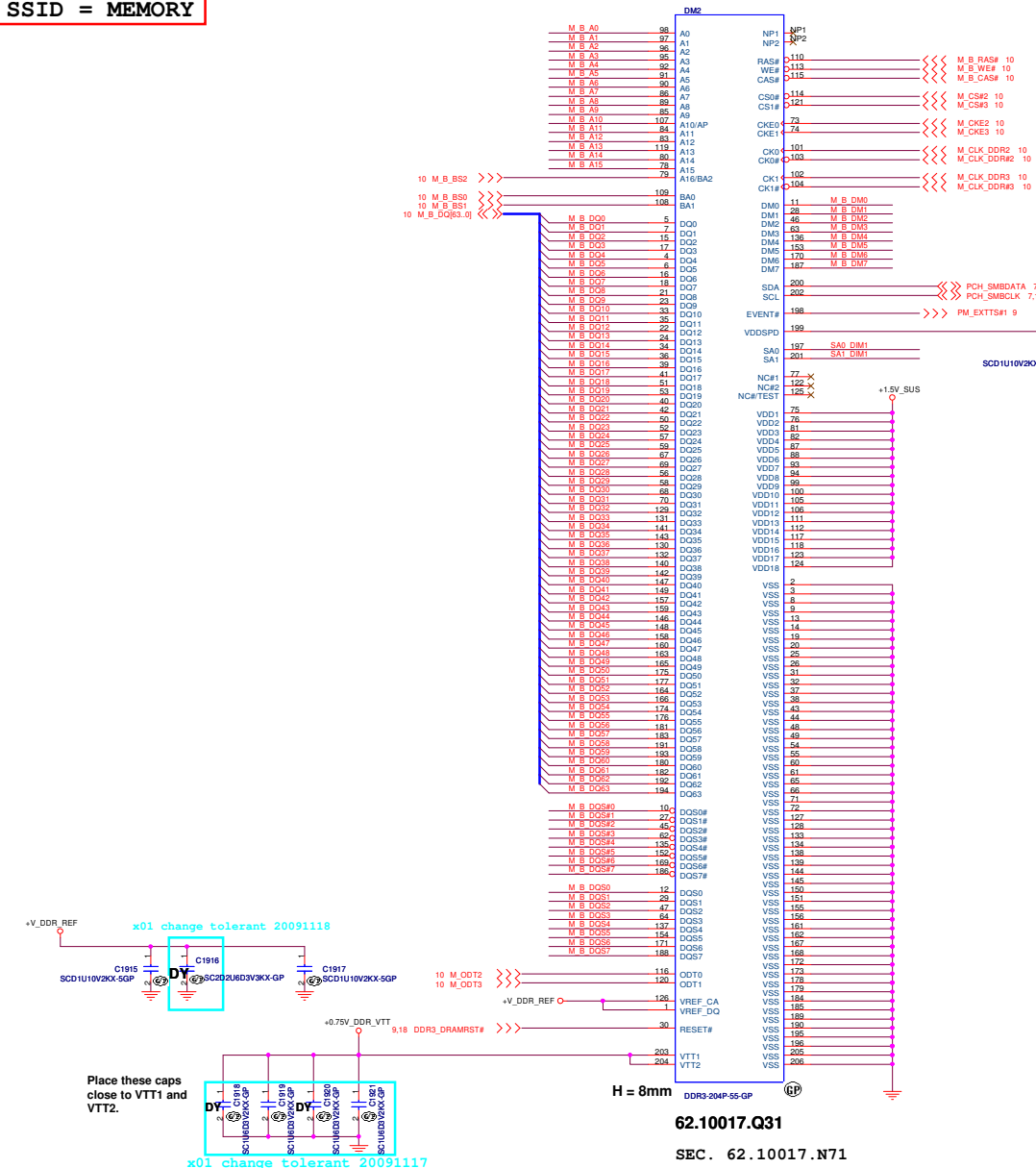
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SSID = MEMORY

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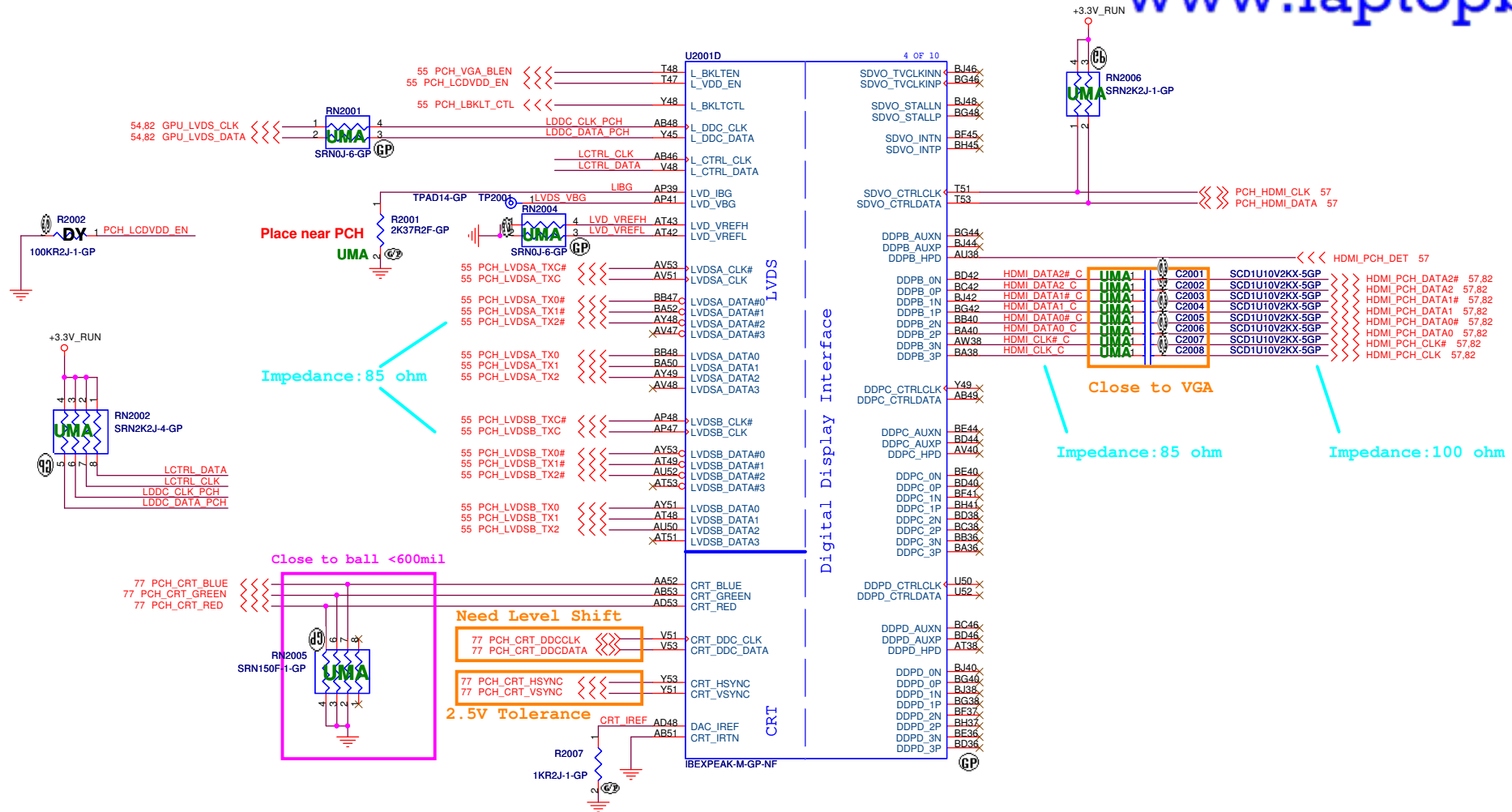


Note:  
If SA0\_DIM0 = 0, SA1\_DIM0 = 0  
SO-DIMMA SPD Address is 0xA0  
SO-DIMMA TS Address is 0x30  
  
If SA0\_DIM0 = 1, SA1\_DIM0 = 0  
SO-DIMMA SPD Address is 0xA2  
SO-DIMMA TS Address is 0x32

Note:  
SO-DIMMB SPD Address is 0xA4  
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from  
the Processor than SO-DIMMA

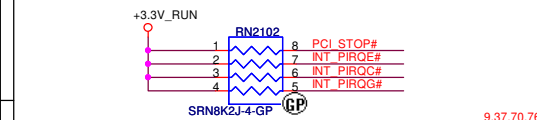
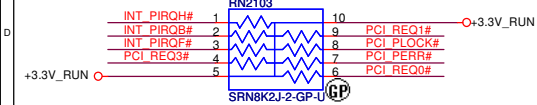
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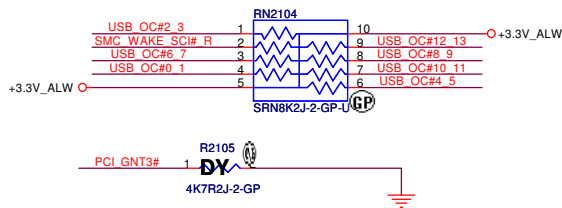
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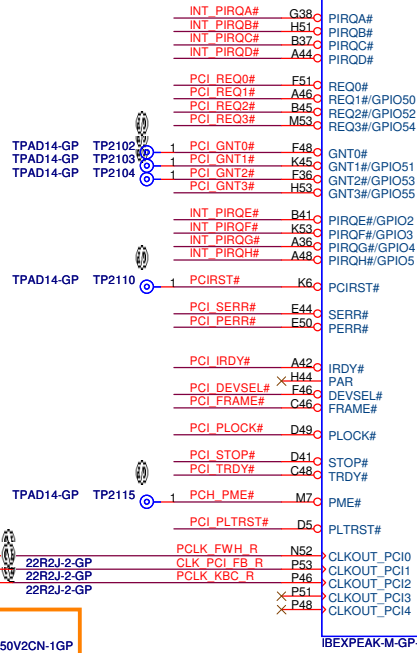
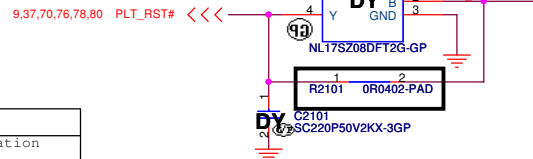
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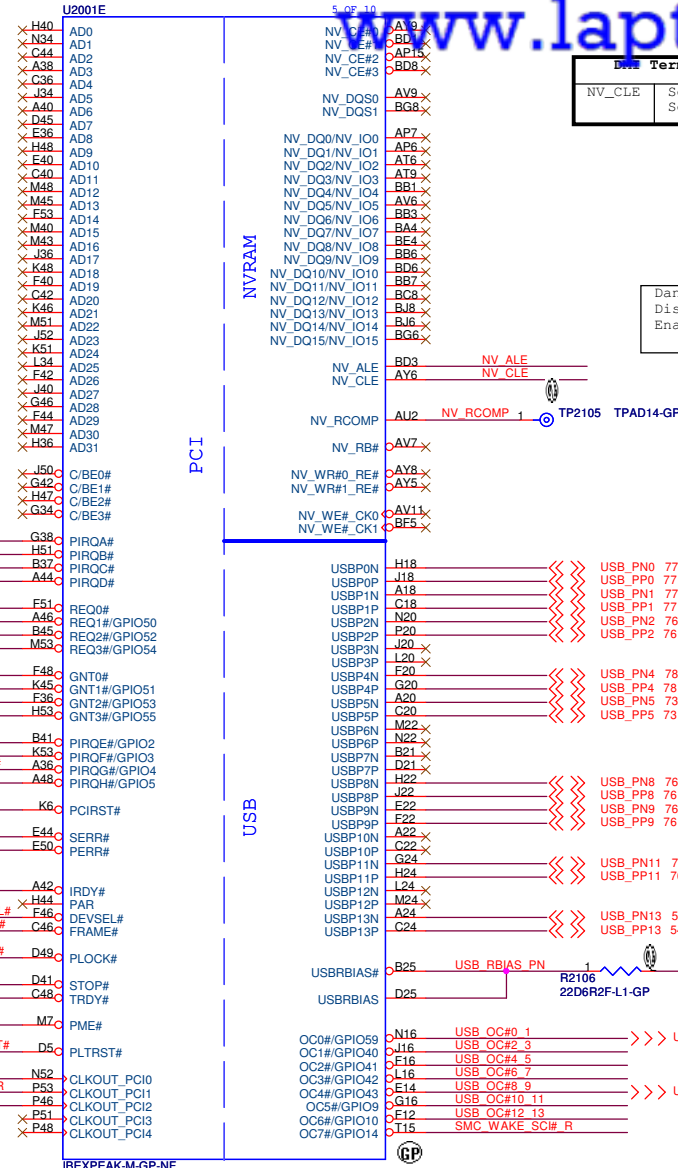
PCI_GNT#1	PCI_GNT#0	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI(Default)



PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default
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KBC CLK EMI



Data Termination Voltage	
NV_CLE	Set to Vss when low. Set to Vcc when high.

Danbury Technology:  
Disabled when Low.  
Enable when High.

USB	
Pair	Device
0	USB2 (CRT Board)
1	USB3 (CRT Board)
2	WLAN (I/O Board)
3	X
4	CARD READER
5	BLUETOOTH
6	X
7	X
8	USB1 (I/O Board)
9	ESATA (I/O Board COMBO)
10	X
11	W-WAN (I/O Board)
12	X
13	CAMERA

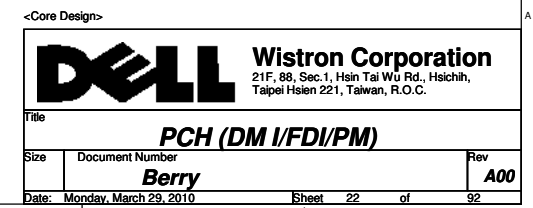
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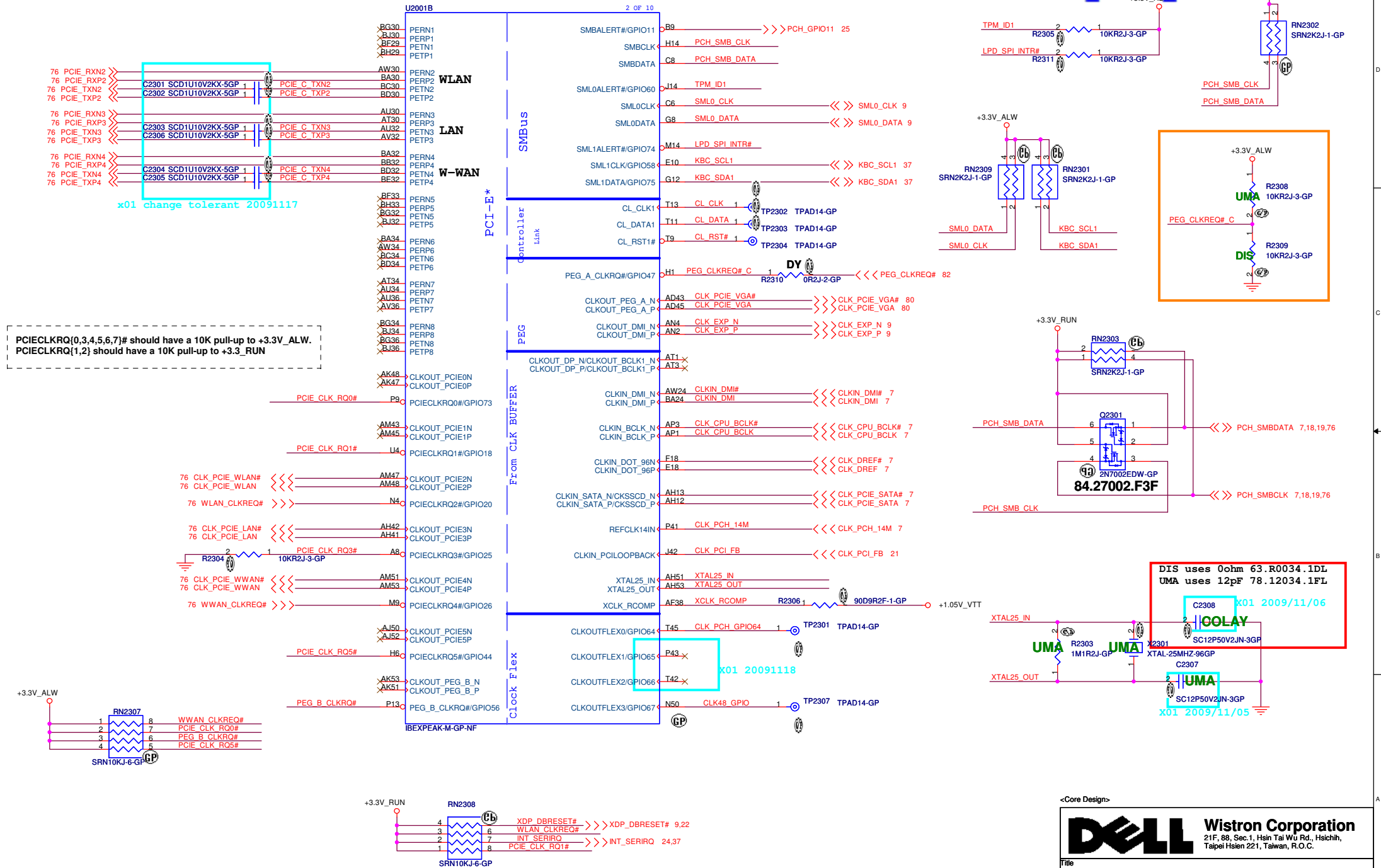
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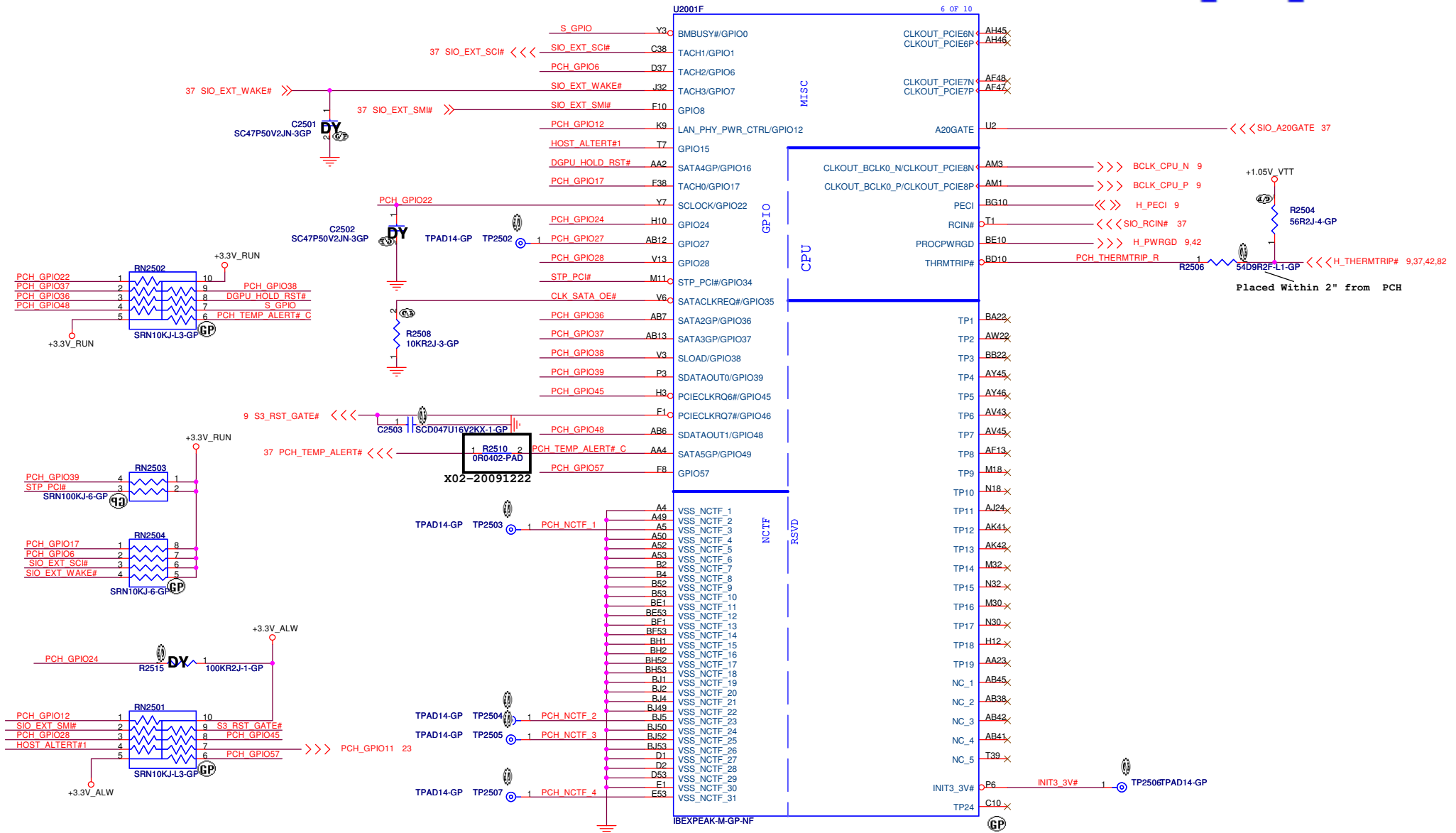


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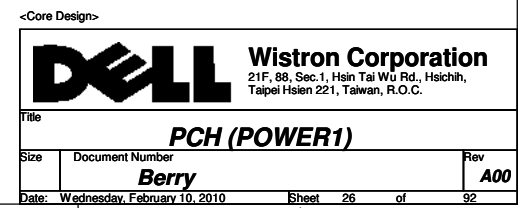
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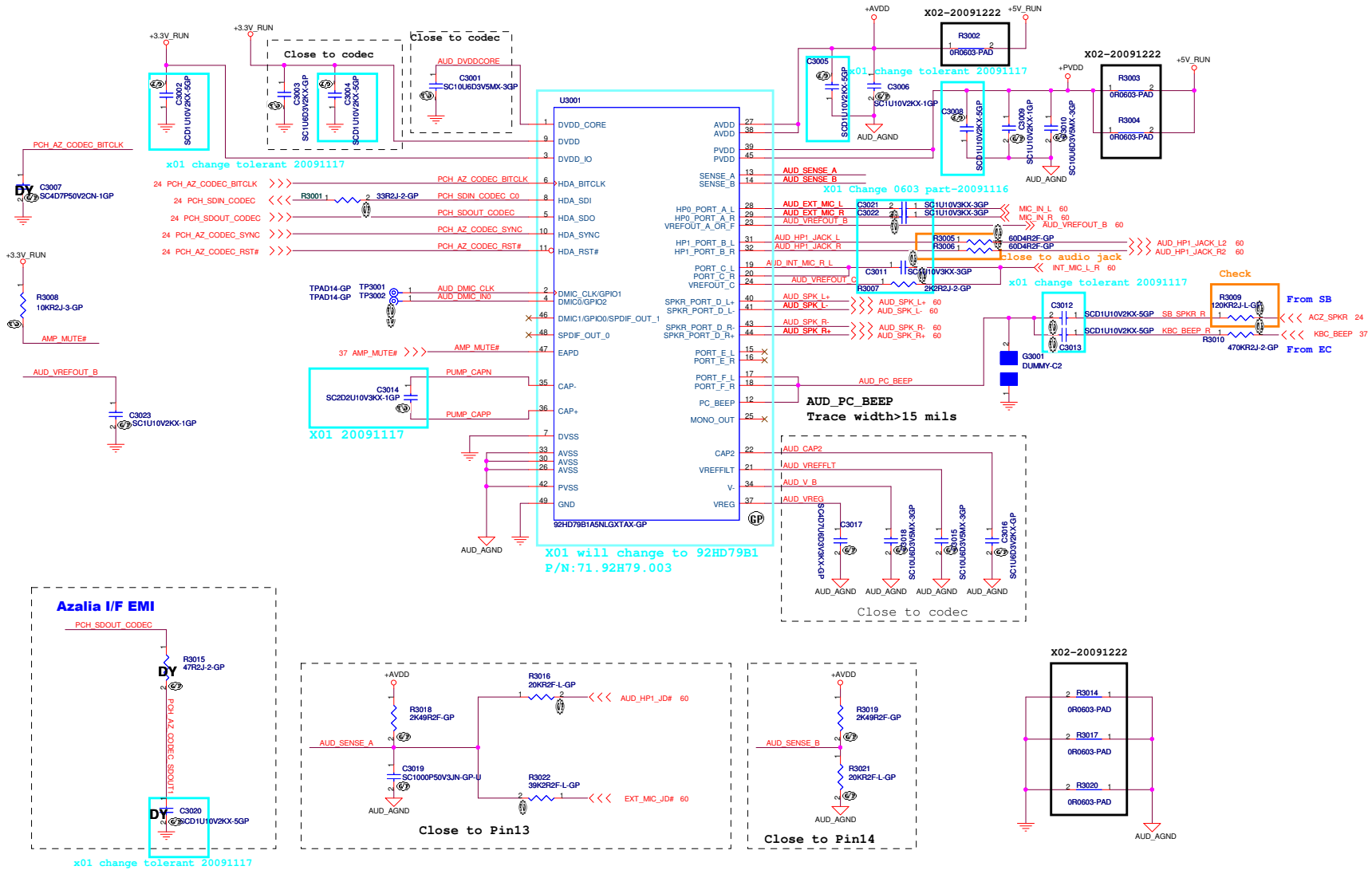
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SSID = AUDIO

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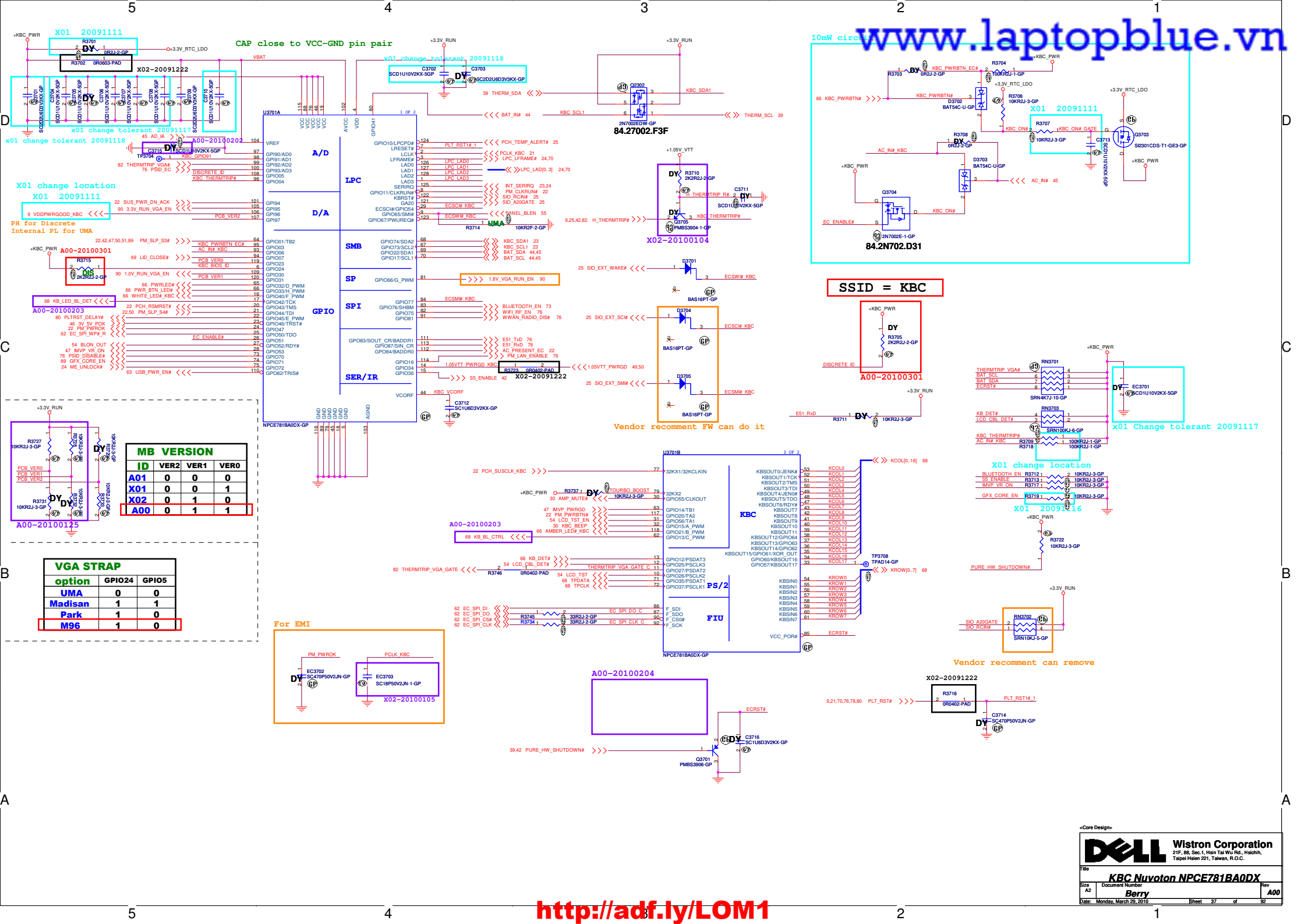
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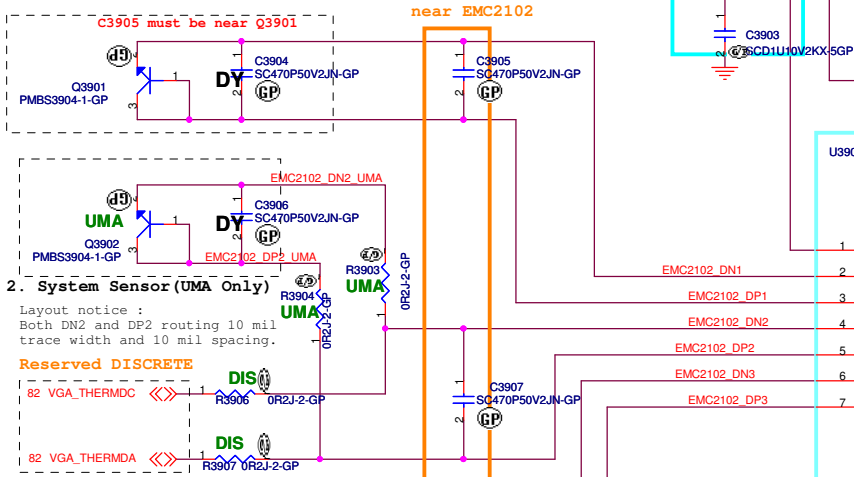
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# SSID = Thermal

## 1. Place near CPU PWM CORE and PCH.

Layout notice :  
Both DN1 and DP1 routing 10 mil  
trace width and 10 mil spacing.



## 2. System Sensor (UMA Only)

Layout notice :  
Both DN2 and DP2 routing 10 mil  
trace width and 10 mil spacing.

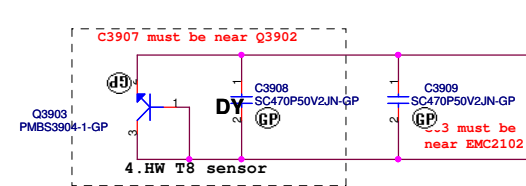
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82 VGA\_THERMDC <<<

82 VGA\_THERMDA <<<

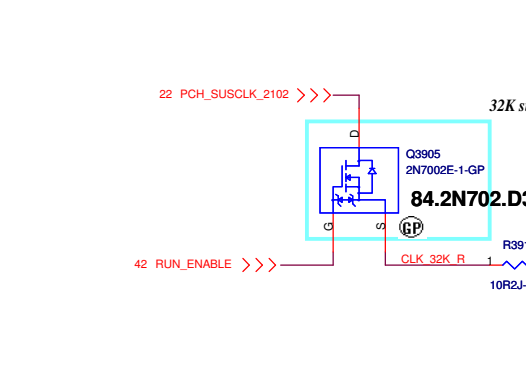
## 3. VGA Sensor (DISCRETE Only)

Layout notice :  
Both VGA\_THERMDA and VGA\_THERMDC routing  
10 mil trace width and 10 mil spacing.



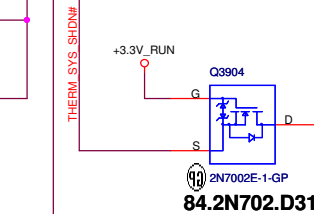
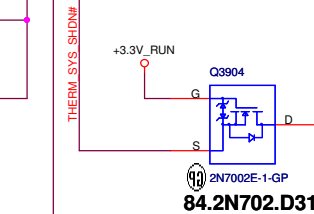
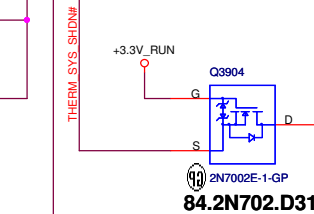
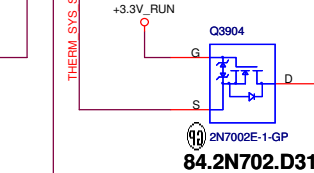
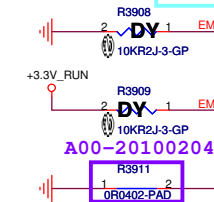
## 4. HW T8 sensor

Layout notice :  
Both DN3 and DP3 routing 10 mil  
trace width and 10 mil spacing.




GND = Channel 1  
OPEN = Channel 3  
+3.3V = Disabled

GND = Fan is OFF  
OPEN = Fan is at 60% full-scale  
+3.3V = Fan is at 75% full-scale



(Blanking)

<Core Design>



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Title

Size  
A3

Document Number  
**Berry**

Date: Wednesday, February 10, 2010

Rev  
**A00**


Sheet 40 of 92

**Reserved**



(Blanking)

<Core Design>



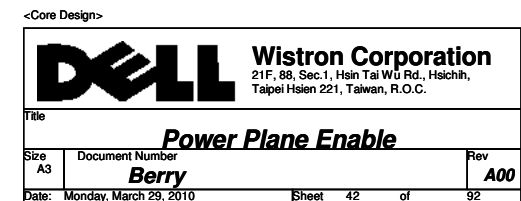
Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

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**<http://adf.ly/LOM1>**

(Blanking)

<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Size  
A3

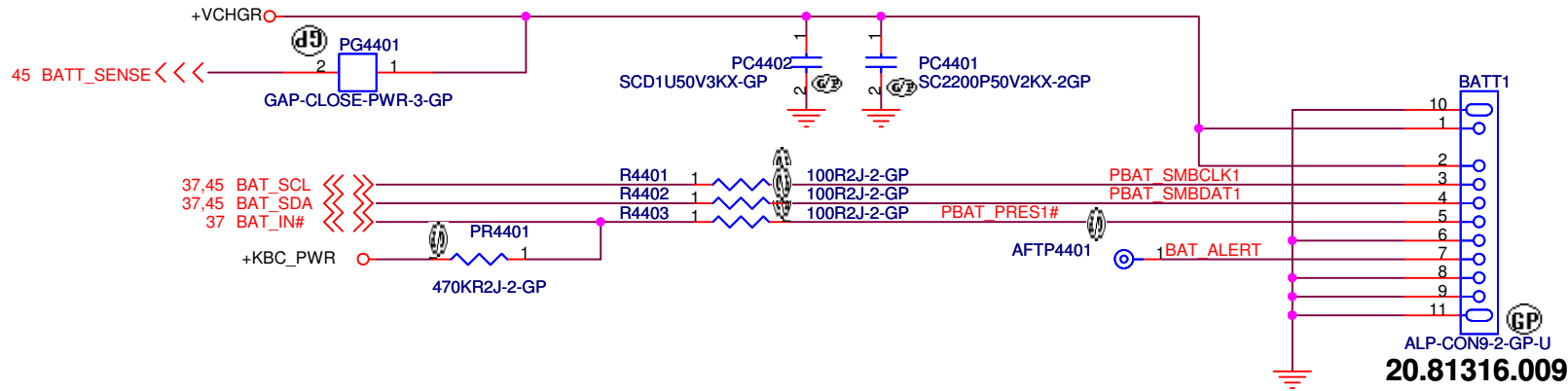
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**Berry**

Date: Wednesday, February 10, 2010

Rev  
**A00**

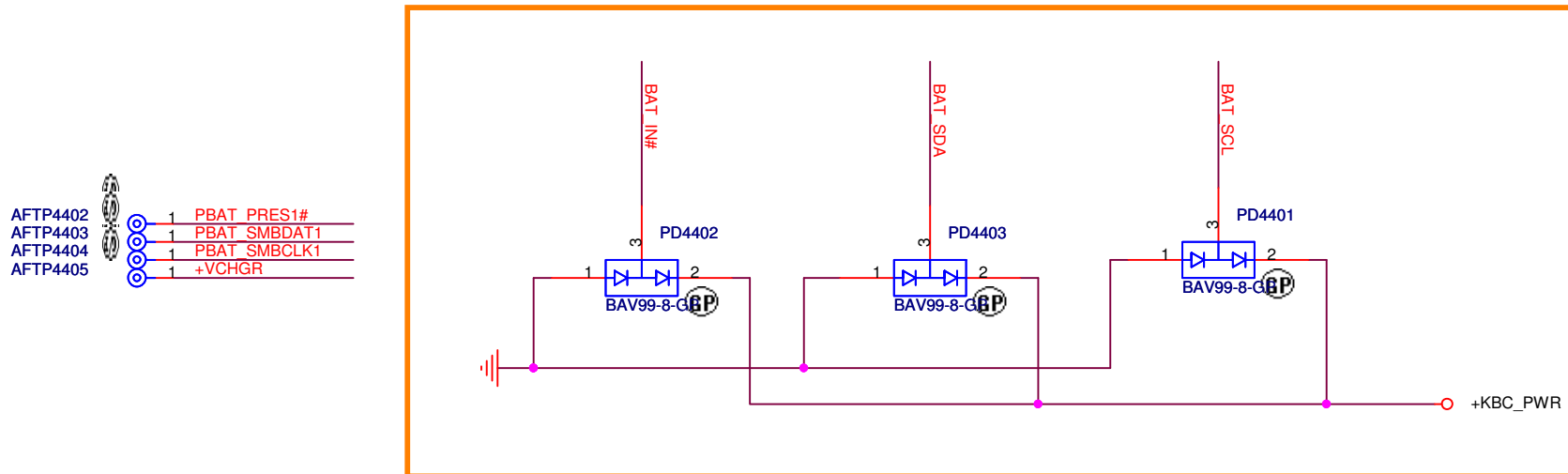
Sheet 43 of 92

**Reserved**



For actual location, need to be swap all pin

### Close to Batt Connector



<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

**BATT CONN**

Size  
A4

Document Number

**Berry**

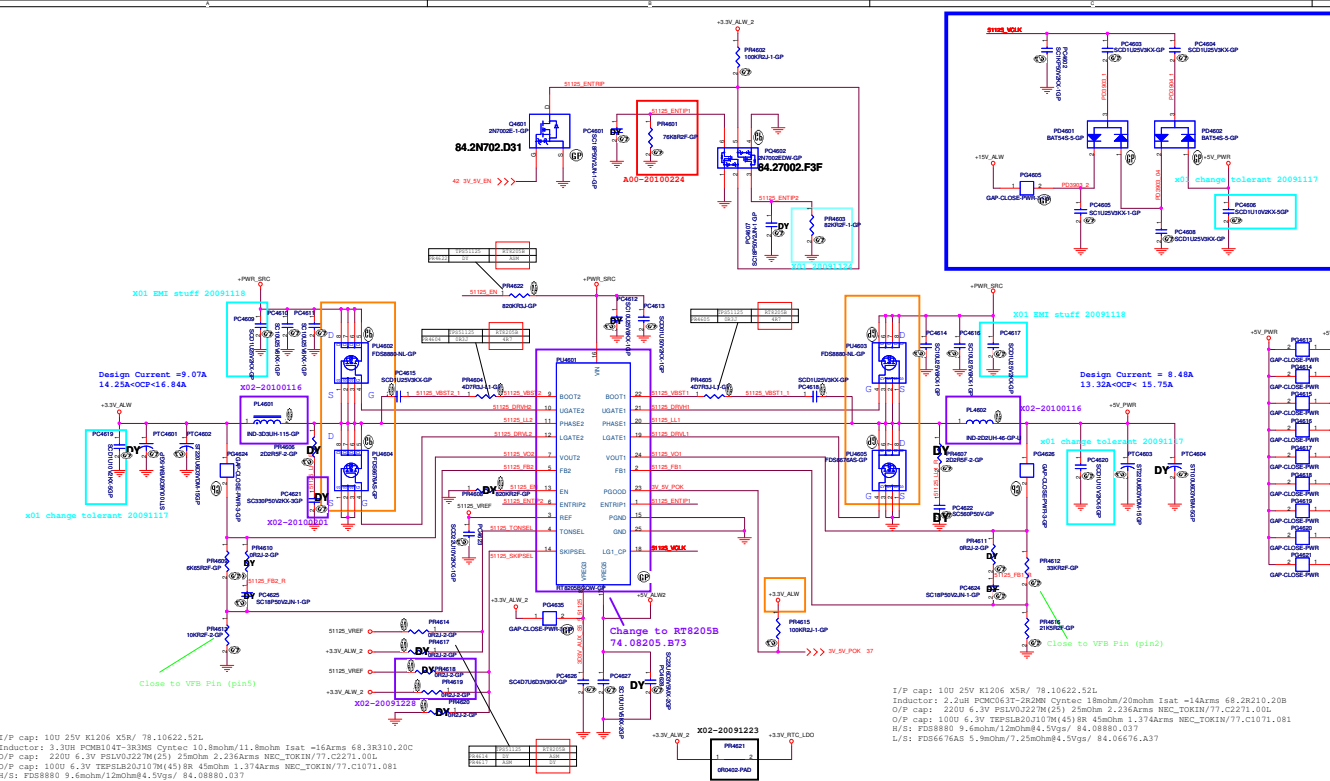
Rev

**A00**

Date: Monday, March 29, 2010

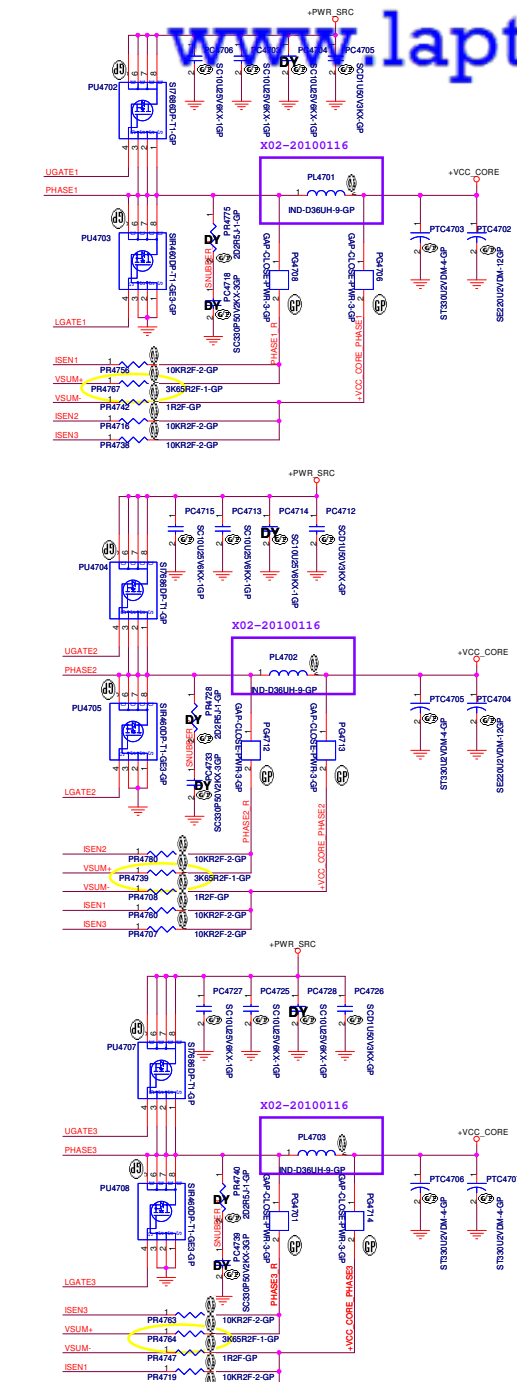
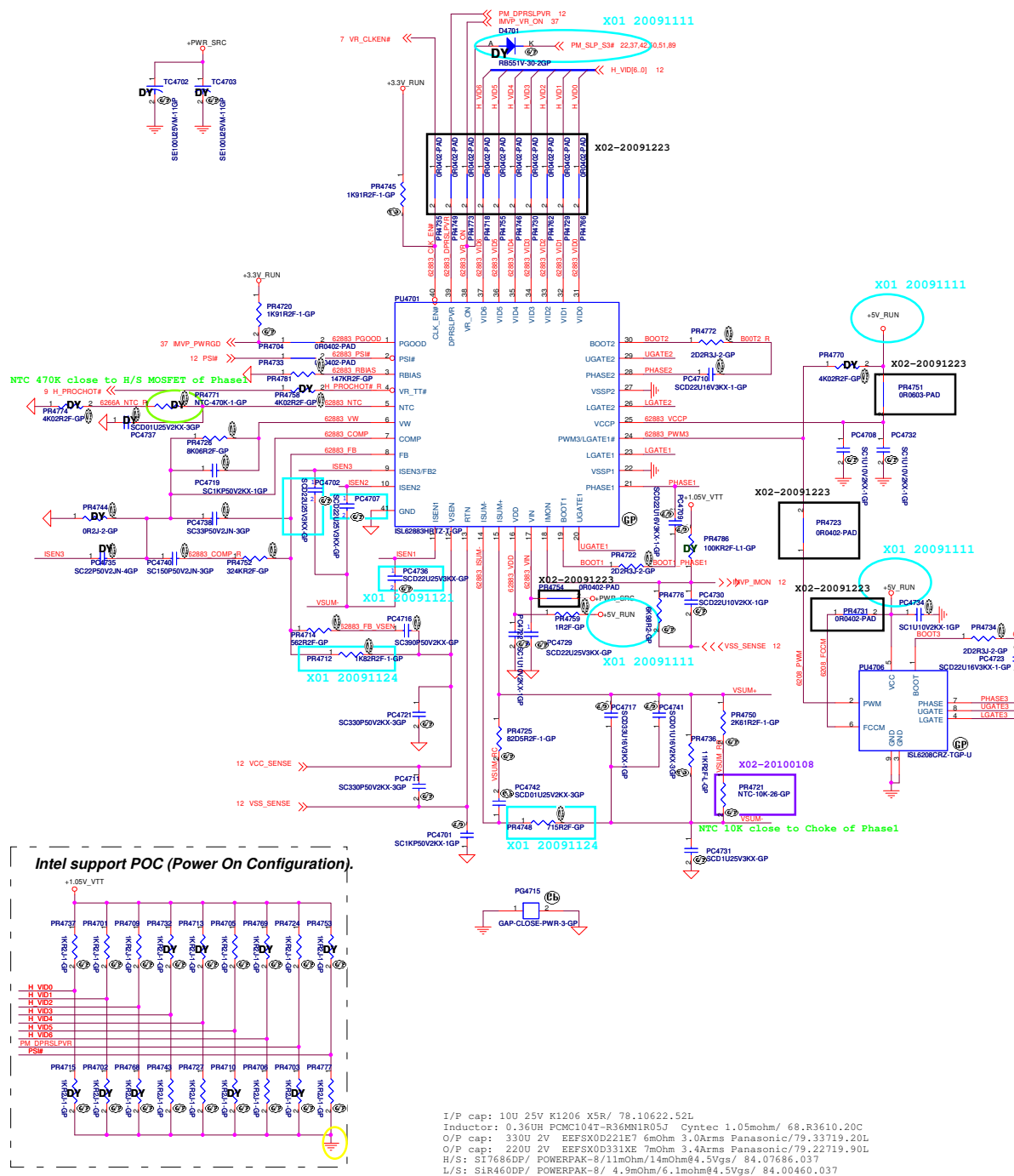
Sheet 44 of 92





TUNNEL		CH1	CH2	SKIPSEL	VRNG3 or VRNG5	VREF(2V)	QND
QND	205KHz	245KHz	245KHz	Operating Mode	OGA Auto Skip	Auto Skip	PWM only
VREF	245KHz	355KHz	355KHz				
VRNG3	305KHz	375KHz	375KHz				
VRNG5	355KHz	465KHz	465KHz	EMO	Open	820KHz to QND	QND
				Operating Mode	enable both LDGs, VCIL off and ready to turn on switcher channels	enable both LDGs, VCIL off and ready to turn on switcher channels	disable all circuit


TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3	365kHz	460kHz
VREG5	365kHz	460kHz



Design Current = 48A  
 52.8A<OCP<67.2A

(Blanking)

<Core Design>



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Title

*Reserved*

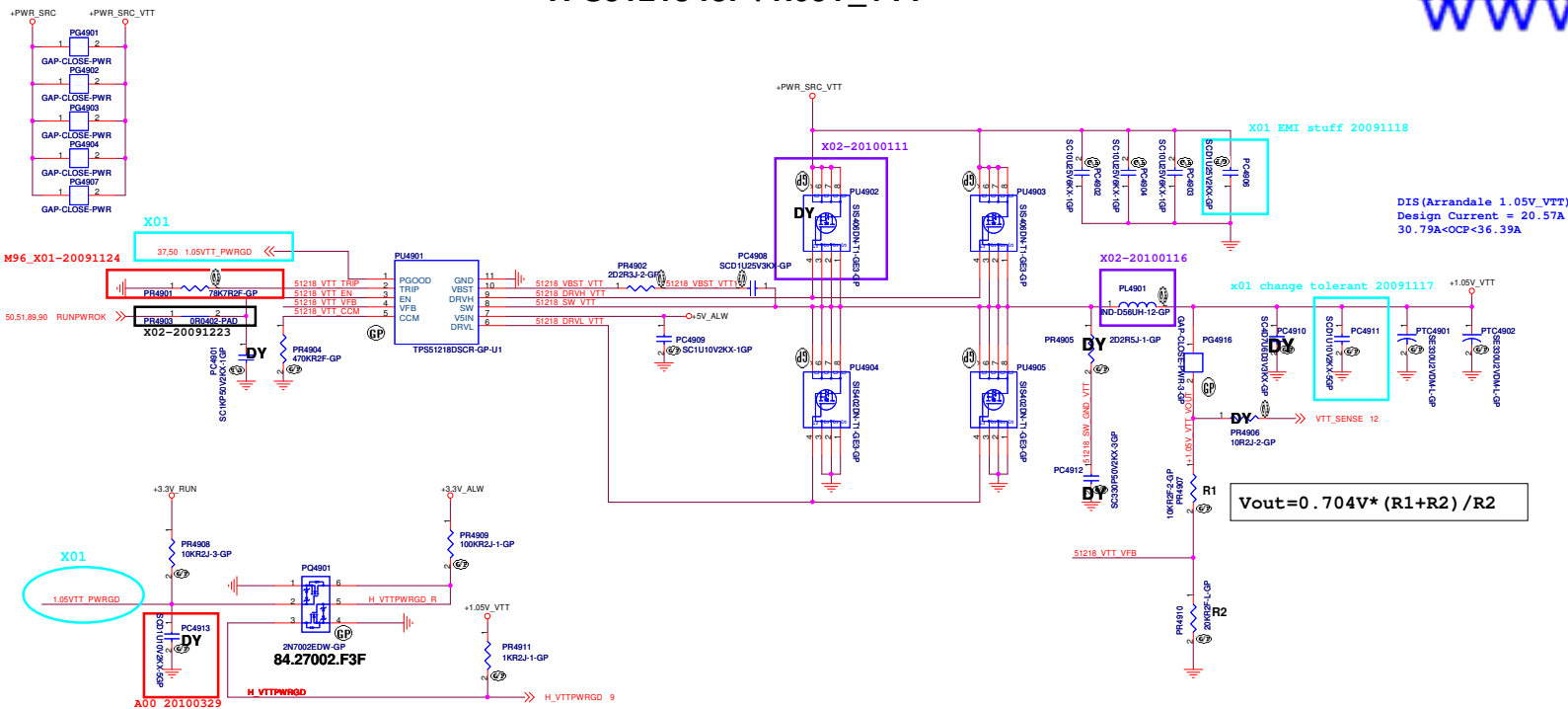
Size	Document Number	Rev
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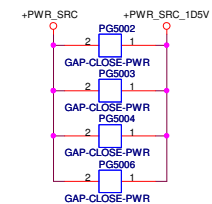
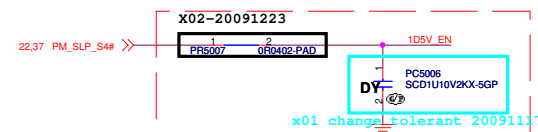
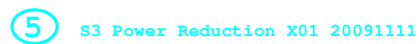


# TPS51218 for +1.05V\_VTT

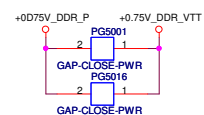
www.laptopblue.vn




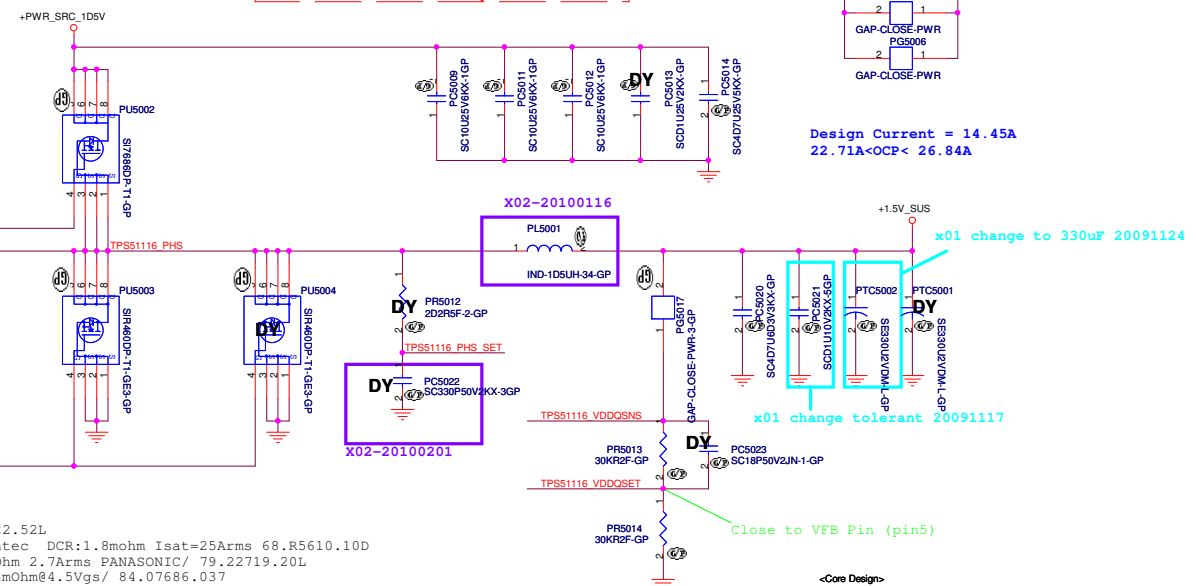
I/P cap: 10U 25V K1206 X5R/ 78.10622.52L  
 Inductor: 0.56uH PCMC104T-R56M Cyntec DCR:1.6mohm/1.8mohm Isat=25Arms 68.R5610.10D  
 O/P cap: 330U 2.5V EEFSX0D331ER 9mOhm 3Arms PANASONIC/ 79.33719.L01  
 H/S: S1S406DN/ POWERPAK-8/ 11.5mOhm/14.5mOhm @4.5Vgs/ 84.00406.037  
 L/S: S1S402DN/ POWERPAK-8/ 6.4mOhm/8mohm@4.5Vgs/ 84.00402.037



+0D75V\_DDR\_P Design Current = 0.7A



TPS51116\_UGT  
TPS51116\_VBST1 1   
PC5019  
SCD1U25V3KX-GF



Close to VFB Pin (pin5)

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L  
Inductor: 0.56uH PCMC104T-R56mN Cynotec DCR:1.8mohm Isat=25Arms 68.R5610.10D  
O/P cap: 220U 2V EEFXC04D221ER 15mOhm 2.7Arms PANASONIC/ 79.22719.20L  
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037  
L/S: SIr460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037  
Switching freq-->400KHz




[illegible]

$$V_{out} = 0.8V * (R1 + R2) / R2$$

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<Core Design>

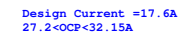


Wistron Corporation  
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

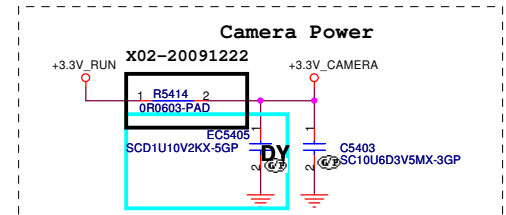
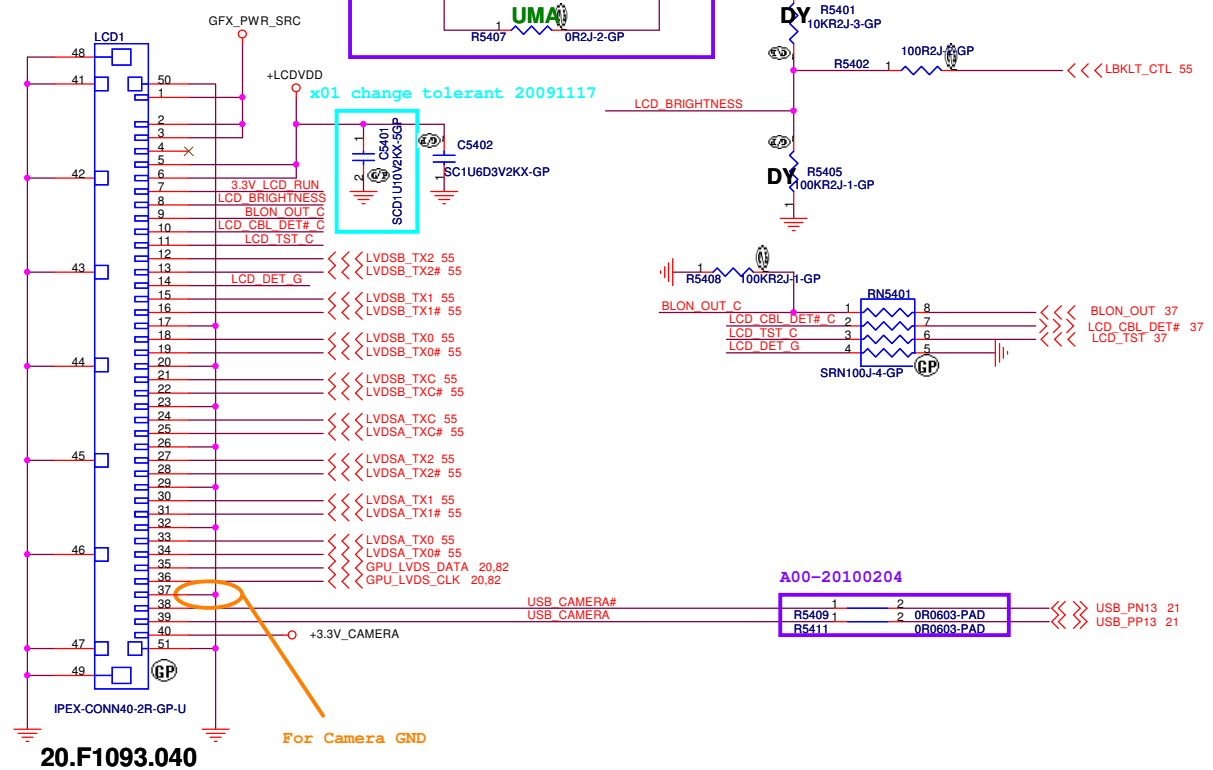
Size	Document Number	Rev
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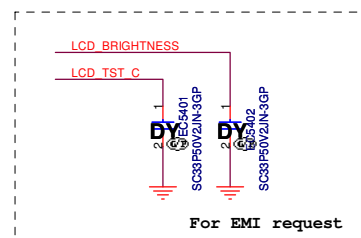
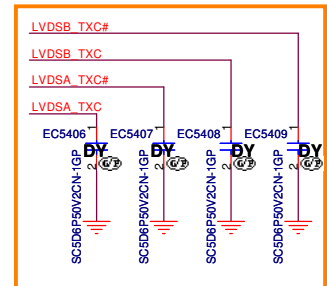
Close to choke (L5301)

SSID = VIDEO

LVDS CONNECTOR



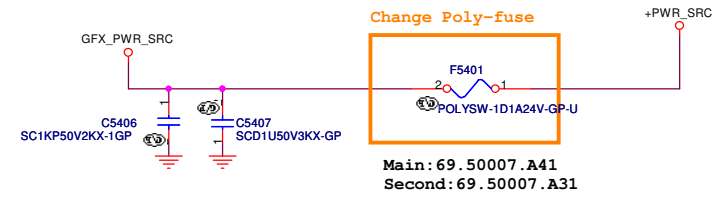
Close to LVDS connector



SSID = Inverter

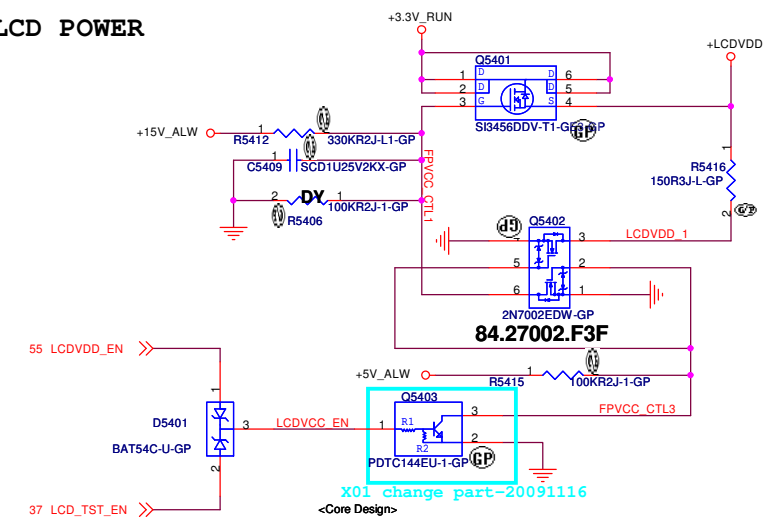
www.laptopblue.vn

INVERTER POWER



SSID = VIDEO

LCD POWER



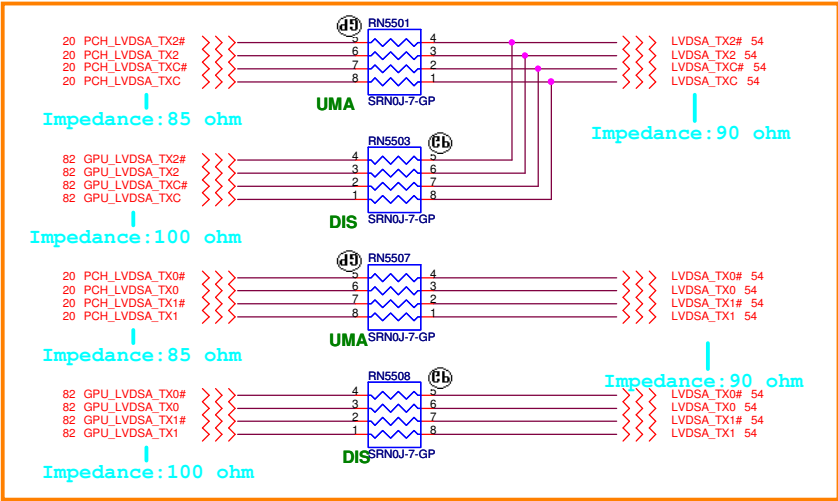
**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,  
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LCD/Inverter Connector**

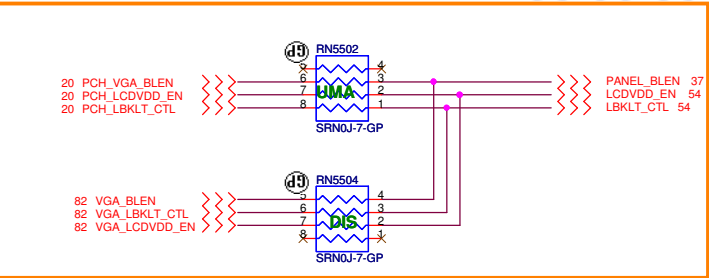
Size: A3	Document Number: <b>Berry</b>	Rev: <b>A00</b>
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<http://adf.ly/LOM1>

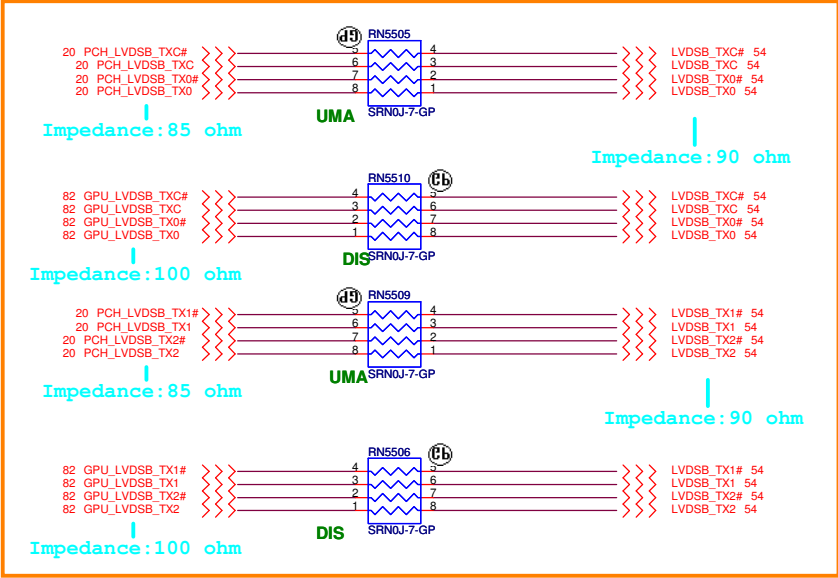
LVDS Channel A



Panel BL brightness/Power on/BI/en




LVDS Channel B



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<Core Design>



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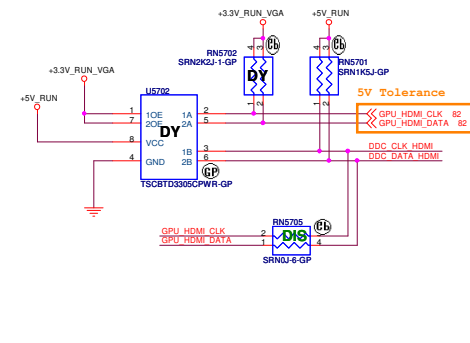
Title

**LVDS Switch**

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H\_CPURST# use pull-up Resistor close  
ITP connector 500 mil ( max ),  
others place near CPU side.



\*Layout\* 15 mil

39 EMC2102\_FAN\_TACH <<< AFTP5801

39 EMC2102\_FAN\_DRIVE >>>

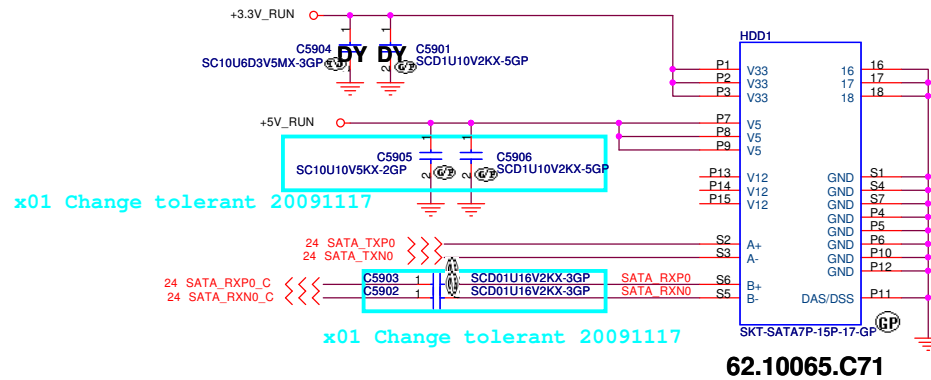
C5801  
SC10U6D3V5MX-3GP

D5801  
RB551V-30-2GP

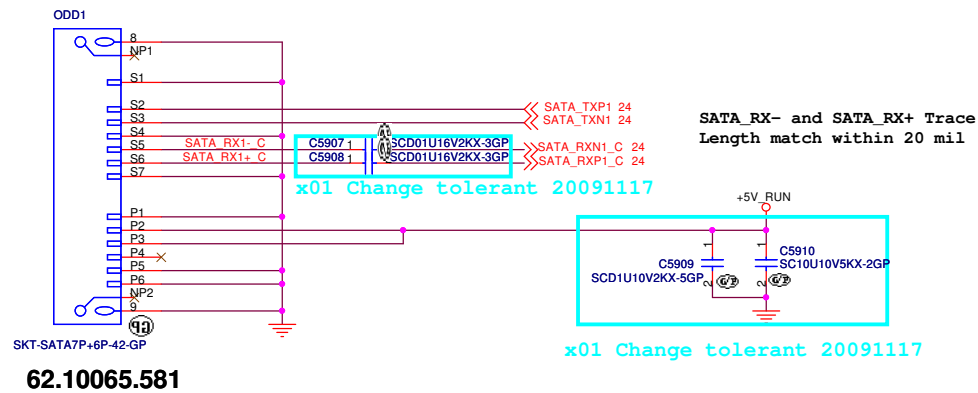
FAN1  
FOX-CON3-6-GP-U

20.D0210.103

## SATA HDD Connector



## ODD Connector

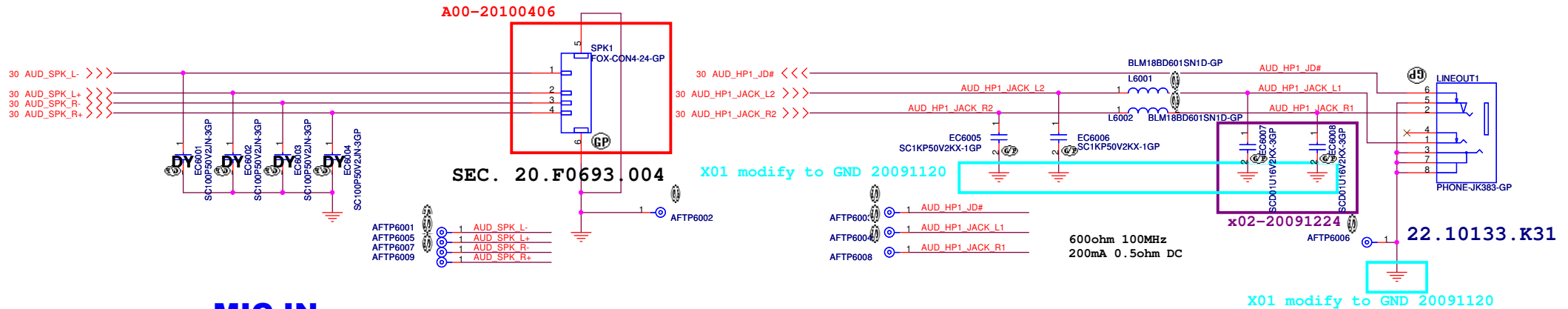


SSID = AUDIO

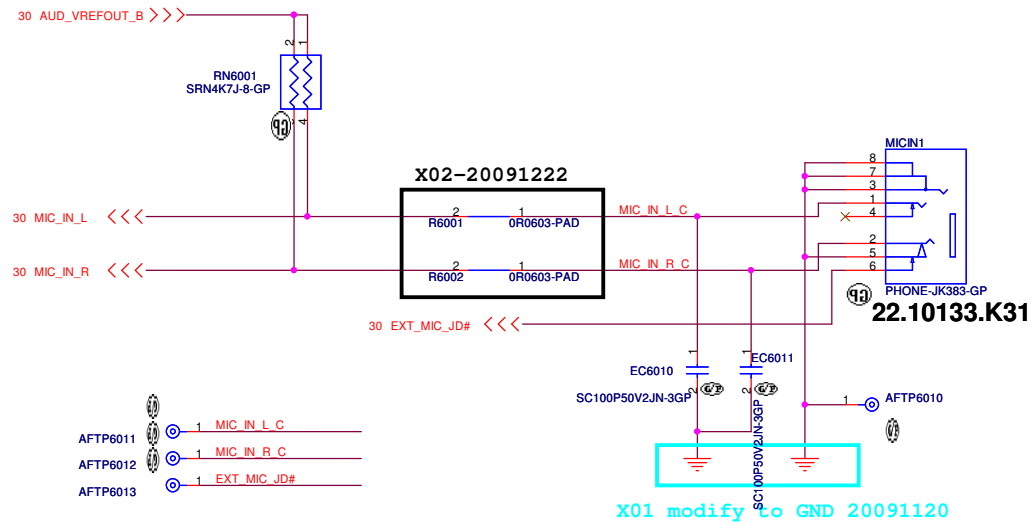
www.laptopblue.vn

## Speaker Connector

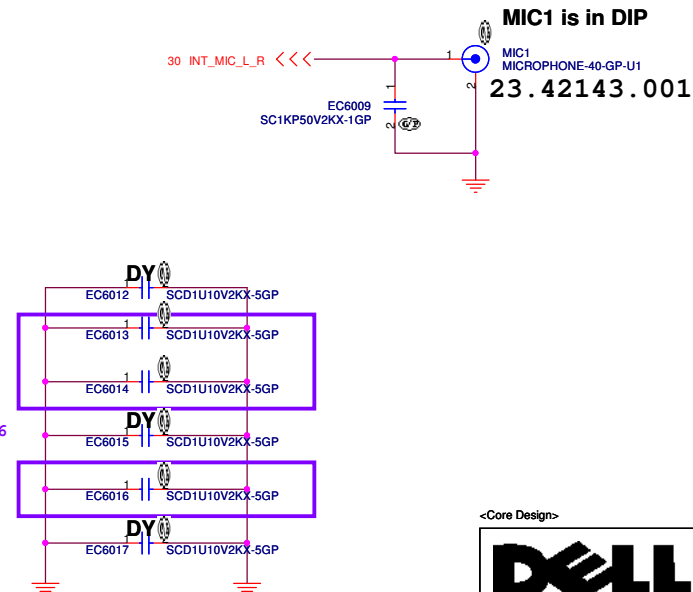
## LINE1 OUT



## MIC IN



## Internal Microphone



<Core Design>


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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
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Title			Audio Jack	
Size	Document Number	Rev		
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<http://adf.ly/LOM1>

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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

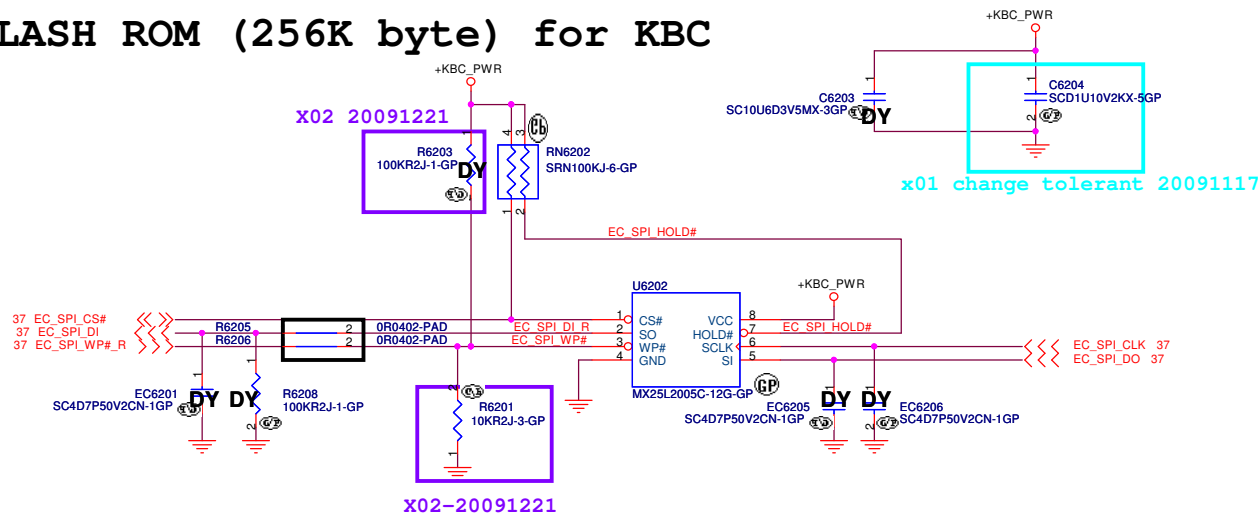
Title

*Reserved*

Size	Document Number	Rev
A3	<i>Berry</i>	<b>A00</b>

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**SPI FLASH ROM (256K byte) for KBC**

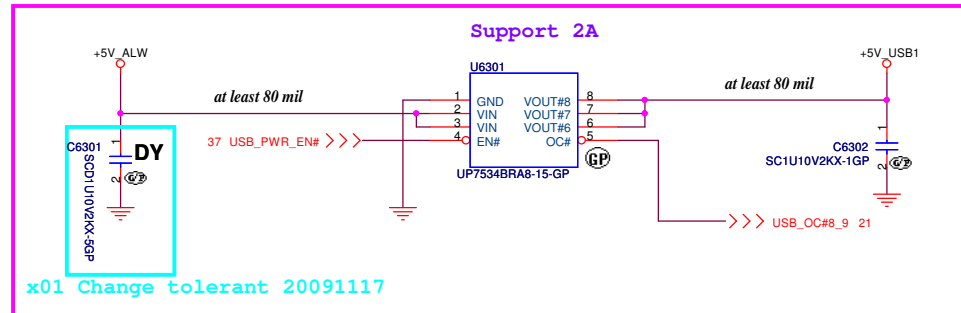
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SSID = USB

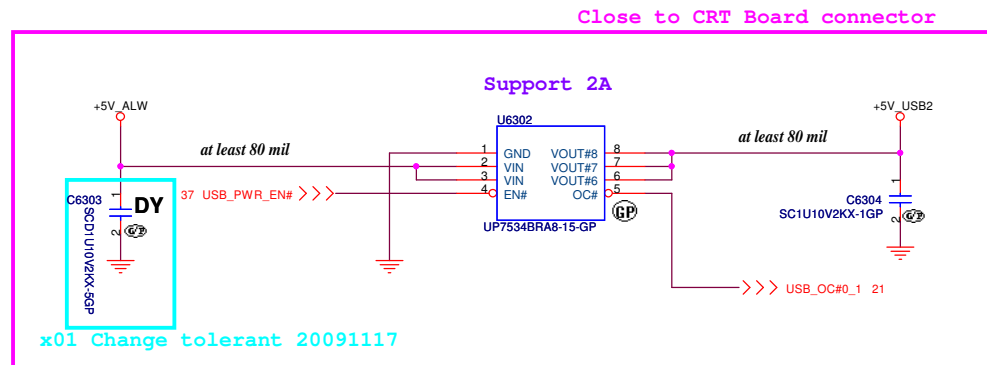
www.laptopblue.vn

## IO Board USB Power

USB POWER SW  
Main UP7534BRA8-15 P/N:74.07534.079  
SEC AP2101MPG-13 P/N: 74.02101.079



## CRT Board USB Power




<Core Design>

<b>DELL</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>USB Power SW</b>			
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<http://adf.ly/LOM1>

(Blanking)

<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

*Reserved*

Size  
A4

Document Number  
*Berry*


Rev  
**A00**

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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

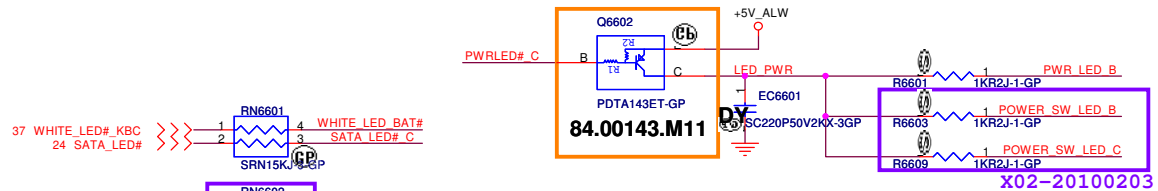
Title

*Reserved*

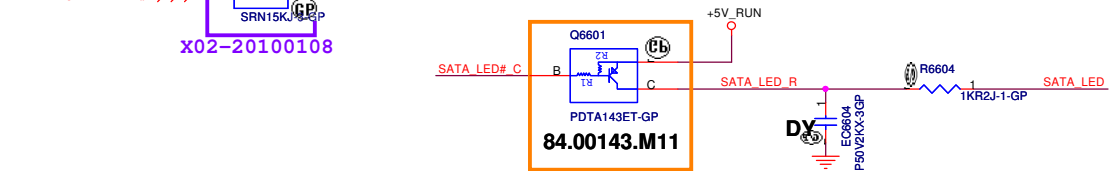
Size	Document Number	Rev
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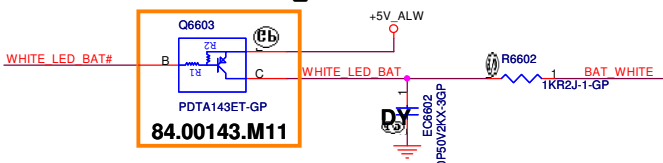
Power LED (White)



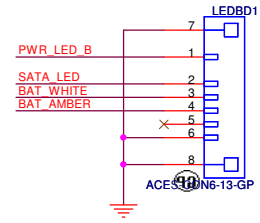
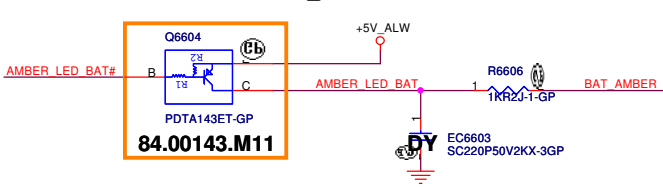
SATA HDD LED (White)



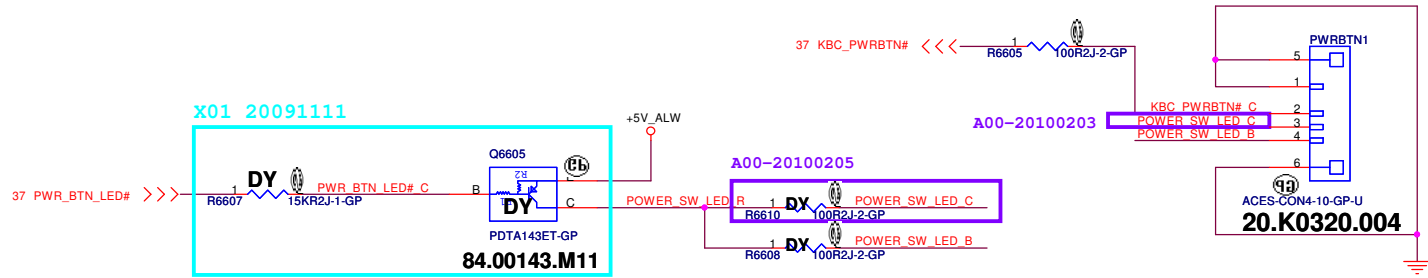
Battery LED1 (White)



Battery LED2 (Amber)




Power button LED (White)



(Blanking)

<Core Design>



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Title

Size  
A3

Document Number  
**Berry**

Date: Wednesday, February 10, 2010

Rev  
**A00**

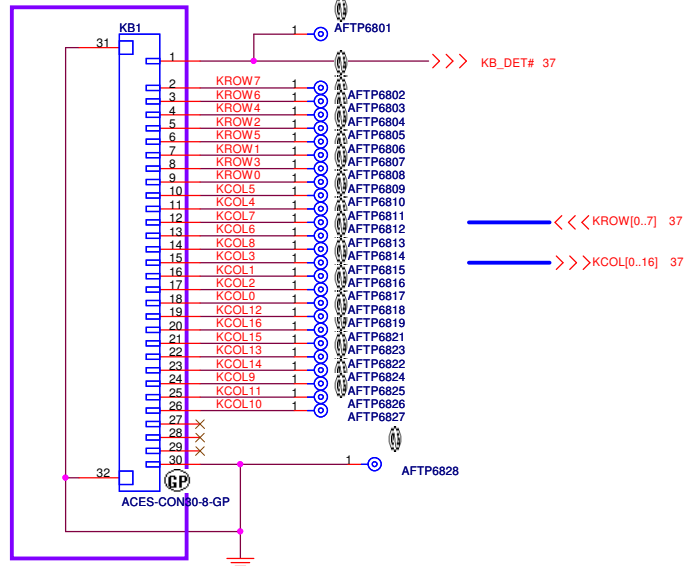
Sheet 67 of 92

**Reserved**

SSID = KBC

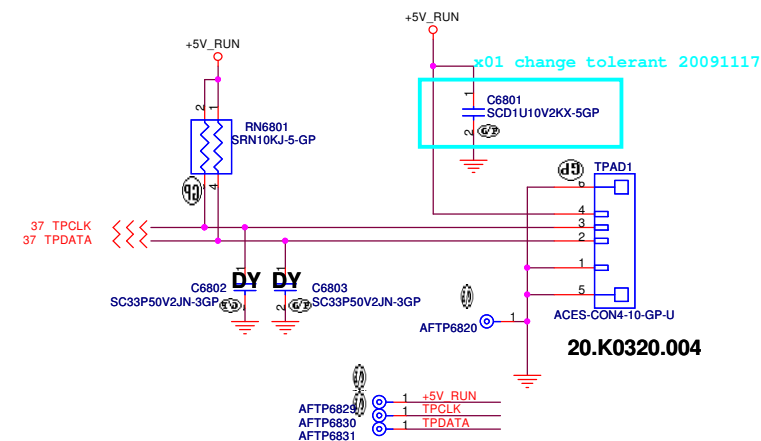
## Internal Keyboard Connector

A00-20100203



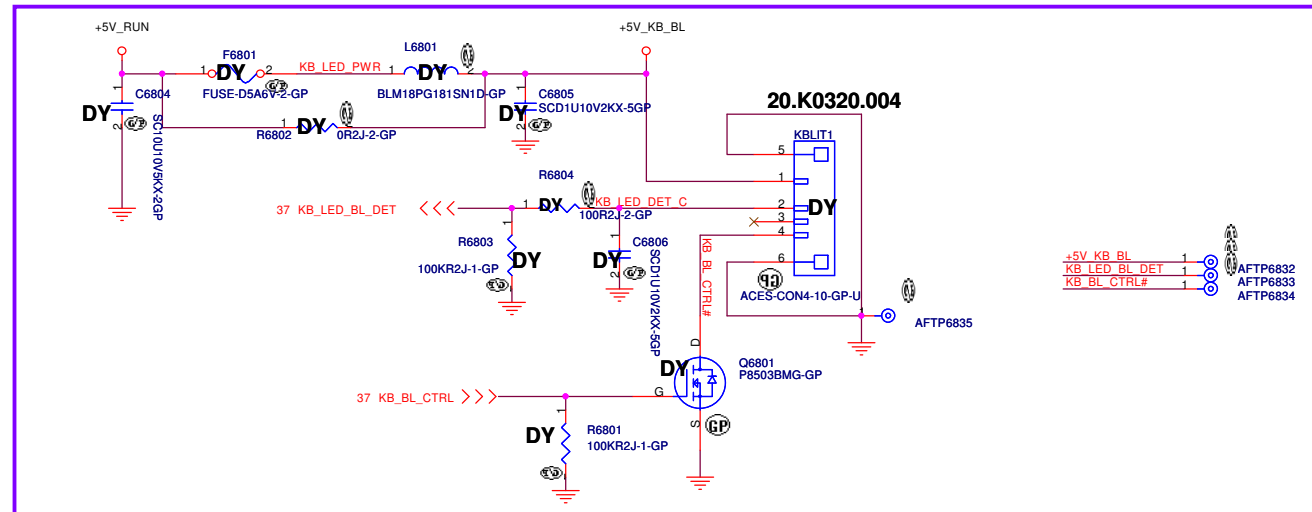
SSID = Touch.Pad

## TouchPad Connector



## KB Backlight Connector

A00-20100205



<http://adf.ly/LOM1>

<Core Design>



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Title

**Key Board/Touch Pad**

Size

Document Number

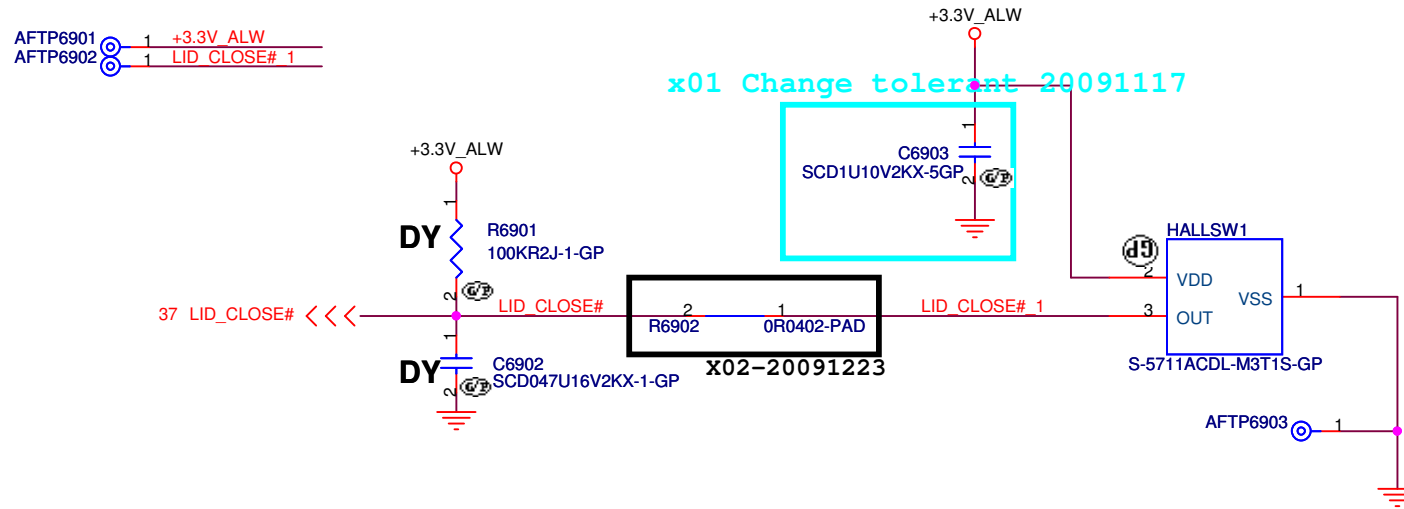
**Berry**

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<Core Design>



**Wistron Corporation**  
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Title

**Hall Sensor**

Size  
A4

Document Number

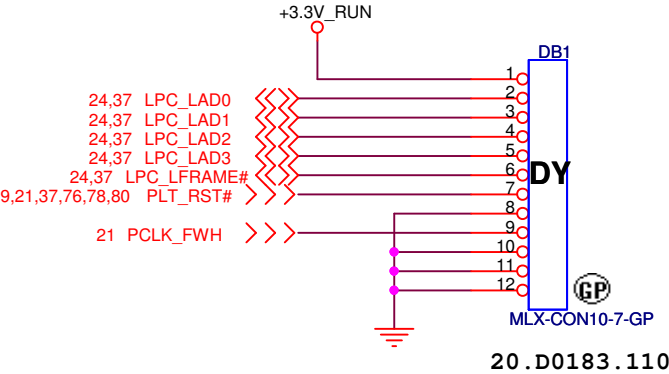
**Berry**

Rev


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<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>Dubug connector</b>			
Size A4	Document Number <b>Berry</b>		Rev <b>A00</b>
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(Blanking)

<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>RESERVED</b>			
Size A4	Document Number <b>Berry</b>		Rev <b>A00</b>
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(Blanking)

<Core Design>



**Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Title

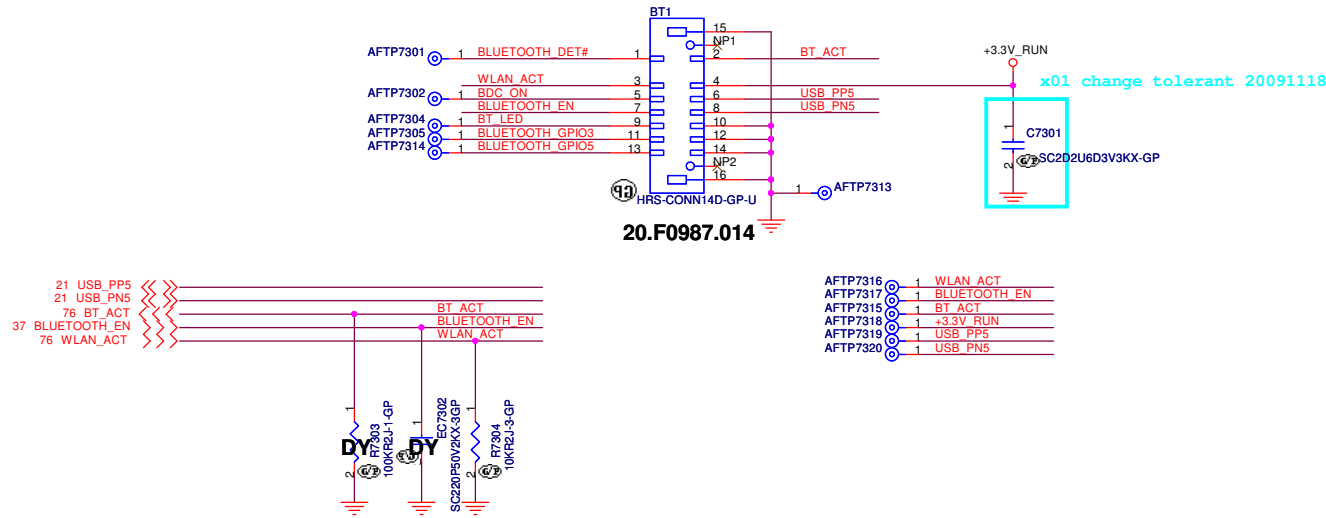
**RESERVED**

Size A3	Document Number <b>Berry</b>	Rev <b>A00</b>
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# Bluetooth Module conn.



<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

**Bluetooth**

Size

A3

Document Number

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Rev


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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title


*Reserved*

Size A3	Document Number <i>Berry</i>	Rev <b>A00</b>
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<Core Design>



**Wistron Corporation**  
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Title

*Reserved*

Size  
A4

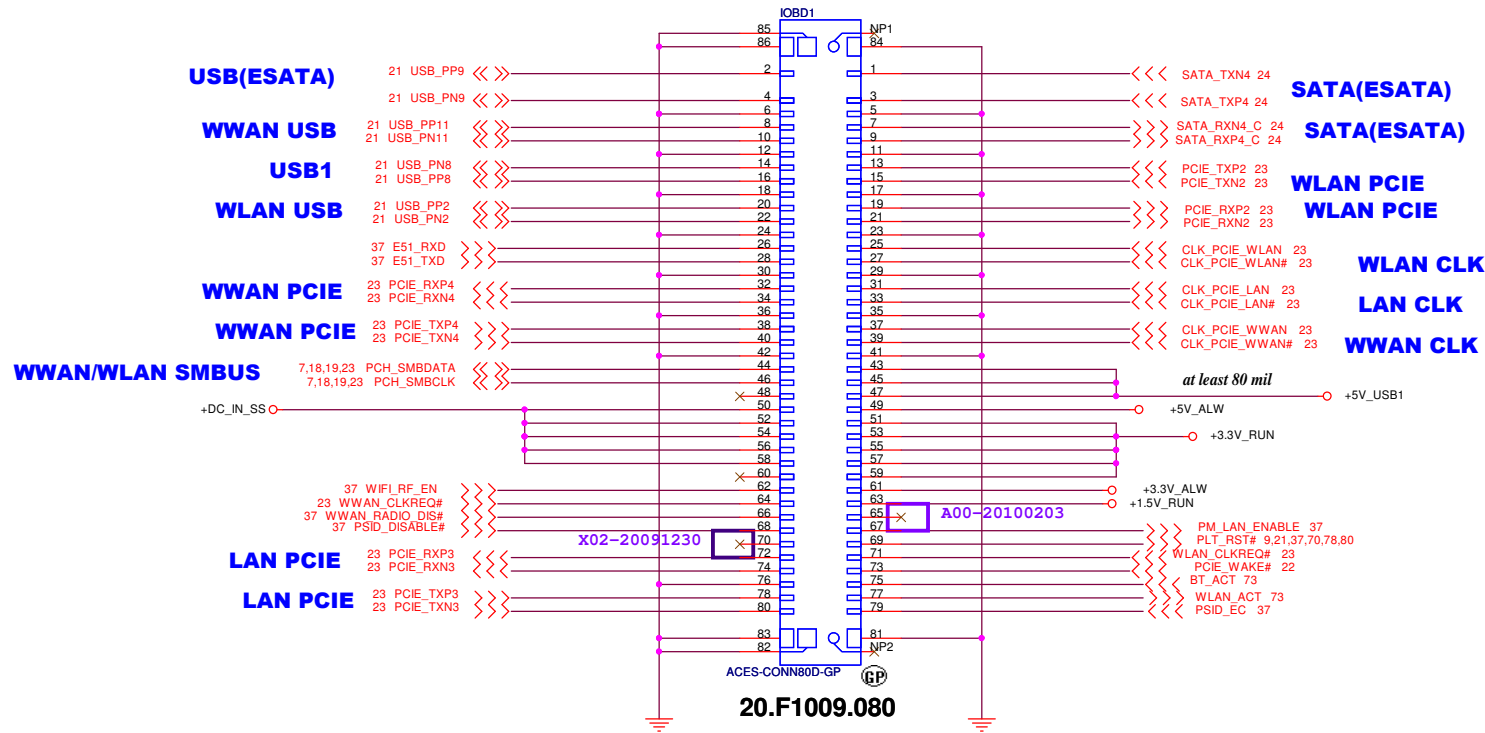
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# IO Board CONN 80 pin

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<http://adf.ly/LOM1>

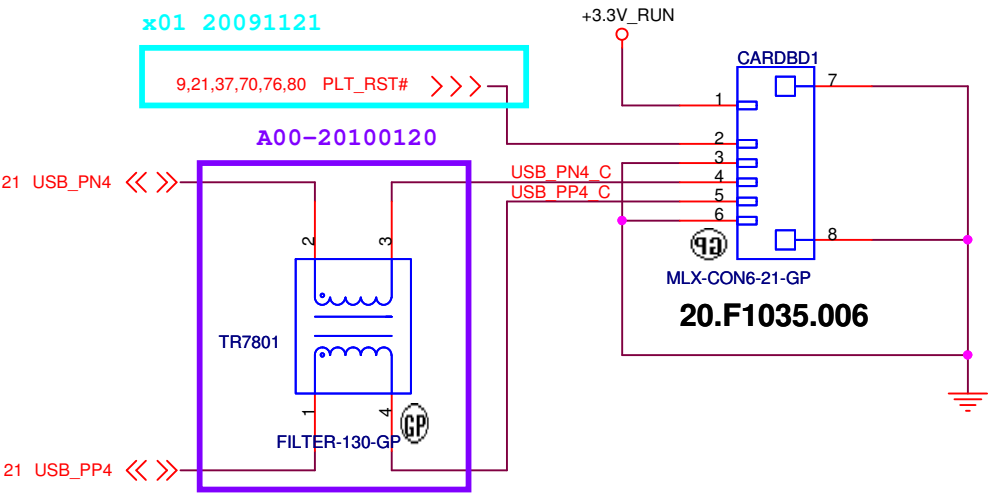
<Core Design>

<b>DELL</b>		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>IO Board Connector</b>			
Size A3	Document Number <b>Berry</b>	Rev <b>A00</b>	
Date: Monday, March 29, 2010	Sheet 76	of 92	




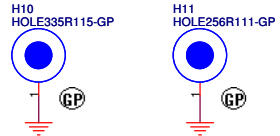
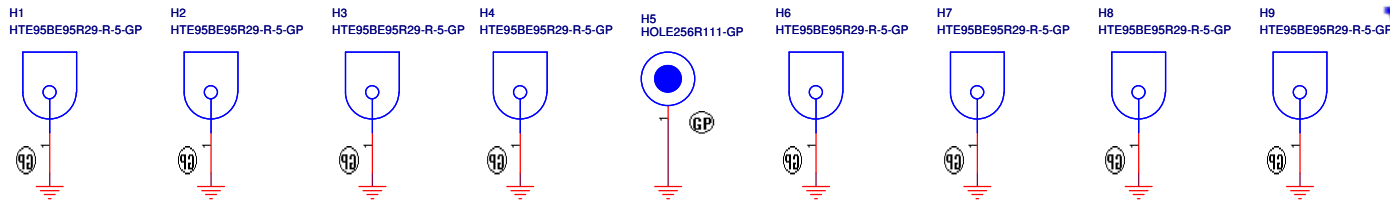
SSID = SDIO

Card Reader connector

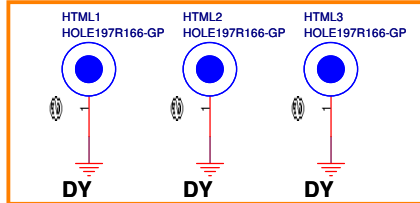


<Core Design>

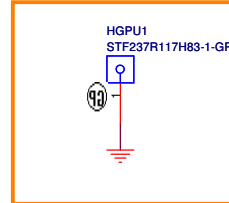
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>CARD Reader CONN</b>			
Size A4	Document Number <b>Berry</b>		Rev <b>A00</b>
Date: Monday, March 29, 2010		Sheet 78 of	92



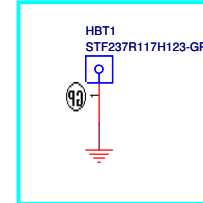
CPU Thermal module hole



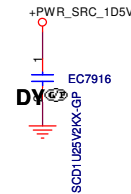
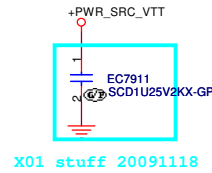
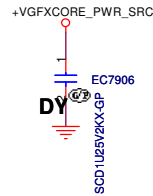
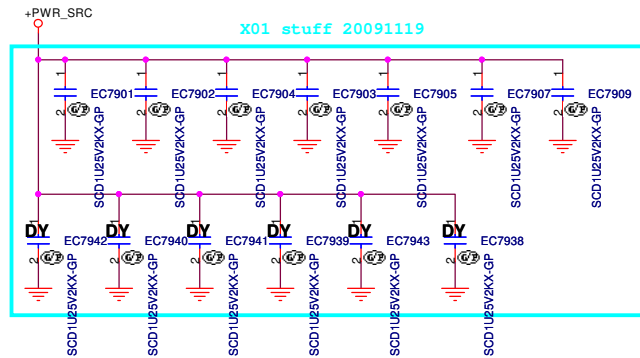
GPU Thermal module hole



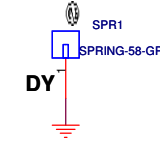
stand off



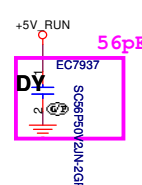
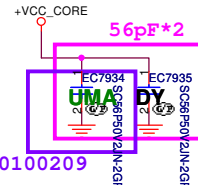
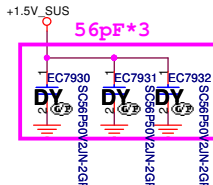
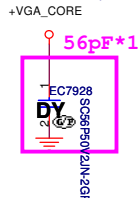
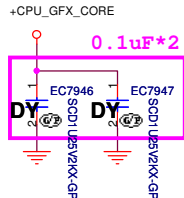
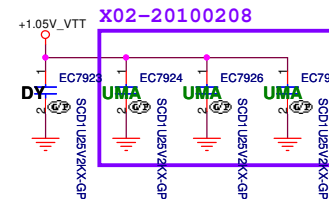
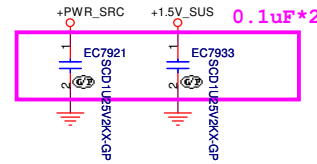
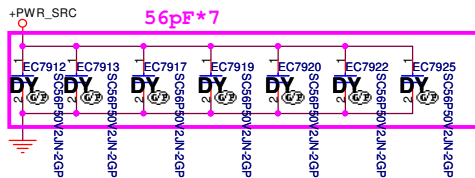
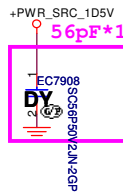
EMI Reserve



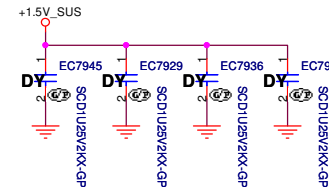
EMI Reserve



X01 RF Reserved-20091118



X02-20100209



A00-20100204

<Core Design>

**DELL** Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title	UNUSED PARTS/EMI Capacitors		
Size	Document Number	Rev	A00
A3	Berry		
Date:	Wednesday, February 10, 2010	Sheet	79 of 92







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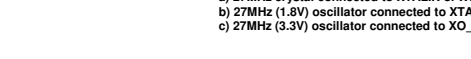
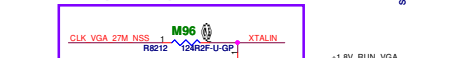
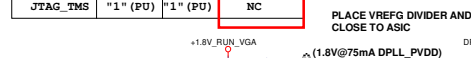
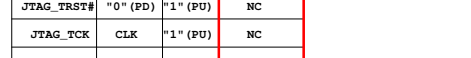
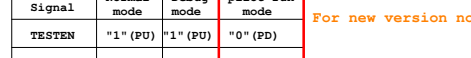
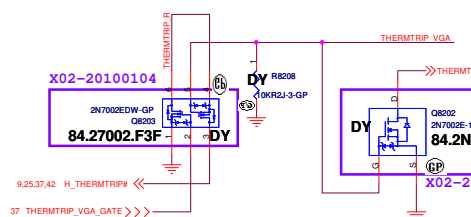
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# MEMORY ID Table

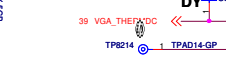
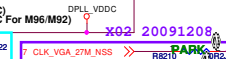
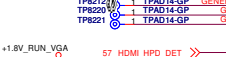
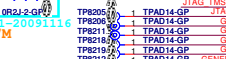
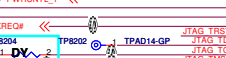
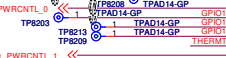
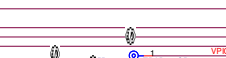
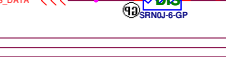
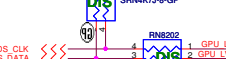
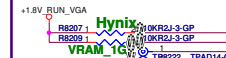
DVPDATA[0:3]	Description
0001	DDR3 Hynix-H5TQ1G63BFR-12C (800MHz) 64M*16
0011	DDR3 Hynix-H5TQ2G63BFR-12C (800MHz) 128M*16
0010	DDR3 SAMSUNG K4W2G1646E-HC12 (800MHz) 128M*16
0000	DDR3 SAMSUNG-K4W1G1646E-HC12 (800MHz) 64M*16

DVPDATA[0:3] Default: Pull down



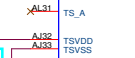
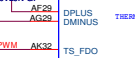
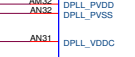
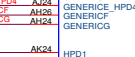
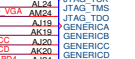
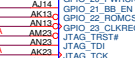
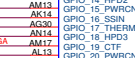
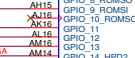
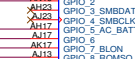
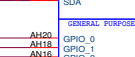
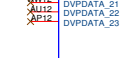
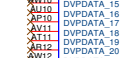
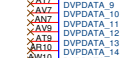
## MEM ID Control

X02-20091222



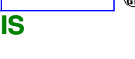
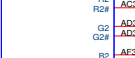
## MEM ID Control

X02-20091222



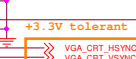
## MEM ID Control

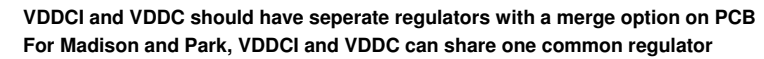
X02-20091222



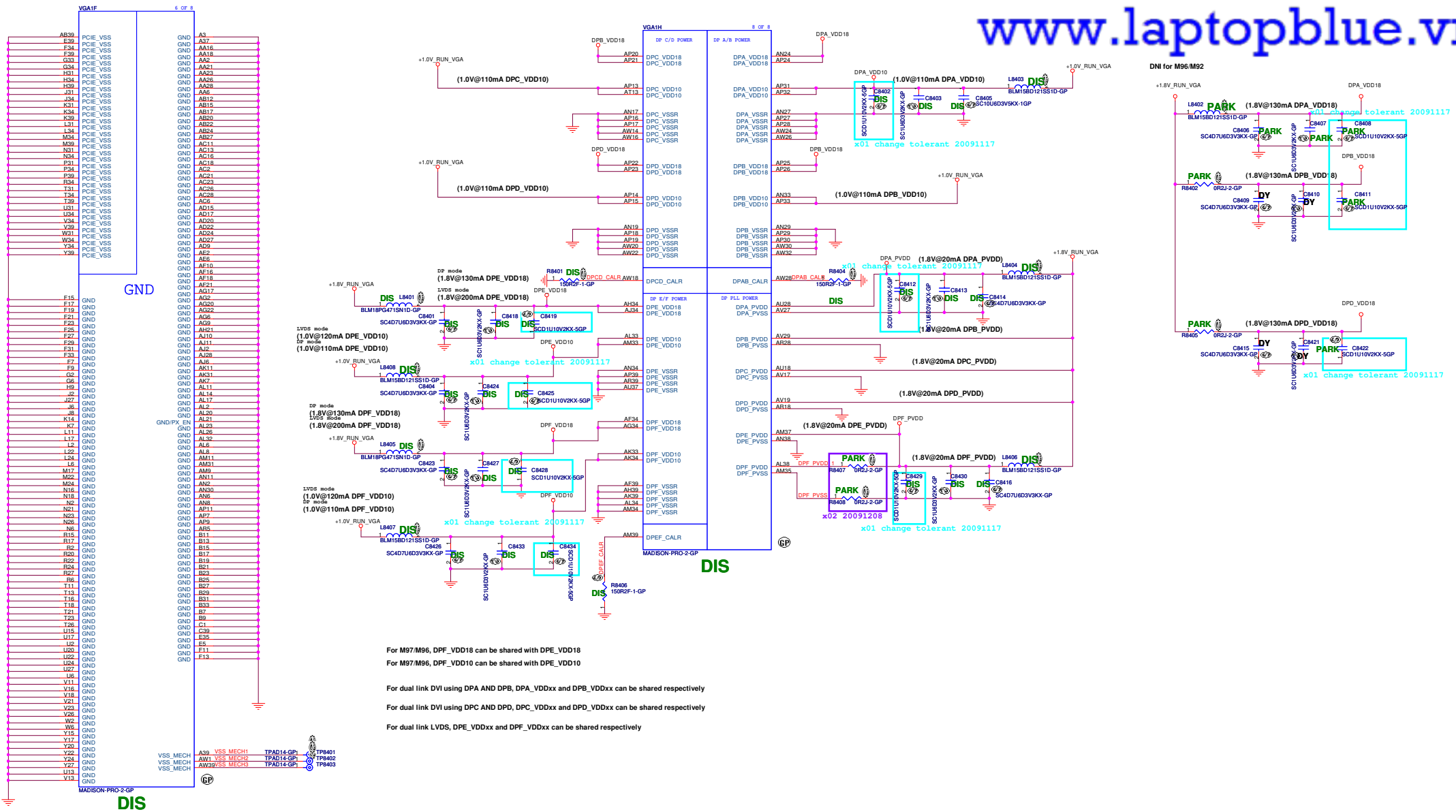
## MEM ID Control

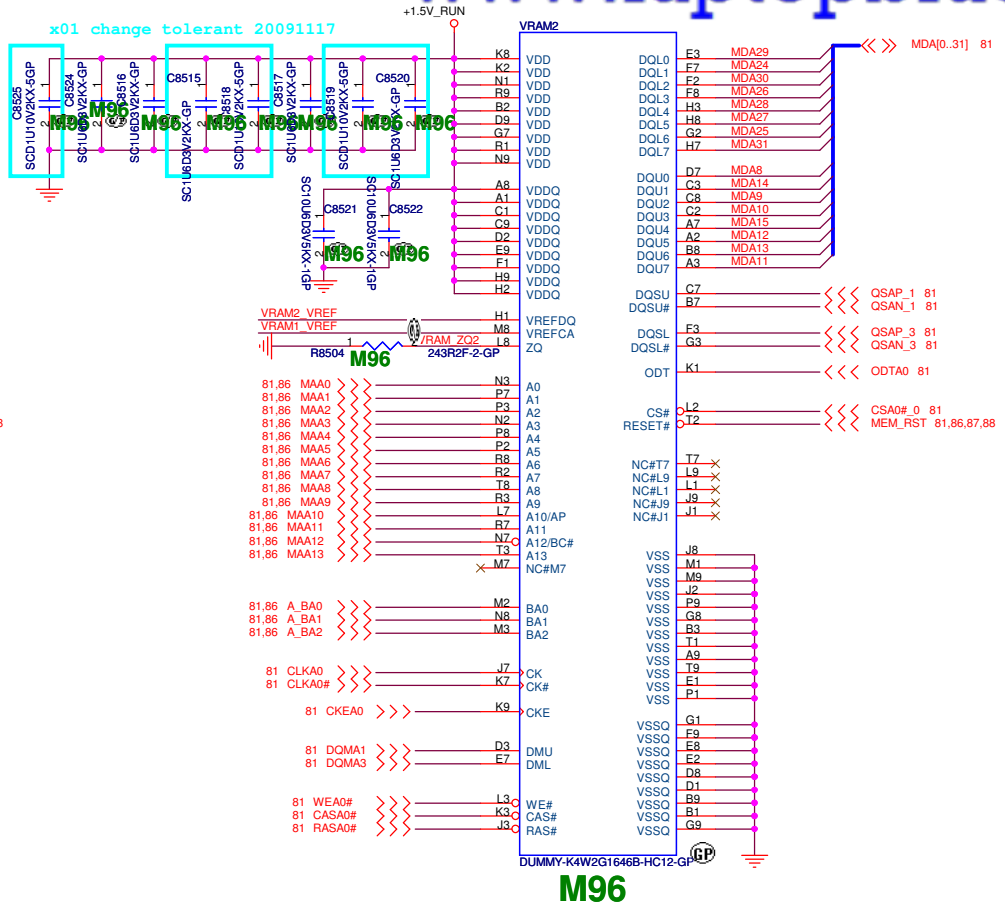
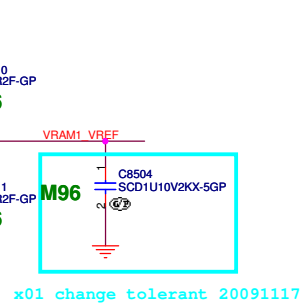
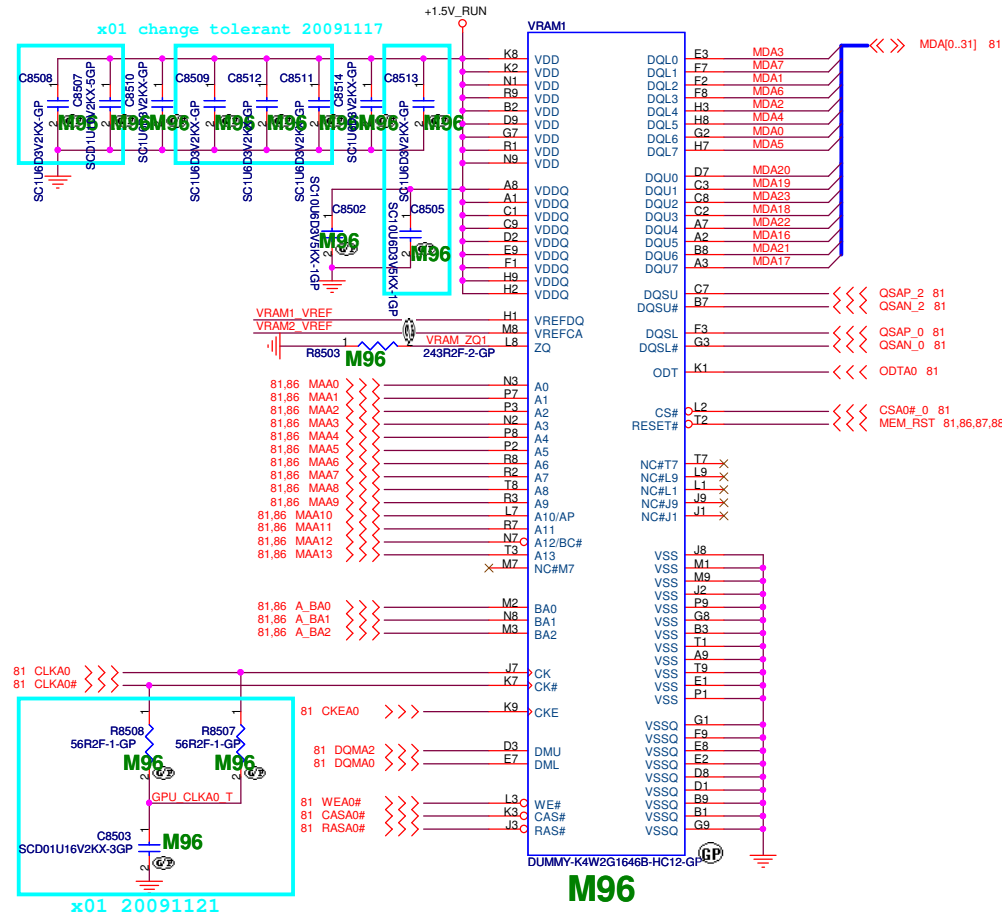
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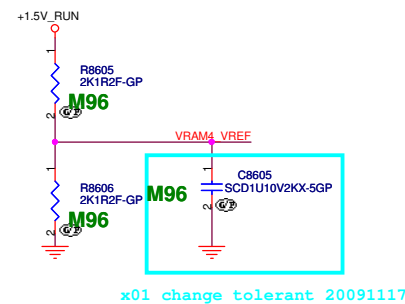
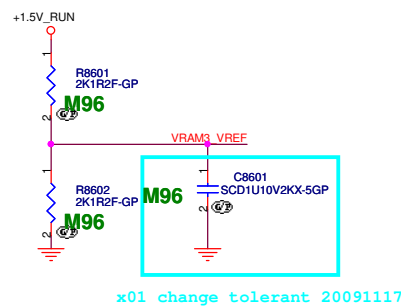
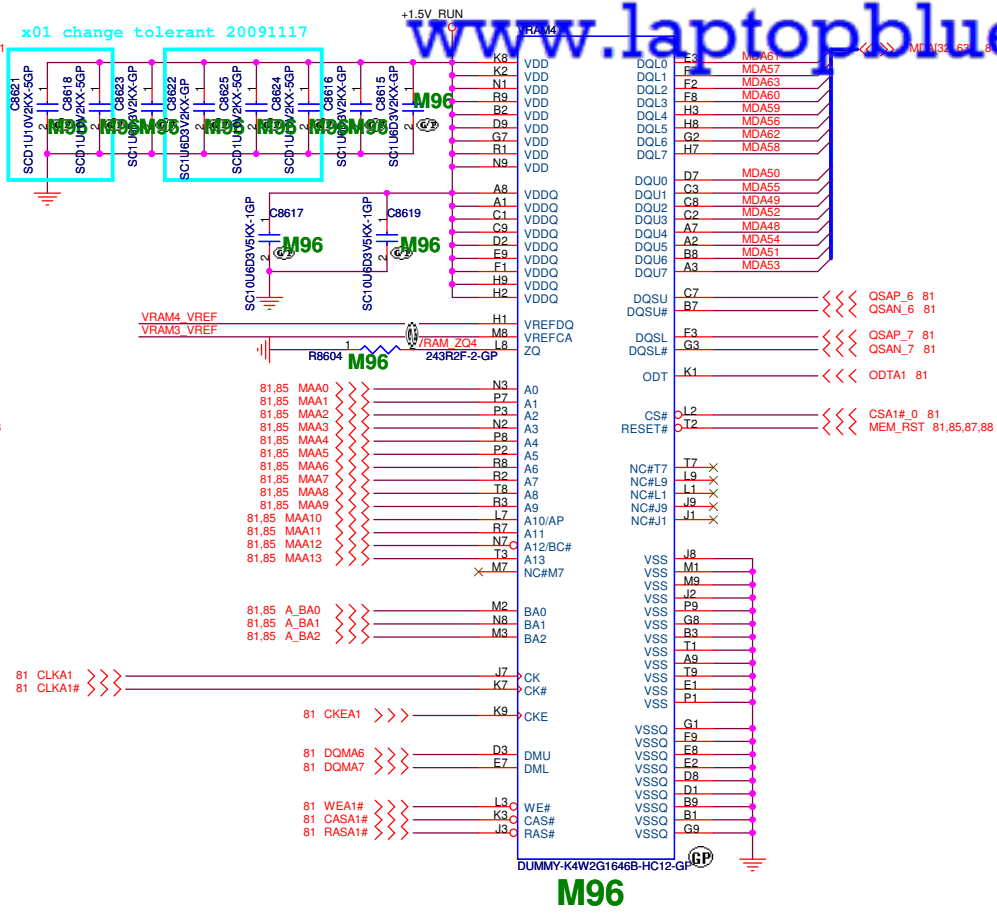
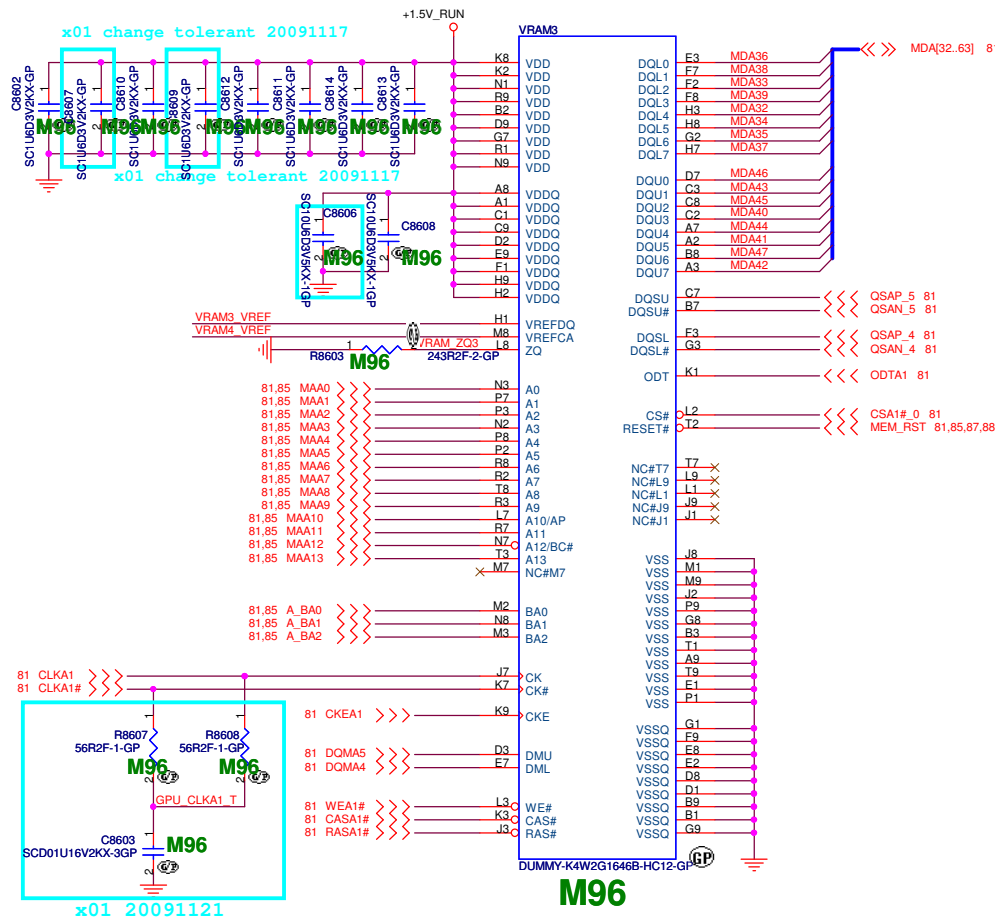


**NOTE4:**  
For M2 design compatibility, refer to the document AN\_M96\_Ax and AN\_M97\_Ax

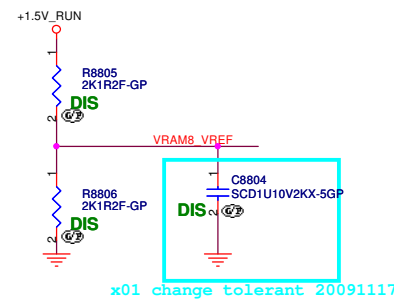
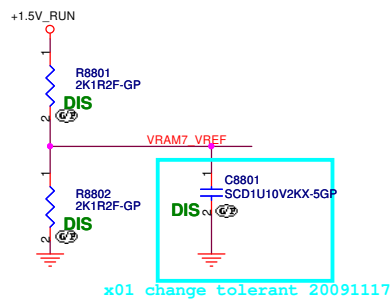
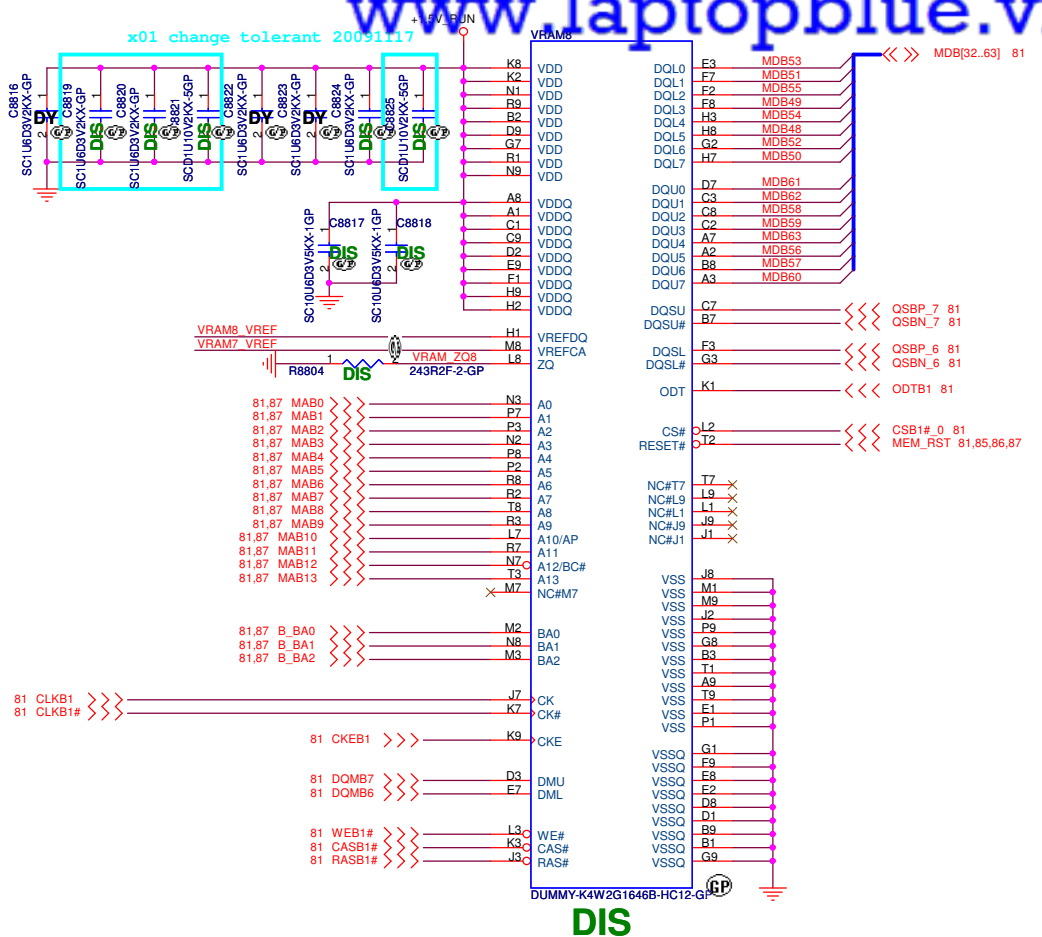
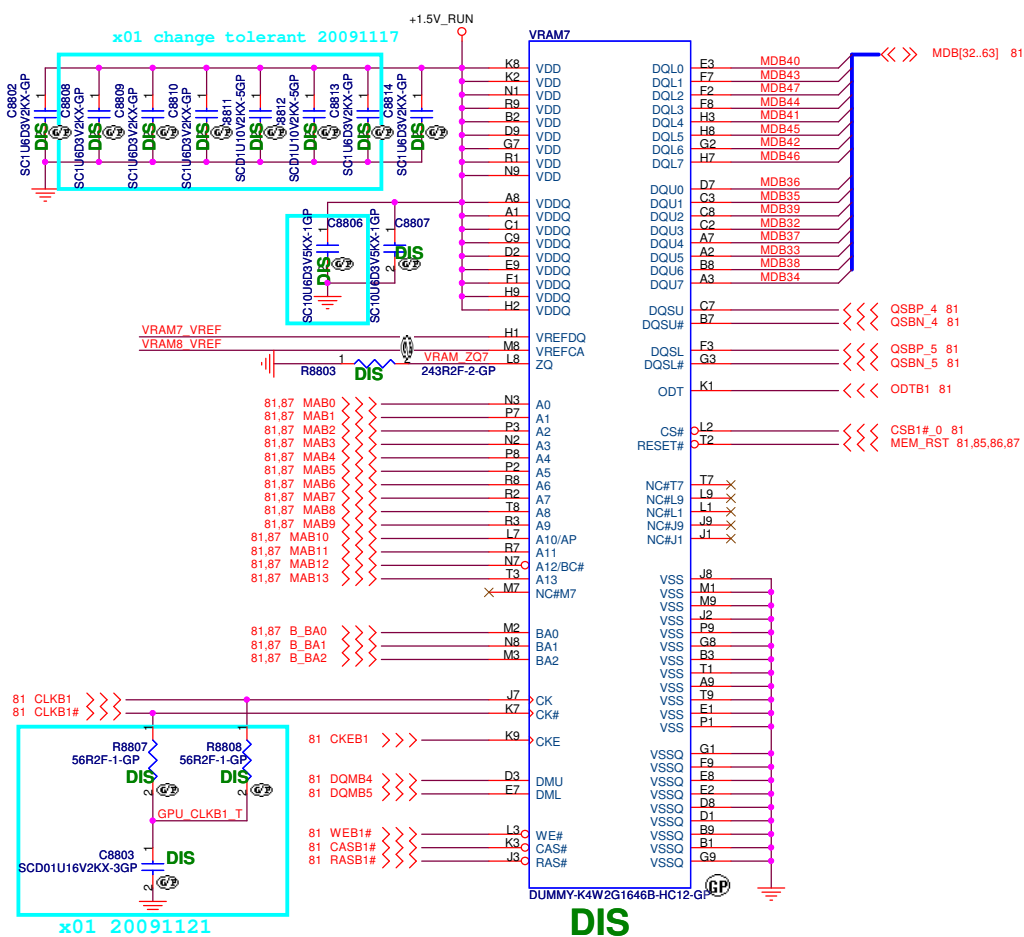












<Core Design>



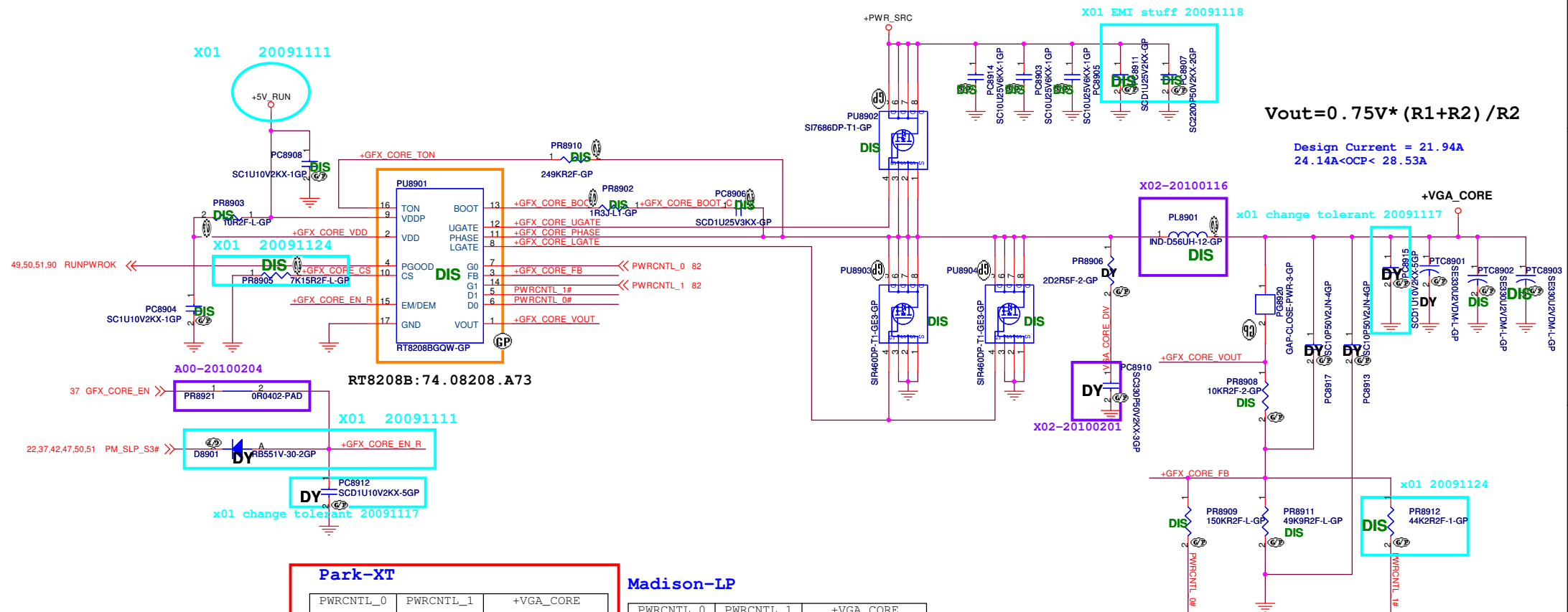
Title			GPU-VRAM7,8 (4/4)	
Size	Document Number	Rev		A00
A3	Berry			
Date: Monday, March 29, 2010	Sheet 88	of 92		



SSID = Video.PWR.Regulator

RT8208BGQW for +VGA\_CORE

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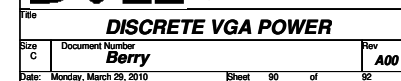
I/P cap: 10U 25V K1206 X5R/ 78.10622.52L  
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.6mohm/1.8mohm Isat=25Arms 68.R5610.10D  
O/P cap: 330U 2.5V PSLV0E337M(15) 15mOhm 2.886Arms NEC\_TOKIN/ 77.C3371.10L  
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037  
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

<Core Design>

**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title: **RT8208B +VGA CORE**  
Size A3 Document Number: **Arsenal DJ1 Discrete** Rev: **A00**  
Date: Wednesday, March 31, 2010 Sheet 89 of 92

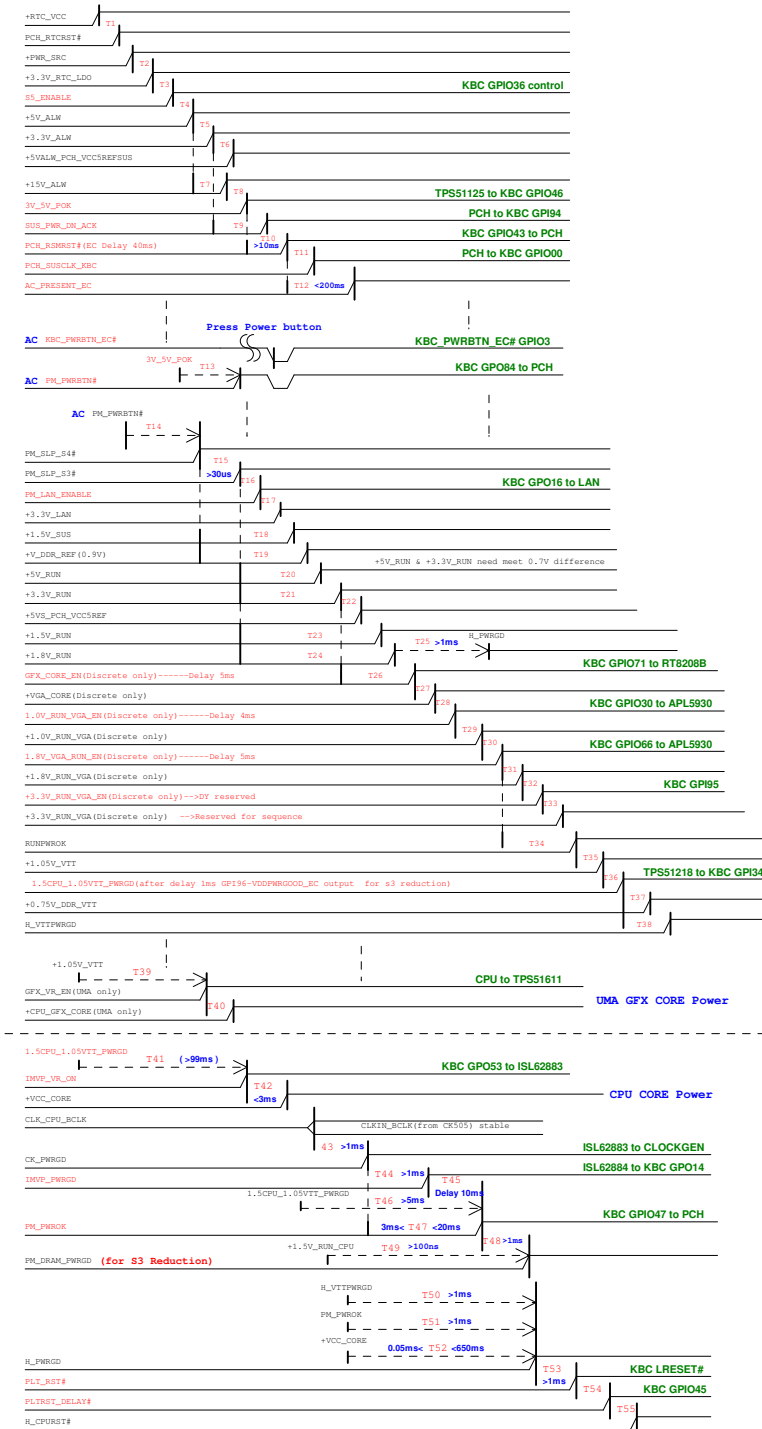
<http://adf.ly/LOM1>



# D15 Intel-Power Up Sequence

(AC mode)

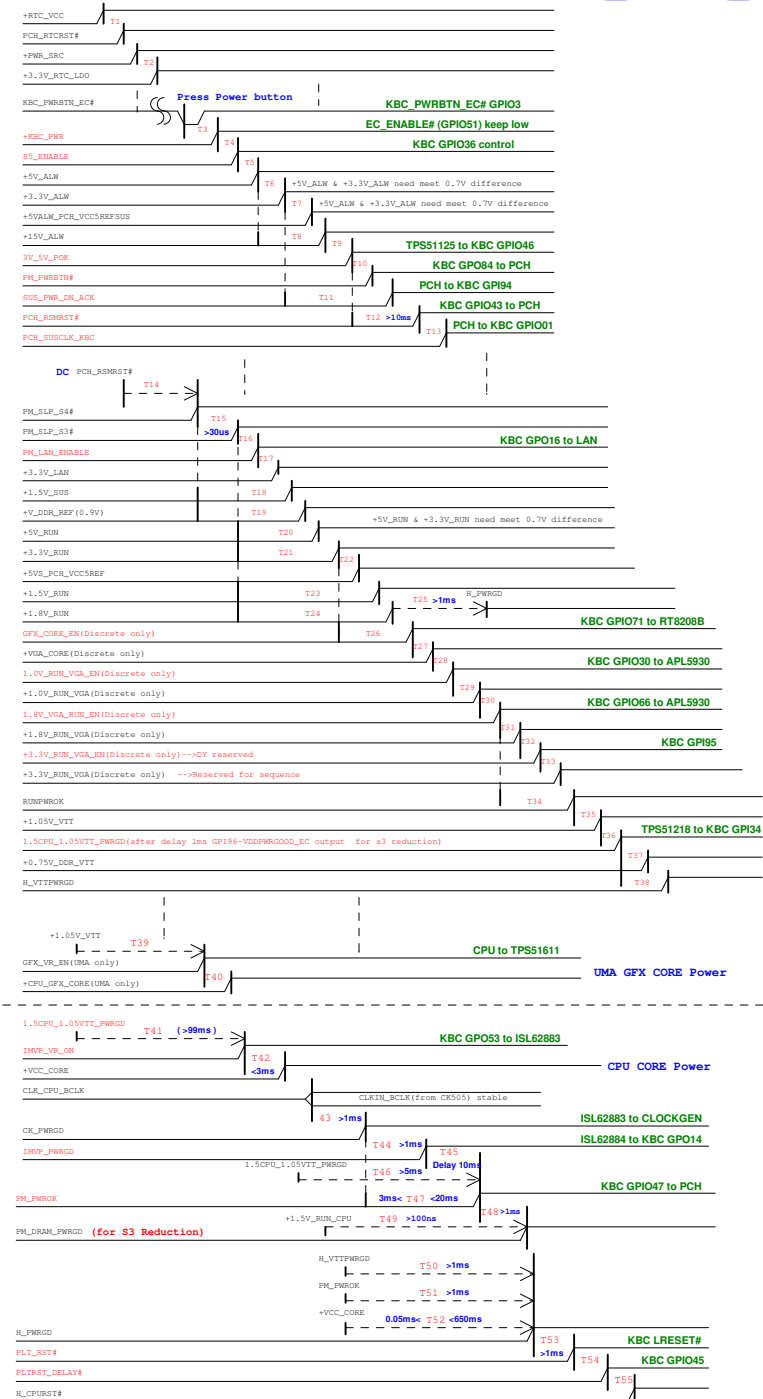
red word: KBC GPIO



(DC mode)

red word: KBC GPIO


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<http://adf.ly/LOM1>

(Blanking)

<Core Design>



**Wistron Corporation**  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Change History**

Size A3	Document Number <b>Berry</b>	Rev <b>A00</b>
Date: Wednesday, February 10, 2010	Sheet 92 of	92