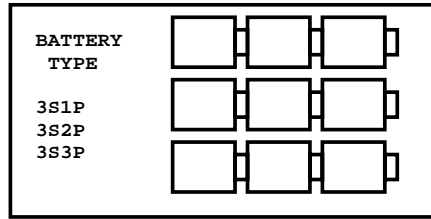
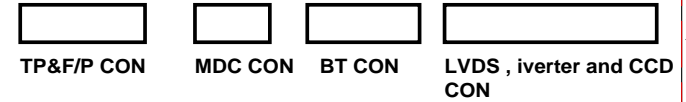


[illegible][illegible]

F6S BLOCK DIAGRAM



Internal IO CON with Cable for MB



Internal IO CON with Cable for IO Board



GDDR2 16Mx16 x4
DDR2 16M*16-2.5 1.8V
INFINEON page42

Merom 478
page4,5,6

CPU CAP page6

THERMAL SENSOR(MAX6657)/ FAN CON.
page6

RTC page25

Discharge circuit page37

CLOCK GEN. ICS9LPR363 page7

AC & BAT CON page47

LVDS & INV CON page17

CRT CON page18

HDMI CONN page19

NB8M-SE G3-64
page40,41,43,44,45

PCI-E X8

SPDIF IN from CODEC

965PM
page8,9,10,11,12,13

HOST BUS

DDR2 SDRAM 533/667MHz

DDR2 533/667 SODIMM X2
+1.8V
+0.9VS page14,15

DDR CAP/RES

DMI X2

ICH8-M
page25,26,27,28

USB2.0

PCI EXPRESS X1

USB2.0

ACZ

MDC CON page19

USB X1

NEWCARD page33

GigaLAN RTL8111B page29

MINI CARD WLAN page20

eSATA JMB360 page30

USB x1 eSATA

USB x2 page24

B/T page21

Camera page17

Touch Pad connector page38

F/P page38

RTS5158 page36

4 IN 1 CON page36

ODD page23

SATA HDD page23

TPM Conn. page21

LPC, 33MHz

EC(IT8511E) page34

ISA ROM (8Mbits TSOP) page35

INTERNAL KEYBOARD page35

Azalia ALC888S

AUDIO AMP TPA6017A2PWP

HP

MIC AMP LM358MX

MIC_IN

Daughter Board

USB x1

MINI CARD WWAN (3G)

SIM CON

RJ11,RJ45 CON

<Variant Name>

ASUS		Title : BLUE DIAGRAM	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	F6S		1.1
Date: Tuesday, August 21, 2007		Sheet	2 of 94

EC-IT8511 GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	LCD_BL_PWM	
33	PWM1/GPA1	FAN_PWM	
36	PWM2/GPA2	BAT1_CNT1#	I
37	PWM3/GPA3	BAT2_CNT1#	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	BATSEL_3S#	O
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	SCRL_LED	O
163	SMCLK0/GPB3	SMB0_CLK	O
164	SMDAT0/GPB4	SMB0_DAT	I/O
5	GA20/GPB5	O	
6	KBRST#/GPB6	RCIN#	O
165	GPB7	THRO_CPU	O
47	CLKOUT/GPC0	N/A	
169	SMCLK1/GPC1	SMB1_CLK	O
170	SMDAT1/GPC2	SMB1_DAT	I/O
171	GPC3	PWRLIMIT#	O
172	TMR10/WUI2/GPC4	ACIN_OC#	I
175	GPC5	OP_SD#	O
176	TMR11/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	EC_IDE_RST#	O
26	RI1#/WUI0/GPD0	SUSB#	I
29	RI2#/WUI1/GPD1	SUSC#	I
30	LPCRST#/WUI4/GPD2	BUF_PLT_RST#	
31	EXT_SC#	EXT_SC#	O
41	GPD4	RF_ON_SW#	O
42	GIN7/GPD5	PM_SLP_M#	O
62	TACH0/GPD6	FAN0_TACH	
63	TACH1/GPD7	COLOREN#	I
87	ADC4/GPE0	BLUETOOTH#	I
88	ADC5/GPE1	INTERNET#	I
89	ADC6/GPE2	MARATHON#	I
90	ADC7/GPE3	DISTP#	I
2	PWRSW/GPE4	PWR_SW#	I
44	WUI5/GPE5	BAT2_IN_OC#	I
24	LPCPD#/WUI6/GPE6	WLAN_SW#	I
25	CLKRUN#/WUI7/GPE7	ME_ALERT#	
110	PS2CLK0/GPF0	NC/PS2CLK0	O
111	PS2DAT0/GPF1	NC/PS2DAT0	I/O
114	PS2CLK1/GPF2	DVD/CD_ON#	I
115	PS2DAT1/GPF3	TV_ON#	I
116	PS2CLK2/GPF4	TP_CLK	O
117	PS2DAT2/GPF5	TP_DAT	I/O
118	PS2CLK3/GPF6	SLOT_ON# ??	I
119	PS2DAT3/GPF7	INSTANT_ON#	I
113	FA16/GPG0	FA16_SWAP	O
112	FA17/GPG1	FA17	O
104	FA18/GPG2	FA18	O
103	FA19/GPG3	FA19 BAT2_IN_OC#	O
3	FA20/GPG4	LID_EC#	I
4	FA21/GPG5	BAT2_IN_OC#	I
27	LPC80HL/GPG6	PMTHERM#	O
28	LPC80LL/GPG7	AC_APR_UC#	I

Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD	I
55	GPH2	CPUPWR_GD	I
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_EC#	O
75	GPH5	SUSB_EC#	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GPI0	ICH8_PWROK	O
149	GPI1	ALL_SYS_PWRGD	I
152	GPI2	BAT1_CNT2#	O
155	GPI3	CHG_EN#	O
156	GPI4	PRECHG	O
168	GPI5	EC_CLK_EN	O
174	GPI6	BAT_LEARN	O

SM_BUS ADDRESS :

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor(MAX6657)	1001100x (98)
VGA Thermal IC(G781-1)	1001101x (9A)

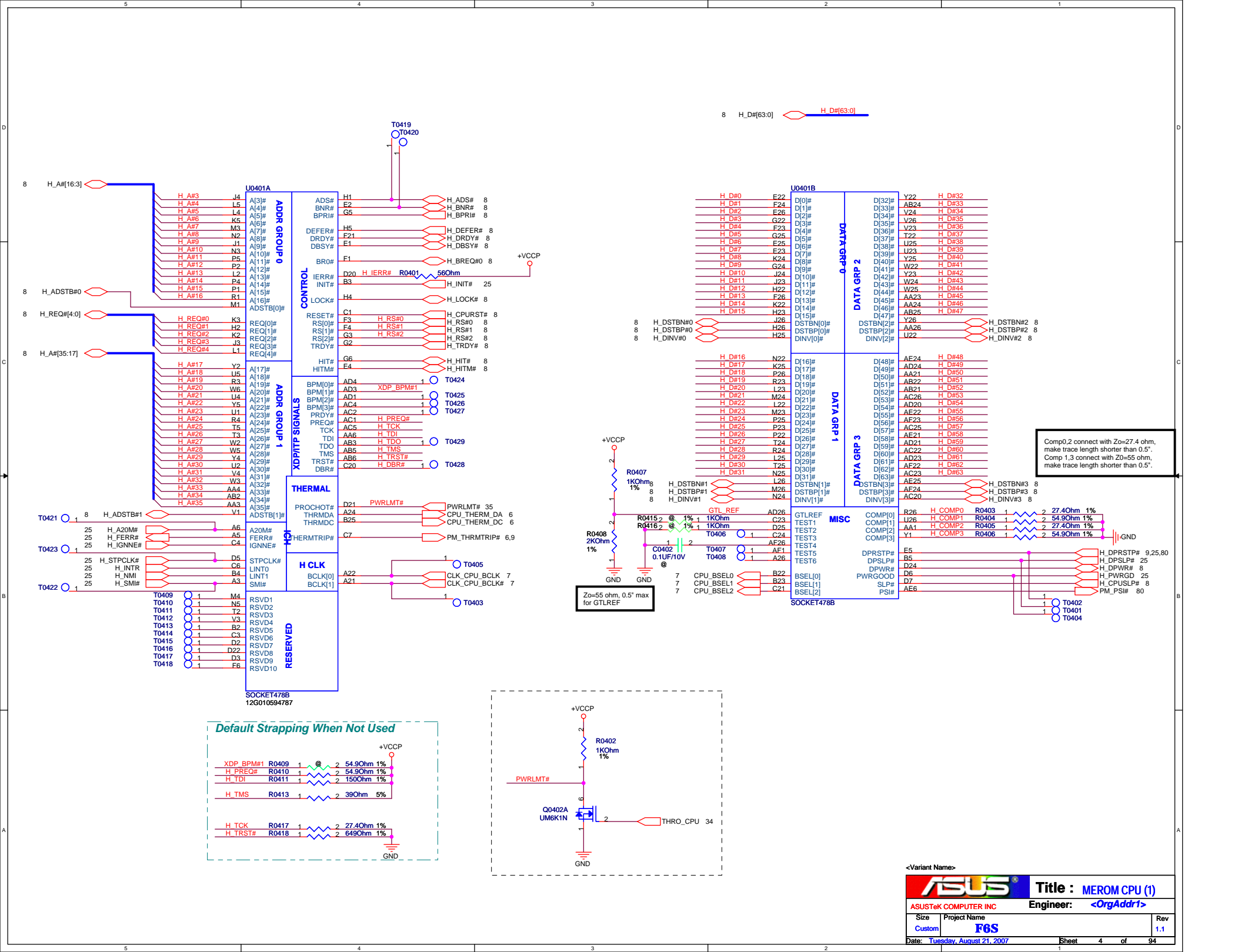
ICH8M_GPIO

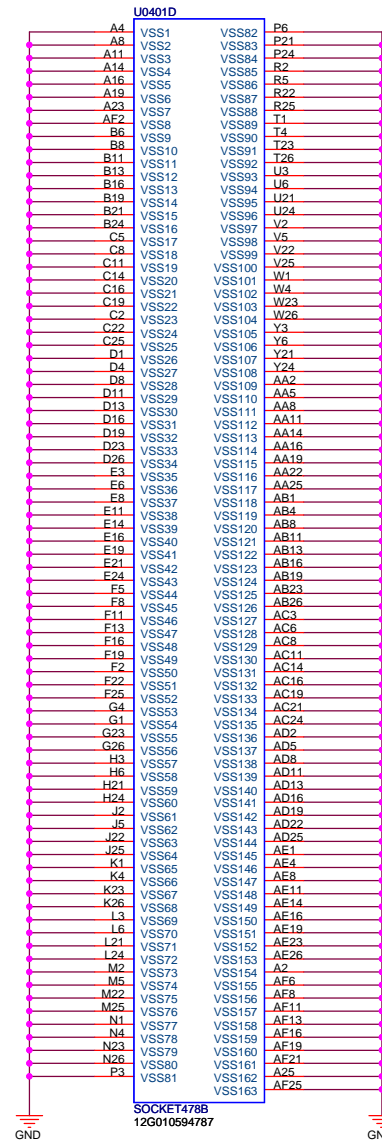
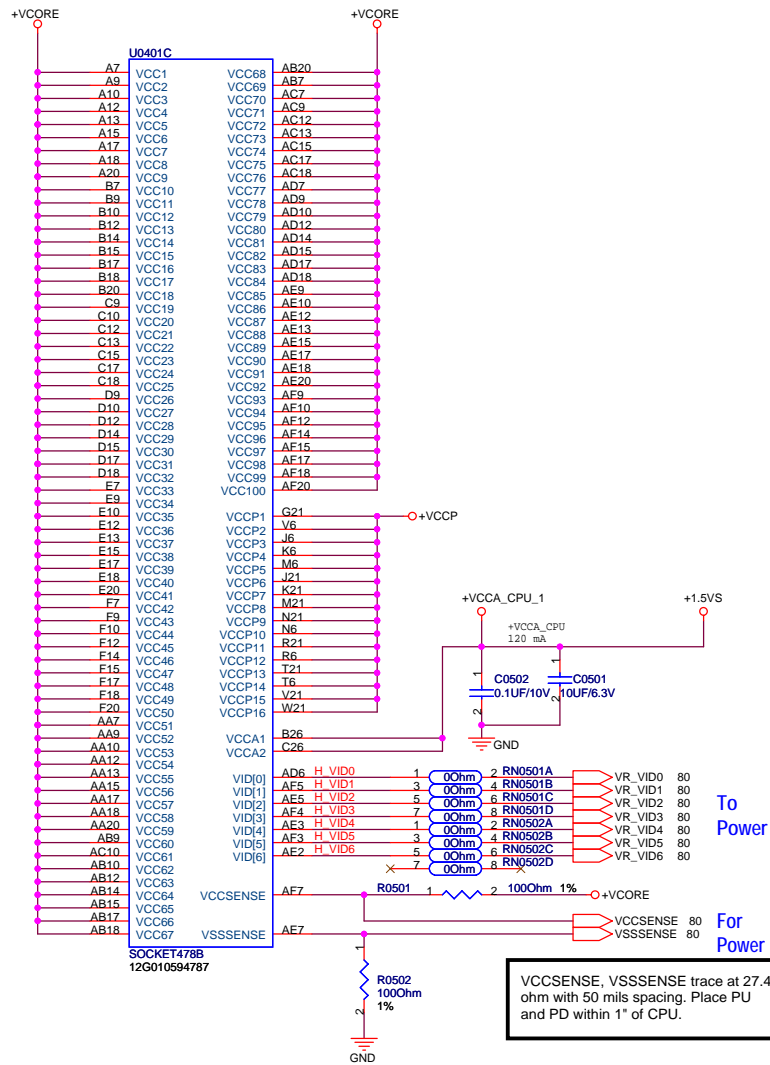
Pin.	Default	Use As	Signal Name	Power	Mux
GPIO 00	i	GPI	PM_BMBUSY#	+3VS	BM_BUSY#
GPIO 01	i	GPI	BT_DET#	+3VS	FACH1
GPIO [5:2]	i	GPI	PCI_INT[H:E]#	+3VS	PIRQ[H:E]#
GPIO 06	i	GPO	BIOS_REC_?_(TP)	+3VS	FACH2
GPIO 07	i	GPO	802_LED_EN	+3VS	FACH3
GPIO 08	i	GPI	EXTSM#	+3VSUS	N/A
GPIO 09	i	GPO	LAN_WOL_?_(TP)	+3VSUS	WOL_EN
GPIO 10	i	GPO	RST#_NEWCARD	+3VSUS	ALERT#
GPIO 11	Nat	Native	SMB_ALERT#	+3VSUS	SMBALERT#
GPIO 12	i	GPI	KBC_SC#	+3VSUS	GLAN_DOCK#
GPIO 13	Nat	GPI	N/A	+3VSUS	ENERGY_DETECT
GPIO 14	i	GPI	N/A	+3VSUS	NETDETECT
GPIO 15	Nat	Native	STP_PC#	+3VSUS	STP_PC# , No-GPIO in Mobile
GPIO 16	Nat	Native	PM DPRSLPVR	+3VS	DPRSLPVR
GPIO 17	i	GPO	WLAN_ON#	+3VS	FACH0
GPIO 18	O	GPO	N/A	+3VS	N/A
GPIO 19	i	GPO	CPU_SELECT	+3VS	SATA1GP
GPIO 20	O	GPO	BT_LED_EN	+3VS	N/A
GPIO 21	i	GPI	CPPE#_DET	+3VS	SATA0GP
GPIO 22	i	GPI	N/A	+3VS	SCLOCK
GPIO 23	Nat	Native	N/A	+3VS	LDRO1#
GPIO 24	O	GPO	MSK_PCIRST	+3VSUS	CLGPIO0(MEM_LED) , Not Cleared by CF9h RST event.
GPIO 25	Nat	Native	STP_CPU#	+3VS	STP_CPU# , No-GPIO in Mobile
GPIO 26	Nat	GPO	CPPE_EN	+3VSUS	S4_STATE#
GPIO 27	O	GPO	BT_ON#	+3VSUS	QRT_STATE0
GPIO 28	O	GPO	CB_SD#_?_(TP)	+3VSUS	QRT_STATE1
GPIO 29	Nat	Native	USB_OC#5	+3VSUS	OC5#
GPIO 30	Nat	Native	USB_OC#6	+3VSUS	OC6#
GPIO 31	Nat	Native	USB_OC#7	+3VSUS	OC7#
GPIO 32	O	Native	PM_CLKRUN#	+3VS	CLKRUN# , No-GPIO in Mobile
GPIO 33	O	GPO	N/A	+3VS	HDA_DOCK_EN#
GPIO 34	O	GPO	N/A	+3VS	HDA_DOCK_RST#
GPIO 35	O	GPO	SATACLKREQ#_?_(TP)	+3VS	SATACLKREQ#
GPIO 36	i	GPO	EMAIL_LED#_?_(TP)	+3VS	SATA2GP
GPIO 37	i	GPI	PCB_ID0	+3VS	SATA3GP
GPIO 38	i	GPI	PCB_ID1	+3VS	SLOAD

Pin	Default	Use As	Signal Name	Power	Mux
GPIO 39	i	GPI	PCB_ID2	+3VS	SDATAOUT0
GPIO [40:43]	Nat	Native	USB_OC[4:1]#	+3VSUS	OC[4:1]#
GPIO [47:44]	n/a	N/A	N/A	N/A	No implement
GPIO 48	i	Native		+3VS	SDATAOUT1
GPIO 49	Nat	Native	H_PWRGD	+VCORE	CPUPWRGD
GPIO 50	Nat	Native	PCI_REQ1#	+5VS	REQ1#
GPIO 51	Nat	Native	PCI_GNT1#	+3VS	GNT1#
GPIO 52	Nat	Native	PCI_REQ2#	+5VS	REQ2#
GPIO 53	Nat	Native	PCI_GNT2#	+3VS	GNT2#
GPIO 54	Nat	Native	PCI_REQ3#	+5VS	REQ3#
GPIO 55	Nat	Native	PCI_GNT3#	+3VS	GNT3#


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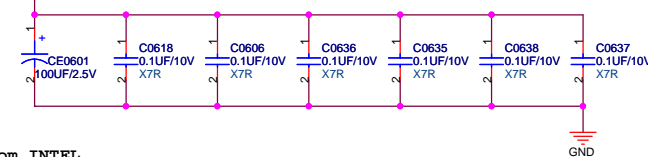
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ASUSTeK COMPUTER INC		Engineer: <OrgAddr1>	
Size	Project Name		
Custom	F6S		
Date: Tuesday, August 21, 2007	Sheet	3	of 94
	Rev	1.1	



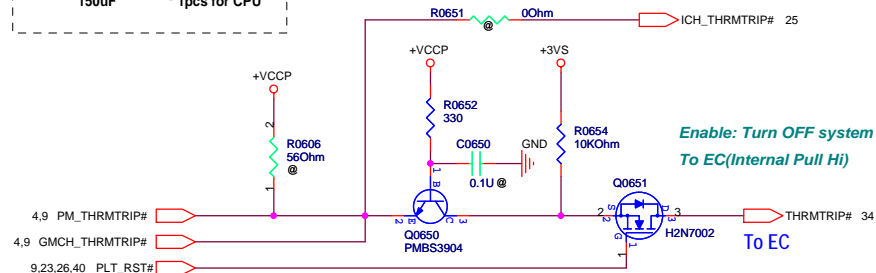
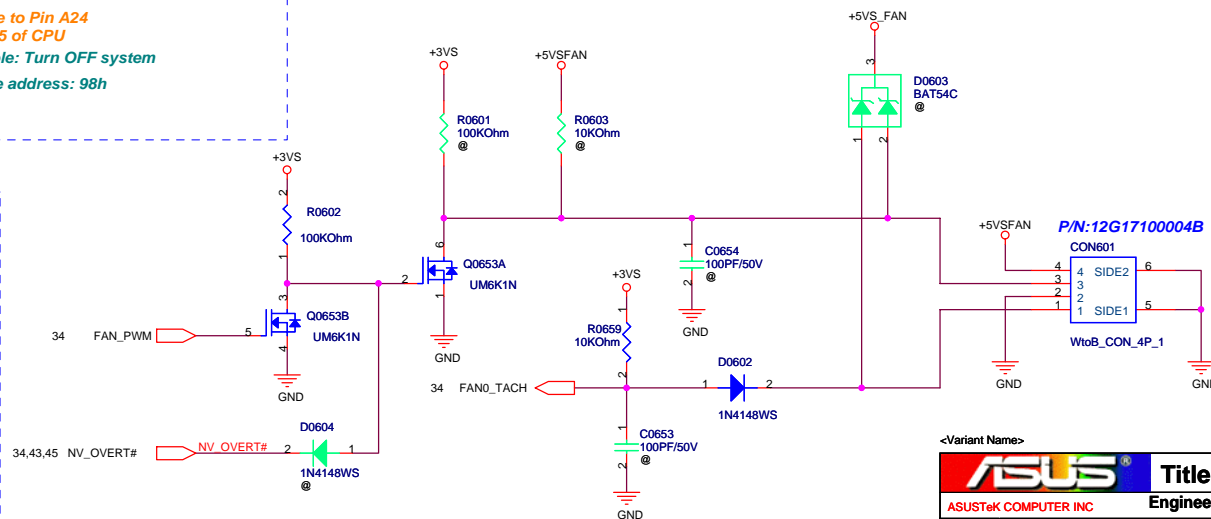


<Variant Name>

+VCCP		+VCCP	4,5,7,8,9,11,12,28,37,85
+VCORE		+VCORE	5,37,80
+3VS		+3VS	7,9,12,13,14,15,17,18,19,20,21,22,23,25,27,28,29,30,33,34,37,39,40,43,44,45,80,91,92
+5VA		+5VA	81



VCORE	22uF/10V	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs for CPU
	150uF	* 1pcs for CPU

[illegible]

H/W Thermal Protect

+5VA (94-98°C protect)

R0670 22.1K 1%

RT0671 100K

GND

C0670 0.1U

U0670 @

NC VCC
SUB GND VOUT

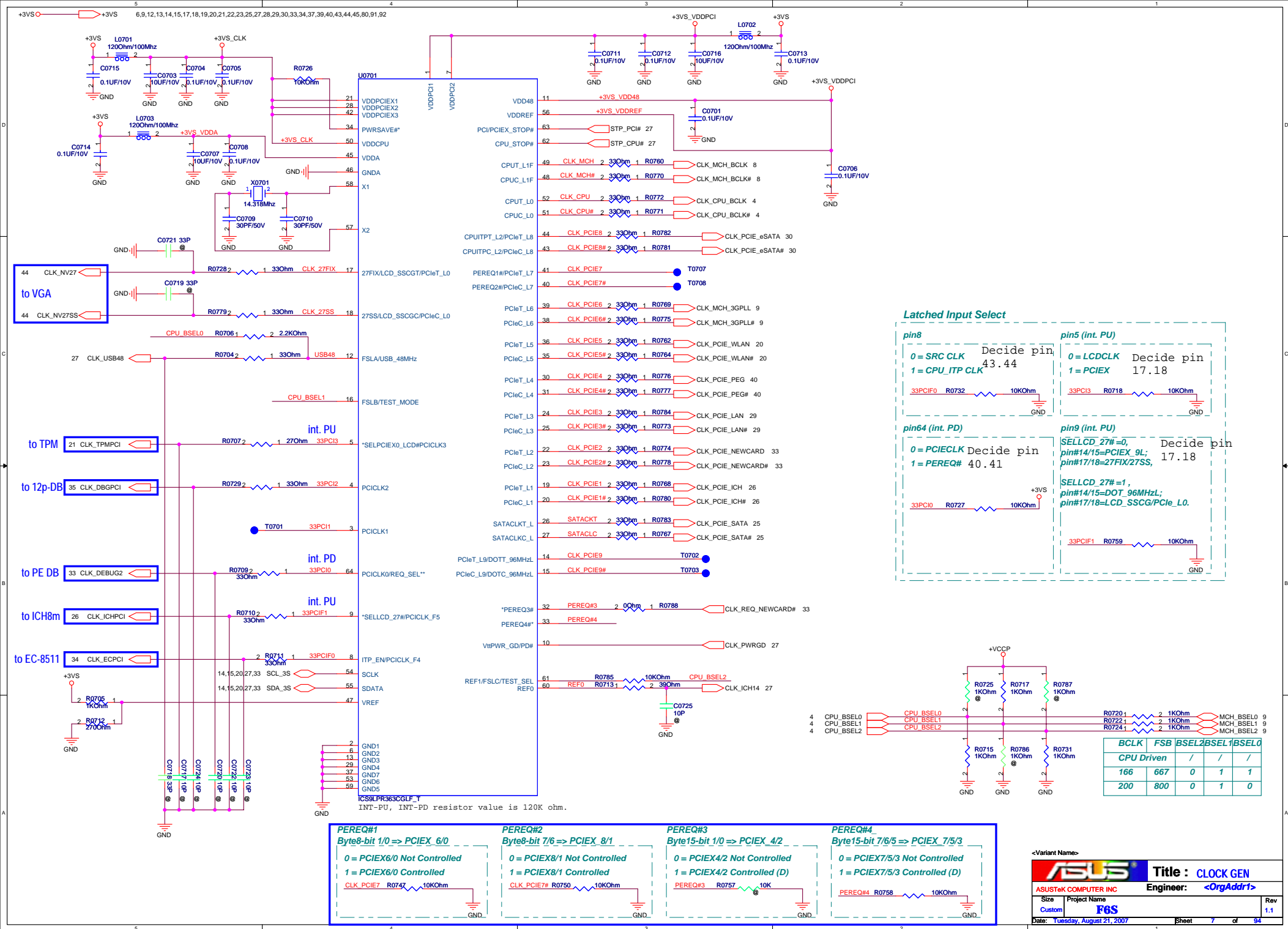
PST9013NR

R0662 4.7KOhm

FORCE_OFF# 34,81,92

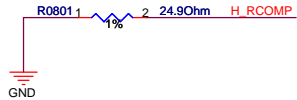
Enable: Turn OFF system
OPEN Collector

		Title : CPU CAP, Thermal,FAN_CTRL	
ASUSTek COMPUTER INC.		Engineer:	
Size Custom	Project Name F6S		Rev 1.1
Date: Tuesday, August 21, 2007		Sheet 6 of 94	



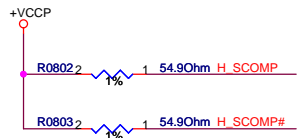
RCOMP

For Calibrating the FSB I/O Buffer



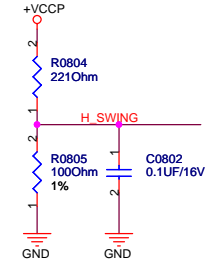
SCOMP

For Slew Rate Compensation on the FSB



Voltage Swing

For Providing a Reference Voltage to The FSB RCOMP circuits



4 H_D#[63:0] H_D#[63:0]

4 H_A#[35:3] H_A#[35:3]

U0801A

H_D#0	E2	H_D#_0
H_D#1	G2	H_D#_1
H_D#2	G7	H_D#_2
H_D#3	M6	H_D#_3
H_D#4	H7	H_D#_4
H_D#5	H3	H_D#_5
H_D#6	G4	H_D#_6
H_D#7	F3	H_D#_7
H_D#8	N8	H_D#_8
H_D#9	H2	H_D#_9
H_D#10	M10	H_D#_10
H_D#11	N12	H_D#_11
H_D#12	N9	H_D#_12
H_D#13	H5	H_D#_13
H_D#14	P13	H_D#_14
H_D#15	K9	H_D#_15
H_D#16	M2	H_D#_16
H_D#17	W10	H_D#_17
H_D#18	Y4	H_D#_18
H_D#19	V4	H_D#_19
H_D#20	M3	H_D#_20
H_D#21	J1	H_D#_21
H_D#22	N5	H_D#_22
H_D#23	N3	H_D#_23
H_D#24	W6	H_D#_24
H_D#25	W9	H_D#_25
H_D#26	N2	H_D#_26
H_D#27	Y7	H_D#_27
H_D#28	Y9	H_D#_28
H_D#29	P4	H_D#_29
H_D#30	W3	H_D#_30
H_D#31	N1	H_D#_31
H_D#32	AD12	H_D#_32
H_D#33	AE3	H_D#_33
H_D#34	AD9	H_D#_34
H_D#35	AC9	H_D#_35
H_D#36	AC7	H_D#_36
H_D#37	AC14	H_D#_37
H_D#38	AD11	H_D#_38
H_D#39	AC11	H_D#_39
H_D#40	AB2	H_D#_40
H_D#41	AD7	H_D#_41
H_D#42	AB1	H_D#_42
H_D#43	Y3	H_D#_43
H_D#44	AC6	H_D#_44
H_D#45	AC5	H_D#_45
H_D#46	AC3	H_D#_46
H_D#47	AJ9	H_D#_47
H_D#48	AH8	H_D#_48
H_D#49	AJ14	H_D#_49
H_D#50	AE9	H_D#_50
H_D#51	AE11	H_D#_51
H_D#52	AH12	H_D#_52
H_D#53	AJ5	H_D#_53
H_D#54	AH5	H_D#_54
H_D#55	AJ6	H_D#_55
H_D#56	AE7	H_D#_56
H_D#57	AJ7	H_D#_57
H_D#58	AJ2	H_D#_58
H_D#59	AE5	H_D#_59
H_D#60	AJ3	H_D#_60
H_D#61	AH2	H_D#_61
H_D#62	AH13	H_D#_62
H_D#63	AH13	H_D#_63

HOST

H_A#_3	J13	H_A#3
H_A#_4	B11	H_A#4
H_A#_5	C11	H_A#5
H_A#_6	M11	H_A#6
H_A#_7	C15	H_A#7
H_A#_8	F16	H_A#8
H_A#_9	L13	H_A#9
H_A#_10	G17	H_A#10
H_A#_11	C14	H_A#11
H_A#_12	K16	H_A#12
H_A#_13	B13	H_A#13
H_A#_14	L16	H_A#14
H_A#_15	J17	H_A#15
H_A#_16	B14	H_A#16
H_A#_17	K19	H_A#17
H_A#_18	P15	H_A#18
H_A#_19	R17	H_A#19
H_A#_20	B16	H_A#20
H_A#_21	H20	H_A#21
H_A#_22	L19	H_A#22
H_A#_23	D17	H_A#23
H_A#_24	M17	H_A#24
H_A#_25	N16	H_A#25
H_A#_26	J19	H_A#26
H_A#_27	B18	H_A#27
H_A#_28	E19	H_A#28
H_A#_29	B17	H_A#29
H_A#_30	B15	H_A#30
H_A#_31	E17	H_A#31
H_A#_32	C18	H_A#32
H_A#_33	A19	H_A#33
H_A#_34	B19	H_A#34
H_A#_35	N19	H_A#35

H_ADS#	G12	H_ADS#	H_ADS# 4
H_ADSTB#_0	H17	H_ADSTB#0	H_ADSTB#0 4
H_ADSTB#_1	G20	H_ADSTB#1	H_ADSTB#1 4
H_BNR#	C8	H_BNR#	H_BNR# 4
H_BPRI#	E8	H_BPRI#	H_BPRI# 4
H_BREQ#	F12	H_BREQ#0	H_BREQ#0 4
H_DEFER#	D6	H_DEFER#	H_DEFER# 4
H_DBSY#	C10	H_DBSY#	H_DBSY# 4
H_DBSY#	AM5	CLK_MCH_BCLK_7	CLK_MCH_BCLK_7 7
H_DPWR#	AM7	H_DPWR#	H_DPWR# 4
H_DRDY#	H8	H_DRDY#	H_DRDY# 4
H_HIT#	K7	H_HIT#	H_HIT# 4
H_HITM#	E4	H_HITM#	H_HITM# 4
H_LOCK#	C6	H_LOCK#	H_LOCK# 4
H_TRDY#	G10	H_TRDY#	H_TRDY# 4
H_TRDY#	B7	H_TRDY#	H_TRDY# 4

H_DINV#_0	K5	H_DINV#0 4
H_DINV#_1	L2	H_DINV#1 4
H_DINV#_2	AD13	H_DINV#2 4
H_DINV#_3	AE13	H_DINV#3 4

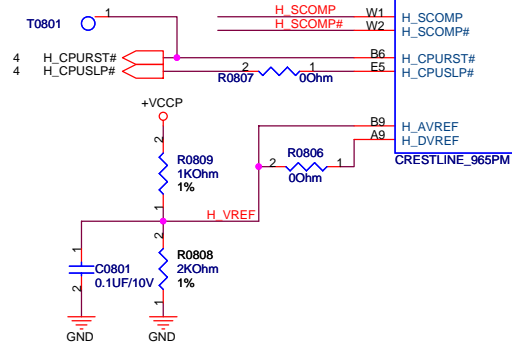
H_DSTBN#_0	M7	H_DSTBN#0 4
H_DSTBN#_1	K3	H_DSTBN#1 4
H_DSTBN#_2	AD2	H_DSTBN#2 4
H_DSTBN#_3	AH11	H_DSTBN#3 4

H_DSTBP#_0	L7	H_DSTBP#0 4
H_DSTBP#_1	K2	H_DSTBP#1 4
H_DSTBP#_2	AC2	H_DSTBP#2 4
H_DSTBP#_3	AJ10	H_DSTBP#3 4

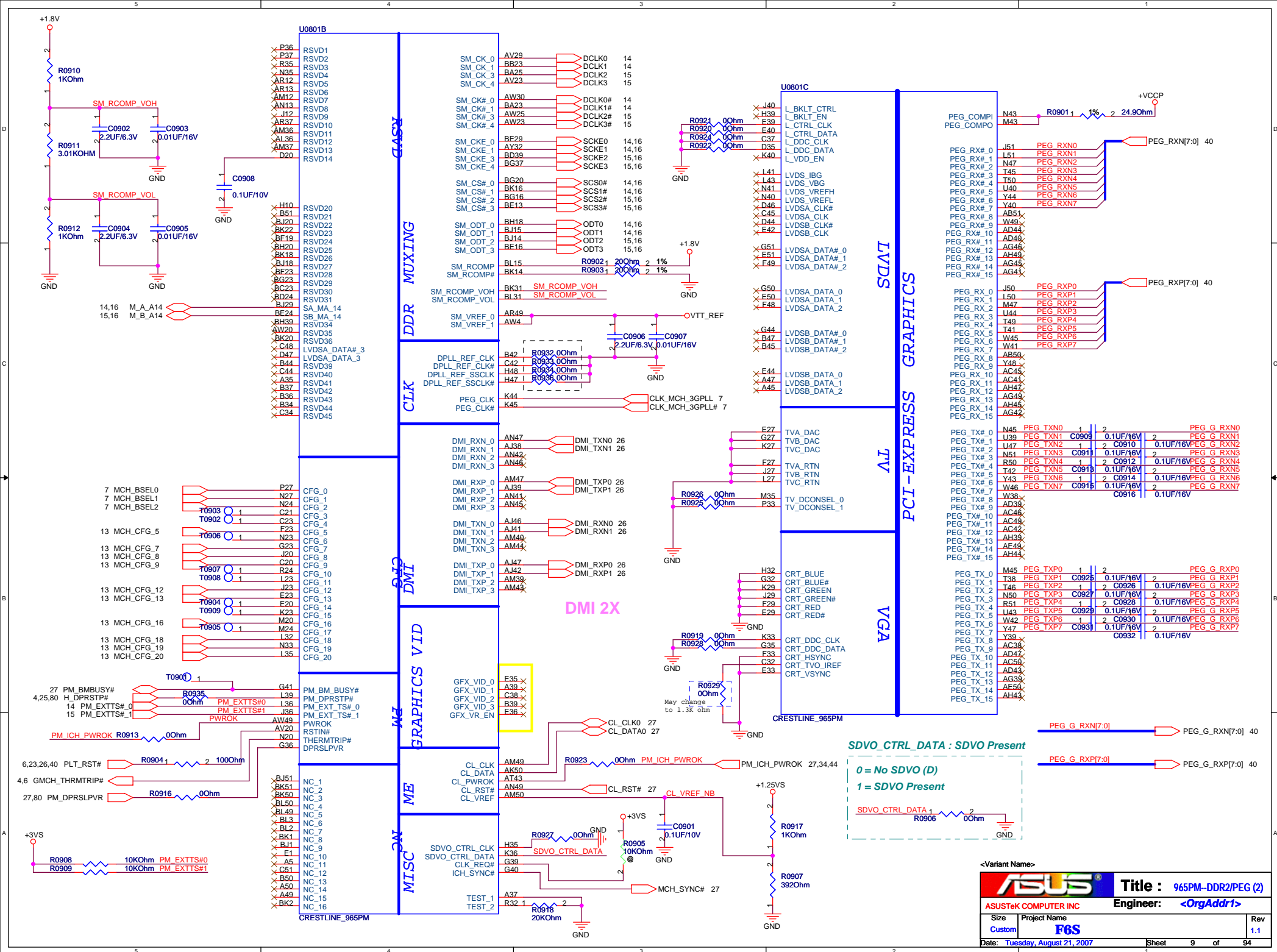
H_REQ#_0	M14	H_REQ#0
H_REQ#_1	E13	H_REQ#1
H_REQ#_2	A11	H_REQ#2
H_REQ#_3	H13	H_REQ#3
H_REQ#_4	B12	H_REQ#4

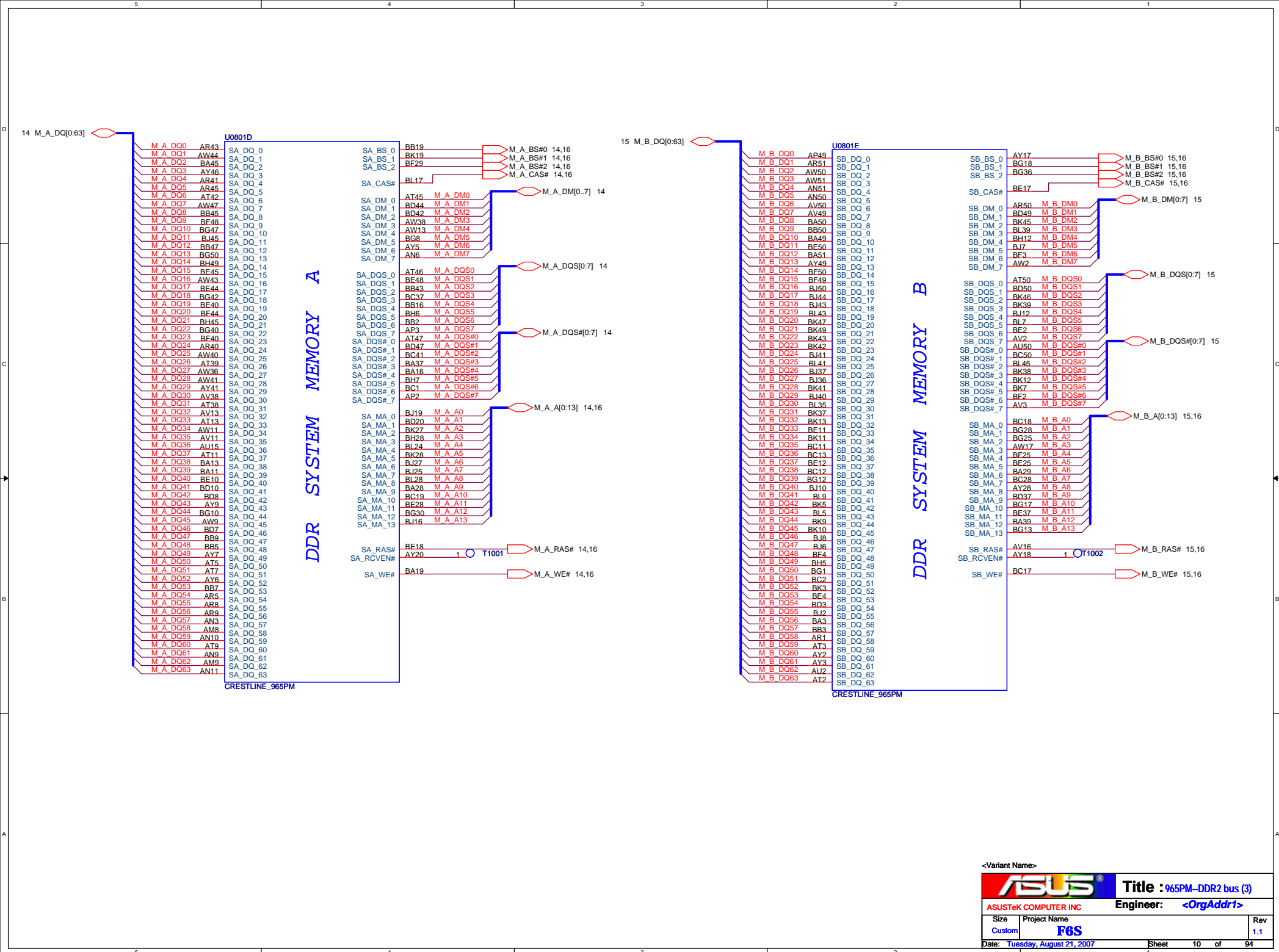
H_RS#_0	E12	H_RS#0 4
H_RS#_1	D7	H_RS#1 4
H_RS#_2	D8	H_RS#2 4

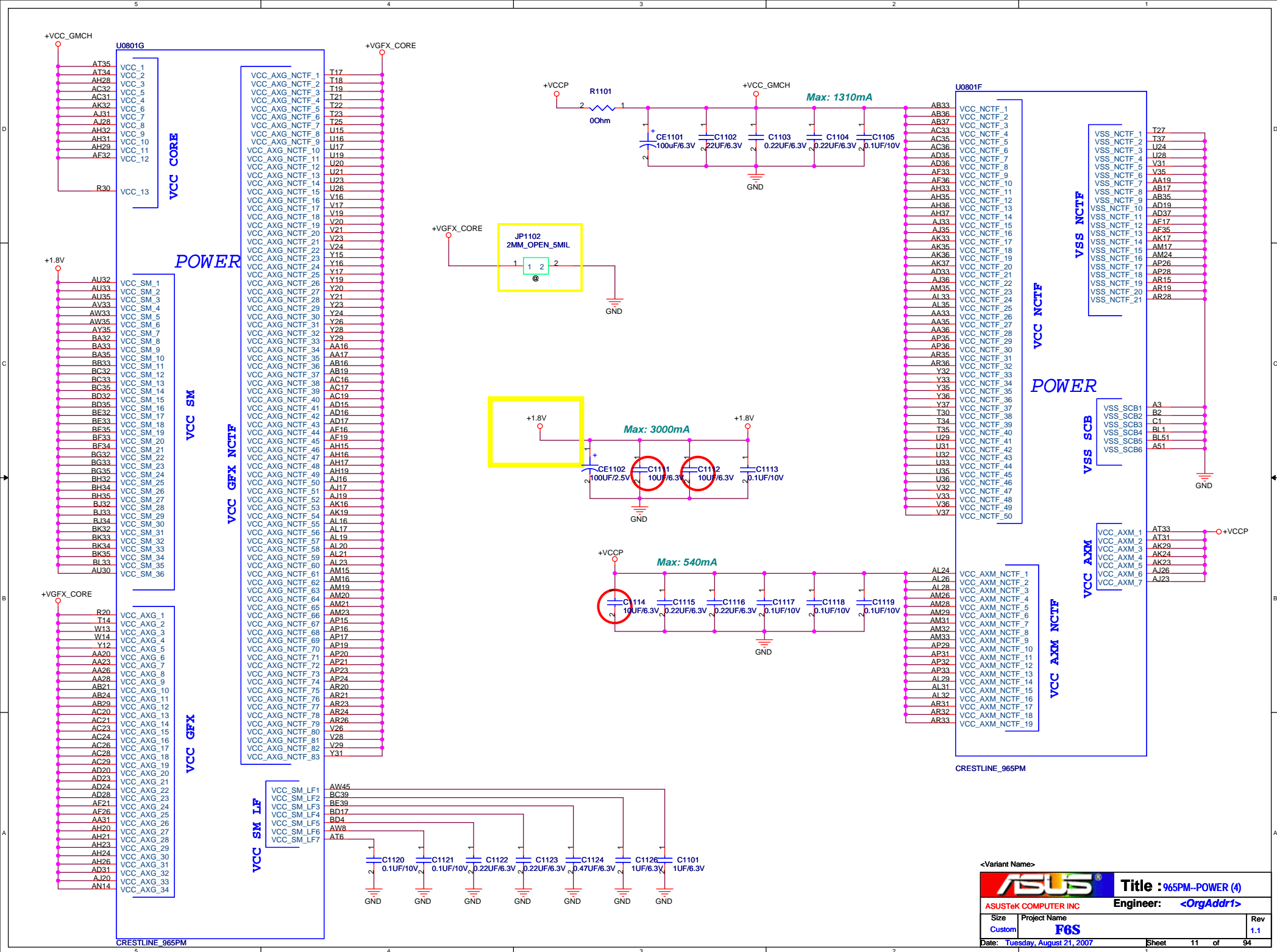
4 H_REQ#[4:0] H_REQ#[4:0]



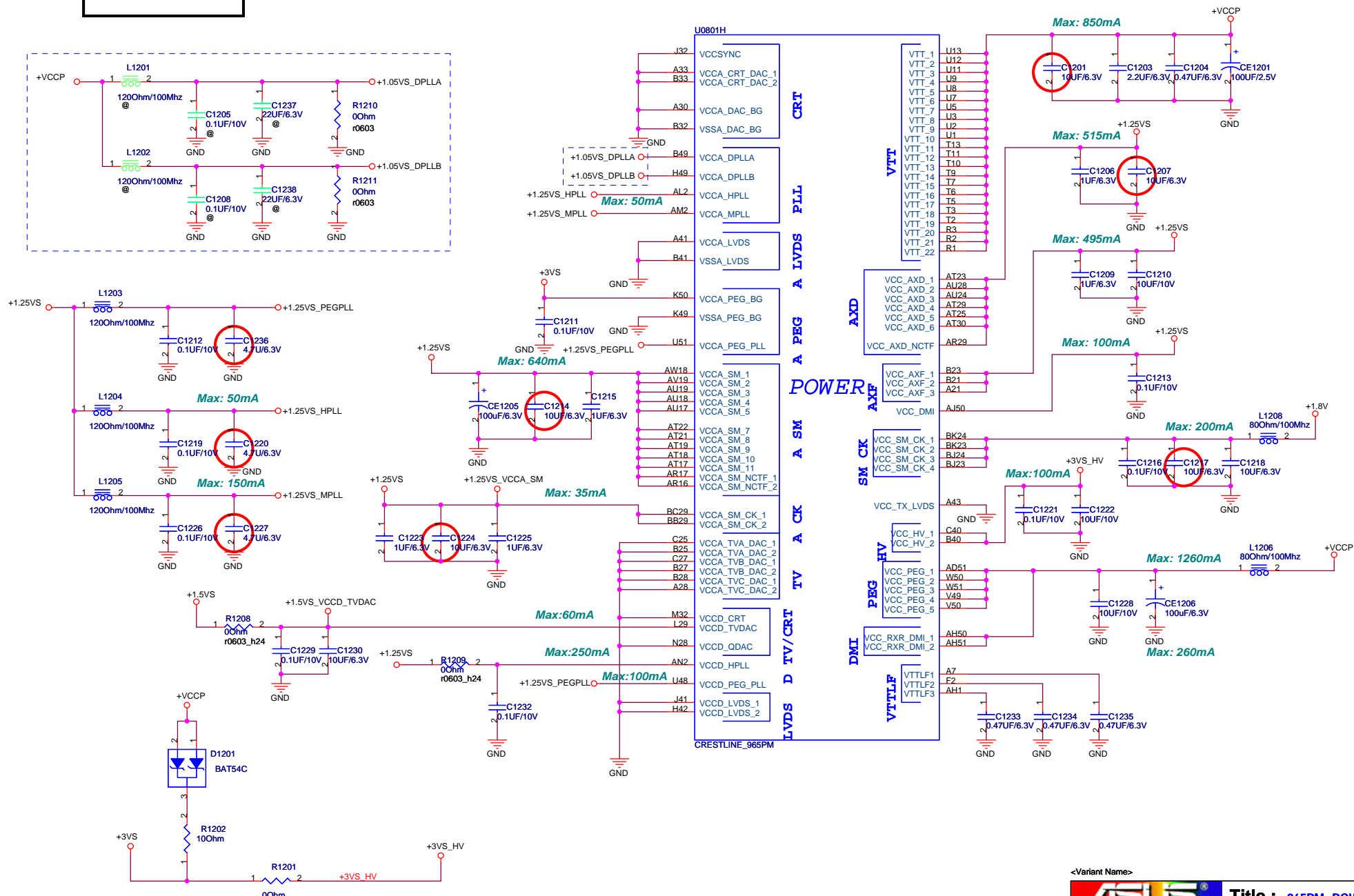
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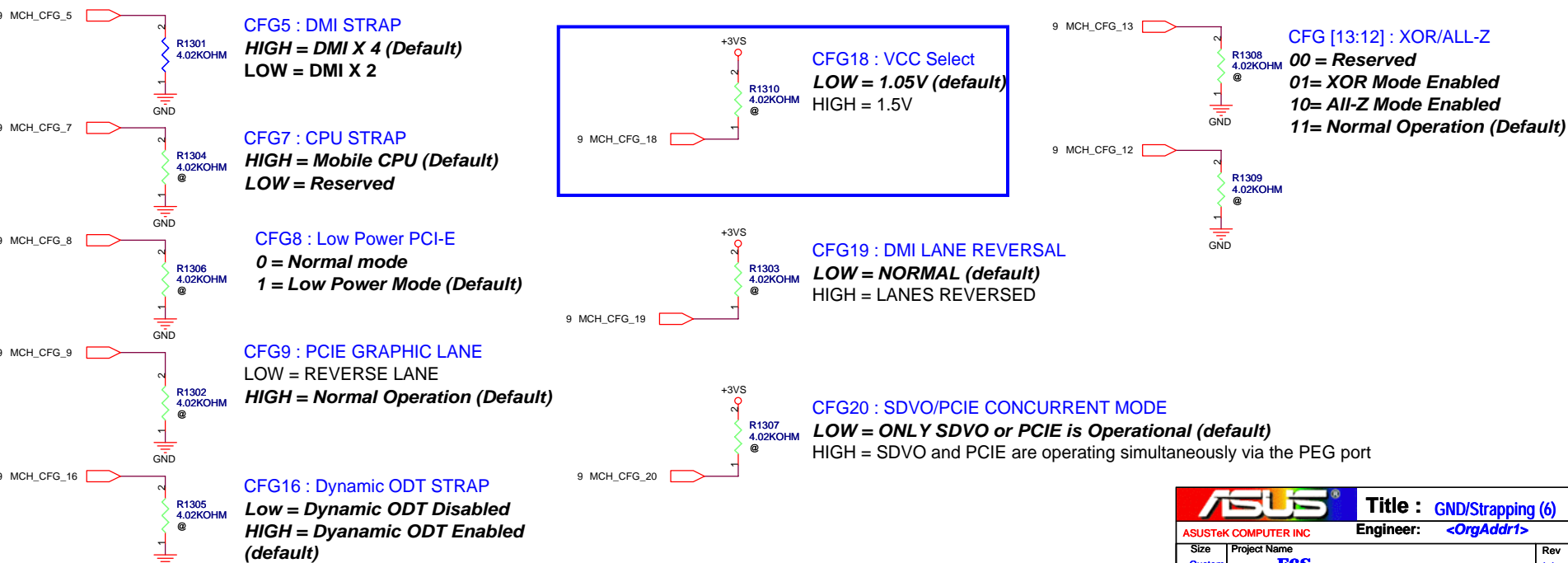


NOTE: 0.1uF caps in 1.5VS_XPLL need to be located as edge caps within 200 mils.

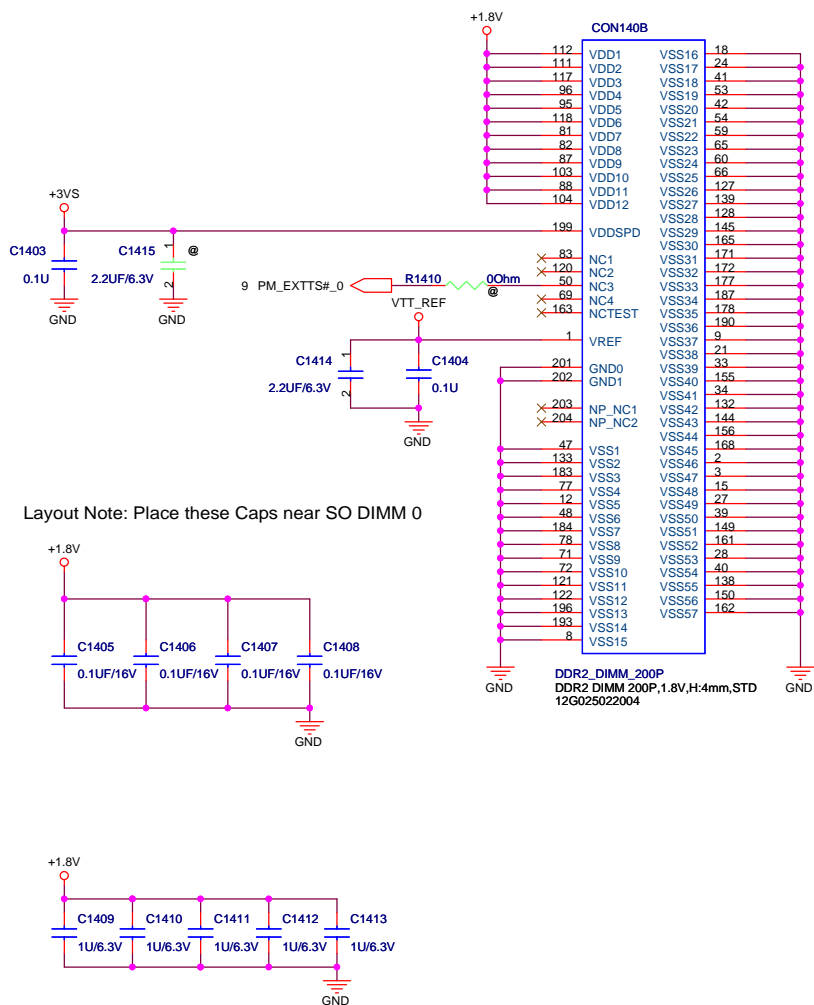
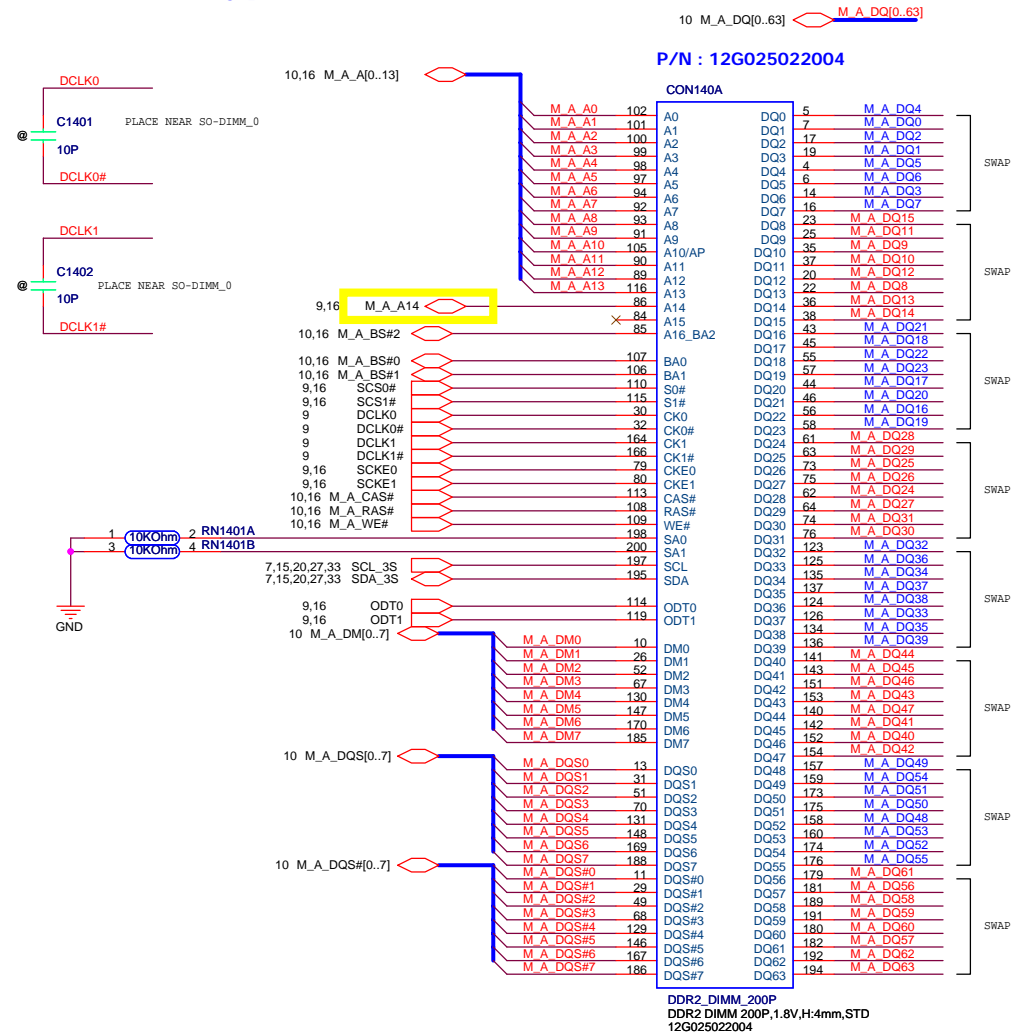


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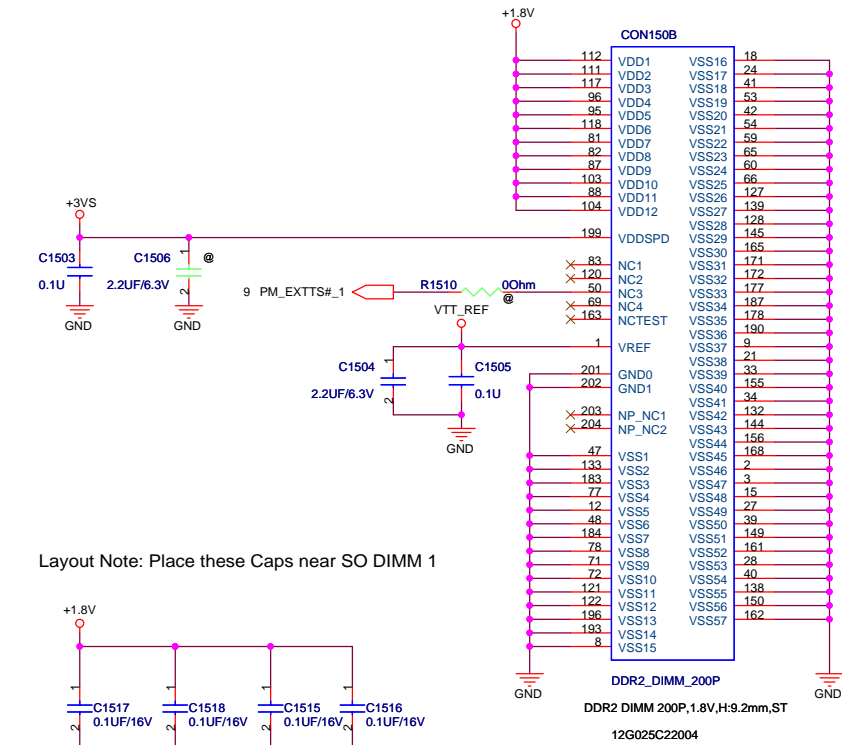
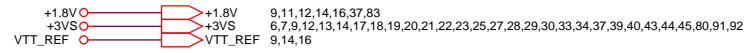
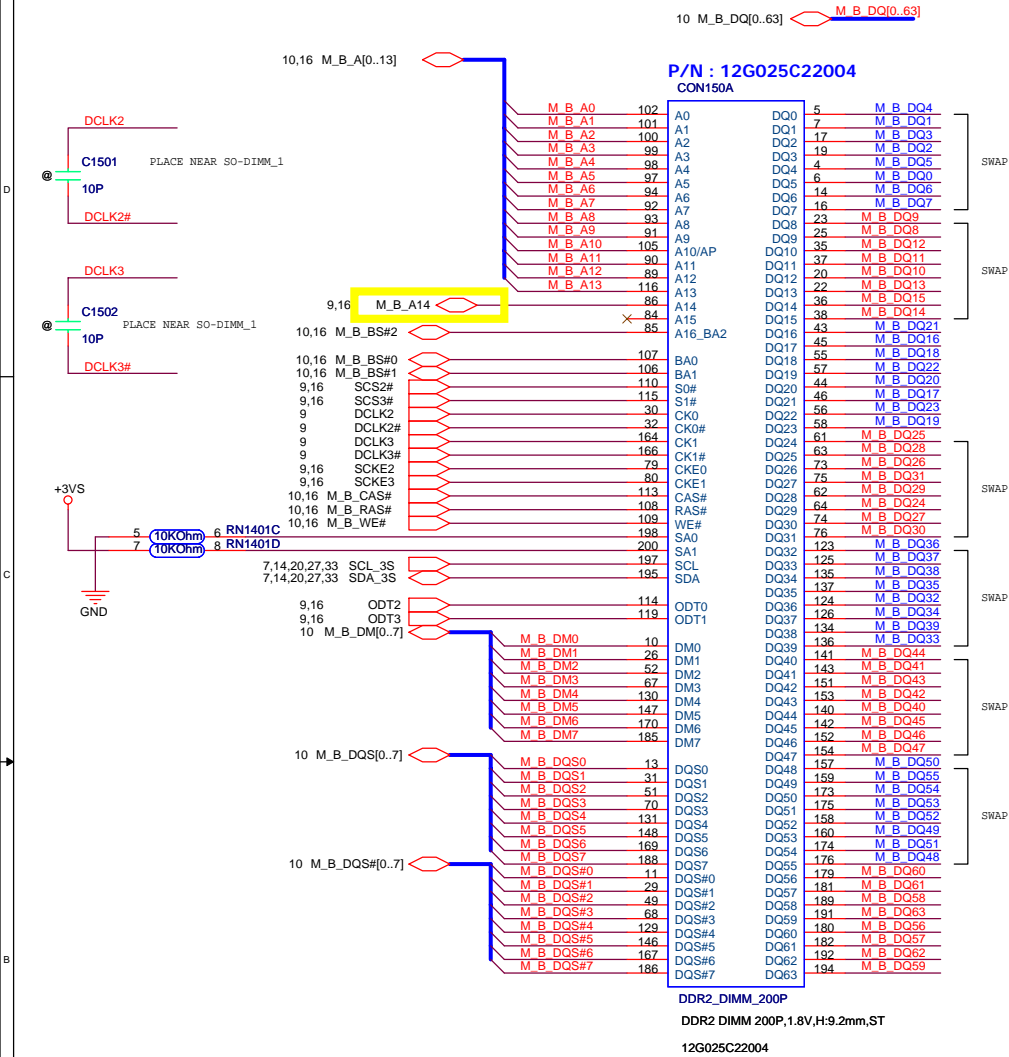




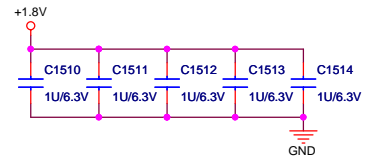
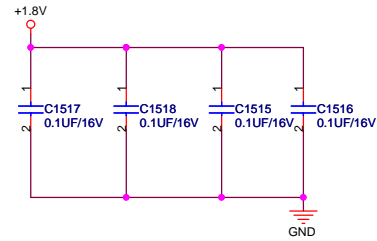
Standard Type



Standard Type

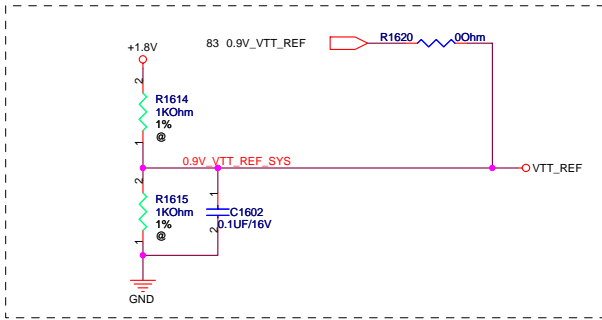


Layout Note: Place these Caps near SO DIMM 1

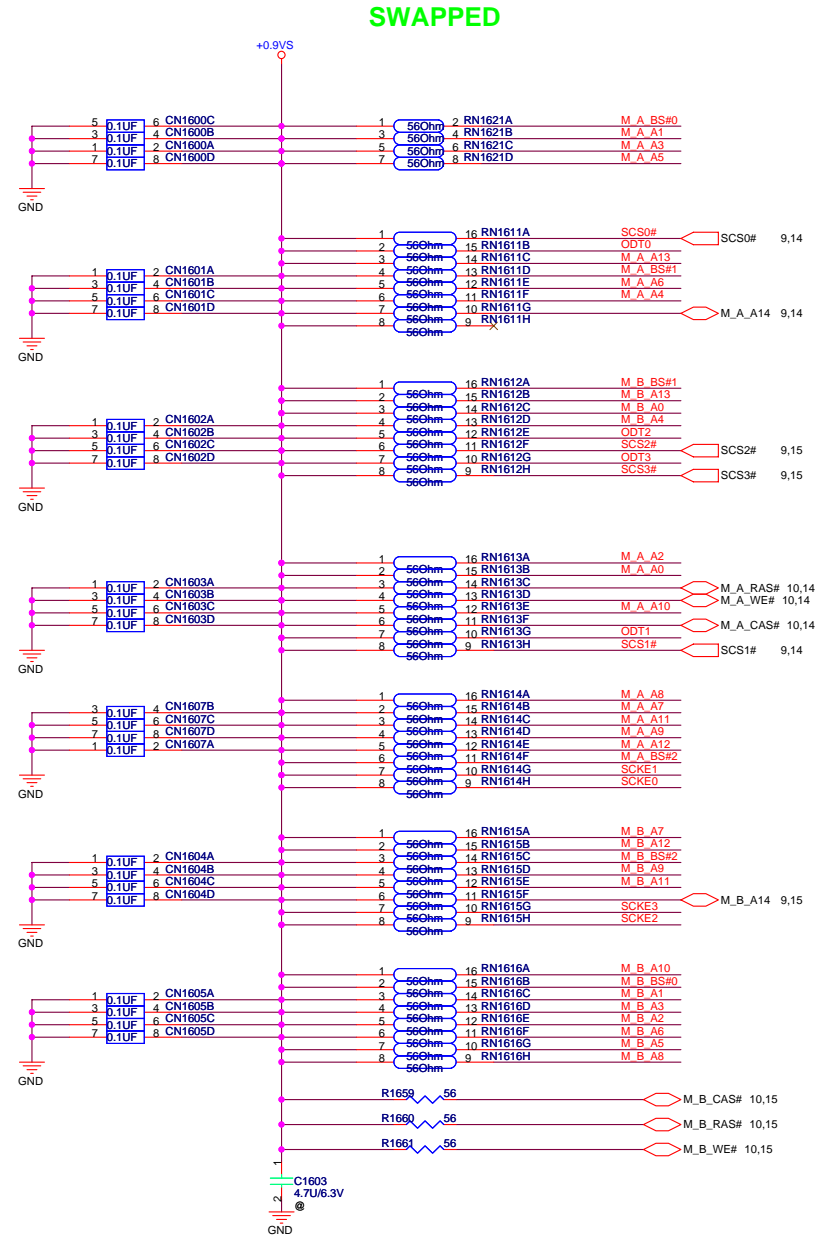


<Variant Name>



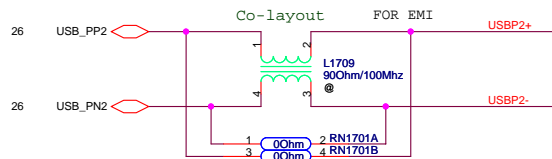


M_A_A[0..13] 10,14
M_A_BS#[0..2] 10,14
M_B_A[0..13] 10,15
M_B_BS#[0..2] 10,15
SCKE[0..3] 9,14,15
ODT[0..3] 9,14,15



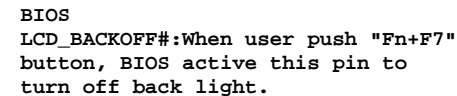
Layout note: Place array cap close to each pullup resistors terminated to +0.9VS

LCD Power



Inverter/CCD conn.

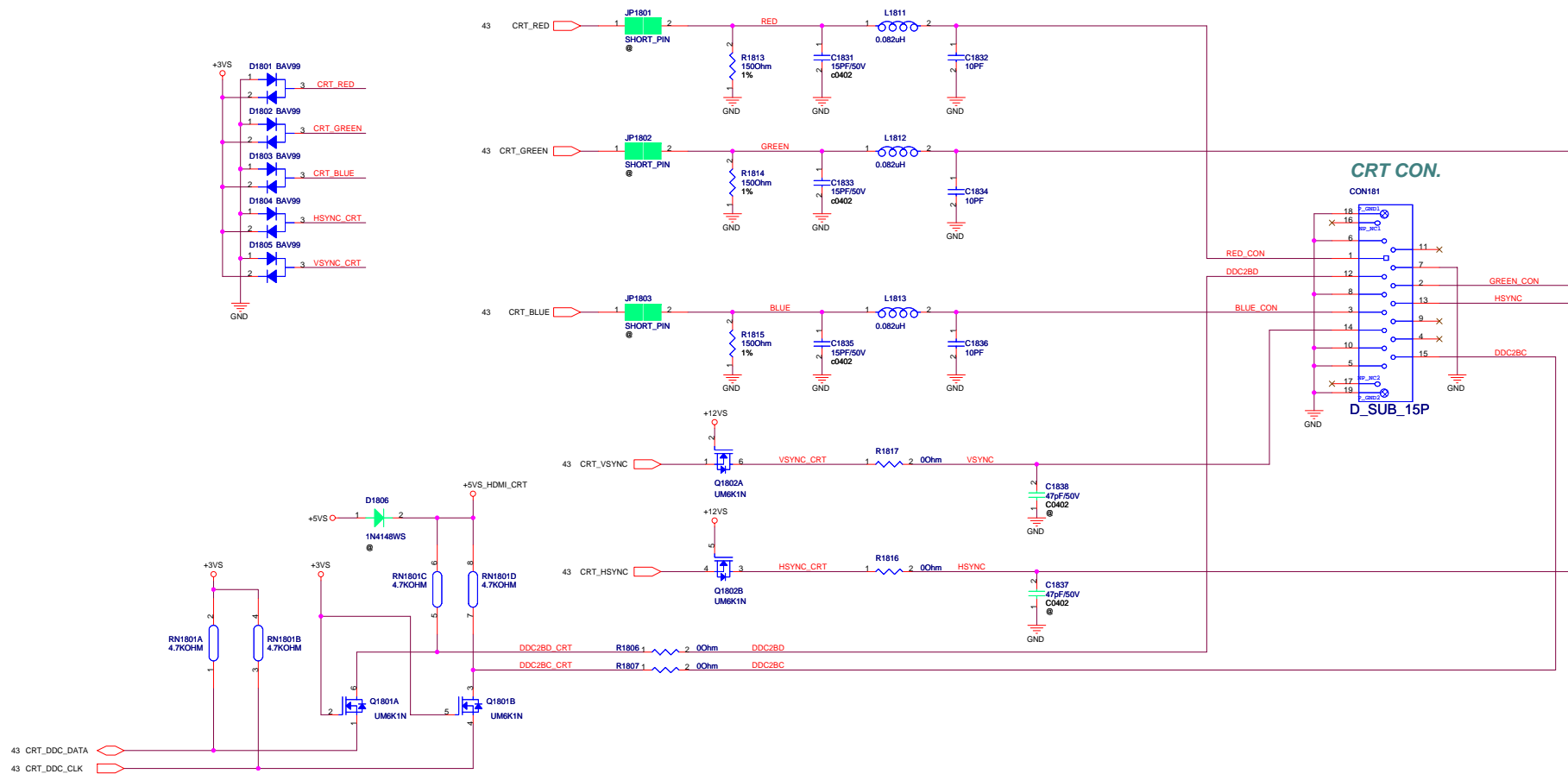
Cable Requirement:
Impedance: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"



From EC brightness control

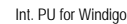
To EC Lid Switch

*Use New inverter
(For F6)*

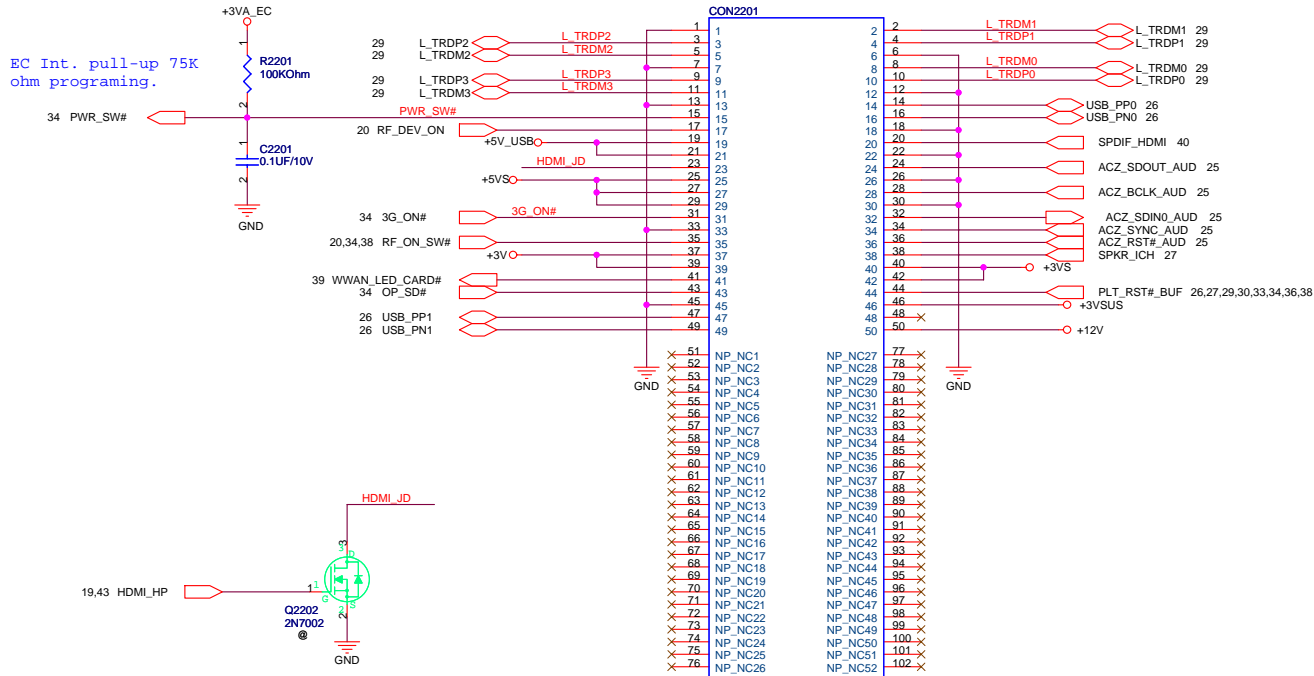


Max= 1100 mA

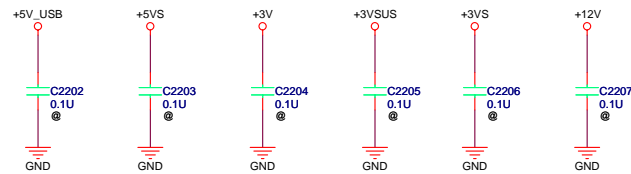
Max= 375 mA



Intel SPEC(18780):Internal
Pull UP 110Kohm



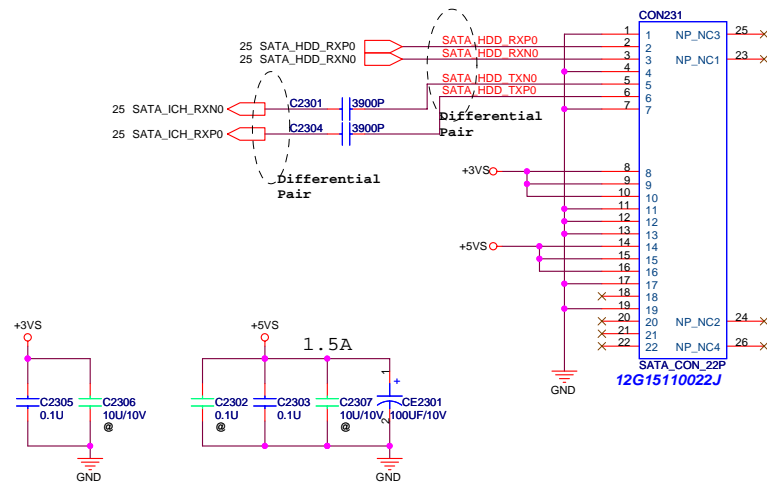
HERDER_2X25P



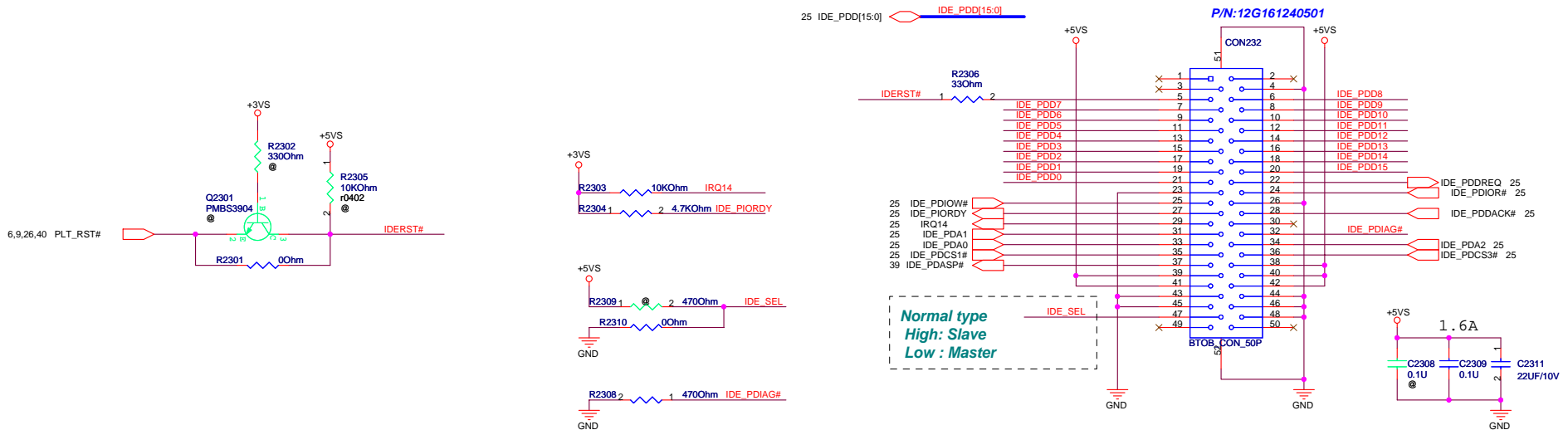
<Variant Name>

ASUS		Title : B TO B CONN(M)	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	F6S	1.1	
Date: Tuesday, August 21, 2007		Sheet	22 of 94

SATA HDD CON

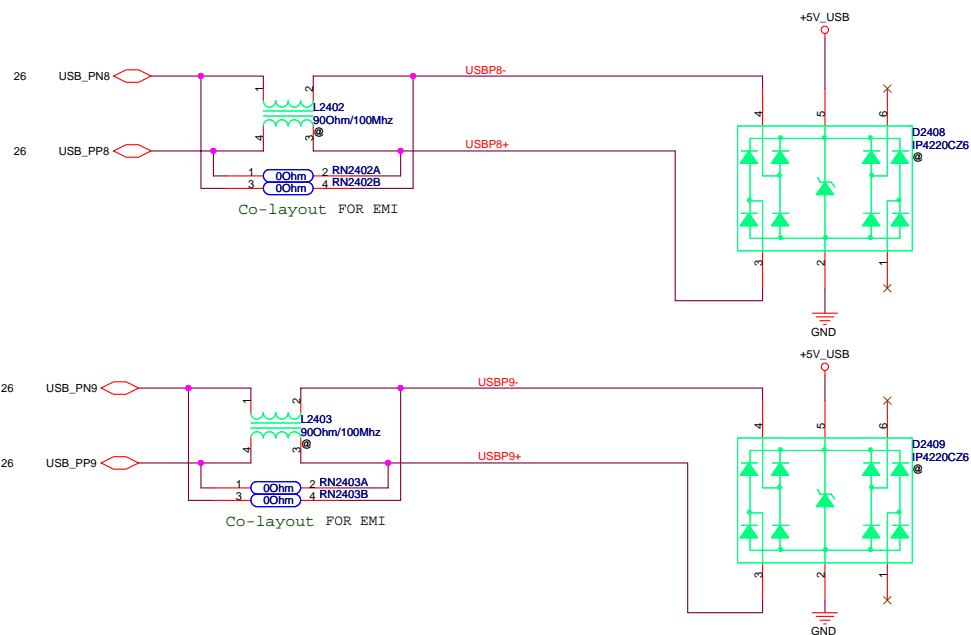


PATA CD-ROM CON



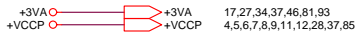
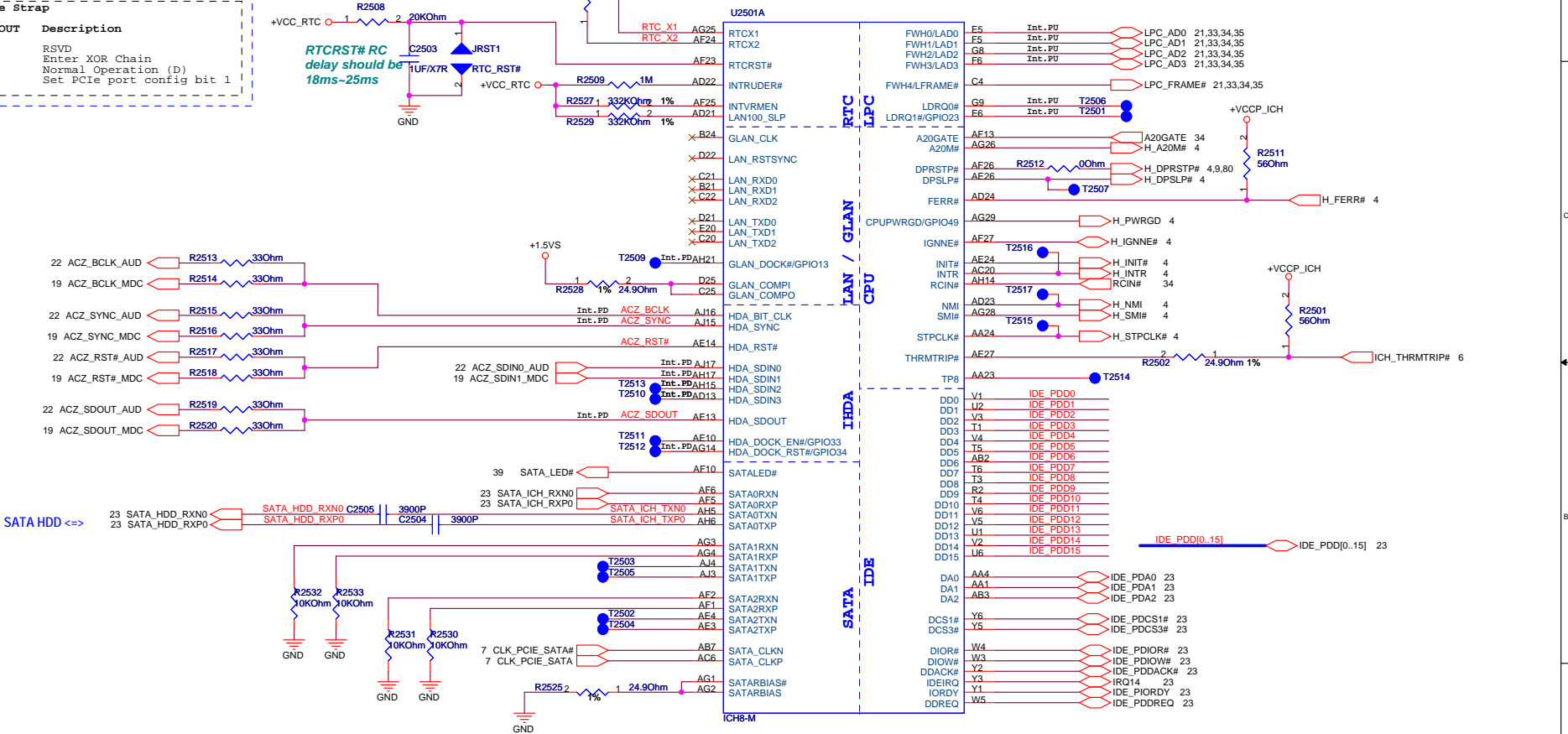
<Variant Name>

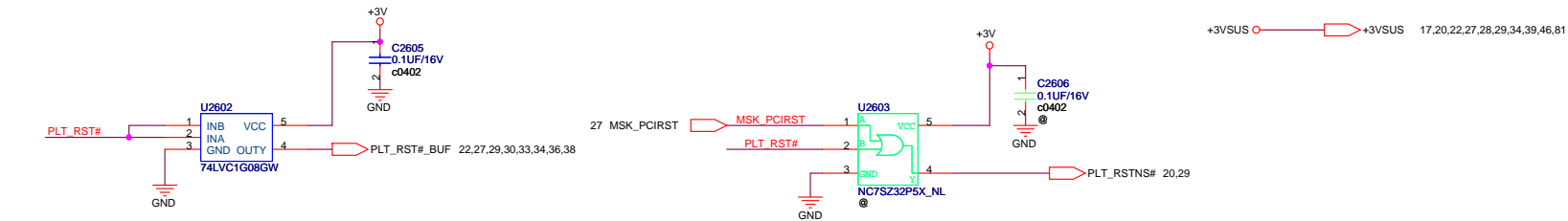
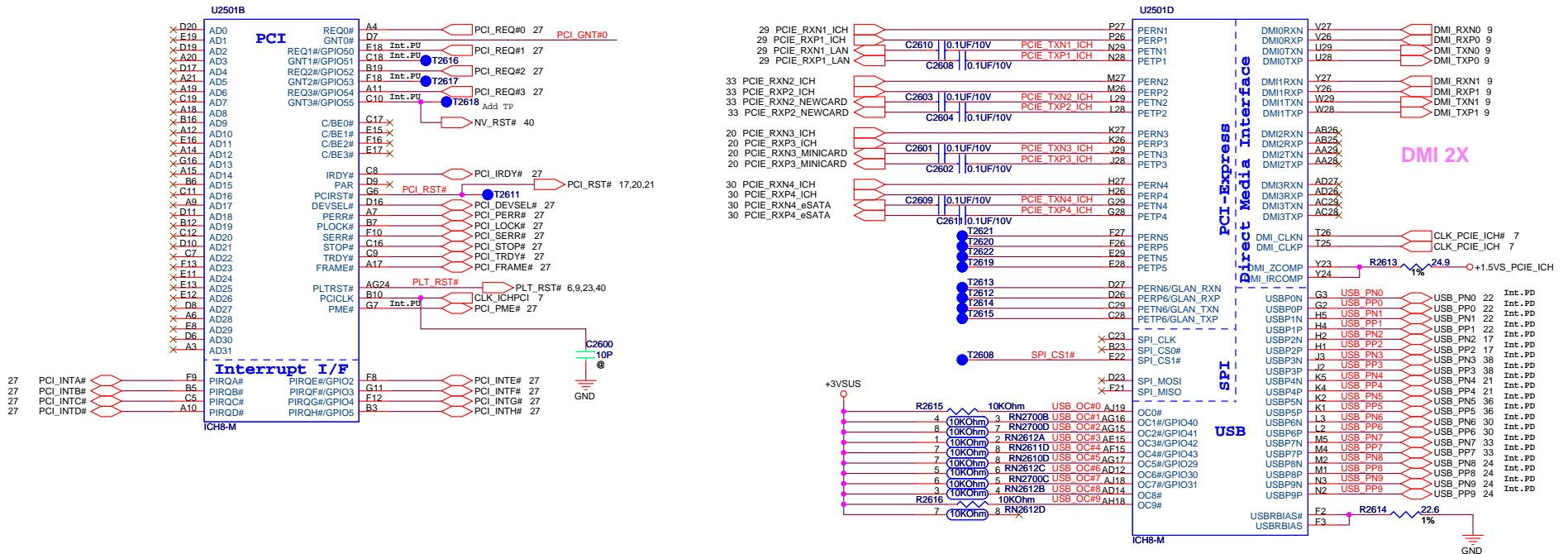
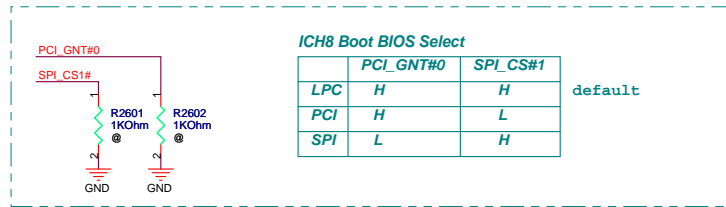
ASUS		Title : HDD & CDROM	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	F6S	1.1	
Date:	Tuesday, August 21, 2007	Sheet	23 of 94





XOR Chain Entrance Strap		
ICH_TP3	ACZ_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (D)
1	1	Set PCIe port config bit 1

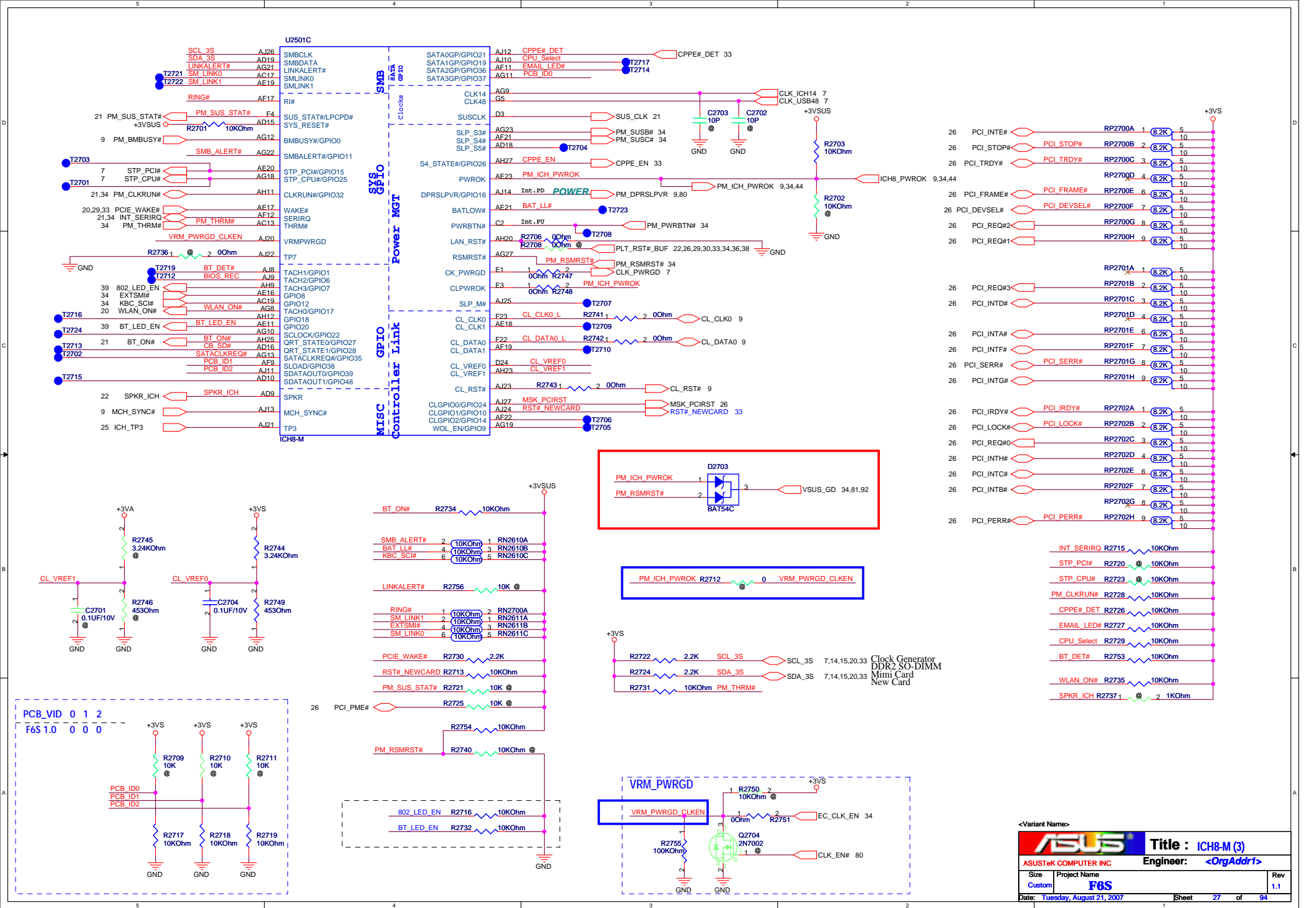


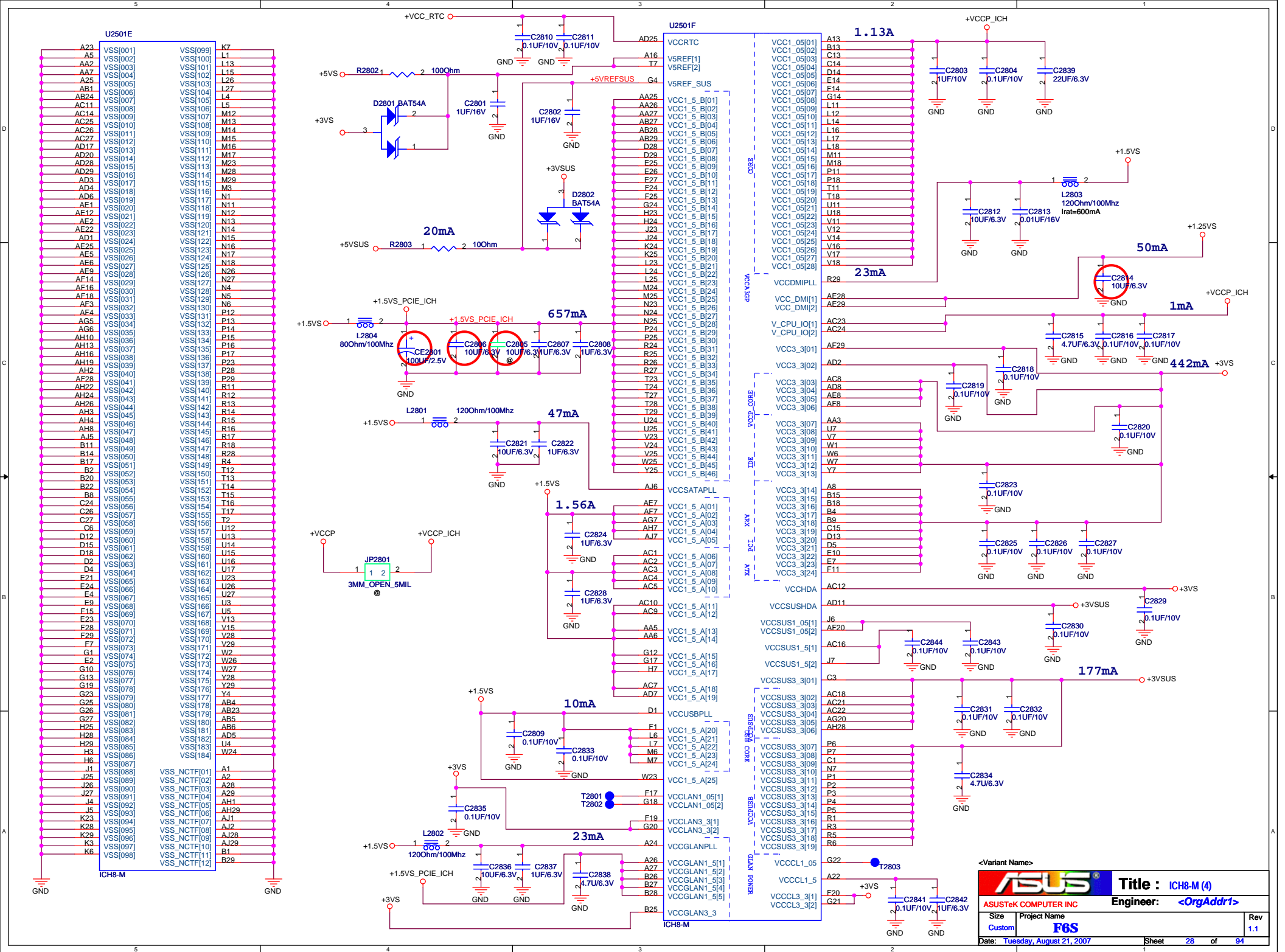


USB 0	USB Conn.
USB 1	WWAN
USB 2	Camera
USB 3	Finger Printer
USB 4	Bluetooth
USB 5	Card Reader
USB 6	USB Conn.
USB 7	Newcard
USB 8	USB Conn.
USB 9	USB Conn.


<Variant Name>

ASUS		Title : ICH8-M (2)	
ASUSTek COMPUTER INC		Engineer: <OrgAddr1>	
Size	Project Name		Rev
Custom	F6S		1.1
Date: Tuesday, August 21, 2007		Sheet	26 of 94

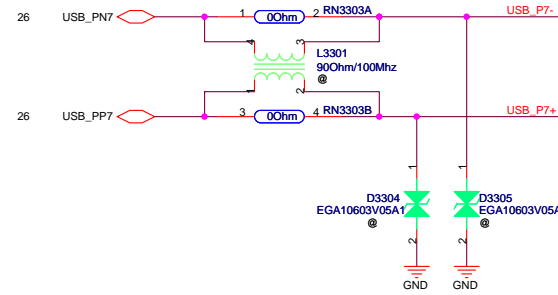
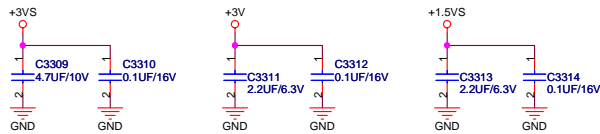
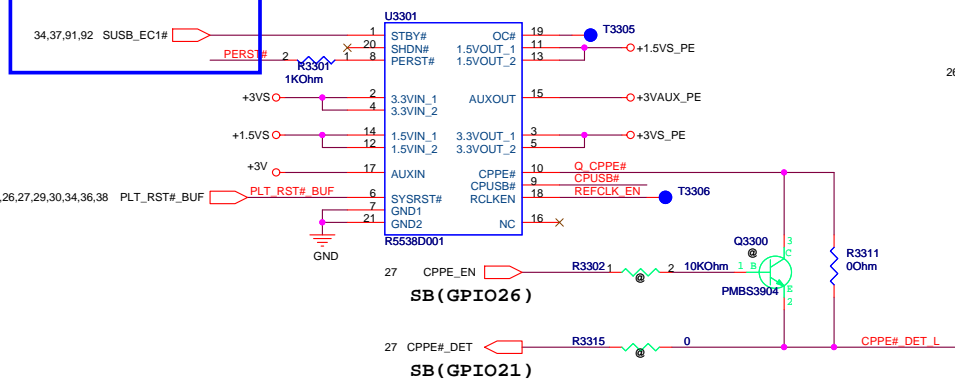




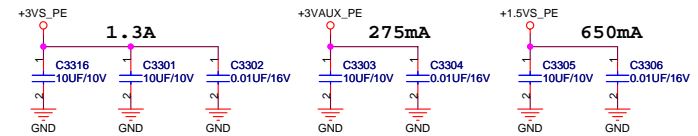
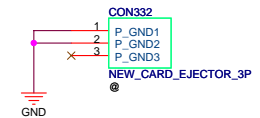
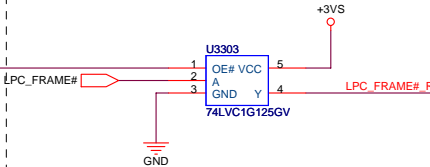
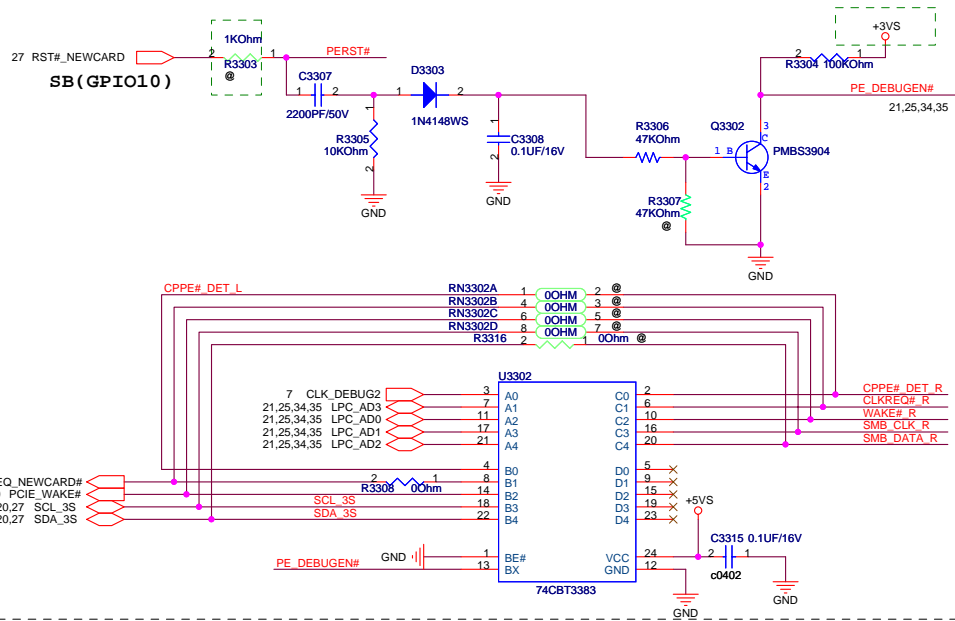
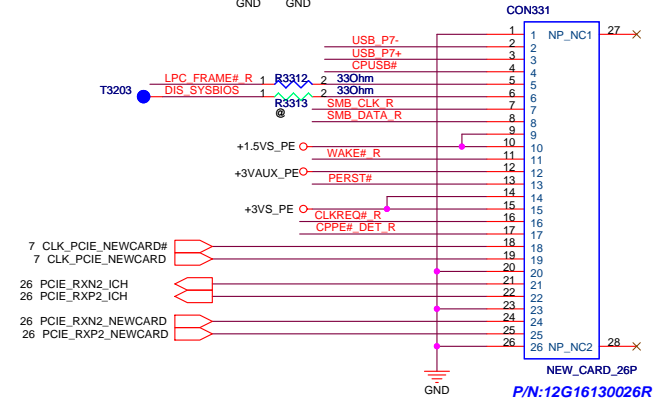
	A	B	C	D	E
1					
2					
3					
4					
5					

		Title : EMPTY	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	F6S		1.1
Date: Tuesday, August 21, 2007		Sheet	31 of 94

New EC pin to avoid the re-recognize when resume from S3/S4..

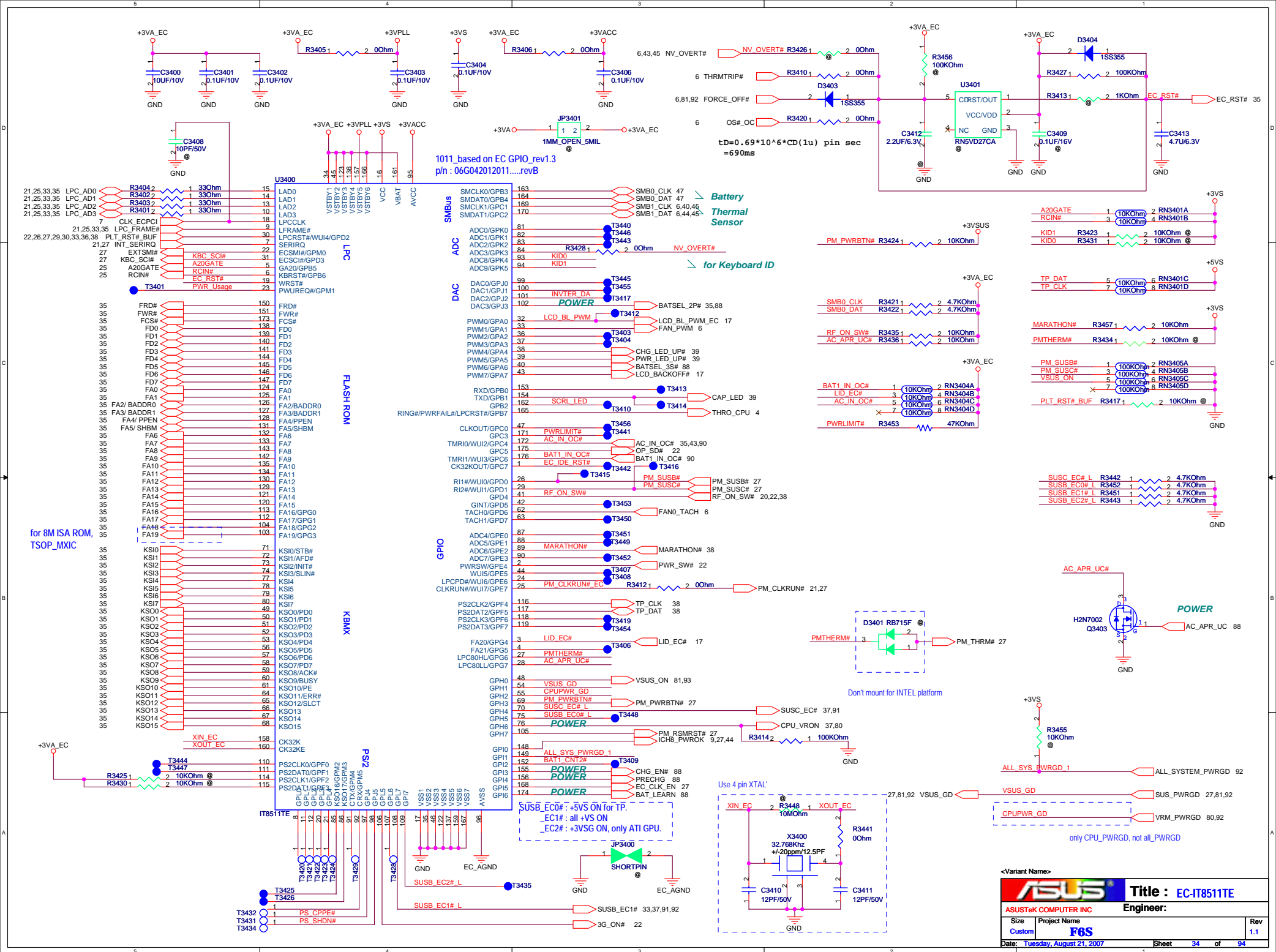


NewCard Header



<Variant Name>

ASUS		Title : NEW CARD	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	F6S	1.1	
Date: Tuesday, August 21, 2007		Sheet	33 of 94

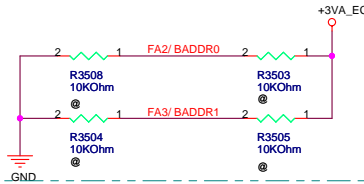


ISA ROM_TSOP

EC Hardware Strapping

FA2/ BADDR0 & FA3/ BADDR1

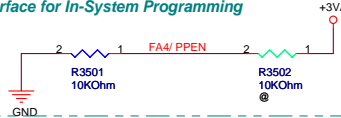
- 00: PNPCNG Access Register Pair Are 002Eh and 002Fh
 10: PNPCNG Access Register Pair Are 004Eh and 004Fh
 01: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.
 11: Reserved



Note: Sampled at VSTBY Power Up Reset

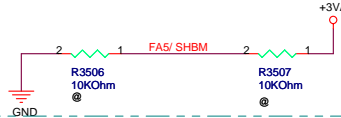
FA4/ PPEN

- 0: Normal
 1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming

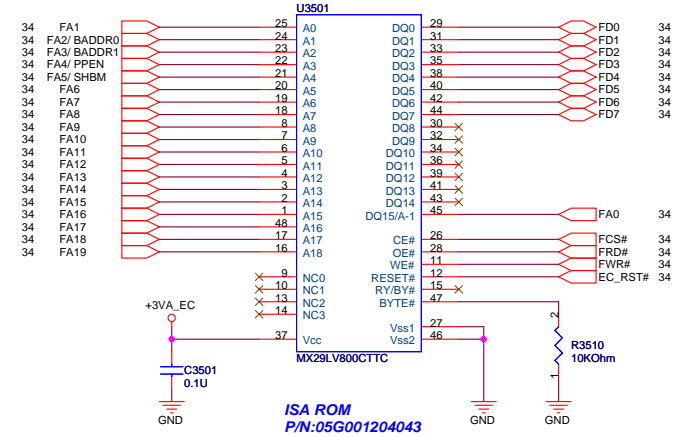


FA5/ SHBM

- 0: Disable Shared Memory with Host BIOS
 1: Enable Shared Memory with Host BIOS



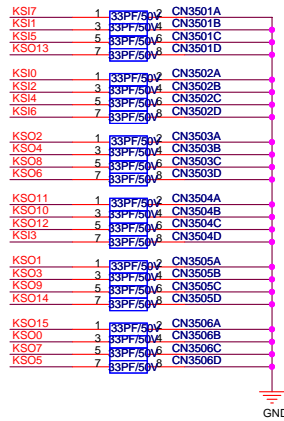
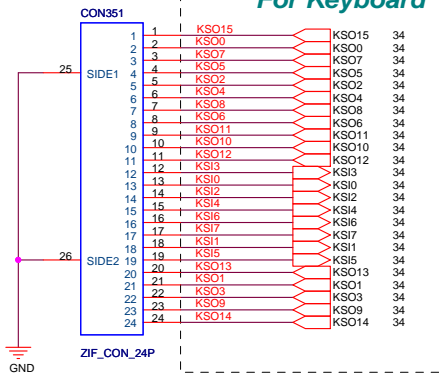
8M TSOP _ MXIC



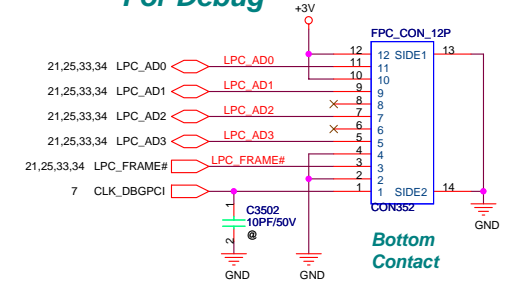
ISA ROM
 P/N:05G001204043

P/N:12G182402404

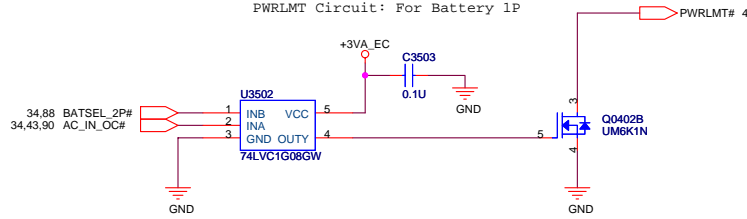
For Keyboard



For Debug

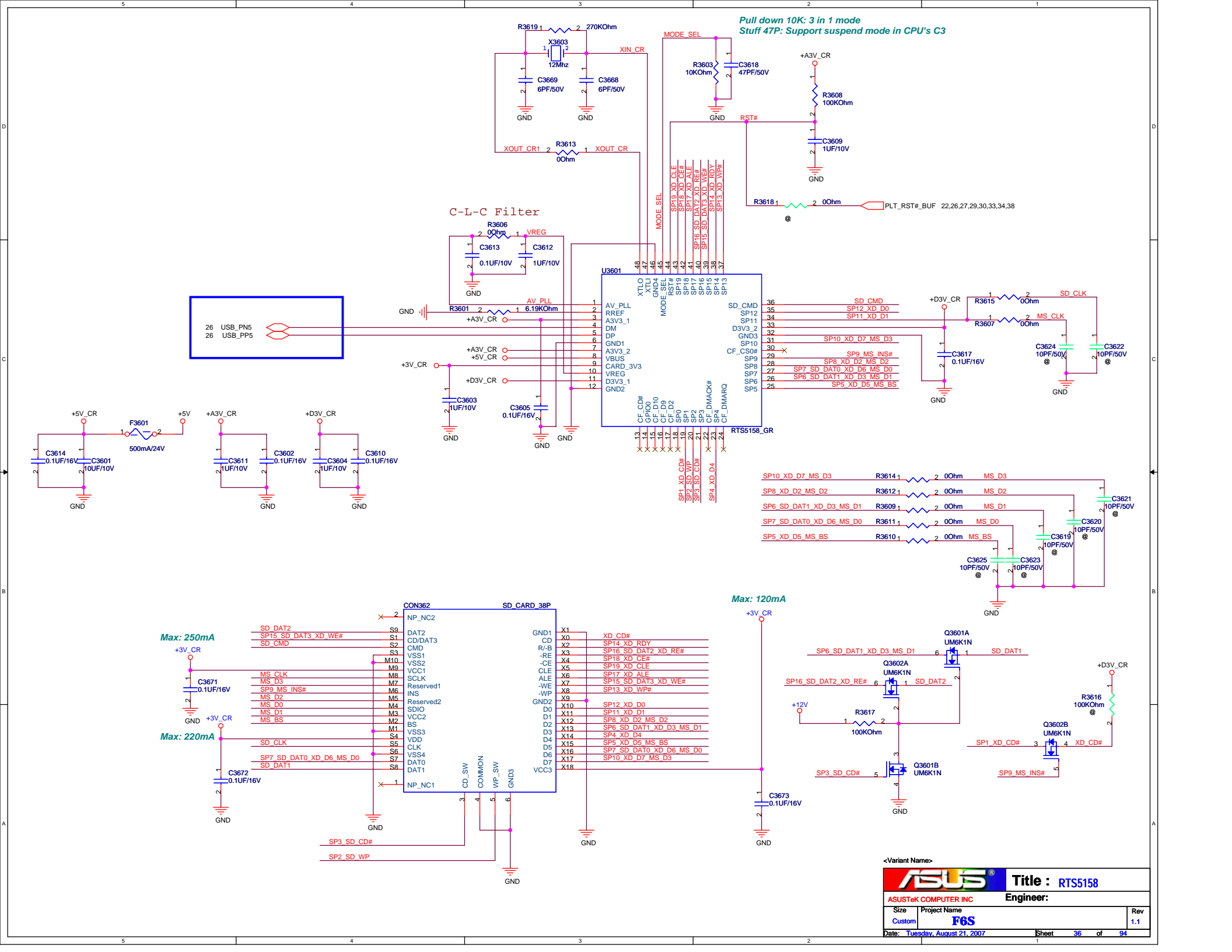


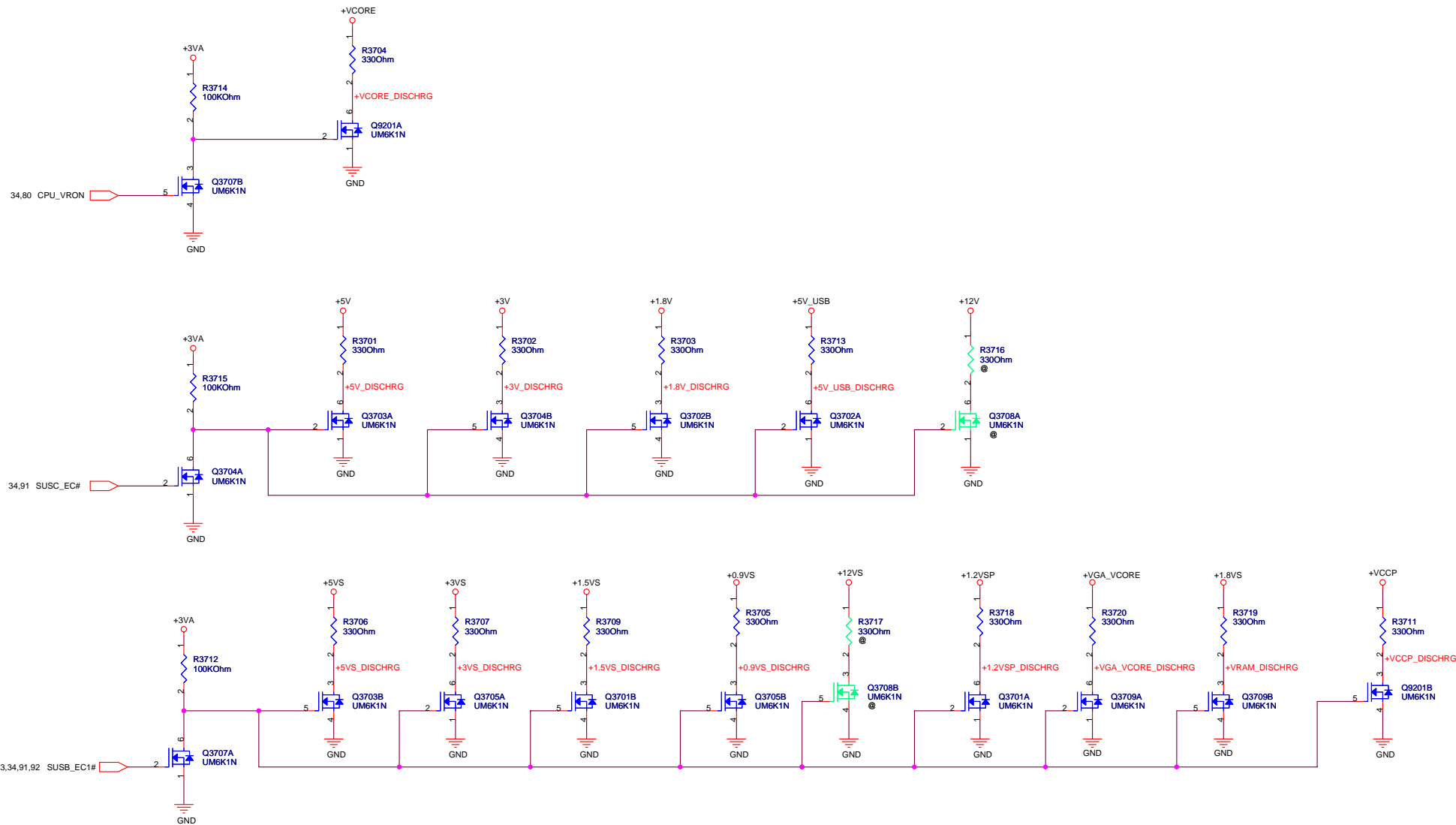
PWRLMT Circuit: For Battery LP



<Variant Name>

ASUS		Title : ISA_ROM&KB conn	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	F6S	1.1	
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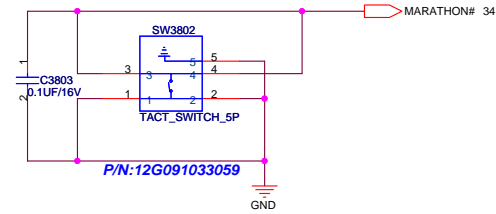




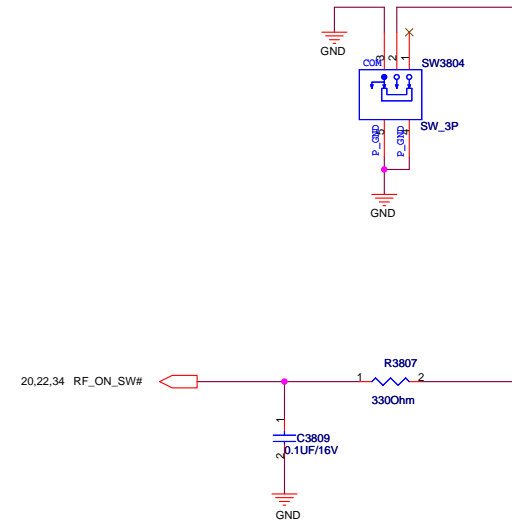
<Variant Name>

ASUS		Title : DISCHARGE	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	F6S	1.1	
Date: Tuesday, August 21, 2007		Sheet	37 of 94

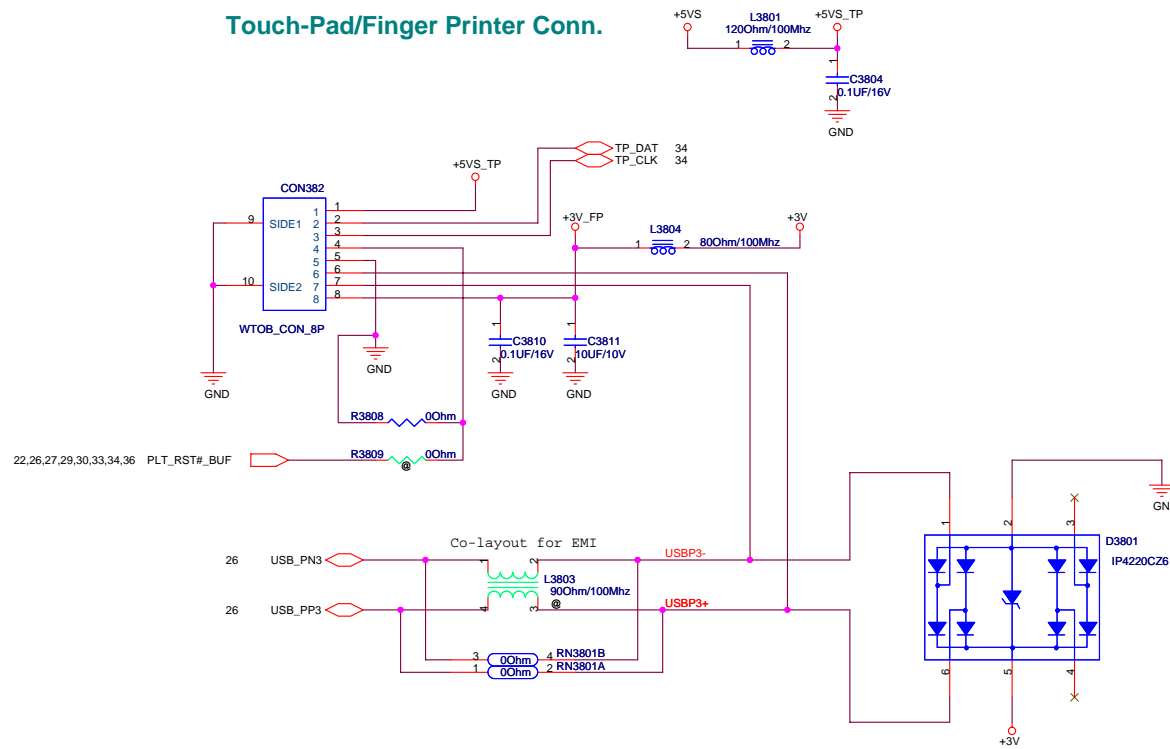
MARATHON#



BT/WLAN SW



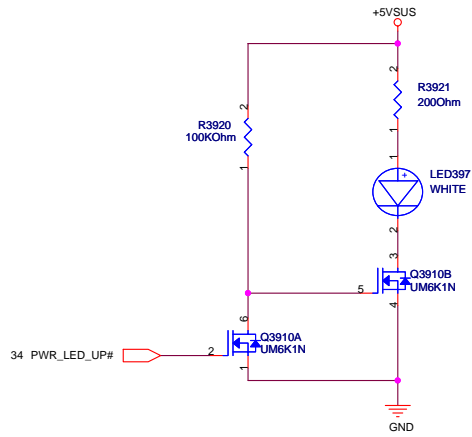
Touch-Pad/Finger Printer Conn.



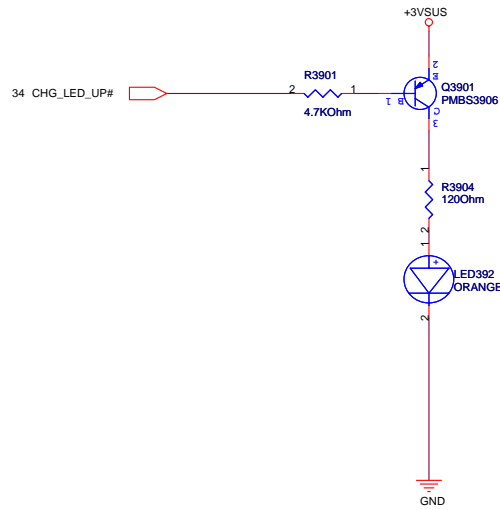
<Variant Name>

ASUS		Title : KEY & LED	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	F6S	1.1	
Date:	Tuesday, August 21, 2007	Sheet	38 of 94

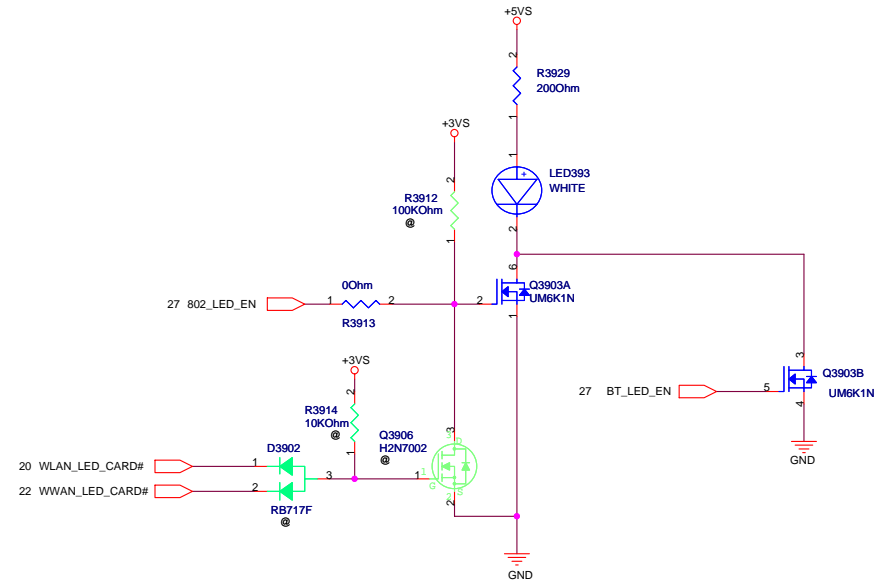
PWR LED



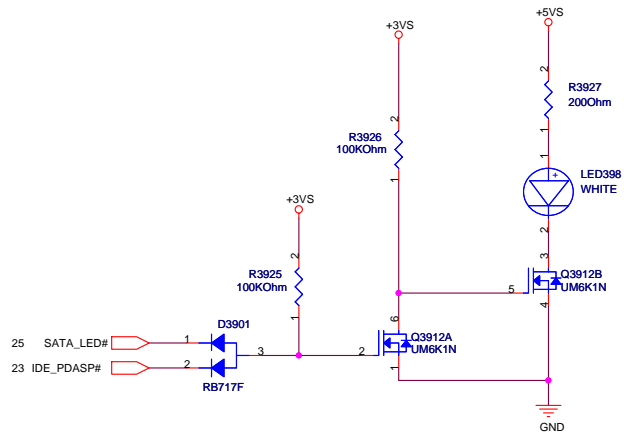
BATTERY LED



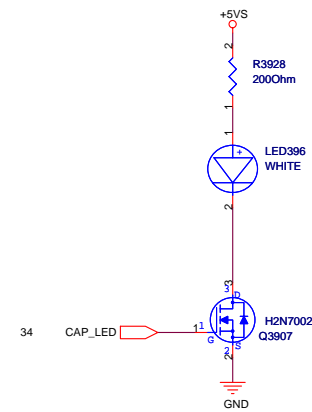
WireLess/BT LED



SATA/IDE LED

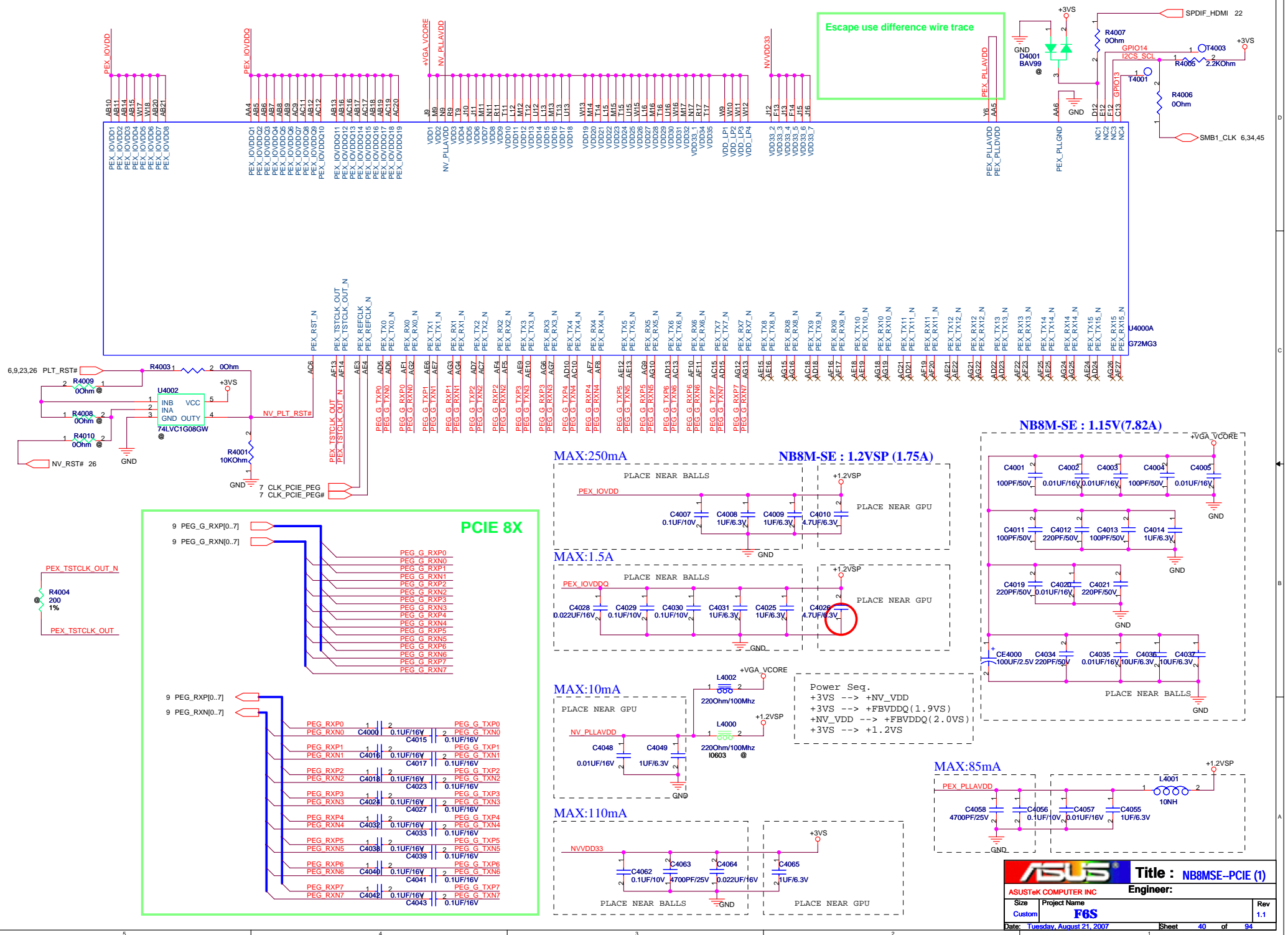


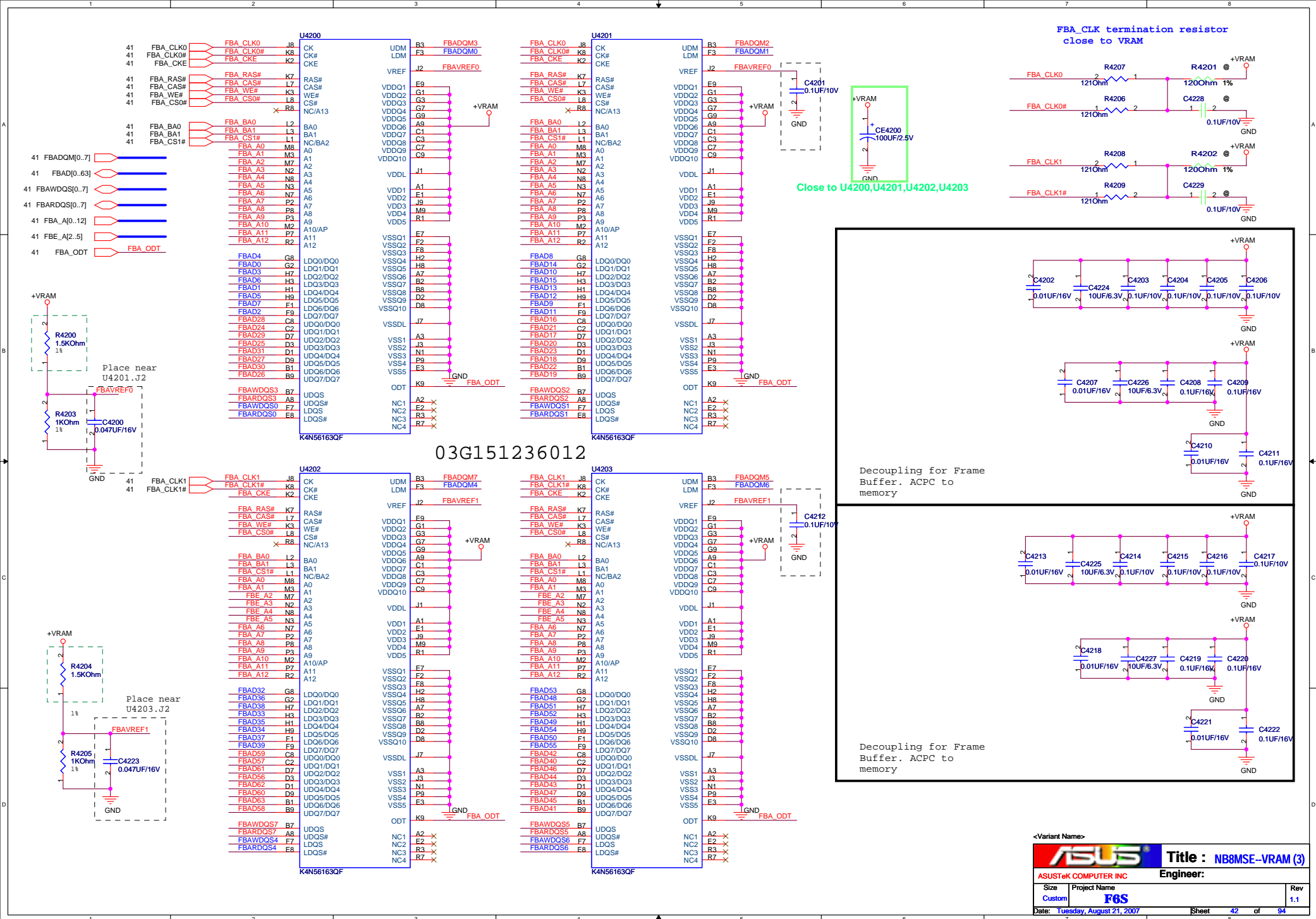
Cap. Lock

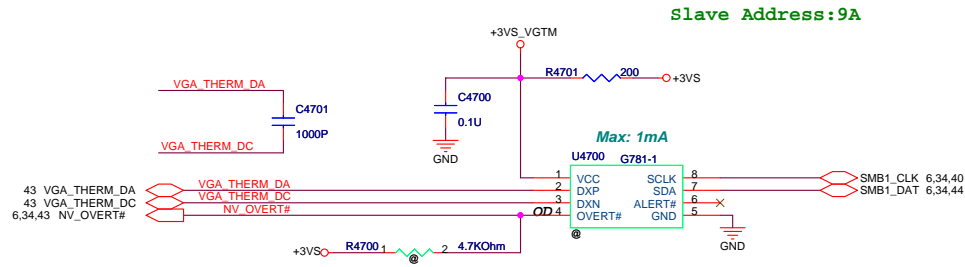


<Variant Name>

ASUS		Title : LEDs	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	F6S	1.1	
Date: Tuesday, August 21, 2007	Sheet	39	of 94



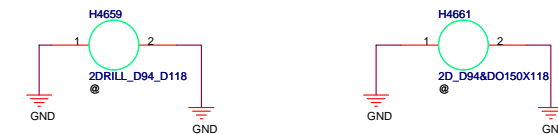
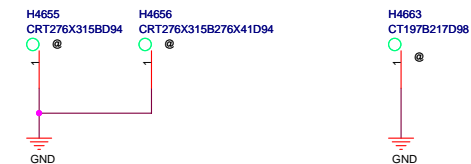
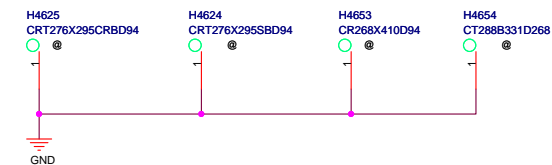
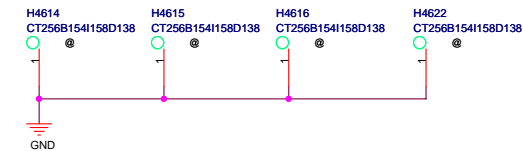
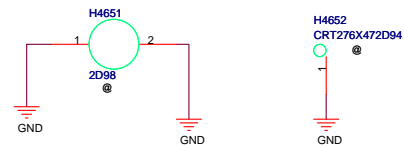
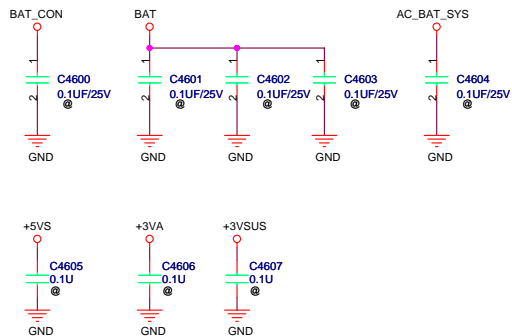
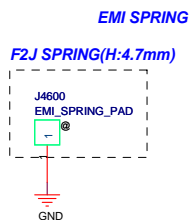
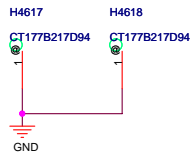


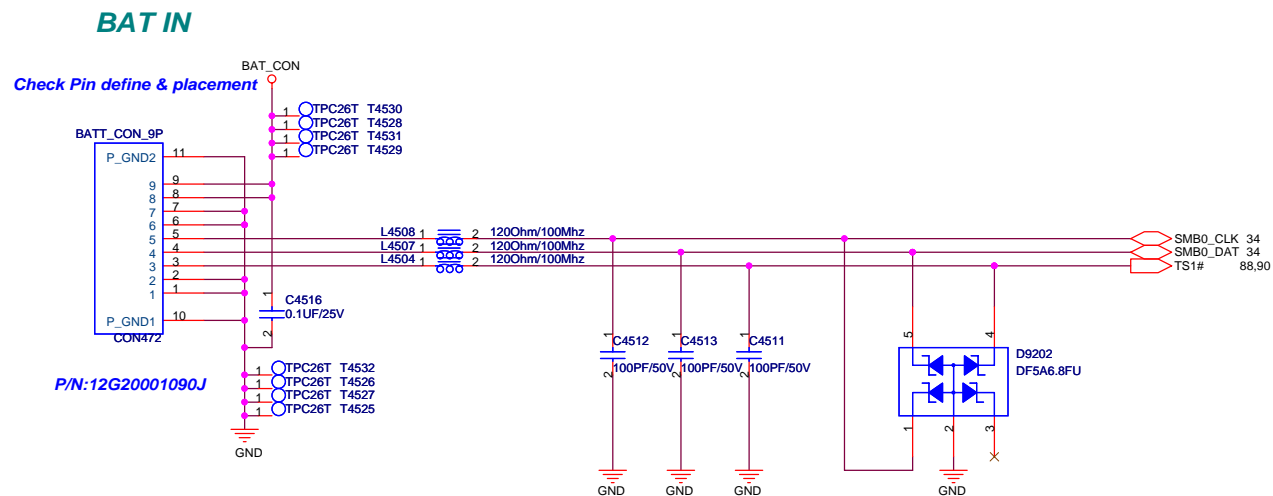
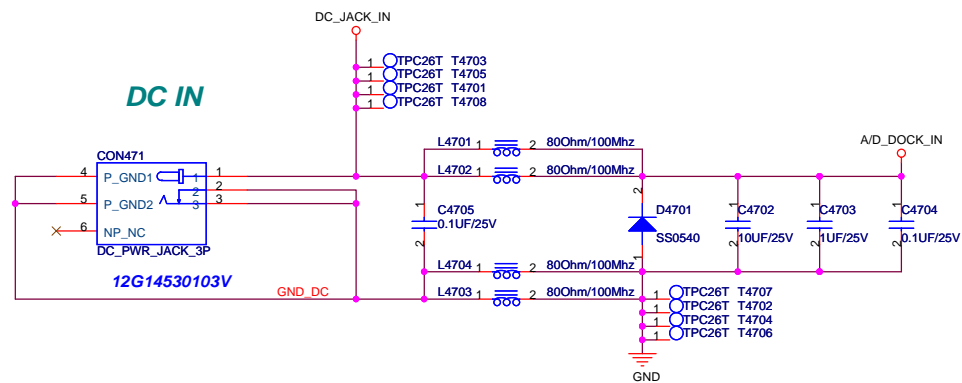


For frame buffer address/command lines those external pull up resistor can be removed for easy layout from Nvidia FAE

<Variant Name>

ASUS		Title NB8MSE-VRAM_TERM	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	F6S	1.1	
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Rev0.3 (Change from R0.2)

1. Page 30: Change C3024, C3025 and C3029 from 4.7uF to 10uF for JMB FAE suggestion.
2. Page 30: Del R3002, R3004, R3005 and R3006.
3. Page 21: Del Finger printer power reset circuit for restart.
4. Page 29: Change C2938 4.7U 0603 to 0805 for cost down.
5. Page 38: Combine TP and F/P to one connector.
6. Page 19: Swap HDMI signals for layout request.
7. Page 20: change H2001 and H2002 to 13GNHC10M020-1.
8. Page 34: Add EC_RST# circuit for EC team suggestion.
9. Page 20: change H2001 and H2002 to 13GN7510M270-1 and change CON2001 to 12G030000523
10. Page 22: Swap CON2201 pin define for IO board layout.

Rev0.4 (Change from R0.3)

11. Page 30 and page 34: Swap RN3401 L3001 and RN3001 for layout.
12. Page 30: Swap RN3001 and D3001 for layout.
13. Page 38: Change SW3802 to 12G091033059.
14. Page 26 and 40: Add NV_RST#(GPIO55) for NV8M-SE reset.
15. Page 7: Add Q0701 for clock generator power saving.
16. Page 47: Change CON472 to 12G20001090J
17. Page 19: Change R1902 and C1901 from 0603 size to 0402 size.
18. Page 38: Swap SW3804 Pin1 and Pin2 to meet ME request.
19. Page 38: Del L1708 and add R1706 100 ohm for short protection.
20. Page 26, 35 and 40: Change U2602, U3502 and U4002 from 06G004131011 to 06-004092010 for cost down.
21. Page 26: Change U2603 from 06G004603217 to 06G004603219 for cost down.
22. Page 7: Mount R0707 for PEREQ1# and PEREQ2#.
23. Page 28: Add C2839 for +VCCP_ICH.
24. Page 28: Change C2812 to 11G23521065320 for cost down.
25. Page 6: Add R0606 for PM_THRMTRIP# pull up to +VCCP.
26. Page 7: Change reference R785 to R0788
27. Page 16: Add C1603 4.7U for +0.9VS.
28. Page 27: Add R2703 and D2702 and DNI R2702 for ICH8_PWROK, to fix auto power on issue.
29. Page 24: Change R2411 0 ohm from 0603 to 0805 size.
30. Page 17: Add R1708 0 ohm for CCD.
31. Page 26 and 27: Del R2714 and R2738, add RN2613, swap RN2610, RN2612 and RN2700 for USB_OC[0~9]. USB_OC[1~7] can be set GPI if not needed (DNI RN2612 and RN2700).

32. Page 30: JMicron suggest to add R3020, C3035 and C3036 for eSATA JMB360.
33. Page 19: Del R1904-R1911, and add RN1901-RN1904.
34. Page 33: Change C3308 0.1u(Y5V) from 0603 to 0402. 0603 0.1u(Y5V) is single part.
35. Page 24: Del D2403, D2404, D2405 and D2406, add D2407 and D2408 for cost issue.
36. Page 43: Add R4314, R4318, R4319, R4338 and Q4301 for using NV8M-SE internal sensor.
37. Page 39: Del BT LED (DED395, R3909) and Num LED (LED394, R3906, Q3905) for sales PM request.
38. Page 47: Del D4504, D4505, D4506 and add D4507 for cost down.
39. Page 30 and 35: Change eSATA connector (CON301) and debug connector (CON352) for ME request.
40. Page 22: Add Q2202 for HDMI SPDIF jack sense.

Rev0.5 (Change from R0.4)

41. Page 39: Modify the LED circuit for white LED.
42. Page 46: Update all screw hole.
43. Page 6: Remane +5VS to +5V_FAN for FAN circuit as power request.
44. Page 46: Update H4631 screw hole.
45. Page 28: Change C2801 and C2801 from 0.1u to 1u.
46. Page 39: Change R3926 pin2 pull high from +5VS to +3VS.

Rev1.0 (Change from R0.5)

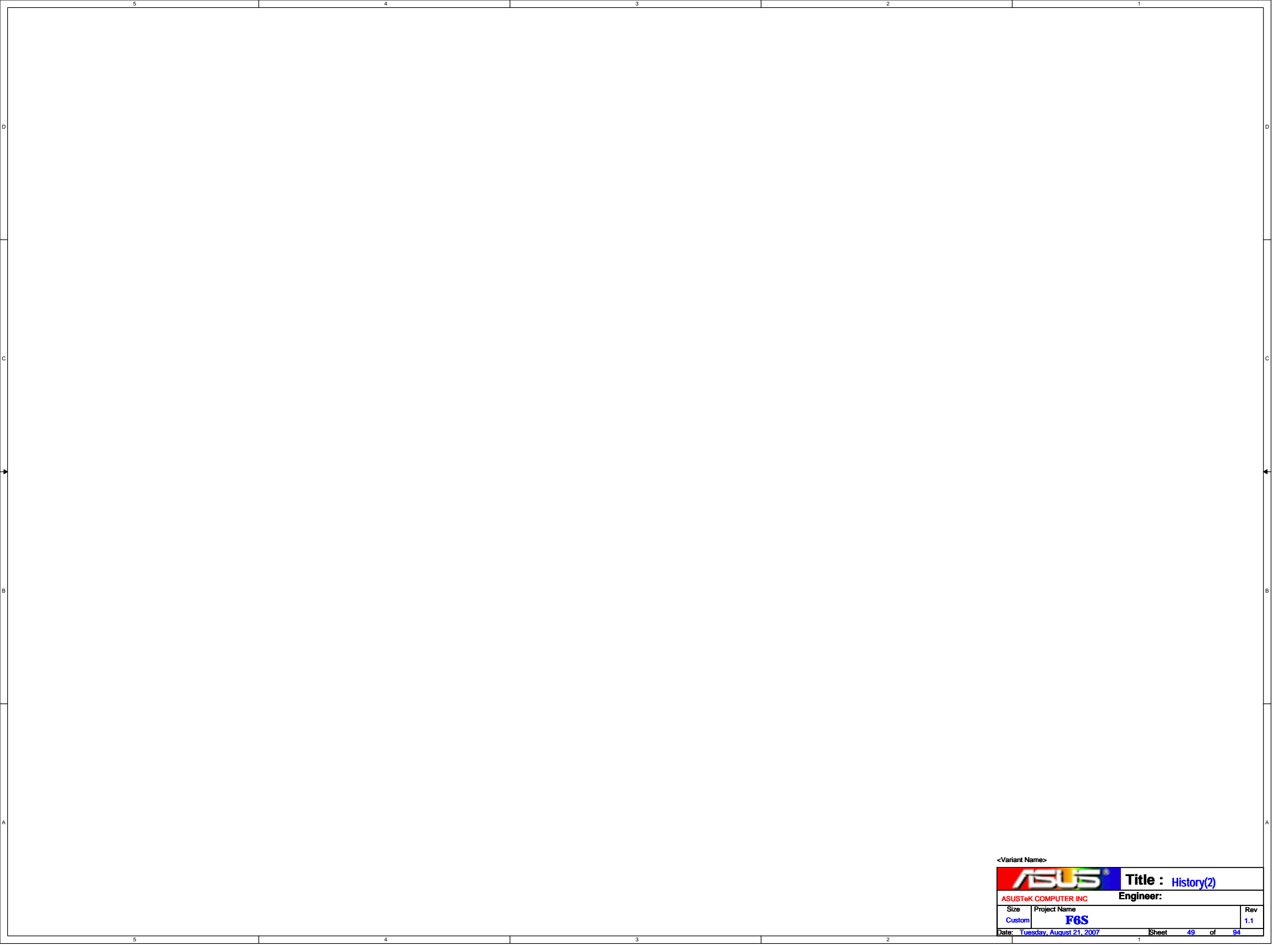
47. Change Rev from 0.5 to 1.0

Rev1.01 (Change from R1.0)


48. Page 16: Change R1614 and R1615 from 10K to 1K, can meet S3 Vref voltage spec.
DNI R1614, R1615 and Mount R1620 for Vref voltage provide from power.
49. Page 07: Change R0713 from 33 ohm to 39 ohm to meet rise and fall timing.
50. Page 12: Change C1220, C1227 and C1236 from 22uF to 4.7uF for cost down.
51. Page 12: Change C1207, C1214, C1217 and C1224 from 22uF to 10uF for cost down.
52. Page 12: Del C1202 4.7uF (0603) and Change C1201 from 4.7U (0603) to 10uF (0805) for cost down.
53. Page 28: DNI C2805 and change C2806 from 22uF to 10uF for cost down.
54. Page 28: Change CE2801 from 220uF to 100uF for cost down.

55. Page 21 & 38: Del Q2101 and R3806 for never use.
56. Page 40: Change C4026 from 22uF (1206) single part to 4.7uF for cost down.
57. Page 6, 9, 30 & 34: Del 0 ohm R0655, R0937, R0938, R3010, R3015, R3418, R3419, R3445, R3449 and R3454 for cost down.
58. Page 30: Del U3002, C3002 and C3015 for never use.
59. Page 36: DNI R3608 and C3619, mount R3618 use PLT_RST#_BUF to reset RTS5158
60. Page 29: Add C2941 and C2942 for _1.8V_LAN.
61. Page 6: DNI R0606 and C0650.
62. Page 6: Mount CN3501, CN3502, CN3503, CN3504, CN3505, and CN3506 for EMI request.
63. Page 27: Del D2701, D2702 for no use as EC pin ICH8_PWROK, PM_RSMRST# open drain output.
64. Page 30: DNI C3035, C3036 (eSATA Issue)
65. Page 23: Del CE2301 100uF and add CE2302 and CE2303 47uF x2 for cost down.
66. Page 30: Change CE3001 to CAP EL 100uF/10V for cost down.
67. Page 36: Add R3619 for Realtek suggestion.
68. Page 35: DNI R3505, R3507 and R3508 for EC team suggestion.
69. Page 39: Del R3922, R3923, Q3911 for mouse.
70. Page 6: Add L4703 and L4704 for EMI request.
71. Page 38: Change SW3804 to 12G09107003M.
72. Page 17: Change CON175 to 12G17001030V.
73. Page 46: Add screw hole H4663.
74. Page 24: Change CON242 and CON243 to 12G131050044.
75. Page 29: Change TRL8111C.
76. Page 29: Change R2903 to 2.21K ohm for GigaLan requires
77. Page 22: DNI Q2202 for not support HDMI jack sense.
78. Page 29: Mount C2943 for 100m cable link. Del C2941 and C2918.
79. Page 38: Add R3808 and R3809 (PLT_RST#_BUF) for Finger Printer.
80. Page 36: Change C3668 and C3669 to 6pF for Realtek suggestion.
81. Page 36: Mount C3618, C3609, R3608 and DNI R3618 for Realtek suggestion.
82. Page 29 & 30: Change C2933, C2934, C3016 and C3017 to 27pF for ITTI suggestion.
83. Page 7: Change C0709, C0710, 30pF for ITTI suggestion.

		Title : History(1)	
ASUSTeK COMPUTER INC		Engineer:	
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<Variant Name>



Title : History(2)

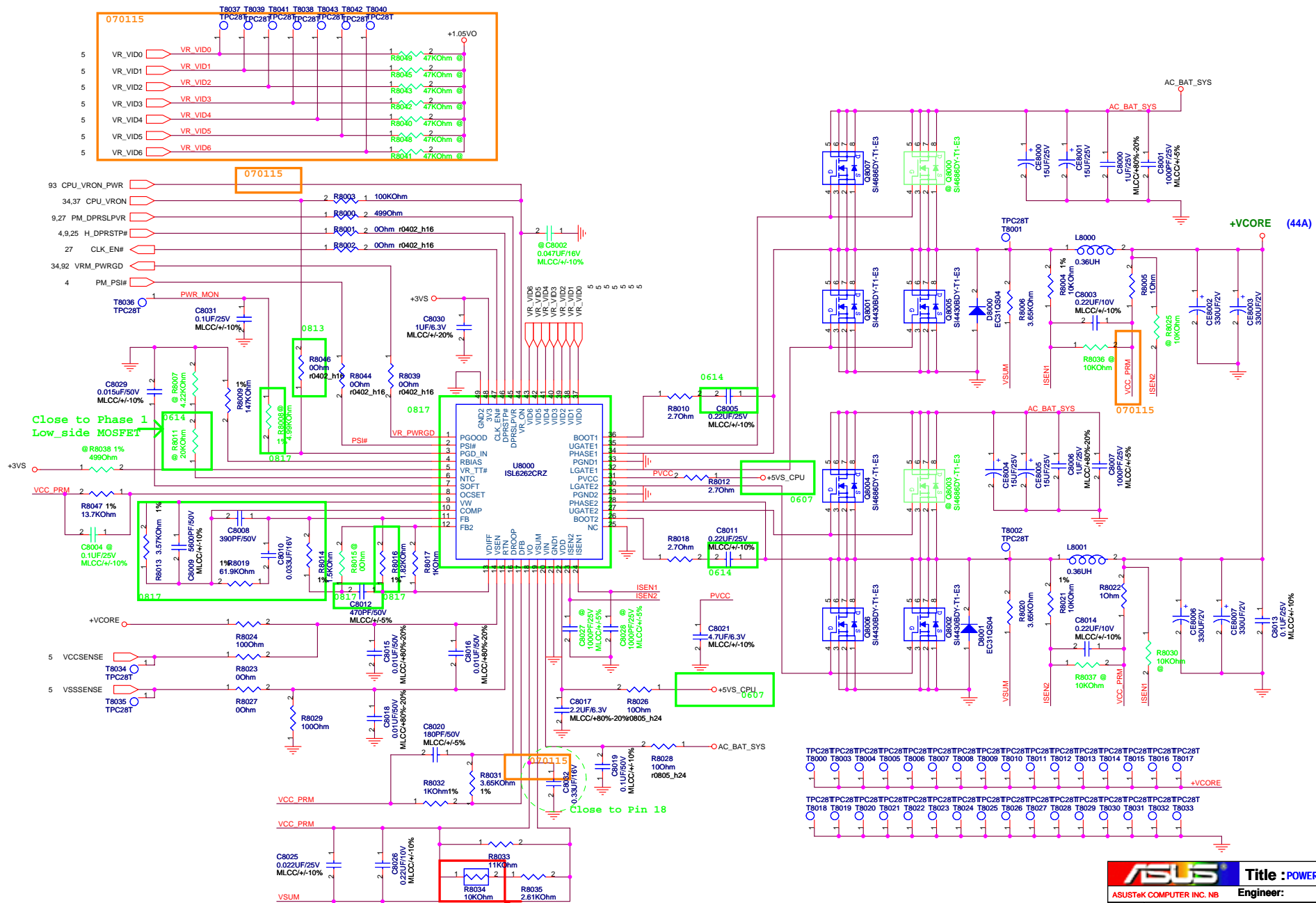
ASUSTeK COMPUTER INC

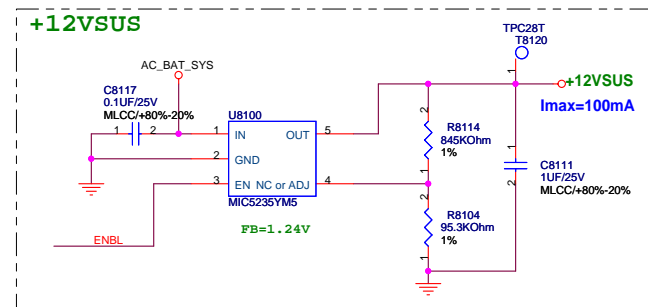
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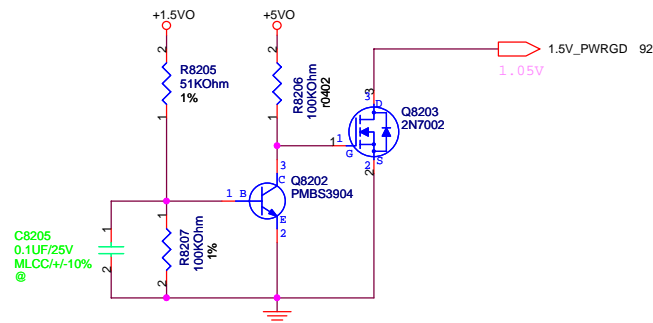
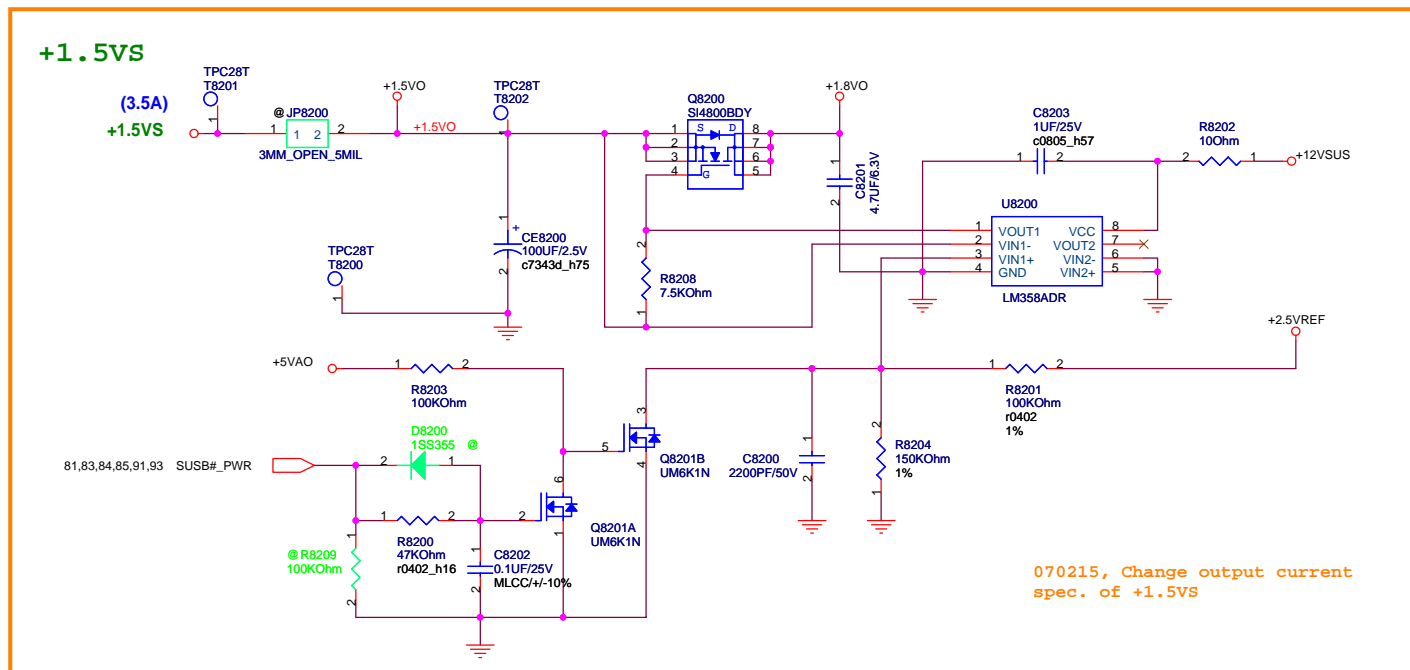
Size	Project Name	Rev
Custom	F6S	1.1

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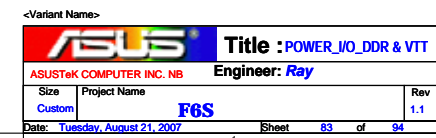


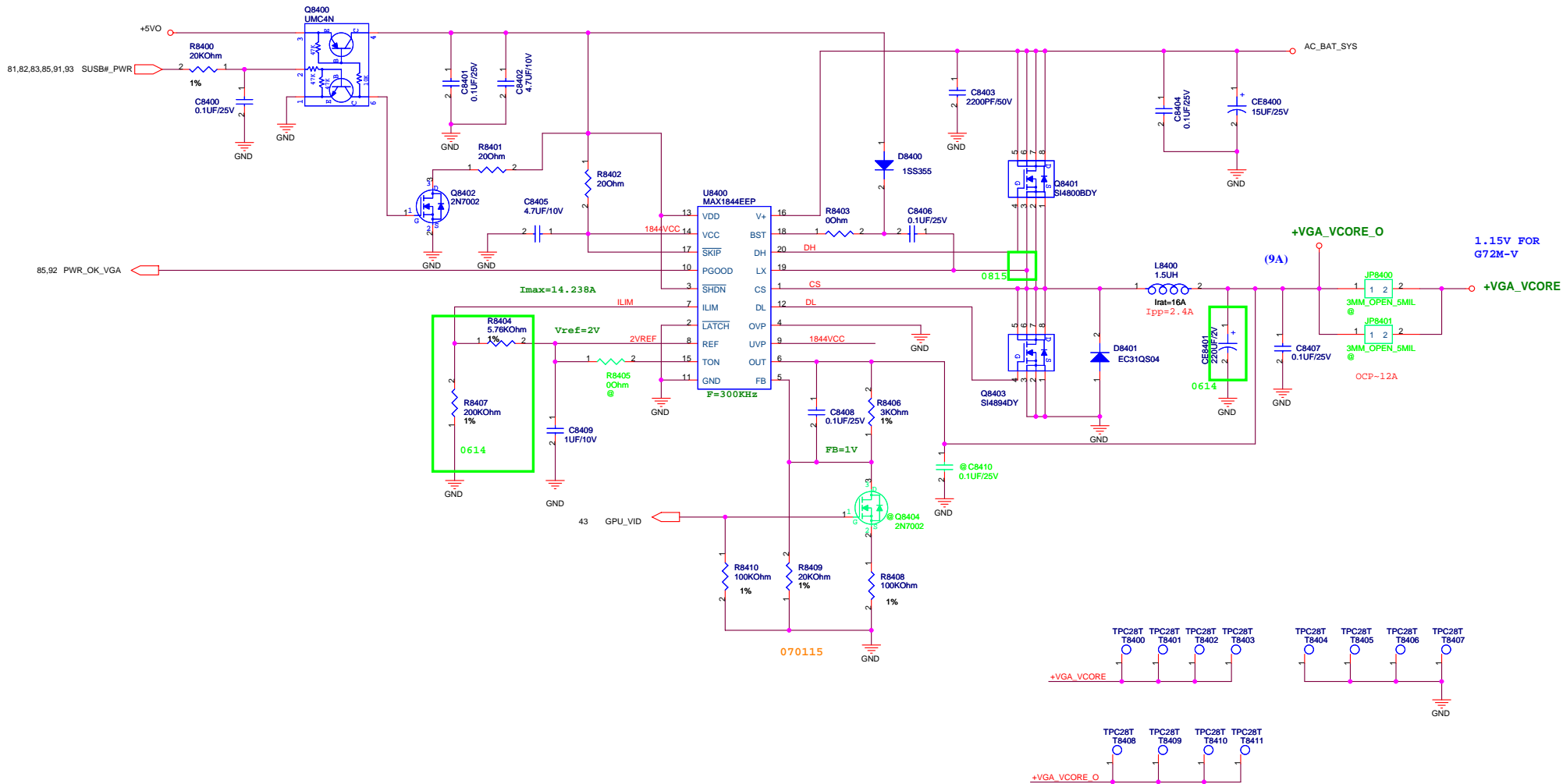




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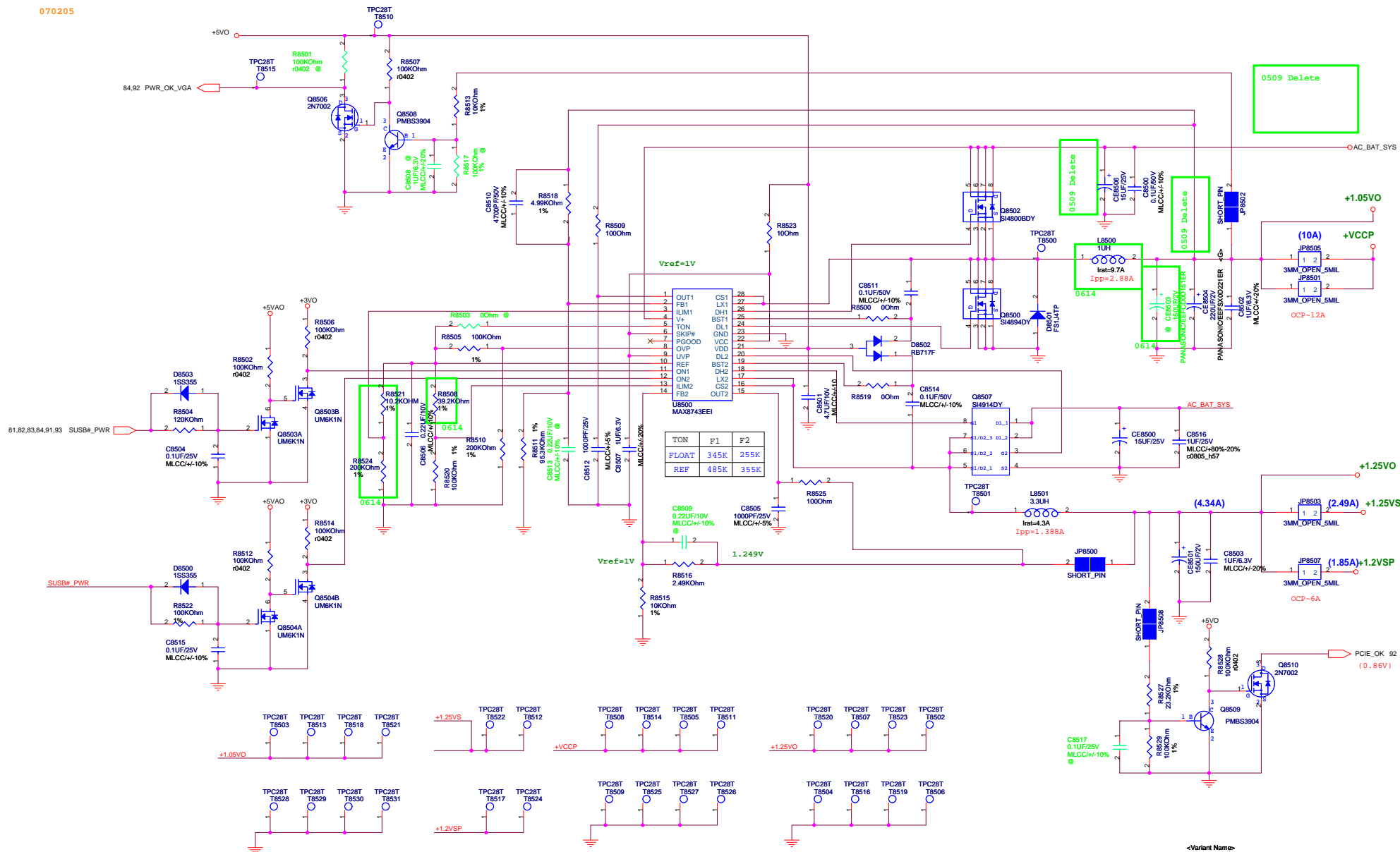
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ASUSTeK COMPUTER INC. NB		Engineer: Ray	
Size B	Project Name F6S		Rev 1.1
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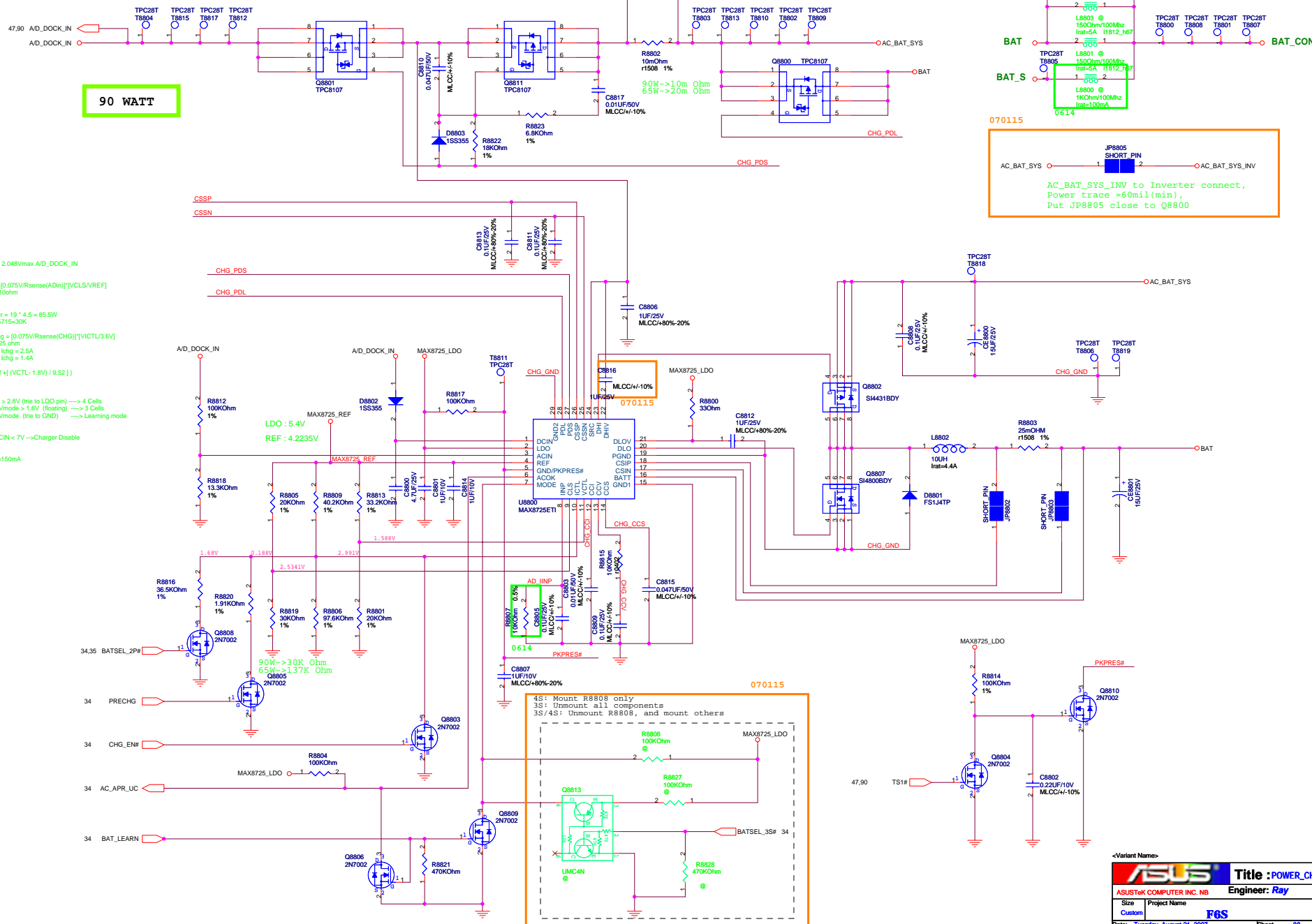


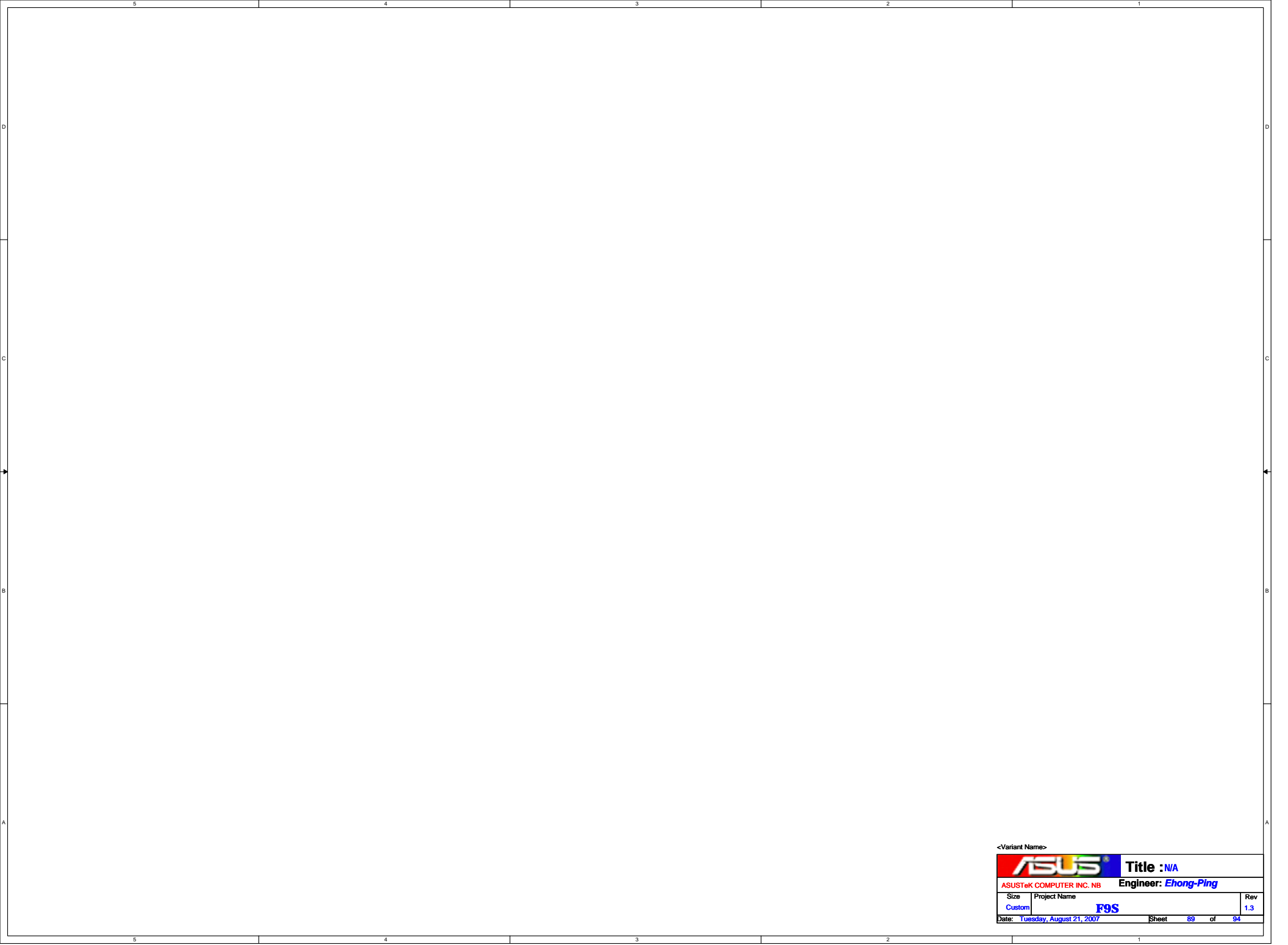
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ASUSTeK COMPUTER INC. NB		Engineer: Ray	
Size	Project Name	Rev	
Custom	F6S	1.1	
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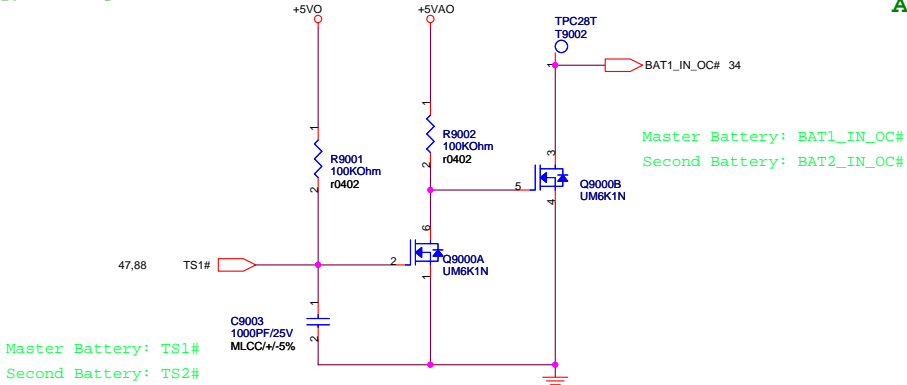
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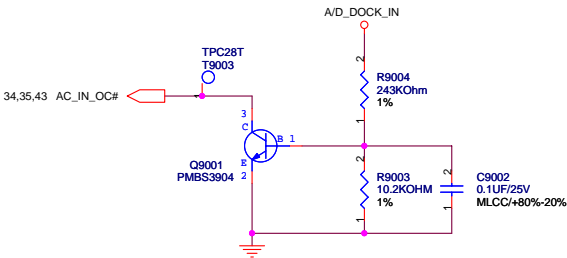


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ASUSTeK COMPUTER INC. NB			Engineer: <i>Ehong-Ping</i>			
Size	Project Name				Rev	
<i>Custom</i>	F9S				<i>1.3</i>	
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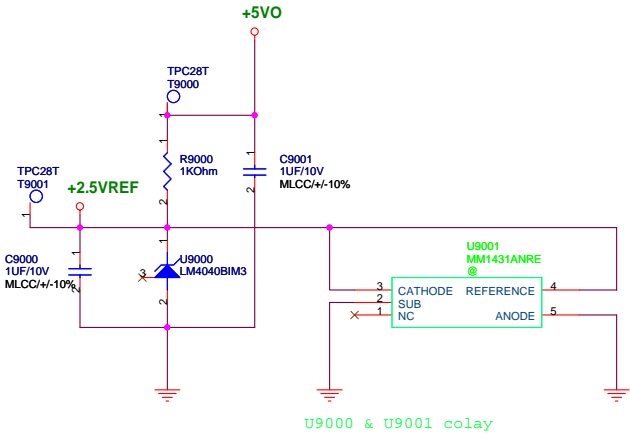
BATTERY IN DETECT



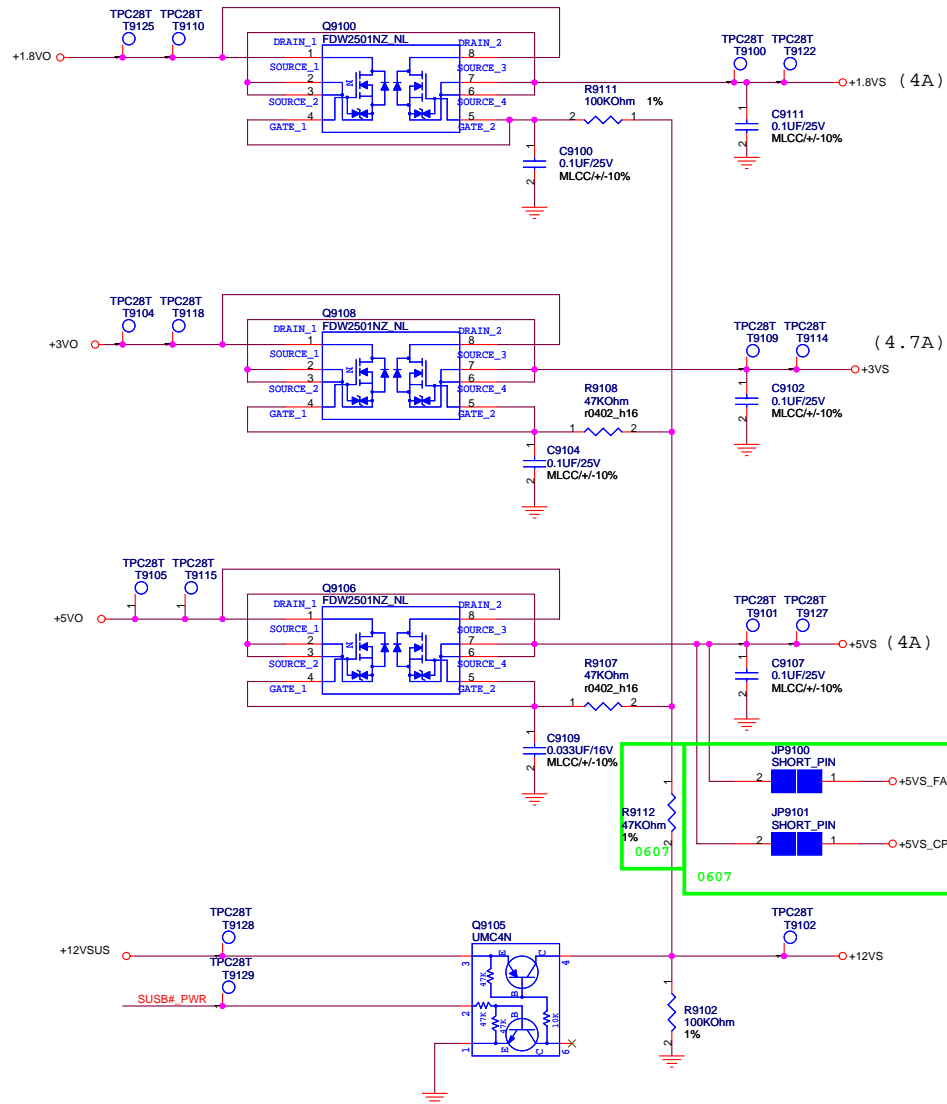
ADAPTER IN DETECT



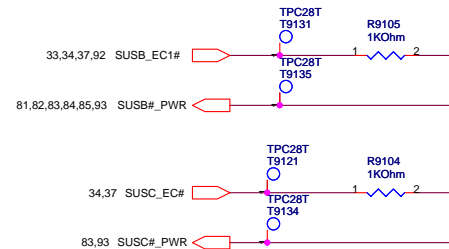
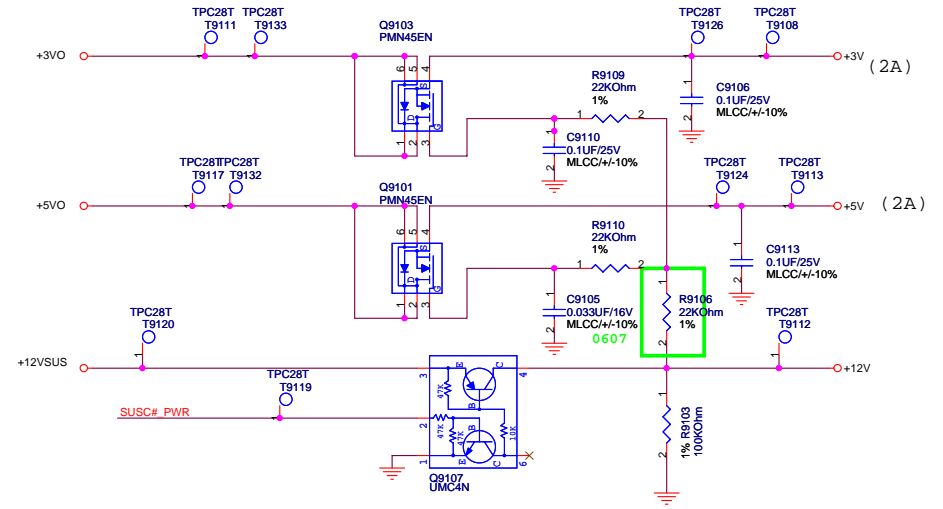
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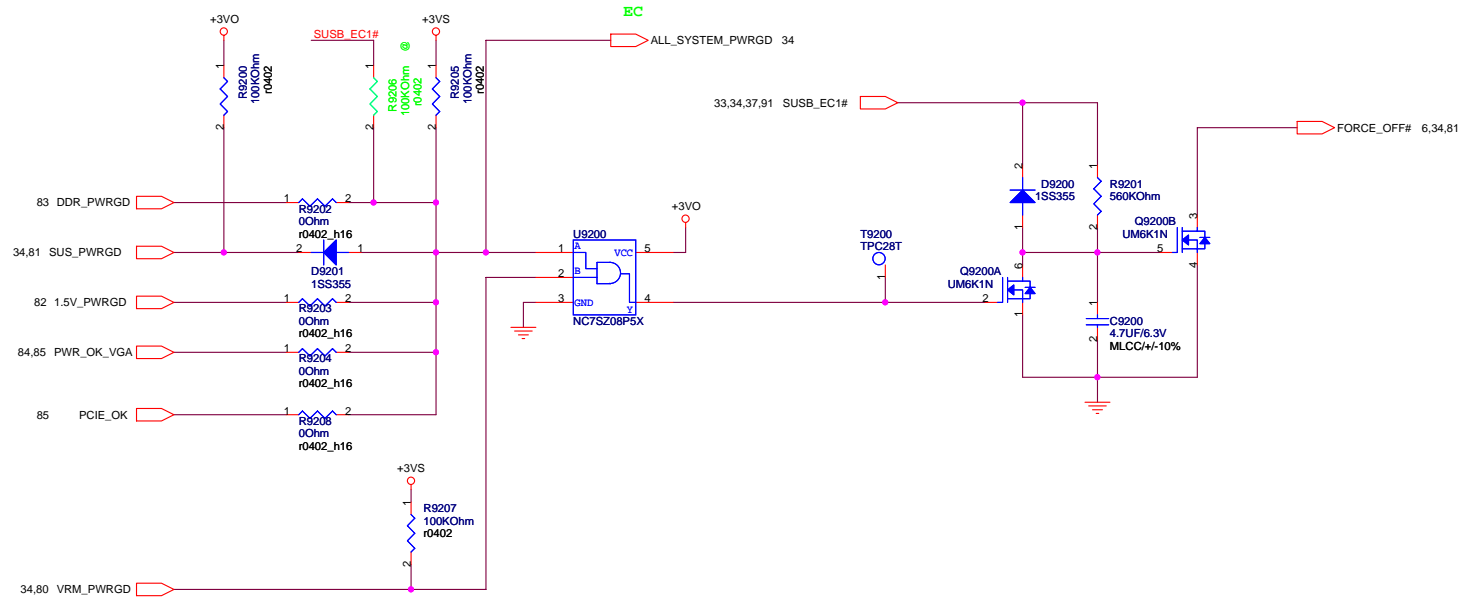
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SUSC#_PWR POWER

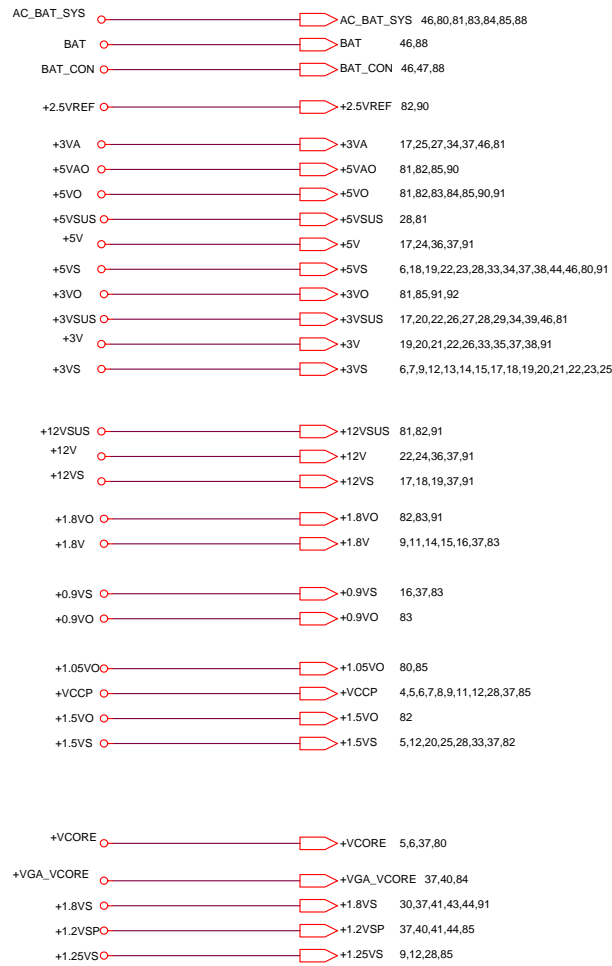


POWER GOOD DETECTER

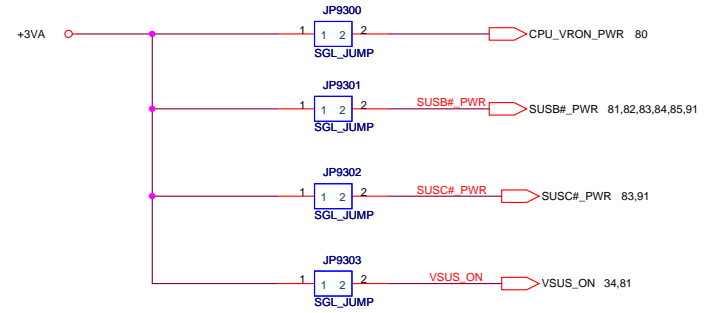


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ASUS		Title :POWER_PROTECT	
ASUSTeK COMPUTER INC. NB		Engineer: Ray	
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Custom		F6S	1.1
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FOR POWER TEST



<Variant Name>

ASUS		Title :POWER_SIGNAL	
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Custom	F6S		1.1
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