

Compal Confidential  
Model Name : V5WE2/T2 (EA/EG)  
File Name : LA-9532P

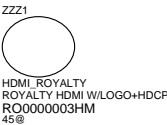
# Compal Confidential

## EA50 UMA M/B Schematics Document Intel Shark Bay ULT (Hasswell + Lynx PointLP)

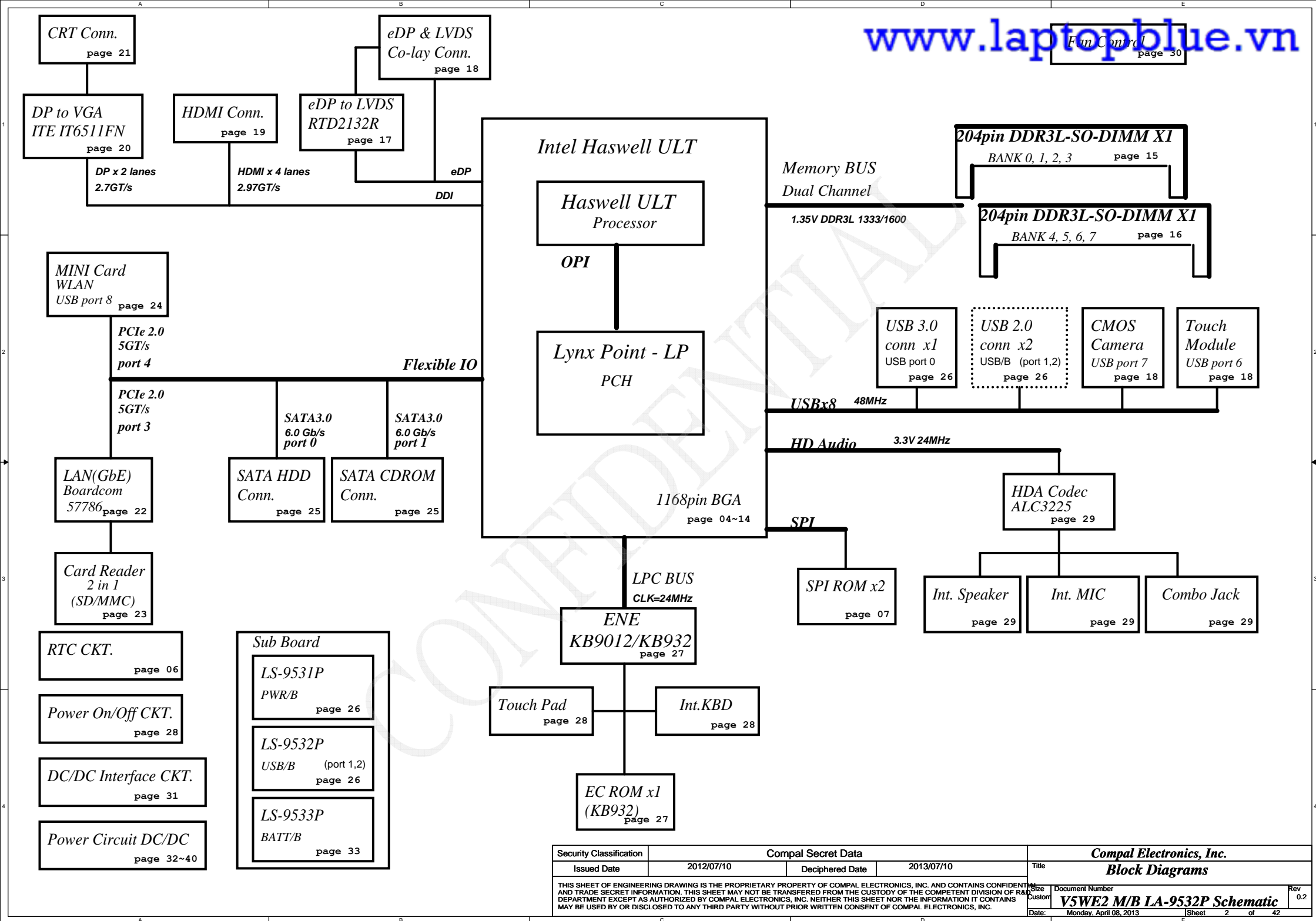
2013-04-18  
REV:1.0

ZZZ

Part Number	Description
DAZ0VR00200 V5WE2_PCB	PCB V5WE2 LA-9532P LS-9531P/9532P/9533P



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Issued Date	2012/07/10	Deciphered Date	2013/07/10	Title	Cover Page
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				V5WE2 M/B LA-9532P Schematic	0.2
				Date: Thursday, April 18, 2013	Sheet 1 of 42



[illegible]

### EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b	On Board Thermal Sensor	1001 101xb

Device			Address	
ChannelA	DIMM0	A0	1010 000X	JDIMM1(SPD)

Device			Address	
ChannelA	DIMM0	A0	1010 000X	JDIMM1(SPD)

PCB P/N	DA60000XR00 : PCB OVR LA-9532P REV0 M/B
EVT BOM config	9012@; AMIC@; CHR@; BL@; EMC@; AOAC@
DVT BOM config	9012@; BL@; EMC@; EDP@ (L01~L04)
	9012@; BL@; EMC@; TL@ (L05)
PVT BOM config	9012@; EMC@; EDP@; 1ROM@; IOAC@
PreMP BOM config	9012@; EMC@; EDP@; 1ROM@; IOAC@

43 Level	Description
4319LWBOL01	SMT MB A9532 V5WE2 UMA I7 QDA7 HDMI
4319LWBOL02	SMT MB A9532 V5WE2 UMA I5 QDJB HDMI
4319LWBOL03	SMT MB A9532 V5WE2 UMA I5 QDJ7 HDMI
4319LWBOL04	SMT MB A9532 V5WE2 UMA I5 QDJ9 HDMI
4319LWBOL05	SMT MB A9532 V5WE2 UMA I5 QDJB LVDS HDMI
4319LWBOL06	SMT MB A9532 V5WE2 UMA WO/CPU HDMI
4319LWBOL07	SMT MB A9532 V5WE2 UMA I5 QEA4 HDMI
4319LWBOL08	SMT MB A9532 V5WE2 UMA I5-4200 HDMI
4319LWBOL09	SMT MB A9532 V5WE2 UMA I3-4010 HDMI
4319LWBOL10	SMT MB A9532 V5WE2 UMA I5-4250 HDMI
4319LWBOL21	SMT MB A9532 V5WC2 UMA I5-4200 HDMI
4319LWBOL22	SMT MB A9532 V5WC2 UMA I3-4010 HDMI

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VAL#	+ GND	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	V <sub>AD_BID</sub> min	V <sub>AD_BID</sub> typ	V <sub>AD_BID</sub> max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

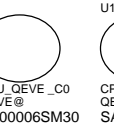
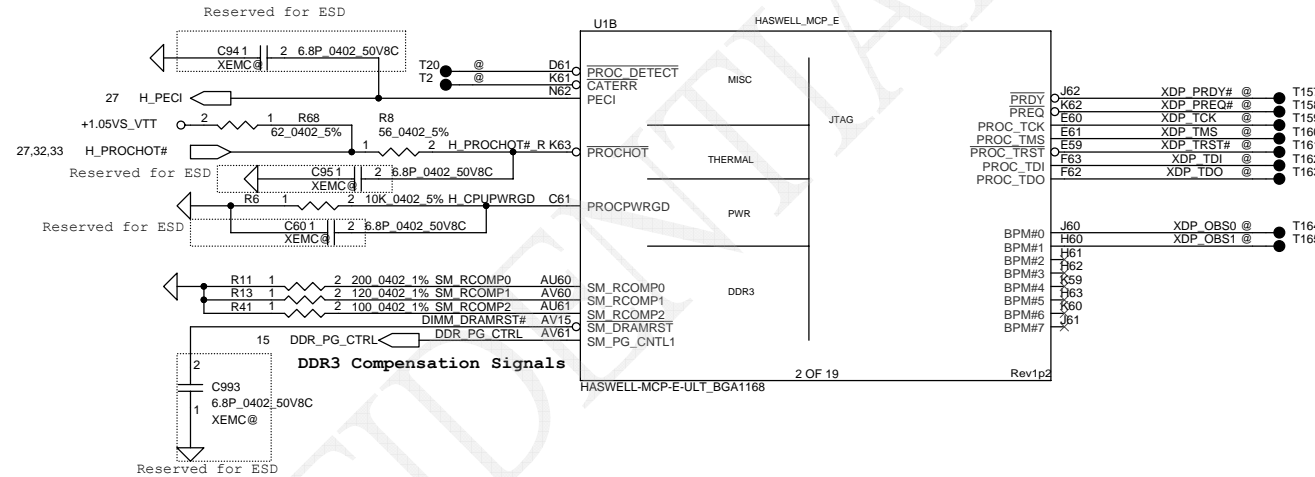
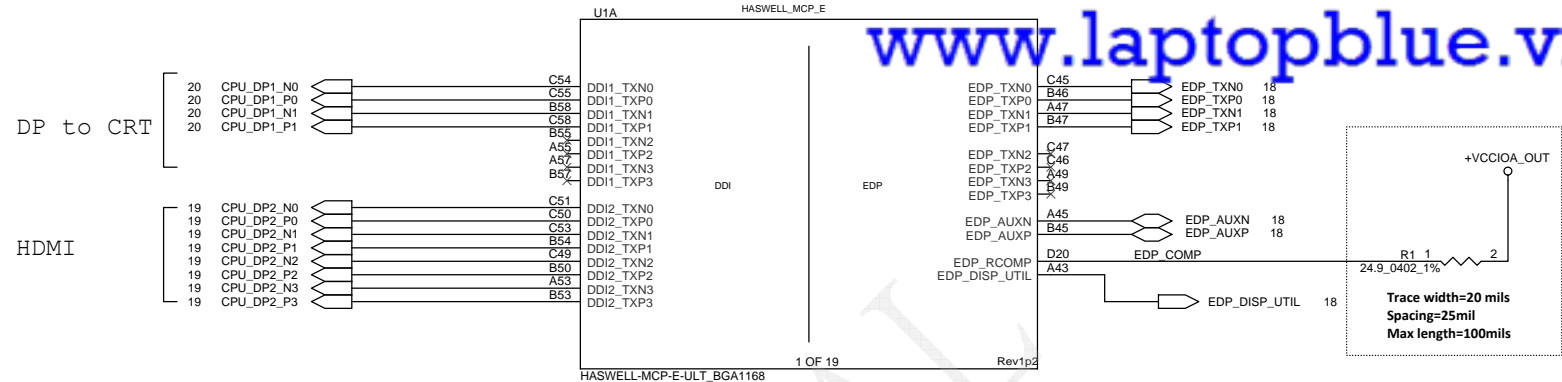
Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	1.0
5	
6	
7	

USB 3.0	Port	
XHCI	1	USB Port(Left 3.0)
	2	
	3	
	4	

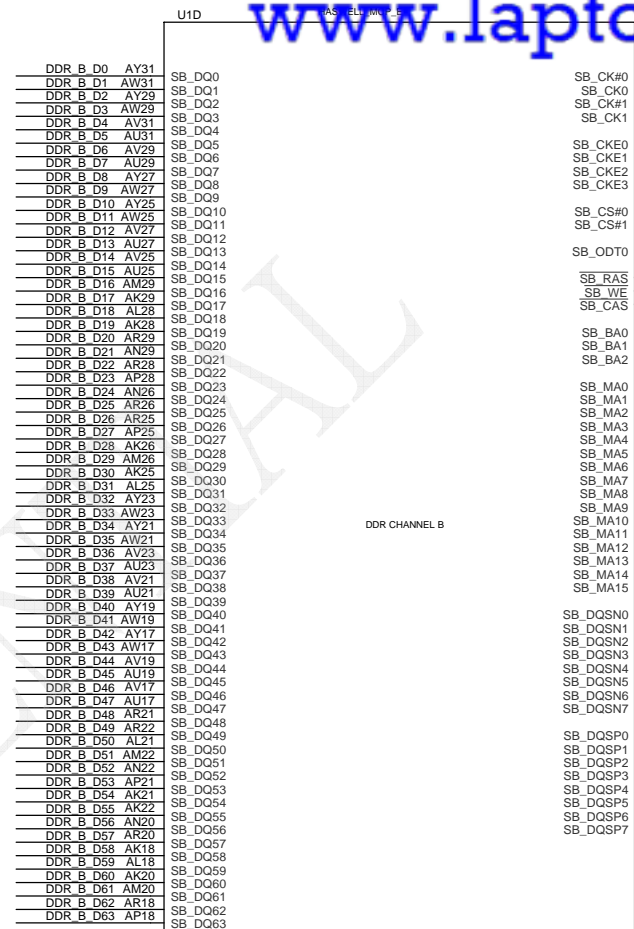
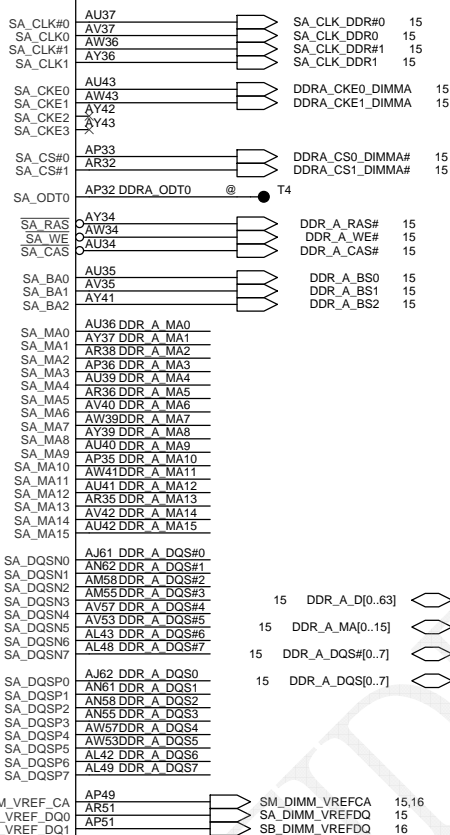
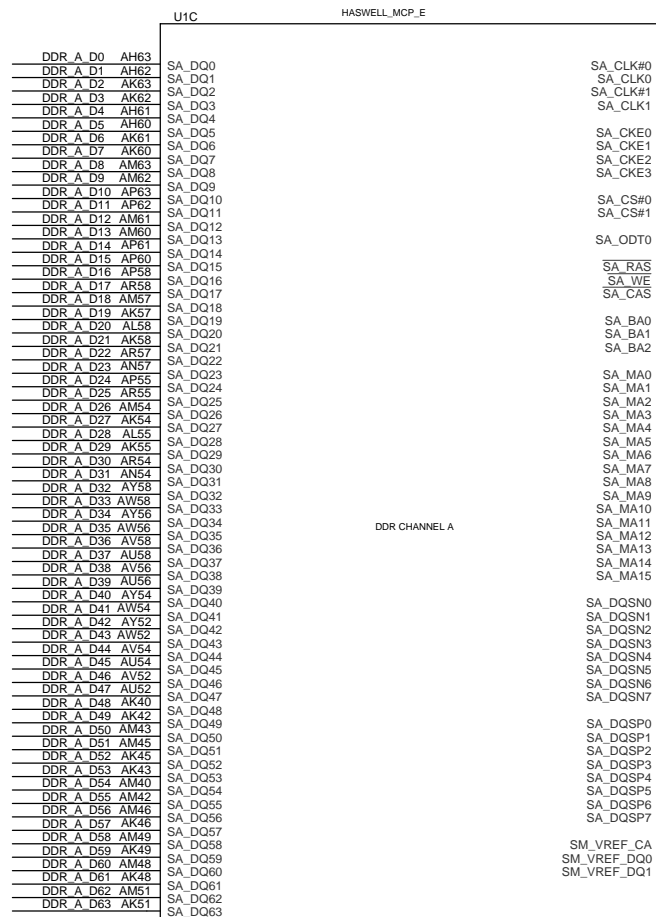
USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB Port(Left 3.0)
		1	USB Port(Right 2.0)
	UHCI1	2	USB Port(Right 2.0)
		3	
	UHCI2	4	Mini Card(WLAN)
		5	
	UHCI3	6	Touch Screen
7		Camera	

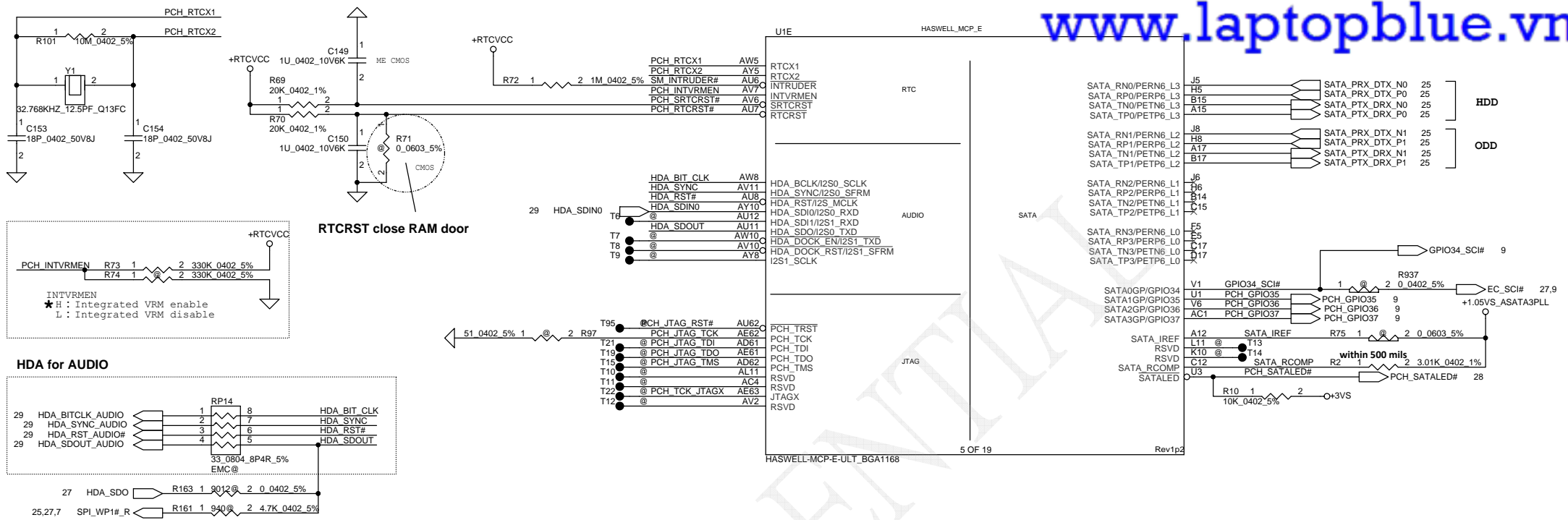
BTO Option Table	
BTO Item	BOM Structure
EC 9012	9012@
EC 940	940@
Unpop	@
TPM Circuit	TPM@
eDP mode	EDP@
eDP to LVDS	TL@
Connector	CONN@
G-Sensor	GSEN@
XDP (Debug Port)	XDP@
KB Backlight	BL@
Debug Only	DEG@
MEC requirement	EMC@
MEC requirement unpop	XEMC@
GPU_Select	VGA@
reserve 3,5V MOS	35V@
BIOS 8M Solution	1ROM@
BIOS 4+2M Solution	2ROM@
IOAC Function	IOAC@
Touch screen Function	TS@

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					Date: Friday, April 12, 2013	Sheet 3 of 42	0.2
					V5WE2 M/B LA-9532P Schematic		

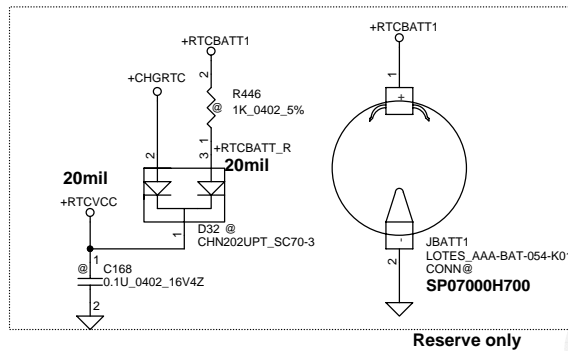


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Customer		V5WE2 M/B LA-9532P Schematic		0.2	
Date:		Friday, April 12, 2013		Sheet 4 of 42	

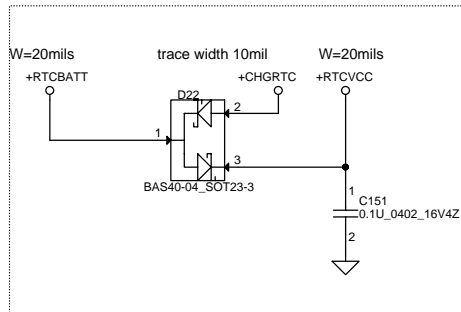




## ME Debug



Reserve only



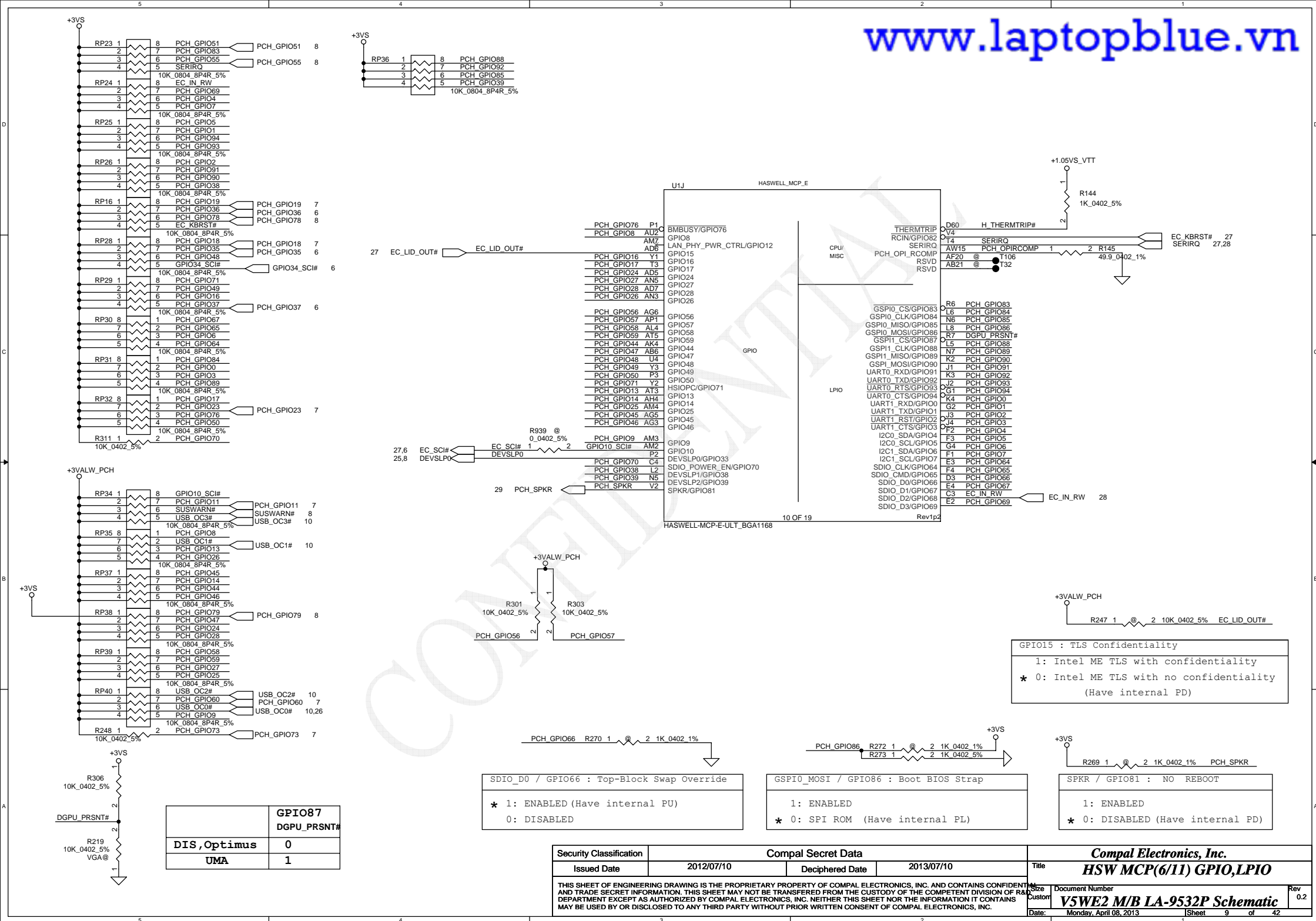
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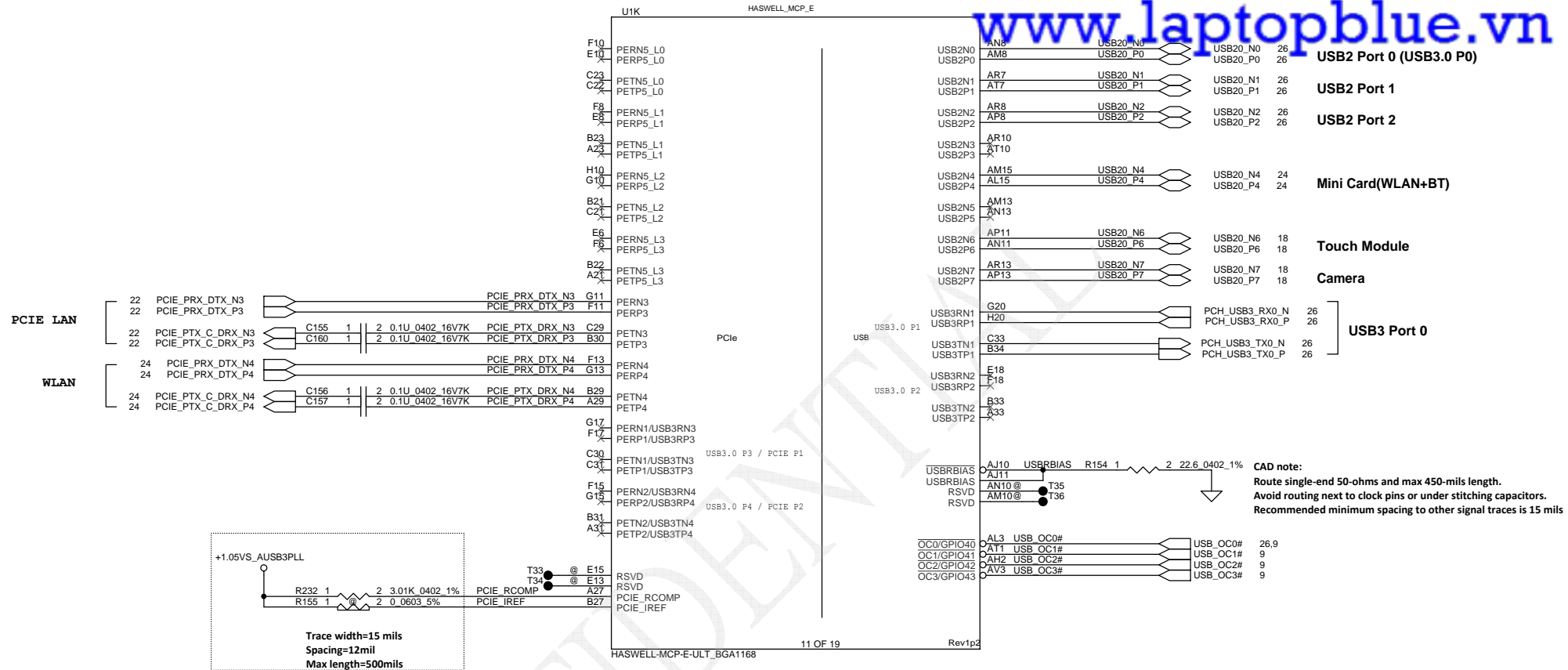




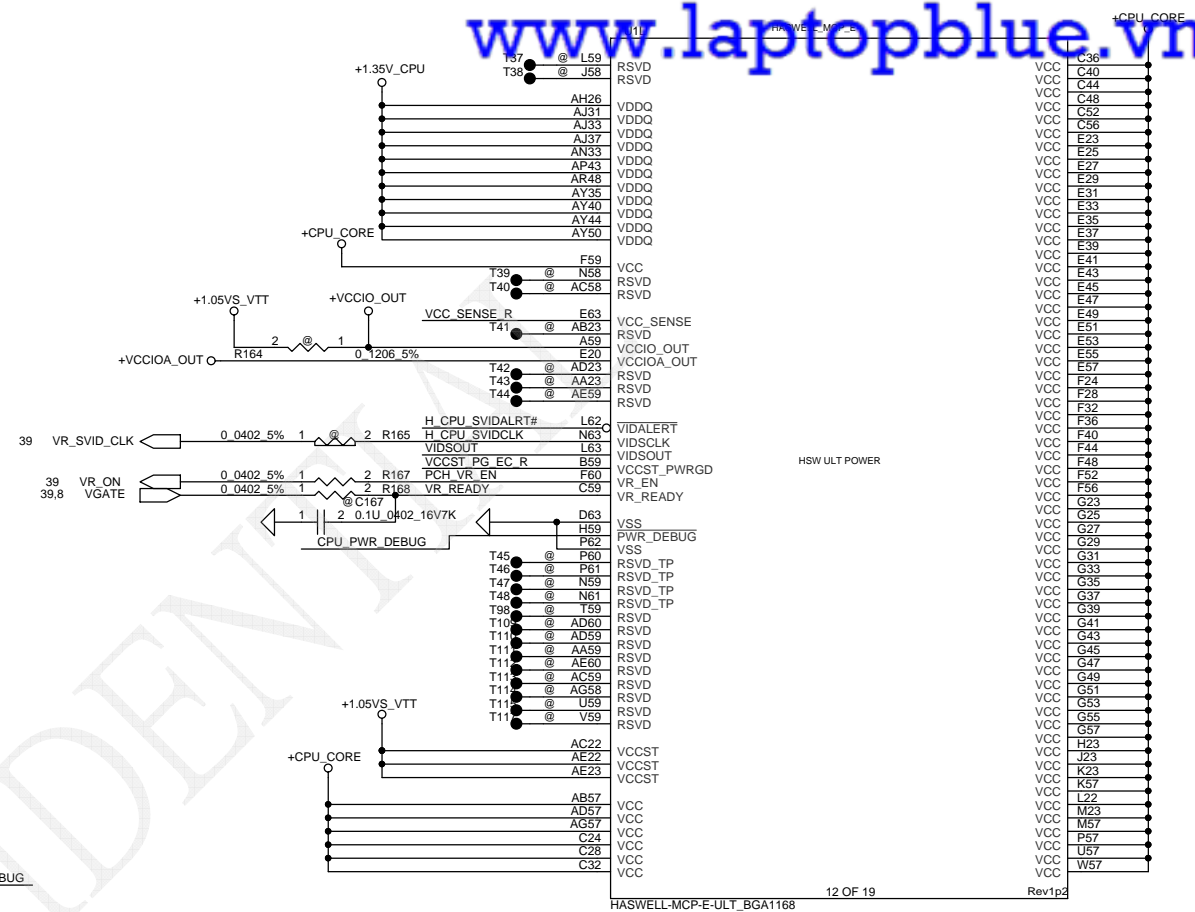
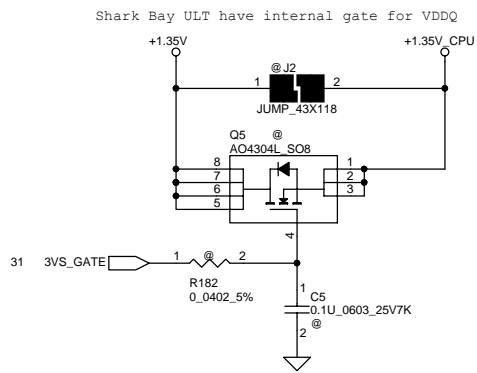
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				Customer	<b>V5WE2 M/B LA-9532P Schematic</b>	0.2
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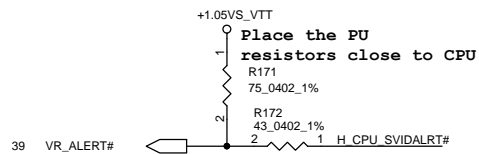




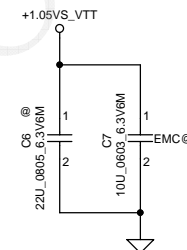
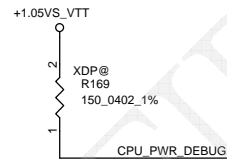
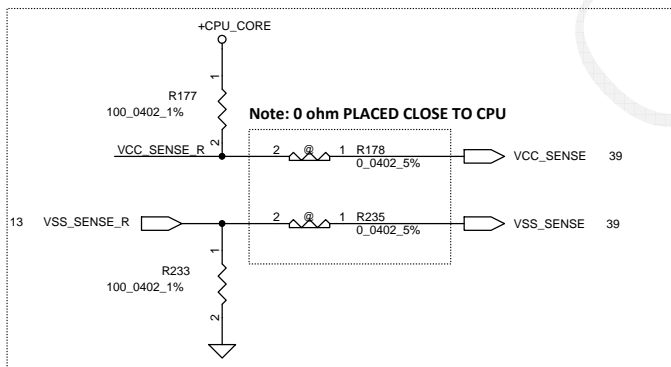
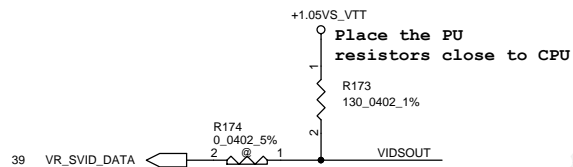
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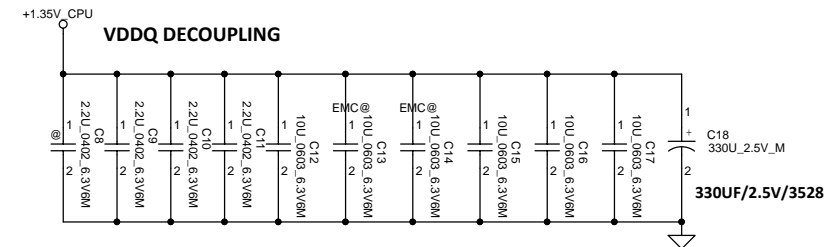
**SVID ALERT**



## SVID DATA



## VDDQ DECOUPLING

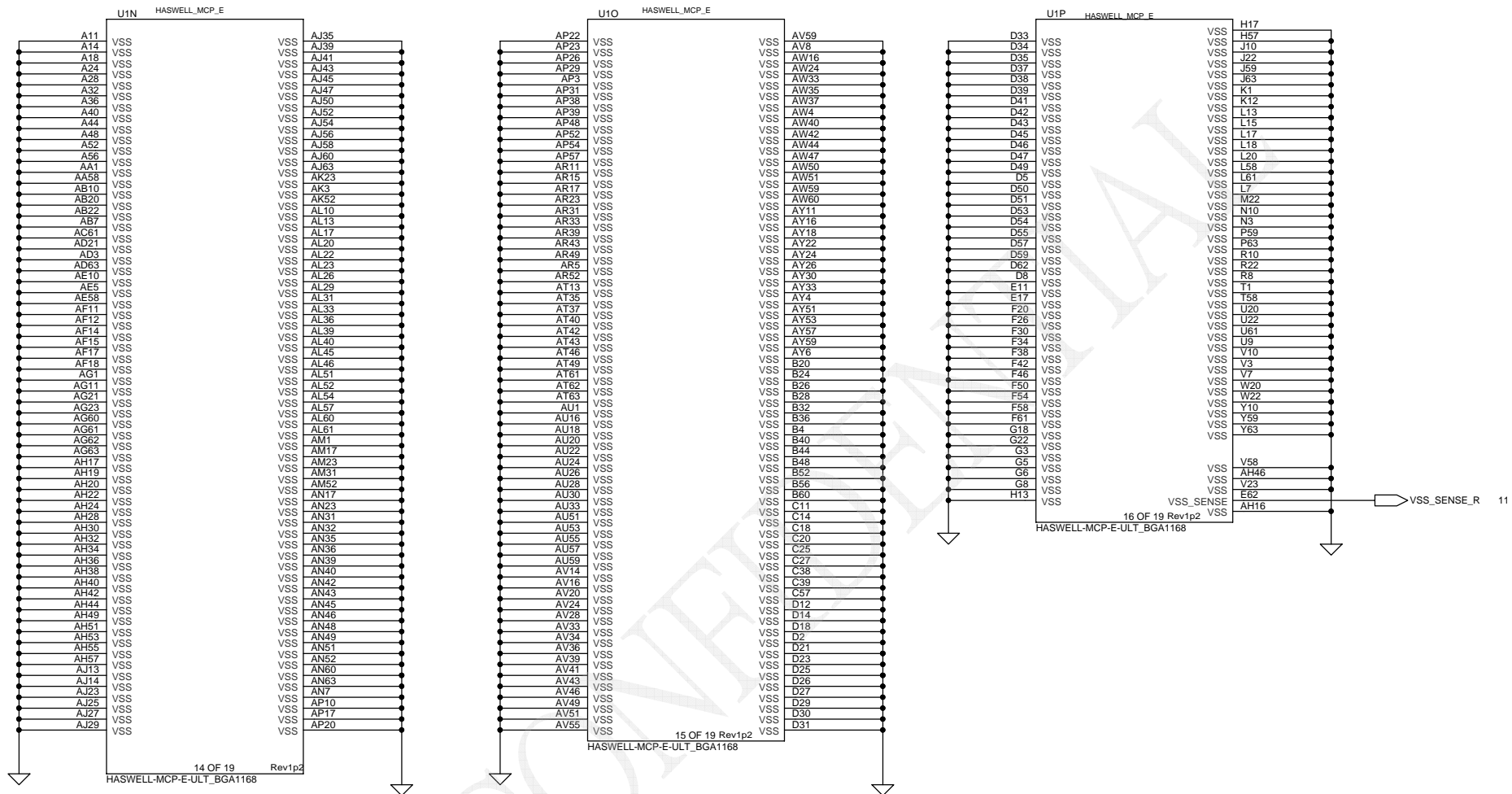


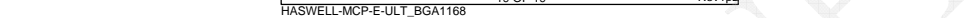
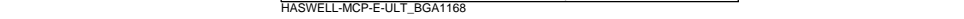
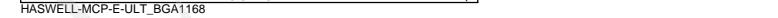
```
+1.35V : 470UF/2V/7343 *2
          10UF/6.3V/0603 * 6
          2.2UF/6.3V/0402 * 4
```

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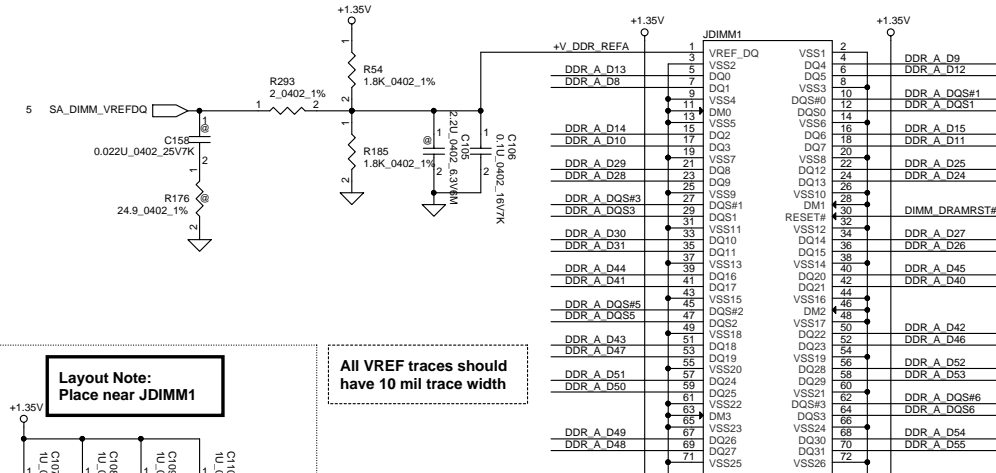




### CFG Straps for Processor

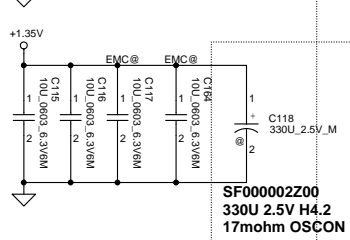
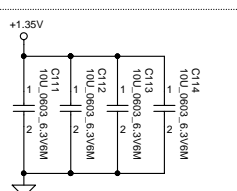
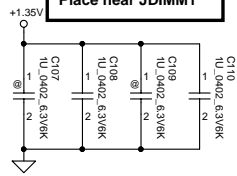
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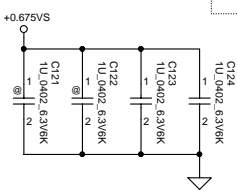


**Layout Note:**  
Place near JDIMM1

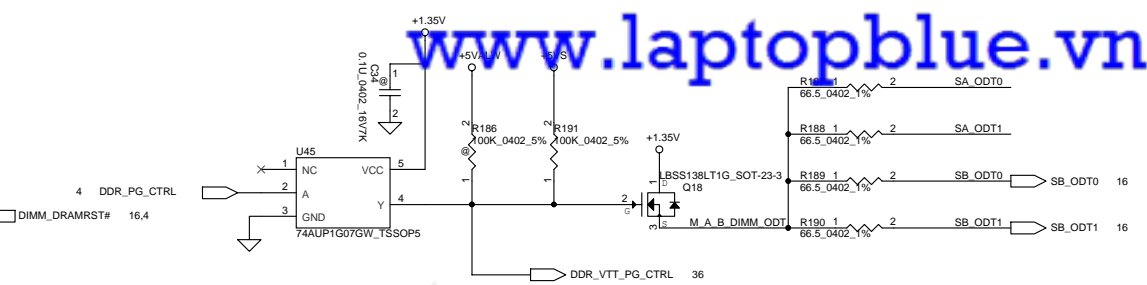
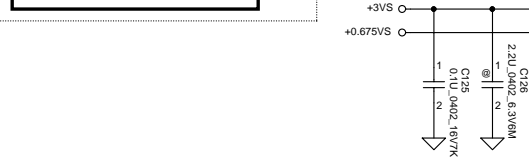
**All VREF traces should have 10 mil trace width**







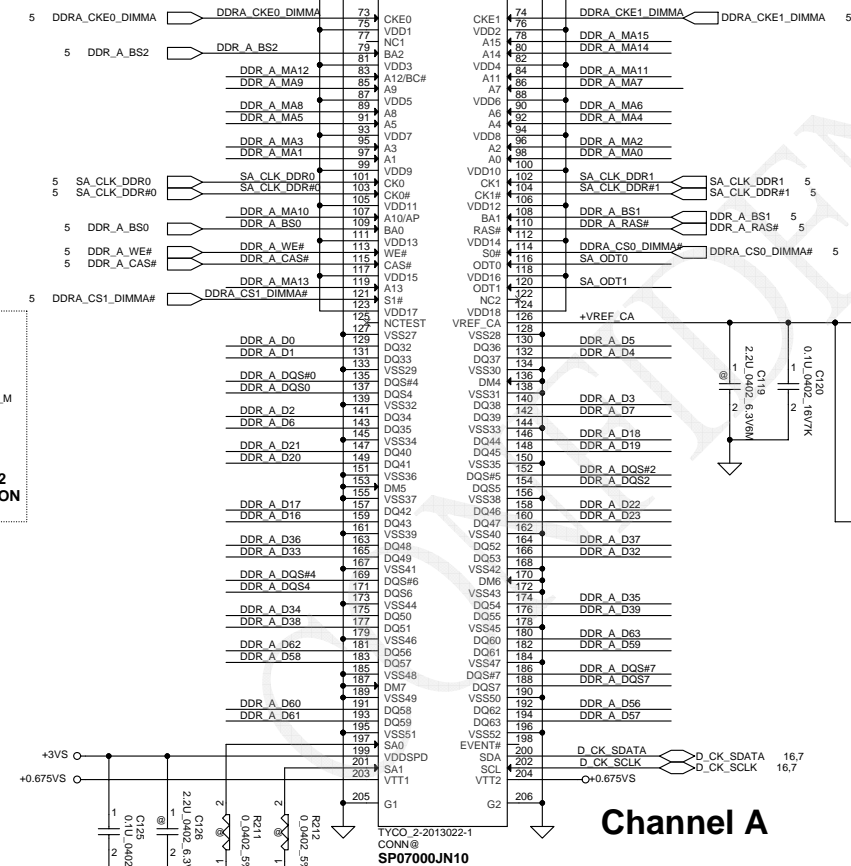
SF000002Z00  
330U 2.5V H4.2  
17mohm OSCON



**Layout Note:**  
Place near JDIMM1.203,204

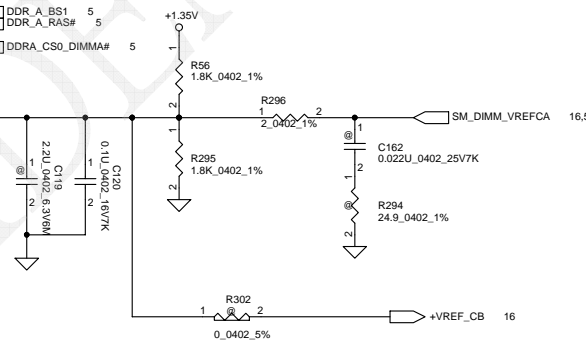


	DDR_A_DQS#[0..7]	5
	DDR_A_DQS[0..7]	5
	DDR_A_D[0..63]	5
	DDR_A_MA[0..15]	5

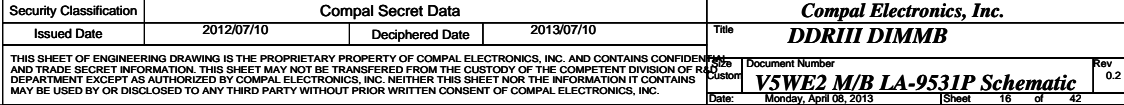


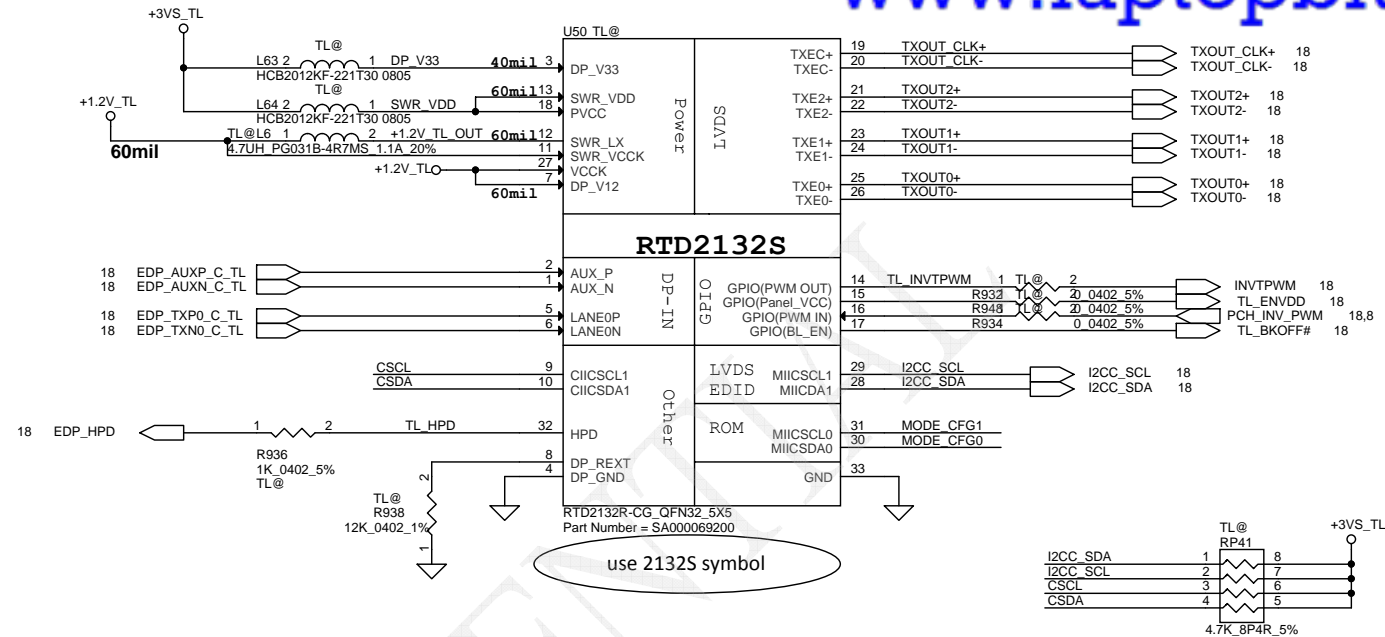
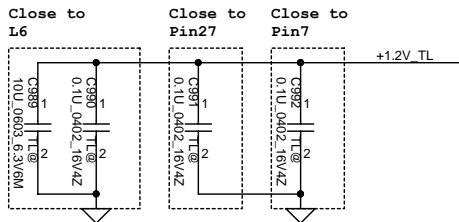
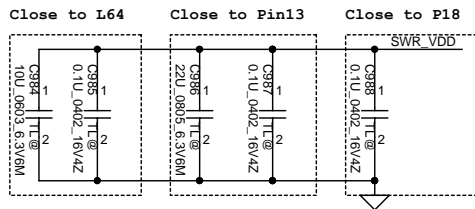
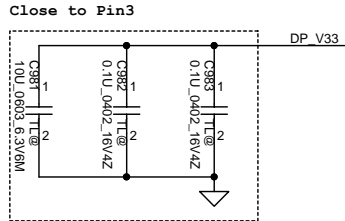
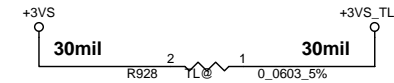
## Channel A

**<Address: SA1:SA0=00>**  
**DIMM\_1 STD H:4mm**



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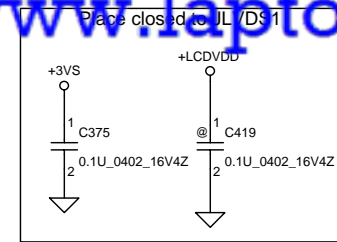
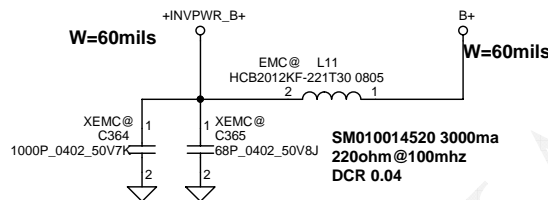
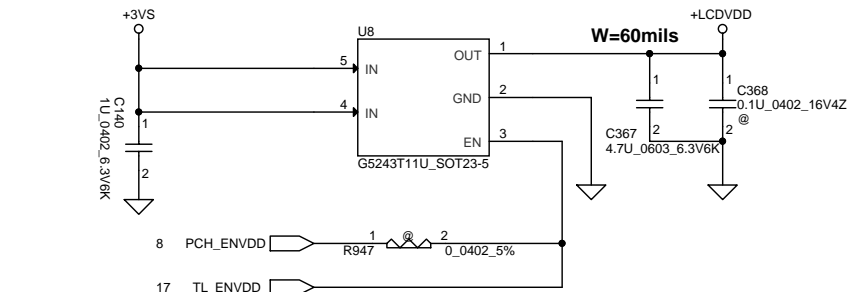


MODE_CFG0(PIN30)		
	0	1
MODE_CFG1(PIN31)	0	X
	1	ROM ONLY MODE
		EEPROM MODE

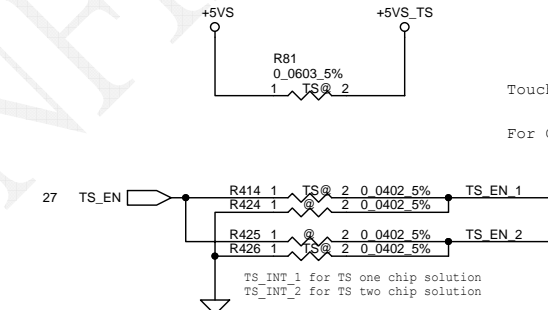
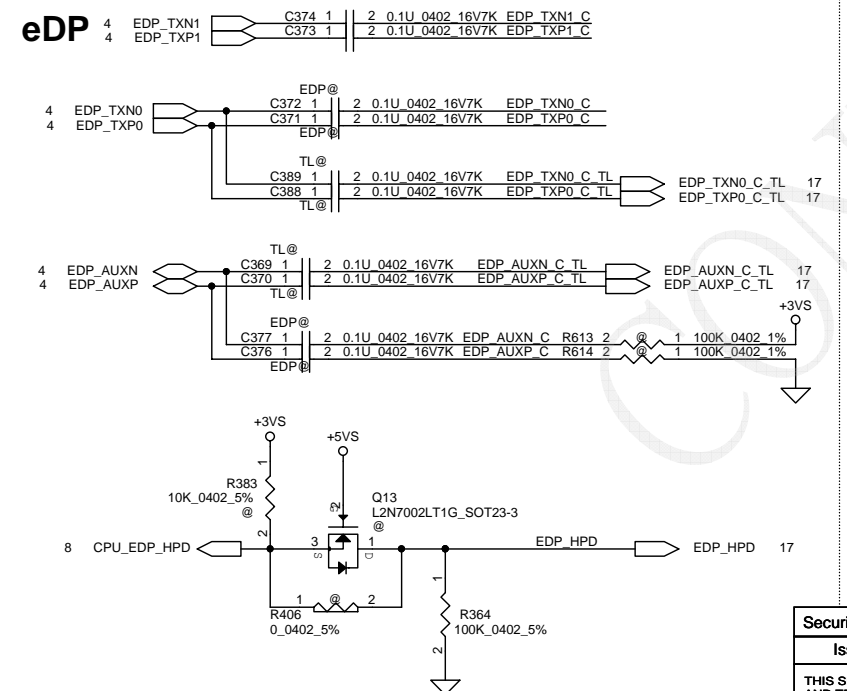
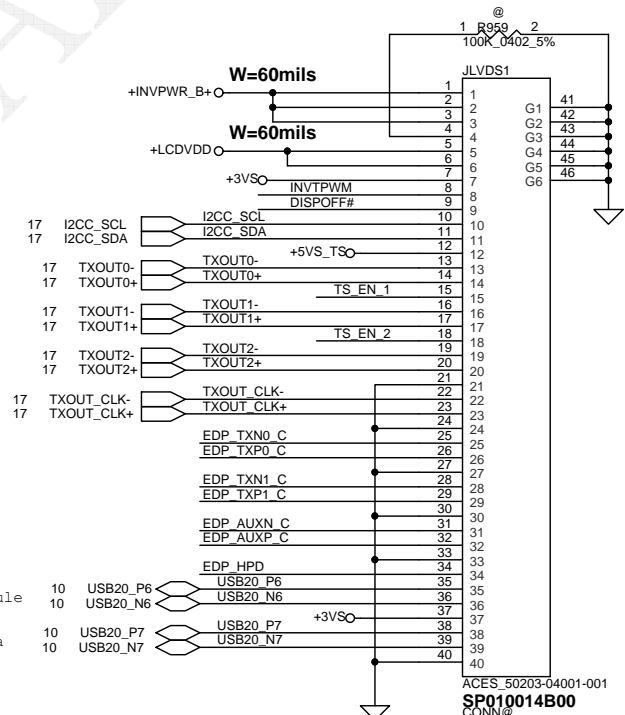
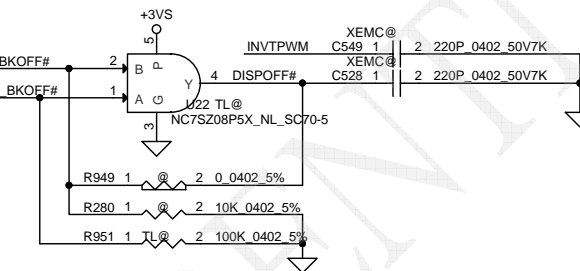
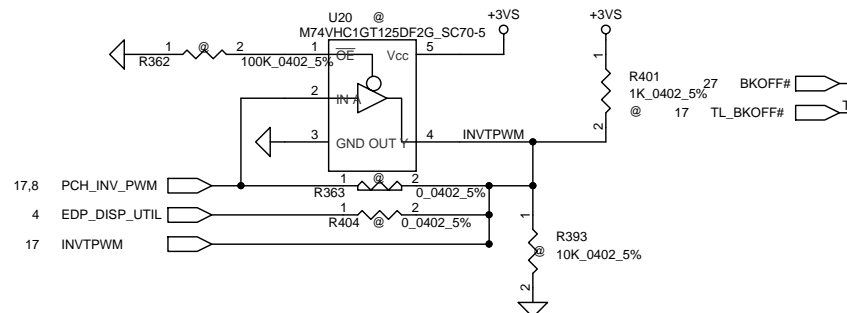
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				LVD5 Translator - RTD2132R			
				Document Number			Rev
				V5WE2 M/B LA-9532P Schematic			0.2
Date: Monday, April 08, 2013				Sheet	17	of	42

# LCD POWER CIRCUIT

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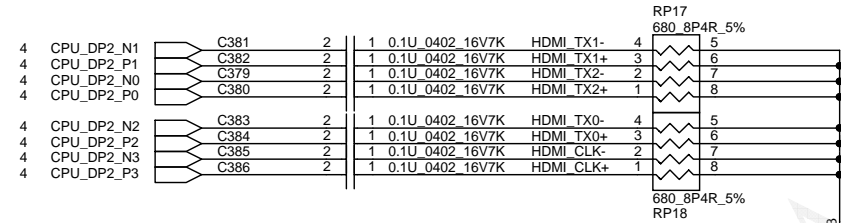
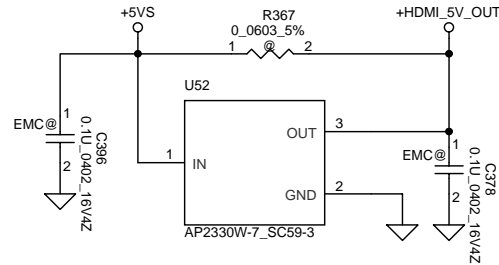


## LCD/ LED PANEL Conn.

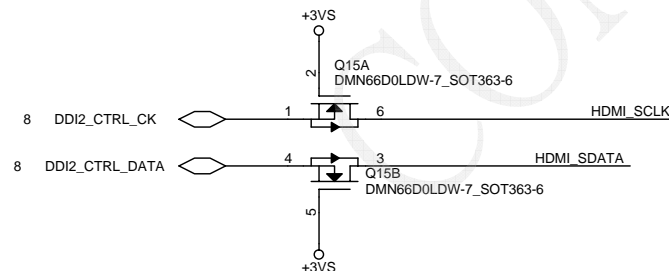
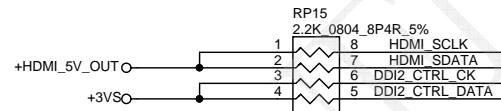
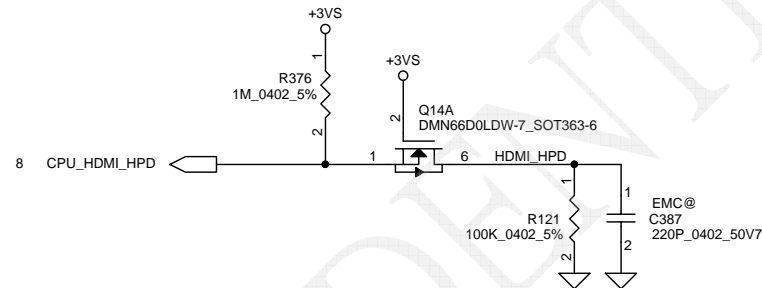
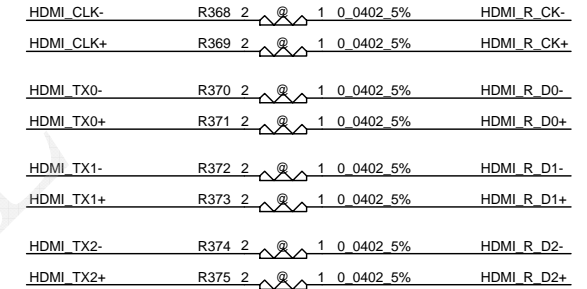


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				Date:	Monday, April 08, 2013
				Sheet	18 of 42

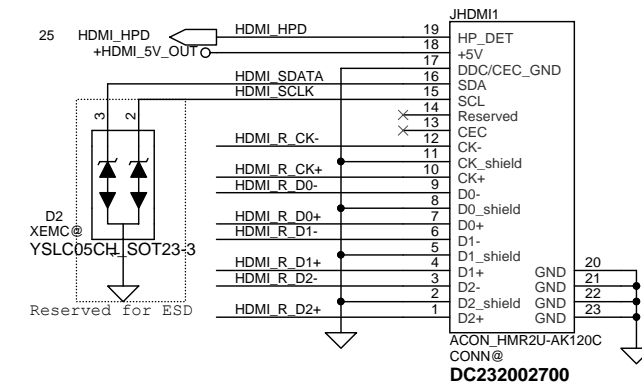
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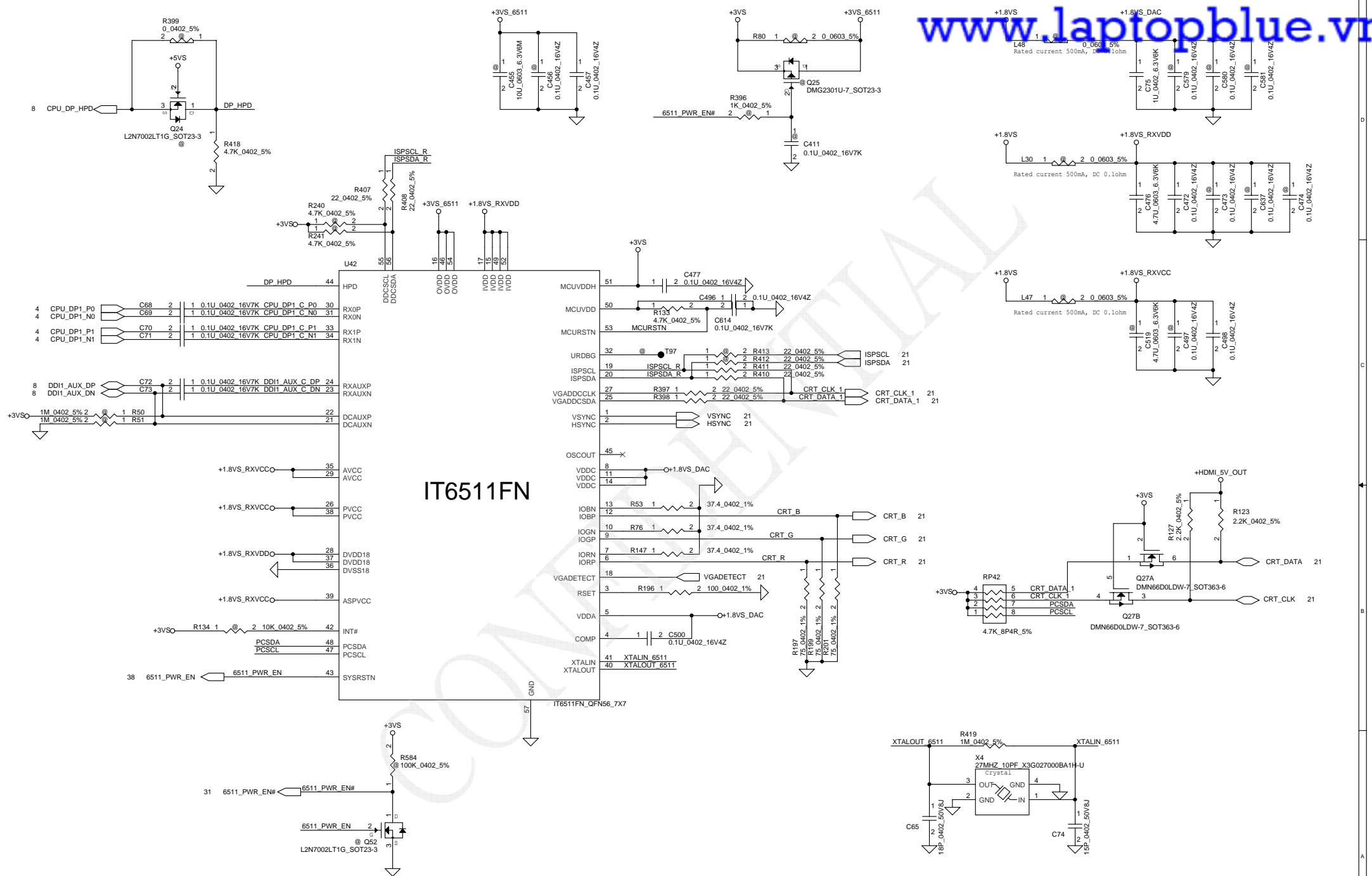
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## HDMI connector

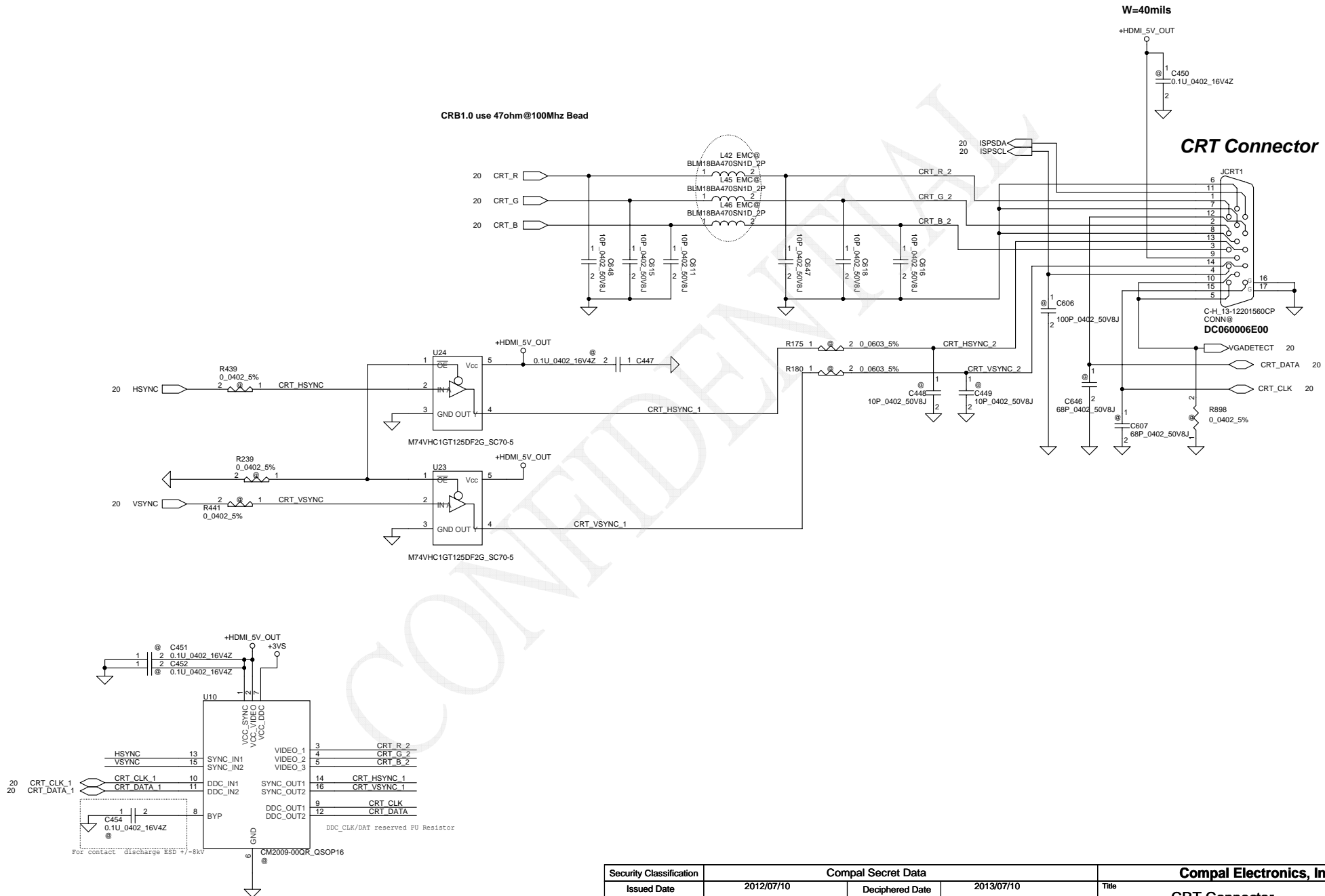


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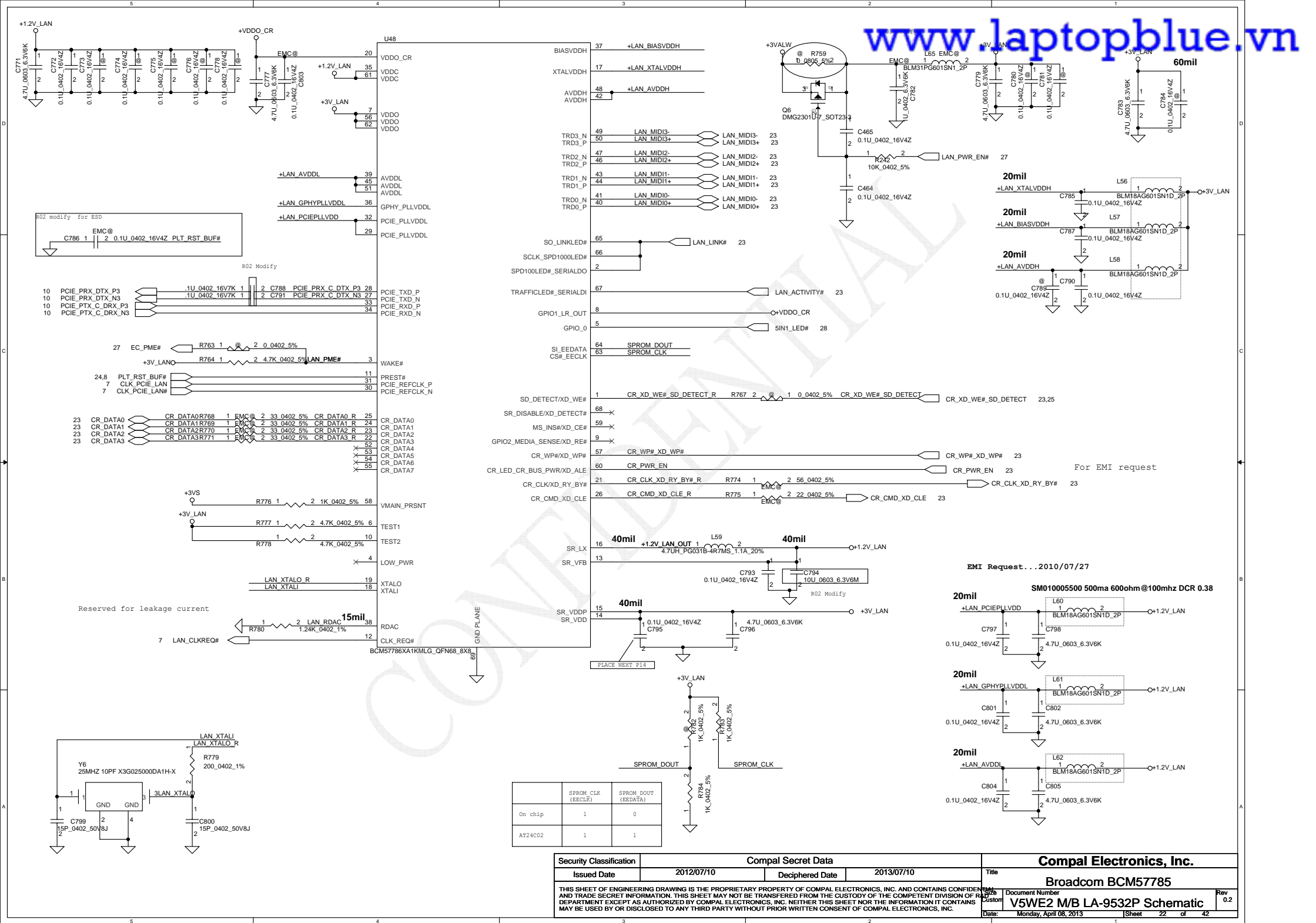


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				V5WE2 M/B LA-9532P Schematic	
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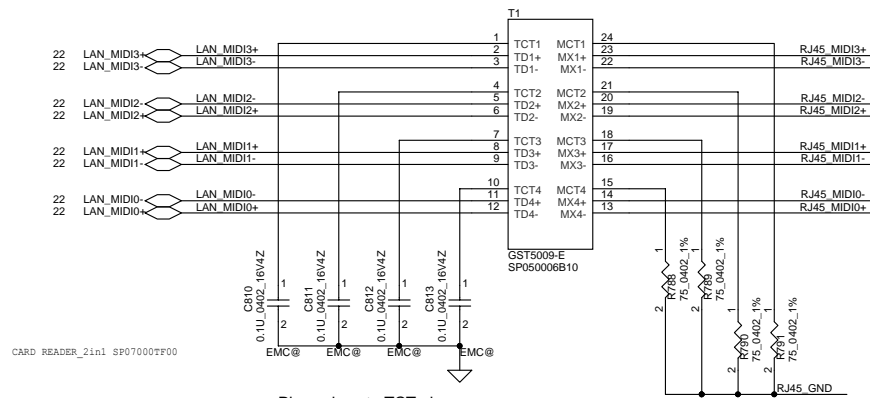




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						Customer		Document Number		Rev	
						Date		V5WE2 M/B LA-9532P Schematic		0.2	
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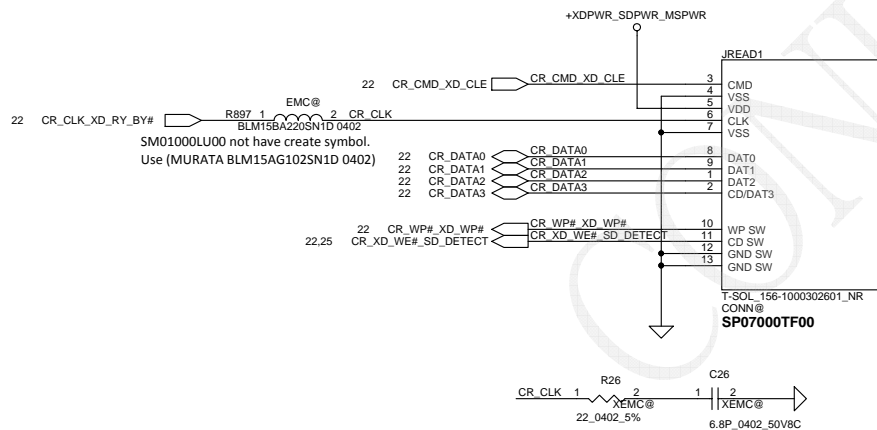
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Issued Date	2012/07/10	Deciphered Date	2013/07/10	Doc Number	Rev 0.2
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Date: Monday, April 08, 2013				Sheet 22 of 42	



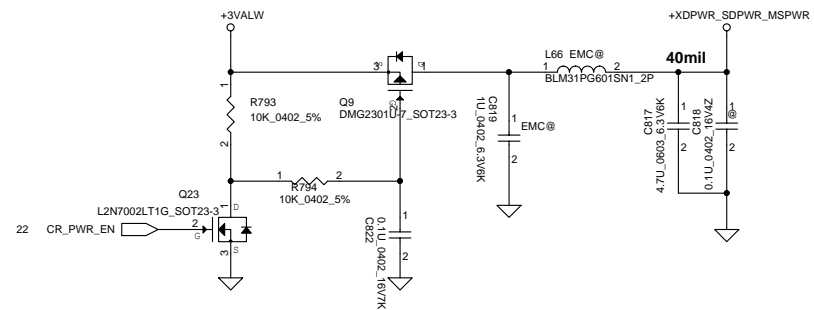
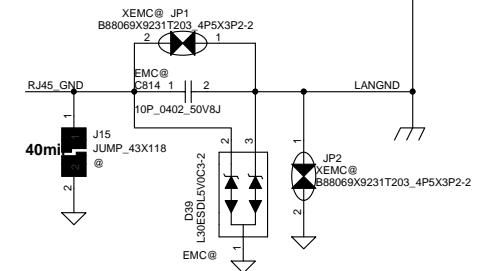
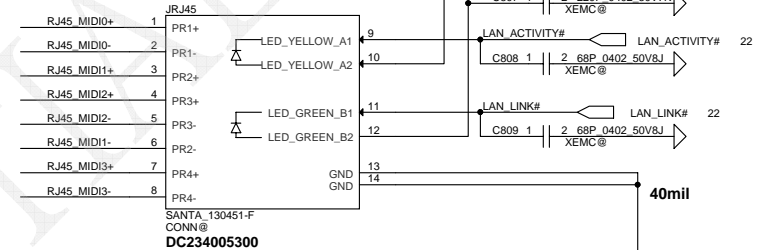
Place close to TCT pin

BOTTHAND: S X'FORM\_ GST5009-E LF LAN, SP050006B10  
TIMAG:S X'FORM\_ IH-160 LAN , SP050006F00

## Card Reader Connector



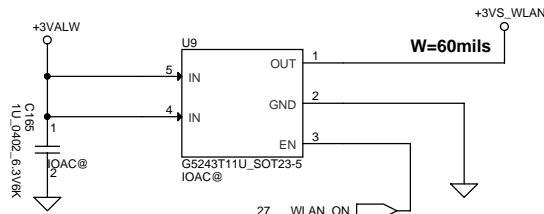
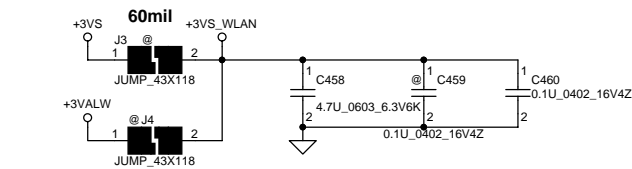
## LAN Connector



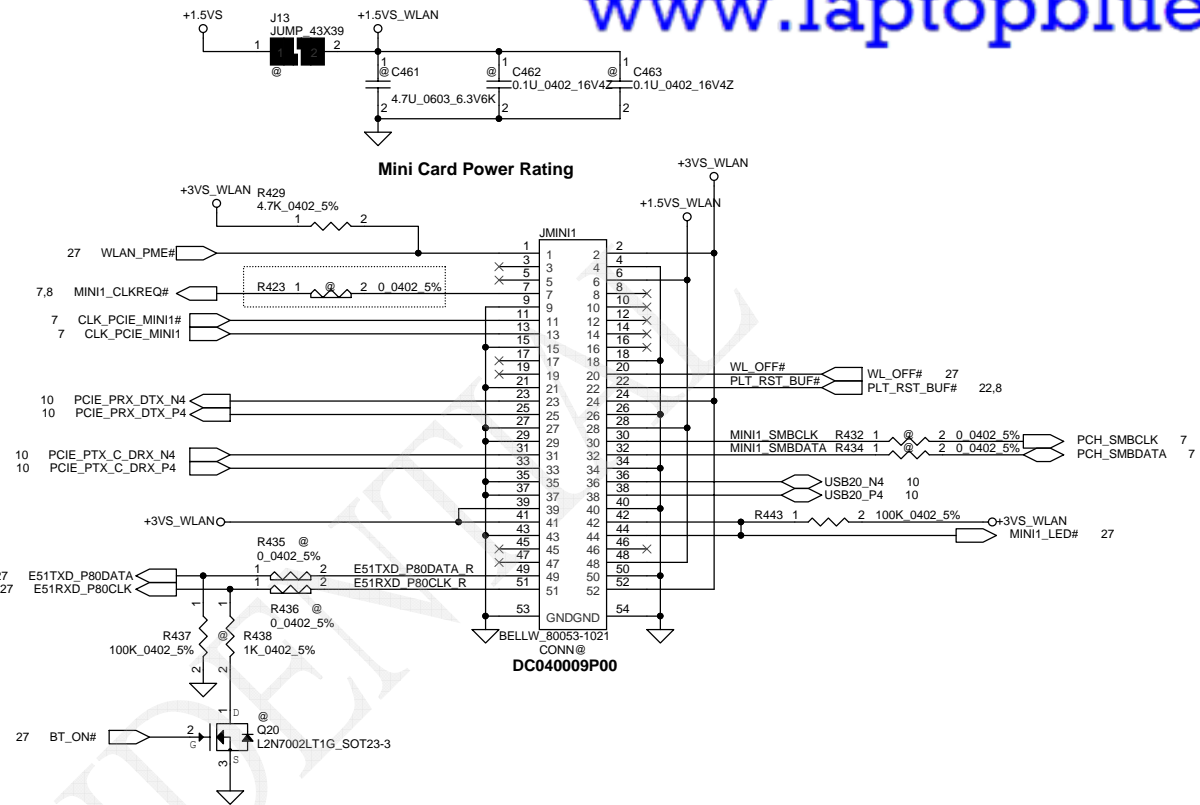
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				LAN Magnetic & RJ45			
				Document Number			
				V5WE2 M/B LA-9532P Schematic			
				Rev 0.2			
Date:		Monday, April 08, 2013		Sheet		23 of 42	

# For Wireless LAN

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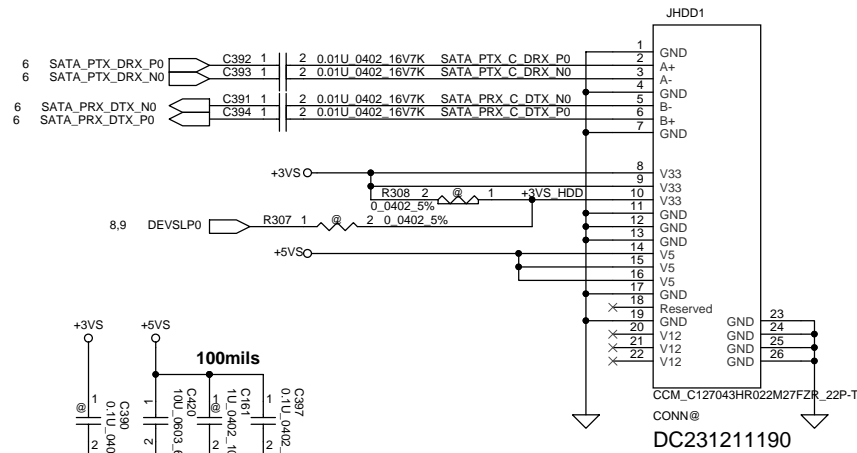


For DVT2 verify IOAC function

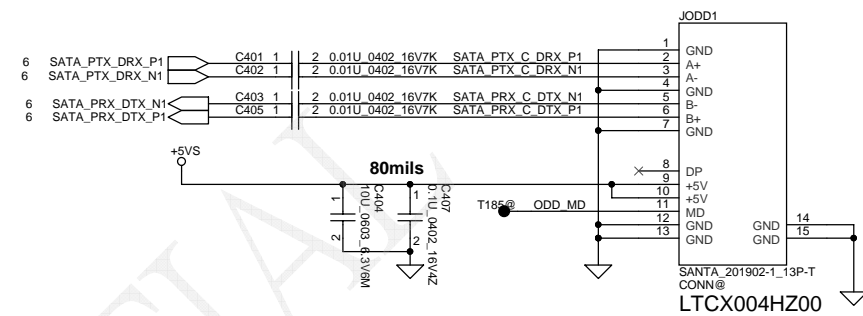


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Date: Monday, April 08, 2013		Sheet 24 of 42		Rev 0.2	

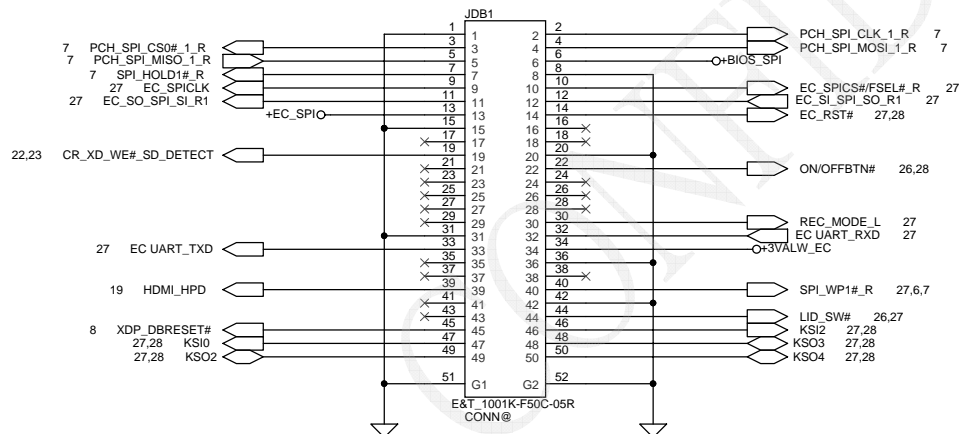
## SATA HDD1 Conn.



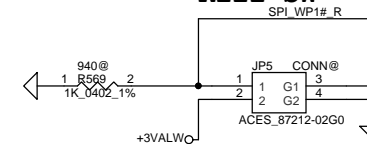
## SATA ODD Conn.



## Debug Board

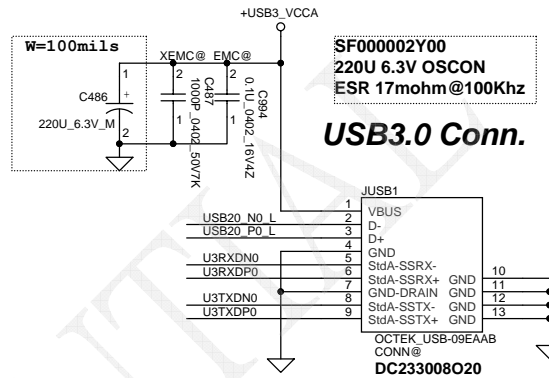
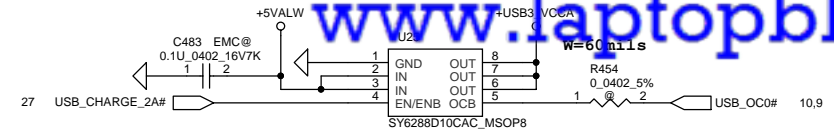
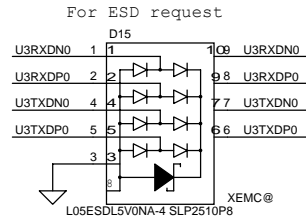
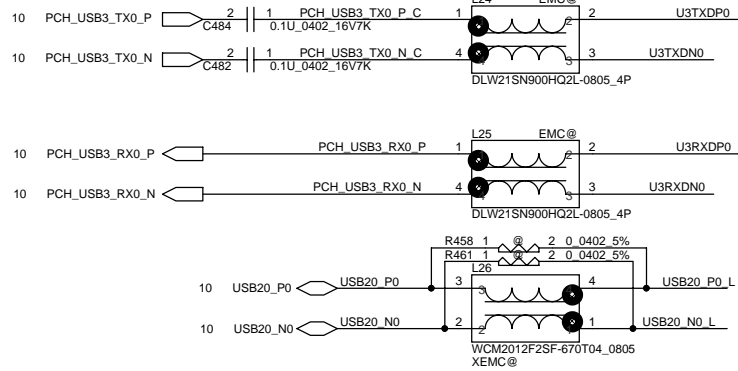


## Kill SW

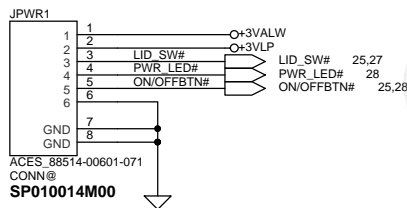


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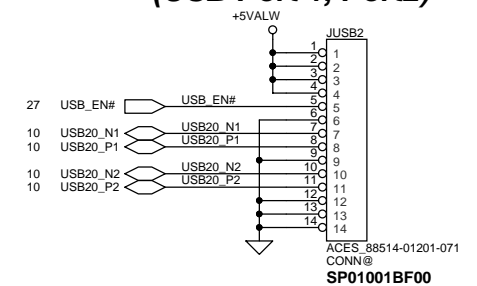
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## PWR/B

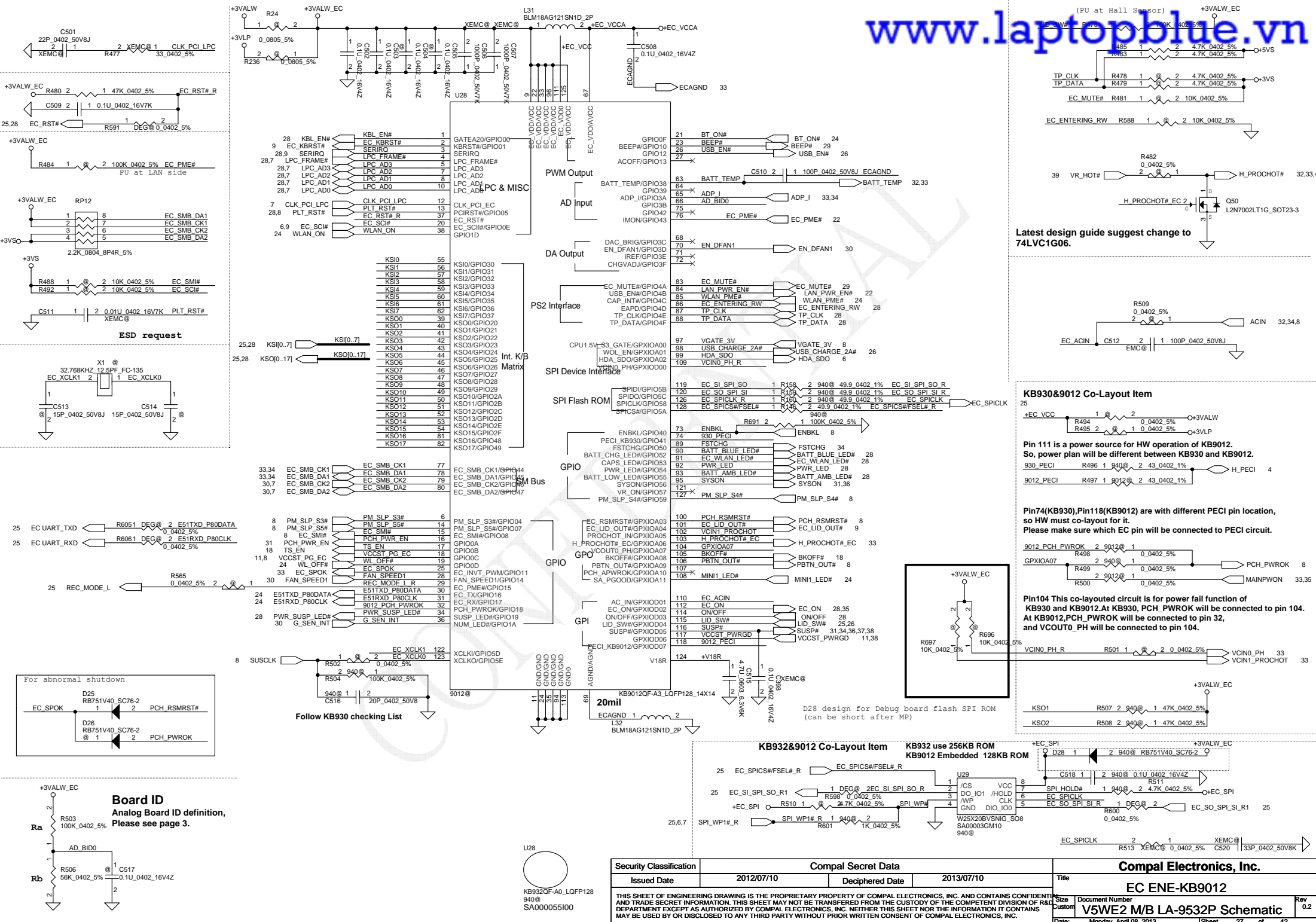


## USB/B (USB Port 1, Port2)



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Latest design guide suggest change to 74LVC1G06.

KB930&9012 Co-Layout Item

Pin 111 is a power source for HW operation of KB9012. So, power plan will be different between KB930 and KB9012.

Pin74(KB930),Pin118(KB9012) are with different PECL pin location, so HW must co-layout for it. Please make sure which EC pin will be connected to PECL circuit.

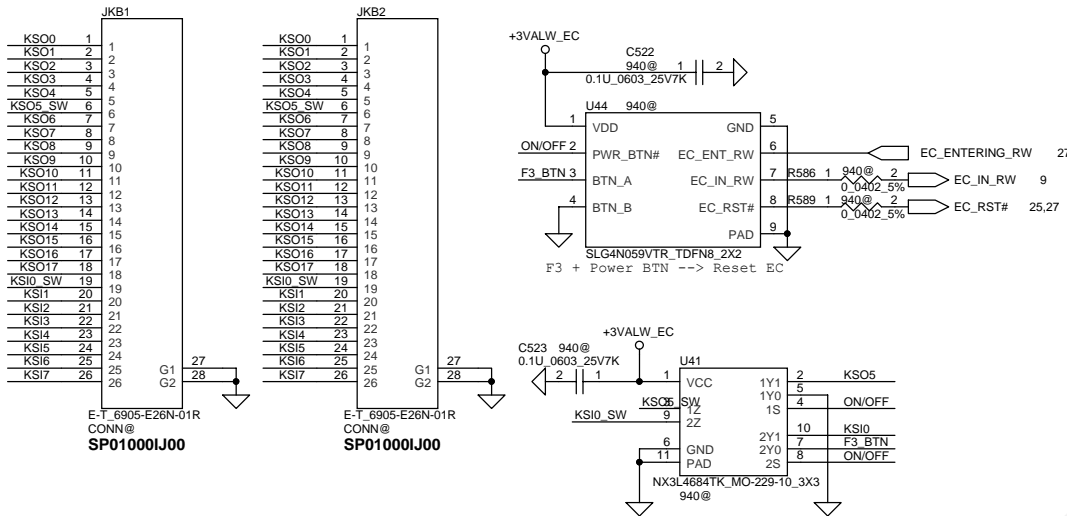
Pin104 This co-layouted circuit is for power fail function of KB930 and KB9012. At KB930, PCH\_PWROK will be connected to pin 104. At KB9012, PCH\_PWROK will be connected to pin 32, and VCOUT0\_PH will be connected to pin 104.

KB932&9012 Co-Layout Item

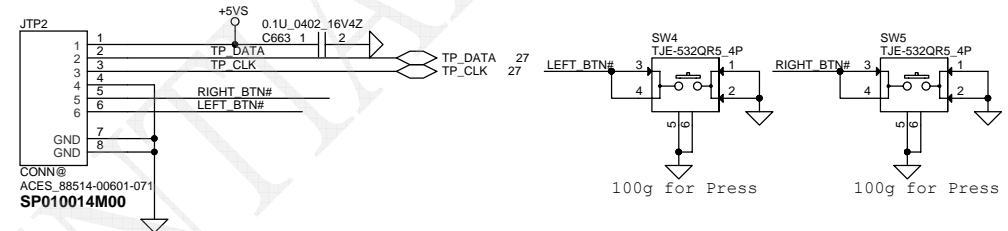
KB932 use 256KB ROM  
KB9012 Embedded 128KB ROM

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				V5WE2 M/B LA-9532P Schematic	0.2
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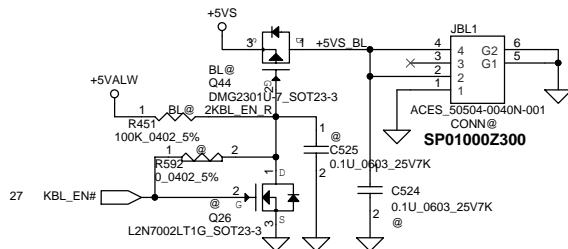
## KB Conn.



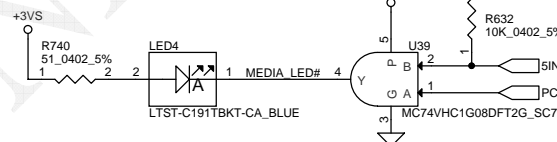
## To TP/B Conn.



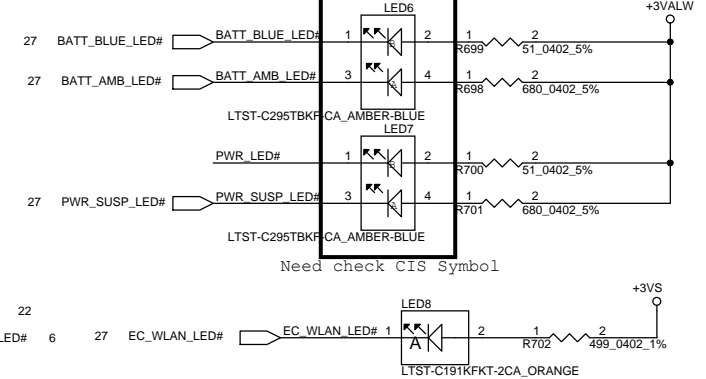
## KB BackLight Conn.



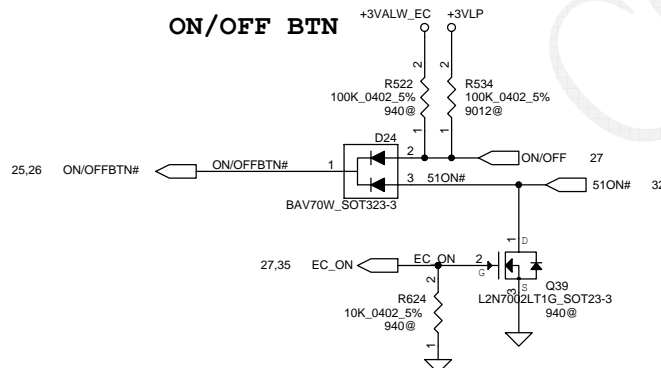
## HDD LED



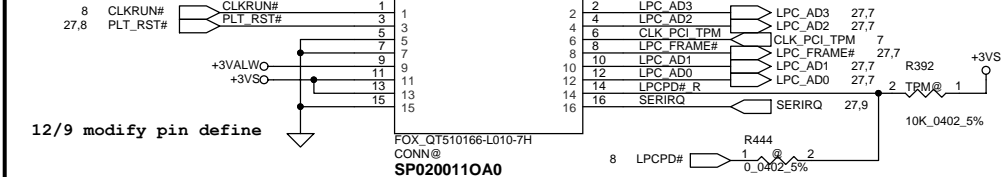
## LED



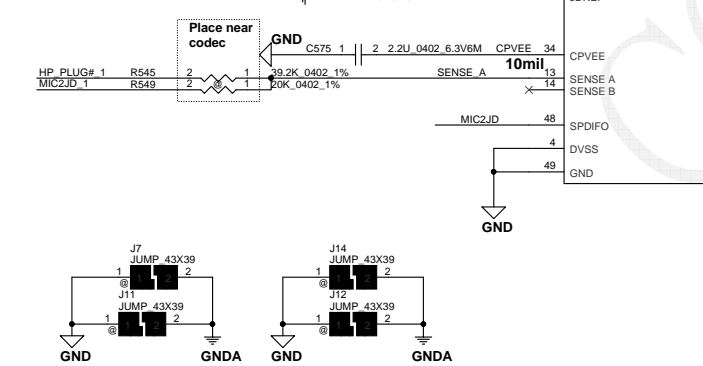
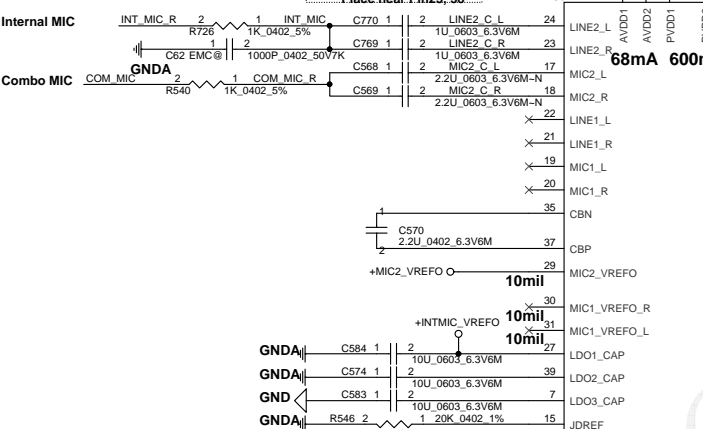
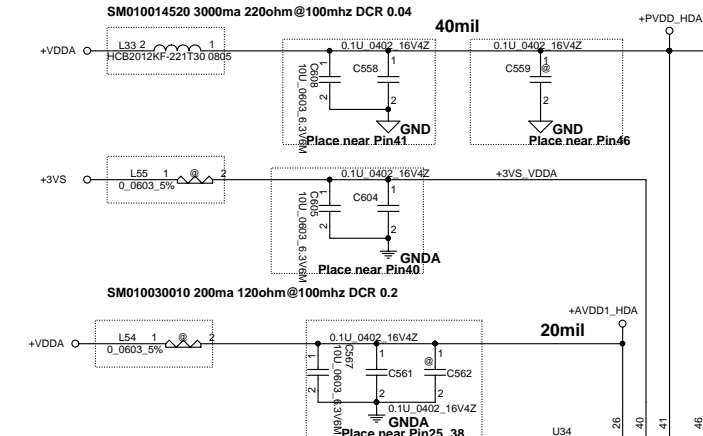
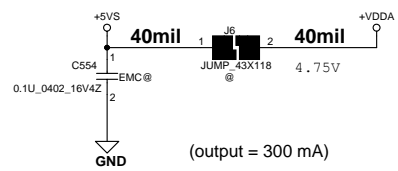
## ON/OFF BTN



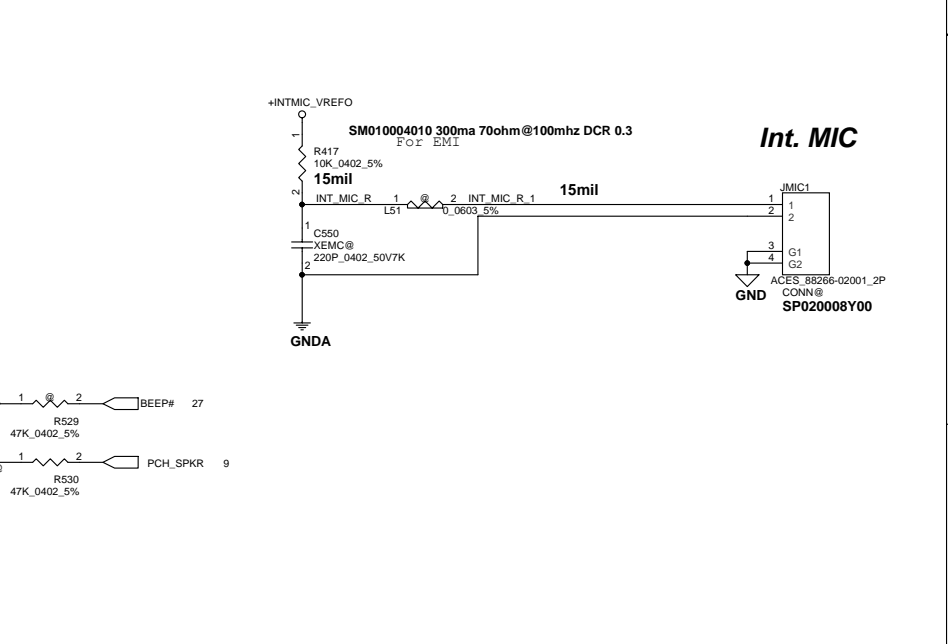
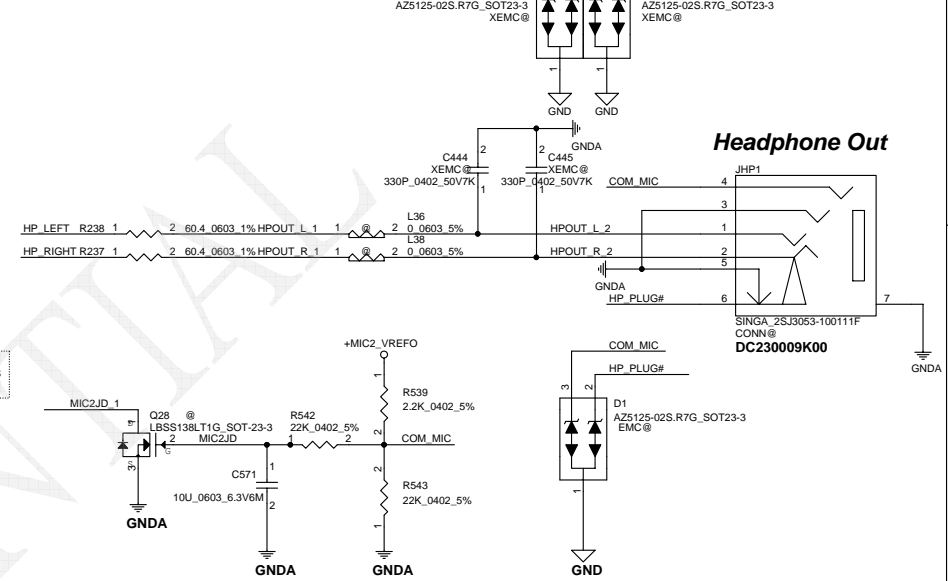
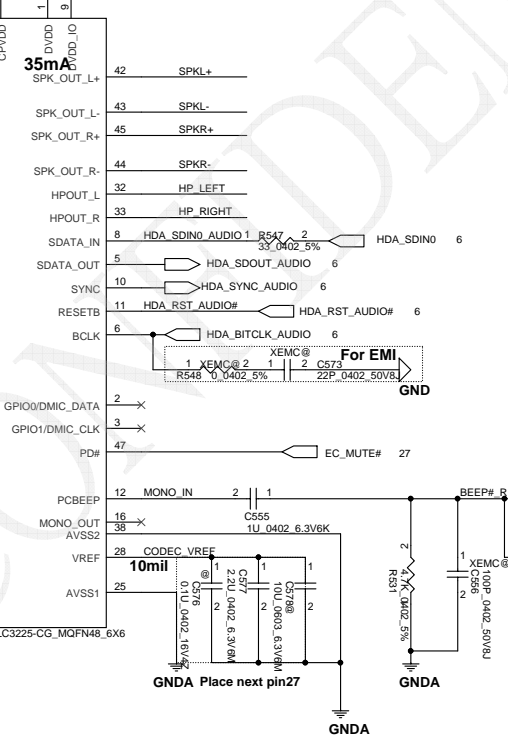
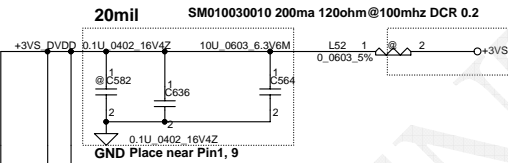
## TPM Board



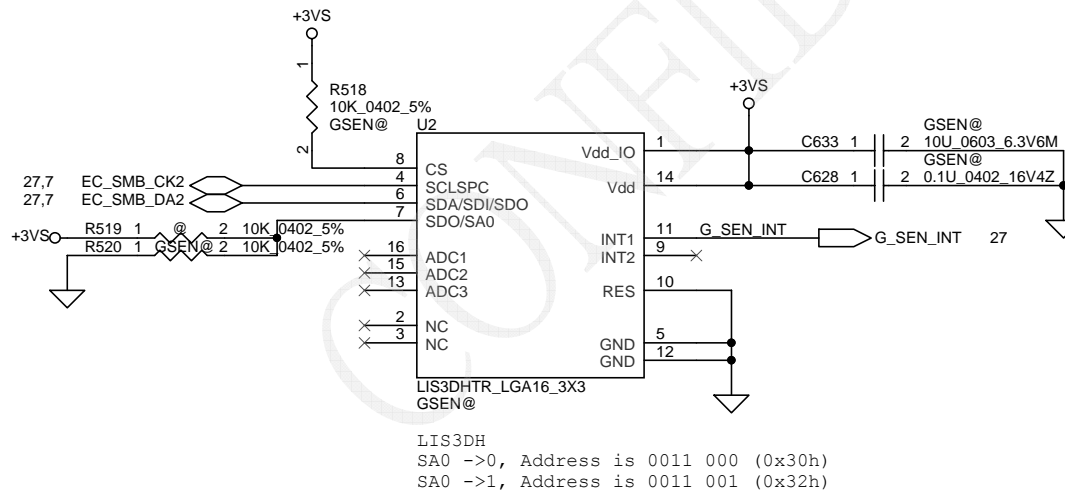
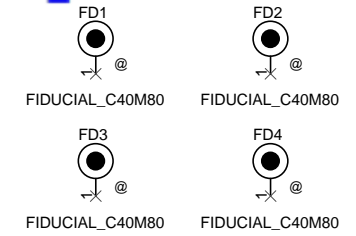
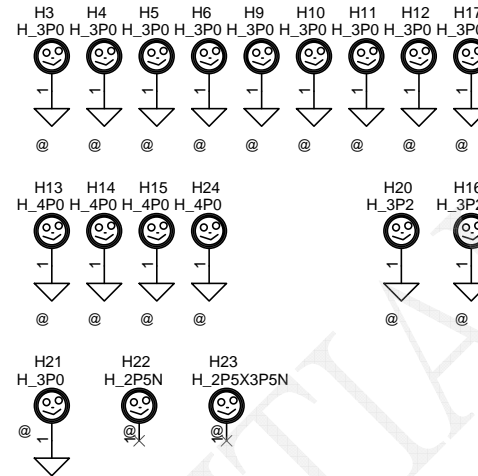
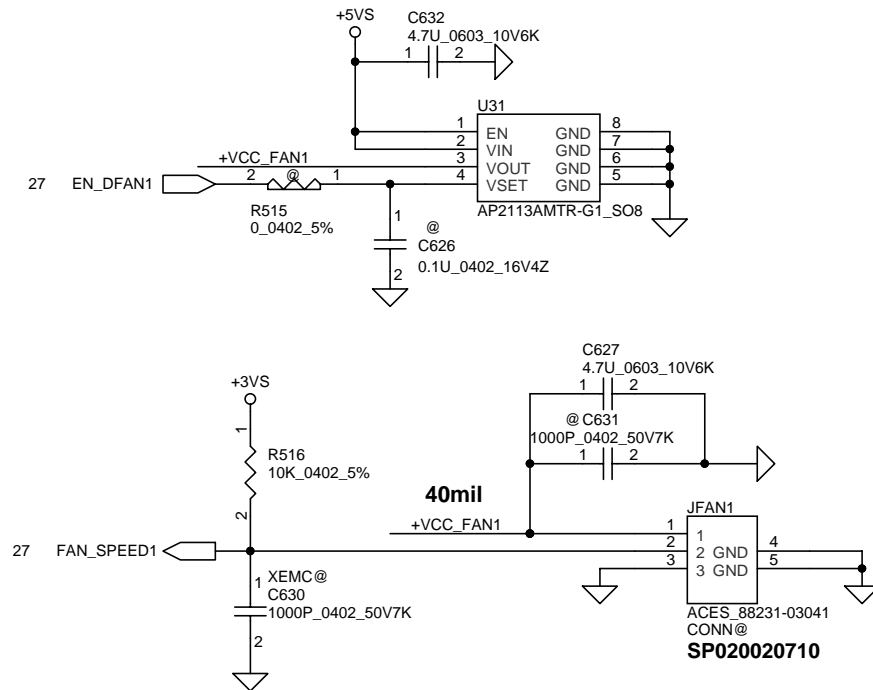
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				Customer	V5WE2 M/B LA-9532P Schematic	0.2
				Date:	Monday, April 08, 2013	Sheet



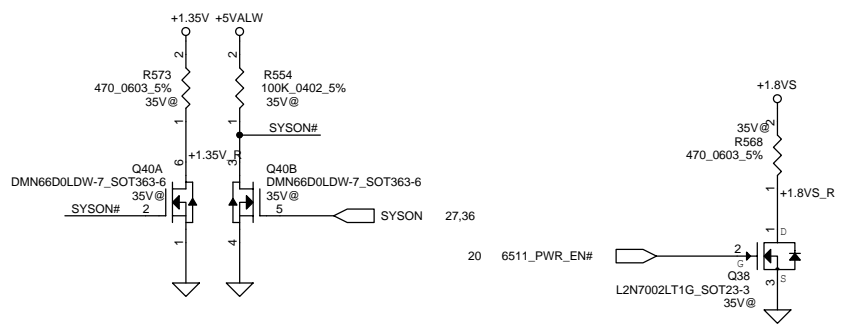
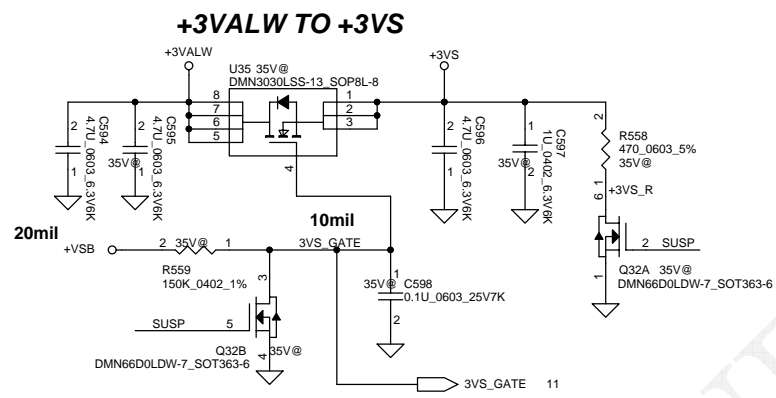
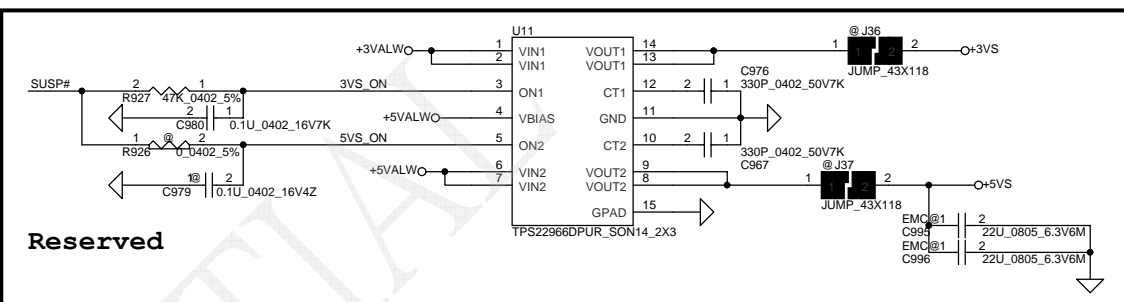
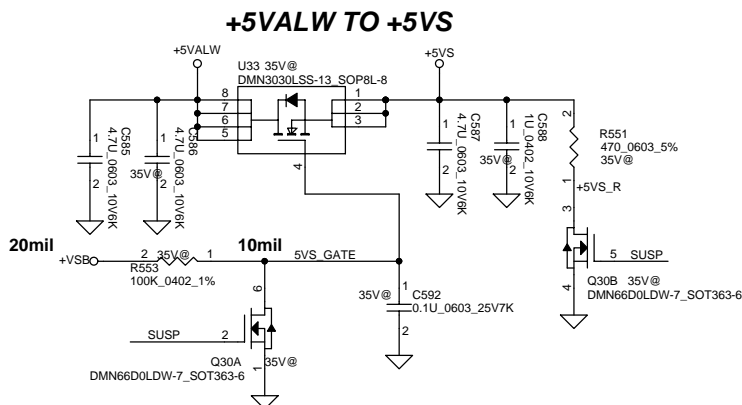
## HD Audio Codec



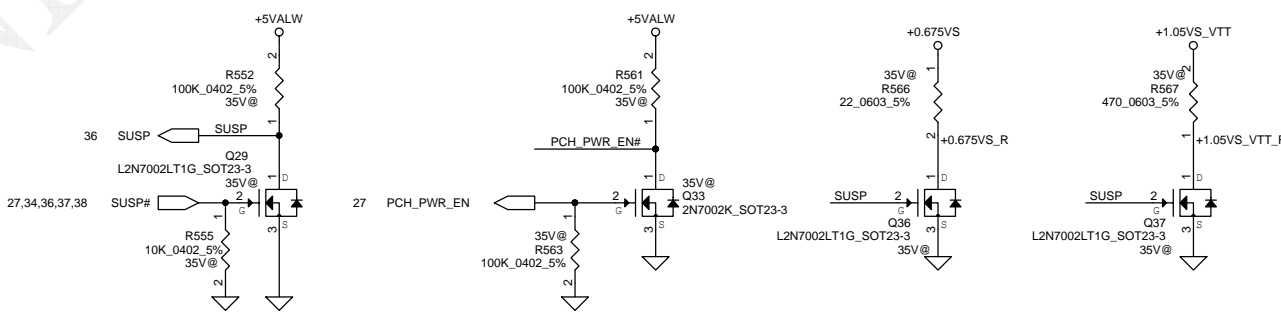
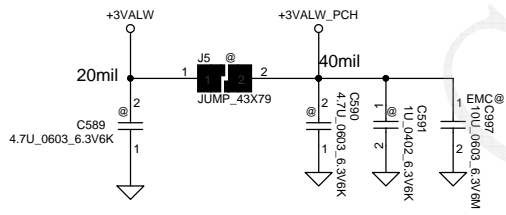
# FAN1 Conn

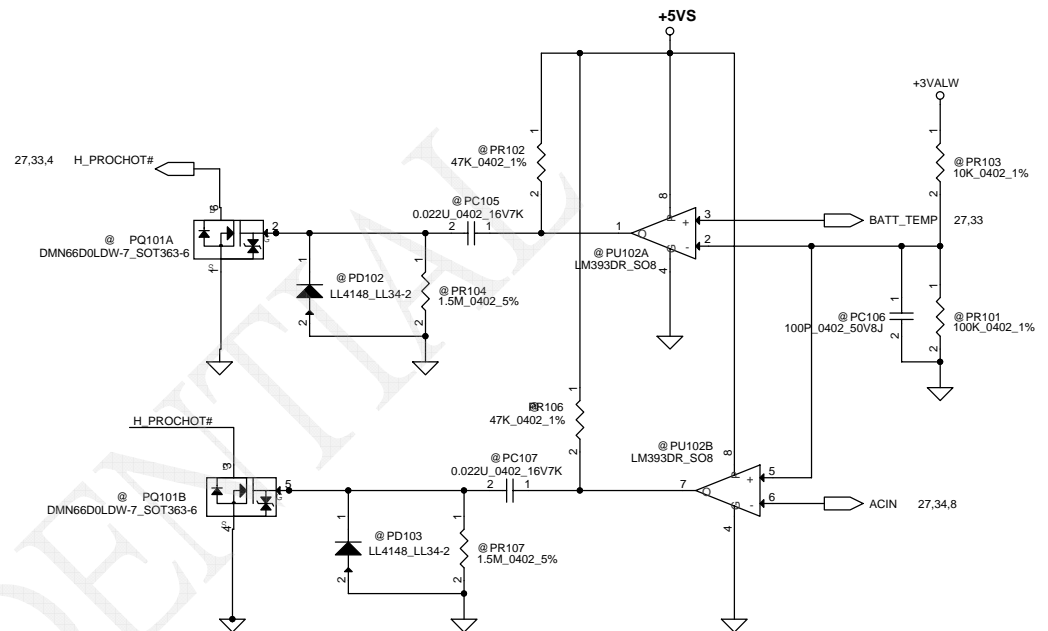
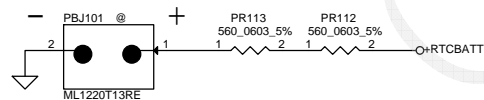
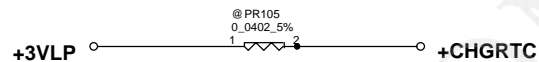
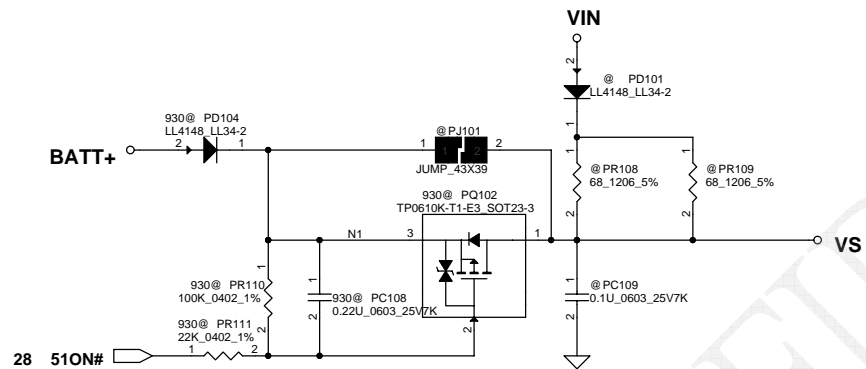


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**+3VALW TO +3VALW(PCH AUX Power)**  
Short J5 for PCH VCCSUS3.3

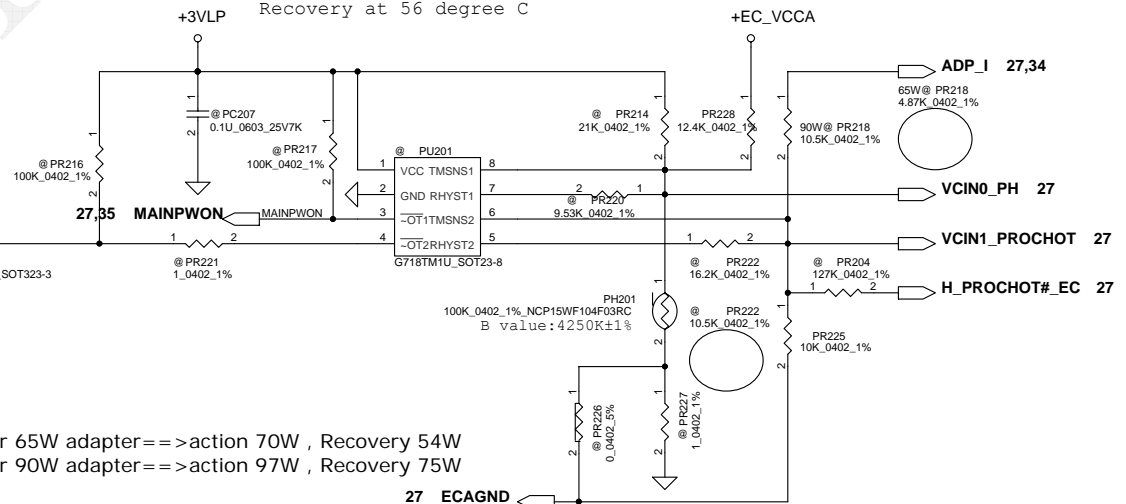




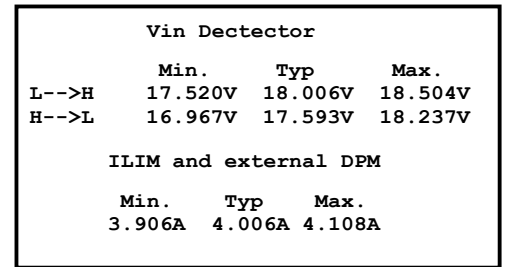
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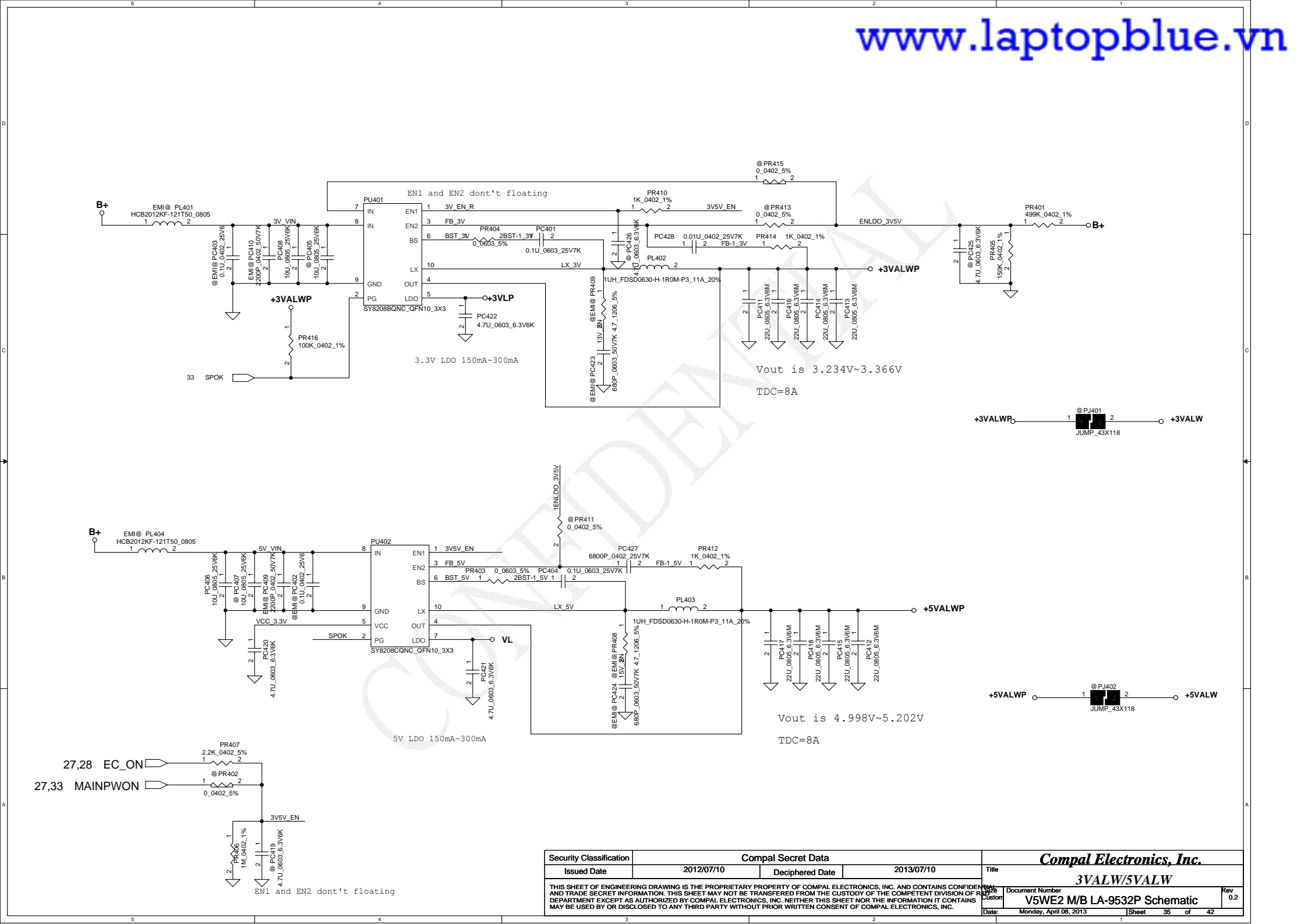
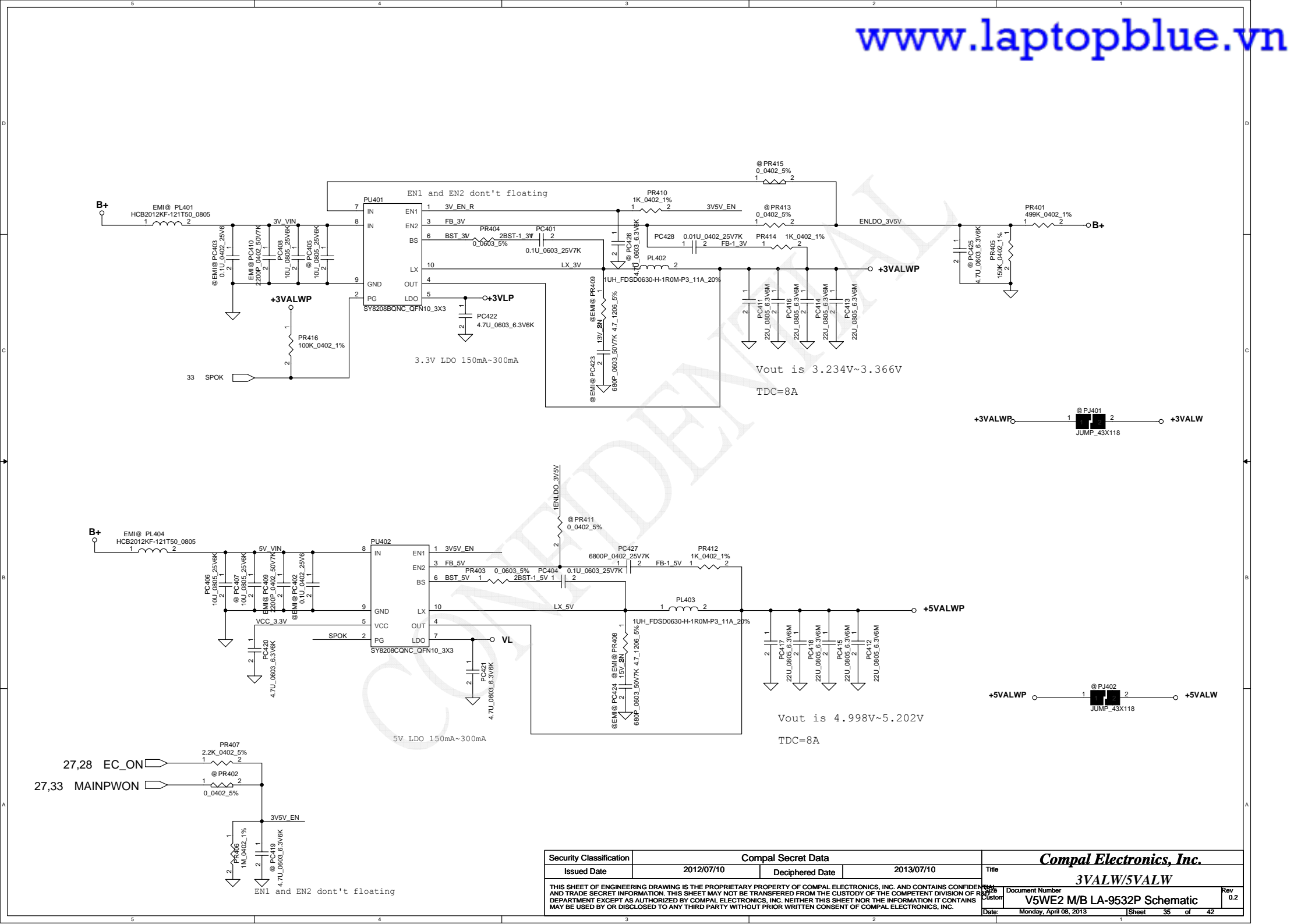
For KB9012 sense 20mΩ	Active	Recovery
65W	84W, 1.2V	56W, 0.793V
90W	117W, 1.2V	77W, 0.791V
120W		

[illegible]

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				Size Custom	Document Number V5WE2 M/B LA-9532P Schematic	Rev 0.2
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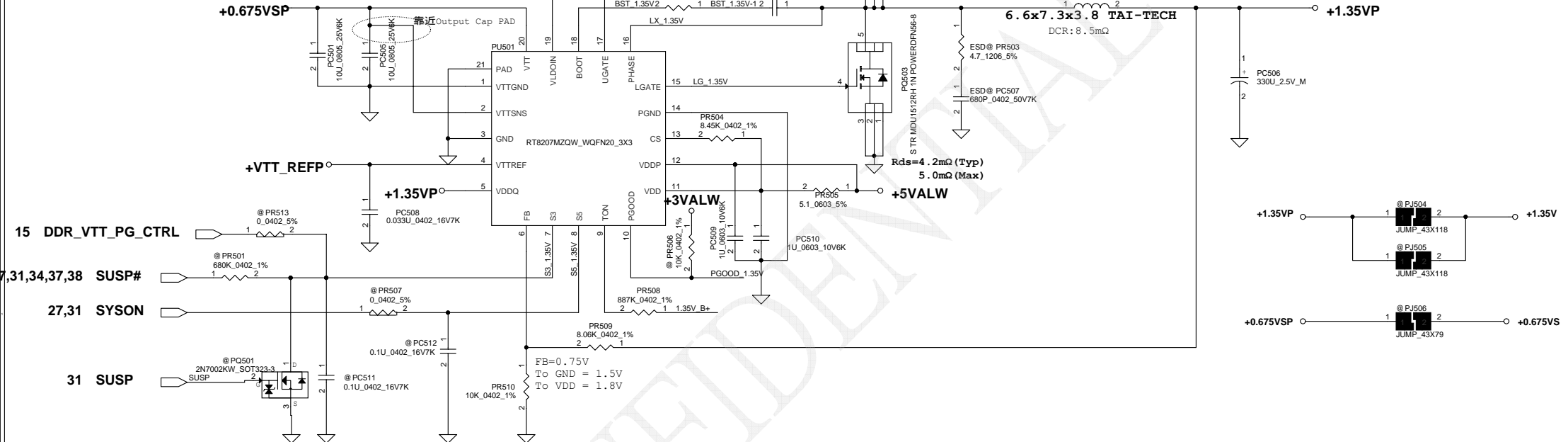


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2011/9/19

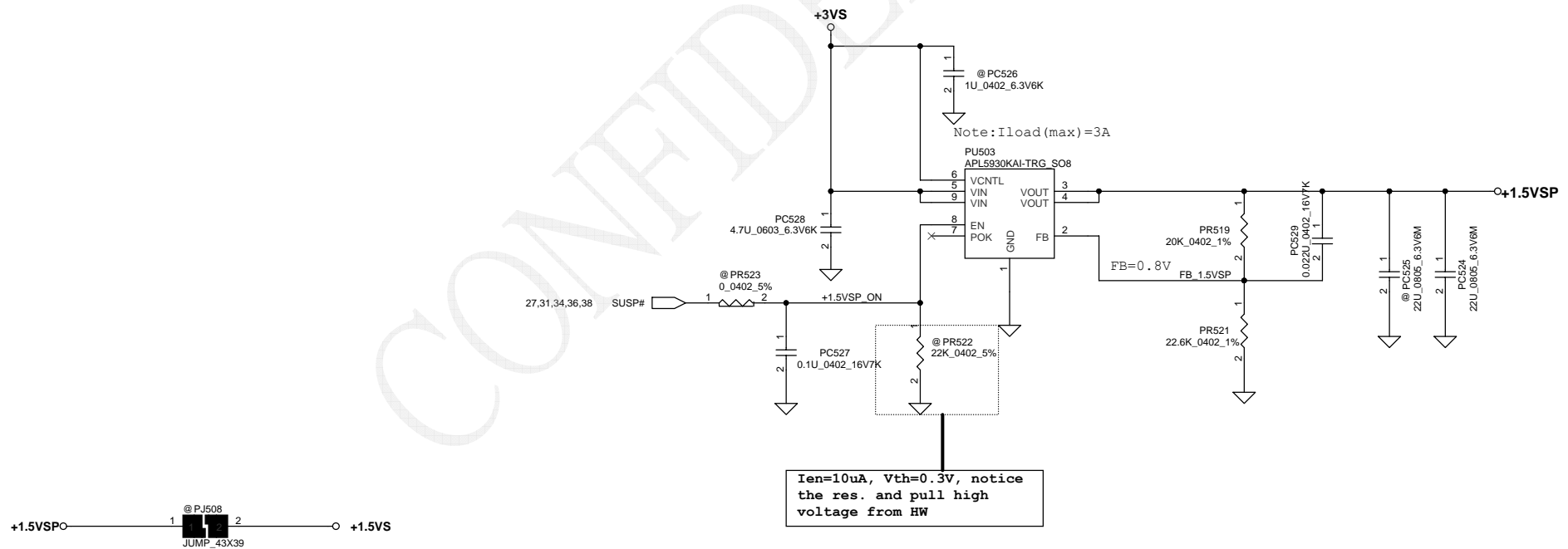
+0.675VSP—



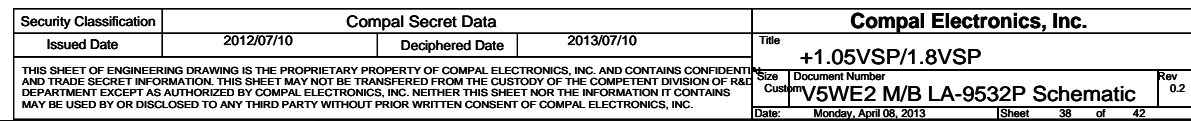
STATE	S3	S5	1.35VP	VTT_REFP	0.675VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)
Note: S3 - sleep ; S5 - power off					

Note: Use VCCSA\_SEL to switch High & Low Level for VID[1]

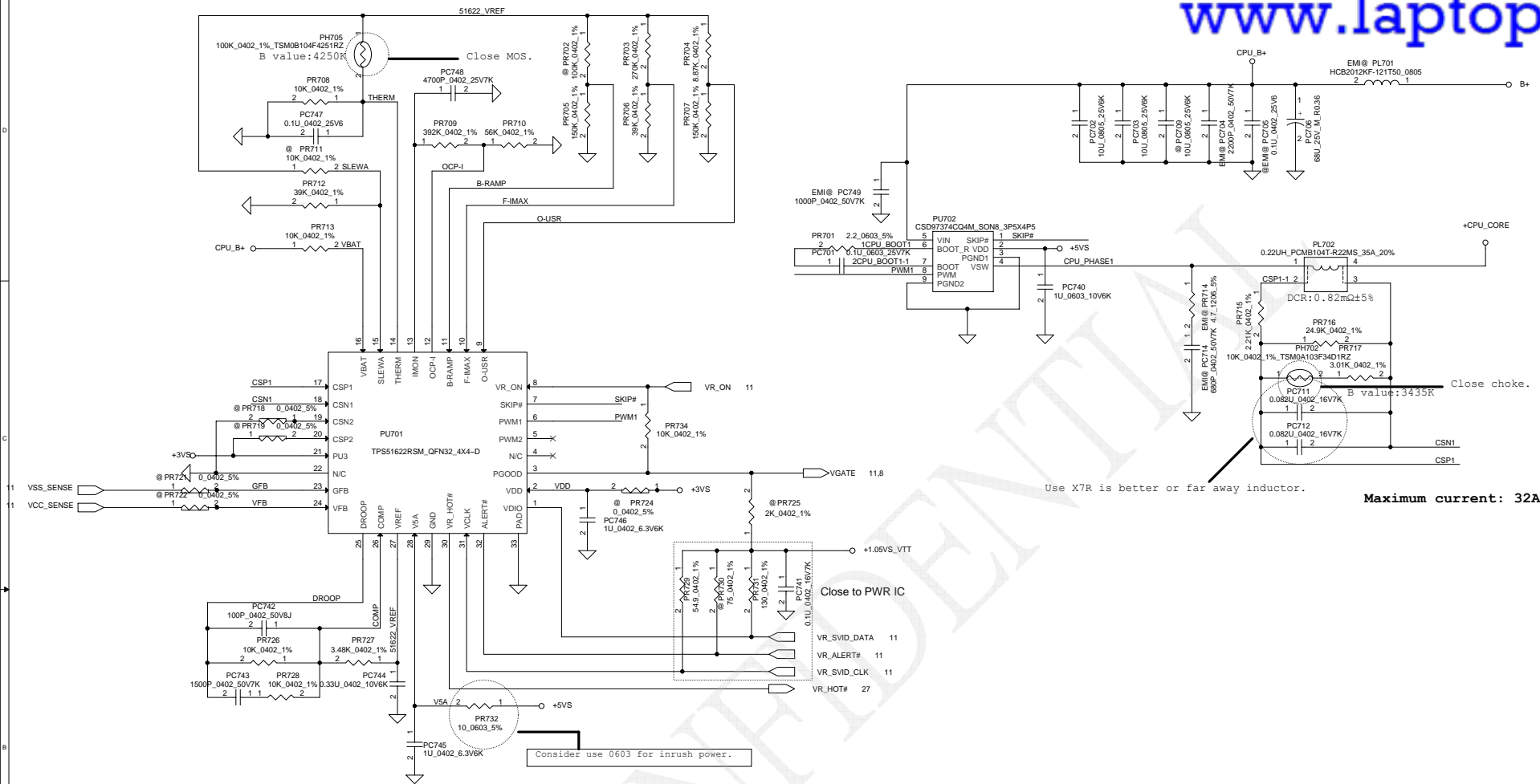
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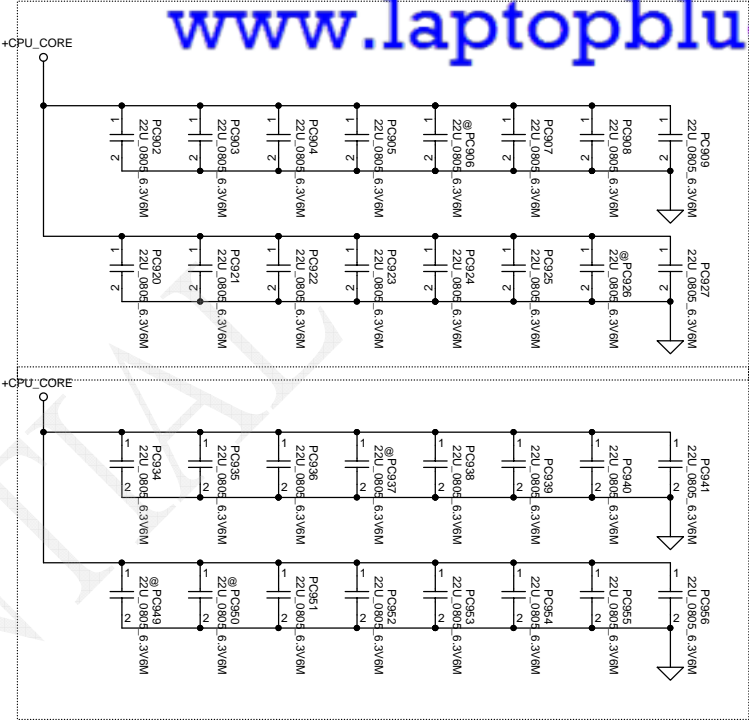




VIN	12V-20V
MAX current	32A
Thermal current	10A
Dynamic current	27A
Over current level	45A
Switching frequency	600KHz
Boot voltage	1.7V
DC Load- line	2m Ohm

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PWR Rule  
CPU DCLL=1.5m ohm design 330uF/9m \*0, 22uF \*30



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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Module Design	Module Design change 3/5V solution		3/5V		11/13	DVT
2		Change RTC type to non-charge		31	Un-pop PR112, PR113	11/13	DVT
3	TPS51622 update to ES2.1	Compensation modify		39	Change PR701 to 2.2, PR703 to 270K, PR727 to 3.48K Un-pop PC742	11/16	DVT
4	EMI request	Cut-in EMI solution		EMI	Add PR313, PC316, PR714, PC714, PC749	11/20	DVT
5	EMI request	EMI confirm remove		EMI	Delete PL102, PC103, PC101, PL202, PC201 and PL703	11/26	DVT
6	Costdown			35	Change PL402, PL403 from 5x5x3 to 7x7x3	12/13	DVT2
7		SY8208B/C update		35	Add PR411, PR413	12/22	DVT2
8	+1.05V ripple close upper and mean too low	Adjust output voltage and add Cff		36	Add PC609 into 4700P Change PR608 from 133K to 127K	12/22	DVT2
9		Improve CPU transient character		40	Unpop PC926	01/09	DVT2
10		Tune sequence		35	Change PC428 from 4700p to 10n, PC427 from 0.047u to 6.8n	02/04	PVT
11		0 ohm reduce			Change PR507, PR513, PR523 to R-pad	02/22	PVT
12		Provide 3/5V PG signal to EC		35	Add PR416	02/22	PVT
13	ESD request			32	Add PC101 into 0.1uF	02/26	PVT
14	ESD request			36	Add PC521, PR503, PC507	02/26	PVT
12							
13							
14							
15							
16							
17							

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				Document Number	V5WE2 M/B LA-9532P Schematic	
				Date:	Monday, April 08, 2013	Sheet 42 of 42