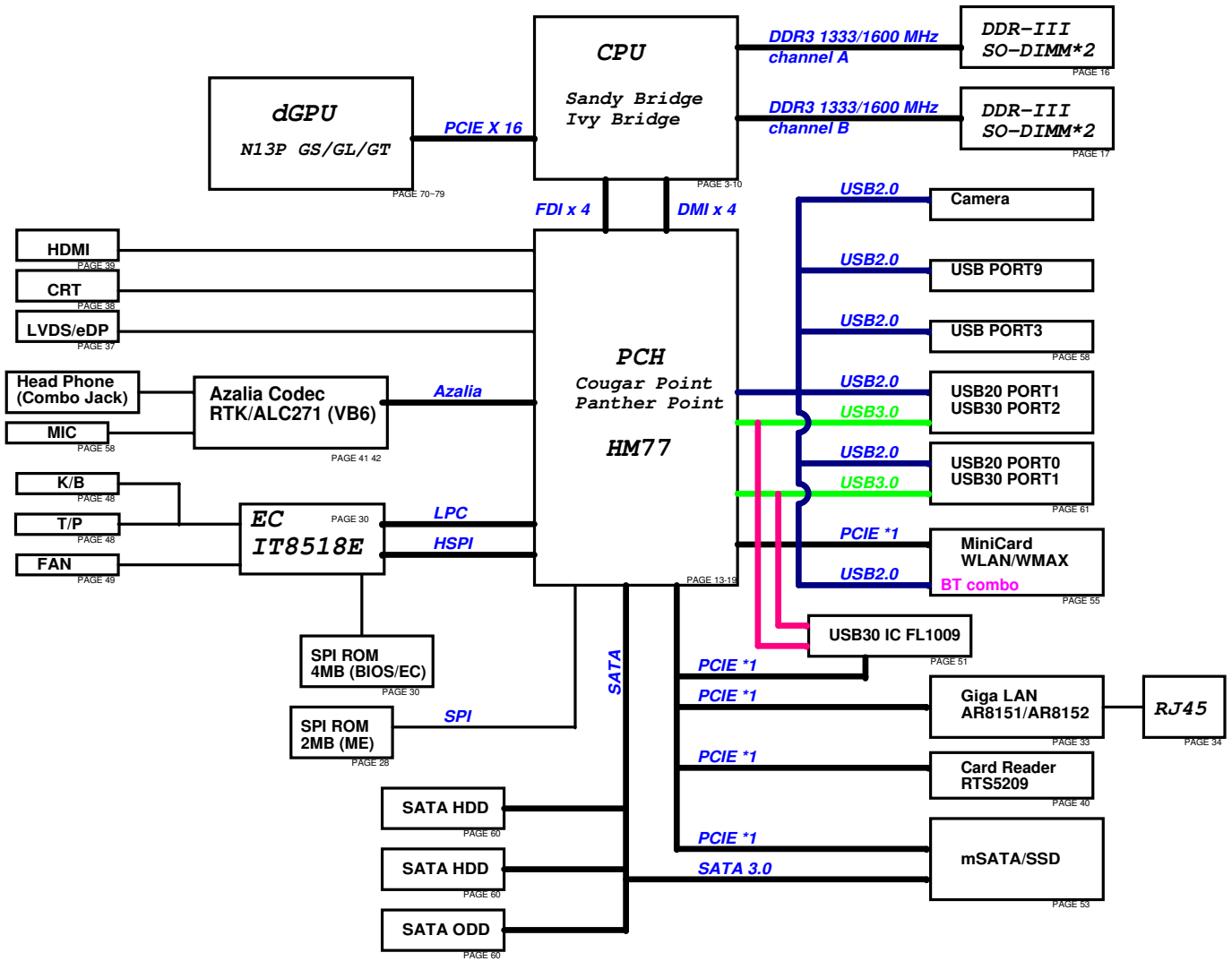
VA70 BLOCK DIAGRAM



POWER

CPU VCORE	PAGE 80
SYSTEM, +3V, +5V	PAGE 81
+VCCP & +VCCP_VT	PAGE 82
DDR & VTT	PAGE 83
2.5V & 1.5VS &1.1VS	PAGE 84
SMART CHARGER	PAGE 88
POWER DETECT	PAGE 90
LOAD SWITCH	PAGE 91
POWER PROTECT	PAGE 92

VGA POWER

GPU VCORE	PAGE 86
+1.05VS_VGA	
+1.5VS_VGA	
+3VS_VGA	
+12VS_VGA	
LOAD SWITCH	PAGE 91
POWER PROTECT	PAGE 92

Power Rails

Sleep State	RTC	VA	VSUS	V	VS
S0	ON	ON	ON	ON	ON
S3	ON	ON	ON	ON	OFF
S4	ON	ON	ON	OFF	OFF
S5/ AC	ON	ON	ON	OFF	OFF
S5/ DC	ON	ON	OFF	OFF	OFF

PCIe Port

PCIE_P1	CARDREADER
PCIE_P2	Mini CARD (WLAN)
PCIE_P3	mSATA
PCIE_P4	USB30
PCIE_P5	
PCIE_P6	LAN

USB20 PORT

USB P00	External MB
USB P01	External MB
USB P02	
USB P03	External DB
USB P04	
USB P05	BT
USB P08	Camera
USB P09	External DB
USB P10	
USB P11	SSD
USB P12	
USB P13	

SATA PORT

SATA P0	HDD 1
SATA P1	HDD 2
SATA P2	ODD 3
SATA P3	mSATA
SATA P4	
SATA P5	

IO BOARD

- USB PORT3
- USB PORT9
- HP_OUT
- MIC IN

TP BT BOARD

- Touch PAD Button
- LID SW

PWR BOARD

- POWER Button
- POWER LED
- LID SW

PEGATRON Title : BLOCK DIAGRAM

BU1-RD Div.1-HW RD Dept.1 Engineer: Wing_Cheng

Size	Project Name	Rev
Custom	BA52HR/CR	1.0

Date: Monday, February 13, 2012 Sheet 1 of 77

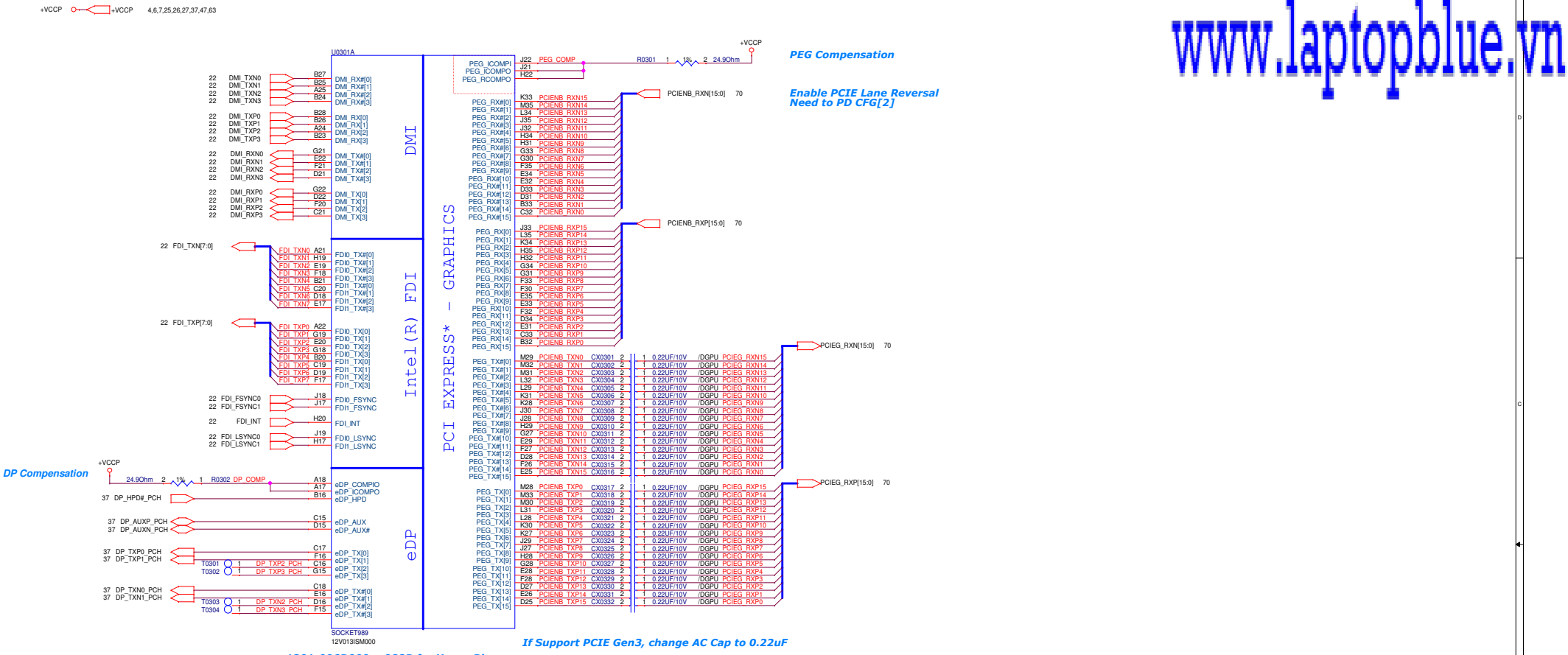
BOM optional	Remark
N/A	For 上件
/ABCT	For ABCT，上件
/niAMT	For no iAMT，上件
/HOME	For 上件
/HR	For Huron River，上件
/Non_HSPI	For ROM SETTING ，上件
Entry	For 上件
Main	For 上件
/USB20	For USB 2.0 ，上件
/HSPI	For 不上件
/HDMI	For HDMI用，不上件
/TP1_AUD	For power control，不上件
/TP1_BT	For power control，不上件
/TP1_CAMERA	For power control，不上件
/TP1_CR	For power control，不上件
/TP1_LAN	For power control，不上件
/TP1_ODD	For power control，不上件
/TP1_WLAN	For power control，不上件
/THERM	For Palm Rest溫度，不上件
/usb30	For USB 3.0 ，不上件
/ZPODD	For ODD battery saving使用Mount R5108，不上件
@	For 不上件
@/MP	For debug port, MP不上件
/BT270	視keypat list而定
/COMBO_BT	視keypat list而定
/SATA+	For Sata Repeater, SR先上件

PEGATRON Title : System Setting

PEGATRON COMPUTER INC Engineer: Wing_Cheng

Size	Project Name	Rev
A	BA52HR/CR	1.0

Date: Monday, February 13, 2012 Sheet 2 of 94



PEGATRON	Title : CPU(1)_DMI,PEG,FDI,CLK,MISC
PEGATRON COMPUTER INC	Engineer: Wing_Cheng
Size: C	Project Name: BA52HR/CR
Rev: 1.0	
Date: Monday, February 13, 2012	Sheet 3 of 94

Select the termination voltage of DMI and FDI Tx/Rx (PCH Strap)
H_SNB_IVB# connected to DF_TVS via 1Kohm
DF_TVS needs PU via 2.2Kohm to +1.8VS

U0301B

MISC
SNB_IVB#
SKTOCC#

THERMAL
CATERR#
PECI
PROCHOT#
THERMTRIP#

PWR MANAGEMENT
PM_SYNC
UNCOREPWRGOOD
SM_DRAMPWROK
RESET#

CLOCKS
BCLK
BCLK#
DPLL_REF_SSCLK
DPLL_REF_SSCLK#

DDR3 MISC
SM_DRAMRST#
SM_RCOMP[0]
SM_RCOMP[1]
SM_RCOMP[2]

JTAG & BPM
PRDY#
PREQ#
TCK
TMS
TRST#
TDI
TDO
DBR#
BPM#[0]
BPM#[1]
BPM#[2]
BPM#[3]
BPM#[4]
BPM#[5]
BPM#[6]
BPM#[7]

SOCKET989
12V013ISM000

do not remove because POWER removed thier PU R. Joyoung0613

R1.0 1229

DDR3 DRAM Reset. @

System Memory Impedance Compensation
Huron River platform Design Guide 436735 P.88 Table 37.
Eric Fang to Alan Chien 11/15/2010

Huron River platform Design Guide Update 440484
SM_RCOMP_1 use 26ohm 1%

R1.0 PU/PD for JTAG signals

PM_SYS_PWRGD is the power good for +1.5V_VCCDDQ

R1.1 change to short pin

1.57 Volt

Power good for +1.5V_VCCDDQ (delay > 100ns)

Reserve S3 power reduction schematic

If don't support S3 power reduction
1. Unmount R0450, R0452, U0404, R0453, Q0403, C0404, R0455, R0454, C0405
2. Change R0449 to 200ohm from 1kohm, change R0409 to 130ohm from 0ohm - Design Guide 1.0 page 106

3. Unmount Q0501, C0501, R0506, R0504, R0507
4. Mount R0501, change r0508 to 0ohm from 1kohm

5 Unmount Q0701, R0703, R0705, Q0702
6. Mount R0702 and short JP0701

7. Unmount R2232, R2231, Q2203

Check Frank remove or not??

R1.0 0119
Sandy Bridge:R0417 = 750 ohm (10V220000093)
Ivy Bridge:R0417 = 680 ohm (10V240000041)

Frank
0506 EVERST check

R1.0 0224
Intel Comments

PEGATRON Title : CPU(1)_DMI,PEG,FDI,CLK,MISC
PEGATRON COMPUTER INC Engineer: Wing_Cheng
Size C | Project Name BA52HR/CR | Rev 1.0
Date: Monday, February 13, 2012 Sheet 4 of 94

+1.5V +1.5V 7,16,51,63

U0301C

DDR SYSTEM MEMORY A

16 M_A_DQ[63:0]

M_A_DQ0	C5	SA_DQ[0]
M_A_DQ1	D5	SA_DQ[1]
M_A_DQ2	D3	SA_DQ[2]
M_A_DQ3	D2	SA_DQ[3]
M_A_DQ4	D6	SA_DQ[4]
M_A_DQ5	C6	SA_DQ[5]
M_A_DQ6	C2	SA_DQ[6]
M_A_DQ7	C3	SA_DQ[7]
M_A_DQ8	F10	SA_DQ[8]
M_A_DQ9	F8	SA_DQ[9]
M_A_DQ10	G10	SA_DQ[10]
M_A_DQ11	G9	SA_DQ[11]
M_A_DQ12	F9	SA_DQ[12]
M_A_DQ13	F7	SA_DQ[13]
M_A_DQ14	G8	SA_DQ[14]
M_A_DQ15	G7	SA_DQ[15]
M_A_DQ16	K4	SA_DQ[16]
M_A_DQ17	K5	SA_DQ[17]
M_A_DQ18	K1	SA_DQ[18]
M_A_DQ19	J1	SA_DQ[19]
M_A_DQ20	J5	SA_DQ[20]
M_A_DQ21	J4	SA_DQ[21]
M_A_DQ22	J2	SA_DQ[22]
M_A_DQ23	K2	SA_DQ[23]
M_A_DQ24	M8	SA_DQ[24]
M_A_DQ25	N10	SA_DQ[25]
M_A_DQ26	N8	SA_DQ[26]
M_A_DQ27	N7	SA_DQ[27]
M_A_DQ28	M10	SA_DQ[28]
M_A_DQ29	M9	SA_DQ[29]
M_A_DQ30	N9	SA_DQ[30]
M_A_DQ31	M7	SA_DQ[31]
M_A_DQ32	AG6	SA_DQ[32]
M_A_DQ33	AG5	SA_DQ[33]
M_A_DQ34	AK6	SA_DQ[34]
M_A_DQ35	AK5	SA_DQ[35]
M_A_DQ36	AH5	SA_DQ[36]
M_A_DQ37	AH6	SA_DQ[37]
M_A_DQ38	AJ5	SA_DQ[38]
M_A_DQ39	AJ6	SA_DQ[39]
M_A_DQ40	AJ8	SA_DQ[40]
M_A_DQ41	AK8	SA_DQ[41]
M_A_DQ42	AJ9	SA_DQ[42]
M_A_DQ43	AK9	SA_DQ[43]
M_A_DQ44	AH8	SA_DQ[44]
M_A_DQ45	AH9	SA_DQ[45]
M_A_DQ46	AL9	SA_DQ[46]
M_A_DQ47	AL8	SA_DQ[47]
M_A_DQ48	AP11	SA_DQ[48]
M_A_DQ49	AN11	SA_DQ[49]
M_A_DQ50	AL12	SA_DQ[50]
M_A_DQ51	AM12	SA_DQ[51]
M_A_DQ52	AM11	SA_DQ[52]
M_A_DQ53	AL11	SA_DQ[53]
M_A_DQ54	AP12	SA_DQ[54]
M_A_DQ55	AN12	SA_DQ[55]
M_A_DQ56	AJ14	SA_DQ[56]
M_A_DQ57	AH14	SA_DQ[57]
M_A_DQ58	AL15	SA_DQ[58]
M_A_DQ59	AK15	SA_DQ[59]
M_A_DQ60	AL14	SA_DQ[60]
M_A_DQ61	AK14	SA_DQ[61]
M_A_DQ62	AJ15	SA_DQ[62]
M_A_DQ63	AH15	SA_DQ[63]

16 M_A_BS0	AE10	SA_BS[0]
16 M_A_BS1	AF10	SA_BS[1]
16 M_A_BS2	V6	SA_BS[2]
16 M_A_CAS#	AE8	SA_CAS#
16 M_A_RAS#	AD9	SA_RAS#
16 M_A_WE#	AF9	SA_WE#

SA_CLK[0]	AB6	M_A_DIM0_CLK_DDR0 16
SA_CLK#[0]	AA6	M_A_DIM0_CLK_DDR#0 16
SA_CKE[0]	V9	M_A_DIM0_CKE0 16
SA_CLK[1]	AA5	M_A_DIM0_CLK_DDR1 16
SA_CLK#[1]	AB5	M_A_DIM0_CLK_DDR#1 16
SA_CKE[1]	V10	M_A_DIM0_CKE1 16
SA_CLK[2]	AB4	M_A_DIM0_CLK_DDR2 16
SA_CLK#[2]	AA4	M_A_DIM0_CLK_DDR#2 16
SA_CKE[2]	W9	M_A_DIM0_CKE2 16
SA_CLK[3]	AB3	M_A_DIM0_CLK_DDR3 16
SA_CLK#[3]	AA3	M_A_DIM0_CLK_DDR#3 16
SA_CKE[3]	W10	M_A_DIM0_CKE3 16
SA_CS#[0]	AK3	M_A_DIM0_CS#0 16
SA_CS#[1]	AL3	M_A_DIM0_CS#1 16
SA_CS#[2]	AG1	M_A_DIM0_CS#2 16
SA_CS#[3]	AH1	M_A_DIM0_CS#3 16
SA_ODT[0]	AH3	M_A_DIM0_ODT0 16
SA_ODT[1]	AG3	M_A_DIM0_ODT1 16
SA_ODT[2]	AG2	M_A_DIM0_ODT2 16
SA_ODT[3]	AH2	M_A_DIM0_ODT3 16

SA_DQS#[0]	C4	M_A_DQS#0
SA_DQS#[1]	G6	M_A_DQS#1
SA_DQS#[2]	J3	M_A_DQS#2
SA_DQS#[3]	M6	M_A_DQS#3
SA_DQS#[4]	AL6	M_A_DQS#4
SA_DQS#[5]	AM8	M_A_DQS#5
SA_DQS#[6]	AR12	M_A_DQS#6
SA_DQS#[7]	AM15	M_A_DQS#7

M_A_DQS#[7:0] 16

SA_DQS[0]	D4	M_A_DQS0
SA_DQS[1]	F6	M_A_DQS1
SA_DQS[2]	K3	M_A_DQS2
SA_DQS[3]	N6	M_A_DQS3
SA_DQS[4]	AL5	M_A_DQS4
SA_DQS[5]	AM9	M_A_DQS5
SA_DQS[6]	AR11	M_A_DQS6
SA_DQS[7]	AM14	M_A_DQS7

M_A_DQS[7:0] 16

SA_MA[0]	AD10	M_A_A0
SA_MA[1]	W1	M_A_A1
SA_MA[2]	W2	M_A_A2
SA_MA[3]	W7	M_A_A3
SA_MA[4]	V3	M_A_A4
SA_MA[5]	V2	M_A_A5
SA_MA[6]	W3	M_A_A6
SA_MA[7]	W6	M_A_A7
SA_MA[8]	V1	M_A_A8
SA_MA[9]	W5	M_A_A9
SA_MA[10]	AD8	M_A_A10
SA_MA[11]	V4	M_A_A11
SA_MA[12]	W4	M_A_A12
SA_MA[13]	AF8	M_A_A13
SA_MA[14]	V5	M_A_A14
SA_MA[15]	V7	M_A_A15

M_A_A[15:0] 16

SOCKET989
12V013ISM000

U0301D

DDR SYSTEM MEMORY B

17 M_B_DQ[63:0]

M_B_DQ0	C9	SB_DQ[0]
M_B_DQ1	A7	SB_DQ[1]
M_B_DQ2	D10	SB_DQ[2]
M_B_DQ3	C8	SB_DQ[3]
M_B_DQ4	A9	SB_DQ[4]
M_B_DQ5	A8	SB_DQ[5]
M_B_DQ6	D9	SB_DQ[6]
M_B_DQ7	D8	SB_DQ[7]
M_B_DQ8	G4	SB_DQ[8]
M_B_DQ9	F4	SB_DQ[9]
M_B_DQ10	F1	SB_DQ[10]
M_B_DQ11	G1	SB_DQ[11]
M_B_DQ12	G5	SB_DQ[12]
M_B_DQ13	F5	SB_DQ[13]
M_B_DQ14	F2	SB_DQ[14]
M_B_DQ15	G2	SB_DQ[15]
M_B_DQ16	J7	SB_DQ[16]
M_B_DQ17	J8	SB_DQ[17]
M_B_DQ18	K10	SB_DQ[18]
M_B_DQ19	K9	SB_DQ[19]
M_B_DQ20	J9	SB_DQ[20]
M_B_DQ21	J10	SB_DQ[21]
M_B_DQ22	K8	SB_DQ[22]
M_B_DQ23	K7	SB_DQ[23]
M_B_DQ24	M5	SB_DQ[24]
M_B_DQ25	N4	SB_DQ[25]
M_B_DQ26	N2	SB_DQ[26]
M_B_DQ27	N1	SB_DQ[27]
M_B_DQ28	M4	SB_DQ[28]
M_B_DQ29	N5	SB_DQ[29]
M_B_DQ30	M2	SB_DQ[30]
M_B_DQ31	M1	SB_DQ[31]
M_B_DQ32	AM5	SB_DQ[32]
M_B_DQ33	AM6	SB_DQ[33]
M_B_DQ34	AR3	SB_DQ[34]
M_B_DQ35	AP3	SB_DQ[35]
M_B_DQ36	AN3	SB_DQ[36]
M_B_DQ37	AN2	SB_DQ[37]
M_B_DQ38	AN1	SB_DQ[38]
M_B_DQ39	AP2	SB_DQ[39]
M_B_DQ40	AP5	SB_DQ[40]
M_B_DQ41	AN9	SB_DQ[41]
M_B_DQ42	AT5	SB_DQ[42]
M_B_DQ43	AT6	SB_DQ[43]
M_B_DQ44	AP6	SB_DQ[44]
M_B_DQ45	AN8	SB_DQ[45]
M_B_DQ46	AR6	SB_DQ[46]
M_B_DQ47	AR5	SB_DQ[47]
M_B_DQ48	AR9	SB_DQ[48]
M_B_DQ49	AJ11	SB_DQ[49]
M_B_DQ50	AT8	SB_DQ[50]
M_B_DQ51	AT9	SB_DQ[51]
M_B_DQ52	AH11	SB_DQ[52]
M_B_DQ53	AR8	SB_DQ[53]
M_B_DQ54	AJ12	SB_DQ[54]
M_B_DQ55	AH12	SB_DQ[55]
M_B_DQ56	AT11	SB_DQ[56]
M_B_DQ57	AN14	SB_DQ[57]
M_B_DQ58	AR14	SB_DQ[58]
M_B_DQ59	AT14	SB_DQ[59]
M_B_DQ60	AT12	SB_DQ[60]
M_B_DQ61	AN15	SB_DQ[61]
M_B_DQ62	AR15	SB_DQ[62]
M_B_DQ63	AT15	SB_DQ[63]

17 M_B_BS0	AA9	SB_BS[0]
17 M_B_BS1	AA7	SB_BS[1]
17 M_B_BS2	R6	SB_BS[2]
17 M_B_CAS#	AA10	SB_CAS#
17 M_B_RAS#	AB8	SB_RAS#
17 M_B_WE#	AB9	SB_WE#

SB_CLK[0]	AE2	M_B_DIM0_CLK_DDR0 17
SB_CLK#[0]	AD2	M_B_DIM0_CLK_DDR#0 17
SB_CKE[0]	R9	M_B_DIM0_CKE0 17
SB_CLK[1]	AE1	M_B_DIM0_CLK_DDR1 17
SB_CLK#[1]	AD1	M_B_DIM0_CLK_DDR#1 17
SB_CKE[1]	R10	M_B_DIM0_CKE1 17
SB_CLK[2]	AB2	M_B_DIM0_CLK_DDR2 17
SB_CLK#[2]	AA2	M_B_DIM0_CLK_DDR#2 17
SB_CKE[2]	T9	M_B_DIM0_CKE2 17
SB_CLK[3]	AA1	M_B_DIM0_CLK_DDR3 17
SB_CLK#[3]	AB1	M_B_DIM0_CLK_DDR#3 17
SB_CKE[3]	T10	M_B_DIM0_CKE3 17
SB_CS#[0]	AD3	M_B_DIM0_CS#0 17
SB_CS#[1]	AE3	M_B_DIM0_CS#1 17
SB_CS#[2]	AD6	M_B_DIM0_CS#2 17
SB_CS#[3]	AE6	M_B_DIM0_CS#3 17
SB_ODT[0]	AE4	M_B_DIM0_ODT0 17
SB_ODT[1]	AD4	M_B_DIM0_ODT1 17
SB_ODT[2]	AD5	M_B_DIM0_ODT2 17
SB_ODT[3]	AE5	M_B_DIM0_ODT3 17

SB_DQS#[0]	D7	M_B_DQS#0
SB_DQS#[1]	F3	M_B_DQS#1
SB_DQS#[2]	K6	M_B_DQS#2
SB_DQS#[3]	N3	M_B_DQS#3
SB_DQS#[4]	AN5	M_B_DQS#4
SB_DQS#[5]	AP9	M_B_DQS#5
SB_DQS#[6]	AK12	M_B_DQS#6
SB_DQS#[7]	AP15	M_B_DQS#7

M_B_DQS#[7:0] 17

SB_DQS[0]	C7	M_B_DQS0
SB_DQS[1]	G3	M_B_DQS1
SB_DQS[2]	J6	M_B_DQS2
SB_DQS[3]	M9	M_B_DQS3
SB_DQS[4]	AN6	M_B_DQS4
SB_DQS[5]	AP8	M_B_DQS5
SB_DQS[6]	AK11	M_B_DQS6
SB_DQS[7]	AP14	M_B_DQS7

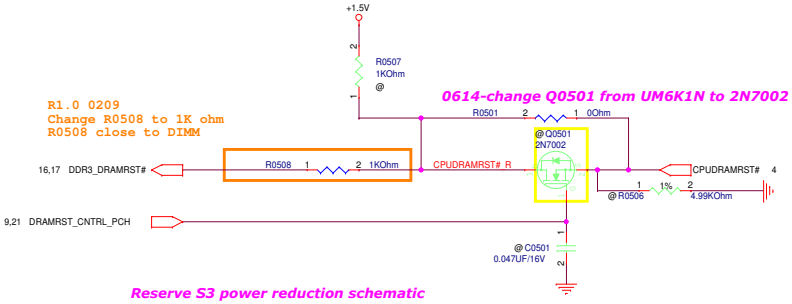
M_B_DQS[7:0] 17

SB_MA[0]	AA8	M_B_A0
SB_MA[1]	T7	M_B_A1
SB_MA[2]	R7	M_B_A2
SB_MA[3]	T6	M_B_A3
SB_MA[4]	T2	M_B_A4
SB_MA[5]	T4	M_B_A5
SB_MA[6]	T3	M_B_A6
SB_MA[7]	R2	M_B_A7
SB_MA[8]	T5	M_B_A8
SB_MA[9]	R3	M_B_A9
SB_MA[10]	AB7	M_B_A10
SB_MA[11]	R1	M_B_A11
SB_MA[12]	T1	M_B_A12
SB_MA[13]	AB10	M_B_A13
SB_MA[14]	R5	M_B_A14
SB_MA[15]	R4	M_B_A15

M_B_A[15:0] 17

SOCKET989
12V013ISM000

R1.0 S3 circuit:- DRAM_RST# to memory should be high during S3



Reserve S3 power reduction schematic

If don't support S3 power reduction
1. Unmount R0450, R0452, U0404, R0453, Q0403, C0404, R0455, R0454, C0405
2. Change R0449 to 200ohm from 1kohm, change R0409 to 130ohm from 0ohm - Design Guide 1.0 page 106

3. Unmount Q0501, C0501, R0506, R0504, R0507
4. Mount R0501, change r0508 to 0ohm from 1kohm

5 Unmount Q0701, R0703, R0705, Q0702
6. Mount R0702 and short JP0701

7. Unmount R2232, R2231, Q2203

PEGATRON Title : CPU(2)_DDR3
PEGATRON COMPUTER INC Engineer: Wing_Cheng
Size C | Project Name BA52HR/CR | Rev 1.0
Date: Monday, February 13, 2012 | Sheet 5 of 94

POWER

Vcc for processor core
Voltage range: 0.3 - 1.52V

SV-QC ICCMAX 94A
SV-DC ICCMAX 53A

Check net name??

Voltage for the memory controller and shared cache defined at the motherboard VCCIO_SENSE and VSS_SENSE_VCCIO

ICCMAX_VCCIO 8.5A

0614-Remove C0641 and nostuff C0651,C0647,C0658

0622-Remove CE0603(powre schematic reserve)

0622-Remove CE0601(powre schematic reserve)

R1.0 0126
Intel Comments

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

Frank
20110602 check pull up/pull down reserve power schematic or not.

Frank
20110516 Change VCCP_SENSE to VCCIO_SENSE and change VSSP_SENSE to VSSIO_SENSE for meet power schematic.

Frank
20110516 Remove R0601 and R0604, because Power is already reserved

HR_Decoupling guide from Intel (POWER + EE)
+VCCP 22uF * 19pcs (7 nostuff)
330uF * 3pcs

EIH31/30 (EE)
+VCCP 10uF * 19pcs (2pcs no stuff)
22uF* 10 pcs (total no stuff)
330 uF *1pcs Power support

CR_Decoupling guide from Intel (POWER + EE)
+VCCP 22uF * 19pcs (7 nostuff)
330uF * 3pcs

Decoupling guide for Everest (EE)
+VCCP 22uF * 19pcs (7 no stuff)
330uF * 1pcs (1 no stuff)=>JE31HR/CR power support

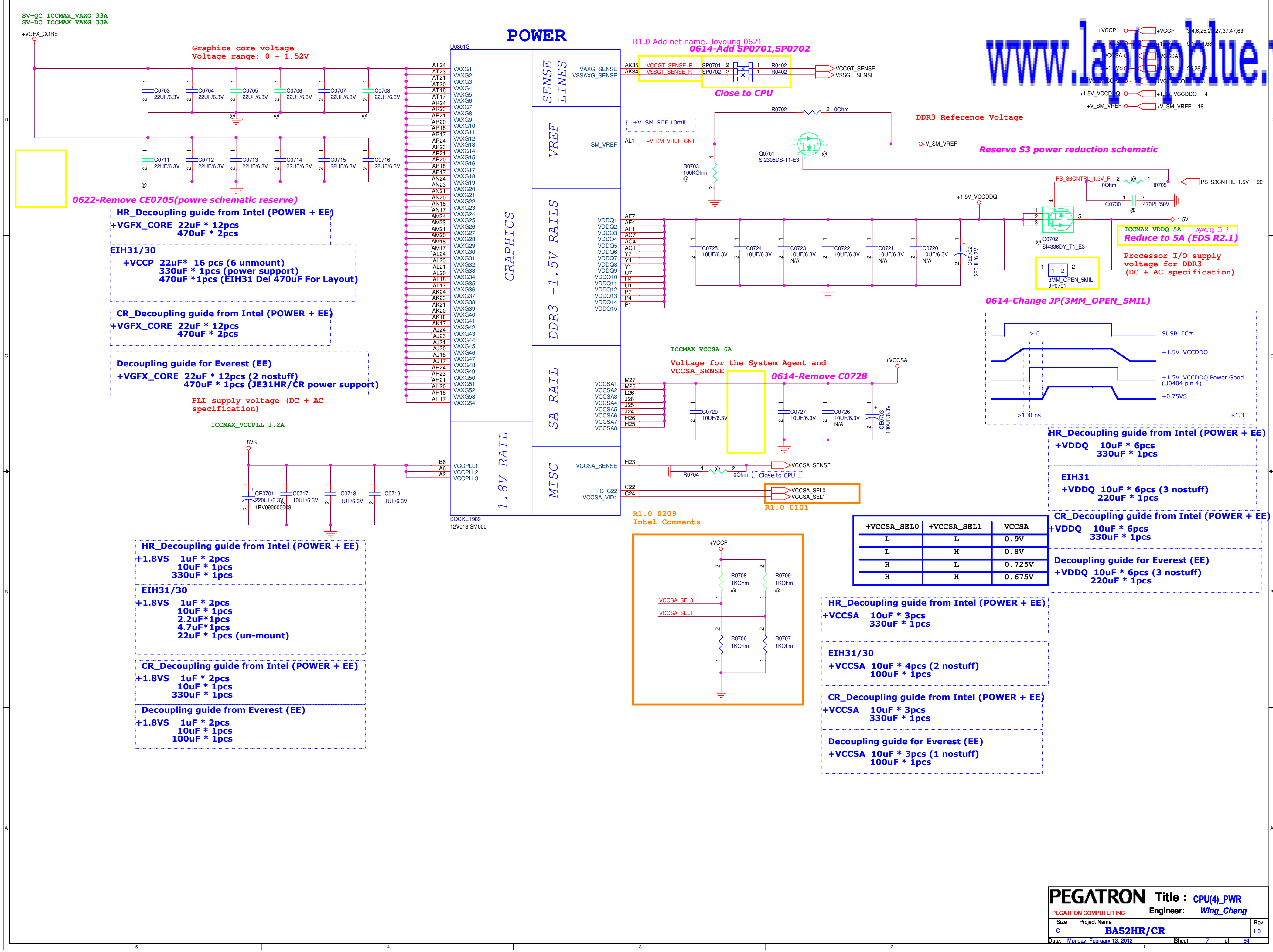
HR_Decoupling guide from Intel (POWER + EE)
+VCC_CORE 22uF * 16pcs
10uF * 10pcs
470uF * 4pcs

EIH31/30
+VCC_CORE 22uF * 14pcs(6pcs unmount)
10uF * 16pcs (4pcs unmount)
470uF * 2pcs (Power support)

CR_Decoupling guide from Intel (POWER + EE)
+VCC_CORE 22uF * 16pcs
10uF * 10pcs
470uF * 4pcs

Decoupling guide for Everest (EE)
+VCC_CORE 22uF * 16pcs (8 nostuff)
10uF * 10pcs (3 nostuff)
470uF * 1pcs=>JE31HR/CR power support

PEGATRON	Title : CPU(4)_PWR		
PEGATRON COMPUTER INC	Engineer: Wing_Cheng		
Size: C	Project Name: BA52HR/CR		Rev: 1.0
Date: Monday, February 13, 2012	Sheet 6 of 94		



SV-QC ICCMAX_VAXG 33A
SV-DC ICCMAX_VAXG 33A
+VGFX_CORE
POWER
U0301G
Graphics core voltage
Voltage range: 0 - 1.52V
C0703 22UF/6.3V
C0704 22UF/6.3V
C0705 22UF/6.3V
C0706 22UF/6.3V
C0707 22UF/6.3V
C0708 22UF/6.3V
C0711 22UF/6.3V
C0712 22UF/6.3V
C0713 22UF/6.3V
C0714 22UF/6.3V
C0715 22UF/6.3V
C0716 22UF/6.3V
0622-Remove CE0705(powre schematic reserve)
GRAPHICS
SENSE LINES
VAXG_SENSE
VSSAXG_SENSE
VREF
SM_VREF
DDR3 -1.5V RAILS
SA RAIL
1.8V RAIL
MISC
VCCSA_SENSE
FC_C22
VCCSA_VID1
SOCKET989
12V013ISM000
R1.0 Add net name, Joyoung 0621
0614-Add SP0701,SP0702
VCCGT_SENSE_R
VSSGT_SENSE_R
VCCGT_SENSE
VSSGT_SENSE
Close to CPU
+V_SM_REF 10mil
+V_SM_VREF_CNT
R0702 0Ohm
R0703 100KOhm
Q0701 SI2308DS-T1-E3
+V_SM_VREF
DDR3 Reference Voltage
Reserve S3 power reduction schematic
PS_S3CNTRL_1.5V_R
R0705 0Ohm
PS_S3CNTRL_1.5V
C0730 470PF/50V
+1.5V_VCCDDQ
Q0702 SI4336DY_T1_E3
+1.5V
ICCMAX_VDDQ 5A
Reduce to 5A (EDS R2.1)
Processor I/O supply voltage for DDR3 (DC + AC specification)
JP0701 3MM_OPEN_5MIL
0614-Change JP(3MM_OPEN_5MIL)
C0725 10UF/6.3V
C0724 10UF/6.3V
C0723 10UF/6.3V N/A
C0722 10UF/6.3V
C0721 10UF/6.3V N/A
C0720 10UF/6.3V N/A
CE0702 220UF/6.3V
SUSB_EC#
+1.5V_VCCDDQ
+1.5V_VCCDDQ Power Good (U0404 pin 4)
+0.75VS
> 0
>100 ns
R1.3
ICCMAX_VCCSA 6A
Voltage for the System Agent and VCCSA_SENSE
0614-Remove C0728
+VCCSA
C0729 10UF/6.3V
C0727 10UF/6.3V
C0726 10UF/6.3V N/A
CE0703 100UF/6.3V
VCCSA_SENSE
R0704 0Ohm
Close to CPU
VCCSA_SEL0
VCCSA_SEL1
R1.0 0101
R1.0 0209
Intel Comments
+VCCP
R0708 1KOhm
R0709 1KOhm
R0706 1KOhm
R0707 1KOhm
PLL supply voltage (DC + AC specification)
ICCMAX_VCCPLL 1.2A
+1.8VS
CE0701 220UF/6.3V 1BV090000003
C0717 10UF/6.3V
C0718 1UF/6.3V
C0719 1UF/6.3V
+VCCP
+VCCSA
+1.5VS
+1.5V_VCCDDQ
+V_SM_VREF
www.laptopblue.vn

HR_Decoupling guide from Intel (POWER + EE)
+VGFX_CORE 22uF * 12pcs
470uF * 2pcs

EIH31/30
+VCCP 22uF* 16 pcs (6 unmount)
330uF * 1pcs (power support)
470uF *1pcs (EIH31 Del 470uF For Layout)

CR_Decoupling guide from Intel (POWER + EE)
+VGFX_CORE 22uF * 12pcs
470uF * 2pcs

Decoupling guide for Everest (EE)
+VGFX_CORE 22uF * 12pcs (2 nostuff)
470uF * 1pcs (JE31HR/CR power support)

HR_Decoupling guide from Intel (POWER + EE)
+1.8VS 1uF * 2pcs
10uF * 1pcs
330uF * 1pcs

EIH31/30
+1.8VS 1uF * 2pcs
10uF * 1pcs
2.2uF*1pcs
4.7uF*1pcs
22uF * 1pcs (un-mount)

CR_Decoupling guide from Intel (POWER + EE)
+1.8VS 1uF * 2pcs
10uF * 1pcs
330uF * 1pcs

Decoupling guide from Everest (EE)
+1.8VS 1uF * 2pcs
10uF * 1pcs
100uF * 1pcs

+VCCSA_SEL0	+VCCSA_SEL1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

HR_Decoupling guide from Intel (POWER + EE)
+VDDQ 10uF * 6pcs
330uF * 1pcs

EIH31
+VDDQ 10uF * 6pcs (3 nostuff)
220uF * 1pcs

CR_Decoupling guide from Intel (POWER + EE)
+VDDQ 10uF * 6pcs
330uF * 1pcs

Decoupling guide for Everest (EE)
+VDDQ 10uF * 6pcs (3 nostuff)
220uF * 1pcs

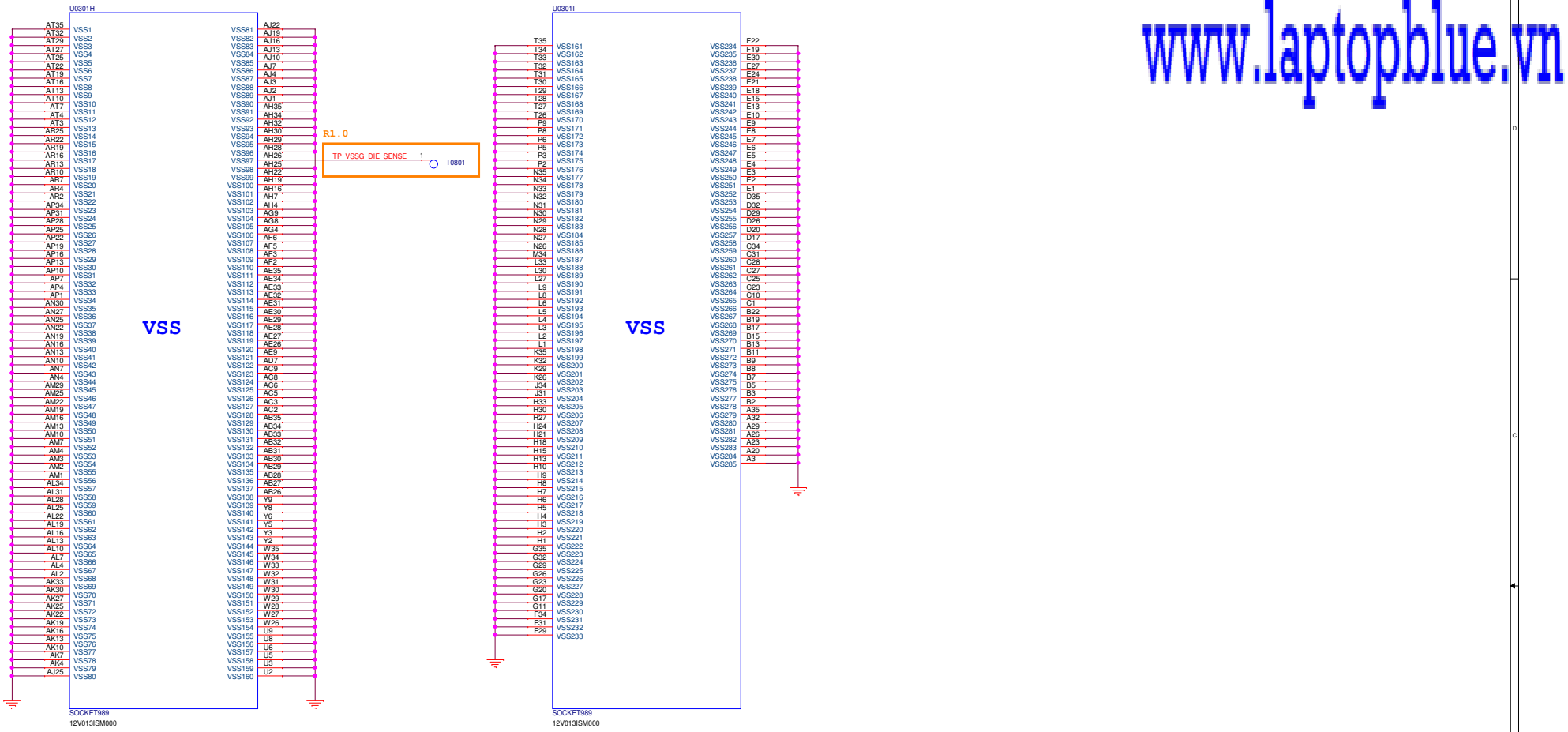
HR_Decoupling guide from Intel (POWER + EE)
+VCCSA 10uF * 3pcs
330uF * 1pcs

EIH31/30
+VCCSA 10uF * 4pcs (2 nostuff)
100uF * 1pcs

CR_Decoupling guide from Intel (POWER + EE)
+VCCSA 10uF * 3pcs
330uF * 1pcs

Decoupling guide for Everest (EE)
+VCCSA 10uF * 3pcs (1 nostuff)
100uF * 1pcs

PEGATRON Title : CPU(4)_PWR
PEGATRON COMPUTER INC Engineer: Wing_Cheng
Size C Project Name BA52HR/CR Rev 1.0
Date: Monday, February 13, 2012 Sheet 7 of 94



PEGATRON Title : CPU(3)_CFG,RSVD,GND

PEGATRON COMPUTER INC Engineer: Wing_Cheng

Size	Project Name	Rev
C	BA52HR/CR	1.0

Date: Monday, February 13, 2012 Sheet 8 of 94

CFG strapping information:

CFG[2]: PCIE Static Numbering Lane Reversal- CFG[2] is for the 16x

- 1: (Default) Normal Operation, Lane # definition matches sockect pin map definition
- 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG[4]: Embedded DisplayPort Detection

- 1: (Default) Disabled ; No Physical Display Port attached to Embedded DisplayPort
- 0: Enabled ; An external Display Port device is connected to the Embedded Display Port

CFG[6:5]: PCI Express Port Bifurcation Straps

- 11 : (Default) x 1 6
- 10 : x 8 , x 8
- 01 : Reserved
- 00 : x 8 , x 4 , x 4

CFG[7]: PEG DEFER TRAINING

- 1: (Default) PEG Train immediately following xxRESETB de assertion
- 0: PEG Wait for BIOS training

R1.0
Add CFG0

Frank
0516 Remove CFGO to XDP

U0301E

TPC26T T0918 1 CFG0 AK28
TPC26T T0917 1 CFG1 AK29
TPC26T T0916 1 CFG2 AL26
TPC26T T0915 1 CFG3 AL27
TPC26T T0914 1 CFG4 AK26
TPC26T T0913 1 CFG5 AL29
TPC26T T0912 1 CFG6 AL30
TPC26T T0911 1 CFG7 AM31
TPC26T T0910 1 CFG8 AM32
TPC26T T0909 1 CFG9 AM30
TPC26T T0908 1 CFG10 AM28
TPC26T T0907 1 CFG11 AM26
TPC26T T0906 1 CFG12 AN28
TPC26T T0905 1 CFG13 AN31
TPC26T T0904 1 CFG14 AN26
TPC26T T0903 1 CFG15 AM27
TPC26T T0902 1 CFG16 AK31
TPC26T T0901 CFG17 AN29

CFG[0] CFG[1] CFG[2] CFG[3] CFG[4] CFG[5] CFG[6] CFG[7] CFG[8] CFG[9] CFG[10] CFG[11] CFG[12] CFG[13] CFG[14] CFG[15] CFG[16] CFG[17]

TPC26T T0953 1 VAXG_VAL_SENSE AJ31
TPC26T T0952 1 VSSAXG_VAL_SENSE AH31
TPC26T T0951 1 VCC_VAL_SENSE AJ33
TPC26T T0950 VSS_VAL_SENSE AH33

RSVD1 RSVD2 RSVD3 RSVD4 AJ26 RSVD5 B4 RSVD6 D1 RSVD7 F25 RSVD8 F24 RSVD9 F23 RSVD10 D24 RSVD11 G25 RSVD12 G24 RSVD13 E23 RSVD14 D23 RSVD15 C30 RSVD16 A31 RSVD17 B30 RSVD18 B29 RSVD19 D30 RSVD20 B31 RSVD21 A30 RSVD22 C29 RSVD23 J20 RSVD24 B18 RSVD25 A19 RSVD26 J15 RSVD27

RESERVED

RSVD28 L7
RSVD29 AG7
RSVD30 AE7
RSVD31 AK2
RSVD32 W8
RSVD33 AT26
RSVD34 AM33
RSVD35 AJ27
RSVD37 T8
RSVD38 J16
RSVD39 H16
RSVD40 G16
RSVD41 AR35
RSVD42 AT34
RSVD43 AT33
RSVD44 AP35
RSVD45 AR34
RSVD46 B34
RSVD47 A33
RSVD48 A34
RSVD49 B35
RSVD50 C35
RSVD51 AJ32
RSVD52 AK32
RSVD53 AH27 TP_VCCG_DIE_SENSE 1 T0954 TPC26T
RSVD54 AN35
RSVD55 AM35
RSVD56 AT2
RSVD57 AT1
RSVD58 AR1
KEY B1

SOCKET989
12V013ISM000

CFG2 R0902 1 1% 2 /DGPU 1KOhm
CFG4 R0903 1 1% 2 1KOhm
CFG5 R0904 1 1% @ 2 1KOhm
CFG6 R0905 1 1% @ 2 1KOhm
CFG7 R0906 1 1% @ 2 1KOhm

This model is UMA, unmount R0902(use Default)

DDR_WR_VREF01
DDR_WR_VREF02

R1.0 0126

1R0909 1% @ 1KOhm
1R0910 1% @ 1KOhm

DIMM0_VREF_DQ_R Pull Down 1k ohm
DIMM1_VREF_DQ_R Pull Down 1k ohm
Design Guide 1.0 P.89 Figure 44 (436735)

Power schematic reserve 1.0V or not??

+VCCIO_SEL	
1	1.05V
0	1.00V

IVB VCCIO for Mobile and Desktop is changed from 1.0v to 1.05v, same as PPT VCCIO. (461017 WW23'11)

R1.0 0111

Delete VCCIO_SEL. Joyoung0614
TPC26T T0955 1 VCCIO_SEL_R

Frank
20110516 Change VCCP_SEL to VCCIO_SEL for meeting Power schematic defined

PROCESSOR DRIVEN Vref PATH WAS STUFFED BY DEFAULT:

R0911 1 @ 2 0Ohm
@ O0901A UM6K1N
DDR_WR_VREF01 1 6 DIMM0_VREF_DQ 18
2
5,21 DRAMRST_CNTRL_PCH

M3 Path:0 Ohm at Page18

R0912 1 @ 2 0Ohm
@ O0901B UM6K1N
DDR_WR_VREF02 4 3 DIMM1_VREF_DQ 18
5

Reserve S3 power reduction schematic

M3: Processor Generated SO-DIMM VREFDQ
– New Requirement

Sandy Bridge CPU Only: M1 Implementation
Sandy Bridge/Ivy Bridge CPU: M1 and M3 Implementation

PEGATRON Title : CPU(3)_CFG,RSVD,GND
PEGATRON COMPUTER INC Engineer: Wing_Cheng
Size C | Project Name BA52HR/CR | Rev 1.0
Date: Monday, February 13, 2012 Sheet 9 of 94

+VTT_PCH_ORG +VTT_PCH_ORG 22,26,27

+3VSUS +3VSUS 4,22,24,27,28,30,33,65

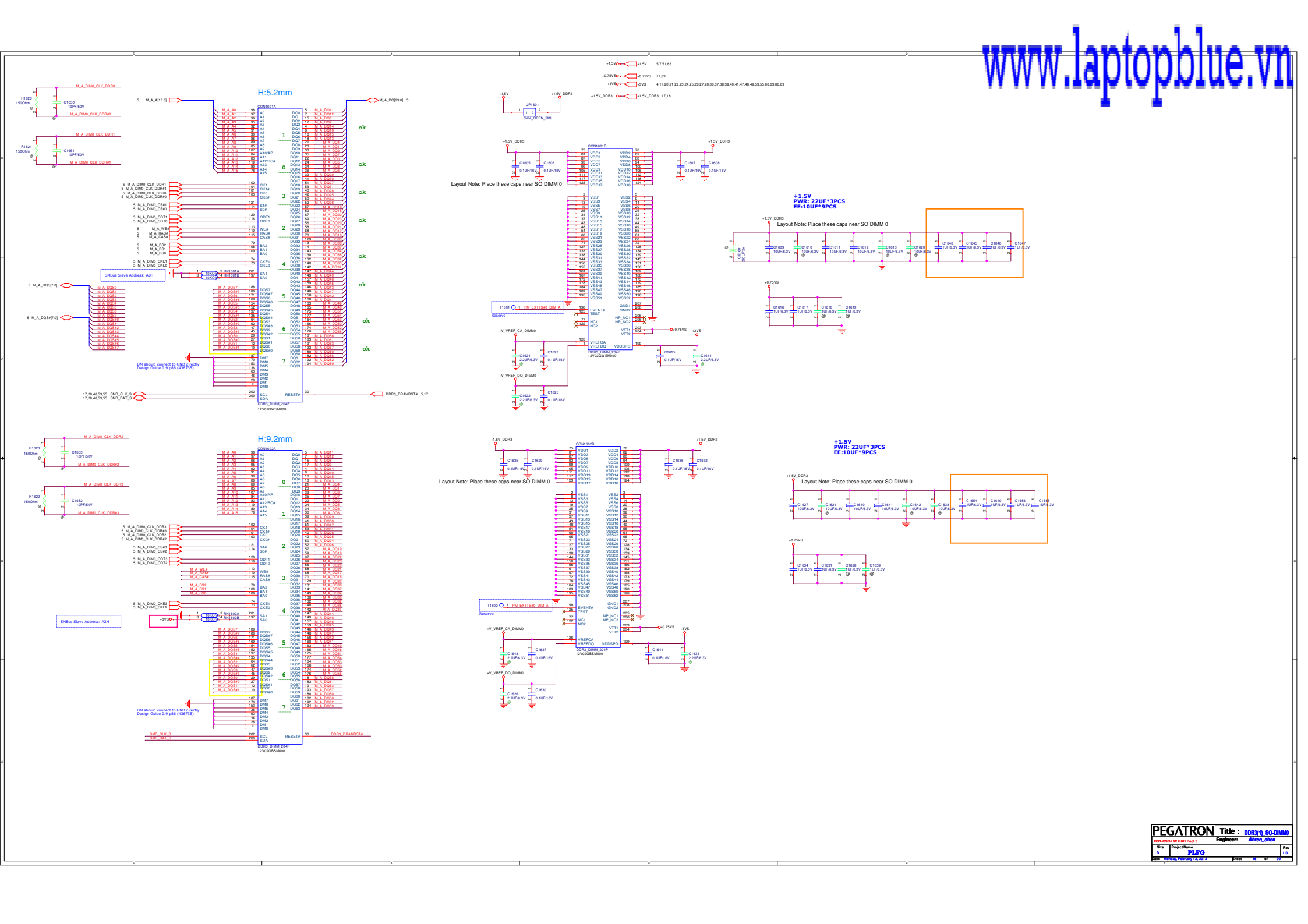
+VCCP +VCCP 3,4,6,7,25,26,27,37,47,63

+3VS +3VS 4,16,17,20,21,22,23,24,25,26,27,28,30,37,38,39,40,41,47,48,49,50,63,65

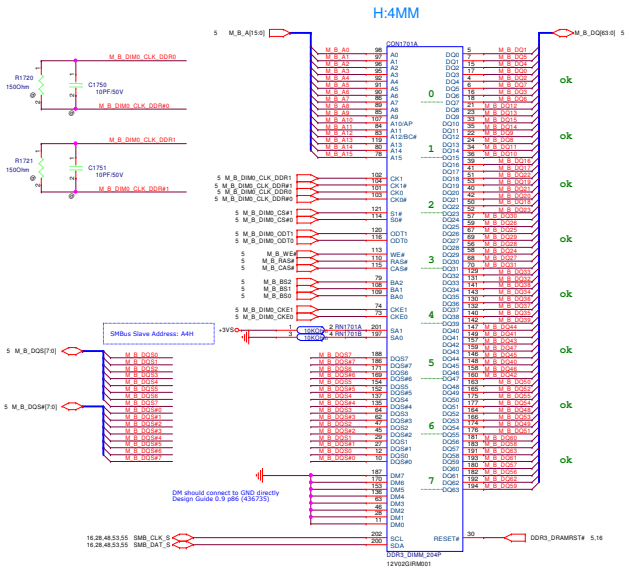
CPU XDP connector

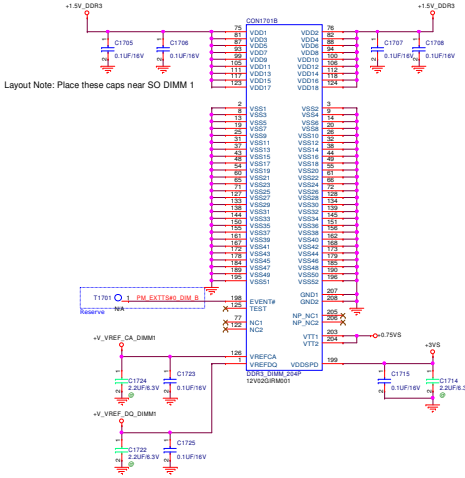
PCH XDP connector

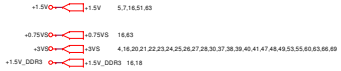
PEGATRON	Title : NB(3)_****	
PEGATRON COMPUTER INC	Engineer: Wing_Cheng	
Size: C	Project Name: BA52HR/CR	Rev: 1.0
Date: Monday, February 13, 2012	Sheet 10 of 99	

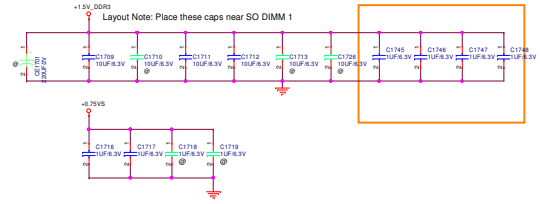


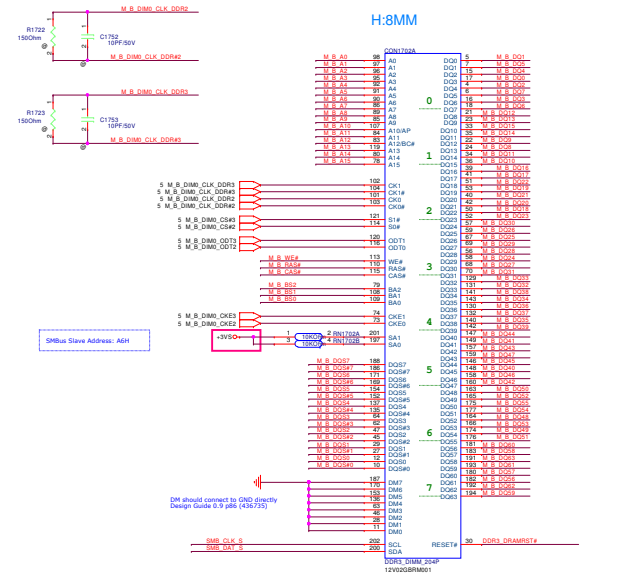
PEGATRON	Title :	DDR3(1)_SO-DIMM0	
SG1-C6C-HW R&D Dept.5	Engineer:	Ahren_chen	
Size: D	Project Name: PLPG		Rev: 1.0
Date: Monday, February 13, 2012	Sheet	16 of 99	

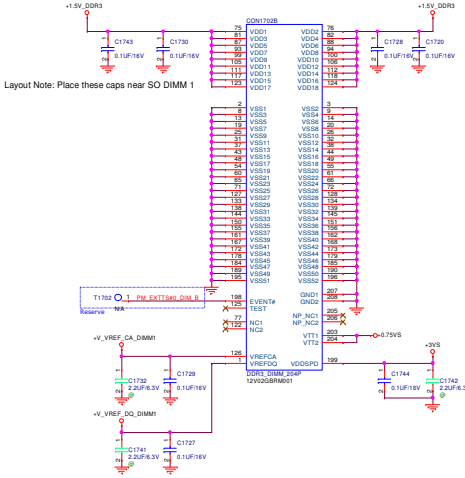


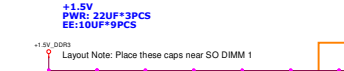






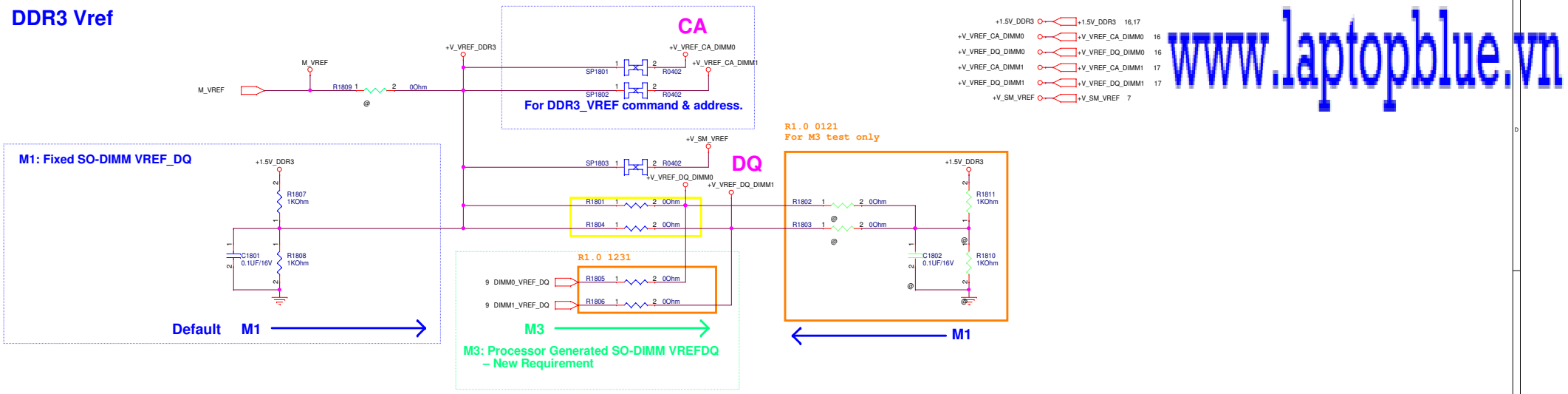






PEGATRON	Title :	DDR3(2)_SO-DIMM1	
BG1-CSC-HW R&D Dept.5	Engineer:	Ahren_chen	
Size: D	Project Name: P1LPG		Rev: 1.0
Date: Monday, February 13, 2012	Sheet: 17	of: 99	

DDR3 Vref



If support M1 :(Sandy Bridge CPU Only)
1. Un mount R1802,R1803,R1805,R1806,R1810,R1811,C1802
2. Mount R1801,R1804
==>CA and DQ are the same path

If support M1 and M3 :(Sandy Bridge/Ivy Bridge CPU)
1. Mount R1802,R1803,R1805,R1806,R1810,R1811,C1802
2. Un mount R1801,R1804
==> CA and DQ are separate path

Sandy Bridge CPU Only: M1 Implementation
Sandy Bridge/Ivy Bridge CPU: M1 and M3 Implementation

PEGATRON	Title : DDR3(3)_CA/DQ Voltage	
PEGATRON COMPUTER INC	Engineer: Wing_Cheng	
Size: C	Project Name: BA52HR/CR	Rev: 1.0
Date: Monday, February 13, 2012	Sheet 18 of 94	

R1.4--2

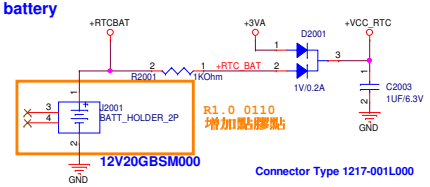
PEGATRON Title : VID Controller

PEGATRON COMPUTER INC Engineer: Wing_Cheng

Size	Project Name	Rev
C	BA52HR/CR	1.0

Date: Monday, February 13, 2012 Sheet 19 of 94

RTC battery



Request by CSC for CMOS clear function

CMOS Settings	JRST2001
Clear CMOS	Shunt
Keep CMOS	Open (Default)

TPM Settings	JRST2002
Clear ME RTC Registers	Shunt
Keep ME RTC Registers	Open (Default)

EMI solution

R1.0 Delete +RTCBAT

+VCC_RTC 22,27
+3VA 27,30,48,63,65
+3VS 4,16,17,21,22,23,24,25,26,27,28,30,37,38,39,40,41,47,48,49,53,55,60,61,66,69
+3VSUS_ORG 21,22,24,25,27
+1.05VM_ORG 27
+VTT_PCH_VCCIO 26,27

RTCRST# RC delay should be 18ms~25ms

INTVRMEN: Integrated SUS 1.05V VRM Enables
Low: Enable External VRs
High:Enable Internal VRs

HDA_DKEN : Flash Descriptor Security Overide
H = Disabled (Default)
L = Enabled

Note : Rising edge of PWROK

R1.0 add JRST3 to follow BIC50. Joyoung 0628

U2001A

RTC: RTCX1 A20, RTCX2 C20, RTCRST# D20, SRTCRST# G22, INTRUDER# K22, INTVRMEN C17
LPC: FWH0/LAD0 C38, FWH1/LAD1 A38, FWH2/LAD2 B37, FWH3/LAD3 C37, FWH4/LFRAME# D36, LDRQ0# E36, LDRQ1#/GPIO23 K36, SERIRQ V5
SATA: SATA0RXN AM3, SATA0RXP AM1, SATA0TXN AP7, SATA0TXP AP5, SATA1RXN AM10, SATA1RXP AM8, SATA1TXN AP11, SATA1TXP AP10, SATA2RXN AD7, SATA2RXP AD5, SATA2TXN AH5, SATA2TXP AH4, SATA3RXN AB8, SATA3RXP AB10, SATA3TXN AF3, SATA3TXP AF1, SATA4RXN Y7, SATA4RXP Y5, SATA4TXN AD3, SATA4TXP AD1, SATA5RXN Y3, SATA5RXP Y1, SATA5TXN AB3, SATA5TXP AB1, SATAICOMPO Y11, SATAICOMPI Y10, SATA3RCOMPO AB12, SATA3COMPI AB13, SATA3RBIAS AH1, SATALED# P3, SATA0GP/GPIO21 V14, SATA1GP/GPIO19 P1
IHDA: HDA_BCLK N34, HDA_SYNC L34, SPKR T10, HDA_RST# K34, HDA_SDIN0 E34, HDA_SDIN1 G34, HDA_SDIN2 C34, HDA_SDIN3 A34, HDA_SDO A36, HDA_DOCK_EN#/GPIO33 C36, HDA_DOCK_RST#/GPIO13 N32
JTAG: JTAG_TCK, JTAG_TMS H7, JTAG_TDI K5, JTAG_TDO H1
SPI: SPI_CLK T3, SPI_CS0# Y14, SPI_CS1# T1, SPI_MOSI V4, SPI_MISO U3
COUGAR_POINT_ES1
02V000000001

0200-00HU000 C.S 907552 A1 QMVY BGA942 INTEL/COUGAR POINT PCH

Strap information:

SB_SPKR: No reboot strap
Low: Disable (Default)
High:Enable

ACZ_SDOUT:
1.Flash descriptor security:
Sampled Low: in effect.
Sampled High: override
2.ACZ_SDOUTwhich sample high on the rising edge of PWROK
Will also disable Intel ME.

ACZ_SYNC: On Die PLL VR voltage selector
Low: 1.8V (Default)
High: 1.5V
note : CRB has no strap
Hrron River Platform Schematic Design Checklist (438390 page 48)

VCCVRAM use +1.5VS in mobile

Pull High

PEGATRON	Title : PCH(1)_SATA,IHDA,RTC,LPC	
PEGATRON COMPUTER INC	Engineer: Wing_Cheng	
Size: C	Project Name: BA52HR/CR	Rev: 1.0
Date: Monday, February 13, 2012	Sheet 20 of 94	

+3VS → +3VS 4,16,17,20,22,23,24,25,26,27,28,30,37,38,39,40,41,47,48,49,53,5,60,63,66,69
+VTT_PCH_ORG → +VTT_PCH_ORG 22,26,27
+3VSUS_ORG → +3VSUS_ORG 20,22,24,25,27

U2001B

PCI-E*
SMBUS
Controller Link
CLOCKS
FLEX CLOCKS
COUGAR_POINT_ES1

40 PCIE_RXN1_CR
40 PCIE_RXP1_CR
40 PCIE_TXN1_CR
40 PCIE_TXP1_CR
C2107 0.1UF/16V PCIE_TXN1_CR_C
C2114 0.1UF/16V PCIE_TXP1_CR_C
BG34 BJ34 AV32 AU32
PERn1 PERp1 PETn1 PETp1

55 PCIE_RXN2_WLAN
55 PCIE_RXP2_WLAN
55 PCIE_TXN2_WLAN
55 PCIE_TXP2_WLAN
C2103 0.1UF/16V PCIE_TXN2_WLAN_C
C2104 0.1UF/16V PCIE_TXP2_WLAN_C
BE34 BF34 BB32 AY32
PERn2 PERp2 PETn2 PETp2

53 PCIE_RXN3_mSATA
53 PCIE_RXP3_mSATA
53 PCIE_TXN3_mSATA
53 PCIE_TXP3_mSATA
C2106 0.1UF/16V PCIE_TXN3_mSATA_C
C2105 0.1UF/16V PCIE_TXP3_mSATA_C
BG36 BJ36 AV34 AU34
PERn3 PERp3 PETn3 PETp3

51 PCIE_RXN_USB30
51 PCIE_RXP_USB30
51 PCIE_TXN_USB30
51 PCIE_TXP_USB30
C2108 0.1UF/16V PCIE_TXN4_USB30_C
C2113 0.1UF/16V PCIE_TXP4_USB30_C
/FL1009
/FL1009
BF36 BE36 AY34 BB34
PERn4 PERp4 PETn4 PETp4

BG37 BH37 AY36 BB36
PERn5 PERp5 PETn5 PETp5

33 PCIE_RXN6_LAN
33 PCIE_RXP6_LAN
33 PCIE_TXN6_LAN
33 PCIE_TXP6_LAN
C2110 0.1UF/16V PCIE_TXN6_GLAN_C
C2111 0.1UF/16V PCIE_TXP6_GLAN_C
BJ38 BG38 AU36 AV36
PERn6 PERp6 PETn6 PETp6

BG40 BJ40 AY40 BB40
PERn7 PERp7 PETn7 PETp7

BE38 BC38 AW38 AY38
PERn8 PERp8 PETn8 PETp8

SMBALERT#/GPIO11 E12 EXT_SCI# → EXT_SCI# 30
SMBCLK H14 SCL_3A → SCL_3A 28
SMBDATA C9 SDA_3A → SDA_3A 28

SML0ALERT#/GPIO60 A12 DRAMRST_CNTRL_PCH → DRAMRST_CNTRL_PCH 5,9
SML0CLK C8 SML0_CLK → T2133
SML0DATA G12 SML0_DAT → T2134

SML1ALERT#/PCHHOT#/GPIO74 C13 SML1ALERT# → T2121
SML1CLK/GPIO58 E14 SML1_CLK → SML1_CLK 28
SML1DATA/GPIO75 M16 SML1_DAT → SML1_DAT 28

CL_CLK1 M7 → T2135
CL_DATA1 T11 → T2136
CL_RST1# P10 → T2137

T2110 CLK_PCH_SRC0_N
T2111 CLK_PCH_SRC0_P
CLKOUT_PCIE0N CLKOUT_PCIE0P 100MHz
T2103 CLK_REQ0# → J2
PCIECLKRQ0#/GPIO73

40 CLK_PCIE_CR#_PCH
40 CLK_PCIE_CR_PCH
SP2117 CLK_PCH_SRC1_N
SP2118 CLK_PCH_SRC1_P
CLKOUT_PCIE1N CLKOUT_PCIE1P 100MHz
AB49 AB47
40 CLK_REQ1_CR# SP2112 CLK_REQ1# M1
PCIECLKRQ1#/GPIO18

55 CLK_PCIE_WLAN#_PCH
55 CLK_PCIE_WLAN_PCH
SP2101 SP2102 R0402 CLK_PCH_SRC2_N CLK_PCH_SRC2_P
CLKOUT_PCIE2N CLKOUT_PCIE2P 100MHz
AA48 AA47
55 CLK_REQ2_WLAN# SP2103 R0402 CLK_REQ2# → V10
PCIECLKRQ2#/GPIO20

53 CLK_PCIE_mSATA#_PCH
53 CLK_PCIE_mSATA_PCH
SP2104 SP2105 R0402 CLK_PCH_SRC3_N CLK_PCH_SRC3_P
CLKOUT_PCIE3N CLKOUT_PCIE3P 100MHz
Y37 Y36
53 CLK_REQ3_PCIE_mSATA# SP2106 R0402 CLK_REQ3# → A8
PCIECLKRQ3#/GPIO25

4.USB3.0
51 CLK_PCIE_USB#_PCH
51 CLK_PCIE_USB_PCH
SP2119 SP2120 CLK_PCH_SRC4_N CLK_PCH_SRC4_P
CLKOUT_PCIE4N CLKOUT_PCIE4P 100MHz
Y43 Y45
51 CLK_REQ_USB30# SP2113 CLK_REQ4# → L12
PCIECLKRQ4#/GPIO26

T2125 CLK_PCH_SRC5_N
T2126 CLK_PCH_SRC5_P
CLKOUT_PCIE5N CLKOUT_PCIE5P 100MHz
V45 V46
T2127 CLK_REQ5# → L14
PCIECLKRQ5#/GPIO44

T2116 CLK_PCH_PEG_B_N
T2117 CLK_PCH_PEG_B_P
CLKOUT_PEG_B_N CLKOUT_PEG_B_P 100MHz
AB42 AB40
T2112 CLK_REQ_PEG_B# → E6
PEG_B_CLKRQ#/GPIO56

33 CLK_PCIE_LAN#
33 CLK_PCIE_LAN
SP2107 SP2108 R0402 CLK_PCH_SRC6_N CLK_PCH_SRC6_P
CLKOUT_PCIE6N CLKOUT_PCIE6P 100MHz
V40 V42
33 CLK_REQ6_LAN# SP2109 R0402 CLK_REQ6# → T13
PCIECLKRQ6#/GPIO45

T2123 CLK_PCH_SRC7_N
T2124 CLK_PCH_SRC7_P
CLKOUT_PCIE7N CLKOUT_PCIE7P 100MHz
V38 V37
T2118 CLK_REQ7# → K12
PCIECLKRQ7#/GPIO46

R1.0 Remove PCIE_CLK_XDP 0602
AK14 AK13
CLKOUT_ITPXDP_N CLKOUT_ITPXDP_P 100MHz

02V000000001

PEG_A_CLKRQ#/GPIO47 M10 CLK_REQ_PEG_A# SP2114 R0402 → CLKREQ_PEG# 70
100MHz CLKOUT_PEG_A_N CLKOUT_PEG_A_P AB37 AB38 CLK_PCIE_PEG#_PCH_L CLK_PCIE_PEG_PCH_L SP2115 SP2116 R0402 R0402 → CLK_PCIE_PEG#_PCH 70 CLK_PCIE_PEG_PCH 70
100MHz CLKOUT_DMI_N CLKOUT_DMI_P AV22 AU22 → CLK_EXP_N 4 CLK_EXP_P 4
120MHz CLKOUT_DP_N CLKOUT_DP_P AM12 AM13 CLK_DP_N CLK_DP_P → CLK_DP_N 4 CLK_DP_P 4
100MHz CLKIN_DMI_N CLKIN_DMI_P BF18 BE18 CLK_BUF_EXP_N CLK_BUF_EXP_P
CLKIN_GND1_N CLKIN_GND1_P BJ30 BG30 CLK_BUF_CPYCLK_N CLK_BUF_CPYCLK_P
96MHz CLKIN_DOT_96N CLKIN_DOT_96P G24 E24 CLK_BUF_DOT96_N CLK_BUF_DOT96_P
100MHz CLKIN_SATA_N CLKIN_SATA_P AK7 AK5 CLK_BUF_CKSSCD_N CLK_BUF_CKSSCD_P
14.31818MHz REFCLK14IN K45 CLK_BUF_REF14
33MHz CLKIN_PCILOOPBACK H45 → CLK_PCI_FB 24
XTAL25_IN XTAL25_OUT V47 V49 XTAL25_IN XTAL25_OUT
XCLK_RCOMP Y47 XCLK_COMP R2106 90.9Ohm → +VCCDIFFCLKN

C2101 10PF/50V → GND
R2142 1MOhm
X2103 25MHZ
C2102 10PF/50V → GND
R0402 SP2111

FLEX CLOCKS
CLKOUTFLEX0/GPIO64 K43 DGPU_EDID_SELECT# → T2122
CLKOUTFLEX1/GPIO65 F47 CLK_OUT1 → T2141
CLKOUTFLEX2/GPIO66 H47 CLK_OUT2 → T2139
CLKOUTFLEX3/GPIO67 K49 DGPU_PRSNT# → T2140

CLK_BUF_CPYCLK_N RN2109B 10KOhm
CLK_BUF_CPYCLK_P RN2109A 10KOhm
CLK_BUF_EXP_N RN2109A 10KOhm
CLK_BUF_EXP_P RN2109B 10KOhm
CLK_BUF_DOT96_N RN2110A 10KOhm
CLK_BUF_DOT96_P RN2110B 10KOhm
CLK_BUF_CKSSCD_N RN2111B 10KOhm
CLK_BUF_CKSSCD_P RN2111A 10KOhm
CLK_BUF_REF14 R2116 10KOhm → GND
CLOCK TERMINATION for FCIM
Default power-on mode is ICC.

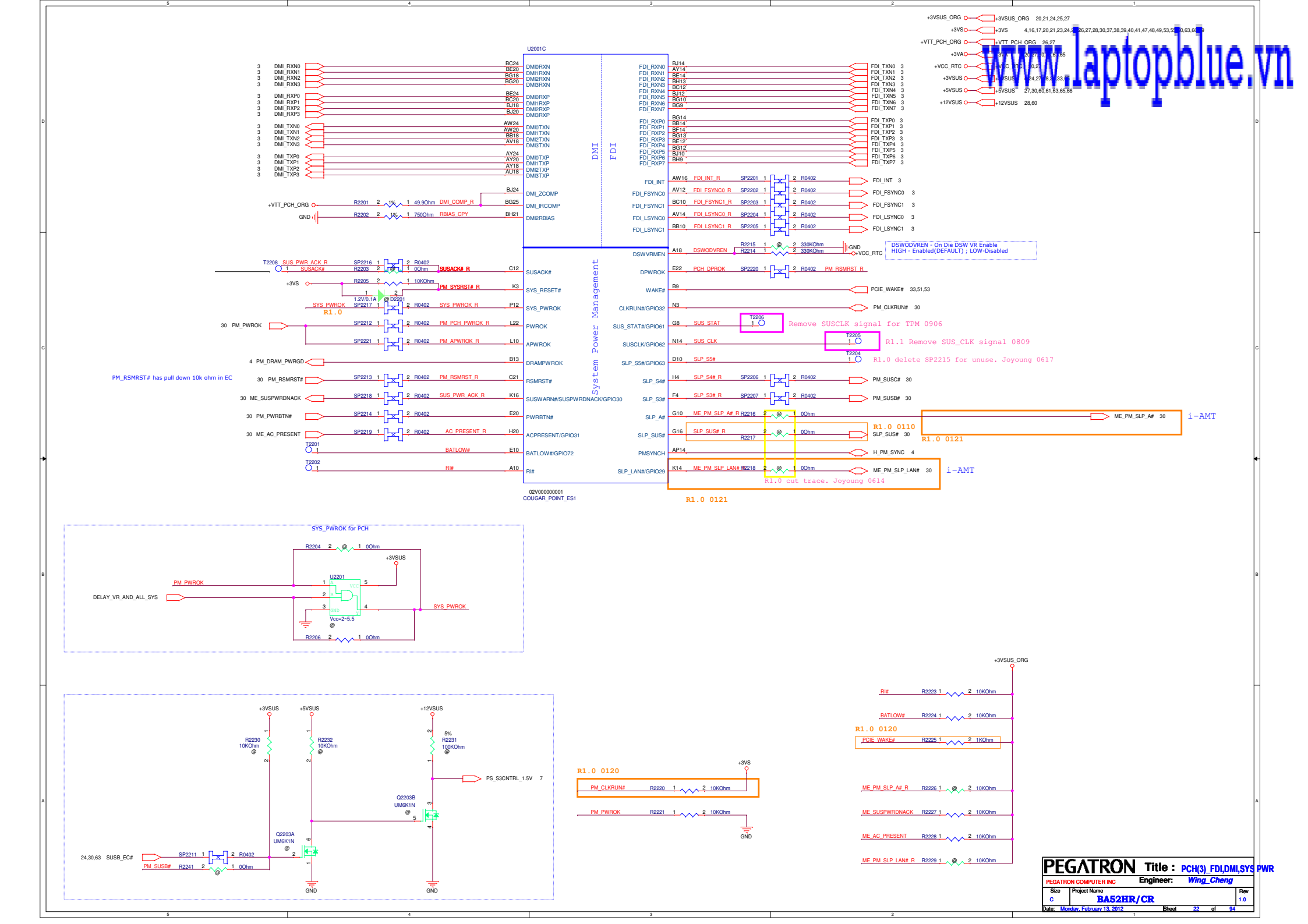
+3VSUS_ORG
EXT_SCI# R2117 10KOhm
SCL_3A RN2103B 2.2KOhm
SDA_3A RN2103A 2.2KOhm
DRAMRST_CNTRL_PCH R2120 1KOhm
SML0_CLK RN2104B 2.2KOhm
SML0_DAT RN2104A 2.2KOhm
SML1_CLK RN2105B 2.2KOhm
SML1_DAT RN2105A 2.2KOhm
SML1ALERT# R2125 10KOhm

+3VS
DGPU_EDID_SELECT# R2144 @ 10KOhm
DGPU_PRSNT# R2126 UMA 10KOhm
DGPU_PRSNT# R2134 /DGPU 10KOhm → GND

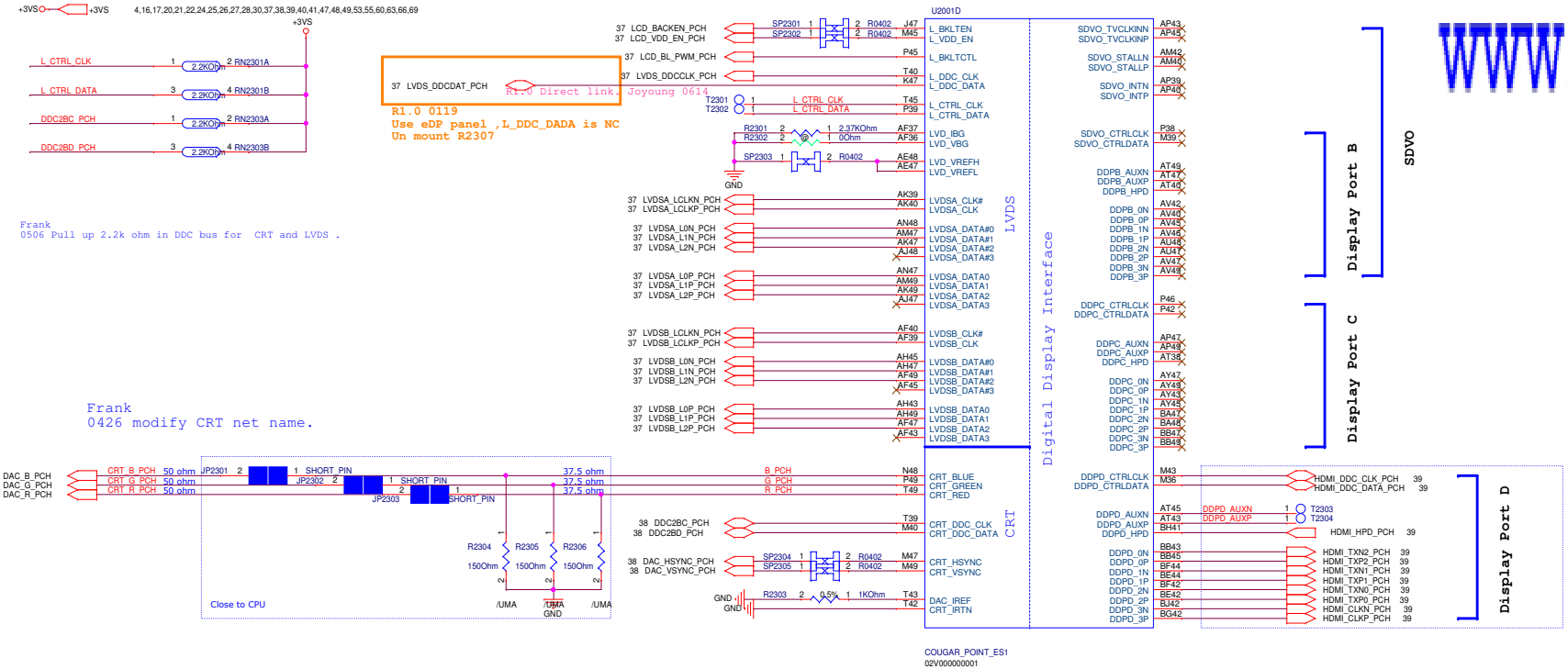
PCH CLKREQ Setting:
Not connected to device.
R1.0 0118
+3VSUS_ORG
CLK_REQ6_LAN# R2149 10KOhm
CLK_REQ0# R2154 10KOhm
CLK_REQ3# R2156 @ 10KOhm
R1.0 CLK_REQ3# is change to +3VSUS 0609
CLK_REQ4# R2157 10KOhm
CLK_REQ5# R2158 10KOhm
CLK_REQ7# R2159 10KOhm
CLK_REQ_PEG_B# R2160 10KOhm
CLK_REQ_PEG_A# R2161 10KOhm

Connected to device.
+3VS
CLK_REQ2_WLAN# R2133 @ 10KOhm
CLK_REQ1# R2155 @ 10KOhm
CLK_REQ4# R2145 @ 10KOhm
CLK_REQ6_LAN# R2143 @ 10KOhm
CLK_REQ2_WLAN# R2138 10KOhm
CLK_REQ3# R2162 10KOhm
CLK_REQ1# R2166 10KOhm → GND

PEGATRON
PEGATRON COMPUTER INC
Title : PCH(2)_PCIE,CLK,SMB,PEG
Engineer: Wing_Cheng
Size C
Project Name BA52HR/CR
Rev 1.0
Date: Monday, February 13, 2012
Sheet 21 of 94



PEGATRON	Title :	PCH(3)_FDI,DMI,SYS PWR	
PEGATRON COMPUTER INC	Engineer:	Wing_Cheng	
Size: C	Project Name: BA52HR/CR		Rev: 1.0
Date: Monday, February 13, 2012	Sheet 22 of 94		



CRT Disable: (For discrete graphic)

1. NC:

CRT_RED,CRT_GREEN,CRT_BLUE

CRT_HSYCN,CRT_VSYNC

2. 1-kΩ ±0.5% pull-down to GND:

DAC_IREF

3. Connected to GND:

CRT_ITRN

4. Connect to +V3.3:

VCCADAC

DisPlay Port Disable: (For discrete graphic)

1. NC:

ALL

LVDS Disable: (For discrete graphic)

1. NC:

LVDSA_DATA [3:0], LVDSA_DATA# [3:0],

LVDSA_CLK, LVDSA_CLK#, LVDSB_DATA [3:0],

LVDSB_DATA# [3:0], LVDSB_CLK, LVDSB_CLK#

L_VDD_EN, L_BKLTEN, L_BKLTCTL, LVD_VREFH

LVD_VREFL, LVD_IBG, LVD_VBG

2. Connected to GND:

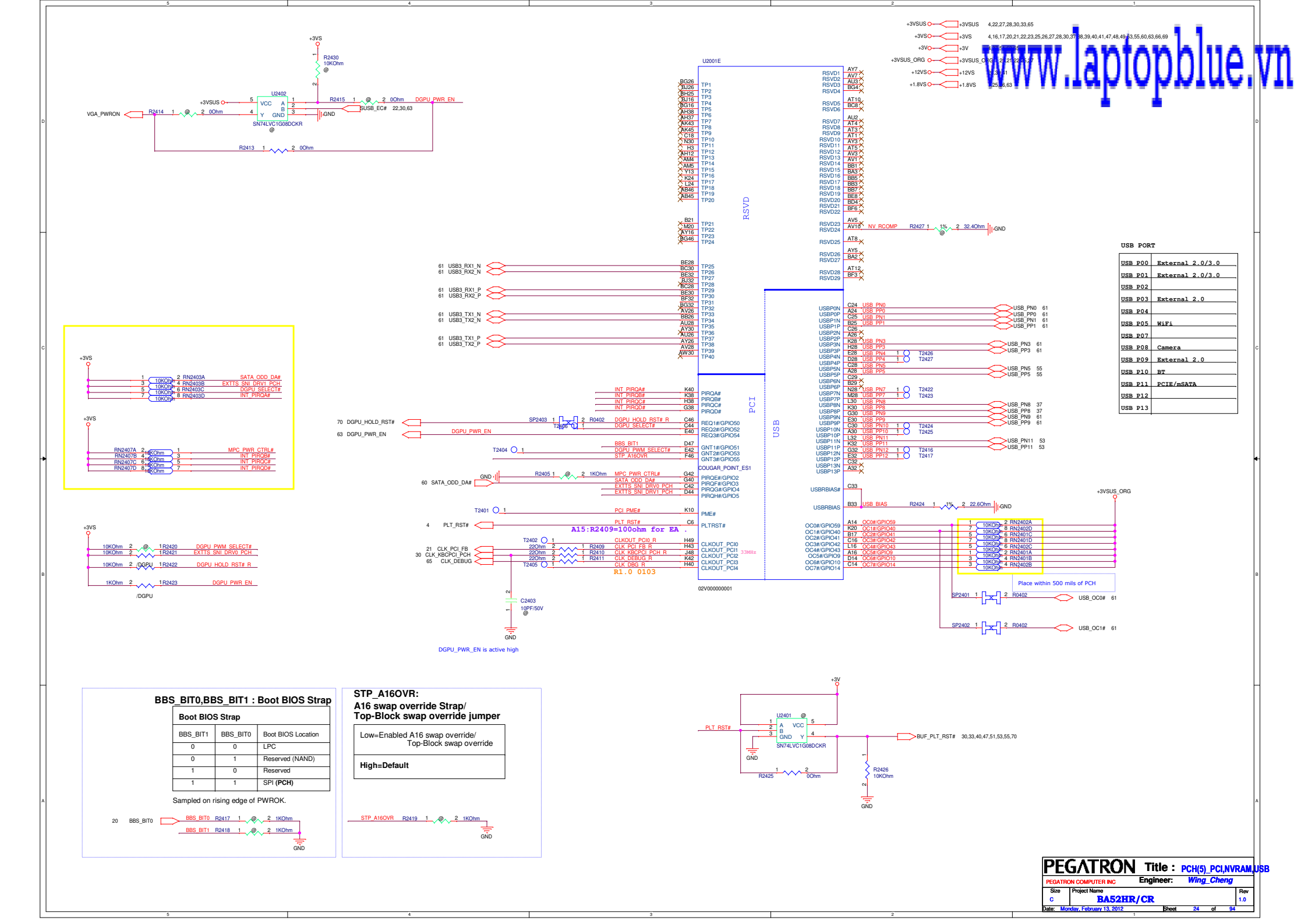
VccALVDS,VccTX_LVDS

PEGATRON Title : PCH(4)_DP,LVDS,CRT

PEGATRON COMPUTER INC Engineer: Wing_Cheng

Size	Project Name	Rev
C	BA52HR/CR	1.0

Date: Monday, February 13, 2012 Sheet 23 of 94



	PCB_ID1	PCB_ID0
A	L	L
B	L	H
C	H	L
MP		

R1.0

Add PCH_GPIO0_R.

Delete ICC_EN#.

Add PM_LANPHY_EN

Add HOST_ALERT#1_R.

Add SATA_DET#4_R.

DGPU_PWROK has 100 ms software delay , no hardware delay requirement

Reserve PCH_GPIO24

Add PLL_ODVR_EN.

Add PSATA_PWR_EN#1_R.

Add SATA_ODD_PRSNT#_R and FDI_OVRVLTG.

Add CRIT_TEMP_REP#_R.

+3VS 4,16,17,20,21,22,23,24,26,27,28,30,37,38,39,40,41,47,48,49,53,55,60,63,66,69

+3VSUS 4,22,24,27,28,30,33,65

+3VSUS_ORG +3VSUS_ORG 20,2[illegible]

R2525 10KOhm PCB_ID0

R2527 10KOhm PCB_ID1

R2526 10KOhm

R2528 10KOhm

GND GND

Frank
0502 Modify PCB_ID

U2001F

69 GSENSOR_INT1_PCH — R2501 100Ohm — PCH_GPIO0_R — T7 BMBUSY#/GPIO0

GPIO1 — A42 TACH1/GPIO1

T2503 — DGPU_HPD_INTR# — H36 TACH2/GPIO6

37 eDP_ON# — eDP_ON# — E38 TACH3/GPIO7

51 USB30_EXT_SMI# — USB30_EXT_SMI# — C10 GPIO8

53,55 WLAN_RST#_PCH — SP2502 R0402 — PM_LANPHY_EN — C4 LAN_PHY_PWR_CTRL/GPIO12

30,65 EXT_SMI# — SP2501 R0402 — HOST_ALERT#1_R — G2 GPIO15

SATA_DET#4 — U2 SATA4GP/GPIO16

DGPU_PWROK — DGPU_PWROK — D40 TACH0/GPIO17

66 WLAN_LED — WLAN_LED — T5 SCLOCK/GPIO22

T2509 — LAN_LPWR — SP2504 R0402 — PCH_GPIO24 — E8 GPIO24/MEM_LED

GPIO27 — E16 GPIO27

WLAN_ON_R — P8 GPIO28

STP_PCI# — K1 STP_PCI#/GPIO34

T2510 — SATA_PWR_EN#1_R — K4 GPIO35

60 SATA_ODD_PRSNT# — SP2503 R0402 — SATA_ODD_PRSNT#_R — V8 SATA2GP/GPIO36

FDI_OVRVLTG — M5 SATA3GP/GPIO37

PCB_ID0 — N2 SLOAD/GPIO38

PCB_ID1 — M3 SDATAOUT0/GPIO39

55 BT_ON_PCH — V13 SDATAOUT1/GPIO48

30 PCH_ALERT# — SP2505 R0402 — CRIT_TEMP_REP#_R — V3 SATA5GP/GPIO49

T2508 — BT_LED — D6 GPIO57

GPIO

TACH4/GPIO68 — C40 — SATA_ODD_PWRGT 60

TACH5/GPIO69 — B41 — R2511 1% 1.5KOhm — GND

TACH6/GPIO70 — C41 — R2512 1% 1.5KOhm — +3VS

TACH7/GPIO71 — A40 — R2513 1% 1.5KOhm — +3VS

need close to EC

CPU/MISC

A20GATE — P4 — A20GATE 30

PECI — AU16 H_PECI_R — 0Ohm — R2514 — 43Ohm — R2515 — H_PECI 4 / H_PECI_EC 30

RCIN# — P5 — RCIN# 30

PROCPWRGD — AY11 — H_CPUPWRGD 4

THRMTRIP# — AY10 PM_THRMTRIP# — 390Ohm 1% R2516 — R2517 56Ohm — H_THRMTRIP# 4,47 — VCCP

INIT3_3V# — T14 INIT3_3V# — T2504

DF_TVS — AY1 NV_CLE — R2502 1KOhm — R2503 2.2KOhm — H_SNB_IVB# 4 — +1.8VS

TS_VSS1 — AH8

TS_VSS2 — AK11

TS_VSS3 — AH10

TS_VSS4 — AK10

NC_1 — P37 — GND

TS Signal Disable Guideline
TS_VSS[1:4] should pull down to GND
Design Guide 0.9 (436735)

Vss_NCTF1 — A4

Vss_NCTF2 — A44

Vss_NCTF3 — A45

Vss_NCTF4 — A46

Vss_NCTF5 — A5

Vss_NCTF6 — A6

Vss_NCTF7 — B3

Vss_NCTF8 — B47

Vss_NCTF9 — BD1

Vss_NCTF10 — BD49

Vss_NCTF11 — BE1

Vss_NCTF12 — BE49

Vss_NCTF13 — BF1

Vss_NCTF14 — BF49

NCTF

Vss_NCTF15 — BG2

Vss_NCTF16 — BG48

Vss_NCTF17 — BH3

Vss_NCTF18 — BH47

Vss_NCTF19 — BJ4

Vss_NCTF20 — BJ44

Vss_NCTF21 — BJ45

Vss_NCTF22 — BJ46

Vss_NCTF23 — BJ5

Vss_NCTF24 — BJ6

Vss_NCTF25 — C2

Vss_NCTF26 — C48

Vss_NCTF27 — D1

Vss_NCTF28 — D49

Vss_NCTF29 — E1

Vss_NCTF30 — E49

Vss_NCTF31 — F1

Vss_NCTF32 — F49

COUGAR_POINT_ES1 02V000000001

+3VSUS_ORG

R1.0 0126 Intel Comments

EXT_SMI# R2529 2K 1KOhm

USB30_EXT_SMI# R2531 2K 10KOhm

PM_LANPHY_EN R2538 2K @ 10KOhm

PCH_GPIO24 R2541 2K 10KOhm — R1.0 0120

R1.0 mount R2541 for LAN_LPWR 0615

RCIN# has pull high at EC side

DGPU_HPD_INTR# R2534 2K 10KOhm

PCH_ALERT# R2535 2K 10KOhm — R1.0 0119

DGPU_PWROK R2539 2K 10KOhm

eDP_ON# R2547 2K 10KOhm

Unused GPIO

GSENSOR_INT1_PCH R2536 2K 10KOhm

GPIO1 R2545 2K @ 10KOhm — R1.0 0119

STP_PCI# R2537 2K 10KOhm

SATA_DET#4 R2546 2K 10KOhm

GPIO27 R2548 2K 10KOhm

#438390 Checklist

GND

R1.0 REMOVE DGPU_PWROK schematic 0602

DGPU_PWROK R2540 2K @ 1 10KOhm

GND

+3VS +3VS

R2549 10KOhm @

R2550 10KOhm @

53,55 WLAN_ON

Q2501B UM6K1N @

Q2501A UM6K1N @

WLAN_ON_R

GND GND

+3VS R2518 1% @ 1KOhm FDI_OVRVLTG R2519 100KOhm GND

FDI TERMINATION VOLTAGE OVERRIDE
- GPIO37 (FDI_OVRVLTG)
LOW - TX, RX terminated to same voltage
(DC Couplong Mode)
DEFAULT

+3VS R2520 1% 200KOhm SATA_ODD_PRSNT#_R

DMI TERMINATION VOLTAGE OVERRIDE
- GPIO36 (SATA_ODD_PRSNT#)
LOW - TX, RX terminated to same voltage
(DC Couplong Mode)
DEFAULT

WLAN_ON_R R2521 @ 1KOhm GND

PLL ON DIE VR ENABLE
HIGH - DISABLED (DEFAULT)
LOW - ENABLED

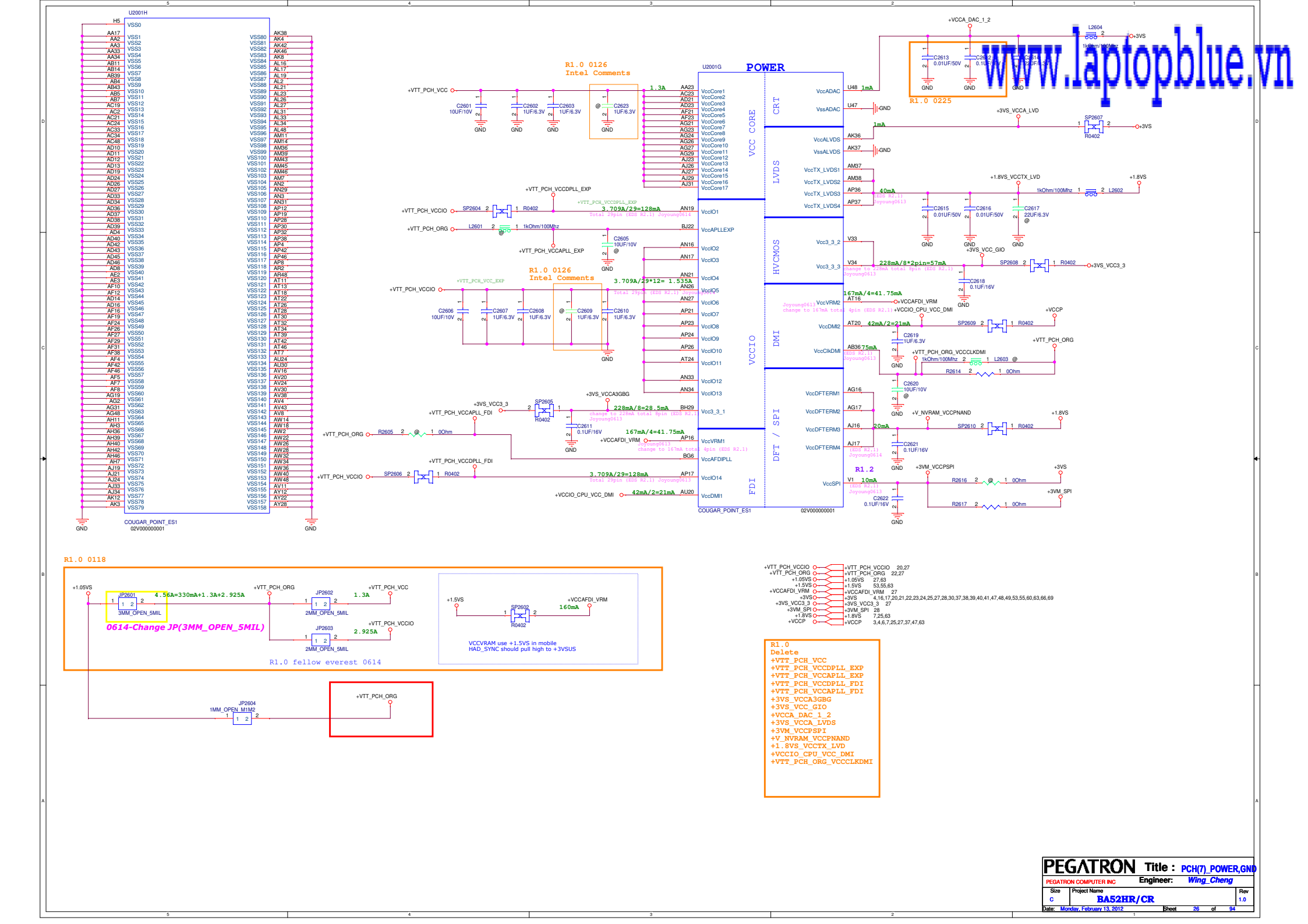
R1.0 Change net name for single net. Joyoung 0621

PEGATRON Title : PCH(6)_CPU,GPIO,MISC

PEGATRON COMPUTER INC Engineer: Wing_Cheng

Size	Project Name	Rev
C	BA52HR/CR	1.0

Date: Monday, February 13, 2012 Sheet 25 of 94

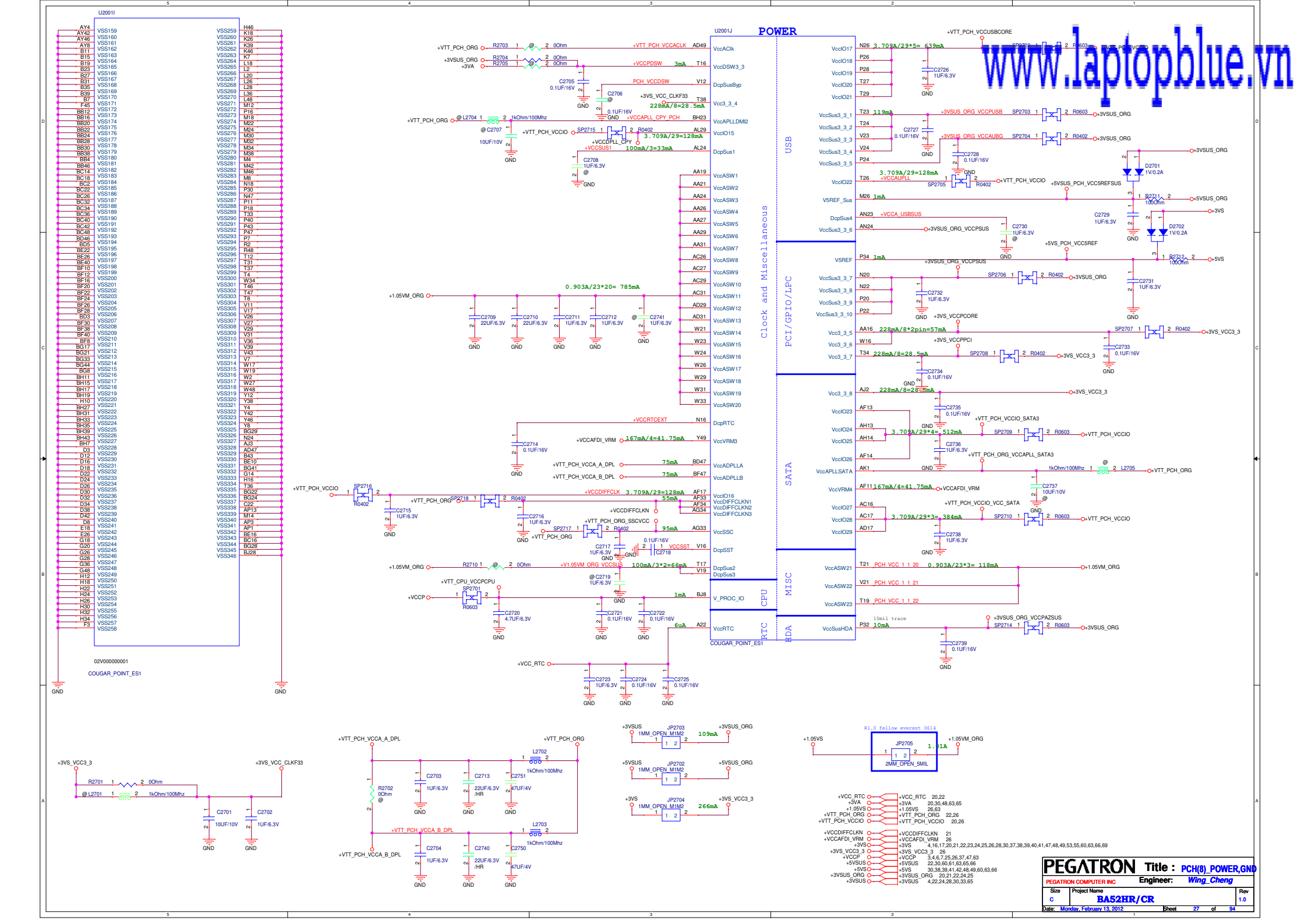


PEGATRON Title : PCH(7)_POWER,GND

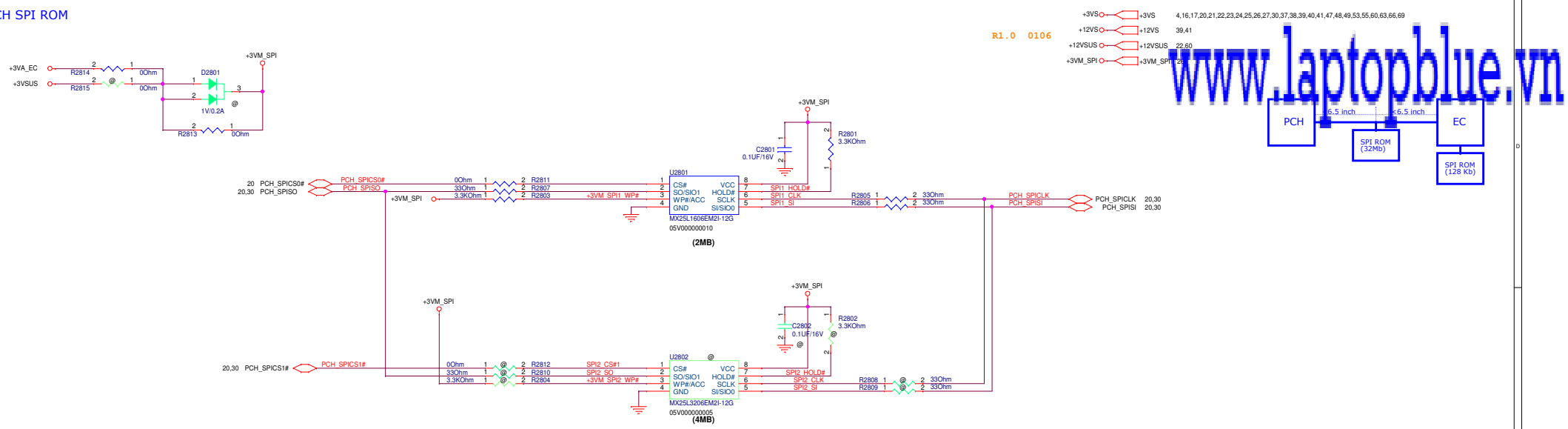
PEGATRON COMPUTER INC Engineer: Wing_Cheng

Size	Project Name	Rev
C	BA52HR/CR	1.0

Date: Monday, February 13, 2012 Sheet 26 of 94

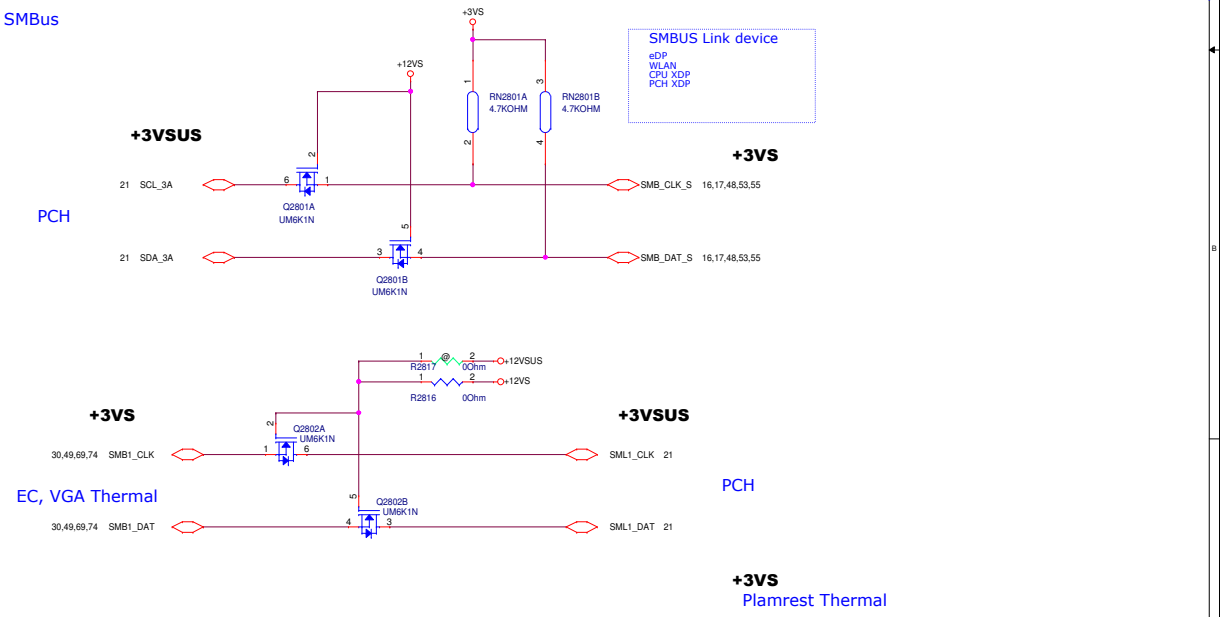

POWER
U2001I
U2001J
COUGAR_POINT_ES1
02V000000001
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
MISC
CPU
RTC
HDA
www.laptopblue.vn
PEGATRON
Title : PCH(8)_POWER,GND
PEGATRON COMPUTER INC
Engineer: Wing_Cheng
Size C
Project Name BA52HR/CR
Rev 1.0
Date: Monday, February 13, 2012
Sheet 27 of 94

PCH SPI ROM



SPI Debug Connector

PCH SMBus



PEGATRON Title : PCH(9)_SPI,SMB
PEGATRON COMPUTER INC Engineer: Wing_Cheng
Size C | Project Name BA52HR/CR | Rev 1.0
Date: Monday, February 13, 2012 Sheet 28 of 94

PEGATRON Title : CLK_ICS9LRS3197

PEGATRON COMPUTER INC Engineer: Wing_Cheng

Size	Project Name	Rev
Custom	BA52HR/CR	1.0

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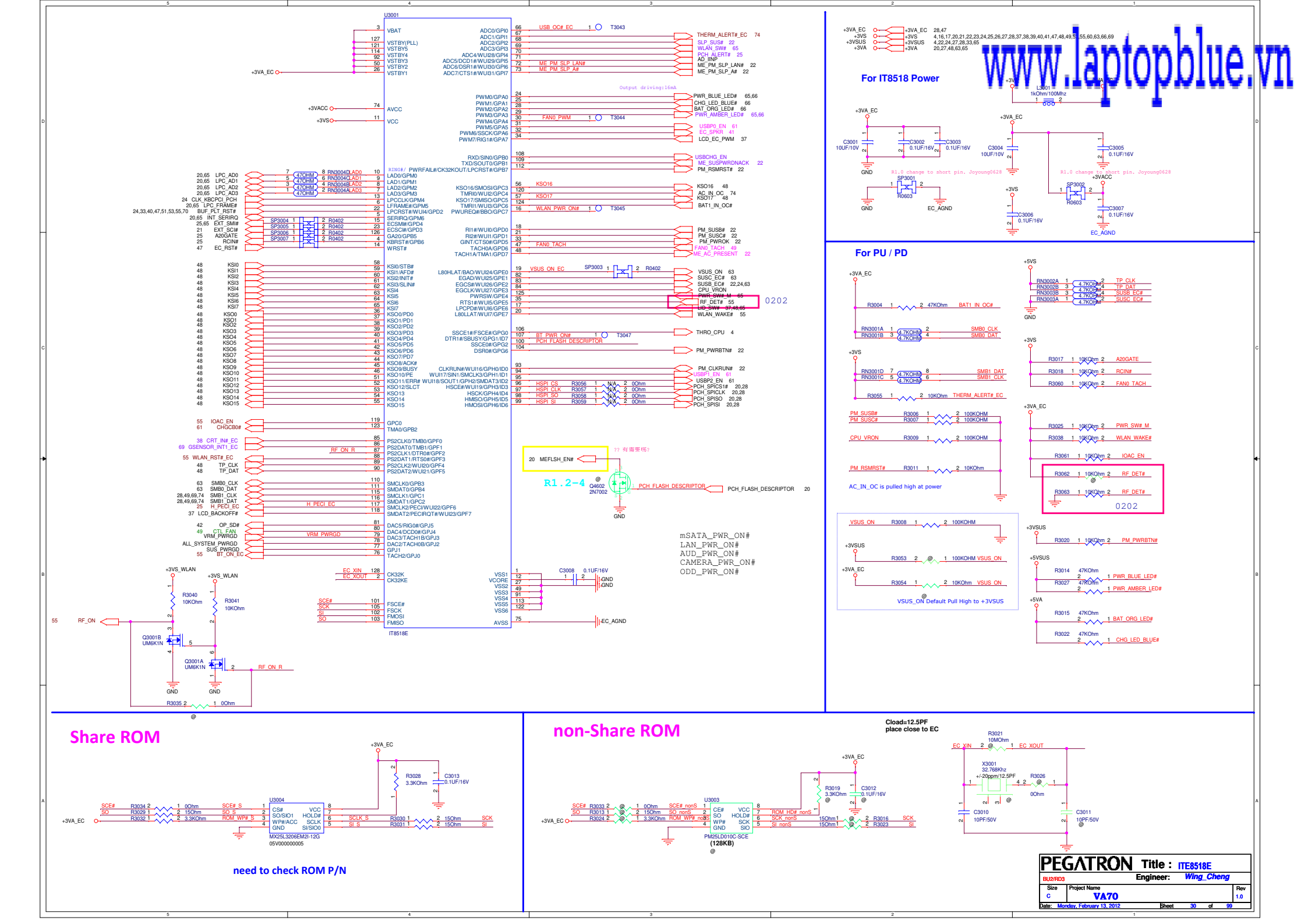
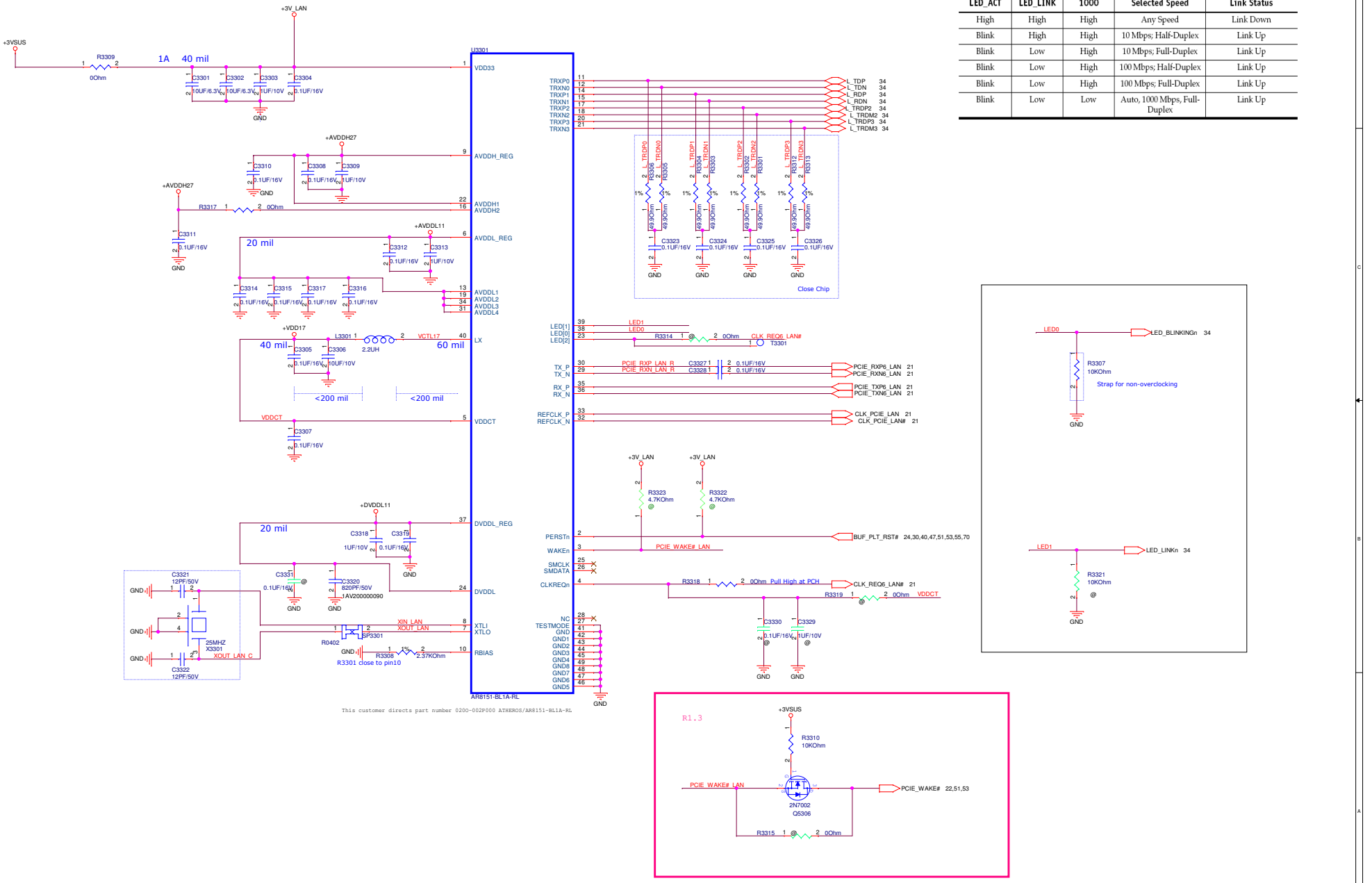


Table 2-6. **LED Link Table**

LED[0] LED_ACT	LED[1] LED_LINK	LED[2] LED_LINK_ 1000	Selected Speed	Link Status
High	High	High	Any Speed	Link Down
Blink	High	High	10 Mbps; Half-Duplex	Link Up
Blink	Low	High	10 Mbps; Full-Duplex	Link Up
Blink	Low	High	100 Mbps; Half-Duplex	Link Up
Blink	Low	High	100 Mbps; Full-Duplex	Link Up
Blink	Low	Low	Auto, 1000 Mbps, Full-Duplex	Link Up



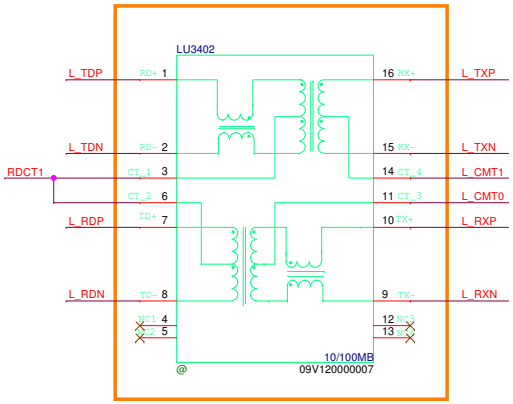
PEGATRON **Title :** LAN_AR8151L

BG1-CSC-HW R&D Dept.5 **Engineer:** *Ahren_chen*

Size	Project Name	Rev
Custom	T13M_RG	1.0

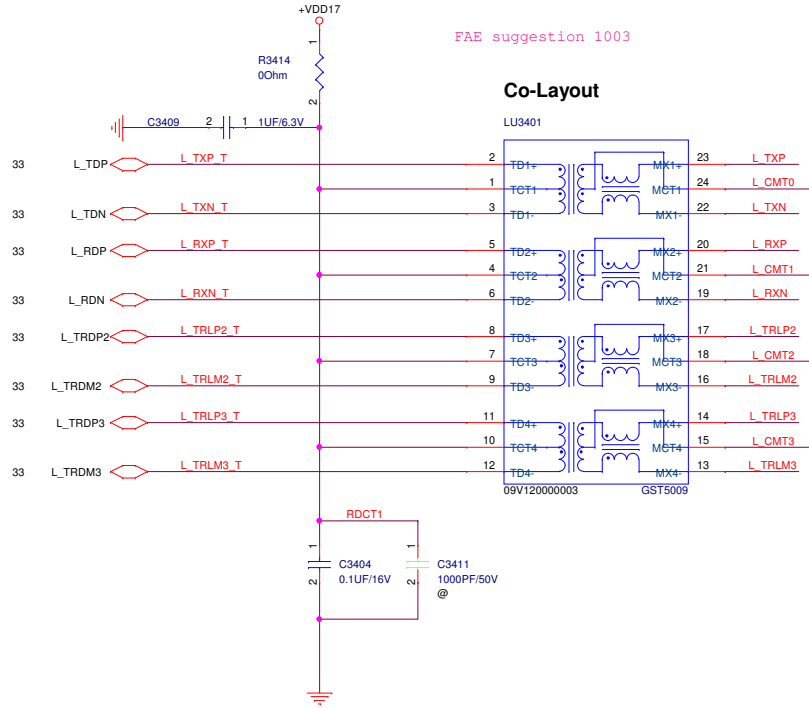
Date: Monday, February 13, 2012 Sheet 33 of 99

11/30 Swap for LU3401/LU3402 co-lay(Elmer)

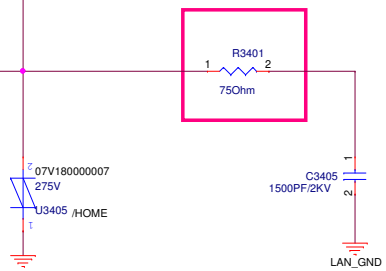


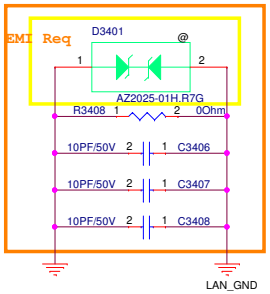
FAE suggestion 1003

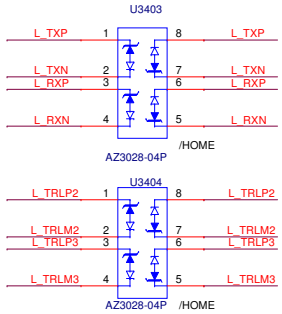
Co-Layout

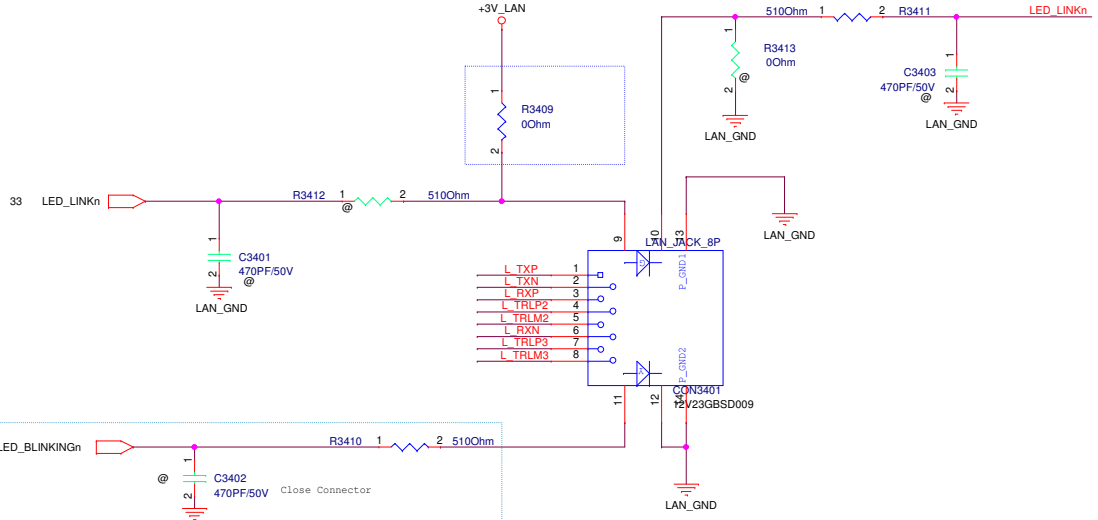


EMI suggest to change 0805 size 0921









<Variant Name>

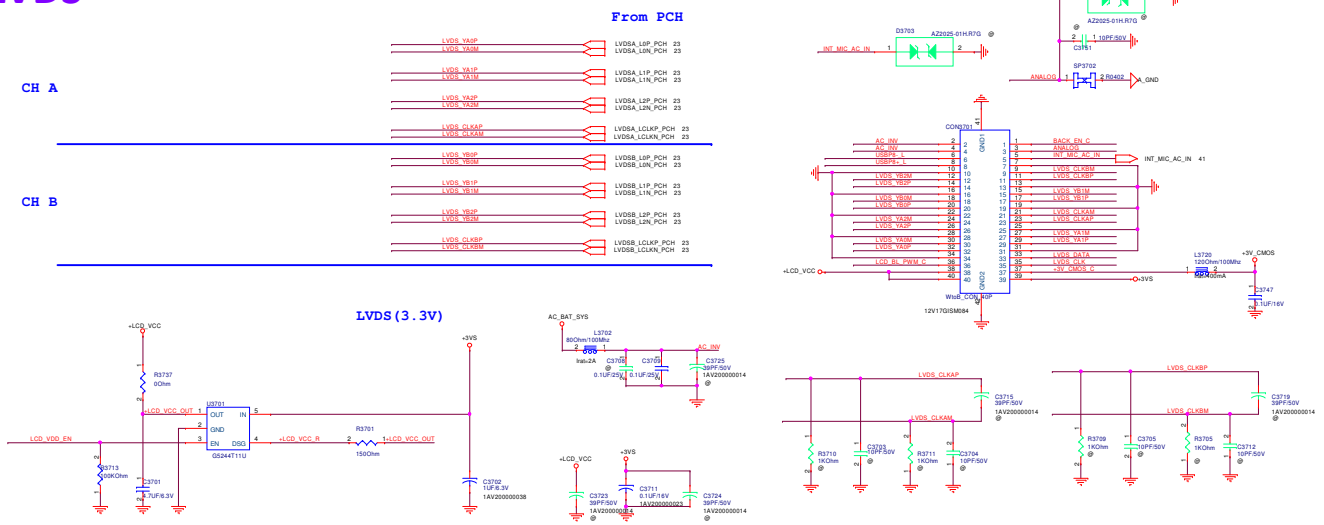
PEGATRON Title : RJ45/ RJ11

BG1-CSC-HW R&D Dept.5 Engineer: Ahren_chen

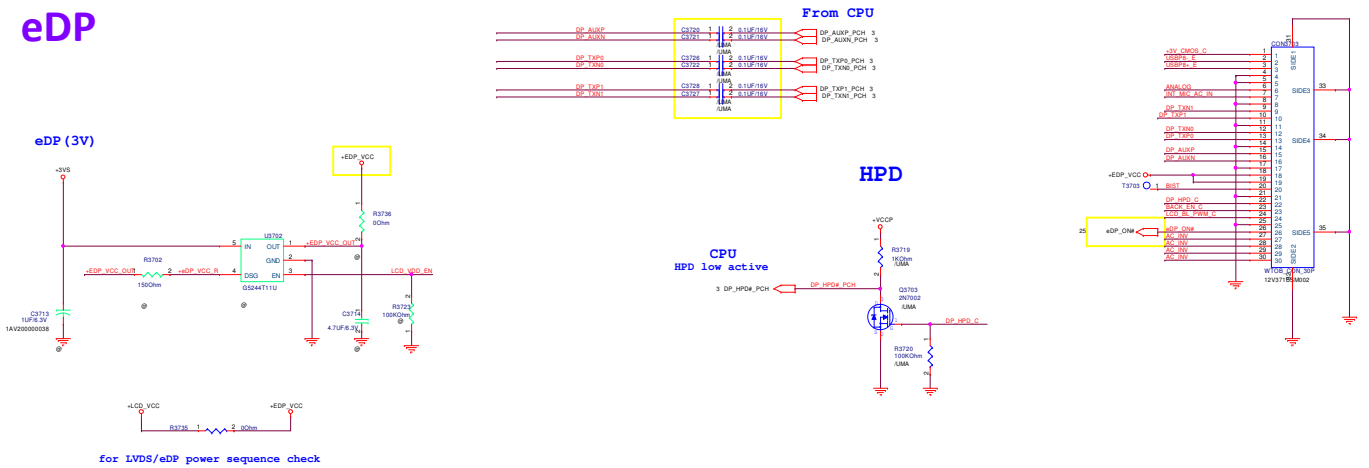
Size	Project Name	Rev
Custom	PLFG	1.0

Date: Monday, February 13, 2012 Sheet 34 of 99

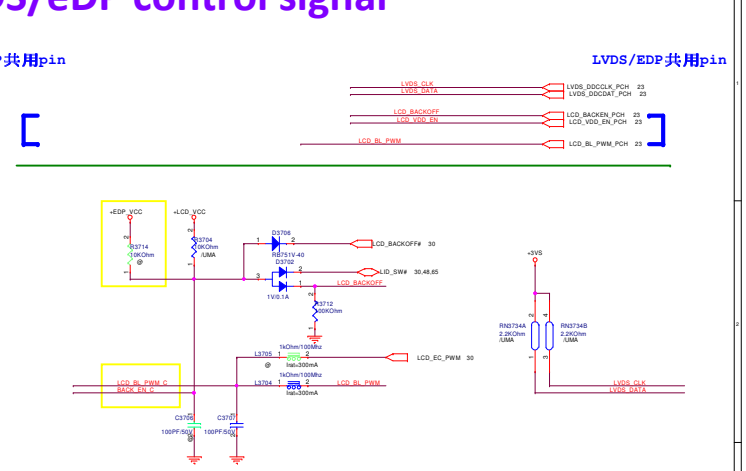
LVDS



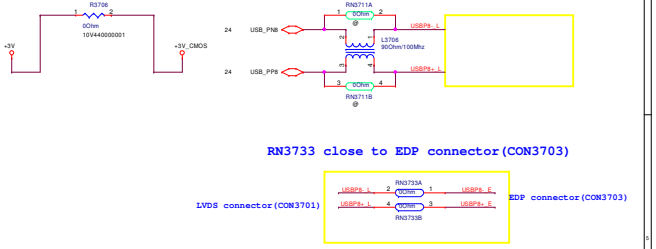
eDP



LVDS/eDP control signal

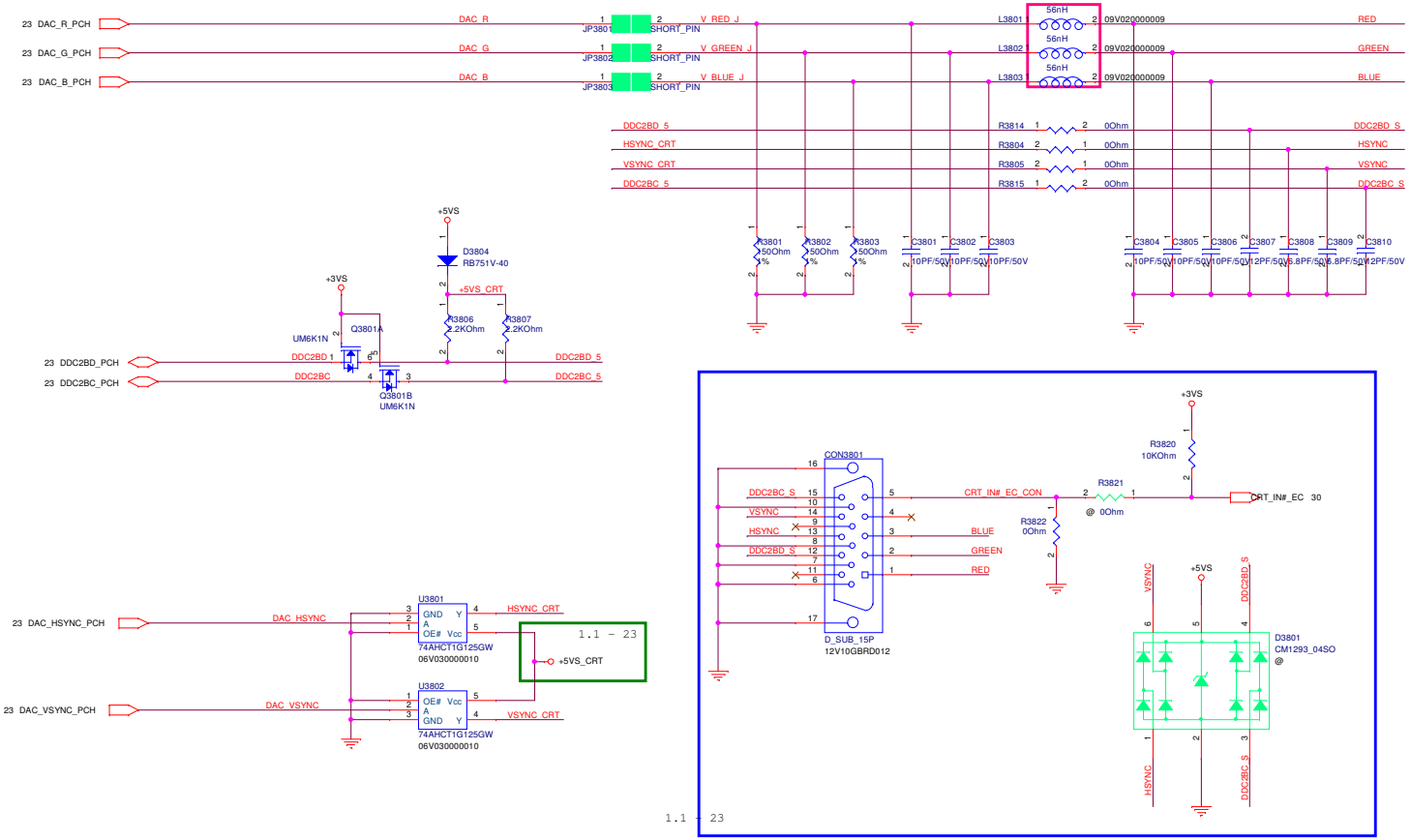


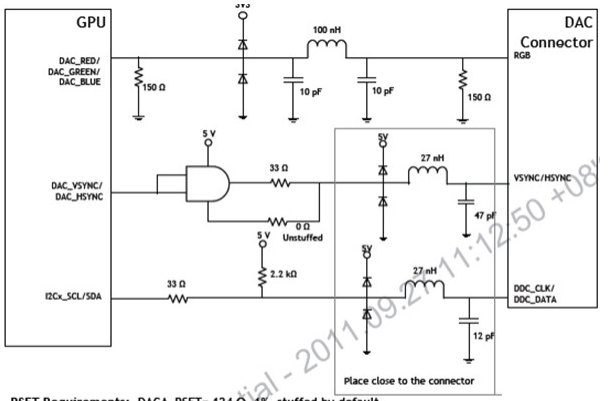
USB Camera



PEGATRON Title : LVDS CONN
BU1-RD Div.1-HW RD Dept.1 Engineer: Wing_Cheng
Size: Custom | Project Name: BA52HR/CR | Rev: 1.0
Date: Monday, February 13, 2012 | Sheet 37 of 89

L3801/3802/3803 changes from inductor to bead 0901-004G000



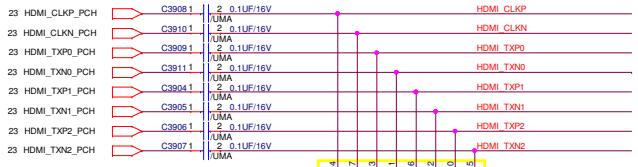


RSET Requirements: DACA_RSET= 124 Ω, 1%, stuffed by default.

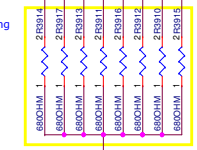
Figure 71. GPU-DAC Connections

The LC filter circuit(NV DSC only)
DDC:L=27nH,C=12PF
HSYNC/VSYNC:L=27nH,C=47PF
RGB:L=100nH,C=10PF

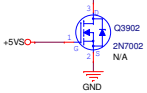
PEGATRON	Title : CRT		
BU1-RD Div.1-HW RD Dept.1	Engineer: Wing_Cheng		
Size: Custom	Project Name: BA52HR/CR		Rev: 1.0
Date: Monday, February 13, 2012	Sheet 38 of 77		



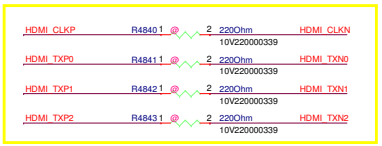
Close to connector and do T routing

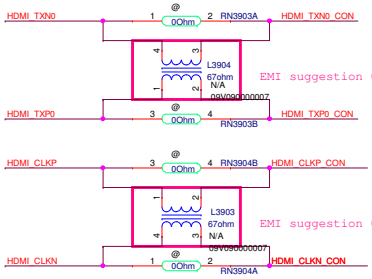


R3910,R3911,R3912,R3913,R3914,R3915,R3916,R3917
Intel design guide : 680ohm /UMA
NV reference schematics : 499ohm /DGPUO

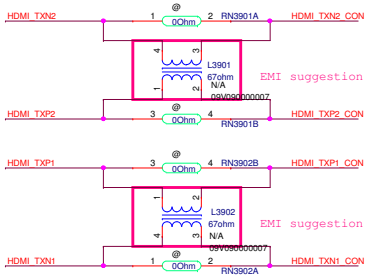


EMI solution



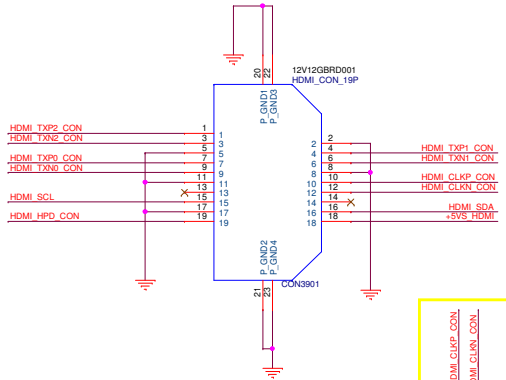


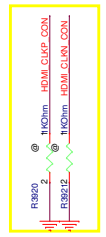
EMI suggestion 0922



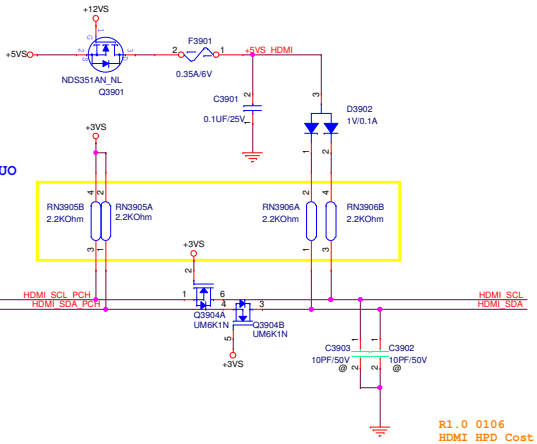
EMI suggestion 0922

HDMI_SCL & HDMI_SDA : no via , trace length should be as short as possible

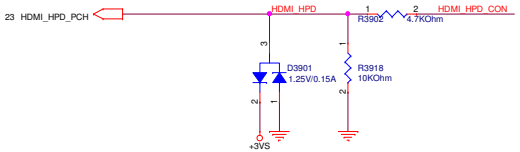




EMI solution



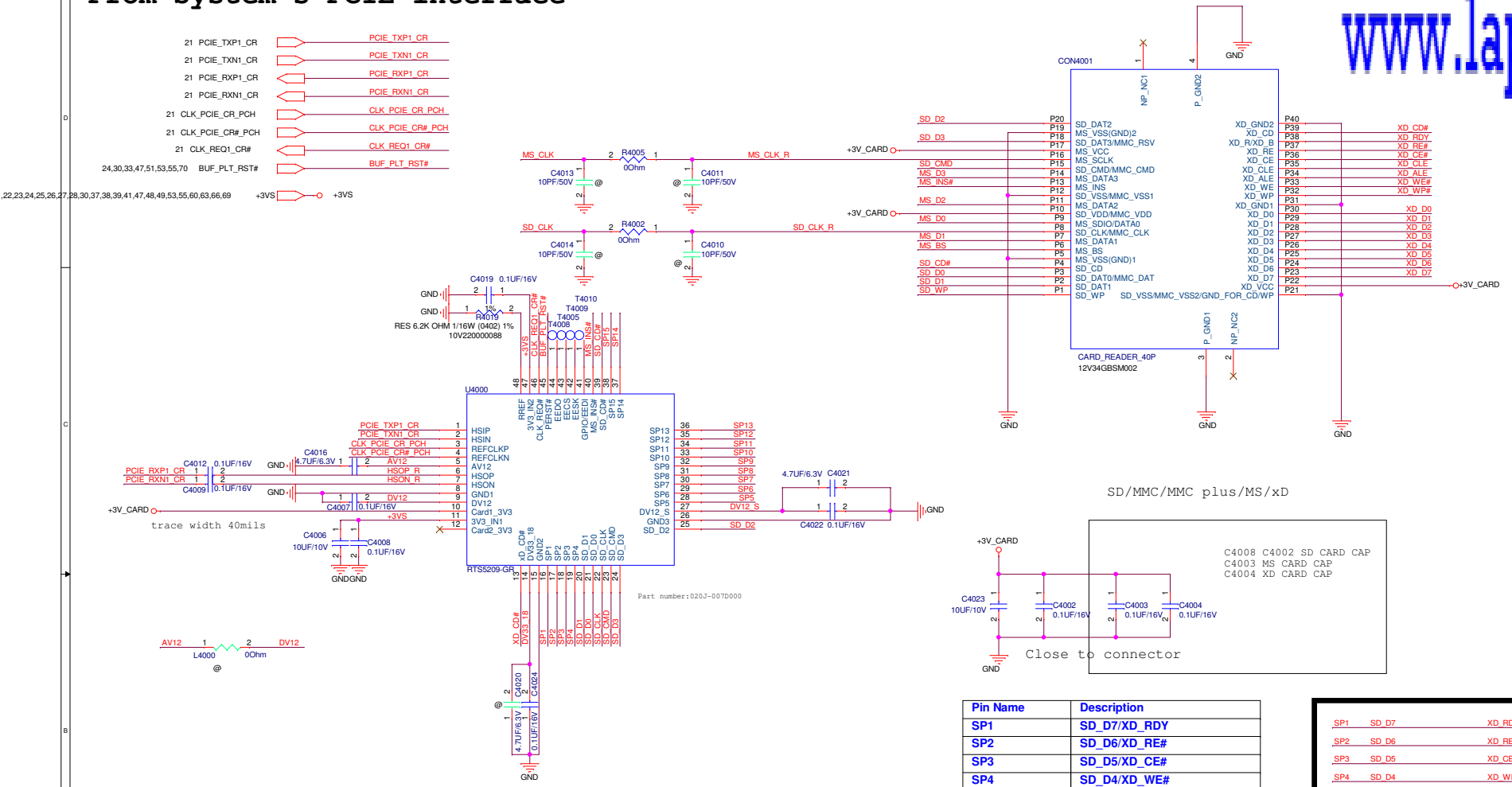
RN3905,RN3906
Intel design guide:2.2K ohm /UMA
NV reference schematics:4.7K ohm /DGPUO



R1.0 0106
HDMI HPD Cost Reduced Level Shifter Design Recommendation

PEGATRON	Title : HDMI		
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Wing_Cheng		
Size: Custom	Project Name: BA52HR/CR		Rev: 1.0
Date: Monday, February 13, 2012	Sheet 39 of 77		

From System's PCIE interface



Remove Serial Flash

Reserve for BIOS boot function

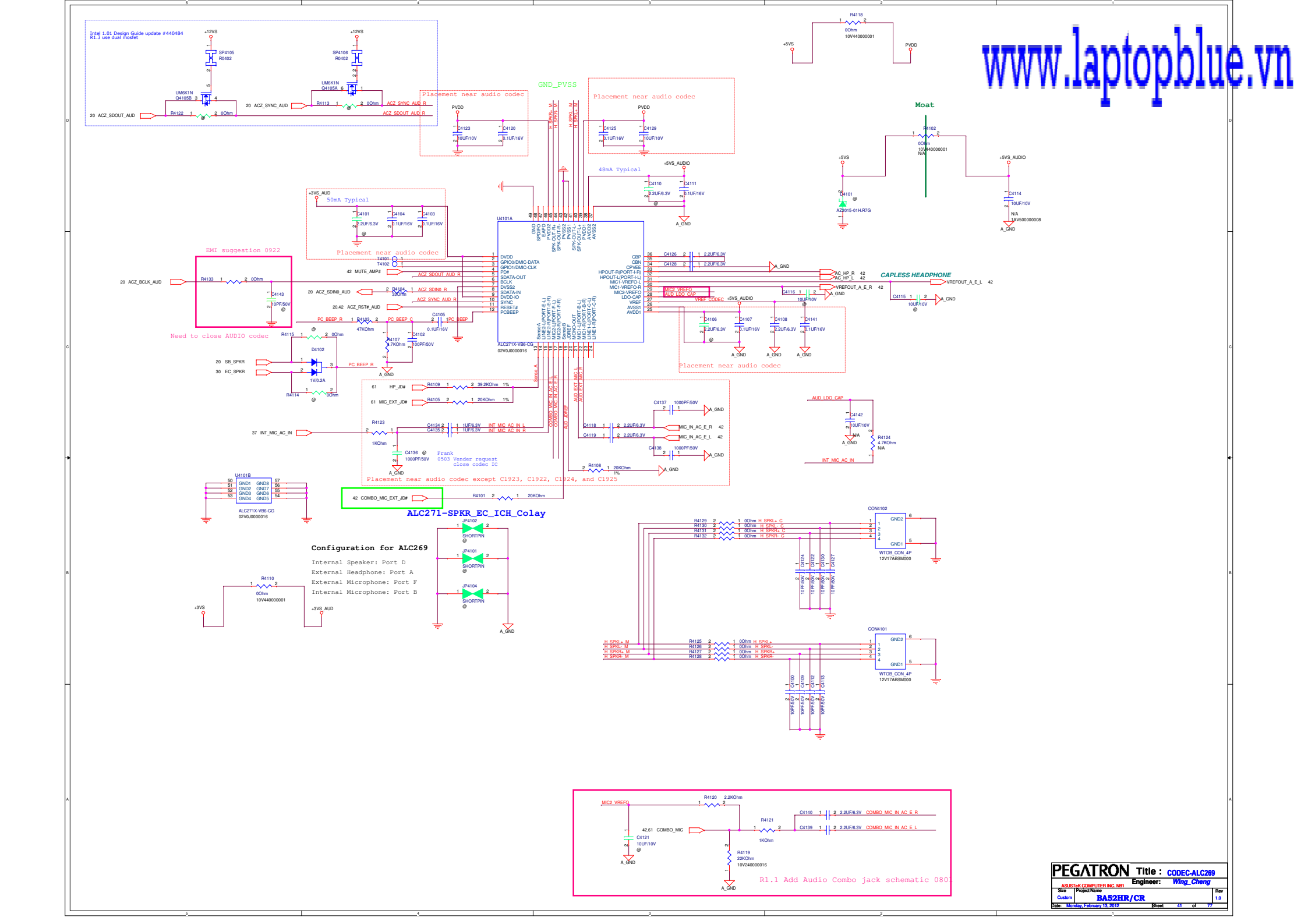
When EECS switch to be D3-Delink sideband signal, Serial Flash function is disabled.

Pin Name	Description
SP1	SD_D7/XD_RDY
SP2	SD_D6/XD_RE#
SP3	SD_D5/XD_CE#
SP4	SD_D4/XD_WE#
SP5	MS_BS/XD_CLE
SP6	MS_D5/XD_ALE
SP7	MS_D1/XD_WP#
SP8	MS_D4/XD_D0
SP9	MS_D0/XD_D1
SP10	MS_D2/XD_D2
SP11	MS_D6/XD_D3
SP12	MS_D3/XD_D4
SP13	MS_D7/XD_D5
SP14	MS_CLK/XD_D6
SP15	SD_WP/XD_D7

SP1	SD_D7	XD_RDY
SP2	SD_D6	XD_RE#
SP3	SD_D5	XD_CE#
SP4	SD_D4	XD_WE#
SP5	MS_BS	XD_CLE
SP6	MS_D5	XD_ALE
SP7	MS_D1	XD_WP#
SP8	MS_D4	XD_D0
SP9	MS_D0	XD_D1
SP10	MS_D2	XD_D2
SP11	MS_D6	XD_D3
SP12	MS_D3	XD_D4
SP13	MS_D7	XD_D5
SP14	MS_CLK	XD_D6
SP15	SD_WP	XD_D7

Share Pin

PEGATRON	Title : RTS5209		
BG1/CSC/HW5	Engineer: Peter5 Huang		
Size: Custom	Project Name: Comal		Rev: 1.0
Date: Monday, February 13, 2012	Sheet 40 of 99		


Intel 1.01 Design Guide update #440484
R1.3 use dual mosfet
Placement near audio codec
GND_PVSS
48mA Typical
50mA Typical
EMI suggestion 0922
Need to close AUDIO codec
Moat
CAPLESS HEADPHONE
Placement near audio codec except C1923, C1922, C1924, and C1925
ALC271-SPKR_EC_ICH_Colay
Configuration for ALC269
Internal Speaker: Port D
External Headphone: Port A
External Microphone: Port F
Internal Microphone: Port B
Frank
0503 Vender request
close codec IC
R1.1 Add Audio Combo jack schematic 080
www.laptopblue.vn
PEGATRON
Title : CODEC-ALC269
Engineer: Wing_Cheng
ASUSTeK COMPUTER INC. NB1
Project Name
BA52HR/CR
Rev 1.0
Date: Monday, February 13, 2012
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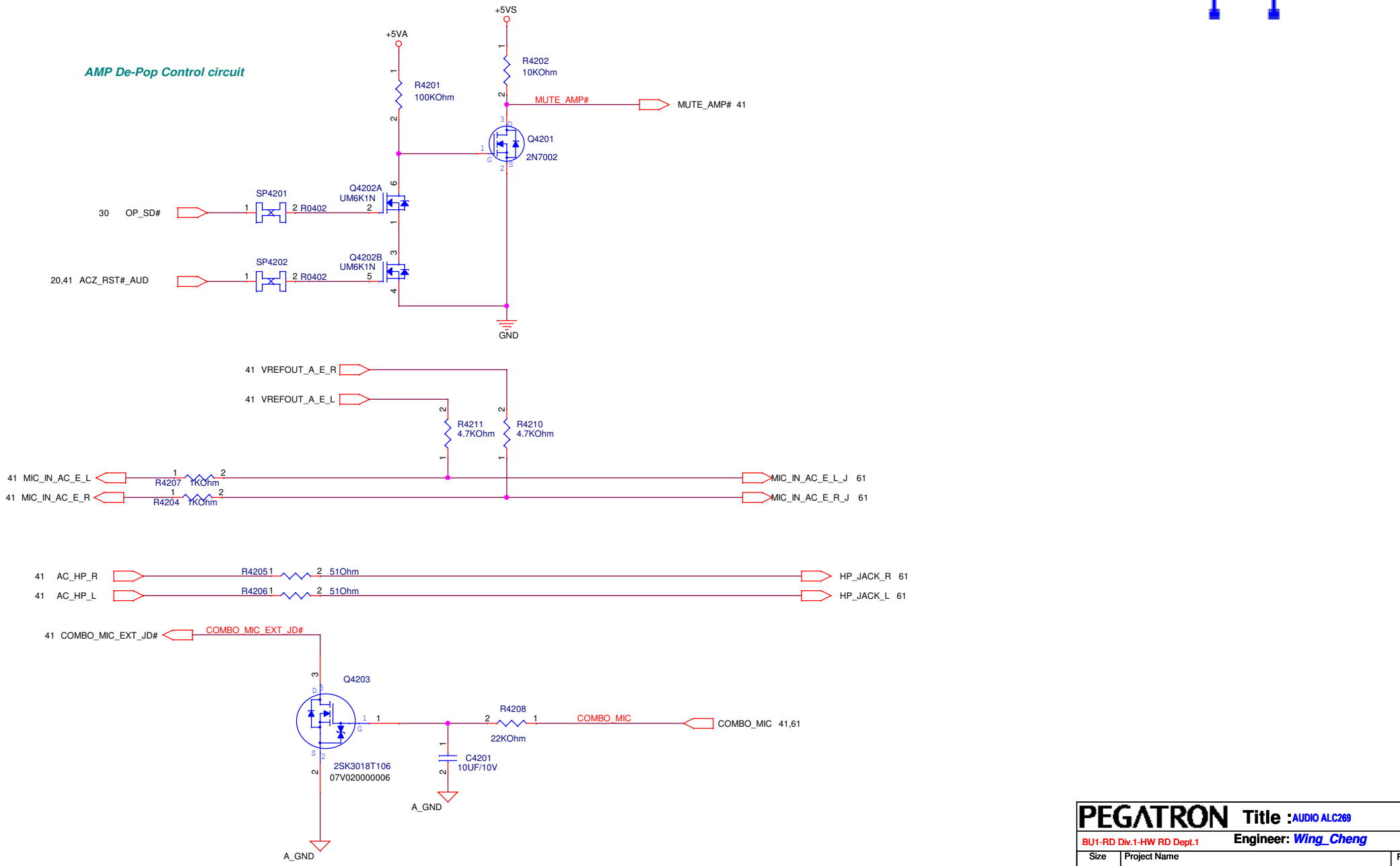


PEGATRON	Title : AUDIO ALC269	
BU1-RD Div.1-HW RD Dept.1	Engineer: Wing_Cheng	
Size: B	Project Name: BA52HR/CR	Rev: 1.0
Date: Monday, February 13, 2012	Sheet 42 of 77	

PEGATRON Title : MDC CONN

BG1-HW RD Div.2-NB RD Dept.5 Engineer: Wing_Cheng

Size	Project Name	Rev
C	BA52HR/CR	1.0

Date: Monday, February 13, 2012 Sheet 43 of 77

Del Entry audio circuit

SR-8
0121-11

PEGATRON Title : CODEC-ALC269

ASUSTeK COMPUTER INC. NB1 Engineer: Wing_Cheng

Size	Project Name	Rev
Custom	BA52HR/CR	1.0

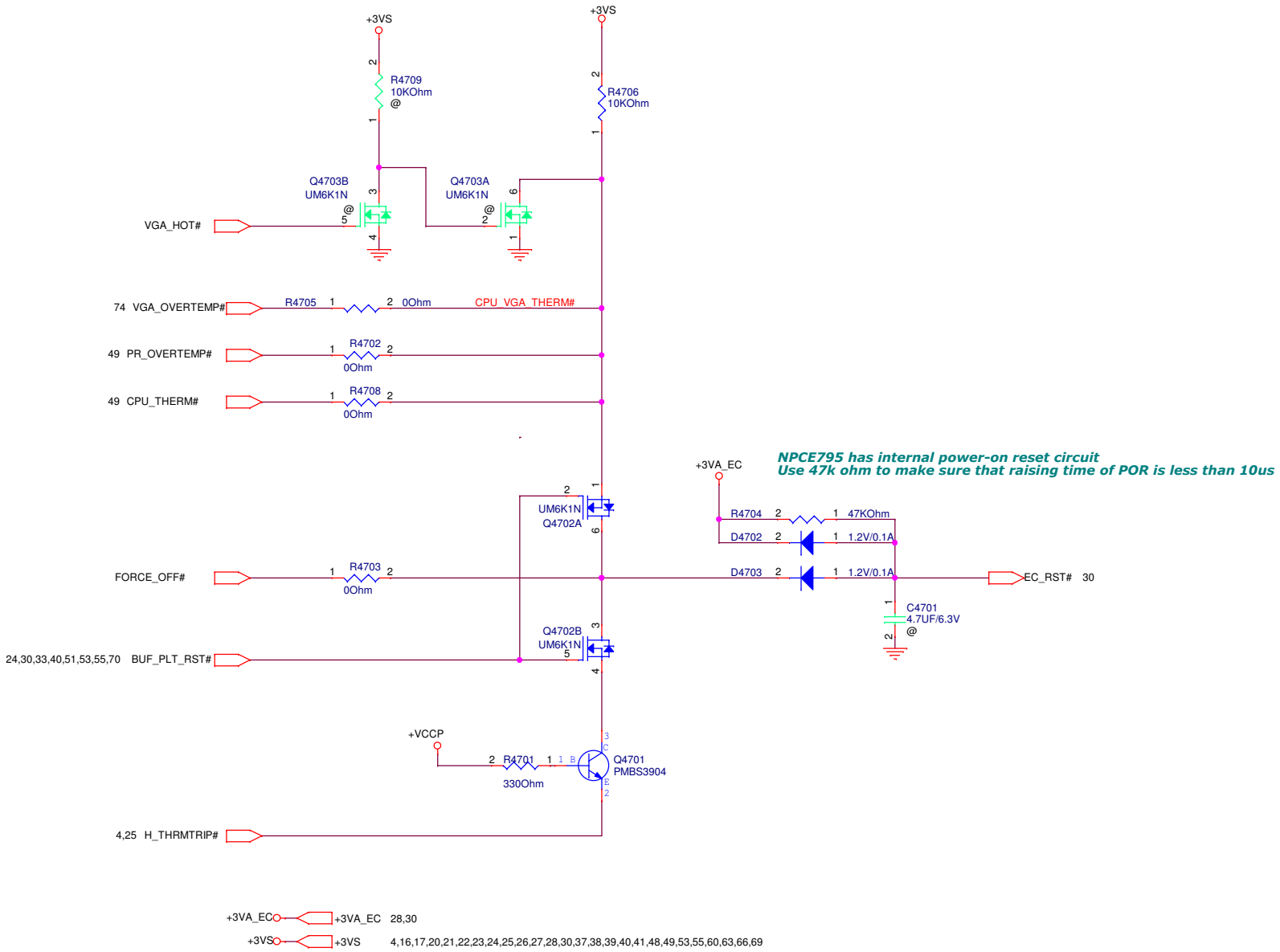
Date: Monday, February 13, 2012 Sheet 44 of 77

Del Entry audio circuit

SR-8
0121-11

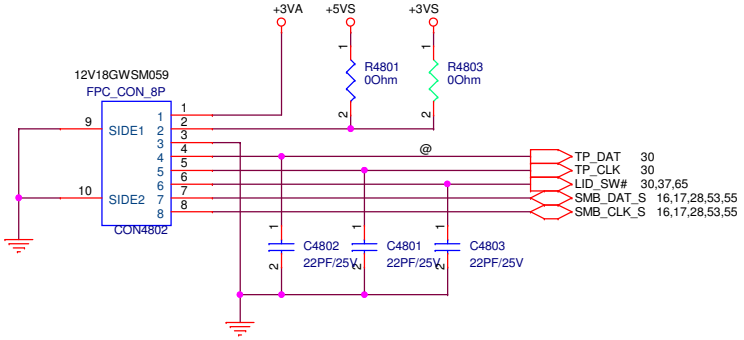
PEGATRON	Title : AUDIO ALC269	
BU1-RD Div.1-HW RD Dept.1	Engineer: Wing_Cheng	
Size: Custom	Project Name: BA52HR/CR	Rev: 1.0
Date: Monday, February 13, 2012	Sheet 45 of 77	

Thermal Policy

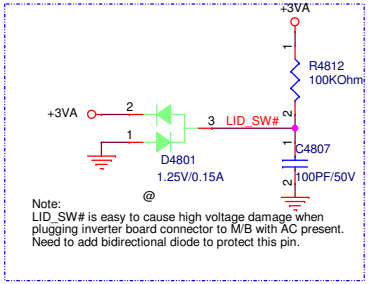


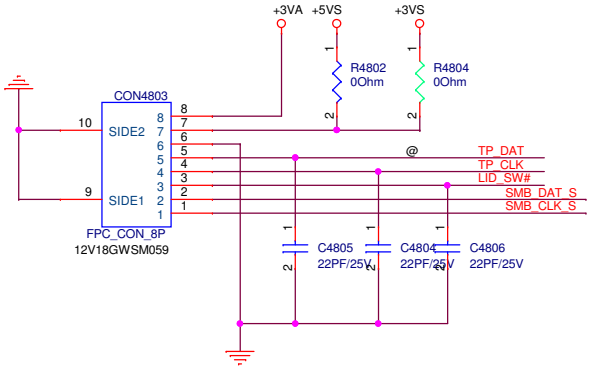
PEGATRON	Title : RST_Reset Circuit	
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Wing_Cheng	
Size: B	Project Name: BA52HR/CR	Rev: 1.0
Date: Monday, February 13, 2012	Sheet 47 of 77	

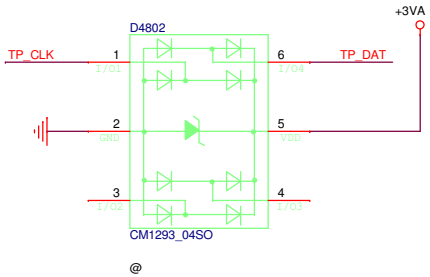
Touch Pad Button/ Hall Sensor



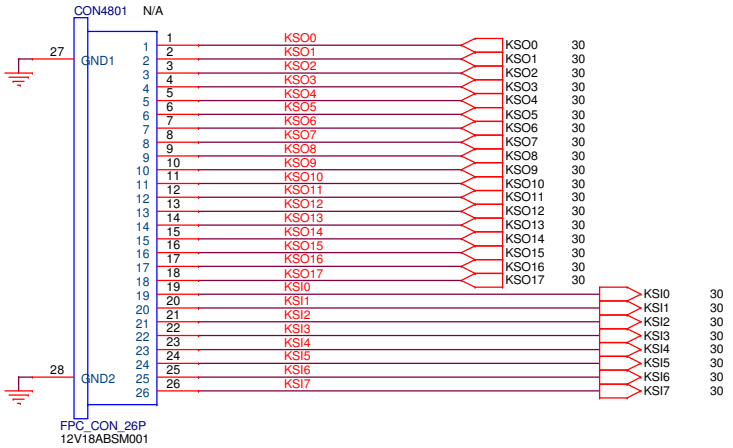
close toU4601



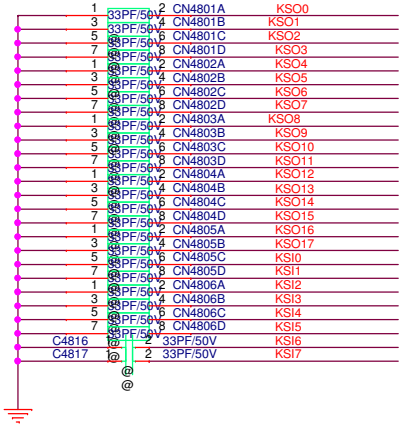




Keyboard



1218-00MW000



PEGATRON	Title : KB/ TP/ FLASH	
BU1-RD Div.1-HW RD Dept.1	Engineer: Wing_Cheng	
Size: Custom	Project Name: BA52HR/CR	Rev: 1.0
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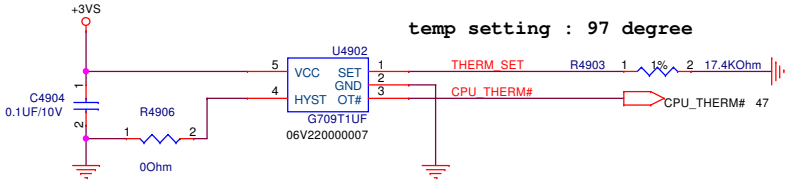
U5001 Close to CPU

temp setting : 97 degree

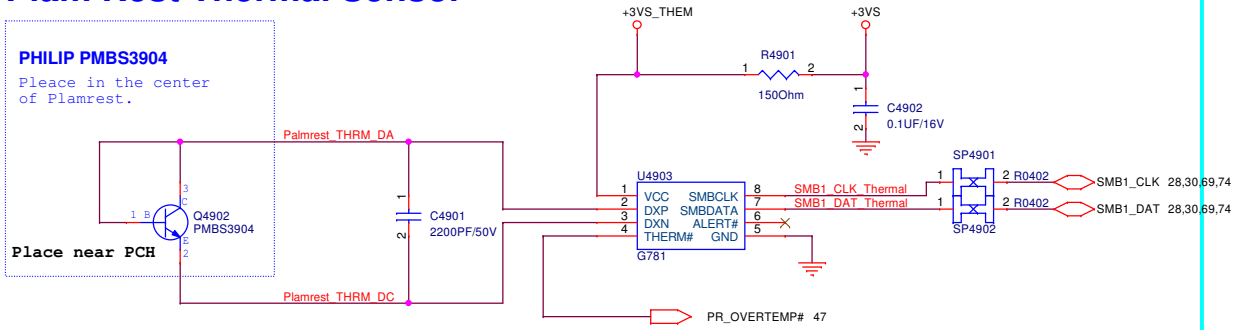


Plam Rest Thermal Sensor

PHILIP PMBS3904

Pleace in the center of Plamrest.

Place near PCH



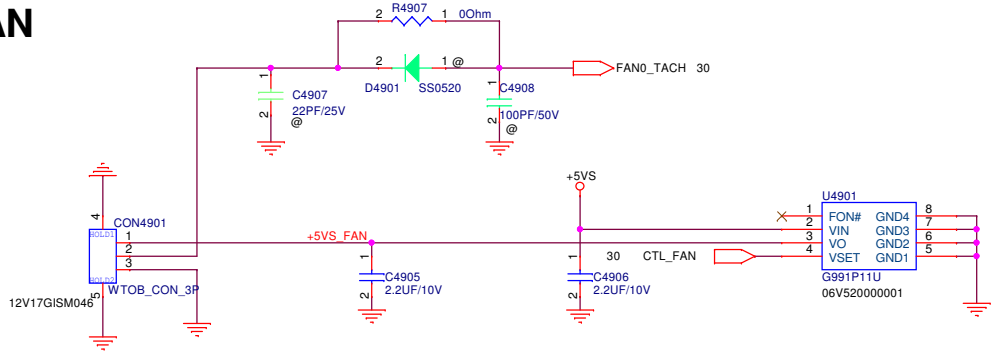
U4903 under palmrest

SMBUS addr=1001100x (98)

U4903: Remote(Local) thermal sensor,use remote mode.

R1.2-10

FAN



PEGATRON	Title : THERMAL/ FAN	
BU1-RD Div.1-HW RD Dept.1	Engineer: Wing_Cheng	
Size: Custom	Project Name: BA52HR/CR	Rev: 1.0
Date: Monday, February 13, 2012	Sheet 49 of 77	

PEGATRON Title : Realtek_RTS5138

BG1-HW RD Div.2-NB RD Dept.5 Engineer: Wing_Cheng

Size	Project Name	Rev
C	BA52HR/CR	1.0

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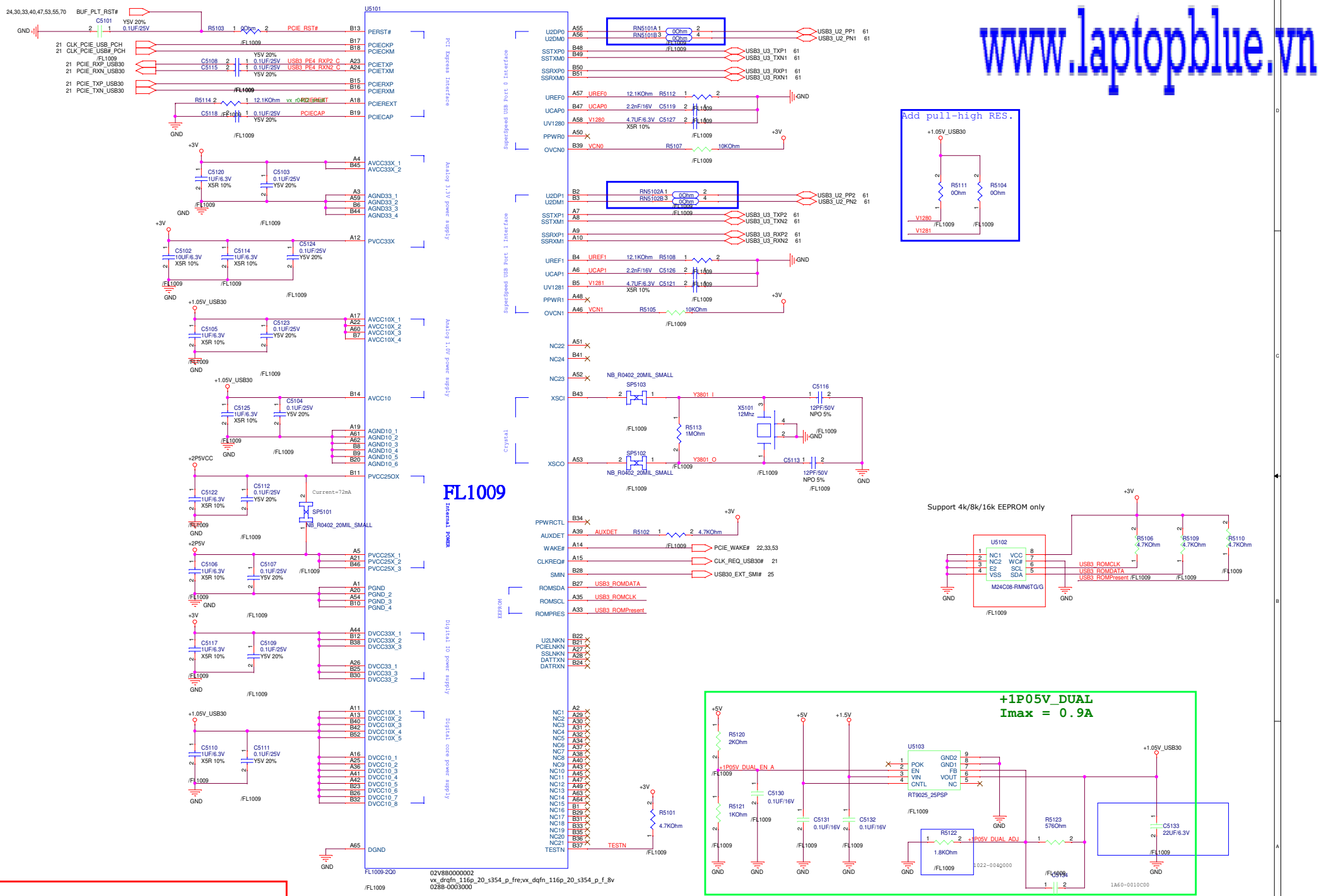


PEGATRON Title : USB3.0 uPD720200
Engineer: Wing_Cheng
BG1\HW1
Size C | Project Name BA52HR/CR | Rev 1.0
Date: Monday, February 13, 2012 | Sheet 51 of 77

PEGATRON Title : PCIE NEW CARD

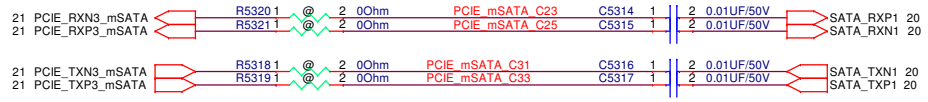
BU1-RD Div.1-HW RD Dept.1 Engineer: Wing_Cheng

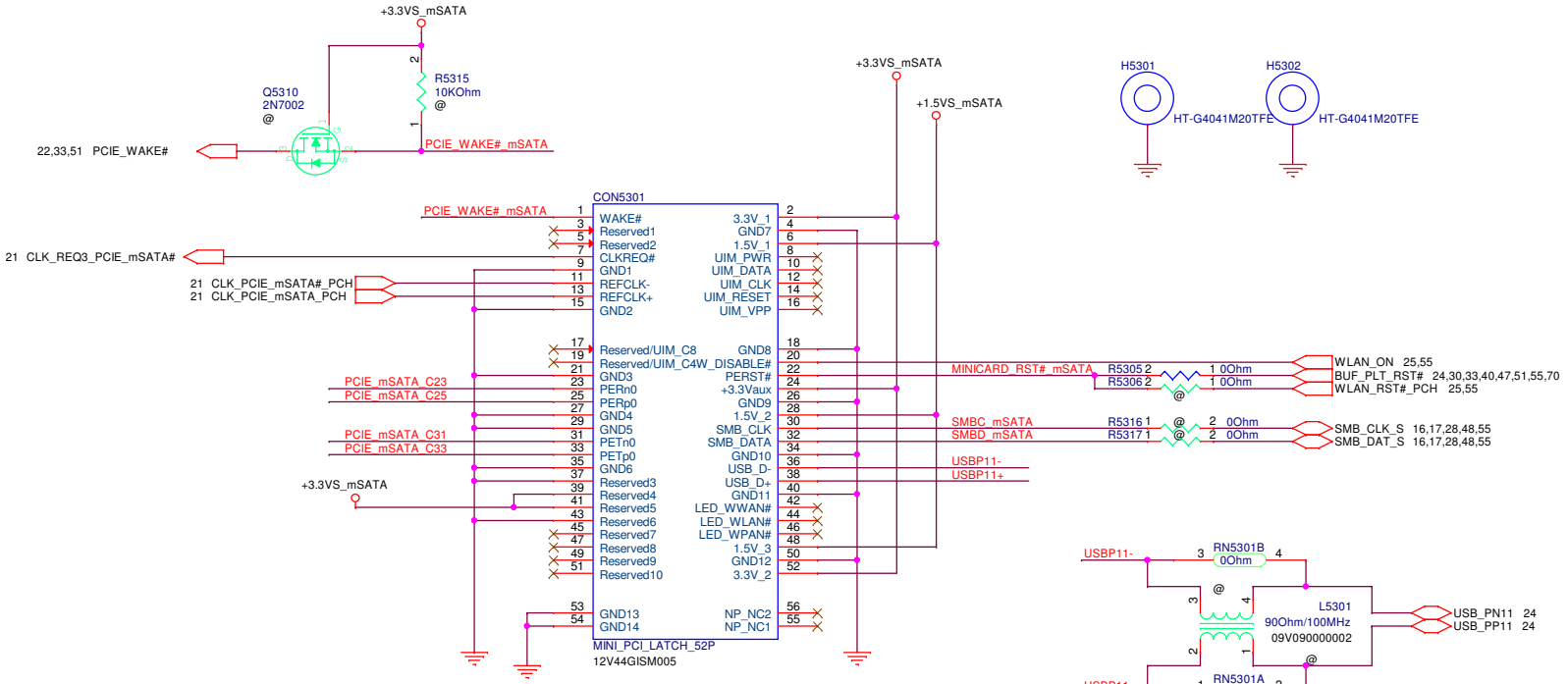
Size	Project Name	Rev
Custom	BA52HR/CR	1.0

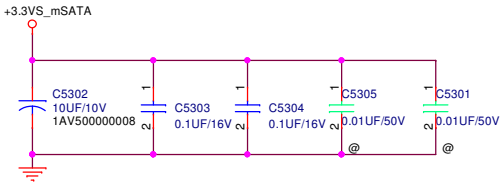
Date: Monday, February 13, 2012 Sheet 52 of 77

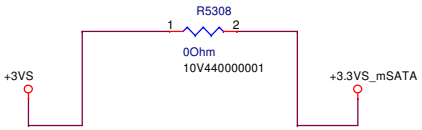
PCIE/mSATA

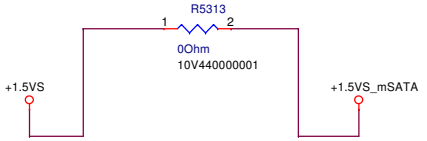
Select PCIE or mSATA IF select mSATA(only +3VAUX)

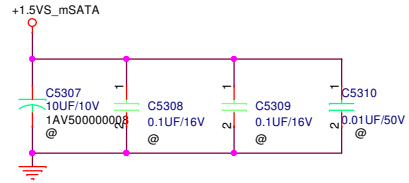






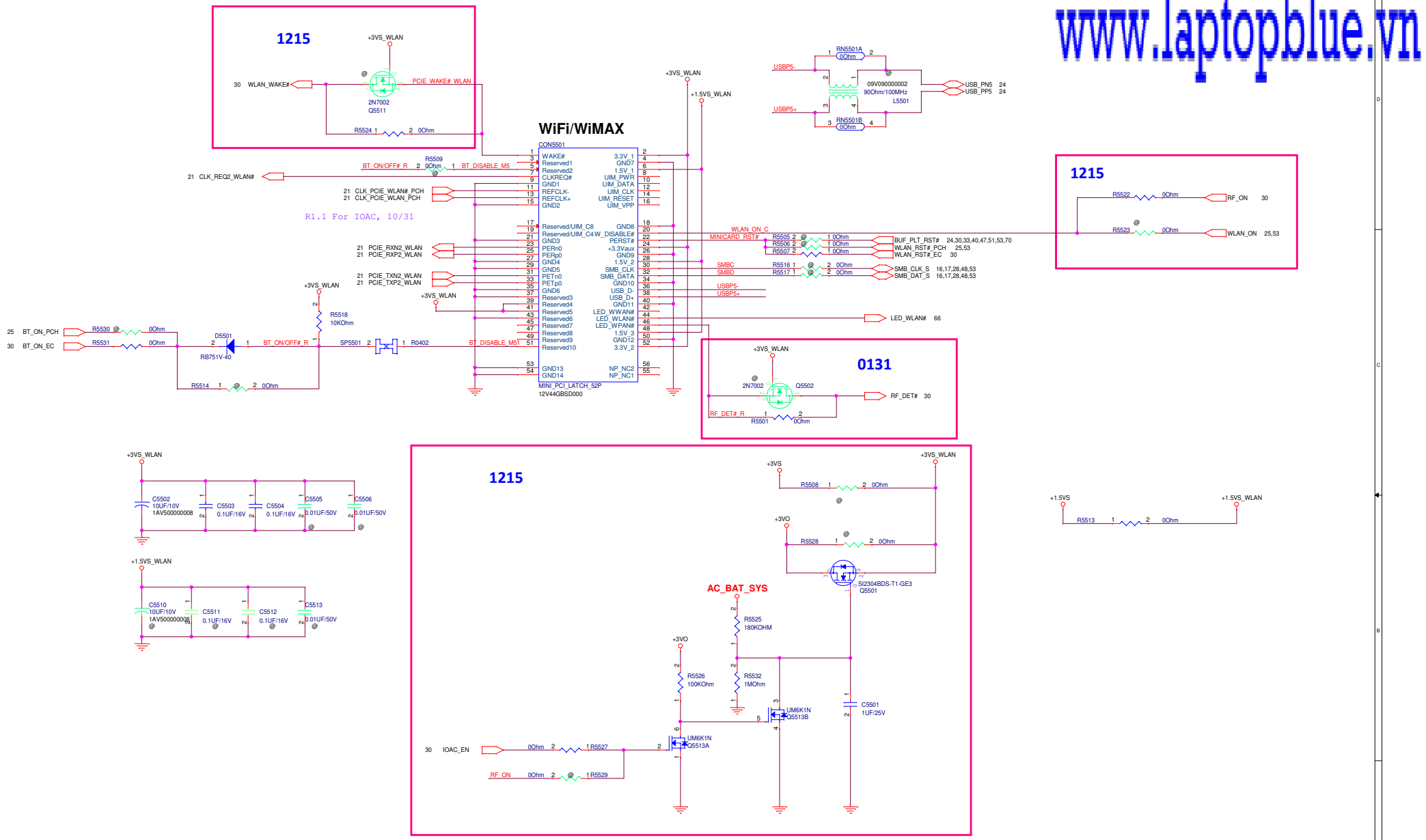






PEGATRON	Title : WiFi/WiMAX	
BU1-RD Div.1-HW RD Dept.1	Engineer:	
Size: Custom	Project Name: BA52HR/CR	Rev: 1.0
Date: Monday, February 13, 2012	Sheet 53 of 77	

PEGATRON	Title : MINICARD (WUSB /UPCONVERT)		
BU1-RD Div.1-HW RD Dept.1	Engineer: *Wing_Cheng*		
Size: Custom	Project Name: BA52HR/CR		Rev: 1.0
Date: Monday, February 13, 2012	Sheet 54 of 77		



PEGATRON	Title : WiFi/WiMAX	
BU1-RD Div.1-HW RD Dept.1	Engineer:	
Size: C	Project Name: VA70	Rev: 1.0
Date: Monday, February 13, 2012	Sheet 55 of 77	

Screw M x 2

TP_H1 C236D110

TP_H2 C236D110

TP_GND

Fix Hole J x 1

TP_H3 CT197D118N

Fix Hole K x 1

TP_H4 DO172X118N

HOTBAR_PAD_8P

0202

TPCON1

TP_+3VA
TP_+5VS
TP_GND
TP_DAT_IO
TP_CLK_IO
TP_LID_SW#
SMB_DAT_IO
SMB_CLK_IO

TPC06 10PF/50V
TPC07 10PF/50V
TPC08 10PF/50V

TP_LEFT — TPR2 0Ohm — TP_LEFT_R

12V09SBSM020 TP_SWITCH_4P — TP_SW1
12V09SBSM020 TP_SWITCH_4P — TP_SW6
12V09SBSM020 TP_SWITCH_4P — TP_SW4

TP_RIGHT — TPR3 0Ohm — TP_RIGHT_R

12V09SBSM020 TP_SWITCH_4P — TP_SW5
12V09SBSM020 TP_SWITCH_4P — TP_SW2
12V09SBSM020 TP_SWITCH_4P — TP_SW3

Touch Pad WIN8

TPCON3

TP_LEFT
TP_RIGHT
TP_CLK_IO
TP_DAT_IO
SMB_DAT_IO
SMB_CLK_IO
TP_GND
TP_+5VS

HOTBAR_PAD_8P

Touch Pad WIN7

TPCON2

TP_+5VS
TP_CLK_IO_C
TP_DAT_IO_C
TPR01 0Ohm TP_CLK_IO
TPR02 0Ohm TP_DAT_IO
TP_LEFT
TP_RIGHT

HOTBAR_6P

TPC02 10PF/50V
TPC03 10PF/50V
TPC04 10PF/50V
TPC05 10PF/50V

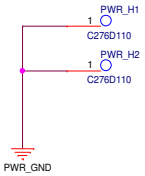
LID Switch

TP_+3VA
TPC01 /VA 0.1UF/10V
TPR09 100KOhm
TP_LID_SW#
AH180-WG-7 Vdd GND OUTPUT TPU01 /VA
TP_D2 AZ5123-01H 07V180000006 /VA
TP_D3 AZ5123-01H 07V180000006 /VA
TPC09 1000PF/50V
TPC10 1000PF/50V
TP_GND

TP_D1 CM1293_04SO
TP_DAT_IO
TP_CLK_IO
TP_RIGHT
TP_LEFT
TP_GND
TP_+3VA

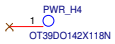
PEGATRON	Title : TP_M	
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Wing_Cheng	
Size: B	Project Name: BA52HR/CR	Rev: 1.0
Date: Monday, February 13, 2012	Sheet 56 of 77	

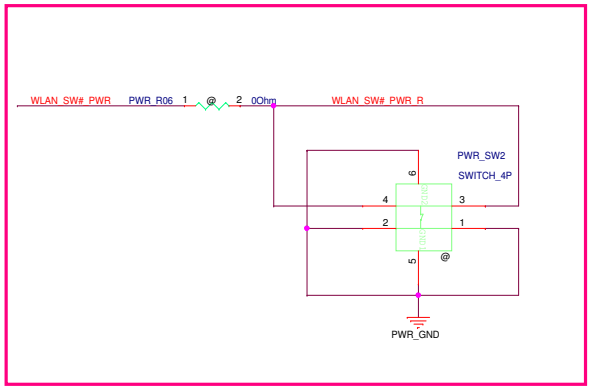
Screw G x 2



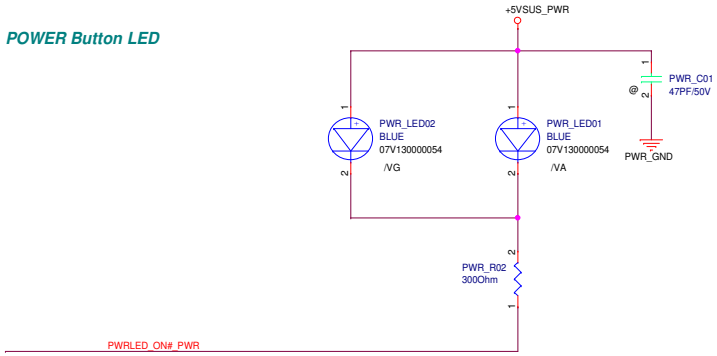
Fix Hole H x 1

Fix Hole I x 1

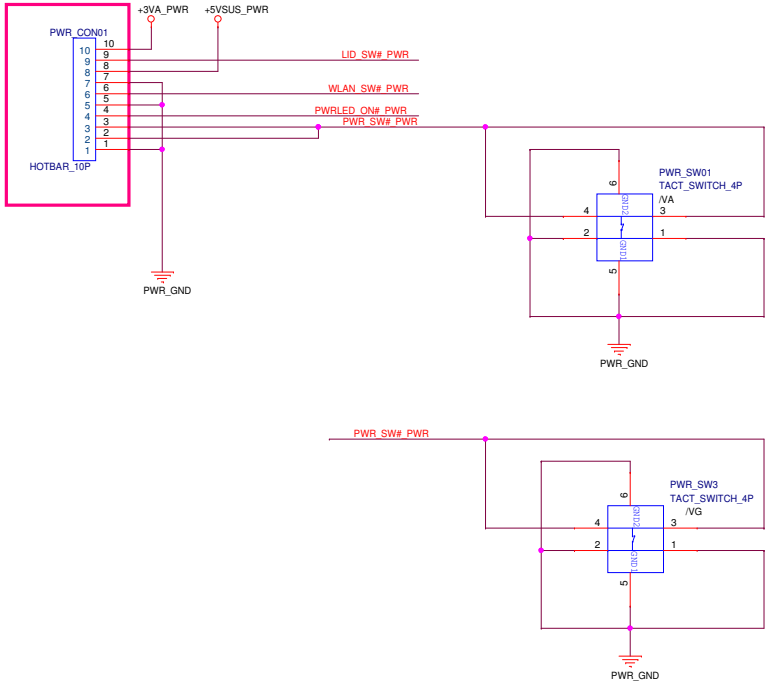


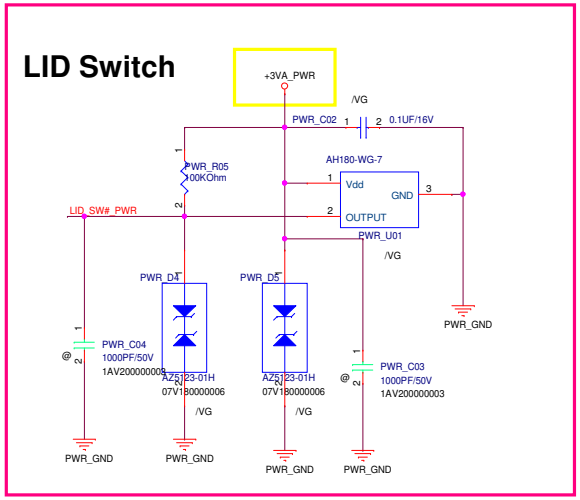


POWER Button LED



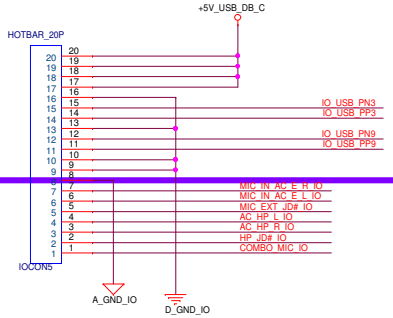
R1.1 reverse PWR_CON01 and change pin 1~4 pin define 1024

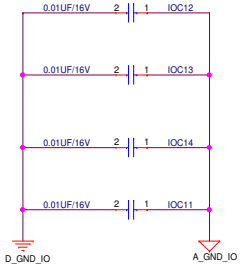


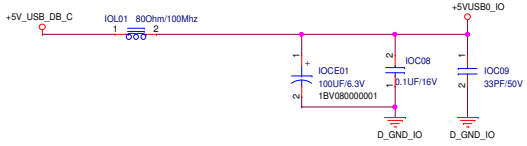


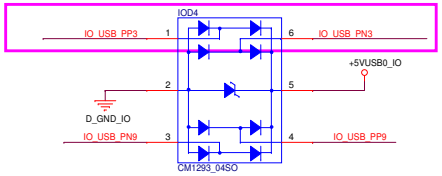
PEGATRON	Title : PWR BTN	
BU1-RD Div.1-HW RD Dept.1	Engineer: Wing_Cheng	
Size: Custom	Project Name: BA52HR/CR	Rev: 1.0
Date: Monday, February 13, 2012	Sheet 57 of 77	

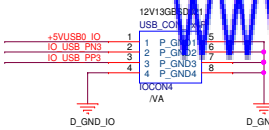
USB 2.0

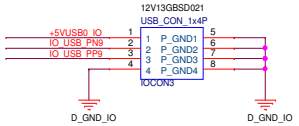






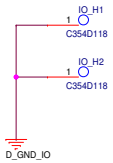




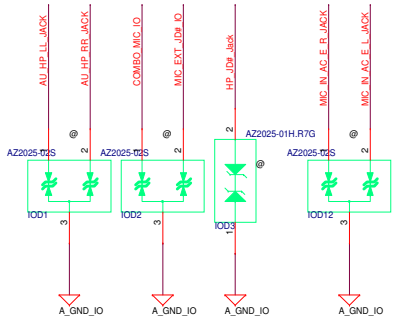


D_GND_IO Moat A_GND_IO

Screw L x 2

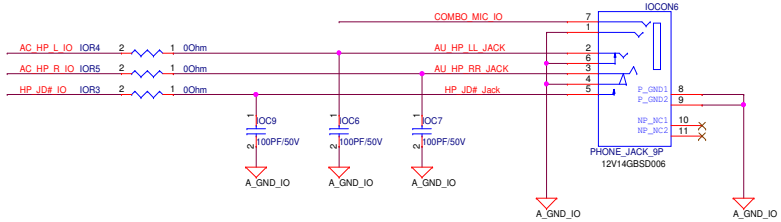


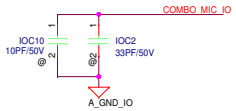
Fix Hole F x 1



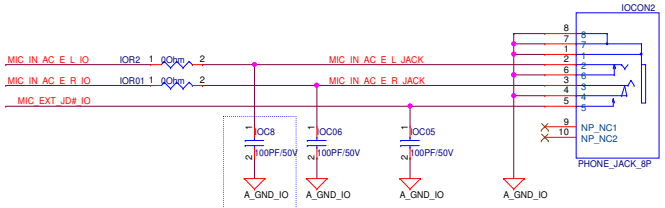
Fix Hole E x 1

Headphone & MIC combo Jack





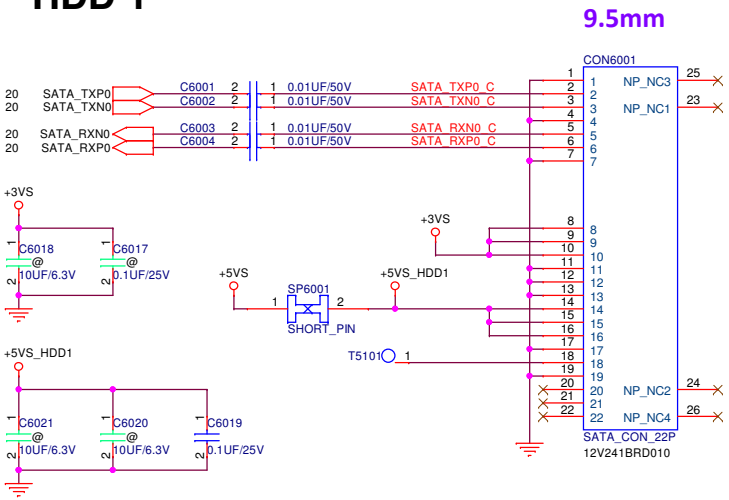
MIC JACK



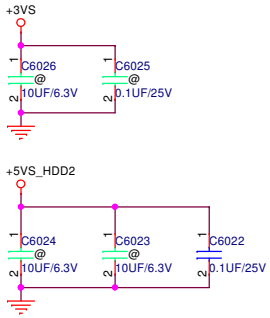
R1.1 Add 2nd MIC schematic 0804

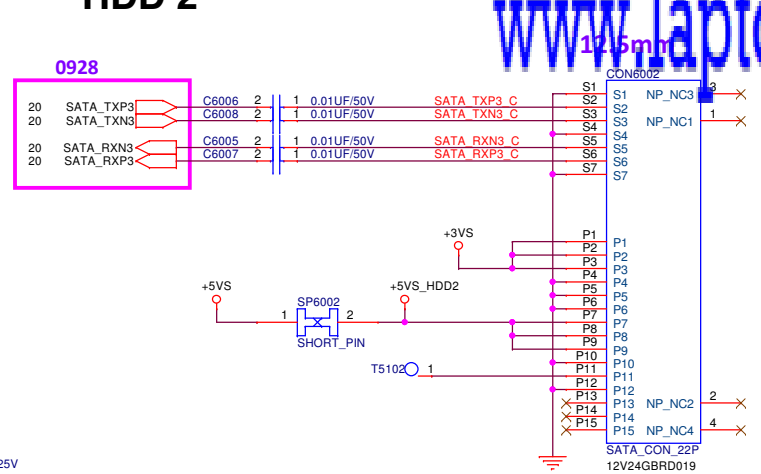
PEGATRON	Title : IO	
BG1-NB1-HW-NB5	Engineer: Wing_Cheng	
Size: C	Project Name: BA52HR/CR	Rev: 1.0
Date: Monday, February 13, 2012	Sheet 58 of 77	

HDD 1

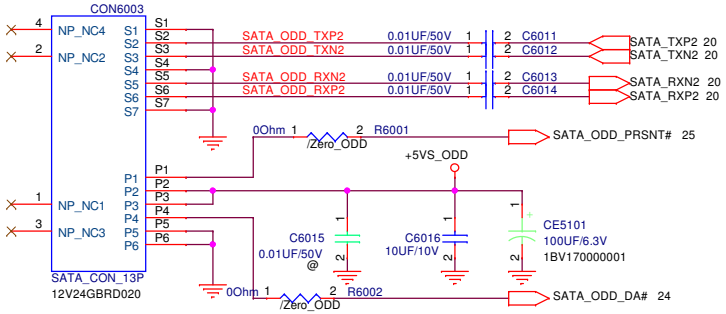


HDD 2



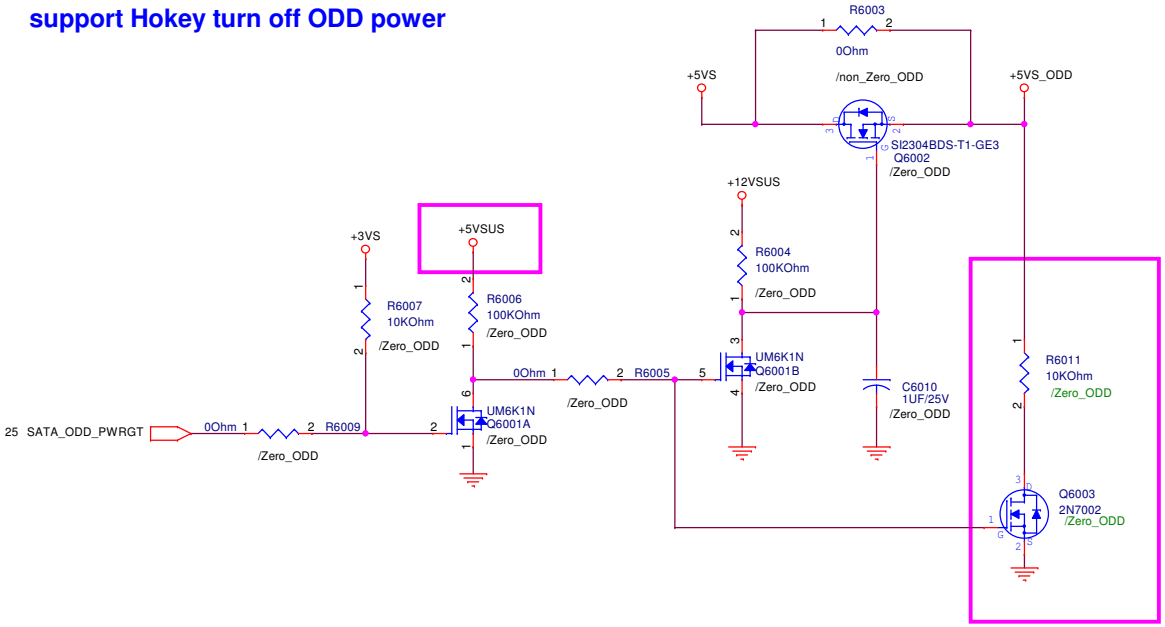


ODD



ZERO POWER ODD SUPPORT

support Hokey turn off ODD power



PEGATRON	Title : SATA HDD/ ODD	
BU1-RD Div.1-HW RD Dept.1	Engineer: Wing_Cheng	
Size: Custom	Project Name: BA52HR/CR	Rev: 1.0
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MB USB

FRESCO(USB30) PCH(USB20) COLAY

FRESCO(USB30) PCH(USB30) COLAY

FRESCO(USB30) PCH(USB20) COLAY

FRESCO(USB30) PCH(USB30) COLAY

Sleep & Charge

PLACE ESD Diodes 0700-0014000 near Connector

USB 3.0

USB 2.0

USB 3.0

USB 2.0

no sleep & charge

IO Board

USB Power Switch for USB DB Main

BIOS debug port

AUDIO BOARD/w USB2.0 x2

A_GND

PEGATRON Title : USB PORTS eSATA

Engineer: Wing_Cheng

BA52HR/CR

PEGATRON Title : Camera/ BT/ FL CONN

BU1-RD Div.1-HW RD Dept.1 Engineer: Wing_Cheng

Size	Project Name	Rev
Custom	BA52HR/CR	1.0

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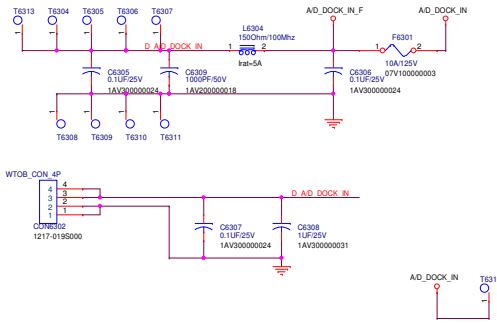
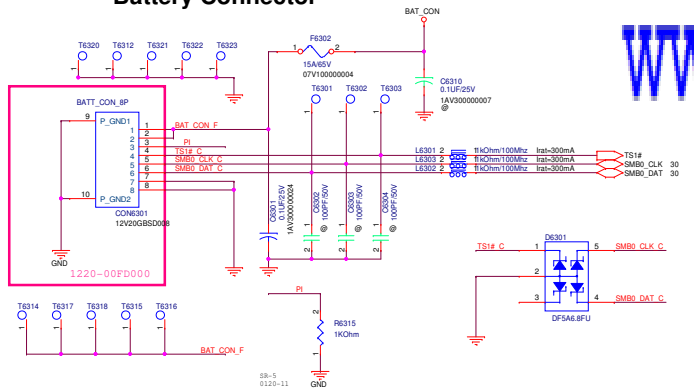
DC IN

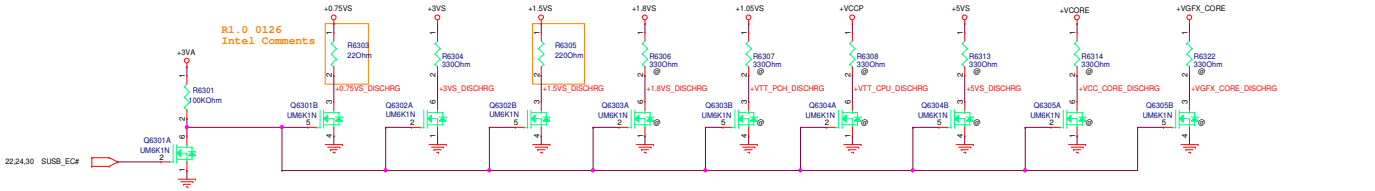


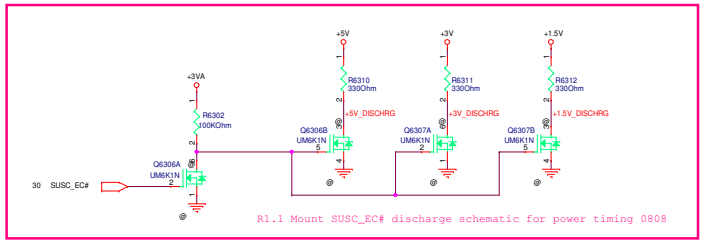
Battery Connector

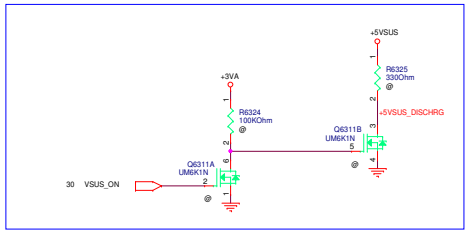


Discharge Circuit

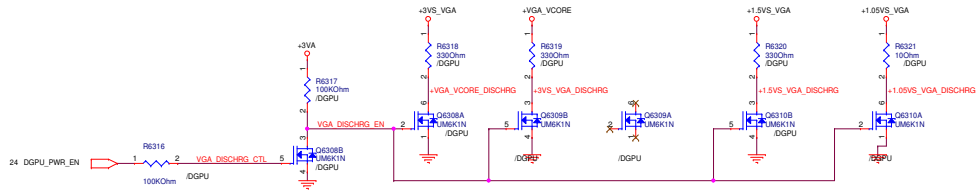
Frank
0505 Follow EVEREST







VGA Discharge Circuit



Unmount +VGA_Vcore discharg

PEGATRON	Title : DC-IN DISCHARGE		
BU1-RD Div.1-HW RD Dept.1	Engineer: Wing_Cheng		
Size: Custom	Project Name: BA52HR/CR		Rev: 1.0
Date: Monday, February 13, 2012	Sheet 63 of 77		

PEGATRON

Title : USB PORTS/ eSATA

BU1-RD Div.1-HW RD Dept.1

Engineer: *Wing_Cheng*

Size	Project Name	Rev
A	**BA52HR/CR**	1.0

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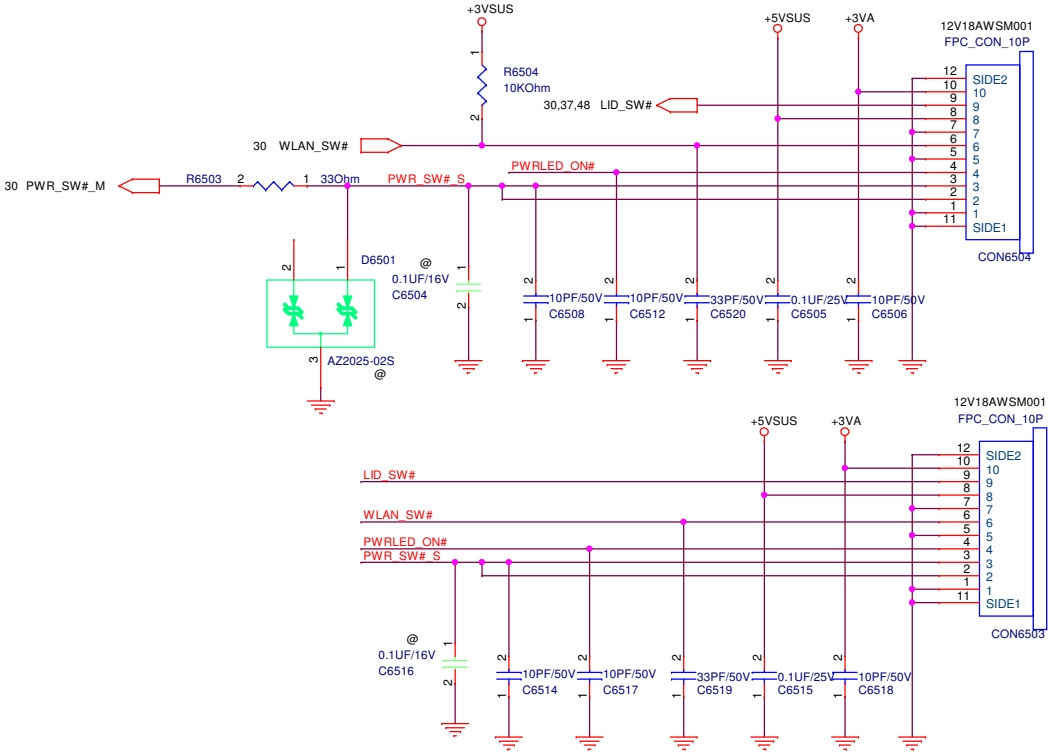
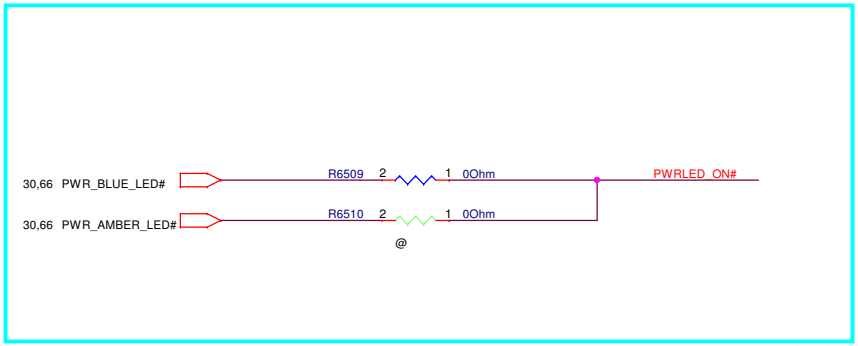
PWR BRD/ AMBIENT/ HALL CONN.

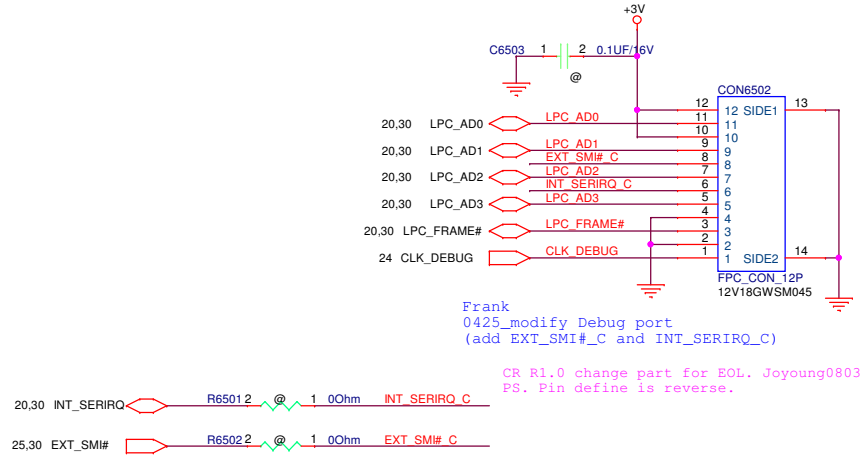




R1.2-28

change Power LED CON6503 circuit

DEBUG CARD CONN.

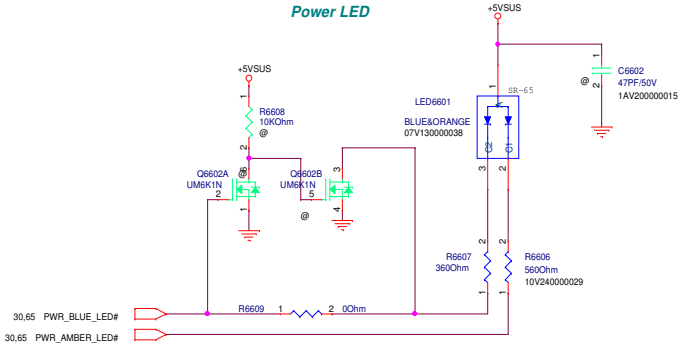


Frank
0425_modify Debug port
(add EXT_SMI#_C and INT_SERIRQ_C)

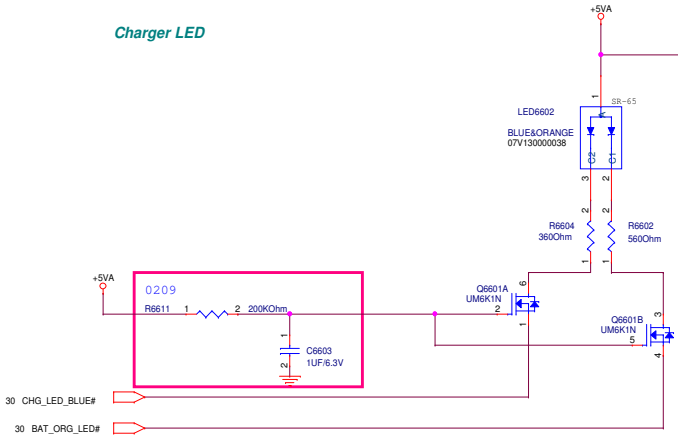
CR R1.0 change part for EOL. Joyoung0803
PS. Pin define is reverse.

PEGATRON	Title : MDC/ PWR SW/ Debug		
BU1-RD Div.1-HW RD Dept.1	Engineer: Wing_Cheng		
Size: Custom	Project Name: BA52HR/CR		Rev: 1.0
Date: Monday, February 13, 2012	Sheet 65 of 77		

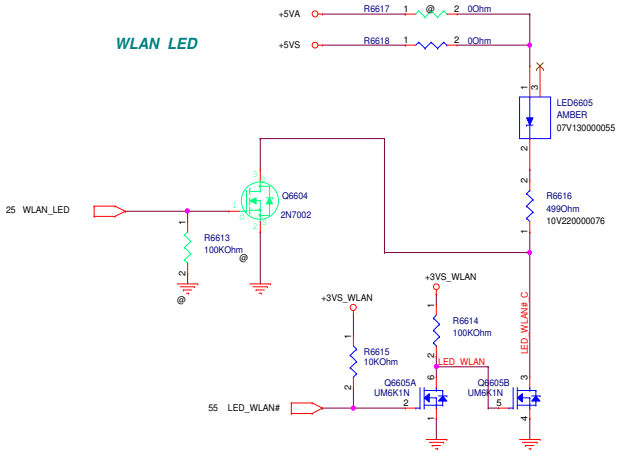
Power LED



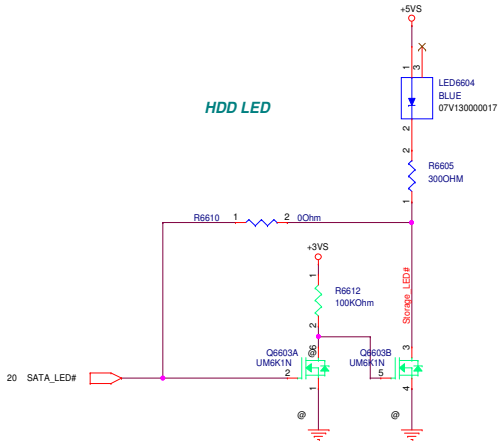
Charger LED



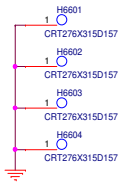
WLAN LED



HDD LED



CPU Screw B x 4

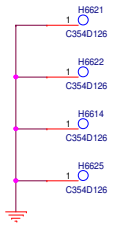


GPU Screw P x 2

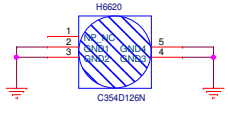
Fix hole D x 1

Fix hole N x 1

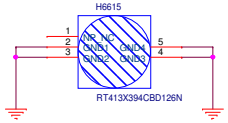
Screw A x 4 (PTH)



Screw A x 2 (NPTH)

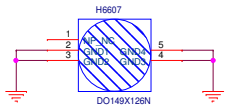


Screw hole R x 1

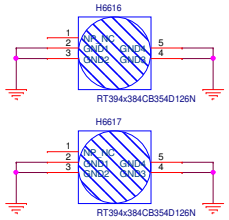


Screw hole T x 1

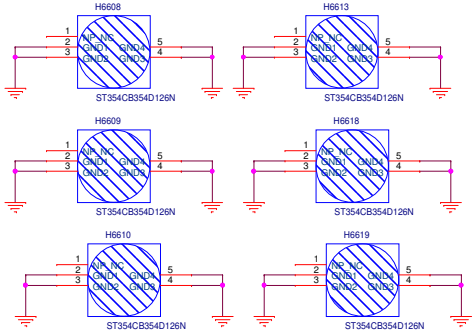
Screw hole V x 1

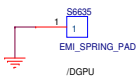


Screw hole S x 2

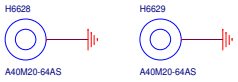


Screw hole Q x 6

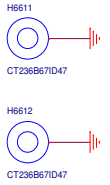




WLAN NUT



PCH Local Side Symbol



PEGATRON	Title : LED/ CIR/ FN/ SCREW	
BU1-RD Div.1-HW RD Dept.1	Engineer: Wing_Cheng	
Size: Custom	Project Name: BA52HR/CR	Rev: 1.0
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PEGATRON	Title : TPM		
Pegatron Corp.	Engineer: Wing_Cheng		
Size: B	Project Name: BA52HR/CR		Rev: 1.0
Date: Monday, February 13, 2012	Sheet 67 of 77		

PEGATRON

Title : Finger Printer

Pegatron Corp.

Engineer: Wing_Cheng

Size	Project Name	Rev
A	BA52HR/CR	1.0

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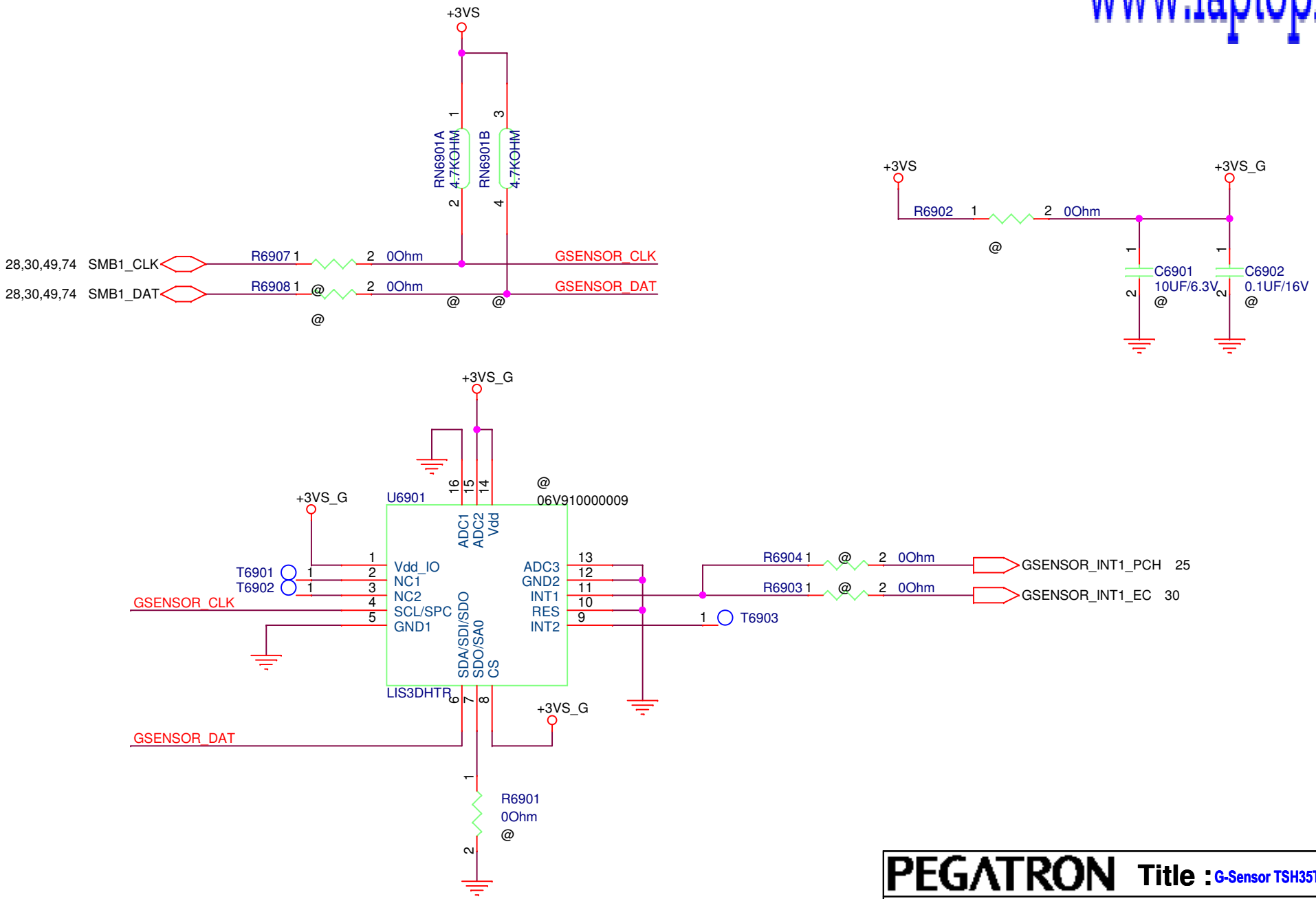
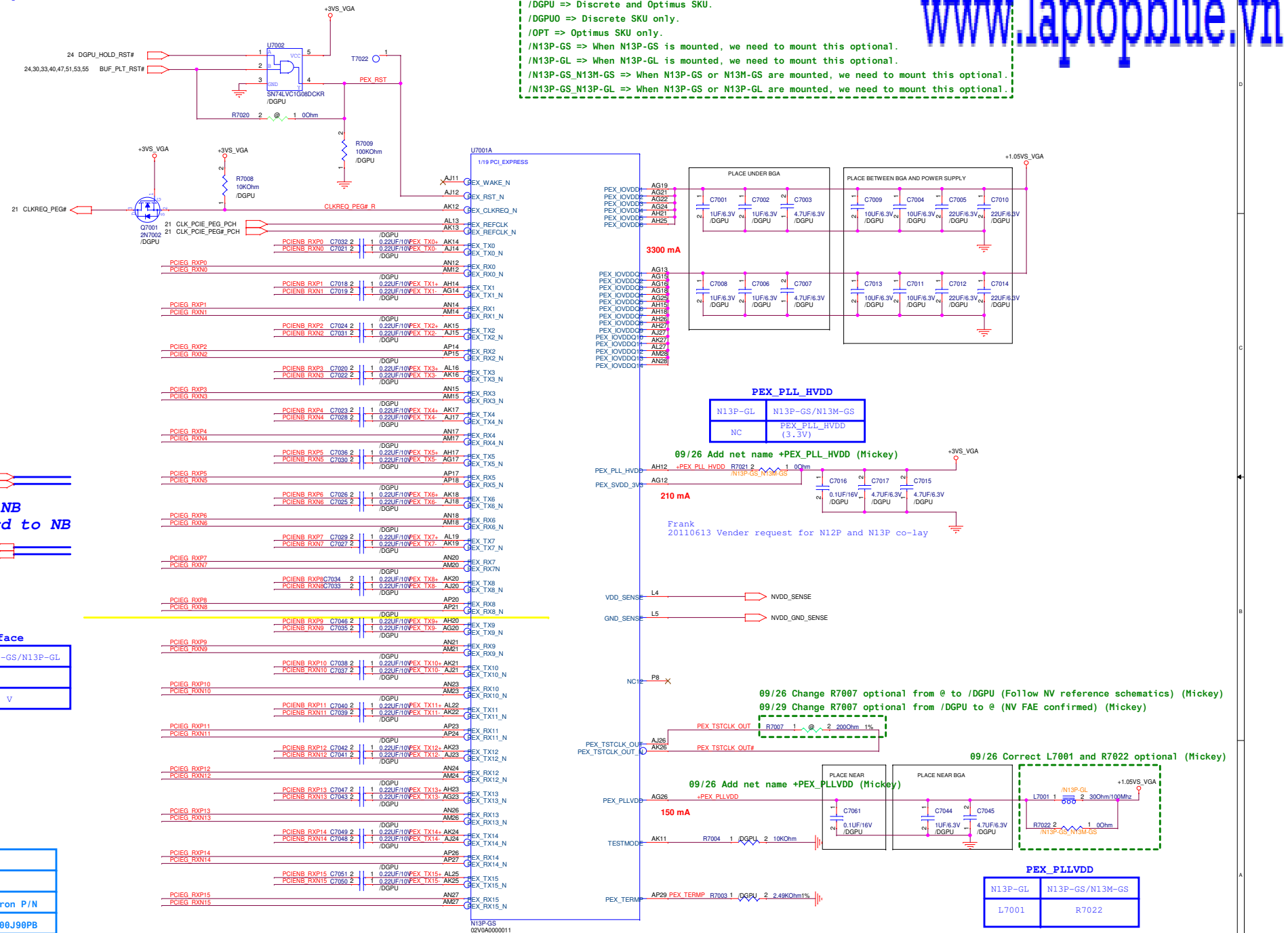


PEGATRON	Title : G-Sensor TSH35TR	
BU1-RD Div.1-HW RD Dept.1	Engineer: Wing_Cheng	
Size: A	Project Name	Rev: 1.0
Date: Monday, February 13, 2012	Sheet 69 of 77	

Frank
20110513 Change N13P GPU.

GPU BOM Optional Definition

@ => Unmount.
/DGPU => Discrete and Optimus SKU.
/DGPUO => Discrete SKU only.
/OPT => Optimus SKU only.
/N13P-GS => When N13P-GS is mounted, we need to mount this optional.
/N13P-GL => When N13P-GL is mounted, we need to mount this optional.
/N13P-GS_N13M-GS => When N13P-GS or N13M-GS are mounted, we need to mount this optional.
/N13P-GS_N13P-GL => When N13P-GS or N13P-GL are mounted, we need to mount this optional.



3 PCIENB_RXP[0..15]
3 PCIENB_RXN[0..15]

PEX=> From NB
EXP: VGA Card to NB

3 PCIEG_RXP[0..15]
3 PCIEG_RXN[0..15]

PCIE interface

	N13M-GS	N13P-GS/N13P-GL
8 Lane	V	
16 Lane		V

GPU Information		
GPU Location : U7001		
Type	Version	Pegatron P/N
N13P-GS	ES	020A-00J90PB
N13P-GL	QS	020A-00K60PB
N13M-GS	ES	020A-00JD0PB

PEGATRON
PEGATRON COMPUTER INC
Title : GPU_PEG*16
Engineer: Mickey_Yu
Size C | Project Name VA70_N13P-GDDR3 | Rev 1.0
P/N
Date: Monday, February 13, 2012 Sheet 70 of 99

FB_CLAMP

N13P-GL	N13P-GS/N13M-GS
NC	PD 10K

09/26 Change R7120 optional from /DGPU to /N13P-GS_N13M-GS (Mickey)

09/27 Change net name from +FB_DLL_AVDD to +FB_PLL_AVDD (Mickey)

FB_DLL_AVDD

N13P-GL	N13P-GS/N13M-GS
NC	FB_DLL_AVDD (1.05V)

09/26 Add net name +FB_DLL_AVDD_R (Mickey)

11/14 Delete T7102,T7103,T7105,T7106,T7107,T7108 (NV Recommend) (Mickey)

09/26 Change R7103,R7104 optional from /DGPU to /N13P-GS_N13P-GL (Mickey)

	N13M-GS	N13P-GS/N13P-GL
R7103/R7104	unmount	mount

For GDDR5

For GDDR5

09/26 Add net name +FB_PLL_AVDD_GPU (Mickey)

Frank
20110613 Vender request for N12P and N13P co-lay

FBB_PLL_AVDD

N13P-GL/N13M-GS	N13P-GS
NC	FBB_PLL_AVDD (1.05V)

Frank
20110613 Vender suggest C7119 change 22UF.

Title :	GPU_DDR3 FB
PEGATRON COMPUTER INC	Engineer: Mickey_Yu
Size: C	Project Name: VA70_N13P-GDDR3
P/N:	Rev: 1.0
Date: Monday, February 13, 2012	Sheet 71 of 99

10/03 Change C7203 optional from /DGPUO to @ (Follow NV FAE recommend) (Mickey)
09/27 Change L7201 from 300ohm bead to 220ohm bead (Follow NV design guide) (Mickey)
09/27 Change R7202,C7206 optional from /DGPU to /N13P-GS_N13P-GL (Mickey)
09/26 Change R7201 optional from /DGPU to /OPT (Mickey)
09/26 Change C7201~7205,L7201 optional from /DGPU to /DGPUO (Mickey)

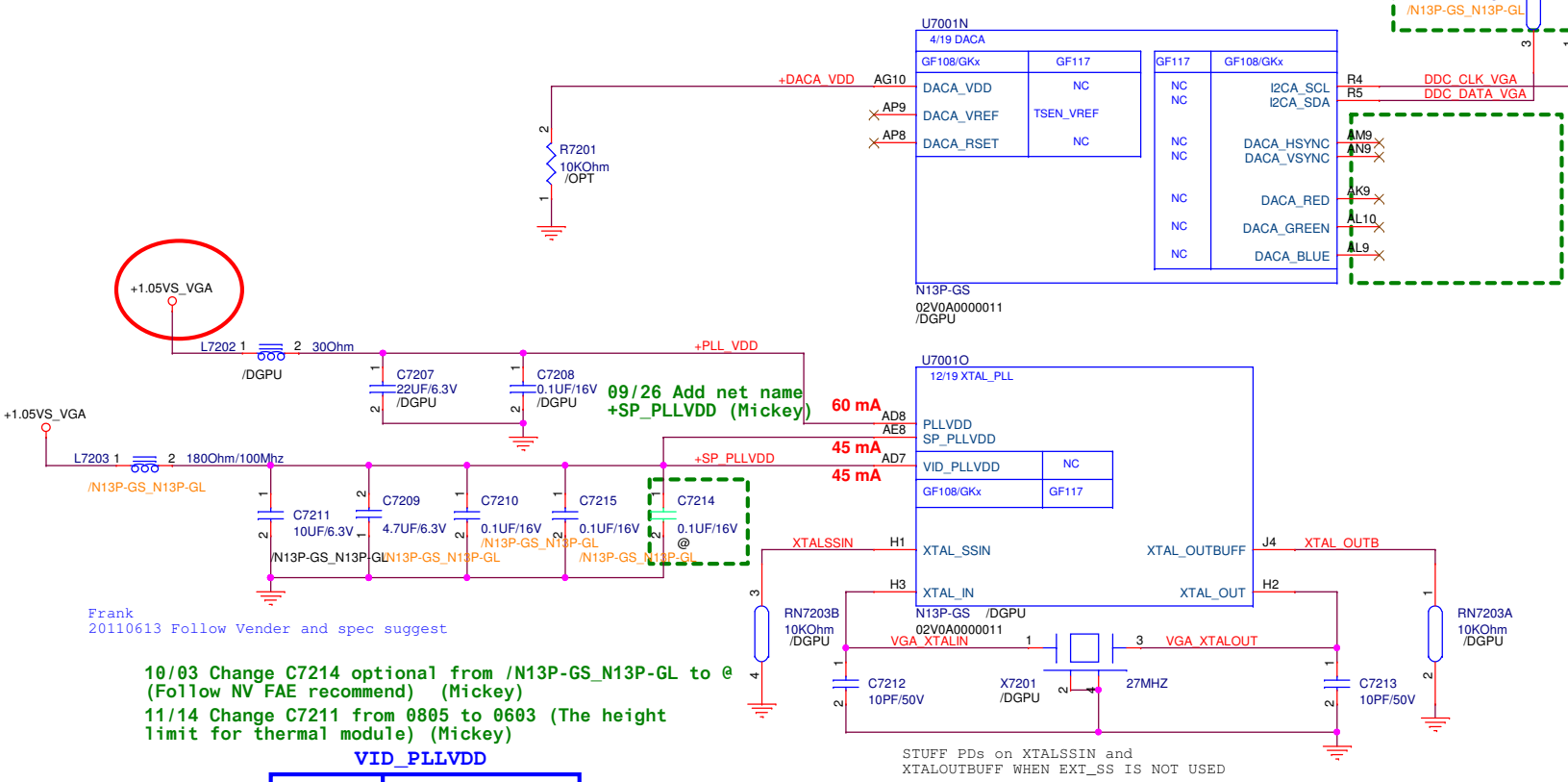
RGB

N13M-GS	N13P-GL/N13P-GS
NC	RGB Function

09/26 Change RN7201 optional from /DGPU to /N13P-GS_N13P-GL (Mickey)

09/29 Correct the net name of DDC_CLK_VGA, DDC_DATA_VGA,DAC_HSYNC_VGA and DAC_VSYNC_VGA (Mickey)

11/29 Remove net DAC_HSYNC_VGA, DAC_VSYNC_VGA, DAC_VR, DAC_VG, DAC_VB for VGA_Vcore power plane improvement(Elmer)



Frank
20110613 Follow Vender and spec suggest

10/03 Change C7214 optional from /N13P-GS_N13P-GL to @ (Follow NV FAE recommend) (Mickey)
11/14 Change C7211 from 0805 to 0603 (The height limit for thermal module) (Mickey)

VID_PLLVDD

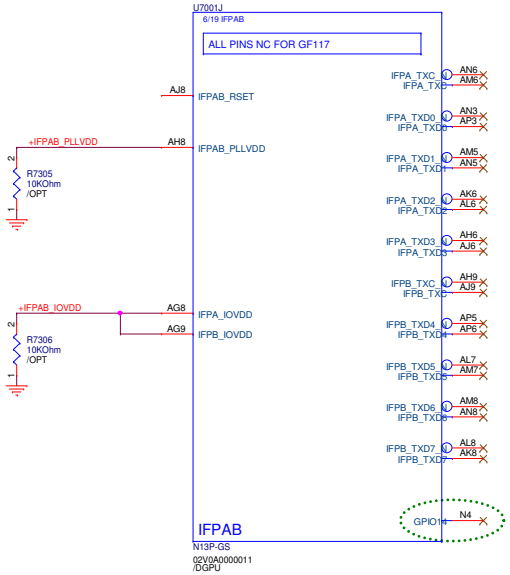
N13M-GS	N13P-GL/N13P-GS
NC	VID_PLLVDD (1.05V)

11/16 Change C7212,C7213 from 18pF to 8.2pF (Crystal vendor recommend) (Mickey)

PEGATRON
PEGATRON COMPUTER INC

Title : GPU_RGB/XTAL
Engineer: Mickey_Yu
Size: B
Project Name: VA70_N13P-GDDR3
P/N:
Rev: 1.0
Date: Monday, February 13, 2012
Sheet 72 of 99

LVDS

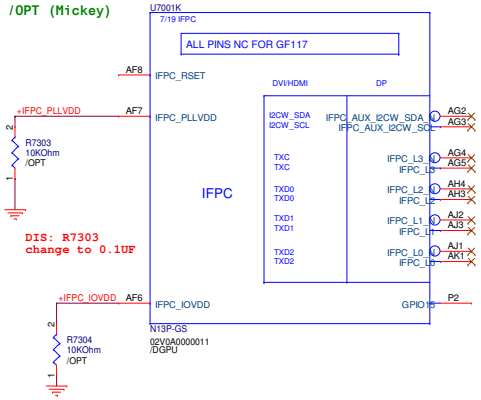


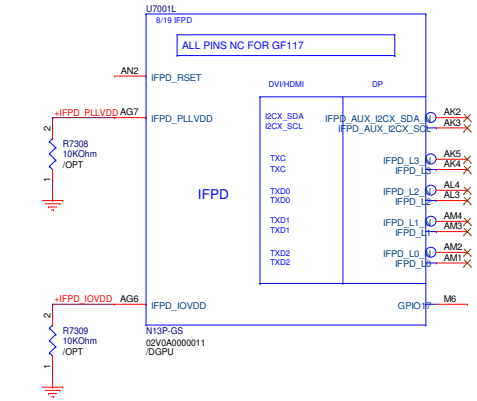
09/27 Change R7302 optional from /DGPU to /N13P-GS_N13P-GL (Mickey)

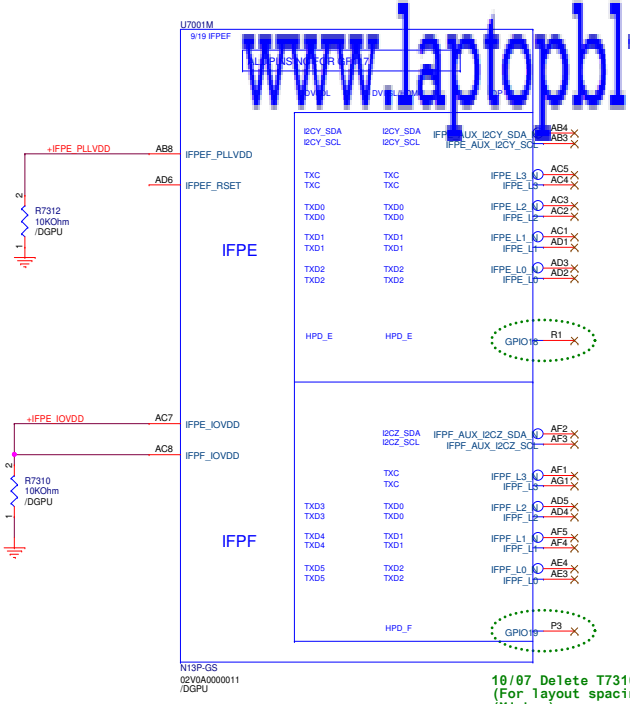
09/26 Change R7303,R7304 optional from /DGPU_ONLY to /OPT (Mickey)

09/26 Change C7307~7315,L7303,L7305 optional from /DGPU_ONLY to /DGPUO (Mickey)

HDMI







10/07 Delete T7310,T7311 (For layout spacing) (Mickey)

GPIO

	N13M-GS	N13P-GS/N13P-GL
GPIO14	X	V
GPIO15	X	V
GPIO16	X	V
GPIO17	X	V
GPIO18	X	V
GPIO19	X	V

IFPX channel

	N13M-GS	N13P-GS/N13P-GL	
IFPA/B	X	V	LVDS
IFPC	X	V	HDMI
IFPD	X	V	EDP
IFPE/F	X	V	

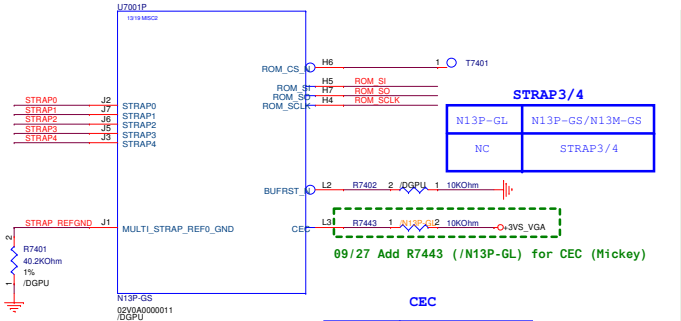
PEGATRON COMPUTER INC

Title : GPU_LVDS/HDMI/EDP

Engineer: Mickey_Yu

Size	Project Name	Rev
C	VA70_N13P-GDDR3	1.0
	P/N	

Date: Monday, February 13, 2012 Sheet 73 of 99



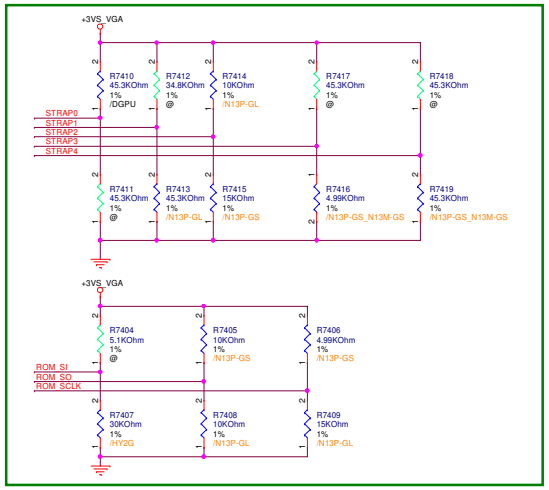
STRAP3/4

N13P-GL	N13P-GS/N13M-GS
NC	STRAP3/4

09/27 Add R7443 (/N13P-GL) for CEC (Mickey)

CEC

N13P-GL	N13P-GS/N13M-GS
PU 10K (3V3)	NC



N13P-GS ES2/QS			
DEVICE ID	0xFDB		
STRAP0	45K PU		
STRAP1	35K PD		
STRAP2	15K PD		
STRAP3	5K PD		
STRAP4	10K PD		
ROM_SCLK	5K PU		
ROM_SI	Hynix 128Mx16	35K PD	
	Hynix 64Mx16	15K PD	R7407
ROM_SO	10K PU		

N13P-GL QS			
DEVICE ID	0xDE9		
STRAP0	45K PU		
STRAP1	45K PD		
STRAP2	10K PU		R7414
STRAP3	NC		
STRAP4	NC		
ROM_SCLK	15K PD		
ROM_SI	Hynix 128Mx16	35K PD	
	Hynix 64Mx16	15K PD	R7407
ROM_SO	10K PD		

Correct the resister value of all straps for N13P-GS ES and N13P-GL QS (Follow NV FAE recommend)

STRAP2--GPU TYPE

N13P-GS	N13P-GL	N13P-GT

ROM_SI--VRAM TYPE

HYNIX		SAMSUNG	
64Mx16	128Mx16	64Mx16	128Mx16

STRAP1 R7413	N13P-GS ES2/QS	N13P-GL QS
	35K	45K

ROM_SI R7407	Hynix 128Mx16	Hynix 64Mx16
	35K	15K

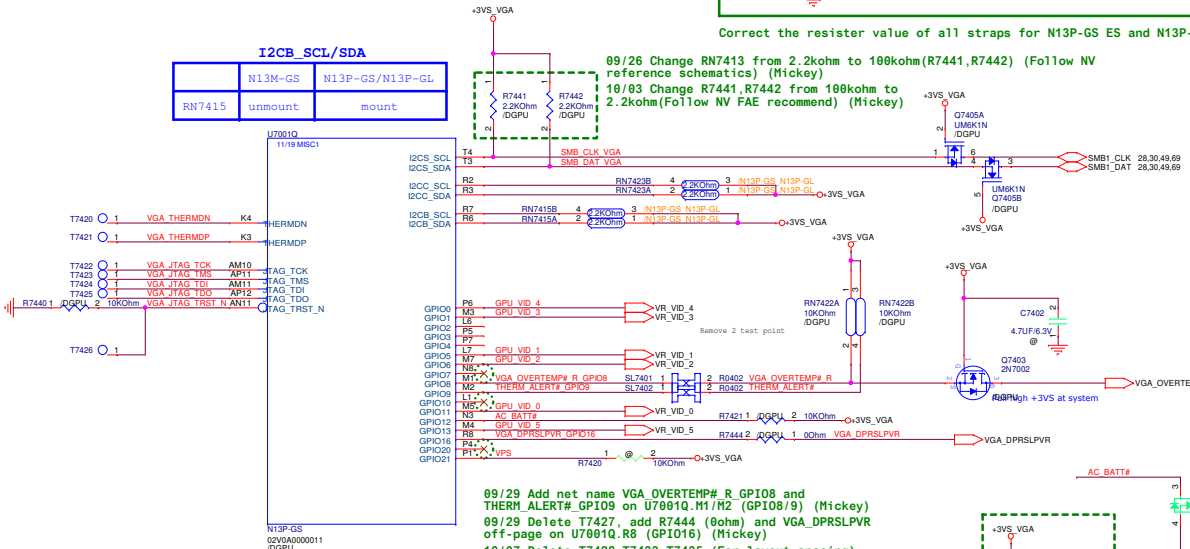
11/28 Change R7413 from /DGPU to /N13P-GS (Follow NV FAE recommend) (Mickey)
11/28 Change R7414 from 20kohm to 10kohm(/N13P-GL) (Follow NV FAE recommend) (Mickey)
11/28 Change R7415 from 5kohm to 15kohm(/N13P-GS) (Follow NV FAE recommend) (Mickey)

N13P-GT ES2/QS			
DEVICE ID	0xFD1		
STRAP0	45K PU		
STRAP1	35K PD		
STRAP2	10K PD		
STRAP3	5K PD		
STRAP4	10K PD		
ROM_SCLK	5K PU		
ROM_SI	Hynix 128Mx16	35K PD	
	Hynix 64Mx16	15K PD	R7407
ROM_SO	10K PU		

I2CB_SCL/SDA

	N13M-GS	N13P-GS/N13P-GL
RN7415	unmount	mount

09/26 Change RN7413 from 2.2kohm to 100kohm(R7441,R7442) (Follow NV reference schematics) (Mickey)
10/03 Change R7441,R7442 from 100kohm to 2.2kohm(Follow NV FAE recommend) (Mickey)



09/29 Add net name VGA_OVERTEMP#_R_GPIO8 and THERM_ALERT#_GPIO9 on U7001Q.M1/M2 (GPIO8/9) (Mickey)
09/29 Delete T7427, add R7444 (0ohm) and VGA_DPRSLPVR off-page on U7001Q.R8 (GPIO16) (Mickey)
10/07 Delete T7428,T7433,T7435 (For layout spacing) (Mickey)

GPIO

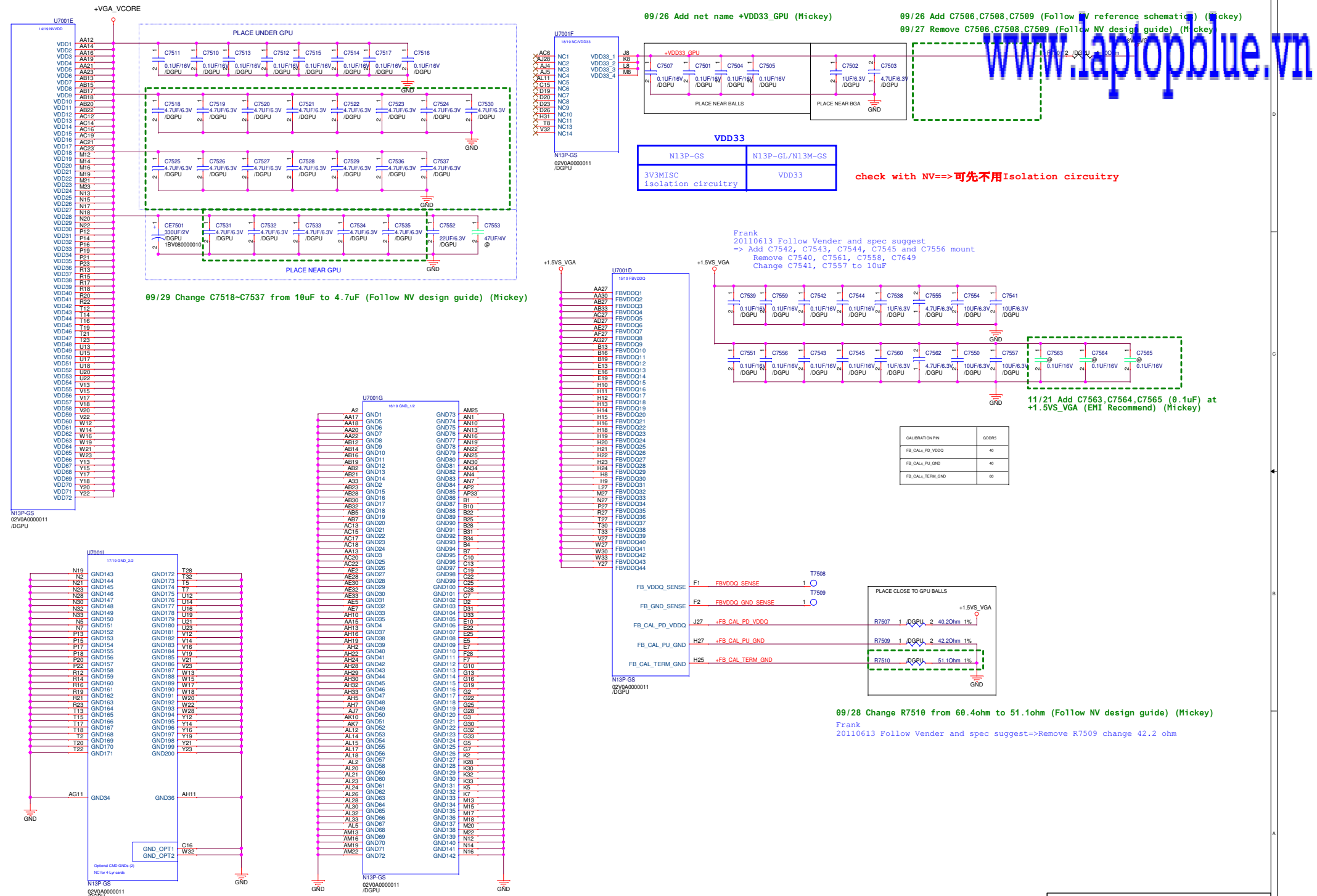
	N13M-GS	N13P-GS/N13P-GL
GPIO20	X	X
GPIO21	X	X

GPIO 8

	N13P-GL	N13P-GS/N13M-GS
Q7403	unmount	NV suggestion mount

09/29 Change Q7401,Q7402 optional from @ to /DGPU(Mickey)
09/29 Change net name from VPS to THERM_ALERT# on Q7402.2 (Mickey)
09/29 Change net name from VPS_EC to THERM_ALERT#_EC on Q7402.3 (Mickey)

PEGATRON
PEGATRON COMPUTER INC
Title : GPU_GPIO/STRAP
Engineer: Mickey_Yu
Size: A2 | Project Name: VA70_N13P-GDDR3 | Rev: 1.0 | P/N:
Date: Monday, February 13, 2012 | Sheet 74 of 99


+VGA_VCORE
U7001E
14/19 NVVDD
N13P-GS
02V0A0000011
/DGPU
PLACE UNDER GPU
PLACE NEAR GPU
09/29 Change C7518~C7537 from 10uF to 4.7uF (Follow NV design guide) (Mickey)
09/26 Add net name +VDD33_GPU (Mickey)
09/26 Add C7506,C7508,C7509 (Follow NV reference schematic) (Mickey)
09/27 Remove C7506,C7508,C7509 (Follow NV design guide) (Mickey)
U7001F
18/19 NC/VDD33
+VDD33_GPU
PLACE NEAR BALLS
PLACE NEAR BGA
VDD33
N13P-GS
N13P-GL/N13M-GS
3V3MISC isolation circuitry
VDD33
check with NV==>可先不用Isolation circuitry
Frank
20110613 Follow Vender and spec suggest
=> Add C7542, C7543, C7544, C7545 and C7556 mount
Remove C7540, C7561, C7558, C7649
Change C7541, C7557 to 10uF
+1.5VS_VGA
U7001D
15/19 FBVDDQ
11/21 Add C7563,C7564,C7565 (0.1uF) at +1.5VS_VGA (EMI Recommend) (Mickey)
CALIBRATION PIN
GDDR5
FB_CALx_PD_VDDQ
40
FB_CALx_PU_GND
40
FB_CALx_TERM_GND
60
U7001G
16/19 GND_1/2
U7001I
17/19 GND_2/2
FB_VDDQ_SENSE
FB_GND_SENSE
FB_CAL_PD_VDDQ
FB_CAL_PU_GND
FB_CAL_TERM_GND
PLACE CLOSE TO GPU BALLS
09/28 Change R7510 from 60.4ohm to 51.1ohm (Follow NV design guide) (Mickey)
Frank
20110613 Follow Vender and spec suggest=>Remove R7509 change 42.2 ohm
www.laptopblue.vn
PEGATRON
PEGATRON COMPUTER INC
Title : GPU_Power/GND
Engineer: Mickey_Yu
Size C
Project Name VA70_N13P-GDDR3
Rev 1.0
P/N
Date: Monday, February 13, 2012
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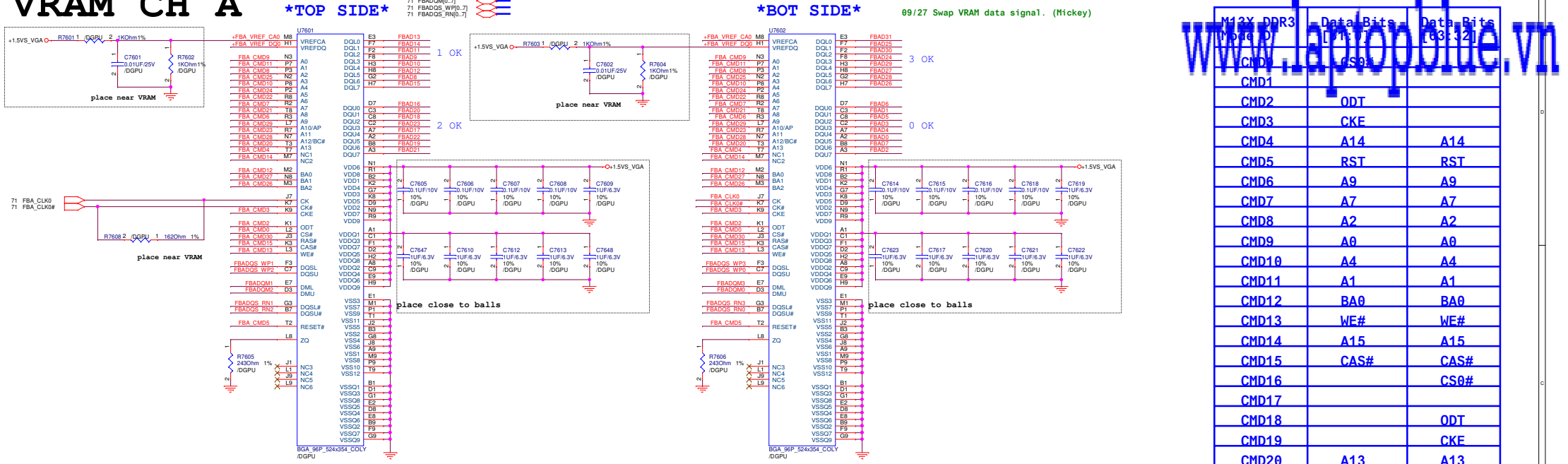
VRAM CH A

TOP SIDE

BOT SIDE

09/27 Swap VRAM data signal. (Mickey)



M13X DDR3	Data Bits [31:0]	Data Bits [63:32]
CMD0	CS0#	
CMD1		
CMD2	ODT	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE#	WE#
CMD14	A15	A15
CMD15	CAS#	CAS#
CMD16		CS0#
CMD17		
CMD18		ODT
CMD19		CKE
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS#	RAS#
CMD31		

VRAM Information				VRAM Strap	
VRAM Location : U7601,U7602,U7603,U7604,U7701,U7702,U7703,U7704				VRAM Strap Location : R7407	
Vendor	Configuration	Pegatron P/N	Manufacturer P/N		
Hynix	128Mx16	0315-00ND0PB	H5TQ2G63BFR-11C	0x6	35K
Hynix	64Mx16	0315-00NF0PB	H5TQ1G63DFR-11C	0x2	15K
Micron	128Mx16	TBD	MT41J128M16JT-107G:K	TBD	TBD
Micron	64Mx16	0315-00SG0PB	MT41J64M16JT-107G:G	TBD	TBD

PEGATRON

PEGATRON COMPUTER INC

Title : GPU_VRAM CHA

Engineer: Mickey_Yu

Size	Project Name	Rev
A2	VA70 N13P-GDDR3	1.0
	P/N	

Date: Monday, February 13, 2012 Sheet 78 of 99

VRAM CH C

TOP SIDE

BOT SIDE

09/27 Swap VRAM data signal. (Mickey)

Mode D	Data Bits [31:0]	Data Bits [63:32]
CMD0	CS0#	
CMD1		
CMD2	ODT	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE#	WE#
CMD14	A15	A15
CMD15	CAS#	CAS#
CMD16		CS0#
CMD17		
CMD18		ODT
CMD19		CKE
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS#	RAS#
CMD31		

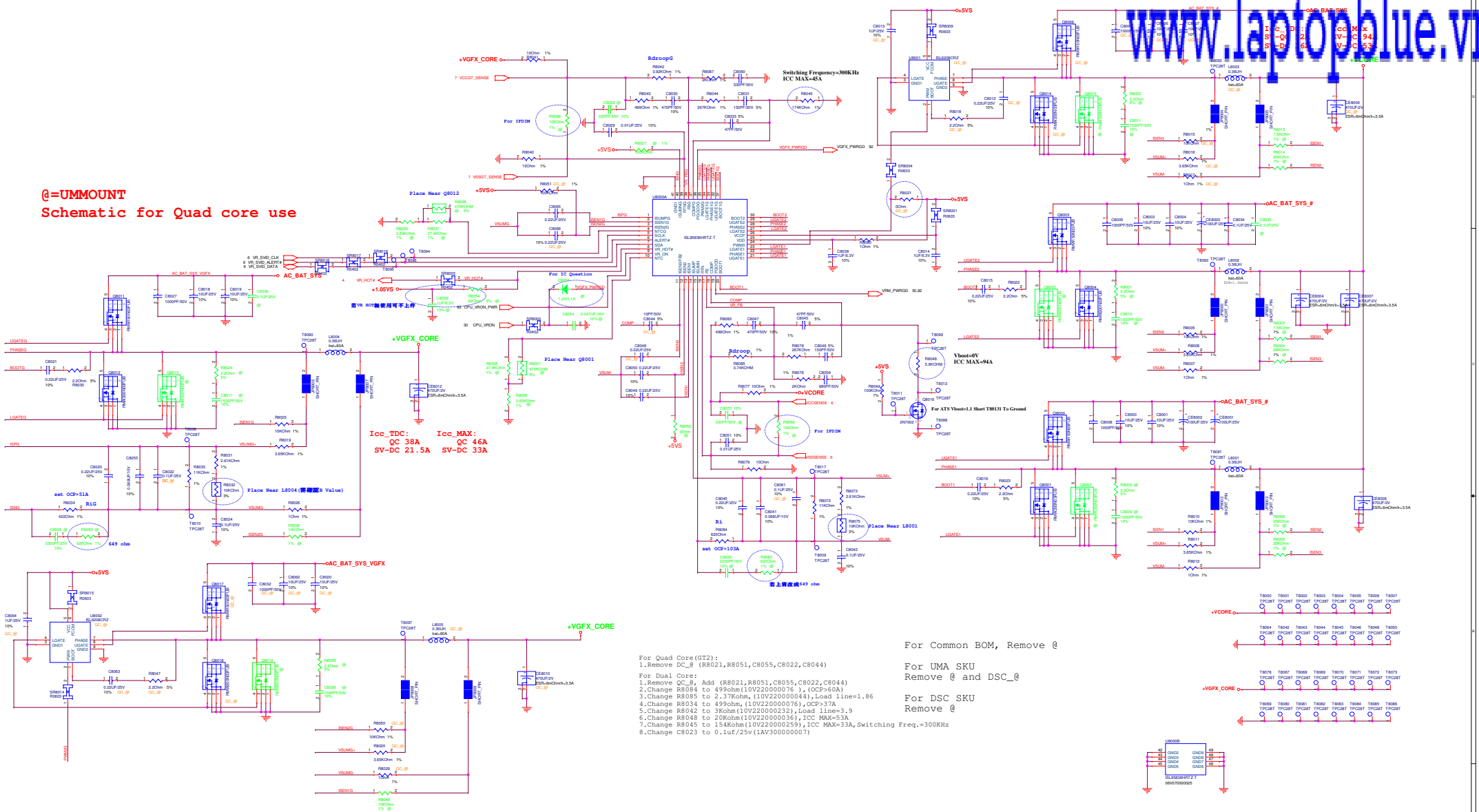
PEGATRON	Title :	GPU_VRAM CHB
PEGATRON COMPUTER INC	Engineer:	Mickey_Yu
Size: Custom	Project Name:	VA70 N13P-GDDR3
P/N:	Rev:	1.0
Date: Monday, February 13, 2012	Sheet	77 of 99

PEGATRON	Title :		
PEGATRON COMPUTER INC	Engineer:	Mickey_Yu	
Size: C	Project Name: VA70_N13P-GDDR3		Rev: 1.0
	P/N:		
Date: Monday, February 13, 2012	Sheet 78 of 99		

PEGATRON	Title : GPU_PEG*16		
PEGATRON COMPUTER INC	Engineer: Mickey_Yu		
Size: C	Project Name: VA70_N13P-GDDR3		Rev: 1.0
	P/N:		
Date: Monday, February 13, 2012	Sheet 79 of 99		

CHIEF RIVER

@=UMMOUNT
Schematic for Quad core use



For Quad Core(GT2):
1.Remove DC_@ (R8021,R8051,C8055,C8022,C8044)

For Dual Core:
1.Remove QC_@, Add (R8021,R8051,C8055,C8022,C8044)
2.Change R8084 to 499ohm(10V2200000076),(OCP>60A)
3.Change R8085 to 2.37Kohm,(10V2200000044),Load line=1.86
4.Change R8034 to 499ohm,(10V2200000076),OCP>37A
5.Change R8042 to 3Kohm(10V2200000232),Load line=3.9
6.Change R8048 to 20Kohm(10V2200000036),ICC MAX=53A
7.Change R8045 to 154Kohm(10V2200000259),ICC MAX=33A,Switching Freq.=300KHz
8.Change C8023 to 0.1uf/25v(1AV300000007)

For Common BOM, Remove @

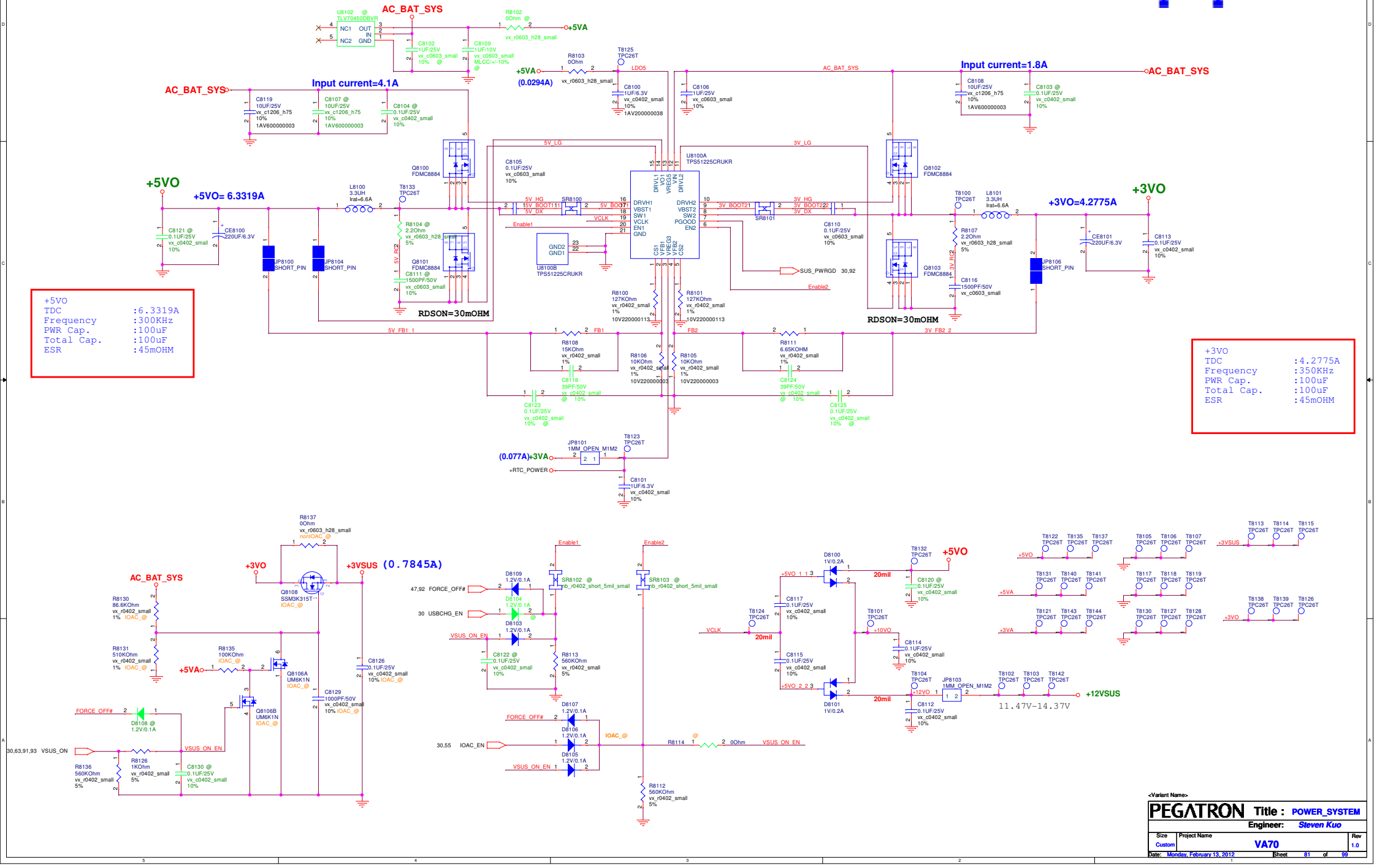
For UMA SKU
Remove @ and DSC_@

For DSC SKU
Remove @

<Variant Name>

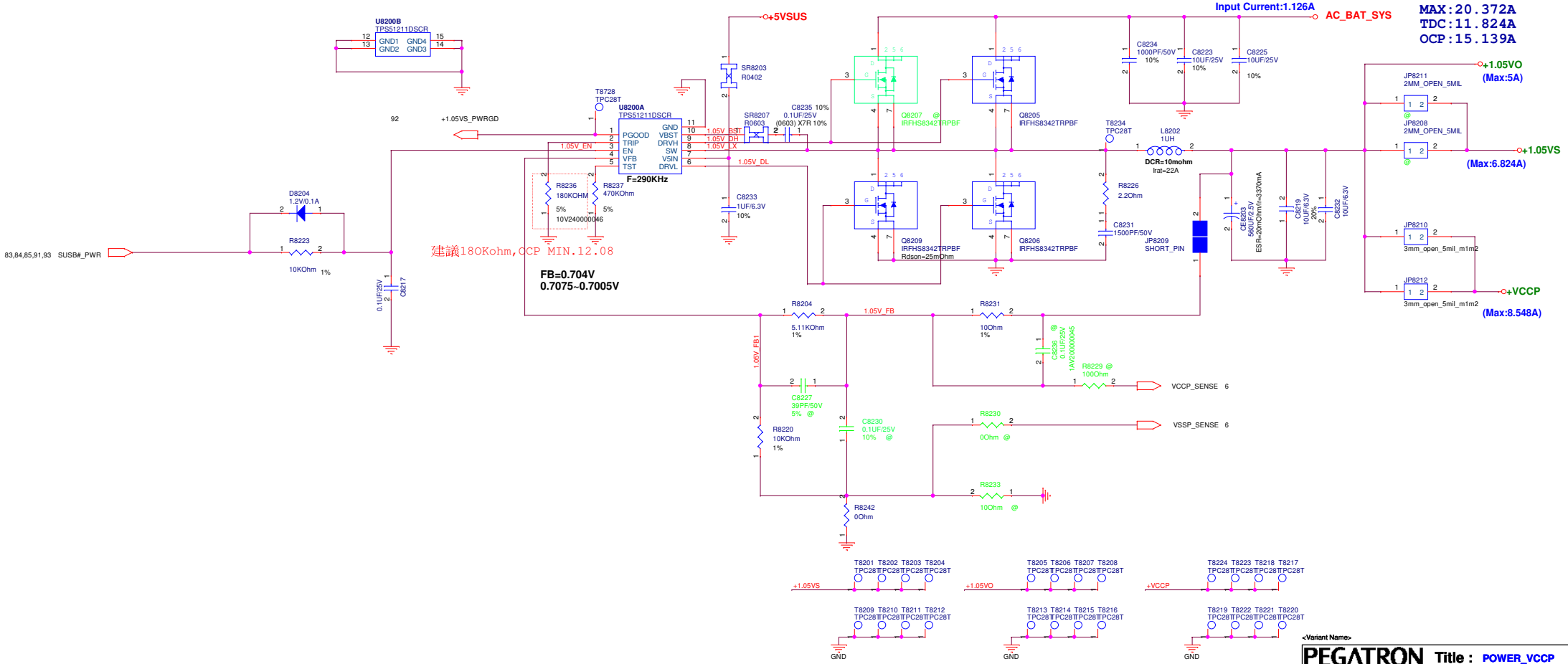
PEGATRON	Title : POWER_VCORE		
	Engineer: Steven Kuo		
Size: Custom	Project Name: VA70		Rev: 1.1
Date: Monday, February 11, 2019	Sheet 80 of 94		

+5VO & +3VO POWER SUPPLY



TRIP V (mV) = TRIP R (k) * TRIP I (mA)
TRIPI current, which is 10uA
VOCP = TRIP V / (8 / Rdson) + (I ripple / 2)

Used for testing purpose in production line.
Pull down to GND with a resistor of 470 kΩ or less



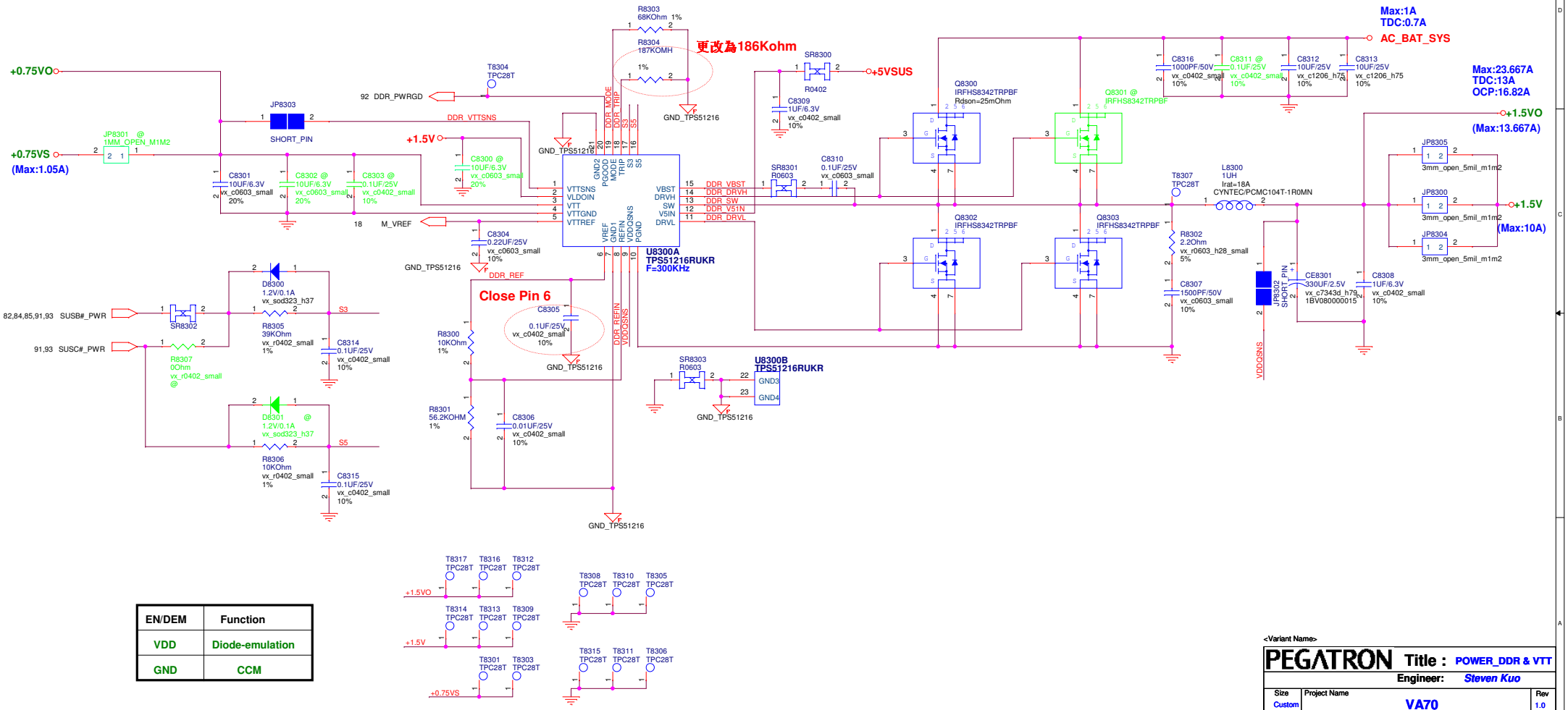
<Variant Name>

PEGATRON Title : POWER_VCCP
Engineer: Steven Kuo

Size	Project Name	Rev
Custom	VA70	1.1

Date: Monday, February 13, 2012 Sheet 82 of 94

DDR & VTT POWER SUPPLY



EN/DEM	Function
VDD	Diode-emulation
GND	CCM

<Variant Name>

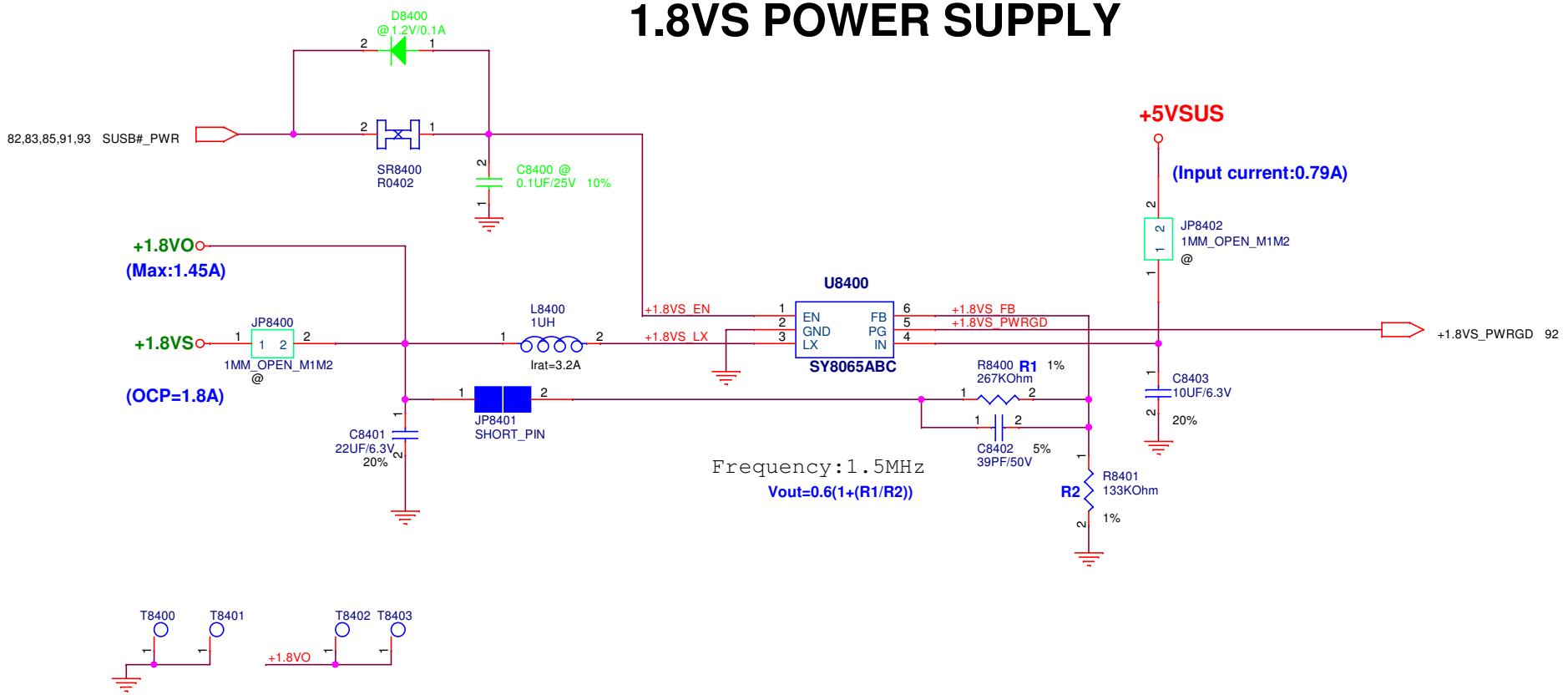
PEGATRON Title : POWER_DDR & VTT

Engineer: Steven Kuo

Size	Project Name	Rev
Custom	VA70	1.0

Date: Monday, February 13, 2012 Sheet 83 of 94

1.8VS POWER SUPPLY



<Variant Name>

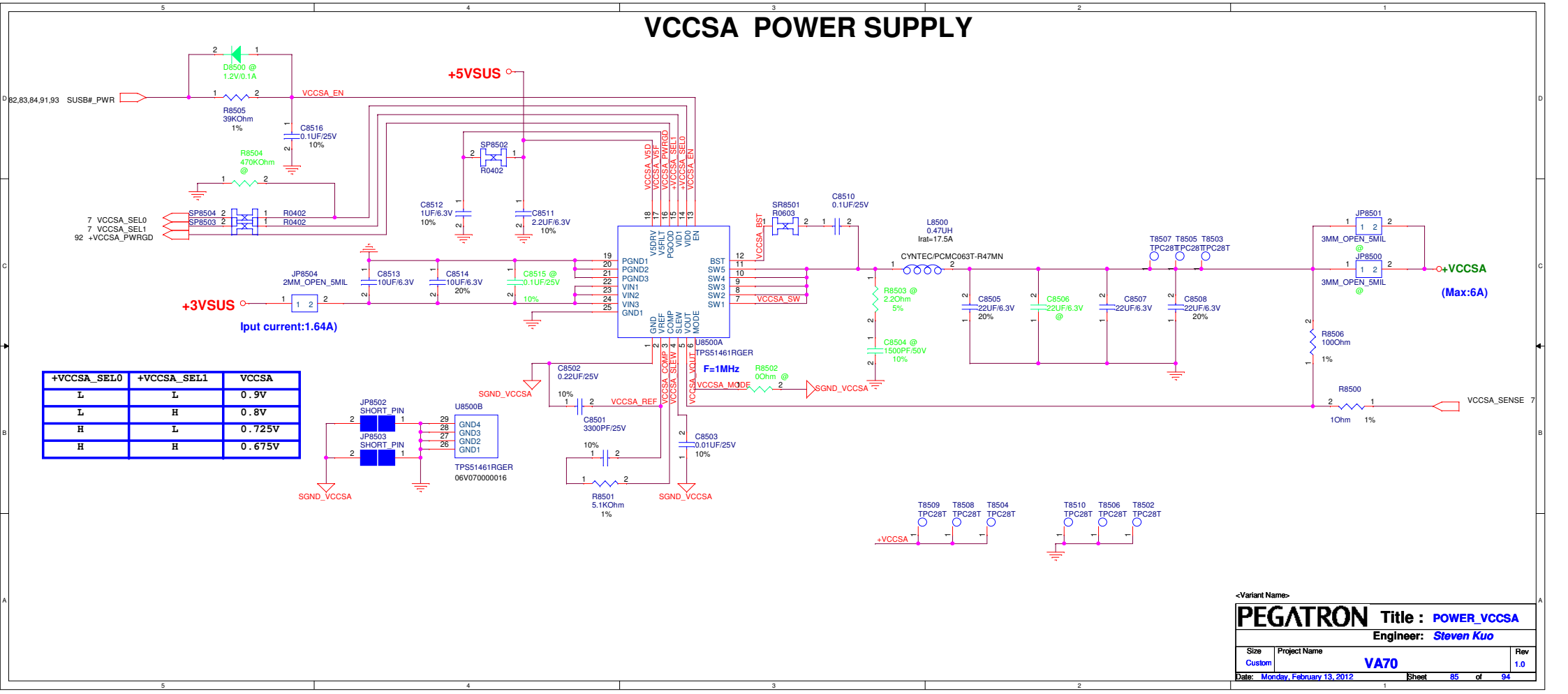
PEGATRON Title : POWER_1.8VS

Engineer: Steven Kuo

Size	Project Name	Rev
Custom	VA70	1.0

Date: Monday, February 13, 2012 Sheet 84 of 94

VCCSA POWER SUPPLY



+VCCSA_SEL0	+VCCSA_SEL1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

<Variant Name>

PEGATRON Title : POWER_VCCSA

Engineer: Steven Kuo

Size	Project Name	Rev
Custom	VA70	1.0

Date: Monday, February 13, 2012 Sheet 85 of 94

<Variant Name>

PEGATRON Title : POWER_

Engineer: Steven Kuo

Size	Project Name	Rev
Custom	VA70	1.0

Date: Monday, February 13, 2012 Sheet 86 of 94

VGA_CORE POWER SUPPLY

VID Set 0.9V

VGA_DPRSLPVR	VGA_PS#	VGA_VID
L	L	1 Phase CCM
H	L	1 Phase DE
L	H	2 Phase CCM
H	H	1 Phase DE

VID Set

OCP : 60A

EDP=50A

+VGA_VCORE_O +VGA_VCORE

AC_BAT_SYS

+3VS_VGA

+1.05VS

+5VS

+VGA_VCORE

U8700A ISL62882CHRTZ-T DSC_@

U8700B ISL62882CHRTZ-T DSC_@

R8703=(Period(us)-0.29)*2.65
Period(us)=1/300KHz

R8706 Setting OCP

<Variant Name>

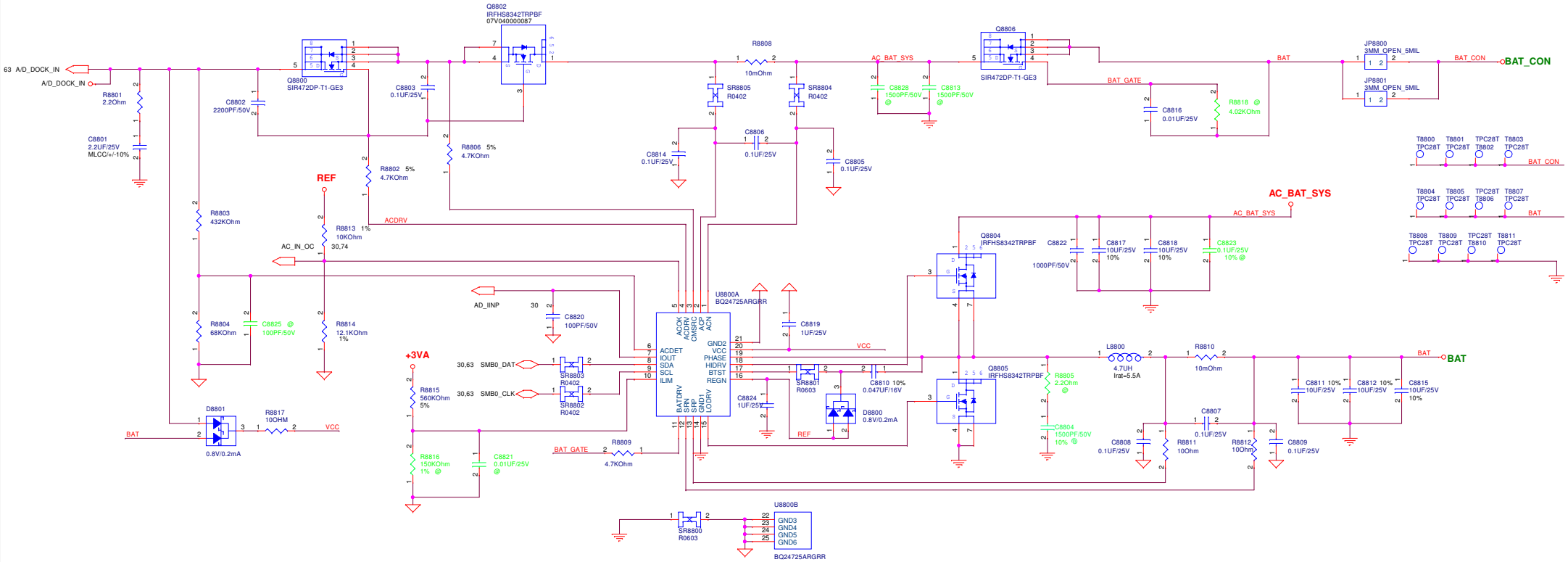
PEGATRON Title : POWER_VGACORE

Engineer: Steven Kuo

Size	Project Name	Rev
Custom	VA70	1.2

Date: Monday, February 13, 2012 Sheet 87 of 99

BATTERY CHARGER



<Variant Name>

PEGATRON Title : POWER_CHARGER

Engineer: Steven Kuo

Size	Project Name	Rev
Custom	VA70	1.0

Date: Monday, February 13, 2012 Sheet 88 of 15

<Variant Name>

PEGATRON Title : POWER_N/A

Engineer:

Size	Project Name	Rev
A		1.1

Date: Monday, February 13, 2012 Sheet 89 of 99

BATTERY IN DETECT

<Variant Name>

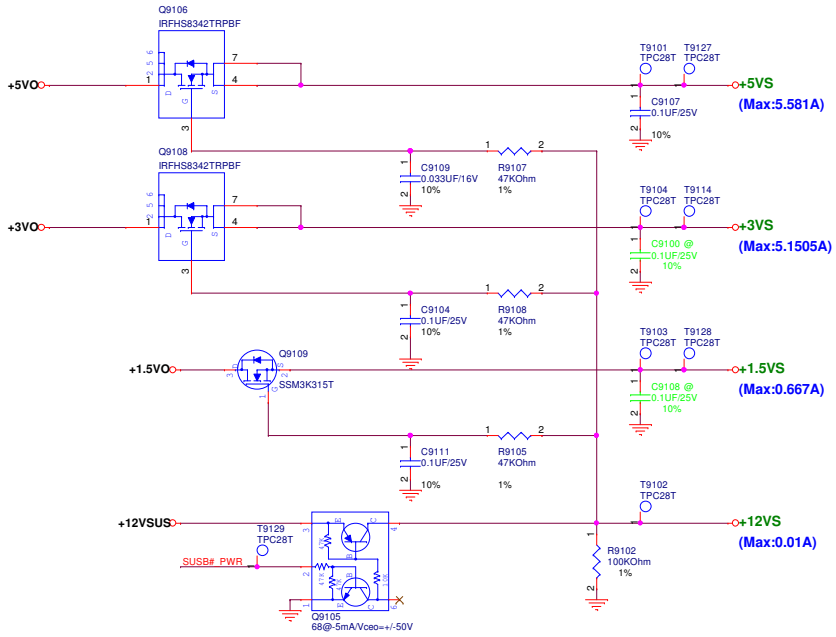
PEGATRON Title : POWER_DETECT

Engineer: Steven Kuo

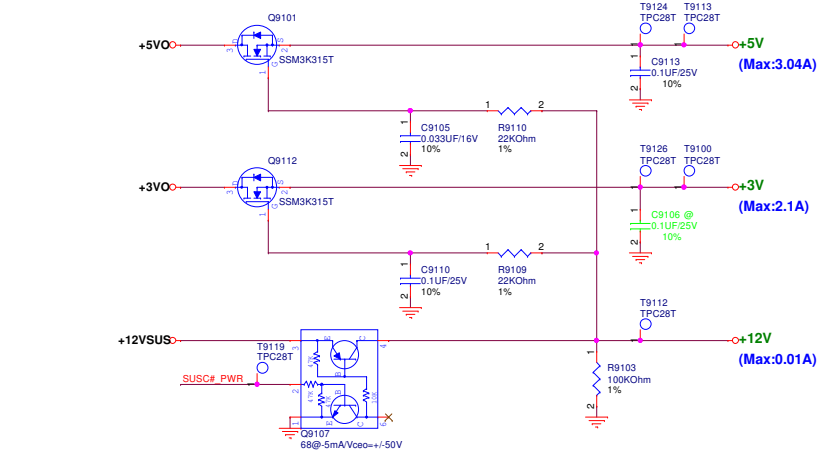
Size	Project Name	Rev
Custom	VA70	1.0

Date: Monday, February 13, 2012 Sheet 90 of 99

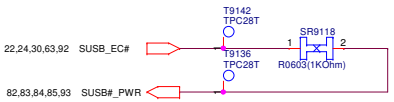
SUSB#_PWR POWER



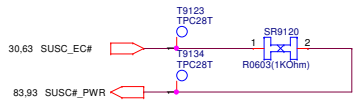
SUSC#_PWR POWER



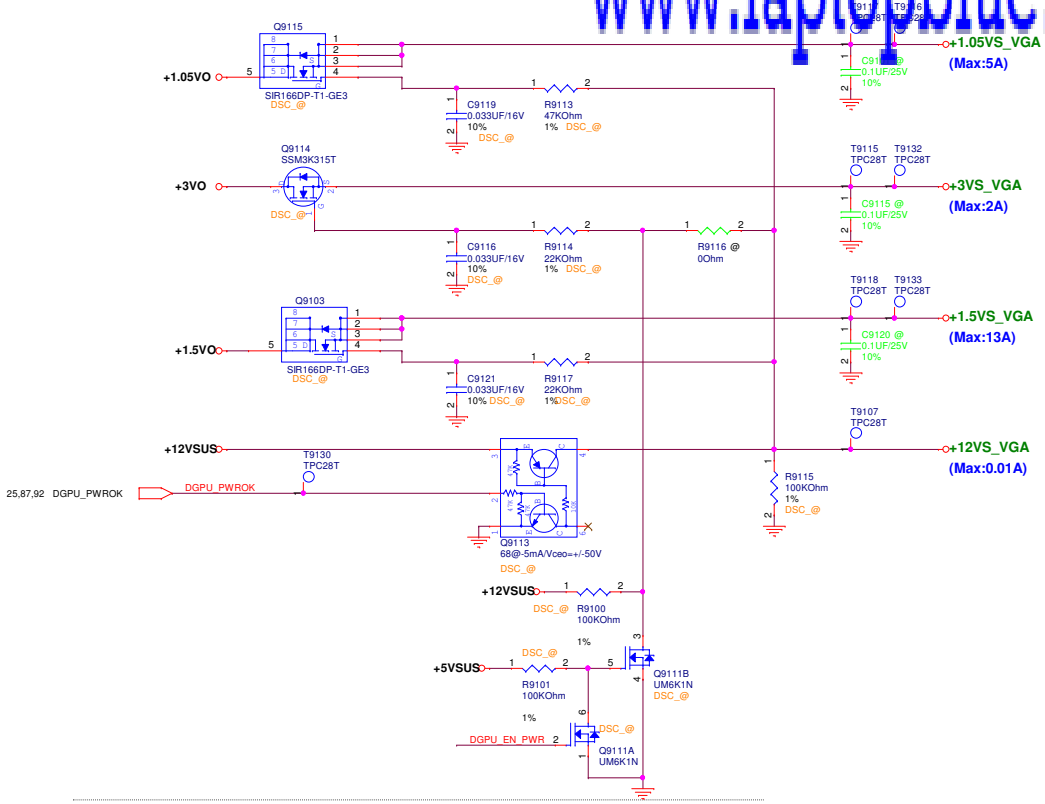
SUSB#_PWR POWER Control



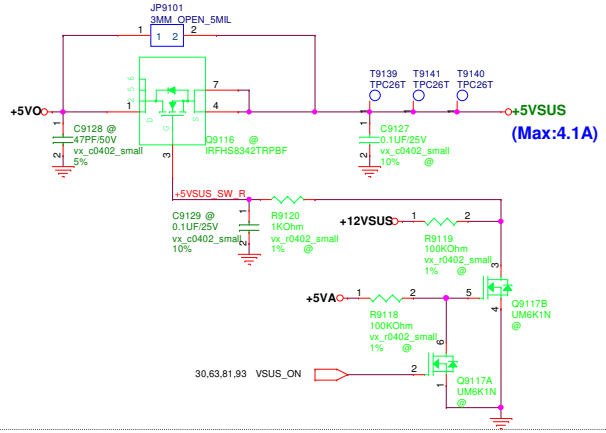
SUSB#_PWR POWER Control



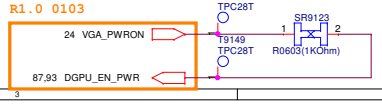
DSC#_PWR POWER (DGPU)



USBCHG#_PWR POWER



DSC_VGA_PWR POWER Control



<Variant Name>

PEGATRON Title : POWER_LOAD SWITCH

Engineer: Steven Kuo

Size	Project Name	Rev
Custom	VA70	1.0

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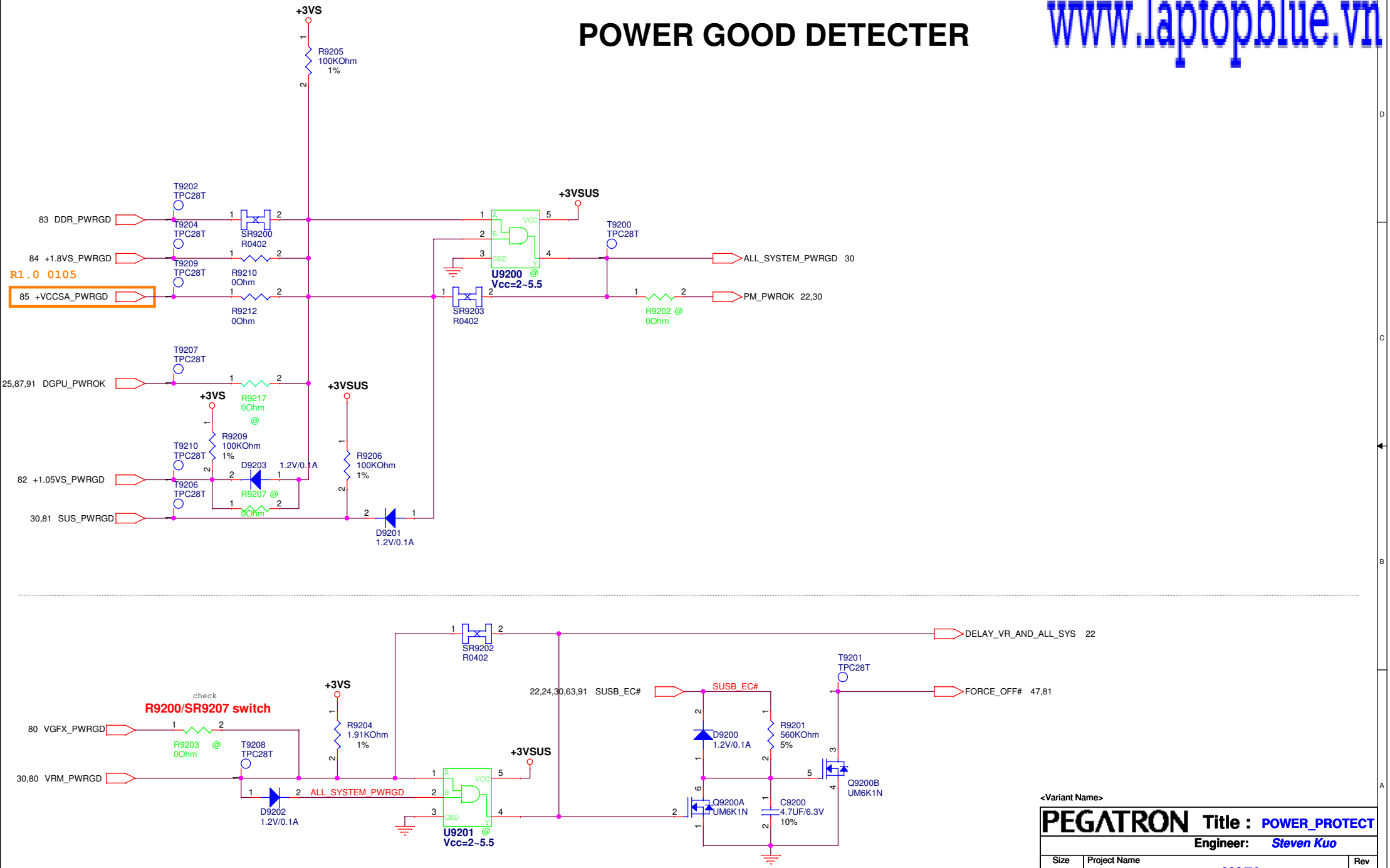
POWER GOOD DETECTER



<Variant Name>

PEGATRON Title : POWER_PROTECT

Engineer: Steven Kuo

Size	Project Name	Rev
Custom	VA70	1.0

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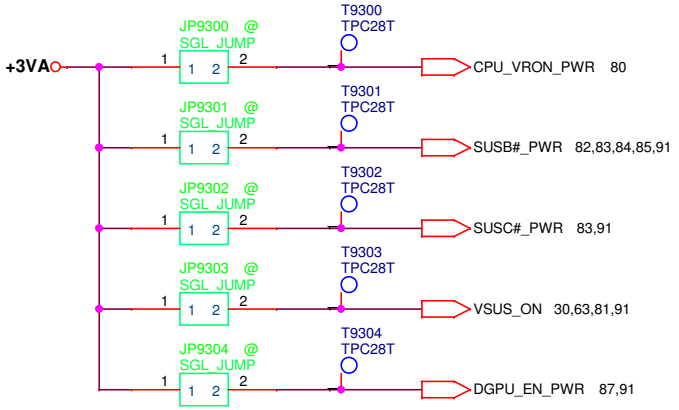
AC_BAT_SYS	AC_BAT_SYS	37,55,80,81,82,83,87,88
BAT_CON	BAT_CON	63,88
+5VA	+5VA	30,42,61,66,81,91
+3VA	+3VA	20,27,30,48,63,65,81,88
+5VO	+5VO	61,81,91
+3VO	+3VO	55,81,91
+1.8VO	+1.8VO	84
+1.5VO	+1.5VO	83,91
+1.05VO	+1.05VO	82,91
+12VSUS	+12VSUS	22,28,60,81,91
+5VSUS	+5VSUS	22,27,30,60,61,63,65,66,82,83,84,85,91
+3VSUS	+3VSUS	4,22,24,27,28,30,33,65,81,85,92
+12V	+12V	91
+5V	+5V	51,63,91
+3V	+3V	4,24,37,51,63,65,91
+1.5V	+1.5V	5,7,16,51,63,83
+12VS	+12VS	28,39,41,91
+5VS	+5VS	27,30,38,39,41,42,48,49,60,63,66,80,87,91
+3VS	+3VS	4,16,17,20,21,22,23,24,25,26,27,28,30,37,38,39,40,41,47,48,49,53,55,60,63,66,69,91,92
+1.8VS	+1.8VS	7,25,26,63,84
+1.5VS	+1.5VS	26,53,55,63,91
+1.05VS	+1.05VS	26,27,63,80,82,87
+0.75VS	+0.75VS	16,17,63,83
+VCCSA	+VCCSA	7,85
+VCCP	+VCCP	3,4,6,7,25,26,27,37,47,63,82
+12VS_VGA	+12VS_VGA	91
+3VS_VGA	+3VS_VGA	63,70,72,74,75,87,91
+1.5VS_VGA	+1.5VS_VGA	63,71,75,76,77,91
+1.05VS_VGA	+1.05VS_VGA	63,70,71,72,91
+VGA_VCORE	+VGA_VCORE	63,75,87
+VGFX_CORE	+VGFX_CORE	7,63,80
+VCORE	+VCORE	6,63,80



<Variant Name>

PEGATRON Title : POWER_SIGNAL

Engineer: Steven Kuo

Size	Project Name	Rev
Custom	A35	1.0

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