

# EA40-CX UMA/Muxless Schematics Document Ivy Bridge Intel PCH

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CSD

USE ONLY

*DY :None Installed*  
*DIS:DIS installed*  
*DIS\_Muxless :BOTH DIS or Muxless installed*  
*DIS\_PX:BOTH DIS or PX installed*  
*DIS\_PX\_Muxless:DIS or PX or Muxless installed.*  
*Muxless: Muxless installed.(PX4.0)*  
*PX:MUX installed.(PX3.0)*  
*PX\_Muxless:BOTH PX or Muxless installed.*  
*UMA:UMA installed*  
*UMA\_Muxless:BOTH UMA or Muxless installed*  
*UMA\_PX\_Muxless:UMA or PX or Muxless installed*

*ANNIE: ONLY FOR ANNIE solution.*  
*PSL: KBC795 PSL circuit for 10mW solution installed.*  
*10mW: External circuit for 10mW solution installed.*  
*65W: for 65W adaptor installed.*  
*90W: for 90W adaptor installed.*

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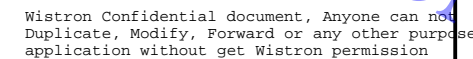
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**Revision : -3**



|                         |  |  |  |
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| Name   | Schematics Notes  |
|--|---|
| SPKR   | <b>Reboot option at power-up</b><br>Default Mode: Internal weak Pull-down.<br><b>No Reboot Mode with TCO Disabled:</b> Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.   |
| INIT3_3V#                                    | Weak internal pull-up. Leave as "No Connect".   |
| GNT3#/GPIO55<br>GNT2#/GPIO53<br>GNT1#/GPIO51 | GNT{3:0}# functionality is not available on Mobile.<br>Mobile: Used as GPIO only<br>Pull-up resistors are not required on these signals.<br>If pull-ups are used, they should be tied to the Vcc3_3power rail.  |
| SPI_MOSI                                     | <b>Enable Danbury:</b> Connect to Vcc3_3 with 8.2-k? weak pull-up resistor.<br><b>Disable Danbury:</b> left floating, no pull-down required.  |
| NV_ALE                                       | <b>Enable Danbury:</b> Connect to +NVRAM_VCCO with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor]<br><b>Disable Danbury:</b> leave floating (internal pull-down)   |
| NC_CLE                                       | DMI termination voltage. Weak internal pull-up. Do not pull low.  |
| HAD_DOCK_EN# /GPIO[33]                       | Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features.<br>High (1) - Security measure defined in the Flash Descriptor will be enabled.<br>Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently.<br>Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions. |
| HDA_SDO                                      | Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.   |
| HDA_SYNC                                     | Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.   |
| GPIO15                                       | Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality<br>Note : This is an un-muxed signal.<br>This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low.<br>Sampled at rising edge of RSMRST#.<br>CRB has a 1-kohm pull-up on this signal to +3.3VA rail.  |
| GPIO8  | GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.   |
| GPIO27                                       | <b>Default = Do not connect (floating)</b><br>High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit.<br>Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.   |

## USB Table

## PCIE Routing

|       |                  |
|-------|------------------|
| LANE1 | Mini Card2(WWAN) |
| LANE2 | Mini Card1(WLAN) |
| LANE3 | Card Reader      |
| LANE4 | Onboard LAN      |
| LANE5 | USB3.0           |
| LANE6 | Intel GBE LAN    |
| LANE7 | Dock             |
| LANE8 | New Card         |

## SATA Table

| SATA |        |
|------|--------|
| Pair | Device |
| 0    | HDD1   |
| 1    | N/A    |
| 2    | N/A    |
| 3    | N/A    |
| 4    | ODD    |
| 5    | ESATA  |

| Pair | Device                                |
|------|---------------------------------------|
| 0    | Touch Panel / 3G SIM                  |
| 1    | USB Ext. port 1 (HS)                  |
| 2    | Fingerprint                           |
| 3    | BLUETOOTH                             |
| 4    | Mini Card2 (WWAN)                     |
| 5    | CARD READER                           |
| 6    | X                                     |
| 7    | X                                     |
| 8    | USB Ext. port 4 / E-SATA /USB CHARGER |
| 9    | USB Ext. port 2                       |
| 10   | EDP CAMERA                            |
| 11   | Mini Card1 (WLAN)                     |
| 12   | CAMERA                                |
| 13   | New Card                              |

| Pin Name | Strap Description                   | Configuration (Default value for each bit is 1 unless specified otherwise)   | Default |
|----------|-------------------------------------|--|---------|
| CFG[2]   | PCI-Express Static Lane Reversal    | 1: Normal Operation.<br>0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...   |         |
| CFG[4]   |                                     | Disabled - No Physical Display Port attached to<br>1: Embedded DisplayPort.<br>Enabled - An external Display Port device is connectd to the EMBEDDED display Port<br>0:  | 0       |
| CFG[6:5] | PCI-Express Port Bifurcation Straps | 11 : x16 - Device 1 functions 1 and 2 disabled<br>10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled<br>01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled)<br>00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled | 11      |
| CFG[7]   | PEG DEFER TRAINING                  | 1: PEG Train immediately following xxRESETB de assertion<br>0: PEG Wait for BIOS for training  |         |

| POWER PLANE   | VOLTAGE   | Voltage Rails |  | DESCRIPTION                                    |
|---|---|---------------|--|--|
|   |   | ACTIVE IN     |  |  |
| 5V_S0<br>3D3V_S0<br>1D8V_S0<br>1D5V_S0<br>1D05V_VTT<br>0D85V_S0<br>0D75V_S0<br>VCC_CORE<br>VCC_SFPCORE<br>1D8V_VGA_S0<br>3D3V_VGA_S0<br>1V_VGA_S0 | 5V<br>3.3V<br>1.8V<br>1.5V<br>1.05V<br>0.95 - 0.85V<br>0.75V<br>0.35V to 1.5V<br>0.4 to 1.25V<br>1.8V<br>3.3V<br>1V | S0            |  | CPU Core Rail<br>Graphics Core Rail            |
| 5V_USBX_S3<br>1D5V_S3<br>DDR_VREF_S3  | 5V<br>1.5V<br>0.75V   | S3            |  |  |
| BT+<br>DCBATOUT<br>5V_S5<br>5V_AUX_S5<br>3D3V_S5<br>3D3V_AUX_S5   | 6V-14.1V<br>6V-14.1V<br>5V<br>5V<br>3.3V<br>3.3V  | All S states  |  | AC Brick Mode only                             |
| 3D3V_LAN_S5   | 3.3V  | WOL_EN        |  | Legacy WOL                                     |
| 3D3V_AUX_KBC  | 3.3V  | DSW, Sx       |  | ON for supporting Deep Sleep states            |
| 3D3V_AUX_S5   | 3.3V  | G3, Sx        |  | Powered by Li Coin Cell in G3 and +V3AUX in Sx |

## SMBus ADDRESSES

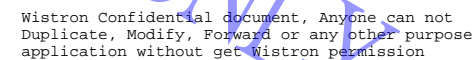
| I <sup>2</sup> C / SMBus Addresses   |  | Ref Des | HURON RIVER ORB |  |
|--|--|---------|-----------------|--|
| Device   |  |         | Address         | Hex Bus  |
| EC SMBus 1<br>Battery CHARGER  |  |         |                 | BAT_SCL/BAT_SDA<br>BAT_SCL/BAT_SDA<br>BAT_SCL/BAT_SDA  |
| EC SMBus 2<br>PCH eDP  |  |         |                 | SML1_CLK/SML1_DATA<br>SML1_CLK/SML1_DATA<br>SML1_CLK/SML1_DATA   |
| PCH SMBus<br>SO-DIMMA (SPD)<br>SO-DIMMB (SPD)<br>Digital Pot<br>G-Sensor<br>MINI |  |         |                 | PCH_SMBDATA/PCH_SMBCLK<br>PCH_SMBDATA/PCH_SMBCLK<br>PCH_SMBDATA/PCH_SMBCLK<br>PCH_SMBDATA/PCH_SMBCLK<br>PCH_SMBDATA/PCH_SMBCLK<br>PCH_SMBDATA/PCH_SMBCLK |

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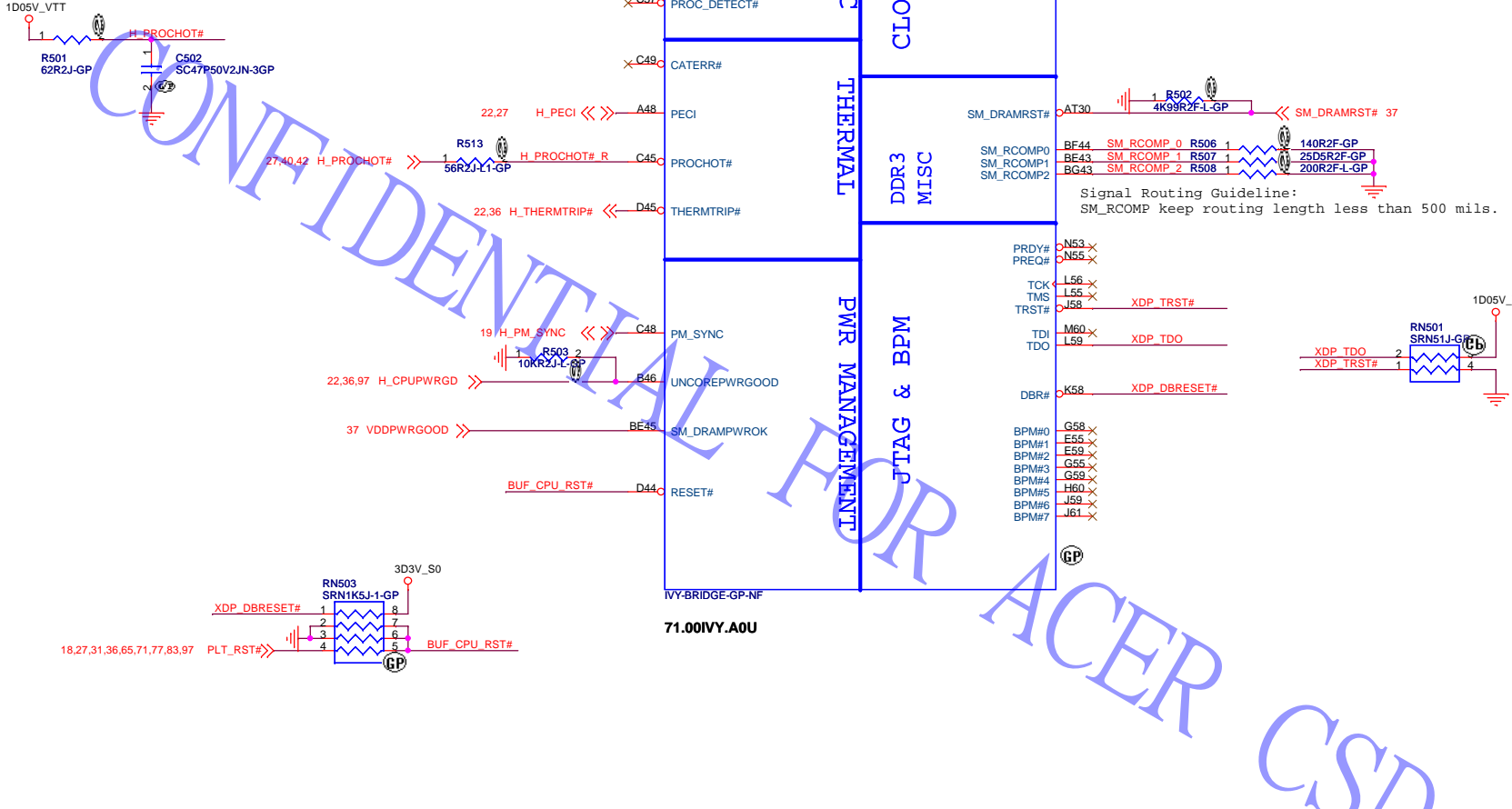
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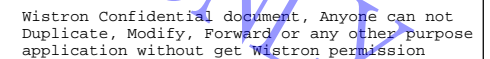
SSID = CPU

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| Title CPU (THERMAL/CLOCK/PM)  |                         |        |
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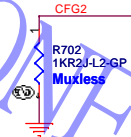




# SSID = CPU

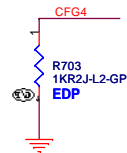
## PEG Static Lane Reversal

CFG2 1: Normal Operation; Lane # definition matches socket pin map definition  
0: Lane Reversed



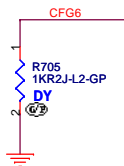
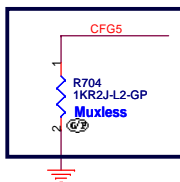
## Enabl EDP function

CFG4 1: Disable  
0: Enable



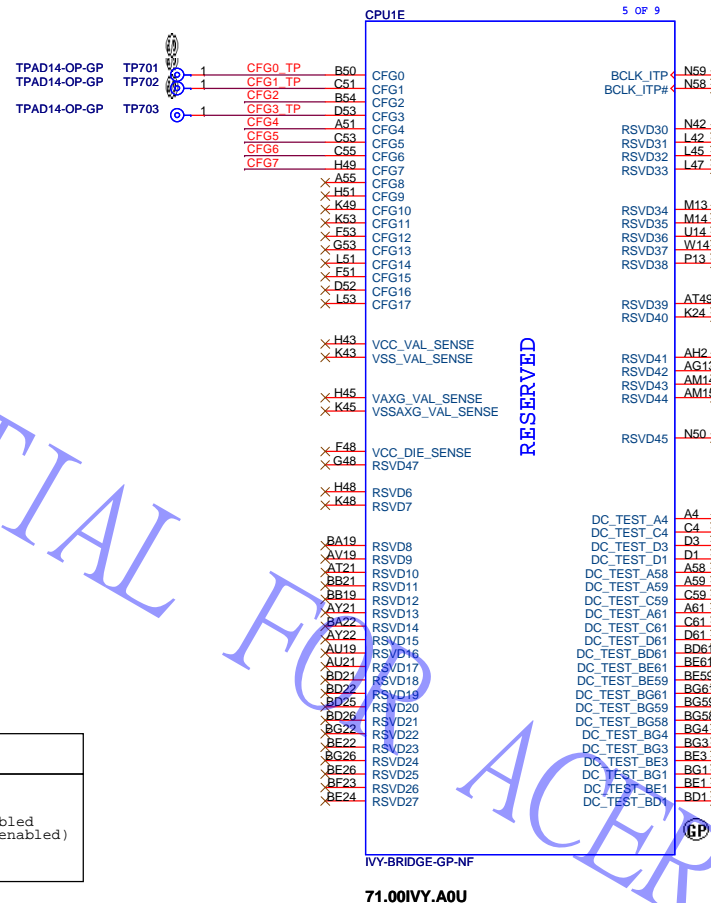
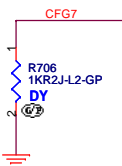
## PCIe Port Bifurcation Straps

CFG[6:5] 11: x16 - Device 1 functions 1 and 2 disabled  
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled  
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)  
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



## PEG DEFER TRAINING

CFG7 1: PEG Train immediately following xxRESETB de assertion  
0: PEG Wait for BIOS for training



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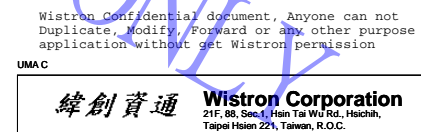
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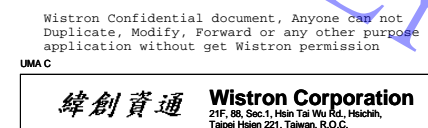
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|-------|-------------------------|---------|----------------|--------|
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| <b>CPU (VCC CORE)</b> |                       |            |     |
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CPU1I 9 OF 9

A13 VSS1 AM38  
A17 VSS2 AM4  
A21 VSS3 AM42  
A25 VSS4 AM45  
A28 VSS5 AM48  
A33 VSS6 AM58  
A37 VSS7 AN1  
A40 VSS8 AN21  
A45 VSS9 AN25  
A49 VSS9 AN28  
A53 VSS10 AN33  
VSS11 VSS101 AN36  
A9 VSS12 VSS102 AN40  
AA1 VSS13 VSS104 AN43  
AA13 VSS14 VSS105 AN47  
AA50 VSS15 VSS106 AN54  
AA51 VSS16 VSS107 AP10  
AA52 VSS16 VSS108 AP51  
AA53 VSS17 VSS109 AP55  
AA55 VSS18 VSS110 AP7  
AA56 VSS20 VSS111 AR13  
AA8 VSS21 VSS112 AR17  
AB16 VSS22 VSS113 AR21  
AB18 VSS23 VSS114 AR41  
AB48 VSS25 VSS115 AR48  
AB61 VSS26 VSS116 AR61  
AC040 VSS27 VSS117 AR7  
AC14 VSS28 VSS118 AT14  
AC48 VSS28 VSS119 AT19  
AC6 VSS29 VSS120 AT36  
AD17 VSS30 VSS121 AT4  
AD20 VSS32 VSS122 AT45  
AD4 VSS33 VSS123 AT52  
AD61 VSS34 VSS124 AT58  
AE13 VSS35 VSS125 AU1  
AEB VSS35 VSS126 AU11  
AF1 VSS36 VSS127 AU28  
AF17 VSS38 VSS128 AU32  
AF21 VSS39 VSS129 AU51  
AF47 VSS40 VSS130 AU7  
AF48 VSS41 VSS131 AV17  
AF50 VSS42 VSS132 AV21  
AF51 VSS43 VSS133 AV22  
AF52 VSS44 VSS134 AV34  
AF53 VSS45 VSS135 AV40  
AF56 VSS46 VSS136 AV48  
AF58 VSS47 VSS137 AV55  
AF59 VSS48 VSS138 AW13  
AG10 VSS49 VSS139 AW43  
AG14 VSS50 VSS140 AW61  
VSS51 VSS141 AW7  
AG18 VSS52 VSS142 AY14  
AG47 VSS53 VSS143 AY19  
AG52 VSS54 VSS144 AY30  
AG61 VSS55 VSS145 AY36  
AG7 VSS56 VSS146 AY4  
AH4 VSS57 VSS147 AY41  
AH58 VSS58 VSS148 AY45  
AJ13 VSS59 VSS149 AY49  
AJ16 VSS60 VSS150 AY55  
AJ20 VSS61 VSS151 AY58  
AJ22 VSS62 VSS152 AY9  
AJ26 VSS63 VSS153 BA1  
AJ30 VSS64 VSS154 BA11  
AJ34 VSS65 VSS155 BA17  
AJ38 VSS66 VSS156 BA21  
AJ42 VSS67 VSS157 BA26  
AJ45 VSS68 VSS158 BA32  
AJ48 VSS69 VSS159 BA48  
AJ7 VSS70 VSS160 BA51  
AK1 VSS71 VSS161 BB53  
AK52 VSS72 VSS162 BC13  
AL10 VSS73 VSS163 BC5  
AL13 VSS74 VSS164 BC57  
AL17 VSS75 VSS165 BD12  
AL21 VSS76 VSS166 BD16  
AL25 VSS77 VSS167 BD19  
AL28 VSS78 VSS168 BD23  
AL33 VSS79 VSS169 BD27  
AL36 VSS80 VSS170 BD32  
AL40 VSS81 VSS171 BD36  
AL43 VSS82 VSS172 BD40  
AL47 VSS83 VSS173 BD44  
AL61 VSS84 VSS174 BD48  
AM13 VSS85 VSS175 BD52  
AM20 VSS86 VSS176 BD56  
AM22 VSS87 VSS177 BD8  
AM26 VSS88 VSS178 BE5  
AM30 VSS89 VSS179 BG13  
AM34 VSS90 VSS180

VSS

BG17 VSS181 M4  
BG21 VSS182 M58  
BG24 VSS183 M6  
BG28 VSS184 N1  
BG37 VSS185 N17  
BG41 VSS186 N21  
BG45 VSS187 N25  
BG49 VSS188 N28  
BG53 VSS189 N33  
BG9 VSS190 N36  
C29 VSS191 N40  
C35 VSS192 N43  
C40 VSS193 N47  
D10 VSS194 N48  
D14 VSS195 N51  
D18 VSS196 N52  
D22 VSS197 N56  
D26 VSS198 N61  
D29 VSS199 N64  
D35 VSS200 N68  
D4 DSS201 N69  
D40 VSS202 P14  
D43 VSS203 P16  
D46 VSS204 P18  
D50 VSS205 P21  
D54 VSS206 P58  
D58 VSS207 P59  
D6 VSS208 P9  
E25 VSS209 R17  
E29 VSS210 R20  
E3 VSS211 R4  
E35 VSS212 R46  
E40 VSS213 T1  
F13 VSS214 T47  
F15 VSS215 T50  
F19 VSS216 T51  
F29 VSS217 T52  
F35 VSS218 T53  
F40 VSS219 T55  
F44 VSS220 T56  
G51 VSS221 U13  
G6 VSS222 U8  
G61 VSS223 V20  
H10 VSS224 V61  
H14 VSS225 W13  
H17 VSS226 W15  
H21 VSS227 W18  
H4 VSS228 W21  
H53 VSS229 W46  
H58 VSS230 W8  
J1 VSS231 Y4  
J49 VSS232 Y47  
K51 VSS233 Y58  
K8 VSS234 Y59  
L16 VSS235  
L20 VSS236  
L22 VSS237  
L26 VSS238  
L30 VSS239  
L34 VSS240  
L38 VSS241  
L43 VSS242  
L48 VSS243  
L61 VSS244  
M11 VSS247  
M15 VSS248

VSS

NCTF

NCTF TEST PIN :  
A5, A57, EC61, BG5  
BG57, C3, E1, E61  
VSS\_NCTF\_1#A5  
VSS\_NCTF\_2#A57  
VSS\_NCTF\_3#BC61  
VSS\_NCTF\_8#BG5  
VSS\_NCTF\_9#BG57  
VSS\_NCTF\_10#C3  
VSS\_NCTF\_13#E1  
VSS\_NCTF\_14#E61

A5  
A57  
BC61  
BG5  
BG57  
C3  
E1  
E61

BD3  
BD59  
BE4  
BE58  
C58  
D59

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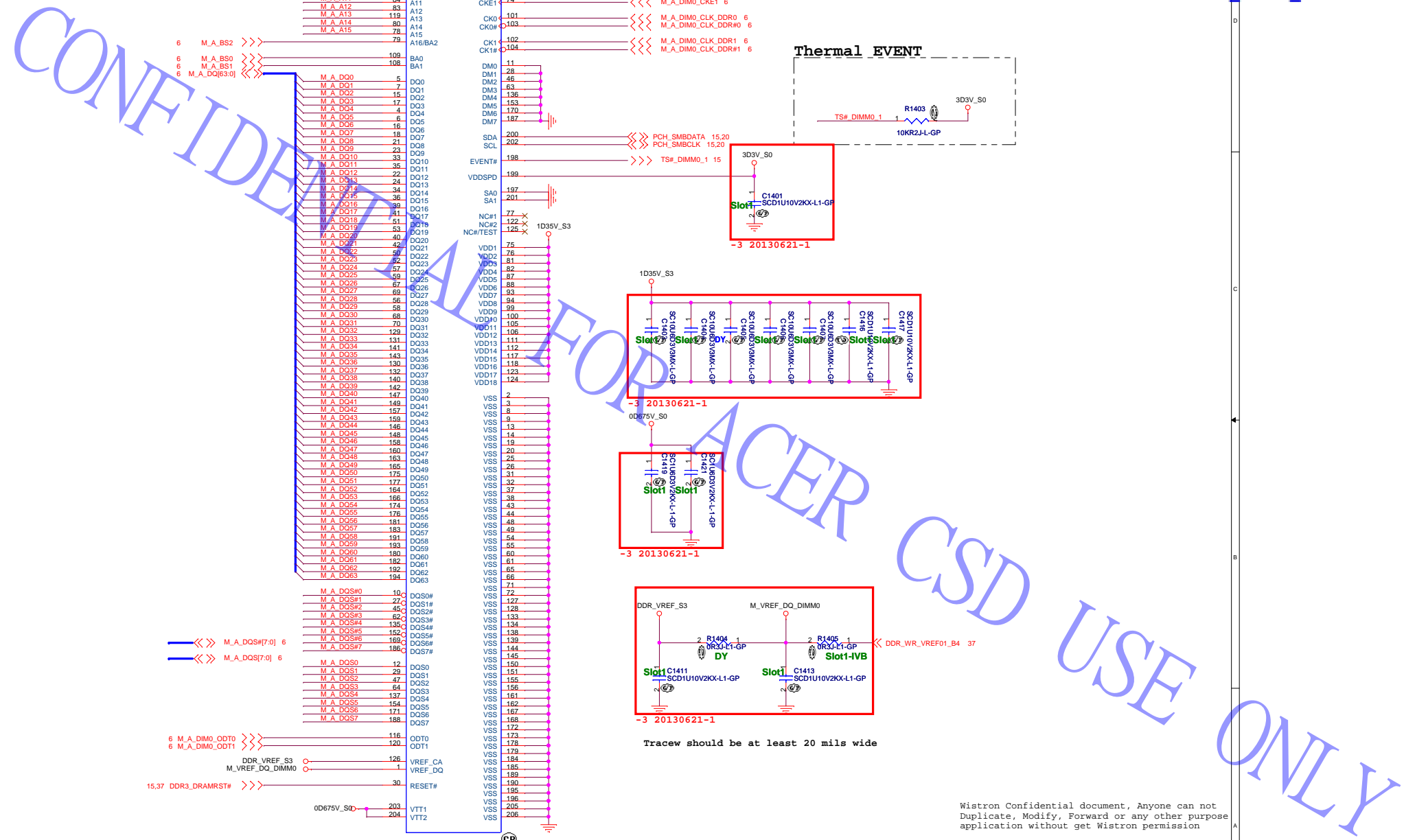
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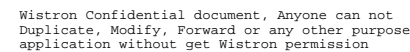
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| Size <div>A4</div>   | Document Number <div>EA40 CX</div> | Rev <div>-3</div> |
| Date: Thursday, June 06, 2013  |                                    | Sheet 13 of 103   |



|                |                       |  |           |
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| Title          |                       |  |           |
| DDR3-SODIMM1   |                       |  |           |
| Size<br>Custom | Document Number       | Rev<br>-1  |           |
| EA40 CX        |                       |  |           |
| Date:          | Friday, June 21, 2013 | Sheet  | 14 of 103 |





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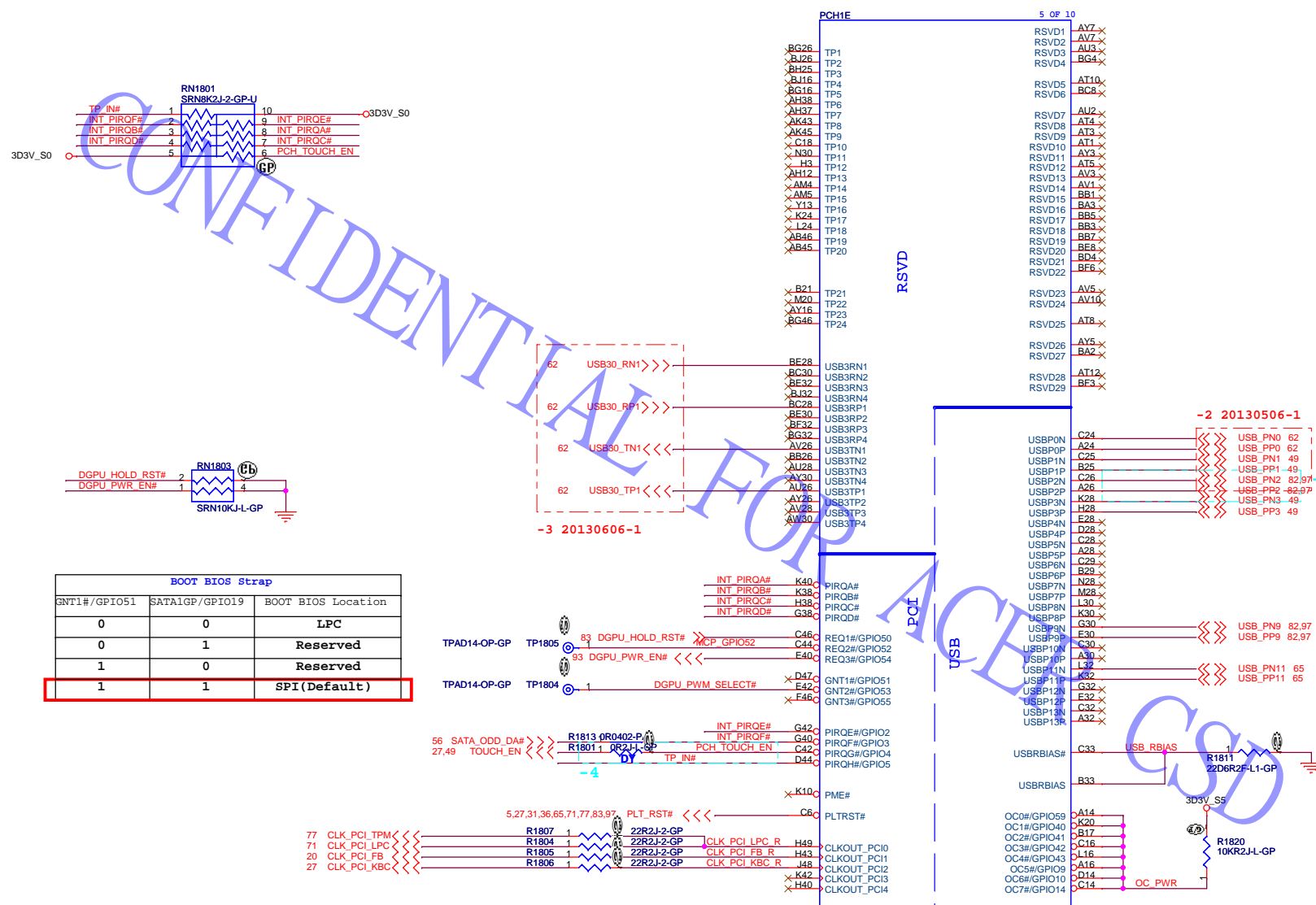
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| Title <div>DDR3-SODIMM2</div>  |                                    |                   |
| Size <div>A4</div>   | Document Number <div>EA40 CX</div> | Rev <div>-3</div> |
| Date: Thursday, June 06, 2013  |                                    | Sheet 16 of 103   |



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Taipei Hsien 221, Taiwan, R.O.C.

|                           |                         |  |                 |
|---------------------------|-------------------------|--|-----------------|
| Title                     |                         |  |                 |
| <b>PCH (LVDS/CRT/DDI)</b> |                         |  |                 |
| Size<br>A3                | Document Number         |  | Rev             |
|                           | <b>EA40 CX</b>          |  | <b>-3</b>       |
| Date:                     | Thursday, June 20, 2013 |  | Sheet 17 of 103 |



| BOOT BIOS Strap |                |                    |
|-----------------|----------------|--------------------|
| GNT1#/GPIO51    | SATA1GP/GPIO19 | BOOT BIOS Location |
| 0               | 0              | LPC                |
| 0               | 1              | Reserved           |
| 1               | 0              | Reserved           |
| 1               | 1              | SPI(Default)       |

USB Table

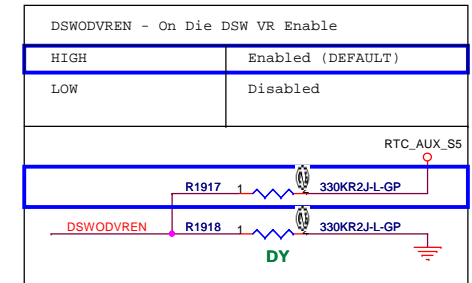
| Pair | Device                    |
|------|---------------------------|
| 0    | USB2.0/USB3.0 Ext. port 1 |
| 1    | Touch panel -3 20130606-1 |
| 2    | USB2.0 Ext. port 1        |
| 3    | CCD                       |
| 4    |                           |
| 5    |                           |
| 6    | may not be available      |
| 7    | may not be available      |
| 8    |                           |
| 9    | USB2.0 Ext. port 3        |
| 10   |                           |
| 11   | Mini Card1 (WLAN+BT)      |
| 12   |                           |
| 13   |                           |

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| Title  |                       |
| PCH (PCI/USB/NVRAM)  |                       |
| Size   | Document Number       |
| Custom   | EA40 CX               |
| Date   | Friday, June 21, 2013 |
| Sheet  | 18 of 103             |
| Rev  | -3                    |

4 DMI\_RXN[3:0]       
4 DMI\_RXP[3:0]       
  
4 DMI\_TXN[3:0]       
4 DMI\_TXP[3:0]     

FDI\_TXN[7:0] 4  
FDI\_TXP[7:0] 4



3D3V\_S5

R1901  
SRN10KJ-6-GP

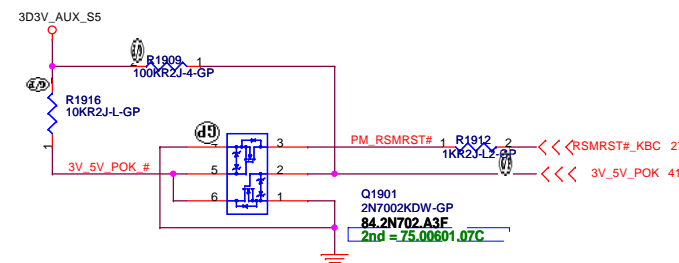
8 1  
7 2  
6 3  
5 4

BATLOW#  
PM R#  
AC PRESENT  
SUS\_PWR\_ACK\_R

PCIE\_WAKE#

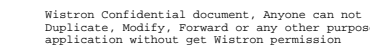
SUS\_PWR\_ACK#

PM RSMRST#



|                          |                       |             |           |
|--------------------------|-----------------------|-------------|-----------|
| Title                    |                       |             |           |
| <b>PCH (DM I/FDI/PM)</b> |                       |             |           |
| Size<br>A3               | Document Number       |             | Rev       |
|                          | <b>EA40 CX</b>        |             | <b>-3</b> |
| Date:                    | Friday, June 21, 2013 | Sheet 19 of | 103       |

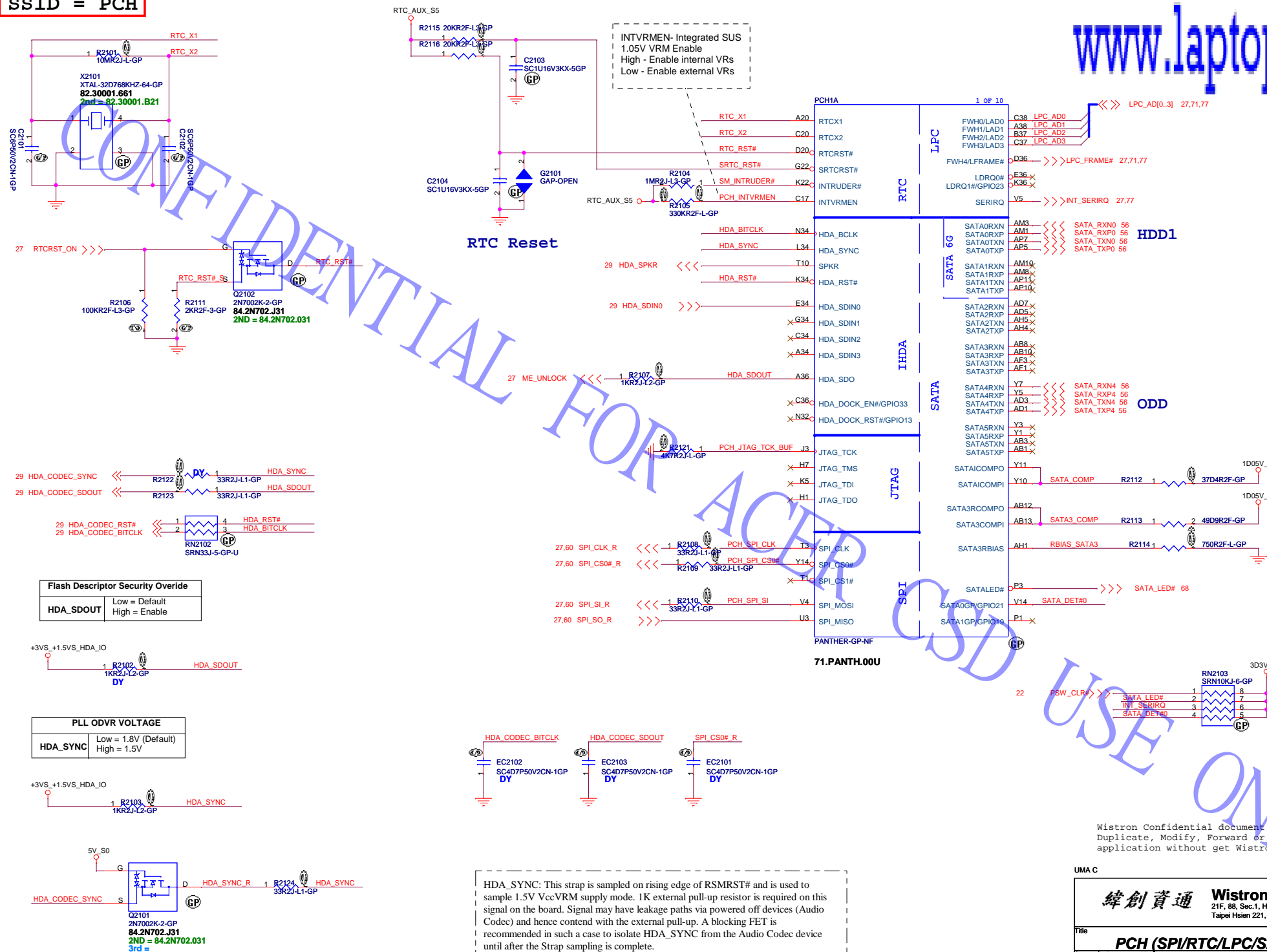
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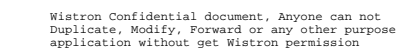


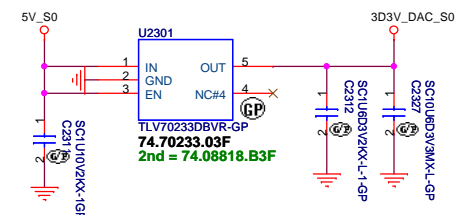
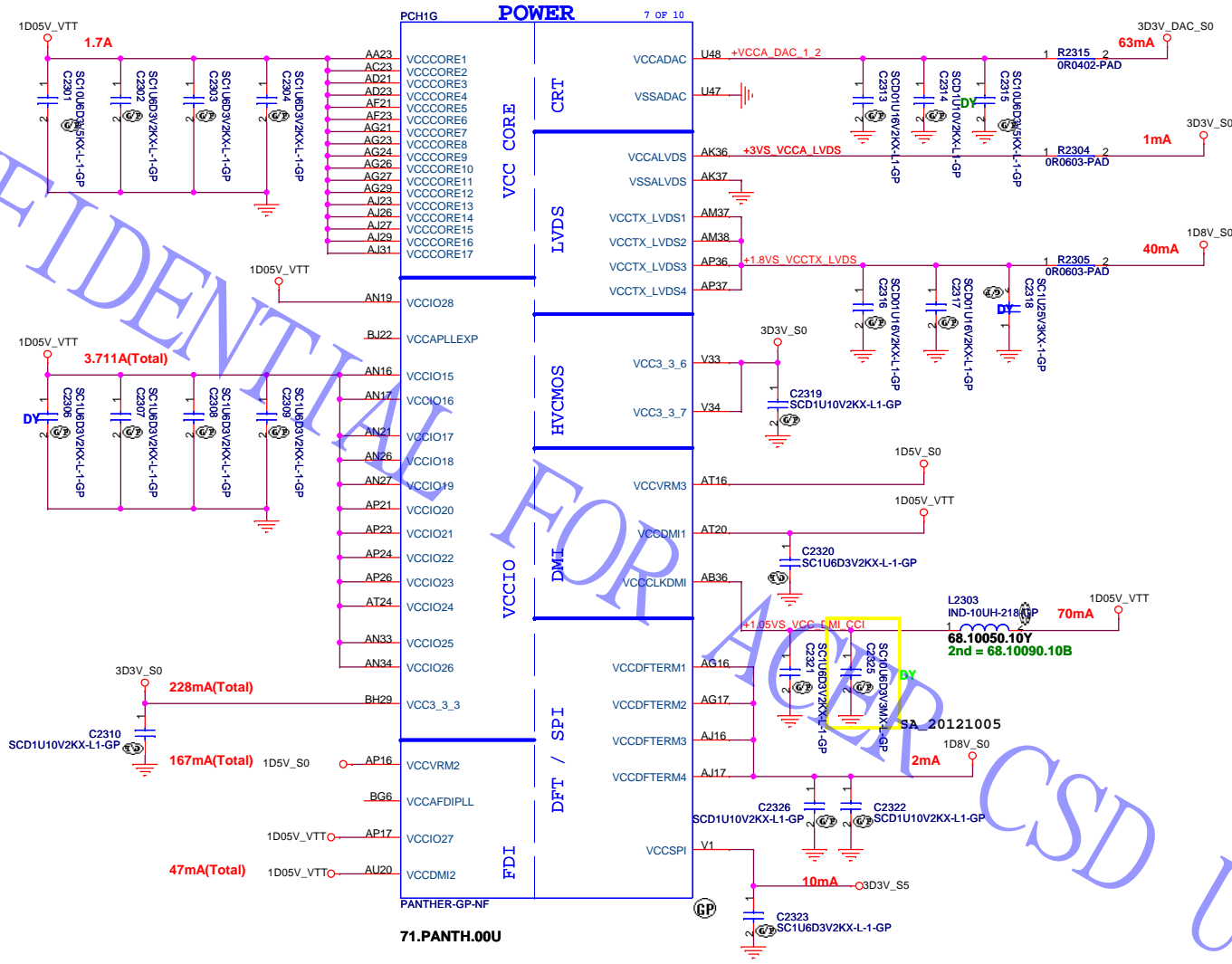


SSID = PCH

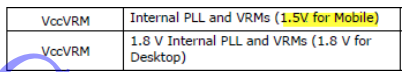
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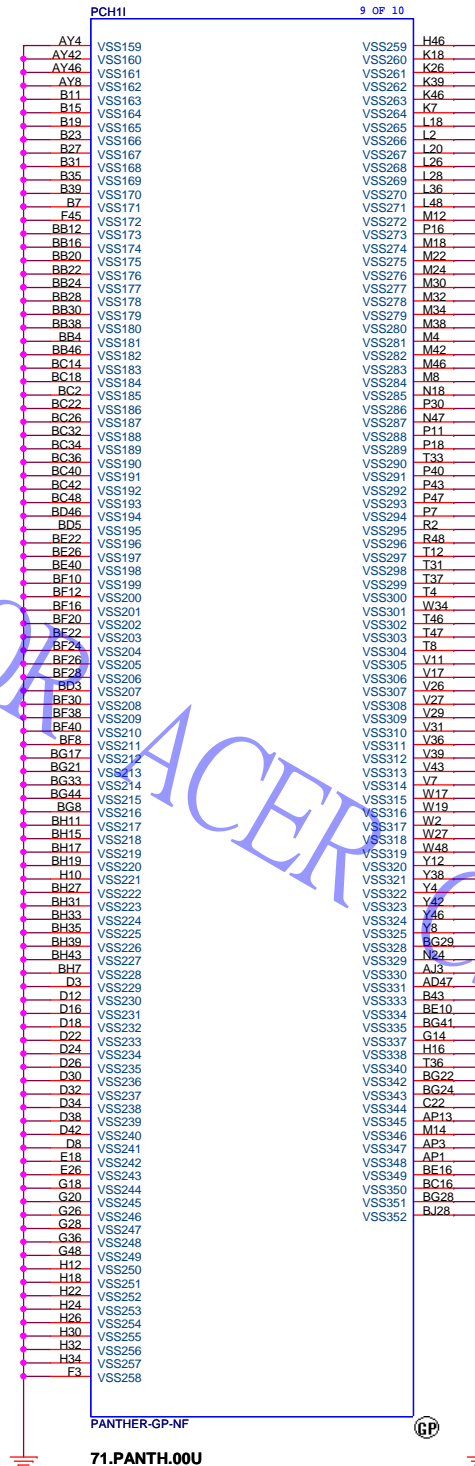
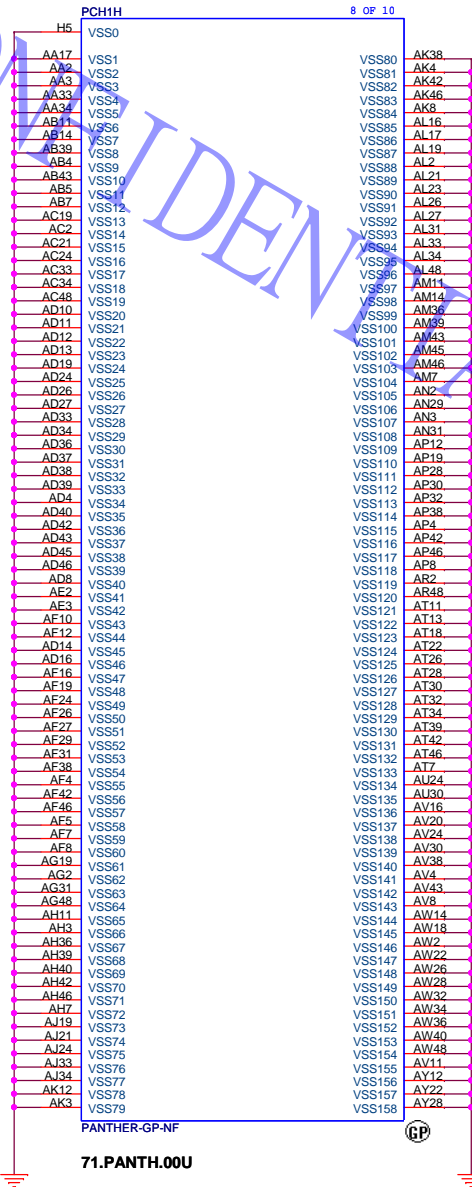
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| Title          |                       | <b>PCH (POWER2)</b><br>_____<br>_____<br>_____  |                  |
| Size<br>Custom | Document Number       | <b>EA40 CX</b><br>_____<br>_____<br>_____   | Rev<br><b>-3</b> |
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SSID = PCH

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| Title PCH (VSS)  |                         |
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| Date: Thursday, June 06, 2013  | Rev -3                  |
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| Title <div>Clock(colay)</div>  |                                    |                   |
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| Date: Thursday, June 06, 2013  |                                    | Sheet 26 of 103   |





SSID = Thermal

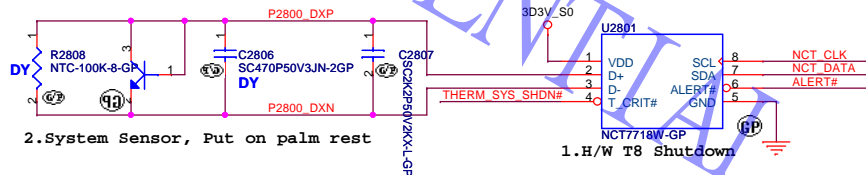
## Thermal sensor NCT 7718W

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\*Layout\* 15 mil

Layout notice :  
Both DXN and DXB routing 10 mil  
trace width and 10 mil spacing.

Q2801  
PMB3904-1-GP  
84.03904.L06

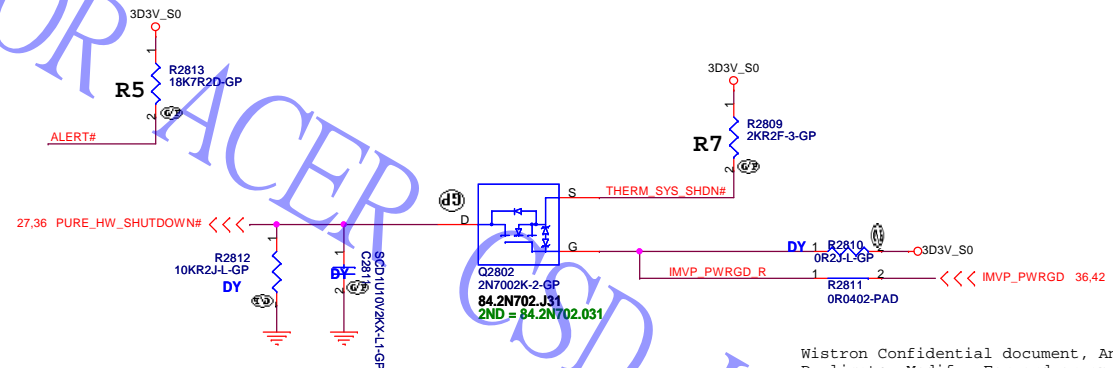


ALERT# /T CRIT#  
Pull-up Resistor

| R5   | 2Kohm | 7.5Kohm | 10.5Kohm | 14Kohm | 18.7Kohm |
|------|-------|---------|----------|--------|----------|
| 77°C | 87°C  | 97°C    | 107°C    | 117°C  |          |
| 79°C | 89°C  | 99°C    | 109°C    | 119°C  |          |
| 81°C | 91°C  | 101°C   | 111°C    | 121°C  |          |
| 83°C | 93°C  | 103°C   | 113°C    | 123°C  |          |
| 85°C | 95°C  | 105°C   | 115°C    | 125°C  |          |

T\_CRIT temperature strapping point

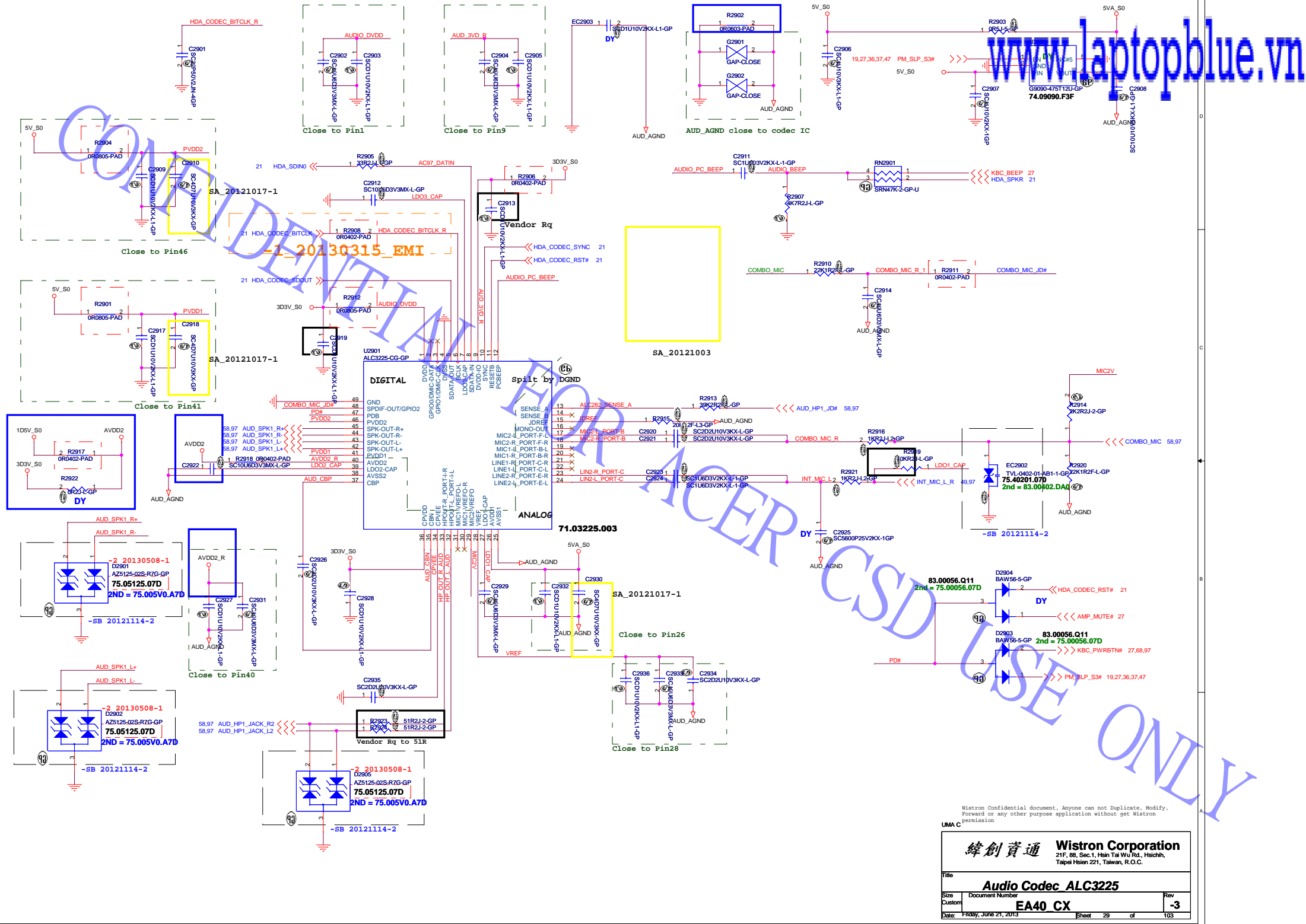
SB T8=85 degree



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| Title<br><b>Thermal NCT7718</b>   |                                   |                     |          |
| Size<br>Custom  | Document Number<br><b>EA40 CX</b> | Rev<br><b>-3</b>    |          |
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| Audio AMP |                         |  |                 |
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| A3        | EA40_CX                 |  | -3              |
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|-----------------------|-------------------------|
| Title                 |                         |
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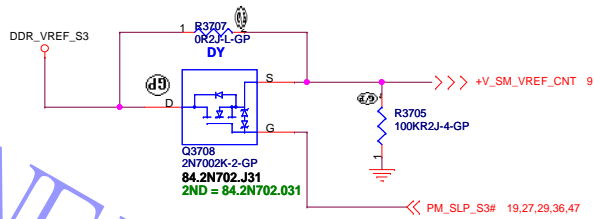
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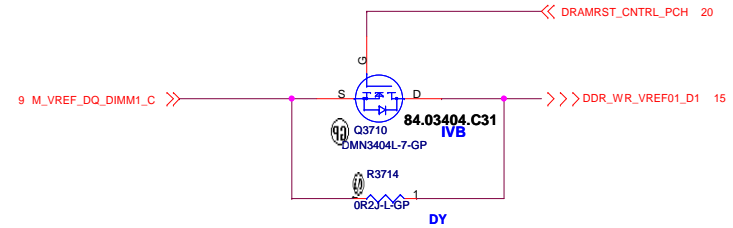
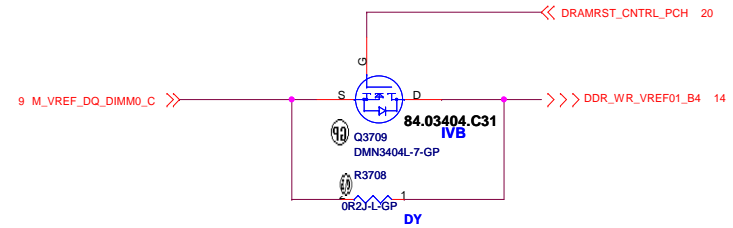
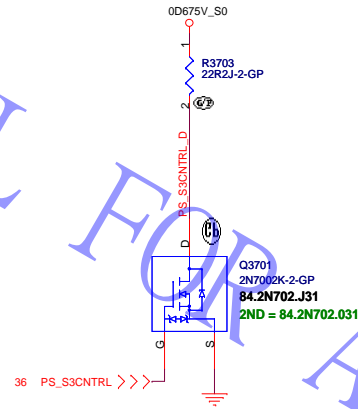
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| Title  |                         |                 |
| USB 3.0 Controller   |                         |                 |
| Size   | Document Number         | Rev             |
| Custom   | EA40 CX                 | -3              |
| Date:  | Thursday, June 06, 2013 | Sheet 35 of 103 |



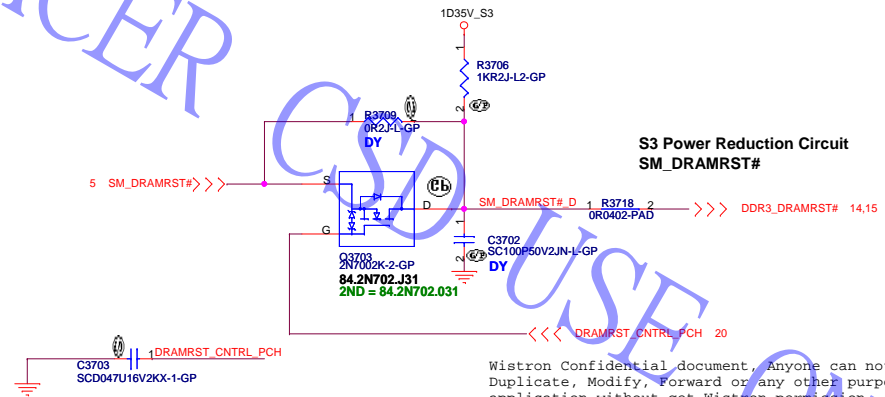
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S3 Power Reduction Circuit Processor VREF\_DQ Implementation



Close to DIMM  
S3 Power Reduction Circuit SM\_DRAMPWROK

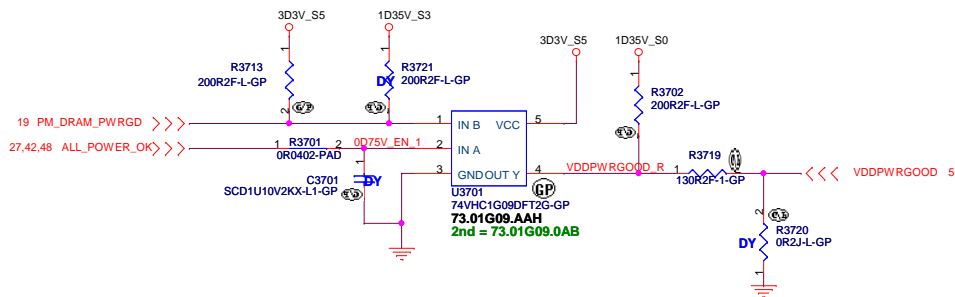


Close to CPU  
S3 Power Reduction Circuit SM\_DRAMPWROK



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Close to CPU  
S3 Power Reduction Circuit SM\_DRAMPWROK



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Title

**ADAPTER**

Size

Document Number

**EA40 CX**

Date

Thursday, June 20, 2013

Sheet

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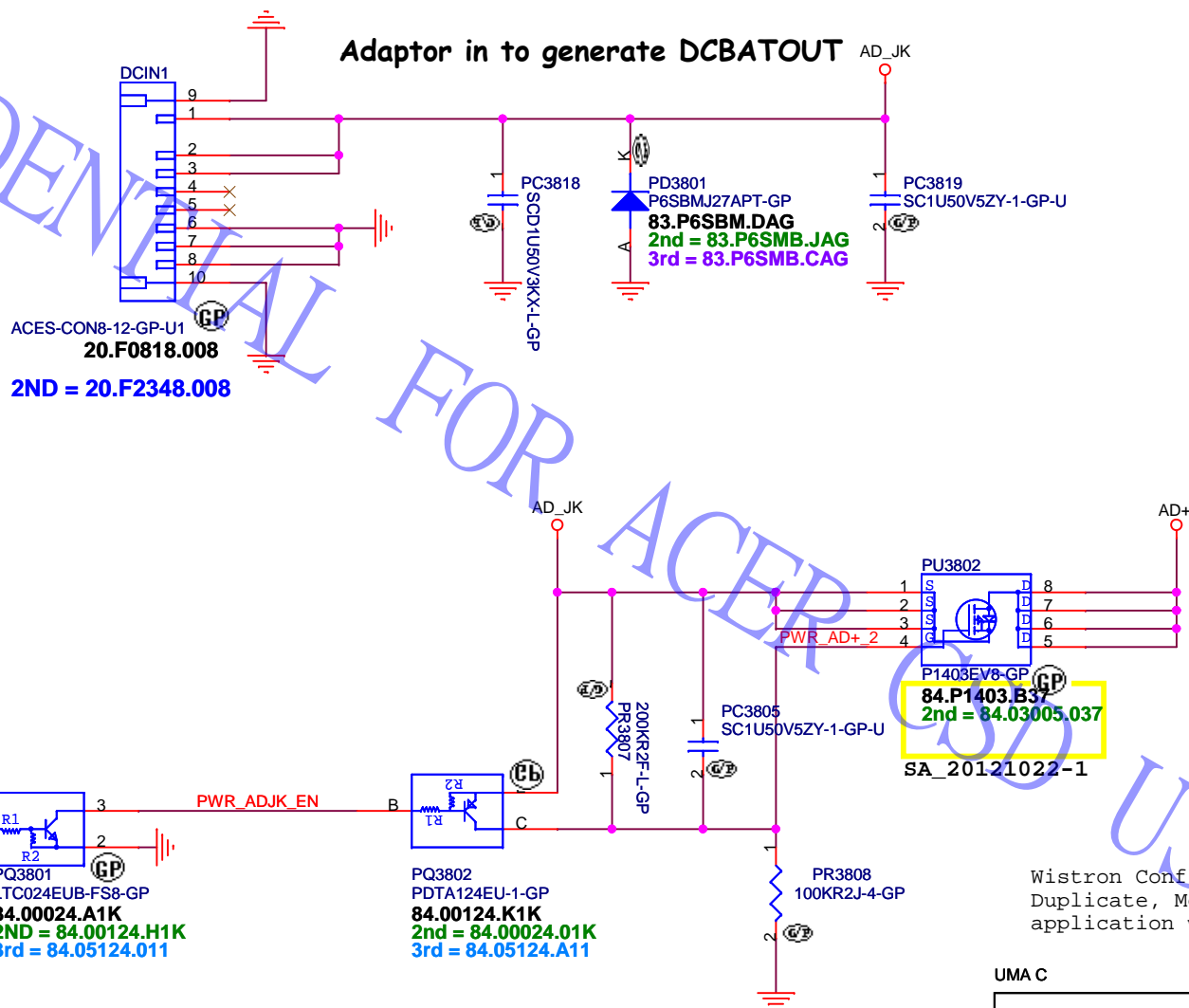
of

103

Rev

**-3**

# Adaptor in to generate DCBATOUT AD\_JK



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Title

**DCIN JACK**

Size  
A4

Document Number

**EA40 CX**

Rev

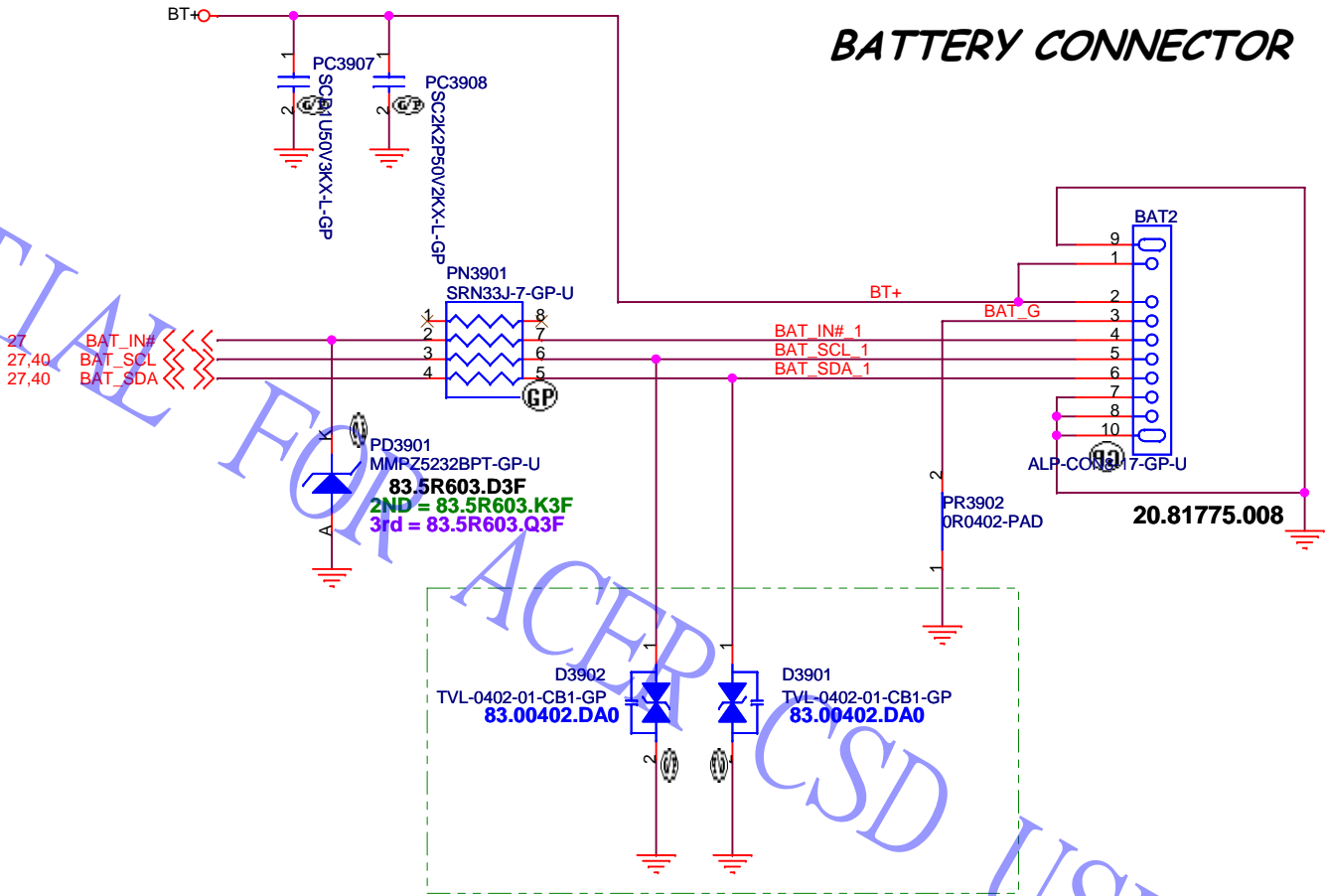
**-3**

Date: Thursday, June 20, 2013

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BATTERY CONNECTOR

97 BAT\_IN#\_1 <<<  
97 BAT\_SCL\_1 <<>>  
97 BAT\_SDA\_1 <<>>  
97 BAT\_G <<<



SC\_20130205\_AFR

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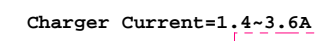
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| BATT CONN  |                         |  |                     |    |        |
| Size   | Document Number         |  |                     |    | Rev    |
| A4   | EA40 CX                 |  |                     |    | -3     |
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SA:change the  
PD4002  
P6SBMJ27APT-GP  
**83.P6SBM.DAG**  
**2nd = 83.P6SMB.JAG**  
**3rd = 83.P6SMB.CAG**

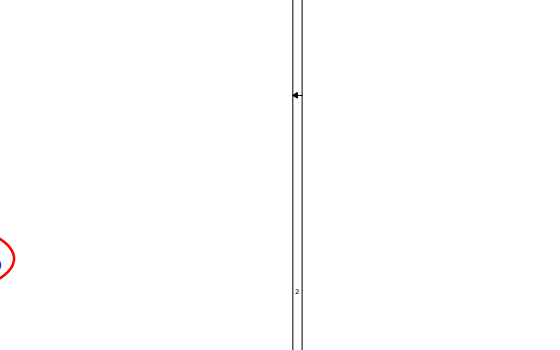
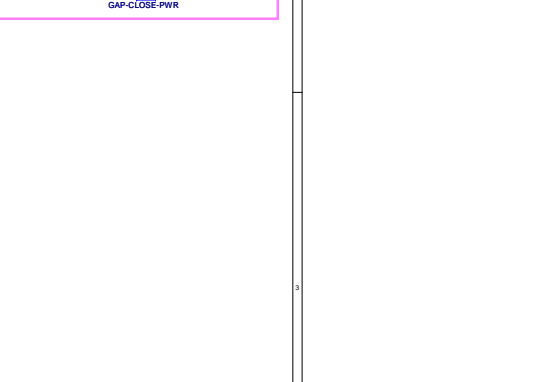
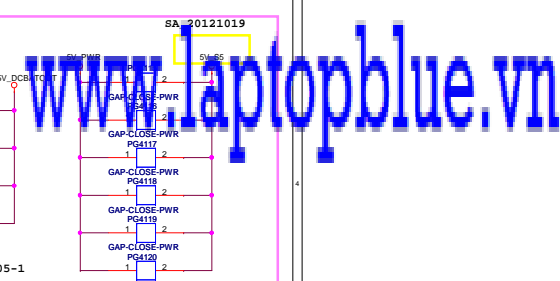
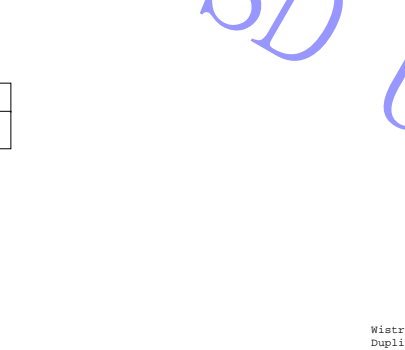
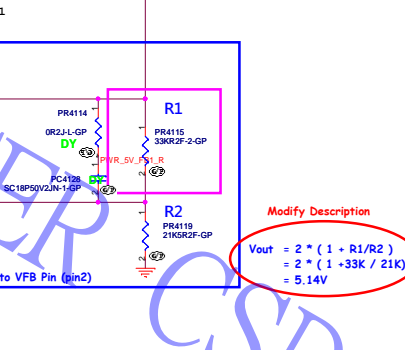
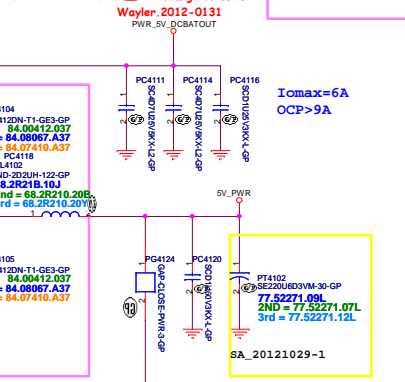
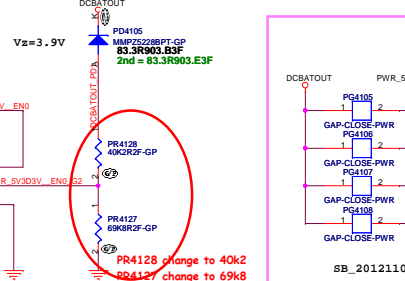
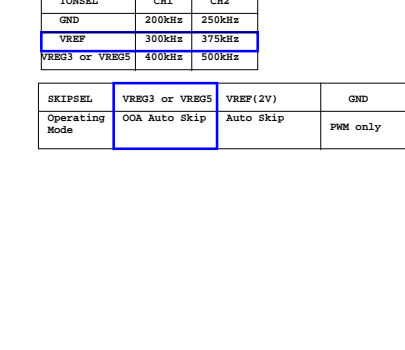
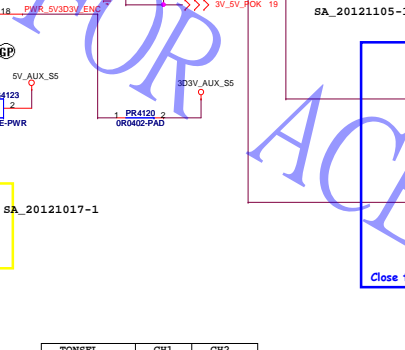
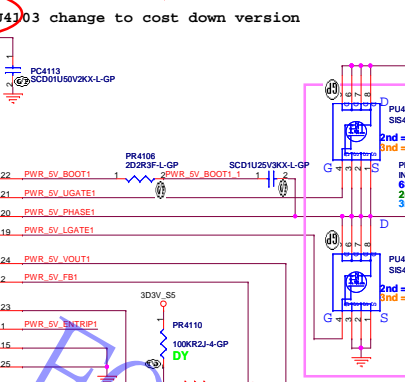
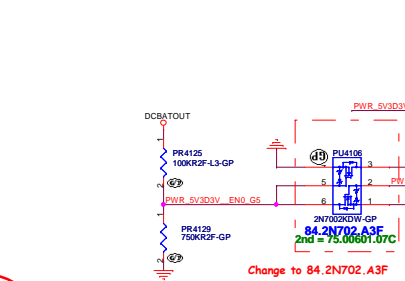
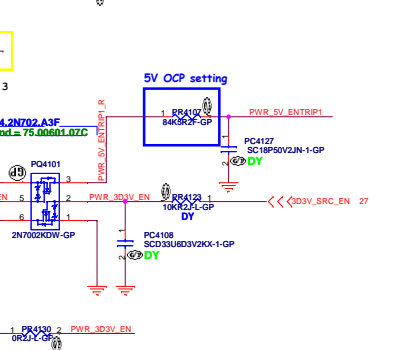
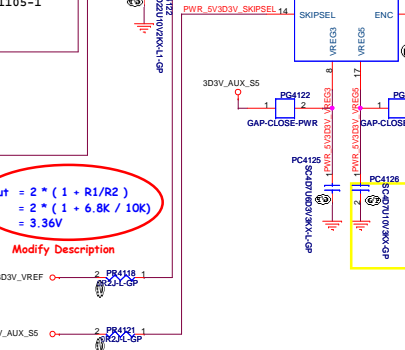
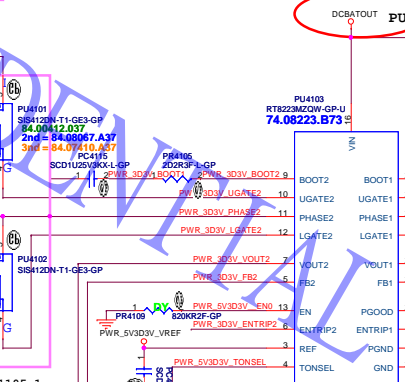
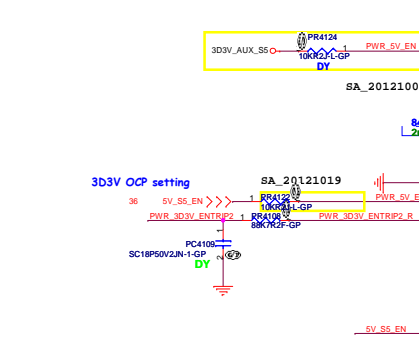
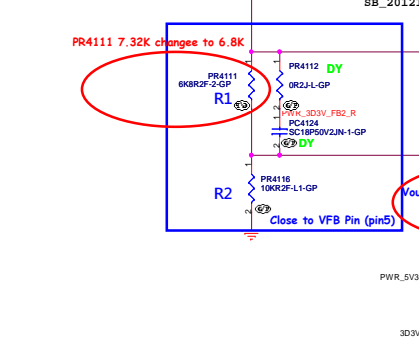
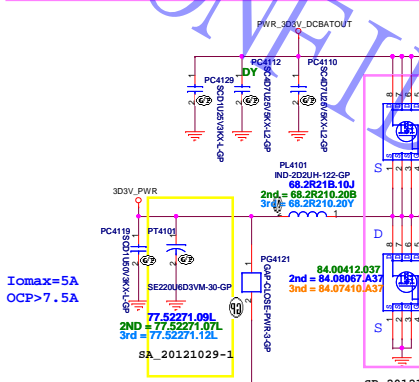
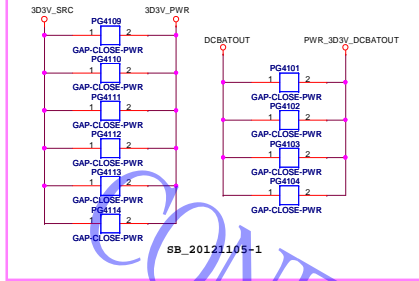
modify schematic  
Wayler , 2013-0315



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| Title  |                       |                 |
| <b>CHARGER BQ24727</b><br><b>EA40 CX</b>   |                       |                 |
| Size Custom  | Document Number       | Rev             |
|  |                       | <b>-3</b>       |
| Date:  | Friday, June 21, 2013 | Sheet 40 of 103 |

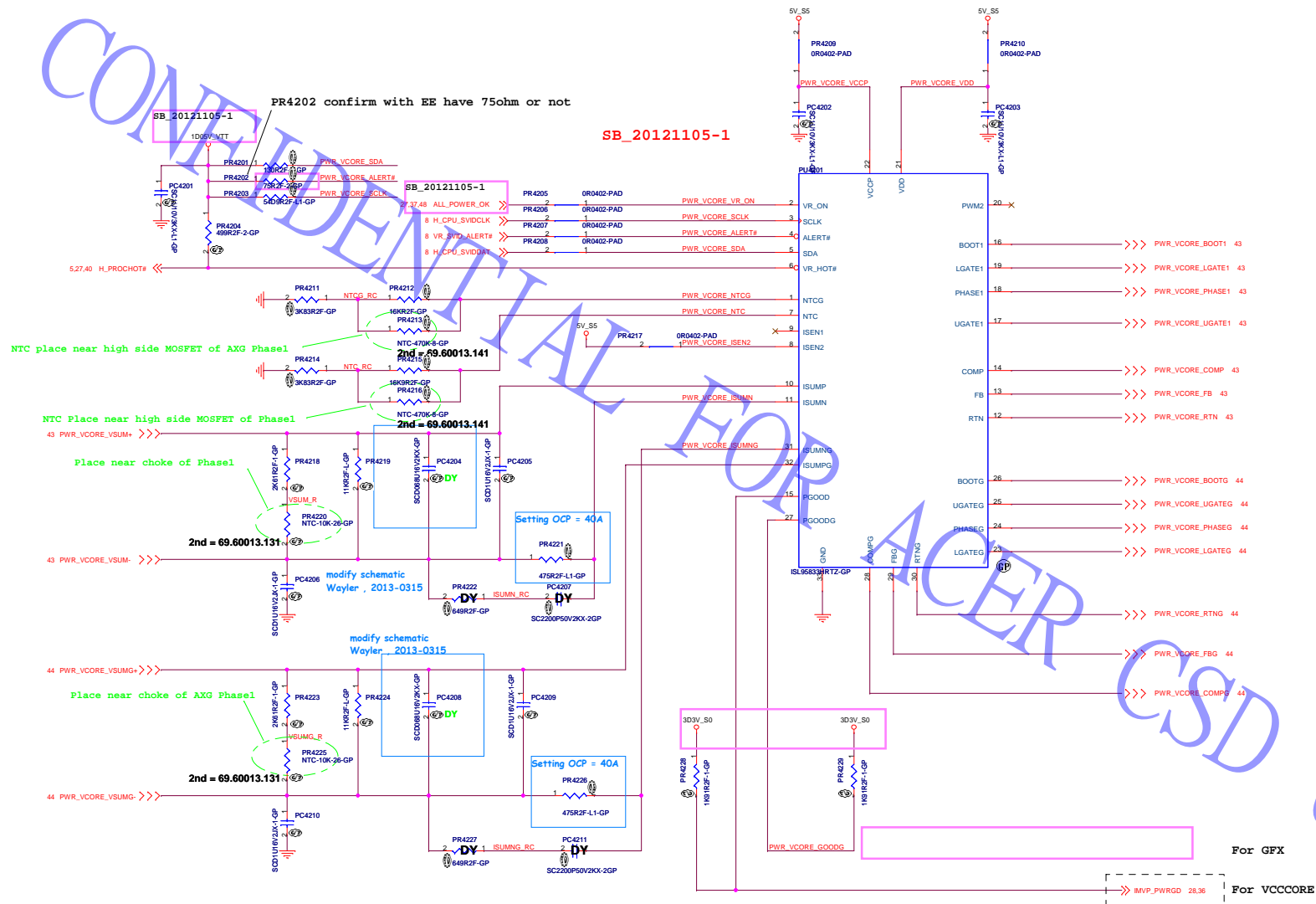




| TONSEL         | CH1    | CH2    |
|----------------|--------|--------|
| GND            | 200kHz | 250kHz |
| VREF           | 300kHz | 375kHz |
| VREG3 or VREG5 | 400kHz | 500kHz |

| SKIPSEL        | VREG3 or VREG5 | VREF(2V)  | GND      |
|----------------|----------------|-----------|----------|
| Operating Mode | OOA Auto Skip  | Auto Skip | PWM only |

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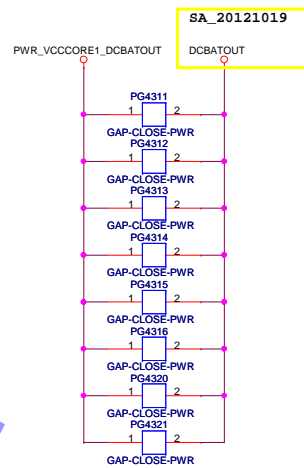
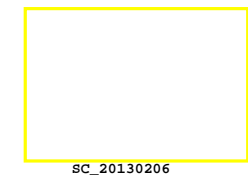
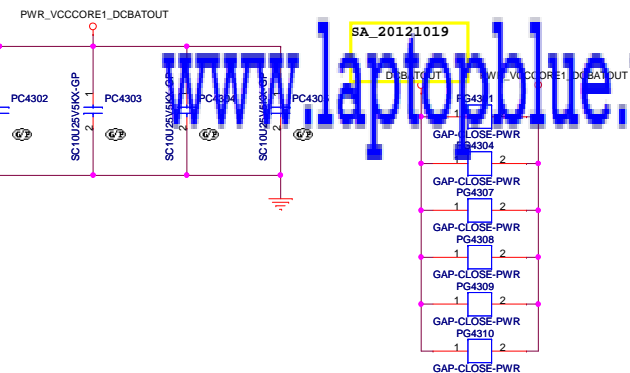
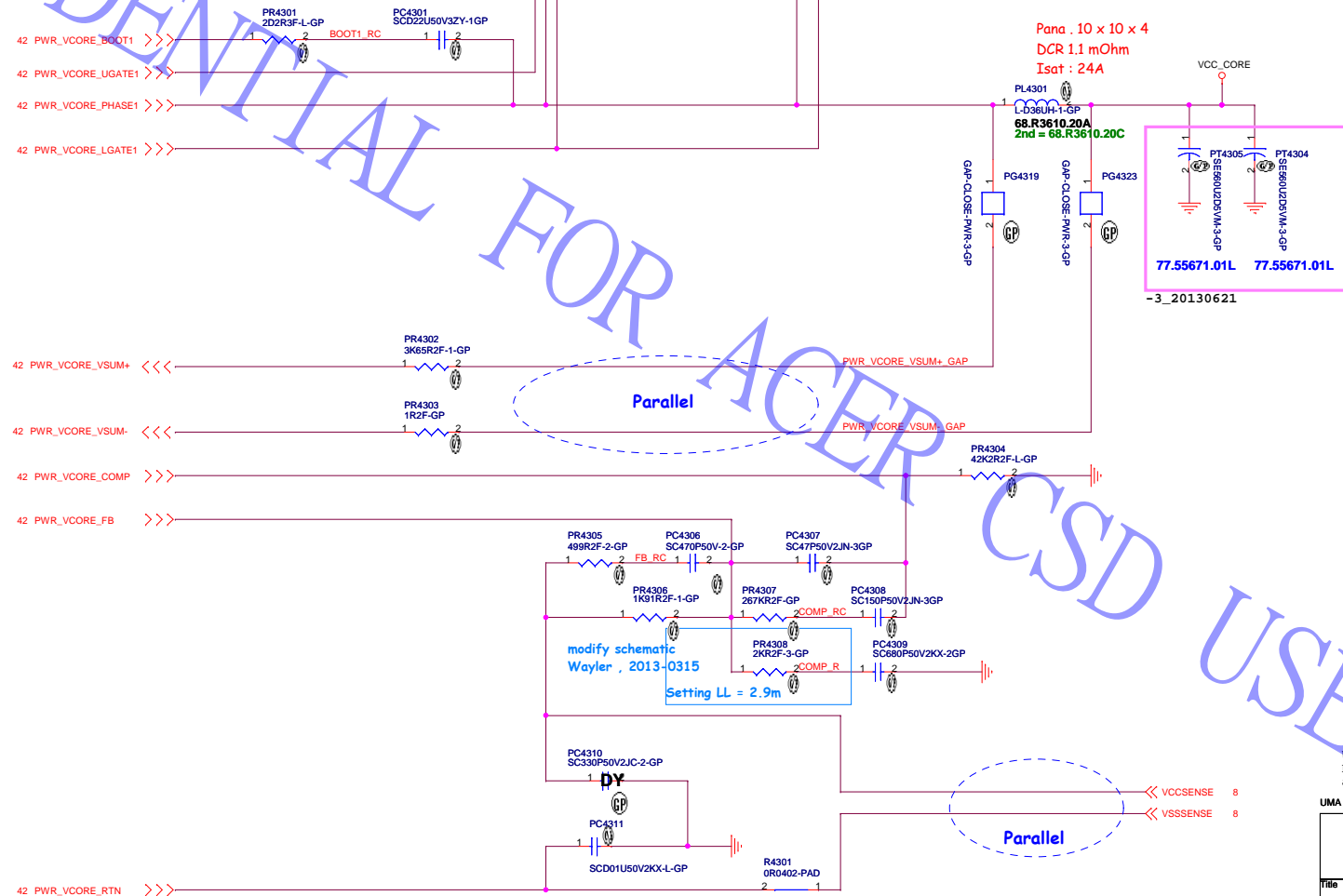
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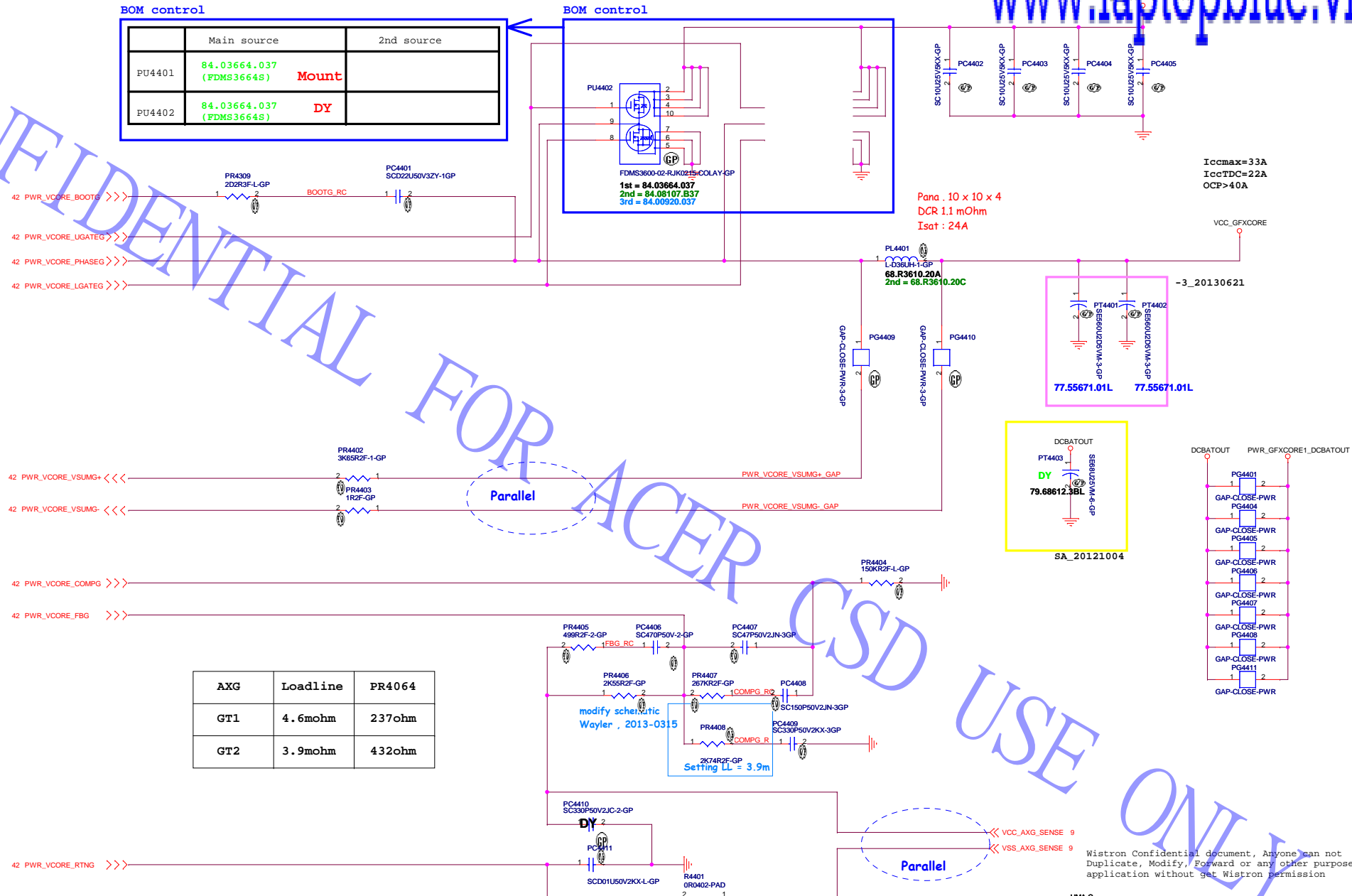
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|                                 |                            |                 |
|---------------------------------|----------------------------|-----------------|
| Title<br>ISL95833_CPU_CORE(1/3) |                            |                 |
| Size<br>Custom                  | Document Number<br>EA40_CX | Rev<br>-3       |
| Date: Friday, June 21, 2013     |                            | Sheet 42 of 103 |

|        | Main source                       | 2nd source |
|--------|-----------------------------------|------------|
| PU4301 | 84.03664.037<br>(FDMS3664S) Mount |            |
| PU4302 | 84.03664.037<br>(FDMS3664S) DY    |            |



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| AXG | Loadline | PR4064 |
|-----|----------|--------|
| GT1 | 4.6mohm  | 237ohm |
| GT2 | 3.9mohm  | 432ohm |

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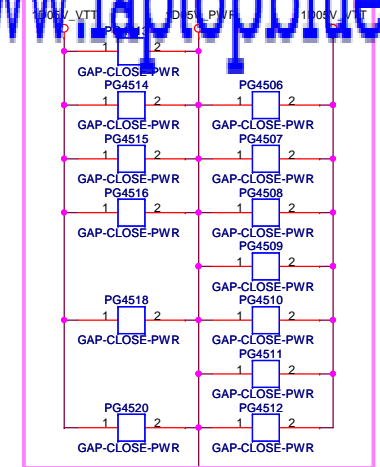
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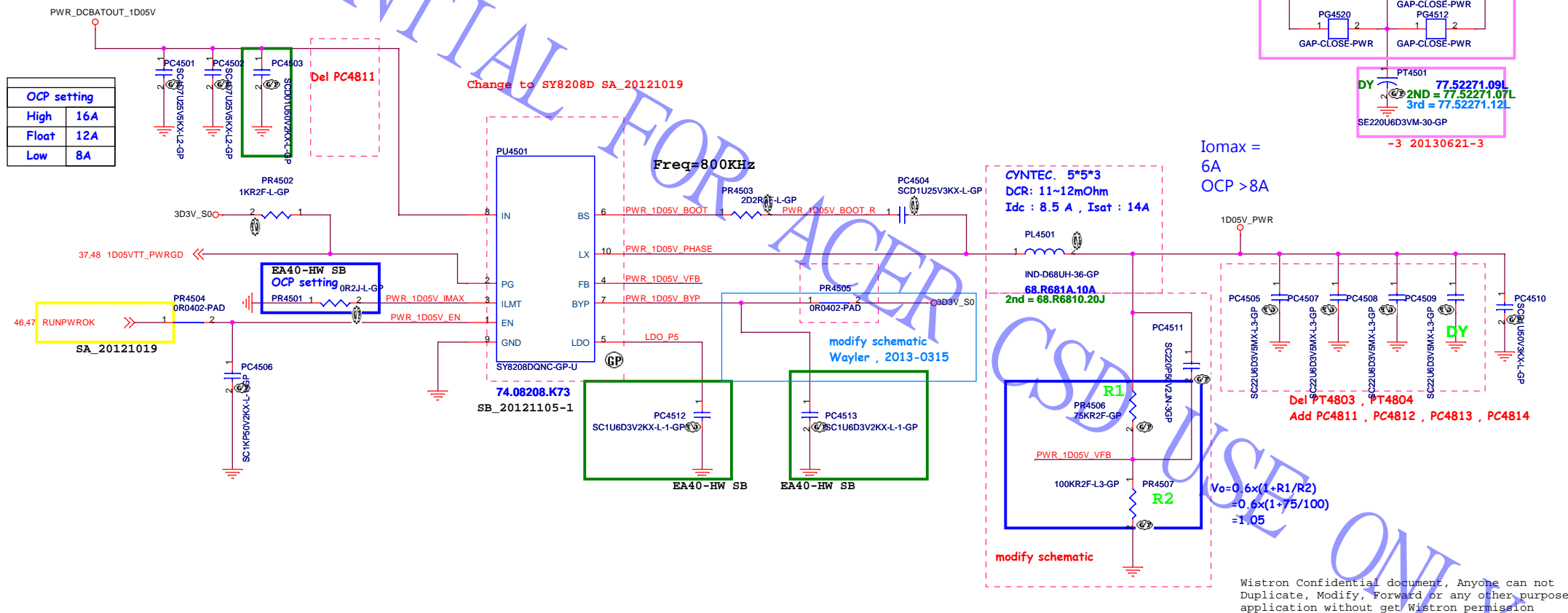
| Title  | ISL95833_CPU_CORE(3/3) |
|--------|------------------------|
| Size   | Document Number        |
| Custom | EA40 CX                |
| Date   | Friday, June 21, 2013  |
| Sheet  | 44 of 103              |
| Rev    | -3                     |

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SB 20121105-1



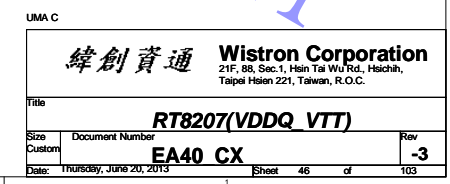
PT4501  
DY  
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3rd = 77.52271.07L  
77.52271.12L  
SE220U6D3VM-30-GP  
-3 20130621-3

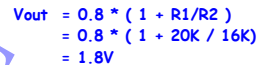


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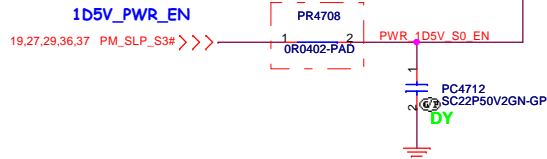
|   |                                   |                  |  |
|---|-----------------------------------|------------------|--|
| Title<br><b>DC to DC 1D05V(SY8208D)</b> |                                   |                  |  |
| Size<br>A3                              | Document Number<br><b>EA40 CX</b> | Rev<br><b>-3</b> |  |
| Date: Friday, June 21, 2013             | Sheet 45                          | of 103           |  |

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**RT8207L for VDDQ**

[illegible]

Icc\_Max:0.167A  
TDC: 0.134A  
OCP:0.217A  
1D5V LDO



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Title

**LDO 1D8V&1D5V(RT9025)**

Size

Document Number

EA40 CX

|     |
|-----|
| Rev |
|-----|

Date: Thursday, June 20, 2013

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The schematic diagram illustrates the electrical connections for the LCD module. It features two main input sections: LVDS (Liquid Crystal Display Voltage-Sensitive Differential Signaling) and DP (DisplayPort). The LVDS section is highlighted with a yellow box and includes components like C4901, C4902, C4903, C4904, C4905, and C4906, which are connected to the LVDS01 input. The DP section is highlighted with a blue box and includes components like C4907, C4908, C4909, C4910, C4911, and C4912, which are connected to the DP input. The diagram also shows the connection of the LCD panel to the module, including the LCD panel, LCD panel driver, and LCD panel controller. A large blue watermark 'SAMPLE IDENTIFICATION' is overlaid on the diagram.

```

97 DP_HPD0_C >>>_____
97 BLON_OUT_C >>>_____
97 LCD_BRIGHTNESS >>>_____

```

For TestPoint

```
97 DP_TXN0_CPU_C>>>
97 DP_TXP1_CPU_C>>>
97 DP_TXN0_CPU_C>>>
97 DP_TXP0_CPU_C>>>
97 DP_AUXP_CPU_C>>>
97 DP_AUXN_CPU_C>>>
```

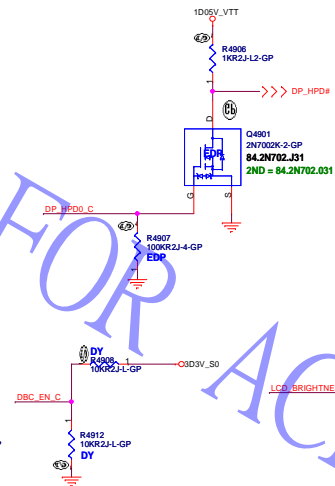
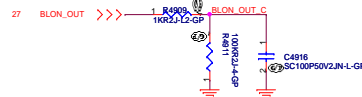
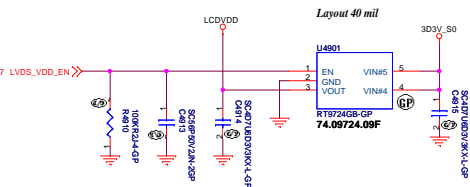
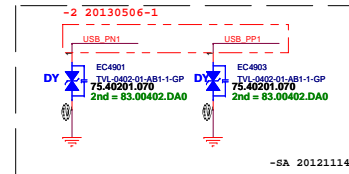
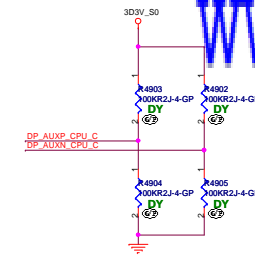
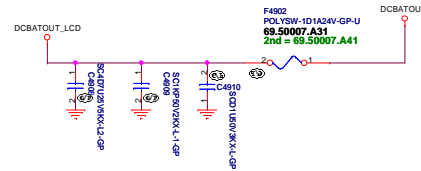
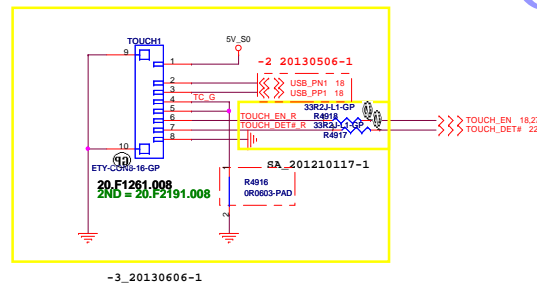
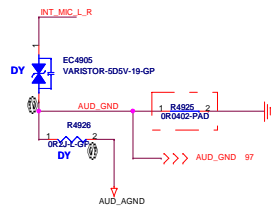


Diagram illustrating the pin connections for the ACES-C6013-6P-U1 connector. The connector is labeled MCCR1 and has pins 1 through 10. The connections are as follows:

- Pins 1 and 2: USB\_CAMERA\_P (Red)
- Pins 3 and 4: USB\_CAMERA\_N (Blue)
- Pins 5 and 6: USB\_CAMERA\_0 (Green)
- Pins 7 and 8: INT\_ABC\_L\_R (Red)
- Pins 9 and 10: AUD\_GND (Red)

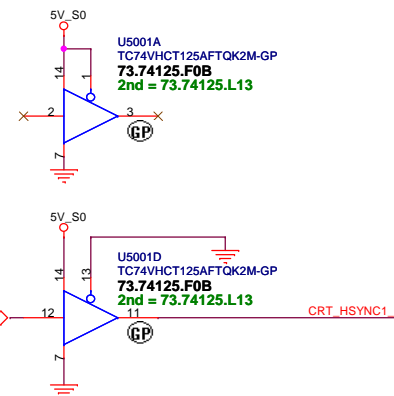
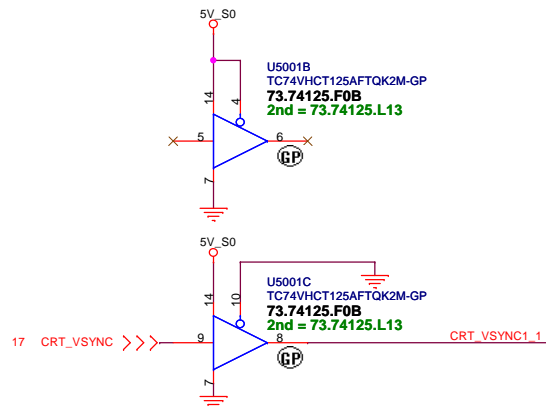
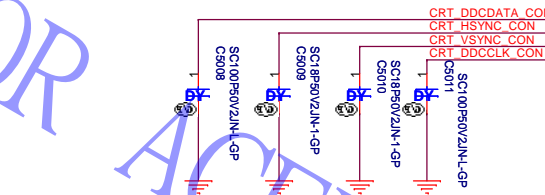
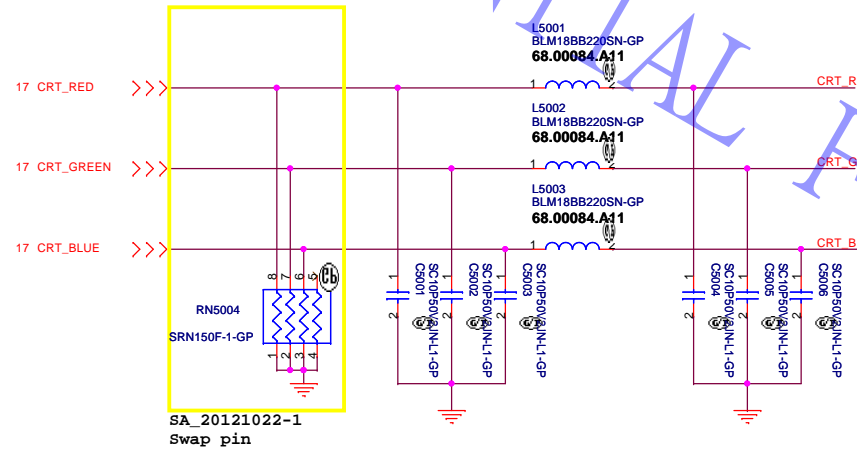
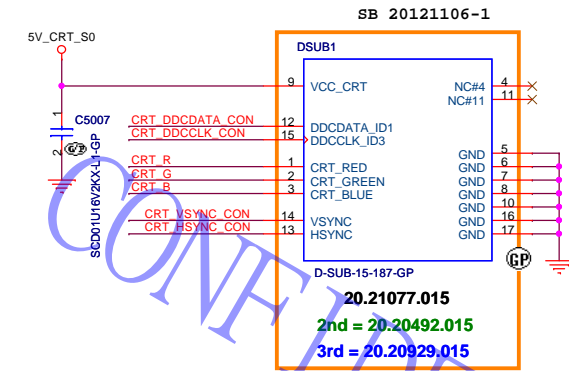
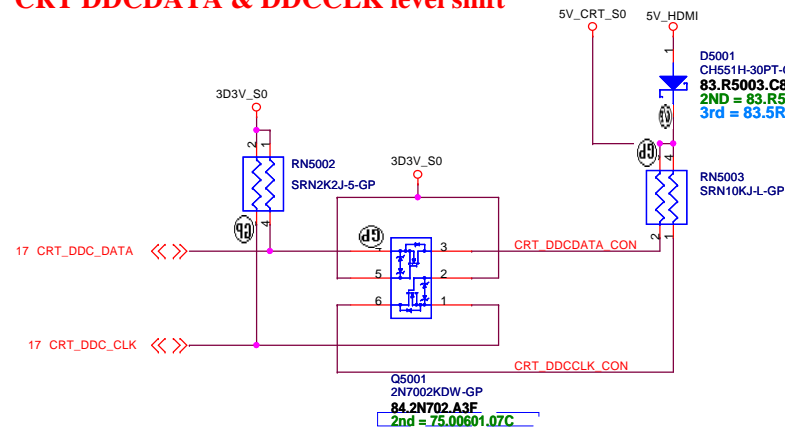
Additional connections and labels:

- Pin 10: ACES-C6013-6P-U1
- Pin 10: 20.F1295.008
- Pin 10: 2ND = 20.F2120.008
- Pin 10: -SB 20121114-2 modify name
- Pin 10: ER4913 2 OR4042-PAD USB\_PP3 18
- Pin 10: ER4914 2 OR4042-PAD USB\_PFN3 18
- Pin 10: USB\_CAMERA\_0
- Pin 10: INT\_ABC\_L\_R 29.87
- Pin 10: AUD\_GND 97



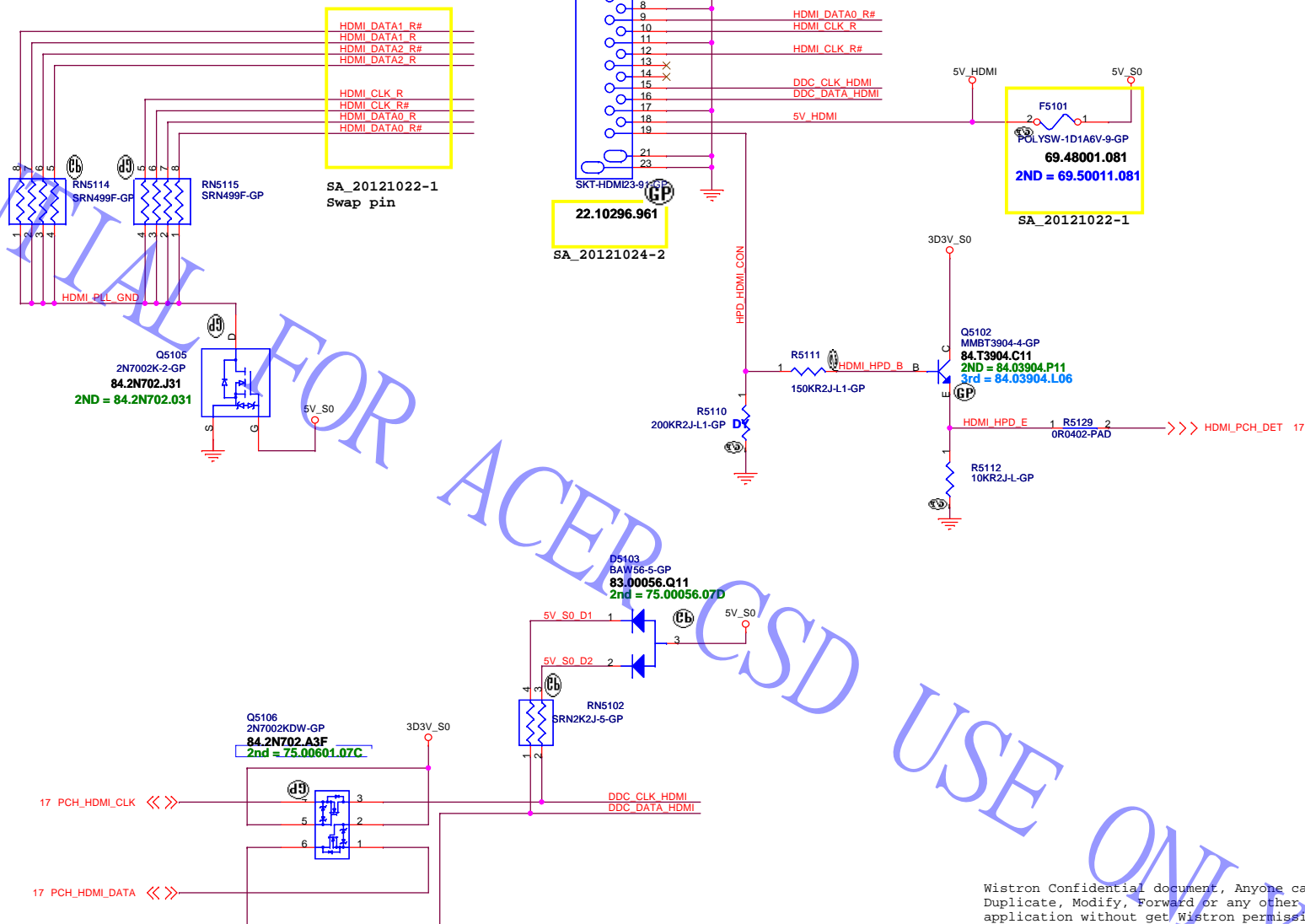
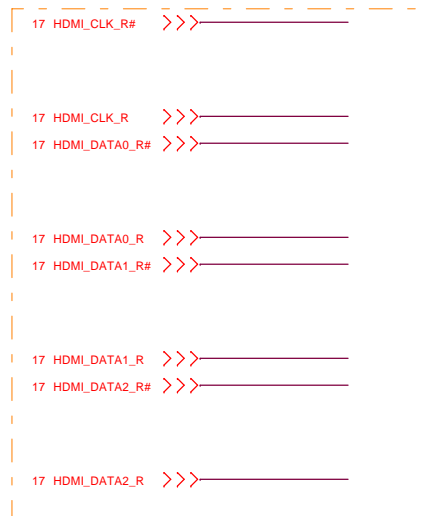
|   |                          |   |        |
|---|--------------------------|---|--------|
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| Title   |                          |   |        |
| <b>LCD Connector</b>  |                          |   |        |
| Size  | Document Number          | Rev   |        |
|   | <b>E40 CX</b>            | <b>-3</b>   |        |
| Date:   | Wednesday, June 10, 2013 | Sheet 48  | of 103 |

|                      |                          |                 |
|----------------------|--------------------------|-----------------|
| Title                |                          |                 |
| <b>LCD Connector</b> |                          |                 |
| Size<br>A2           | Document Number          | Rev             |
|                      | <b>EA40 CX</b>           | <b>-3</b>       |
| Date:                | Wednesday, June 19, 2013 | Sheet 49 of 103 |



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**-1 20130315A**



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Title

### **HDMI Level Shifter/Connector**

Size

|   |                 |
|---|-----------------|
| e | Document Number |
|---|-----------------|

A3

**EA40\_CX**

Date: Thursday, June 20, 2013

Sheet 4

Rev

3

103

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| Title eDP  |                         |
| Size A3  | Document Number EA40 CX |
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| Title <div>S-VIDEO</div>   |                                    |                   |
| Size <div>A4</div>   | Document Number <div>EA40 CX</div> | Rev <div>-3</div> |
| Date: Thursday, June 06, 2013  |                                    | Sheet 53 of 103   |

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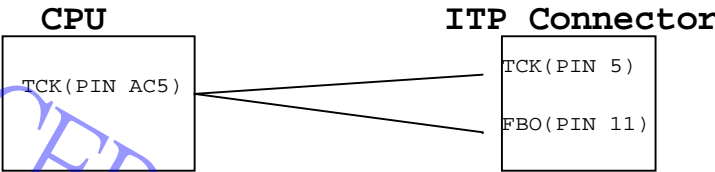
Title  
**Reserved**

|            |                                   |                  |
|------------|-----------------------------------|------------------|
| Size<br>A4 | Document Number<br><b>EA40 CX</b> | Rev<br><b>-3</b> |
|------------|-----------------------------------|------------------|

SSID = User.Interface

ITP Connector

H\_CPURST# use pull-up Resistor close  
ITP connector 500 mil ( max ),  
others place near CPU side.

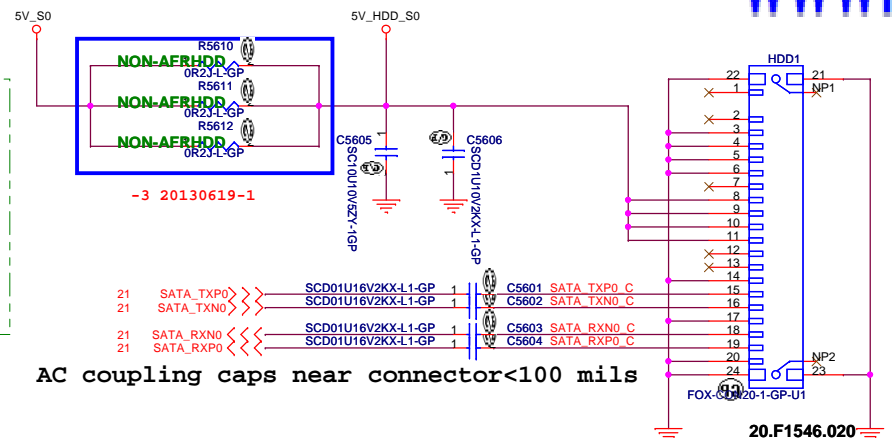


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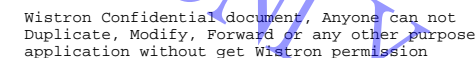
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| Title  |                 |  |                     |  |     |
| ITP  |                 |  |                     |  |     |
| Size   | Document Number |  |                     |  | Rev |
| A4   | EA40 CX         |  |                     |  | -3  |
| Date: Thursday, June 06, 2013  |                 |  | Sheet 55 of 103     |  |     |

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2nd = 20.F1473.020  
3rd = 20.F2307.020

## SATA Zero Power ODD



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**HDD / ODD / NGFF SSD**

## EA40 CX

Sheet 56 of 103

-3



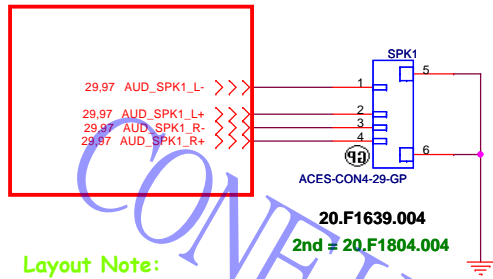
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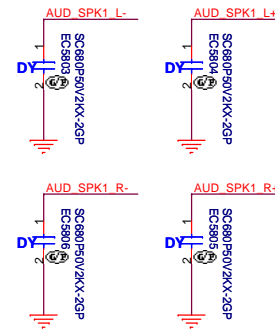
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| Title              |                         |  |                 |
| E-SATA/USB CHARGER |                         |  |                 |
| Size               | Document Number         |  | Rev             |
| A3                 | EA40_CX                 |  | -3              |
| Date:              | Thursday, June 06, 2013 |  | Sheet 57 of 103 |

SSID = AUDIO *Speaker*

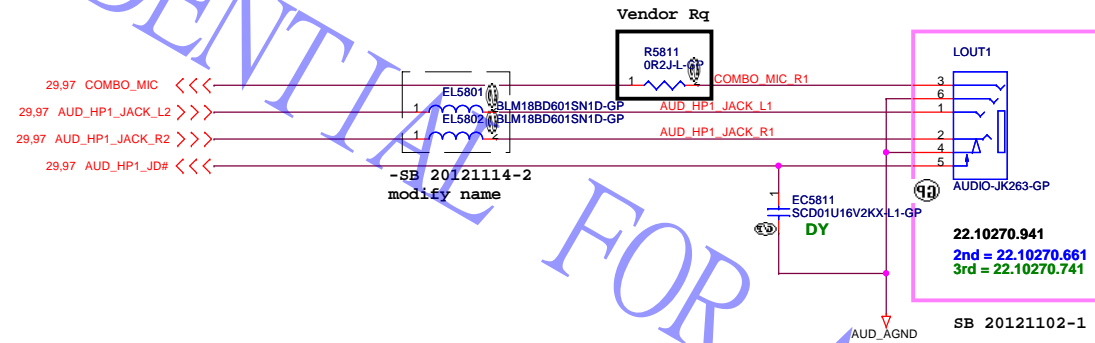


Trace width=40mil



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### Combo Jack



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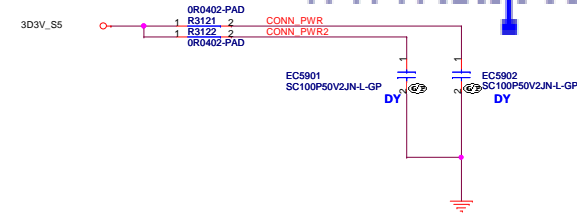
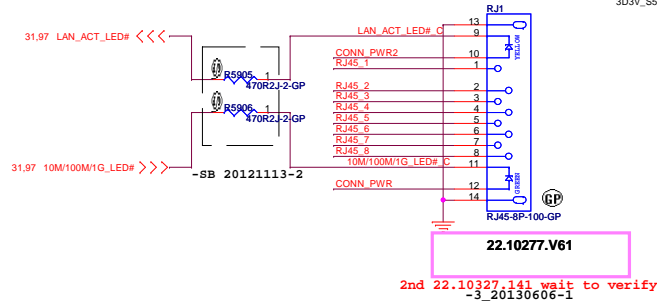
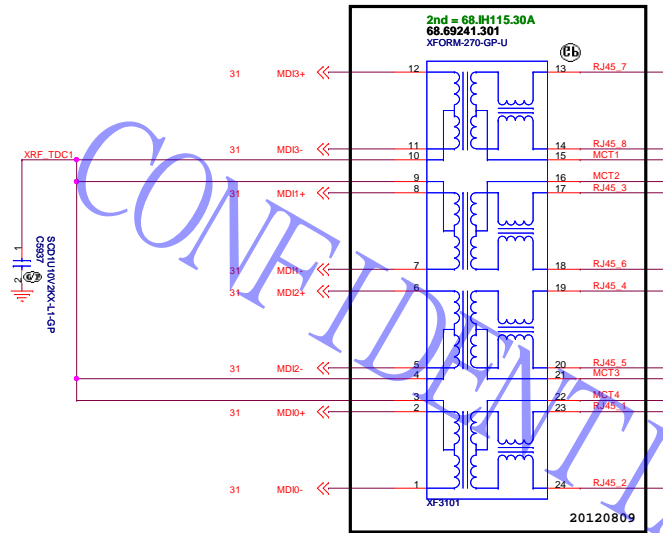
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|                   |                         |  |                 |
|-------------------|-------------------------|--|-----------------|
| Title             |                         |  |                 |
| <b>Audio Jack</b> |                         |  |                 |
| Size<br>A3        | Document Number         |  | Rev             |
|                   | <b>EA40 CX</b>          |  | <b>-3</b>       |
| Date:             | Thursday, June 06, 2013 |  | Sheet 58 of 103 |

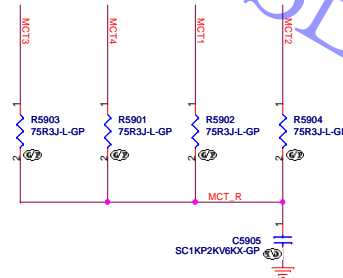
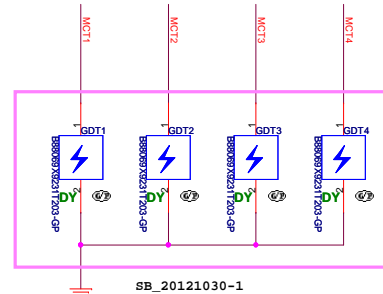
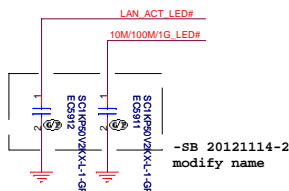
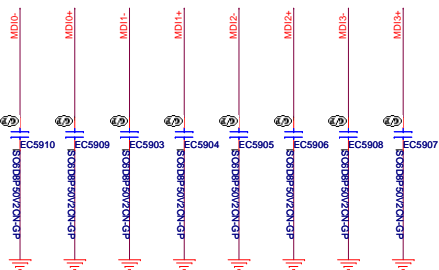
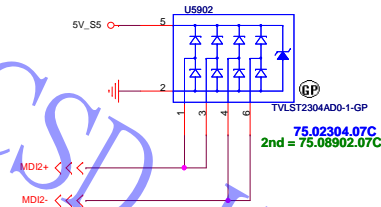
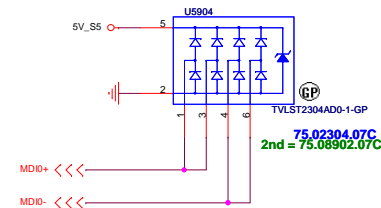
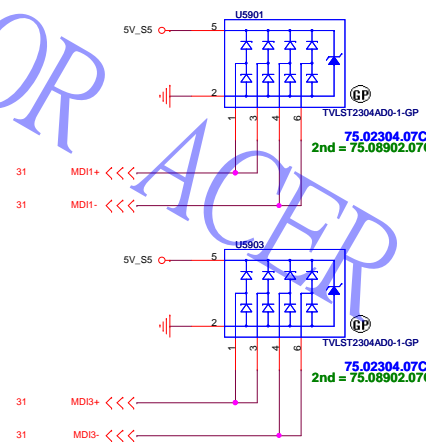
SSID = LAN

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97 RJ45\_1 >>>>  
97 RJ45\_2 >>>>  
97 RJ45\_3 >>>>  
97 RJ45\_4 >>>>  
97 RJ45\_5 >>>>  
97 RJ45\_6 >>>>  
97 RJ45\_7 >>>>  
97 RJ45\_8 >>>>

31.97 LAN\_ACT\_LED# >>>>  
31.97 10M/100M/1G\_LED# >>>>  
97 CONN\_PWR >>>>  
97 CONN\_PWR2 >>>>

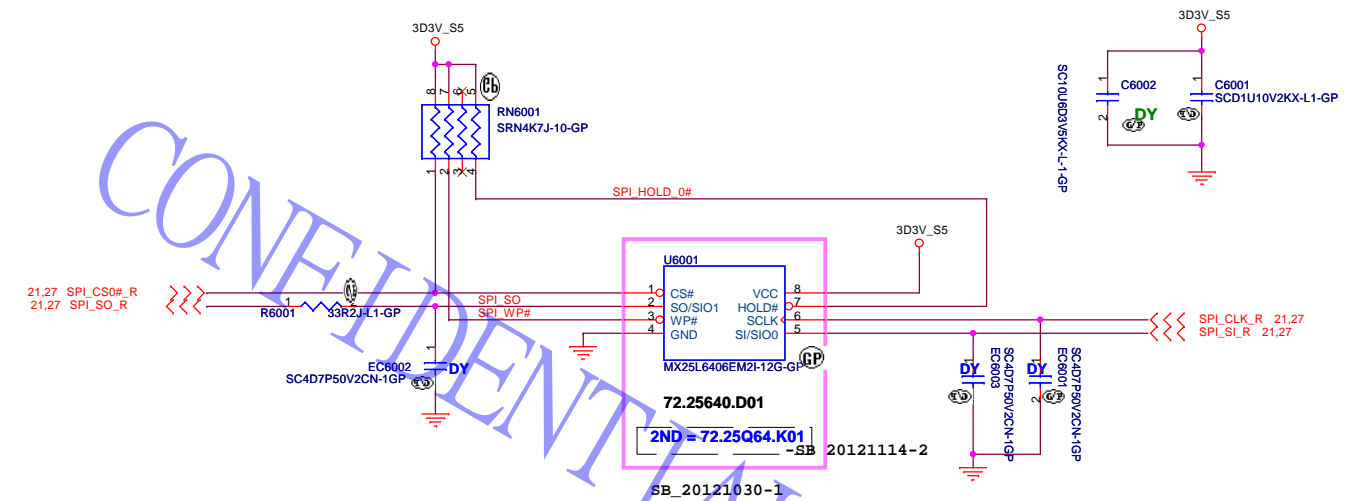


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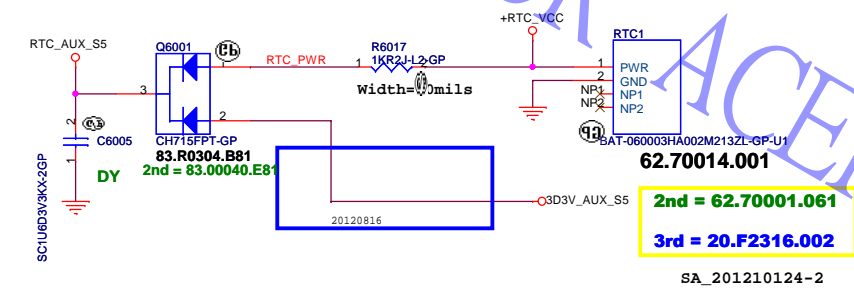
|  |                         |
|--|-------------------------|
| UMAC   |                         |
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| Title  | LAN CONNECTOR           |
| Size   | Document Number         |
| Custom   | EA40 CX                 |
| Date   | Thursday, June 20, 2013 |
| Sheet  | 59 of 103               |
| Rev  | -3                      |

SSID = Flash.ROM

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SSID = RTC



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| Title Flash/RTC  |                         |
| Size Custom  | Document Number EA40 CX |
| Date: Thursday, June 20, 2013  | Sheet 60 of 103         |

SSID = USB

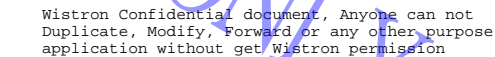
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| Title<br>USB Power SW  |                            |
| Size<br>A3   | Document Number<br>EA40_CX |
| Date: Thursday, June 06, 2013  | Rev<br>-3                  |
| Sheet 61 of 103  |                            |

| USB 3.0 Connector<br>Pin definition |                          |
|-------------------------------------|--------------------------|
| 1                                   | POWER                    |
| 2                                   | USB 2.0 D-               |
| 3                                   | USB 2.0 D+               |
| 4                                   | GND                      |
| 5                                   | StdA_SSRX- SuperSpeed RX |
| 6                                   | StdA_SSRX+               |
| 7                                   | GND                      |
| 8                                   | StdA_SSTX- SuperSpeed TX |
| 9                                   | StdA_SSTX+               |



SSID = User.Interface  
Bluetooth Module conn.

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*ANNIE Bluetooth Module*

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**Bluetooth**

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Rev  
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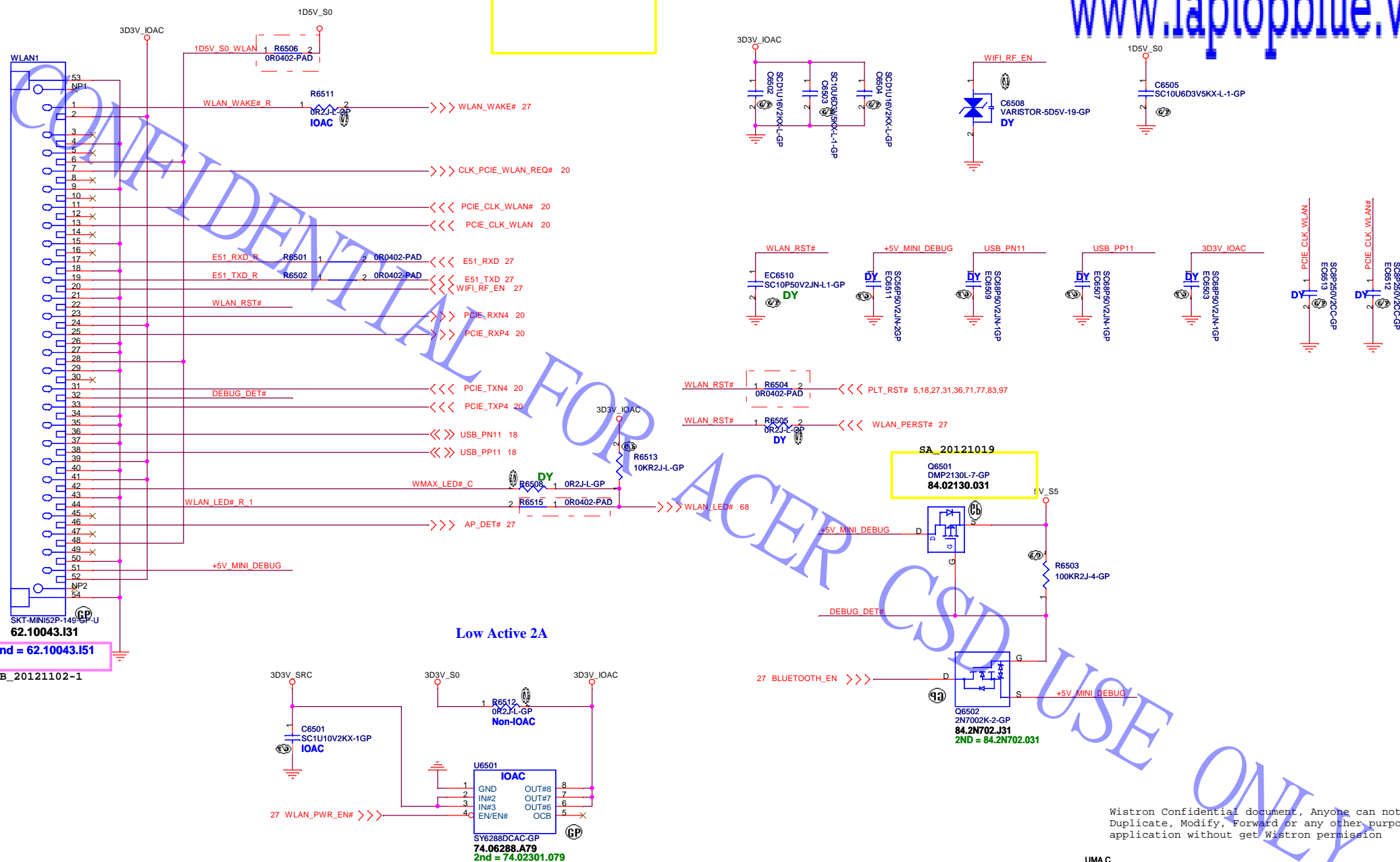
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|------------|-----------------------------------|------------------|



### *Mini Card Connector(802.11a/b/g/n)*

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Title

**MINICARD(WLAN)/ITP CONN**

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SSID = Wireless

Mini Card Connector(WWAN)

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| A4                            | EA40 CX         |  |  |  | -3  |
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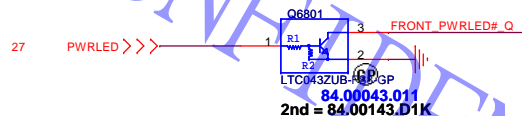
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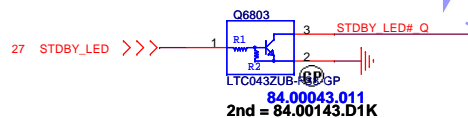
SSID = User.Interface

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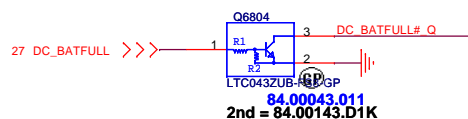
## Power button LED



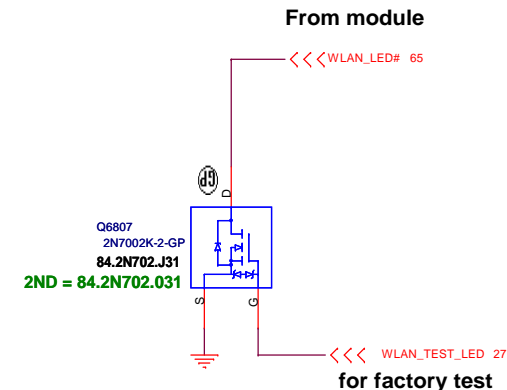
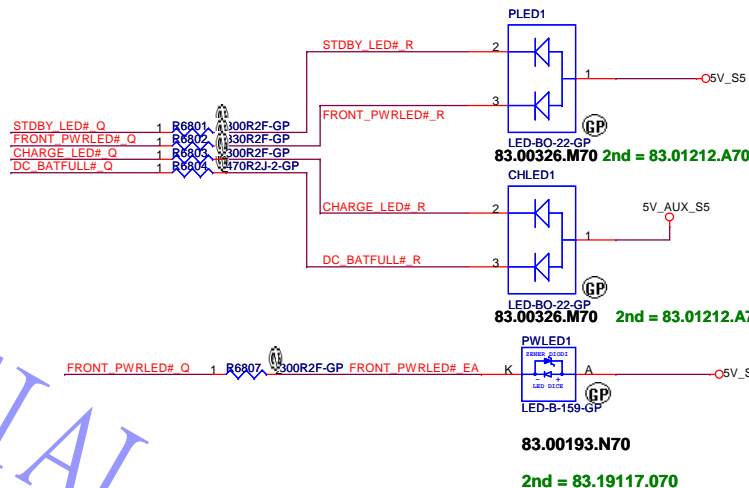
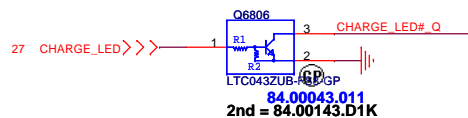
## Power STDBY\_LED



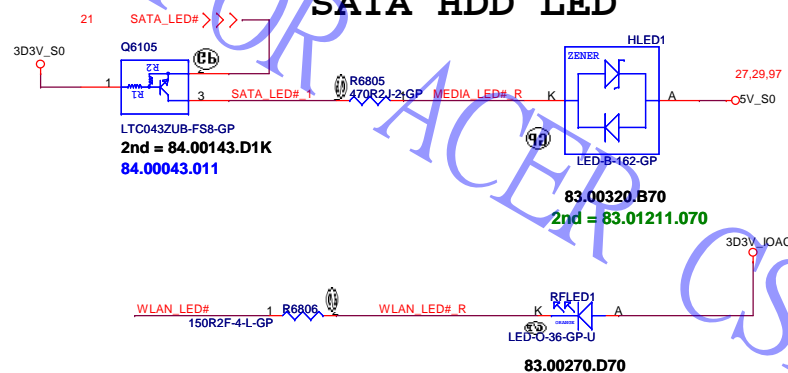
## Battery LED2(DC\_BATFULL)



## Battery LED1(CHARGE)



## SATA HDD LED



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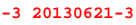
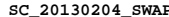
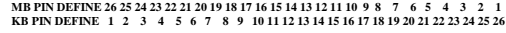
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| LED Bard/Power Button |                         |                 |
| Size                  | Document Number         | Rev             |
| Custom                | EA40_CX                 | -3              |
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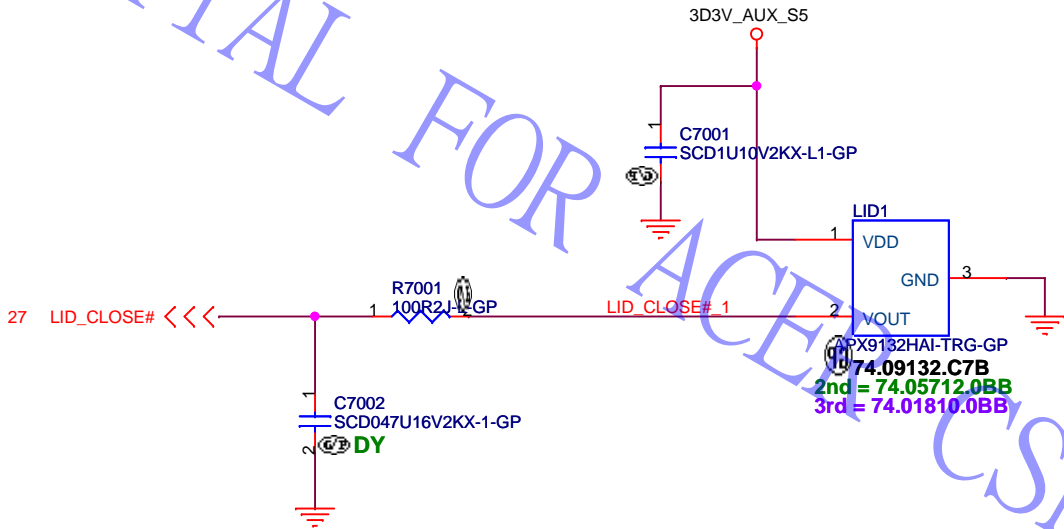
## ***Internal KeyBoard Connector***

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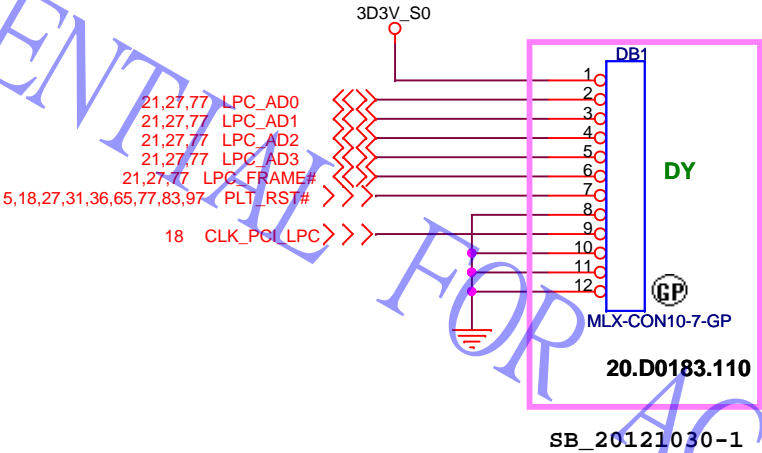
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| <b>Hall Sensor</b> |                                   |   |                  |
| Size<br>A4         | Document Number<br><b>EA40 CX</b> |   | Rev<br><b>-3</b> |
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| Dubug connector               |                 |          |  |        |     |
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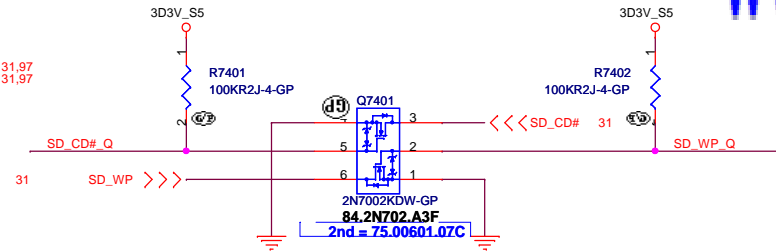
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|      |      |        |         |        |
|------|------|--------|---------|--------|
| SP1  | SP1  | SD_D7  |         | xD_RDY |
| SP2  | SP2  | SD_D6  | MS_INS# | xD_RE# |
| SP3  | SP3  | SD_D5  |         | xD_CE# |
| SP4  | SP4  | SD_D4  |         | xD_WE# |
| SP5  | SP5  | SD_D1  | MS_CLK  | xD_D6  |
| SP6  | SP6  | SD_D0  | MS_D7   | xD_D5  |
| SP7  | SP7  | SD_CLK | MS_D3   | xD_D4  |
| SP8  | SP8  | SD_CMD | MS_D6   | xD_D3  |
| SP9  | SP9  | SD_D3  | MS_D2   | xD_D2  |
| SP10 | SP10 | SD_D2  |         | xD_D7  |
| SP11 | SP11 |        | MS_BS   | xD_CLE |
| SP12 | SP12 | SD_WP  | MS_D1   | xD_WP# |
| SP13 | SP13 | SD_CD# | MS_D5   | xD_ALE |
| SP14 | SP14 |        | MS_D4   | xD_D0  |
| SP15 | SP15 |        | MS_D0   | xD_D1  |
| SP16 | SP16 |        |         | xD_CD# |

```

97 SD_WP_Q      >>>_____
97 SD_CD#_Q     >>>_____

```

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|       |                         |
|-------|-------------------------|
| Title | <b>CARD Reader CONN</b> |
|-------|-------------------------|

|                               |                                   |                  |
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SSID = ExpressCard

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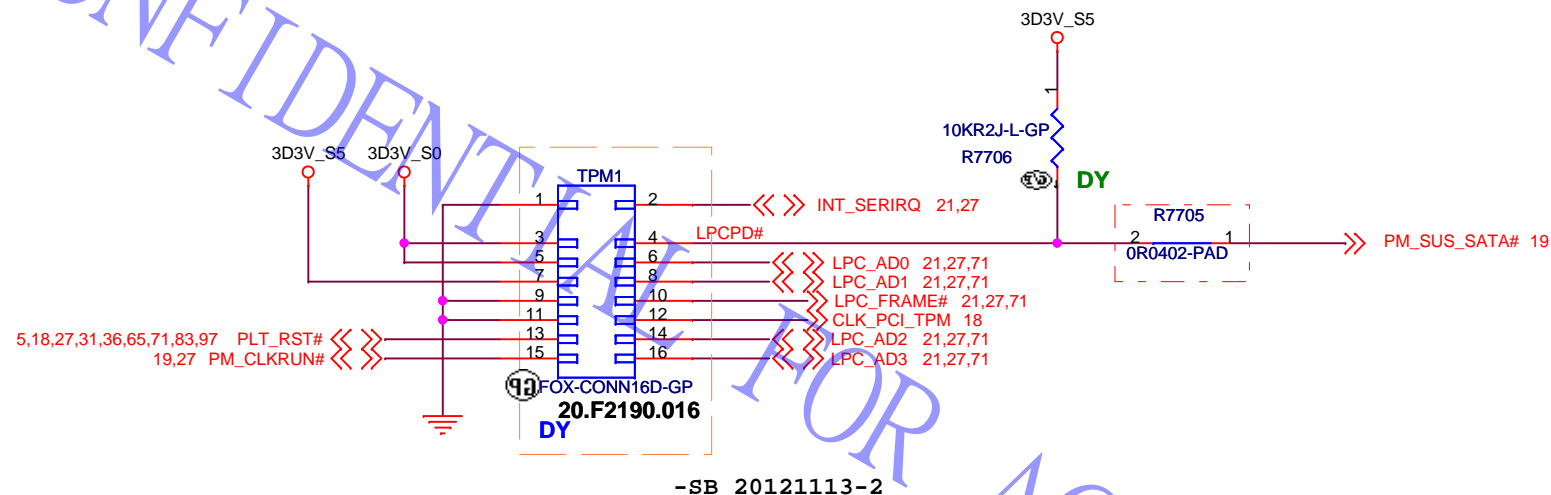
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A4

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| Document Number |
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## EA40 CX

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| Size <div>A4</div>   | Document Number <div>EA40 CX</div> | Rev <div>-3</div> |
| Date: Thursday, June 06, 2013  |                                    | Sheet 78 of 103   |

SSID = User.Interface

## Free Fall Sensor

### Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

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Title

**G- Sensor**

Size  
A4

Document Number

**EA40 CX**

Rev  
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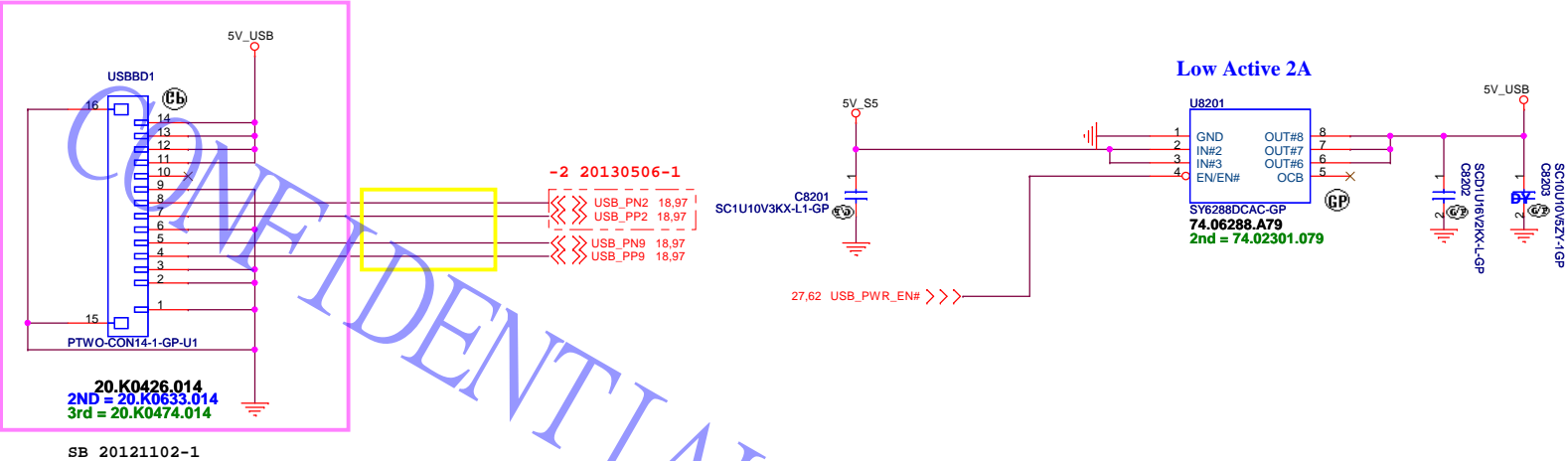
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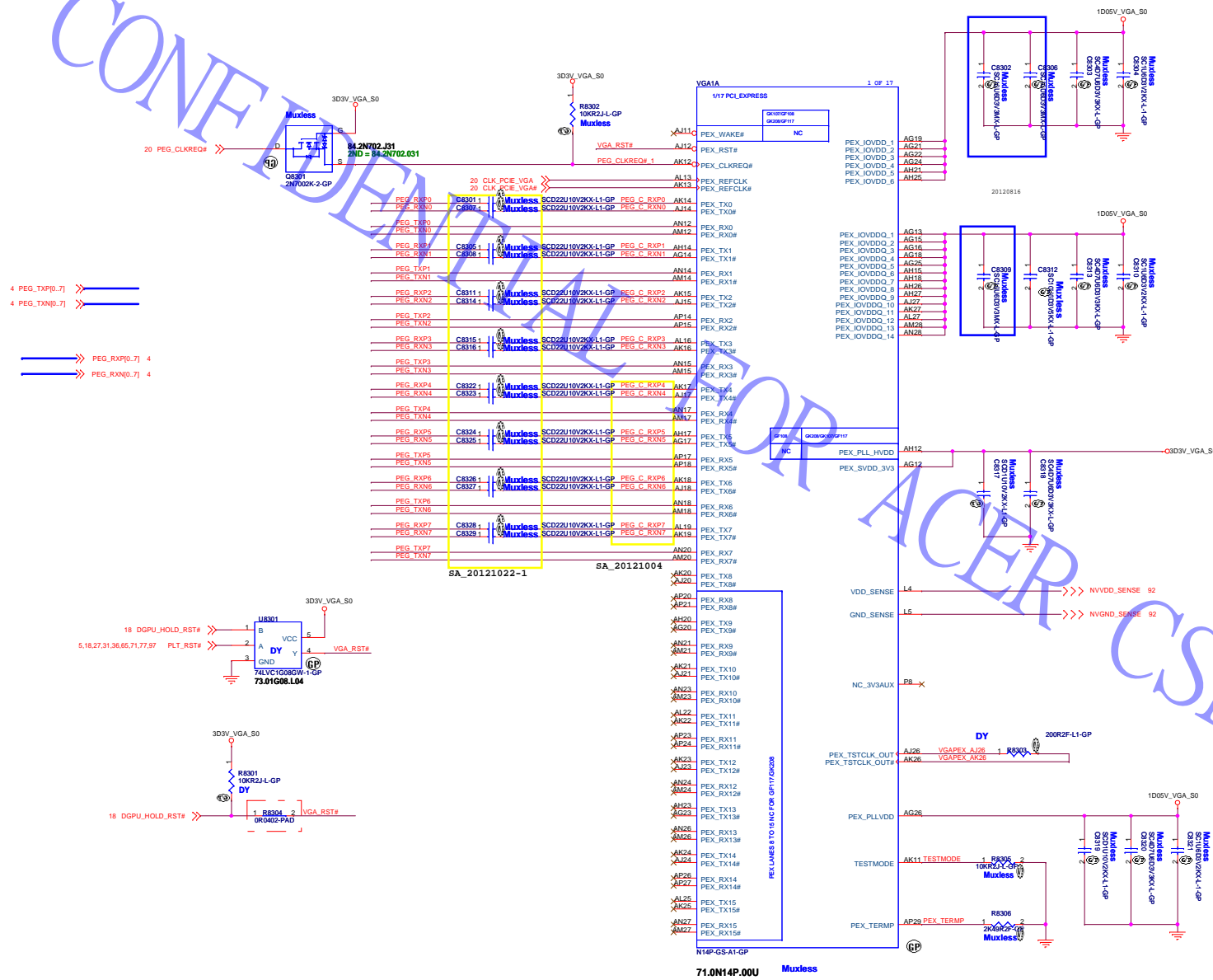
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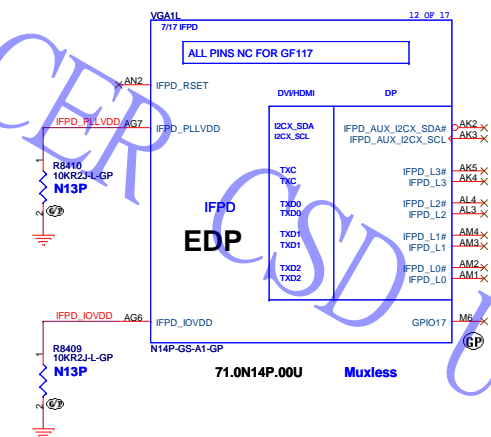
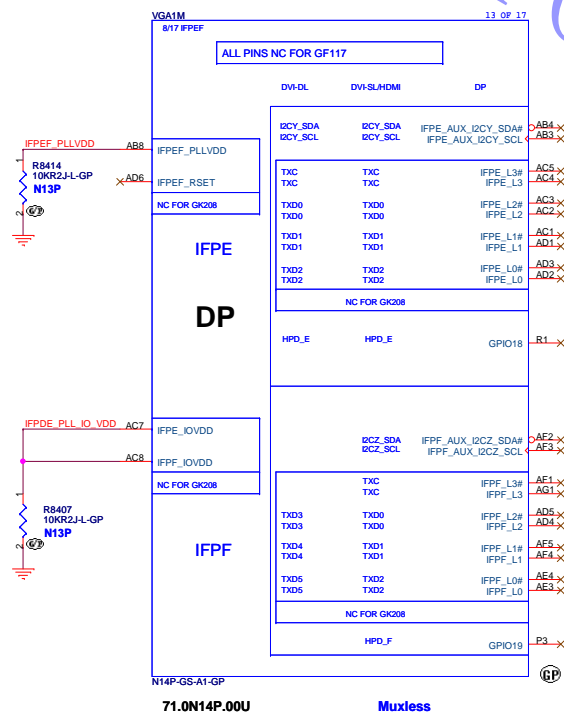
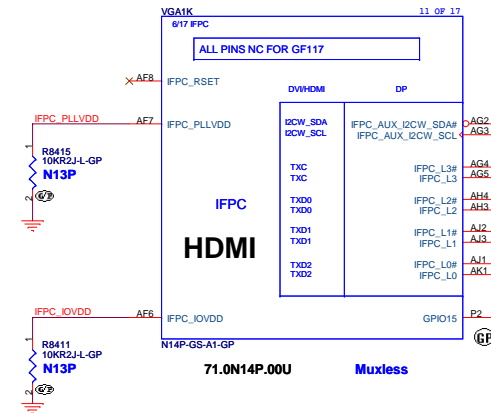
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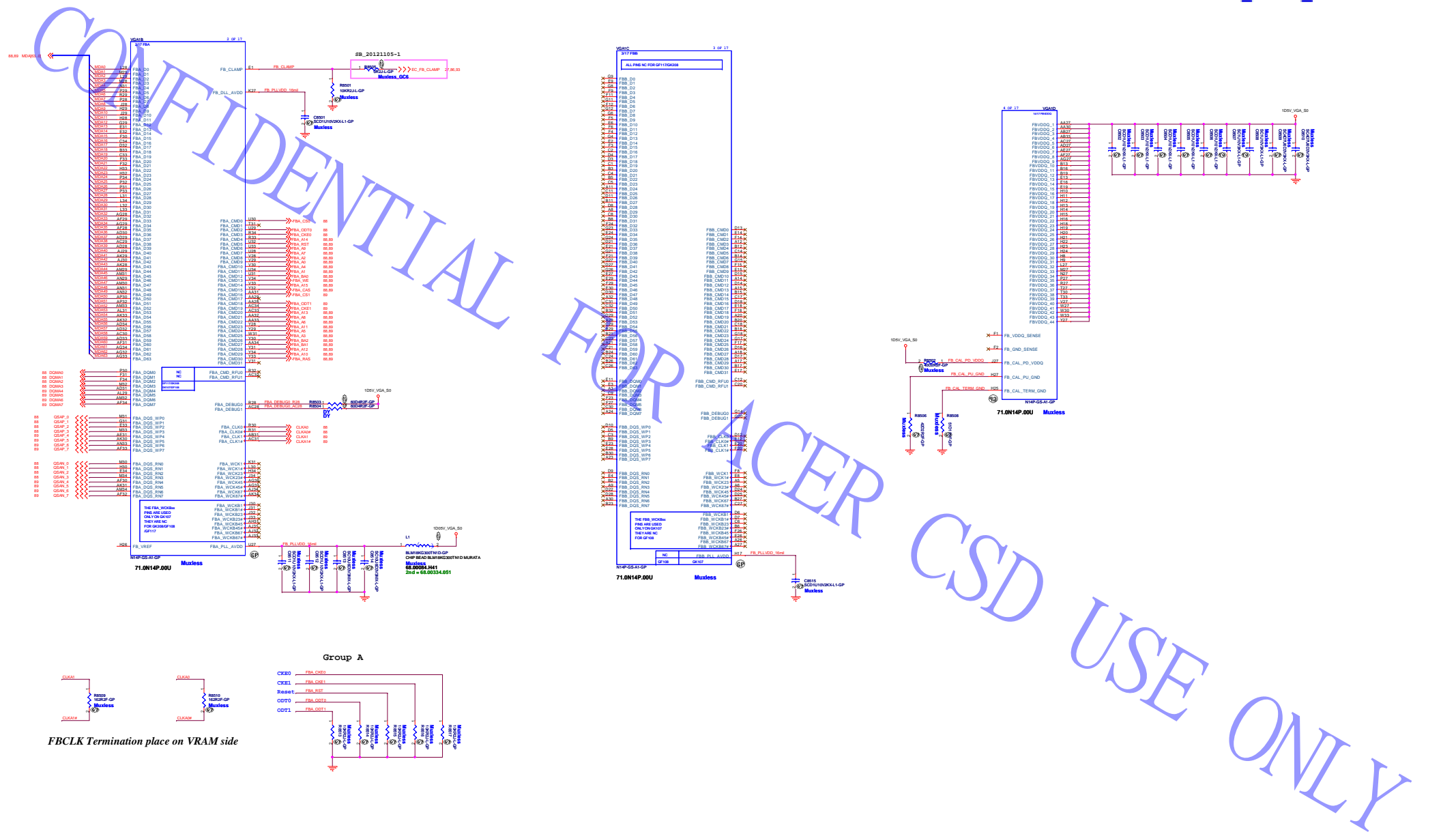
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|-----------------|-------------------------|-------------|-----|
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| Size<br>A2      | Document Number         | Rev         |     |
|                 | <b>EA40 CX</b>          | <b>-3</b>   |     |
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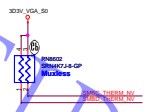
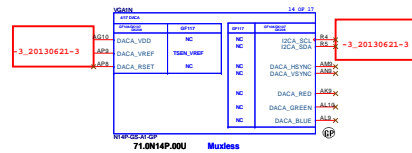


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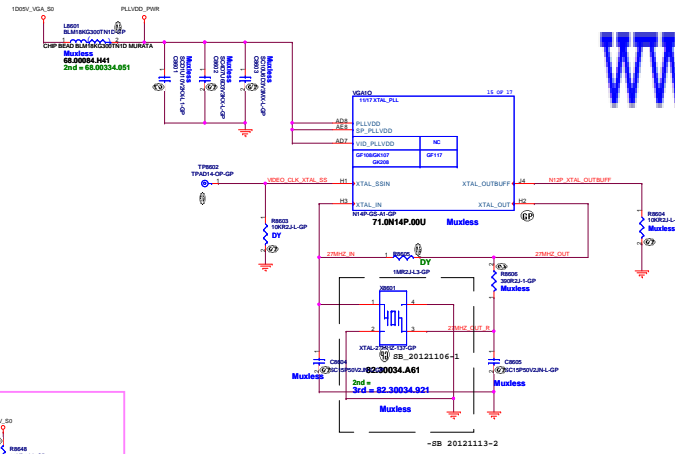
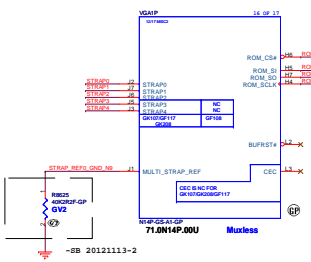
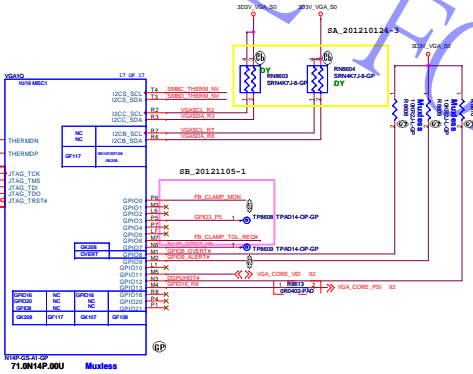
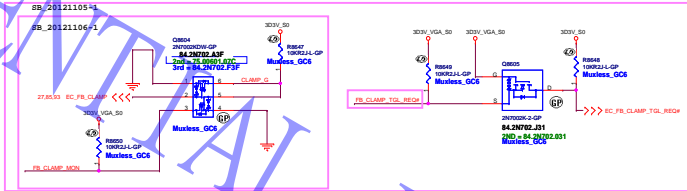
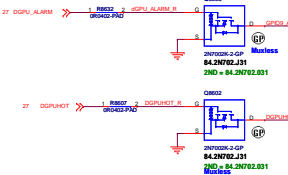


Table 113. Resistance Mapping to Hex Values

| Resistor Values | Pull-up to VDD33 | Pull-down to GND |
|-----------------|------------------|------------------|
| 4.99 k          | 1000             | 0000             |
| 10.0 k          | 1001             | 0001             |
| 15.0 k          | 1010             | 0010             |
| 20.0 k          | 1011             | 0011             |
| 24.9 k          | 1100             | 0100             |
| 30.1 k          | 1101             | 0101             |
| 34.8 k          | 1110             | 0110             |
| 45.3 k          | 1111             | 0111             |

4.99Kohm  
10Kohm  
15Kohm  
20Kohm  
24.9Kohm  
30.1Kohm  
34.8Kohm  
45Kohm

Table 1. N14M-GE/GL DDR3 Recommended Memories 128Mx16 Configuration

| Configuration | Vendor  | Strap | FBVDDQ / FBVDDQ2 | Manufacturer Part Number | Max Speed (MHz) | Memory Data Code Minimum | Status           |
|---------------|---------|-------|------------------|--------------------------|-----------------|--------------------------|------------------|
| 128Mx16 (GL)  | Samsung | 0x5   | 1.5 V / 1.5 V    | K4V2G1648E-BC1A          | 1000            | 1204                     | Production ready |
|               | Samsung | 0x5   | 1.5 V / 1.5 V    | K4V2G1648E-BC1A          | 1000            | 1204                     | Production ready |
|               | Hynix   | 0x6   | 1.5 V / 1.5 V    | H5TQ2G63DFR-11C          | 1000            | N/A                      | Production ready |
|               | Hynix   | 0x6   | 1.5 V / 1.5 V    | H5TQ2G63DFR-11C          | 1000            | N/A                      | Production ready |
|               | Hynix   | 0x6   | 1.5 V / 1.5 V    | H5TQ2G63DFR-11C          | 1000            | N/A                      | Production ready |

Table 2. N14M-GE/GL DDR3 Recommended Memories 256Mx16 Configuration

| Configuration | Vendor  | Strap | FBVDDQ / FBVDDQ2 | Manufacturer Part Number | Max Speed (MHz) | Memory Data Code Minimum | Status               |
|---------------|---------|-------|------------------|--------------------------|-----------------|--------------------------|----------------------|
| 256Mx16 (GL)  | Samsung | 0x6   | 1.5 V / 1.5 V    | K4V4G1648E-BC1A          | 900             | N/A                      | Production ready     |
|               | Micron  | 0x0   | 1.5 V / 1.5 V    | AT41H256M16HA-107GE      | 900             | N/A                      | Production ready     |
|               | Hynix   | 0x3   | 1.5 V / 1.5 V    | H5TQ4G63MFR-11C          | 900             | N/A                      | Production ready     |
|               | Hynix   | 0x4   | 1.5 V / 1.5 V    | H5TQ4G63AFR-11C          | N/A             | N/A                      | Production Candidate |

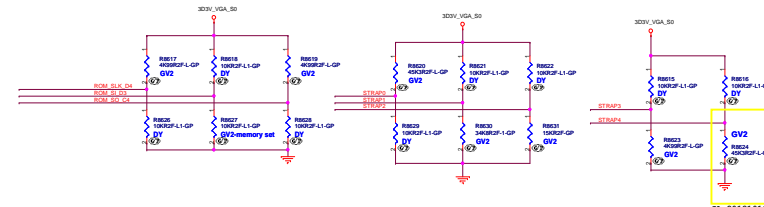
N14M-GE use Binary Strap. Please see the below information.

Table 122 Binary Strap Mode Mapping

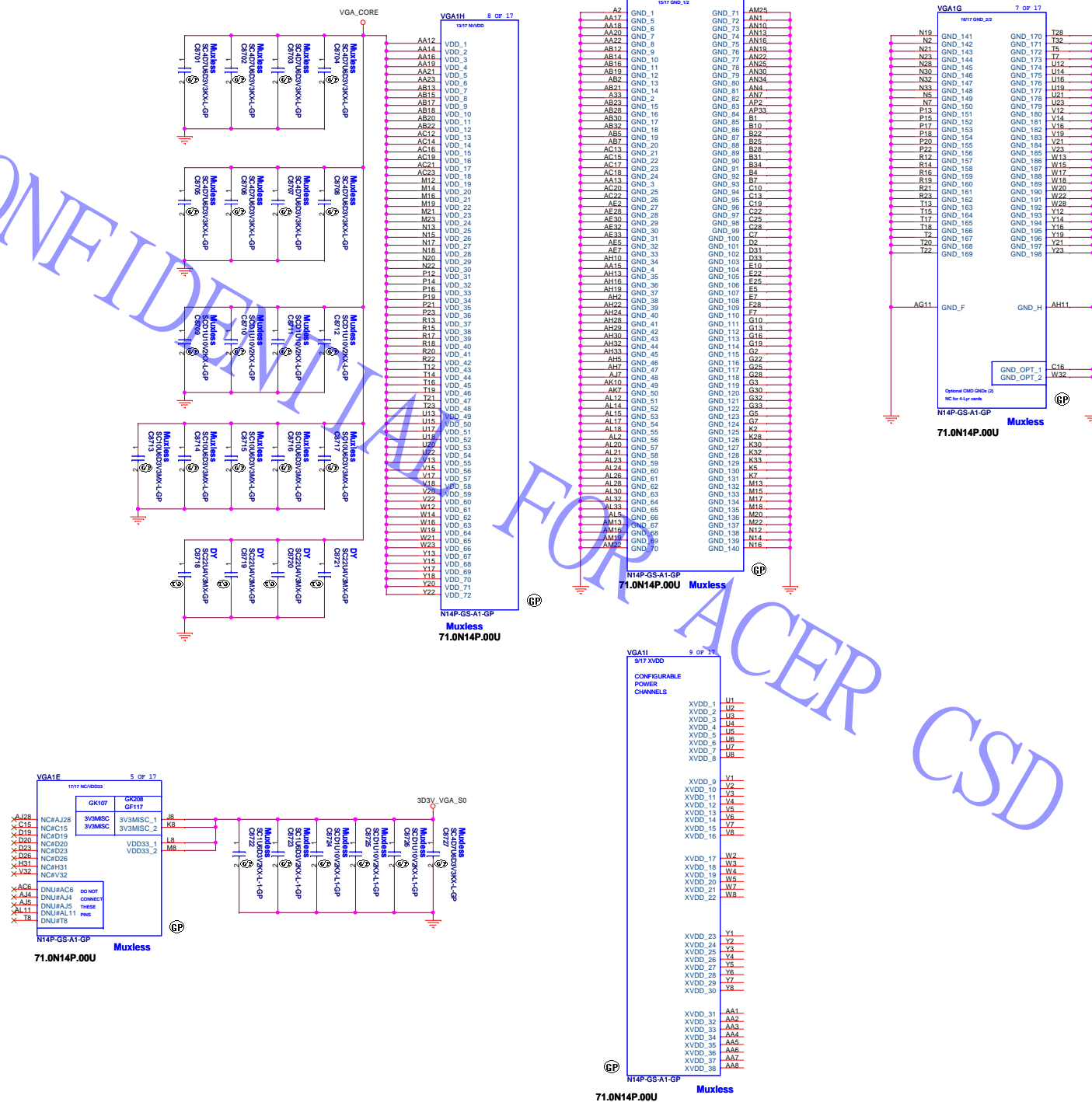
| Strap Pin Name | Strap Mapping  | Resistance | Polarity   |
|----------------|----------------|------------|--|
| ROM_SCLK       | SMB_ALT_ADDR   | 10k Ω      | Pull-down to GND   |
| ROM_SI         | SMB_VENDOR     | 10k Ω      | Pull-up to 3V3 if VBIOS ROM exists<br>Pull-down to GND if no VBIOS ROM |
| ROM_SO         | VGA_DEVICE     | 10k Ω      | Pull-down to GND (no display)  |
| STRAP0         | RAM_CFG[0]     | 10k Ω      | See Note below   |
| STRAP1         | RAM_CFG[1]     | 10k Ω      | See Note below   |
| STRAP2         | RAM_CFG[2]     | 10k Ω      | See Note below   |
| STRAP3         | RAM_CFG[3]     | 10k Ω      | See Note below   |
| STRAP4         | PCIE_MAX_SPEED | 10k Ω      | Pull-down to GND   |

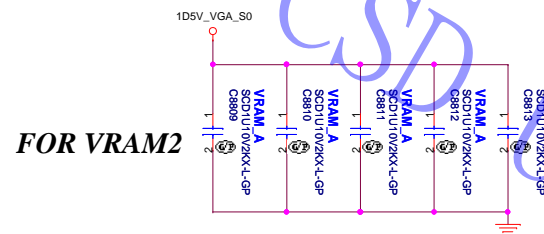
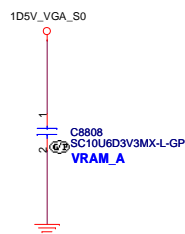
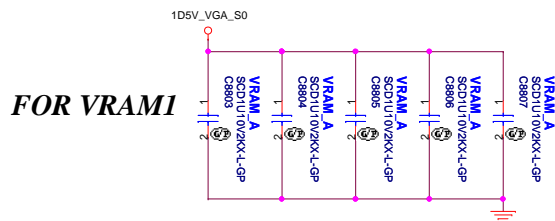
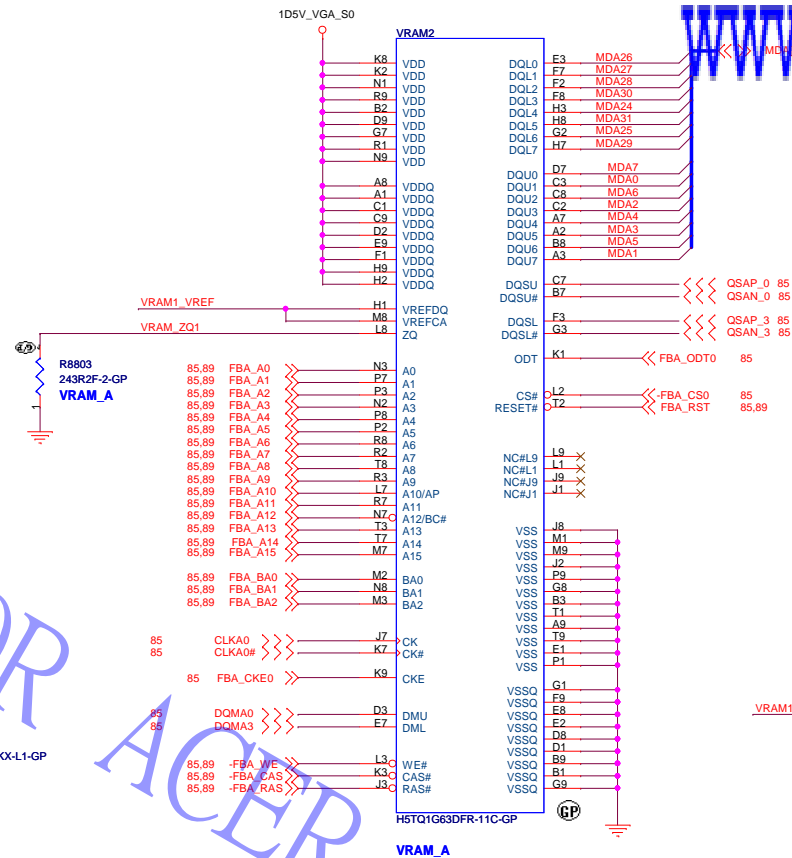
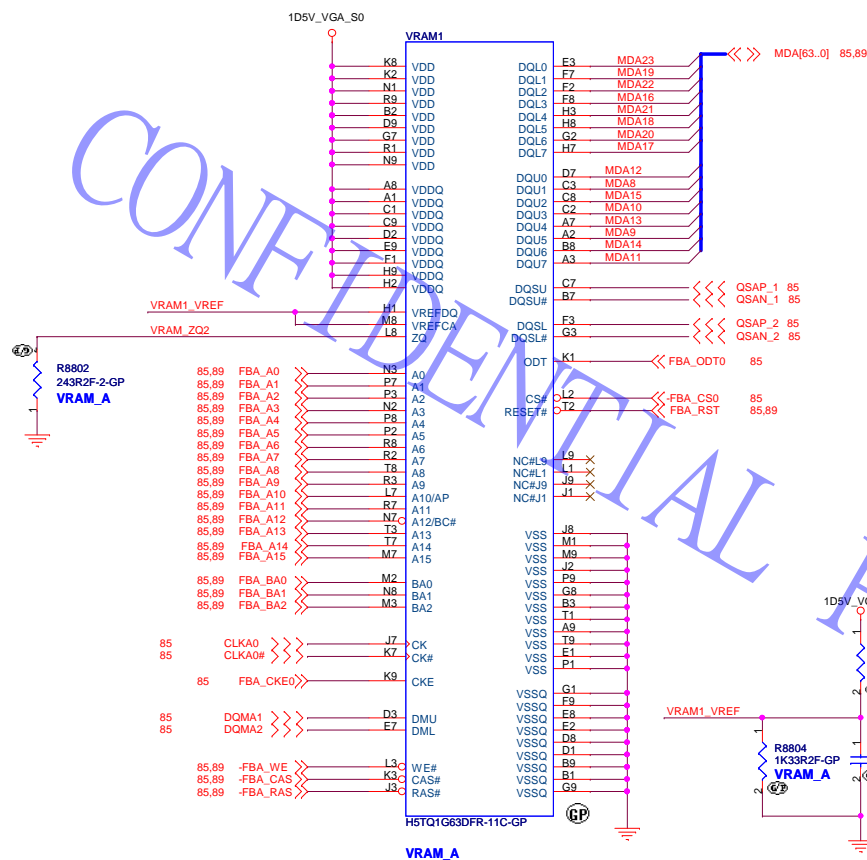
| N14P-GV2 Strap Pin Name | Logical Strapping Bit3 | Logical Strapping Bit2 | Logical Strapping Bit1 | Logical Strapping Bit0 |
|-------------------------|------------------------|------------------------|------------------------|------------------------|
| ROM_SCLK                | PCI_DEVID[4]           | SMB_VENDOR             | PCI_DEVID[5]           | PEX_PLL_EN_TERM        |
| ROM_SI                  | RAM_CFG[3]             | RAM_CFG[2]             | RAM_CFG[1]             | RAM_CFG[0]             |
| ROM_SO                  | FB[1]                  | FB[0]                  | SMB_ALT_ADDR           | VGA_DEVICE             |
| STRAP 0                 | USER[3]                | USER[2]                | USER[1]                | USER[0]                |
| STRAP 1                 | 3GIO_PADCFG[3]         | 3GIO_PADCFG[2]         | 3GIO_PADCFG[1]         | 3GIO_PADCFG[0]         |
| STRAP 2                 | PCI_DEVID[3]           | PCI_DEVID[2]           | PCI_DEVID[1]           | PCI_DEVID[0]           |
| STRAP 3                 | SOR3_EXPOSED           | SOR2_EXPOSED           | SOR1_EXPOSED           | SOR0_EXPOSED           |
| STRAP 4                 | RESERVED               | PCIE_SPEED_CHANGE_GEN3 | PCIE_MAX_SPEED         | DP_PLL_VDD33V          |

|               |        |      |                   |      |                   |
|---------------|--------|------|-------------------|------|-------------------|
| N14P-GT1-A2   | 0x0FE4 | 0010 | 15K ohm pull-down | 0100 | 25K ohm pull-down |
| N14P-GV2-B-A1 | 0x1292 | 1000 | 5K ohm pull-up    | 0010 | 15K ohm pull-down |



N14M-GE+Micron 4Gb  
Strap3|Strap2|Strap1|Strap0  
1 1 0 1





***FOR VRAM1***

***FOR VRAM2***

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| Title                    |                         |           |           |
| <b>GPU-VRAM1,2 (1/4)</b> |                         |           |           |
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| Custom                   | <b>EA40_CX</b>          | <b>-3</b> |           |
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| GPU-VRAM5,6 (3/4)  |                         |  |                     |  |                 |
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| Custom   | EA40 CX                 |  |                     |  | -3              |
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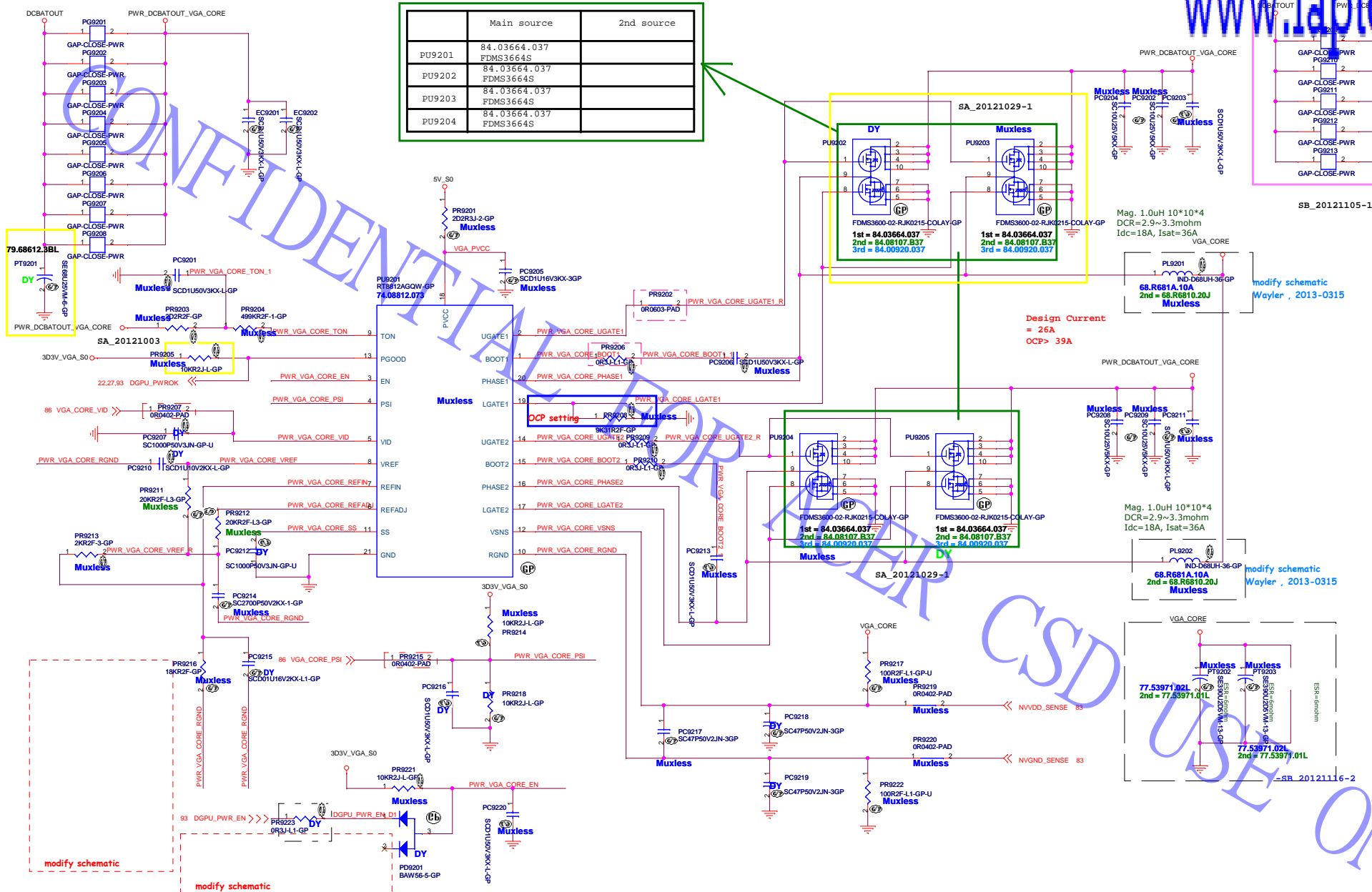
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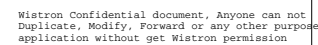
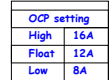
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| GPU-VRAM7,8 (4/4)             |                 |  |        |
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| Size<br>Custom                | Document Number<br><b>EA40 CX</b> | Rev<br><b>-3</b> |
| Date<br>Friday, June 21, 2013 | Sheet<br>92 of                    | 103              |



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| Title <div>LVDS Switch</div>   |                                    |                                       |
| Size <div>A4</div>   | Document Number <div>EA40 CX</div> | Rev <div>-3</div>                     |
| Date <div>Thursday, June 06, 2013</div>  |                                    | Sheet <div>94</div> of <div>103</div> |

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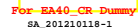
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| CRT Switch |                         |  |                 |
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| A3         | EA40_CX                 |  | -3              |
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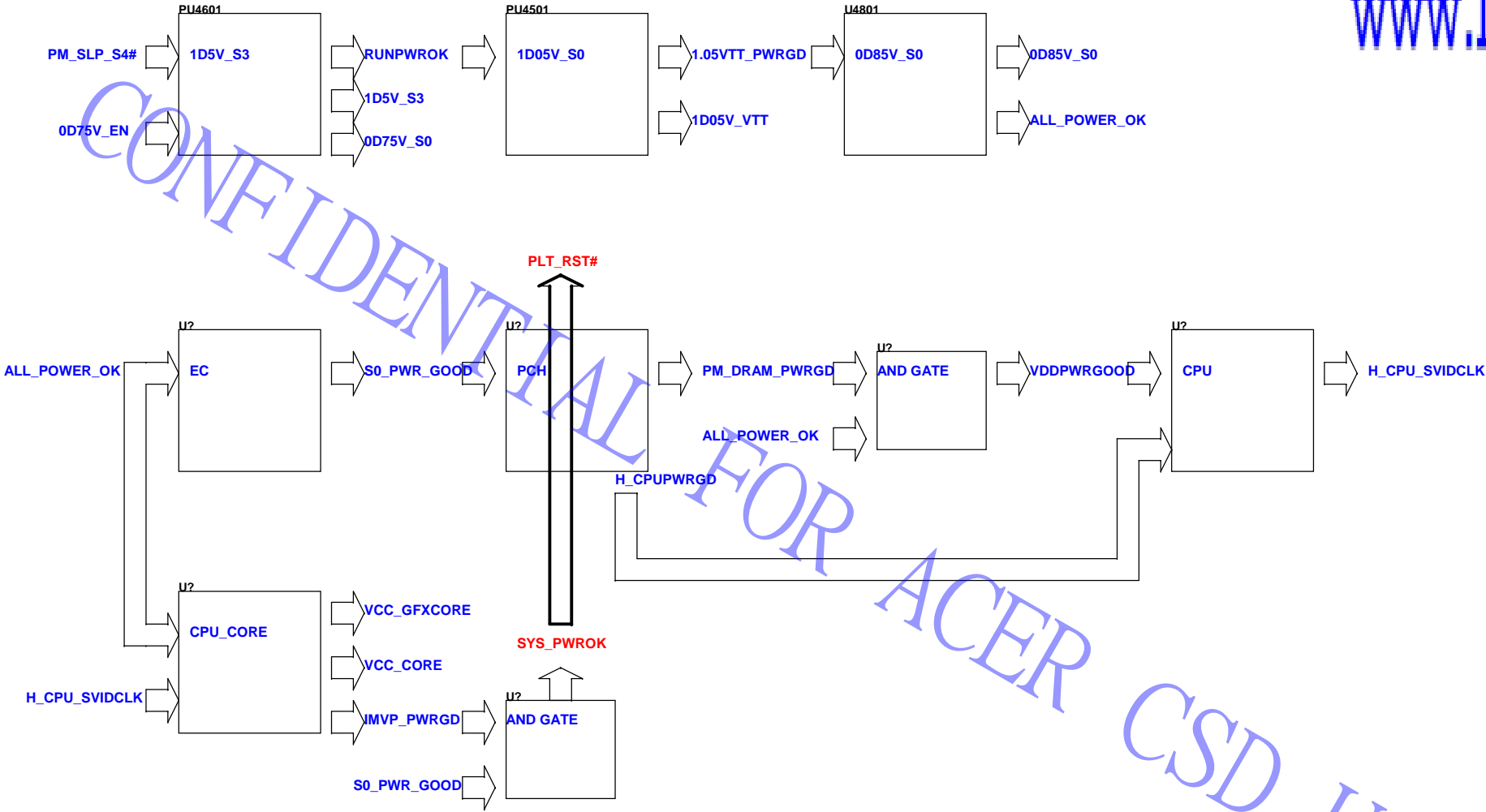
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Date: Thursday, June 20, 2013

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Power Sequence

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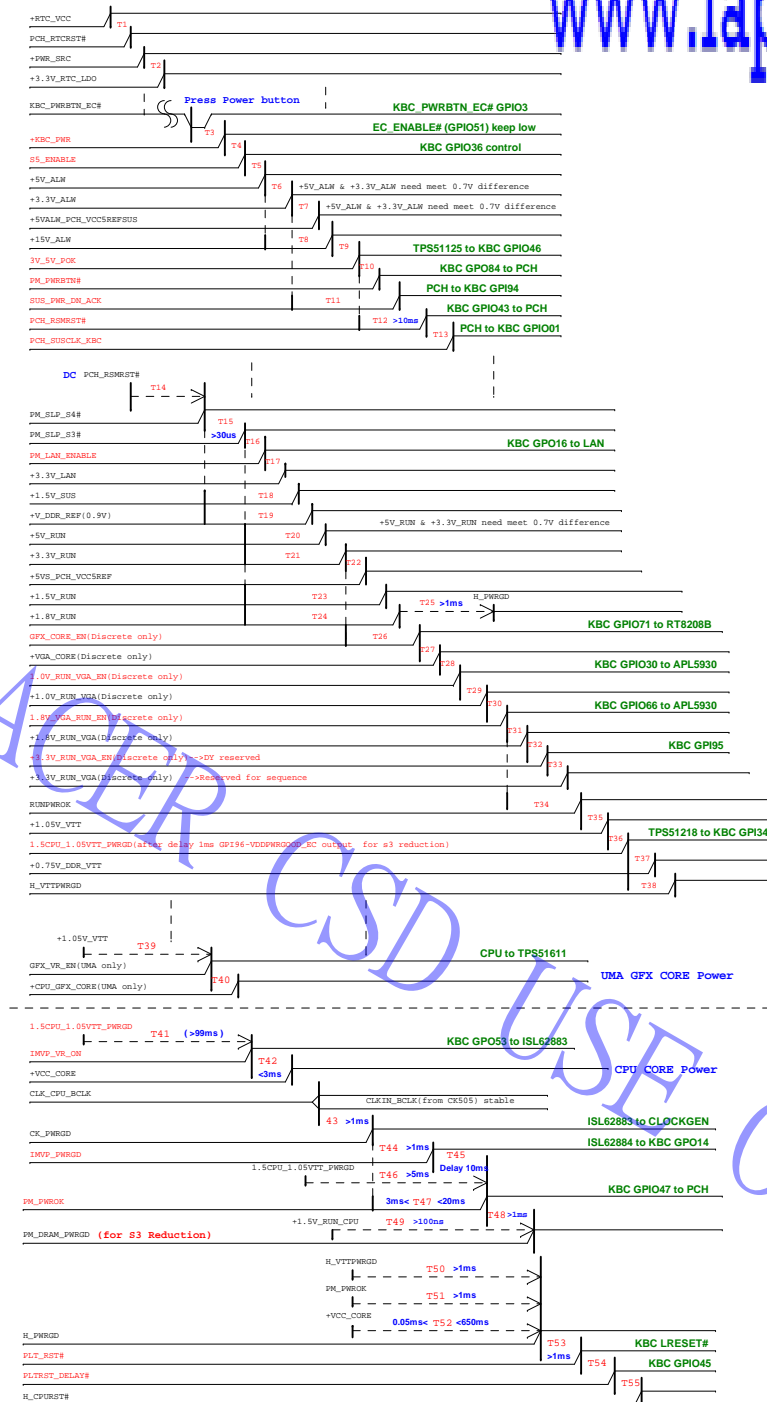
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| Date: Thursday, June 06, 2013  | EA40_CX         | Sheet 98 of 103  |    |

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[illegible]

red word: KBC GPIO

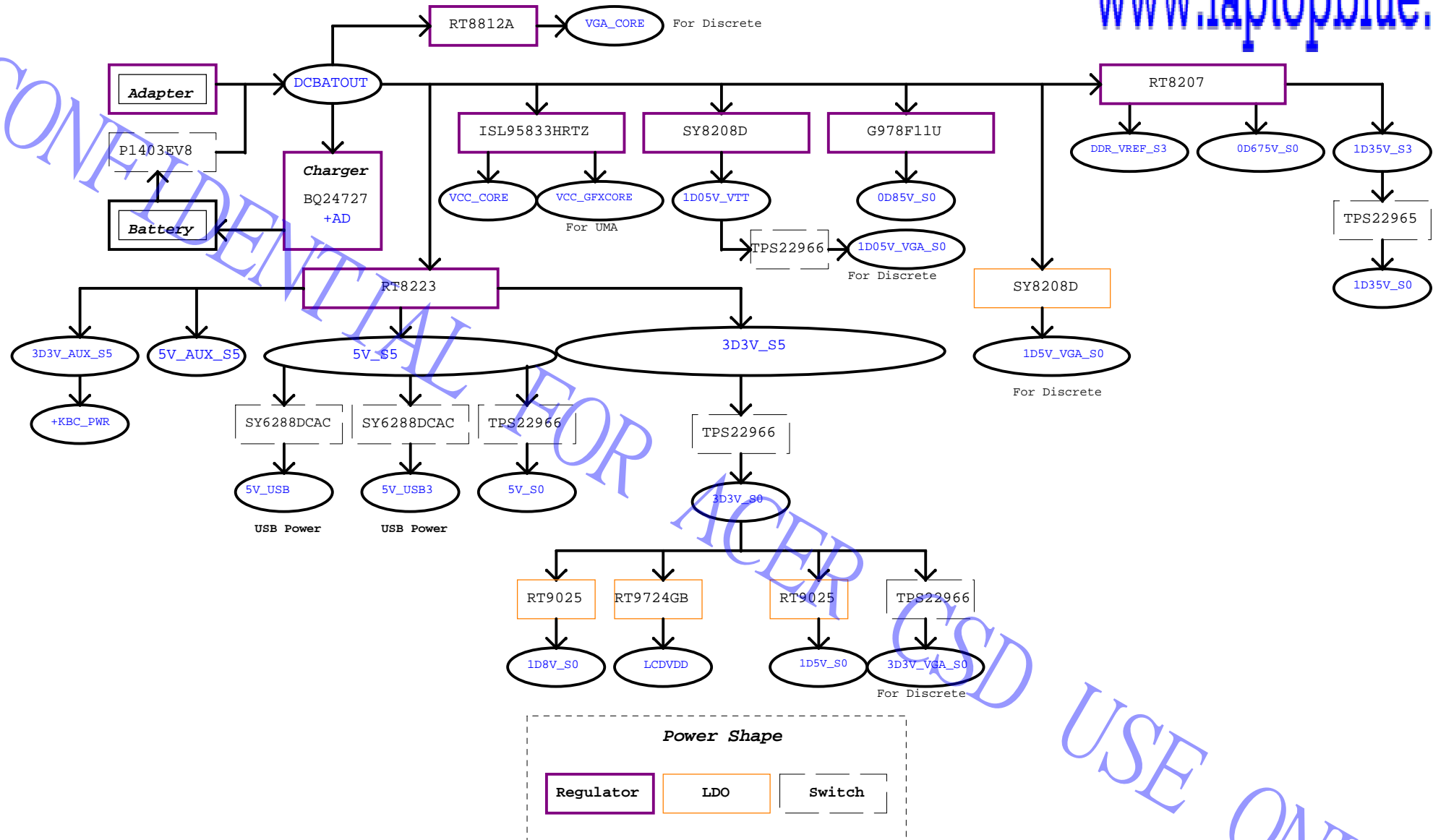


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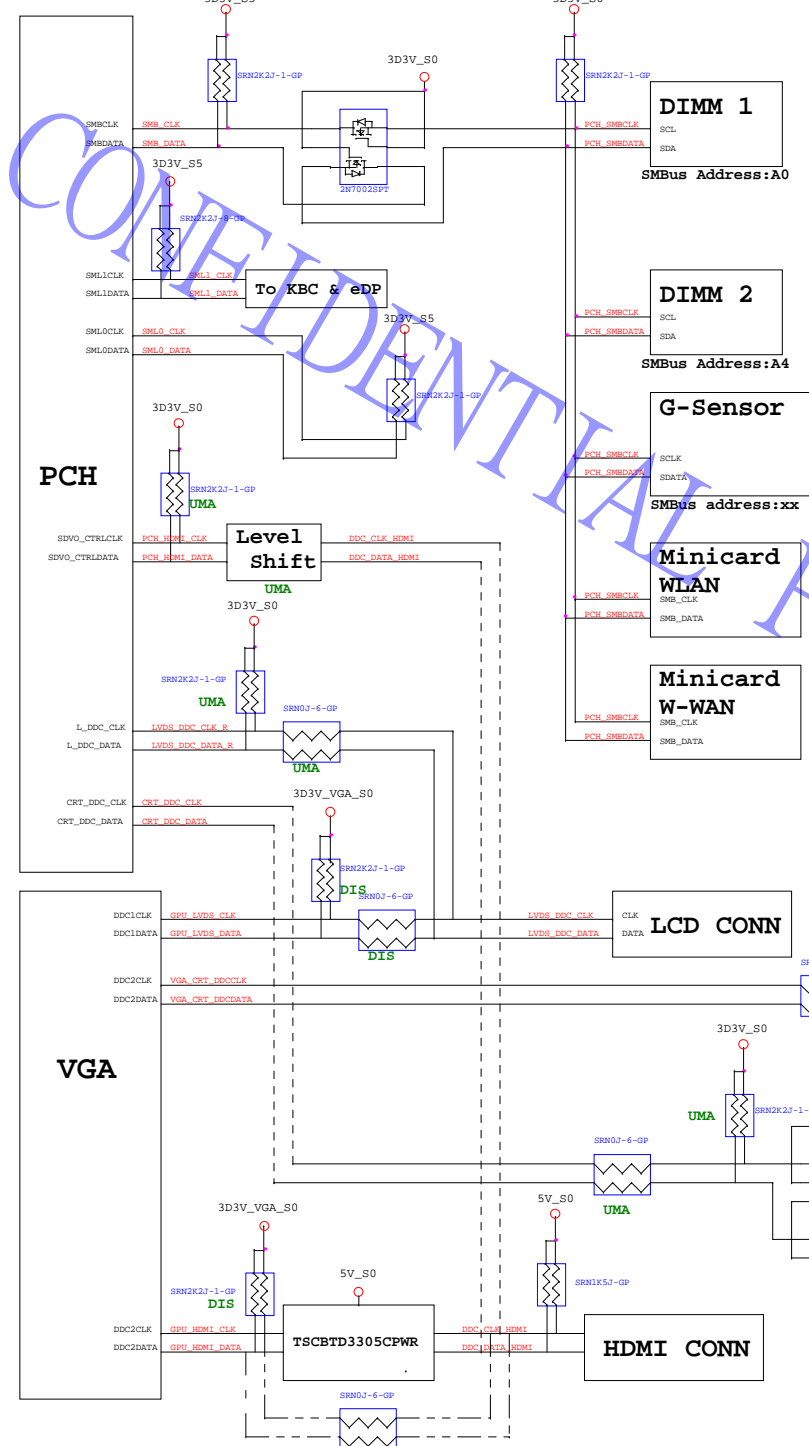


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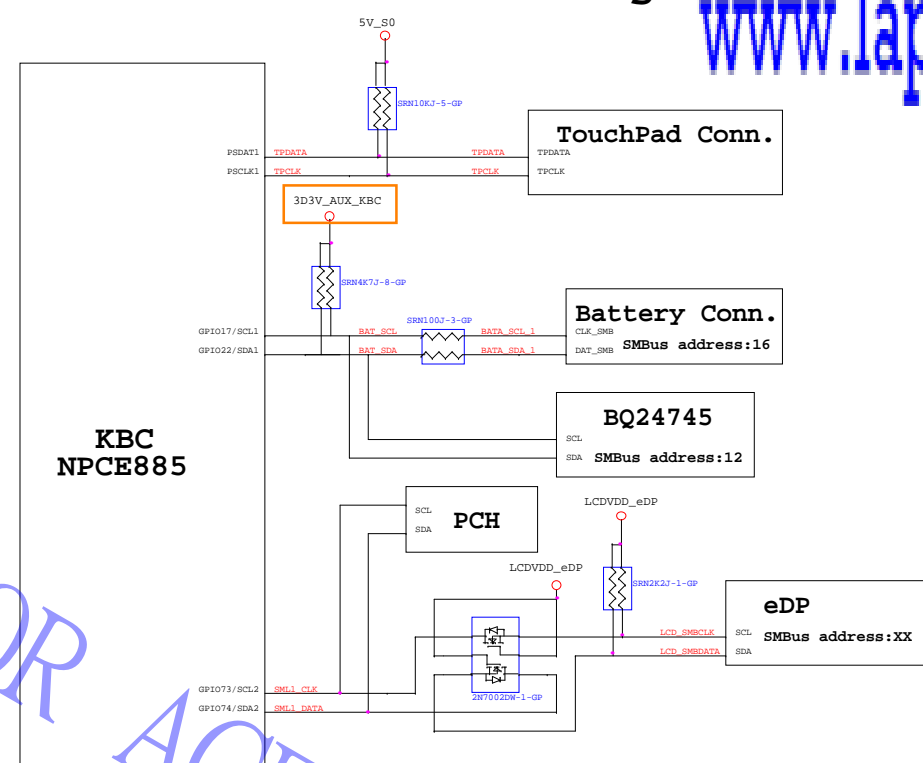
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| <b>Title</b><br><b>Power Block Diagram</b>  |  |
| <b>Size</b><br>A3   | <b>Document Number</b><br><b>EA40 CX</b> |
| <b>Date:</b> Thursday, June 06, 2013  | <b>Rev</b><br><b>-3</b>                  |
| <b>Sheet</b> 100  | <b>of</b> 103                            |

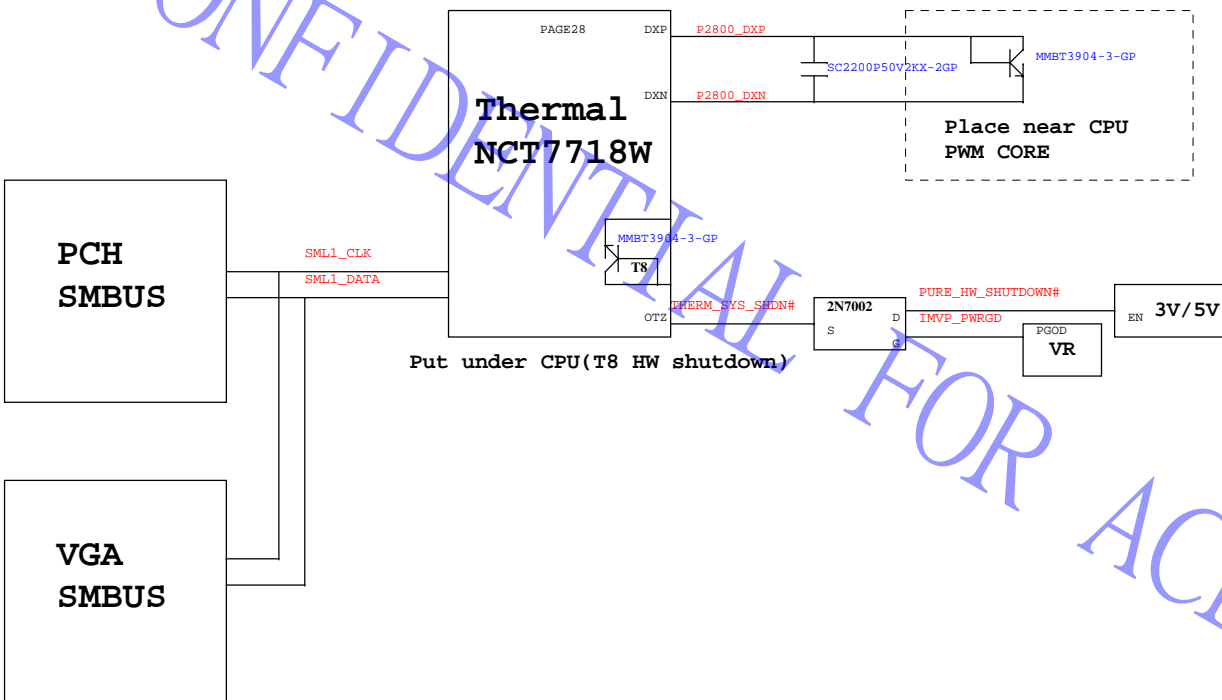
PCH SMBus Block Diagram



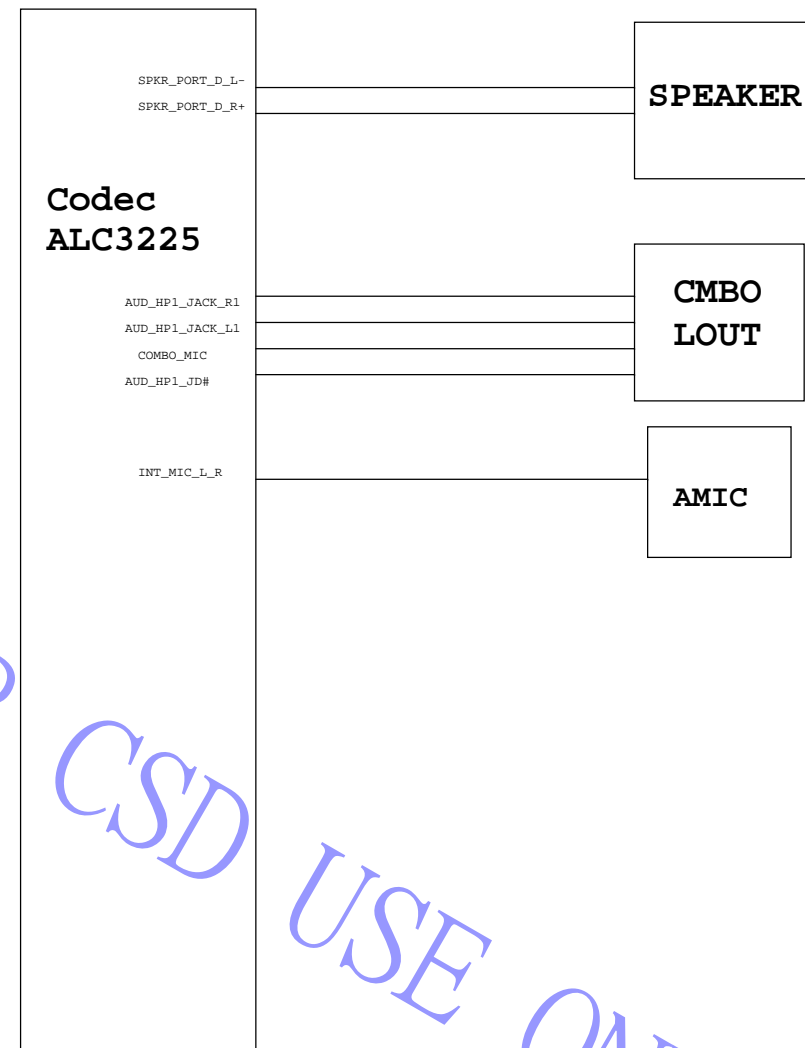
KBC SMBus Block Diagram



## Thermal Block Diagram



*Audio Block Diagram*



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| USB charger                   |                 |  |     |
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