Merom / Crestline / ICH8-M

Docking(RQ7)
USB (USB4)
1394 X1
LAN 10/100/1G
MODEM
Audio/Spdif JACK
CRT/S-Video
Parallel/Serial Port
DVI Port
PS2 Port *2
Battery Charger
PG 40

14.318MHz
CLOCK GEN
ICS9LPRS365
64pins
PG 2

Merom
(478 Micro-FCPGA)
PG 3,4

CPU THERMAL SENSOR
PG 3

VIDEO RAM *4
DDRII
PG 23,24

FSB
667/800 MHz

DVI

DVI / 7307 Chrontel
PG 41

SDVO

DDRII-SODIMM1
PG12, 13

DDRII 533/667 MHz

DDRII-SODIMM2
PG 12,13

DDRII 533/667 MHz

Crestline
1299 uFCBGA
PG 5,6,7,8,9,10,11

DMI LINK
4X PCI-E

PCI-EXPRESS

27MHz

64bit/256MB

ATI
M71-s/M72-s
PG 18,19,20,21,22

DVI

LCD Panel
PG 25

CRT
PG 26

S-Video
PG 26

FOR Crestline (LCD/CRT/S-VIDEO)

FINGER PRINT
USB8
PG 38

Bluetooth
USB6
PG 36

USB PORT X 4
USB0~1 PG 35
USB2~3 PG 31

32.768KHz

ICH8-M
676 BGA
PG14,15,16,17

33MHZ, 3.3V PCI

PCI-E

Azalia

WIRE

24.576MHz

Modularity
PATA ODD/HDD
SATA HDD
AUX Battery
USB FDD (USB5)
PG 34

PATA

2nd SATA

Internal HDD
PG 34

1st

MDC Module 1.5
PG 32

Azalia
STAC9200
PG 31

Intel 82566
PG 27

MINI PCI-E Card * 2
USB7
USB9
PG 33

CARDBUS / IEEE 1394 CONTROLLER/CF
PCI7612
PG 29

25MHz

Amplifier
MAX9789A
PG 31

SIM Card
PG 33

Smart Card
PG 30

4 IN 1
CARD READER
SD/MMC, MS,XD
PG 30

CARDBUS SLOT X1
PG 29

1394 CONN
PG 29

LPC

32.768KHz

TPM
PG 38

IT8512
LQFP 128
PG 37

SIO PC87383
PG 39

RJ11 JACK
PG 28

JACK
HEADPHONE,
2ND HEADPHONE,
MIC
PG 31

RJ45 JACK
PG 28

Audio Board

FAN
PG 3

Touchpad
PG 38

Keyboard
PG 38

SPI FLASH
PG 37

MAX1993 VGACORE (1.1V/1.2V) PG 53

2.5V PG 52

SYSTEM POWER(3/5V) PG 51

CPU CORE POWER ISL6262A PG 50

+1.5V PG 49

+1.05V/+1.25V PG 48

+1.8VSUS/+0.9V PG 47

CHARGER MAX8724 & SELECTER PG 45,46

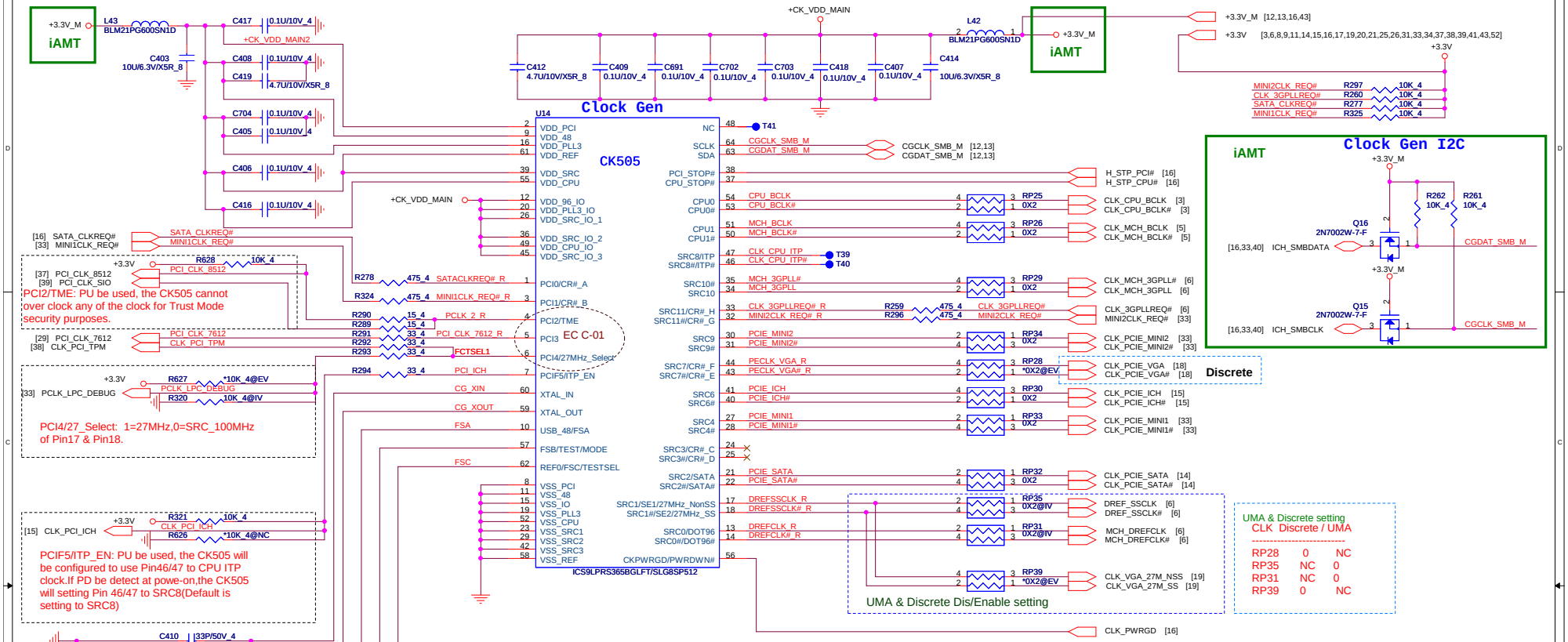
DISCHARGE PG 44

PCI DEVICES IRQ ROUTING

DEVICE	IDSEL #	REQ/GNT #	PCI_INT
CardBus/1394	AD25	0	A,B,C,D

PROJECT : NA1
Quanta Computer Inc.

Size	Document Number	Rev
	01 -- Block Diagram	2A
Date: Friday, March 23, 2007	Sheet 1 of 55	



CPU Clock select

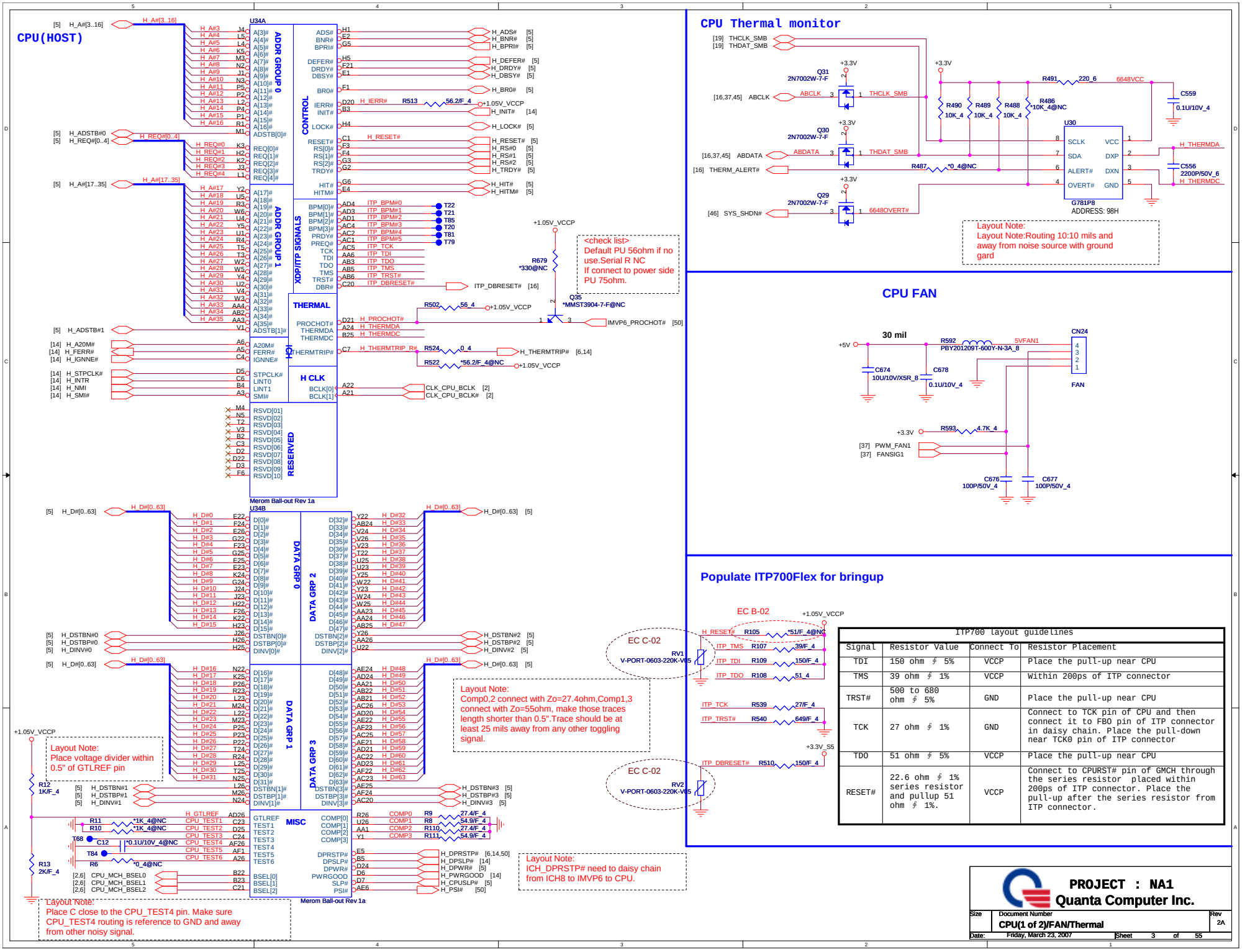
FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

GCLK_SEL = FCTSEL1

FCTSEL1 (PIN6)	PIN13	PIN14	PIN17	PIN18
0=UMA	DOT96T	DOT96C	SRCT1/LCDT_100	SRCC1/LCDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS

PROJECT : NA1
Quanta Computer Inc.

Size	Document Number	Rev
	Clock Gen	2A
Date: Friday, March 23, 2007	Sheet 2 of 55	



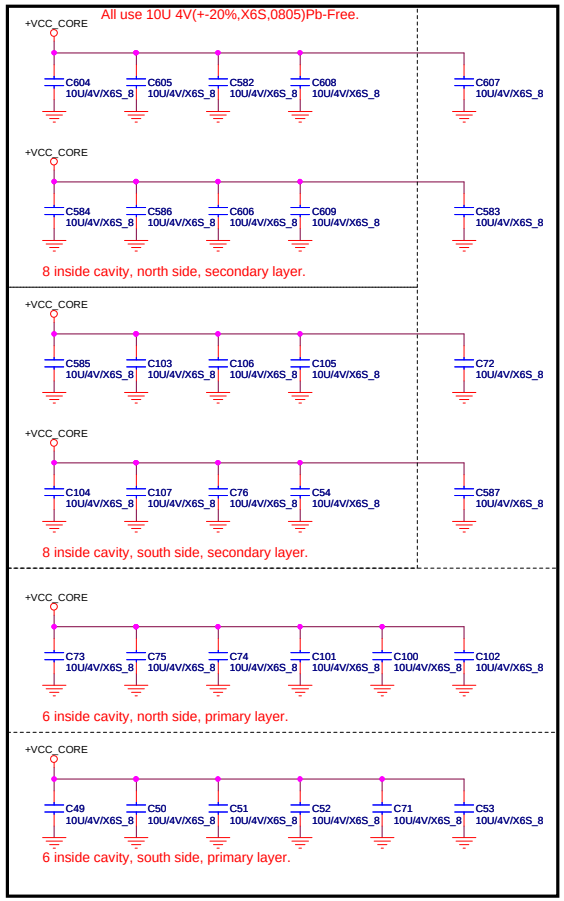
ITP700 layout guidelines

Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm ± 5%	VCCP	Place the pull-up near CPU
TMS	39 ohm ± 1%	VCCP	Within 200ps of ITP connector
TRST#	500 to 680 ohm ± 5%	GND	Place the pull-up near CPU
TCK	27 ohm ± 1%	GND	Connect to TCK pin of CPU and then connect it to FBO pin of ITP connector in daisy chain. Place the pull-down near TCK0 pin of ITP connector
TDO	51 ohm ± 5%	VCCP	Place the pull-up near CPU
RESET#	22.6 ohm ± 1% series resistor and pullup 51 ohm ± 1%.	VCCP	Connect to CPURST# pin of GMCH through the series resistor placed within 200ps of ITP connector. Place the pull-up after the series resistor from ITP connector.

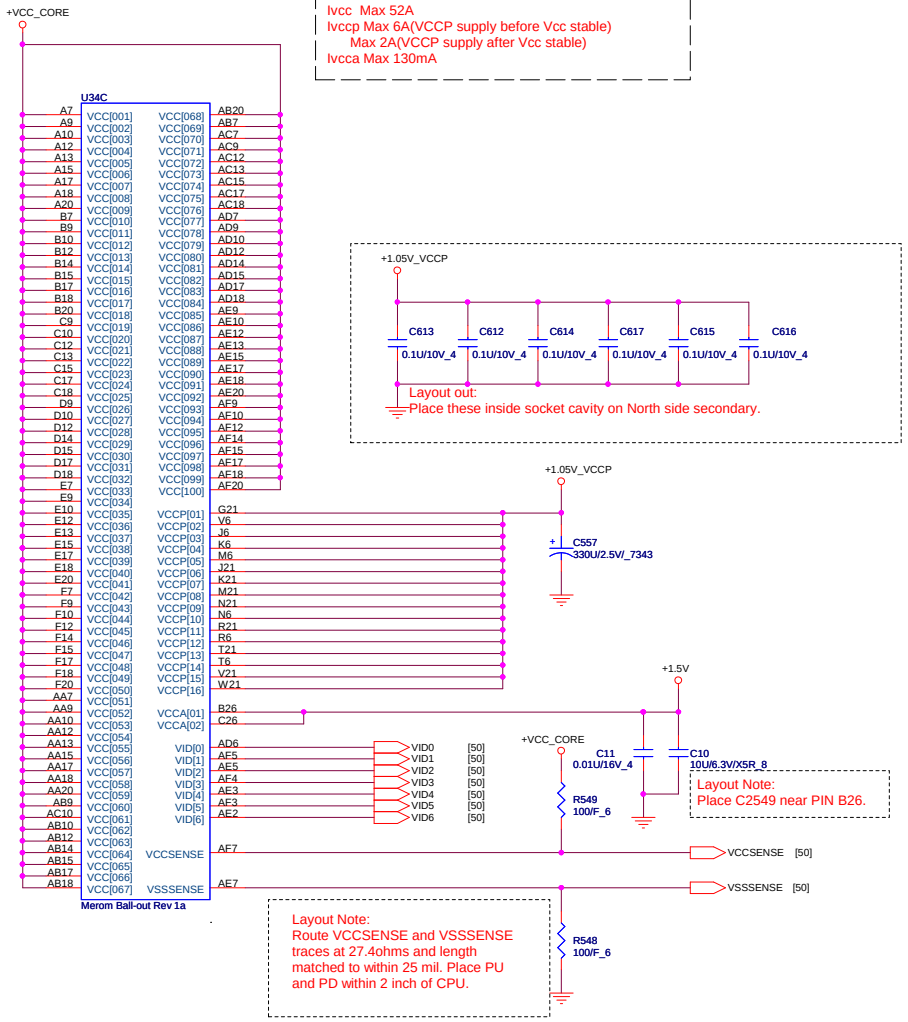
PROJECT : NA1
Quanta Computer Inc.

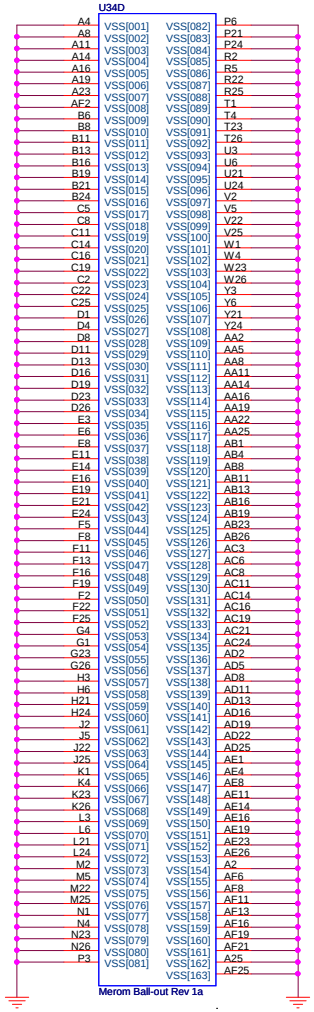
Size	Document Number	Rev
	CPU(1 of 2)/FAN/Thermal	2A
Date: Friday, March 23, 2007	Sheet 3 of 55	

CPU(Power)



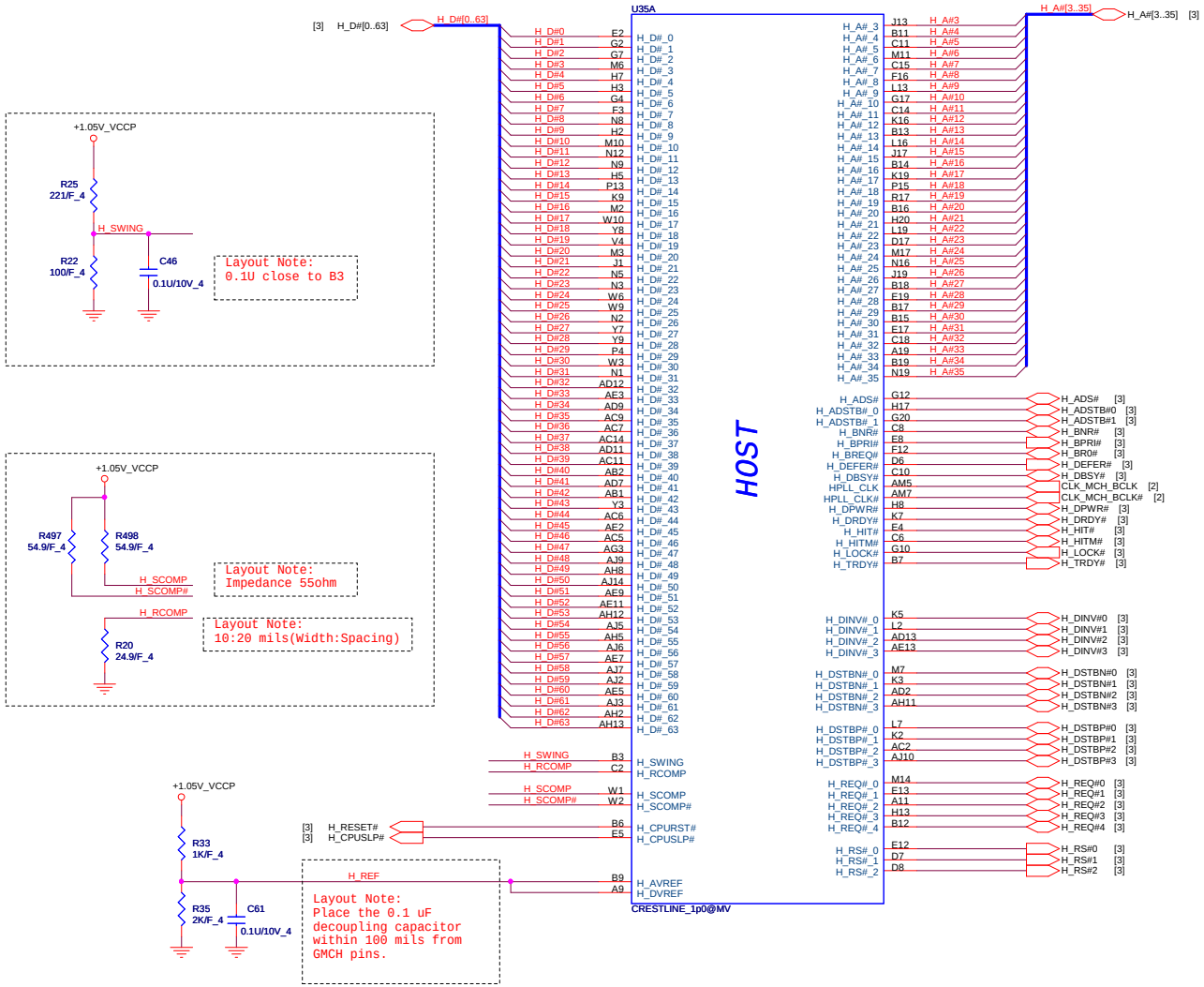
<REV.NO. 0.5/REF.NO.19343>
Ivcc Max 52A
Ivccp Max 6A(VCCP supply before Vcc stable)
Max 2A(VCCP supply after Vcc stable)
Ivcca Max 130mA





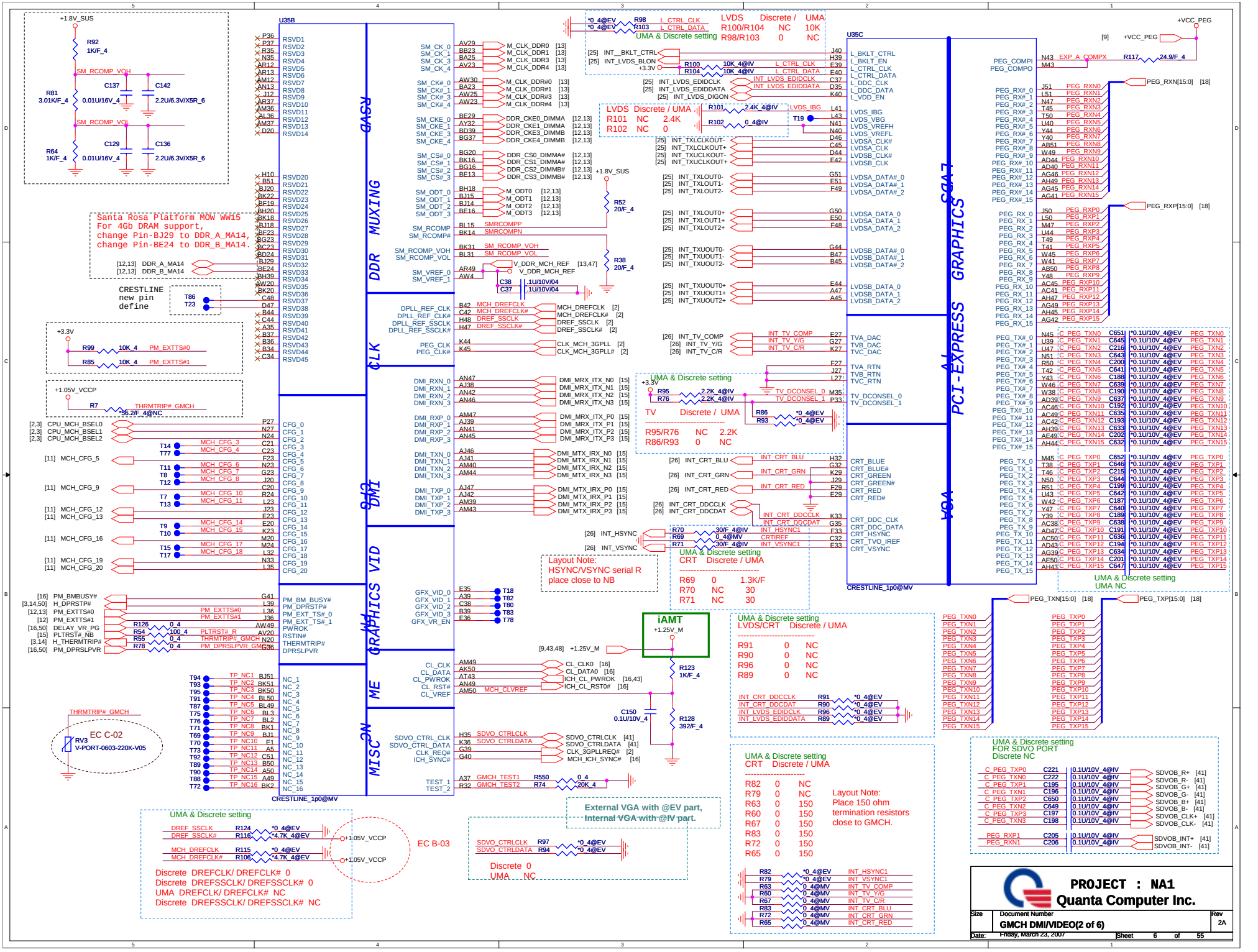
PROJECT : NA1		
Quanta Computer Inc.		
Size	Document Number: CPU(2 of 2)	Rev: 1A
Date: Friday, March 23, 2007	Sheet 4 of 55	

NB(HOST)

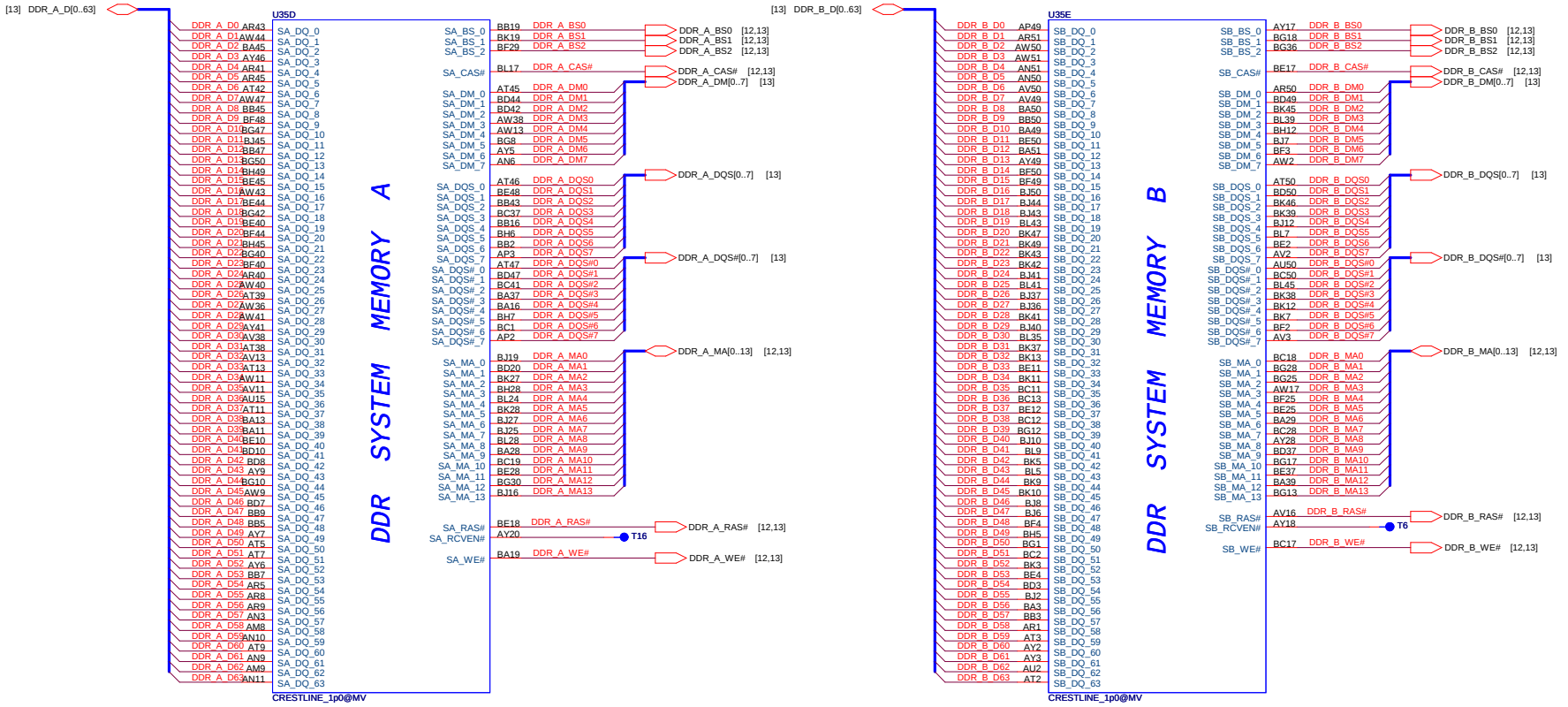


PROJECT : NA1
Quanta Computer Inc.

Size	Document Number	Rev
	GMCH HOST(1 of 6)	C
Date: Friday, March 23, 2007	Sheet 5 of 55	



NB(Memory controller)

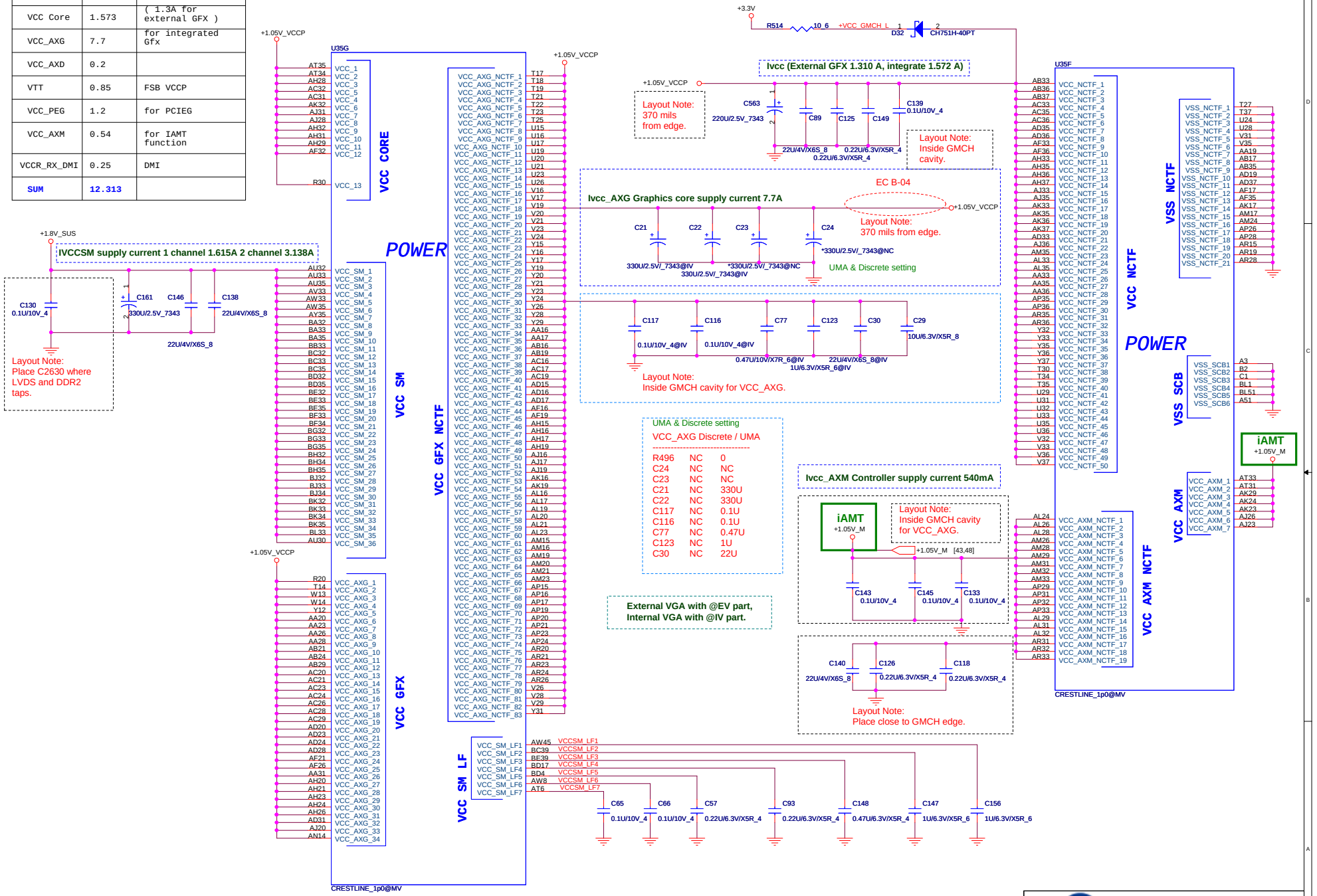


<OrgName>
<OrgAddr1>
<OrgAddr2>
<OrgAddr3>
<OrgAddr4>
Quanta Computer Inc.

PROJECT : NA1

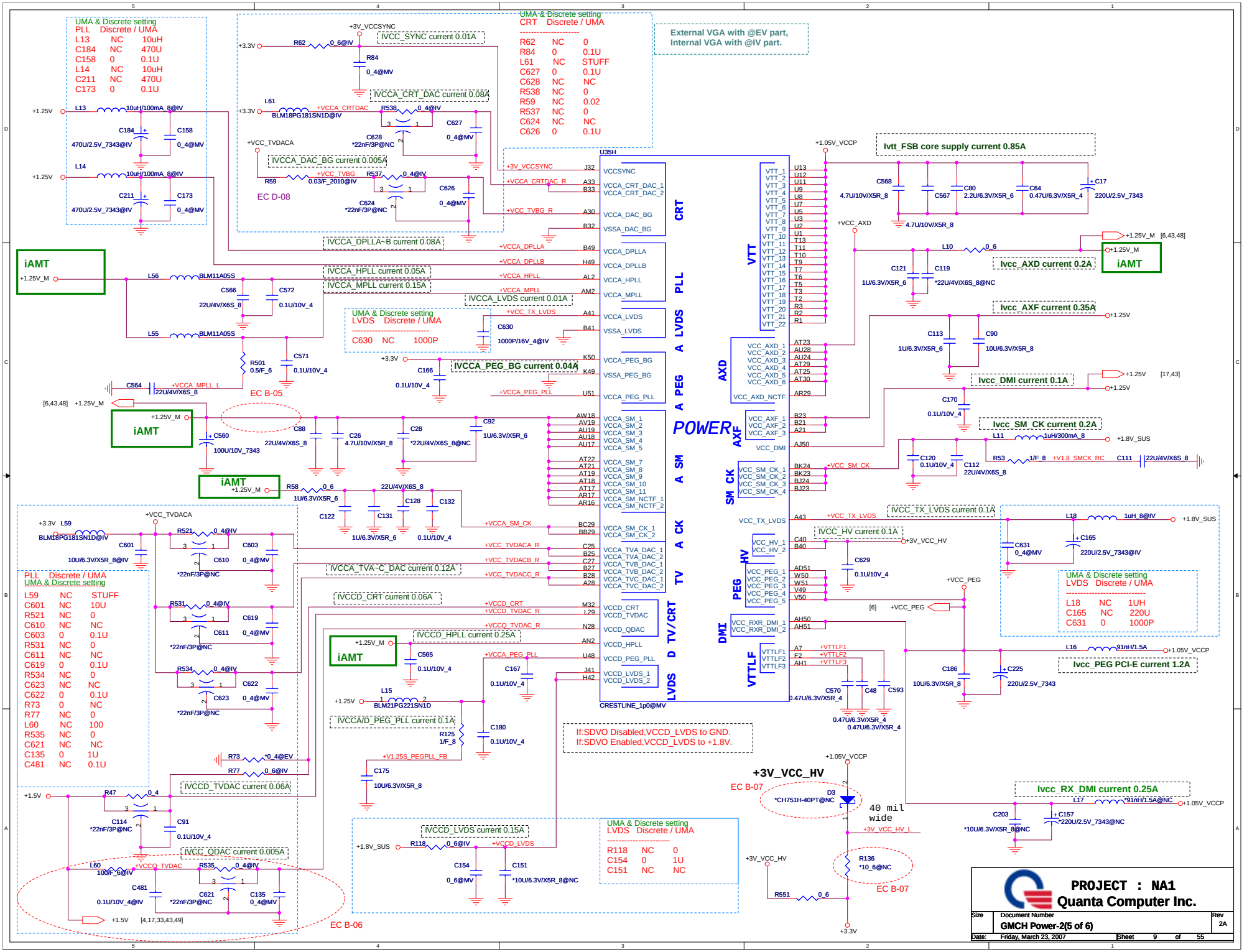
Size	Document Number	Rev
	GMCH DDR/Strap(3 of 6)	1A
Date: Friday, March 23, 2007	Sheet 7 of 55	

GMCH 1.05V	current(A)	Remark
VCC Core	1.573	(1.3A for external GFX)
VCC_AXG	7.7	for integrated Gfx
VCC_AXD	0.2	
VTT	0.85	FSB VCCP
VCC_PEG	1.2	for PCIEG
VCC_AXM	0.54	for IAMT function
VCCR_RX_DMI	0.25	DMI
SUM	**12.313**	

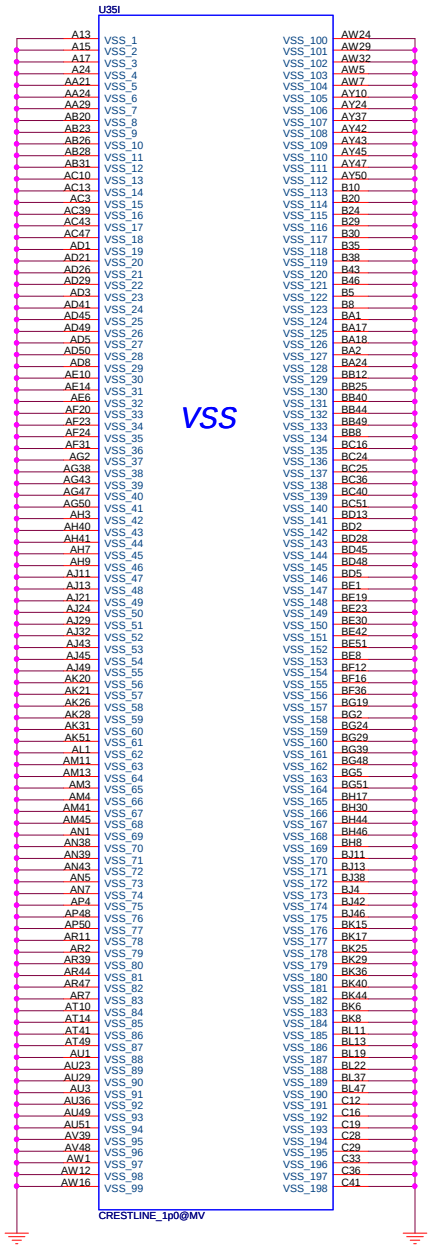


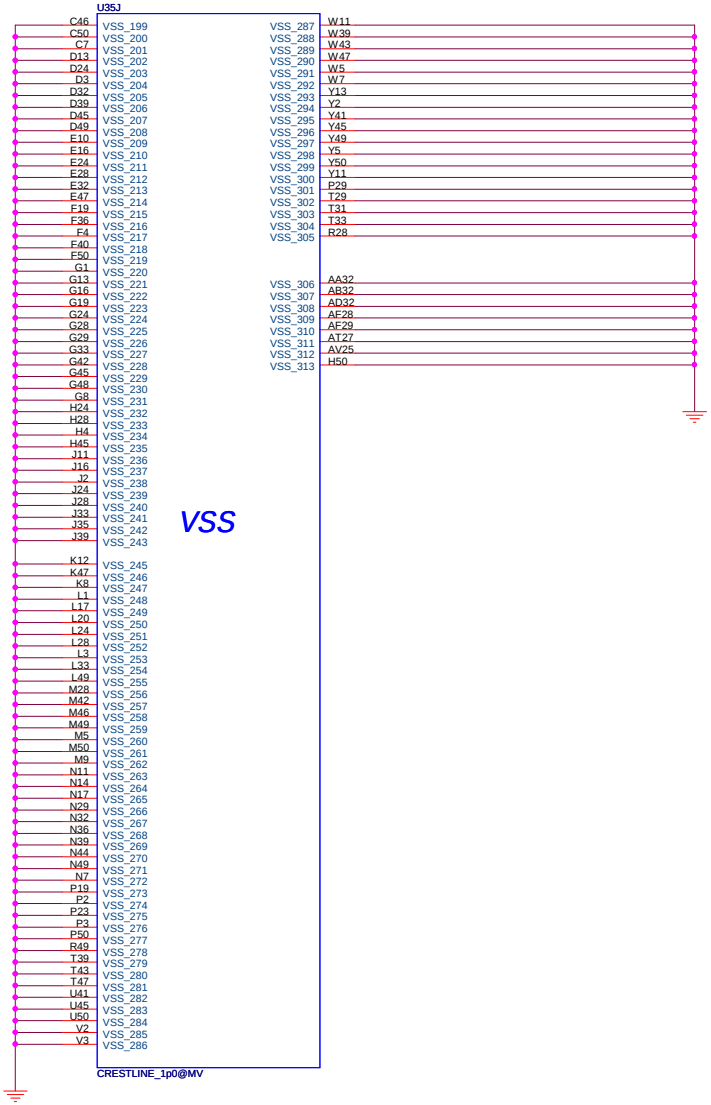
PROJECT : NA1
Quanta Computer Inc.

Size	Document Number	Rev
	GMCH Power-1(4 of 6)	2A
Date: Friday, March 23, 2007	Sheet 8 of 55	



NB(Power-3)





PROJECT : NA1
Quanta Computer Inc.

Size	Document Number	Rev
	GMCH Power-3(6 of 6)	1A
Date: Friday, March 23, 2007	Sheet 10 of 55	

Strap table

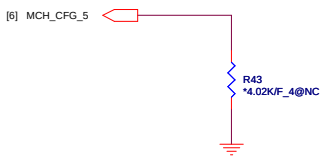
All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal

CFG[17:3] Have internal Pull-up
CFG[18:19] Have internal Pull-down
Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIe concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

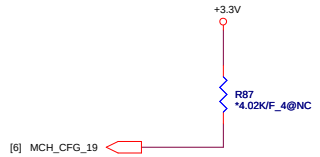
DMI X2 Select

MCH_CFG_5	Low = DMIX2 High = IDMIX4(Default)



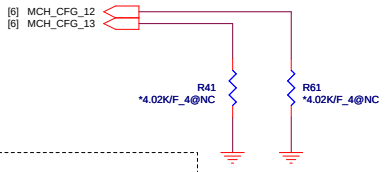
DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane



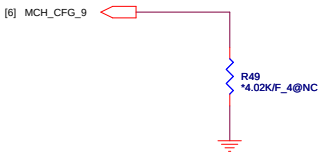
XOR /ALLz /Clock Un-gating

MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)



PCI Express Graphics

MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)

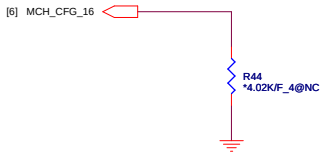


SDVO Present

Strap define at External DVI control page

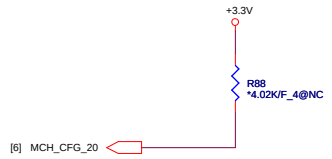
FSB Dynamic ODT

MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)



SDVO/PCIE Concurrent operation

MCH_CFG_20	Low = Only SDVO or PCIE X1 is operational(Default) High = SDVO andPCIE X1 are operating simultaneously via the PEG port



Layout Note:
Location of all MCH_CFG strap resistors needs to be close to minmize stub.

PROJECT : NA1
Quanta Computer Inc.

Size	Document Number	Rev
	GMCH Strap Table	1A
Date: Friday, March 23, 2007	Sheet 11 of 55	

DDR2 Dual channel A/B PU

DDRII A CHANNEL

+0.9V_DDR_VTT

Layout note: Place 1 cap close to every 1 R-pack terminated to SMDDR_VTERM.

C244 C152 C237 C259 C164 C252 C241 C243 C159 C258 C249 C245 C238 C251
0.1U/10V_4

DDRII B CHANNEL

+0.9V_DDR_VTT

C178 C168 C254 C171 C177 C153 C257 C181 C248 C172 C174 C160 C239 C169
0.1U/10V_4

+0.9V_DDR_VTT

+0.9V_DDR_VTT [43,47]

[7,13] DDR_A_MA[0..13]

DDR_B_MA[0..13] [7,13]

DDR_A_MA7 / DDR_A_MA11	RP21	56X2	RP18	56X2	DDR_B_MA11 / DDR_B_MA7
DDR_A_MA4 / DDR_A_MA6	RP17	56X2	RP14	56X2	DDR_B_MA6 / DDR_B_MA4
[7,13] DDR_A_RAS# / [7,13] DDR_A_BS1	RP9	56X2	RP8	56X2	DDR_B_RAS# [7,13] / DDR_B_BS1 [7,13]
DDR_A_MA13 / [6,13] M_ODT0	RP3	56X2	RP2	56X2	DDR_B_MA13 / M_ODT2 [6,13]
[7,13] DDR_A_BS2 / DDR_A_MA12	RP20	56X2	RP11	56X2	DDR_B_MA1 / DDR_B_MA3
DDR_A_MA9 / DDR_A_MA8	RP16	56X2	RP19	56X2	DDR_B_MA9 / DDR_B_MA12
DDR_A_MA5 / DDR_A_MA3	RP12	56X2	RP15	56X2	DDR_B_MA5 / DDR_B_MA8
DDR_A_MA10 / DDR_A_BS0 [7,13]	RP6	56X2	RP7	56X2	DDR_B_MA10 / DDR_B_BS0 [7,13]
[7,13] DDR_A_WE# / [7,13] DDR_A_CAS#	RP4	56X2	RP5	56X2	DDR_B_WE# [7,13] / DDR_B_CAS# [7,13]
DDR_A_MA0 / DDR_A_MA2	RP13	56X2	RP10	56X2	DDR_B_MA2 / DDR_B_MA0

[6,13] M_ODT1 / DDR_A_MA1	R127 / R140	56_4	R131 / R154	56_4	M_ODT3 [6,13] / DDR_B_BS2 [7,13]
[6,13] DDR_CS0_DIMMA#	R135	56_4	R134	56_4	DDR_CS2_DIMMB# [6,13]
[6,13] DDR_CS1_DIMMA#	R129	56_4	R132	56_4	DDR_CS3_DIMMB# [6,13]
[6,13] DDR_CKE0_DIMMA	R151	56_4	R149	56_4	DDR_CKE3_DIMMB [6,13]
[6,13] DDR_CKE1_DIMMA	R155	56_4	R152	56_4	DDR_CKE4_DIMMB [6,13]
[6,13] DDR_A_MA14	R153	56_4	R148	56_4	DDR_B_MA14 [6,13]

Please these resistor closely DIMMA,all trace length<750 mil.

Please these resistor closely DIMMB,all trace length<750 mil.

DDR2 Thermal Sensor SO-DIMM 0 & 1

Uninstall

+3.3V_M

+3.3V_M [2,13,16,43]

R171 *220_6@NC

C253 *0.1U/10V_4@NC

U7

[2,13] CGCLK_SMB_M — SCLK (8)

[2,13] CGDAT_SMB_M — SDA (7)

[6,13] PM_EXTTS#0 — ALERT# (6)

[6] PM_EXTTS#1 — R170 *0_4@NC — OVERT# (4)

VCC (1) LM86_3V

DXP (2) DDR_THERMDA

DXN (3) C759 *2200P/50V_6@NC

GND (5) DDR_THERMDC

*MMBT3904_NL@NC Q40

*LM86CIMM@NC

Size	Document Number	Rev
	DDR RES. ARRAY	1A

PROJECT : NA1

Quanta Computer Inc.

Date: Friday, March 23, 2007 Sheet 12 of 55

A is required to route to Top SoDIMM for AMT to function.This will need to change for M08

DDR2 Dual channel A/B CONN

PC4800 DDR2 SDRAM SO-DIMM (200P)

CN21 — DIMM1_9.2 — H 9.2

CKE 0,1
CLOCK 0,1

SMbus address A0

CN22 — DIMM2_5.2 — H 5.2

CKE 2,3
CLOCK 3,4

SMbus address A4

iAMT

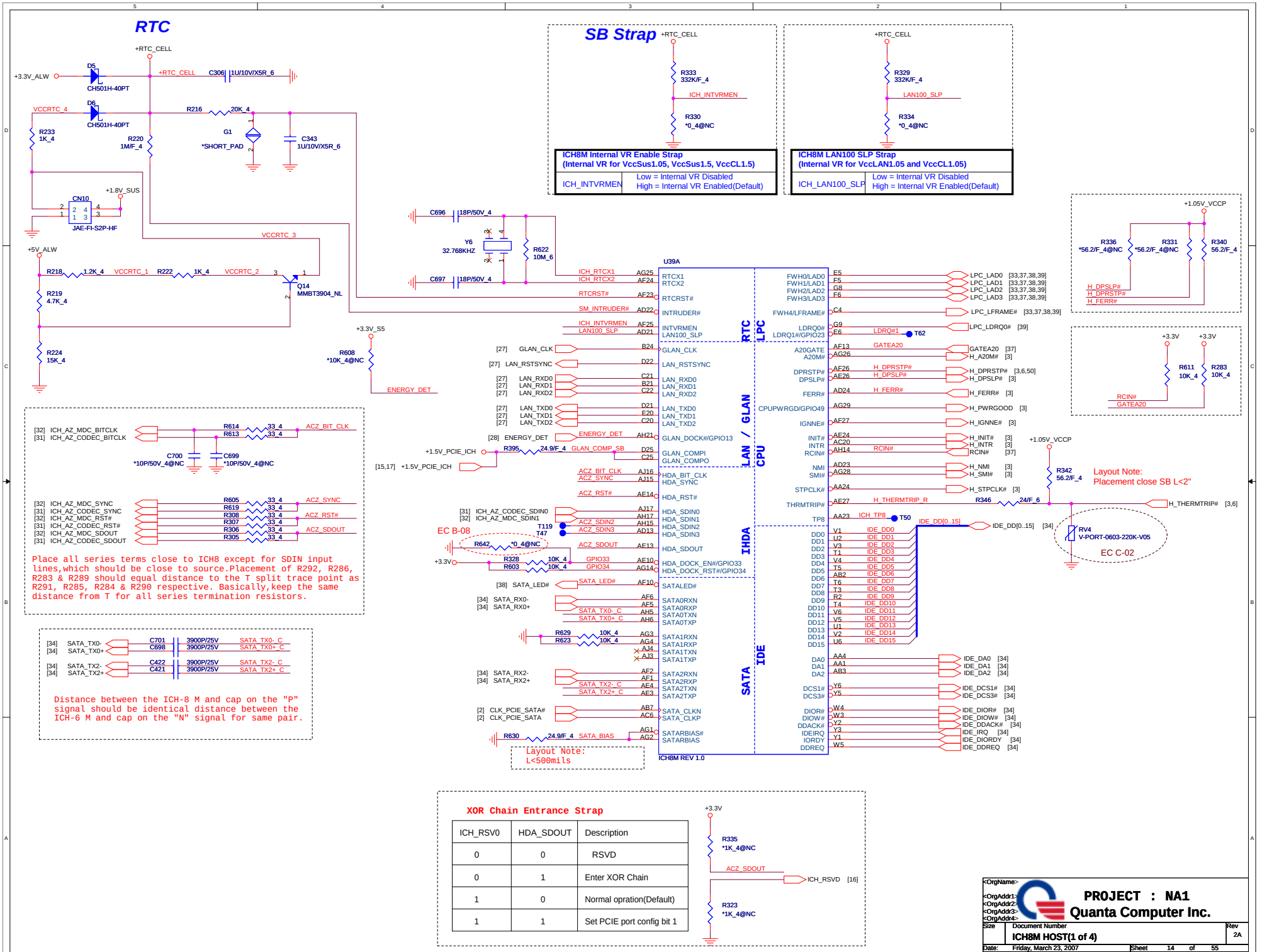
Place these Caps near So-Dimm1.

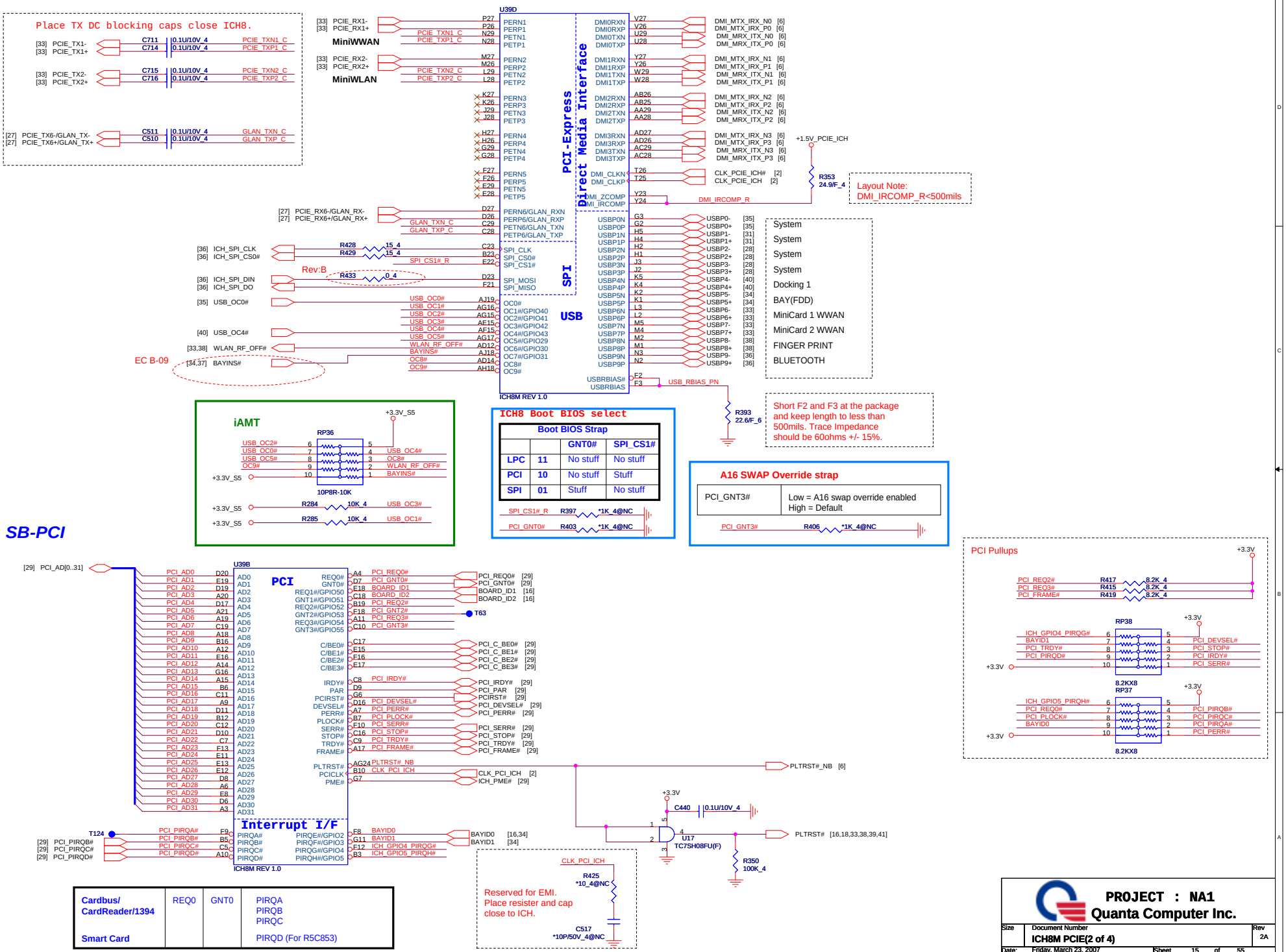
EC C-03
Delete C124

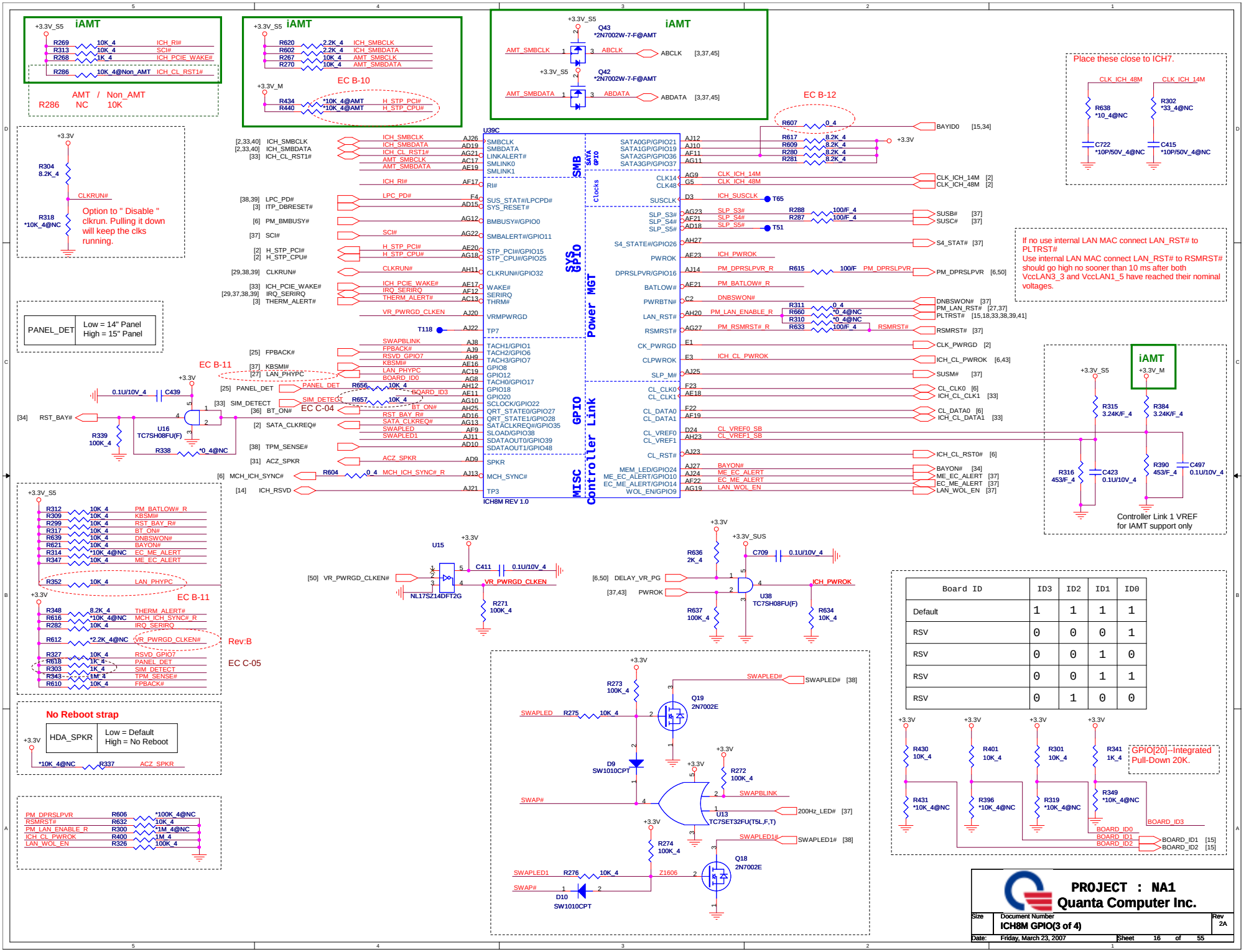
Place these Caps near So-Dimm2.

PROJECT : NA1
Quanta Computer Inc.

Size	Document Number	Rev
	DDR SO-DIMM(200P)	1A
Date: Friday, March 23, 2007	Sheet 13 of 55	



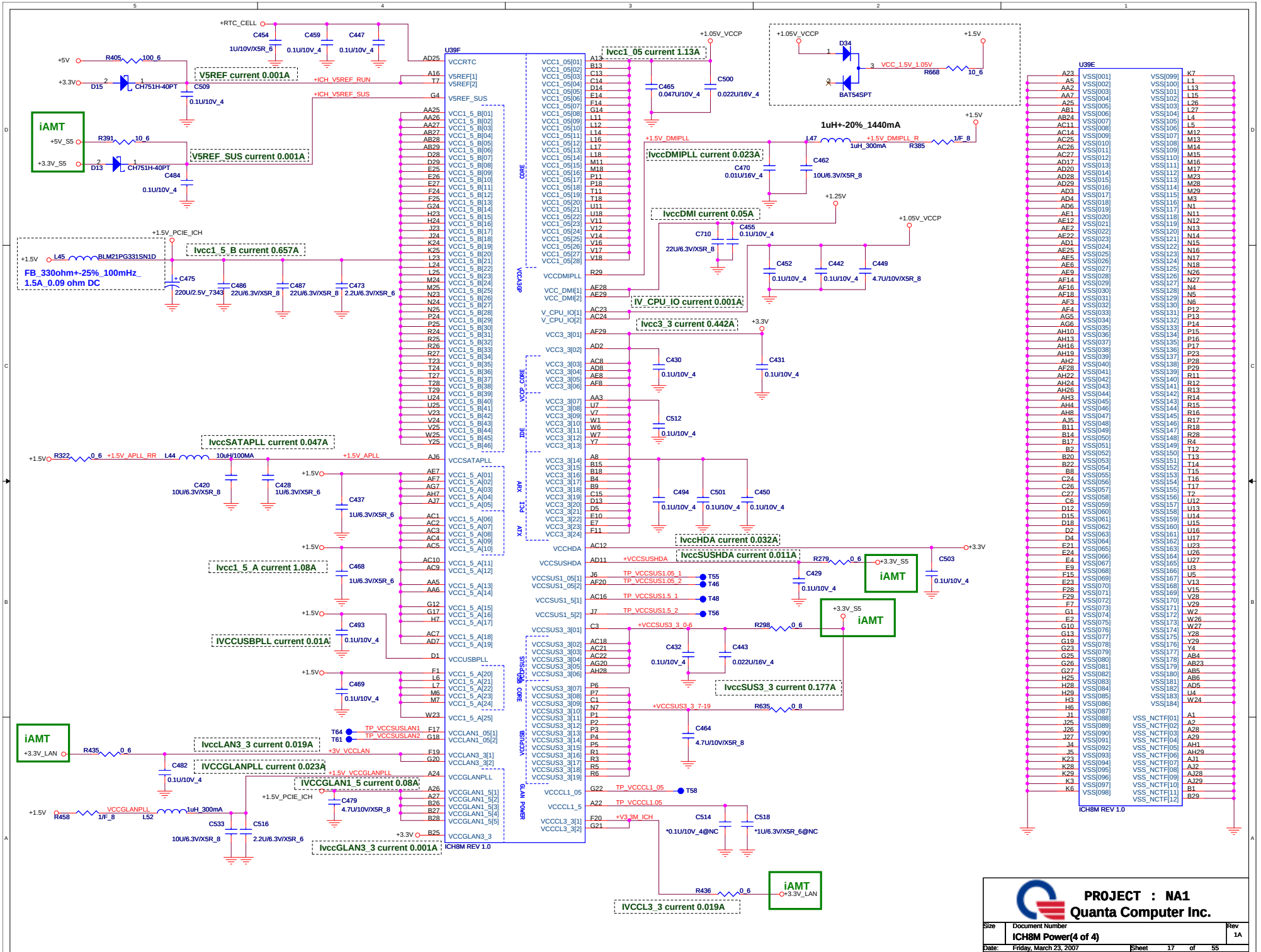


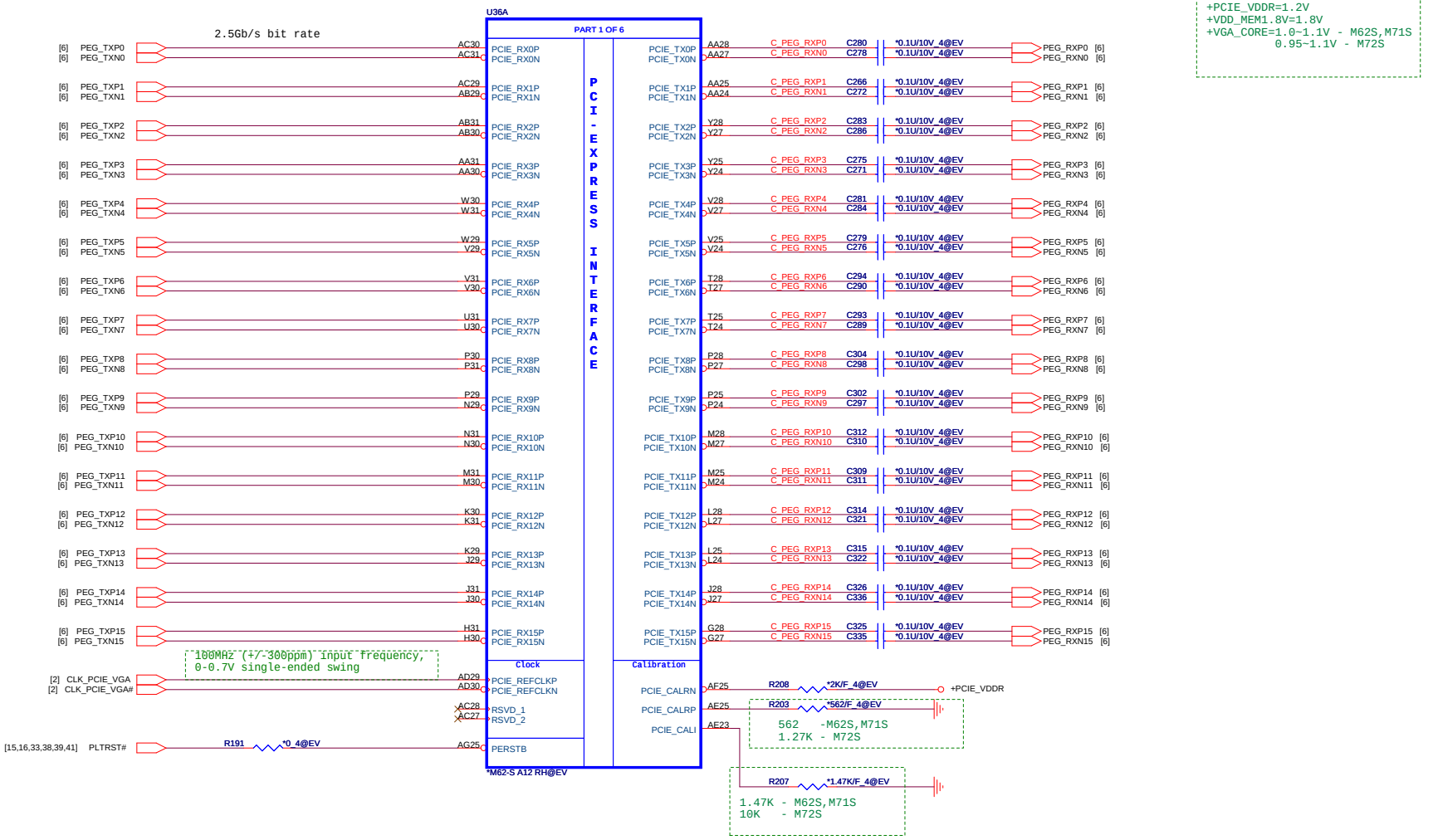


Board ID	ID3	ID2	ID1	ID0
Default	1	1	1	1
RSV	0	0	0	1
RSV	0	0	1	0
RSV	0	0	1	1
RSV	0	1	0	0

PROJECT : NA1
Quanta Computer Inc.

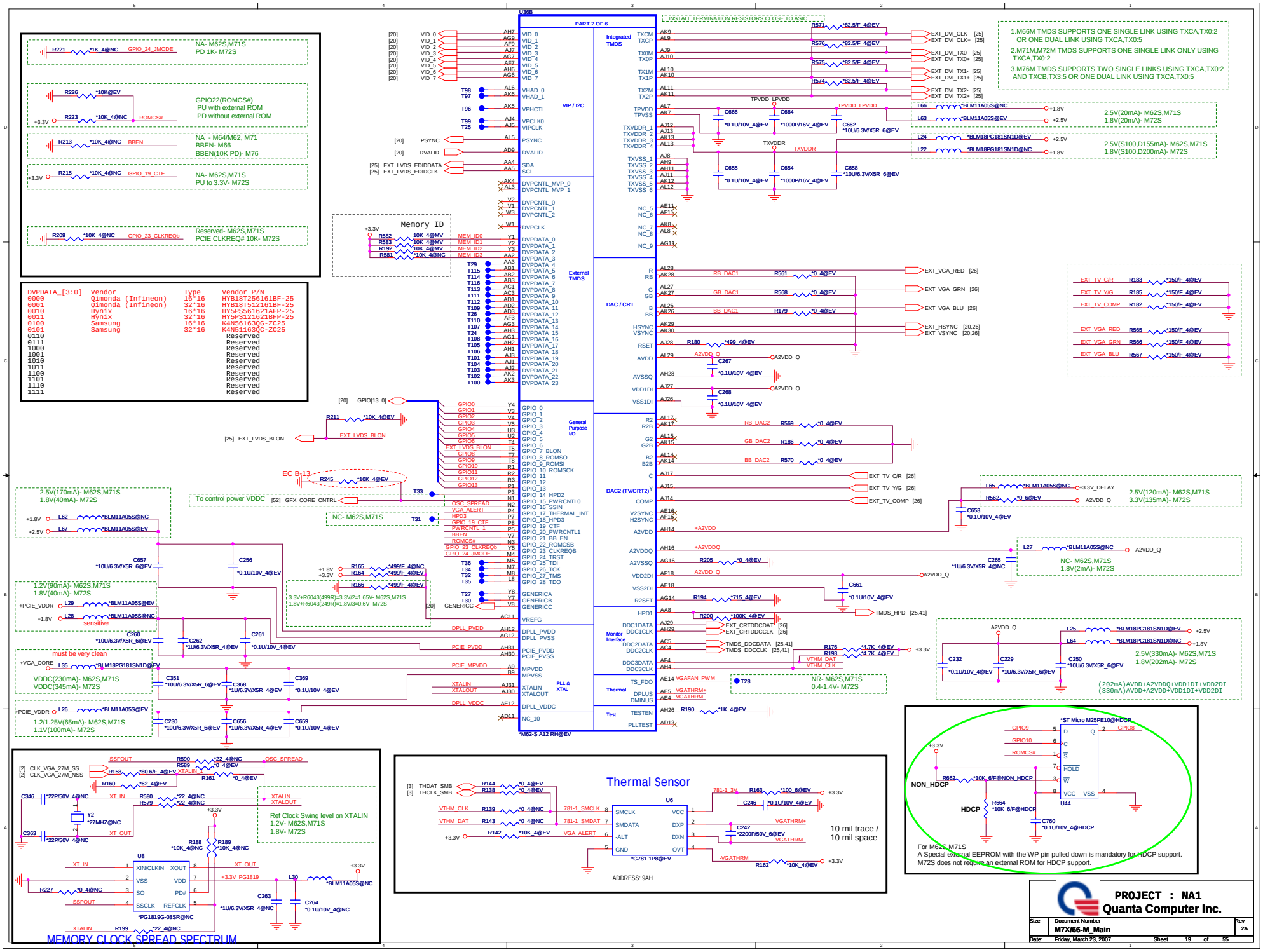
Size	Document Number	Rev
	ICH8M GPIO(3 of 4)	2A
Date: Friday, March 23, 2007	Sheet 16 of 55	

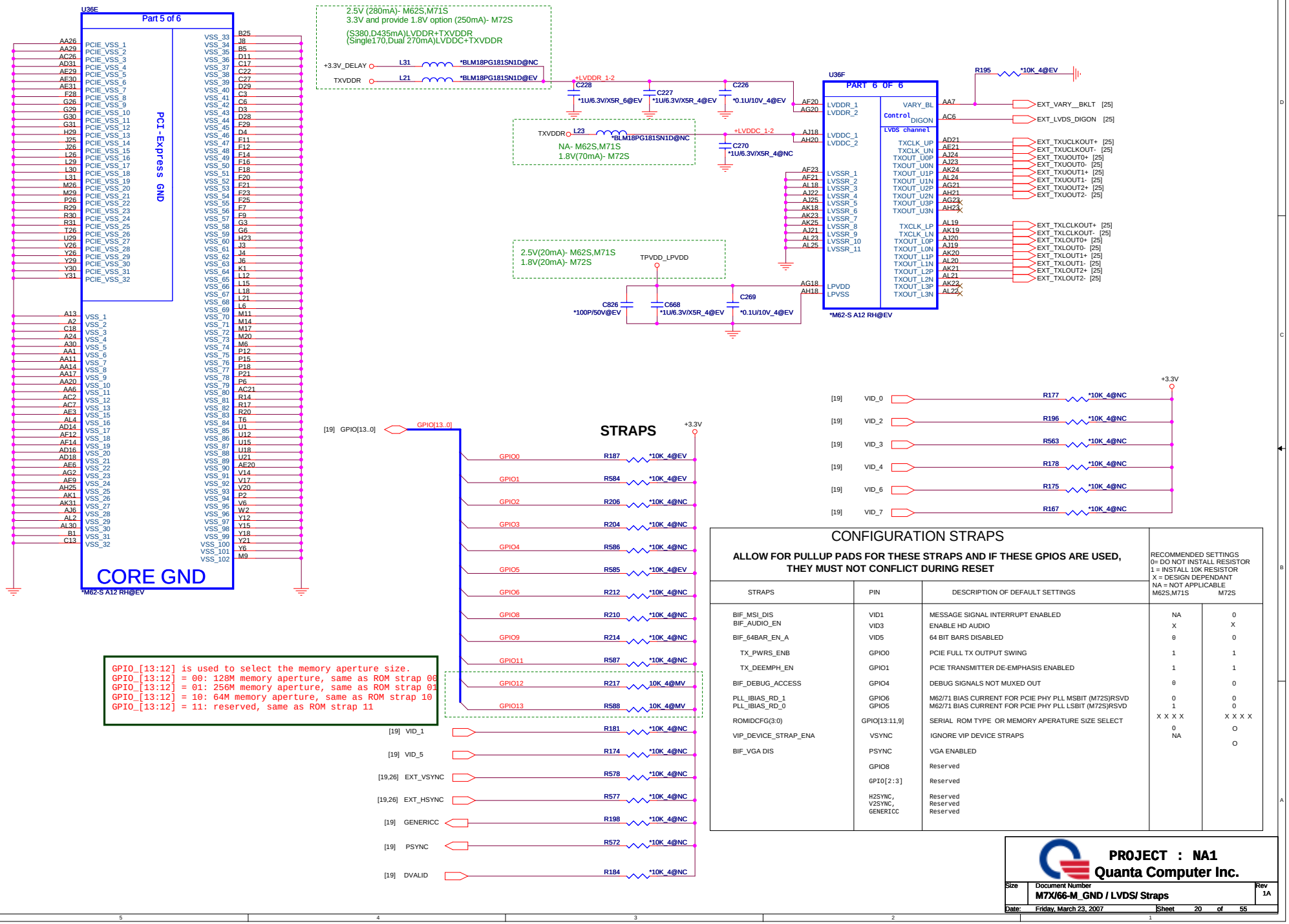


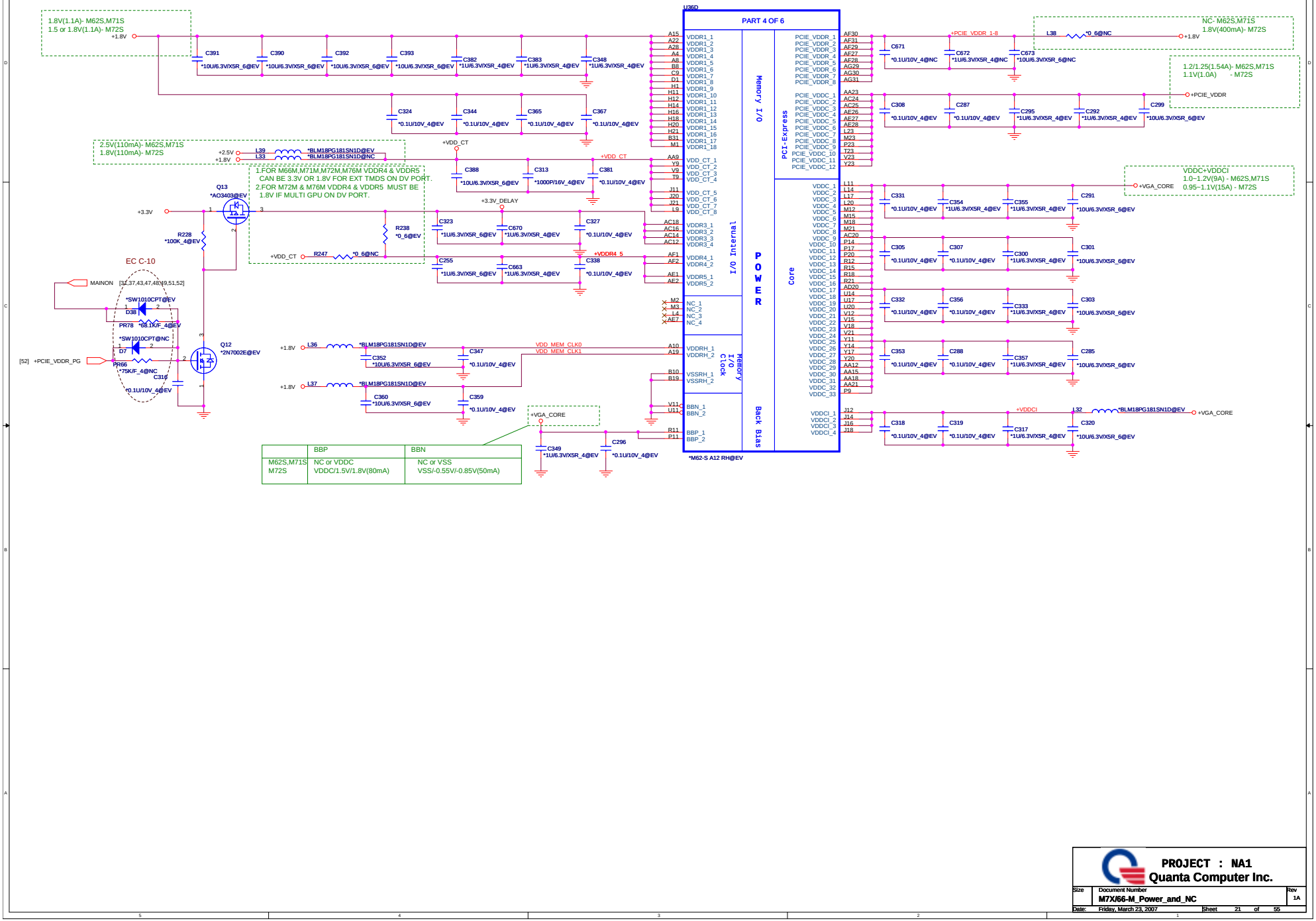


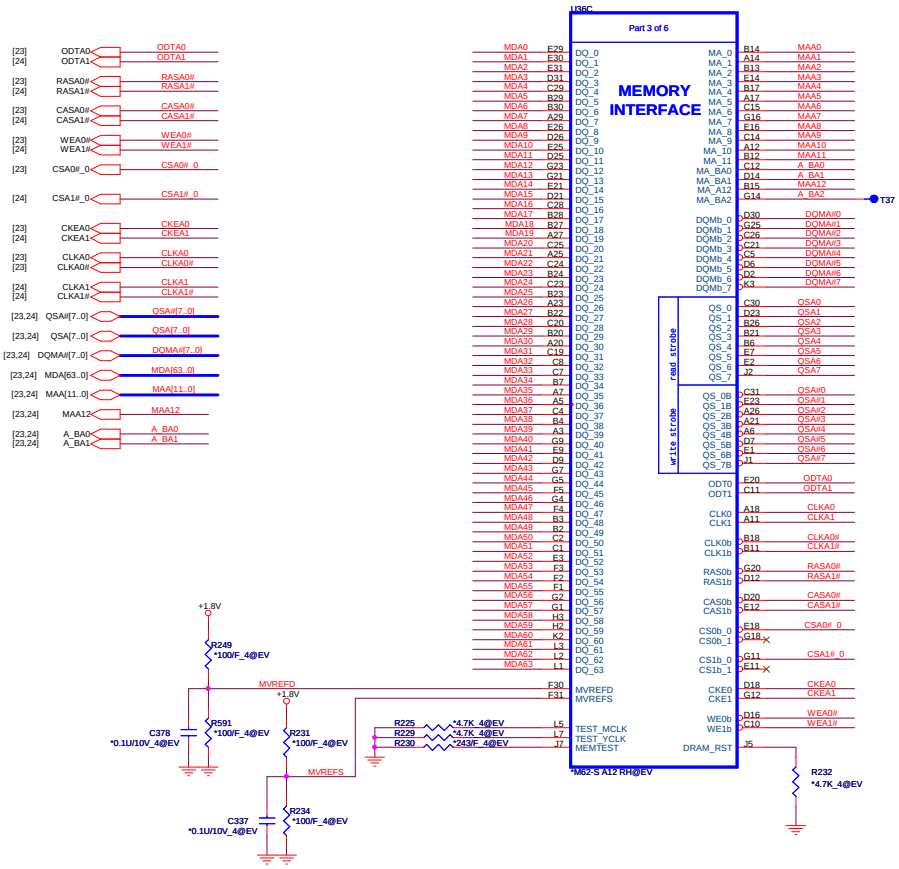
PROJECT : NA1
Quanta Computer Inc.

Size	Document Number	Rev
	M7X/66-M_PCIE_Interface	1A
Date: Friday, March 23, 2007	Sheet 18 of 55	









PROJECT :	NA1
Quanta Computer Inc.	
Size	Document Number: M7X/66-M MEM_Interface
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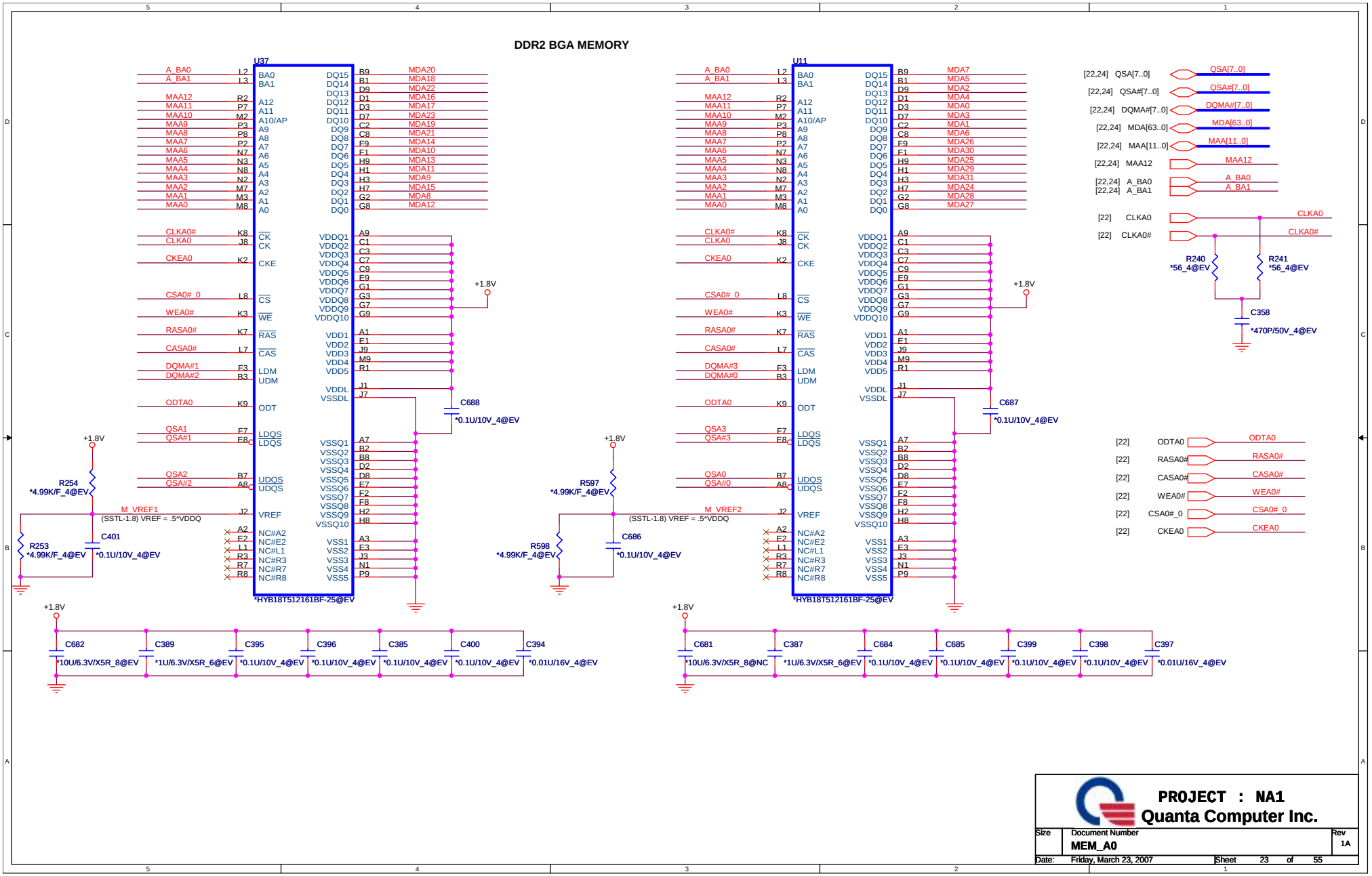
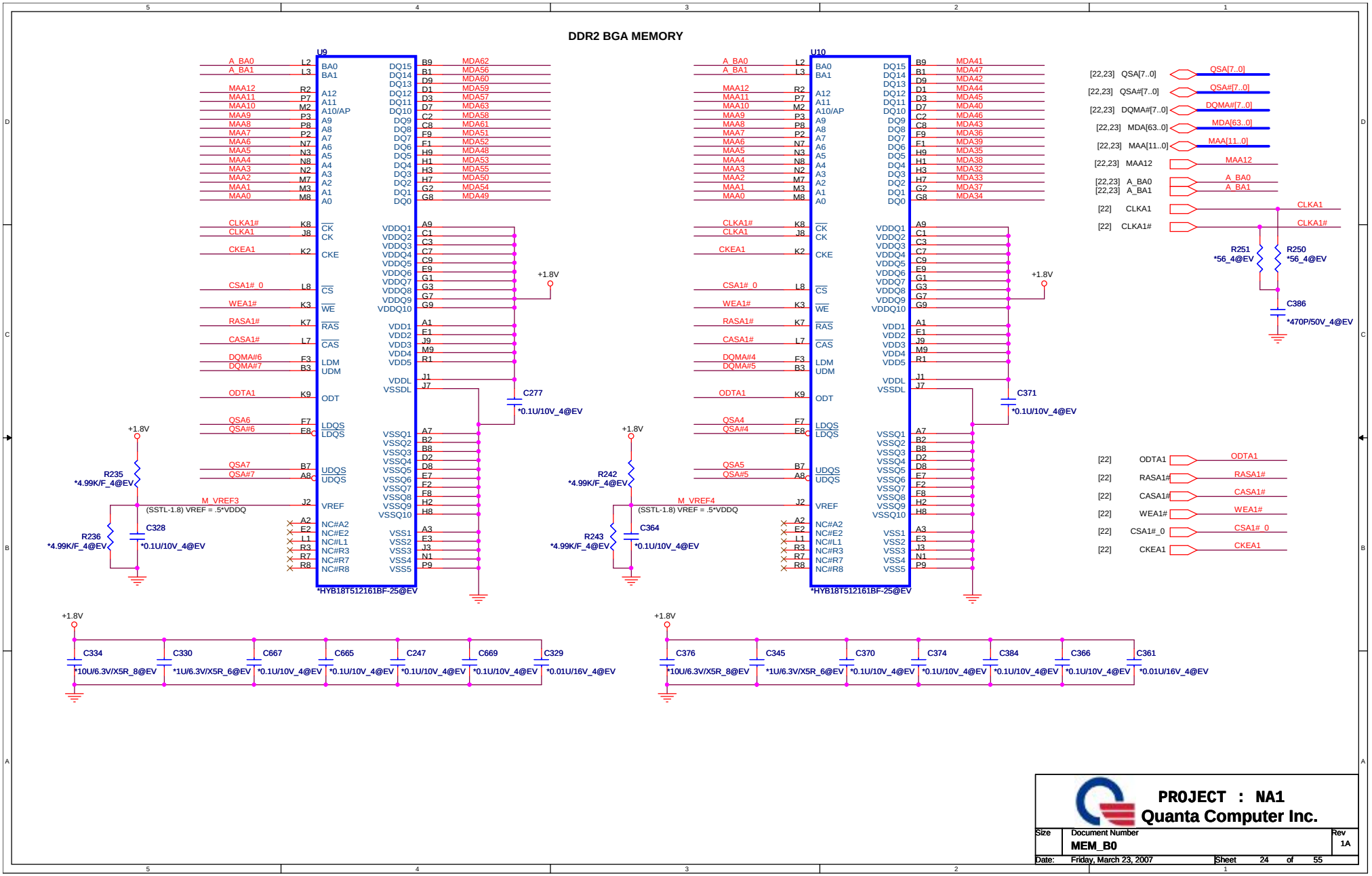
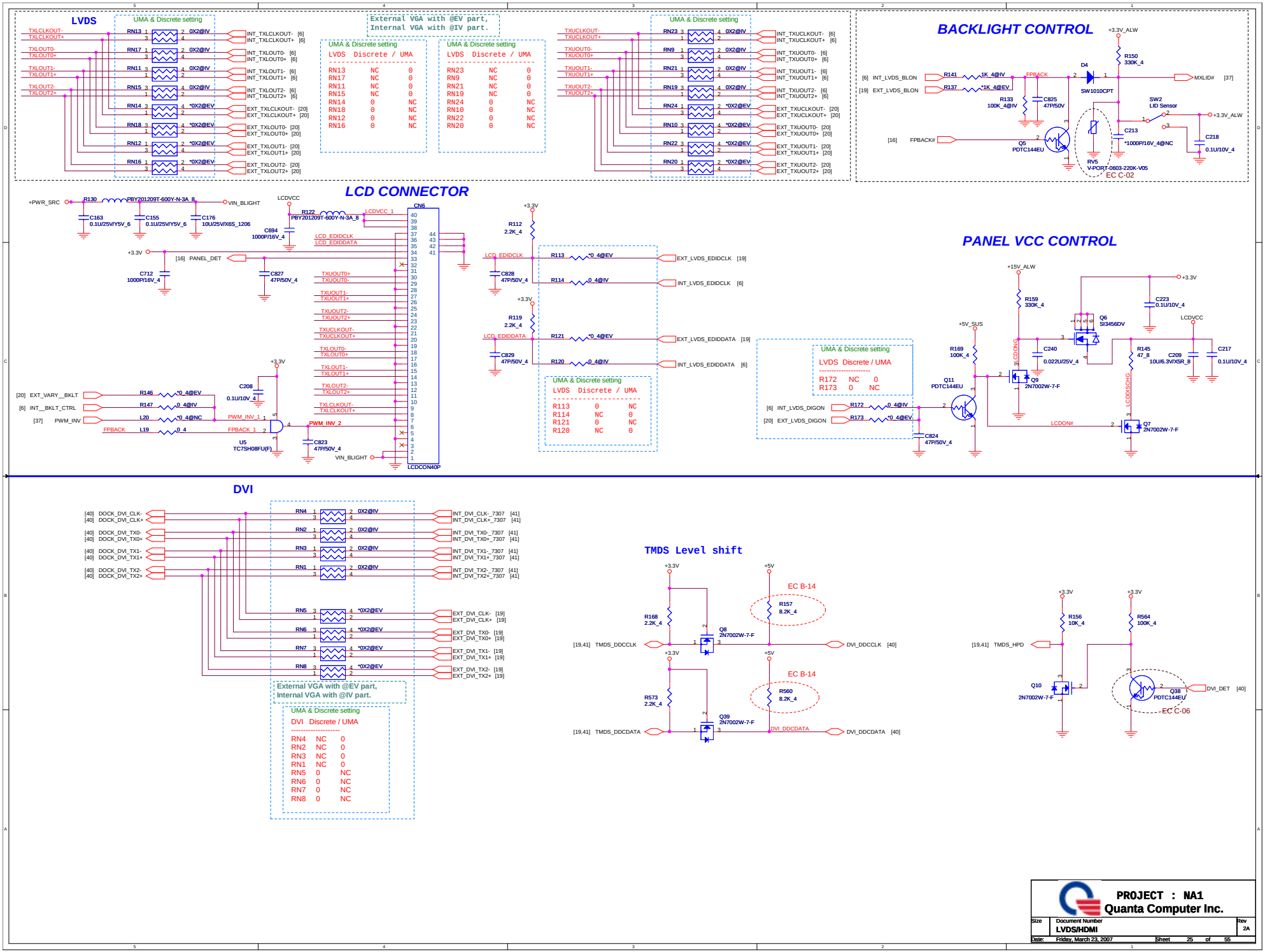
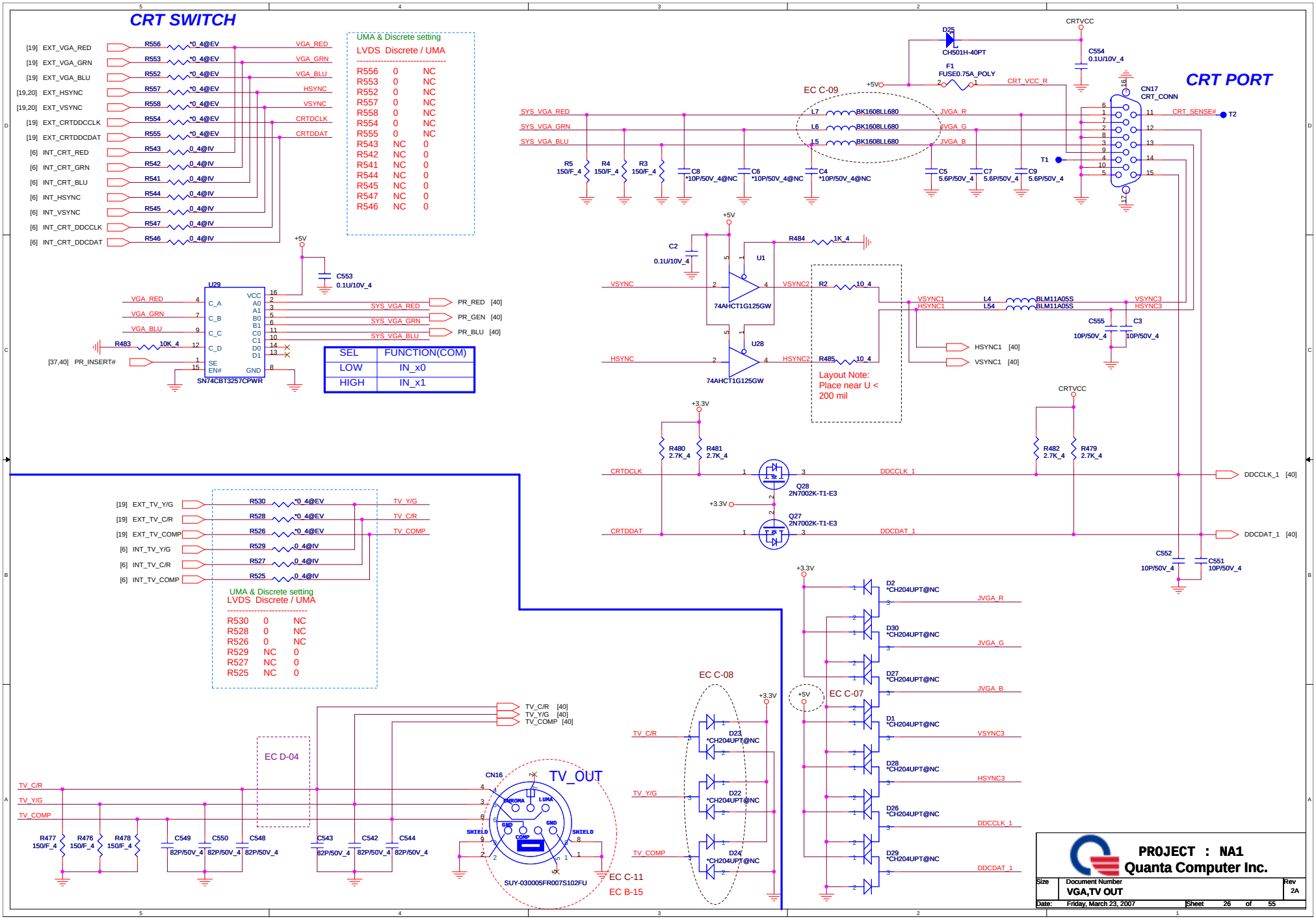
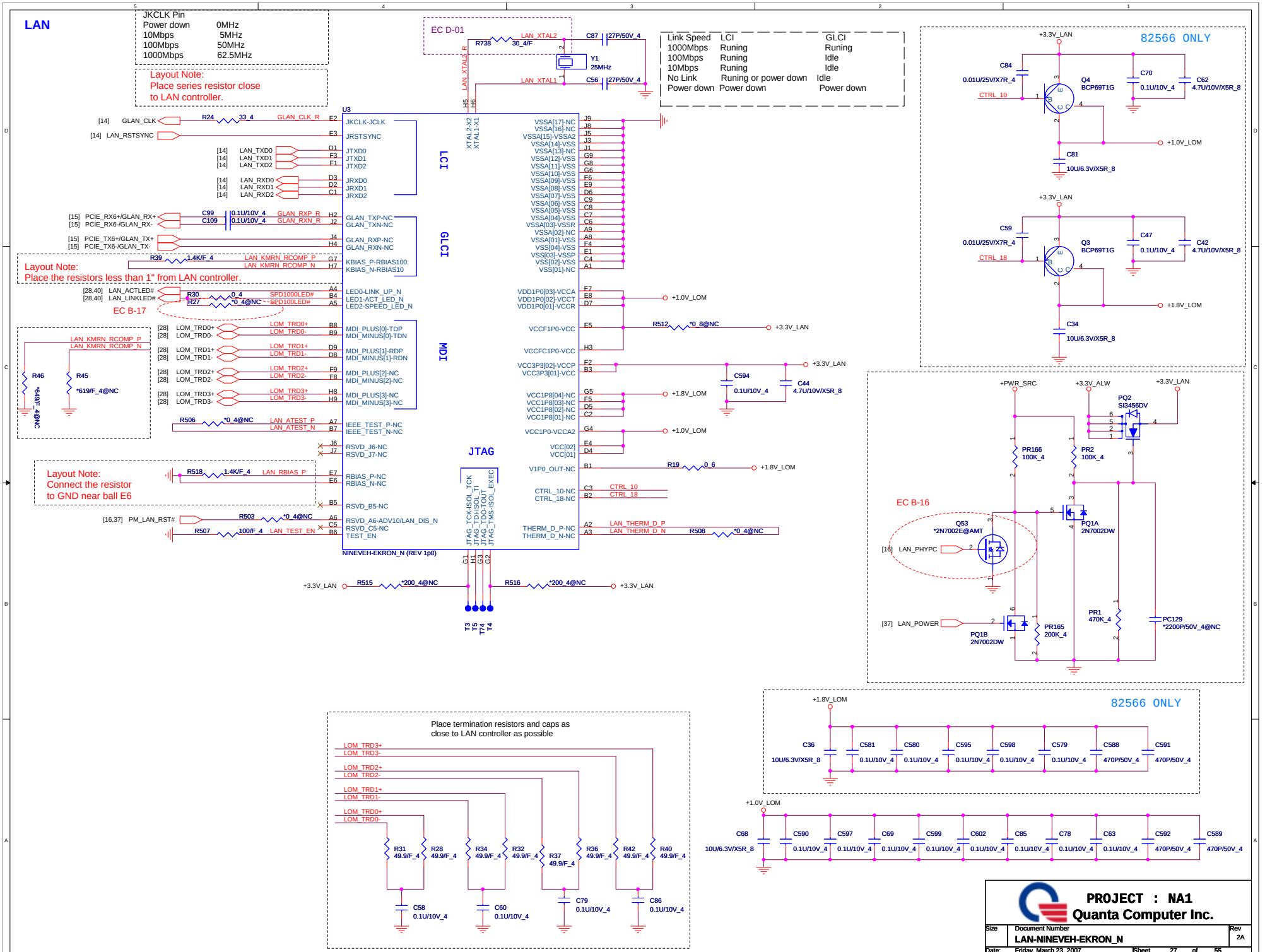
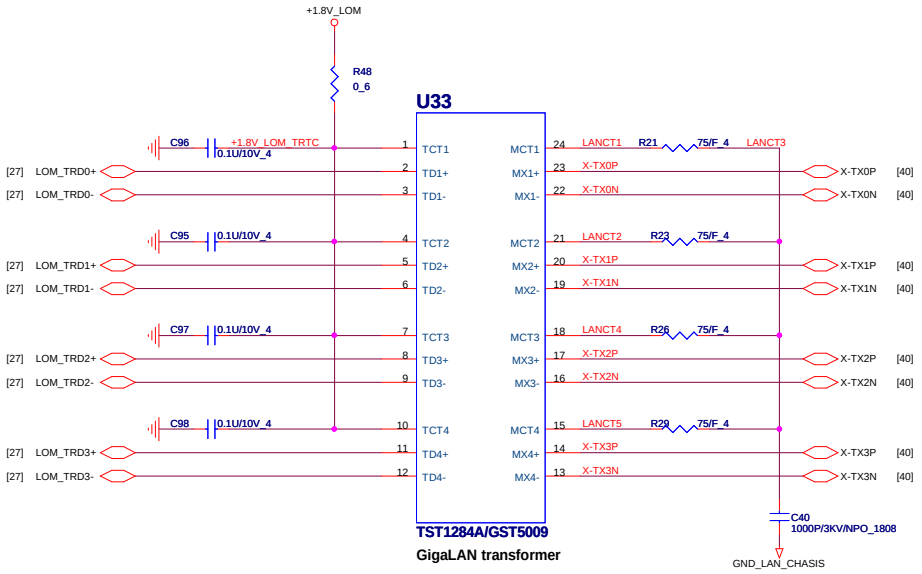


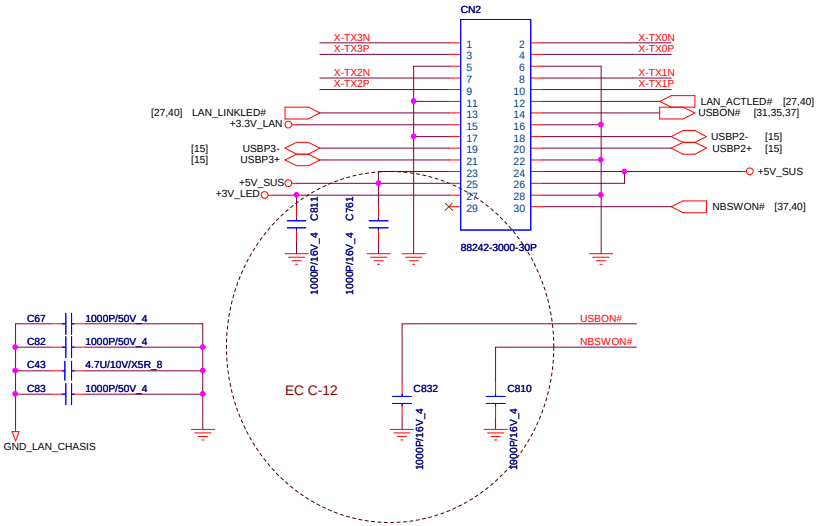






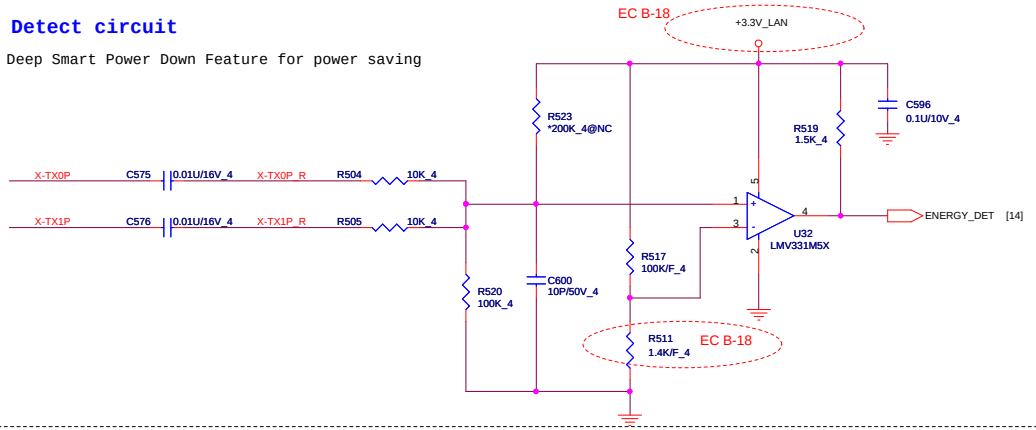






LAN Energy Detect circuit

82556 Support Deep Smart Power Down Feature for power saving



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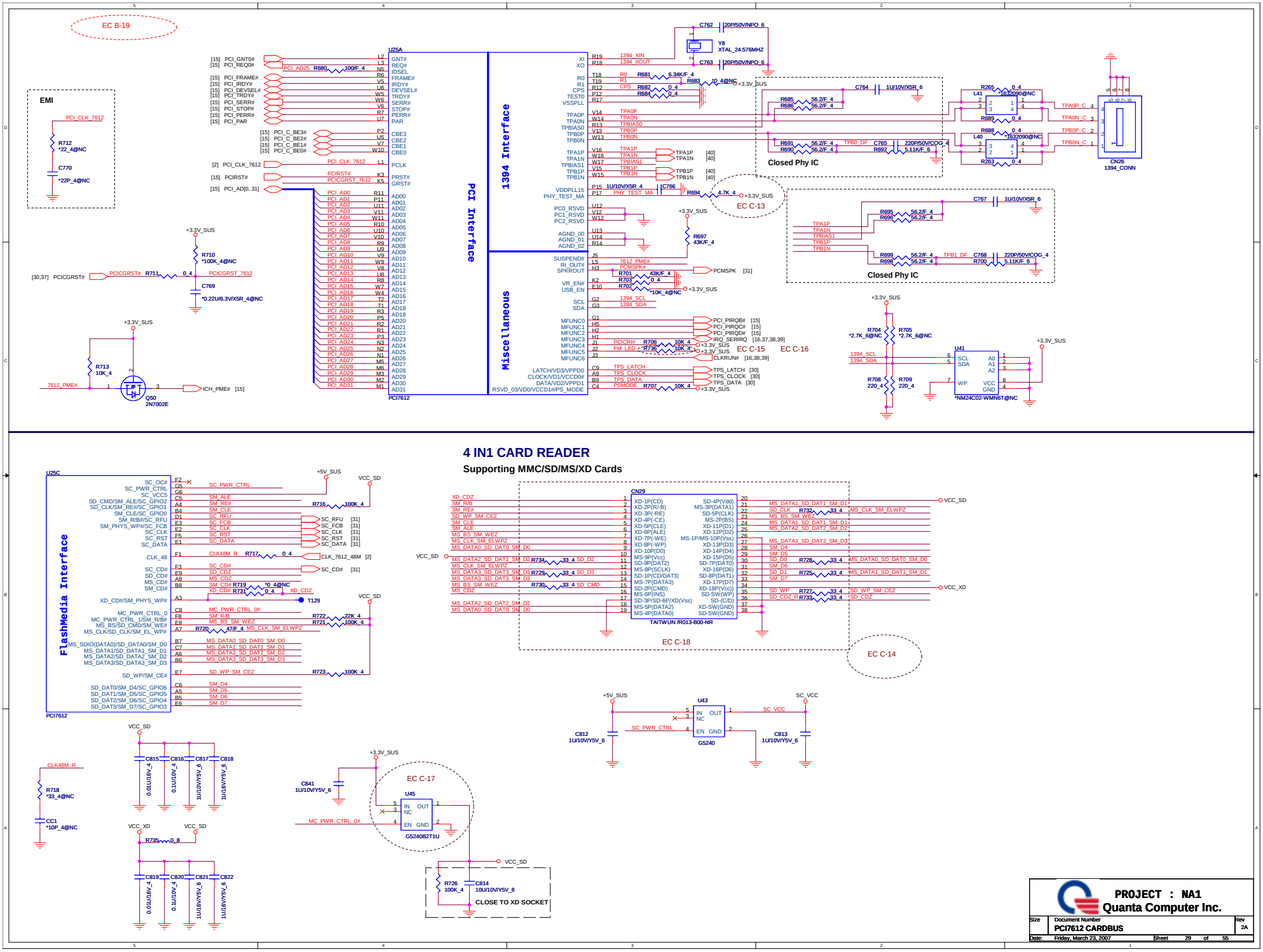
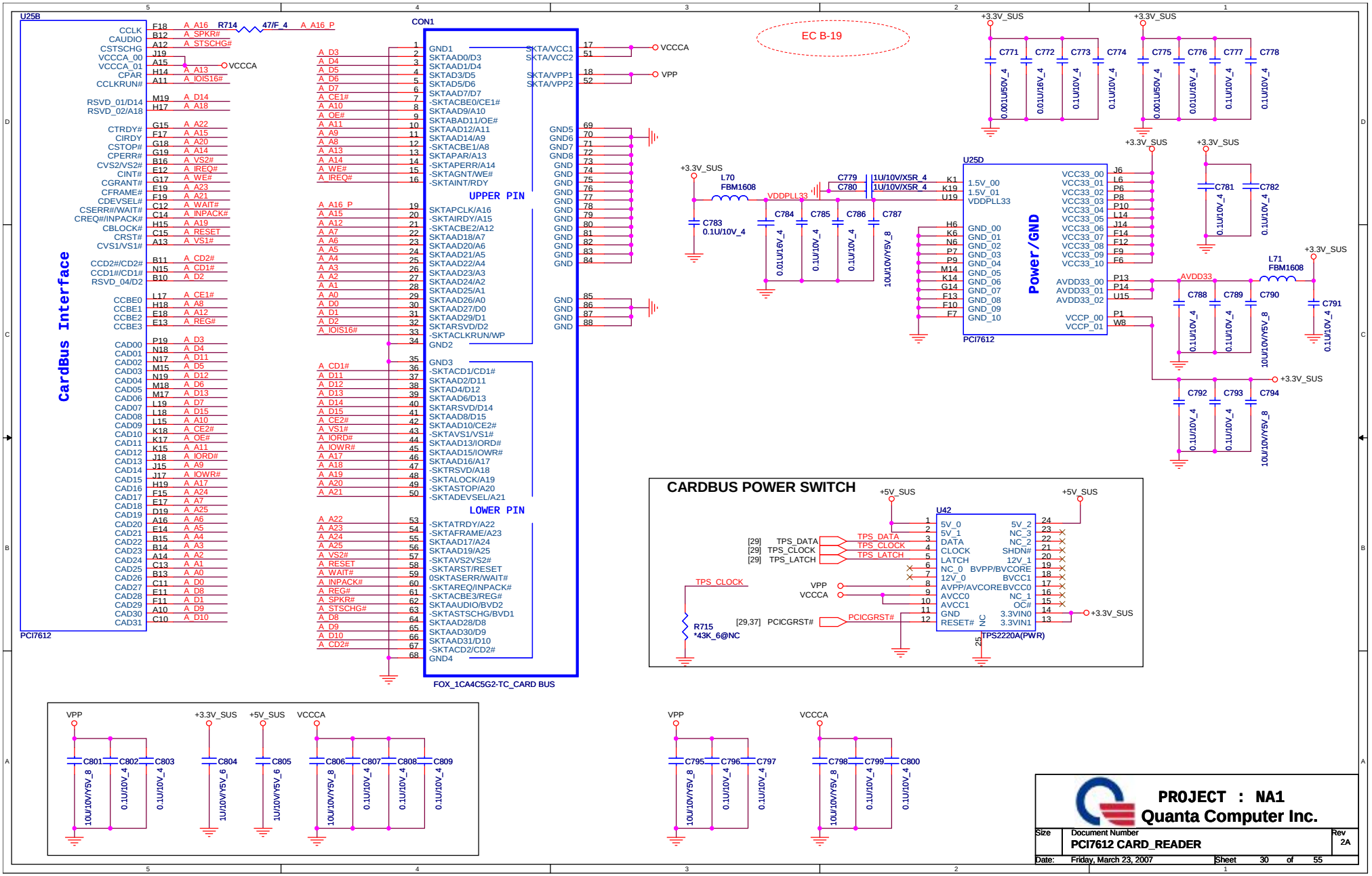
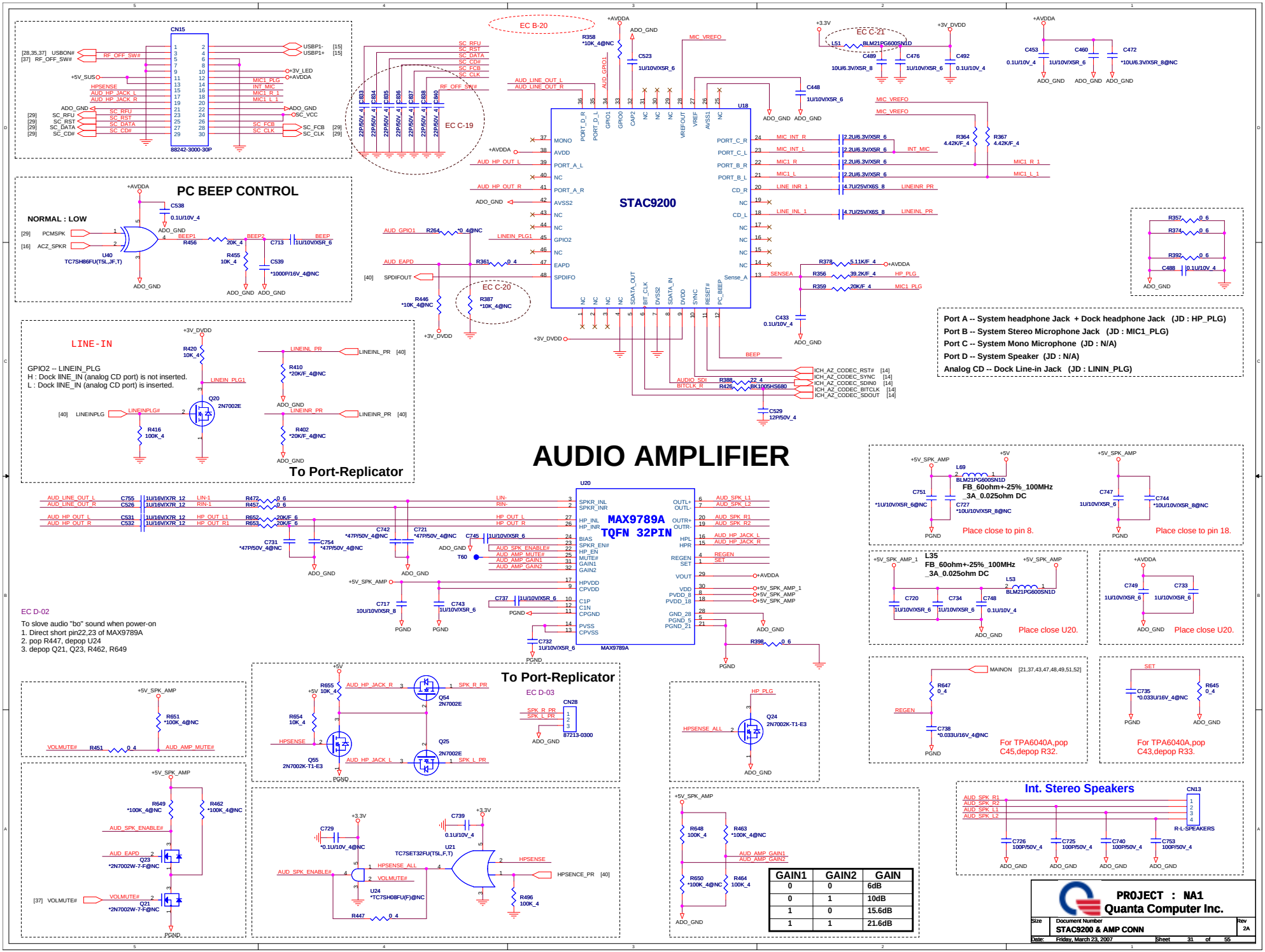
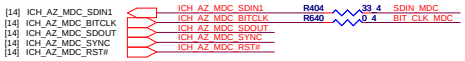
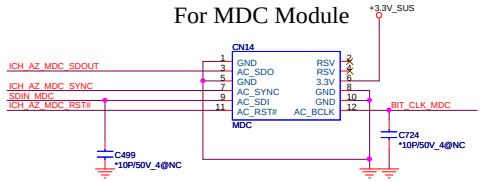








For MDC Module



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Quanta Computer Inc.

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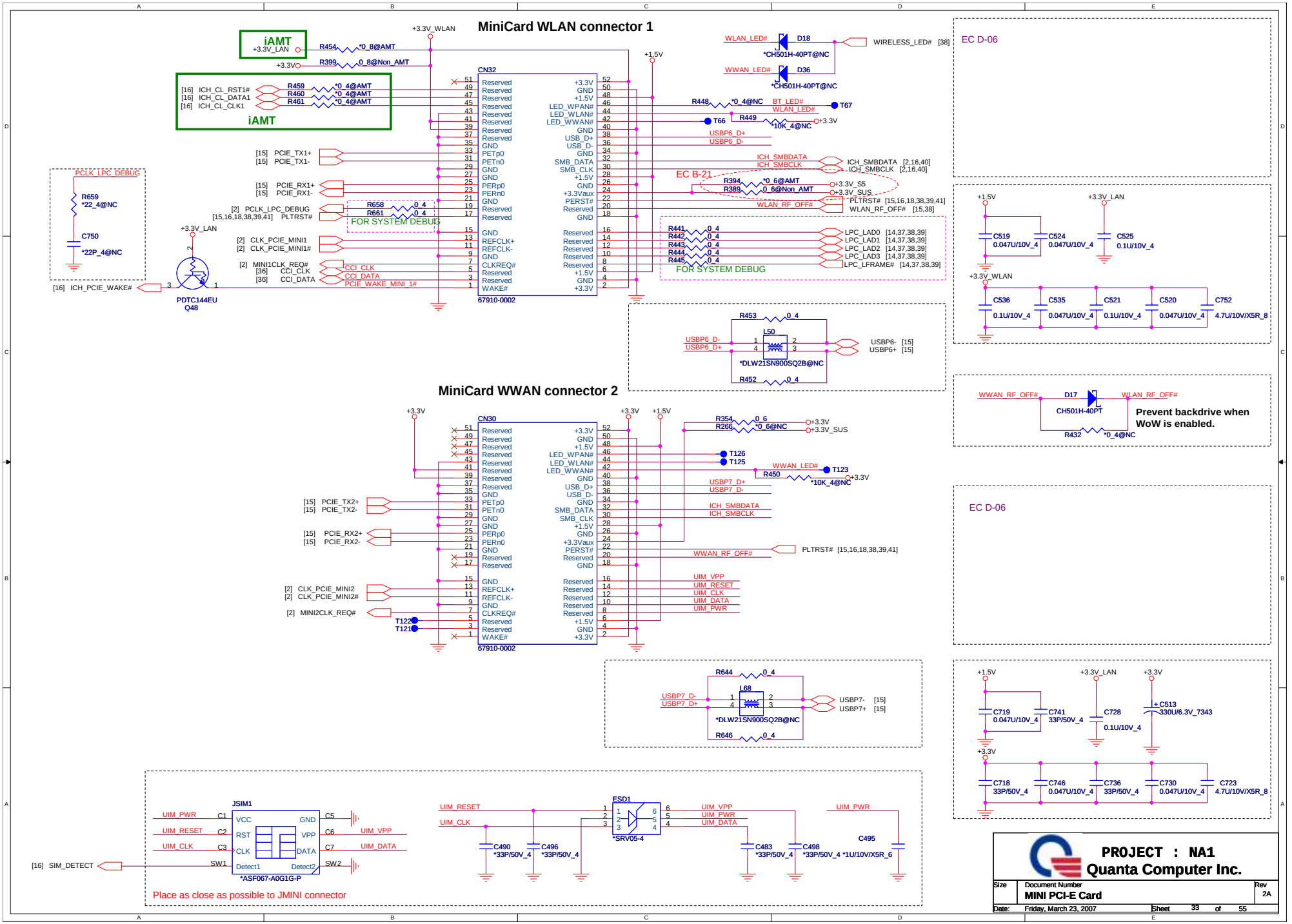
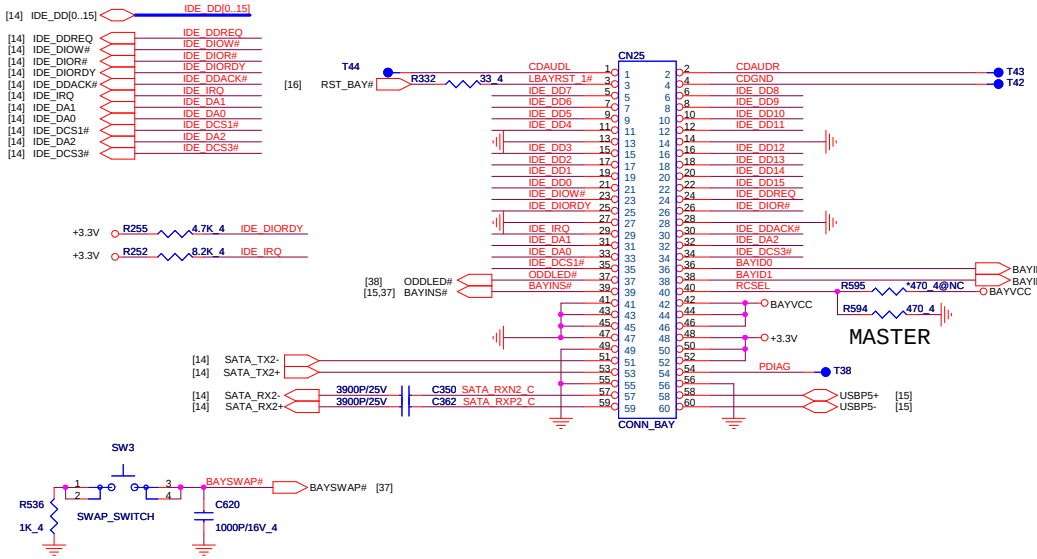
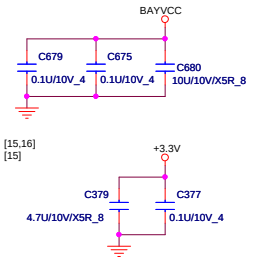


LEFT BAY(CD-ROM, HDD-PATA/SATA, FDD,)

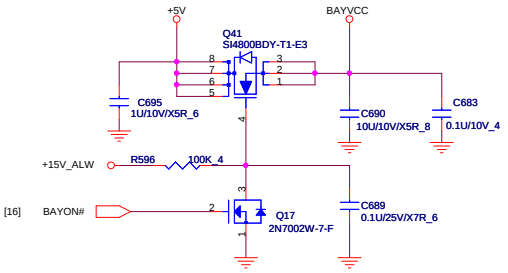


LBAY_ID_STATUS

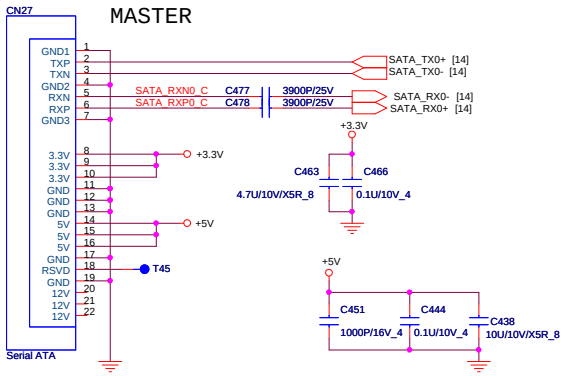
LEFT BAYID1	LEFT BAYID0	STATUS
0	0	HDD(PATA)
0	1	ODD
1	0	HDD(SATA)
1	1	Reserve



BAY POWER CONTROL



SATA CONNECTOR



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Quanta Computer Inc.		
Size	Document Number: SATA HDD,ODD,USB	Rev: 1A
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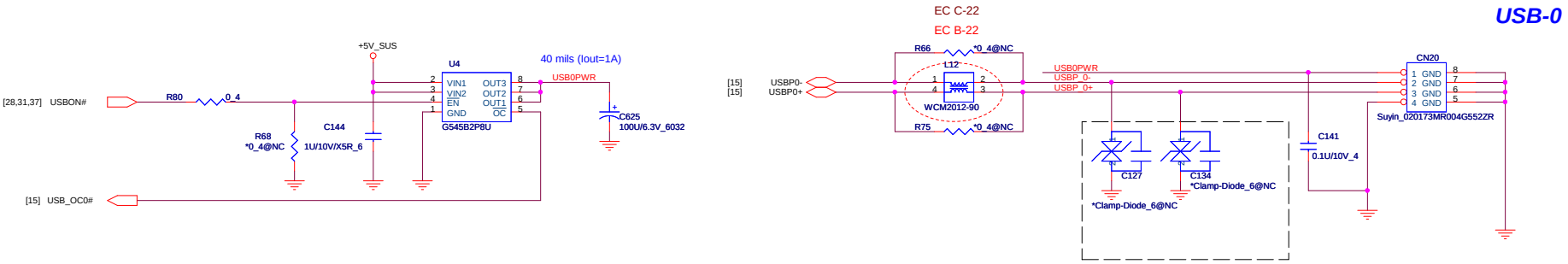

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Quanta Computer Inc.

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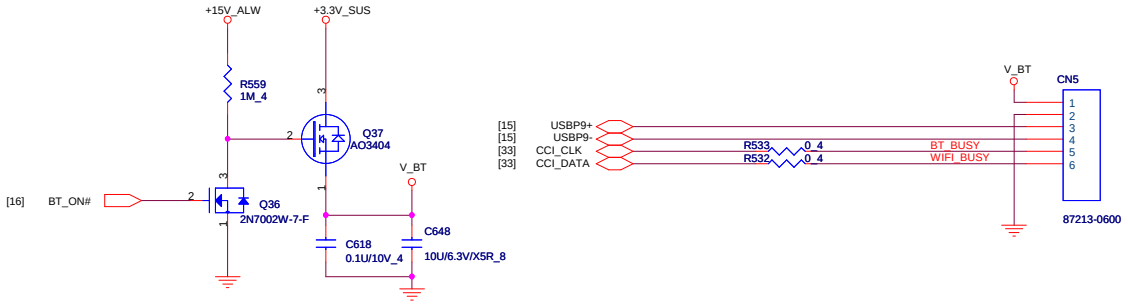
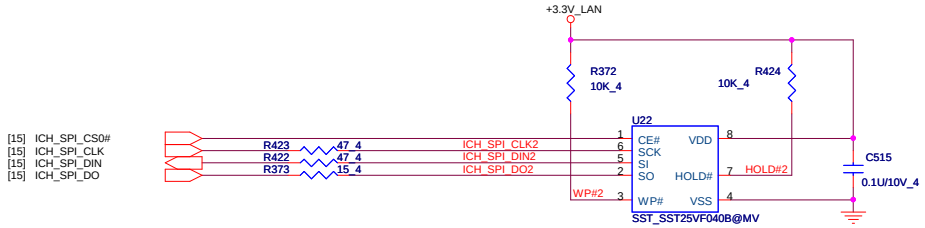
BLUETOOTH CONNECTOR



16Mbit (2M Byte), SPI **iAMT**

Layout Note:
Place R471,R498,R534 within 500 mils from SPI Flash.Place R567 within 500mils from R534; R520 within 500mils from R498 and R570 within 500mils from R471.

EC D-07



Size	Document Number: BLUETOOTH & iAMT flash	Rev: 1A
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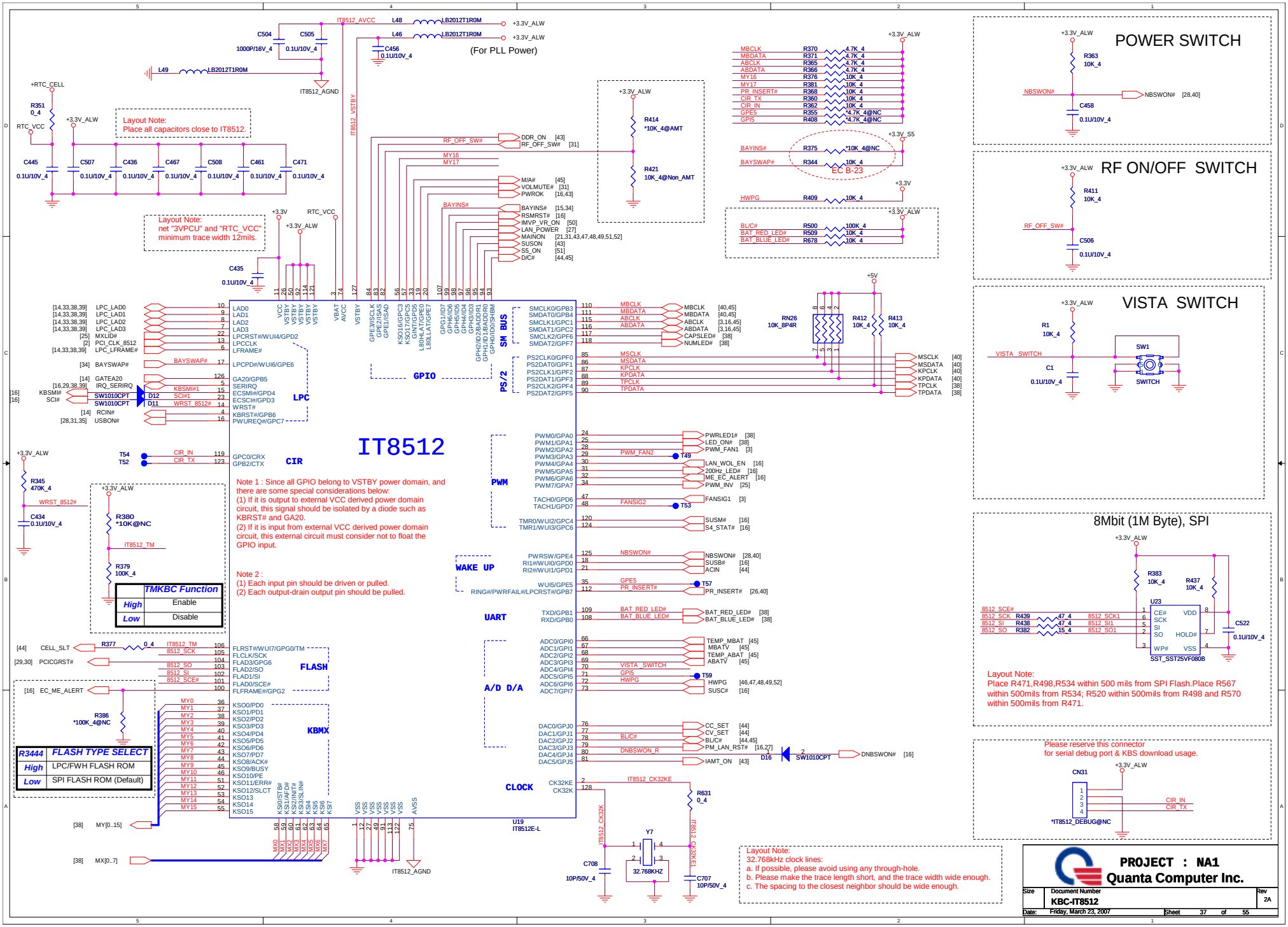
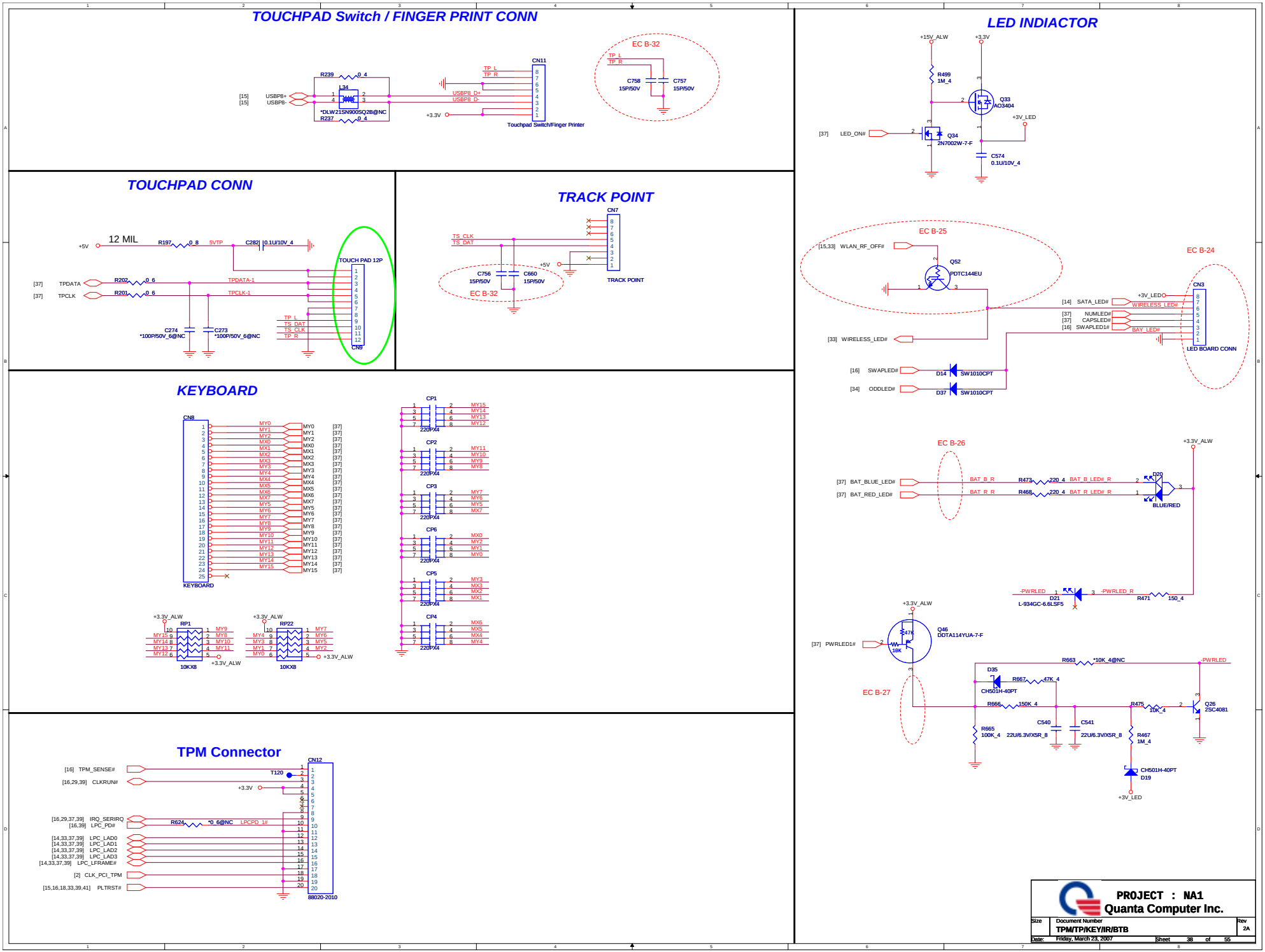
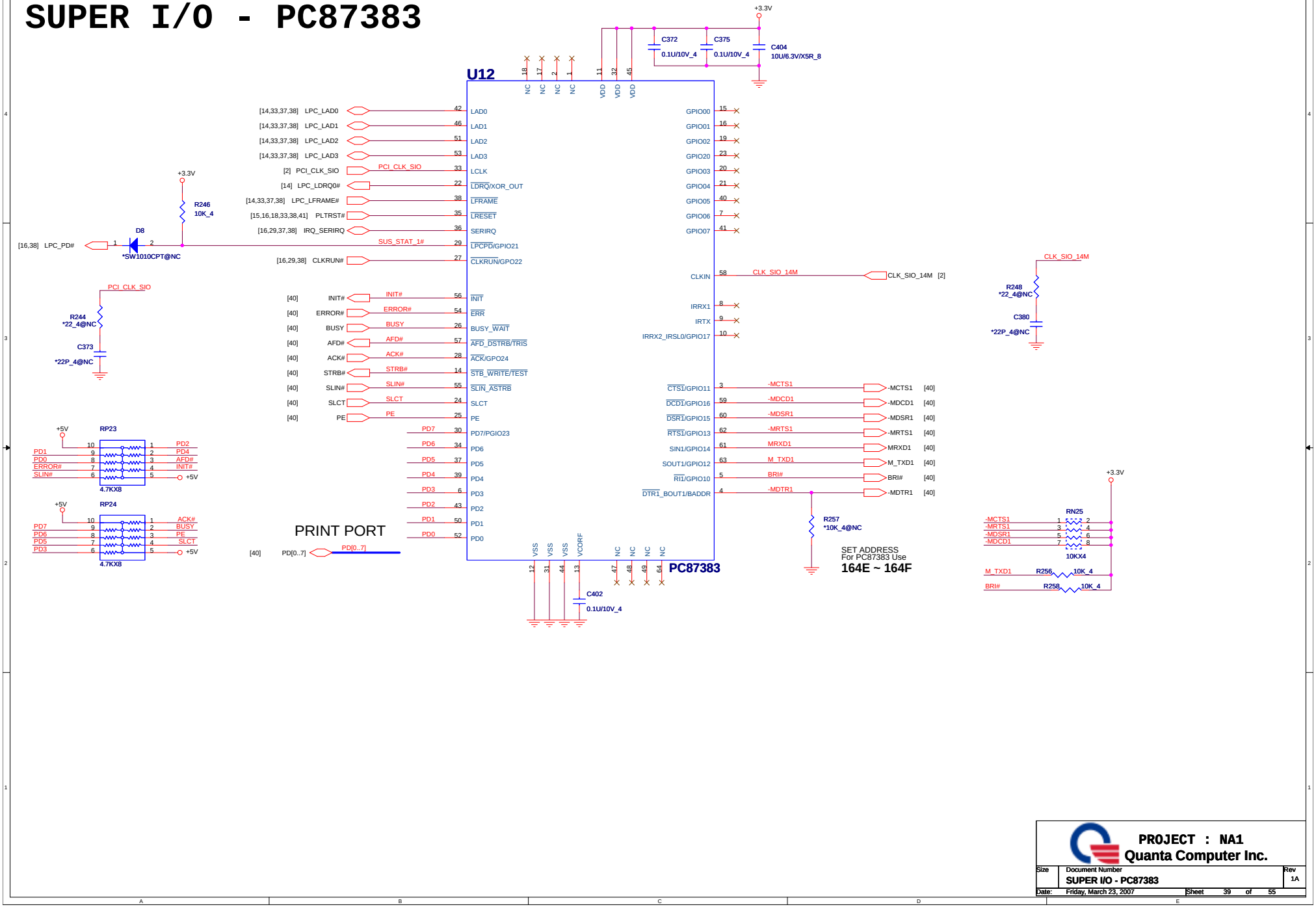
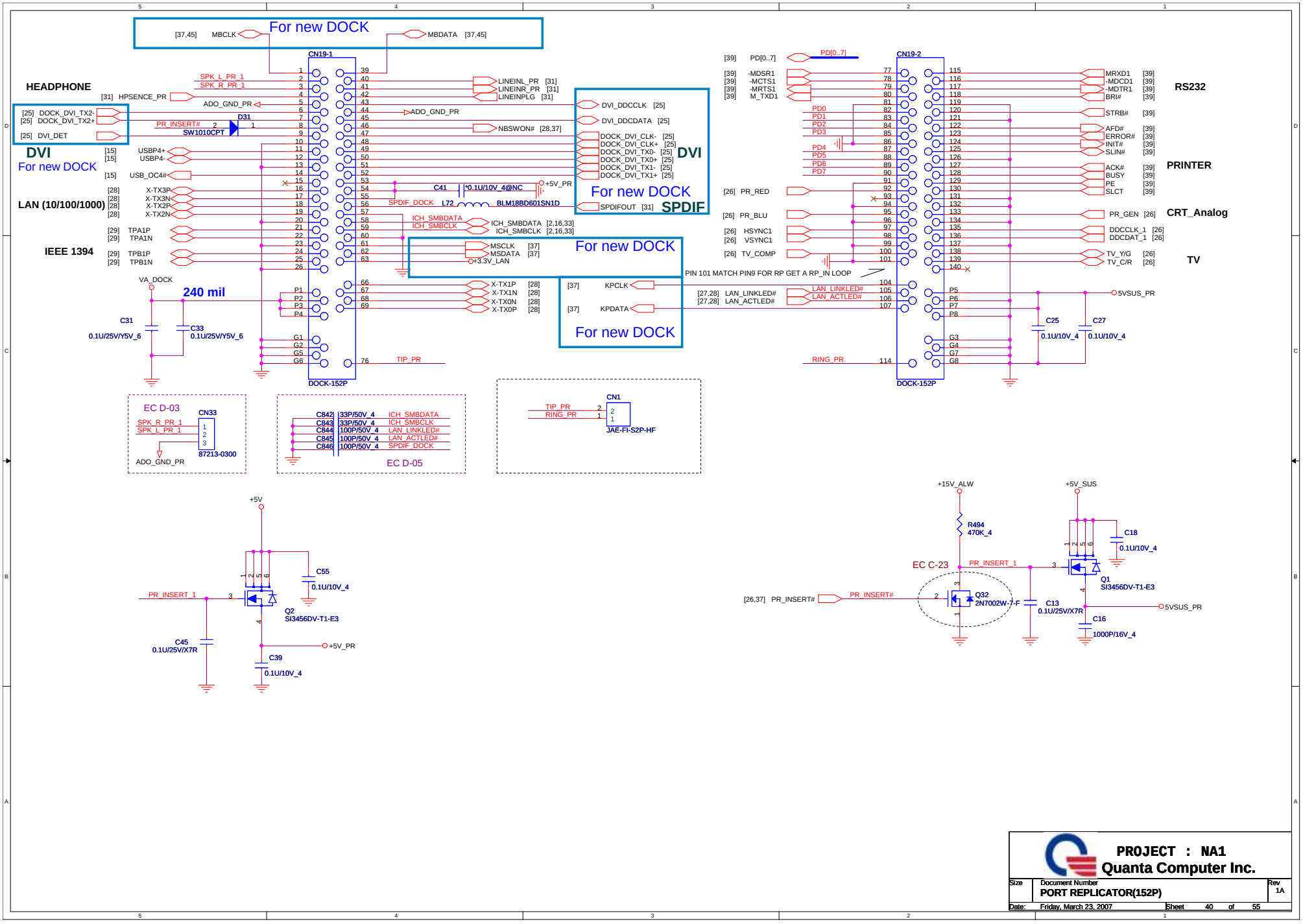
Quanta Computer Inc.



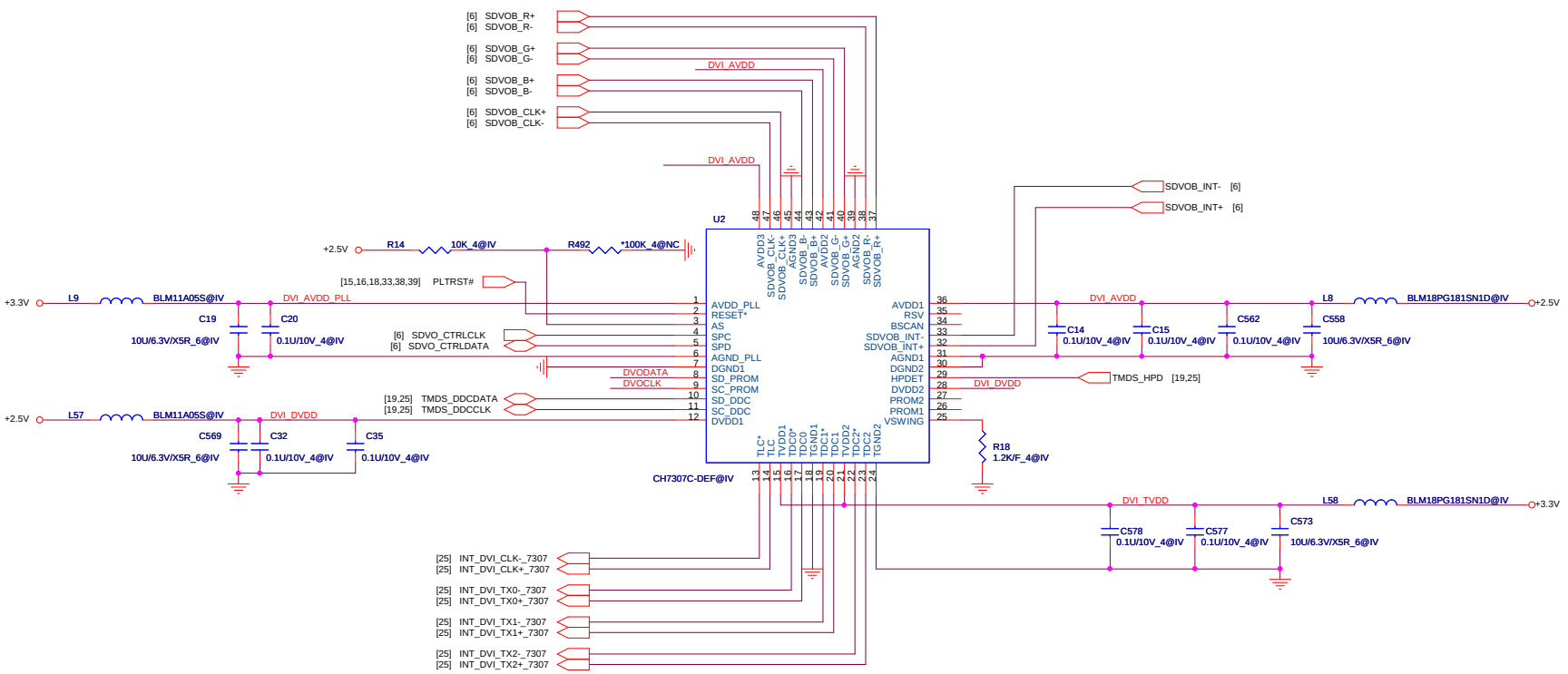


SUPER I/O - PC87383

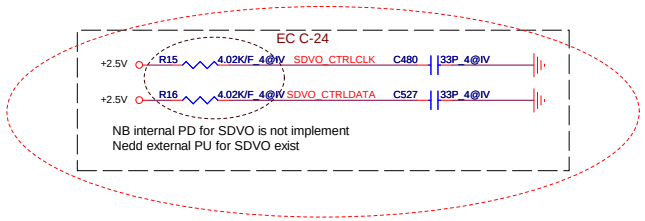


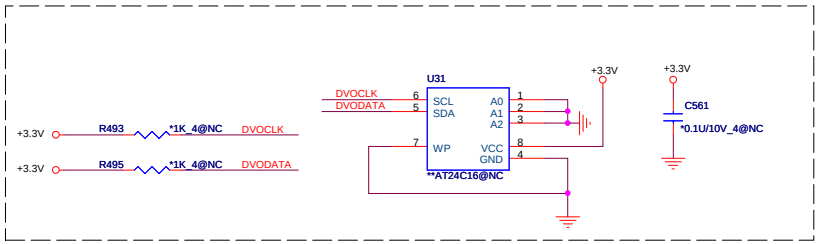


SDVO-DVI



EC B-28





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Quanta Computer Inc.

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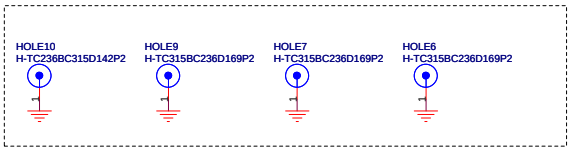

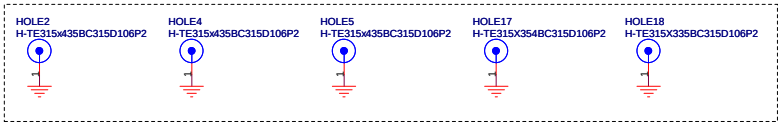

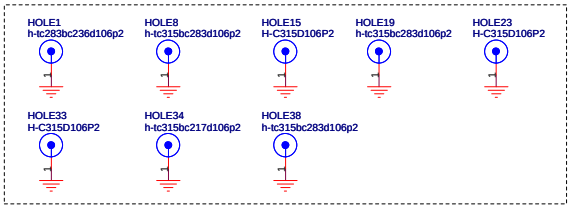

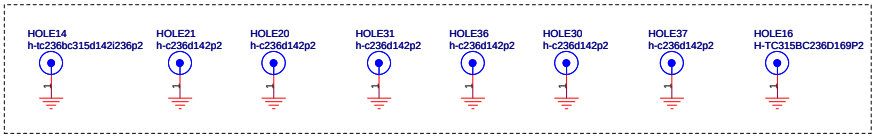

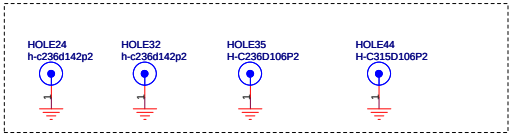

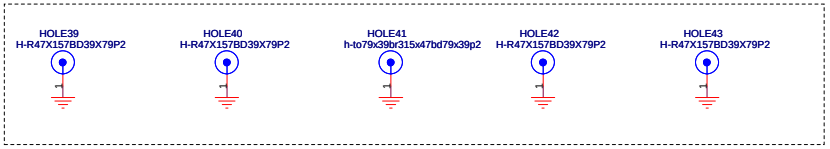

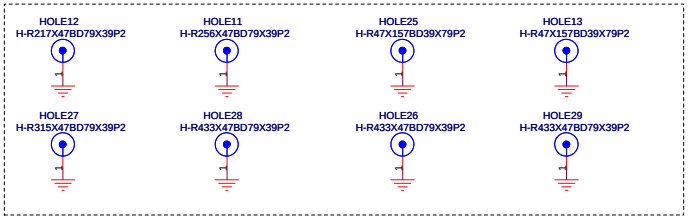

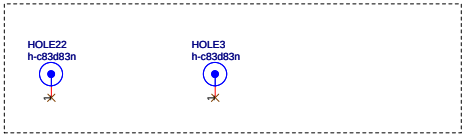

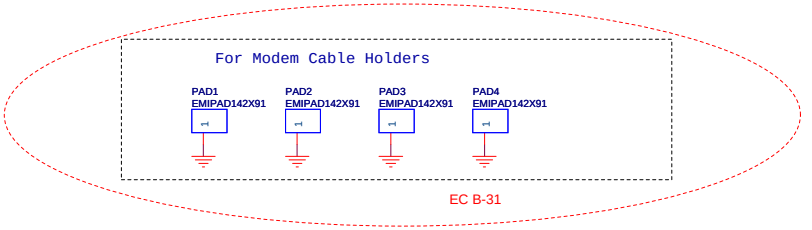

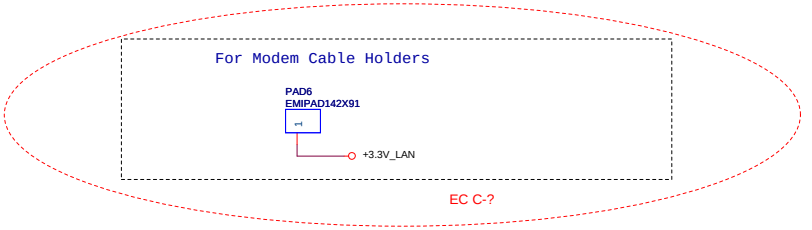

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Quanta Computer Inc.

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	PAD & SCREW	2A
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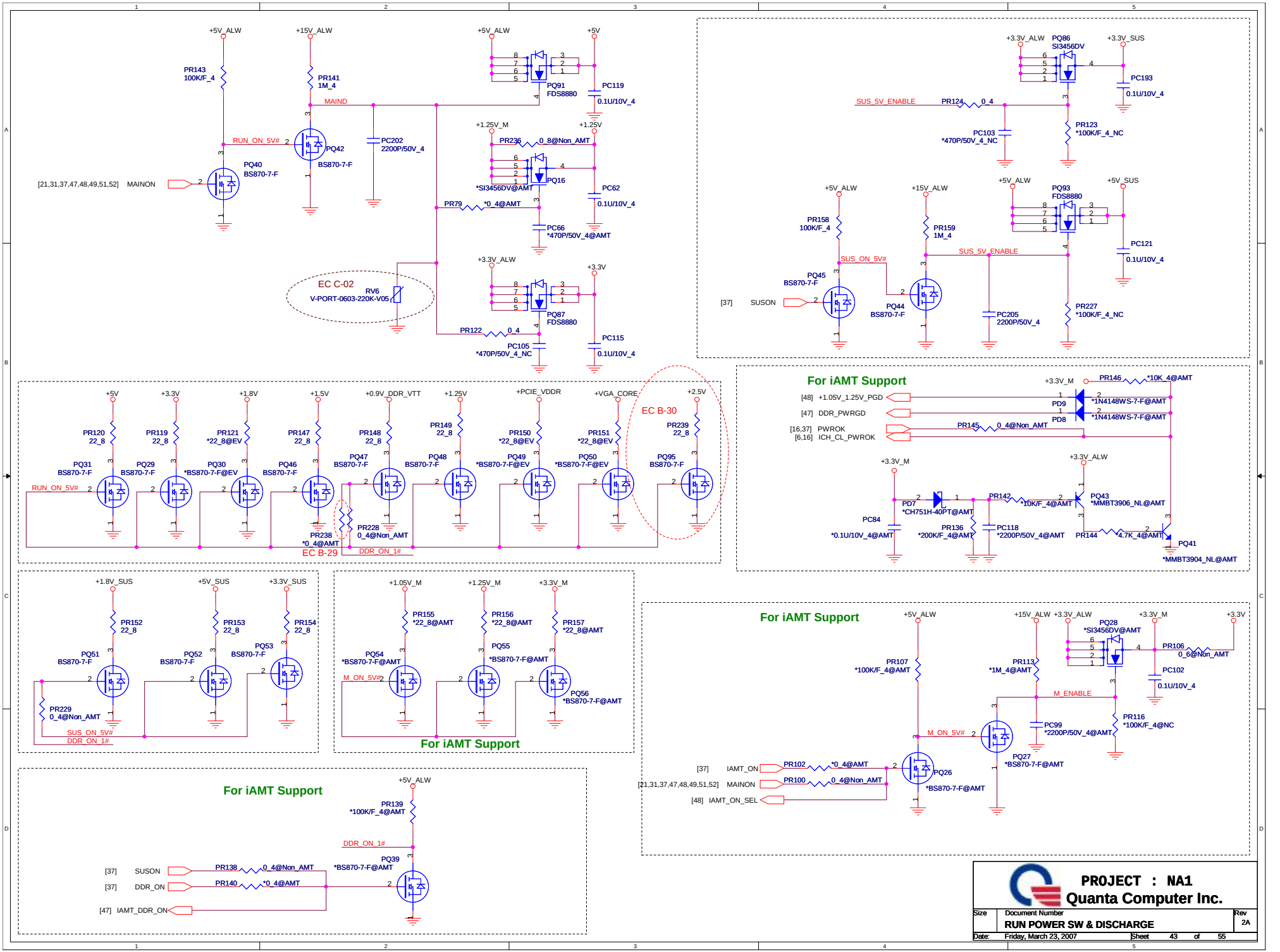

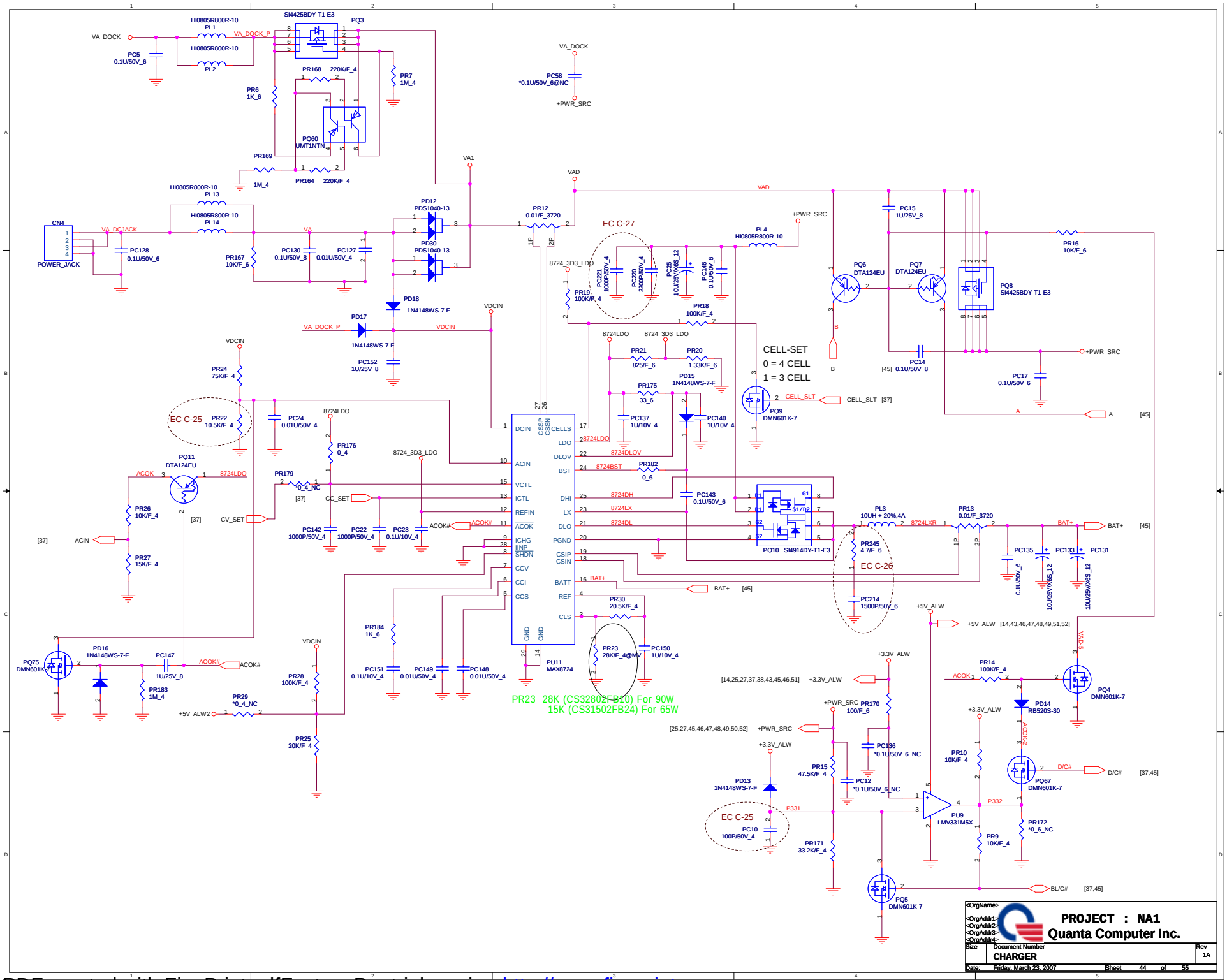

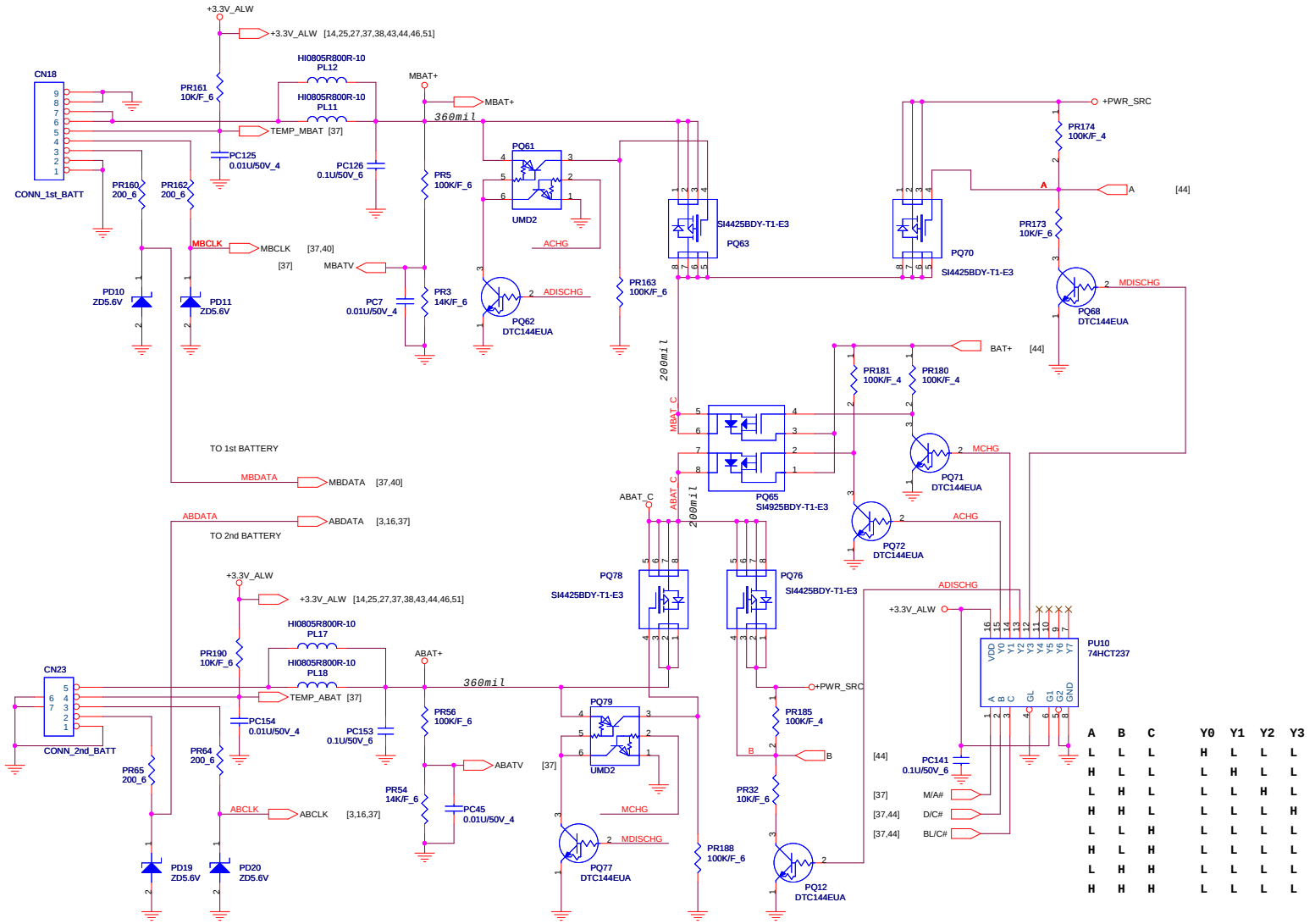

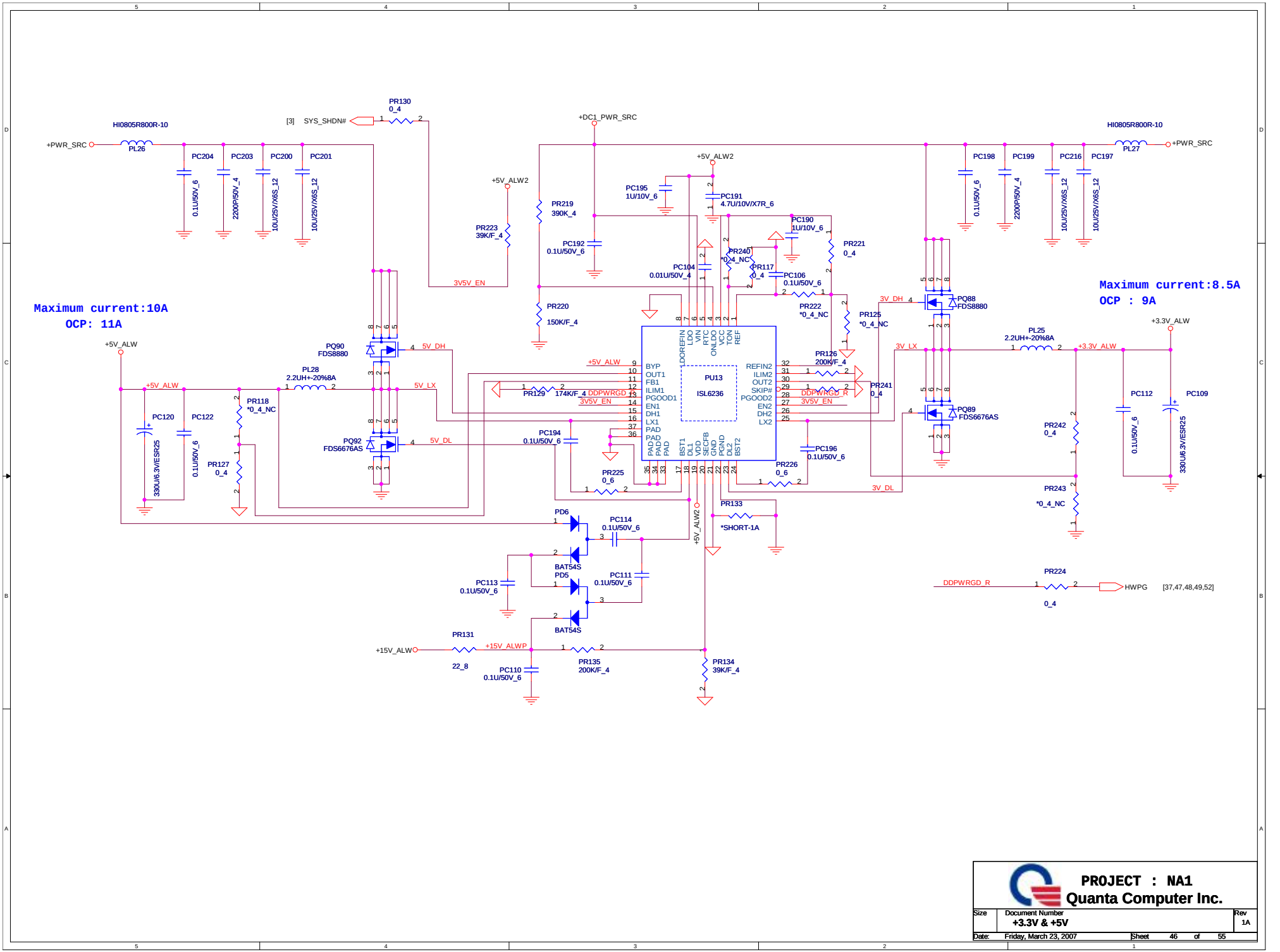

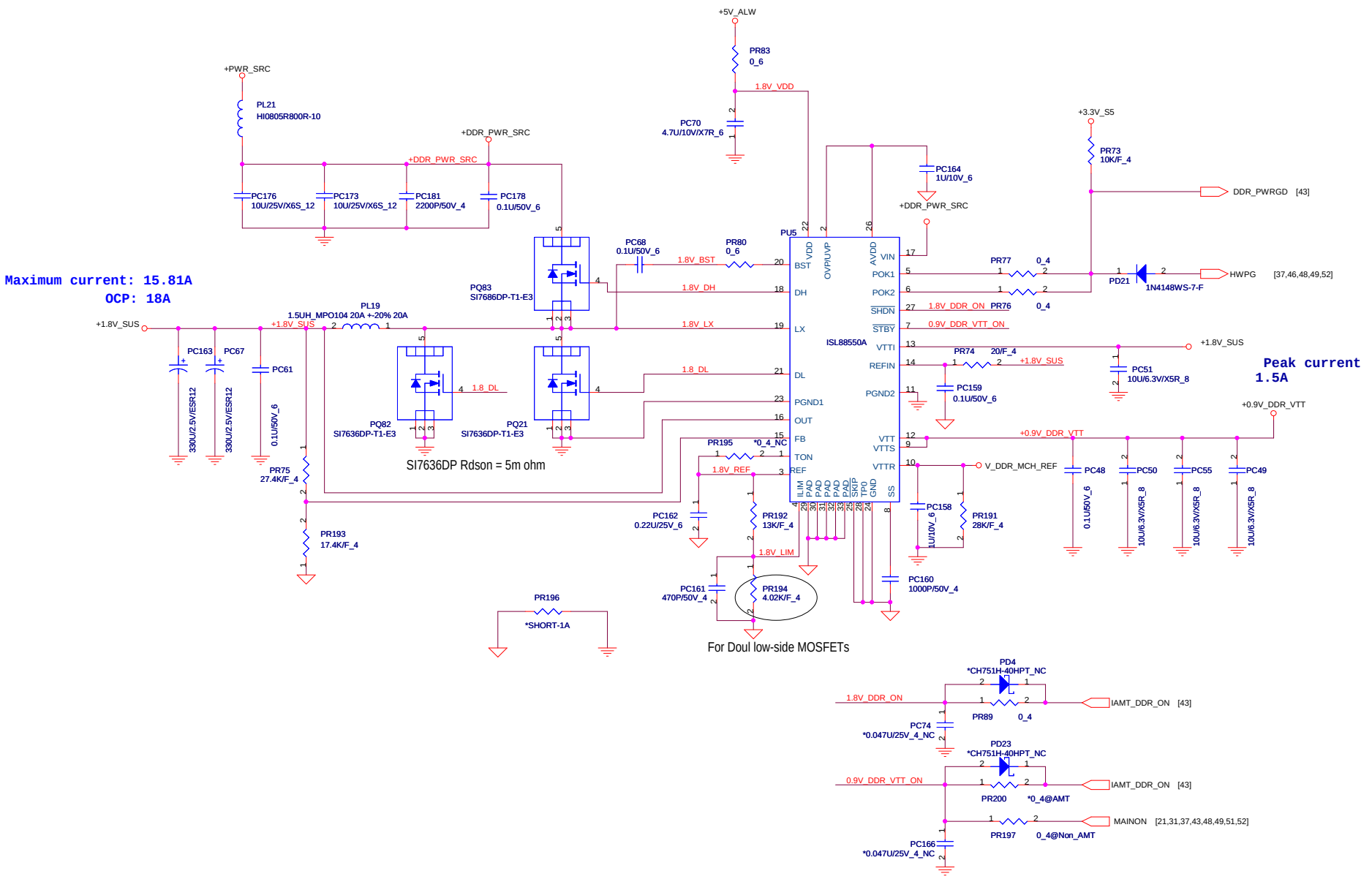

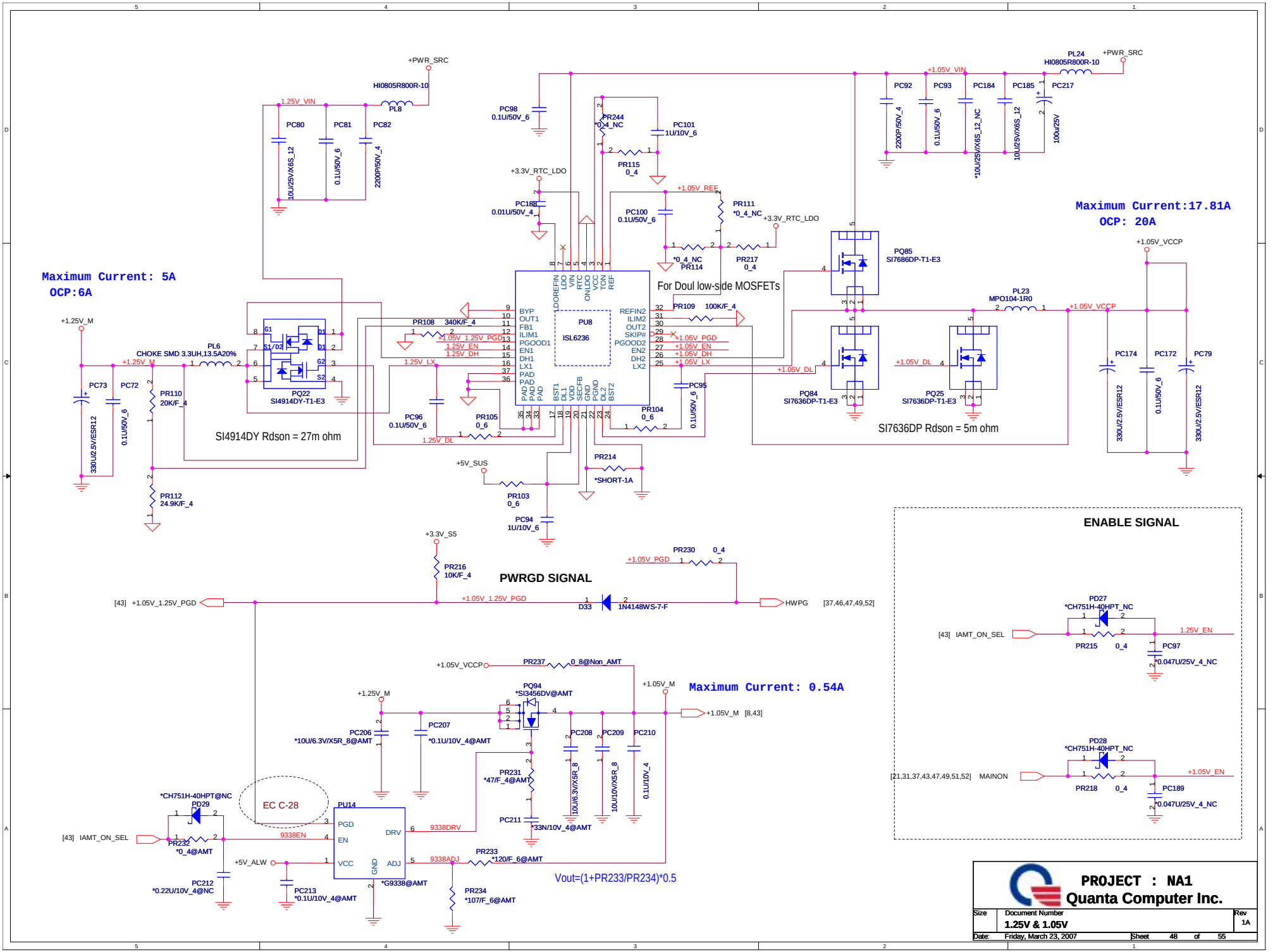

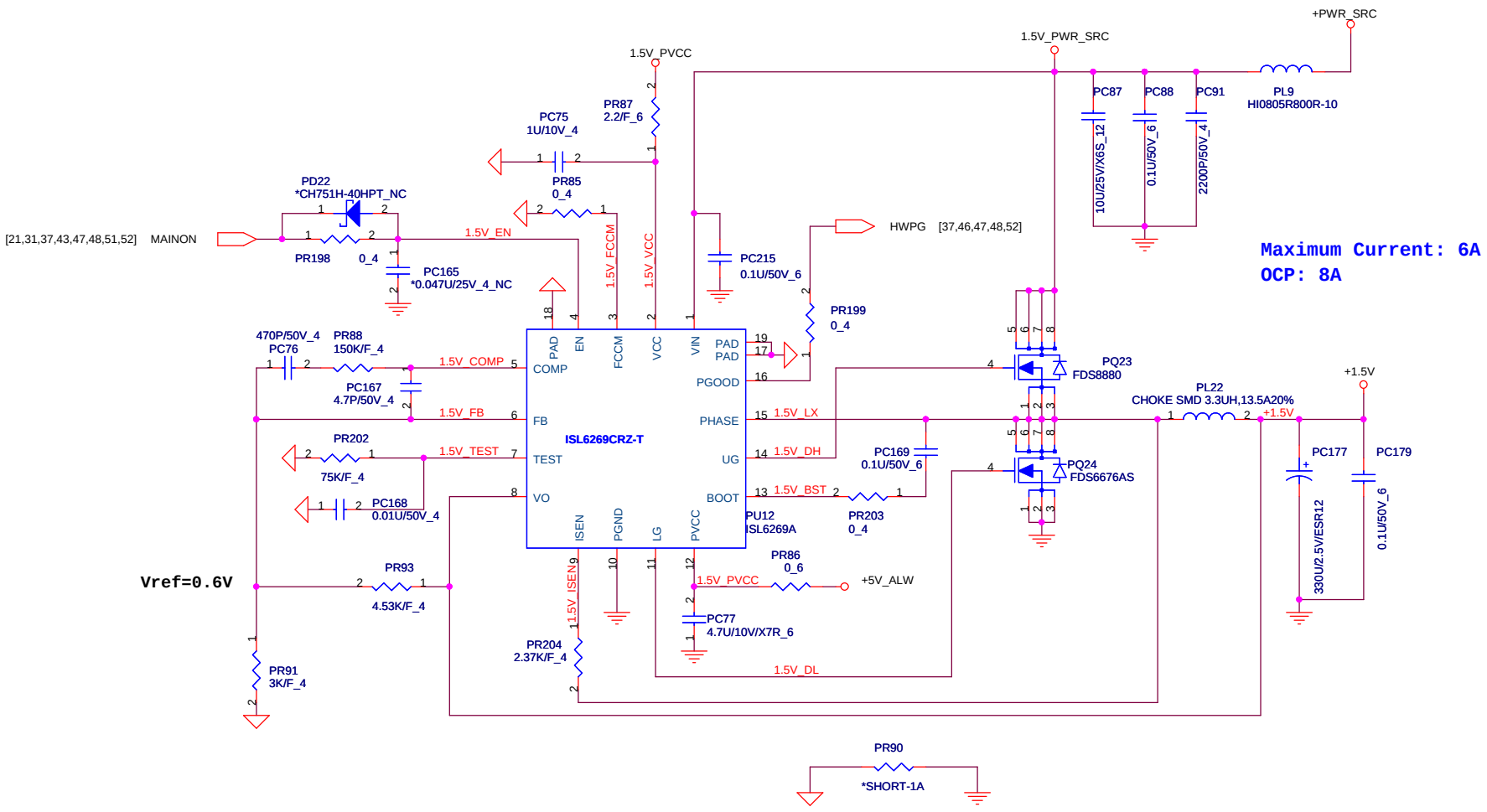

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Quanta Computer Inc.		
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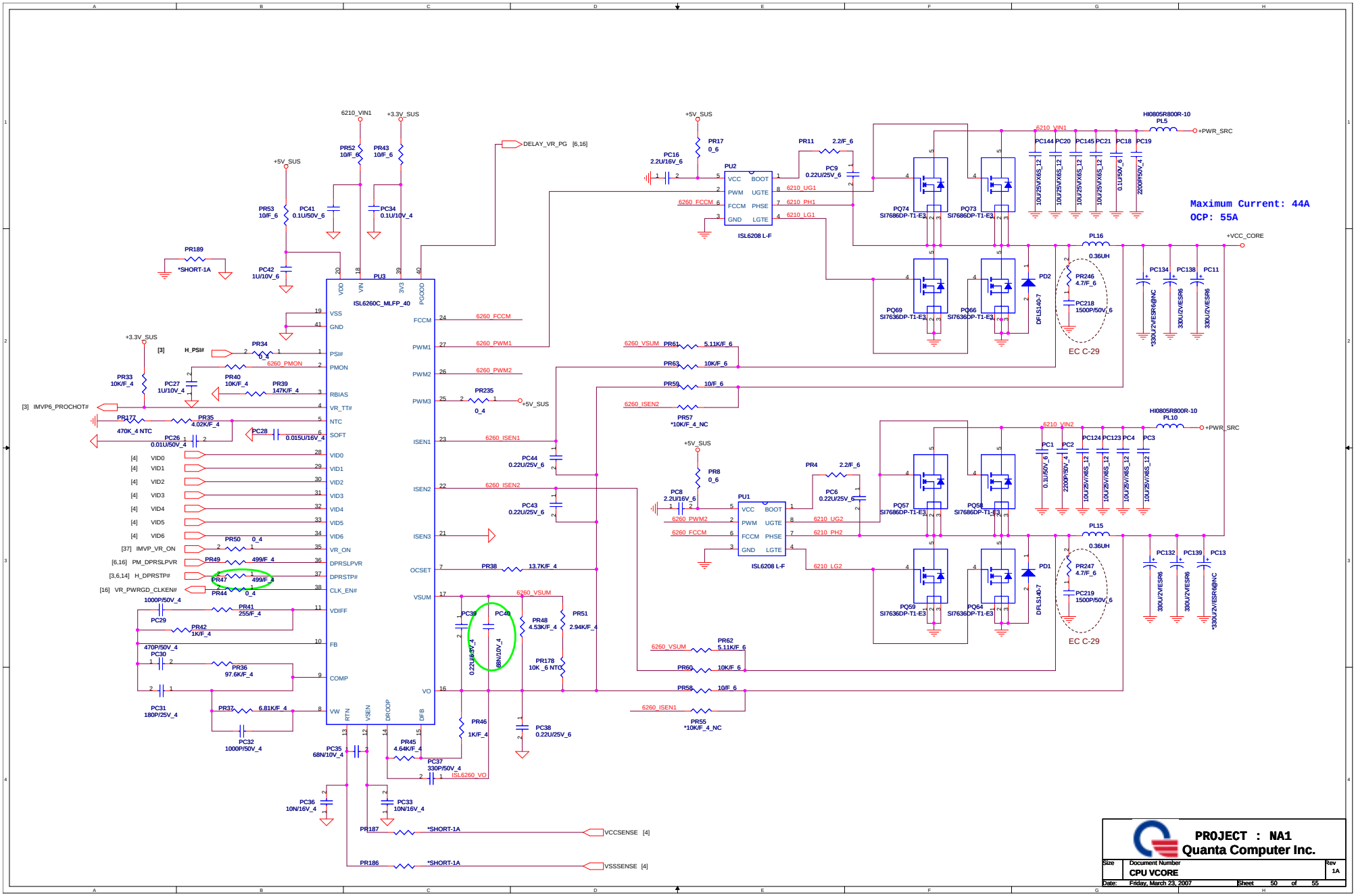

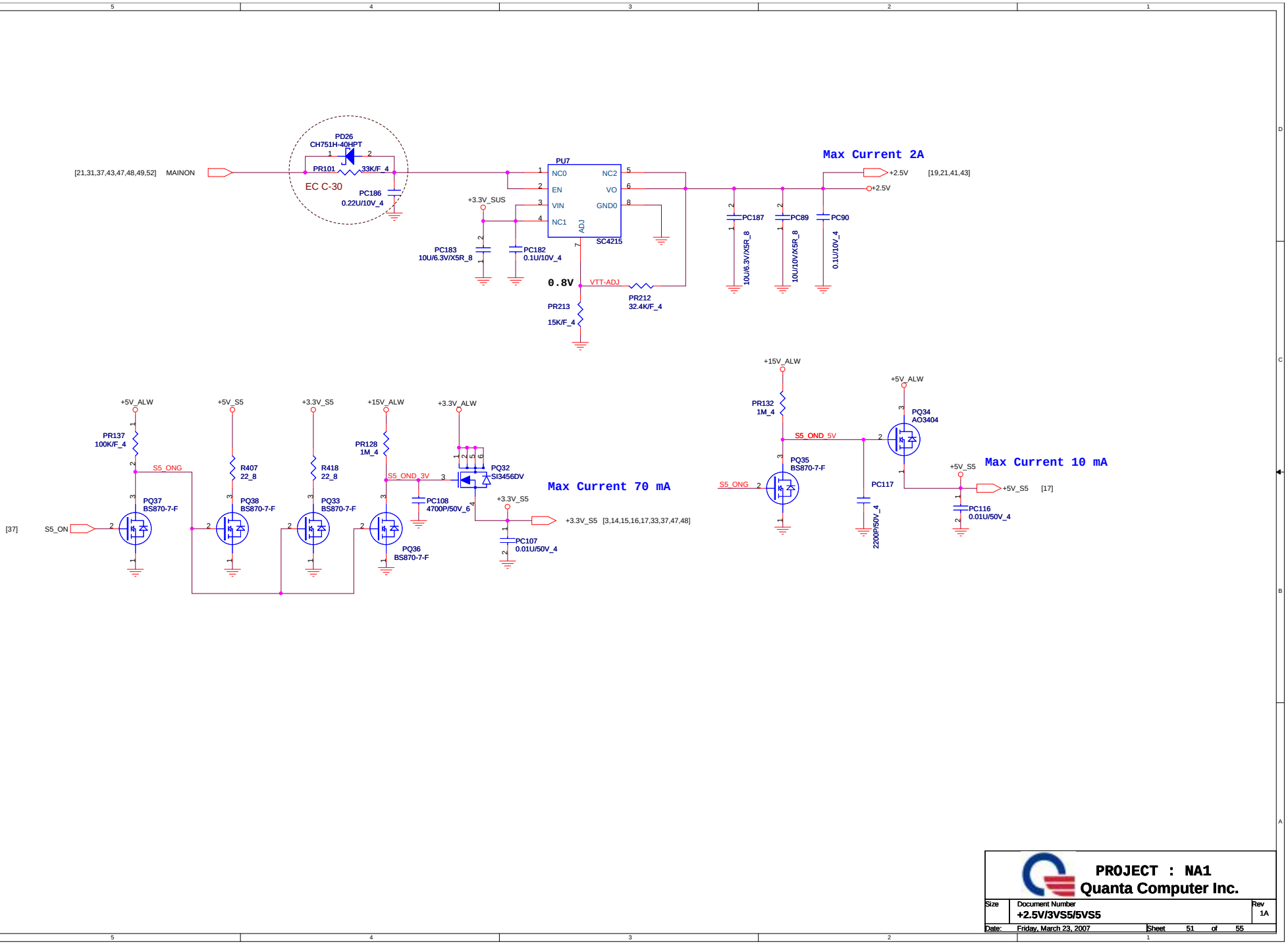

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Quanta Computer Inc.

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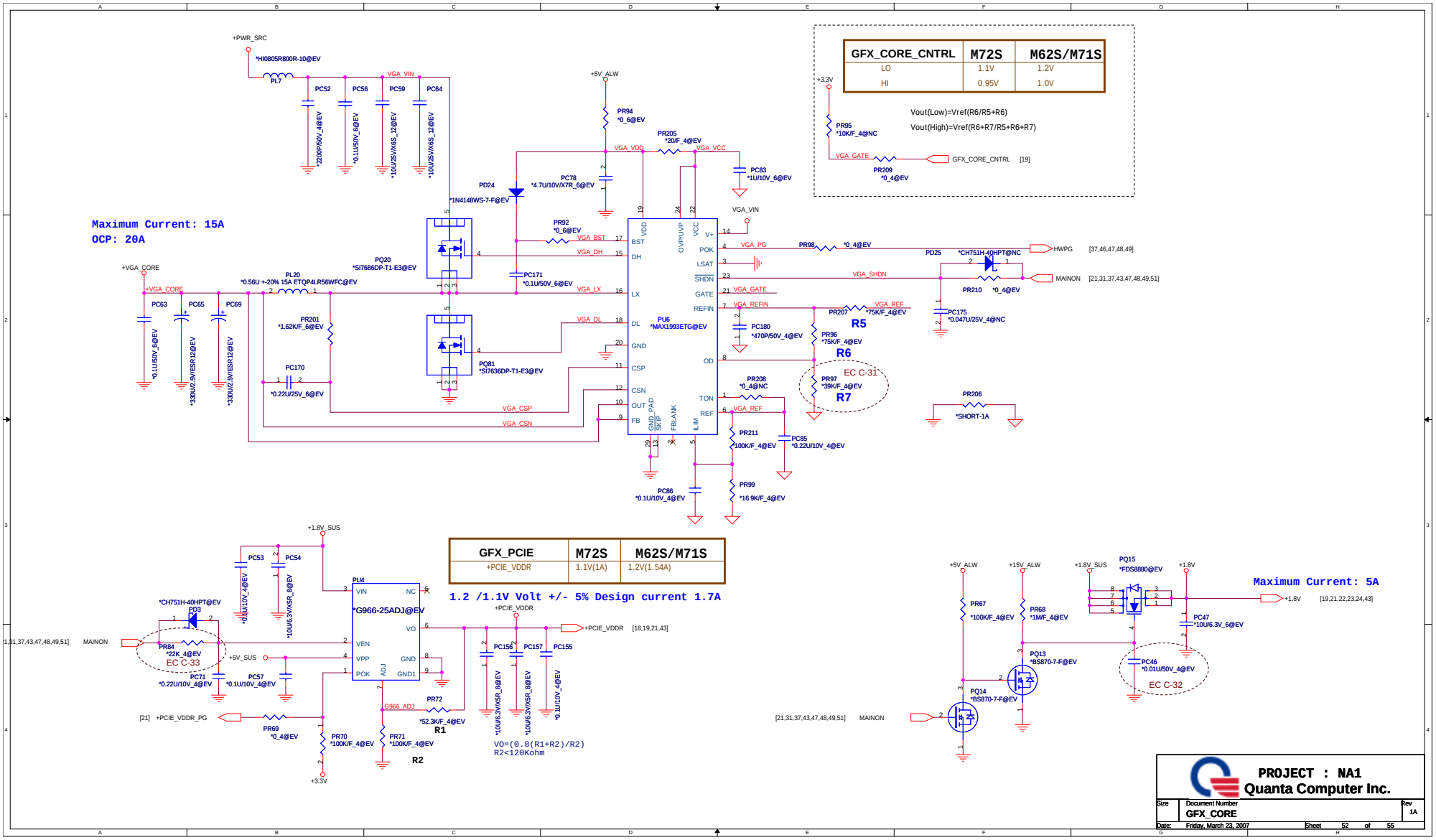

NA1/QA1 Schematic EC Tracking Record B (for A --> B) Nov. 22, 2006
EC #/Page/Description/Part Affected

EC B-01 /02/ Add C528,C530,C534,C830 33pF for EMI issue.
EC B-02 /03/ No_stuff R105_51 on H_RESET# signal for Intel platform request(ITP port unused).
EC B-03 /06/ Change R106,R116 connect From GND to +1.05V_VCCP for Intel design guide Rev_1.3 recommend.
EC B-04 /08/ Delete R496 for PCB layout issue.
EC B-05 /09/ Delete R17,R245 for PCB layout issue.
EC B-06 /09/ Change L60 to 100 and add C481/0.1uF for TV/CRT power VCCD_QDAC ripple issue.
EC B-07 /09/ No_stuff D3,R136 for Double stuff the between +1.05V_VCCP and +3.3V.
EC B-08 /14/ Add R642_0 of reserve for IAMT function request.
EC B-09 /15/ Change BAYINS# signal from GPIO12 to GPIO31pin for IAMT function request.
EC B-10 /16/ Add pull up resister R434,R440_10K of reserve on STP_PCI# & CPU_PCI# signals for IAMT function request.
EC B-11 /16/ Add signal "LAN_PHYPC" on GPIO12 pin for IAMT function request.
EC B-12 /16/ Stuff R607_0 for SATA HDD Modularity.
EC B-13 /19/ Add R245_10K for ATI request.
EC B-14 /25/ Change R157 & R560 from 10K to 8.2K for ATI request.
EC B-15 /26/ Modify CN16 footprint for correct layout.
EC B-16 /27/ Add Q53 for IAMT function request.
EC B-17 /27/ No_Stuff R27 for correct LAN LED indicator.
EC B-18 /28/ Change R511 from 3.92K to 1.4K for Intel platform LAN energy detect circuit request.
EC B-19 /29,30/ Change cardbus controller from Ricoh-R5C853 to TI-PCI7612.
EC B-20 /31/ Move Audio codec & amplifier circuit from Audio board to M/B for EMI issue.
EC B-21 /33/ Add R394 MiniCard WLAN_AUX power connection to +3.3V_S5 for IAMT function request.
EC B-22 /35/ Add EMI filter L12 for EMI issue.
EC B-23 /37/ Change BAYSWAP# signal connection from +3.3V to +3.3V_S5 for Modularity Bay detect.
EC B-24 /38/ Change CN3 Pin definitions for cable assembly issue.
EC B-25 /01/ Add Q52 for correct WLAN LED indicator.
EC B-26 /38/ DeleteQ24,Q25 for correct battery LED indicator.
EC B-27 /01/ Delete R664 for correct power LED indicator.
EC B-28 /41/ Add C480 & C527_33pF for EMI request.
EC B-29 /43/ Add PR238_0 for IAMT function request.
EC B-30 /43/ Add PR239 & PQ95 for +2.5V discharger.
EC B-31 /42/ Add PAD1~PAD5 for modem cable holders.
EC B-32 /38/ Add C660,C756~C758 for EMI request.

	PROJECT : NA1 **Quanta Computer Inc.**	
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NA1/QA1 Schematic EC Tracking Record C (for B --> C) Jan. 17, 2007
EC #/Page/Description/Part Affected

EC C-01 /02/ Re-arrange PCICLK fanout according to Intel design guide recommend.
EC C-02 /03,06,14,25,43/ Add Varistors for ESD.
EC C-03 /13/ Delete C124 due to layout space is tight.
EC C-04 /16/ Add new serial 10K resistor.
EC C-05 /16/ Change pull up from 10K to 1K.
EC C-06 /25/ Q38 from 2N7002W-7-f to PDTC144EU.
EC C-07 /26/ Change D1,D28,D26,D29 to +5V.
EC C-08 /26/ Correct the ESD diode D22,D23,D24 connection.
EC C-09 /26/ L5, L6, L7 change to BK1608LL680.
EC C-10 /21/ L5, L6, L7 Change value and add part for M71-S power sequence.
EC C-11 /26/ S-video connector change to black surface.
EC C-12 /28/ Add C810, C811, C831, C832 1000pF for EMI.
EC C-13 /29/ R694 change to connect +3.3V_SUS.
EC C-14 /29/ Delete CN28 bacause it will no longer be used.
EC C-15 /29/ Add pull-up R736.
EC C-16 /29/ R706 from 2.2K to 10K.
EC C-17 /29/ U45 change from MOSFET to power switch.
EC C-18 /29/ Use 33ohm damping for SD/MMC interface.
EC C-19 /31/ Add 22pF C833~C840 for EMI.
EC C-20 /31/ R387 from 10K to No_stuff to fix DOS mode no sound issue.
EC C-21 /31/ L51 change to BLM21PG600SN1D for EMI.
EC C-22 /35/ L12 USB common mode choke change footprint.
EC C-23 /40/ Q32 From PDTC144EU to 2N7002W-7-F to fix S5 DC-mode leakage.
EC C-24 /41/ R15, R16 4.7K to 4.02K for Intel Design Guide WW48.
EC C-25 /44/ PR22 change from 10K ohm to 10.5K ohm , PC10 change from N.C. to 100pF. Fix shutdown issue when high loading.
EC C-26 /44/ Add snubber PR245, PC214 on charger for EMI.
EC C-27 /44/ Add PC220, PC221 for EMI.
EC C-28 /48/ PU14 Pin3 connect to +1.05V_1.25V_PGD.
EC C-29 /50/ Add snubber PR246, PC218, PR247, PC219 on CPUCORE phase1&2 for EMI.
EC C-30 /51/ PR101 from 27K to 33K , PC186 from 0.1 F to 0.22 F for M71-S power sequence.
EC C-31 /52/ PR97 Please from 16.9K to 39K to set +VGA_CORE=1.2V.
EC C-32 /52/ PC46 from 2200pF to 0.01 F for M71-S power sequence.
EC C-33 /52/ PR84 from 36K to 22K for M71-S power sequence.

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EC D-01 /27/ Follow Intel LAN errata to add a serial 30 ohm resister to the crystal.
EC D-02 /31/ To fix "bo" noise, direct short pin22,23 of MAX9789A, pop R447, depop U24, Q21, Q23, R462, R649.
EC D-03 /31/40 Using cable to connect line-out function instead of route on PCB.
EC D-04 /26 Remove L1, L2, L3 because it's easily crack. EMI confirm it's ok.
EC D-05 /40 Add EMI solution for Docking LAN port.
EC D-06 /33 Directly connect the ICH_SMBus to MINIPCI-e.
EC D-07 /36 Delete U27 releated circuit for layout space issue.
EC D-08 /09 VCCA_DAC_BG follow intel circuit to fix CRT waving issue.

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