QT8G SYSTEM DIAGRAM

AMD Smarter Choice

01

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : IN3
LAYER 7 : SGND1
LAYER 8 : BOT

DDRII-SODIMM1 PAGE 7,8 — DDRII 667/800 MHz
DDRII-SODIMM2 PAGE 7,8 — DDRII 667/800 MHz

AMD Griffin Lion Sabie
S1G2 Processor
638P (uPGA)/35W
PAGE 3,4,5,6

CPU THERMAL SENSOR PAGE 5

14.318MHz

CLOCK GEN
ICS9LPRS476AKLFT-->HP
SLG8SP626VTR-->HP
RTM880N-795 -->HP
PAGE 2

CPU_CLK
NBGFX_CLK
NBGPP_CLK
SBLINK_CLK

HT3

PCI-E

NORTH BRIDGE
RX781 A13
21mm X 21mm, 528pin BGA
PAGE 8,9,10,11,

PCI-Express 16X

HDMI PAGE 23
CRT PAGE 24
LVDS PAGE 23

M86-ME
64 Bit,DDR2*4
PAGE 17,18,19 20,21,22,23
SBSRC_CLK

Cable Docking PAGE 37
VGA
RJ-45
CIR/Pwr btn
SPDIF Out
Stereo MIC
Headphone Jack
USB Port
VOL Cntr

X1 LAN Realtek PCIE-LAN RTL8102E/8111C (10/100/GagaLAN) PAGE 31,32
X1 Express Card (NEW CARD) PAGE 33
X3 Mini PCI-E Card (Wireless LAN/TV TUNNER) PAGE 36

RJ45 PAGE 31

10 PCI-E WLAN Card x1 PAGE 36
11 TV-TUNER Card x1 PAGE 36
7 Express Card x1 PAGE 33
4 Cable Docking x1 PAGE 37

ALINK X4

SYSTEM CHARGER(ISL6251A) PAGE 44
SYSTEM POWER ISL6236IRZA-T PAGE 38
DDR II SMDDR_VTERM 1.8V/1.8VSUS(TPS51116REGR) PAGE 41
VCCP +1.1V AND +1.2V(MAX8717) PAGE 39
VGACORE(1.1V~1.2V)Oz8118 PAGE 42
CPU CORE ISL6265A PAGE 40

TWO SATA - HDD PAGE 33 — SATA0,1 150MB
SATA - CD-ROM PAGE 33 — SATA0 150MB
E-SATA PAGE 30 — SATA4 150MB

SOUTH BRIDGE
SB700 A12
21mm X 21mm, 528pin BGA
4.5W(Ext)
4.3W(Int)
PAGE 12,13.14.15.16

USB2.0
1,8,9 USB2.0 Ports X3 PAGE 30
5 Blueflame PAGE 30
2 Webcam X1 PAGE 30
6 Fingerprint PAGE 30
3 Flash Media for UMA only RTS5158 PAGE 25
Touch Screen for Discrete only

PCIE BUS
JMICRON JMD380 for Discrete only PAGE 27

Azalia

SMBUS
Accelerometer LIS3LV02DL PAGE 28
Keyboard PAGE 34
Touch Pad PAGE 34
CIR (AUDIO CONN) PAGE 27
Capacitive Sense SW PAGE 34

LPC

ENE KBC
KB3926 Cx
PAGE 35

MDC CONN PAGE 29

IDT 92HP61B7 PAGE 27

AUDIO Amplifier TPA6017A2 PAGE 28

IEEE1394 connect for Discrete only PAGE 26

Memory CardReader PAGE 25

Digital MIC PAGE 30
AUDIO CONN (Phone/ MIC) PAGE 27
Audio Conn PAGE 28

FAN PAGE 37
SPI PAGE 35

SMBUS TABLE		
SB--SCL0/SD0	Clock gen/Robson/TV tuner /DDR2/DDR2 thermal/Accelerometer	+3V
	epress card Wlan Card	+3VS5
EC --SCL/SD	Battery charge/discharge	+3VPCU
EC--SCL2/SD2	VGA thermal/system thermal	+3V

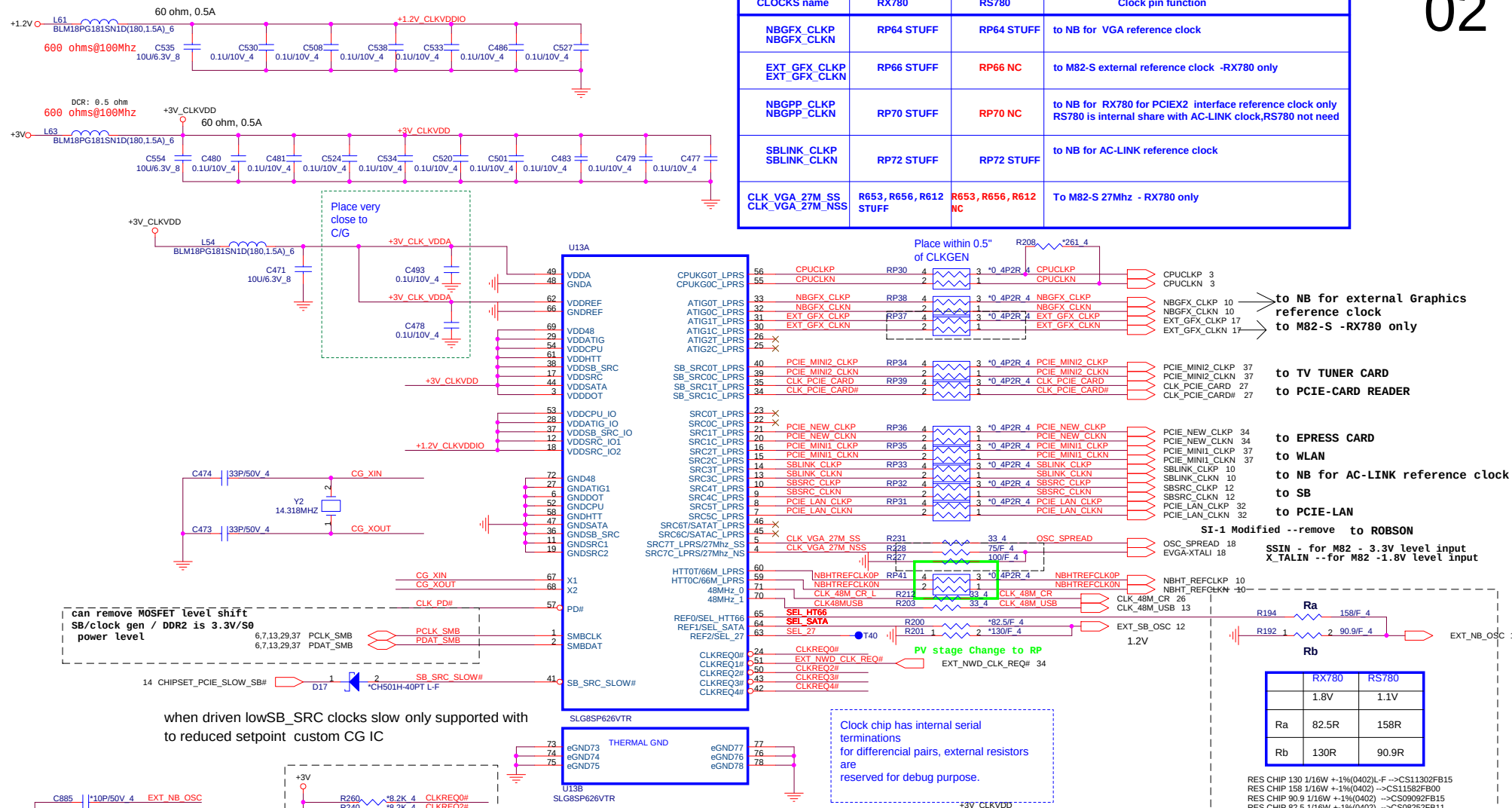
NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size Custom | Document Number Block Diagram | Rev 1A
Date: Friday, August 29, 2008 | Sheet 1 of 46

http://mycomp.su/x/

CLOCKS name	RX780	RS780	Clock pin function
NBGFX_CLKP NBGFX_CLKN	RP64 STUFF	RP64 STUFF	to NB for VGA reference clock
EXT_GFX_CLKP EXT_GFX_CLKN	RP66 STUFF	RP66 NC	to M82-S external reference clock -RX780 only
NBGPP_CLKP NBGPP_CLKN	RP70 STUFF	RP70 NC	to NB for RX780 for PCIEX2 interface reference clock only RS780 is internal share with AC-LINK clock,RS780 not need
SBLINK_CLKP SBLINK_CLKN	RP72 STUFF	RP72 STUFF	to NB for AC-LINK reference clock
CLK_VGA_27M_SS CLK_VGA_27M_NSS	R653,R656,R612 STUFF	R653,R656,R612 NC	To M82-S 27Mhz - RX780 only



* default

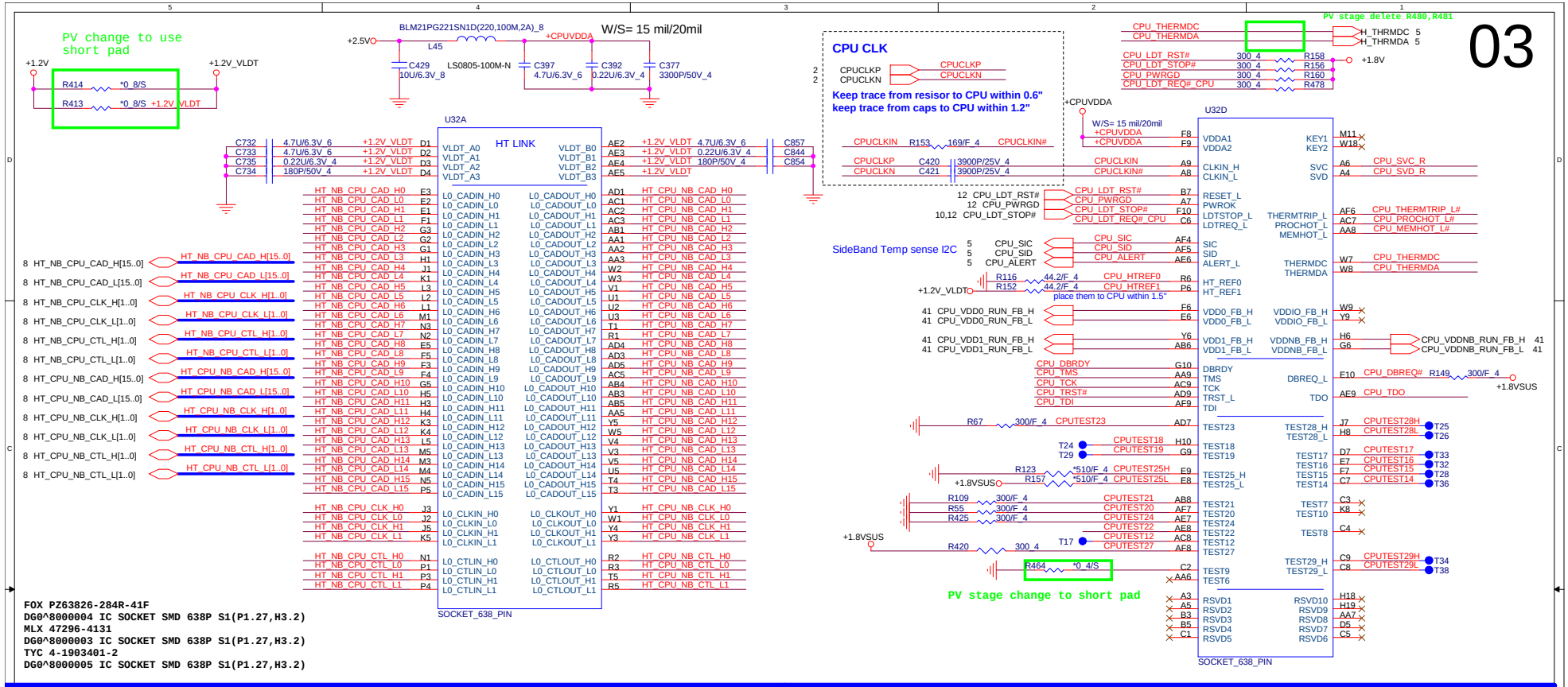
SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1	100 MHz non-spreading differential SRC clock
	0*	100 MHz spreading differential SRC clock
SEL_27	1*	27MHz non-spreading singled clock
	0	100 MHz spreading differential SRC clock

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Clock Generator	1A

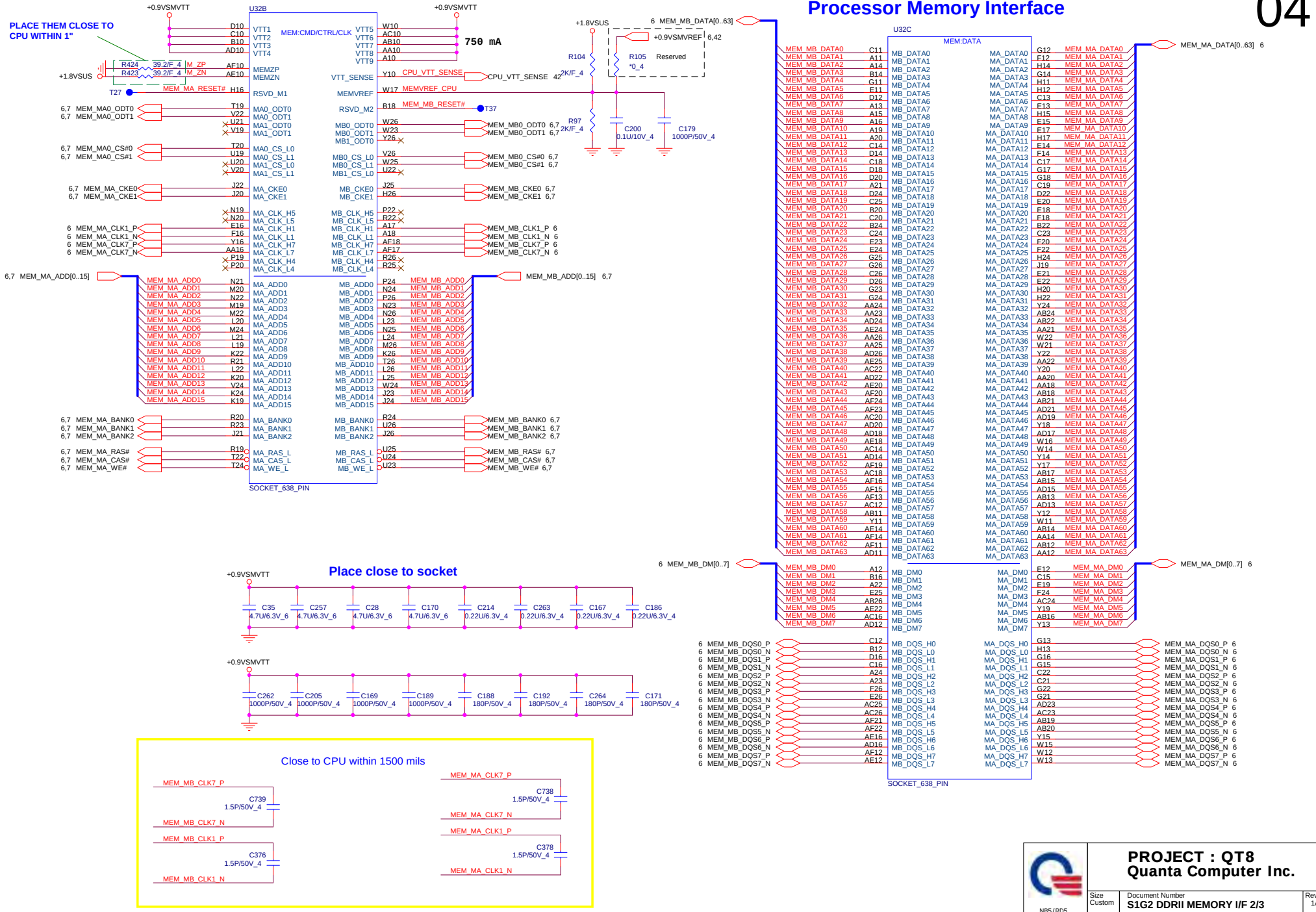
Date: Friday, August 29, 2008 Sheet 2 of 46

http://mycomp.su/x/



http://mycomp.su/x/

Processor Memory Interface



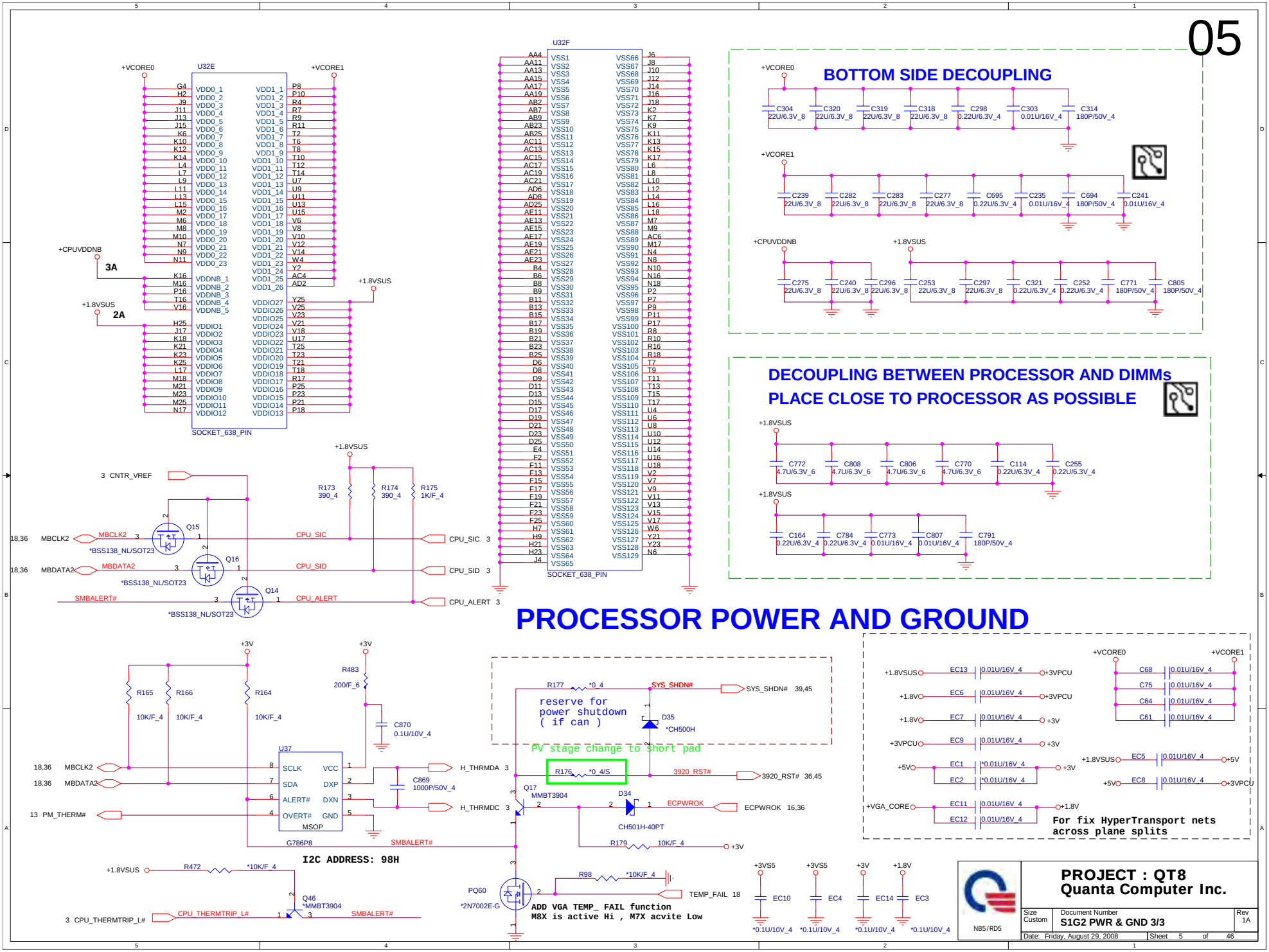
PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	S1G2 DDRII MEMORY I/F 2/3	1A

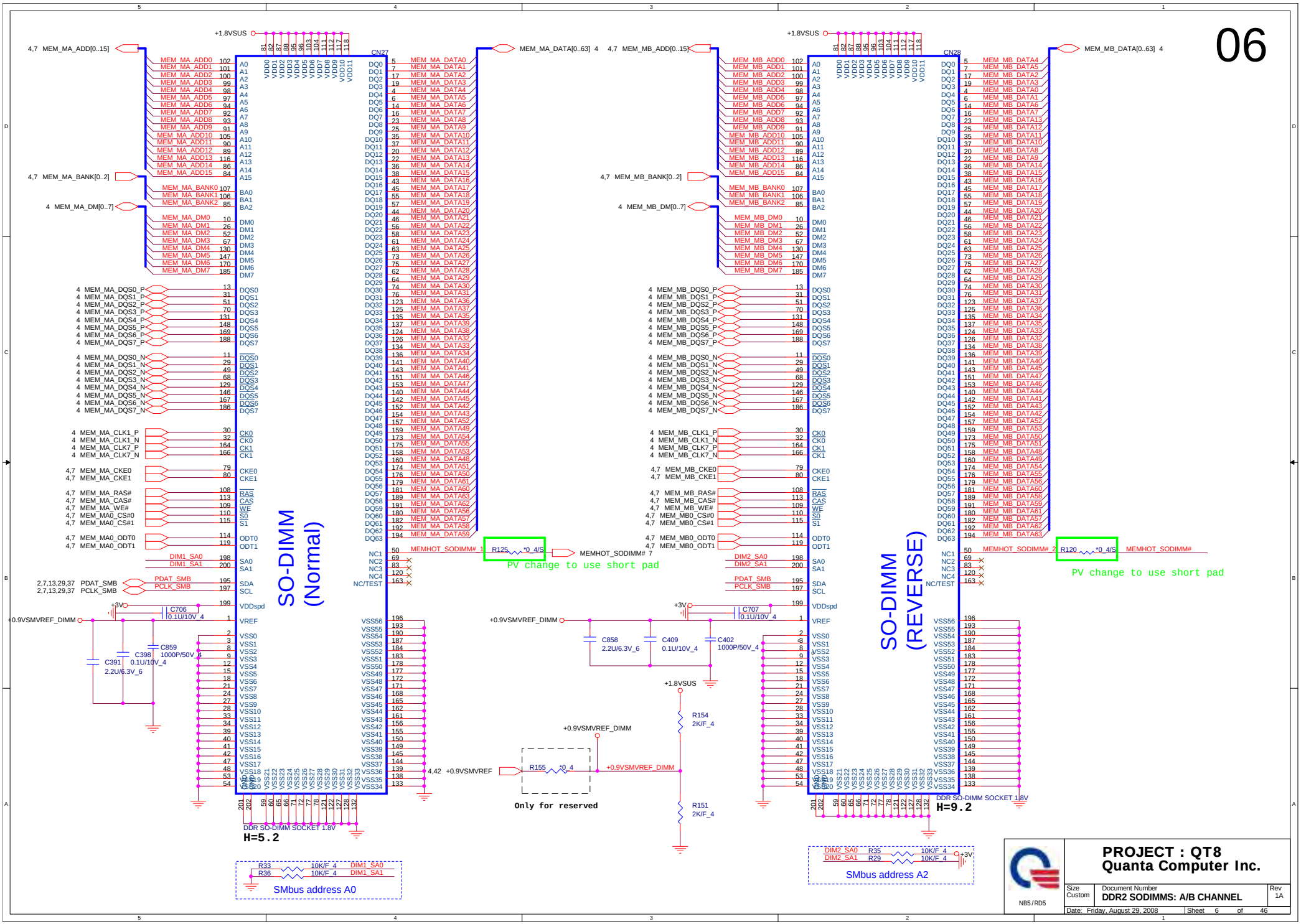
NB5/RD5

Date: Friday, August 29, 2008 Sheet 4 of 46

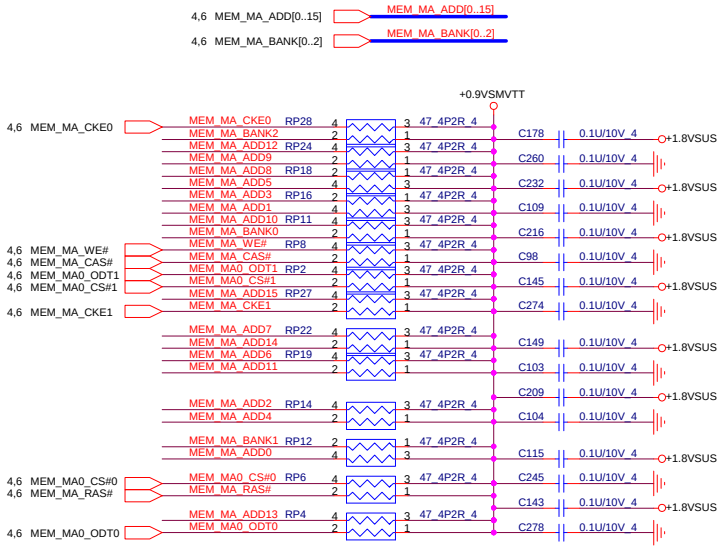
http://mycomp.su/x/

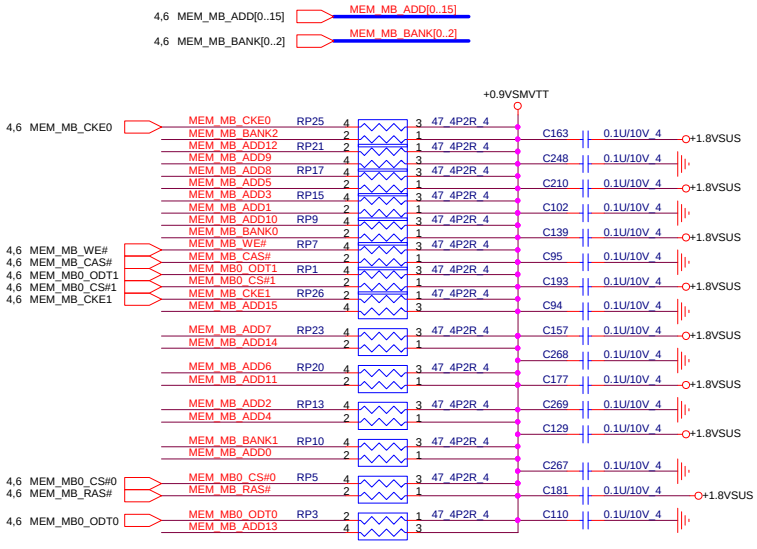


http://mycomp.su/x/

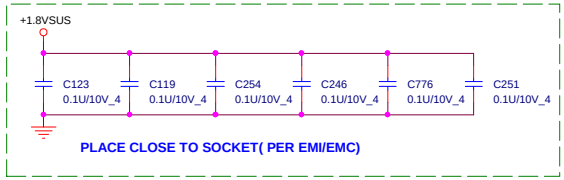


http://mycomp.su/x/

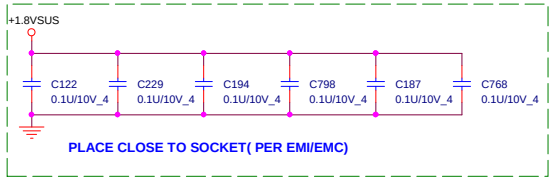


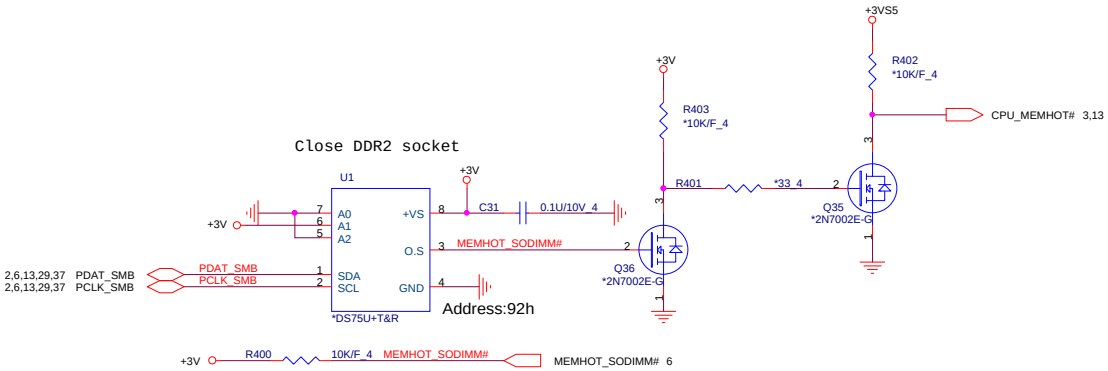


PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH



PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH





NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR2 SODIMMS TERMINATIONS	1A

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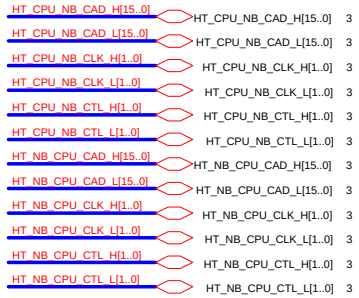
http://mycomp.su/x/

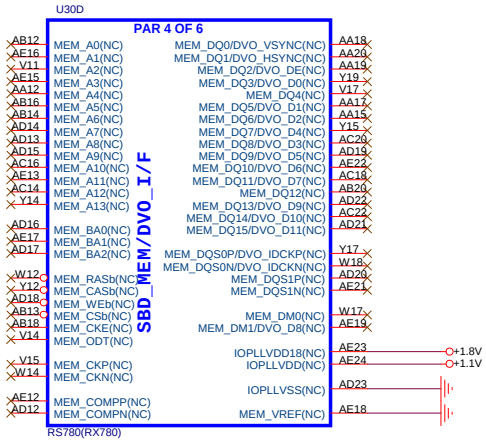


signals	RS780	RX780
HT_TXCALP	R641 301 ohm 1%	R641 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	R655 301 ohm 1%	R655 1.21k ohm 1%
HT_RXCALN		

RES CHIP 1.21K 1/16W +-1%(0402)
P/N : CS21212FB18

RES CHIP 301 1/16W +-1%(0402)
P/N : CS13012FB14

This block is for side port memory only



IOPLLVDD18 - memory PLL not applicable to RX780

IOPLLVDD- memory PLL not applicable to RX780

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS740/RS780-HT LINK I/F 1/5	1A

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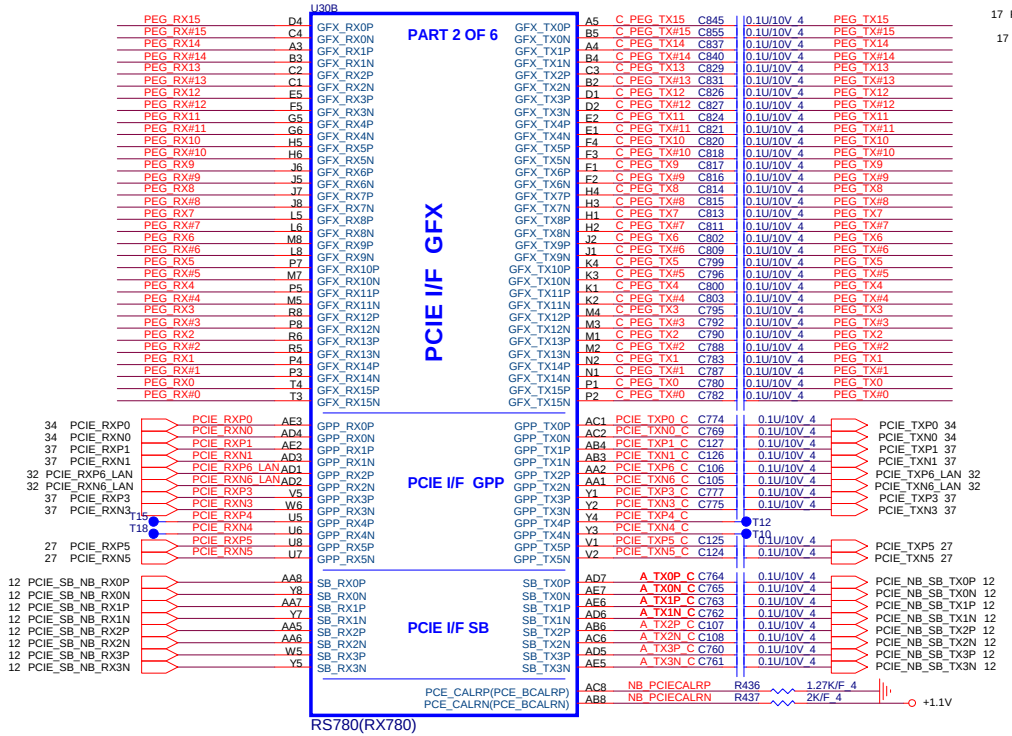
http://mycomp.su/x/



17 PEG_RX#[15:0] PEG_RX#[15:0]
17 PEG_RX[15:0] PEG_RX[15:0]
PEG_TX#[15:0] PEG_TX#[15:0] 17
PEG_TX[15:0] PEG_TX[15:0] 17

Close to North Bridge

TO EPRESS CARD

TO WLAN

TO PCIE-LAN

TO TV TUNNER

TO PCIE CARD READER

RX780/RS740/RS780 difference table (PCIE LINK)

	RS740	RX780/RS780
NB_PCIECALRP	562R (GND)	1.27K (GND)
GPP4	NC	GPP4
GPP5	NC	GPP5

RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

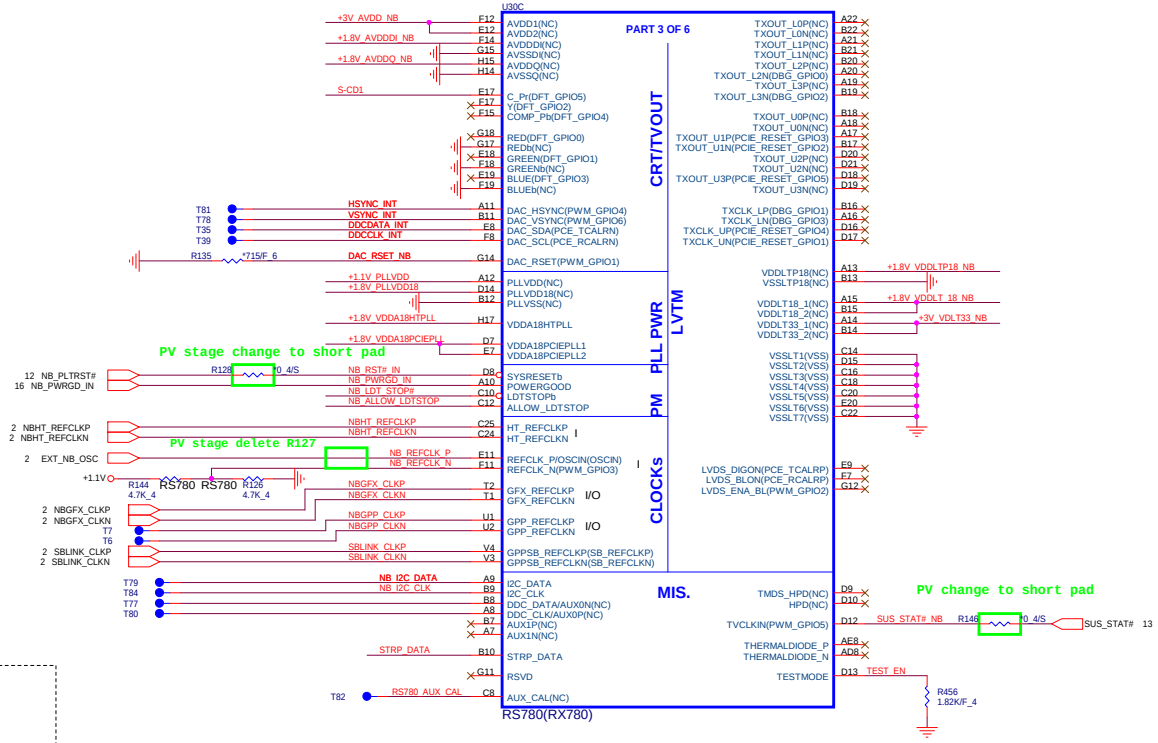
NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS740/RS780-PCIE I/F 2/5	1A

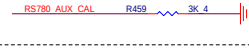
Date: Friday, August 29, 2008 Sheet 9 of 46

http://mycomp.su/x/



selects Loading of straps from
EPROM
1 : use default vaule , default
0 : I2C Master can load strap
values from EEPROM
if connected, or use default
values if not connected
RX780 --RS780_AUX_CAL
RS780 -- SUS_ATAT

RX780

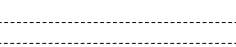


Enables Debug Bus acess
through memory T/O pads and GPIO.
0 : Enable RS780 , Default
1 : Disable RS780
(RS780 use VSYNC#)

RS780

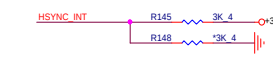
Indicates if memory Side port
is available or not
0: available RS780 , Default
1: Not available RS780
(RS780 use HSYNC#)

RS780



For extrnal EEPROM Debug only

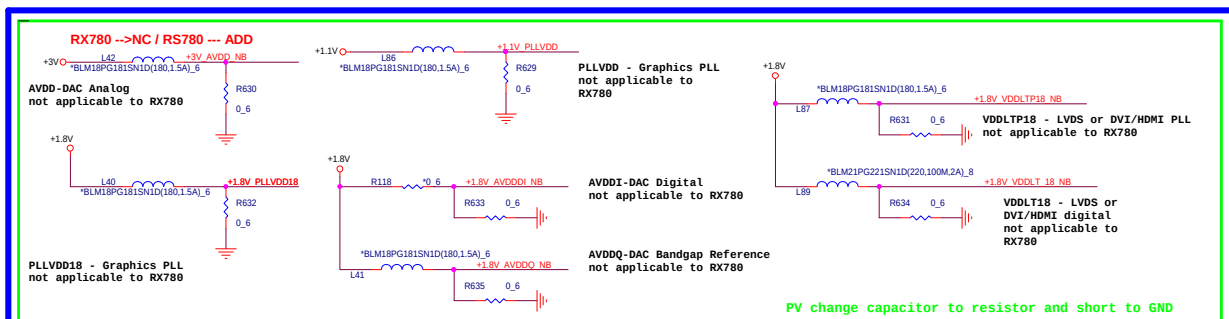
RS780/RX780

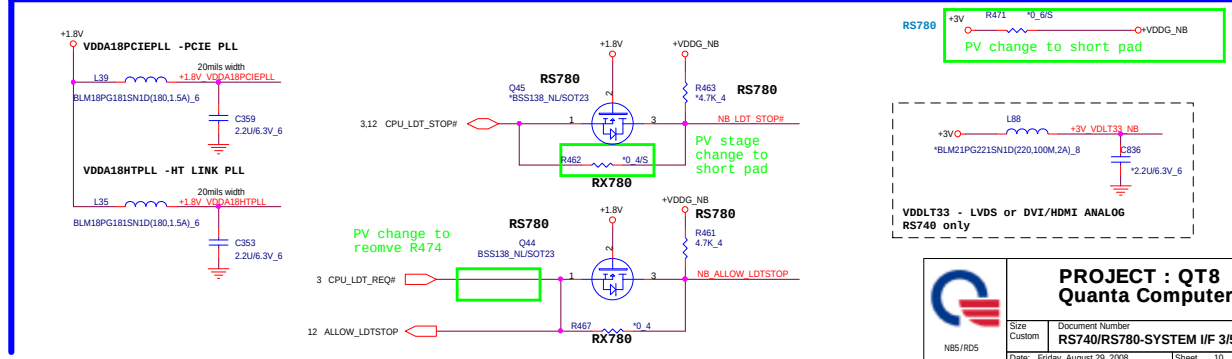


Enables Debug Bus acess
through memory T/O pads and GPIO.
1 : Enable RX780 , Default
0 : Disable RX780

RX780

Reserved only





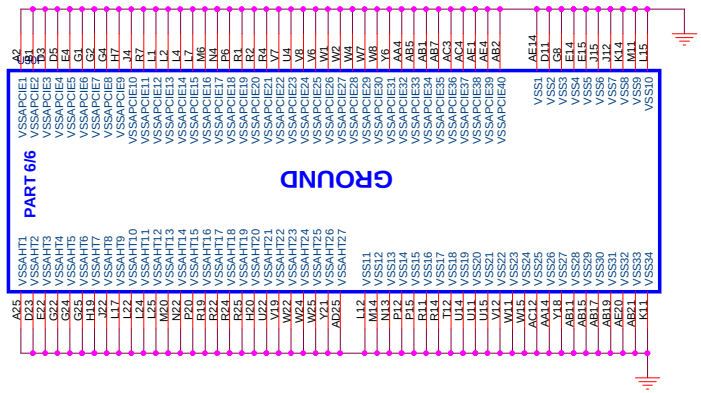
PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS740/RS780-SYSTEM I/F 3/5	1A

Date: Friday, August 29, 2008 Sheet 10 of 46

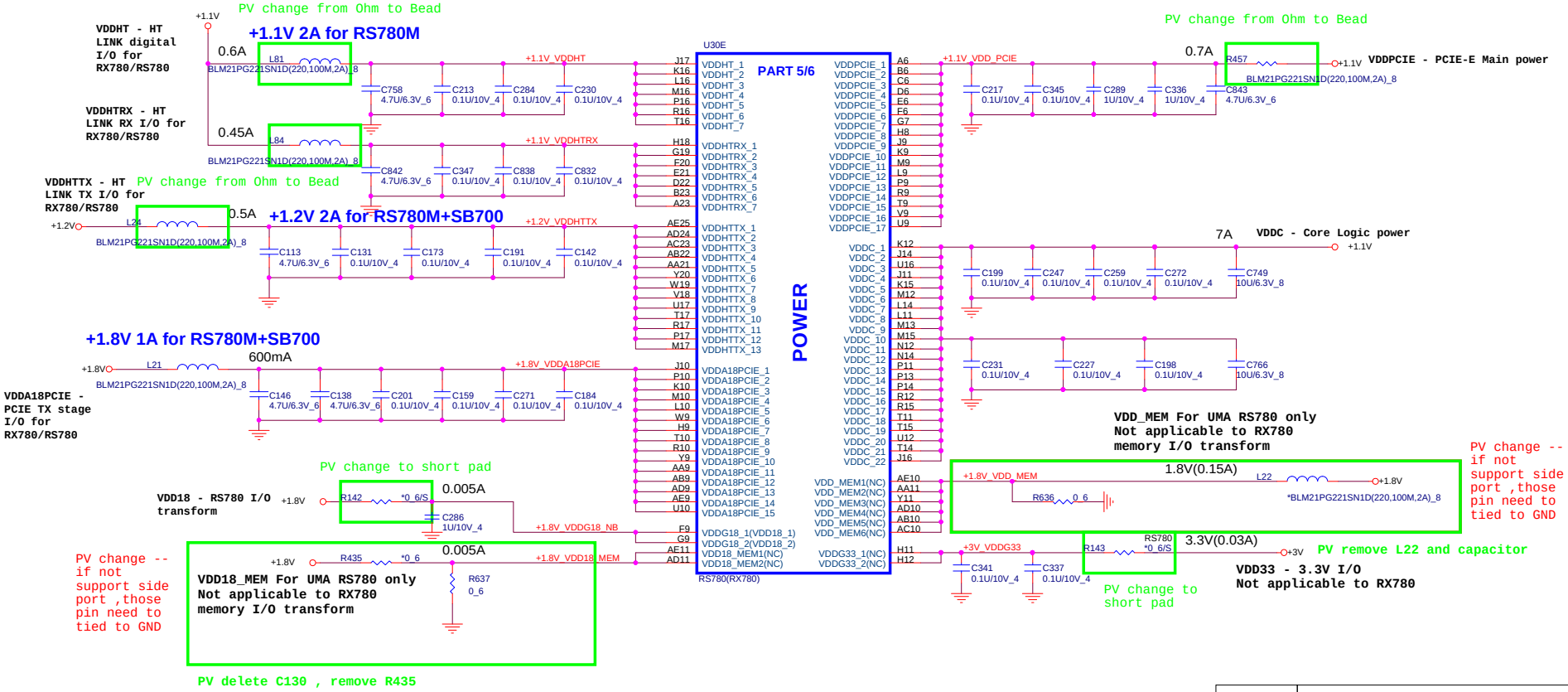
NB5/RD5

http://mycomp.su/x/



RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RX780	RS780	PIN NAME	RX780	RS780
VDDHT	+1.1V	+1.1V	IOPLLVDD	NC	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	NC	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	NC	+1.8V
VDDG18	+1.8V	+1.8V	PLLVDD	NC	+1.1V
VDD18_MEM	NC	+1.8V	PLLVDD18	NC	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	NC	+1.8V/1.5V	VDDLTP18	NC	+1.8V
VDDG33	NC	+3.3V	VDDLT18	NC	+1.8V
IOPLLVDD18	NC	+1.8V	VDDLT33	NC	NC



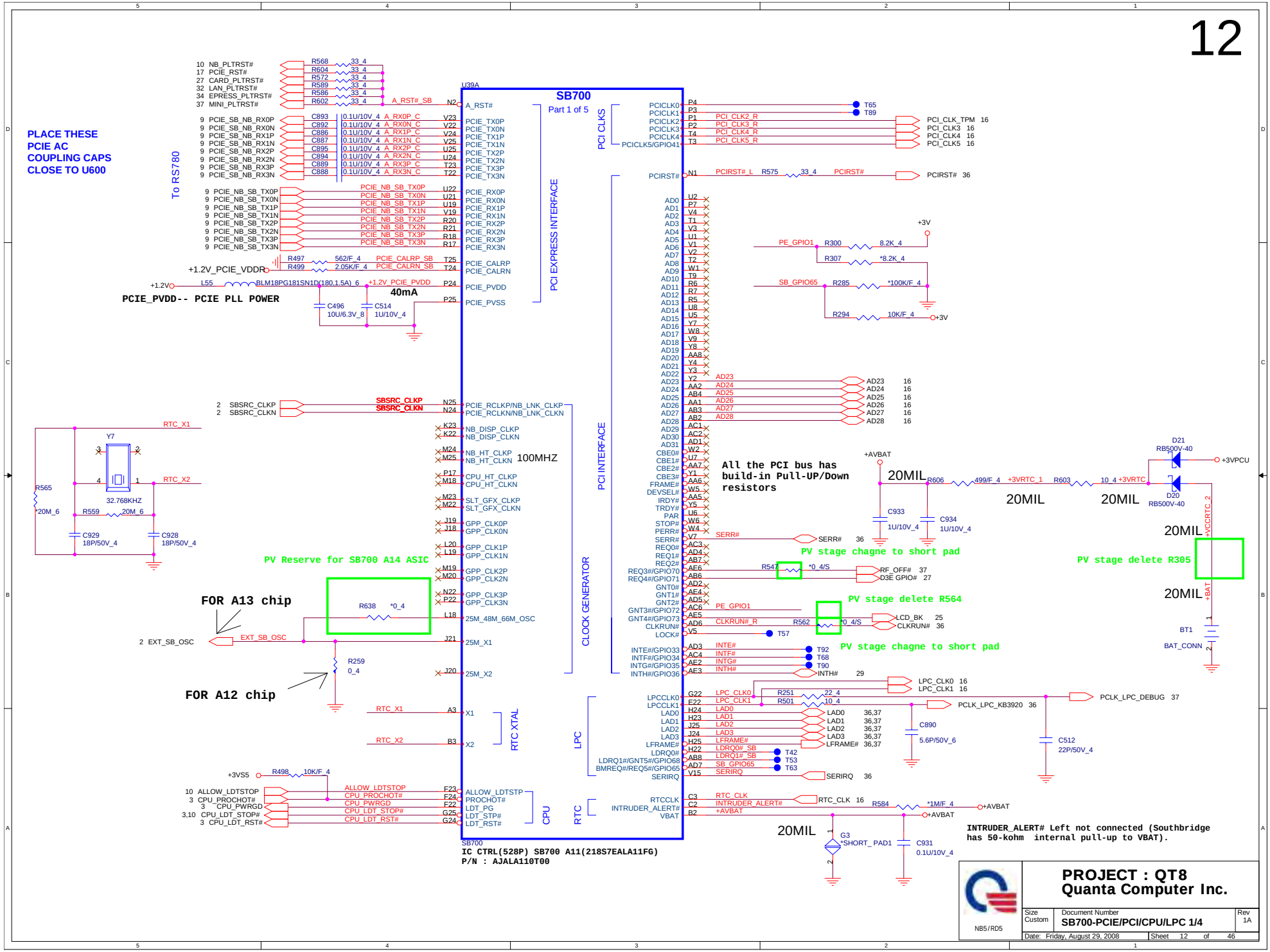
PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS740/RS780-POWER5/5	1A

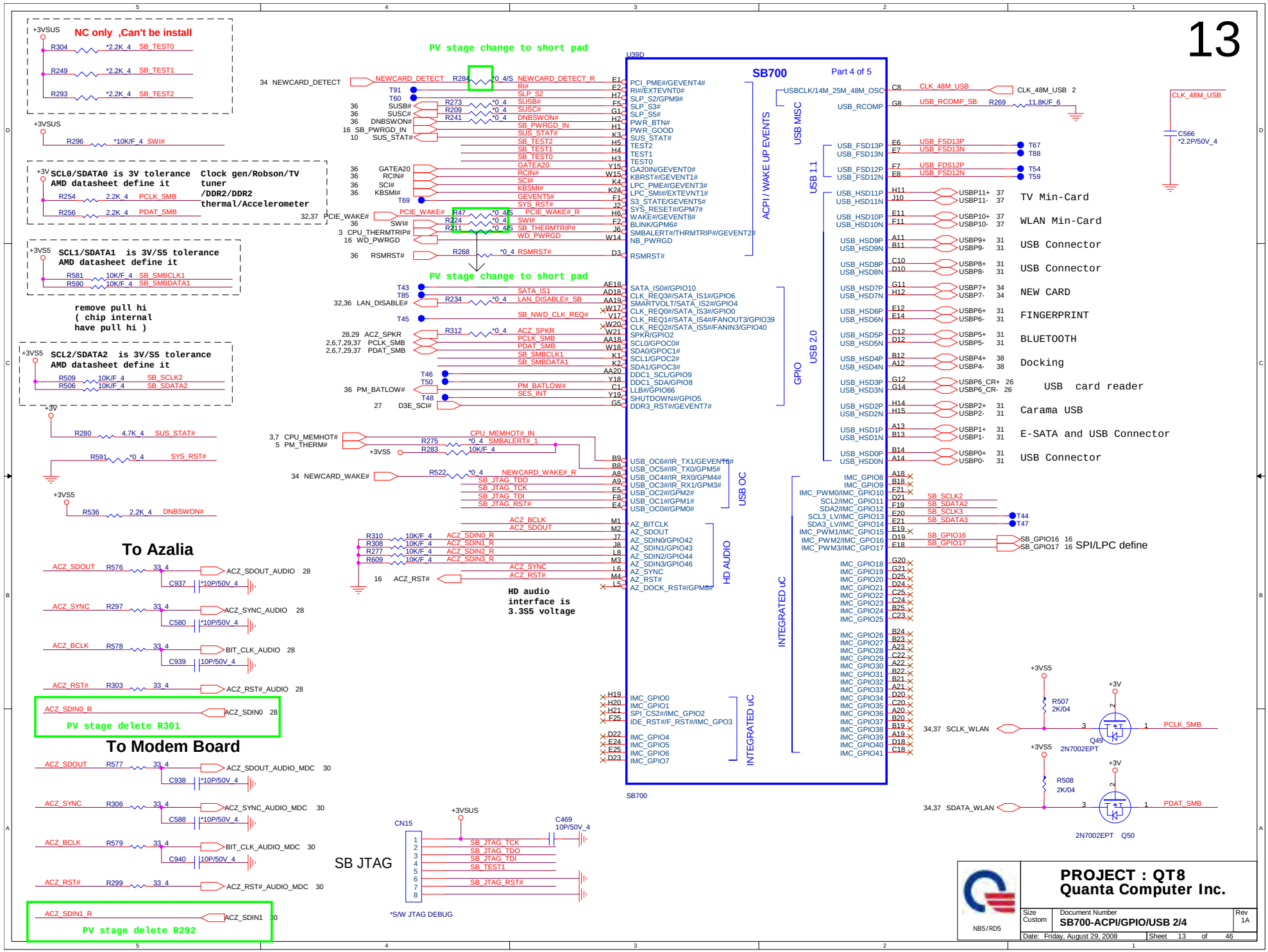
Date: Friday, August 29, 2008 Sheet 11 of 46

NB5/RD5

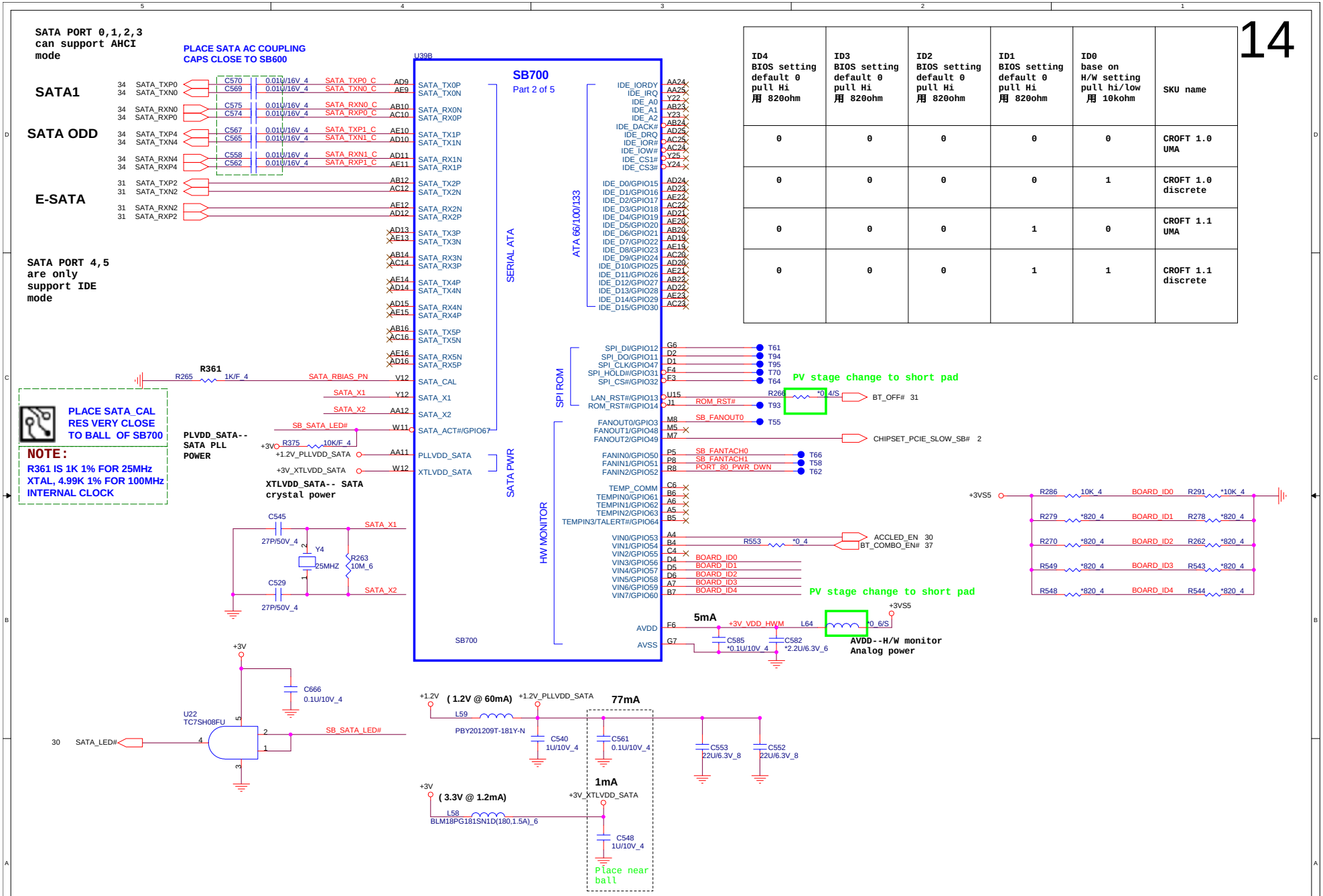
http://mycomp.su/x/



http://mycomp.su/x/



http://mycomp.su/x/



ID4 BIOS setting default 0 pull Hi 用 820ohm	ID3 BIOS setting default 0 pull Hi 用 820ohm	ID2 BIOS setting default 0 pull Hi 用 820ohm	ID1 BIOS setting default 0 pull Hi 用 820ohm	ID0 base on H/W setting pull hi/low 用 10kohm	SKU name
0	0	0	0	0	CROFT 1.0 UMA
0	0	0	0	1	CROFT 1.0 discrete
0	0	0	1	0	CROFT 1.1 UMA
0	0	0	1	1	CROFT 1.1 discrete

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB700-ACPI/GPIO/USB 2/4	1A

Date: Friday, August 29, 2008 Sheet 14 of 46

NB5/RD5

http://mycomp.su/x/

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

PV change to use short pad

VDDQ--3.3V I/O power 0.8A

VDD-- S/B CORE power

604mA

1.8V : FLASH MEMORY MODE(DEFAULT)
3.3V: IDE MODE

PV change to delete R237

VDD33_18--3.3V IDE I/O power
1.8V flash memory I/O power 0.45A

CKVDD_1.2V-- Internal clock Generator I/O power

286mA

PCIE_VDDR--PCIE I/O power 844mA

S5_3.3--3.3v standby power

0.01A

PV change to use short pad

AVDD_SATA--SATA phy power 0.2A

0.22A

S5_1.2V--1.2V standby power

0.2A

For support USB wakeup-->3V_S5

AVDDTX--USB Phy Analog I/O power 0.2A

V5_VREF--PCI 5V TOLERANCE

4mA

7mA

44mA

16mA

PV change to use short pad

USB_PHY_1.2V--USB Phy digital power

AVDDC--USB Analog PLL power

AVDDCK_1.2--USB Phy digital power

AVDDCK_3.3--Analog system PLL power

PROJECT : QT8
Quanta Computer Inc.

Size Custom | Document Number SB700-PWR/DECOUPLING 4/4 | Rev 1A

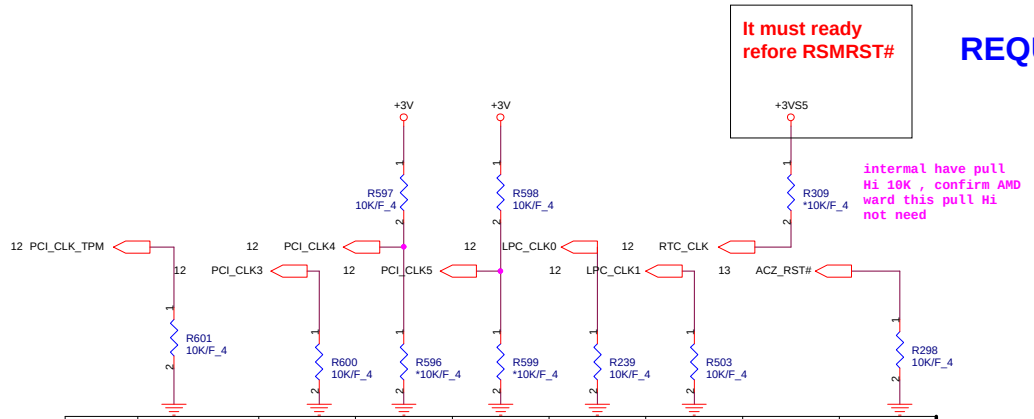
Date: Friday, August 29, 2008 | Sheet 15 of 46

NB5/RD5

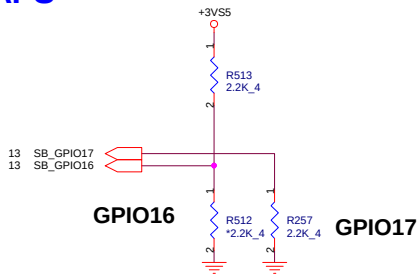
http://mycomp.su/x/

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

REQUIRED STRAPS



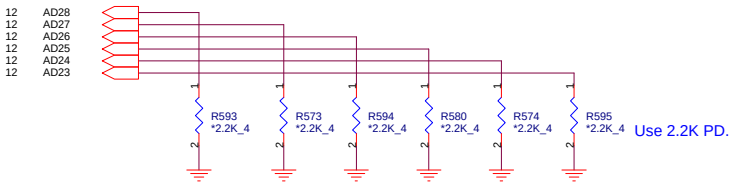
	PCI_CLK_TPM	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	IMC ENABLED	CLKGEN ENABLED	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT



TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

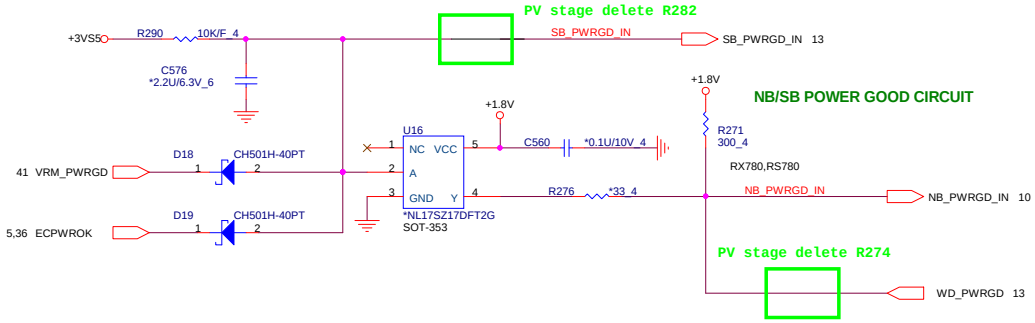
DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)



AL17SZ17000	IC(5P) NL17SZ17DFT2G(SOT-353)	SOT-353
ALUC1G17000	IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5)	SOT23-5

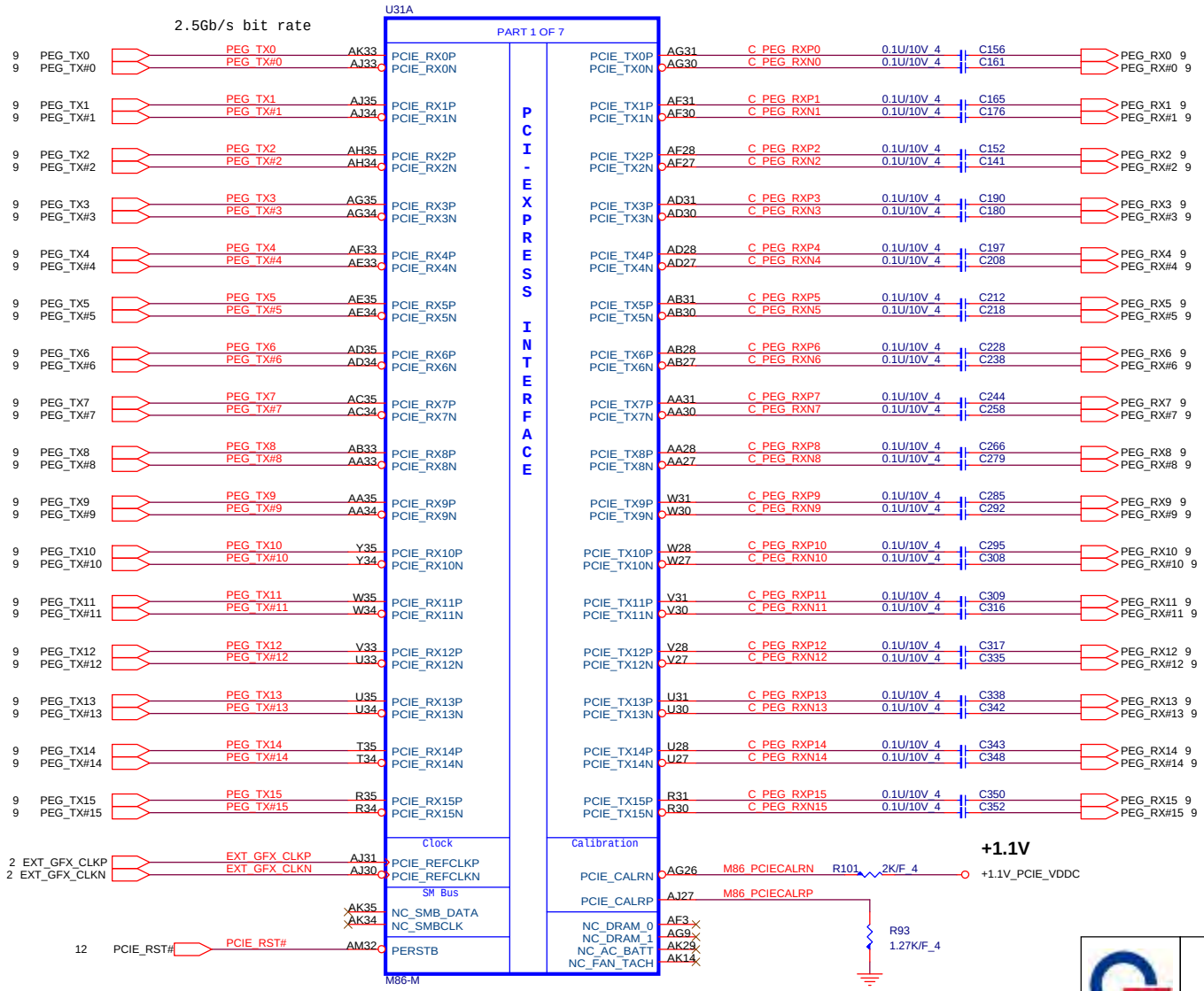
NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB700-STRAPS	1A

Date: Friday, August 29, 2008 Sheet 16 of 46

http://mycomp.su/x/



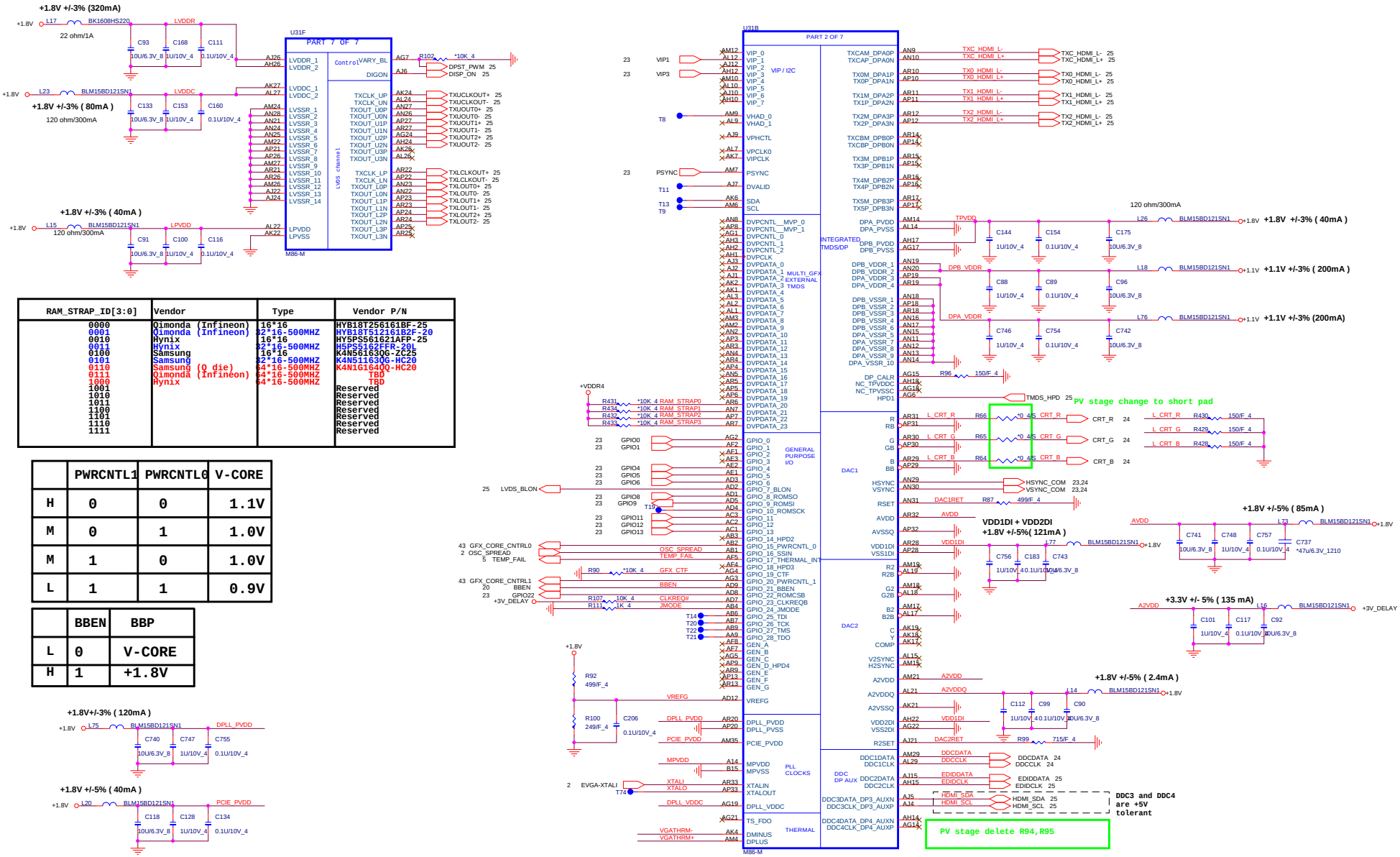
NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
B	M86 PCIE	1A

Date: Friday, August 29, 2008 | Sheet 17 of 46

http://mycomp.su/x/

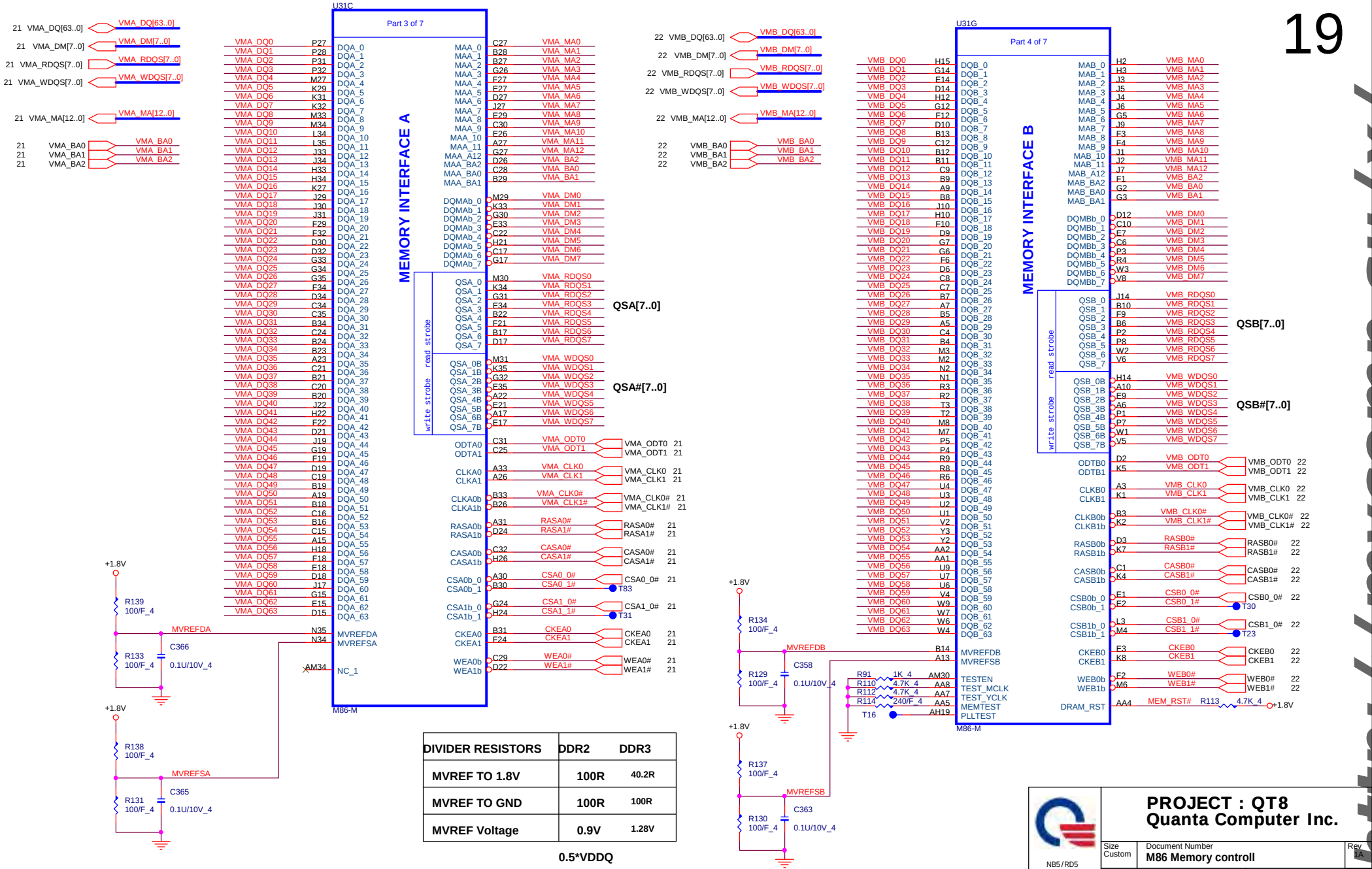


RAM_STRAP_ID[3:0]	Vendor	Type	Vendor P/N
0000	Qimonda (Infineon)	16*16	HYB18T256161BF-25
0001	Qimonda (Infineon)	32*16-500MHZ	HYB18T512161BZF-20
0010	Hynix	16*16	HY5PS561621AFP-25
0011	Hynix	32*16-500MHZ	H5PS5162FFR-20L
0100	Samsung	16*16	K4N56163QG-ZC25
0101	Samsung	32*16-500MHZ	K4N51163QG-HC20
0110	Samsung (Q die)	64*16-500MHZ	K4N1G164QQ-HC20
0111	Qimonda (Infineon)	64*16-500MHZ	TBD
1000	Hynix	64*16-500MHZ	TBD
1001			Reserved
1010			Reserved
1011			Reserved
1100			Reserved
1101			Reserved
1110			Reserved
1111			Reserved

	PWRCNTL1	PWRCNTL0	V-CORE
H	0	0	1.1V
M	0	1	1.0V
M	1	0	1.0V
L	1	1	0.9V

	BBEN	BBP
L	0	V-CORE
H	1	+1.8V

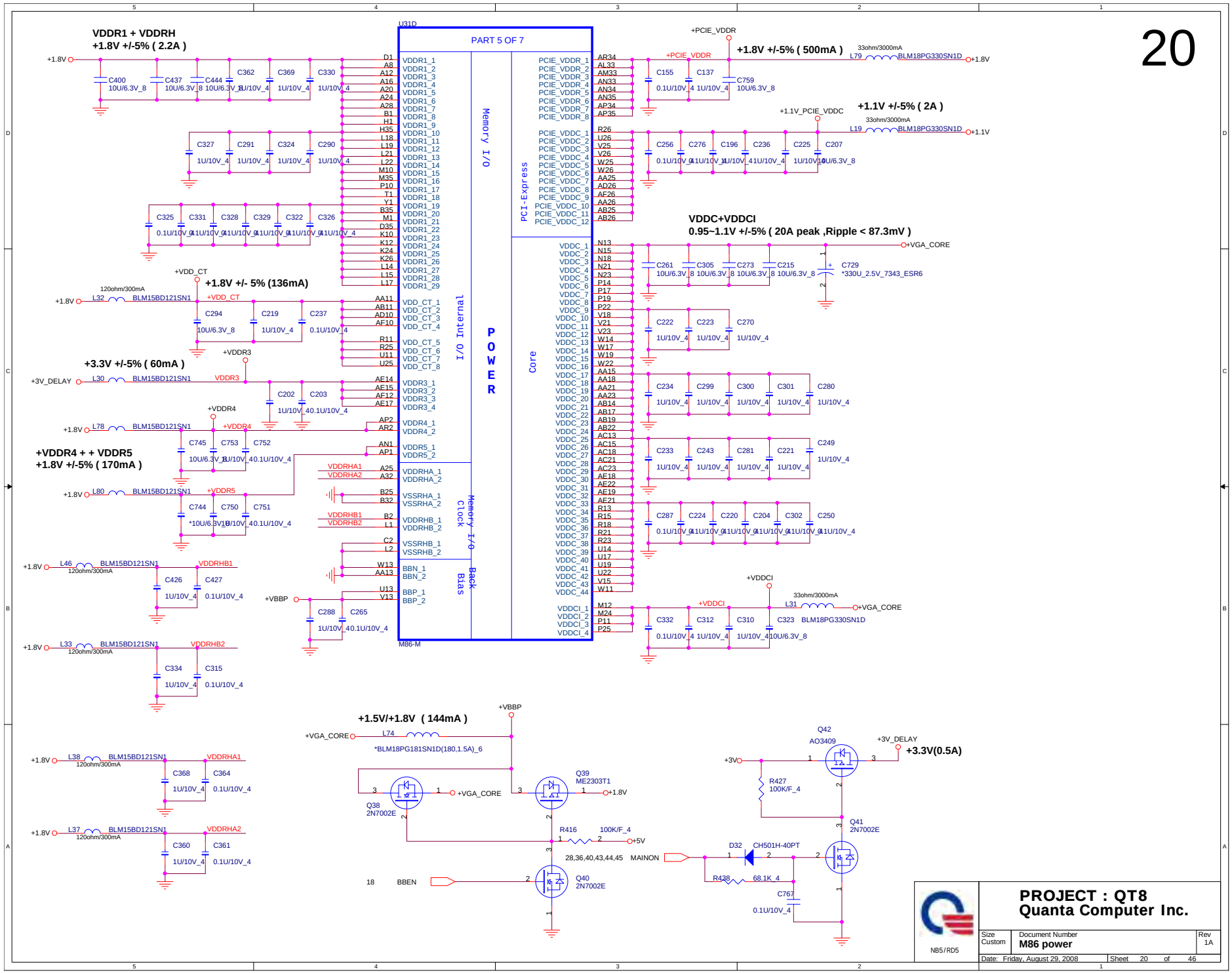
http://mycomp.su/x/



DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R
MVREF Voltage	0.9V	1.28V

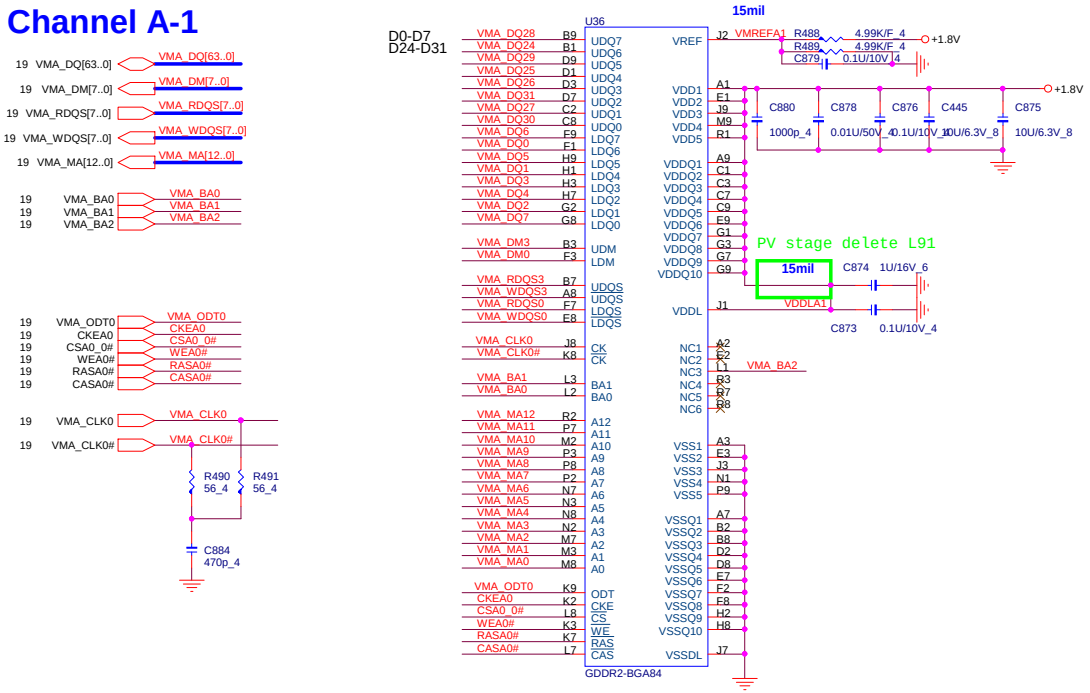
0.5*VDDQ

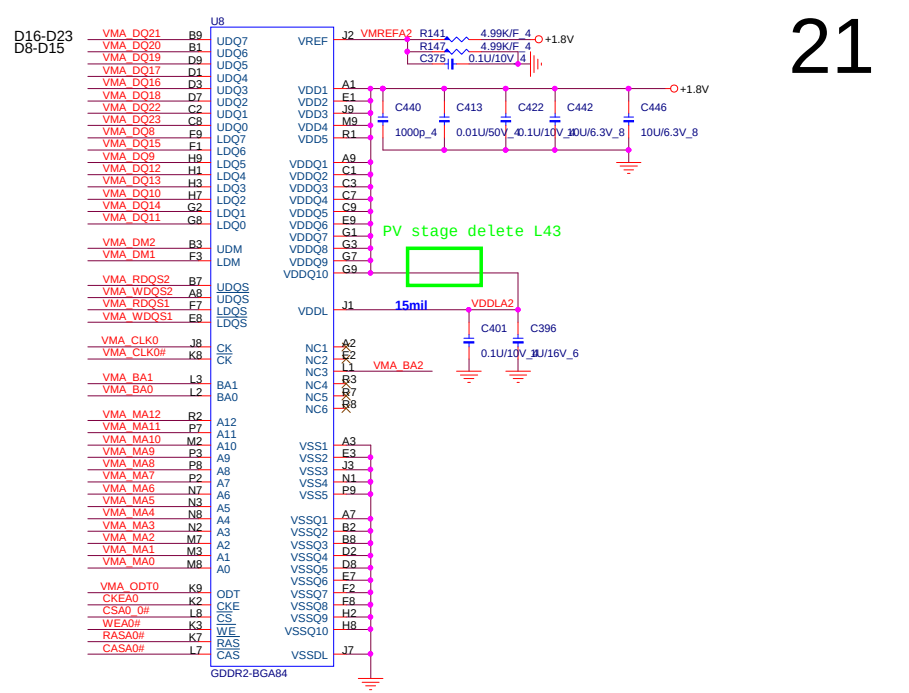
http://mycomp.su/x/



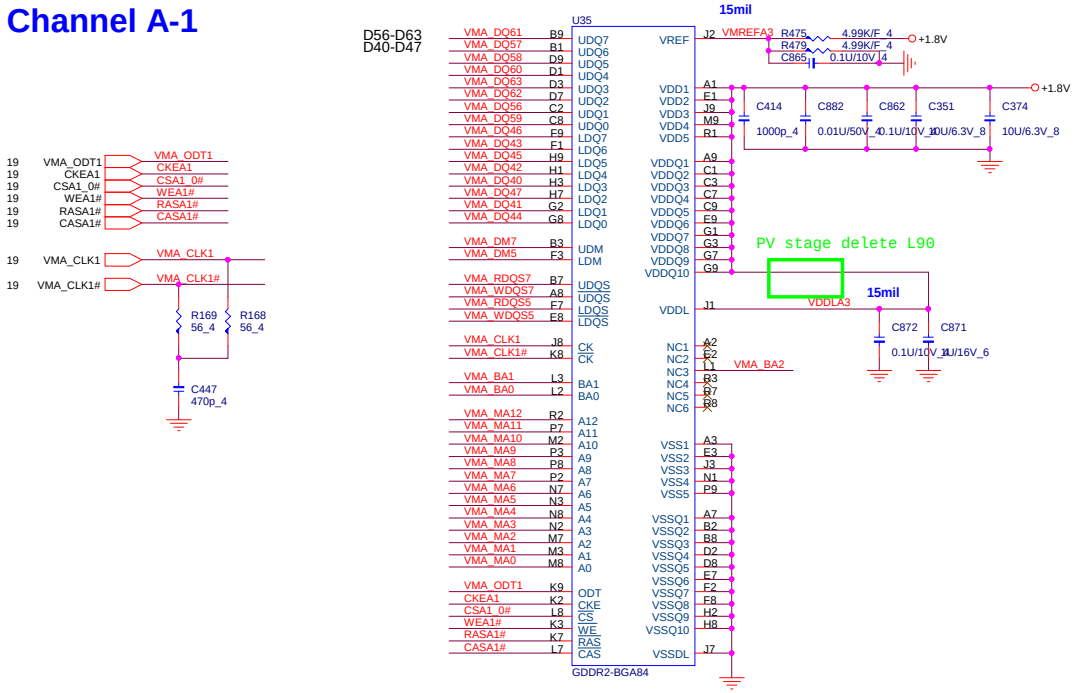
http://mycomp.su/x/

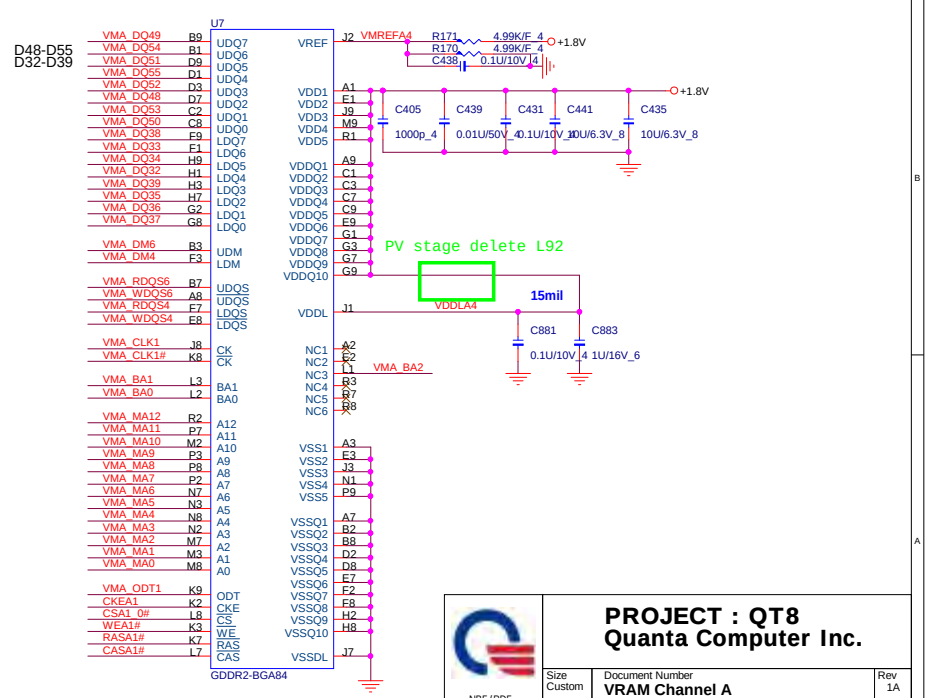
Channel A-1





Channel A-1





NB5/RD5

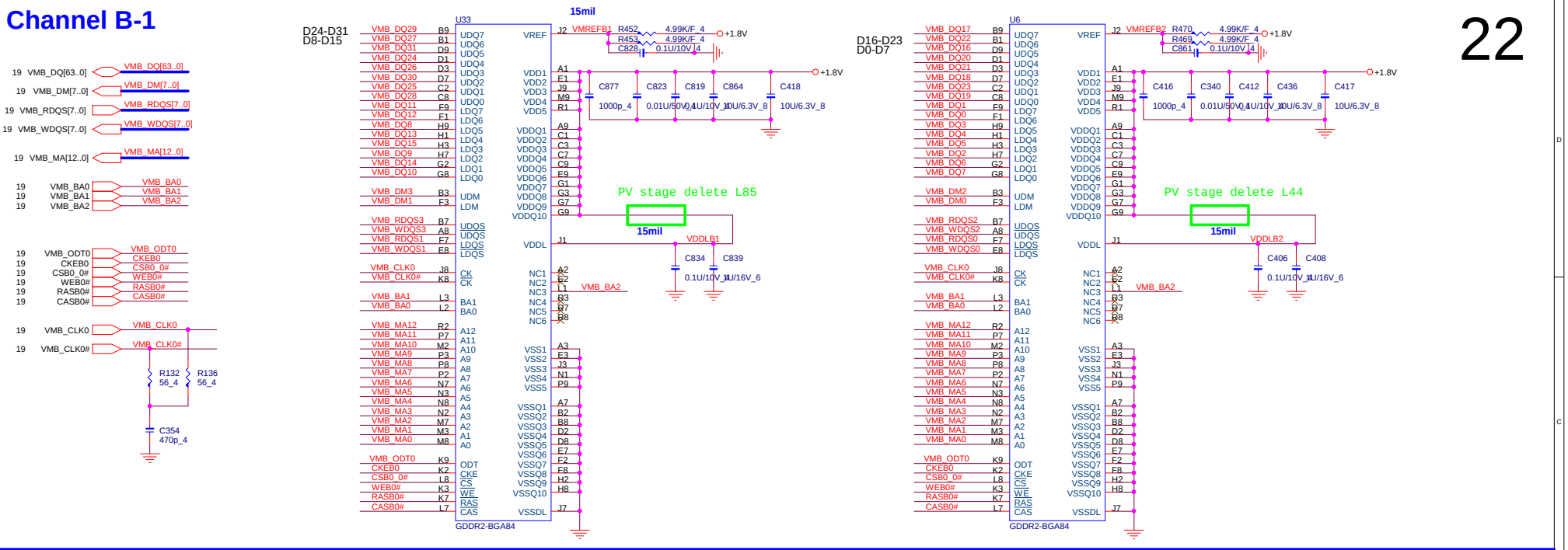
PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	VRAM Channel A	1A

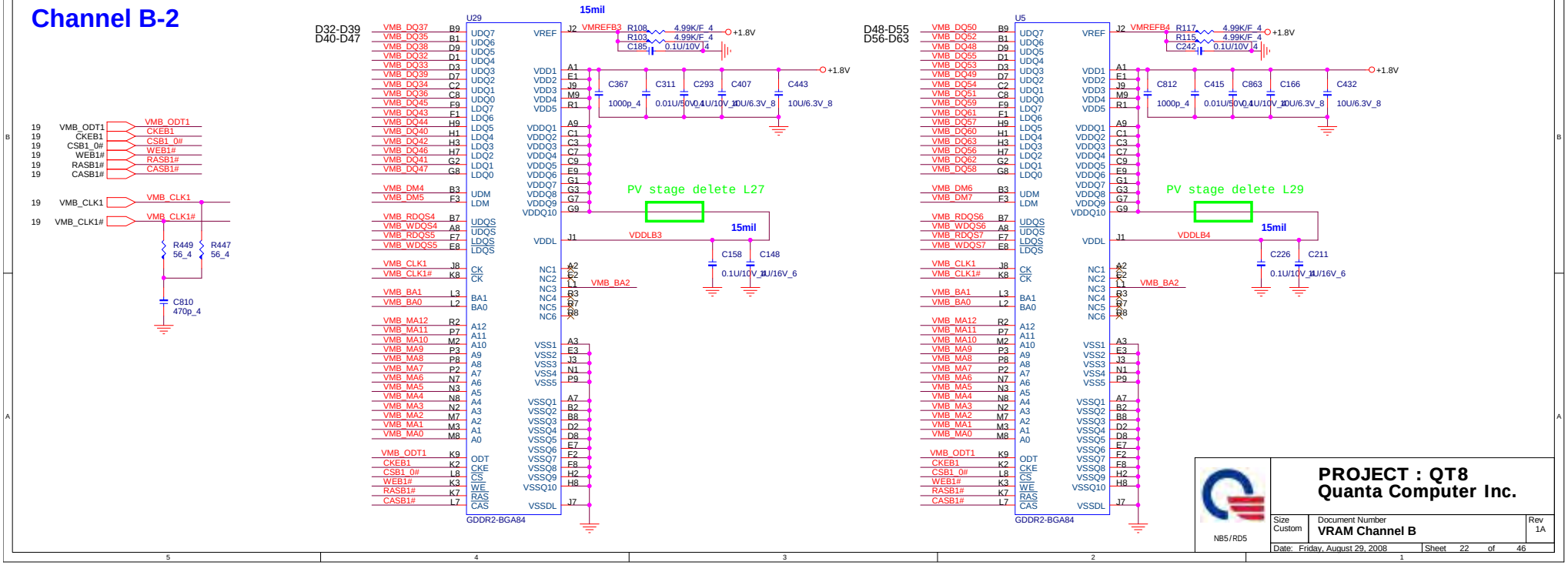
Date: Friday, August 29, 2008 | Sheet 21 of 46

http://mycomp.su/x/

Channel B-1



Channel B-2



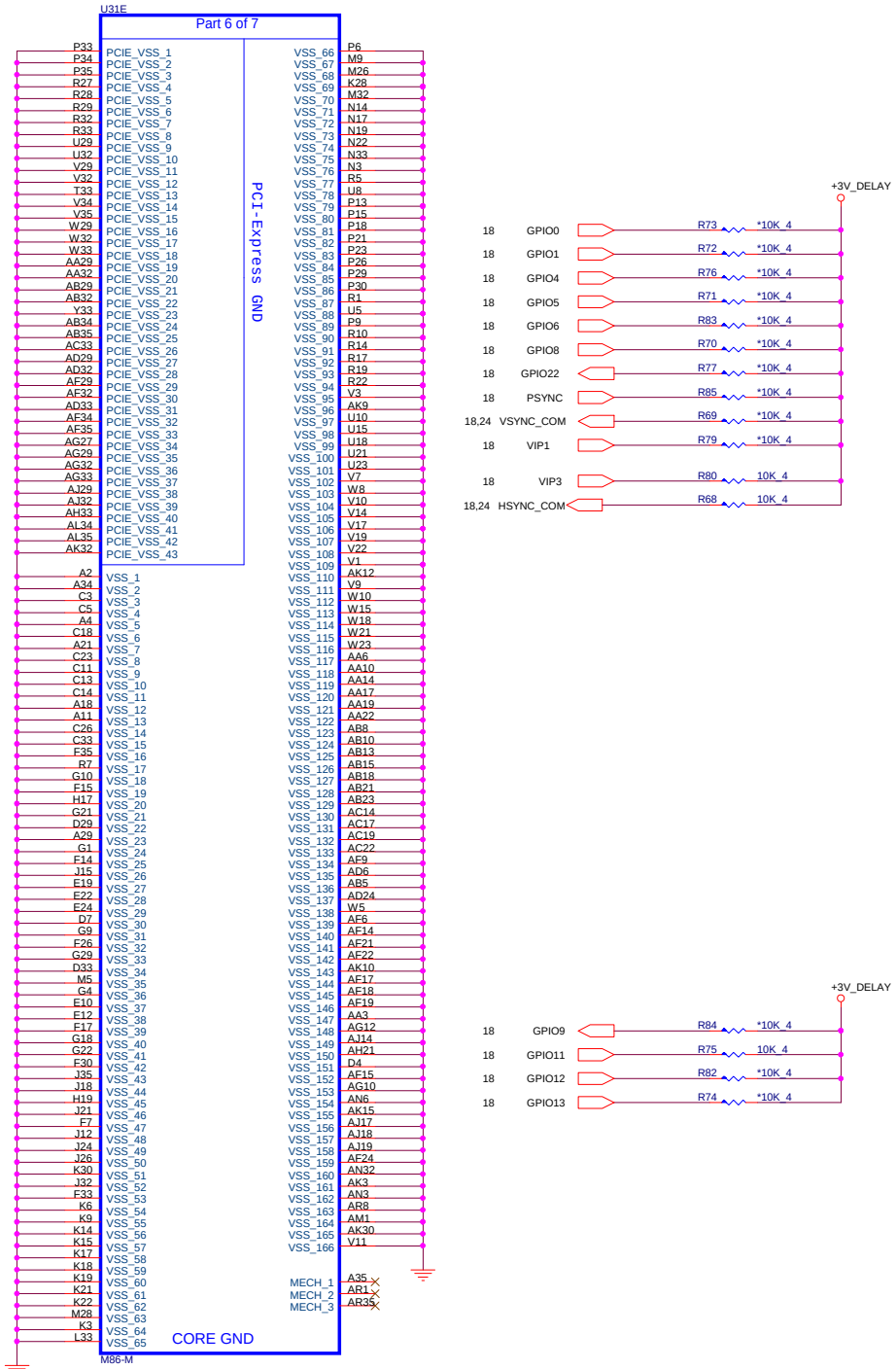
NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	**VRAM Channel B**	1A

Date: Friday, August 29, 2008 | Sheet 22 of 46

http://mycomp.su/x/



STRAP PIN

CONFIGURATION STRAPS		
PIN	**DESCRIPTION OF DEFAULT SETTINGS**	**M86-ME**
GPIO0	**PCIE FULL TX OUTPUT SWING , 0 = 50% , 1 = FULL**	**0**
GPIO1	**PCIE TRANSMITTER DE-EMPHASIS ENABLED , 0 = DISABLE**	**0**
GPIO5	**Allows eitherPCIe 2.5GT/s or 5GT/s operation , 0 = 2.5G , 1 = 5G**	**0**
VIP3	**ENABLE HD AUDIO (M86-M) , 1 = ENABLE**	**1**
GPIO8	**ENABLE HD AUDIO (M82-S)**	**REV**
HSYNC	**ENABLED HDMI**	**1**
GPIO22	**0 : DISABLED EXTERNAL BIOS ROM**	**0**
GPIO4	**FOR DEBUG ONLY**	**0**
GPIO6	**INTERNAL USE ONLY**	**0**
VSYNC	**IGNORE VIP DEVICE STRAPS**	**0**
PSYNC	**VGA ENABLE , 0 = VGA CONTROLLER CAPACITY ENABLE**	**0**

Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	NO SUPPORT		
0	1G	NO SUPPORT		
0	2G	NO SUPPORT		
0	4G	NO SUPPORT		

NB5/RD5

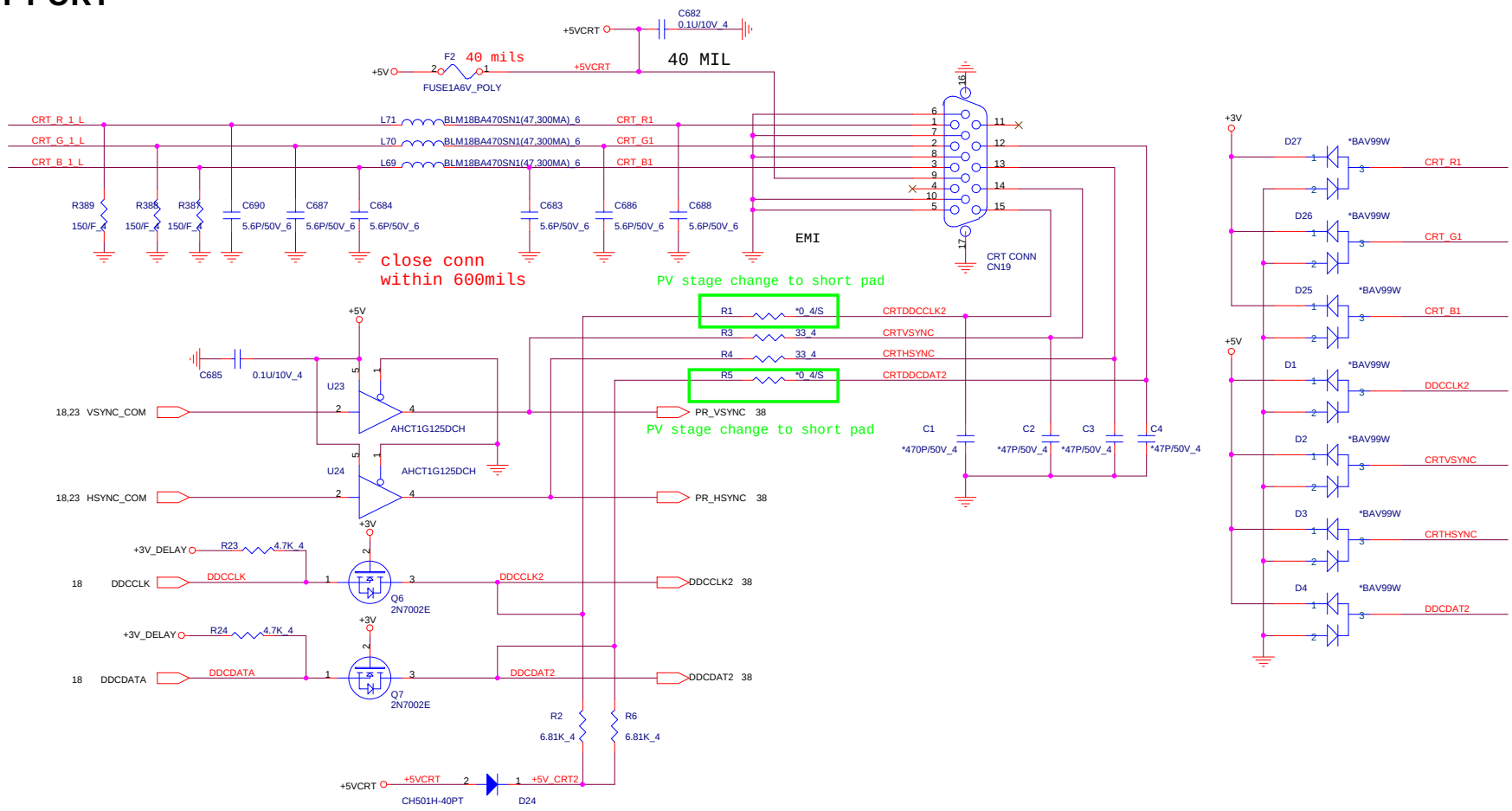
PROJECT : QT8
Quanta Computer Inc.

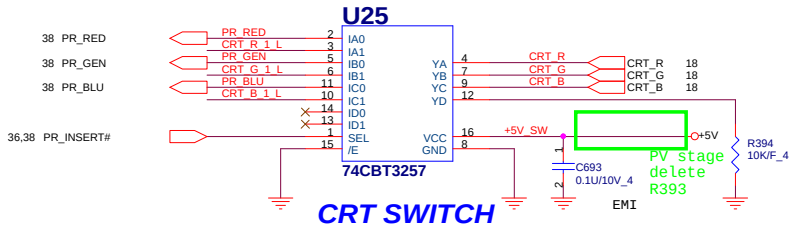
Size	Document Number	Rev
Custom	M86-STRAPS & GND	1A

Date: Friday, August 29, 2008 Sheet 23 of 46

http://mycomp.su/x/

CRT PORT





inputs		function
/E	SET	
L	L	Y - port 0
L	H	Y - port 1
H	X	Disconnect

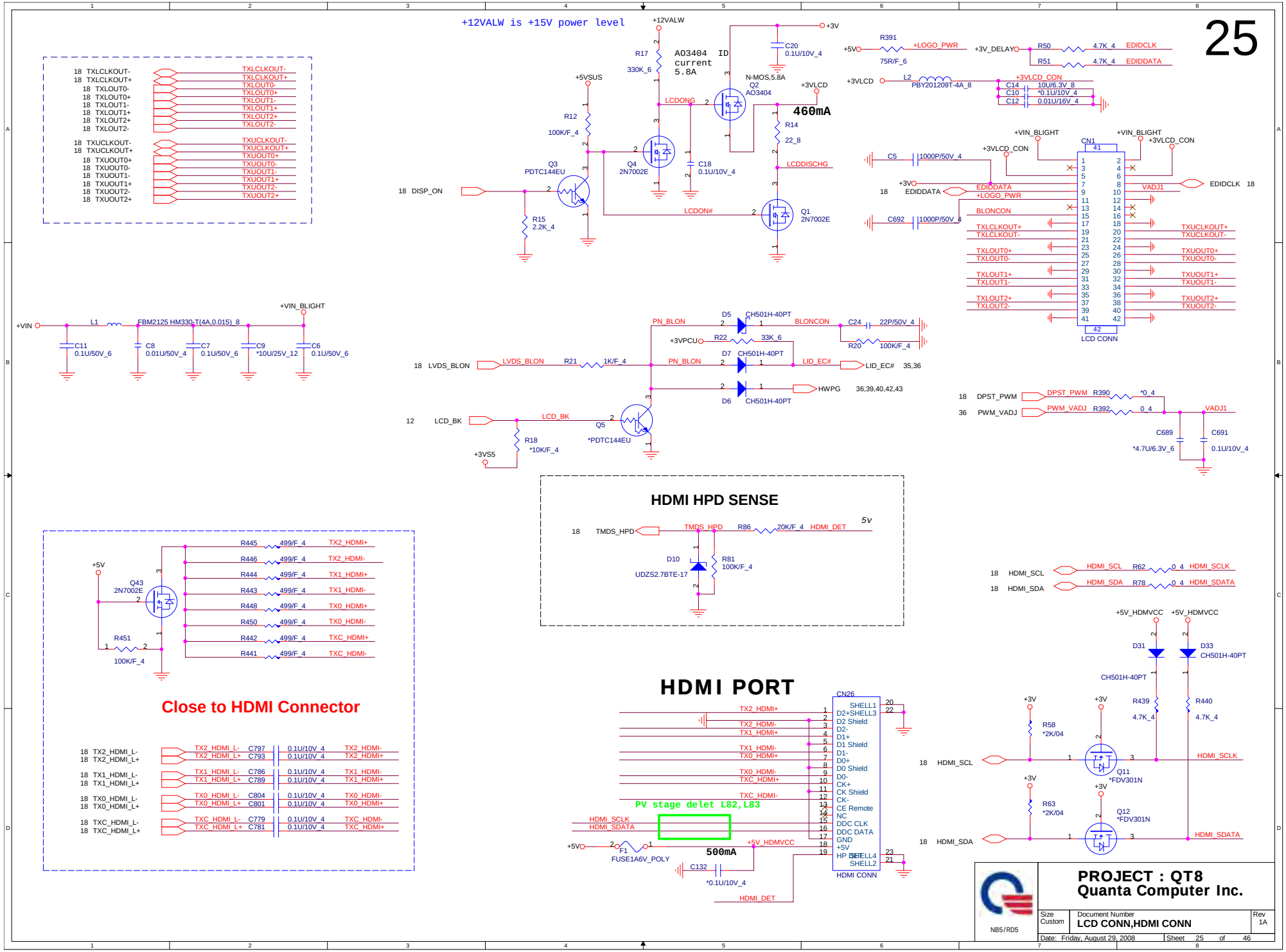
NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT	1A

Date: Friday, August 29, 2008 Sheet 24 of 46

http://mycomp.su/x/



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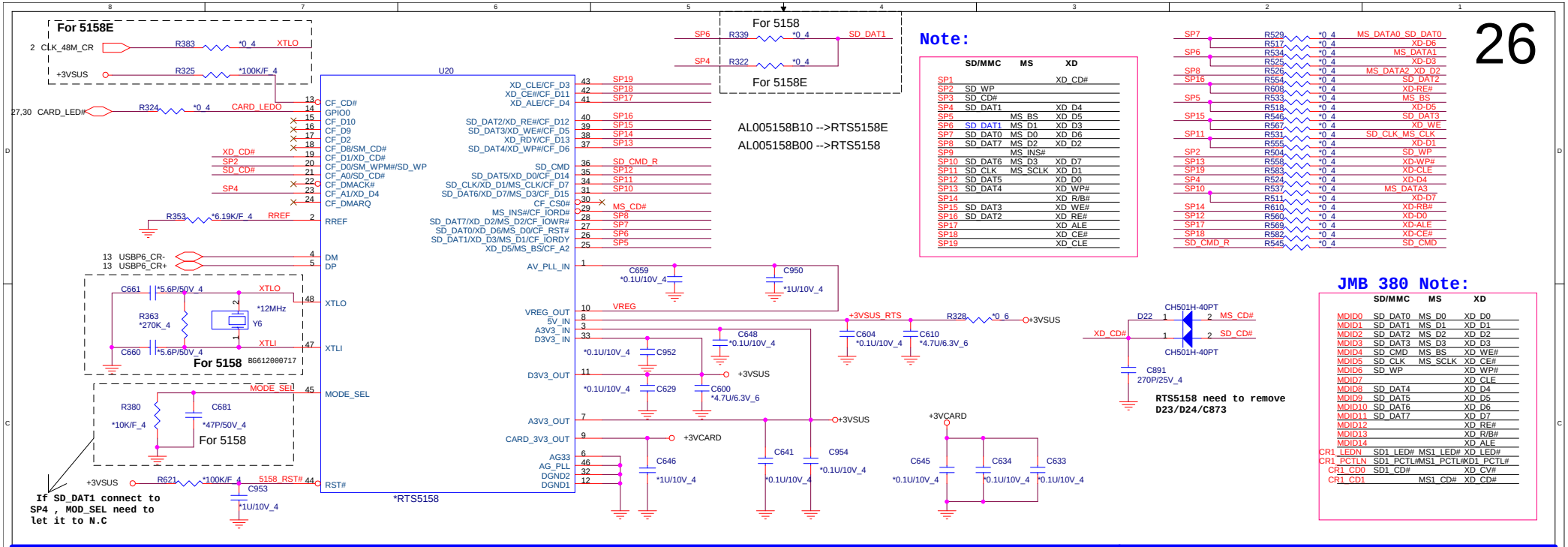

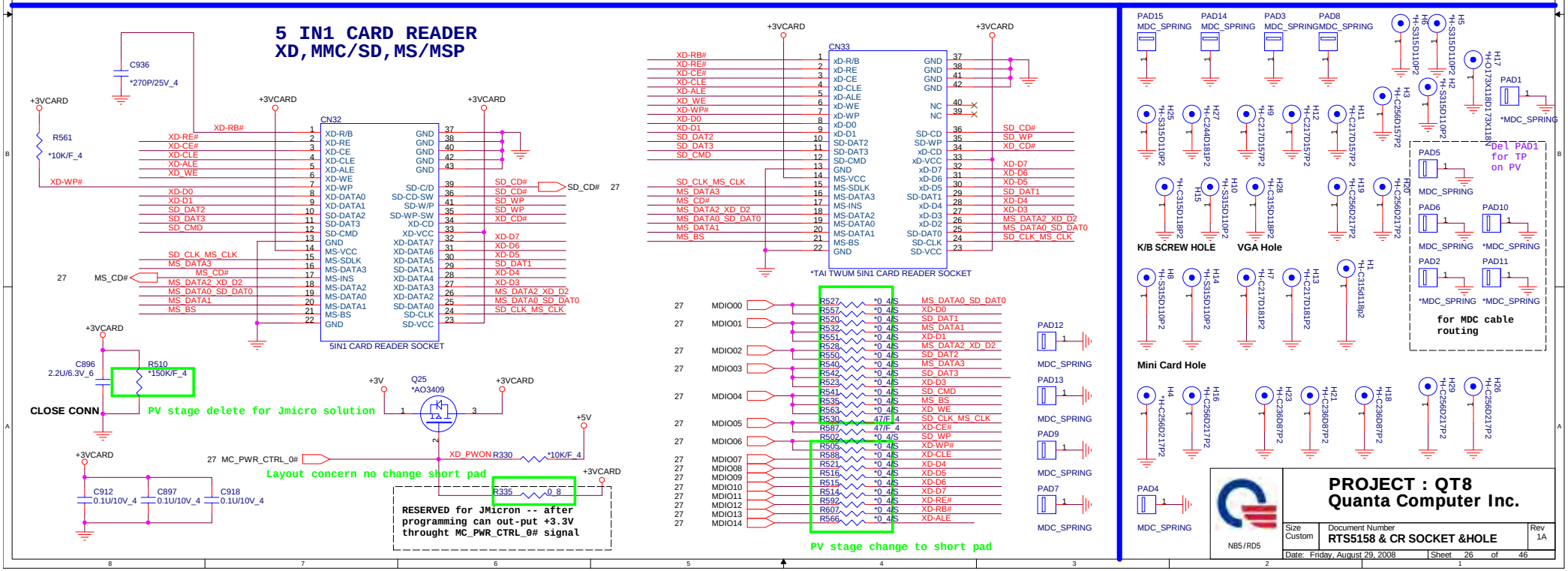

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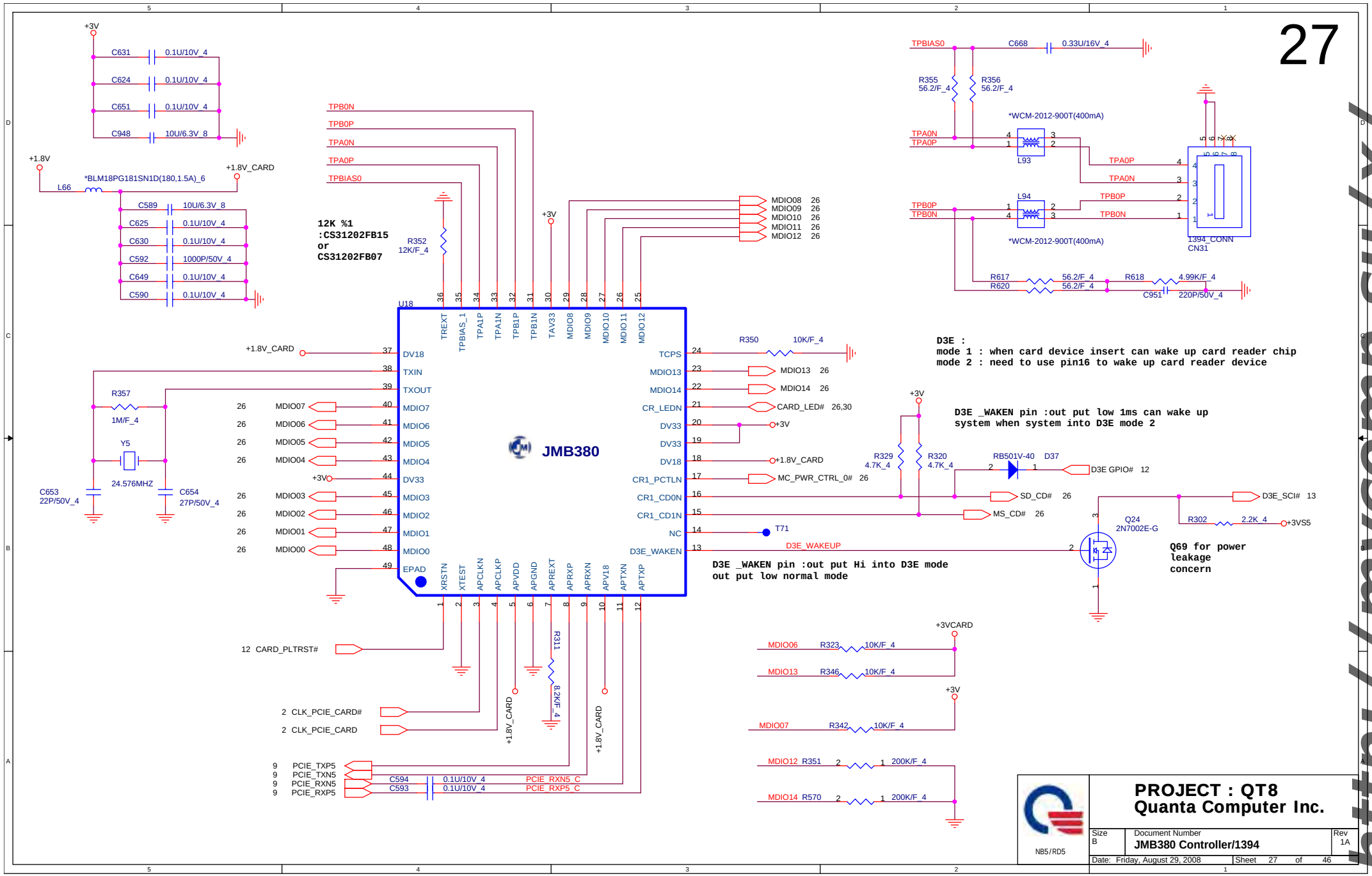

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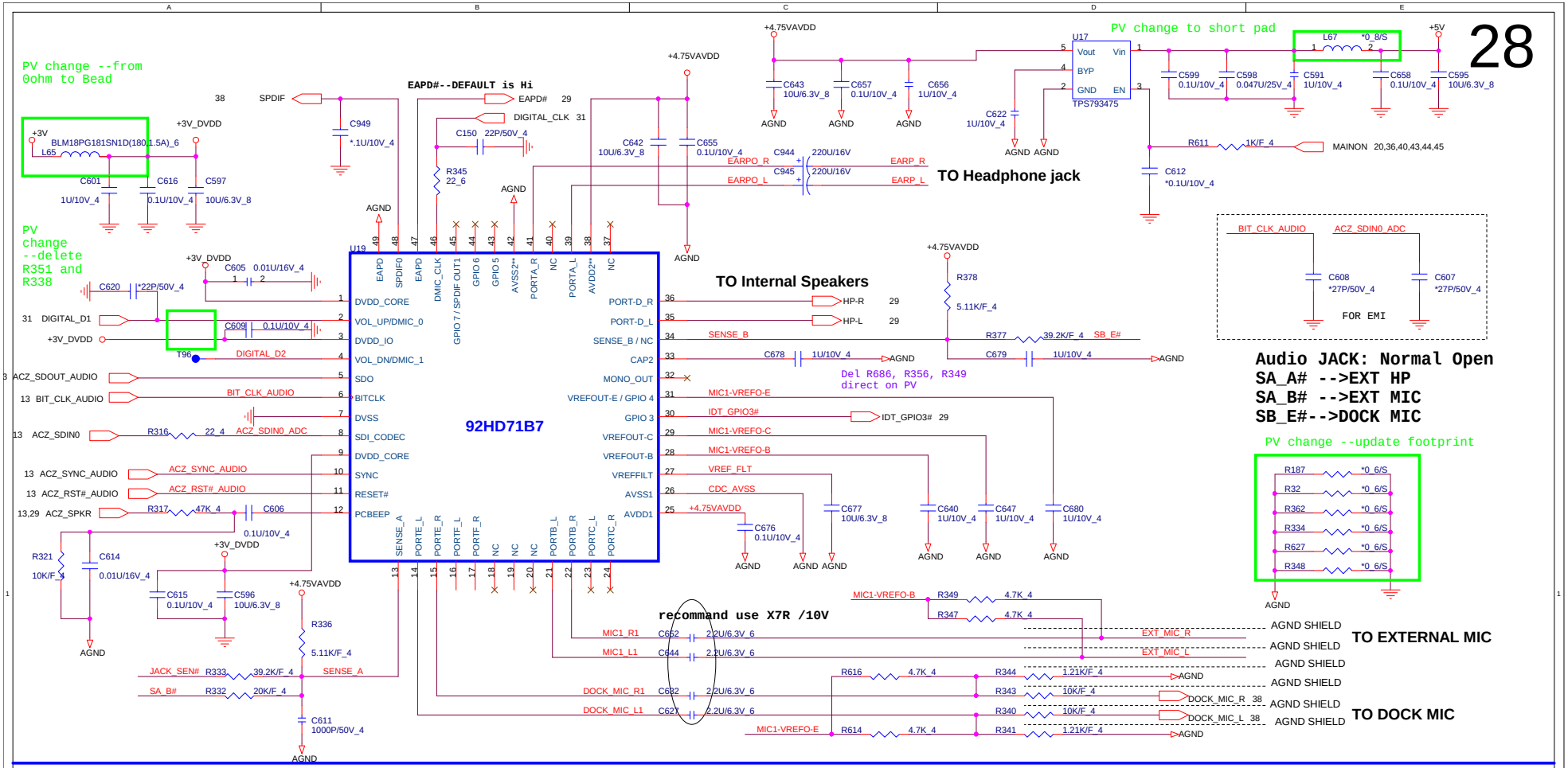

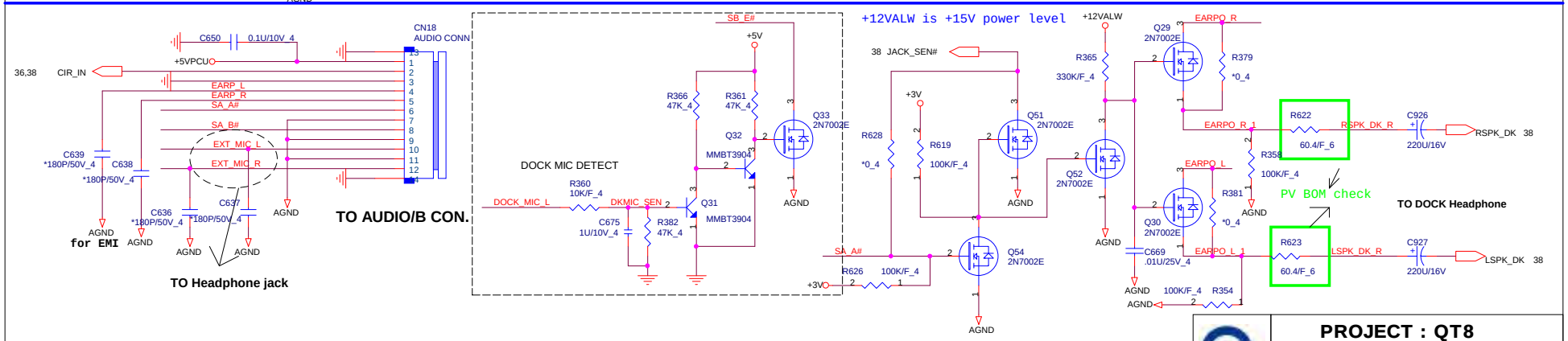

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Azalia AD1883	1A

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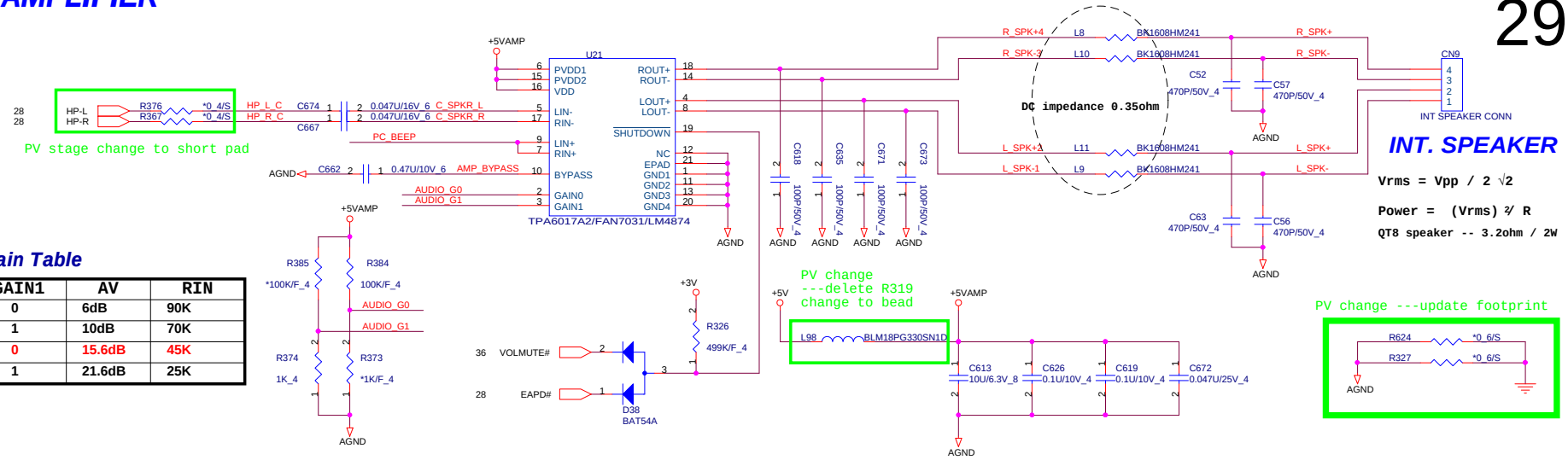
NB5/RD5

http://mycomp.su/x/

AUDIO AMPLIFIER



INT. SPEAKER

Vrms = Vpp / 2 √2

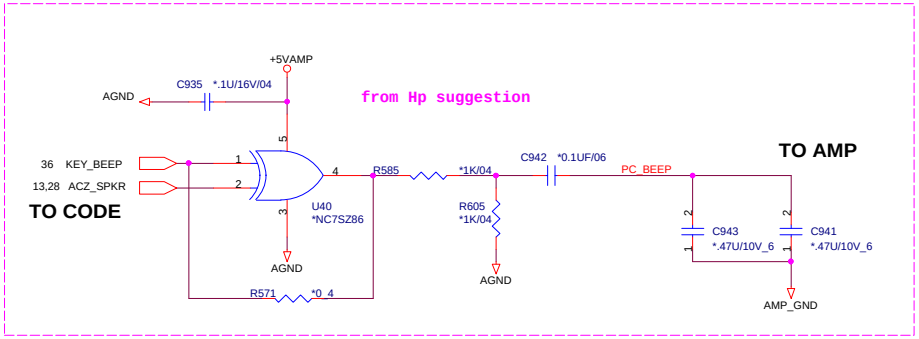
Power = (Vrms) ²/ R

QT8 speaker -- 3.2ohm / 2W

6017A2 Gain Table

GAIN0	GAIN1	AV	RIN
0	0	6dB	90K
0	1	10dB	70K
1	0	15.6dB	45K
1	1	21.6dB	25K

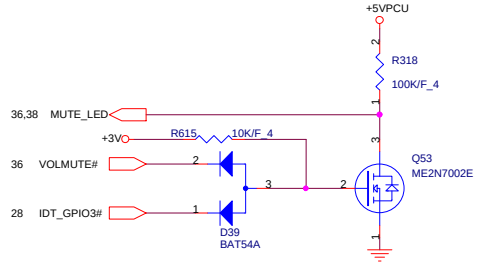
PC-BEEP



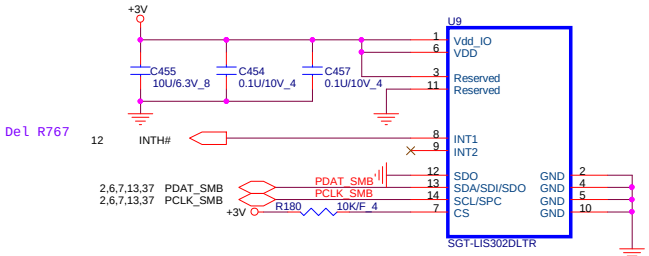
MUTE_LED

Low -->un-MUTE

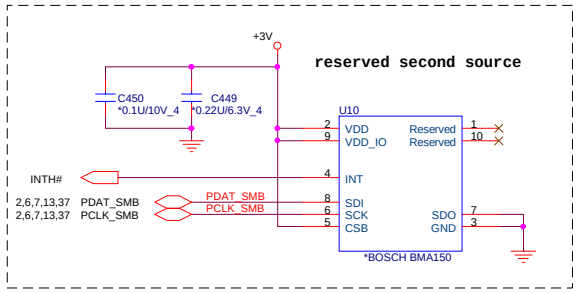
High-->Mute



Acceleration sensor



SGT-LIS302DLTR interrupt pin default is low / active Hi , BIOS need to programming 22h to change status from active Hi to low



PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	AMP_TPA6017/INT SPK	1A

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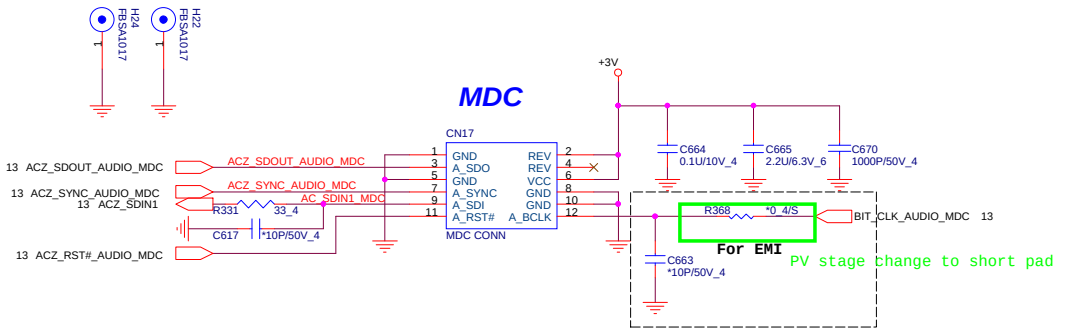
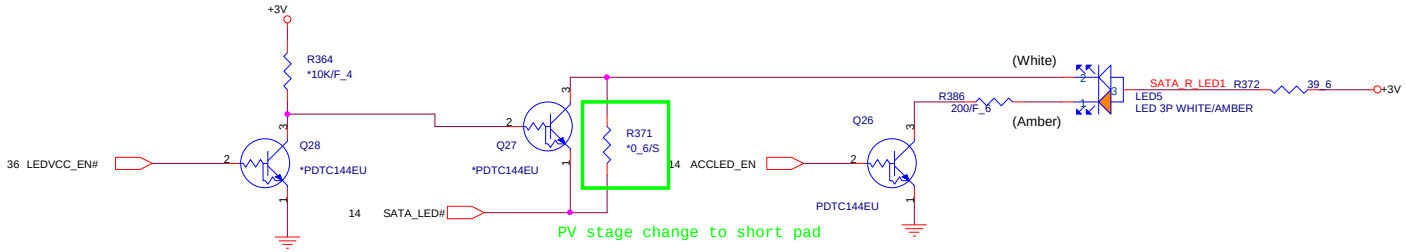
NB5/RD5

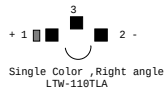
http://mycomp.su/x/

Modem CONN

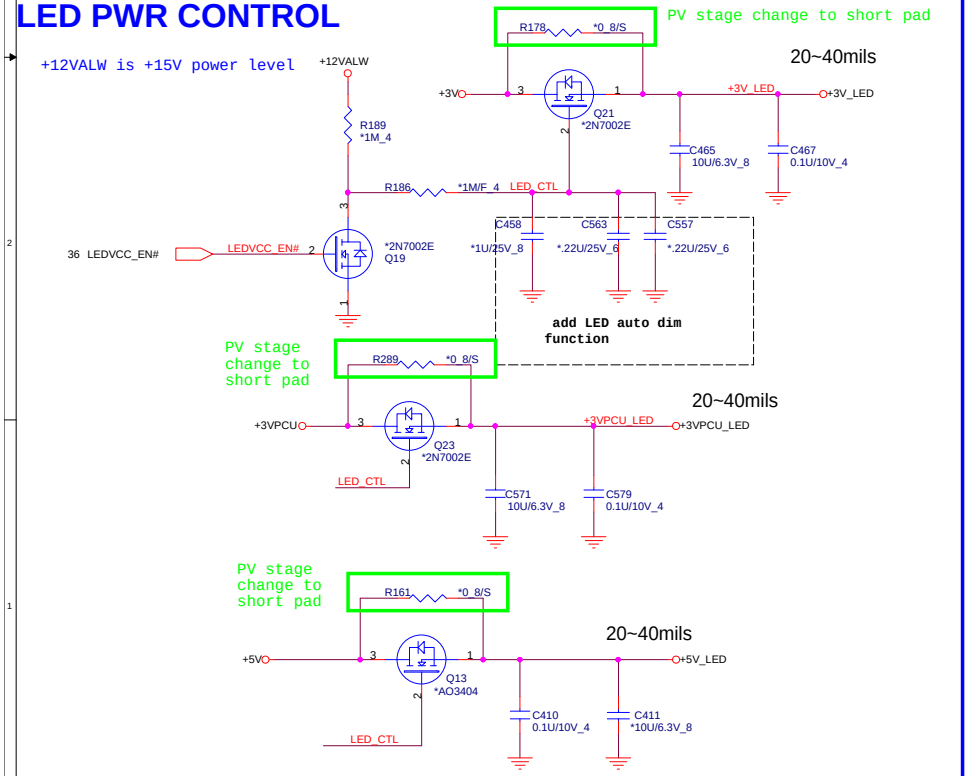


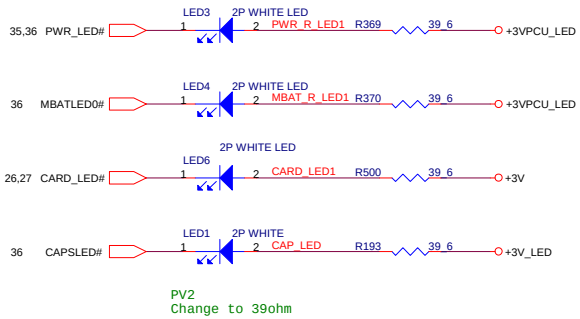
LED

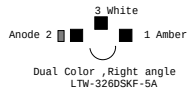


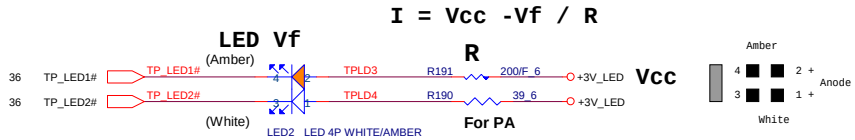


LED PWR CONTROL









NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MDC1.5 Con Accelerometer/ILED	1A

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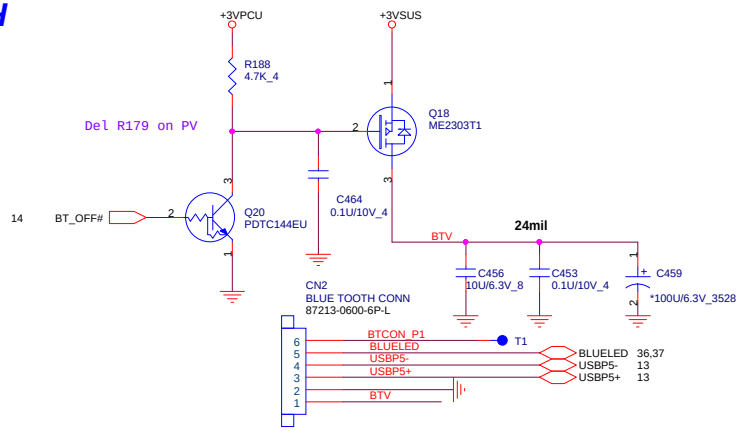
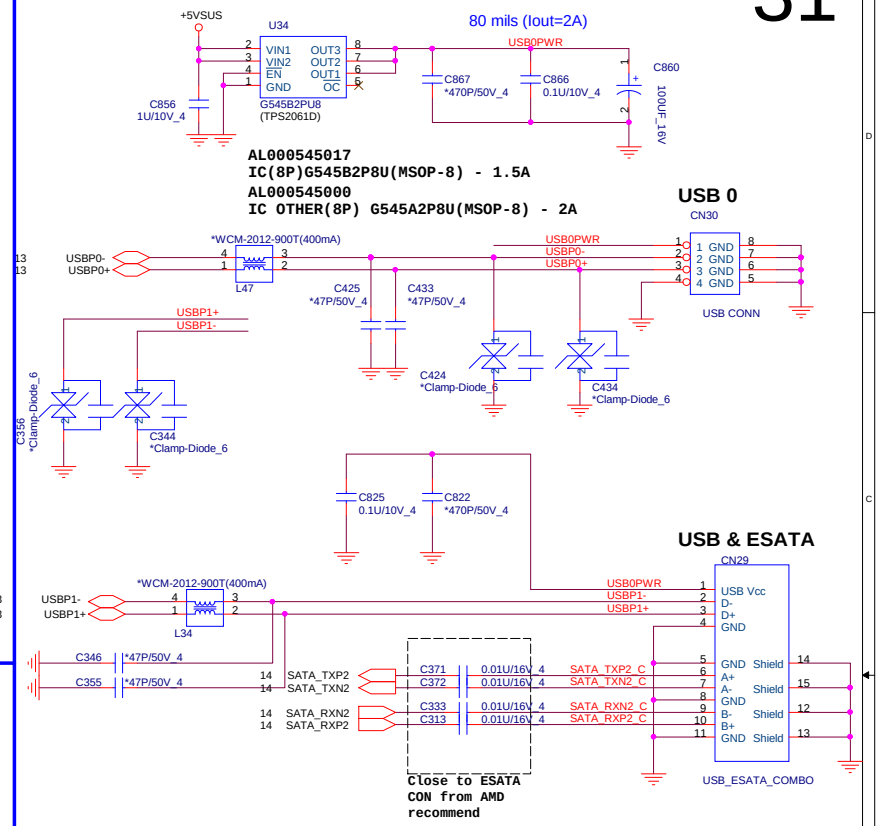
http://mycomp.su/x/

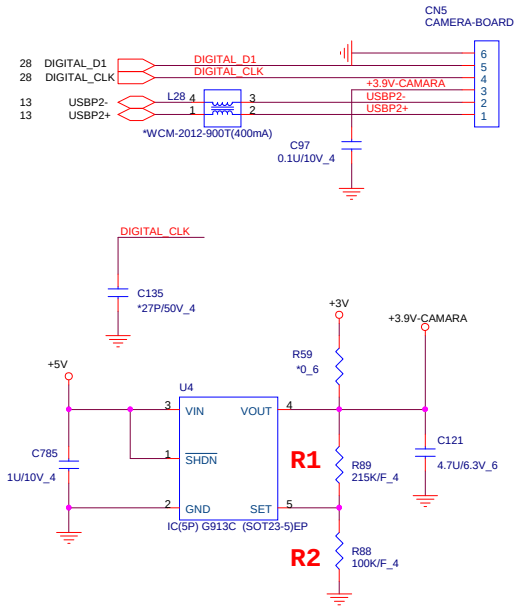
BLUETOOTH



LEFT SIDE USBX1 and E-SATA/USB COMBO

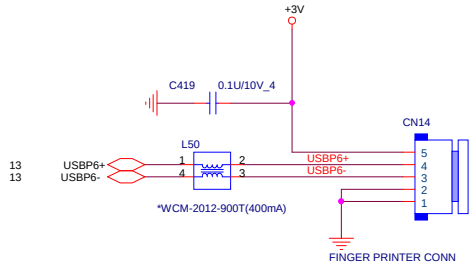


USB CAMERA CONNECT

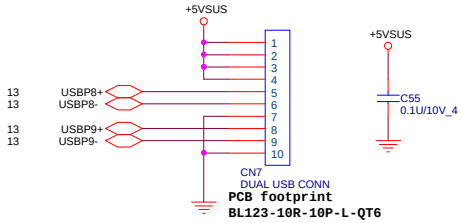


USB Fingerprint CON

1. ESD GND
2. SYSTEM GND
3. USB-
4. USB+
5. USB PWR(+3V)



RIGHT SIDE USBX2



NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BT/WEBCAM/FT/USBX4/ESATA	1A

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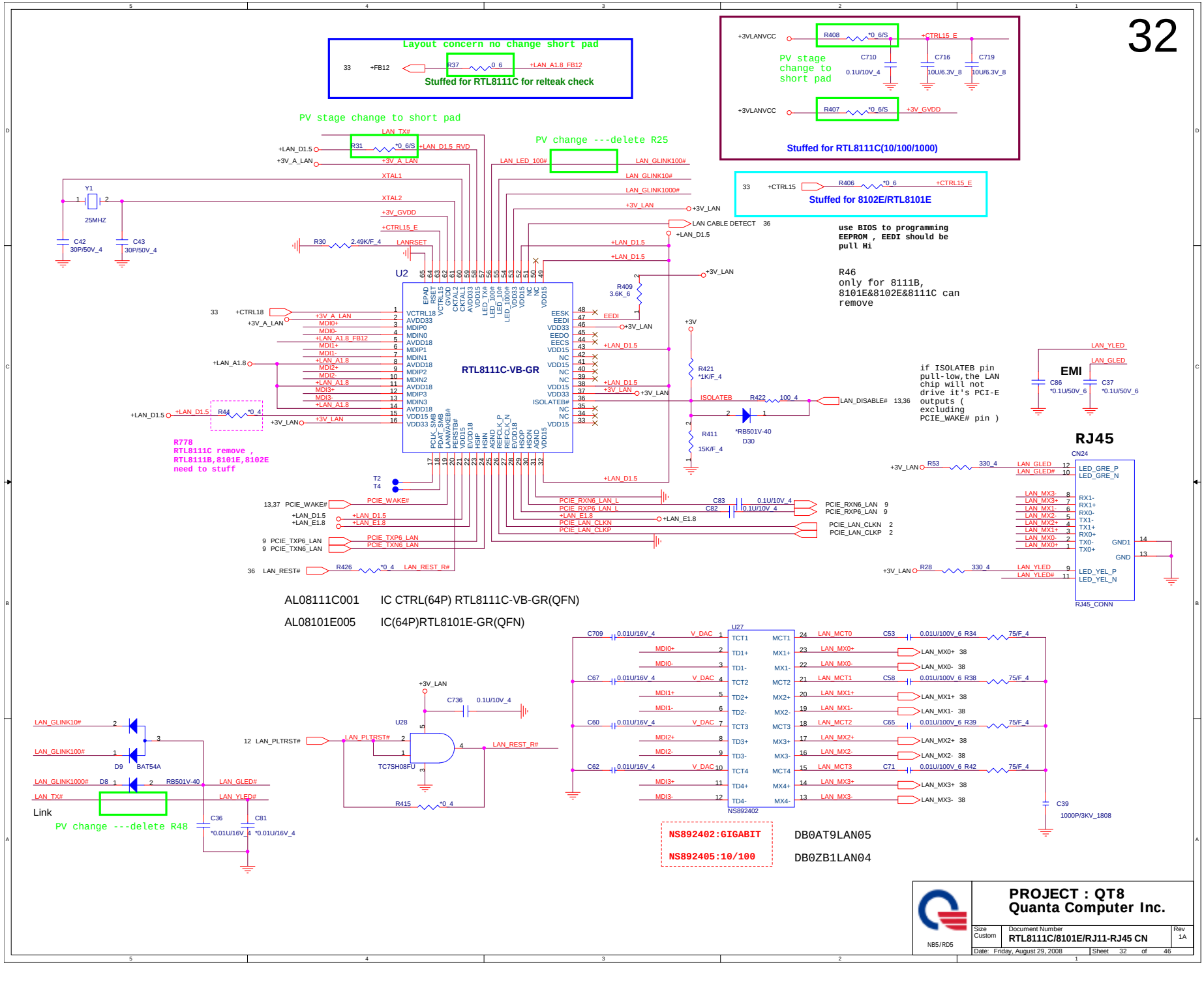
http://mycomp.su/x/



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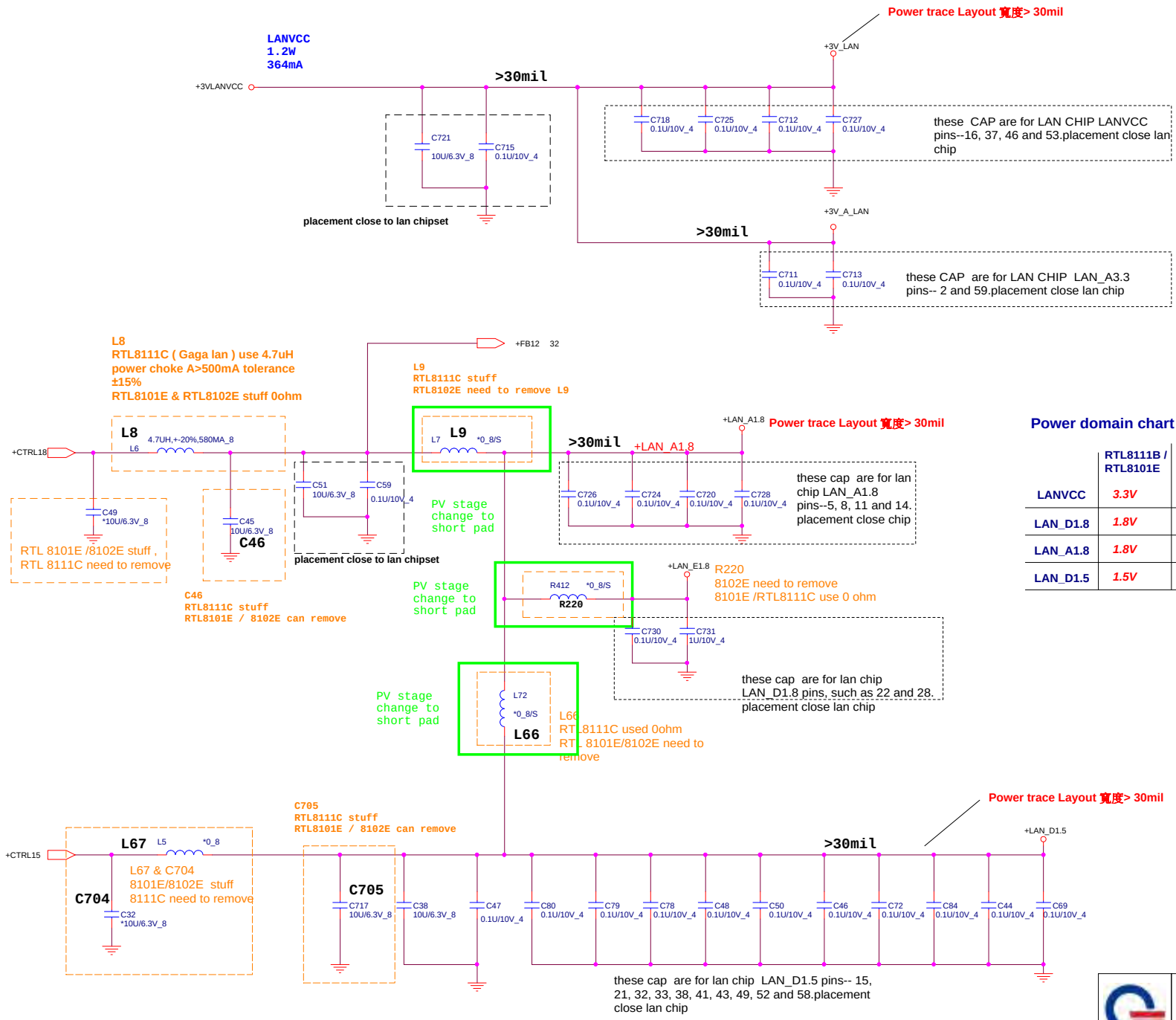

Power domain chart

	RTL8111B / RTL8101E	RTL8111C RTL8102E
LANVCC	3.3V	3.3V
LAN_D1.8	1.8V	1.2V
LAN_A1.8	1.8V	1.2V
LAN_D1.5	1.5V	1.2V

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LAN Power	1A

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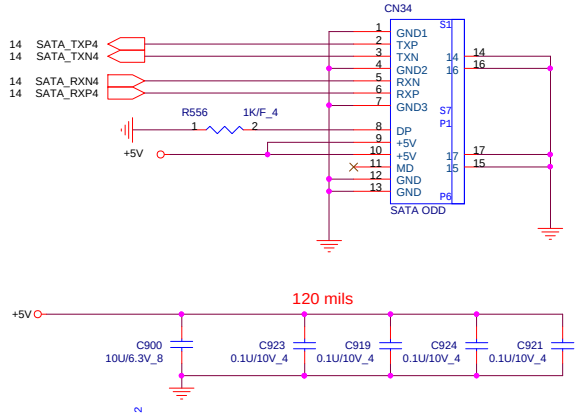
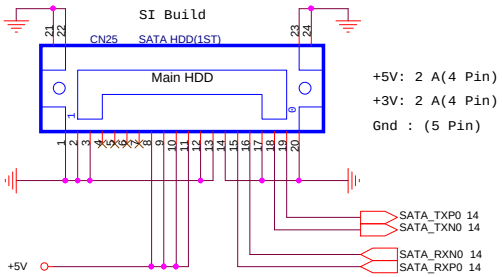
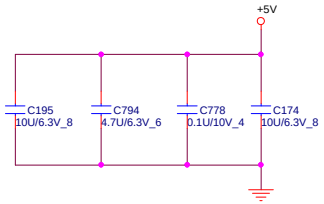
http://mycomp.su/x/

SATA CD-ROM



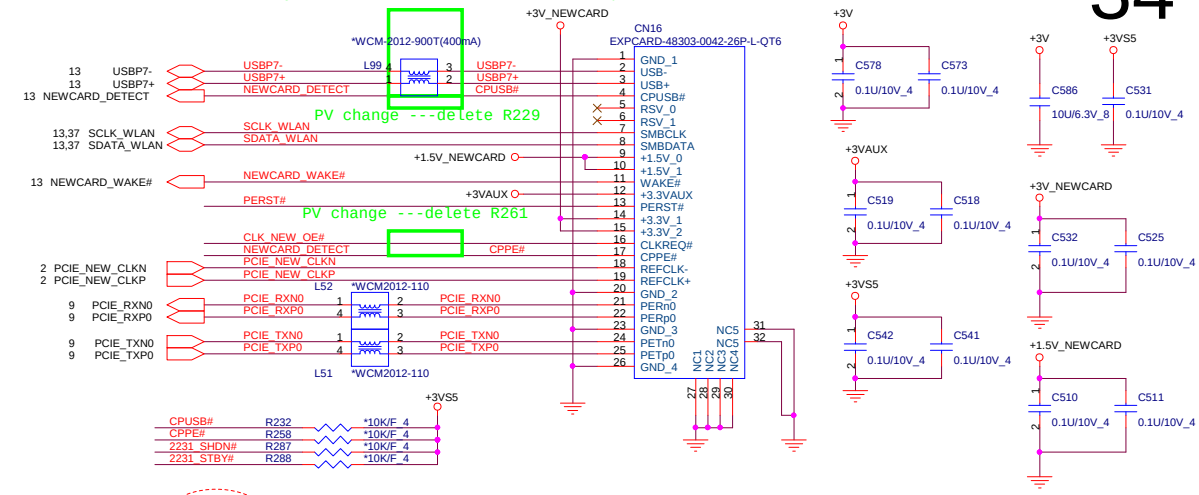


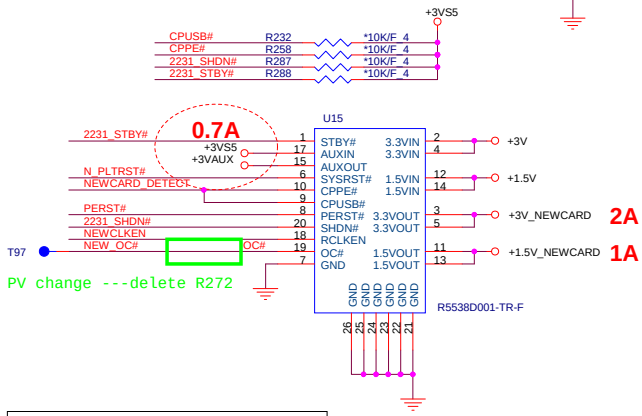


NEWCARD

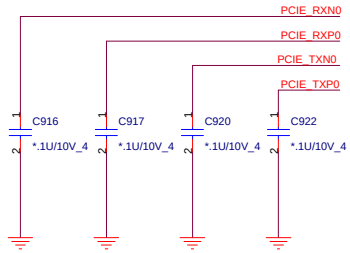
NEWCARD (PCIEXPRESS*1 + USB*1)

PV change ---delete R222,R226 , add short pad

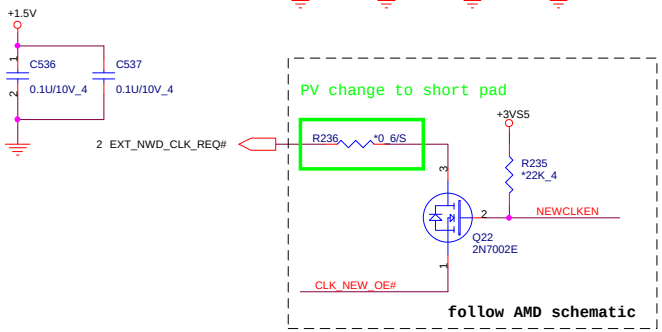


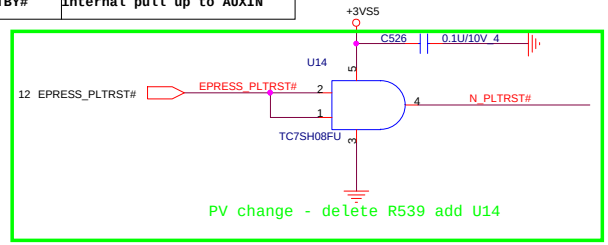


For HP request to reserve



R5538 NEW CARD POWER SWITCH	
pin name	pull hi/low
CPPE#	internal pull up to AUXIN
SYSRST#	internal pull up to AUXIN
CPUSB##	internal pull up to AUXIN
PERST#	a logic level power good
SHDN#	internal pull up to AUXIN
RCLKEN	internal pull up to AUXIN
OC#	over current status
STBY#	internal pull up to AUXIN





NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NEW CARD/SATA ODD/SATA HDD	1A

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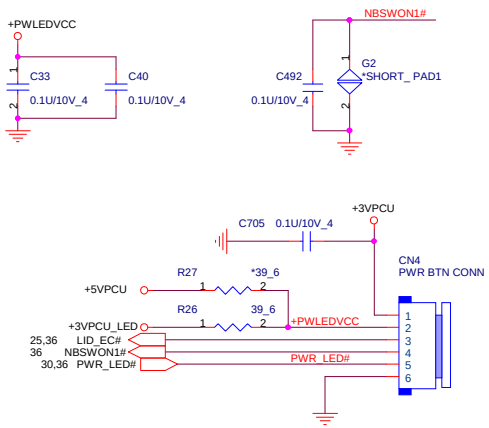
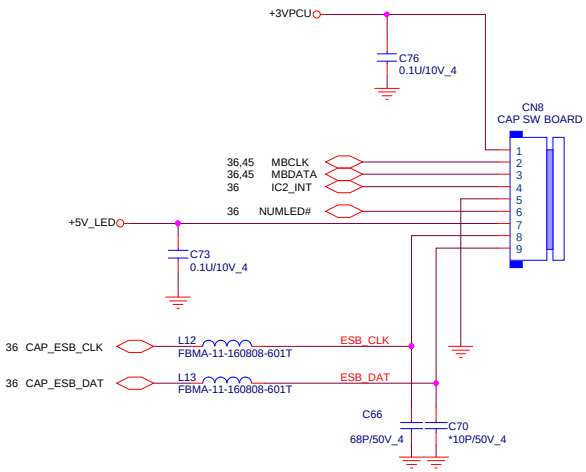
http://mycomp.su/x/

POWER BUTTON CONNECT

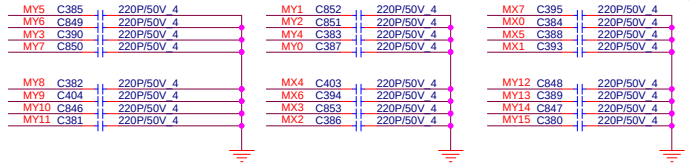


1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4.POWERON#
5. PWRLED#
6. GND

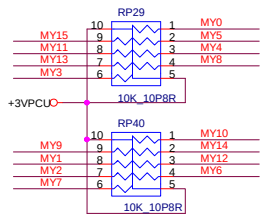
CAP SW CONNECT

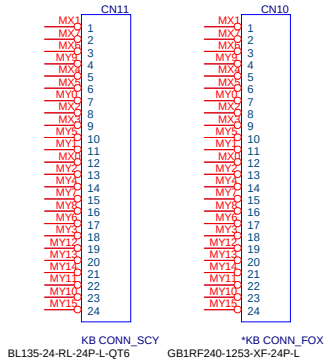


1. +3VPCU
2. MBCLK
3. MBDATA
4. CAP_INT
5. GND
6. NUM LOCK LED
7. +5V
8. ESB_CLK
9. ESB_DAT



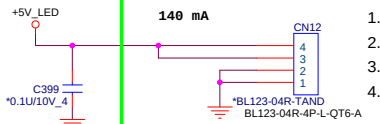
KEYBOARD PULL-UP



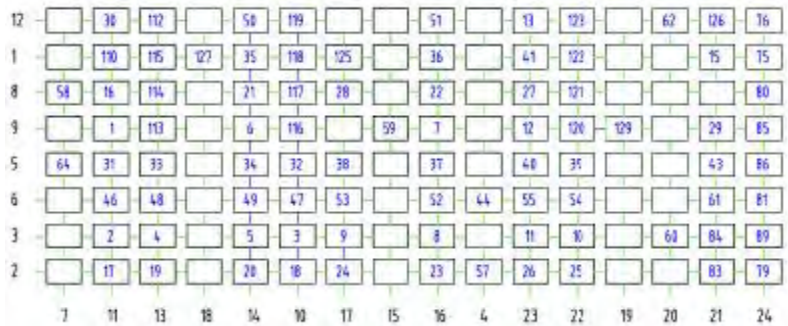


PV change - REMOVE CN12

140 mA



1.LEDVCC
2.LEDVCC
3. NC
4. GND



PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LED/KEYBOARD/SW	1A

NB5/RD5

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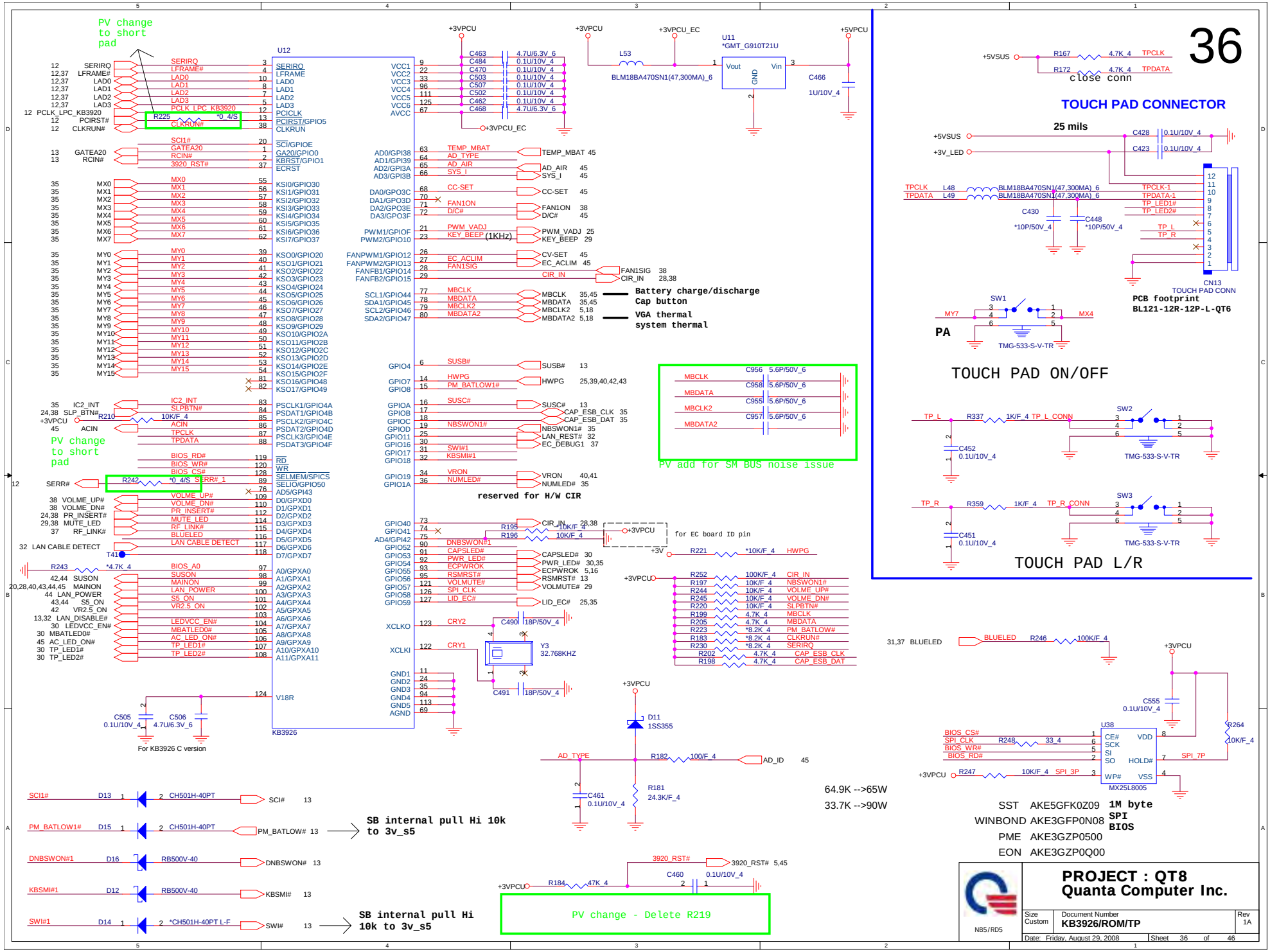
http://mycomp.su/x/



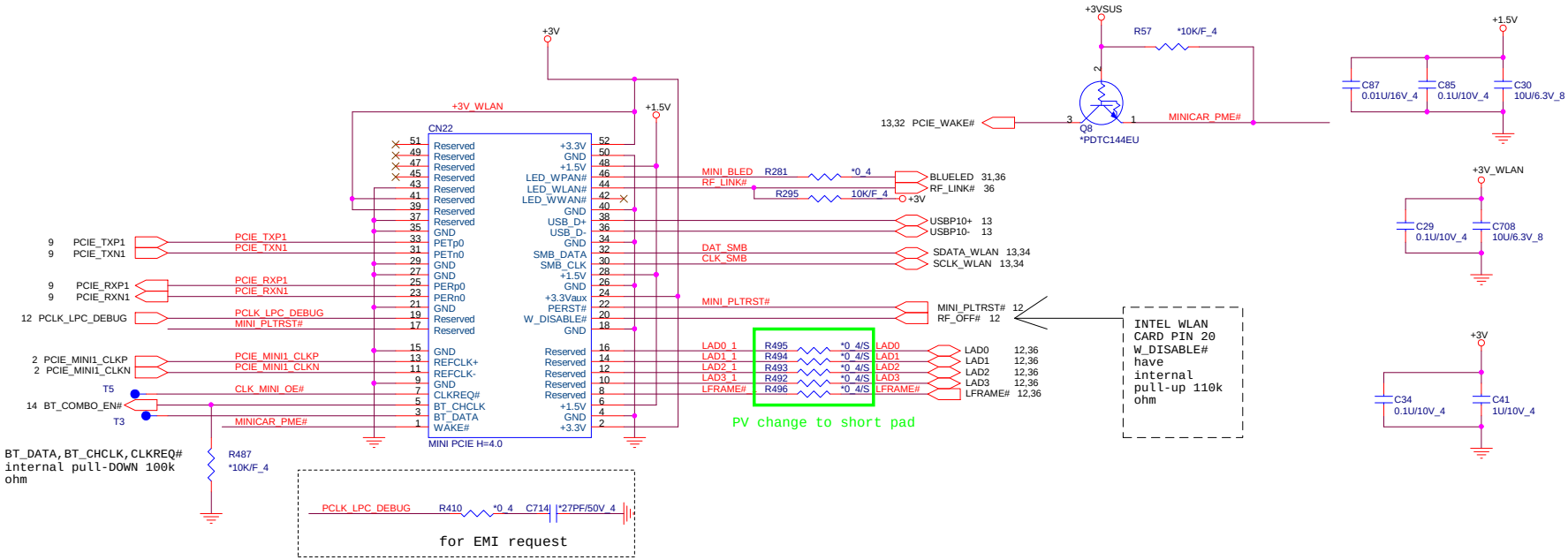
PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KB3926/ROM/TP	1A

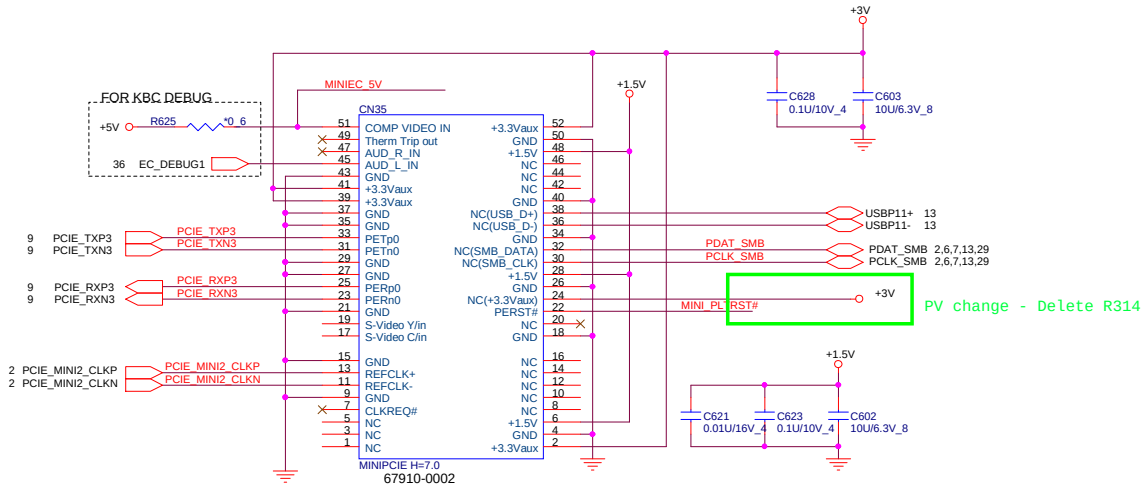
Date: Friday, August 29, 2008 Sheet 36 of 46

http://mycomp.su/x/

Mini PCI-E Card 1 WLAN



Mini PCI-E Card 2 TV tuner card



PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Mini CARD X 3	1A

NB5/RD5

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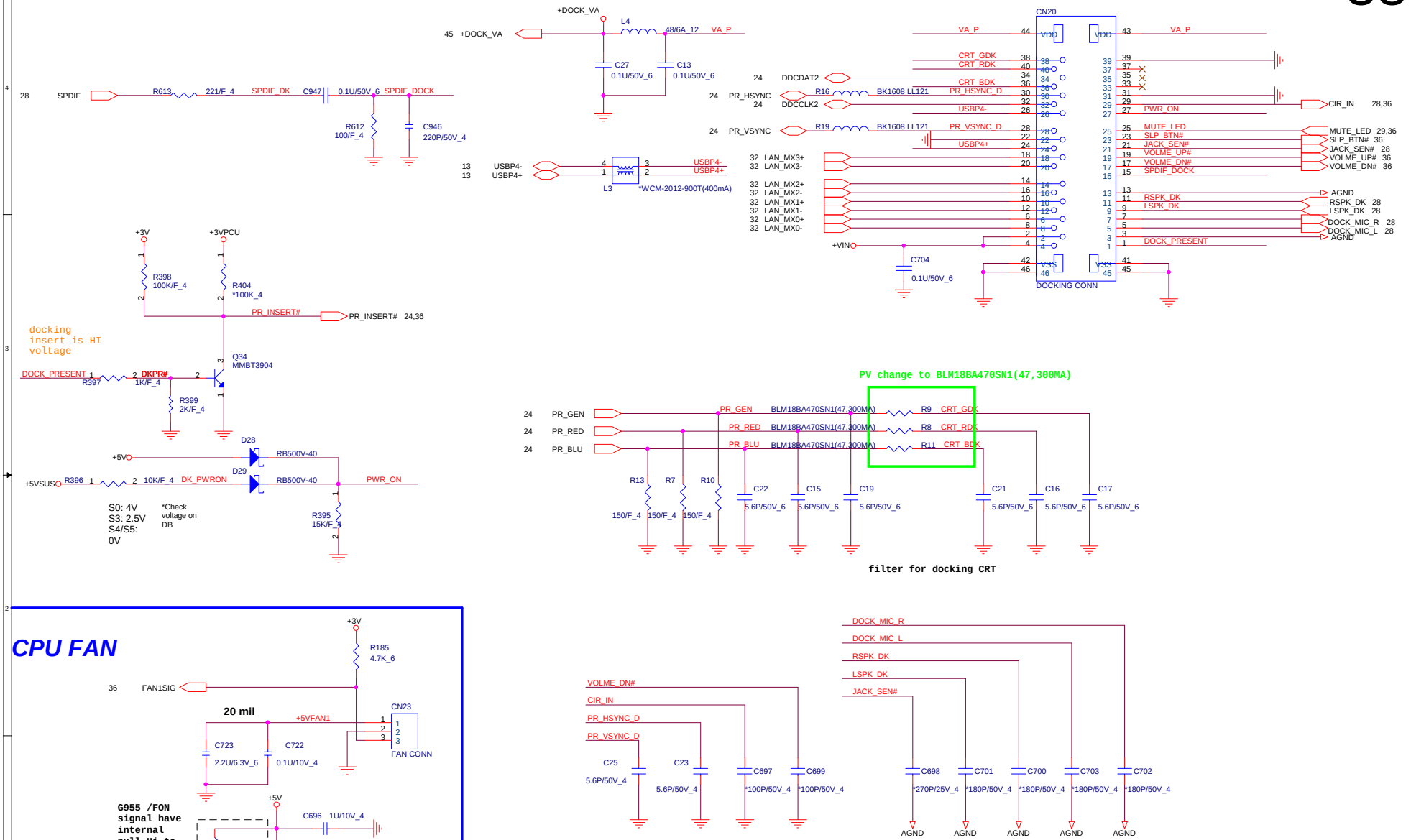
http://mycomp.su/x/

CABLE DOCK

support 6A 200mils
CX000480005



NB5/RD5	**PROJECT : QT8** **Quanta Computer Inc.**
Size: Custom	Document Number: **CABLE DOCKING/FAN**
Rev: 1A	
Date: Friday, August 29, 2008	Sheet 38 of 46

http://mycomp.su/x/

DC/DC +3VPCU/+ 5VPCU/ +12VALW

+3V 2,3,5,6,7,10,11,12,13,14,15,16,20,24,25,26,27,28,29,30,31,32,34,36,37,38,44

+5VPCU 28,29,35,36,40,41,42,43
+3VPCU 5,12,25,30,31,35,36,38,41,42,43,45
+3VSUS 13,26,31,37,40,42,44
+3VS5 5,7,12,13,14,15,16,25,27,34,44
+5VSUS 25,31,36,38,44
+5V 5,15,20,24,25,26,28,29,30,31,34,37,38,43,44
+LANVCC

TON: 5V / 3.3V
GND = 400 / 500KHz
REF = 400 / 300KHz
VCC = 200 / 300KHz

DB modify

PV modify

Del PR159 for TP on PV

Place these CAPs close to FETs

Place these CAPs close to FETs

5 Volt +/- 5%
+5VPCU
C/C:8A
P/C:10A

3.3 Volt +/- 5%
+3VPCU
C/C:8A
P/C:10A

Vout=0.7(Ra+Rb)/Rb

Rb around 49.9k

Rds(on) 15m ohm

Rds(on) 15m ohm

I_lim*MOSFET(RDSON)=V_ILIM(mV)/10
V_ILIM(mV)=5uA*R_ILIM

+12VALW is +15V power level

Please use +15VALW to prevent voltage rating issue

+3V
6.76A
S0-S1

+3VS5
0.5A
S0-S5

+3VSUS
1.84A
S0-S3

+5V
4.31A
S0-S1

For EMI-SI

+5VSUS
4.5A
S0-S3

+LANVCC
0.27A

PROJECT : QT8
Quanta Computer Inc.

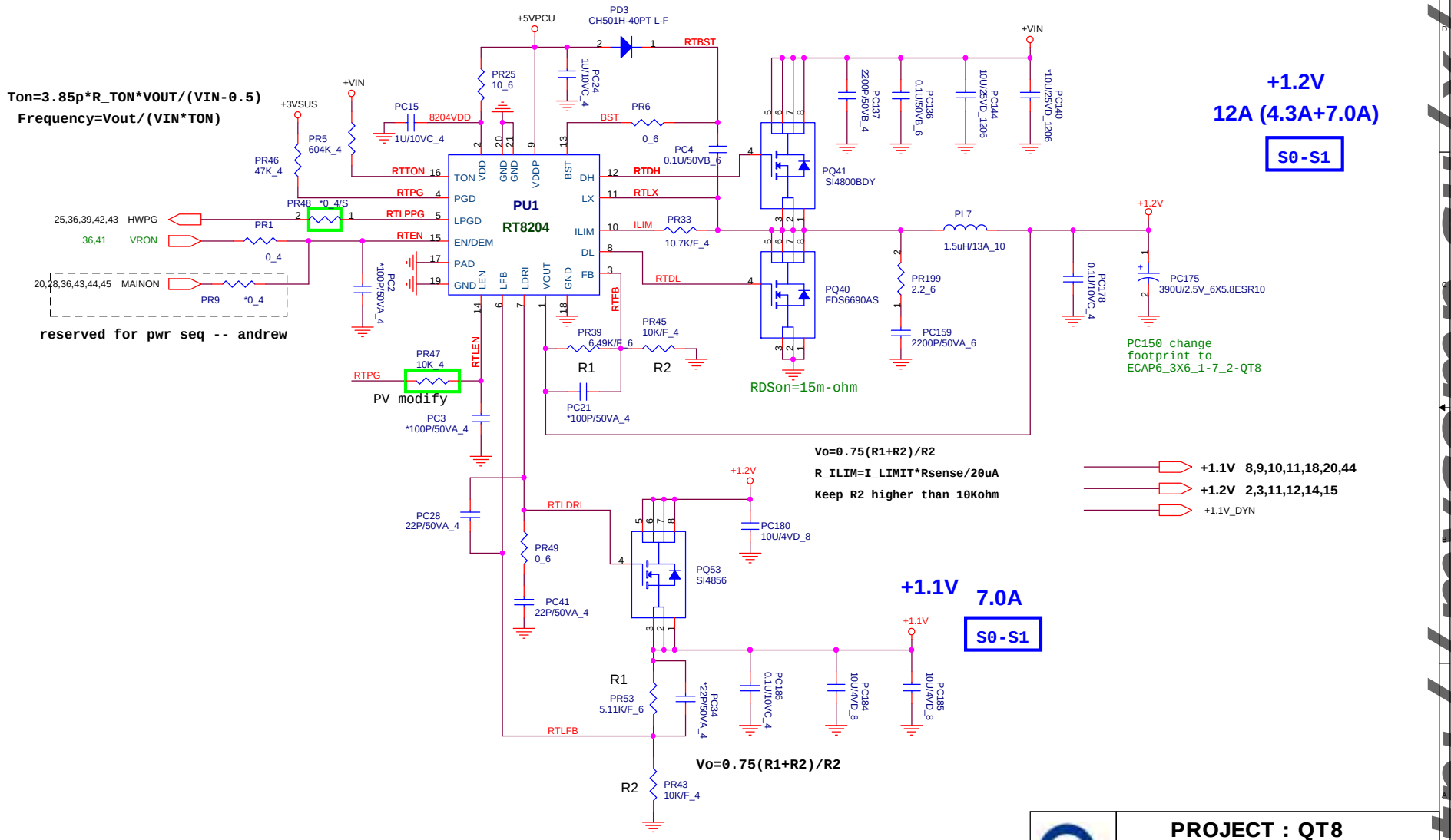
Size: Custom | Document Number: +5V/+3V(ISL6237) | Rev: 1A

Date: Friday, August 29, 2008 | Sheet 39 of 46

NB5/RD5

http://mycomp.su/x/

+1.1V & +1.2V



PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
B	+1.2V & +1.1V(RT8204)	1A

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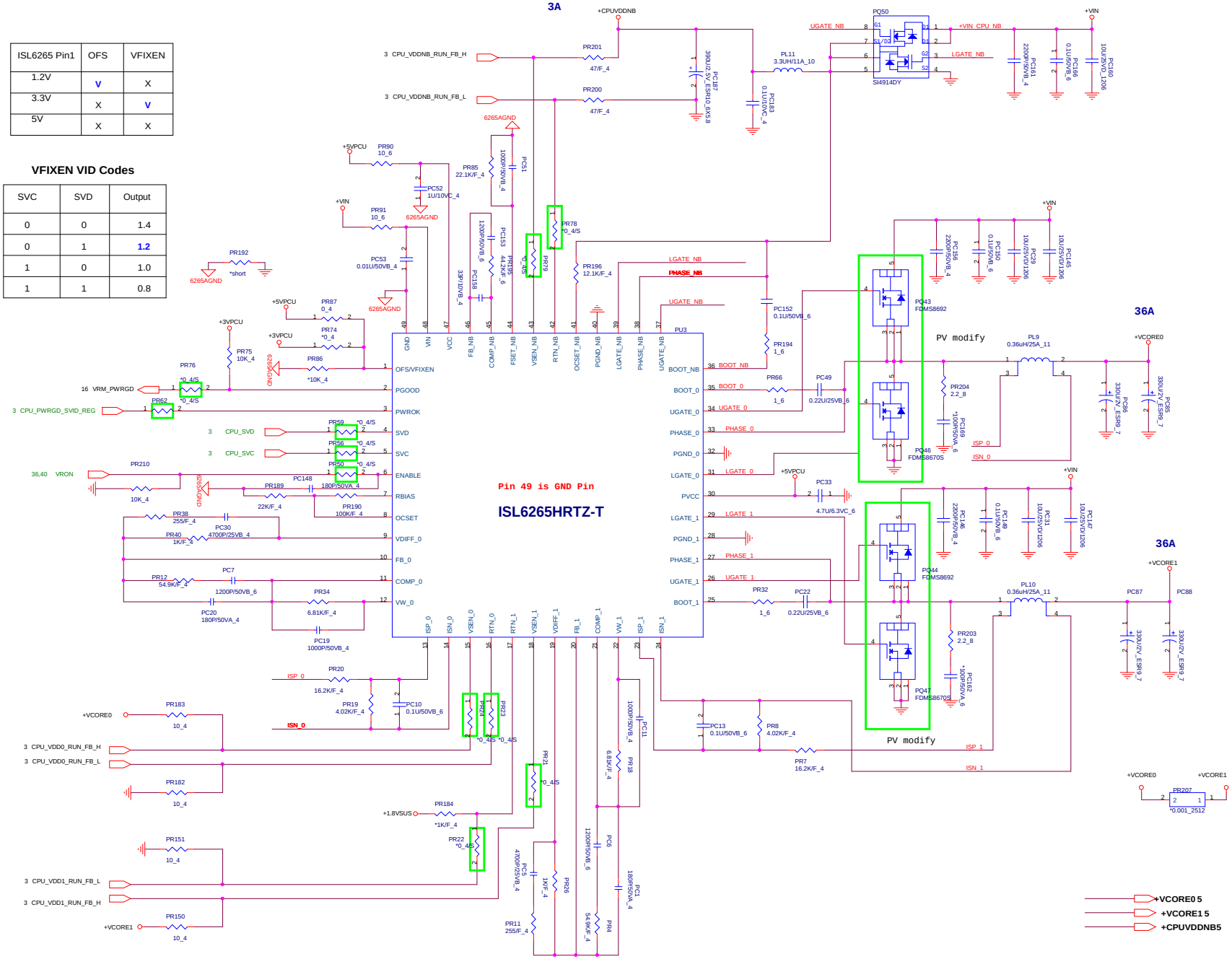
NB5/RD5

http://myconp.su/x/

ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8



PROJECT : QT8
Quanta Computer Inc.

Size C | Document Number CPU_CORE(ISL6265) | Rev 1A

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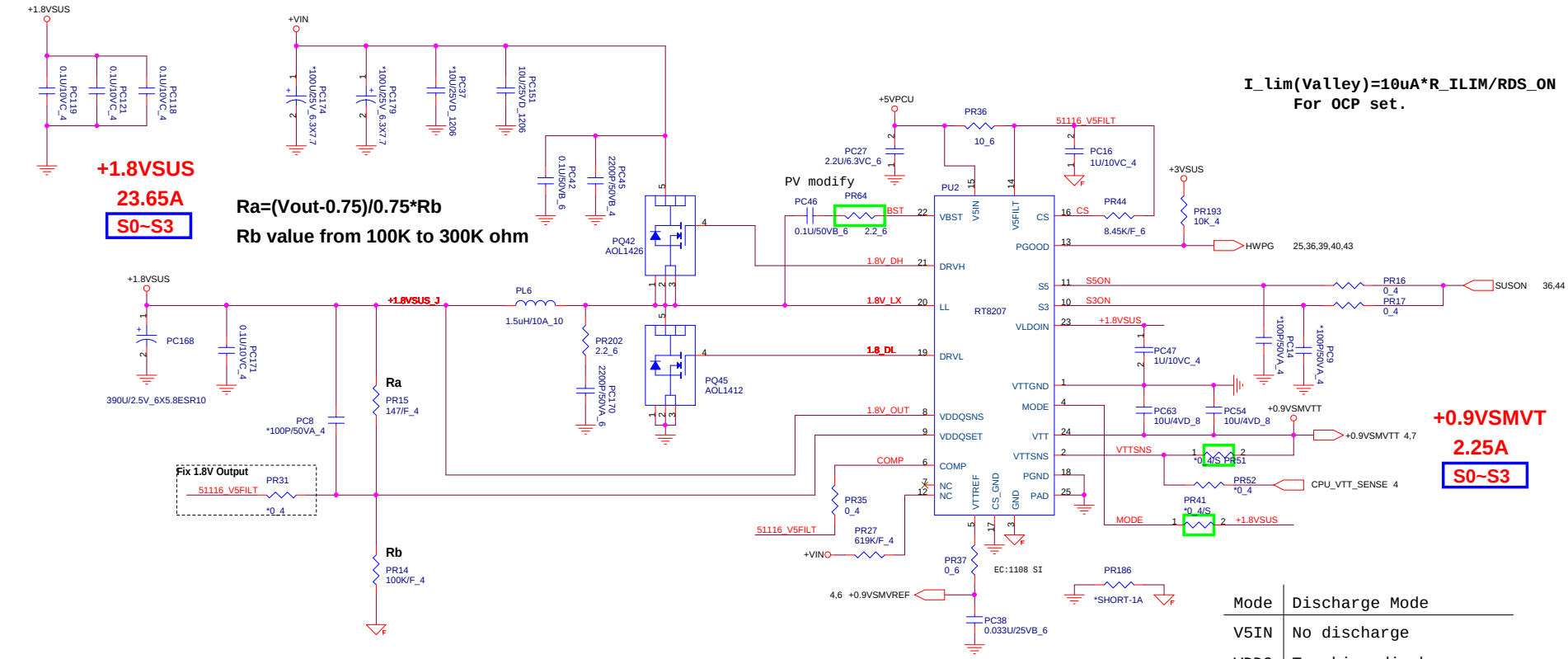
NB5 / RD5

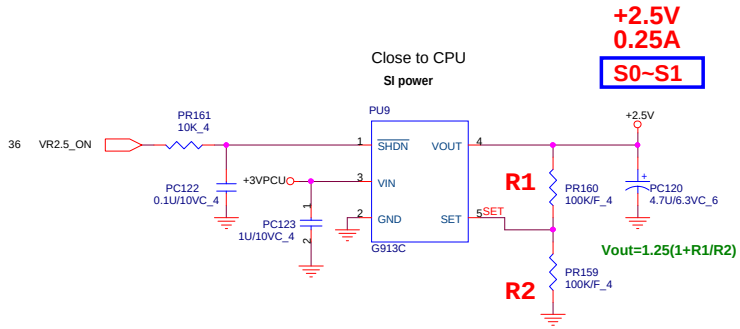
http://mycomp.su/x/

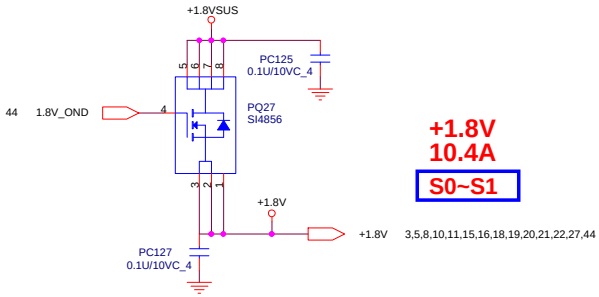
+2.5V 3
+1.8VSUS 3,4,5,6,7,41,43



I_lim(Valley)=10uA*R_ILIM/RDS_ON
For OCP set.

Mode	Discharge Mode
V5IN	No discharge
VDDQ	Tracking discharge
Gnd	Non-tracking discharge





V_TRIP(mV)=R_TRIP(Kohm)*10(uA)

I_OCP=V_trip/Rds_on+I_Ripple/2

VDDQSET	VDDQ(V)	VTTREF and Vtt	Note
GND	2.5	V_ vddqsns/2	DDR
V5IN	1.8	V _vddqsns/2	DDR2
FB	adjustable	V_VDDQSNS/2	1.5V<VDDQ<3V

Discrete:SI4856
UMA:SI4800

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	1.8VSUS/DDR_VTER/+1.8V/2.5V	1A

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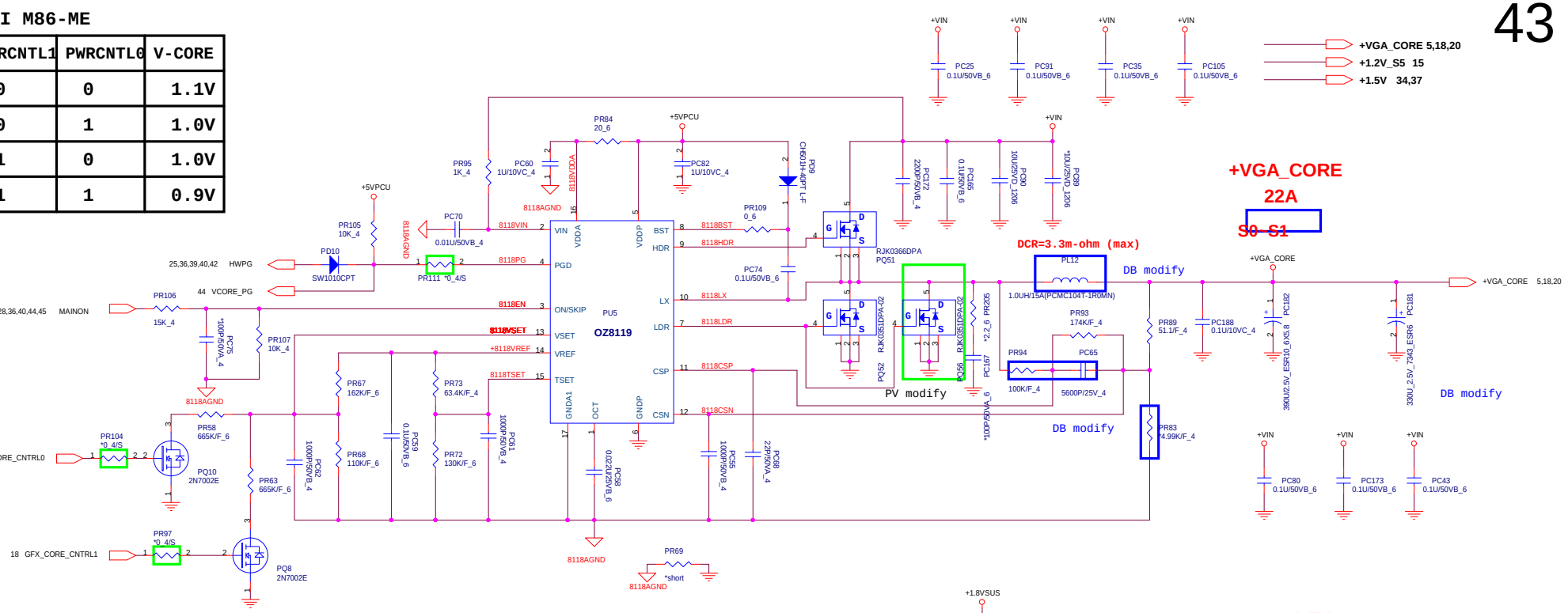
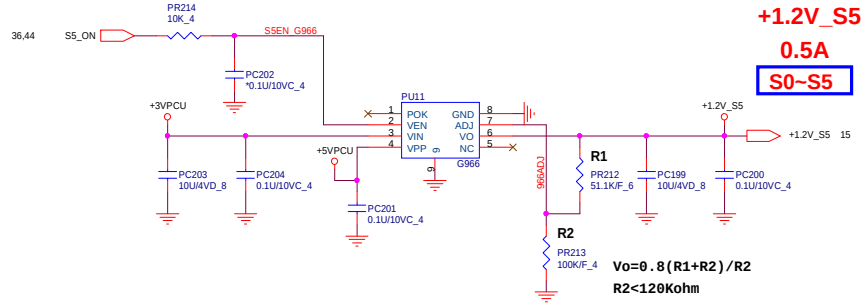
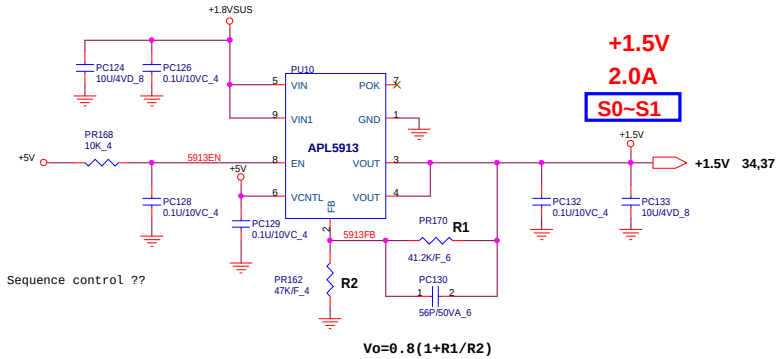
http://mycomp.su/x/

ATI M86-ME

	PWRCNTL1	PWRCNTL0	V-CORE
H	0	0	1.1V
M	0	1	1.0V
M	1	0	1.0V
L	1	1	0.9V







PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	VGA PWR OZ8118/1.2V_S5/+1.5	1A

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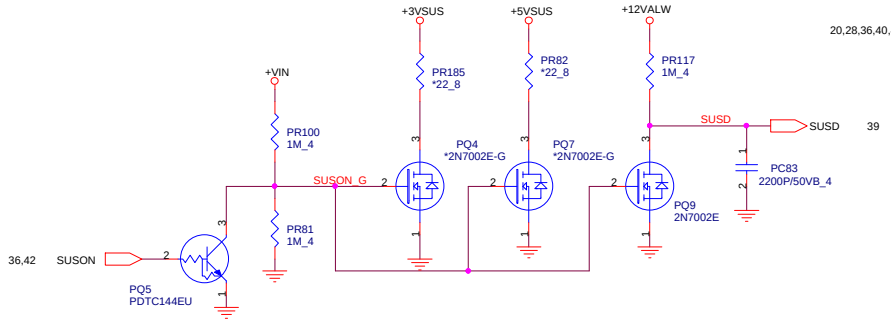
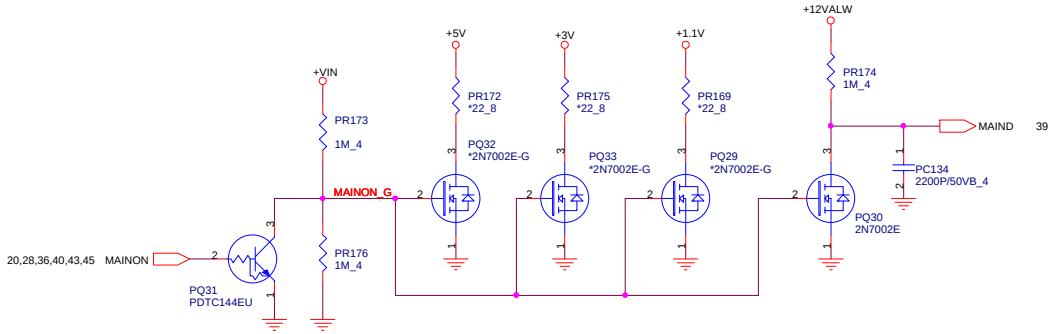
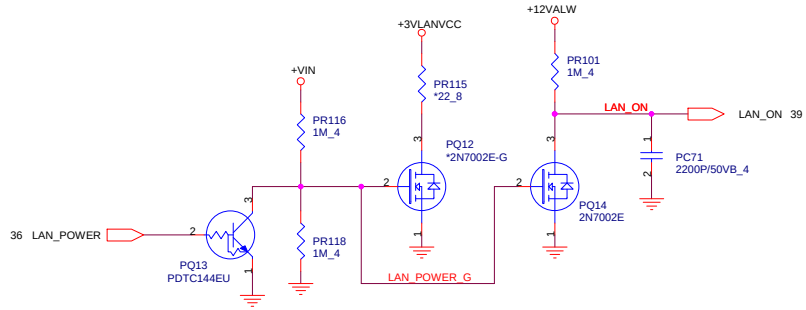
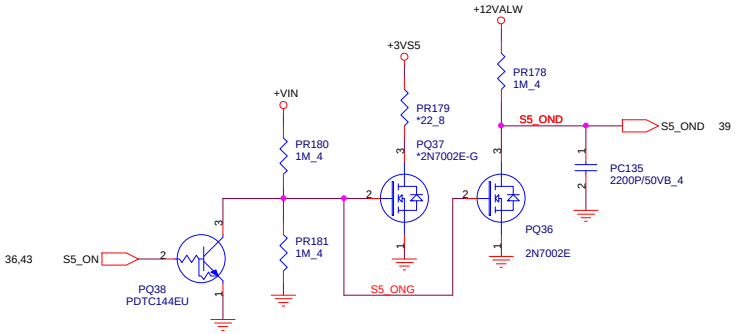
NB5/RD5

http://mycomp.su/x/

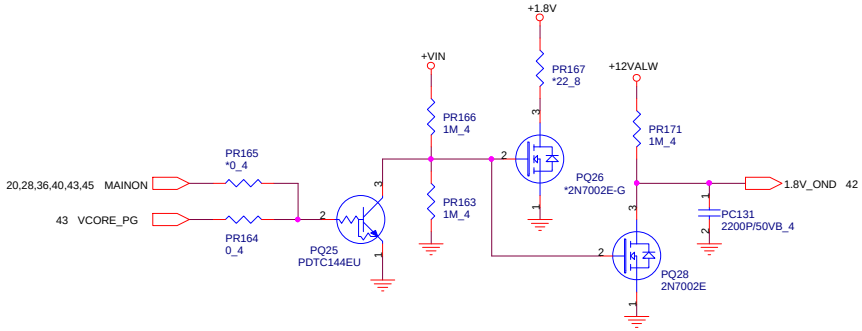






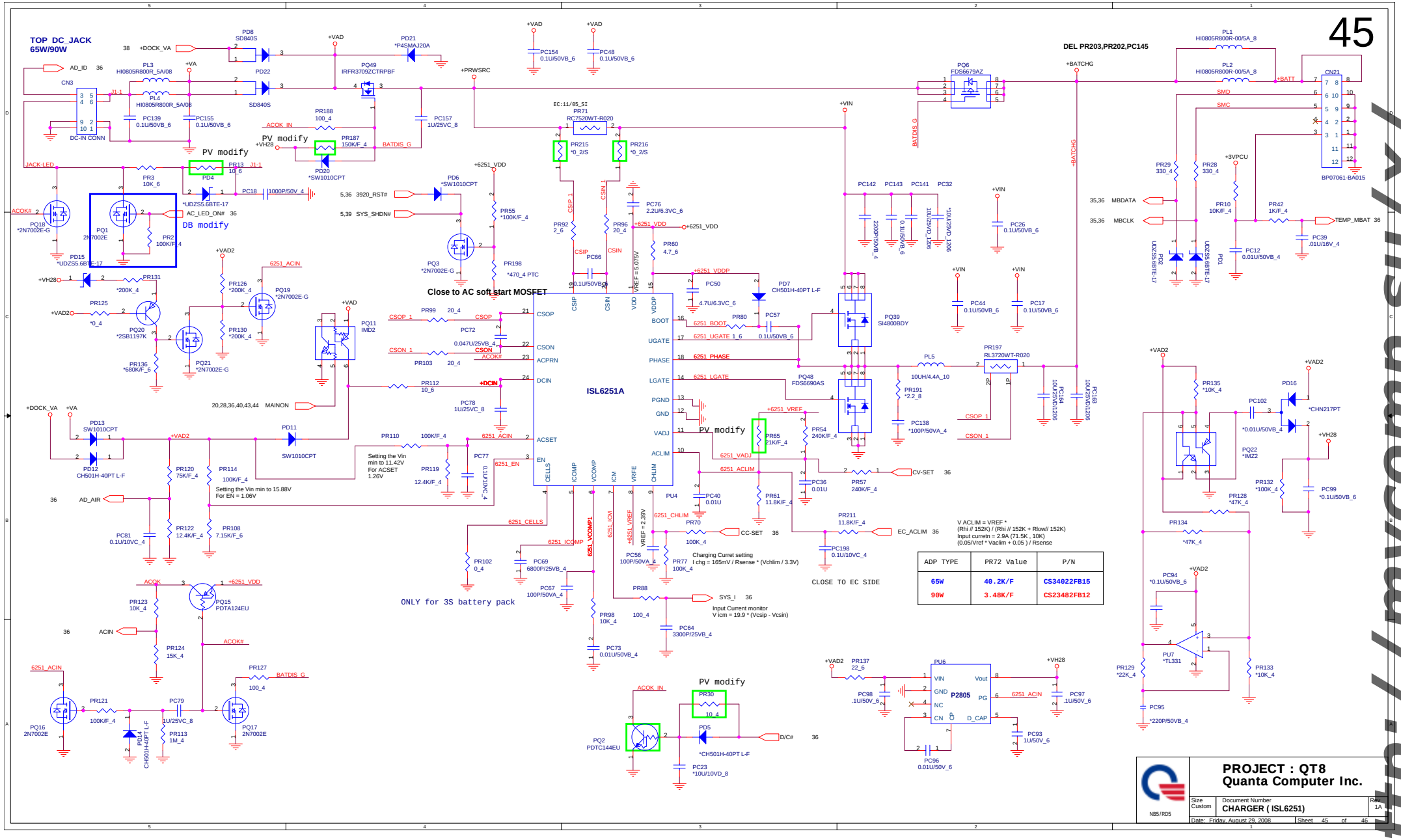


For Discrete Only



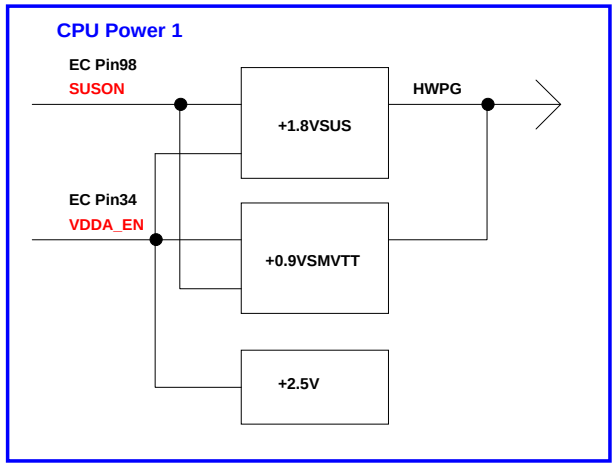
NB5/RD5	**PROJECT : QT8** **Quanta Computer Inc.**	
Size Custom	Document Number **DISCHARGE**	Rev 1A
	Date: Friday, August 29, 2008	Sheet 44 of 46

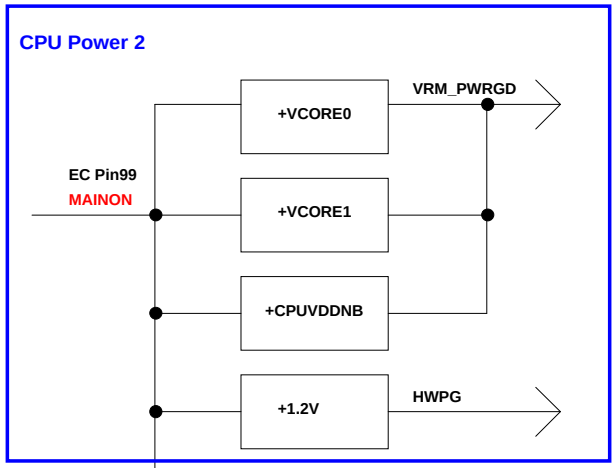
http://mycomp.su/x/

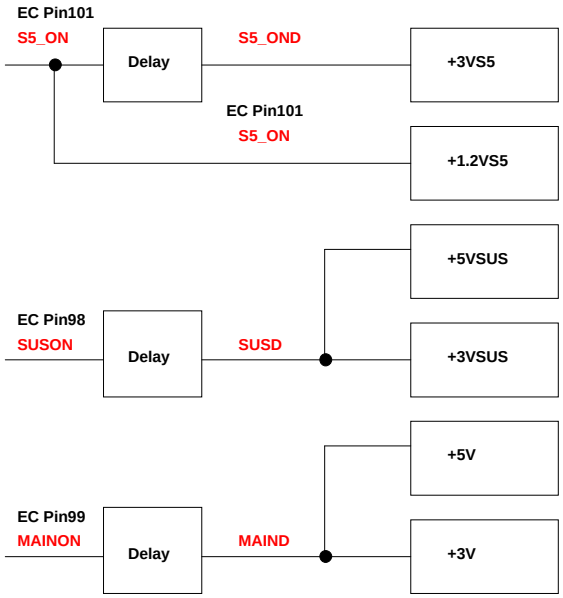


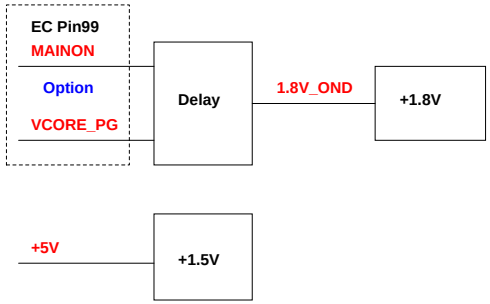
ADP TYPE	PR72 Value	P/N
65W	40.2K/F	CS34022FB15
90W	3.48K/F	CS23482FB12

http://mycomp.su/x/









1	2	3	4	EC Pin76		
S5_ON	SUSON	MAINON	HWPG	ECPWROK	SB_PWRGD_IN	NB_PWRGD_IN
S5_OND	SUSD	MAIND	VCORE_PG	Delay 600ms	3.3V	1.8V
RSMRST#			VRM_PWRGD			

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Power control	1A

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