

Compal confidential

HGL30/HGL31 Schematics Document

Mobile Yonah uFCPGA with Intel 945GM/PM+ICH7-M

LA-3241P

REV:1.0

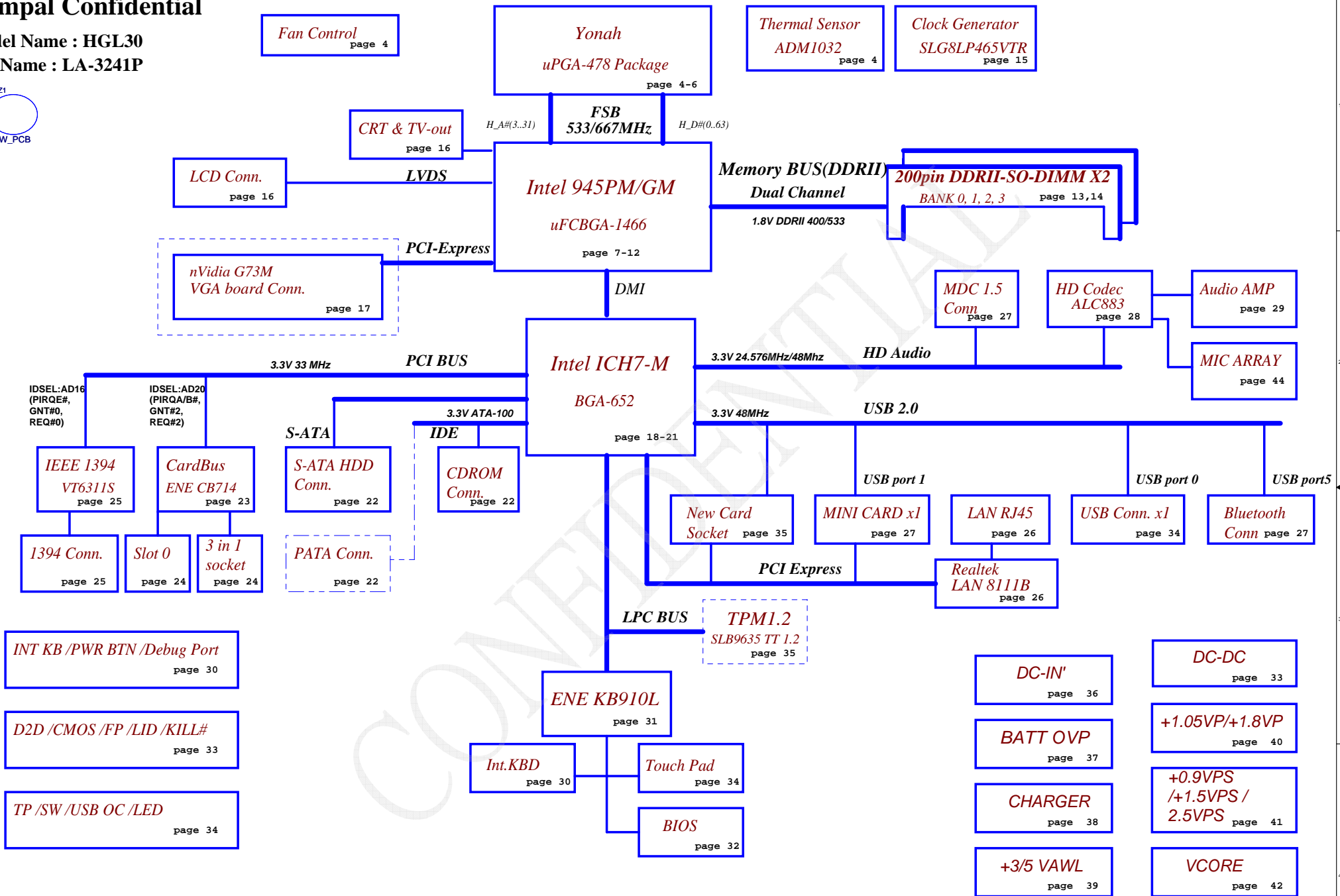
2006/4/28

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				Date:	Wednesday, January 03, 2007	Sheet 1 of 45

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Model Name : HGL30

File Name : LA-3241P



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				Date	Wednesday, January 03, 2007
				Sheet	2 of 45
				Rev	C

Voltage Rails

<div>power plane</div> <div>State</div>	<div>+B</div> <div>LDO3</div> <div>LDO5</div>	<div>+5VALW</div> <div>+3VALW</div>	<div>+1.8V</div> <div>+5V</div>	<div>+5VS</div> <div>+3VS</div> <div>+2.5VS</div> <div>+1.8VS</div> <div>+1.5VS</div> <div>+1.2VS</div> <div>+VGA_CORE</div> <div>+0.9VS</div> <div>+CPU_CORE</div> <div>+VCCP</div>
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

O MEANS ON

X MEANS OFF

S3 : STR

S4 : STD

S5 : SOFT OFF

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD20	2	PIRQA/B
1394	AD16	0	PIRQE

EC SM Bus1 address

EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 100X b
EEPROM(24C16/02)	1010 000X b	EEPROM(24C02)	1010 000X b

ICH7 SM Bus address

Device	Address
Clock Generator (SLG8LP465VTR)	1101 001Xb
DDRII DIMM0	1010 000Xb
DDRII DIMM1	1010 010Xb

SKU ID Table

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

SKU ID	HEL30/31 SKU
* 0	HEL30 SKU
1	HEL31 SKU
2	TEST MODE
3	
4	
5	
6	
7	

BOM Structure

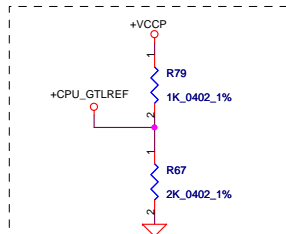
MARK	FUNCTION
@	NC FOR ALL
UMA@	Internal 945GM
VGA@	External G7xM
TPM@	TPM1.2
VP1020@	MIC ARRAY
1394@	1394
SATA@	SATA HDD
ONEMIC@	ONE MIC
IOMP@	IOMP
PATA@	PATA HDD
APA@	HP out from AMP
HPA@	HP out from HP AMP
HP@	HP out from CODEC

USB PORT LIST

PORT	DEVICE
0	LEFT SIDE
1	BLUE TOOTH
2	RIGHT SIDE
3	CMOS
4	RIGHT SIDE
5	FINGER PRINTER
6	NEW CARD
7	

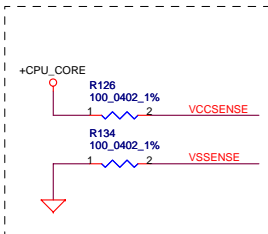
+3VALW	KB910L SB RTL8110SBL/CL	mA 160mA
+CPU_CORE	CPU	36A
+VCCP	CPU NB	2.5A 9.8A (14.7A)
+5VS	EXPRESS CARD HDD ODD MDC APA2066 TPA0211 AD1986 USB PORT * 6	1A 1.5A 1.8A 300mA 1A mA 70mA 3A
+3VS	NB EXPRESS CARD CLK_GEN LCDVCC VGA CARD (G7XM) SB R5C832 BIOS ROM KB910L CB1410	480mA 1A 200mA 1A 655mA 680mA mA 15mA 200mA mA
+2.5VS	VGA CARD (G7XM) NB	130mA (143mA)
+1.8V	DDR2_DIMM NB (667Mhz)	8A 3.1A
+1.8VS	GDDR2 VGA CARD (G7XM)	6A 4.06A
+0.9VREF	DDR2_DIMM	10mA
+0.9VS	GDDR2 DDR2_DIMM	1A 2A
+1.5V	SB	40mA
+1.5VS	NB SB MiniCard EXPRESS CARD VGA CARD (G7XM)	8.9A(13.8A) 3.8A 1A 0.65A 2A

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				C	401426	C
				Date:	Wednesday, January 03, 2007	Sheet 3 of 45



Close to CPU pin AD26
within 500mils.

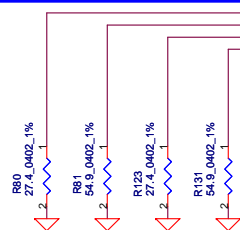
Trace / Width = 4 / 25 mils



Close to CPU pin
within 500mils.

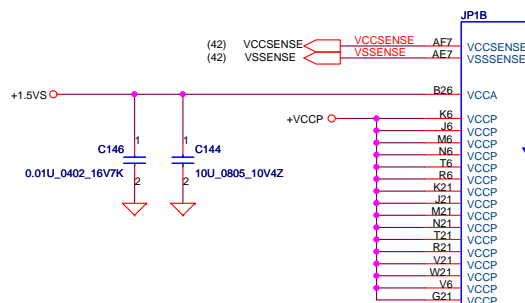
Trace / Width = 18 / 50 mils

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1



Resistor placed within
0.5" of CPU pin. Trace
should be at least 25
mils away from any
other toggling signal.

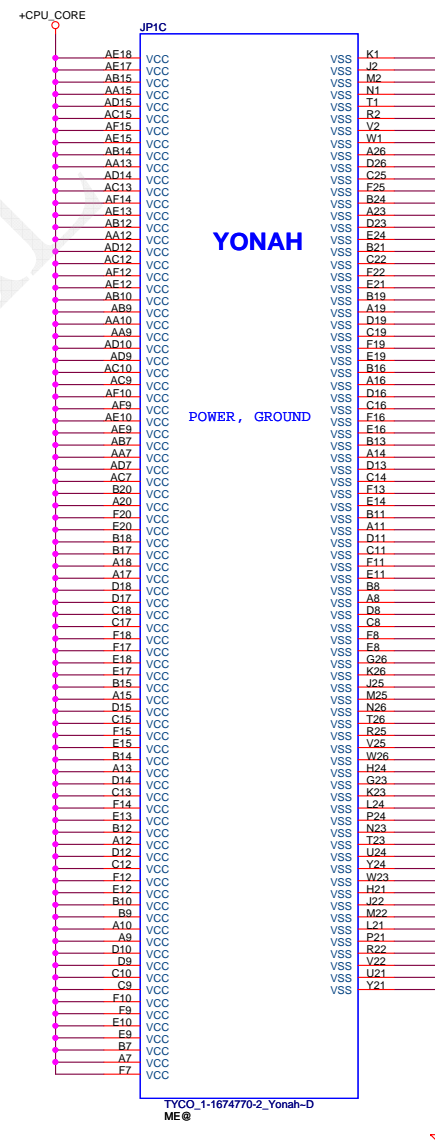
COMP 0/2 Trace / Width = 18 / 25 mils
COMP 1/3 Trace / Width = 5 / 25 mils



YONAH

POWER, GROUND, RESERVED SIGNALS AND NC

TYCO_1-1674770-2_Yonah-D
ME@



YONAH

POWER, GROUND

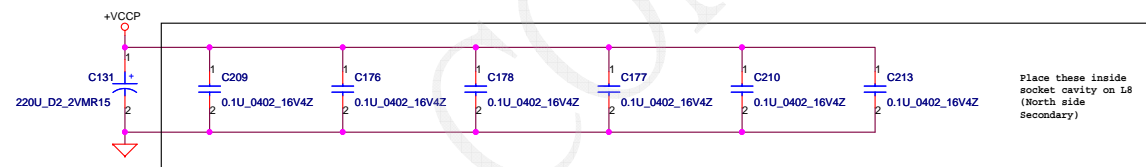
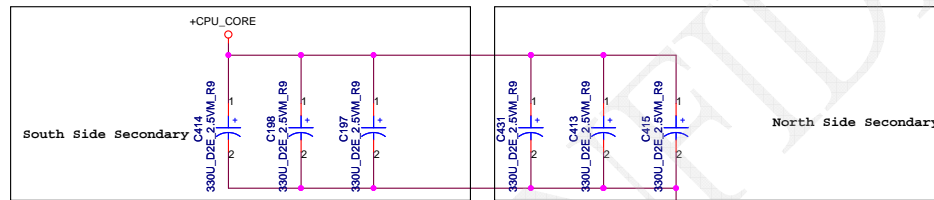
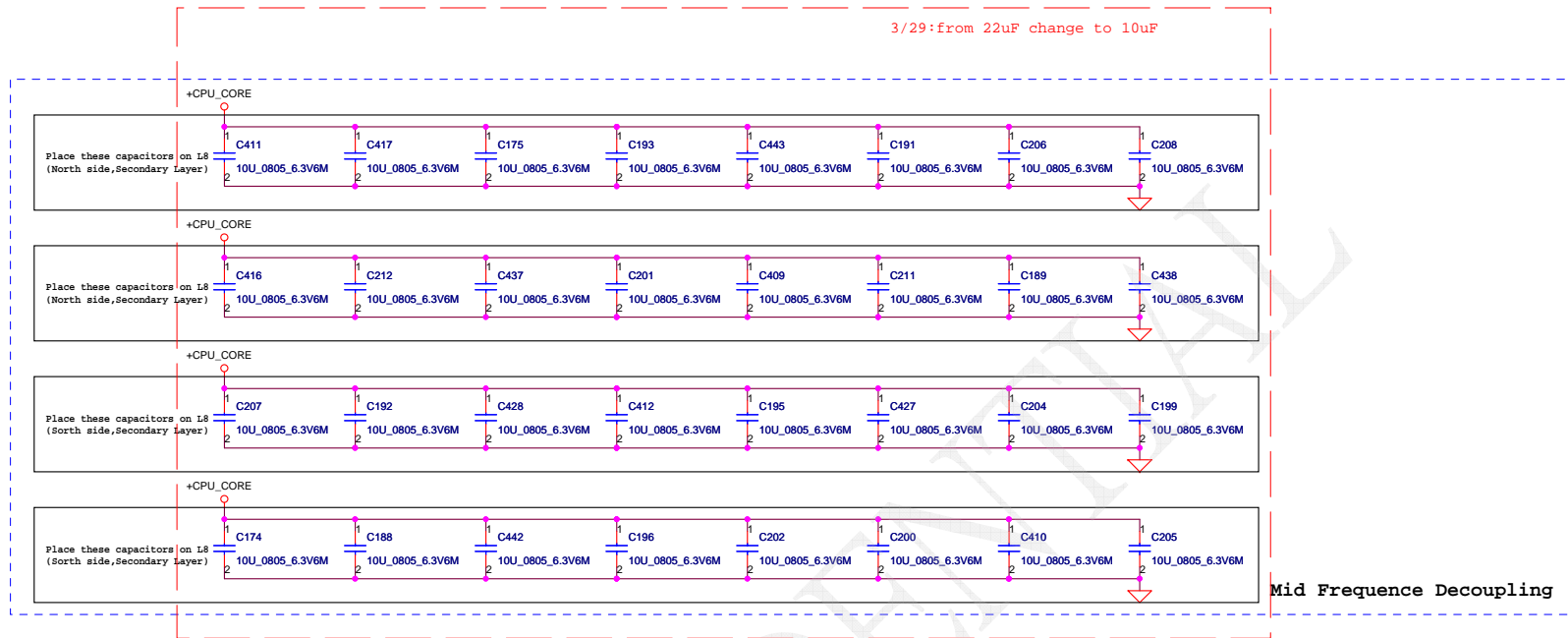
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ME@

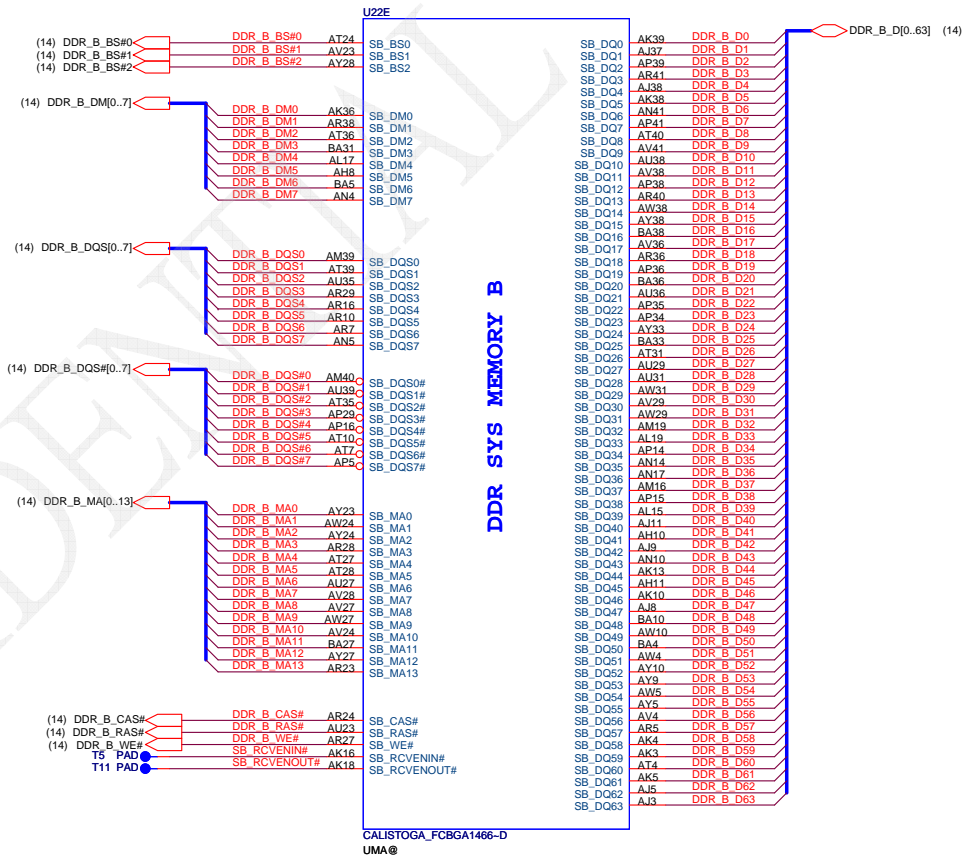
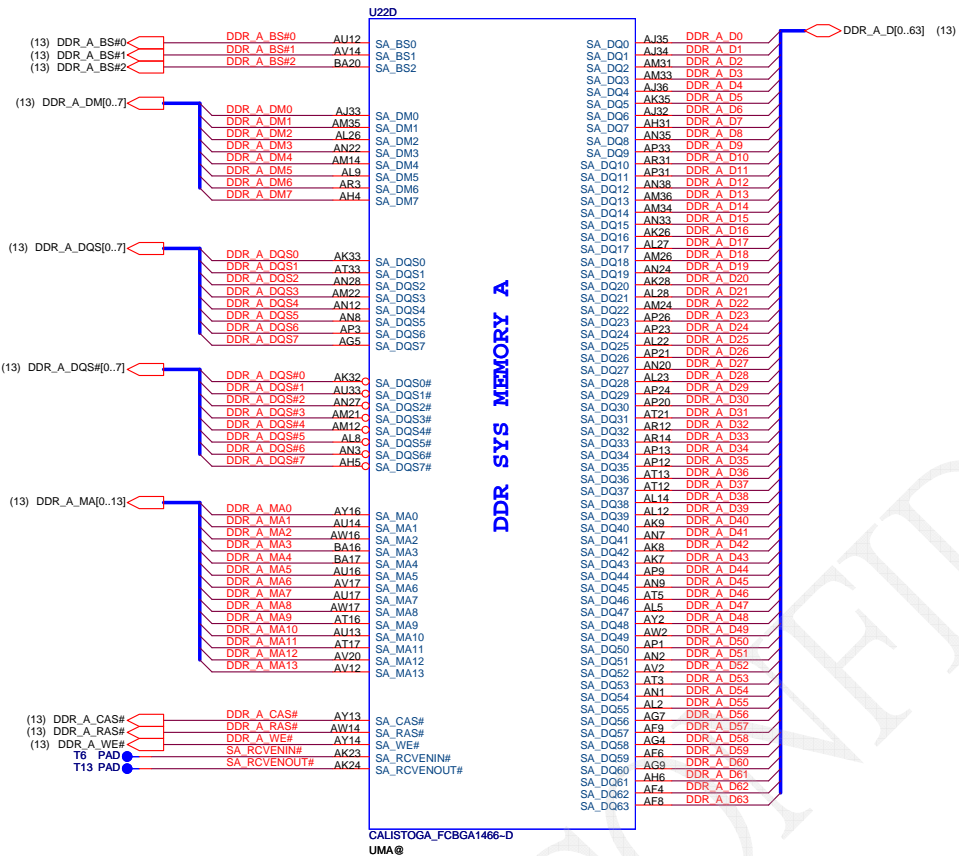
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						Sheet	5 of 45

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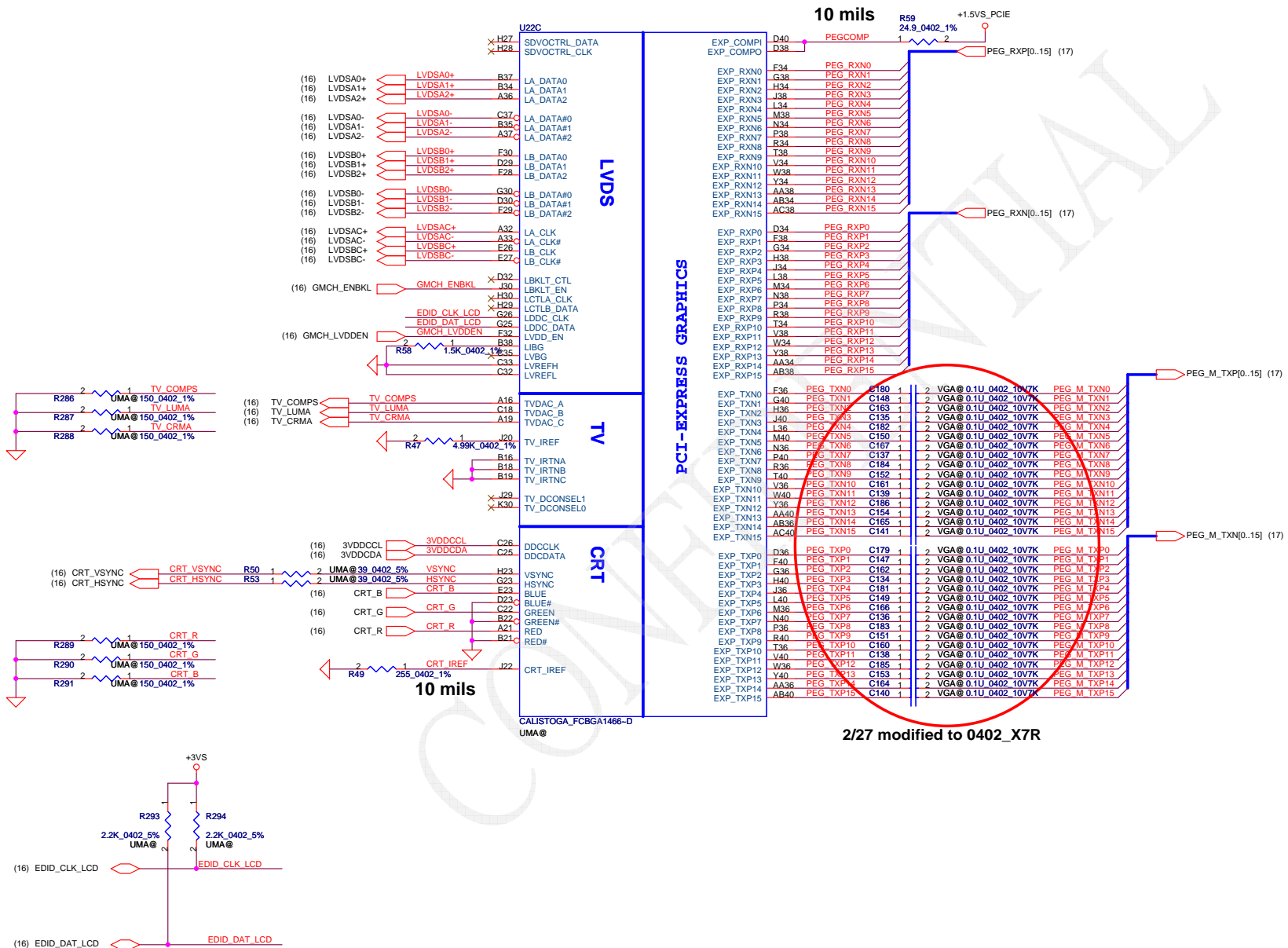
SCHEMATIC, M/B LA-3241P

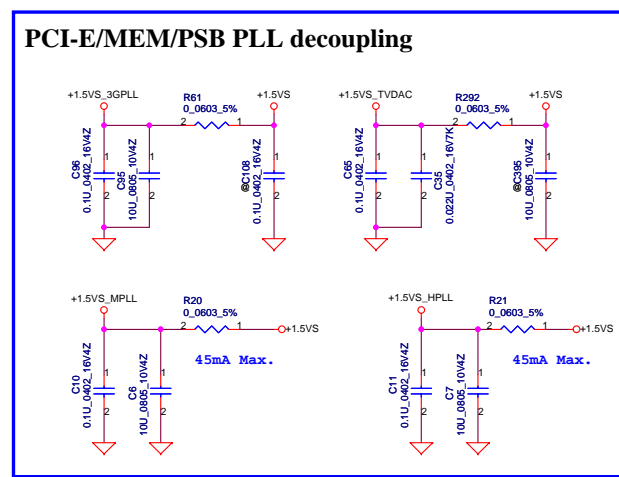
Rev C





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				401426	C
				Date: Wednesday, January 03, 2007	Sheet 8 of 45





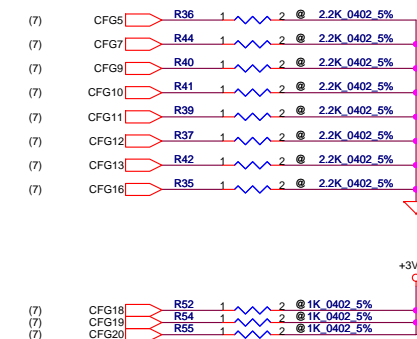
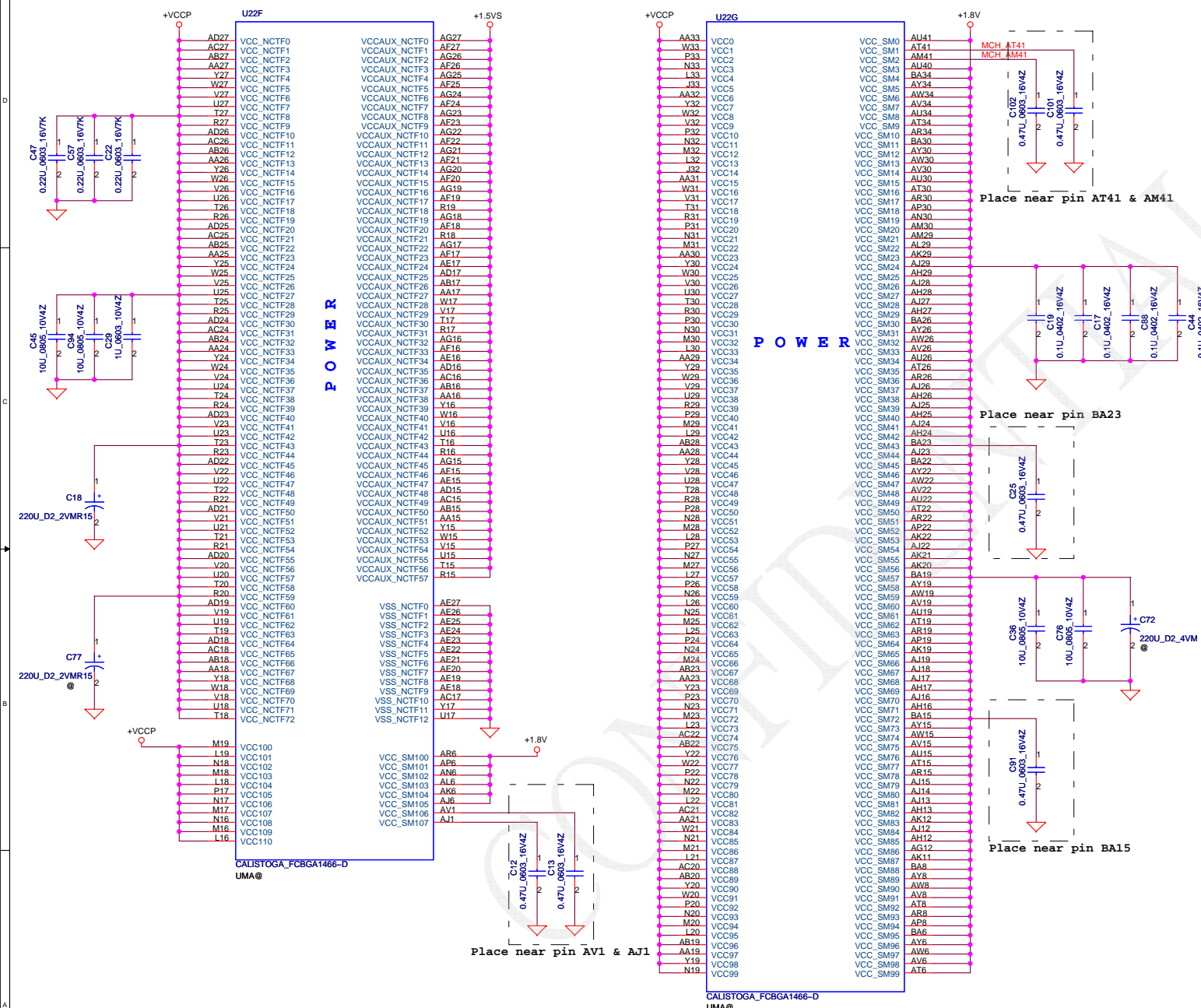
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				Date:	Wednesday, January 03, 2007	Sheet 10 of 45

Strap Pin Table

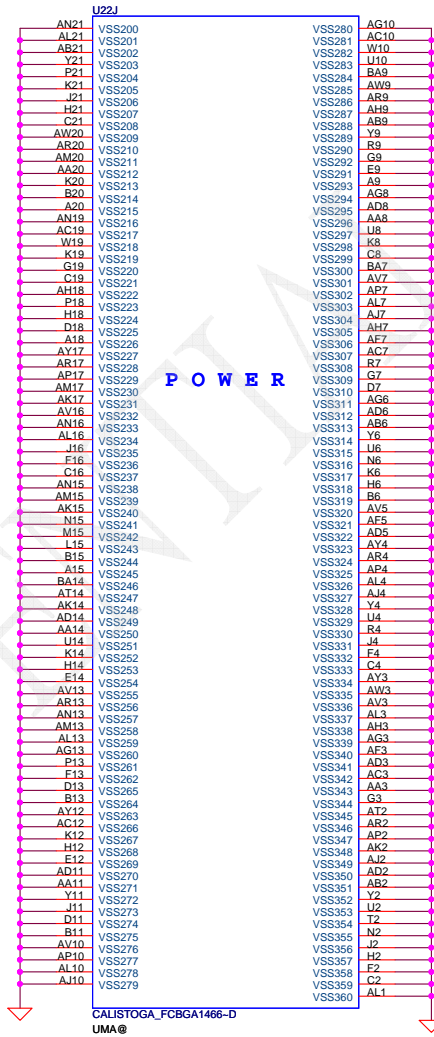
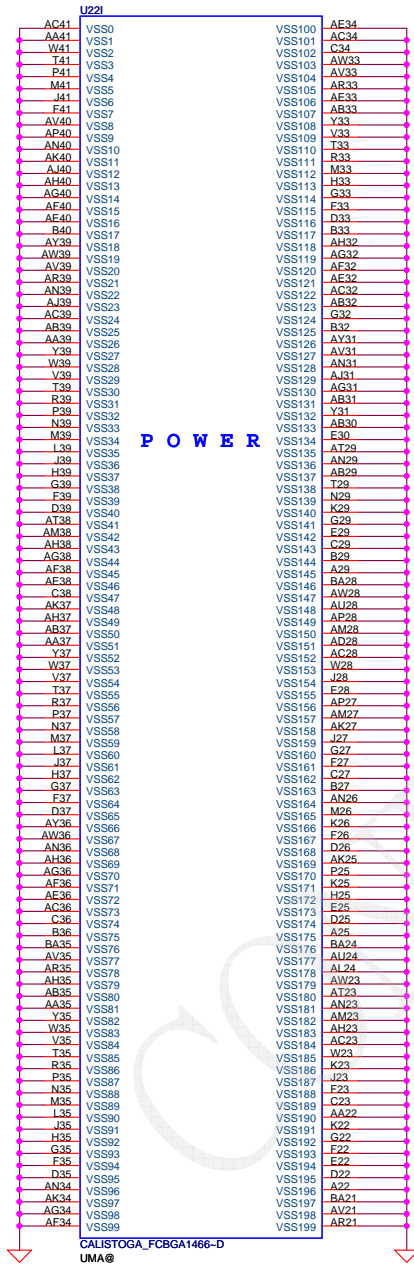
CFG[3:17] have internal pull up

CFG[19:18] have internal pull down

CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU *(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation (Default)*
CFG6	0 = Reserved
PSB 4X CLK Enable	1 = Calistoga *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation *(Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG10 CFG18	10 = 1.05V *(Default) 01 = 1.5V
CFG19	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present *(Default) 1 = SDVO Device Present
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. *(Default) 1 = PCIE/SDVO are operating simu.

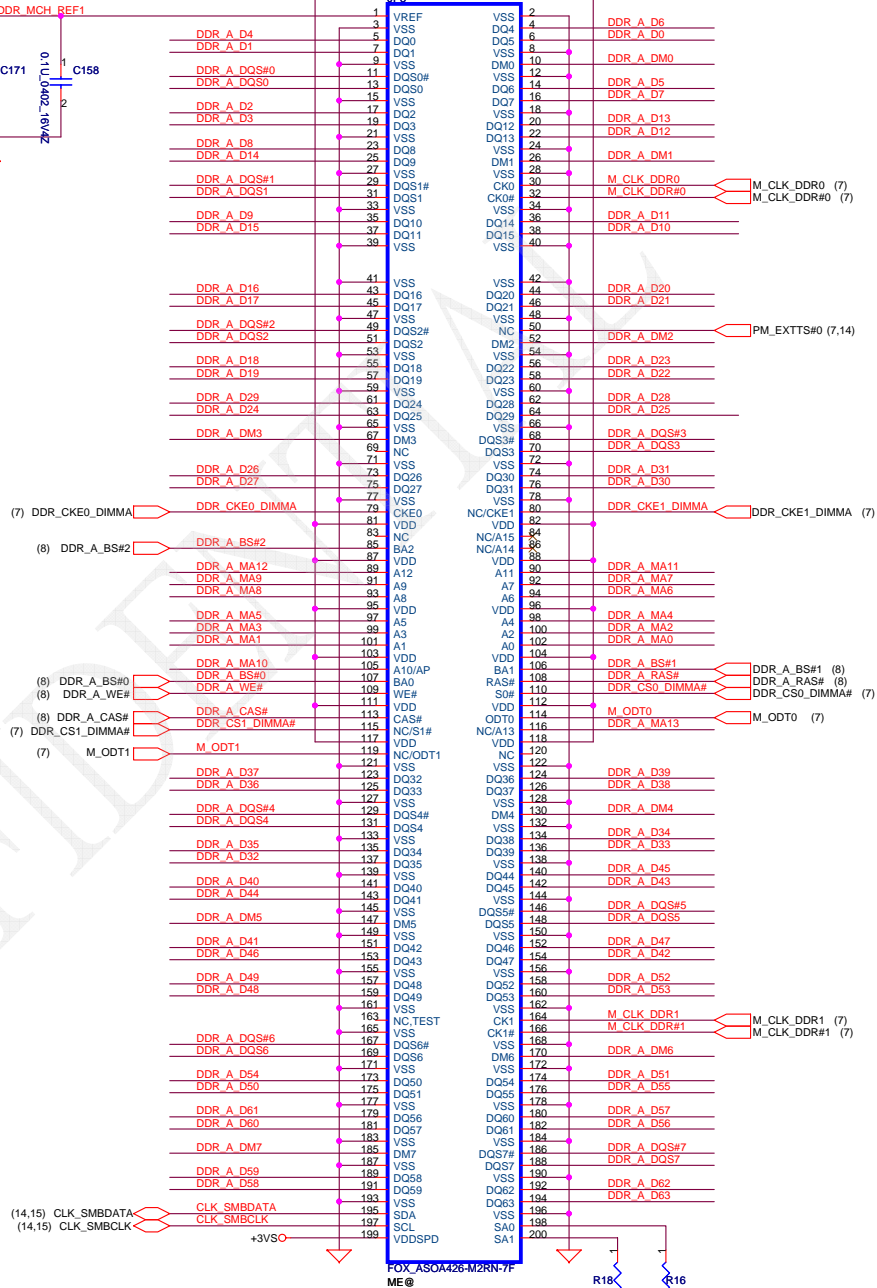
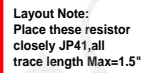
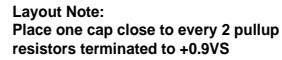


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						Document Number		Rev	
						401426		C	
						Date: Wednesday, January 03, 2007		Sheet 11 of 45	





Layout Note:
+DDR_MCH_REF
trace width and
spacing is 20/20.



SO-DIMM A

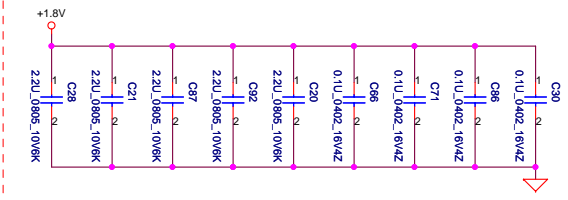
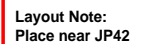
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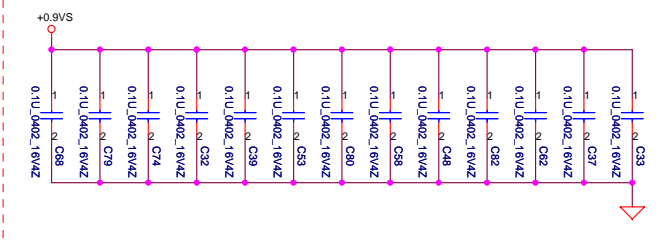
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Rev	Doc Number	Rev C	
426	401426		
Date:	Wednesday, January 03, 2007	Sheet	13 of 45

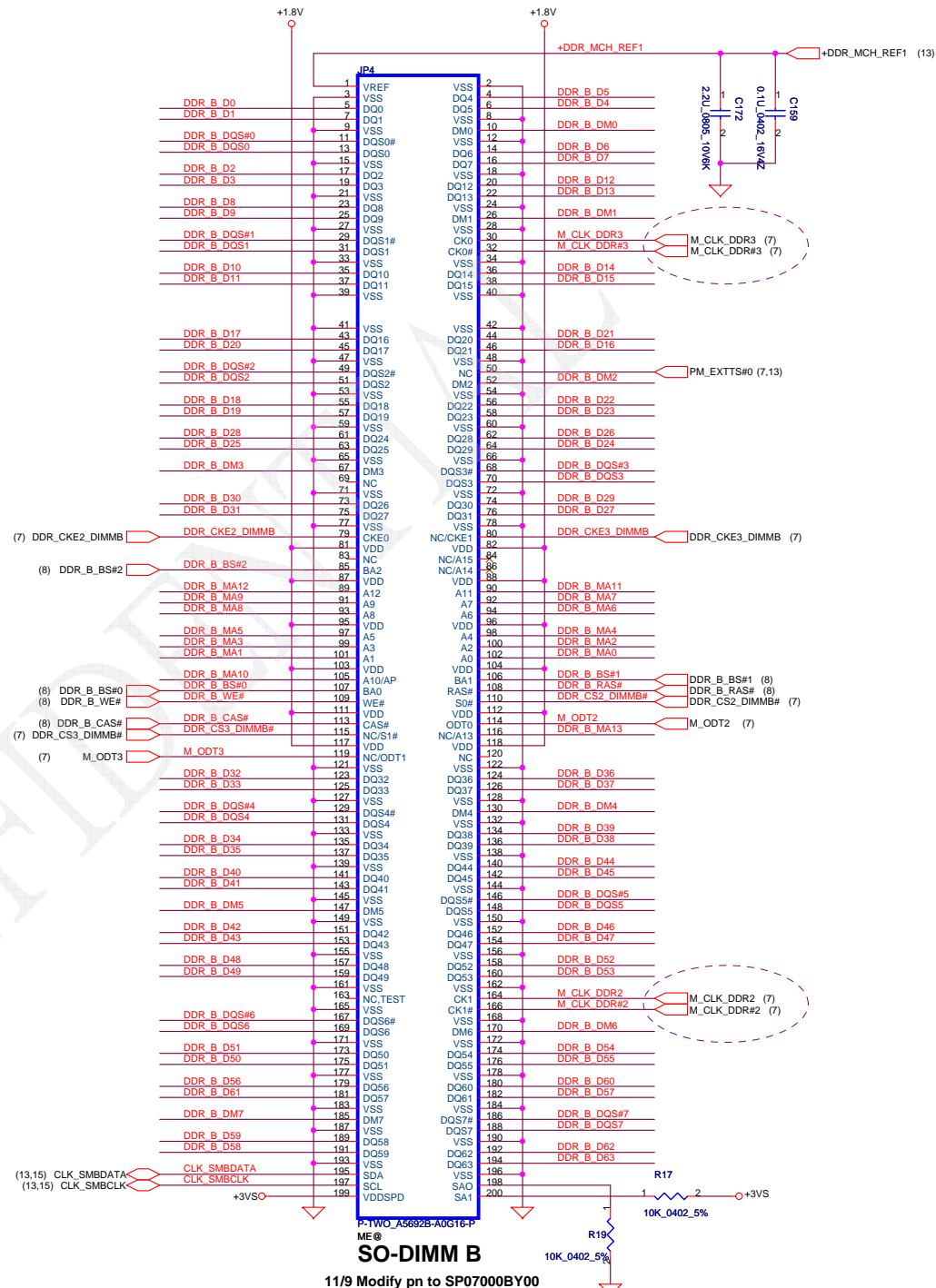
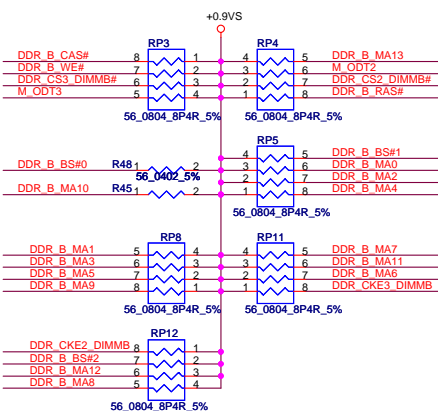
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				401426	C
Date:		Wednesday, January 03, 2007		Sheet	13 of 45



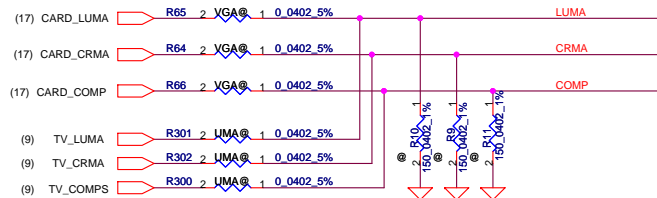
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



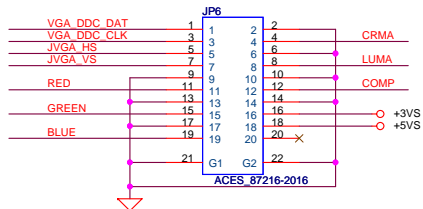
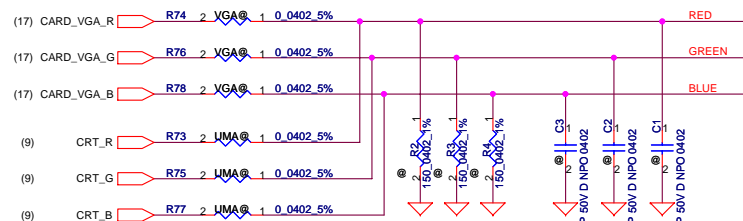
Layout Note:
Place these resistor
closely JP42,all
trace length Max. 4.5"



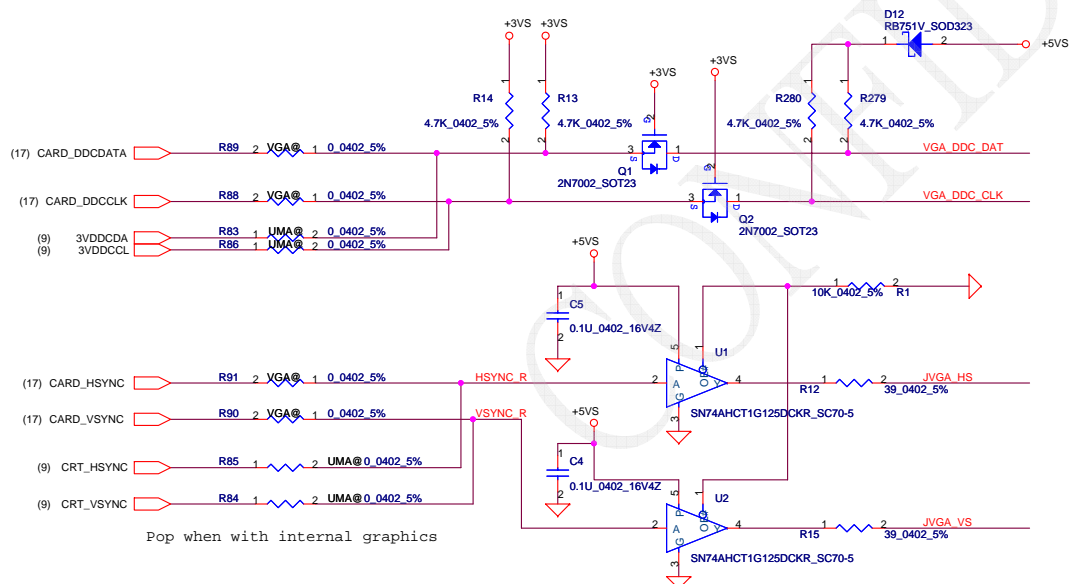
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						Doc. Number
Date: Wednesday, January 03, 2007						401426
Sheet 14 of 45						C

TV-OUT Conn.

Pop when with internal graphics

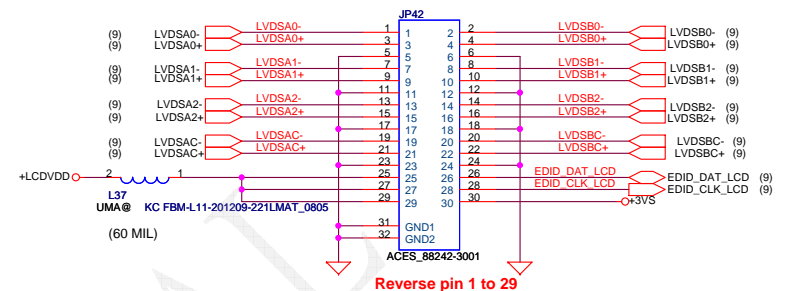
VGA I/O PORT Conn.**CRT Conn.**

Pop when with internal graphics

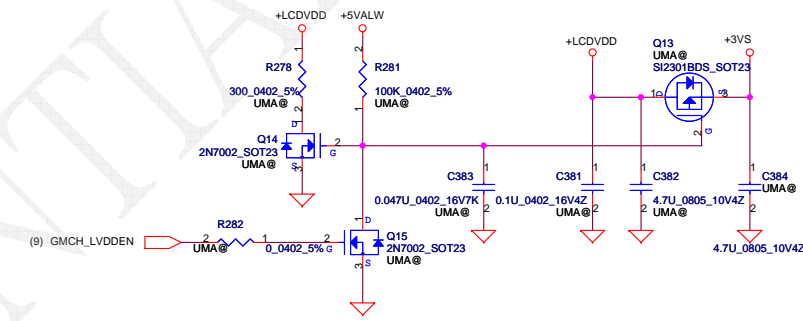
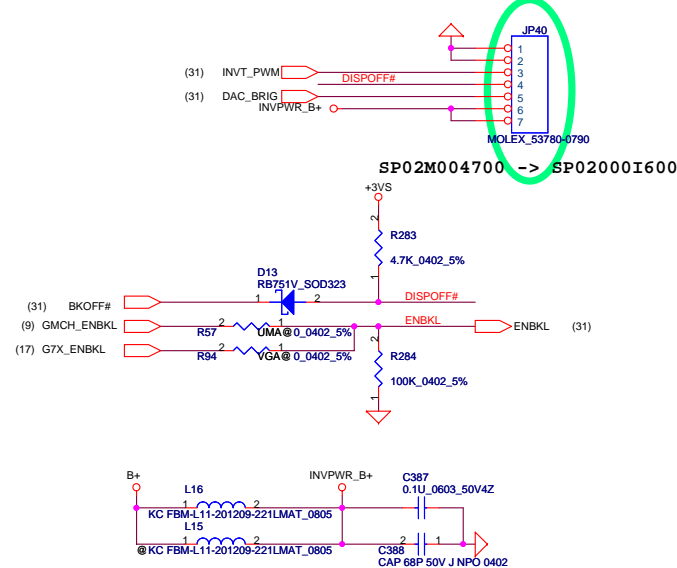


Pop when with internal graphics

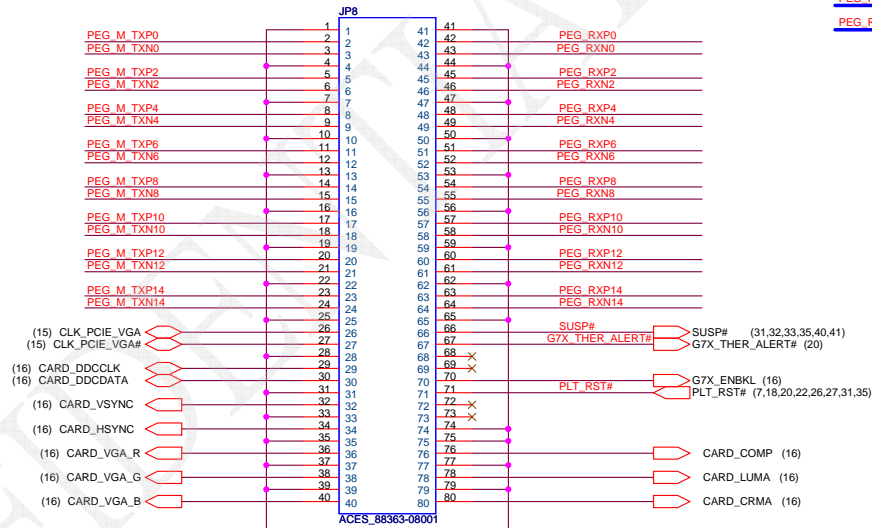
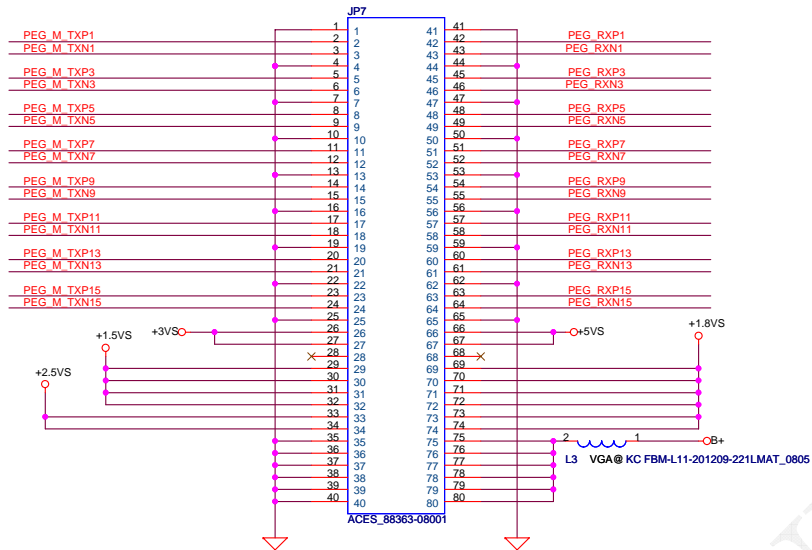
UMA LCD / PANEL Conn.



Reverse pin 1 to 29

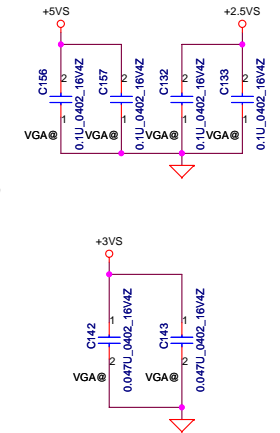
**INVERTER Conn.**

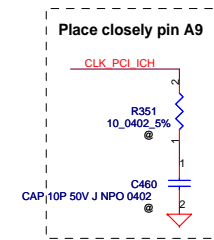
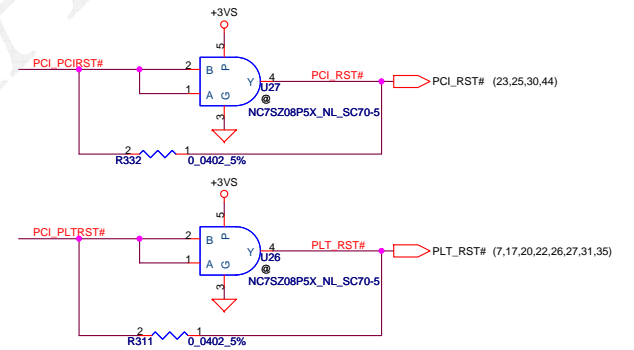
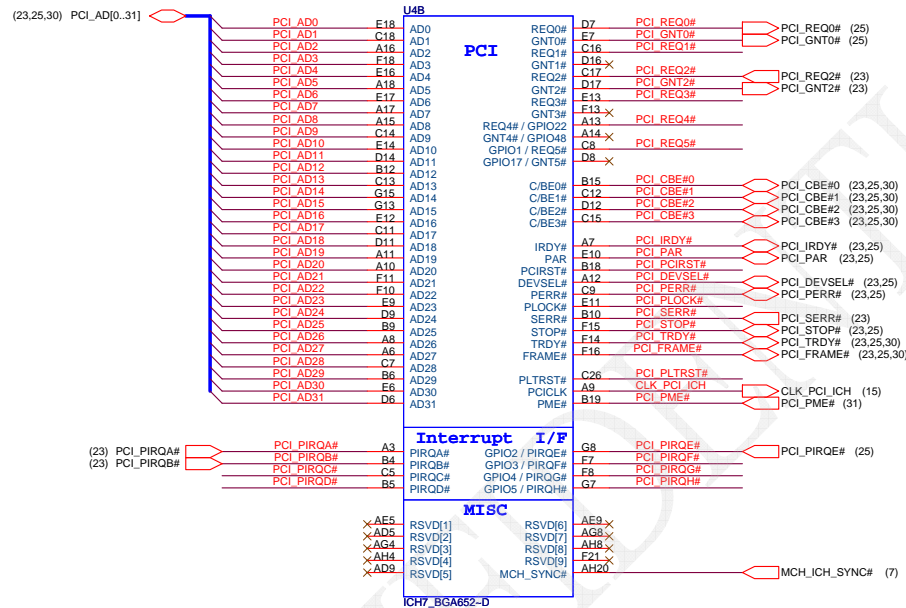
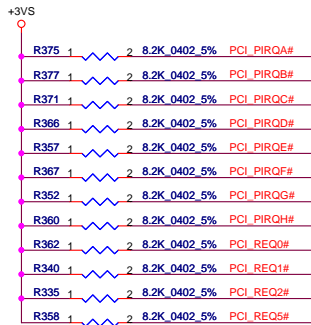
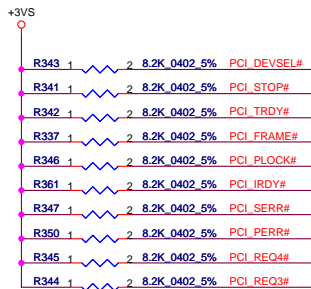
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				Date:	Wednesday, January 03, 2007
				Sheet	16 of 45

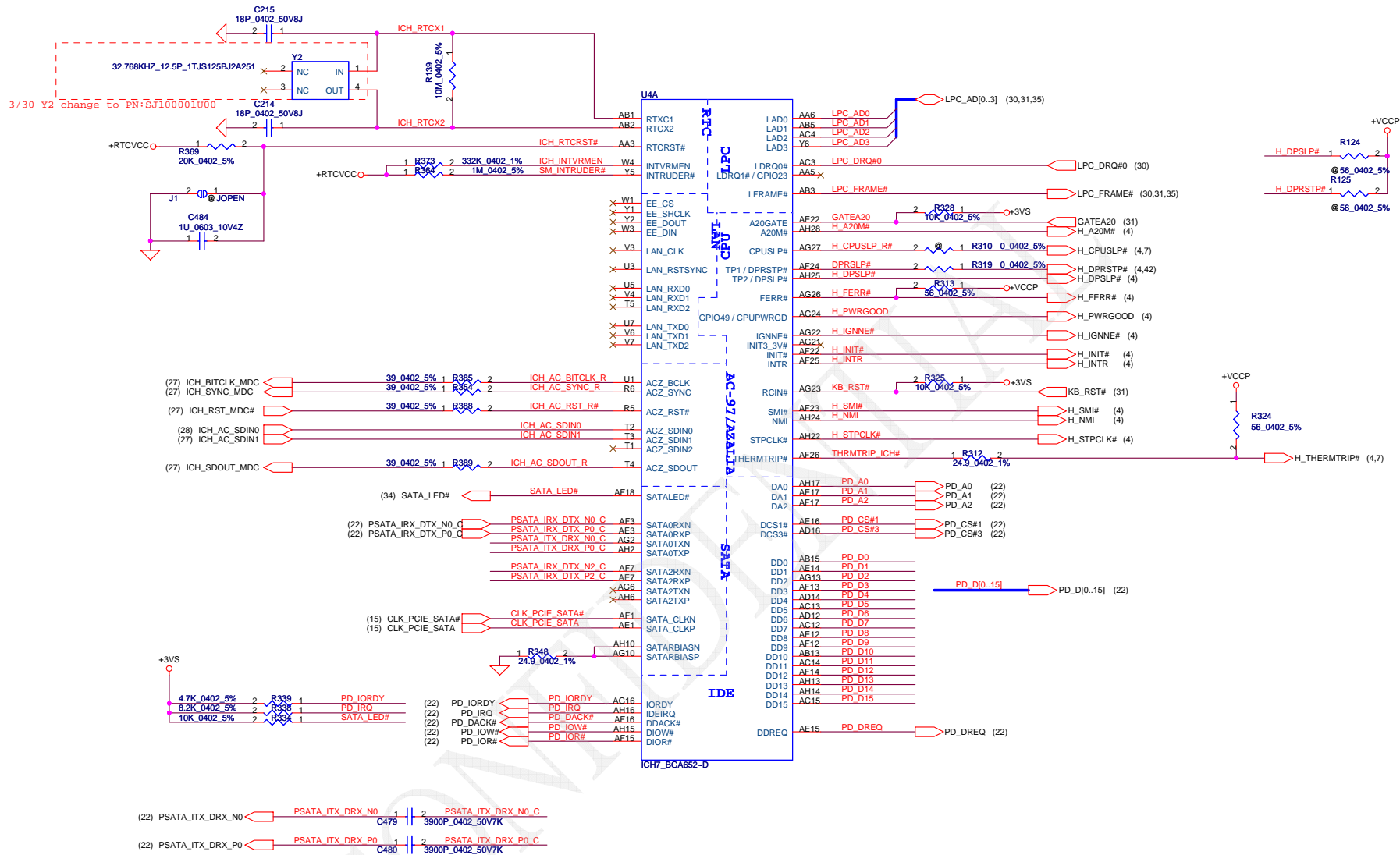


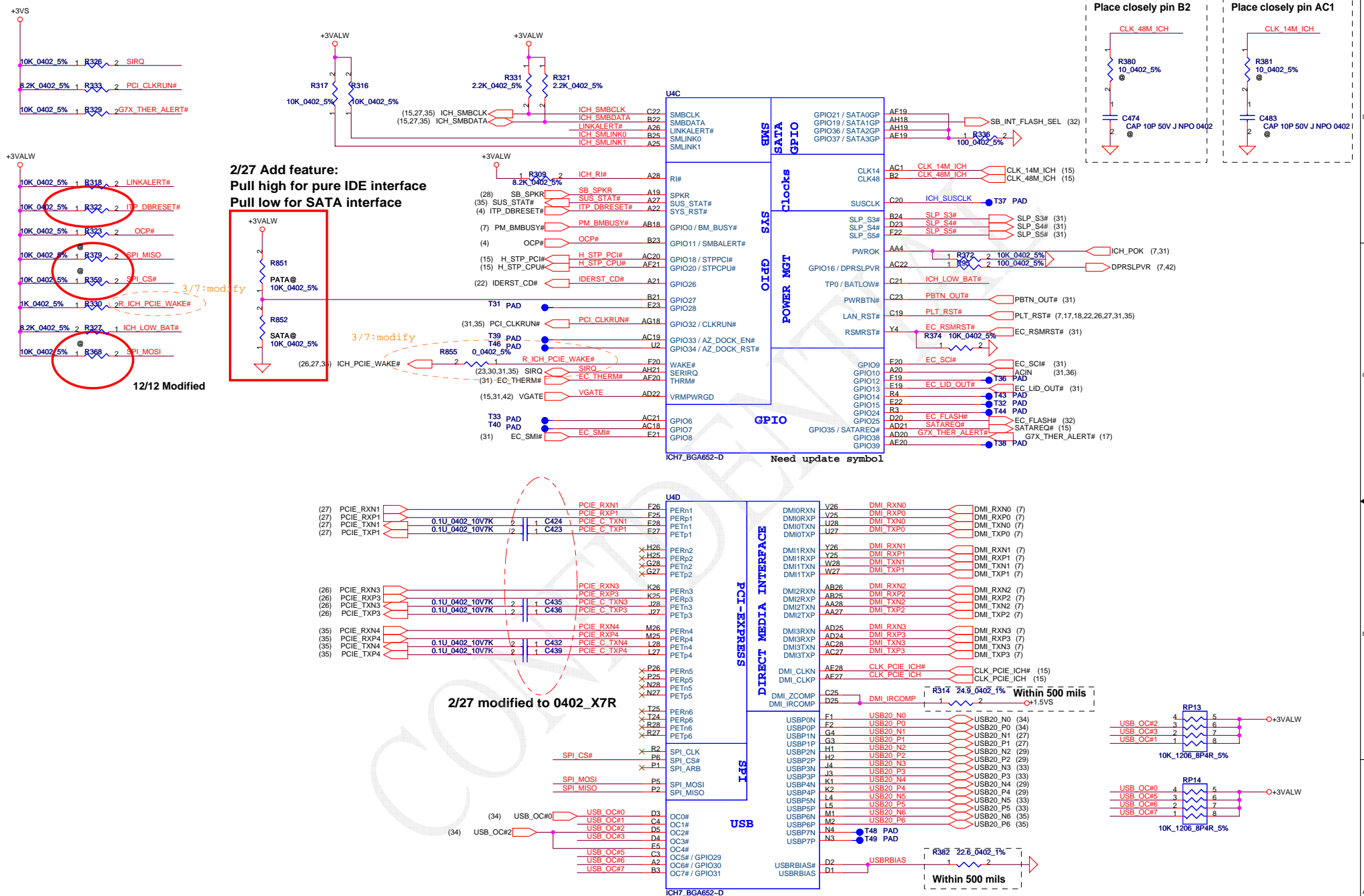
MAX. 4.06A @ 1.8V
MAX. 130mA @ 2.5V
MAX. 655mA @ 3.3V

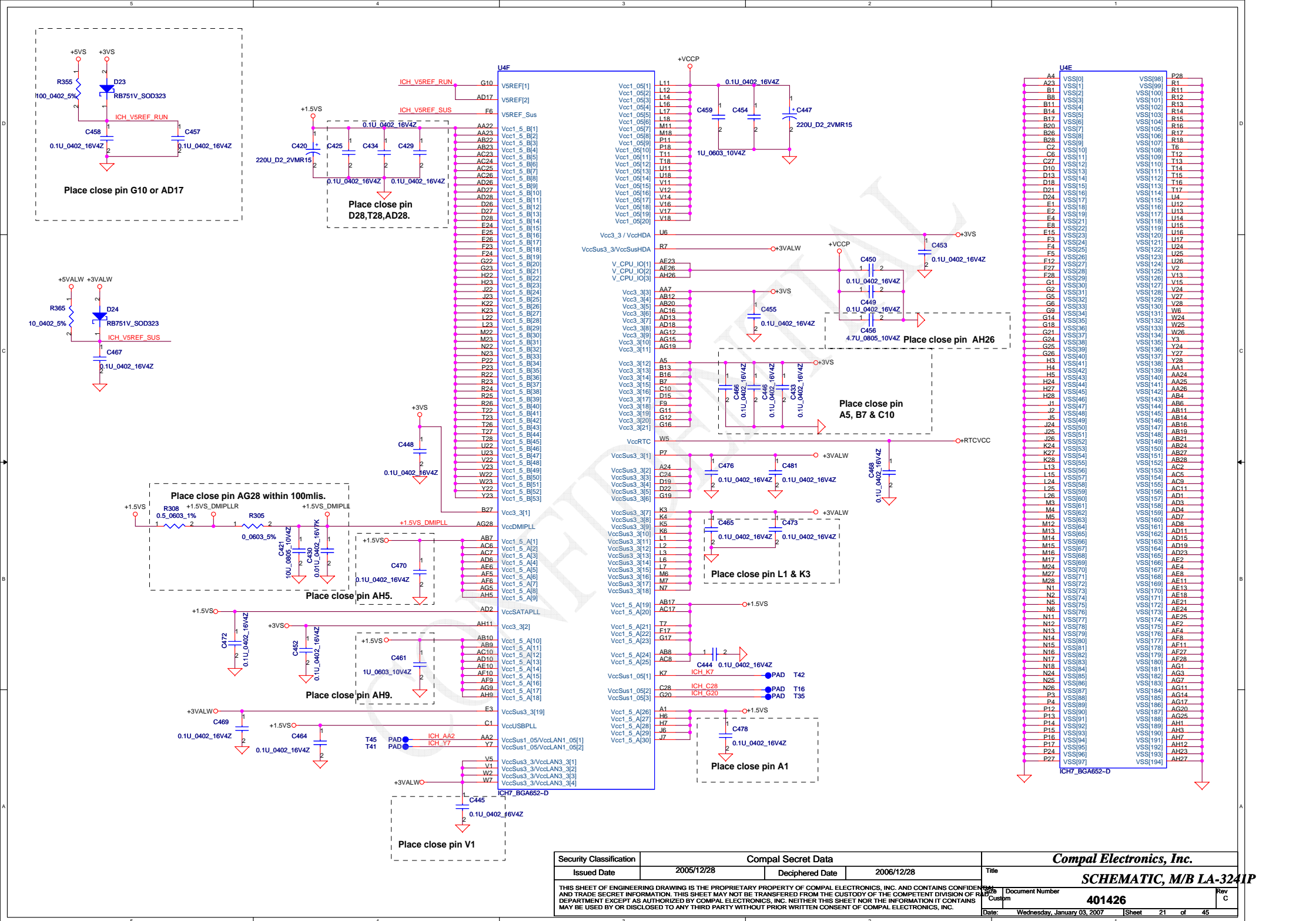
PEG_M_TXP[0..15] PEG_M_TXP[0..15] (9)
PEG_M_TXN[0..15] PEG_M_TXN[0..15] (9)
PEG_RXP[0..15] PEG_RXP[0..15] (9)
PEG_RXN[0..15] PEG_RXN[0..15] (9)





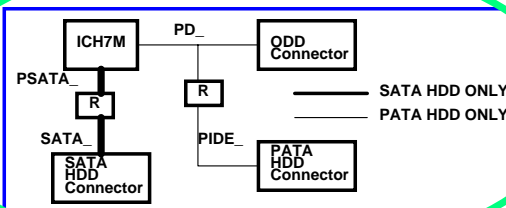
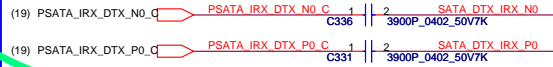




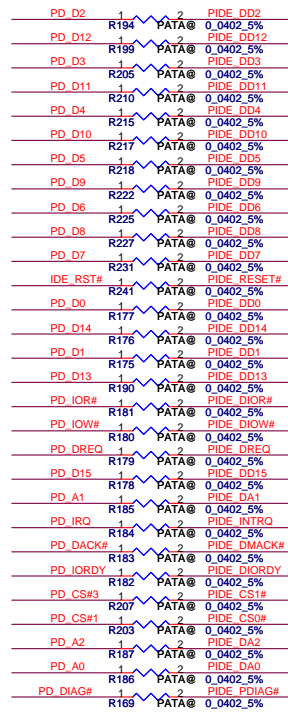
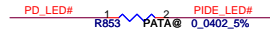


Place closed to 3811
2005/09/04

01/18 : Remove RP15,RP16



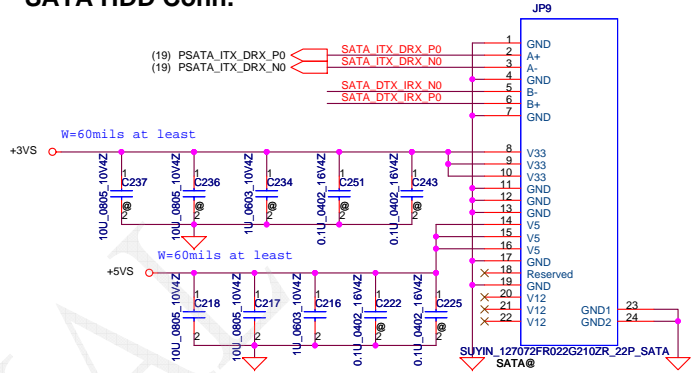
01/17 : Remove SATA to PATA Route



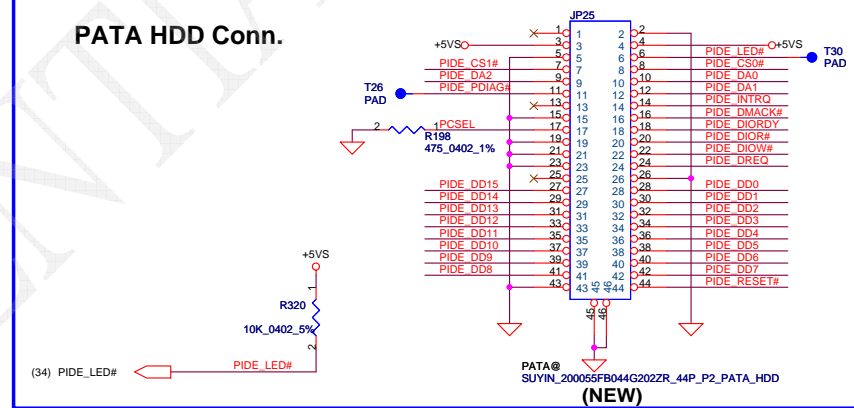
SATA HDD Conn.

2005/11/4 Modified library pn:DC010003J00

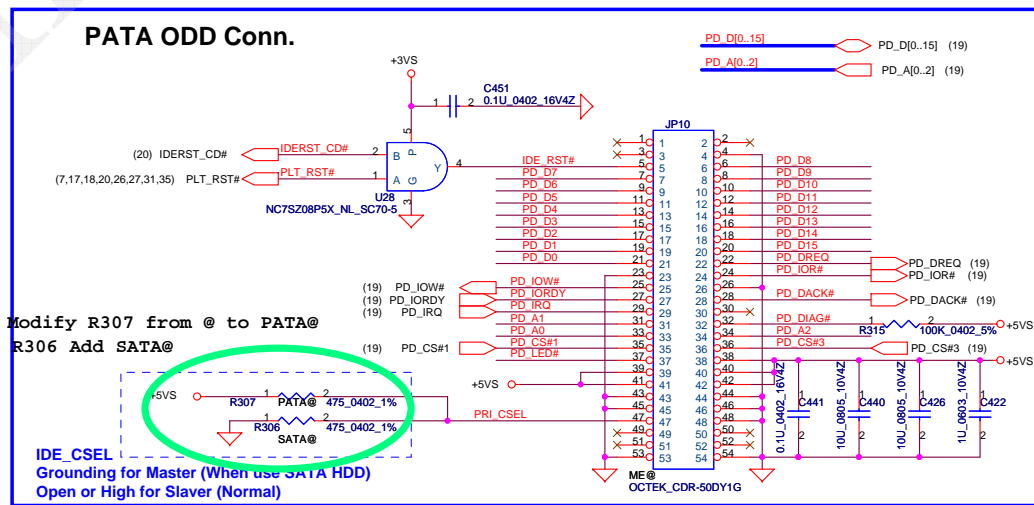
Main SATA +5V Default



PATA HDD Conn.



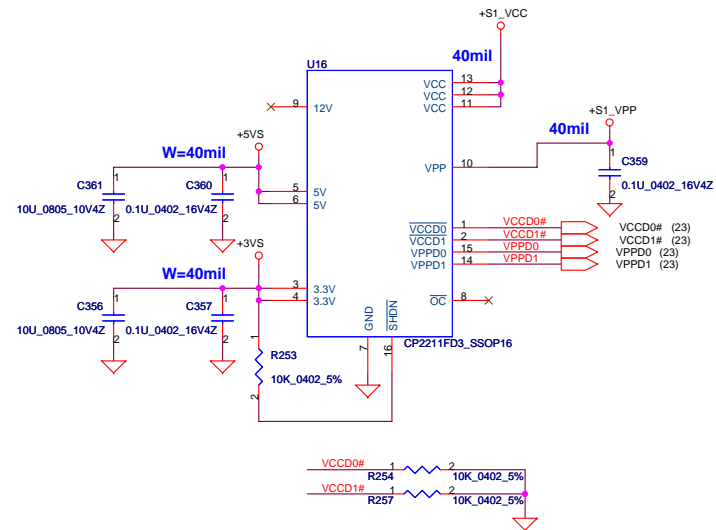
PATA ODD Conn.



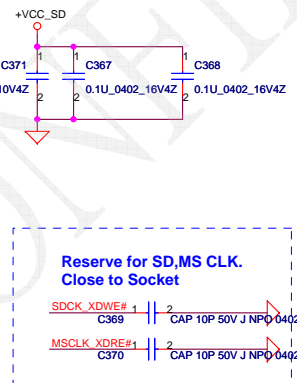
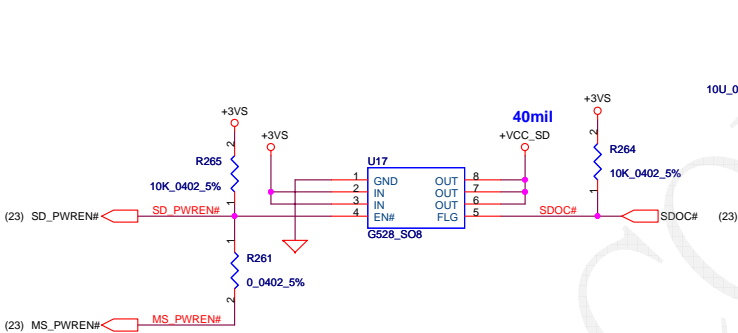
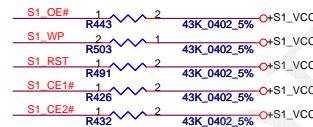
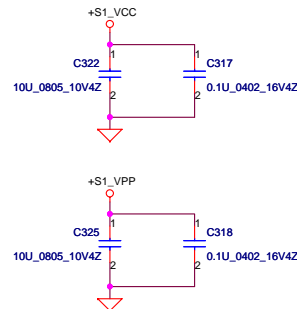
01/17 : Modify R307 from @ to PATA@
R306 Add SATA@

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Date: Wednesday, January 03, 2007				Sheet	22 of 45

PCMCIA Power Control



(23) S1_A[0..25] S1_A[0..25]
(23) S1_D[0..15] S1_D[0..15]

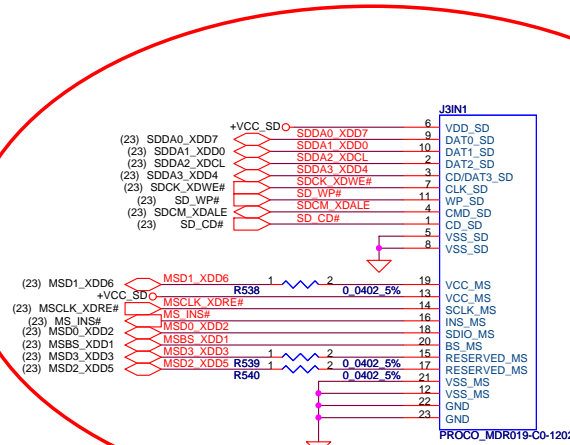
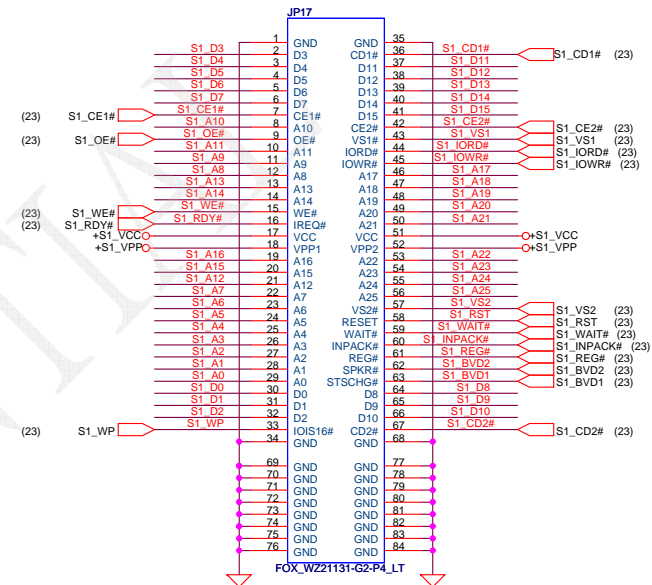


PCMCIA Socket

Note : 11/10 modify library to meet spec

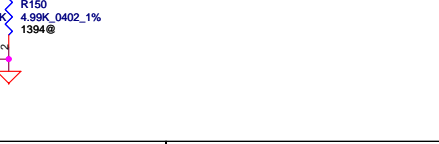
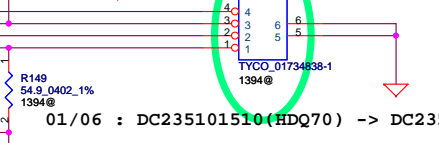
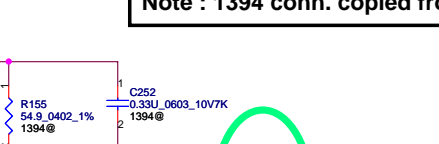
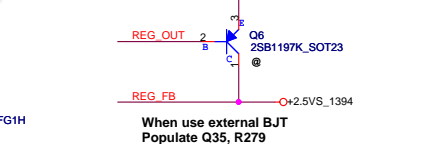
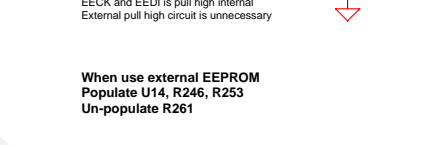
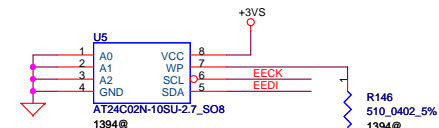
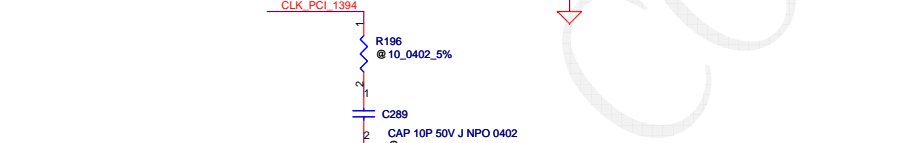
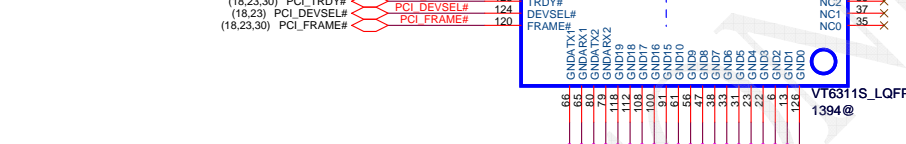
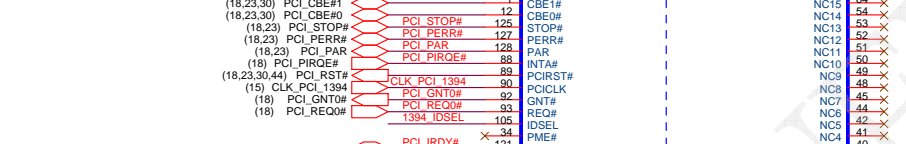
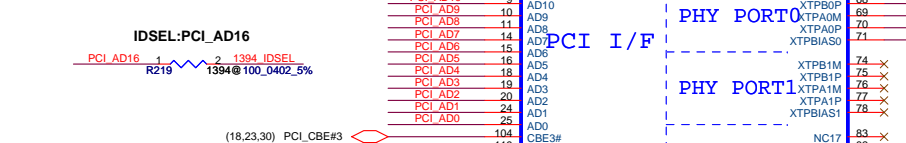
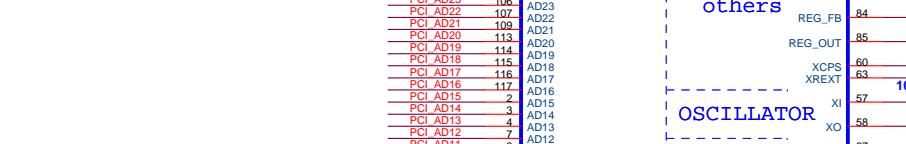
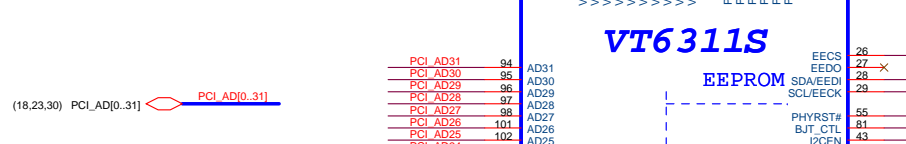
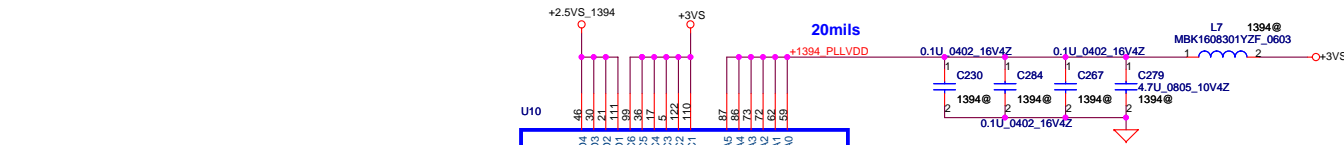
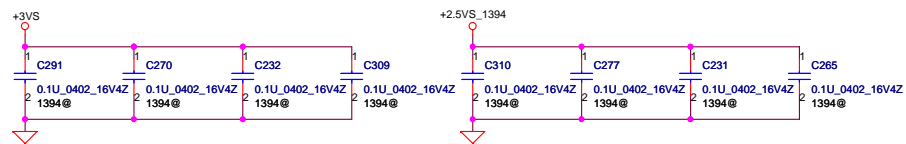
pn: SP01000IC00

11/14 modify footprint to FOX_1CA41521-TC2-4F_68P_LT



12/20 modified

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								Date:		Wednesday, January 03, 2007		Sheet 24 of 45	



Note : This page copied from HBL50

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				401426	C
				Date: Wednesday, January 03, 2007	Sheet 25 of 45

Note : 1394 conn. copied from HDL00

Note : 24.576M this crystal is non- lead free

01/06 : DC235101510(HDQ70) -> DC235000C00

2/27 modified to 0402_X7R

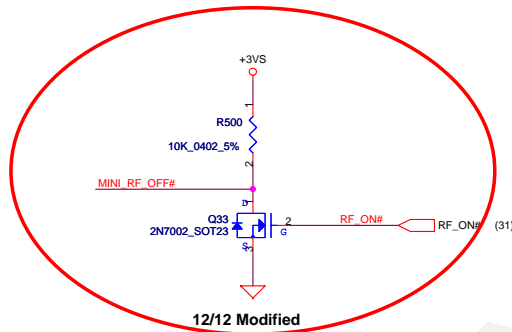
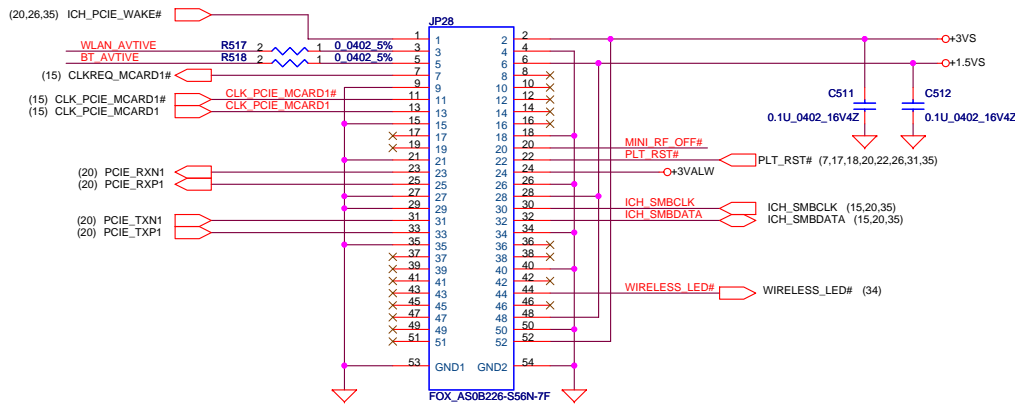


01/06 : DC234103600(HAZ00) -> DC234001A00

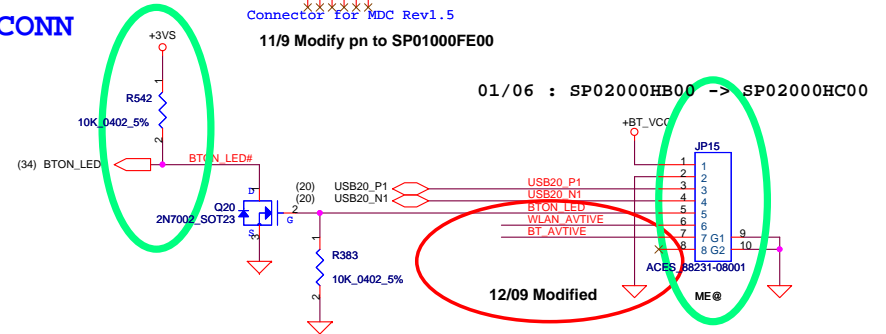
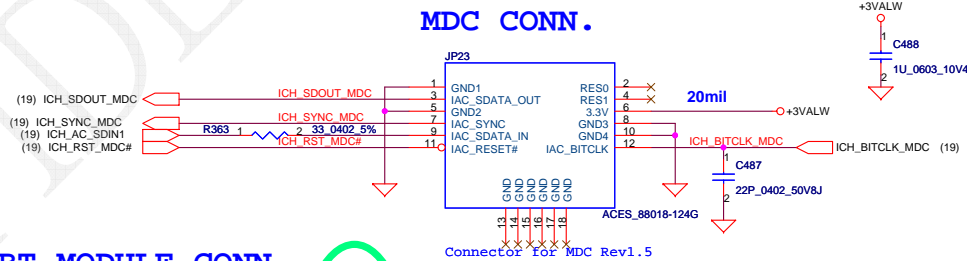
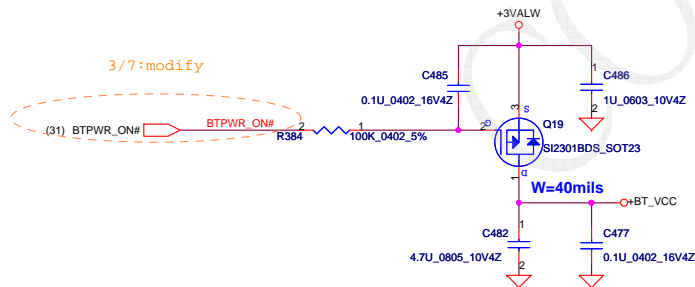


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				Date	Wednesday, January 03, 2007	Sheet 26 of 45

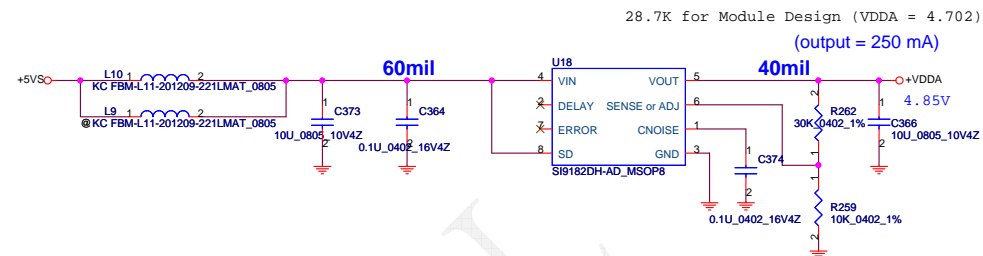
Mini-Express Card(Slot 1-WLAN)



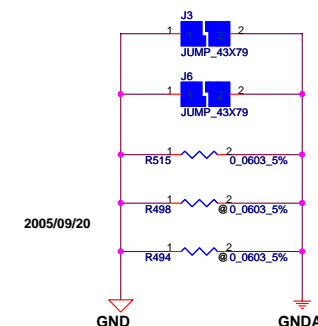
BT MODULE CONN



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						Doc Number		401426		Rev C	
						Date:		Wednesday, January 03, 2007		Sheet 27 of 45	



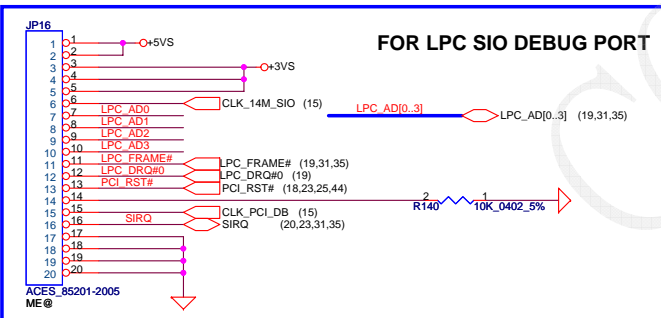
For EMI



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				Rev	C
Date:		Wednesday, January 03, 2007		Sheet	28 of 45

[illegible]

2005/12/21 Modified footprint : ACES_88502-2501_25P



FOR PORT 80 DEBUG PORT

Pin	Signal	Signal	Signal
20	PCI_CBE#0	PCI_CBE#0	(18,23,25)
19	PCI_AD6	PCI_AD6	(18,23,25)
18	PCI_AD5	PCI_AD5	(18,23,25)
17	PCI_AD4	PCI_AD4	(18,23,25)
16	PCI_AD3	PCI_AD3	(18,23,25)
15	PCI_AD2	PCI_AD2	(18,23,25)
14	PCI_AD1	PCI_AD1	(18,23,25)
13	PCI_AD0	PCI_AD0	(18,23,25)
12	PCI_AD0	PCI_AD0	(18,23,25)
11	PCI_AD0	PCI_AD0	(18,23,25)
10	PCI_CBE#1	PCI_CBE#1	(18,23,25)
9	PCI_CBE#2	PCI_CBE#2	(18,23,25)
8	PCI_CBE#3	PCI_CBE#3	(18,23,25)
7			
6			
5			
4			
3			
2			
1	PCI_AD9	PCI_AD9	(18,23,25)

ACES_85201-2005
ME@

EC DEBUG PORT

(31) EC_TX

+5VALW

JP26

1

2

3

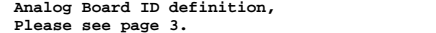
4

EC_TX

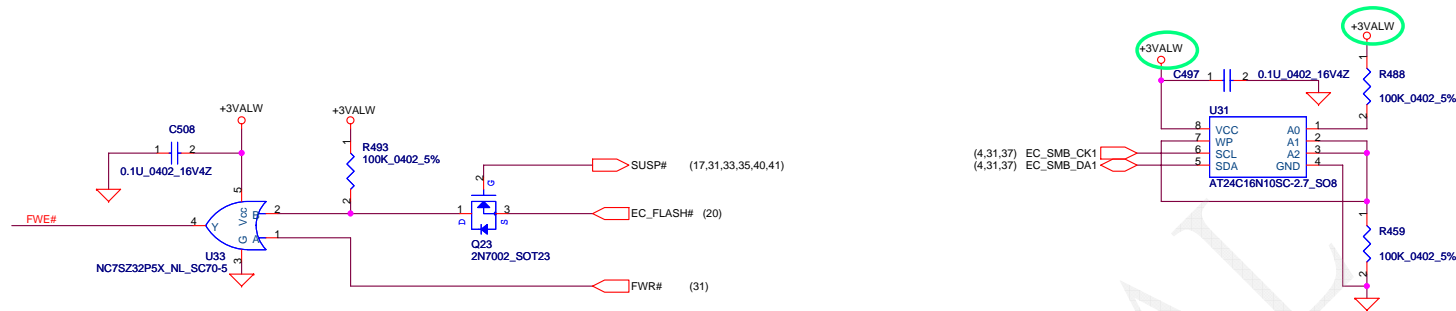
ACES_85205-0400

ME@

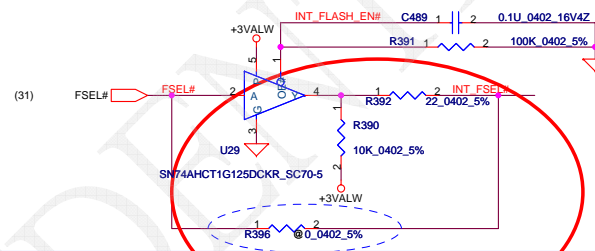
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						Date:		Wednesday, January 03, 2007	
						Sheet		30 of 45	
						Rev		C	



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Doc No	Document Number	Rev	C
Customer	401426		
Date:	Wednesday, January 03, 2007	Sheet	31 of 45



FOR DEBUG ONLY

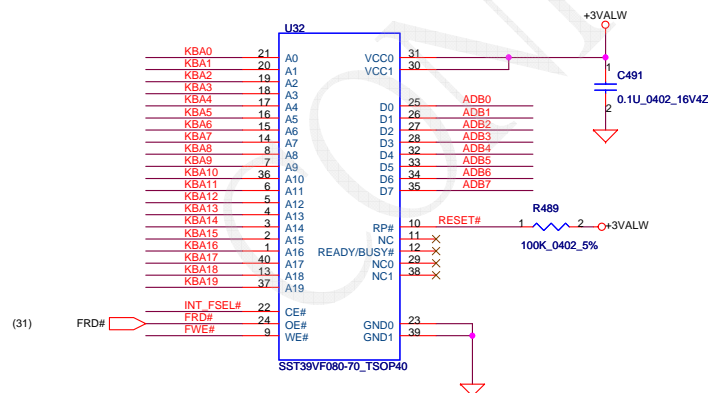


12/9 Modified BOM Structure

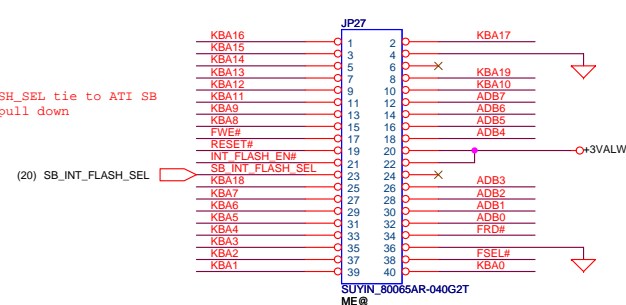
(31) KBA[0..19] KBA[0..19]

(31) ADB[0..7] ADB[0..7]

1MB Flash ROM



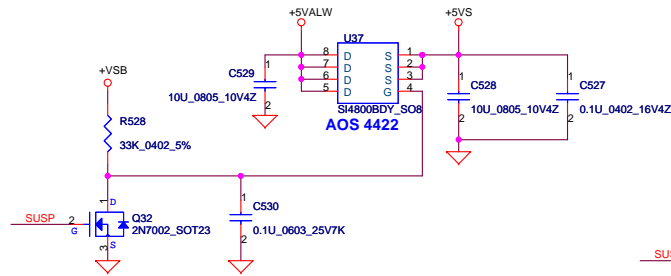
1MB ROM Socket



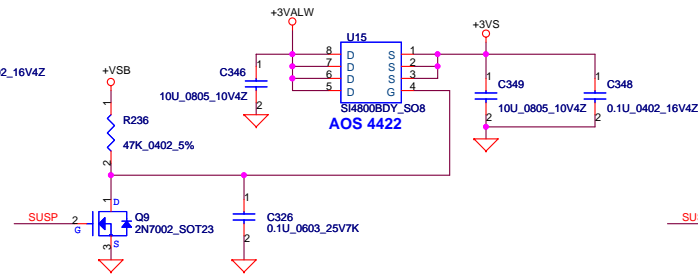
Not Lead Free

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				Date	Wednesday, January 03, 2007
				Sheet	32 of 45

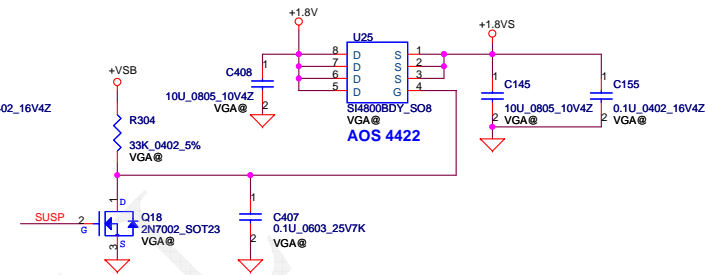
+5VALW to +5VS Transfer



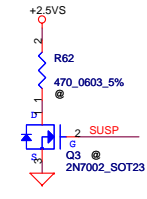
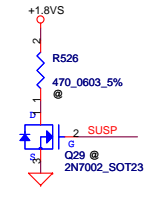
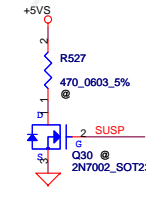
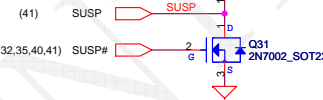
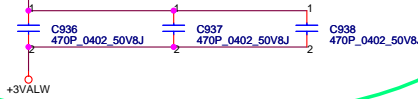
+3VALW to +3VS Transfer



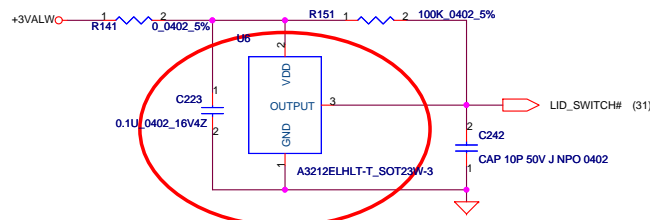
+1.8V to +1.8VS Transfer



For PCI BUS
For EMI

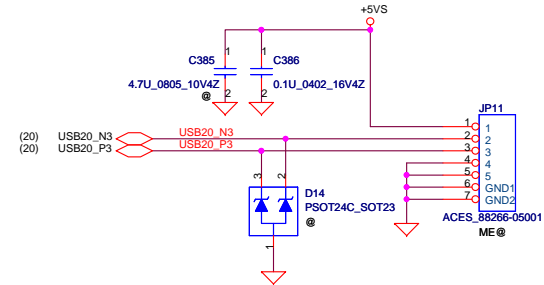


LID Switch

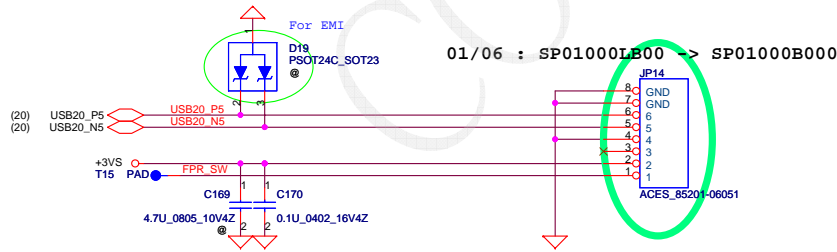


12/9 Change to SA032120010

CMOS Camera Conn

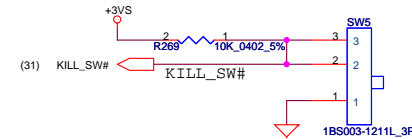


Finger Print board + MP3 Module CONN.



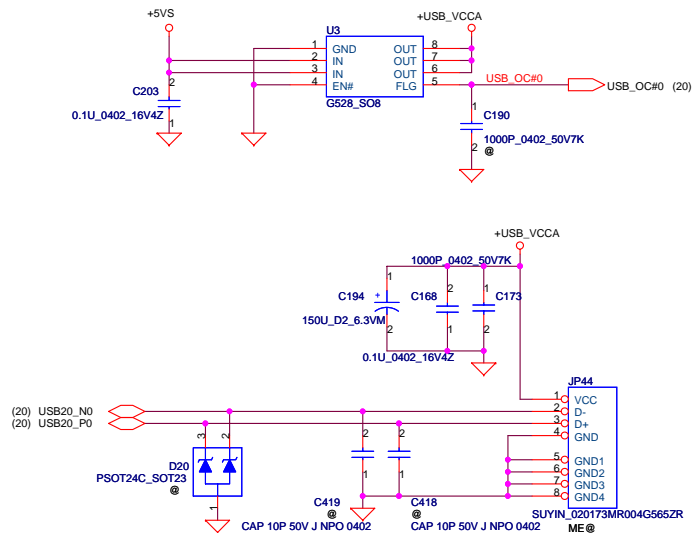
ACES

Kill Switch

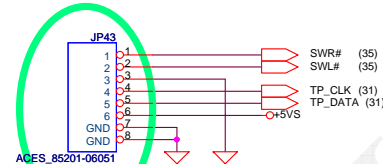


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Date: Wednesday, January 03, 2007				Sheet	33 of 45

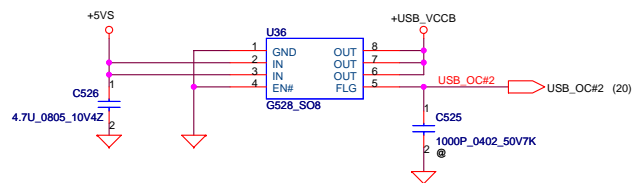
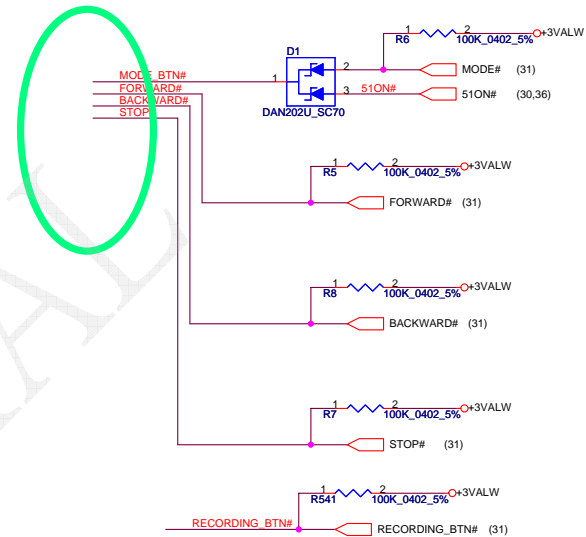
USB Port



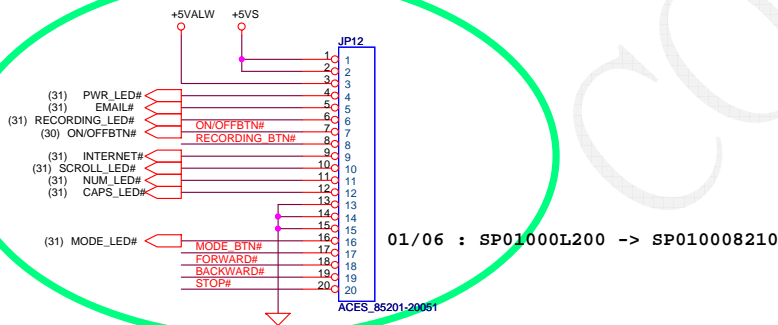
T/P Board



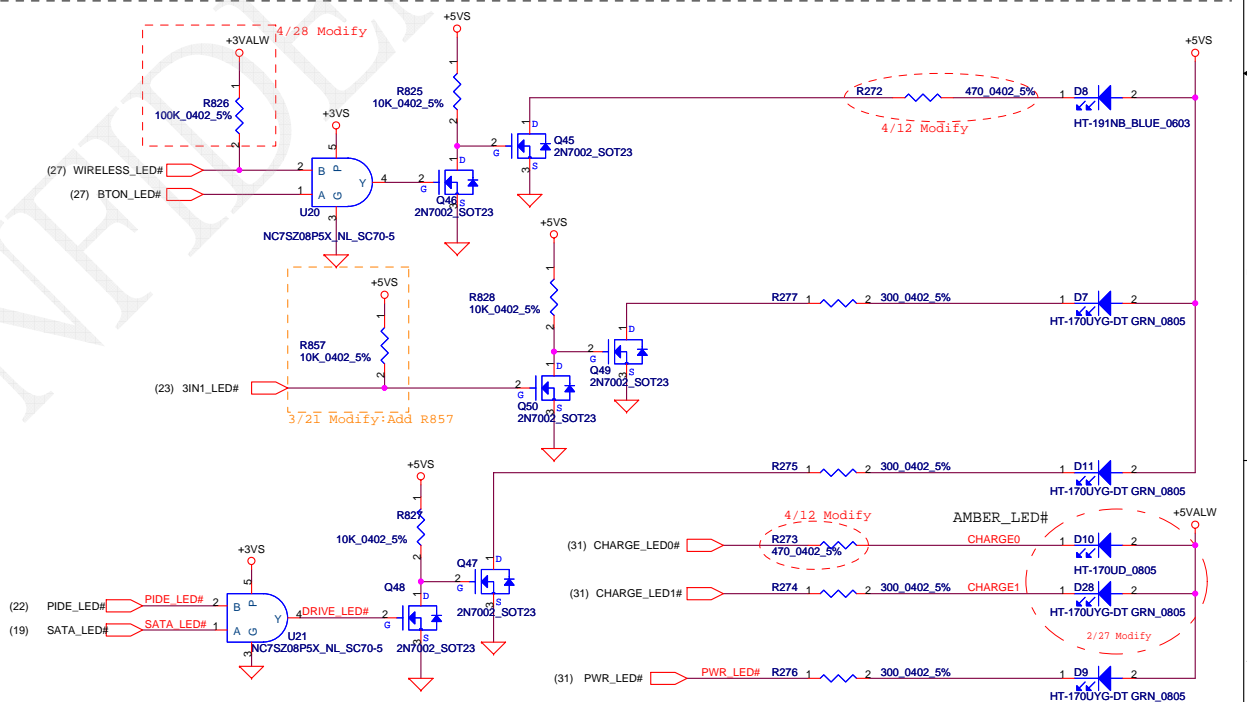
01/06 : SP01000LB00 -> SP01000B000



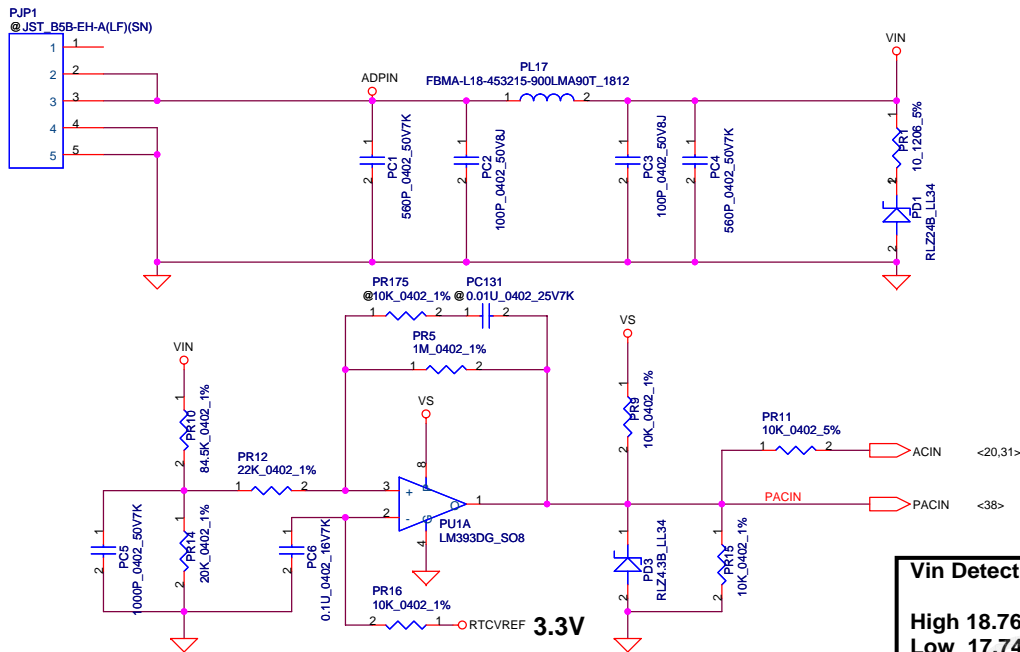
Switch Board CONN.



01/06 : SP01000L200 -> SP010008210



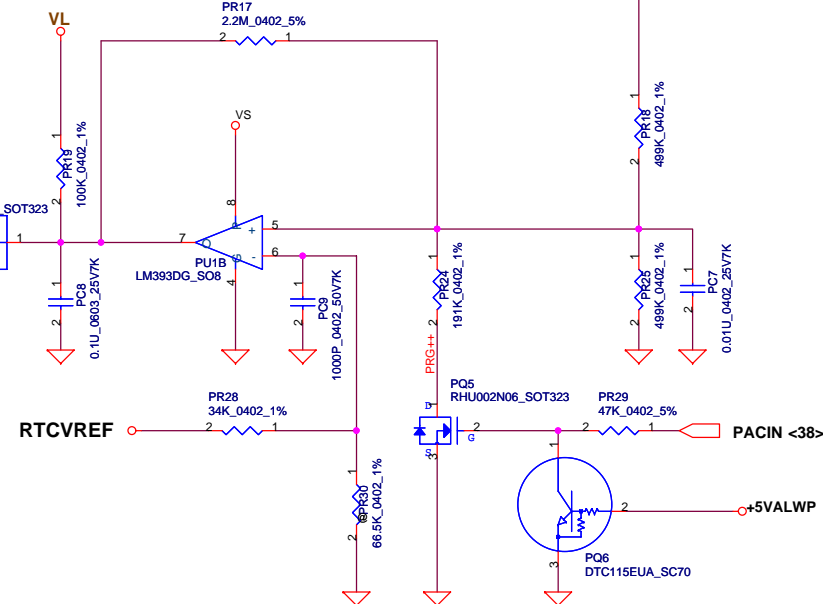
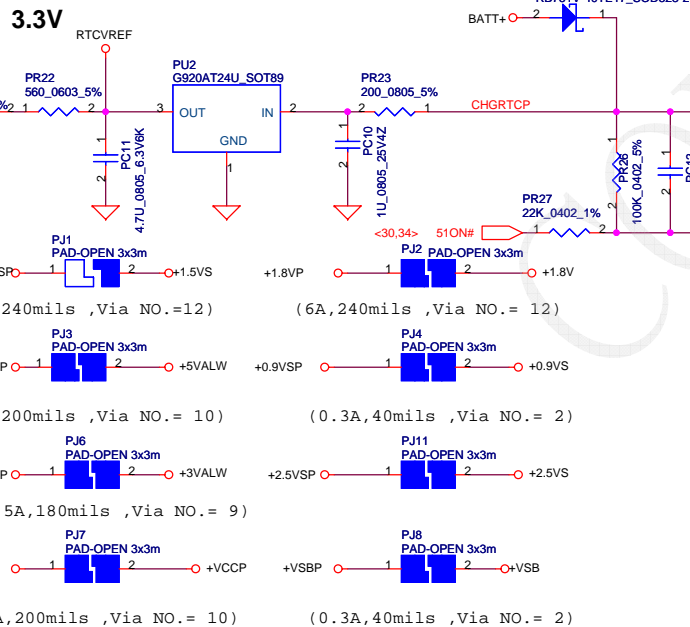
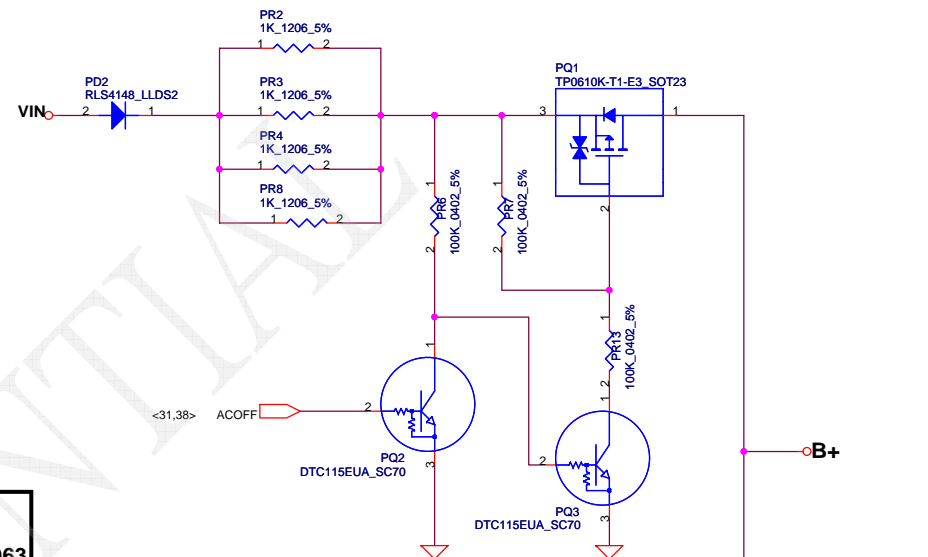
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		401426		C	
Date:		Wednesday, January 03, 2007		Sheet 34 of 45	



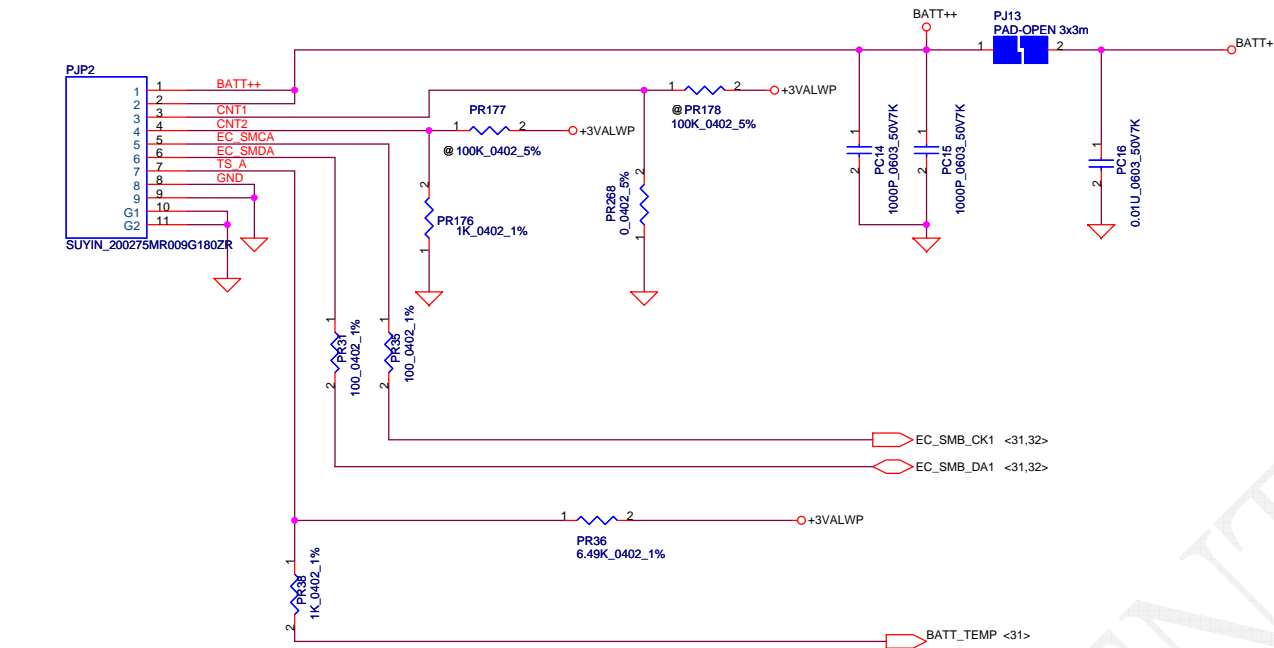
Vin Detector			
High	18.764	17.901	17.063
Low	17.745	16.9	16.03

ACIN			
Precharge detector			
	Min.	typ.	Max
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

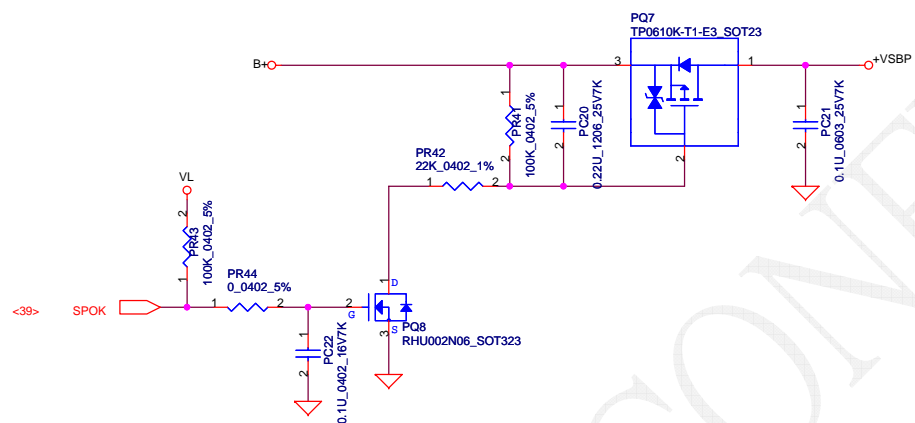
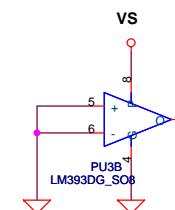
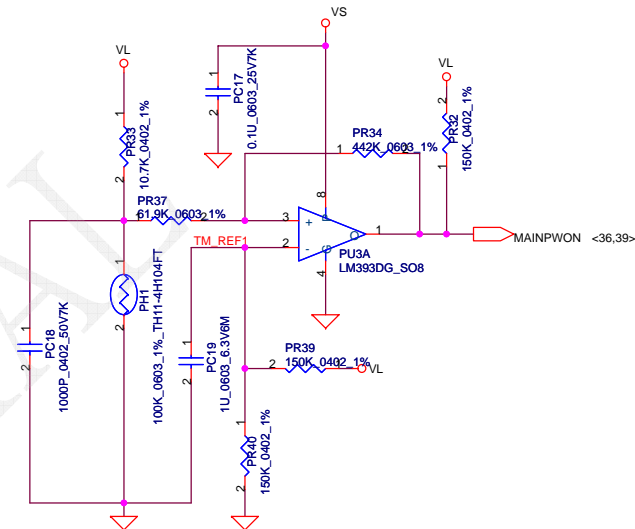
BATT ONLY			
Precharge detector			
	Min.	typ.	Max
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V



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				401426	C
				Date: Wednesday, January 03, 2007	Sheet 36 of 45



PH1 under CPU botten side :
CPU thermal protection at 85 degree C
Recovery at 70 degree C

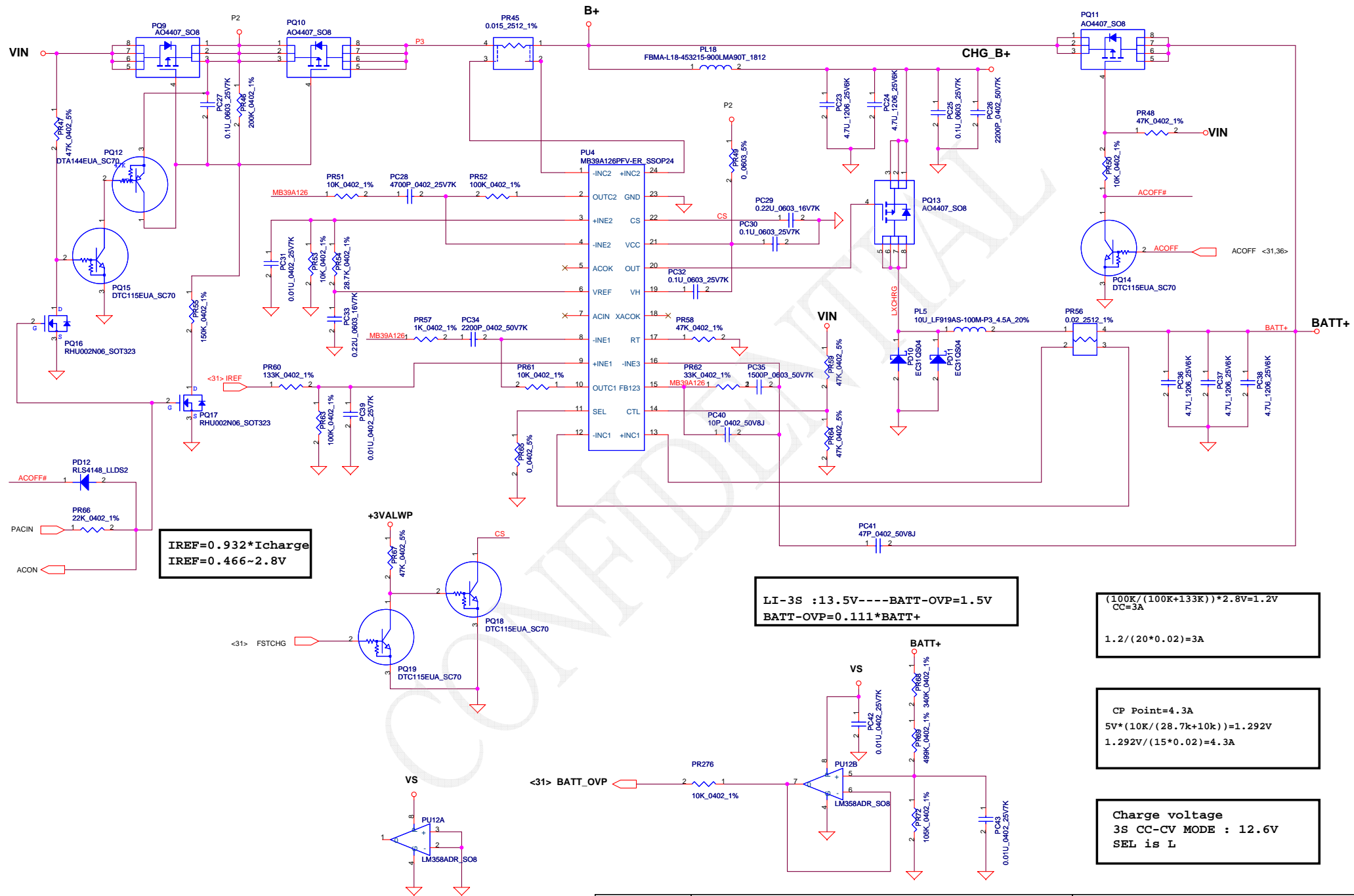


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Size B	Document Number	401426			Date: Wednesday, January 03, 2007
Sheet	37	of	45		

75W PR45=0.02_2512_1% PR54=23.7K_0402_1% Iadp=0~3.71A
90W PR45=0.15_2512_1% PR54=28.7K_0402_1% Iadp=0~4.3A

Fosc=14100/Rt=14100/47=300KHz

Charger



IREF=0.932*Icharge
IREF=0.466~2.8V

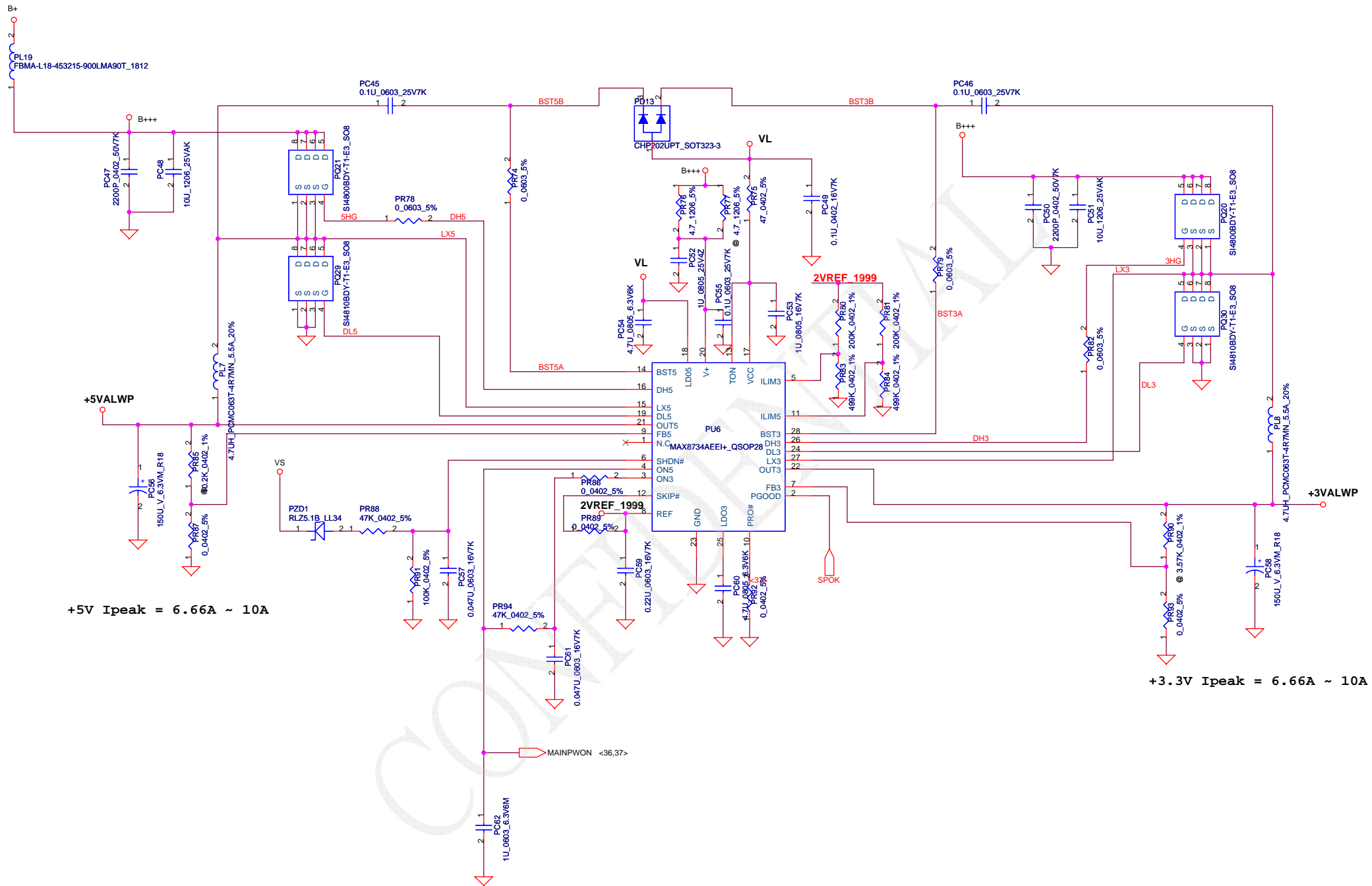
LI-3S :13.5V----BATT-OVP=1.5V
BATT-OVP=0.111*BATT+

$(100K/(100K+133K))*2.8V=1.2V$
CC=3A
 $1.2/(20*0.02)=3A$

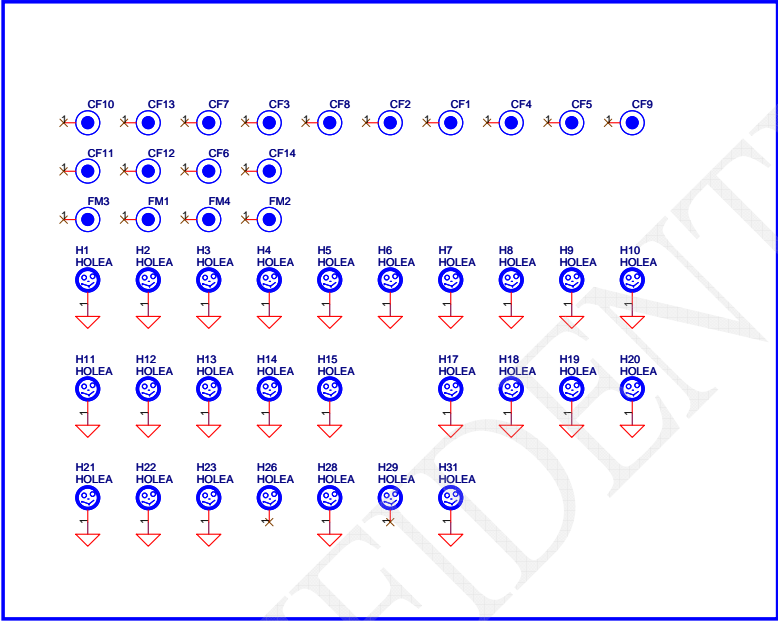
CP Point=4.3A
 $5V*(10K/(28.7k+10k))=1.292V$
 $1.292V/(15*0.02)=4.3A$

Charge voltage
3S CC-CV MODE : 12.6V
SEL is L

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				401426	C
				Date: Wednesday, January 03, 2007	Sheet 38 of 45



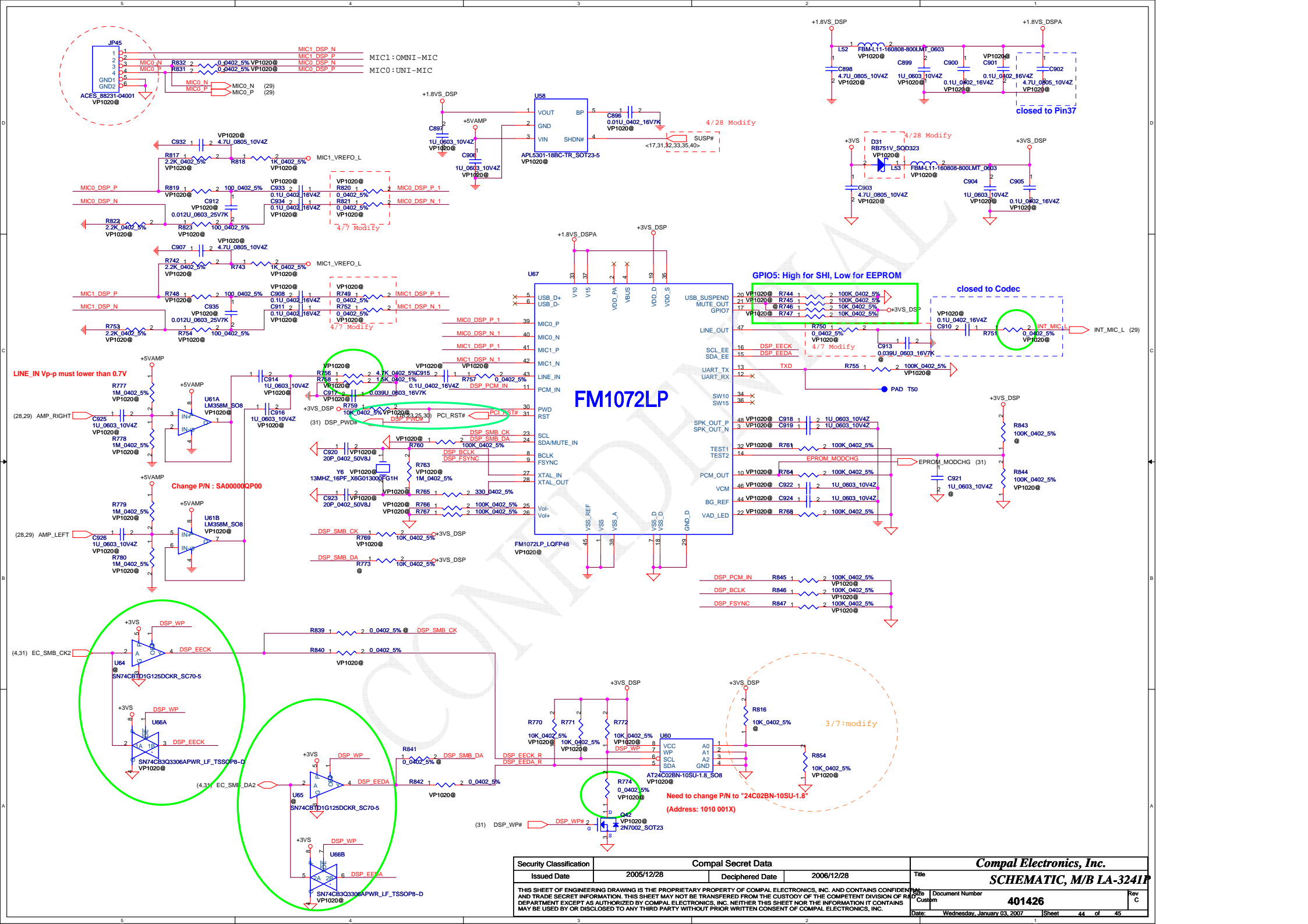
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				Document Number	401426
				Rev	C
				Date:	Wednesday, January 03, 2007
				Sheet	39 of 45



01/19 : Modify

H8----->H_S315D118
H17.H22.H23----->H_C315D146
H10----->H_S315D146

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Date: Wednesday, January 03, 2007				Sheet	43 of 45



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				Rev	C
				Date	Wednesday, January 03, 2007
				Sheet	44 of 45

DVT

page	Reason for change	Modify list
42	Vss_ sense feedback	PC174 change 1000P to 4700p
42	Vcc_ sense resistance	PR235 change 100 ohm to 0 ohm
42	load line	PR242 change 3.65K ohm to 4.22K
42	Vcc_ sense resistance (H.W. had pull-high)	Delete PR229
36	Prevent PACIN Low	PR11 change 0 ohm to 10K ohm
42	Heavy load unstable	change PQ33,PQ34,PQ36,PQ37 from AO4410 to IRF8113

PVT

page	Reason for change	Modify list
36	Battery and Adapter in sequence	PD4 Pin2 voltage change VS to VIN
38	Battery and Adapter in sequence	Add PR276 between PU12 pin 7 and BATT_OVP.
42	For EMI	Change High side gate resister 0ohm to 2.2ohm
42	For EMI	Change boost resister 2.2ohm to 0ohm
38	Delete sunbber for EMI	Delete PR256_4.7ohm,PR224_4.7ohm, PC182_680pf,PC167_680pf
38	Reduce delay time for EC	Delete PR175_10K, PC131_0.01uF

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		401426		Rev C	
Date:		Wednesday, January 03, 2007		Sheet 45 of 45	