JE40 HR
DIS/UMA/Muxless Schematics Document
Sandy Bridge
Intel PCH

DY :None Installed
DIS:DIS installed
DIS_Muxless :BOTH DIS or Muxless installed
DIS_PX:BOTH DIS or PX installed
DIS_PX_Muxless:DIS or PX or Muxless installed.
Muxless: Muxless installed.(PX4.0)
PX:MUX installed.(PX3.0)
PX_Muxless:BOTH PX or Muxless installed.
UMA:UMA installed
UMA_Muxless:BOTH UMA or Muxless installed
UMA_PX_Muxless:UMA or PX or Muxless installed

ANNIE: ONLY FOR ANNIE solution.
PSL: KBC795 PSL circuit for 10mW solution installed.
10mW: External circuit for 10mW solution installed.
65W: for 65W adaptor installed.
90W: for 90W adaptor installed.

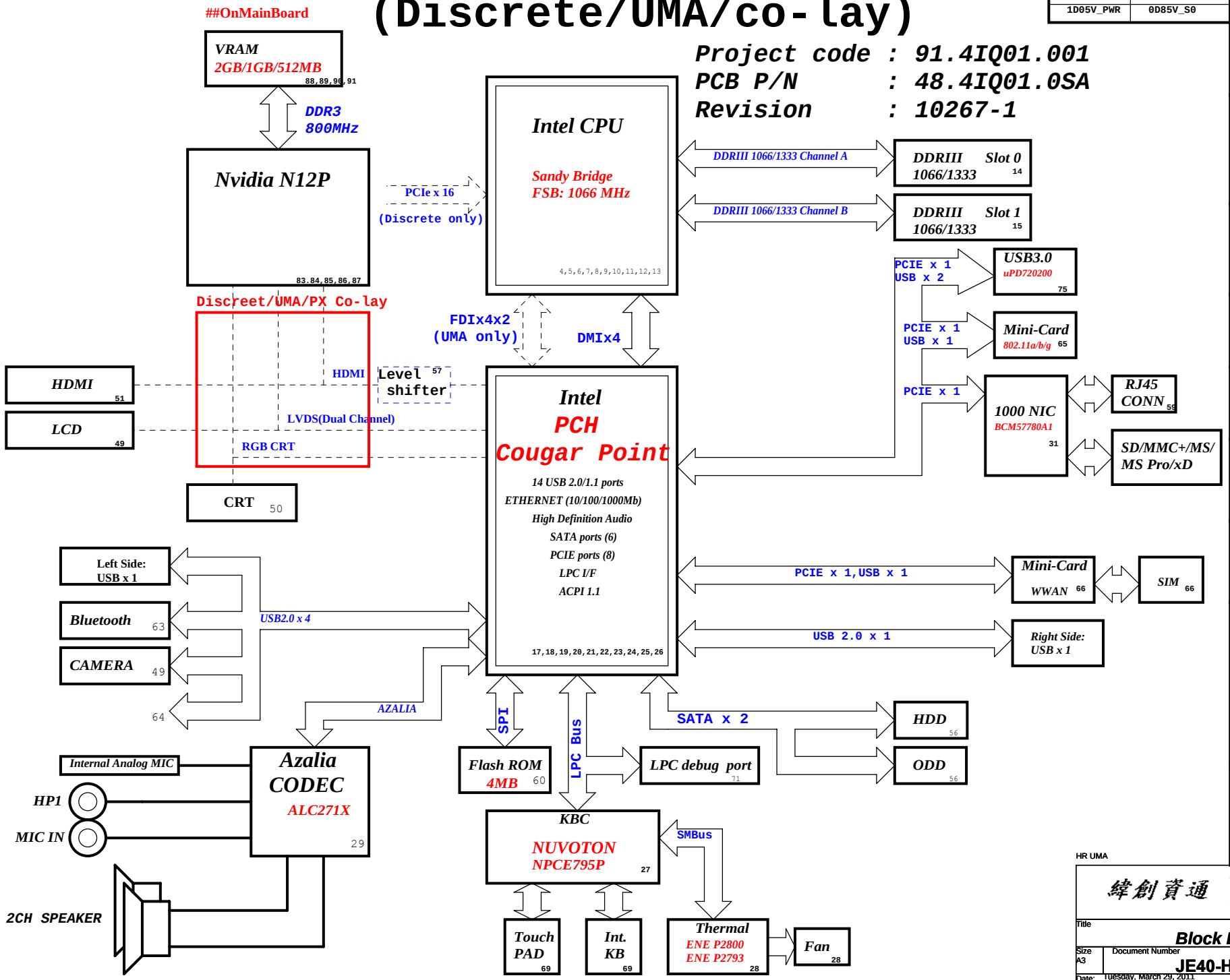
HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Cover Page	
Size A3	Document Number JE40-HR	Rev -1
Date: Tuesday, March 29, 2011	Sheet 1 of 102	

JE40 HR Block Diagram (Discrete/UMA/co-lay)

Project code : 91.4IQ01.001
PCB P/N : 48.4IQ01.0SA
Revision : 10267-1



SYSTEM DC/DC APL5916KAI 48	
INPUTS	OUTPUTS
1D05V_PWR	0D85V_S0

CPU DC/DC NCP6131S52MNR 42~43	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC UP6128PQDD 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC UP6183PQAG 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC UP6165BQKF 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

SYSTEM DC/DC NCP5911MNTBG 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE_PWR

VGA RT8208BGQW 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

TI CHARGER BQ24745RHDR 40	
INPUTS	OUTPUTS
DCBATOUT	BT+

SYSTEM DC/DC RT9025 47	
INPUTS	OUTPUTS
3D3V_S0	1D8V_S0

SYSTEM DC/DC RT9025-25PSP 93	
INPUTS	OUTPUTS
1D5V_S3	1V_VGA_S0
3D3V_S5	1D8V_VGA_S0

Switches	
INPUTS	OUTPUTS
1D5V_S3	1D5V_VGA_S0
3D3V_S0	3D3V_VGA_S0

PCB LAYER

L1:Top L4:Signal
L2:VCC L5:GND
L3:Signal L6:Bottom

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram

Size: A3 | Document Number: JE40-HR | Rev: -1

Date: Tuesday, March 29, 2011 | Sheet 2 of 102

PCH Strapping

Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	1

Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Mini Card1(WLAN)
LANE3	Card Reader
LANE4	Onboard LAN
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA	
Pair	Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

SMBus ADDRESSES

I² C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address Hex	Bus
EC SMBus 1 Battery CHARGER			BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP			SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI			PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Table of Content

Size: A3 | Document Number: JE40-HR | Rev: -1

Date: Tuesday, March 29, 2011 | Sheet 3 of 102

SSID = CPU

CPU1A
SANDY
62.10055.421
Change:62.10053.611
2nd = 62.10055.321
3rd = 62.10040.821

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect

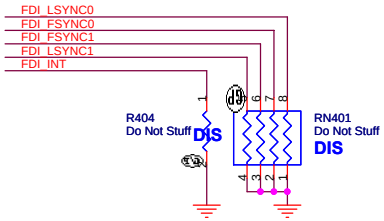
PEG Static Lane Reversal

JE40 delete eDP function

20100614 V1.1

NOTE:
Select a Fast FET similar to 2N7002E whose rise/fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.

Stuff to disable internal graphics function for power saving.



HR UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCIE/DMI/FDI)
Size: A3
Document Number: JE40-HR
Rev: -1
Date: Tuesday, March 29, 2011
Sheet 4 of 102

SSID = CPU

CPU1B
SANDY

2 OF 9

SANDY

MISC

18 H_SNB_IVB# — C26 — SNB_IVB#

JE40 modify — AN34 — SKTOCC#

THERMAL

JE40 modify — AL33 — CATERR#

22,27 H_PECI — AN33 — PECI

27,42 H_PROCHOT# — R513 56R2J-4-GP — H_PROCHOT# R — AL32 — PROCHOT#

22,36 H_THERMTRIP# — AN32 — THERMTRIP#

PWR MANAGEMENT

19 H_PM_SYNC — AM34 — PM_SYNC

R503 10KR2J-3-GP

22,36,97 H_CPUPWRGD — AP33 — UNCOREPWRGOOD

-2M DY

37 VDDPWRGOOD — V8 — SM_DRAMPWROK

BUF_CPU_RST# — AR33 — RESET#

CLOCKS

BCLK — A28 — CLK_EXP_P 20
BCLK# — A27 — CLK_EXP_N 20

DPLL_REF_SSCLK — A16 — CLK_DP_P_R
DPLL_REF_SSCLK# — A15 — CLK_DP_N_R

RN502
Do Not Stuff
DIS

JE40 modify — 1D05V_VTT

DDR3 MISC

SM_DRAMRST# — R8 — R502 4K99R2F-L-GP — SM_DRAMRST# 37

SM_RCOMP0 — AK1 — SM_RCOMP_0 R506 — 140R2F-GP
SM_RCOMP1 — A5 — SM_RCOMP_1 R507 — 25D5R2F-GP
SM_RCOMP2 — A4 — SM_RCOMP_2 R508 — 200R2F-L-GP

Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.

JTAG & BPM

PRDY# — AP29
PREQ# — AP27

JE40 modify

TCK — AR26
TMS — AR27
TRST# — AP30 — XDP_TRST#

TDI — AR28
TDO — AP26 — XDP_TDO

DBR# — AL35 — XDP_DBRESET#

BPM#0 — AT28
BPM#1 — AR29
BPM#2 — AR30
BPM#3 — AT30
BPM#4 — AP32
BPM#5 — AR31
BPM#6 — AT31
BPM#7 — AR32

JE40 modify

1D05V_VTT

RN501
SRN51J-GP

XDP_TDO
XDP_TRST#

1D05V_VTT — R501 62R2J-GP — H_PROCHOT# — C502 SC47P50V2JN-3GP

CRB : 47pf
CEKLT:43pf

Connect EC to PROCHOT# through inverting OD buffer.

3D3V_S0

RN503
SRN1K5J-1-GP

XDP_DBRESET#
18,27,31,36,65,66,82,97 PLT_RST# — BUF_CPU_RST#

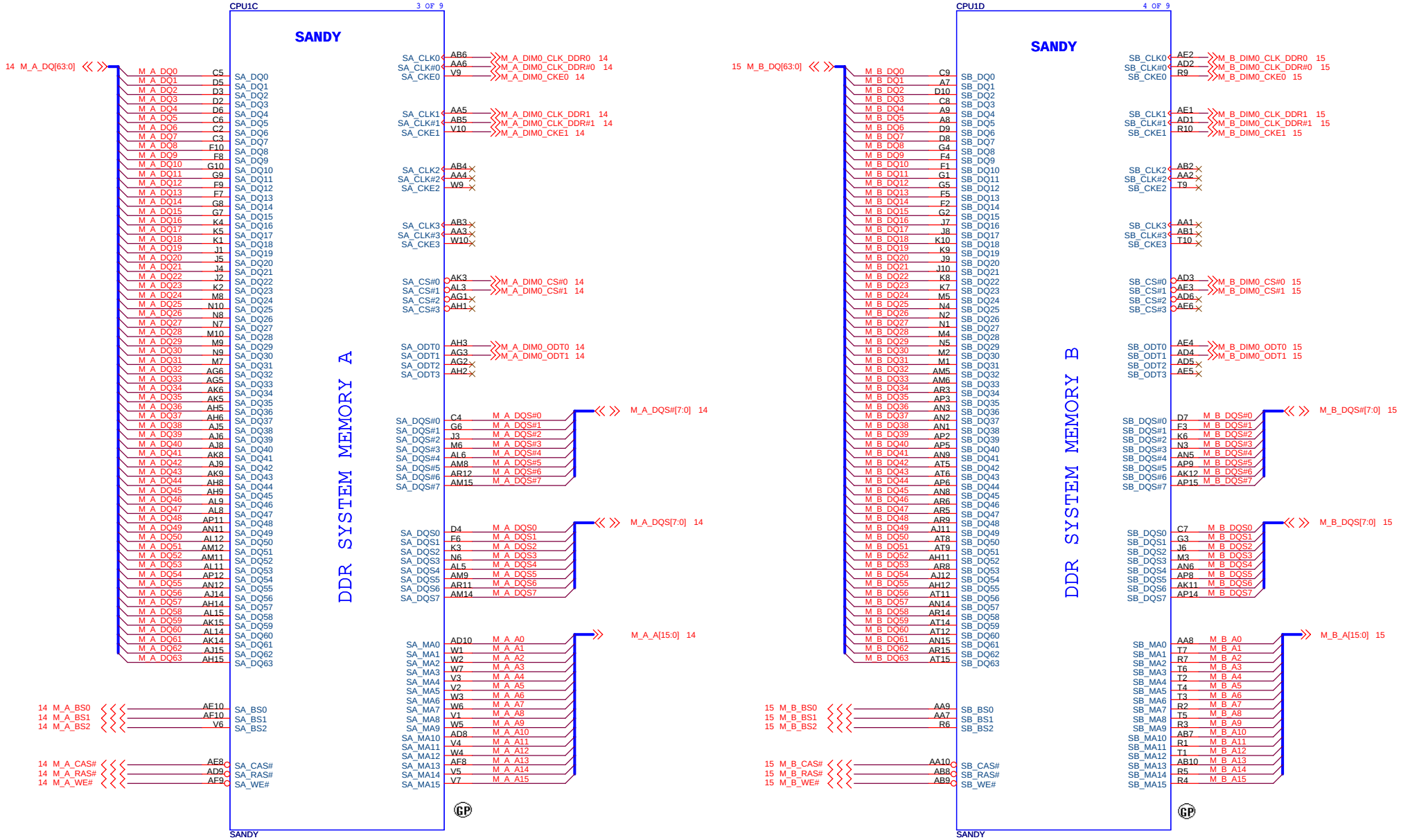
Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistorpower (~15 mW) may be wasted.

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU (THERMAL/CLOCK/PM)	
Size: Custom	Document Number: JE40-HR	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 5 of 102	

SSID = CPU



HR UMA

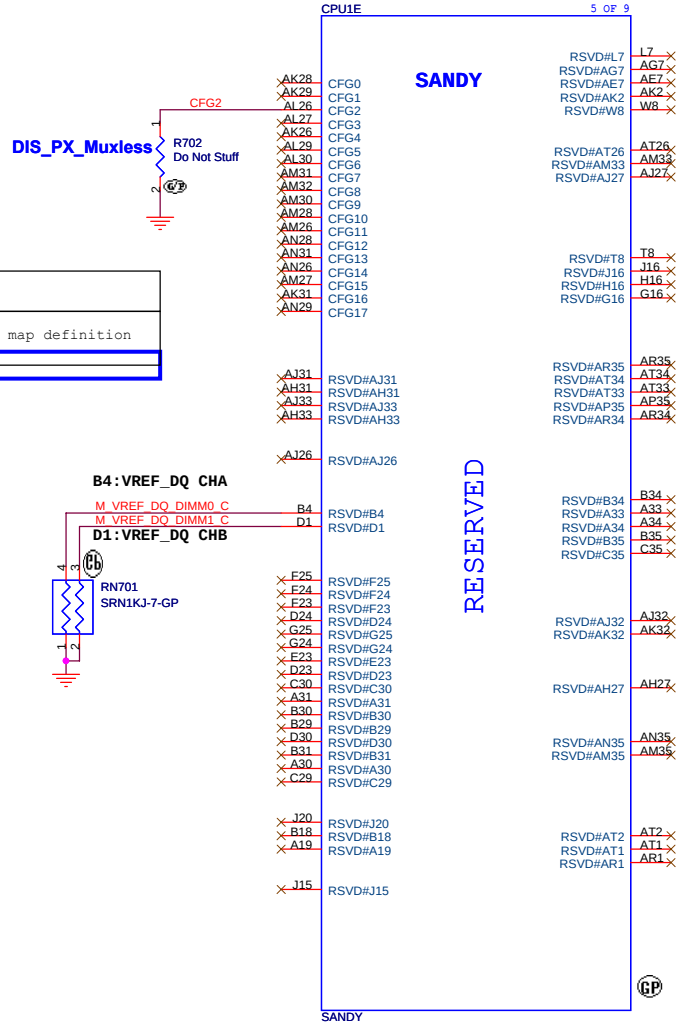
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (DDR)***

Size	Document Number	Rev
A3	**JE40-HR**	**-1**

Date: Tuesday, March 29, 2011 Sheet 6 of 102

SSID = CPU



PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
	0:Lane Reversed

HR UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***CPU (RESERVED)***
Size A3	Document Number **JE40-HR** Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 7 of 102

SSID = CPU

POWER

PROCESSOR CORE POWER

53A

VCC_CORE

-2 M DY

C816 SC10U6D3V5KX-1GP, C822 SC10U6D3V5KX-1GP, C823 SC10U6D3V5KX-1GP, C824 SC10U6D3V5KX-1GP, C825 SC10U6D3V5KX-1GP, C826 SC10U6D3V5KX-1GP, C827 SC10U6D3V5KX-1GP — -2 M DY

C837 SC10U6D3V5KX-1GP, C836 SC10U6D3V5KX-1GP, C835 SC10U6D3V5KX-1GP, C834 SC10U6D3V5KX-1GP, C833 SC10U6D3V5KX-1GP, C828 SC10U6D3V5KX-1GP — -2 M DY

VCC Output Decoupling Recommendation:
4 x 470 uF at Bottom Socket Edge
8 x 22 uF at Top Socket Cavity
8 x 22 uF at Top Socket Edge
8 x 22 uF at Bottom Socket Cavity

CPU1F — SANDY — 6 OF 9

CORE SUPPLY: VCC AG35, AG34, AG33, AG32, AG31, AG30, AG29, AG28, AG27, AG26, AE35, AE34, AE33, AE32, AE31, AE30, AE29, AE28, AE27, AE26, AD35, AD34, AD33, AD32, AD31, AD30, AD29, AD28, AD27, AD26, AC35, AC34, AC33, AC32, AC31, AC30, AC29, AC28, AC27, AC26, AA35, AA34, AA33, AA32, AA31, AA30, AA29, AA28, AA27, AA26, Y35, Y34, Y33, Y32, Y31, Y30, Y29, Y28, Y27, Y26, V35, V34, V33, V32, V31, V30, V29, V28, V27, V26, U35, U34, U33, U32, U31, U30, U29, U28, U27, U26, R35, R34, R33, R32, R31, R30, R29, R28, R27, R26, P35, P34, P33, P32, P31, P30, P29, P28, P27, P26

PEG AND DDR: VCCIO AH13, AH10, AG10, AC10, Y10, U10, P10, L10, J14, J13, J12, J11, H14, H12, H11, G14, G13, G12, F14, F13, F12, F11, E14, E12, E11, D14, D13, D12, D11, C14, C13, C12, C11, B14, B12, A14, A13, A12, A11, J23

VCCIO Output Decoupling Recommendation:
2 x 330 uF (3 x 330 uF for 2012 capable designs)
5 x 22 uF & 5 x 0805 no-stuff at Bottom
7 x 22 uF & 2 x 0805 no-stuff at Top

1D05V_VTT

C805, C806, C807, C809, C810, C838, C839, C840, C841 SC10U6D3V5KX-1GP

No-stuff sites outside the socket may be removed.
No-stuff sites inside the socket cavity need to remain.

1D05V_VTT

C812, C813, C814, C829, C830 SC10U6D3V5KX-1GP — -2 M DY — C843 Do Not Stuff, C844, C845 SC10U6D3V5KX-1GP

SVID:
VIDALERT# AJ29 — H_CPU_SVIDALRT# — R803 43R2J-GP — VR_SVID_ALERT# 42
VIDSCLK AJ30 — H_CPU_SVIDCLK 42
VIDSOUT AJ28 — H_CPU_SVIDDAT 42

For CRB VIDSOUT need to pull high 130 ohm closr to CPU and IMVP7
For CRB VIDALERT# need to pull high 75 ohm close to CPU

1D05V_VTT

H_CPU_SVIDDAT — R804 130R2F-1-GP

SENSE LINES:
VCC_SENSE AJ35 — VCCSENSE 42
VSS_SENSE AJ34 — VSSSENSE 42
VCCIO_SENSE B10 — VCCIO_SENSE 45
VSSIO_SENSE A10 — VSSIO_SENSE 45

VCC_CORE

R801,R802 close to CPU

R801 100R2F-L1-GP-U

R802 100R2F-L1-GP-U

SANDY

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VCC_CORE)

Size: Custom | Document Number: JE40-HR | Rev: -1

Date: Tuesday, March 29, 2011 | Sheet 8 of 102

SSID = CPU

VAXG Output Decoupling Recommendation:
2 x 470 uF at Bottom Socket Edge
2 x 22 uF at Top Socket Cavity
4 x 22 uF at Top Socket Edge
2 x 22 uF at Bottom Socket Cavity
4 x 22 uF at Bottom Socket Edge

R906,R907 close to CPU

POWER

CPU1G — SANDY — GRAPHICS — 7 OF 9

VCC_GFXCORE

PROCESSOR VAXG: 24A

C902 C903 C904 C905 SC10U6D3V5KX-1GP — -2 M DY — UMA_PX_Muxless

C908 C919 C920 C921 SC10U6D3V5KX-1GP — -2 M DY — UMA_PX_Muxless

VCC_GFXCORE

R903 Do Not Stuff DIS
R904 Do Not Stuff DIS
R905 Do Not Stuff DIS
R901 Do Not Stuff DIS

Disabling Guidelines for External Graphics Designs:
Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.
Can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed

1D8V_S0

PROCESSOR VCCPLL: 1.2A

C922 SC1U10V2KX-1GP

VCCPLL Output Decoupling Recommendation:
1 x 330 uF
2 x 1 uF
1 x 10 uF

SENSE LINES

VAXG_SENSE AK35 — VCC_AXG_SENSE 42
VSSAXG_SENSE AK34 — VSS_AXG_SENSE 42

Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on S3 power reduction implementation.

+V_SM_VREF_CNT should have 10 mil trace width

VREF

SM_VREF AL1 — +V_SM_VREF_CNT 37

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT should have 10 mils trace width.

DDR3 -1.5V RAILS

1D5V_S0

PROCESSOR VDDQ: 10A

C910 C911 C912 C913 SC10U6D3V5KX-1GP — -2M DY

-2M add R908 R909 for intel update support Celeron Pentium CPU

SA RAIL

0D85V_S0 — 1D05V_VTT

PROCESSOR VCCSA: 6A

C915 SC10U6D3V5KX-1GP — -2M DY

Celeron R909 Do Not Stuff
R910 Do Not Stuff Celeron

R902 10R2J-2-GP

R902 need be close to pin H23.

MISC

VCCSA_SENSE H23 — VCCUSA_SENSE — TP901 Do Not Stuff

FC_C22 C22 — H_FC_C22
VCCSA_VID1 C24 — VCCSA_SEL

-2 M DY page off

RN901 SRN1KJ-7-GP

VCC_GFXCORE

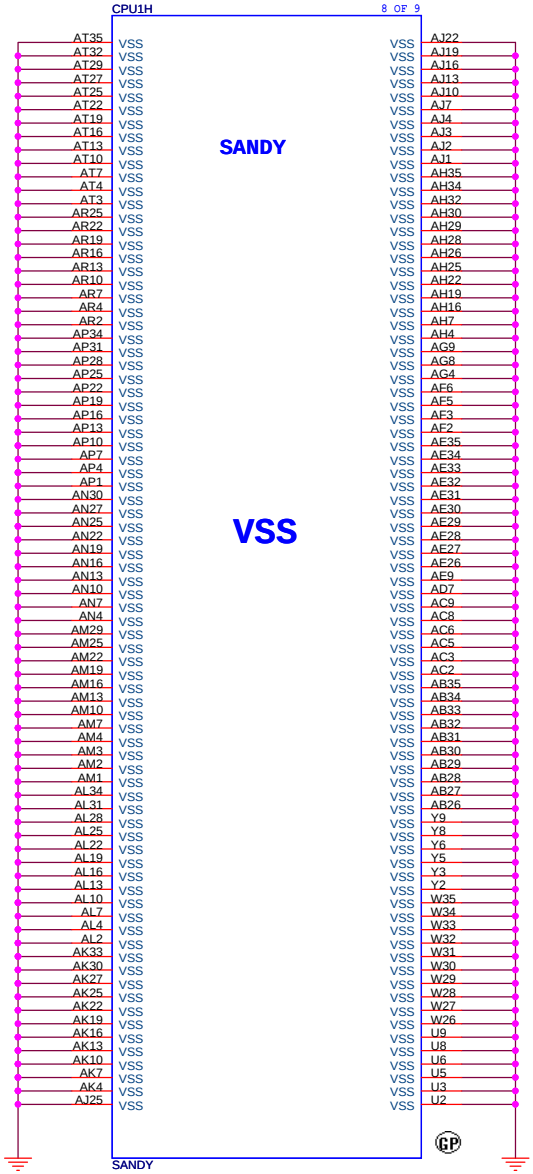
R906 100R2F-L1-GP-U
R907 100R2F-L1-GP-U

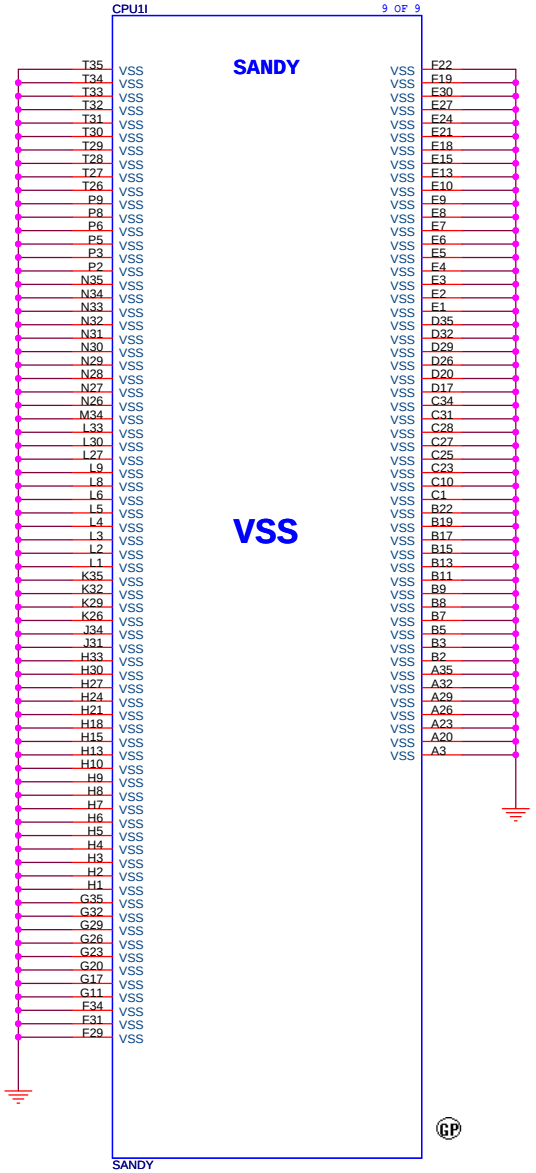
VCC_AXG_SENSE
VSS_AXG_SENSE

HR UMA

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	CPU (VCC_GFXCORE)
Size A3	Document Number JE40-HR
Rev	-1
Date: Tuesday, March 29, 2011	Sheet 9 of 102

SSID = CPU





HR UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CPU (VSS)***	
Size A3	Document Number **JE40-HR**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 10 of 102	

JE40 delete XDP function

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *XDP*

Size	Document Number	Rev
A3	JE40-HR	-1

Date: Tuesday, March 29, 2011 Sheet 11 of 102

(Blanking)

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Tuesday, March 29, 2011 Sheet 12 of 102

(Blanking)

HR UMA

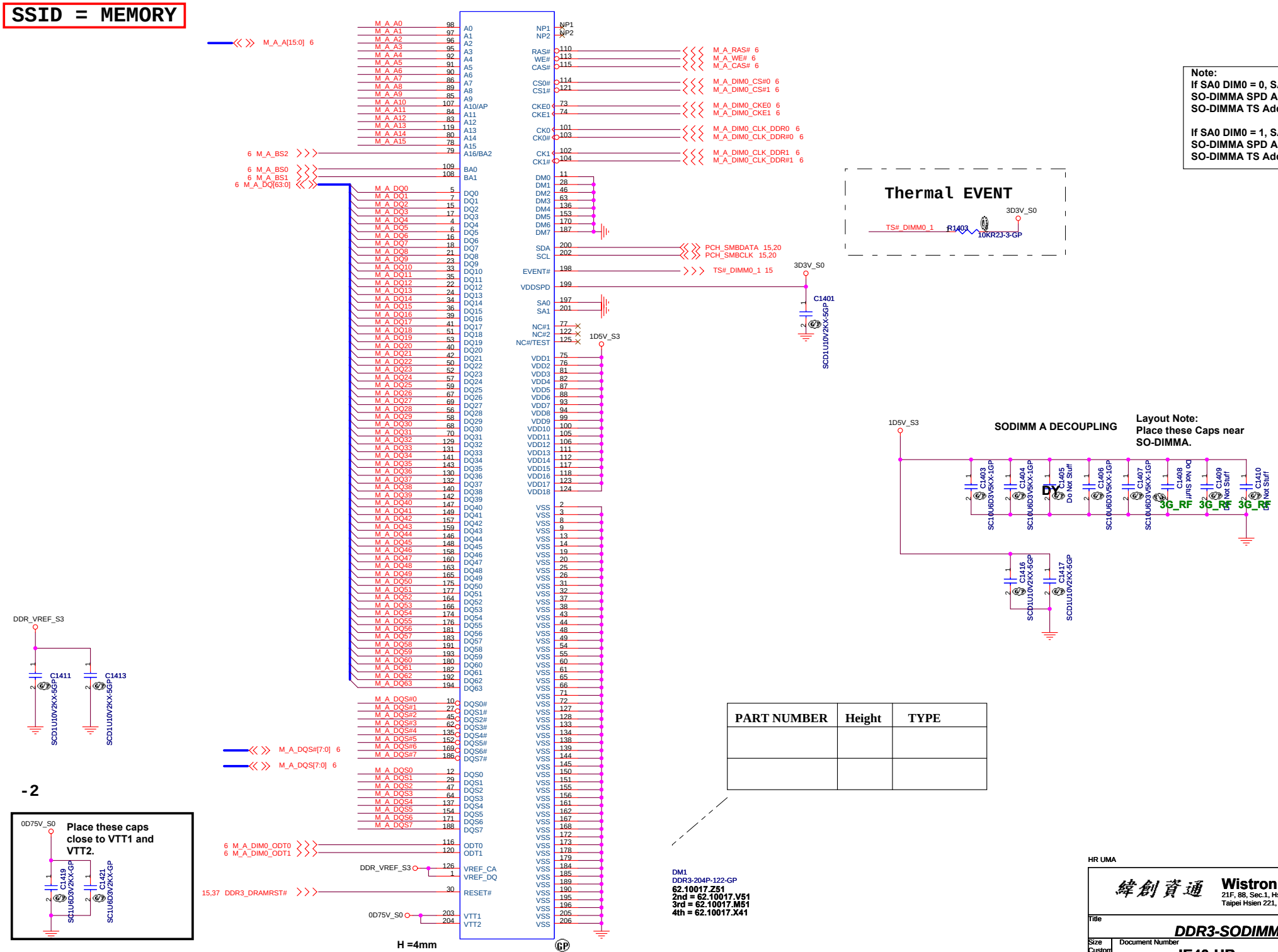
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Tuesday, March 29, 2011 Sheet 13 of 102

SSID = MEMORY



PART NUMBER	Height	TYPE

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR3-SODIMM1***

Size: Custom | Document Number: **JE40-HR** | Rev: **-1**

Date: Tuesday, March 29, 2011 | Sheet 14 of 102

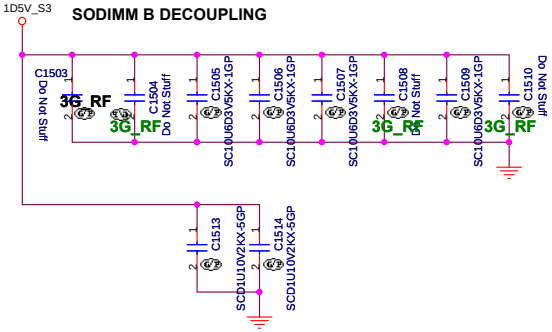
SSID = MEMORY

DM2
DDR3-204P-126-GP
62.10024.D41

2nd = 62.10017.R91
3rd = 62.10017.V61
4th = 62.10017.X51

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA



Layout Note:
Place these Caps near SO-DIMMB.

DDR_VREF_S3

C1515 SCD1U10V2KX-5GP

C1517 SCD1U10V2KX-5GP

-2

Place these caps close to VTT1 and VTT2.

0D75V_S0

C1519 SC1U6D3V2KX-GP

C1521 SC1U6D3V2KX-GP

HR UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	***DDR3-SODIMM2***		
Size Custom	Document Number **JE40-HR**		Rev **-1**
Date: Tuesday, March 29, 2011		Sheet 15 of 102	

(Blanking)

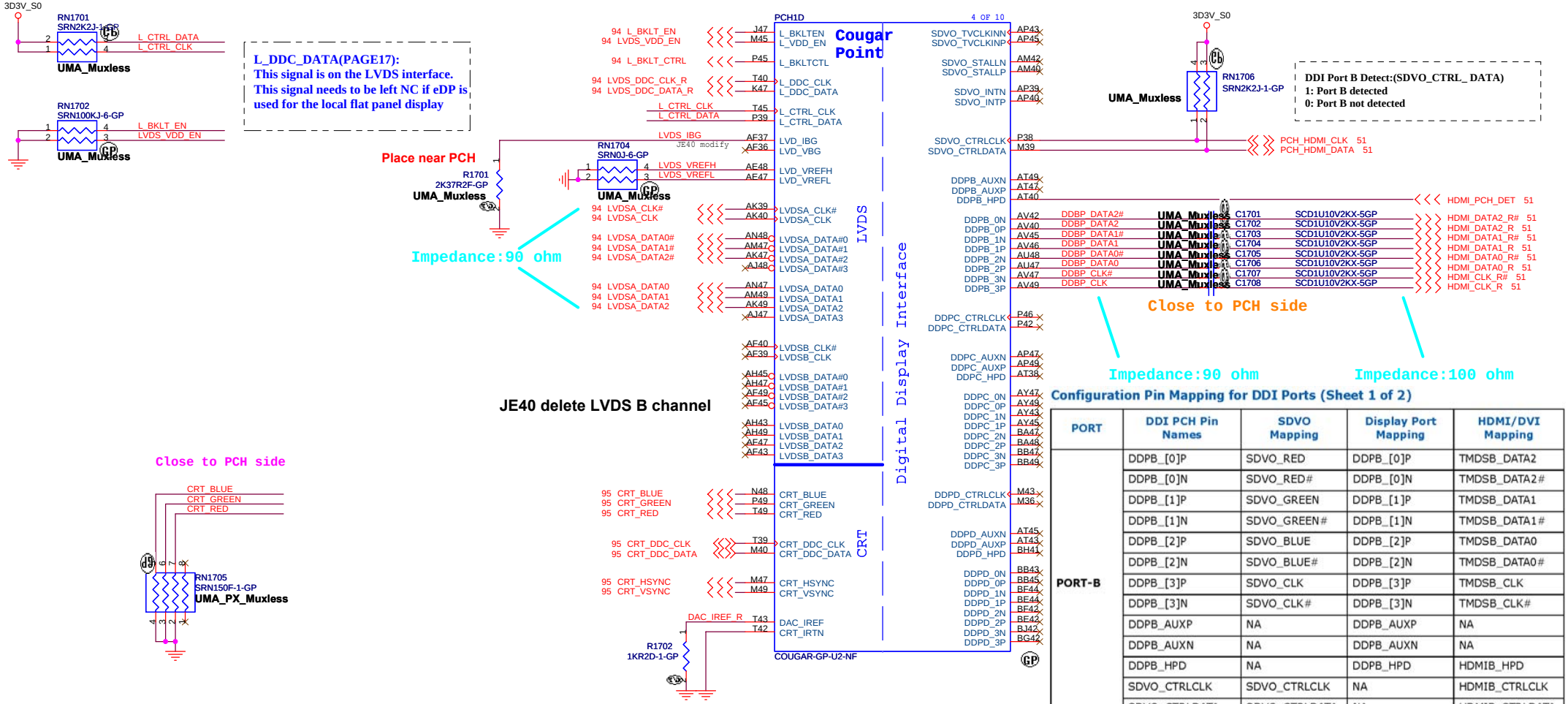
HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM2

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Tuesday, March 29, 2011 Sheet 16 of 102



Configuration Pin Mapping for DDI Ports (Sheet 1 of 2)

PORT	DDI PCH Pin Names	SDVO Mapping	Display Port Mapping	HDMI/DVI Mapping
PORT-B	DDPB_[0]P	SDVO_RED	DDPB_[0]P	TMDSB_DATA2
	DDPB_[0]N	SDVO_RED#	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	SDVO_GREEN	DDPB_[1]P	TMDSB_DATA1
	DDPB_[1]N	SDVO_GREEN#	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	SDVO_BLUE	DDPB_[2]P	TMDSB_DATA0
	DDPB_[2]N	SDVO_BLUE#	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	SDVO_CLK	DDPB_[3]P	TMDSB_CLK
	DDPB_[3]N	SDVO_CLK#	DDPB_[3]N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
	DDPB_HPD	NA	DDPB_HPD	HDMIB_HPD
	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMIB_CTRLCLK
	SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMIB_CTRLDATA

HR UMA

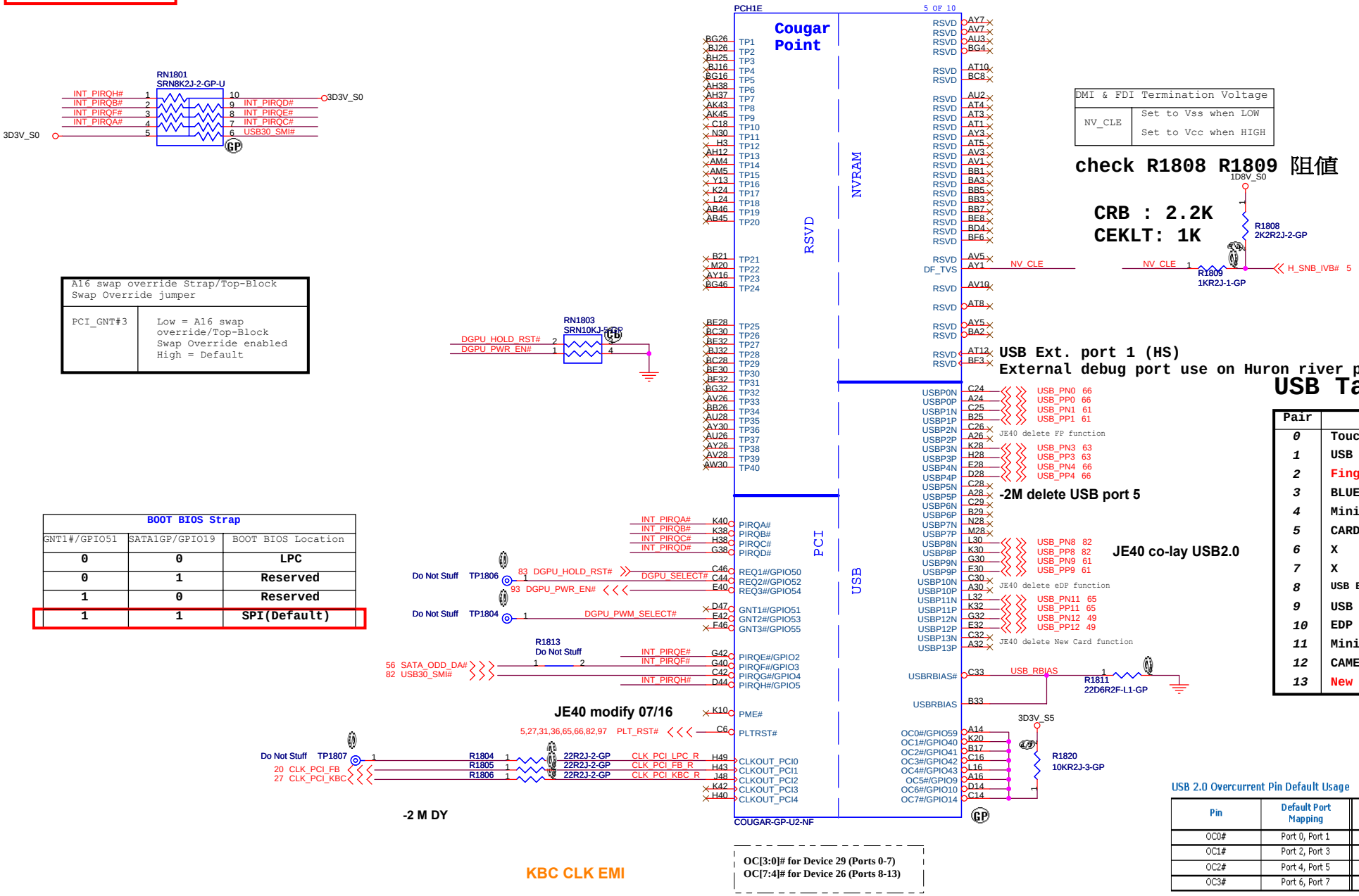
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PCH (LVDS/CRT/DDI)***

Size: A3 | Document Number: **JE40-HR** | Rev: **-1**

Date: Tuesday, March 29, 2011 | Sheet 17 of 102

SSID = PCH



DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

check R1808 R1809 阻值

CRB : 2.2K
CEKLT: 1K

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER(DY)
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

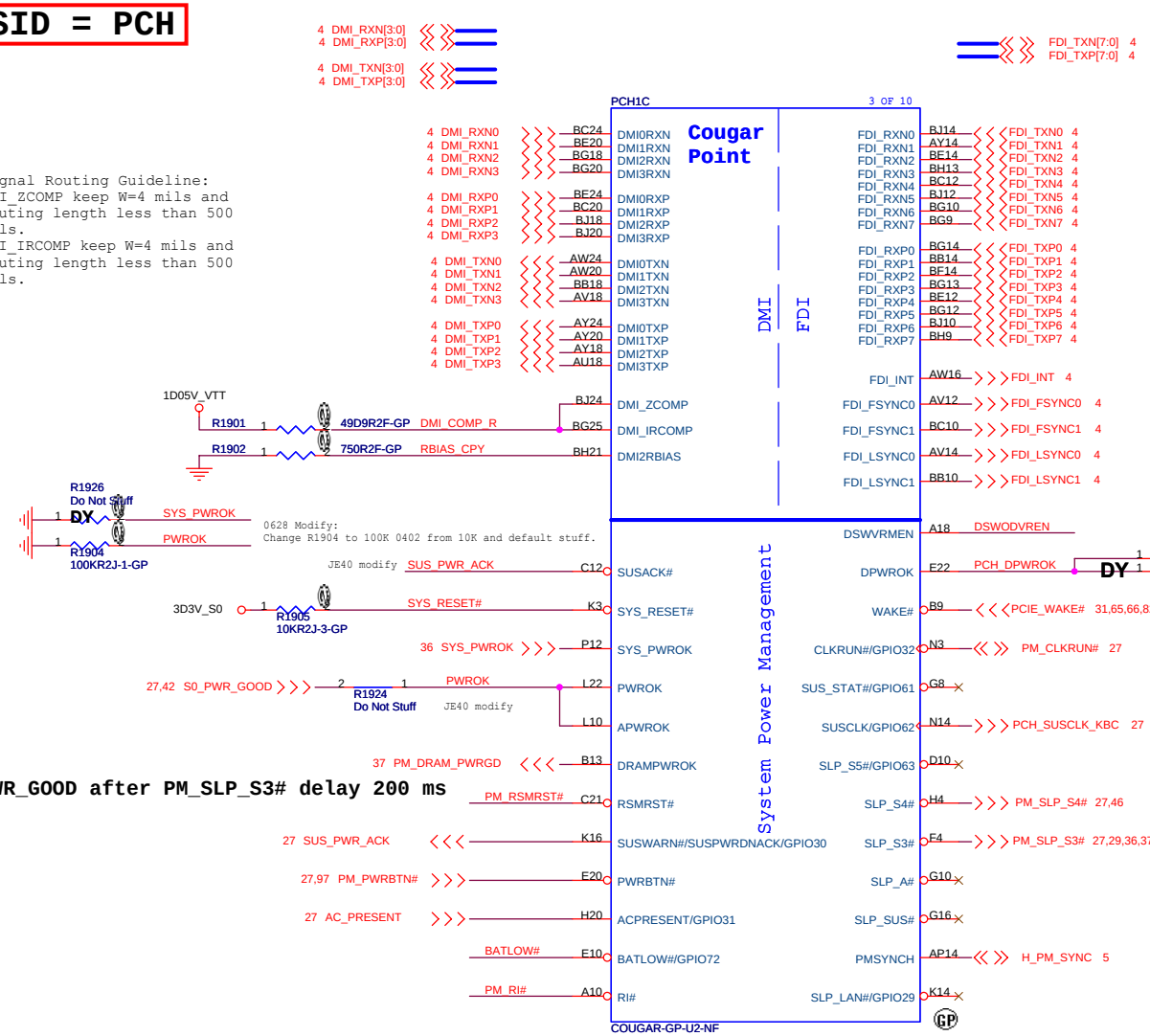
Title: PCH (PCI/USB/NVRAM)

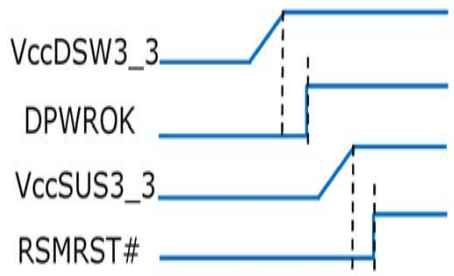
Size: A3 | Document Number: JE40-HR | Rev: -1

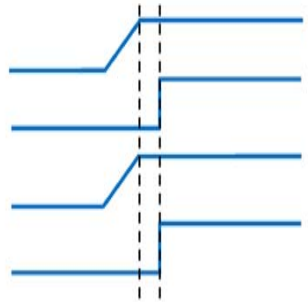
Date: Tuesday, March 29, 2011 | Sheet 18 of 102

SSID = PCH

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.







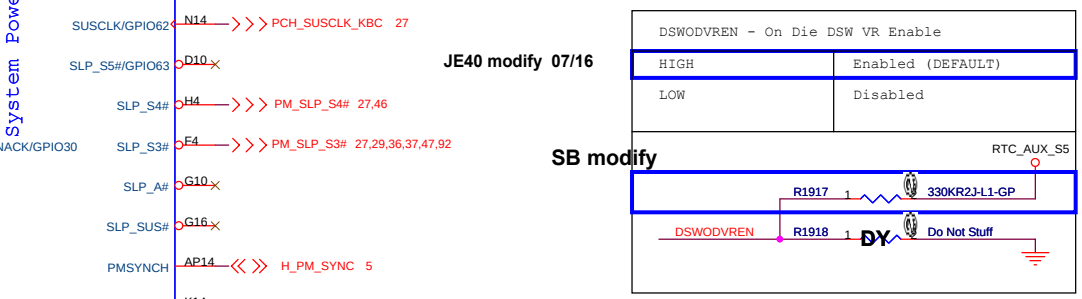
For platforms not supporting Deep S4/S5
1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
2.DPWROK and RSMRST# will rise at the same time (connected on board)
3.SLP_SUS# and SUSACK# are left as 'no connect'
4.SUSWARN# used as SUSPWRDNACK/GPIO30

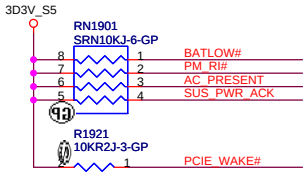
S0_PWR_GOOD after PM_SLP_S3# delay 200 ms

JE40 modify 07/16

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

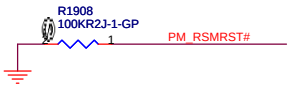
SB modify



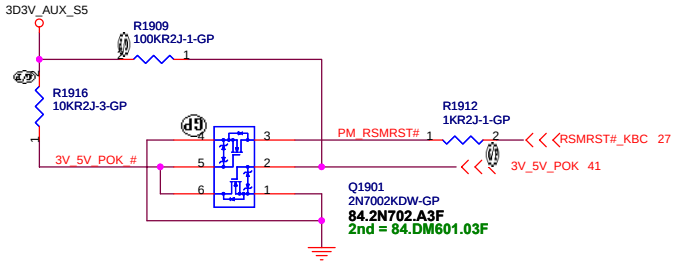


PCIE_WAKE#
CRB : 1K
CEKLT: 10K

PWRBTN#
This signal has an internal pull-up resistor



PM_RSMRST#
CRB : PL 10K
ANNIE : PL 100K



HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	PCH (DM I/FDI/PM)	
Size A3	Document Number JE40-HR	Rev -1
Date: Tuesday, March 29, 2011	Sheet 19 of 102	

SSID = PCH

PCH1B — Cougar Point — 2 OF 10

PCI-E*: W-WAN, WLAN, Card Reader, LAN, USB3.0, Intel GBE LAN, Dock, NEW CARD

SMBUS: SMBALERT#/GPIO11, SMBCLK, SMBDATA, SML0ALERT#/GPIO60, SML0CLK, SML0DATA, SML1ALERT#/PCHHOT#/GPIO74, SML1CLK/GPIO58, SML1DATA/GPIO75

Controller Link: CL_CLK1, CL_DATA1, CL_RST1#

CLOCKS: CLKOUT_PCIE0N/P, PCIECLKRQ0#/GPIO73, CLKOUT_PCIE1N/P, PCIECLKRQ1#/GPIO18, CLKOUT_PCIE2N/P, PCIECLKRQ2#/GPIO20, CLKOUT_PCIE3N/P, PCIECLKRQ3#/GPIO25, CLKOUT_PCIE4N/P, PCIECLKRQ4#/GPIO26, CLKOUT_PCIE5N/P, PCIECLKRQ5#/GPIO44, CLKOUT_PEG_B_N/P, PEG_B_CLKRQ#/GPIO56, CLKOUT_PCIE6N/P, PCIECLKRQ6#/GPIO45, CLKOUT_PCIE7N/P, PCIECLKRQ7#/GPIO46, CLKOUT_ITPXDP_N/P, PEG_A_CLKRQ#/GPIO47, CLKOUT_PEG_A_N/P, CLKOUT_DMI_N/P, CLKOUT_DP_N/P, CLKIN_DMI_N/P, CLKIN_GND1_N/P, CLKIN_DOT_96N/P, CLKIN_SATA_N/P, REFCLK14IN, CLKIN_PCILOOPBACK, XTAL25_IN/XTAL25_OUT, XCLK_RCOMP

FLEX CLOCKS: CLKOUTFLEX0/GPIO64, CLKOUTFLEX1/GPIO65, CLKOUTFLEX2/GPIO66, CLKOUTFLEX3/GPIO67

COUGAR-GP-U2-NF

65 PCIE_RXN2 / 65 PCIE_RXP2 / 65 PCIE_TXN2 / 65 PCIE_TXP2 — C2001, C2002 — SCD1U10V2KX-5GP — PCIE_TXN2_C, PCIE_TXP2_C

31 PCIE_RXN4 / 31 PCIE_RXP4 / 31 PCIE_TXN4 / 31 PCIE_TXP4 — C2005, C2006 — SCD1U10V2KX-5GP — PCIE_TXN4_C, PCIE_TXP4_C

82 PCIE_RXN5 / 82 PCIE_RXP5 / 82 PCIE_TXN5 / 82 PCIE_TXP5 — C2009, C2010 — SCD1U10V2KX-5GP — PCIE_TXN5_C, PCIE_TXP5_C

JE40 delete New Card function

JE40 delete XDP function

JE40 modify

For DIS_PX mode or MXM mode.

SB

3D3V_S0 — R2004 10KR2J-3-GP — PEG_CLKREQ# R — R2005 Do Not Stuff (DY)

3D3V_S5 — RN2003 SRN2K2J-1-GP (SMB_CLK, SMB_DATA) — RN2004 SRN2K2J-1-GP (SML0_DATA, SML0_CLK) — RN2005 SRN2K2J-1-GP (SML1_CLK, SML1_DATA) — RN2006 SRN10KJ-5-GP (PCH_GPIO74, PCIE_CLK_REQ6#) — R2009 1KR2J-1-GP (DRAMRST_CNTRL_PCH)

CRB : 1K
CEKLT: 10K

3D3V_S0 — RN2007 SRN2K2J-1-GP — Q2001 2N7002KDW-GP — 84.2N702.A3F — 2nd = 84.DM601.03F — SMB_DATA, SMB_CLK — PCH_SMBDATA 14,15 — PCH_SMBCLK 14,15

R2008 and C2008 CO-LAY

XTAL25_IN — R2006 1M1R2J-GP — X2001 XTAL-25MHZ-102-GP — 82.30020.851 — 2nd = 82.30020.791 — C2008 SC12P50V2JN-3GP — C2007 SC12P50V2JN-3GP — XTAL25_OUT

WWAN CLK — CLK_PCIE_WWAN_REQ#

WLAN CLK — RN2012 SRN0J-6-GP — 65 CLK_PCIE_WLAN# / 65 CLK_PCIE_WLAN — CLK_PCH_SRC1_N / CLK_PCH_SRC1_P — 65 CLK_PCIE_WLAN_REQ#

LAN CLK — RN2014 SRN0J-6-GP — 31 CLK_PCIE_LAN# / 31 CLK_PCIE_LAN — CLK_PCH_SRC3_N / CLK_PCH_SRC3_P — PCIE_CLK_RQ2# — 31 PCIE_CLK_LAN_RQ#

USB3.0 CLK — RN2013 SRN0J-6-GP — 82 CLK_PCIE_USB3# / 82 CLK_PCIE_USB3 — CLK_PCH_SRC4_N / CLK_PCH_SRC4_P — 82 USB3_PEGB_CLKREQ#

3D3V_S0 — RN2018 SRN10KJ-5-GP — PCIE_CLK_RQ2# — CLK_PCIE_WLAN_REQ#

PCIE_CLK_REQ5# — PEG_B_CLKRQ# — PCIE_CLK_REQ6# — CLK_PCIE_NEW_REQ#

PCIECLKRQ1# and PCIECLKRQ2#
Support S0 power only

RN2016 SRN0J-6-GP — CLK_PCIE_VGA# 83 / CLK_PCIE_VGA 83 — CLK_EXP_N 5 / CLK_EXP_P 5

RN2008 SRN10KJ-5-GP — CLK_BUF_CPYCLK_N / CLK_BUF_CPYCLK_P

R2003 Do Not Stuff — PEG_CLKREQ# 83

R2007 90D9R2F-1-GP — XCLK_RCOMP — 1D05V_VTT

-2M DY delete 48MHz

3D3V_S0 — R2012 UMA_Muxless (10KR2J-3-GP) — R2010 DIS_PX (Do Not Stuff)

3D3V_S0 — R2013 DIS_UMA (10KR2J-3-GP) — R2011 PX_Muxless (Do Not Stuff) — DGPU_PRSNT# — UMA_DIS# 22

UMA_DISCRETE#
UMA: 1 1
DIS :0 1
SG(PX) : 0 0
Optimus(Muxless) : 1 0

RN2009 SRN10KJ-L3-GP — CLK_BUF_REF14, CLK_BUF_CKSSCD_P, CLK_BUF_CKSSCD_N — CLK_BUF_EXP_P, CLK_BUF_EXP_N, CLK_BUF_DOT96_N, CLK_BUF_DOT96_P

need very close to PCH

3D3V_S5 — RN2001 SRN10KJ-6-GP — PCIE_CLK_LAN_RQ#, CLK_PCIE_WWAN_REQ#, USB3_PEGB_CLKREQ#

RN2002 SRN10KJ-6-GP — PCIE_CLK_REQ5#, CLK_PCIE_NEW_REQ#, PEG_B_CLKRQ#, EC_SWI#

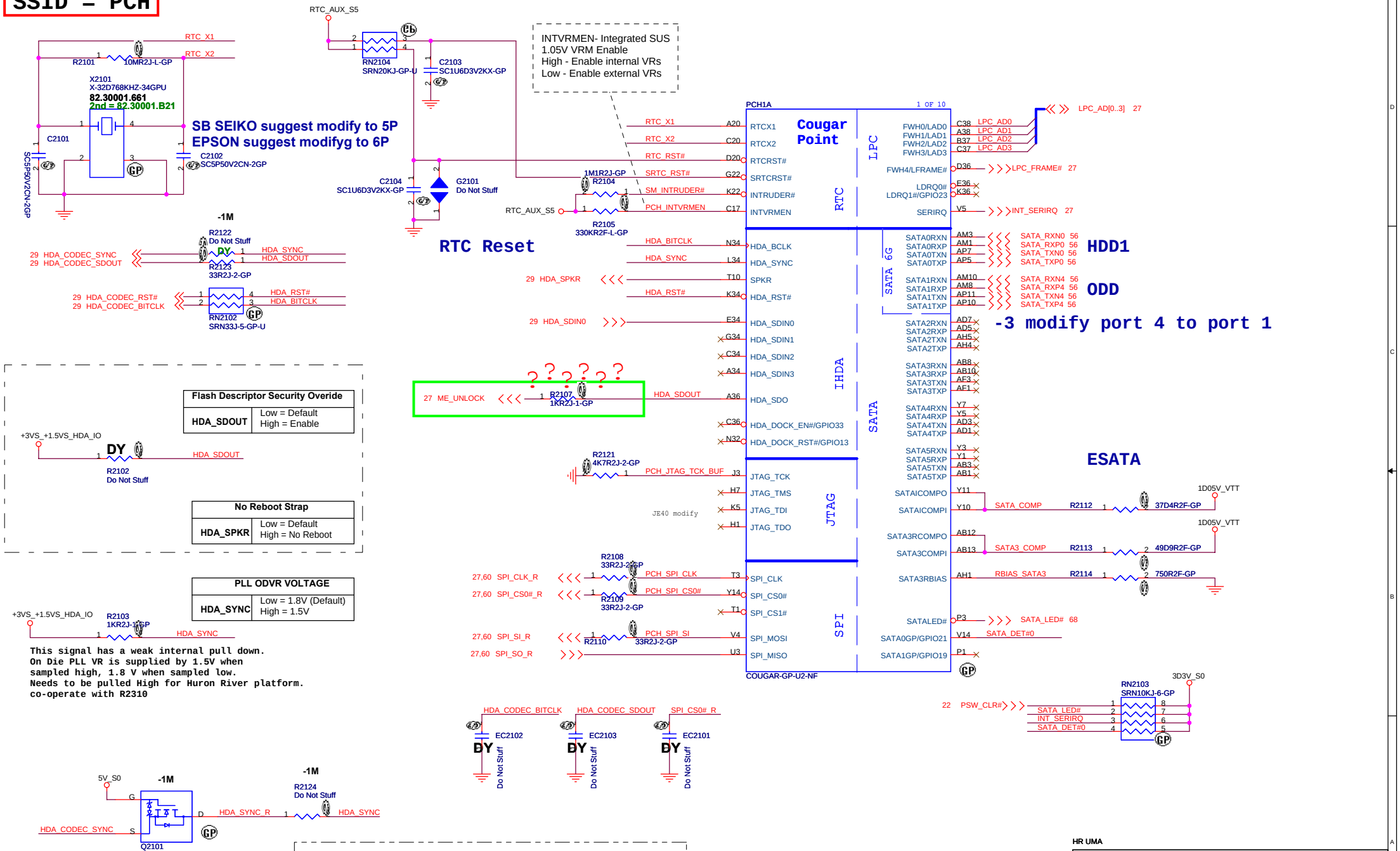
- Prioritize 27/14/24/48/25-MHz FLEX on FLEX1 and FLEX3
- Do not configure 27/14/24/48/25-MHz FLEX clock on FLEX0 and FLEX2 if more than 2 PCI clocks + PCI loopback are routed.

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

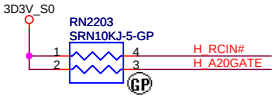
Title: PCH (PCI-E/SMBUS/CLOCK/CL)
Size: A3 | Document Number: JE40-HR | Rev: -1
Date: Tuesday, March 29, 2011 | Sheet 20 of 102

SSID = PCH

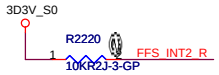

RTC_X1
RTC_X2
R2101
10MR2J-L-GP
X2101
X-32D768KHZ-34GPU
82.30001.661
2nd = 82.30001.B21
C2101
C2102
SC5P50V2CN-2GP
SB SEIKO suggest modify to 5P
EPSON suggest modifyg to 6P
RTC_AUX_S5
RN2104
SRN20KJ-GP-U
C2103
SC1U6D3V2KX-GP
C2104
SC1U6D3V2KX-GP
G2101
Do Not Stuff
INTVRMEN- Integrated SUS 1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs
1M1R2J-GP
R2104
R2105
330KR2F-L-GP
RTC Reset
PCH1A
1 OF 10
Cougar Point
RTC
LPC
SATA 6G
IHDA
SATA
JTAG
SPI
COUGAR-GP-U2-NF
RTCX1
RTCX2
RTCRST#
SRTCRST#
INTRUDER#
INTVRMEN
SRTC_RST#
SM_INTRUDER#
PCH_INTVRMEN
HDA_BITCLK
HDA_SYNC
SPKR
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDO
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO13
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
SPI_CLK
SPI_CS0#
SPI_CS1#
SPI_MOSI
SPI_MISO
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
SERIRQ
LPC_AD[0..3] 27
LPC_FRAME# 27
INT_SERIRQ 27
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA3RXN
SATA3RXP
SATA3TXN
SATA3TXP
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATAICOMPO
SATAICOMPI
SATA3RCOMPO
SATA3COMPI
SATA3RBIAS
SATALED#
SATA0GP/GPIO21
SATA1GP/GPIO19
HDD1
ODD
-3 modify port 4 to port 1
ESATA
SATA_COMP
R2112
37D4R2F-GP
1D05V_VTT
SATA3_COMP
R2113
49D9R2F-GP
RBIAS_SATA3
R2114
750R2F-GP
SATA_LED# 68
SATA_DET#0
RN2103
SRN10KJ-6-GP
3D3V_S0
22 PSW_CLR#
-1M
R2122
Do Not Stuff
DY
29 HDA_CODEC_SYNC
29 HDA_CODEC_SDOUT
HDA_SYNC
HDA_SDOUT
R2123
33R2J-2-GP
29 HDA_CODEC_RST#
29 HDA_CODEC_BITCLK
HDA_RST#
HDA_BITCLK
RN2102
SRN33J-5-GP-U
29 HDA_SPKR
29 HDA_SDIN0
27 ME_UNLOCK
R2107
1KR2J-1-GP
HDA_SDOUT
Flash Descriptor Security Overide
HDA_SDOUT
Low = Default
High = Enable
+3VS_+1.5VS_HDA_IO
R2102
Do Not Stuff
No Reboot Strap
HDA_SPKR
Low = Default
High = No Reboot
R2121
4K7R2J-2-GP
PCH_JTAG_TCK_BUF
JE40 modify
R2108
33R2J-2-GP
27,60 SPI_CLK_R
PCH_SPI_CLK
27,60 SPI_CS0#_R
PCH_SPI_CS0#
R2109
33R2J-2-GP
PLL ODVR VOLTAGE
HDA_SYNC
Low = 1.8V (Default)
High = 1.5V
R2103
1KR2J-1-GP
This signal has a weak internal pull down.
On Die PLL VR is supplied by 1.5V when
sampled high, 1.8 V when sampled low.
Needs to be pulled High for Huron River platform.
co-operate with R2310
27,60 SPI_SI_R
R2110
PCH_SPI_SI
33R2J-2-GP
27,60 SPI_SO_R
HDA_CODEC_BITCLK
HDA_CODEC_SDOUT
SPI_CS0# R
EC2102
EC2103
EC2101
DY
Do Not Stuff
5V_S0
-1M
HDA_CODEC_SYNC
HDA_SYNC_R
R2124
Do Not Stuff
HDA_SYNC
Q2101
Do Not Stuff
Do Not Stuff
2ND = 84.2N702.031
HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.
HR UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (SPI/RTC/LPC/SATA/IHDA)
Size
A3
Document Number
JE40-HR
Rev
-1
Date: Tuesday, March 29, 2011
Sheet 21 of 102

SSID = PCH

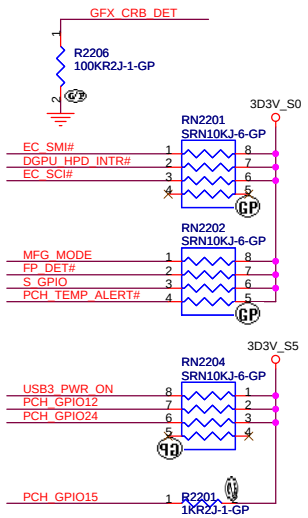
Note:
For PCH debug with XDP, need to NO STUFF R2218

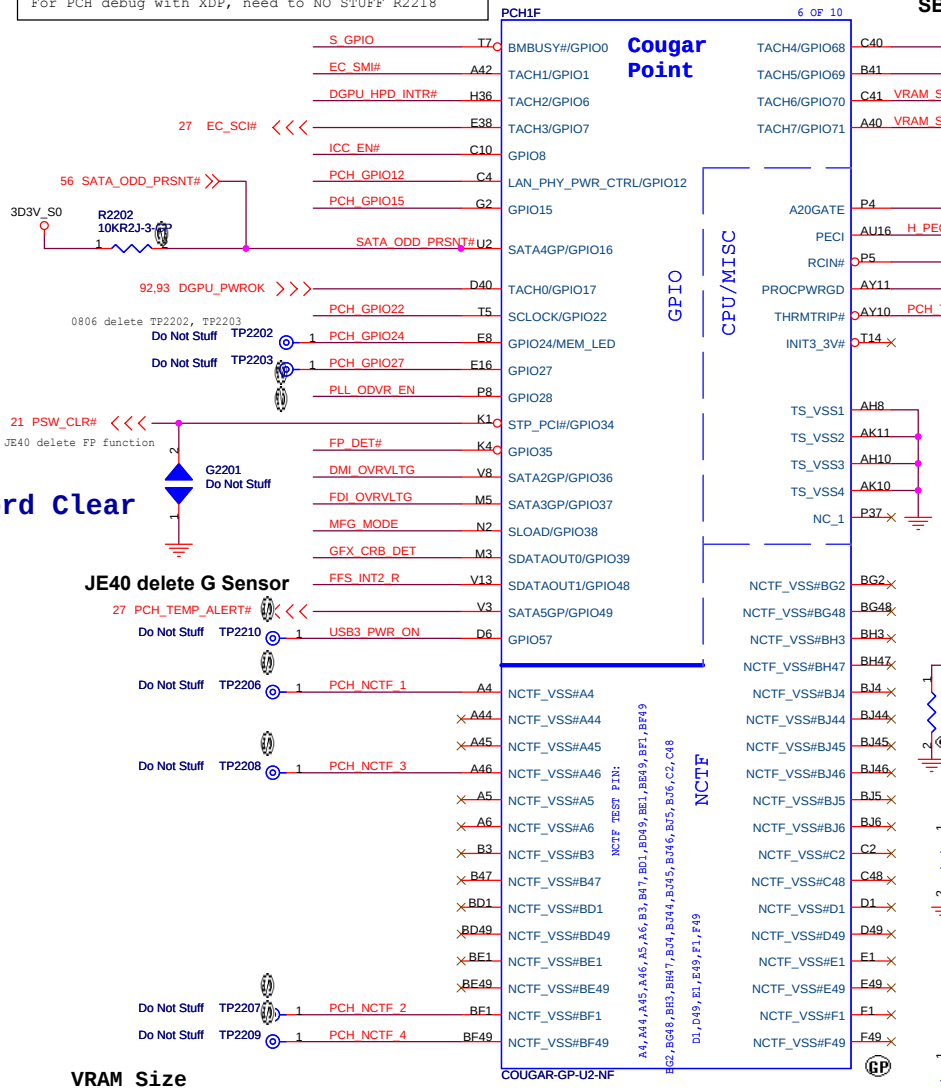


GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator, should not place external pull down.



	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY





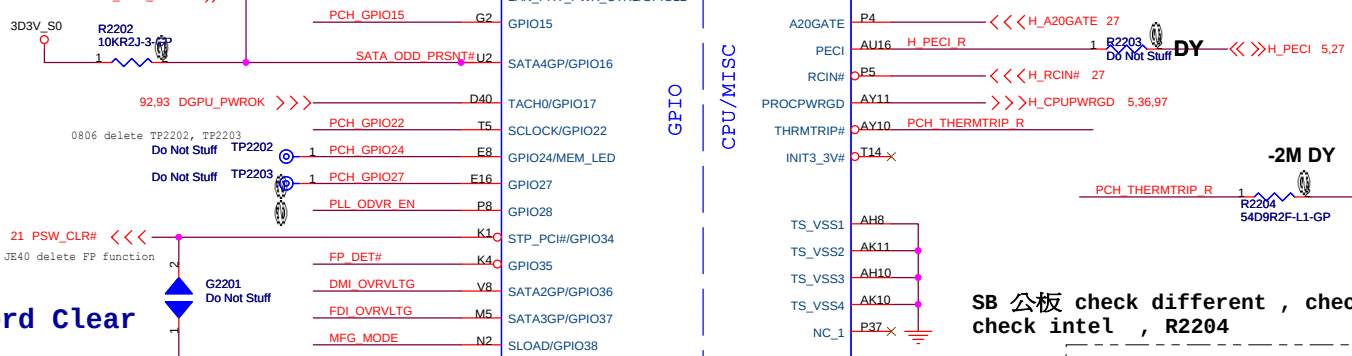
Do Not Stuff TP2202
Do Not Stuff TP2203
0806 delete TP2202, TP2203
JE40 delete FP function
G2201 Do Not Stuff
Do Not Stuff TP2210
Do Not Stuff TP2206
Do Not Stuff TP2208
Do Not Stuff TP2207
Do Not Stuff TP2209

Pass Word Clear

JE40 delete G Sensor

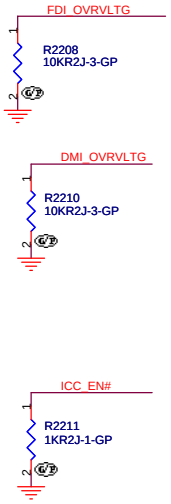
SB add Zero ODD function

SATA_ODD_PWRGT 56
UMA_DIS# 20



SB 公板 check different , check need modify or not check intel , R2204

TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.



FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

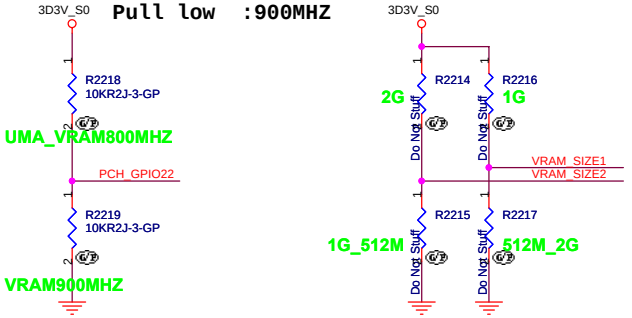
Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT]
	LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

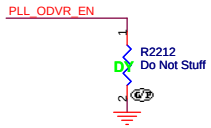
SB VRAM Frequency

Pull high: 800MHZ
Pull low :900MHZ

VRAM Size



PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)



HR UMA

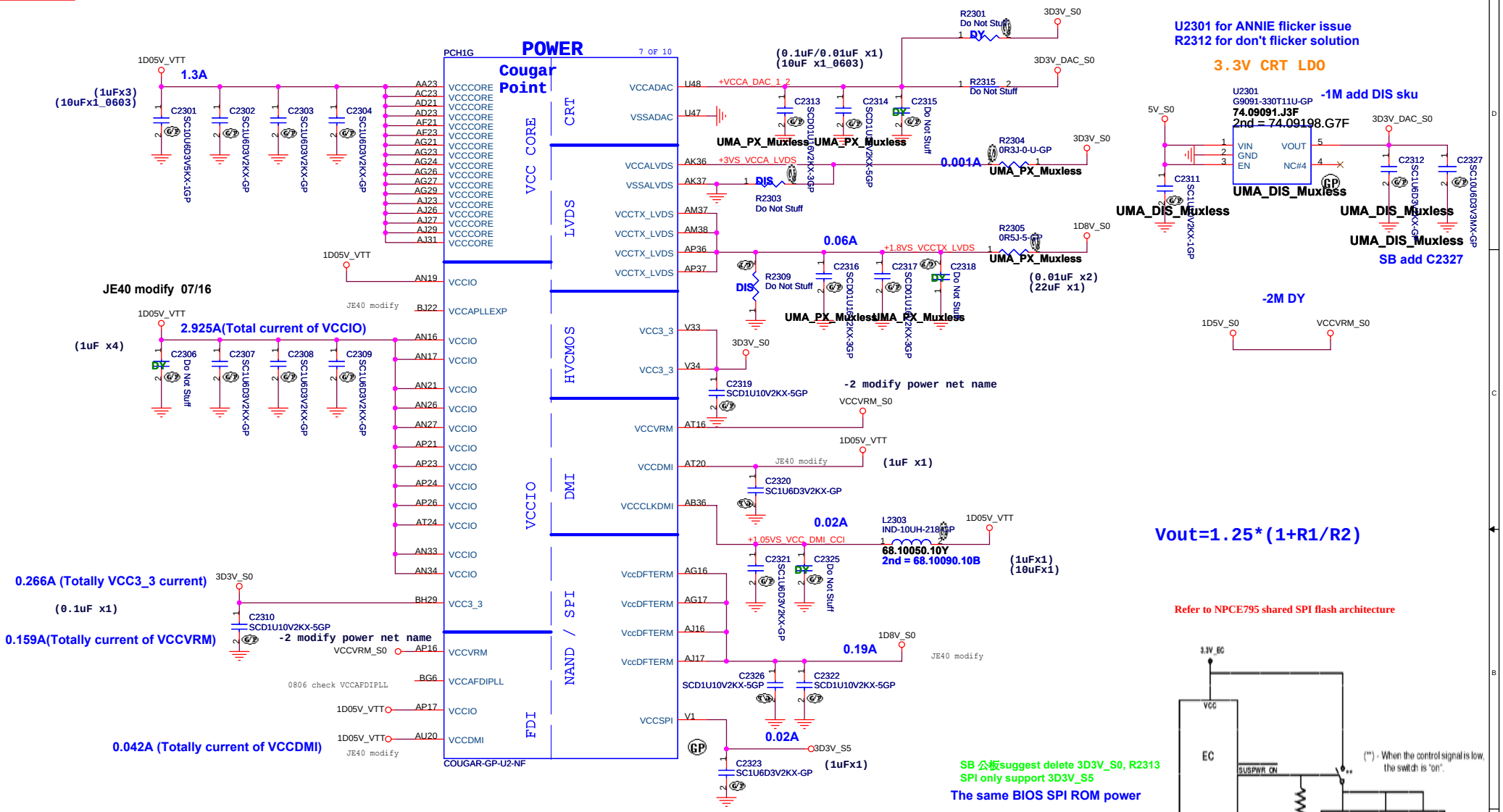
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (GPIO/CPU)

Size: A3 | Document Number: JE40-HR | Rev: -1

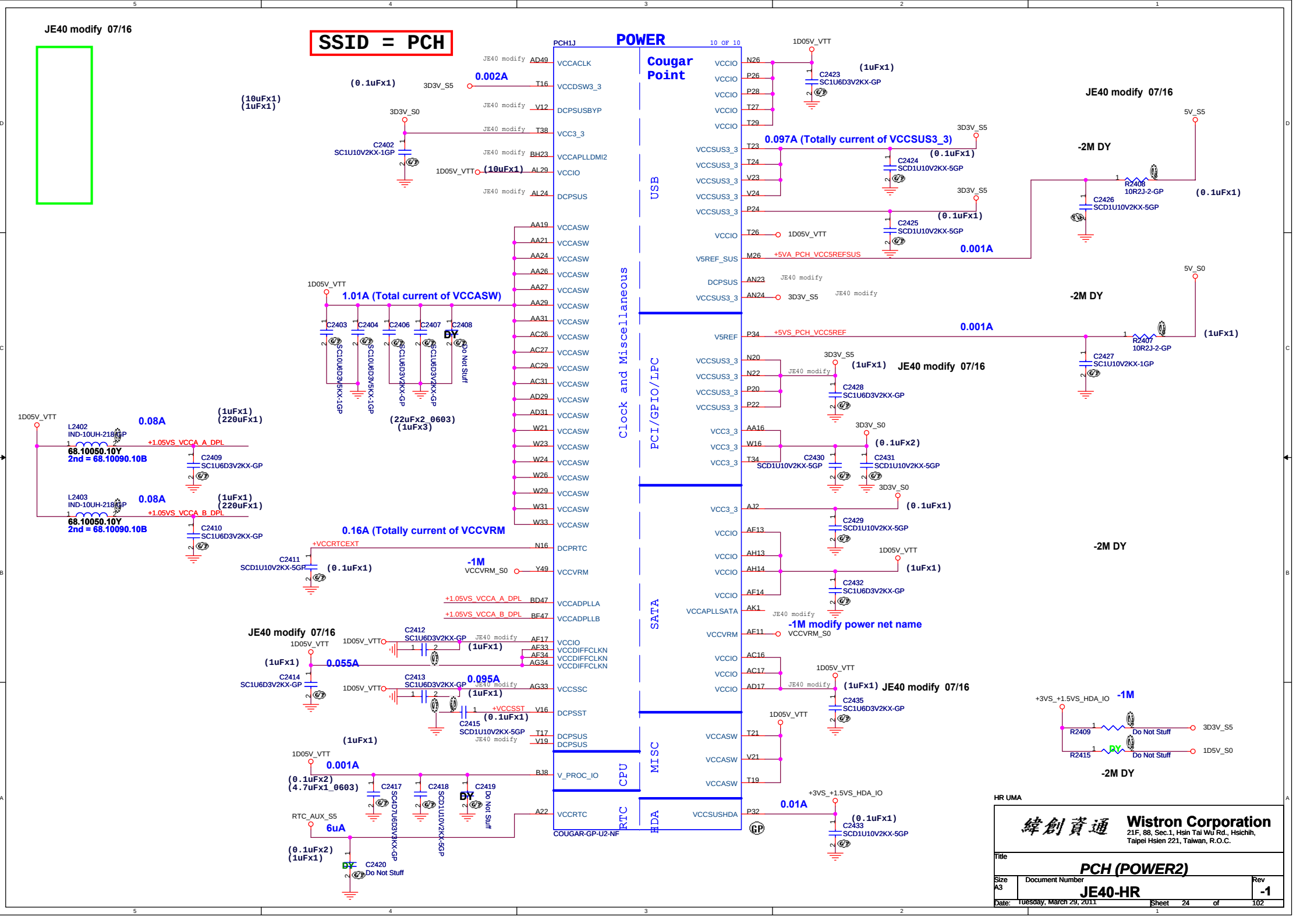
Date: Tuesday, March 29, 2011 | Sheet 22 of 102

SSID = PCH 6A

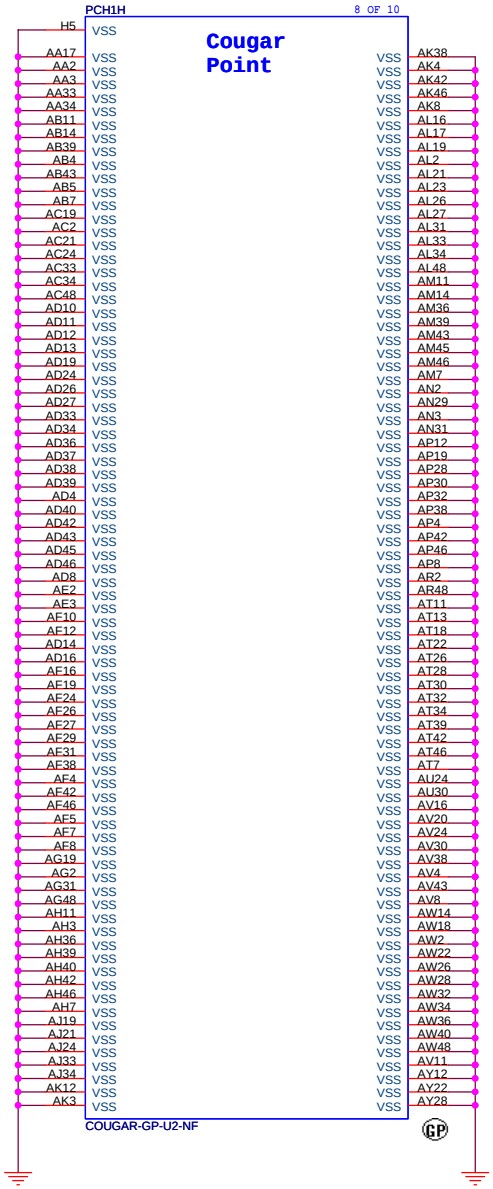


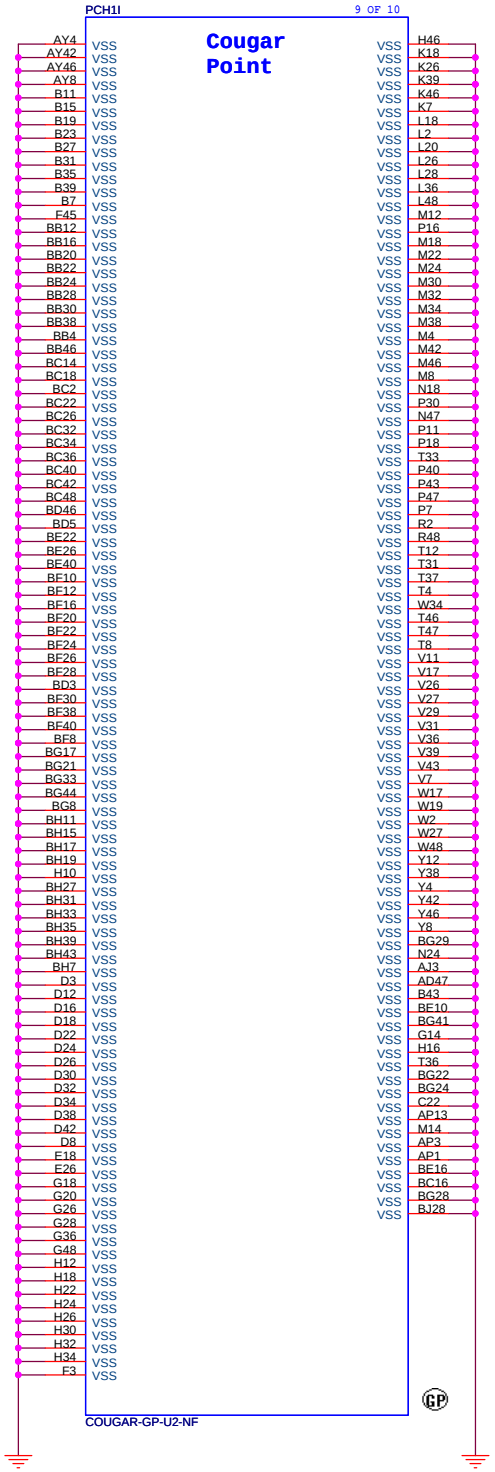
HR UMA

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	PCH (POWER1)	
Size A3	Document Number JE40-HR	Rev -1
Date: Tuesday, March 29, 2011	Sheet 23 of 102	


JE40 modify 07/16
SSID = PCH
PCH1J
POWER
10 OF 10
Cougar Point
USB
Clock and Miscellaneous
PCI/GPIO/LPC
SATA
MISC
CPU
RTC
HDA
COUGAR-GP-U2-NF
0.002A
(0.1uFx1)
(10uFx1)
(1uFx1)
3D3V_S5
3D3V_S0
C2402
SC1U10V2KX-1GP
1D05V_VTT
(10uFx1)
1.01A (Total current of VCCASW)
C2403
C2404
C2406
C2407
C2408
DY
Do Not Stuff
(22uFx2_0603)
(1uFx3)
1D05V_VTT
L2402
IND-10UH-218GP
0.08A
(1uFx1)
(220uFx1)
+1.05VS_VCCA_A_DPL
68.10050.10Y
2nd = 68.10090.10B
C2409
SC1U6D3V2KX-GP
L2403
IND-10UH-218GP
0.08A
(1uFx1)
(220uFx1)
+1.05VS_VCCA_B_DPL
68.10050.10Y
2nd = 68.10090.10B
C2410
SC1U6D3V2KX-GP
0.16A (Totally current of VCCVRM
+VCCRTCEXT
C2411
SCD1U10V2KX-5GP
(0.1uFx1)
-1M
VCCVRM_S0
+1.05VS_VCCA_A_DPL
+1.05VS_VCCA_B_DPL
JE40 modify 07/16
C2412
SC1U6D3V2KX-GP
(1uFx1)
0.055A
C2414
SC1U6D3V2KX-GP
C2413
SC1U6D3V2KX-GP
0.095A
(1uFx1)
+VCCSST
(0.1uFx1)
C2415
SCD1U10V2KX-5GP
(1uFx1)
0.001A
(0.1uFx2)
(4.7uFx1_0603)
C2417
C2418
C2419
DY
Do Not Stuff
RTC_AUX_S5
6uA
(0.1uFx2)
(1uFx1)
C2420
Do Not Stuff
0.097A (Totally current of VCCSUS3_3)
(0.1uFx1)
C2424
SCD1U10V2KX-5GP
C2425
SCD1U10V2KX-5GP
0.001A
+5VA_PCH_VCC5REFSUS
JE40 modify 07/16
-2M DY
R2408
10R2J-2-GP
(0.1uFx1)
C2426
SCD1U10V2KX-5GP
0.001A
+5VS_PCH_VCC5REF
R2407
10R2J-2-GP
(1uFx1)
C2427
SC1U10V2KX-1GP
(1uFx1)
C2428
SC1U6D3V2KX-GP
(0.1uFx2)
C2430
SCD1U10V2KX-5GP
C2431
SCD1U10V2KX-5GP
(0.1uFx1)
C2429
SCD1U10V2KX-5GP
(1uFx1)
C2432
SC1U6D3V2KX-GP
-1M modify power net name
VCCVRM_S0
(1uFx1) JE40 modify 07/16
C2435
SC1U6D3V2KX-GP
+3VS_+1.5VS_HDA_IO
-1M
R2409
Do Not Stuff
R2415
DY
Do Not Stuff
0.01A
(0.1uFx1)
C2433
SCD1U10V2KX-5GP
HR UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (POWER2)
Size
A3
Document Number
JE40-HR
Rev
-1
Date: Tuesday, March 29, 2011
Sheet 24 of 102

SSID = PCH





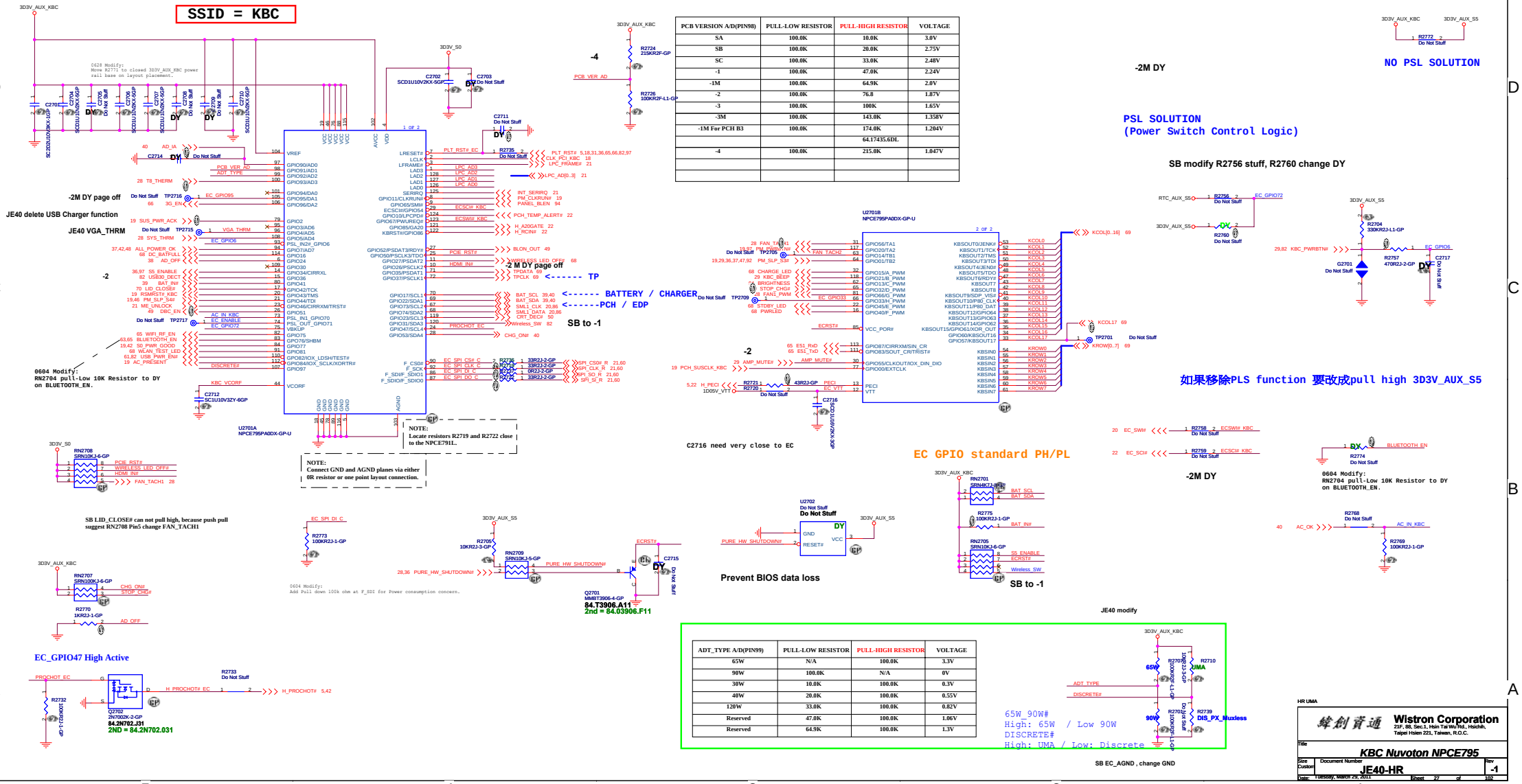
HR UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***PCH (VSS)***	
Size A3	Document Number **JE40-HR**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 25 of 102	

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***Clock(colay)***	
Size A4	Document Number **JE40-HR**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 26 of 102	



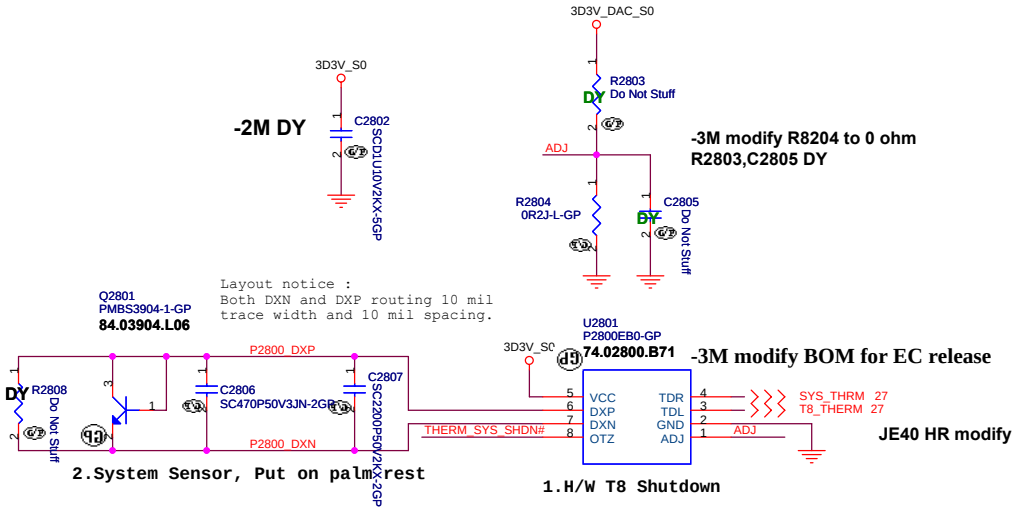
PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
-1	100.0K	47.0K	2.24V
-1M	100.0K	64.9K	2.0V
-2	100.0K	76.8	1.87V
-3	100.0K	100K	1.65V
-3M	100.0K	143.0K	1.358V
-1M For PCH B3	100.0K	174.0K	1.204V
		64.17435.6DL	
-4	100.0K	215.0K	1.047V

ADT_TYPE A/D(PIN99)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
65W	N/A	100.0K	3.3V
90W	100.0K	N/A	0V
30W	10.0K	100.0K	0.3V
40W	20.0K	100.0K	0.55V
120W	33.0K	100.0K	0.82V
Reserved	47.0K	100.0K	1.06V
Reserved	64.9K	100.0K	1.3V

Document Number: JE40-HR
Rev: -1
Date: TUESDAY, MARCH 29, 2011
Sheet 27 of 102

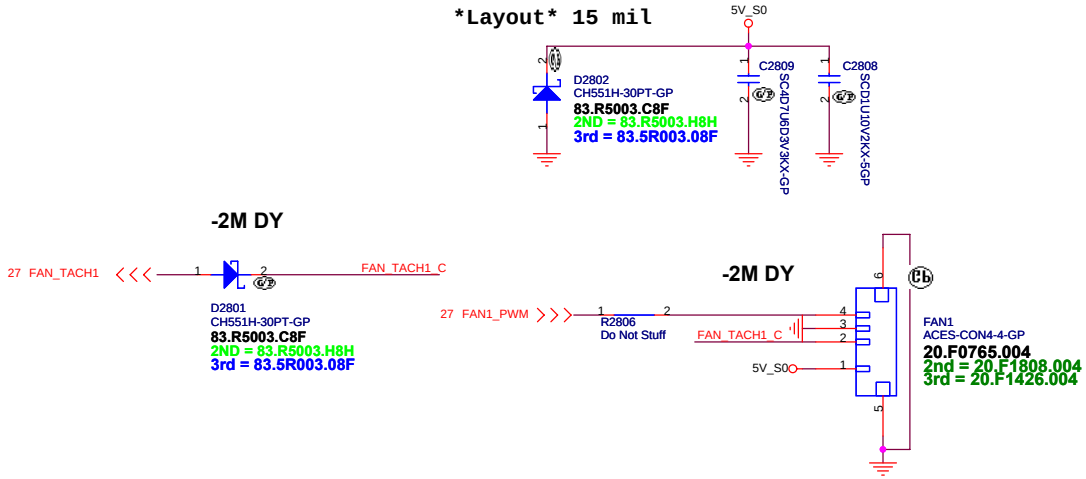
SSID = Thermal

Thermal sensor P2800



Fan controller P2793

Layout 15 mil



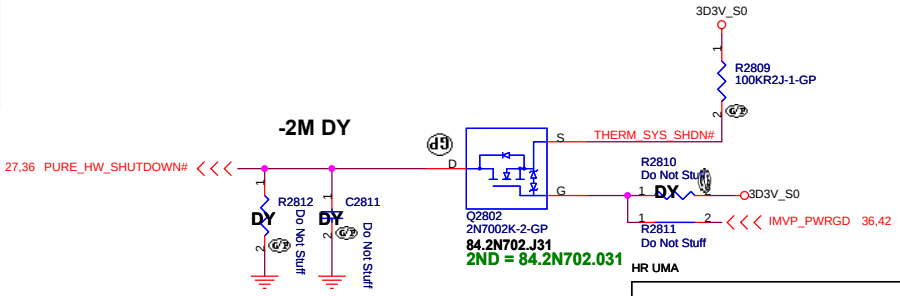
For PWM FAN

ADJ Table (Reference to SYNTON-TECH Metal Film Resistor E-96 ±1% Series)

RADJ1 (KΩ)	RADJ2 (KΩ)	VADJ (V)	OTZ Threshold Temperature (°C)
124	226	2.13	101
118	226	2.17	96.3
113	226	2.20	92.1
110	226	2.22	89.6
107	226	2.24	87
105	226	2.25	85.3
100	226	2.29	80.9

VGA Thermal sensor P2800

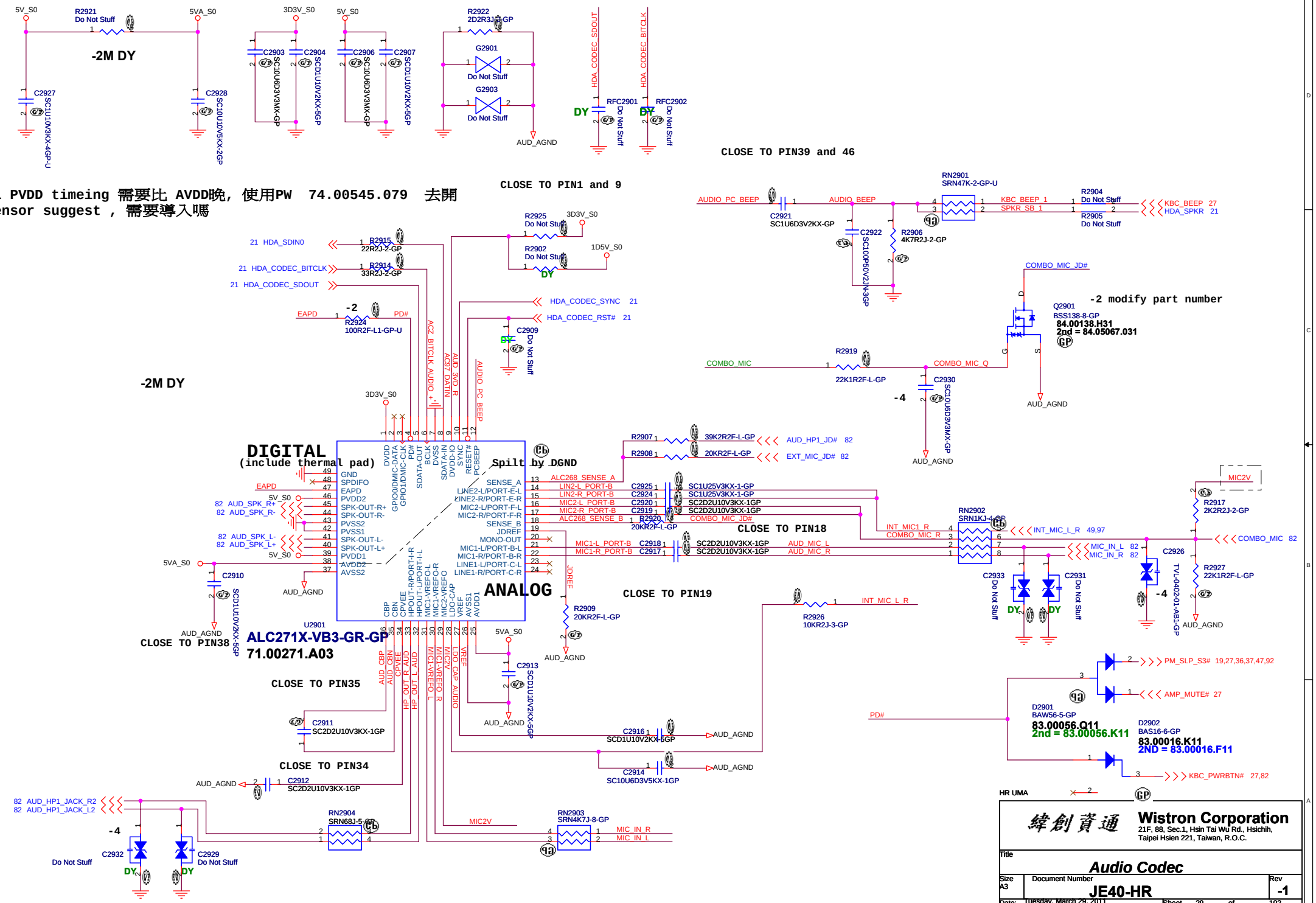
SMBUS modify to Page 84



HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Thermal P2800/Fan Controllor P2793		
Size: Custom	Document Number: JE40-HR	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 28 of 102	


-1 PVDD timeing 需要比 AVDD晚, 使用PW 74.00545.079 去開
vensor suggest , 需要導入嗎
-2M DY
CLOSE TO PIN1 and 9
CLOSE TO PIN39 and 46
-2 modify part number
DIGITAL
(include thermal pad)
Spilt by DGND
ANALOG
CLOSE TO PIN18
CLOSE TO PIN19
CLOSE TO PIN38
CLOSE TO PIN35
CLOSE TO PIN34
U2901
ALC271X-VB3-GR-GP
71.00271.A03
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Audio Codec
Size A3
Document Number
JE40-HR
Rev -1
Date: Tuesday, March 29, 2011
Sheet 29 of 102

AUDIO OP AMPLIFIER

JE40 delete AMP function

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Audio AMP	
Size A4	Document Number JE40-HR	Rev -1
Date: Tuesday, March 29, 2011	Sheet 30 of 102	

SB modify L3101,2,4,5,6 to 0 ohm

SB modify R3102 DY, R3104 to pull low

SB mmodify vendor suggest

SB delete EEPROM

128K byte

SB delete R3112

SB delete R3117

SB delete R3129 for LDO power

Card-reader Off-Page

Check VDDO_CR power plan

SB for B version

SB for B version can no use LDO delete LDO

SB to -1 modify to short pad

SB C3134, C3135 change 15P

10月底改打71.57785.M03

U3101 BCM57785XA0KMLG-GP
71.57785.M02
Change:71.57785.M03

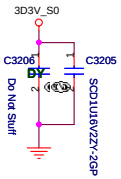
HR UMA

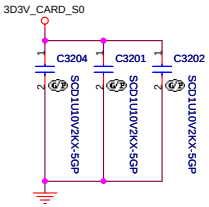
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: BCM57780

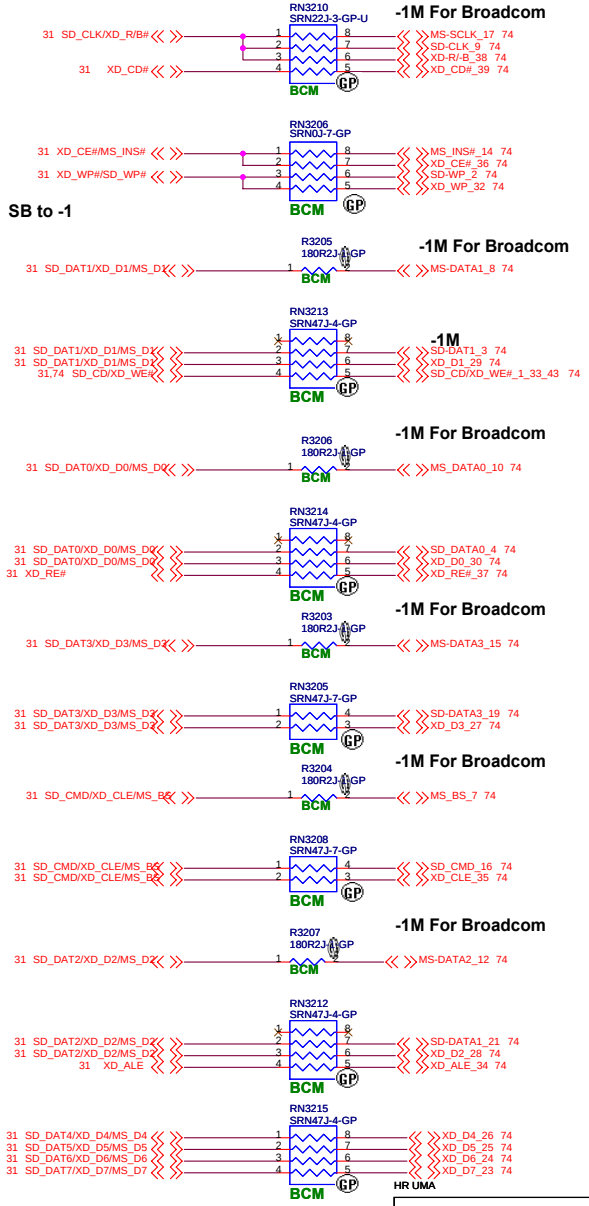
Size: Custom | Document Number: JE40-HR | Rev: -1

Date: Tuesday, March 29, 2011 | Sheet 31 of 102





Near CARD1 Pin11, Pin18, Pin22



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***RTS5159 (CARD READER)***	
Size: Custom	Document Number: **JE40-HR**	Rev: **-1**
Date: Tuesday, March 29, 2011	Sheet 32 of 102	

(Blanking)

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Tuesday, March 29, 2011 Sheet 33 of 102

(Blanking)

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Tuesday, March 29, 2011 Sheet 34 of 102

HR UMA

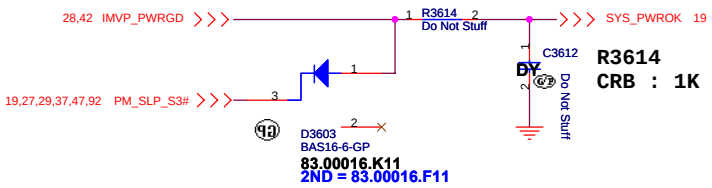
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

USB 3.0 Controller

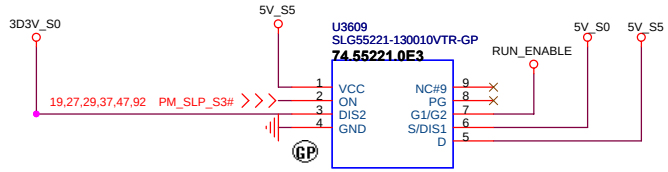
Size	Document Number	Rev
A3	JE40-HR	-1

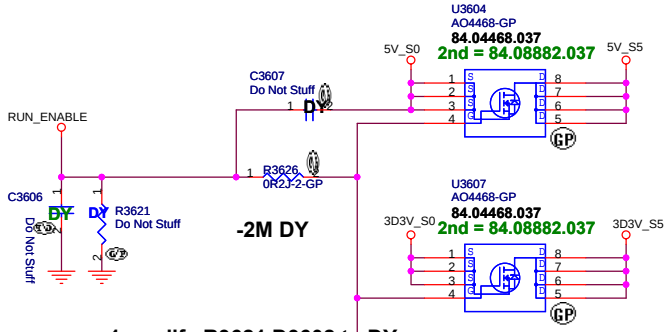
Power Sequence



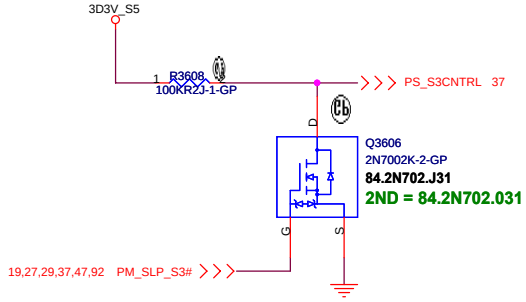
R3614
CRB : 1K

ANNIE Run Power



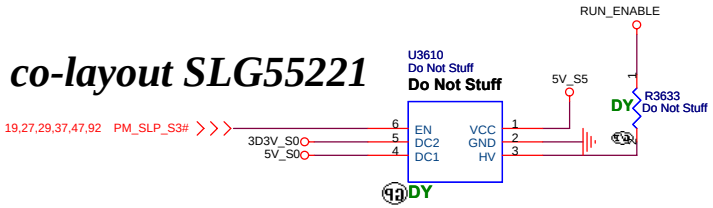


-1 modify R3621,D3602 to DY



SB modify part number

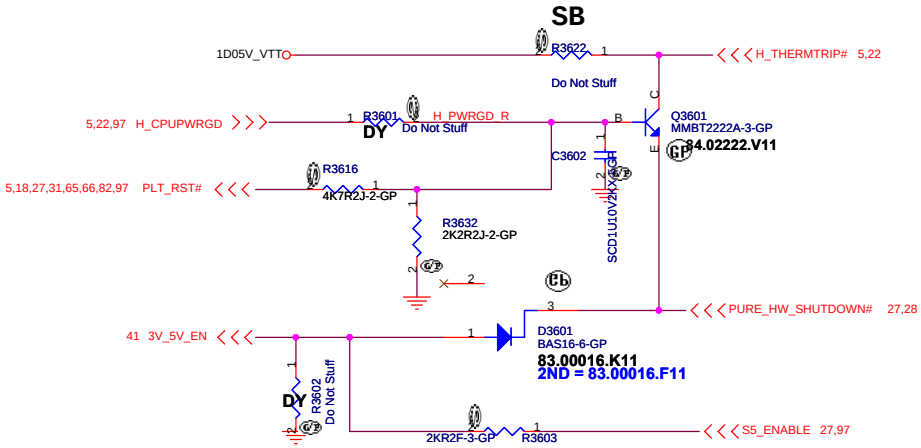
-1 co-layout SLG55221



1D5V_S0

MAX Current 3000 mA
Design Current 2100 mA
Total= 11.39A

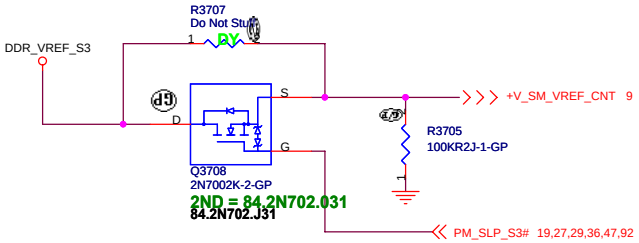
SB



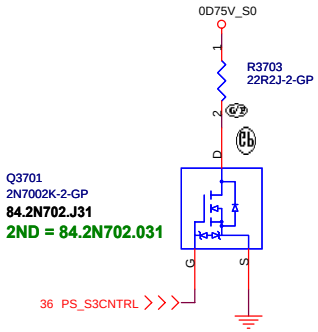
HR UMA

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Power Plane Enable	
Size A3	Document Number JE40-HR	Rev -1
Date: Tuesday, March 29, 2011	Sheet 36 of 102	

Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation



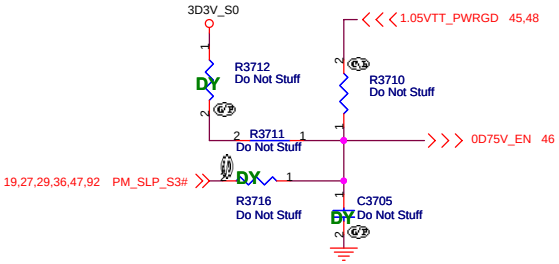
Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



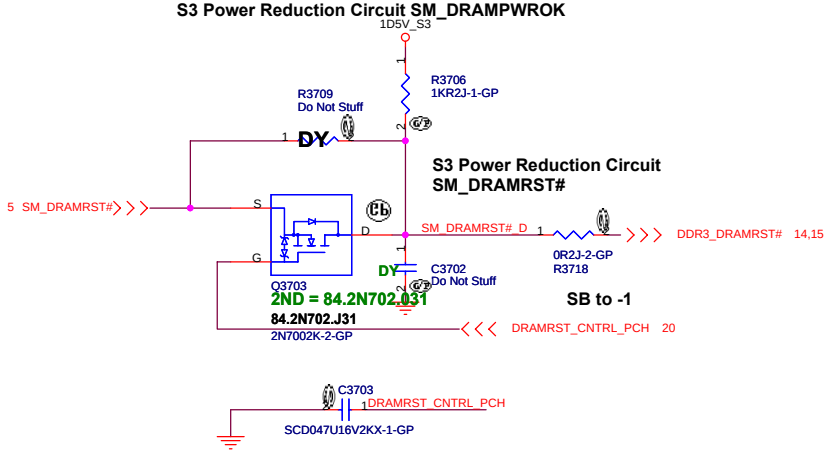
5 S3 Power Reduction X01 20091111 JE40 HR modify 驗證R3710上件

SB to -1 reserve R3723

-2M DY

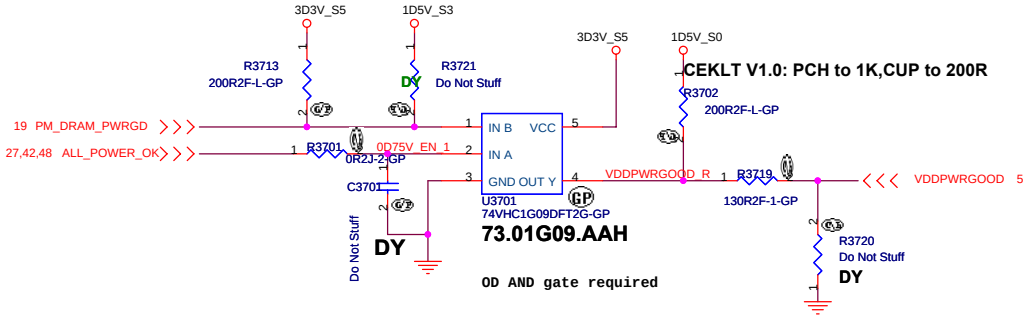


Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



SB

Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



OD AND gate required

For U3701 not OD AND gate
R3719 to 64.15015.6DL
R3720 to 64.75005.6DL
R3702 to DY

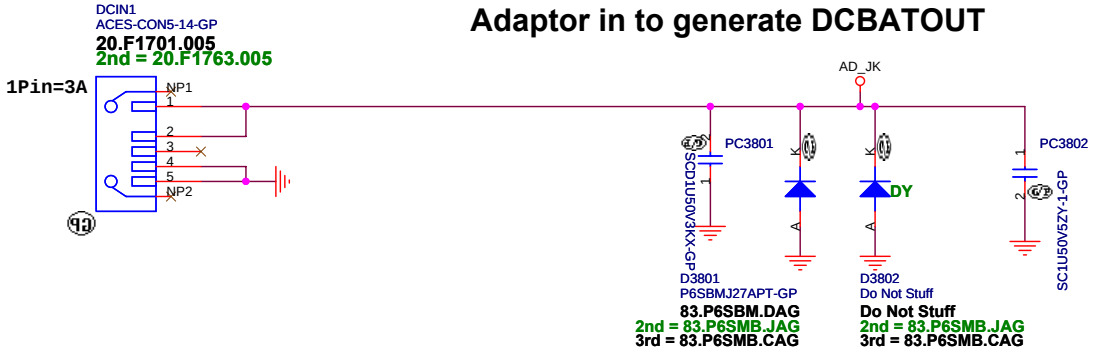
SM_DRAMPWROK must have a maximum of 15ns rise or fall time
over VDDQ * 0.55± 200mV and the edge must be monotonic

HR UMA

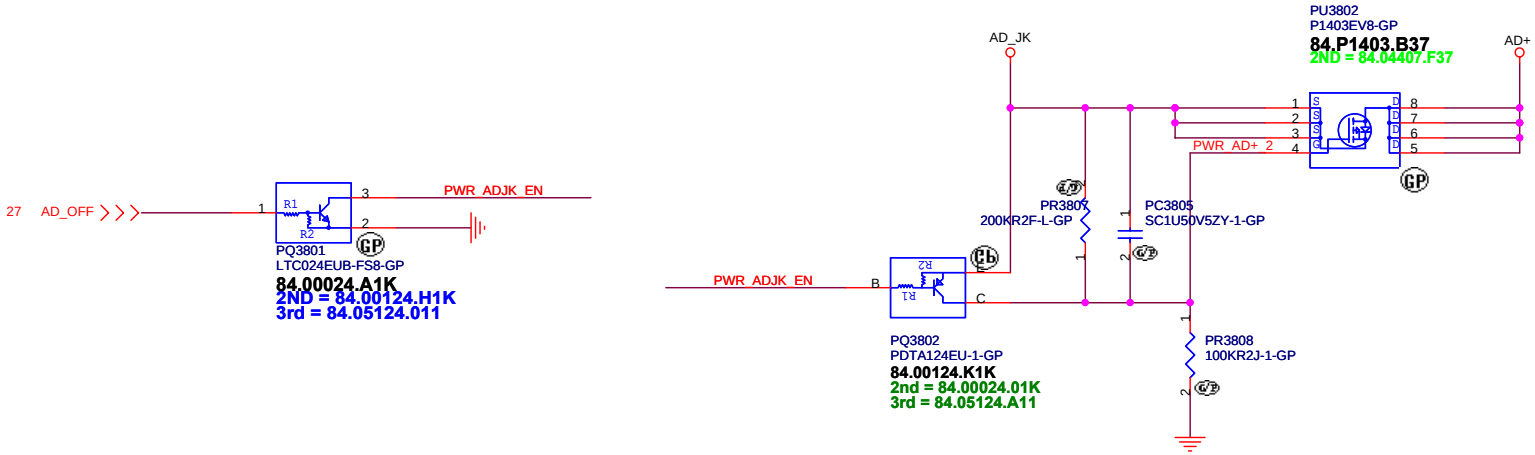
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	ADAPTER	
Size A3	Document Number JE40-HR	Rev -1
Date: Tuesday, March 29, 2011	Sheet 37 of 102	

ANNIE solution

Adaptor in to generate DCBATOUT



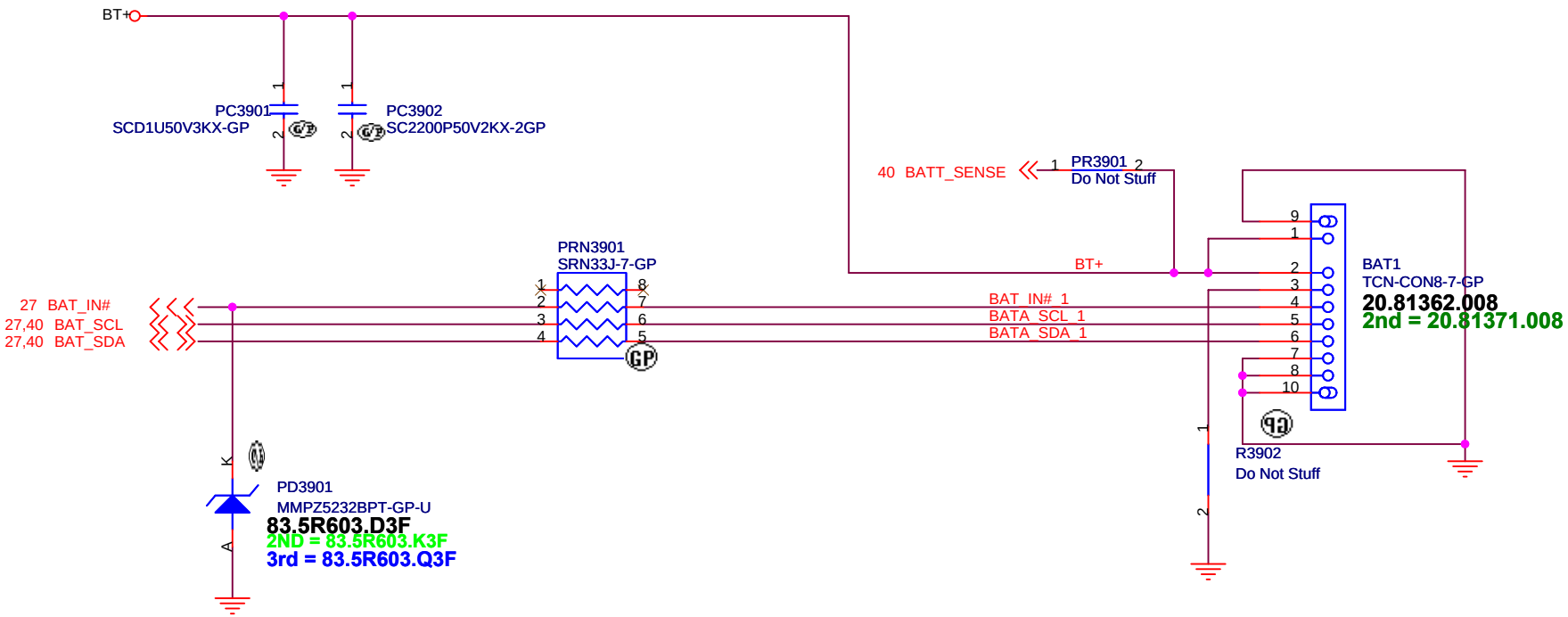
JE40 change DCIN1 part number



HR UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***DCIN JACK***	
Size Custom	Document Number **JE40-HR**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 38 of 102	

BATTERY CONNECTOR



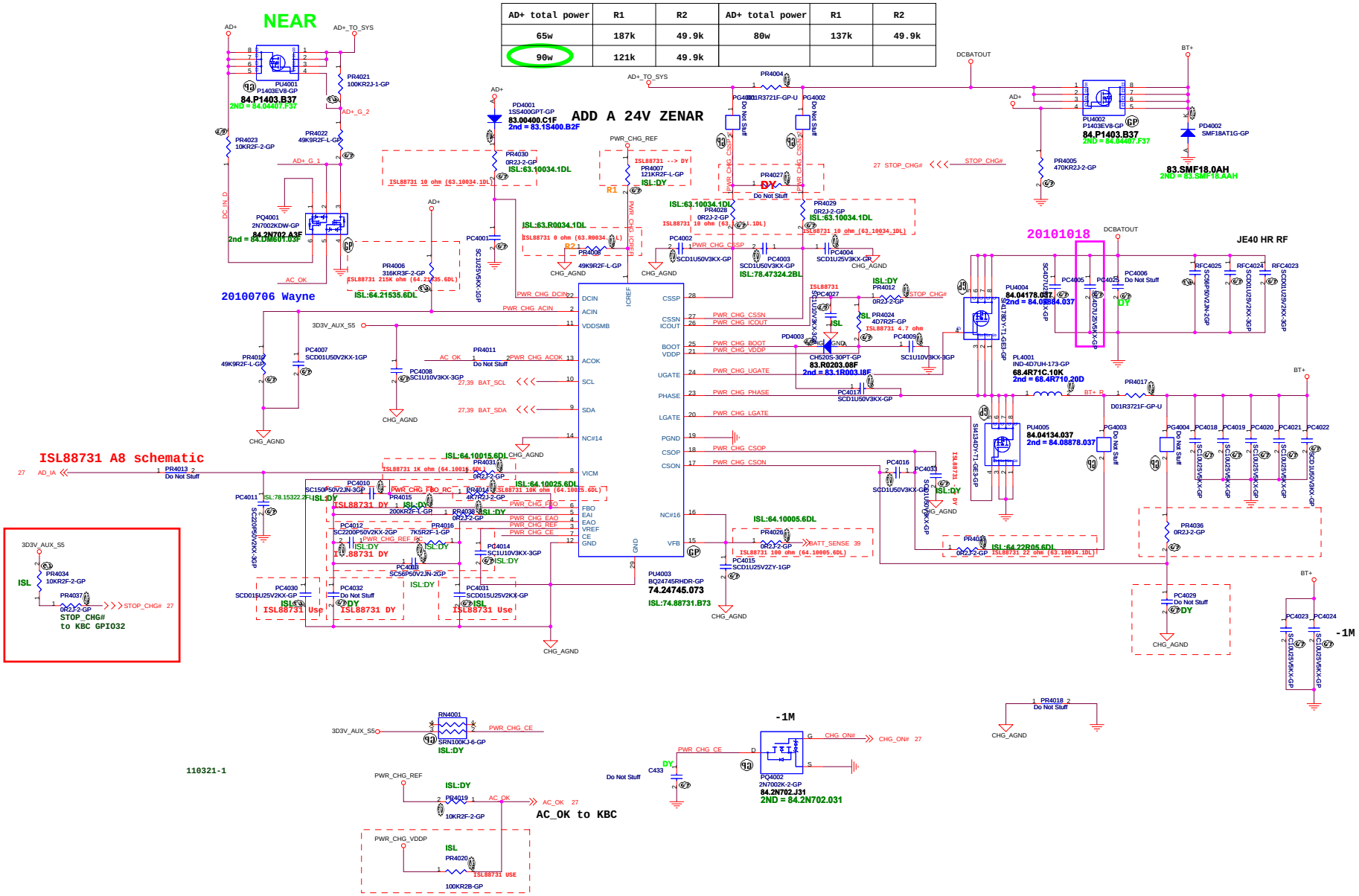
EC Protect

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
BATT CONN		
Size A4	Document Number **JE40-HR**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 39 of 102	

AD+ total power	R1	R2	AD+ total power	R1	R2
65w	187k	49.9k	80w	137k	49.9k
90w	121k	49.9k			

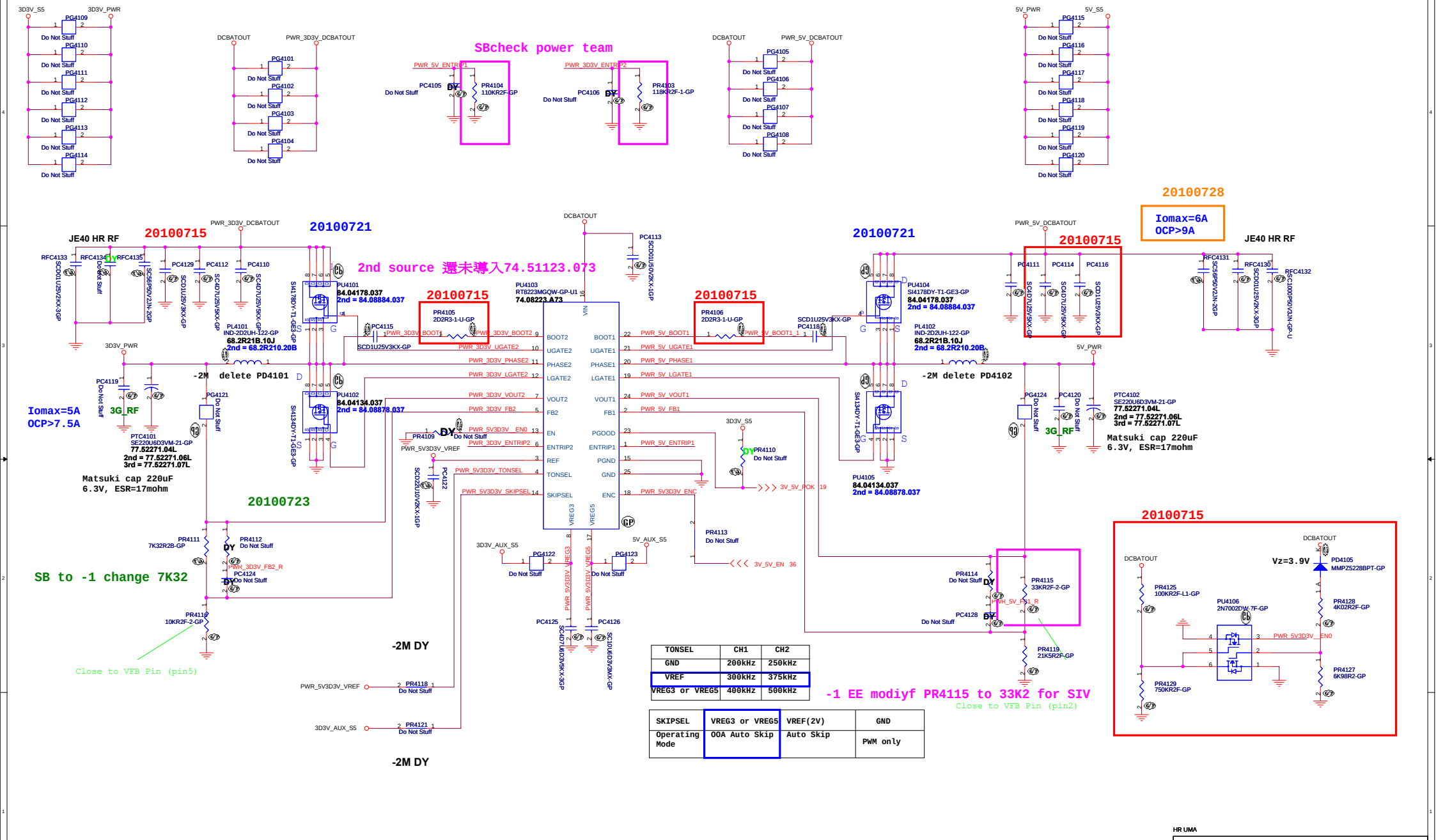


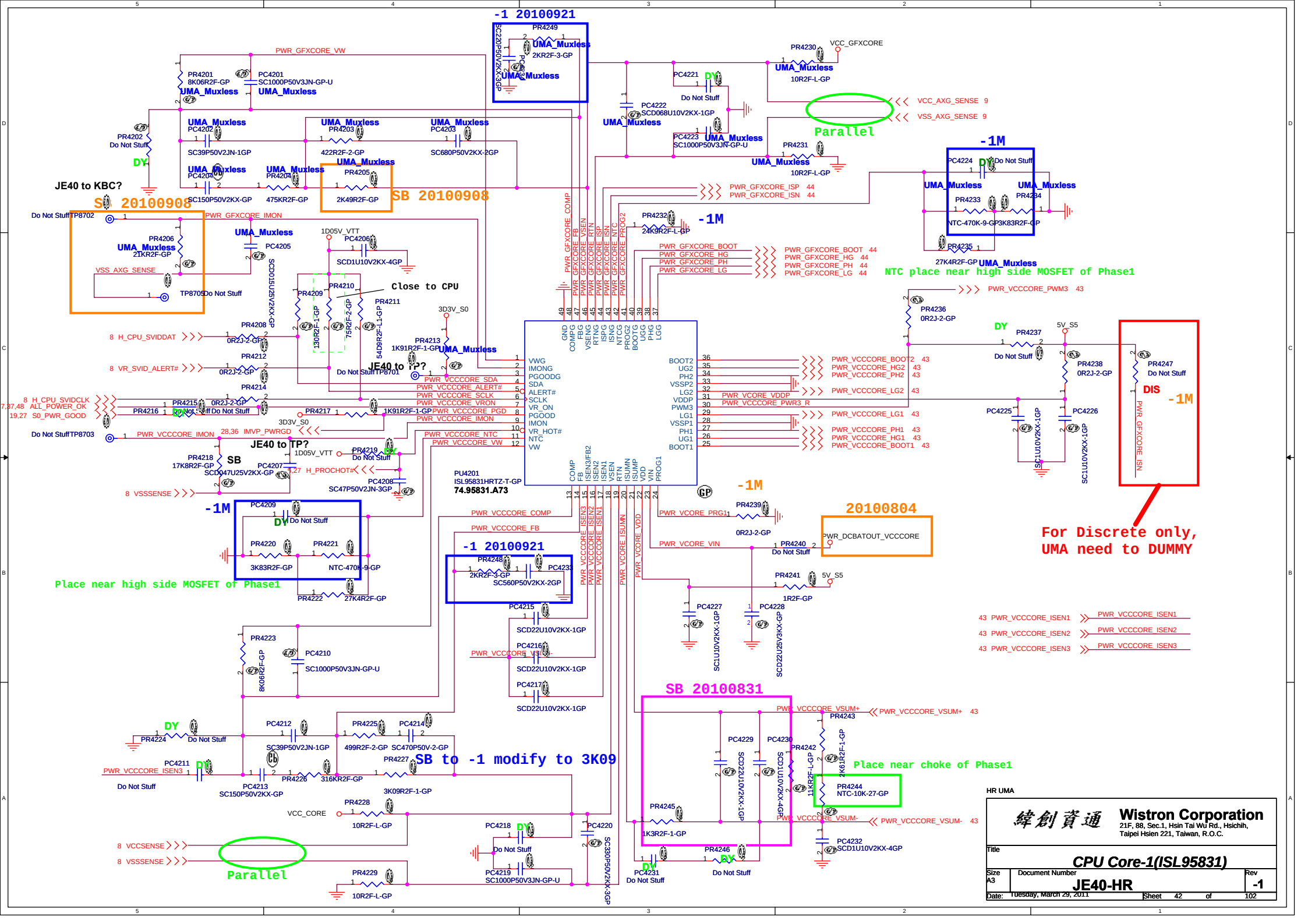
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

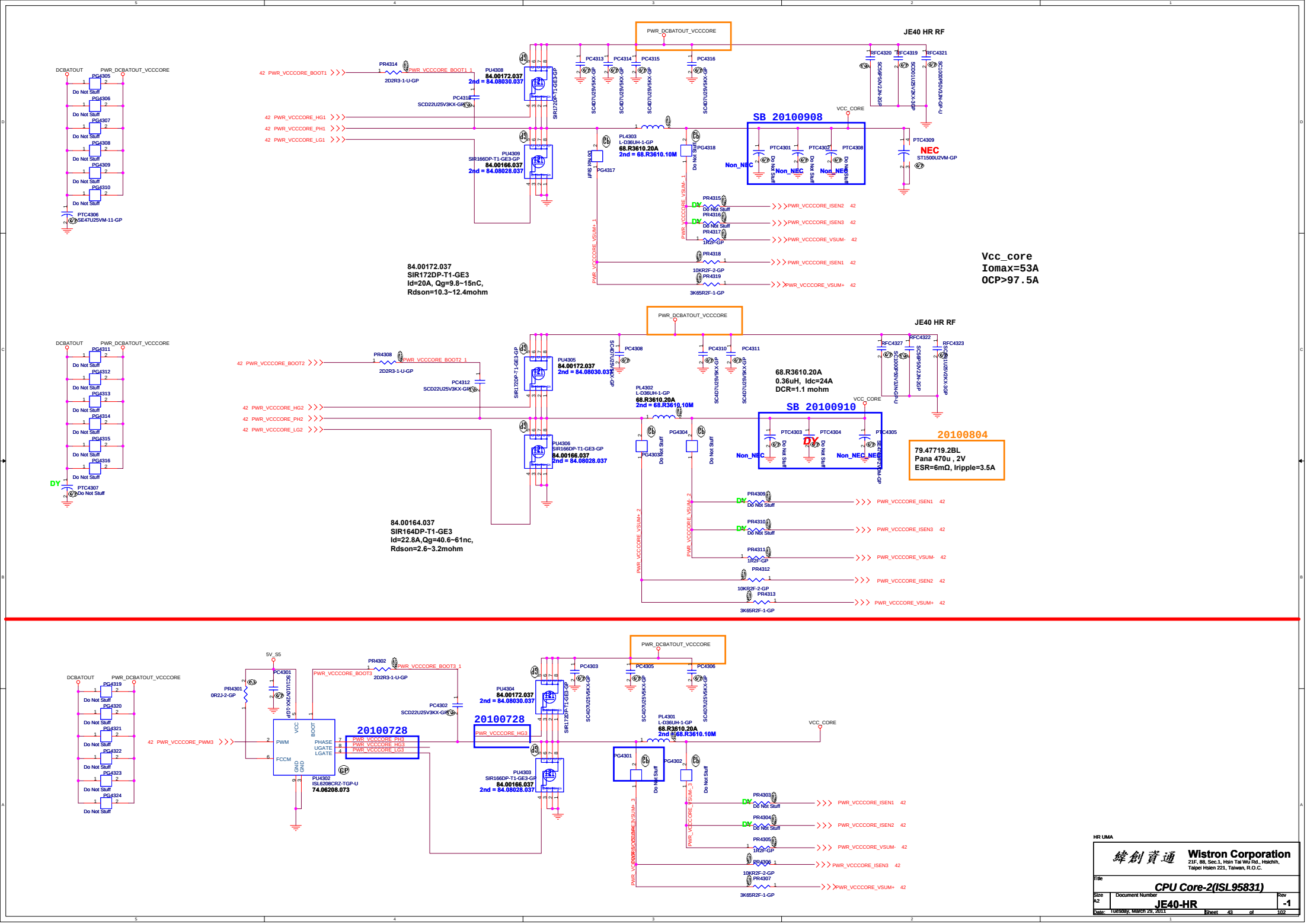
Title: CHARGER BQ24745

Size: A2 | Document Number: JE40-HR | Rev: -1

Date: Tuesday, March 29, 2011 | Sheet 40 of 102


SBcheck power team
20100715
20100721
20100723
20100728
JE40 HR RF
3G_RF
2nd source 還未導入74.51123.073
Iomax=6A
OCP>9A
Iomax=5A
OCP>7.5A
-2M delete PD4101
-2M delete PD4102
Matsuki cap 220uF
6.3V, ESR=17mohm
SB to -1 change 7K32
Close to VFB Pin (pin5)
-2M DY
-1 EE modiyf PR4115 to 33K2 for SIV
Close to VFB Pin (pin2)
PU4103
RT8223MGQW-GP-U1
74.08223.A73
PU4101
84.04178.037
2nd = 84.08884.037
PU4102
84.04134.037
2nd = 84.08878.037
PU4104
SI4178DY-T1-GE3-GP
84.04178.037
2nd = 84.08884.037
PU4105
84.04134.037
2nd = 84.08878.037
PU4106
2N7002DW-7F-GP
PD4105
MMPZ5228BPT-GP
Vz=3.9V
PR4105
2D2R3-1-U-GP
PR4106
2D2R3-1-U-GP
PL4101
IND-2D2UH-122-GP
68.2R21B.10J
2nd = 68.2R210.20B
PL4102
IND-2D2UH-122-GP
68.2R21B.10J
2nd = 68.2R210.20B
PTC4101
SE220U6D3VM-21-GP
77.52271.04L
2nd = 77.52271.06L
3rd = 77.52271.07L
PTC4102
SE220U6D3VM-21-GP
77.52271.04L
2nd = 77.52271.06L
3rd = 77.52271.07L
PR4111
7K32R2B-GP
PR4112
10KR2F-2-GP
PR4115
33KR2F-2-GP
PR4119
21K5R2F-GP
PR4125
100KR2F-L1-GP
PR4128
4K02R2F-GP
PR4127
6K98R2-GP
PR4129
750KR2F-GP
PR4104
110KR2F-GP
PR4103
118KR2F-1-GP
PR4118
PR4121
PR4122
PR4124
PR4109
PR4110
PR4113
PR4114
PR4128
PR4130
PR4131
PR4132
PR4133
PR4134
PR4135
PR4136
PR4137
PR4138
PR4139
PR4140
PR4141
PR4142
PR4143
PR4144
PR4145
PR4146
PR4147
PR4148
PR4149
PR4150
PR4151
PR4152
PR4153
PR4154
PR4155
PR4156
PR4157
PR4158
PR4159
PR4160
PR4161
PR4162
PR4163
PR4164
PR4165
PR4166
PR4167
PR4168
PR4169


-1 20100921
SB 20100908
JE40 to KBC?
Do Not Stuff TP8702
TP8705 Do Not Stuff
Close to CPU
JE40 to TP?
Do Not Stuff TP8701
Do Not Stuff TP8703
SB
-1M
Place near high side MOSFET of Phase1
PU4201
ISL95831HRTZ-T-GP
74.95831.A73
20100804
PWR_DCBATOUT_VCCCORE
For Discrete only,
UMA need to DUMMY
SB 20100831
SB to -1 modify to 3K09
Place near choke of Phase1
Parallel
NTC place near high side MOSFET of Phase1
DIS
VCC_GFXCORE
VCC_AXG_SENSE 9
VSS_AXG_SENSE 9
PWR_GFXCORE_ISP 44
PWR_GFXCORE_ISN 44
PWR_GFXCORE_BOOT 44
PWR_GFXCORE_HG 44
PWR_GFXCORE_PH 44
PWR_GFXCORE_LG 44
PWR_VCCCORE_PWM3 43
PWR_VCCCORE_BOOT2 43
PWR_VCCCORE_HG2 43
PWR_VCCCORE_PH2 43
PWR_VCCCORE_LG2 43
PWR_VCCCORE_LG1 43
PWR_VCCCORE_PH1 43
PWR_VCCCORE_HG1 43
PWR_VCCCORE_BOOT1 43
43 PWR_VCCCORE_ISEN1
43 PWR_VCCCORE_ISEN2
43 PWR_VCCCORE_ISEN3
PWR_VCCCORE_VSUM+ 43
PWR_VCCCORE_VSUM- 43
8 H_CPU_SVIDDAT
8 VR_SVID_ALERT#
8 H_CPU_SVIDCLK
7,37,48 ALL_POWER_OK
19,27 S0_PWR_GOOD
8 VSSSENSE
8 VCCSENSE
VCC_CORE
HR UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU Core-1(ISL95831)
Size A3
Document Number
JE40-HR
Rev -1
Date: Tuesday, March 29, 2011
Sheet 42 of 102



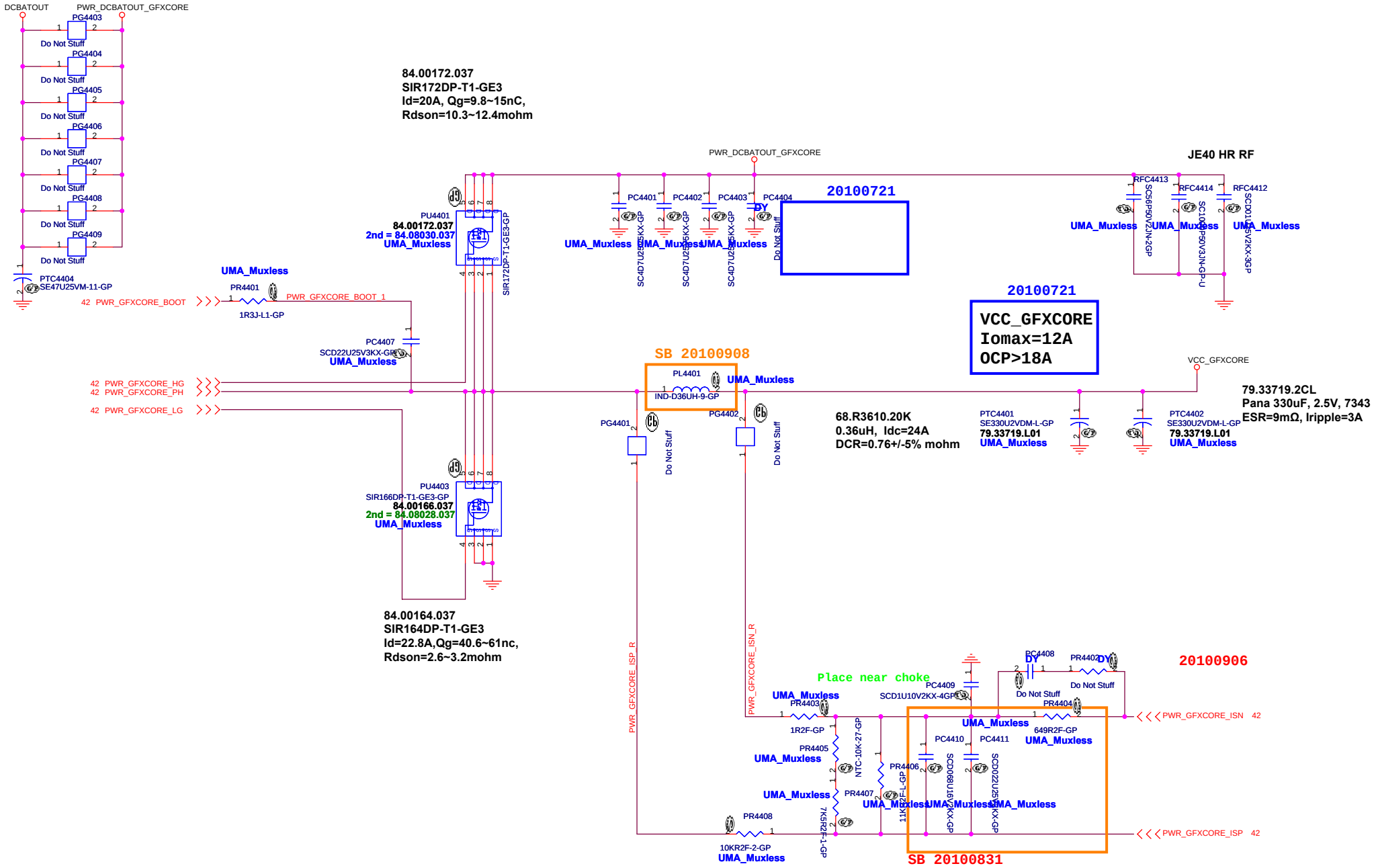
HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CPU Core-2(ISL95831)*

Size	Document Number	Rev
A2	JE40-HR	-1

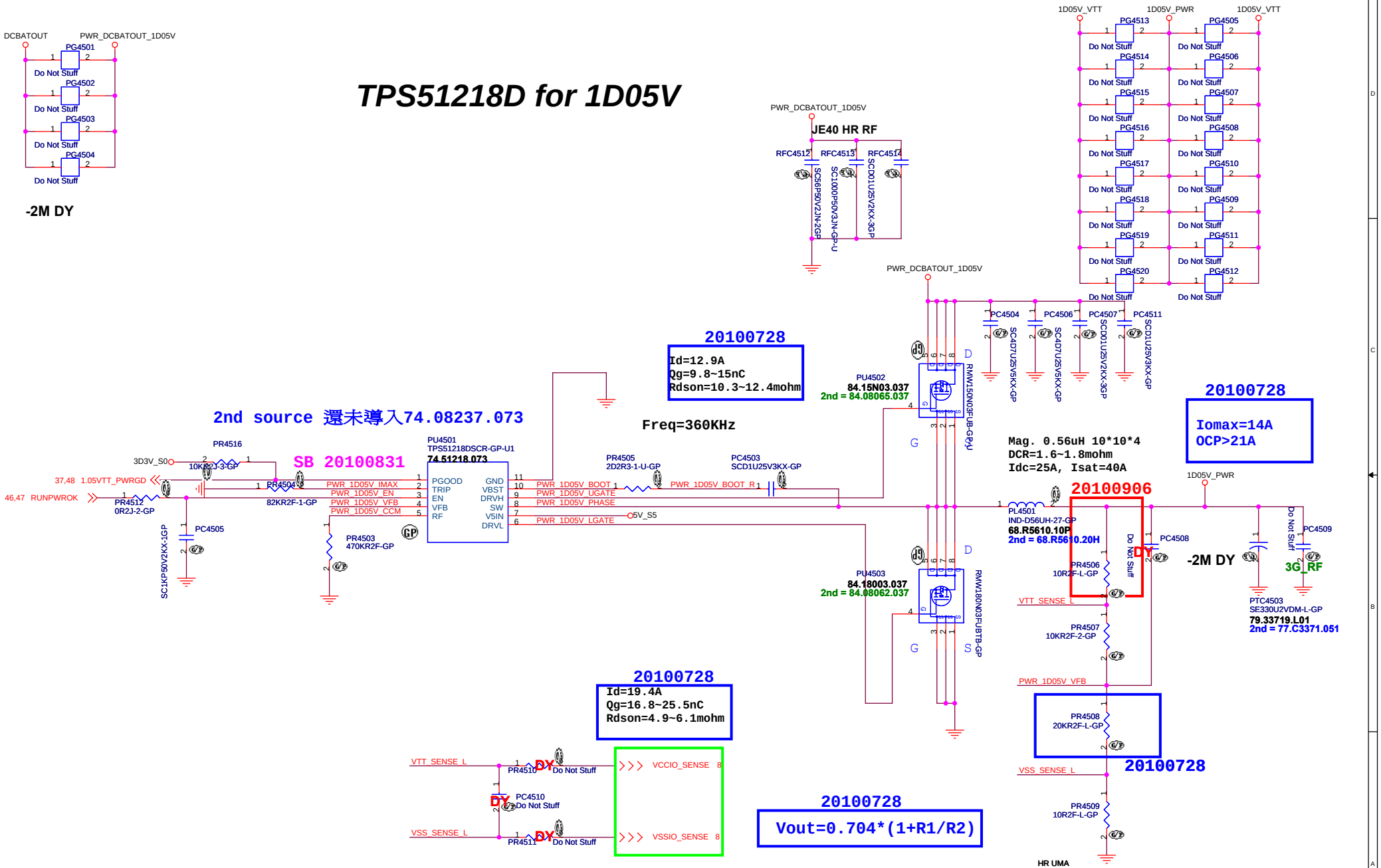
Date: Tuesday, March 29, 2011 Sheet 43 of 102



HR UMA

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	CPU Core-3(ISL95831)	
Size A3	Document Number JE40-HR	Rev -1
Date: Tuesday, March 29, 2011	Sheet 44 of 102	

TPS51218D for 1D05V



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC 1D05V(TPS51218D)

Size: A3 | Document Number: JE40-HR | Rev: -1

Date: Tuesday, March 29, 2011 | Sheet 45 of 102

SSID = PWR.Plane.Regulator_1p5v0p75v

20100805

RT8207L for 1D5V

DCBATOUT PWR_DCBATOUT_1D5V
PG4601 Do Not Stuff
PG4602 Do Not Stuff
PG4603 Do Not Stuff
PG4604 Do Not Stuff
PTC4601 Do Not Stuff
DY

19,27 PM_SLP_S4# PR4612 Do Not Stuff PWR_1D5V_EN
PC4612 Do Not Stuff
DY

SB 20100831

PWR_1D5V_VCC5 PR4604 5D1R2F-GP 5V_S5
PC4606 SC1U10V2KX-1GP
PC4602 SC1K50V2KX-1GP
PR4603 12K4R2F-GP
PWR_1D5V_VDDP PR4605 Do Not Stuff 5V_S5
C694 SC1U10V2KX-1GP
PWR_1D5V_CS

3D3V_S5 PR4602 10KR2F-2-GP

Close to pin23

45,47 RUNPWROK
PWR_DCBATOUT_1D5V PR4610 620KR2F-GP PWR_1D5V_TON
20100728
PWR_1D5V_EN
PWR_0D75V_EN
PWR_1D5V_VTTIN
1D5V_S3 PG4605 Do Not Stuff
PG4606 Do Not Stuff
PC4603 SC10U6D3V5MX-3GP
1D5V_S3 PG4607 Do Not Stuff
PWR_1D5V_VDDQ
DDR_VREF_PWR

Close to pin23

20100728
Iomax=1A
OCP>1.5A

Close to output cap pin1, not inside of the output cap

CS VDD VDDP
PGOOD TON S5 S3 VLDOIN NC#7 VTTGND MODE VTT VTTSNS GND GND
BOOT UGATE PHASE LGATE PGND NC#17 VDDQ FB DEM VTTREF
PWR_1D5V_BOOT PWR_1D5V_UGATE PWR_1D5V_PHASE PWR_1D5V_LGATE PWR_1D5V_VDDQ PWR_1D5V_FB 5V_S5

PU4601
RT8207LGQW-GP-U1
74.08207.B73

2nd source 還未導入74.51116.073

PWR_1D5V_VTTREF PR4607 Do Not Stuff DDR_VREF_S3
PC4608 SCD033U16V2KX-GP

SB
PR4606 2D2R3-1-U-GP
PC4609 SCD1U25V3KX-GP

20100728
Id=12.9A
Qg=9.8~15nC
Rdson=10.3~12.4mohm

PU4602
84.15N03.037
2nd = 84.08065.037

-1 PR4608 需要將來都改32K4R

R1 PR4608 33KR2F-GP DY PC4610 Do Not Stuff
R2 PR4609 30KR2F-GP

Close to PIN9

PWR_DCBATOUT_1D5V
JE40 HR RF
RFC4617 SC10U25V2KX-3GP
RFC4618 SC10U0P5V3JN-GP-U
RFC4616 SC5P50V2JN-2GP

PWR_DCBATOUT_1D5V
20100906
PC4611 SC4D7U25V5KX-GP
PC4614 SC4D7U25V5KX-GP
PC4616 SC4D7U25V5KX-GP
PC4617 SC4D7U25V5KX-GP
PC4615 SCD1U25V3KX-GP

PU4603
84.18003.037
2nd = 84.08052.037

Mag. 1.0uH 10*10*4
DCR=2.9~3.3mohm
Idc=18A, Isat=36A

Iomax=12A
OCP>20A

1D5V_S3
PL4601 IND-1UH-93-GP
68.1R01B.10J
2nd = 68.1R01C.10Q
PC4613 Do Not Stuff DY
PTC4602 SE390U2D5VM-7GP
79.3971V.30L
2nd = 79.3971V.6AL
Matsuki cap 390uF
2.5V, ESR=10mohm

20100728
Id=19.4A
Qg=16.8~25.5nC
Rdson=4.9~6.1mohm

Vout=0.75*(1+R1/R2)

SB R4608 chekc 修改31K6R
Vout 需再1.55V 以上

+0.75VS
Iomax: 1.2A

0D75V_S0 PG4608 Do Not Stuff DDR_VREF_PWR
PG4609 Do Not Stuff
PC4604 SC10U6D3V5MX-3GP
PC4605 Do Not Stuff
DY

37 0D75V_EN PR4615 Do Not Stuff PWR_0D75V_EN

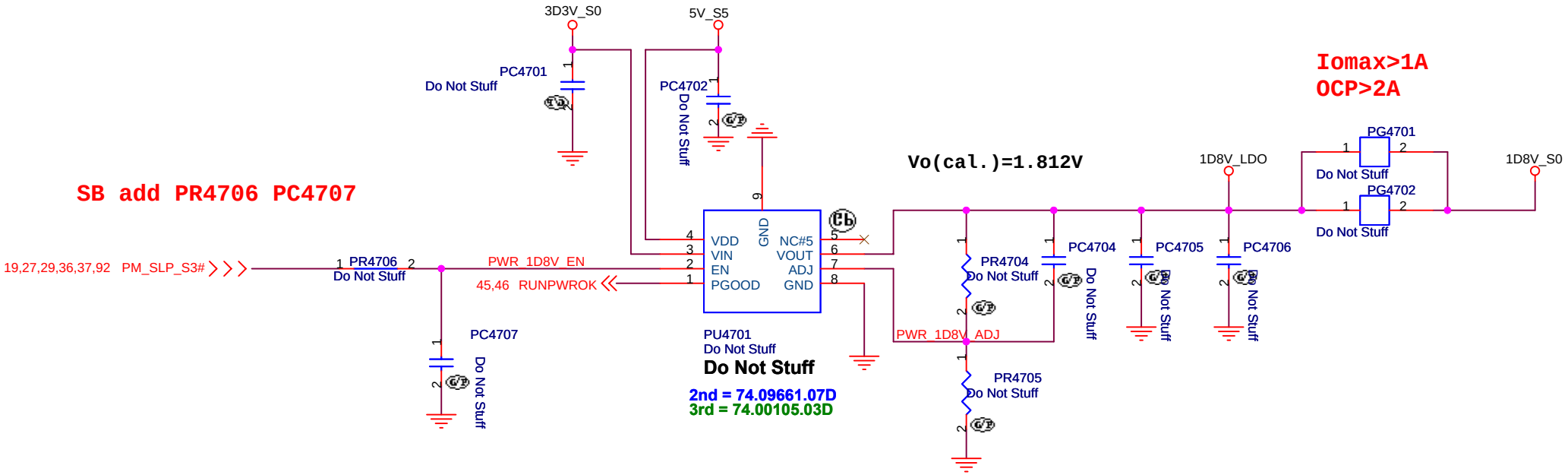
HR UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS5111
Size: Custom
Document Number: JE40-HR
Rev: -1
Date: Tuesday, March 29, 2011
Sheet 46 of 102

SSID = PWR.Plane.Regulator_1p8v

RT9025 for 1D8V_S0



HR UMA

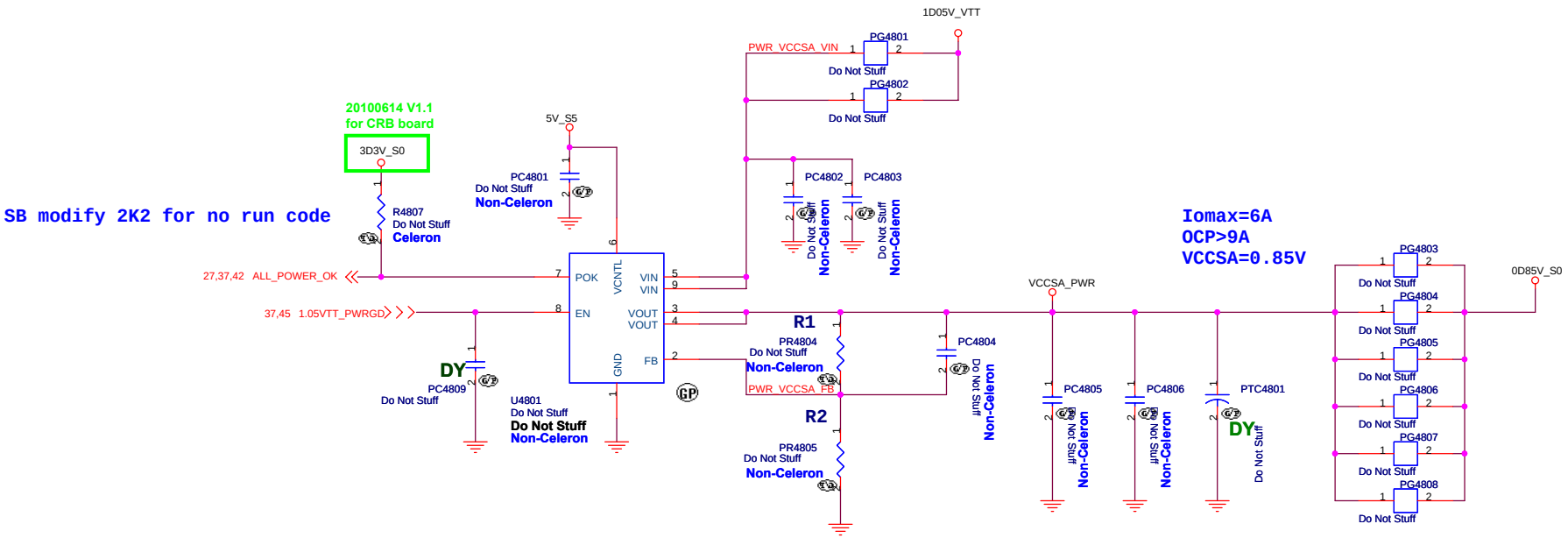
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *LDO_1D8V(RT9025)*

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Tuesday, March 29, 2011 Sheet 47 of 102

APL5916 for VCCSA



Vout=0.8*(1+R1/R2)

VCCSA_SEL	VCCSA_PWR
L	0.9V
H	0.8V

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

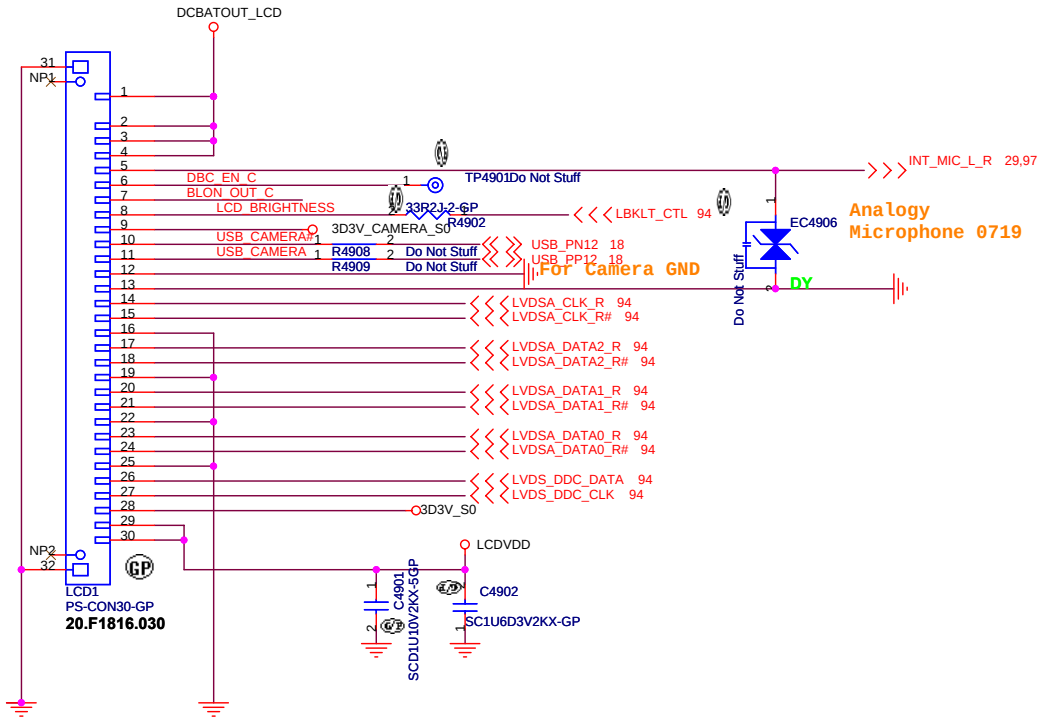
Title: *LDO VCCSA(APL5916)*

Size: A3 | Document Number: JE40-HR | Rev: -1

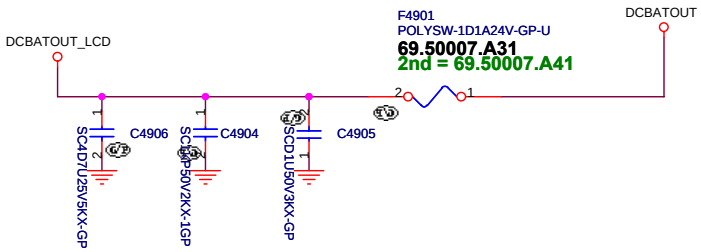
Date: Tuesday, March 29, 2011 | Sheet 48 of 102

SSID = VIDEO

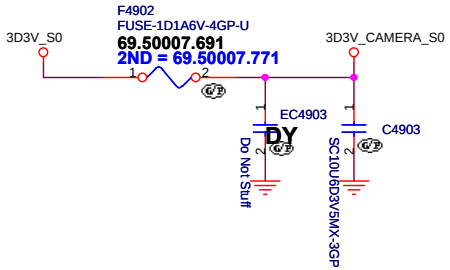
LVDS CONNECTOR



INVERTER POWER

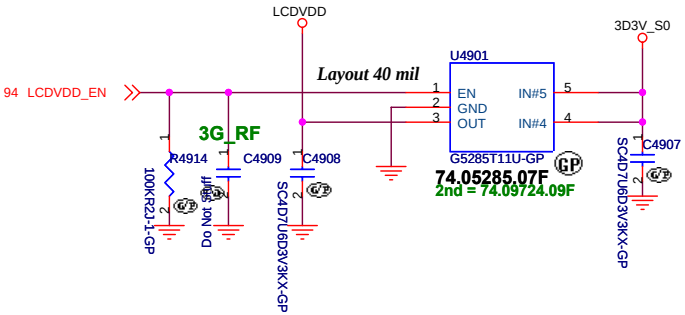


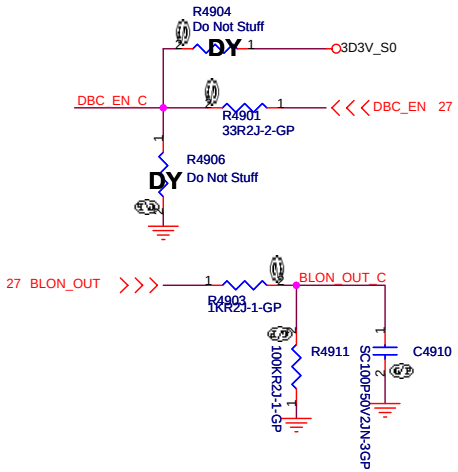
Camera Power



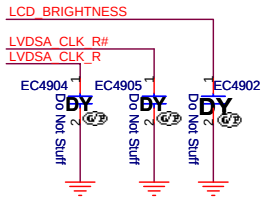
SSID = VIDEO

LCD POWER for ANNIE





For EMI request
Close to LVDS connector



HR UMA

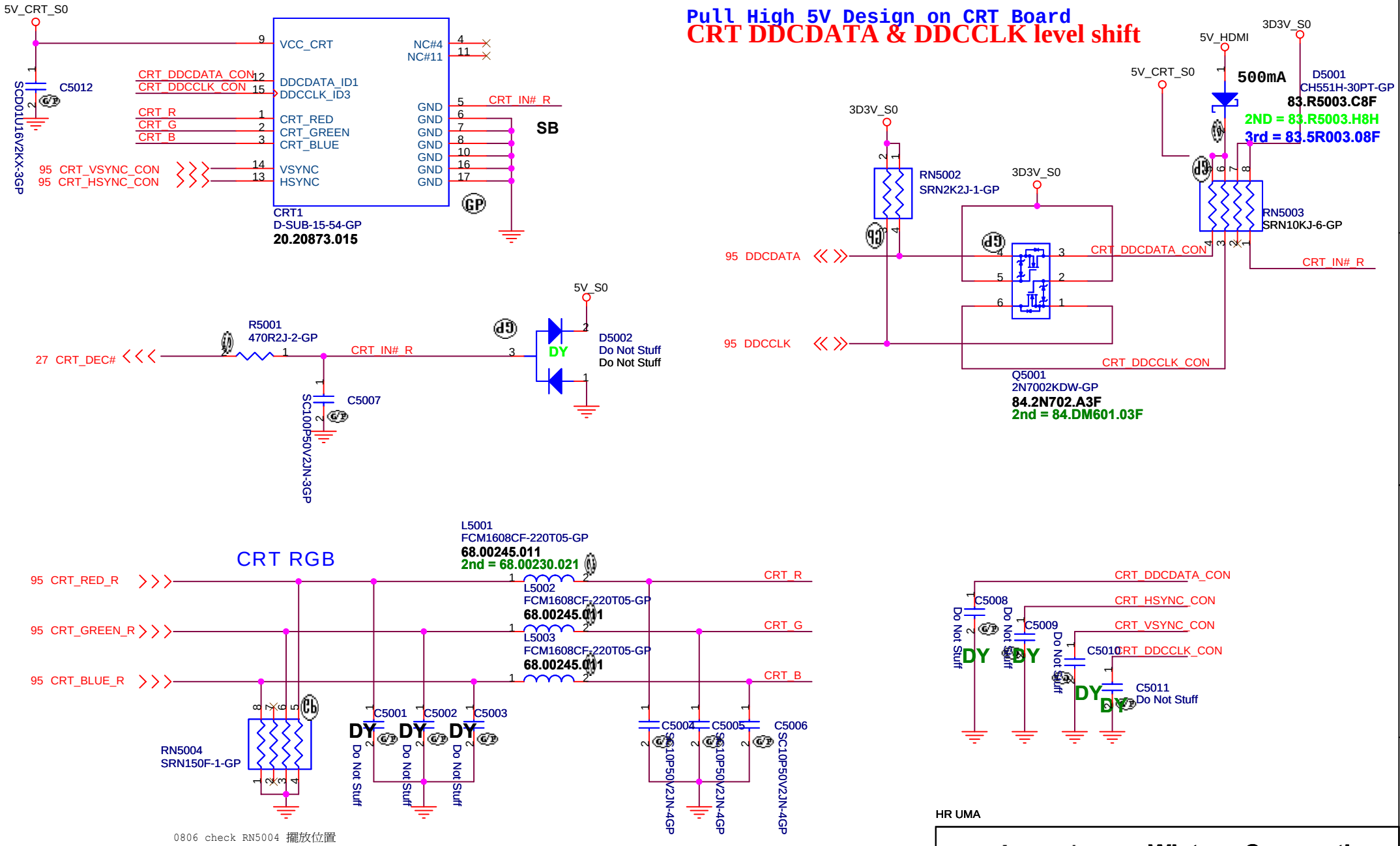
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD Connector

Size	Document Number	Rev
Custom	JE40-HR	-1

Date: Tuesday, March 29, 2011 Sheet 49 of 102

Pull High 5V Design on CRT Board
CRT DDCDATA & DDCCLK level shift



HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT Connector**

Size	Document Number	Rev
A4	JE40-HR	-1

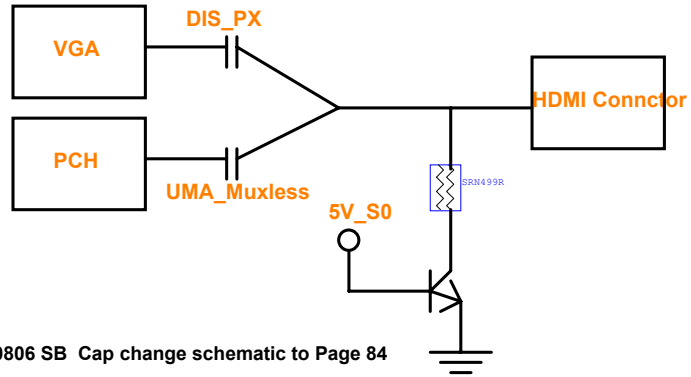
Date: Tuesday, March 29, 2011 Sheet 50 of 102

SSID = VIDEO

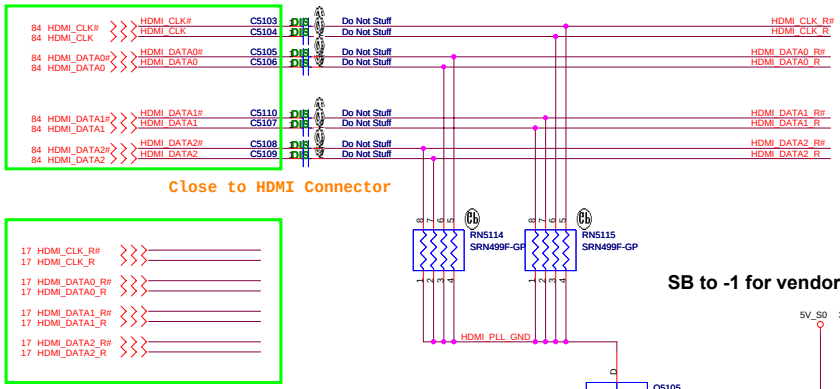
HDMI Level Shifter & CONNECTOR

UMA_Muxless : default setting used PS8101. if don't used PS8101
please change C5103~C5110 to 0 ohm resister

HDMI DISCRETE/ UMA Co-lay

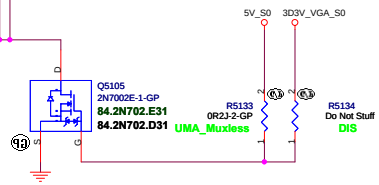


0806 SB Cap change schematic to Page 84



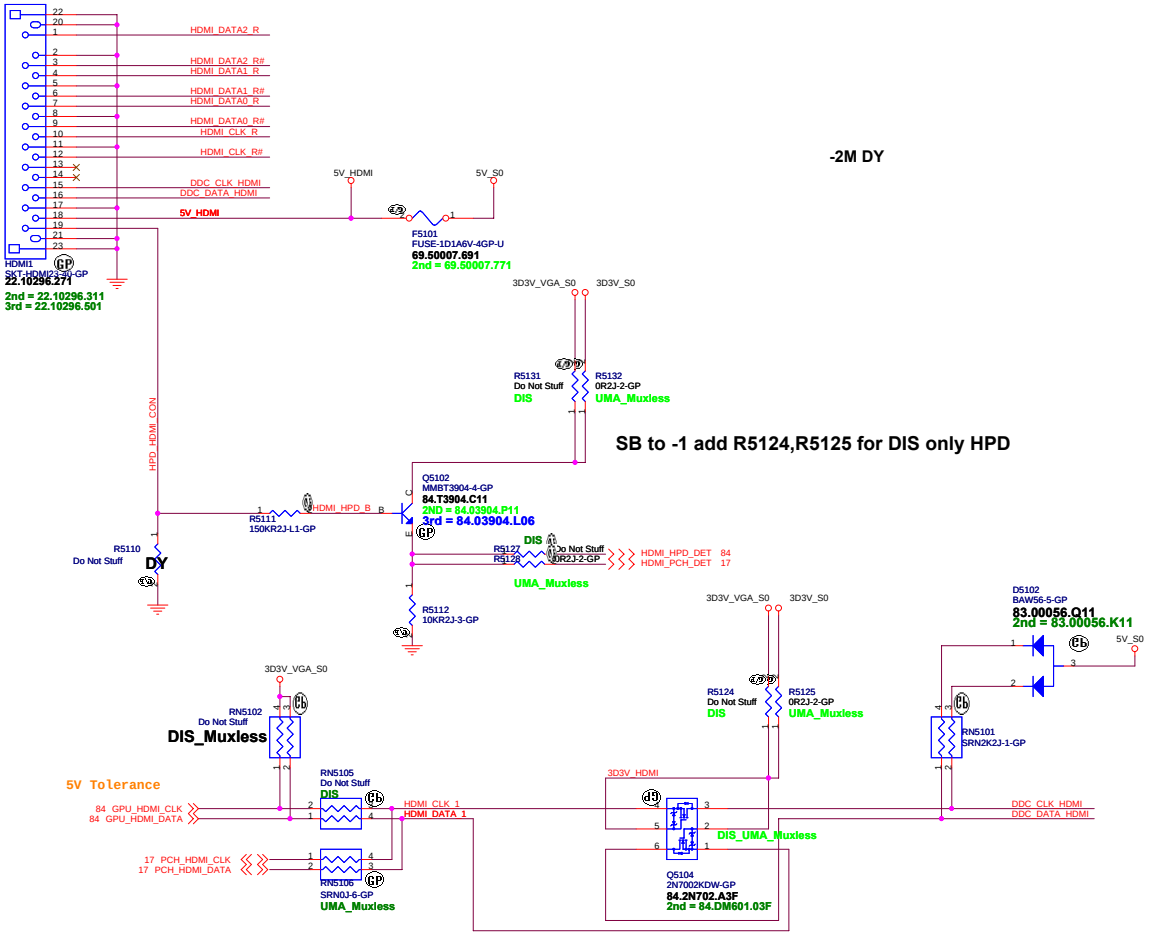
Close to HDMI Connector

SB to -1 for vendor suggest



Close to Level Shift

HDMI CONN



-2M DY

SB to -1 add R5124,R5125 for DIS only HPD

5V Tolerance

HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: HDMI Level Shifter/Connector	
Size: Custom	Document Number: JE40-HR	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 51 of 102

LED BACKLIGHT CONVERTER POWER

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *eDP*

Size	Document Number	Rev
A3	JE40-HR	-1

Date: Tuesday, March 29, 2011 Sheet 52 of 102

(Blanking)

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: S-VIDEO

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Tuesday, March 29, 2011 Sheet 53 of 102

(Blanking)

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

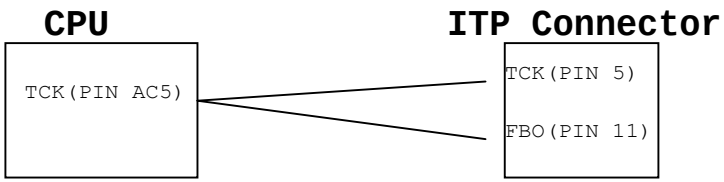
Size	Document Number	Rev
A4	JE40-HR	-1

Date: Tuesday, March 29, 2011 Sheet 54 of 102

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



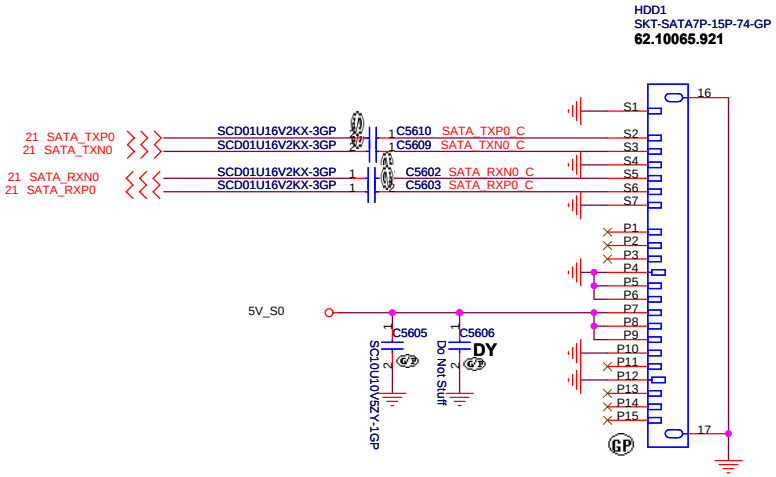
HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

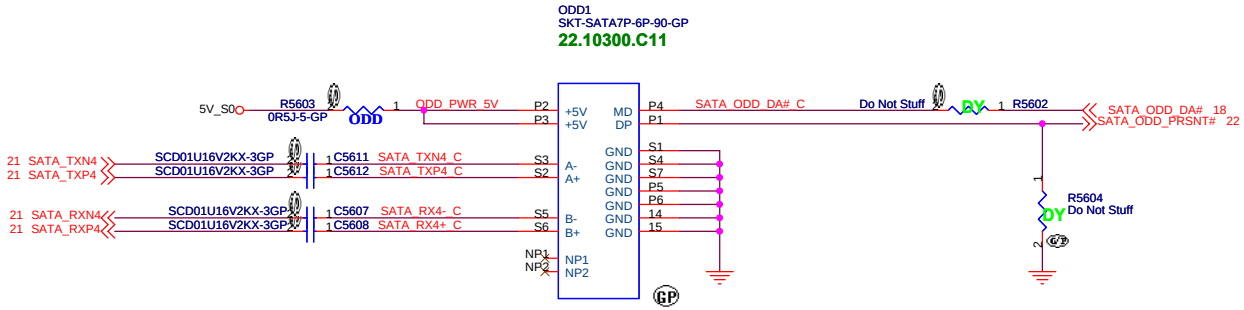
Title	ITP	
Size A4	Document Number JE40-HR	Rev -1
Date: Tuesday, March 29, 2011	Sheet 55 of 102	

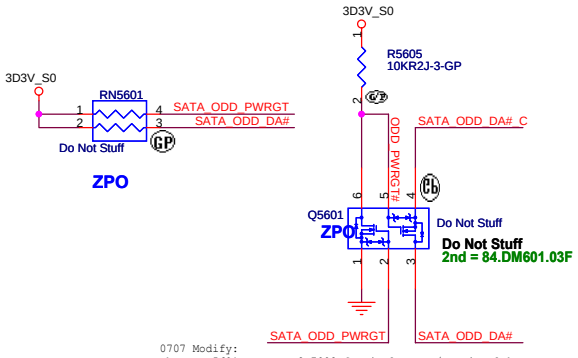
SSID = SATA

SATA HDD Connector



ODD Connector



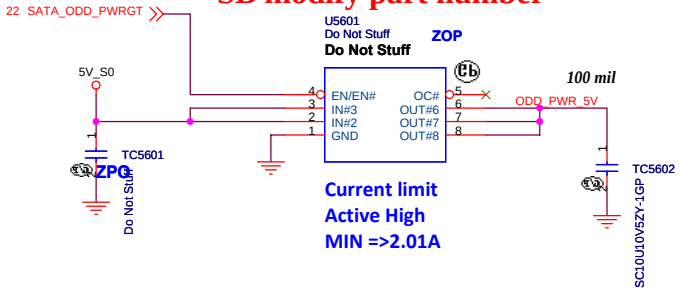


0707 Modify:
Change Q5601 to DUAL 2N7002 for isolate MD/DA signal between PCH and ODD.

SB

SATA Zero Power ODD

SB modify part number



HR UMA

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	HDD/ODD	
Size A3	Document Number JE40-HR	Rev -1
Date: Tuesday, March 29, 2011	Sheet 56 of 102	

ESATA Power

USB CHARGER

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *E-SATA/USB CHARGER*

Size	Document Number	Rev
A3	JE40-HR	-1

Date: Tuesday, March 29, 2011 Sheet 57 of 102

SSID = AUDIO

Speaker Connector

LINE1 OUT
SPDIF

JE40 Modify LINE OUT

Audio at small board

MIC IN

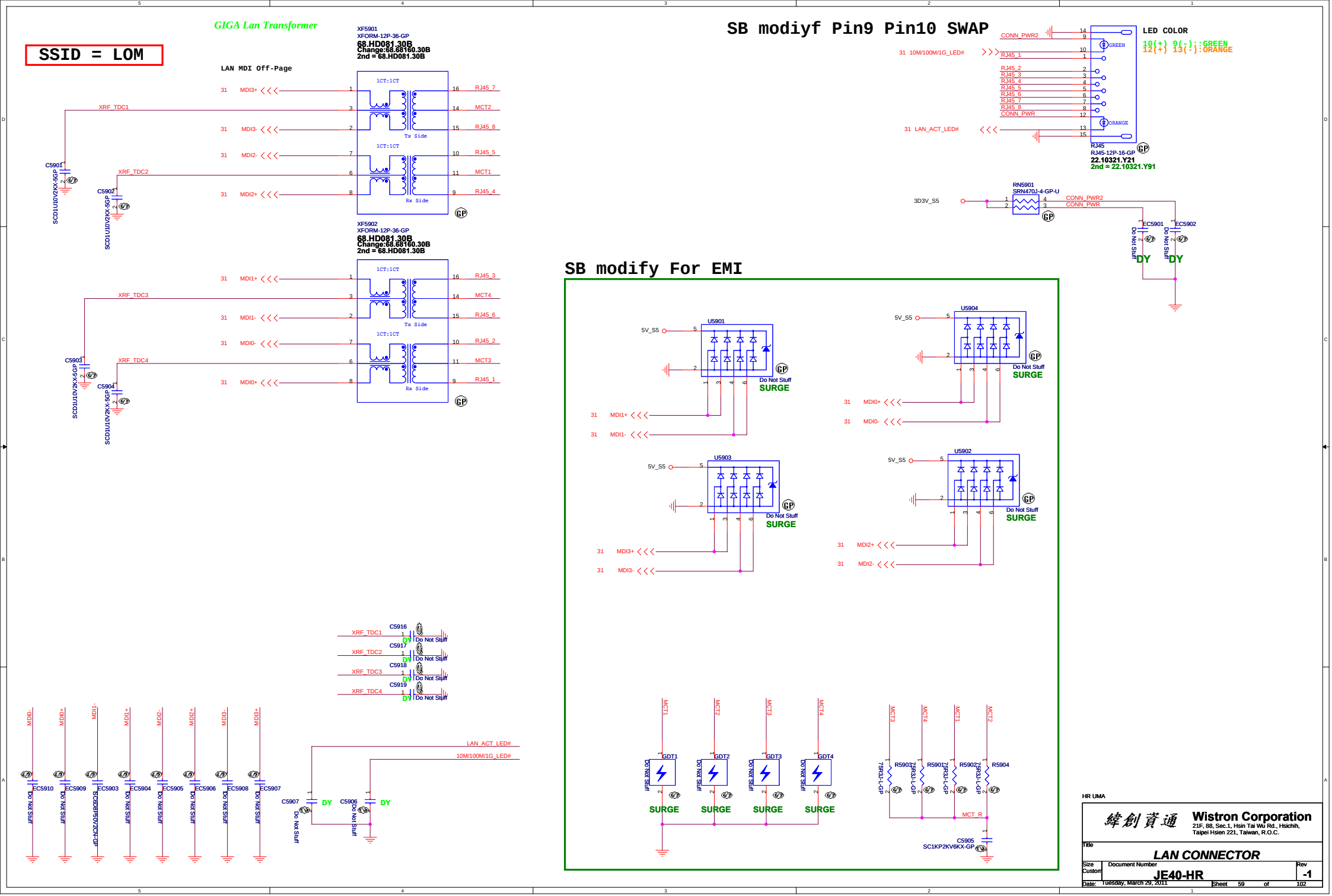
Internal
Microphone

JE40 delete Line in function

HR UMA

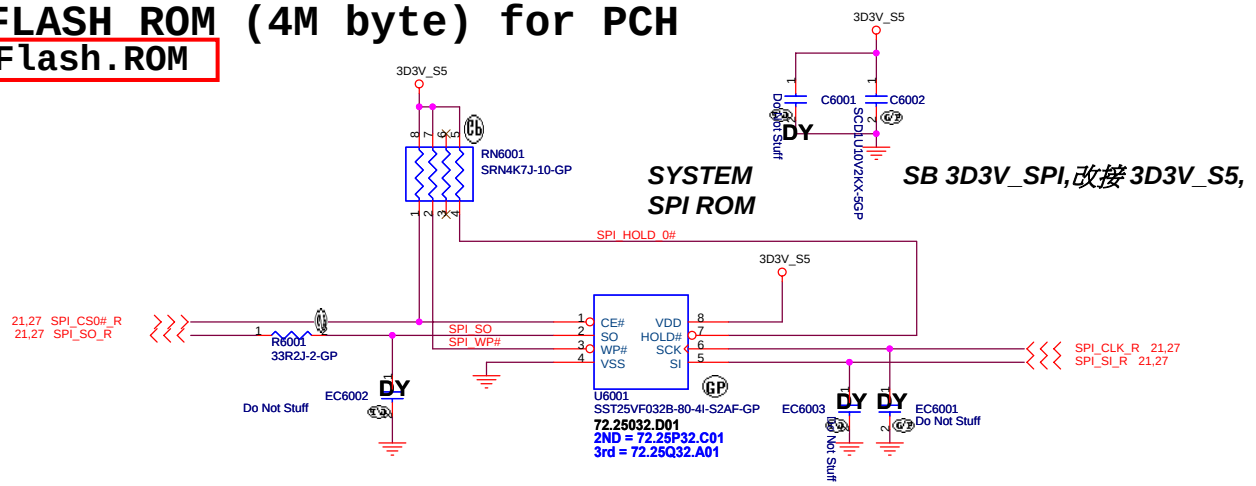
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
	Audio Jack	
Size A3	Document Number JE40-HR	Rev -1
Date: Tuesday, March 29, 2011	Sheet 58 of 102	


SSID = LOM
GIGA Lan Transformer
LAN MDI Off-Page
XF5901
XFORM-12P-36-GP
68.HD081.30B
Change:68.68160.30B
2nd = 68.HD081.30B
XF5902
XFORM-12P-36-GP
68.HD081.30B
Change:68.68160.30B
2nd = 68.HD081.30B
1CT:1CT
Tx Side
Rx Side
MDI3+
MDI3-
MDI2-
MDI2+
MDI1+
MDI1-
MDI0-
MDI0+
RJ45_7
MCT2
RJ45_8
RJ45_5
MCT1
RJ45_4
RJ45_3
MCT4
RJ45_6
RJ45_2
MCT3
RJ45_1
XRF_TDC1
XRF_TDC2
XRF_TDC3
XRF_TDC4
C5901
C5902
C5903
C5904
SCD1U10V2KX-5GP
SCD1U10V2KX-5GP
SCD1U10V2KX-5GP
SCD1U10V2KX-5GP
C5916
C5917
C5918
C5919
DY
Do Not Stuff
MDI0-
MDI0+
MDI1-
MDI1+
MDI2-
MDI2+
MDI3-
MDI3+
EC5910
EC5909
EC5903
EC5904
EC5905
EC5906
EC5908
EC5907
SCD28P50V2CN-GP
LAN_ACT_LED#
10M/100M/1G_LED#
C5907
C5906
SB modiyf Pin9 Pin10 SWAP
LED COLOR
10(+) 9(-)::GREEN
12(+) 13(-):ORANGE
CONN_PWR2
31 10M/100M/1G_LED#
RJ45_1
RJ45_2
RJ45_3
RJ45_4
RJ45_5
RJ45_6
RJ45_7
RJ45_8
CONN_PWR
31 LAN_ACT_LED#
GREEN
ORANGE
RJ45
RJ45-12P-16-GP
22.10321.Y21
2nd = 22.10321.Y91
RN5901
SRN470J-4-GP-U
3D3V_S5
CONN_PWR2
CONN_PWR
EC5901
EC5902
DY
DY
SB modify For EMI
U5901
U5904
U5903
U5902
5V_S5
Do Not Stuff
SURGE
31 MDI1+
31 MDI1-
31 MDI0+
31 MDI0-
31 MDI3+
31 MDI3-
31 MDI2+
31 MDI2-
MCT1
MCT2
MCT3
MCT4
GDT1
GDT2
GDT3
GDT4
R5903
R5901
R5902
R5904
75R3J-L-GP
MCT_R
C5905
SC1KP2KV6KX-GP
HR UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
LAN CONNECTOR
Size
Custom
Document Number
JE40-HR
Rev
-1
Date: Tuesday, March 29, 2011
Sheet 59 of 102

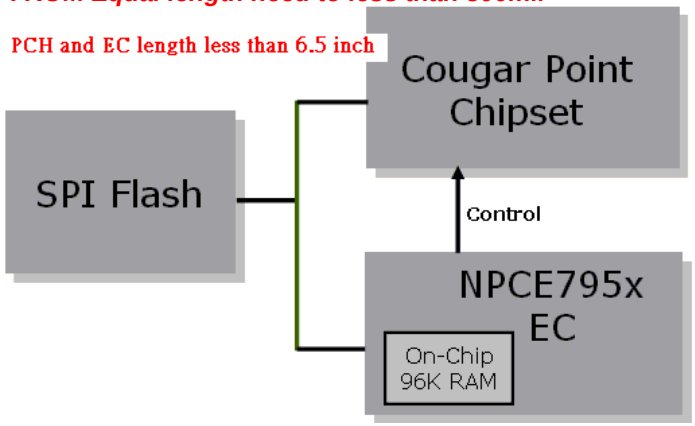
SPI FLASH ROM (4M byte) for PCH

SSID = Flash.ROM

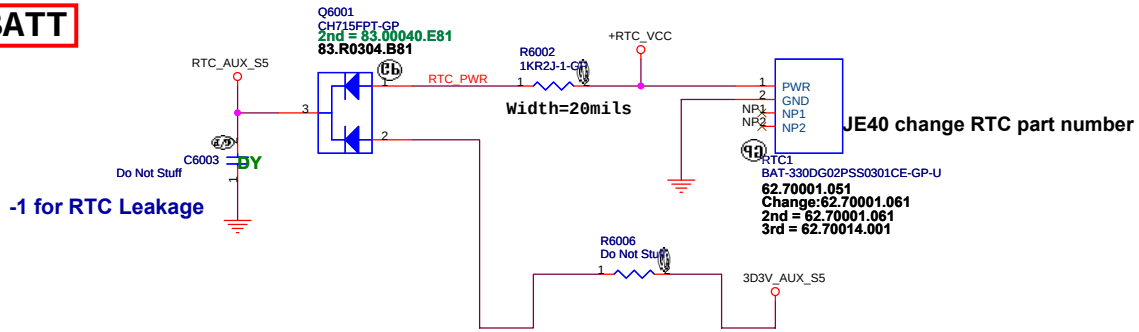


SPI ROM Equal length need to less than 500mil

PCH and EC length less than 6.5 inch



SSID = RBATT



JE40 change RTC part number

-1 for RTC Leakage

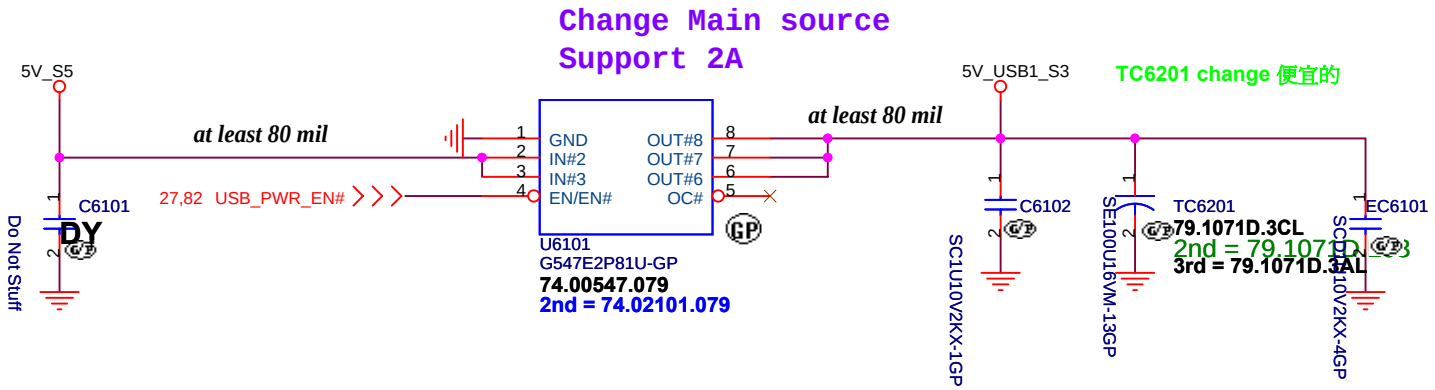
-2M DY

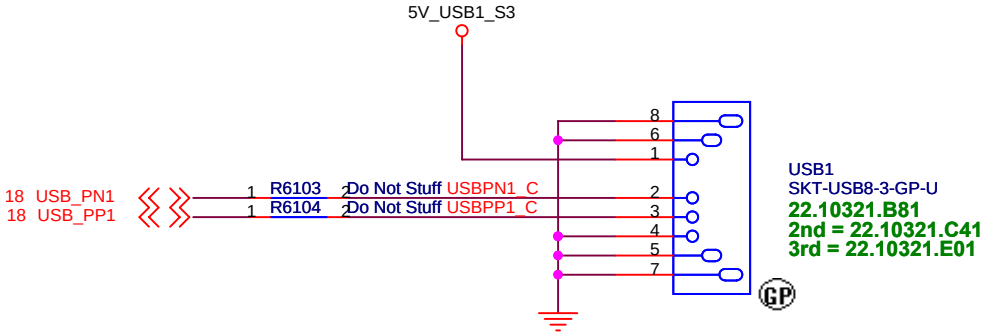
HR UMA

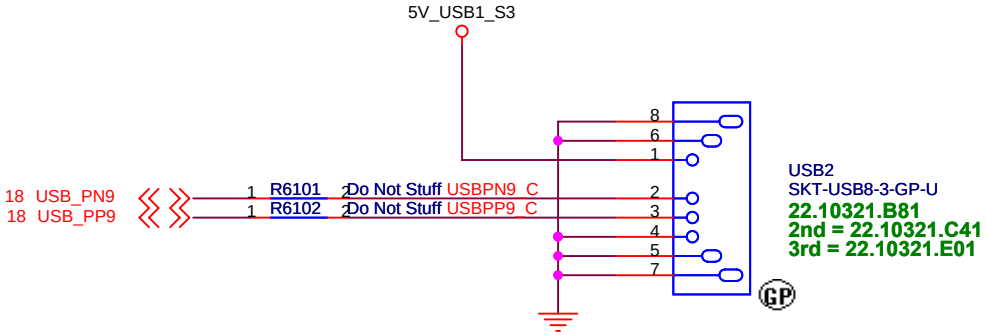
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*Flash/RTC*	
Size	Document Number	Rev
Custom	JE40-HR	-1
Date: Tuesday, March 29, 2011	Sheet 60 of 102	

SSID = USB

IO Board USB Power







HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	USB Power SW	
Size A4	Document Number JE40-HR	Rev -1
Date: Tuesday, March 29, 2011	Sheet 61 of 102	

HR UMA

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

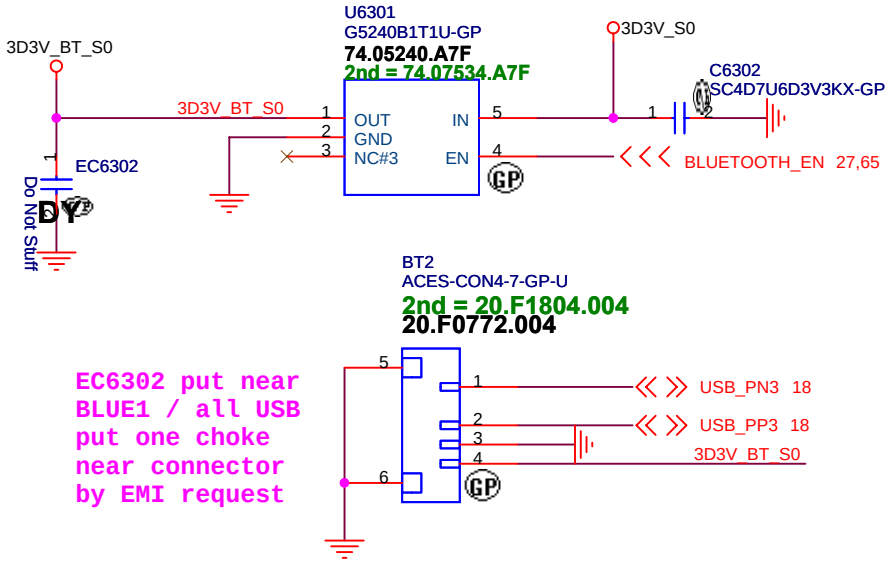
USB 3.0 Port

Size	Document Number	Rev
A3	**JE40-HR**	**-1**

Date: Tuesday, March 29, 2011 Sheet 62 of 102

SSID = User.Interface
Bluetooth Module conn.

ANNIE Bluetooth Module

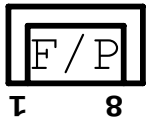


HR UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Bluetooth***
Size A4	Document Number **JE40-HR** Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 63 of 102

Finger printer

JE40 delete FP function



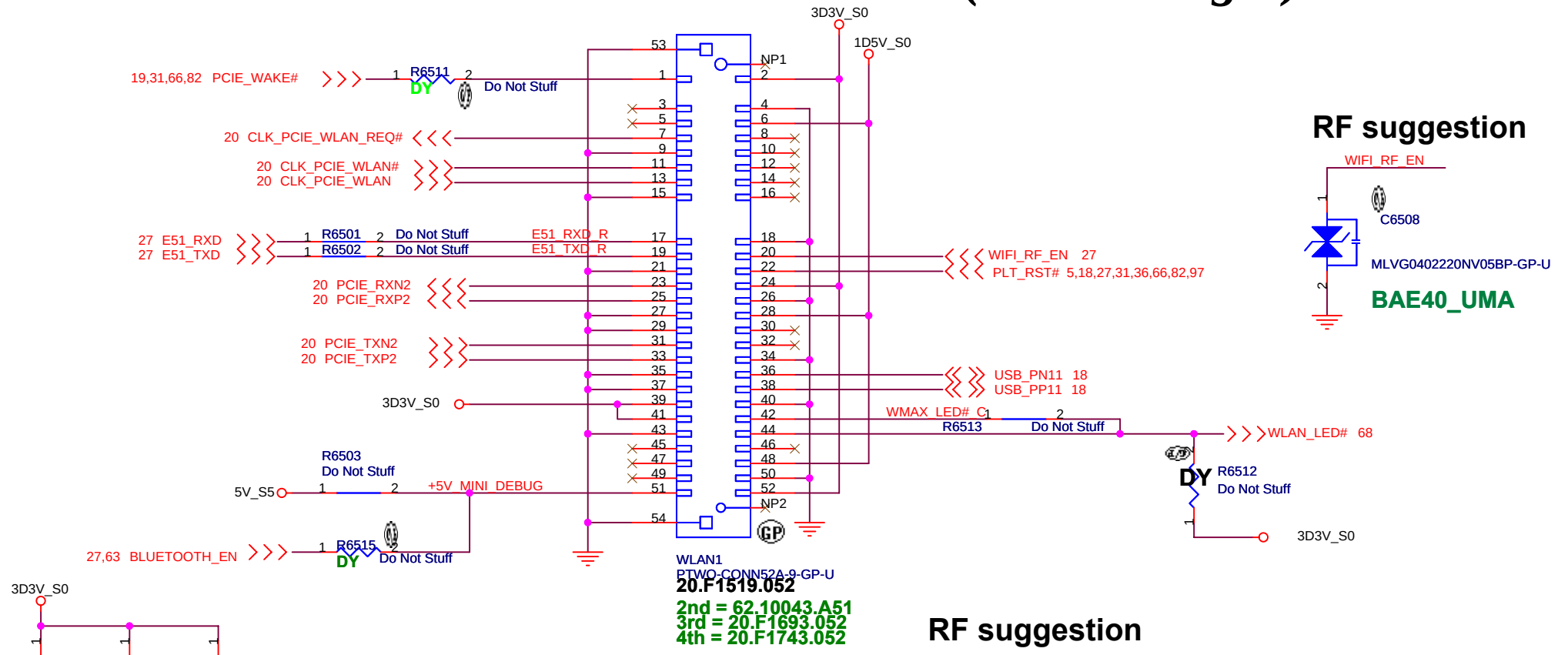
HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

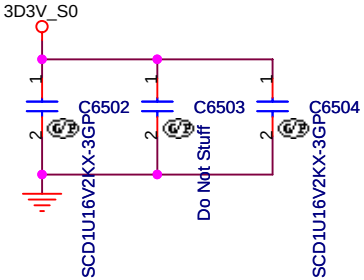
Title	***RESERVED***	
Size A4	Document Number **JE40-HR**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 64 of 102	

SSID = Wireless

Mini Card Connector(802.11a/b/g/n)

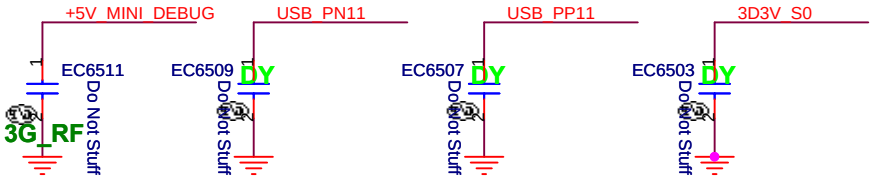


RF suggestion

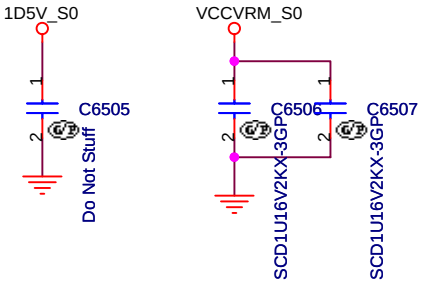


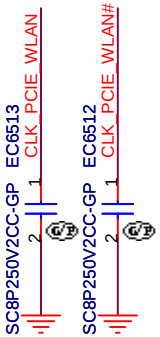
SB modify for SIV

RF suggestion



-2





HR UMA

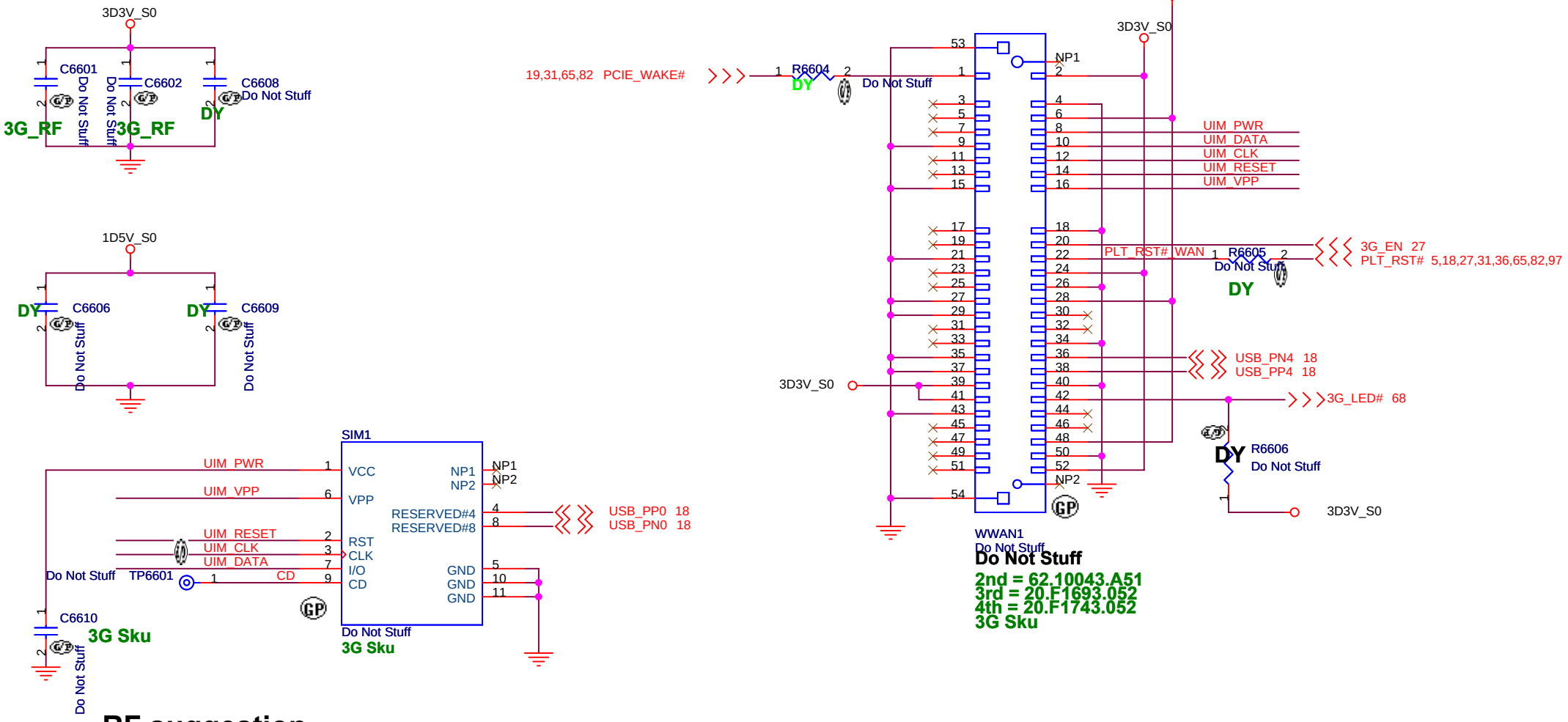
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	MINICARD(WLAN)/ITP CONN	
Size A4	Document Number JE40-HR	Rev -1
Date: Tuesday, March 29, 2011	Sheet 65 of 102	

SSID = Wireless

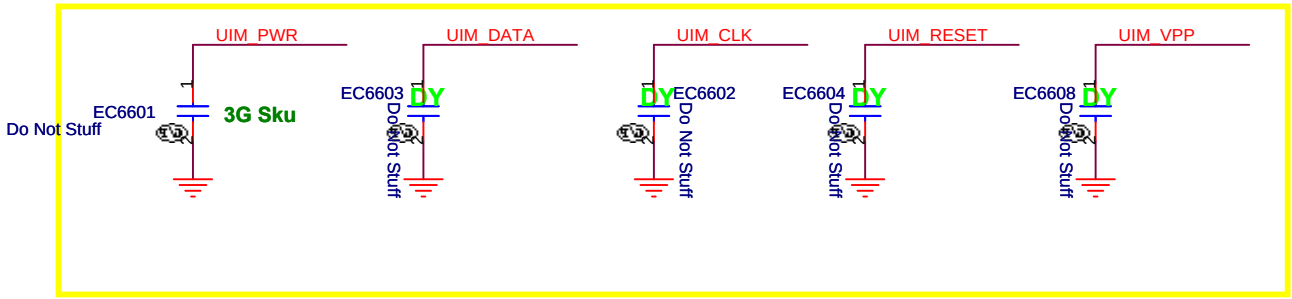
Mini Card Connector(WWAN)

20100712 V1.5

Place near MINI Card CONN



RF suggestion



HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: WWAN Connector

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Tuesday, March 29, 2011 Sheet 66 of 102

(Blanking)

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

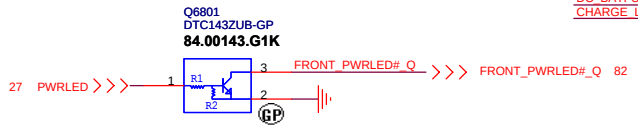
Reserved

Size	Document Number	Rev
A4	JE40-HR	-1

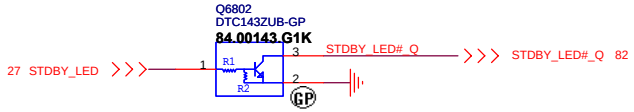
Date: Tuesday, March 29, 2011 Sheet 67 of 102

SSID = User.Interface

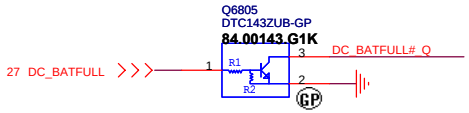
Power button LED



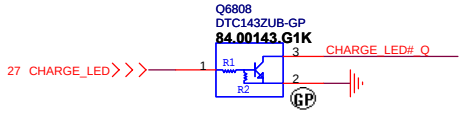
Power STDBY_LED

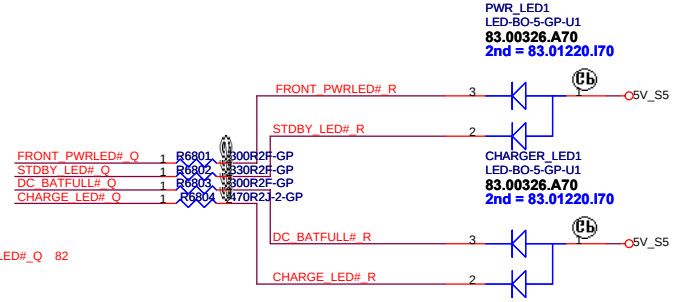


Battery LED2(DC_BATFULL)

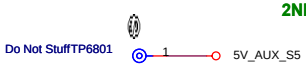


Battery LED1(CHARGE)

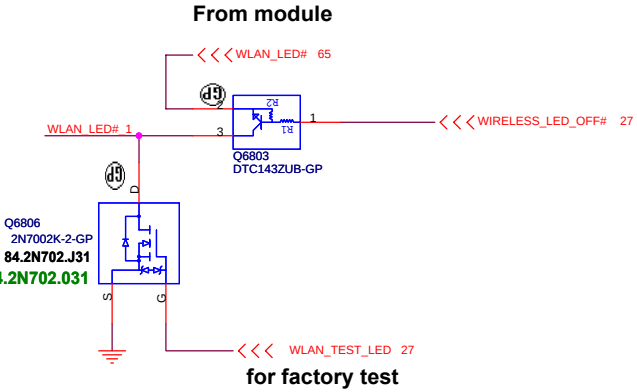




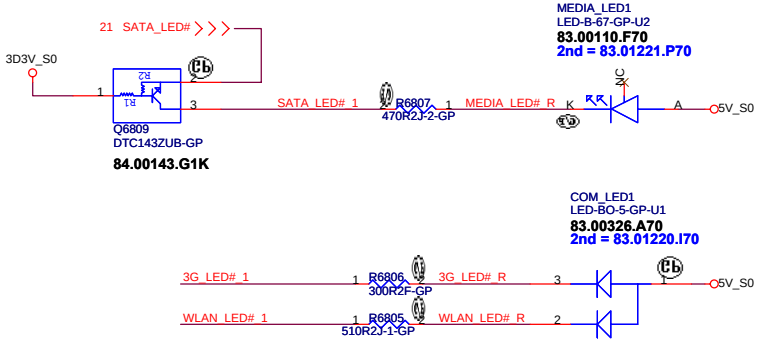
-2M DY



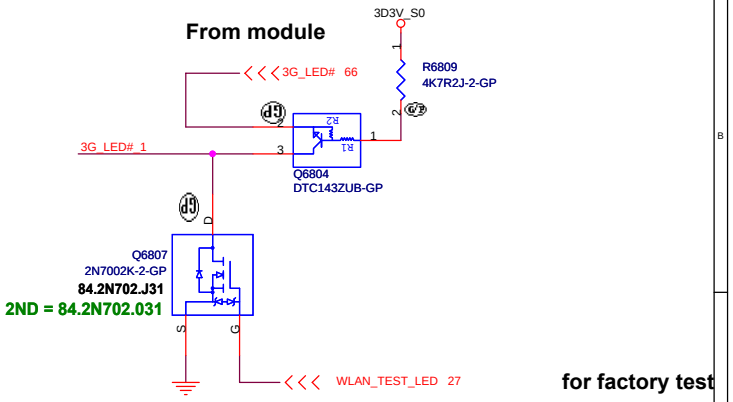
WLAN_LED



SATA HDD LED



3G LED

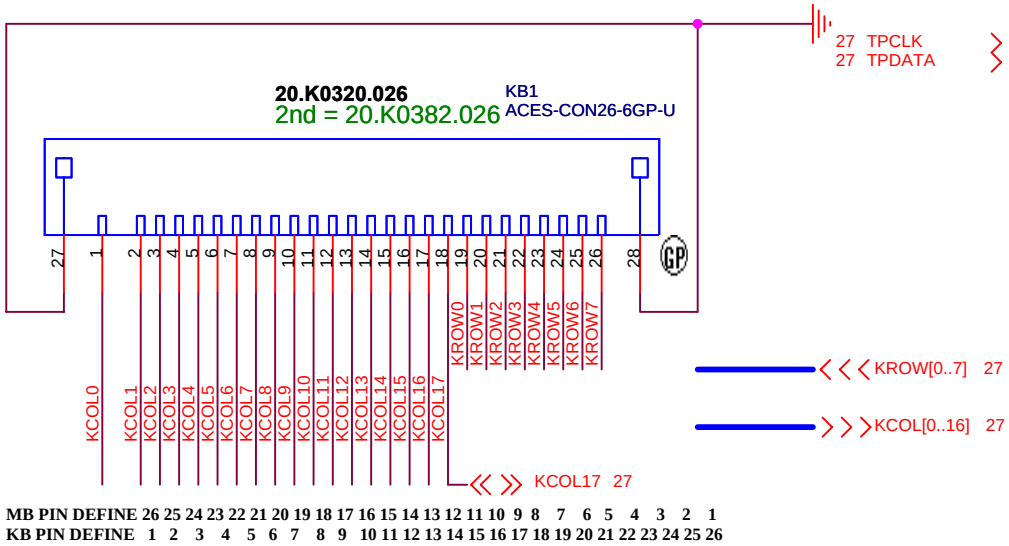


HR UMA

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	LED Bard/Power Button	
Size: Custom	Document Number: JE40-HR	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 68 of 102	

SSID = KBC

Internal KeyBoard Connector



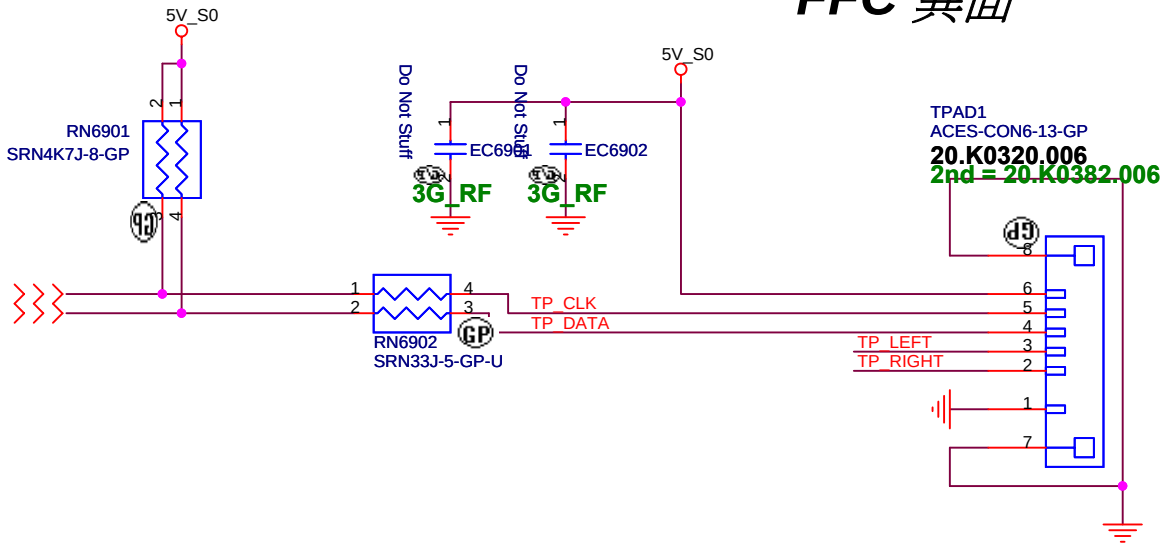
MB PIN DEFINE 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
KB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26

26 K/B 1

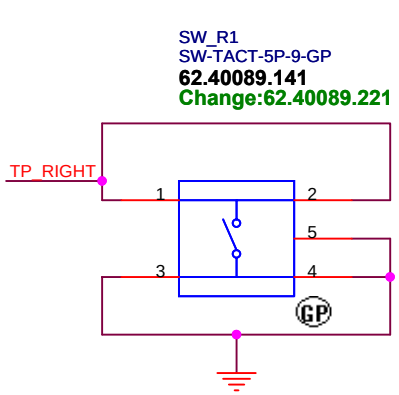
SB to -1 modify Part number

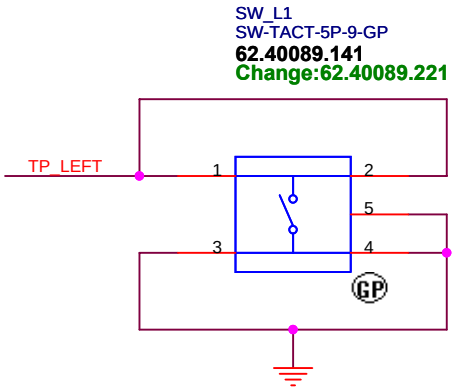
TOUCH PAD

FFC 異面



-2M DY

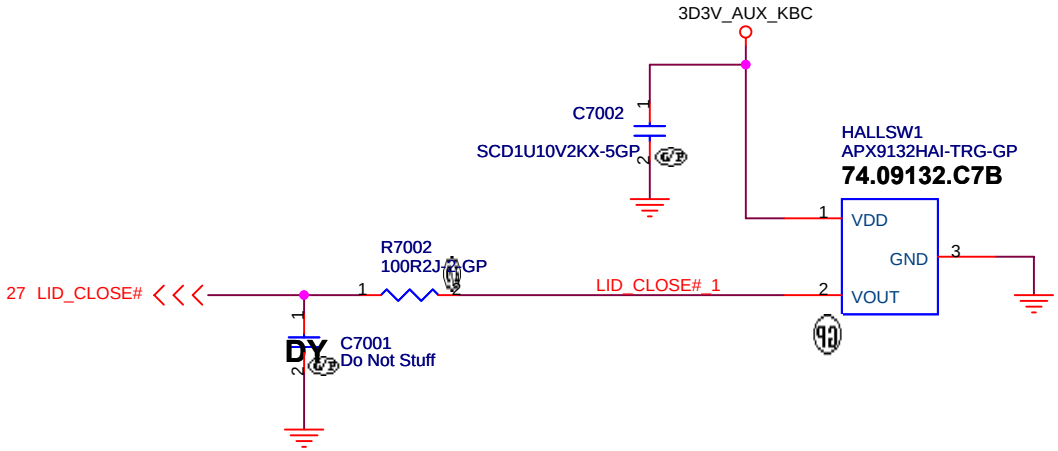




HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Key Board/Touch Pad	
Size A4	Document Number JE40-HR	Rev -1
Date: Tuesday, March 29, 2011	Sheet 69 of 102	



HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Sensor***

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Tuesday, March 29, 2011 Sheet 70 of 102

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Dubug connector

Size	Document Number	Rev
A4	**JE40-HR**	**-1**

Date: Tuesday, March 29, 2011 Sheet 71 of 102

(Blanking)

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	JE40-HR	-1

Date: Tuesday, March 29, 2011 Sheet 72 of 102

(Blanking)

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

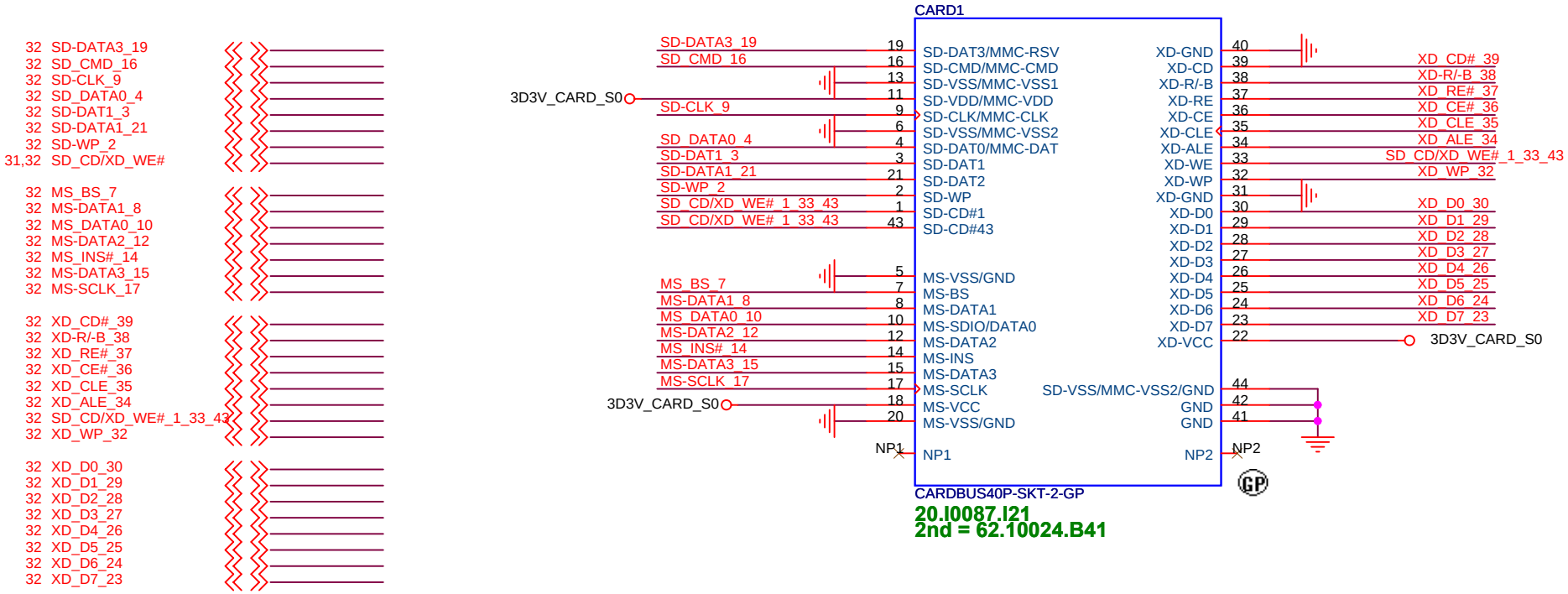
Title: *Reserved*

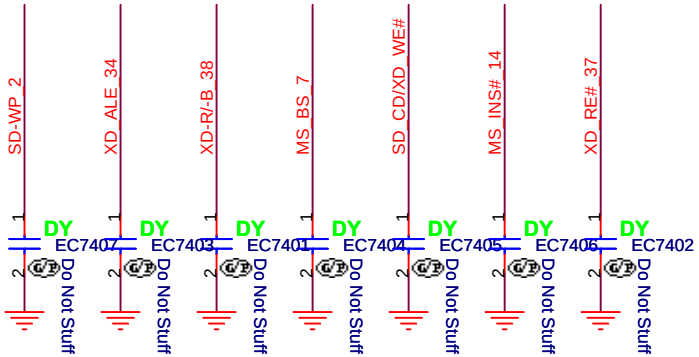
Size	Document Number	Rev
A3	JE40-HR	-1

Date: Tuesday, March 29, 2011 Sheet 73 of 102

SD/XD/MS Card Reader

SSID = SDIO





HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CARD Reader CONN**

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Tuesday, March 29, 2011 Sheet 74 of 102

SSID = ExpressCard

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: New Card

Size	Document Number	Rev
A3	JE40-HR	-1

Date: Tuesday, March 29, 2011 Sheet 75 of 102

(Blanking)

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	**JE40-HR**	**-1**

Date: Tuesday, March 29, 2011 Sheet 76 of 102

(Blanking)

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Tuesday, March 29, 2011 Sheet 77 of 102

(Blanking)

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	**JE40-HR**	**-1**

Date: Tuesday, March 29, 2011 Sheet 78 of 102

SSID = User.Interface

Free Fall Sensor

```
Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can
```

JE40 delete G Sensor Function

```
Note
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.
```

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*Free Fall Sensor*	
Size A4	Document Number JE40-HR	Rev -1
Date: Tuesday, March 29, 2011	Sheet 79 of 102	

(Blanking)

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Tuesday, March 29, 2011 Sheet 80 of 102

(Blanking)

HR UMA

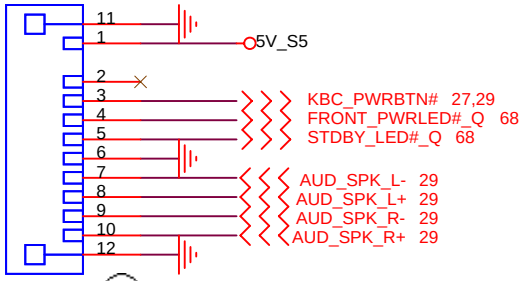
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

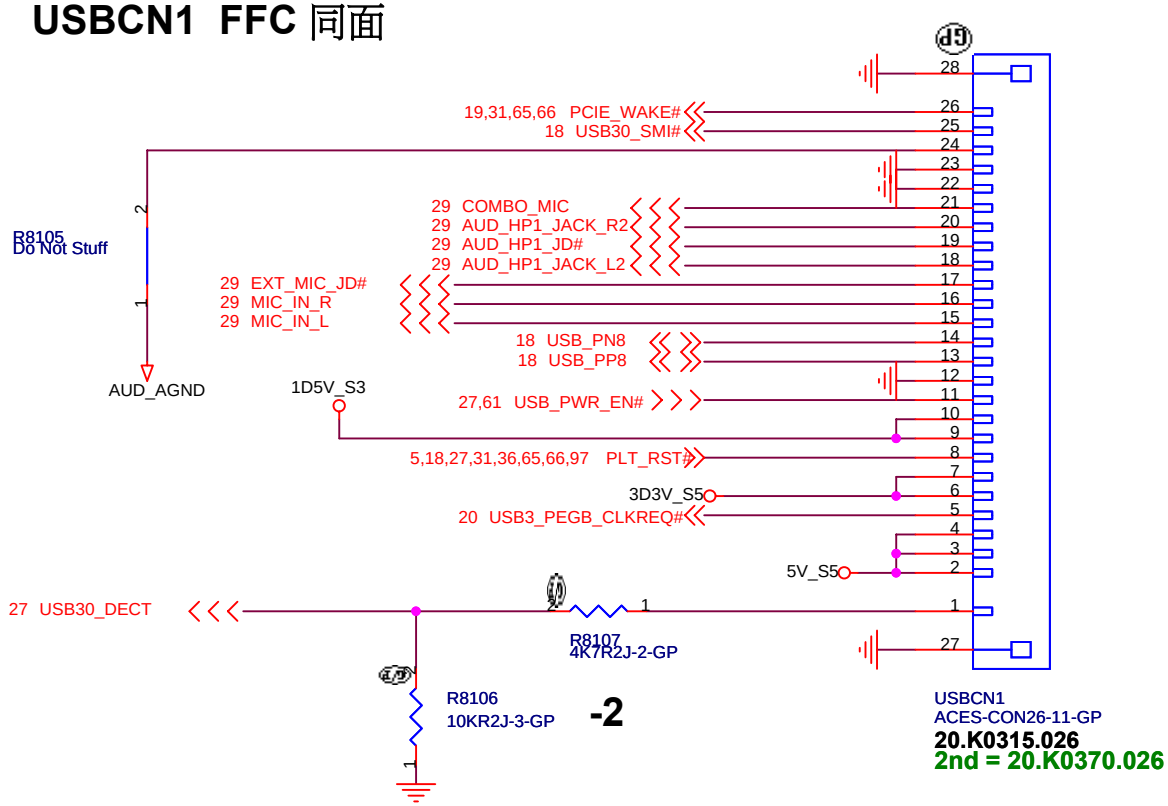
Size	Document Number	Rev
A4	JE40-HR	-1

Date: Tuesday, March 29, 2011 Sheet 81 of 102

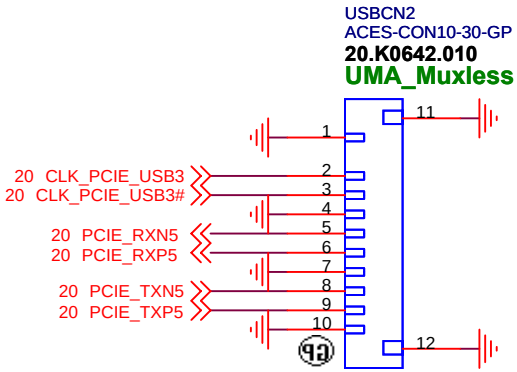
PWRCN1 FFC 異面



USBCN1 FFC 同面

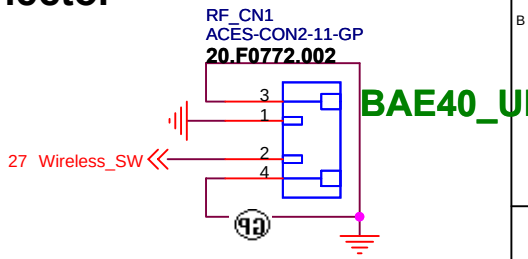


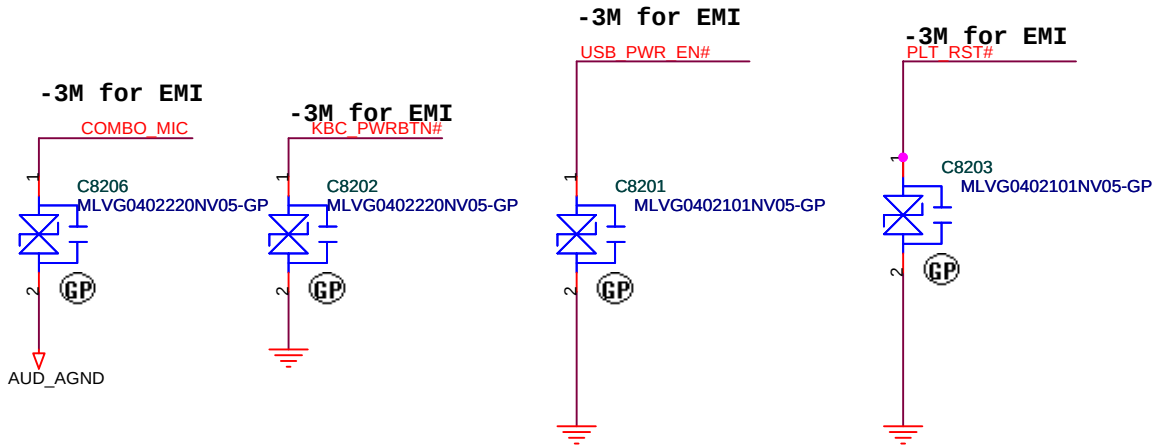
-4 modify part number



USBCN2 FFC 同面

-1 add RF connector
BAE40 Only

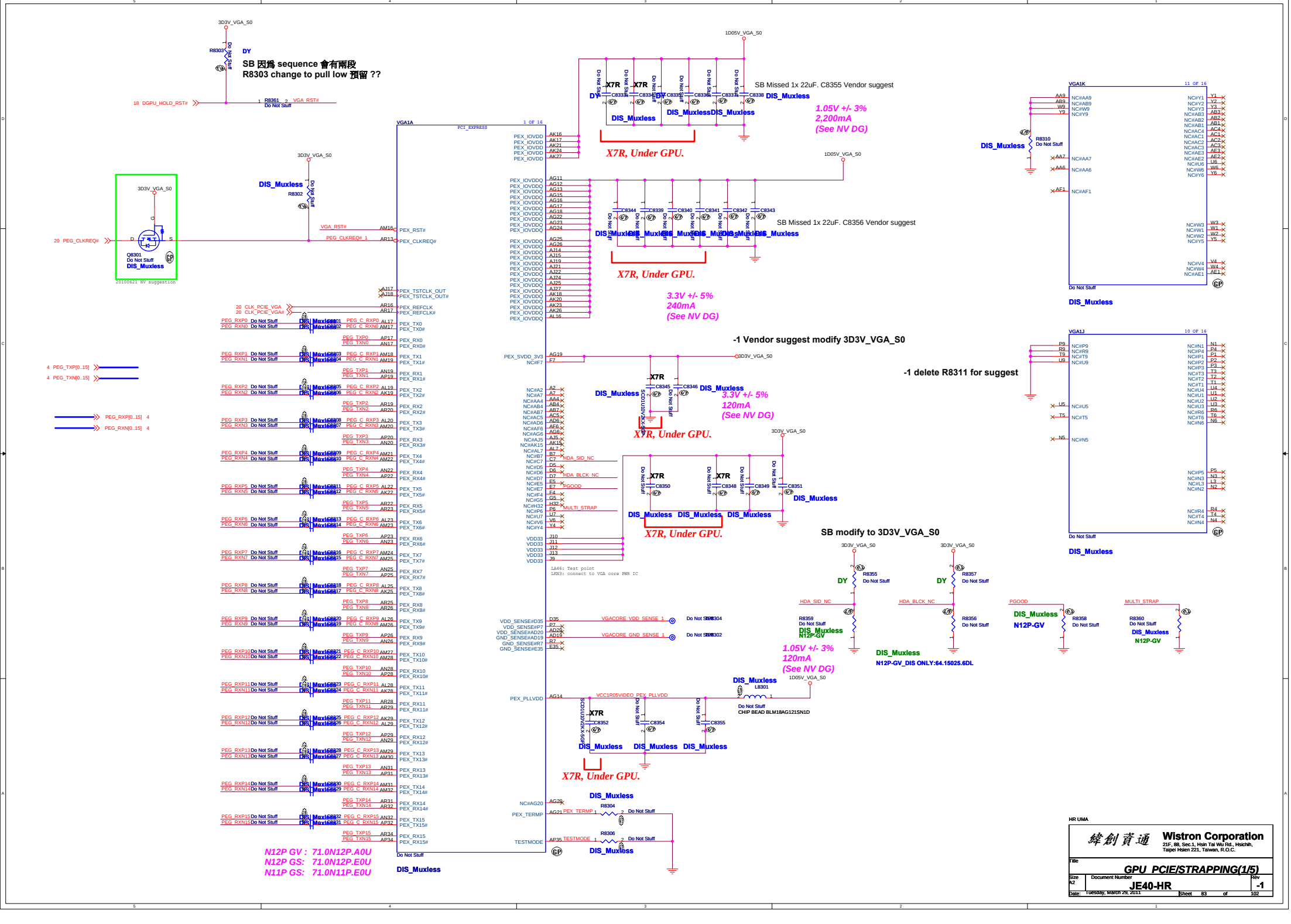




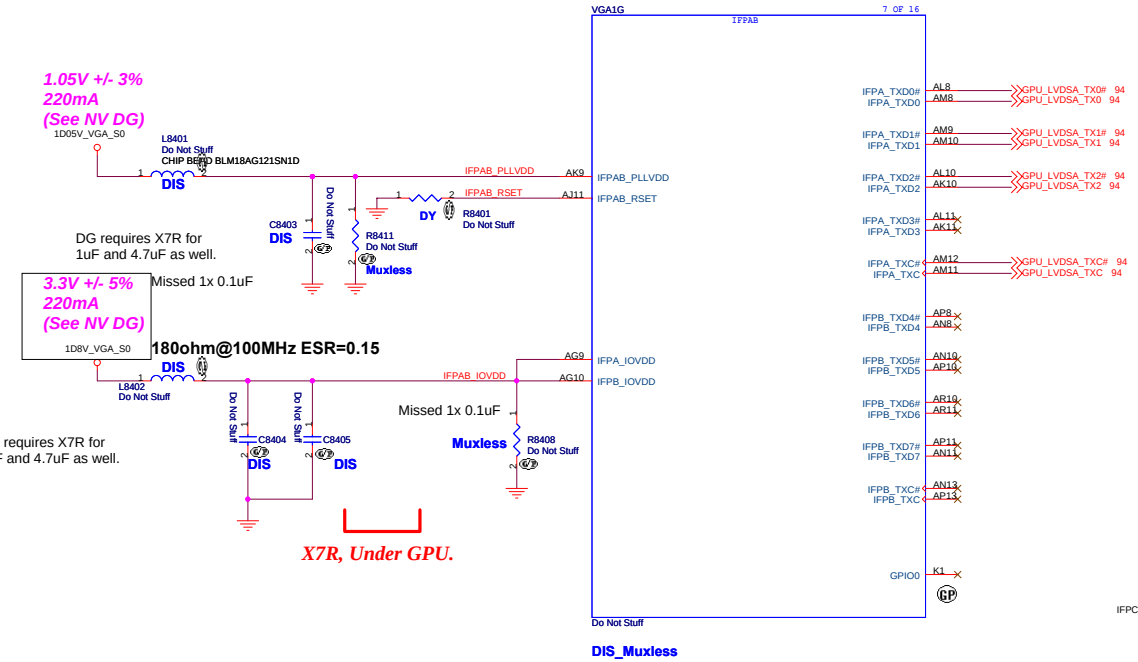
Cabele Wire to BD

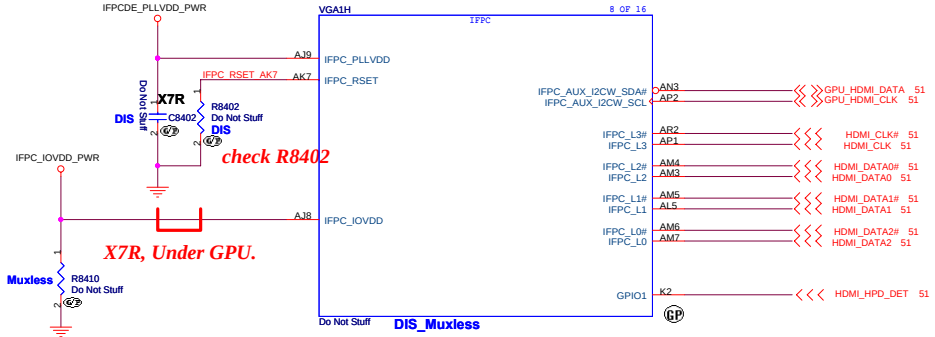
HR UMA

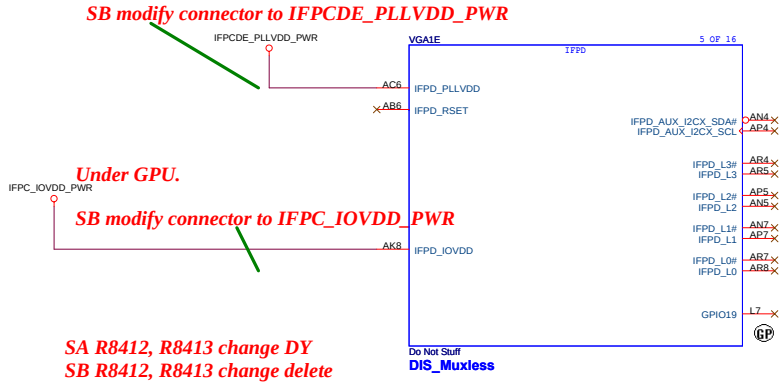
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***IO Board Connector***	
Size A4	Document Number **JE40-HR**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 82 of 102	

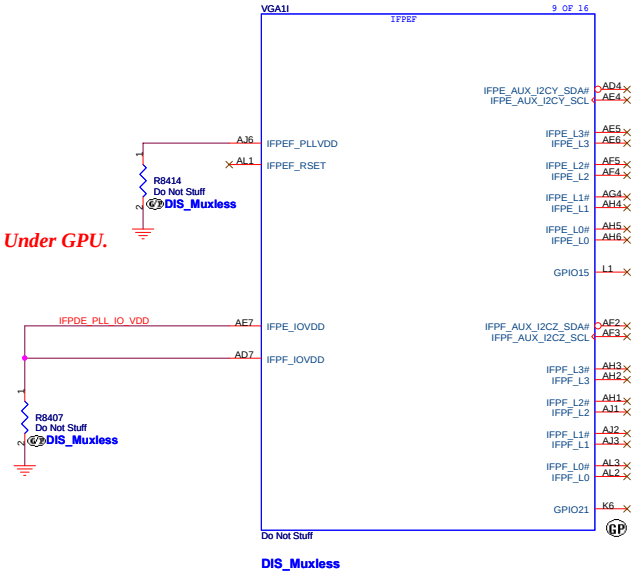

SB 因爲 sequence 會有兩段
R8303 change to pull low 預留 ??
SB Missed 1x 22uF. C8355 Vendor suggest
1.05V +/- 3%
2,200mA
(See NV DG)
X7R, Under GPU.
SB Missed 1x 22uF. C8356 Vendor suggest
3.3V +/- 5%
240mA
(See NV DG)
-1 Vendor suggest modify 3D3V_VGA_S0
3.3V +/- 5%
120mA
(See NV DG)
-1 delete R8311 for suggest
SB modify to 3D3V_VGA_S0
1.05V +/- 3%
120mA
(See NV DG)
N12P GV : 71.0N12P.A0U
N12P GS: 71.0N12P.E0U
N11P GS: 71.0N11P.E0U
Wistron Corporation
GPU_PCIE/STRAPPING(1/5)
JE40-HR
-1

LVDS Interface

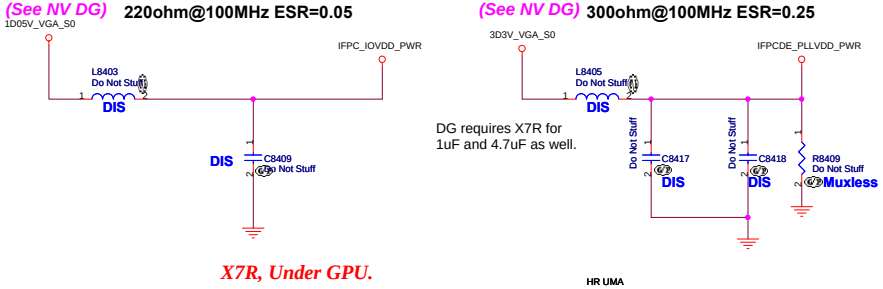








HDMI Interface

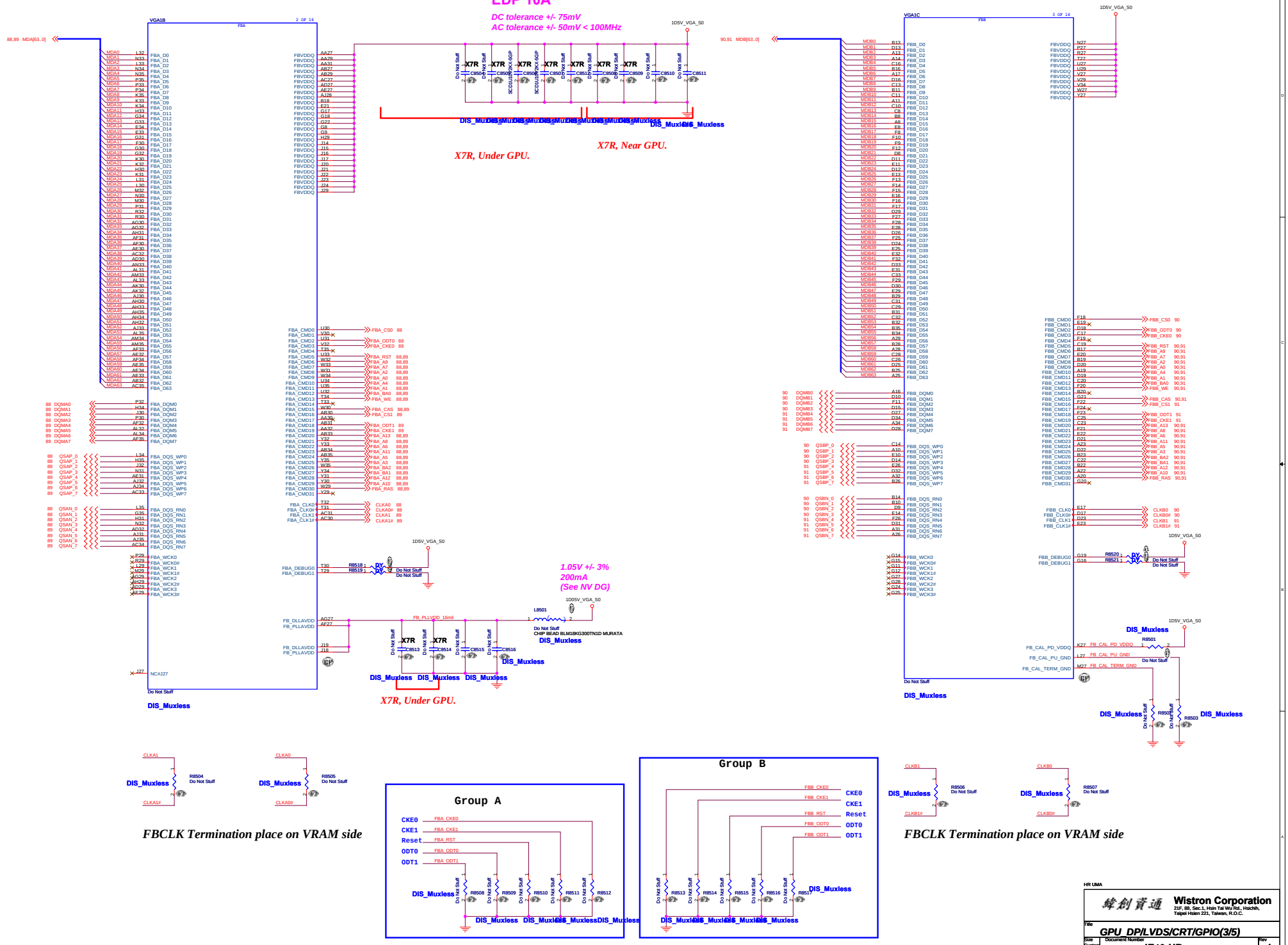


HR UMA

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	GPU Memory(2/5)	
Size Custom	Document Number JE40-HR	Rev -1
Date: Tuesday, March 29, 2011	Sheet 84 of 102	

EDP 10A

DC tolerance +/- 75mV
AC tolerance +/- 50mV < 100MHz



HR UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_DP/LVDS/CRT/GPIO(3/5)

Size: Custom | Document Number: JE40-HR | Rev: -1

Date: Tuesday, March 29, 2011 | Sheet 85 of 102

300ohm@100MHz ESR=0.25ohm

3.3V +/- 5%
120mA
(See NV DG)

Missed 3x 0.1uF

X7R, Under GPU.

delete 10K DY to GND

1.05V +/- 3%
150mA
(See NV DG)

X7R, Under GPU.

SB DIS_Muxless 都要上件或DY??

SB HOSONIC modify to 12P, R8607 modify to 390R

VGA Thermal sensor P2800

Modify SMBUS

SB 修改上件,才能跑全速

Pull high 在Page 94

SB R8619 15" DY

SJM50-CP SUPPORT							
P-STATE	NVVDD_ALTV1	NVVDD_ALTV0	N11M-GE1	N11M-GE2	N11M-GP1	N11P-GE1	N11P-GE Fermi
P12	0	0	0.85V	0.85V	0.85V	0.80V	0.85V
P8	0	1	0.85V	0.85V	0.85V	0.85V	0.9V
P0	1	0	1.03V	1.03V	1.03V	0.95V	0.95V

預設0.9V

NVIDIA TABLE

	Hynix 2G 0110 128*16*8 800MHZ	Hynix 1G 0000 64*16*8 800MHZ	Samsung 1G 0011 64*16*8 800MHZ	Samsung 512 64*16*4 800MHZ	Samsung 2G 0111 128*16*8 800MHZ
RO M_SIPD R8627	34.8Kohm 64.34825.6DL	5Kohm 64.49915.6DL	20Kohm 64.20025.6DL	20Kohm 64.20025.6DL	45Kohm 64.45325.6DL

GPU_ROM_SI

for 1Gbit Hynix VRAM	for 2Gbit Hynix VRAM	for 1Gbit Samsung VRAM	for 2Gbit Samsung VRAM
RAM_CFG[0]=0	RAM_CFG[0]=0	RAM_CFG[0]=1	RAM_CFG[0]=1
RAM_CFG[1]=1	RAM_CFG[1]=1	RAM_CFG[1]=1	RAM_CFG[1]=1
RAM_CFG[2]=0	RAM_CFG[2]=1	RAM_CFG[2]=0	RAM_CFG[2]=1
RAM_CFG[3]=0	RAM_CFG[3]=0	RAM_CFG[3]=0	RAM_CFG[3]=0

GPU_ROM_SO

VGA_DEVICE =1 (low bit)
SMB_ALT_ADDR =0
FB_0_BAR_SIZE =0
XCLK_417 =0 (High bit)

GPU_ROM_SCLK

PEX_PLL_EN_TERM =0
SLOT_CLK_CFG =1
SUB_VENDOR =0
PCI_DEVID[4] =1 N11P Fermi QS 1

Logical Strap Bit Mapping

Resistor	Pull-up	Pull-down
5Kohms	1000	0000
10Kohms	1001	0001
15Kohms	1010	0010
20Kohms	1011	0011
25Kohms	1100	0100
30Kohms	1101	0101
35Kohms	1110	0110
45Kohms	1111	0111

TABLE NVIDIA

-1 modify N12P GV setting

	71.0N12P.E0U	71.0N12P.A0U			
	N12P-GS DEV ID: 0x0DF4	N12P-GV DEV ID: 0x1050	N11P-GE Fermi DEV ID: 0x0DF1 (0001)	N11P-GS Fermi DEV ID: 0x0DF0 (0000)	N12P-GE DEV ID: 0x0DF5 (0101)
STRAP2 PU	25Kohm 64.24925.6DL	45Kohm ES 45K QS 5K 64.49915.6DL	10Kohm 63.10334.1DL	5Kohm 64.49915.6DL	30Kohm 64.30025.6DL
	N12P-GS	N12P-GV	N11P-GE Pull Low	N11P-GS Pull Low	N12P-GE

STRAP0 USER[0]=1 USER[1]=1 USER[2]=1 USER[3]=1 USE 1111 (45K)

STRAP1 3GIO_PADCFG[0]=0 3GIO_PADCFG[1]=1 3GIO_PADCFG[2]=1 3GIO_PADCFG[3]=1 USE 0110 (35K)

STRAP2 PCI_DEVID[0]=1 N12P-GS GF108-730-A1 0x0DF4 (0X4) (0100)
PCI_DEVID[1]=0 N12P-GV1 GF108-705-A1 0x0DF7 (0X7) (0111)
PCI_DEVID[2]=0 N11P-GS Fermi 0x0DF0 (0000)
PCI_DEVID[3]=0 N11P-GE Fermi 0x0DF1 (0001)

SB change 3D3V_VGA_S0, R8638 change DY

Hy2G_64.34825.6DL,Hy1G_64.15025.6DL,Sam1G512M_64.20025.6DL,Sam2G_64.45325.6DL

N12PGS_N12PGV:64.49915.6DL

N12PGS_N12PGV:64.49915.6DL

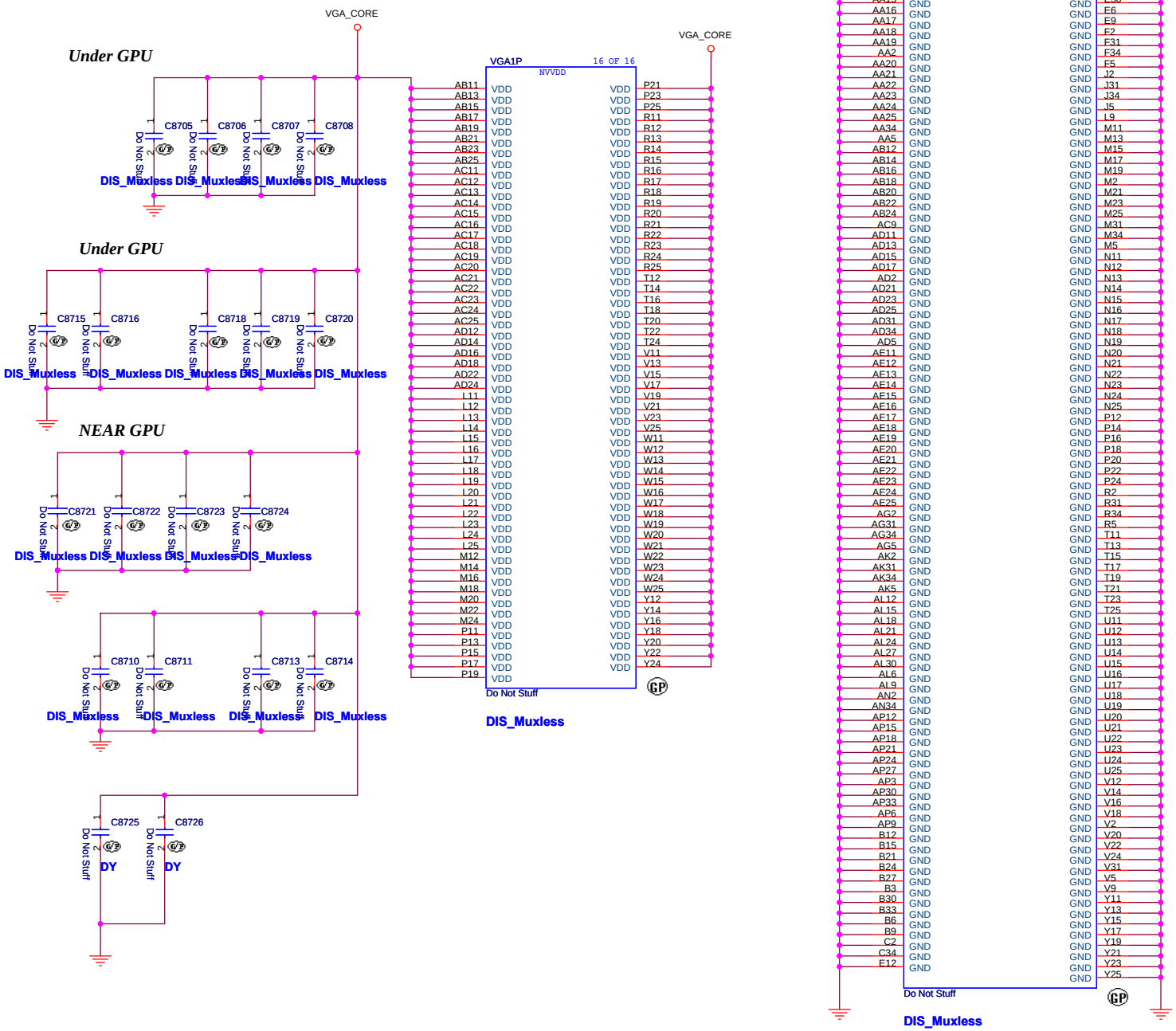
Wistron Corporation
22F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

GPU_POWER(4/5)

Size A1 | Document Number JE40-HR | Rev -1

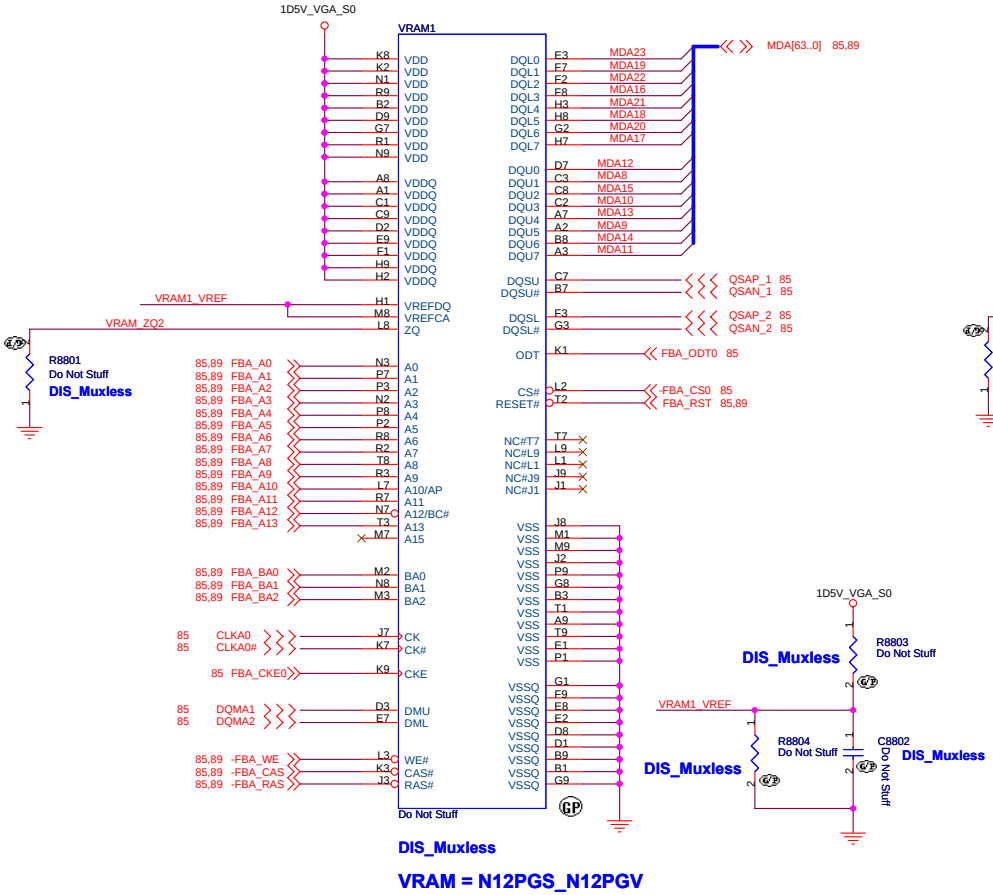
Date: Tuesday, March 29, 2011 | Sheet 85 of 102

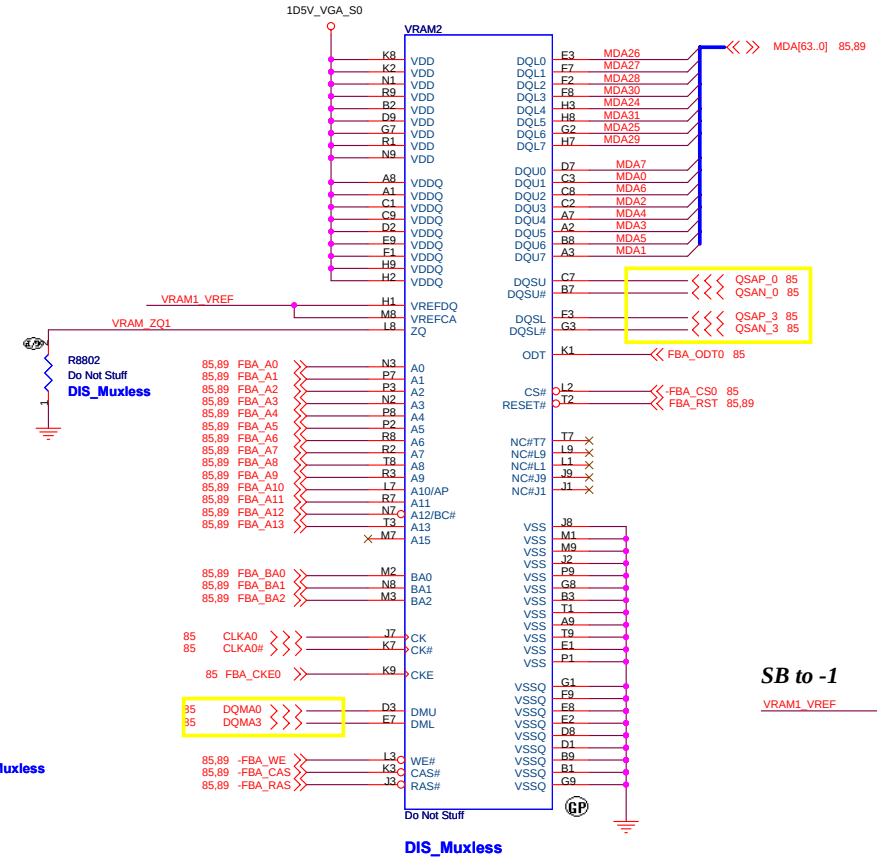
EDP 50A
(TDP 37W)



HR UMA

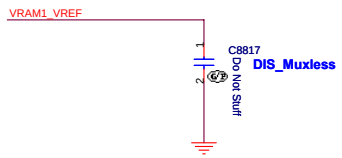
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***GPU DPPWR/GND(5/5)***
Size A3 / Document Number	**JE40-HR** / Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 87 of 102





FB CMD mapping Mode D-N12x

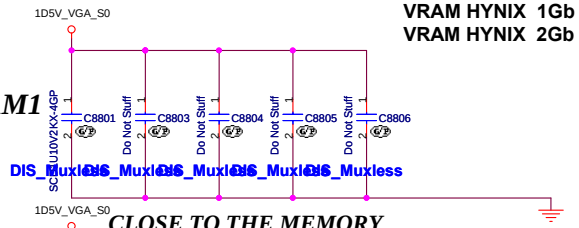
SB to -1



VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
VRAM HYNIX 2Gb VR.2GB0G.001

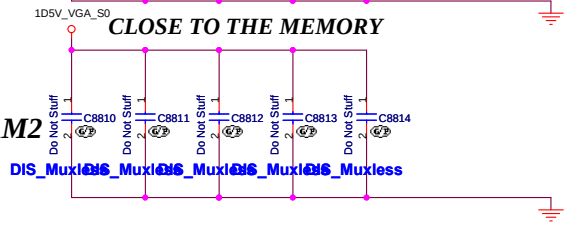
DG requires 4x0.1uF and 8x1.0uF per VRAM chip

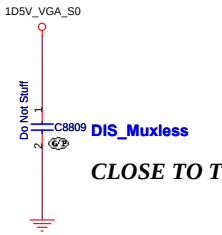
FOR VRAM1



CLOSE TO THE MEMORY

FOR VRAM2





CLOSE TO THE MEMORY

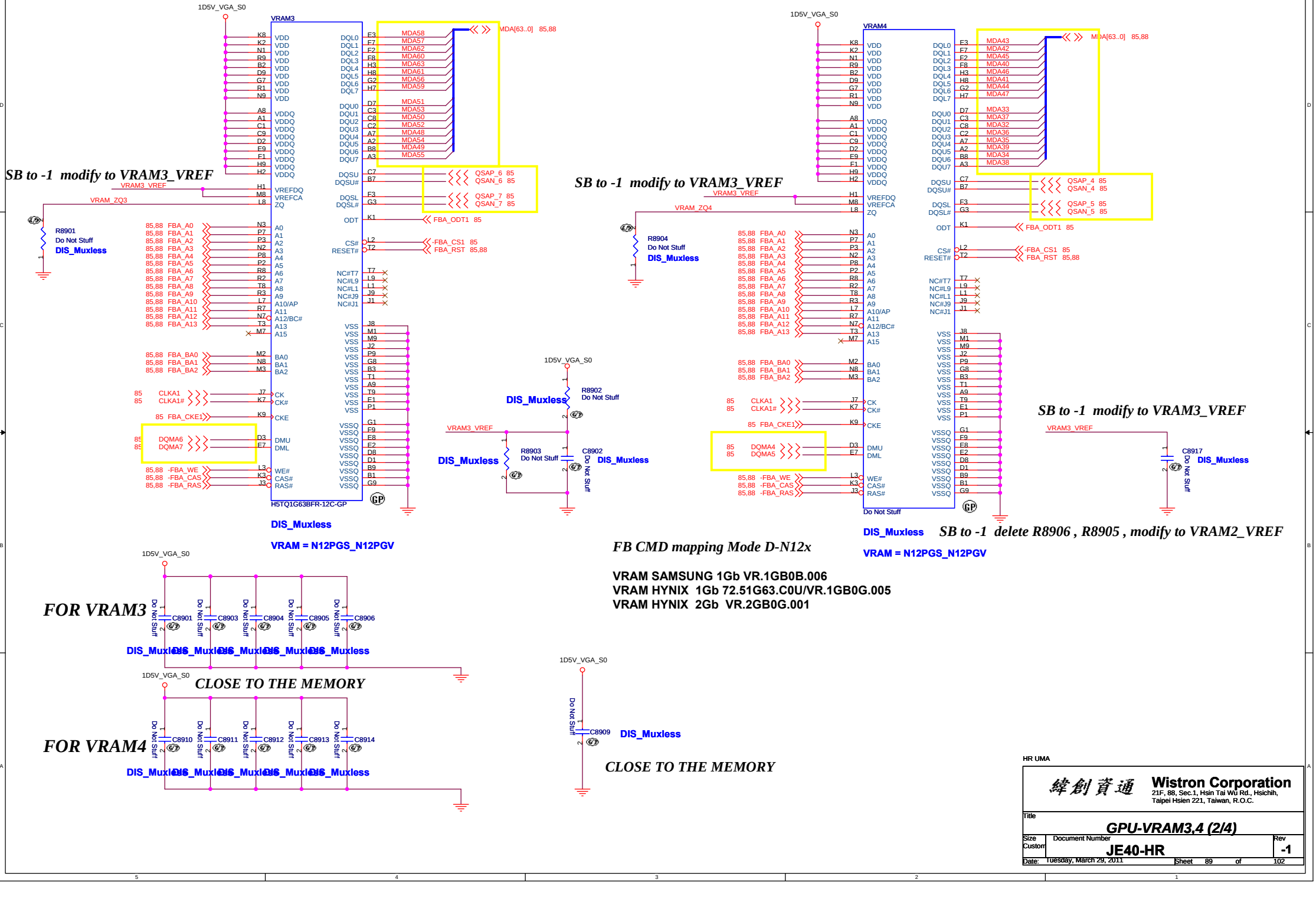
HR UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM1,2 (1/4)

Size: Custom | Document Number: JE40-HR | Rev: -1

Date: Tuesday, March 29, 2011 | Sheet 88 of 102



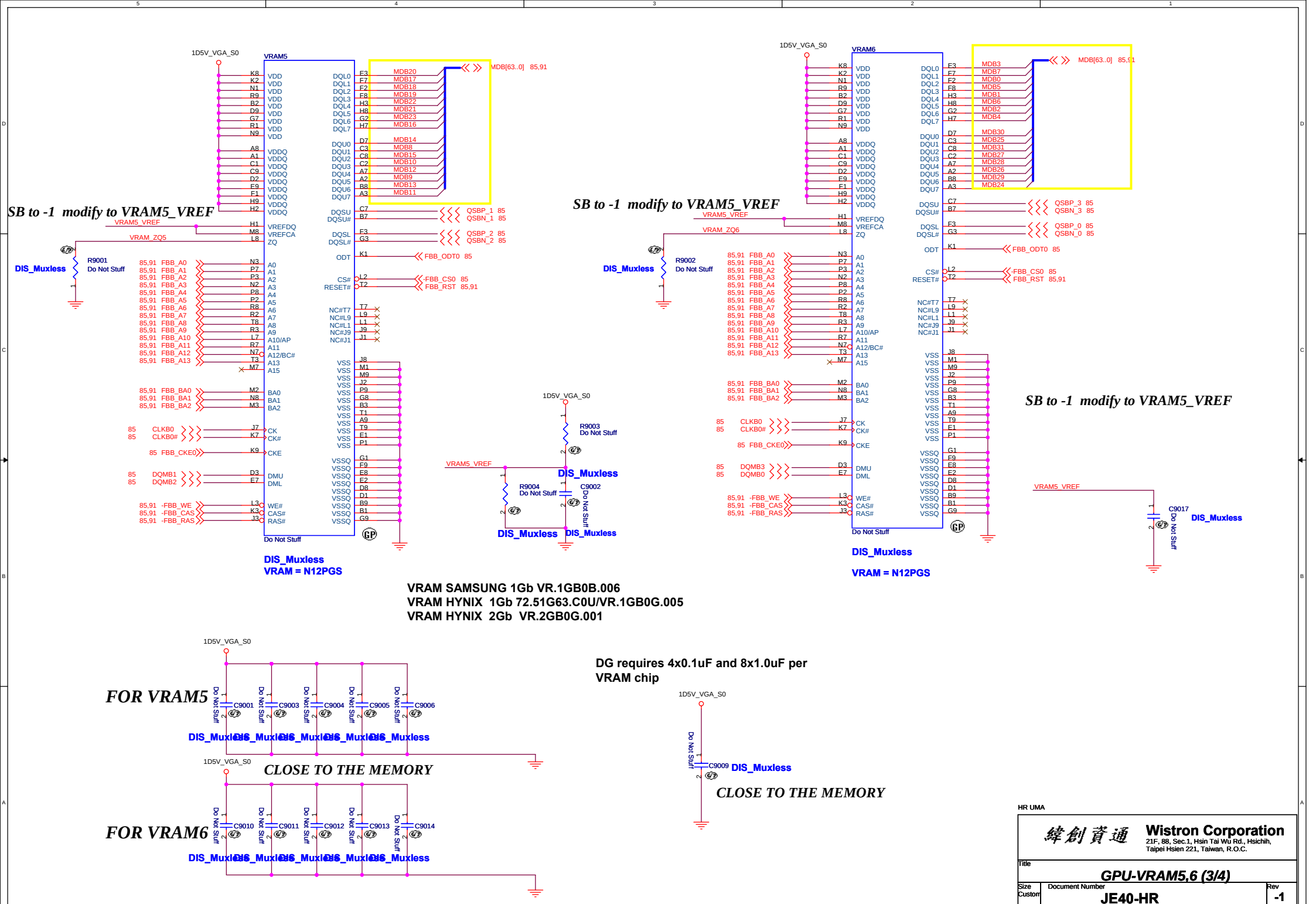
HR UMA

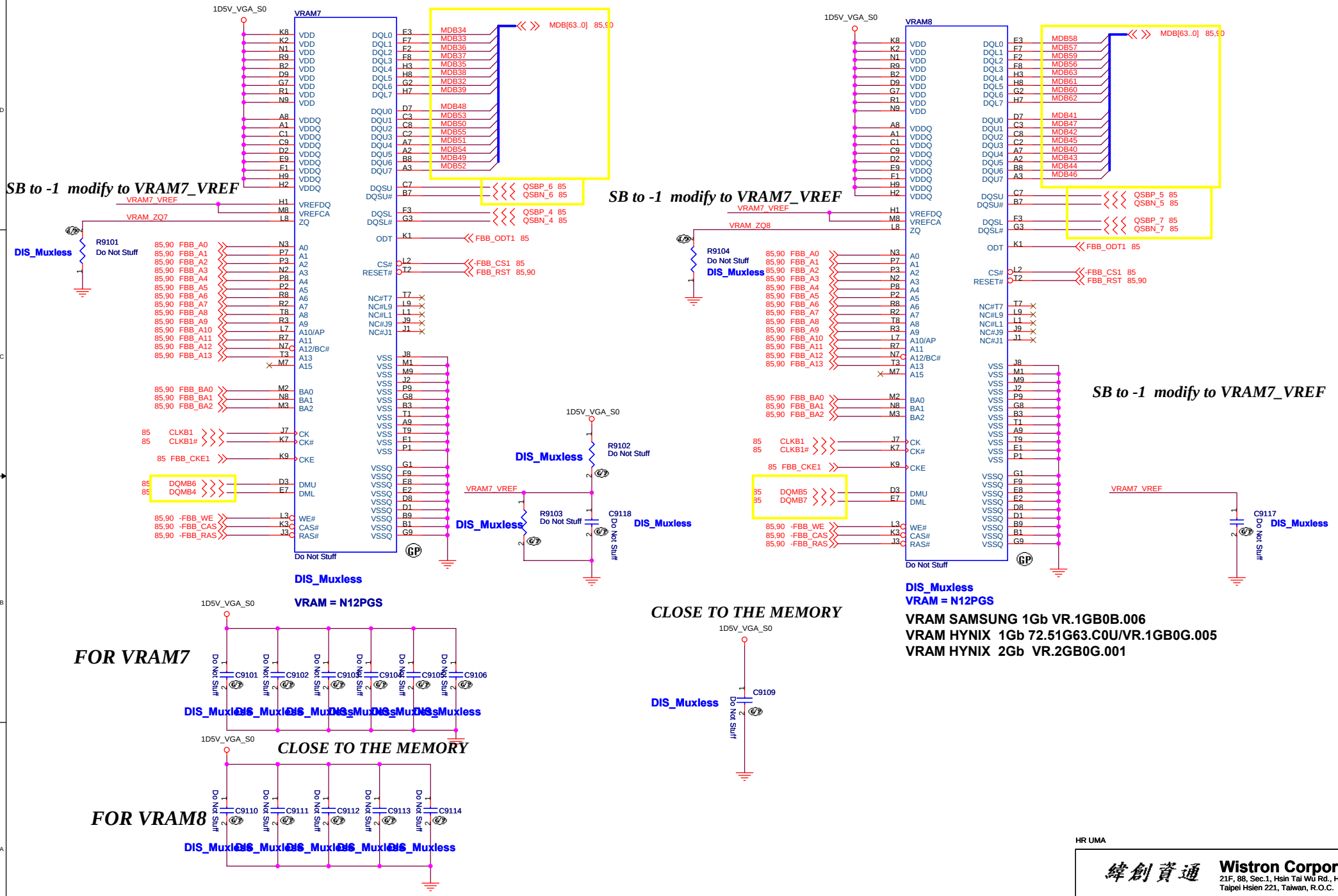
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM3,4 (2/4)

Size: Custom | Document Number: JE40-HR | Rev: -1

Date: Tuesday, March 29, 2011 | Sheet 89 of 102

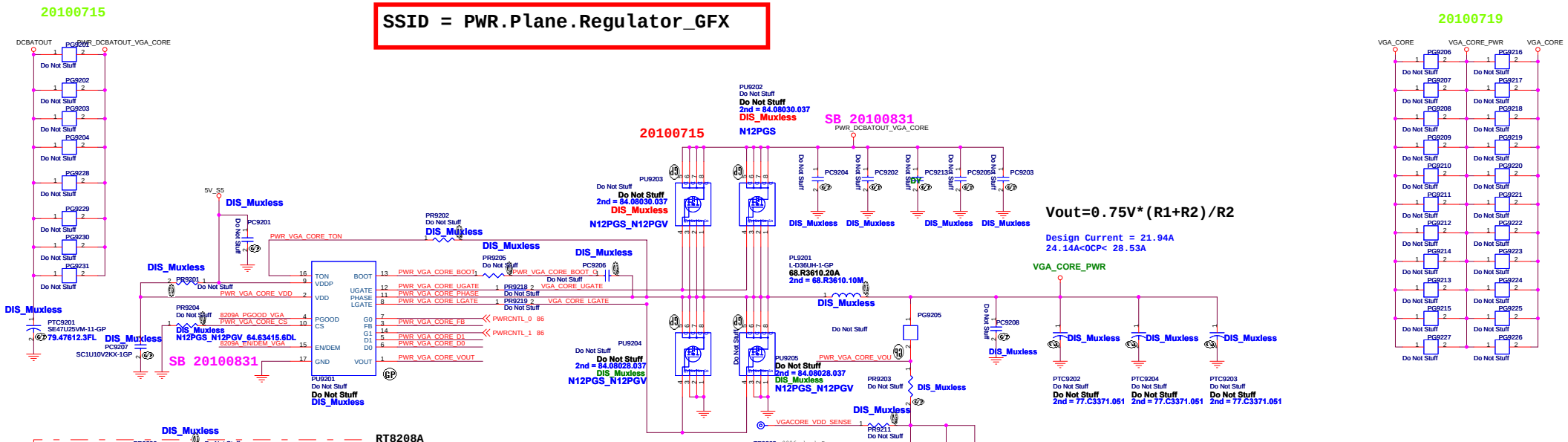

VRAM5
VRAM6
1D5V_VGA_S0
SB to -1 modify to VRAM5_VREF
VRAM5_VREF
VRAM_ZQ5
VRAM_ZQ6
R9001
R9002
R9003
R9004
C9002
C9017
Do Not Stuff
DIS_Muxless
MDB[63..0] 85,91
QSBP_1 85
QSBN_1 85
QSBP_2 85
QSBN_2 85
QSBP_3 85
QSBN_3 85
QSBP_0 85
QSBN_0 85
FBB_ODT0 85
FBB_CS0 85
FBB_RST 85,91
VRAM = N12PGS
VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
VRAM HYNIX 2Gb VR.2GB0G.001
DG requires 4x0.1uF and 8x1.0uF per VRAM chip
FOR VRAM5
FOR VRAM6
C9001
C9003
C9004
C9005
C9006
C9010
C9011
C9012
C9013
C9014
C9009
CLOSE TO THE MEMORY
HR UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
GPU-VRAM5,6 (3/4)
Size Custom
Document Number
JE40-HR
Rev -1
Date: Tuesday, March 29, 2011
Sheet 90 of 102



HR UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**GPU-VRAM7,8 (4/4)**
Size: Custom	Document Number: **JE40-HR**	Rev: **-1**
Date: Tuesday, March 29, 2011	Sheet 91 of 102

SSID = PWR.Plane.Regulator_GFX



P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
P8 , P12	L	L	0.825V
P0 - HOT	L	H	0.975V
P0 - COLD	H	L	1.00V
	H	H	

P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
P8 , P12	L	L	0.85V
P0 - HOT	L	H	1.00V
P0 - COLD	H	L	1.025V
	H	H	

HR UMA

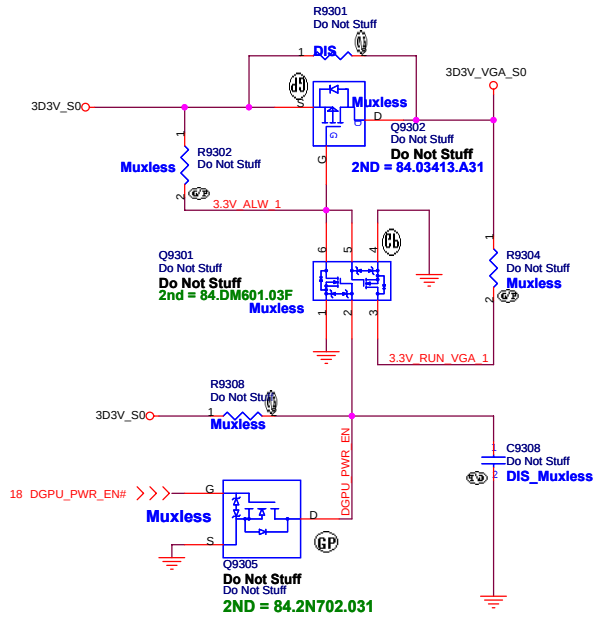
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8208B +VGA CORE

Size: Custom | Document Number: JE40-HR | Rev: -1

Date: Tuesday, March 29, 2011 | Sheet 92 of 102

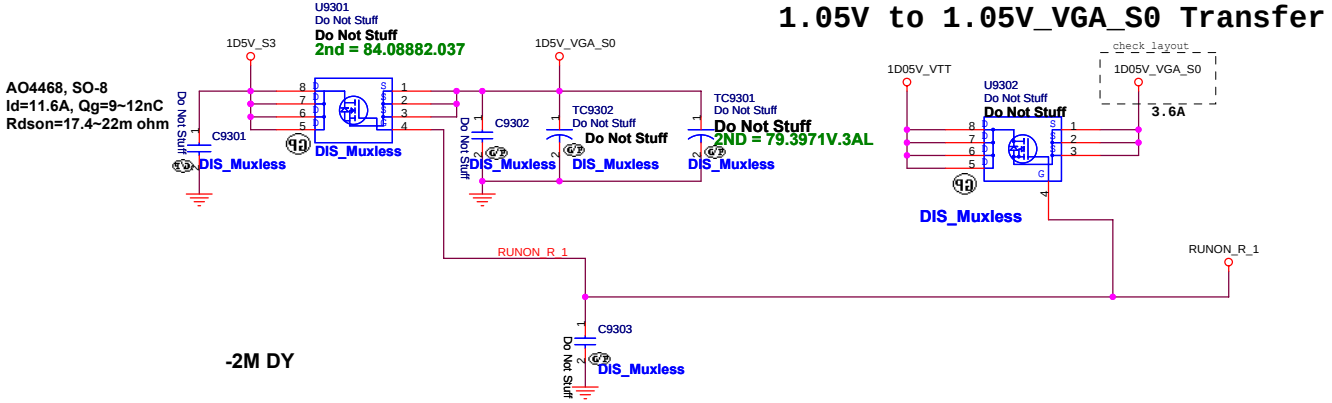
+3VS to 3.3V_DELAY Transfer

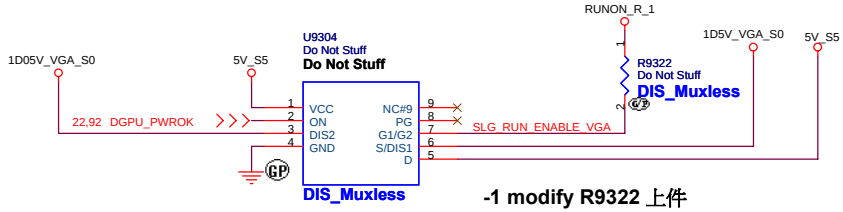


1D5V_VGA_S0

SB modify to 84.03006.A37

1.05V to 1.05V_VGA_S0 Transfer

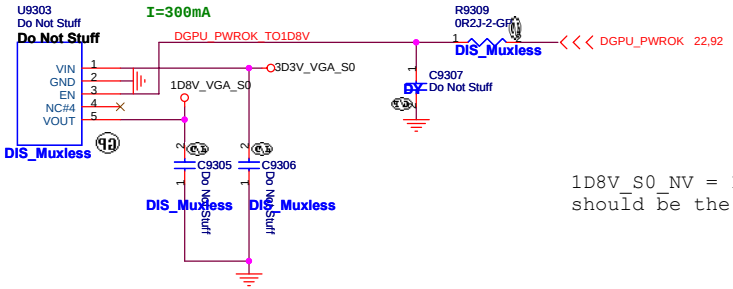




-1 modify R9322 上件

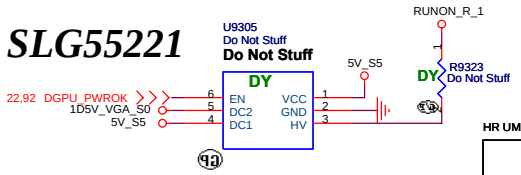
RT9025 for 1D8V_VGA

+3VS to 1.8V Transfer



1D8V_S0_NV = IFPA_IOVDD & IFPB_IOVDD, it should be the latest ramp up rail.

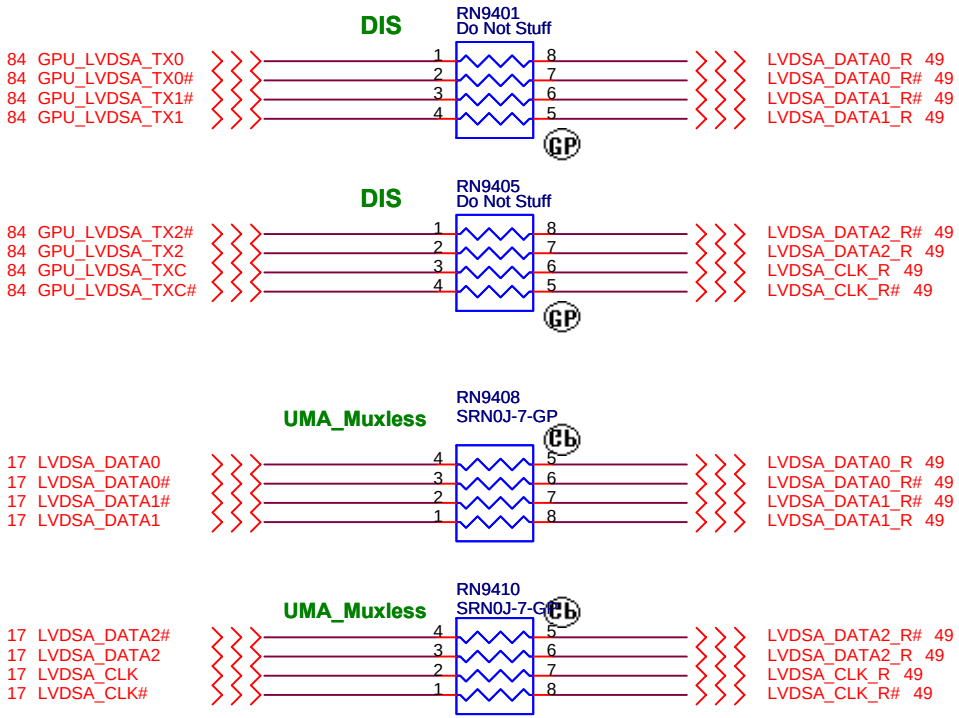
-1 co-layout SLG55221

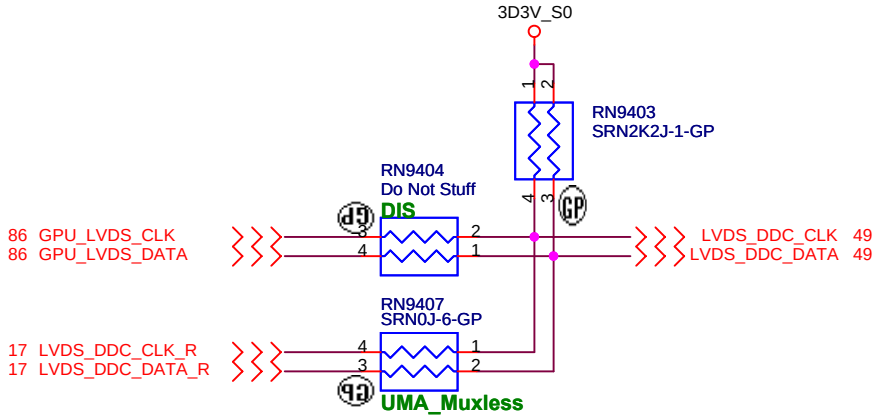


HR UMA

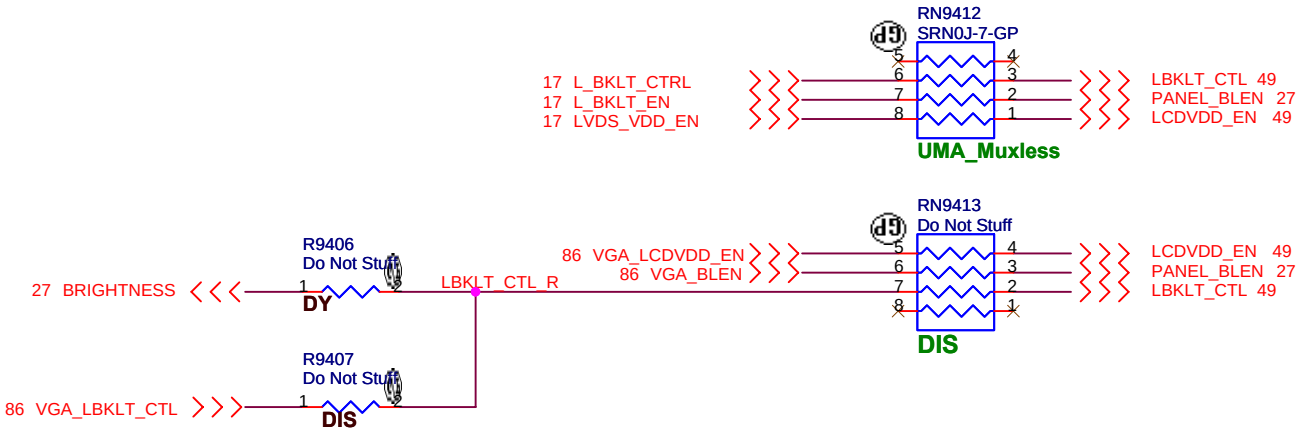
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	DISCRETE VGA POWER	
Size: Custom	Document Number: JE40-HR	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 93 of 102	

LVDS Channel A





Panel BL brightness/Power En/BL En



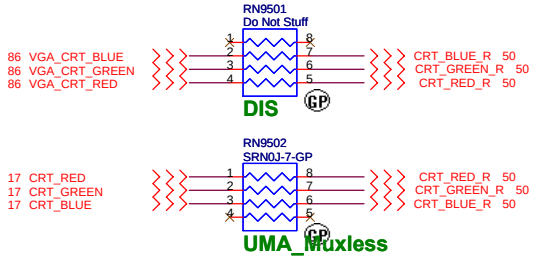
HR UMA

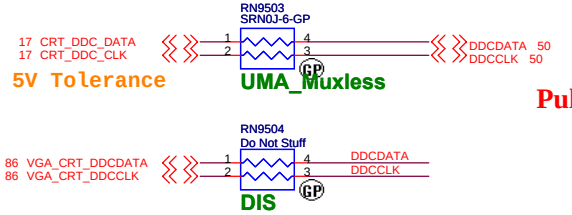
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LVDS_Switch	
Size A4	Document Number JE40-HR	Rev -1
Date: Tuesday, March 29, 2011	Sheet 94 of 102	

Close to CRT Board CONN

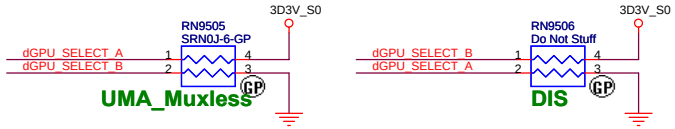
CRT DDCDATA & DDCCLK





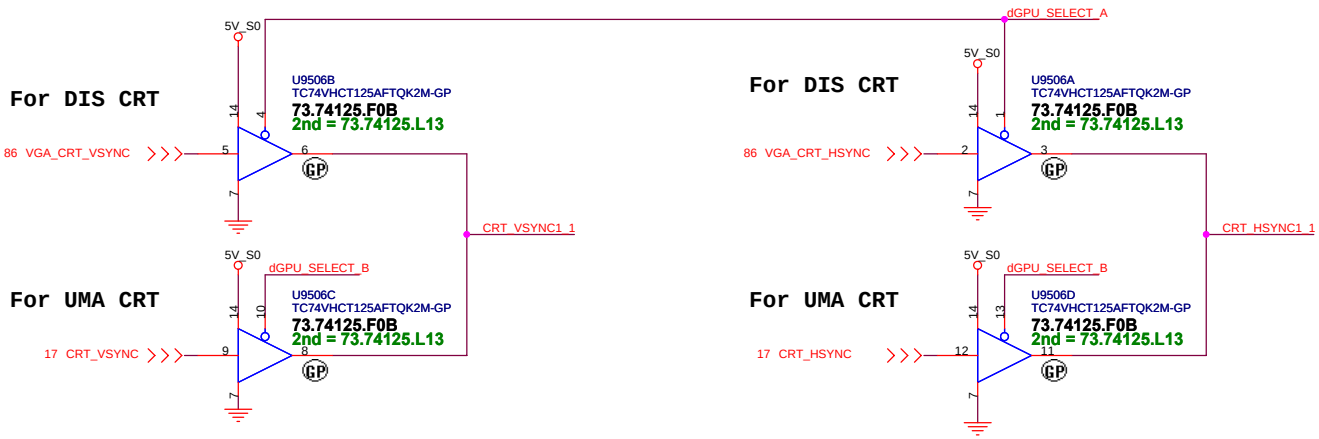
Pull high 在CRT

SB to -1 modify 4 port Logic



CRT Hsync & Vsync level shift

L=>B0 -DIS
H=>B1 -UMA



SB to -1 modify R9503,R9504 to 10 ohm

HR UMA

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	CRT Switch	
Size A3	Document Number JE40-HR	Rev -1
Date: Tuesday, March 29, 2011	Sheet 95 of 102	

SSID = SDIO

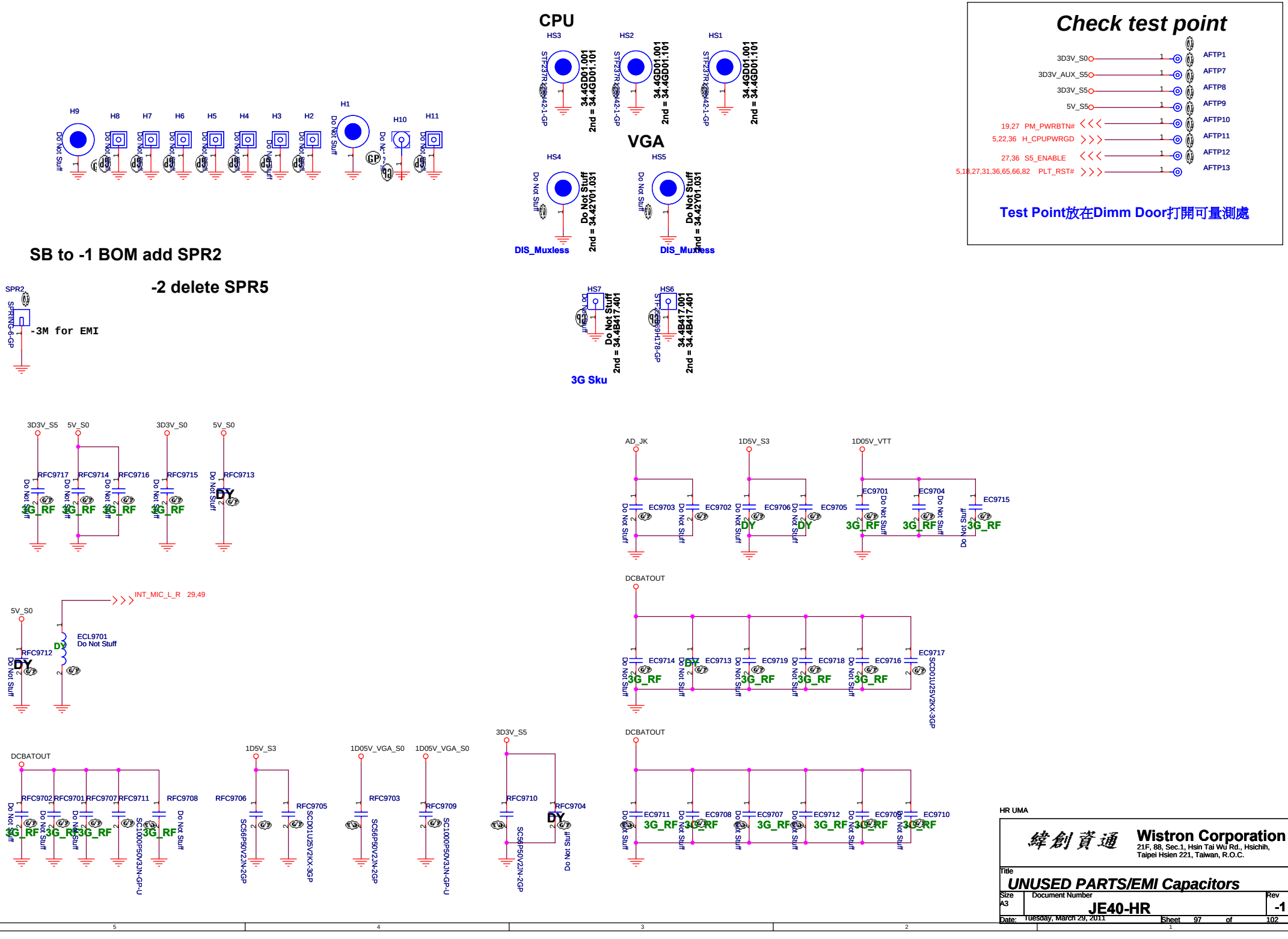
HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

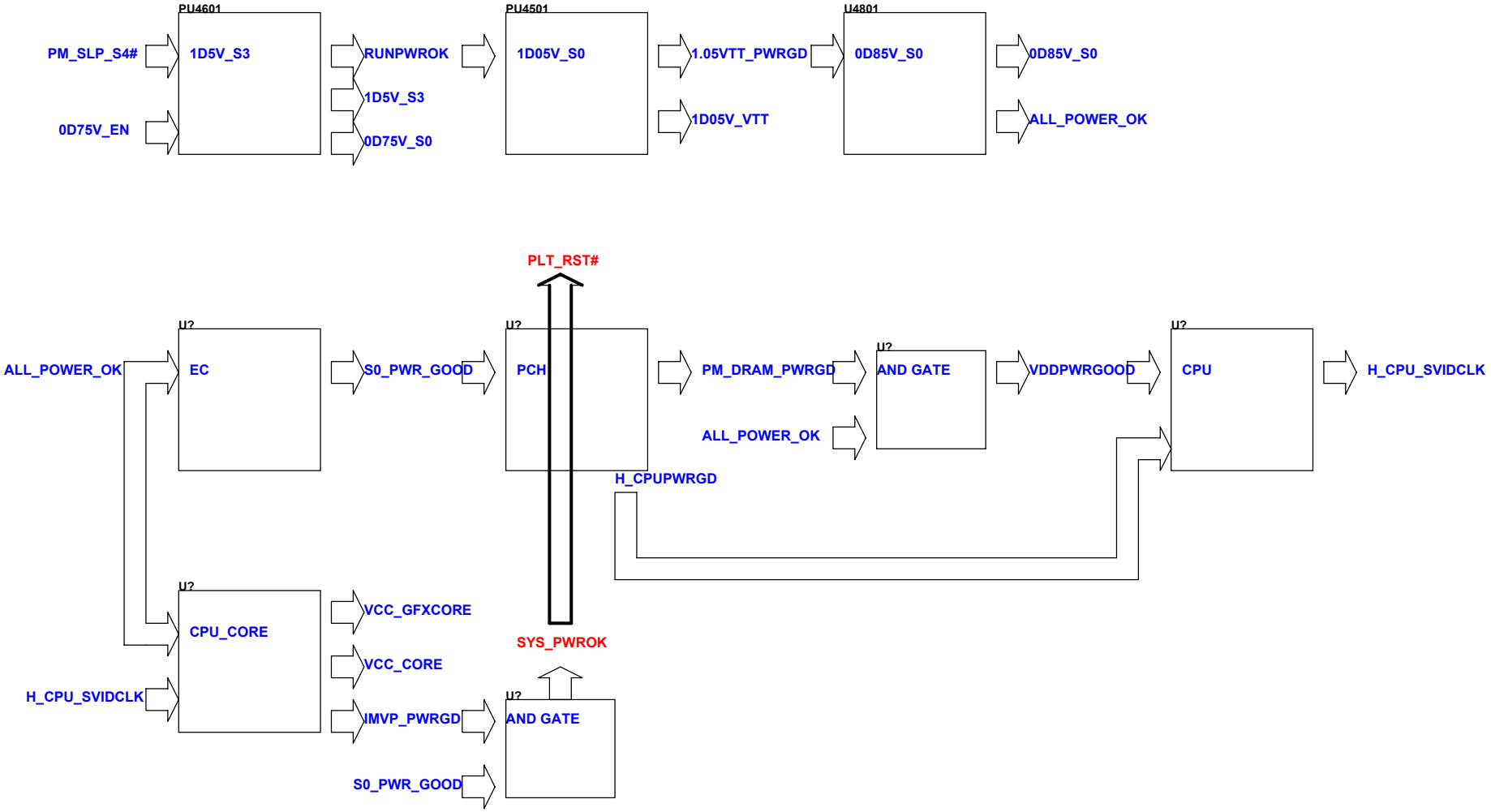
Title: TOUCH PANEL

Size: A2 | Document Number: JE40-HR | Rev: -1

Date: Tuesday, March 29, 2011 | Sheet 96 of 102


CPU
HS3
HS2
HS1
34.4GD01.001
2nd = 34.4GD01.101
VGA
HS4
HS5
Do Not Stuff
2nd = 34.42Y01.031
DIS_Muxless
H9
H8
H7
H6
H5
H4
H3
H2
H1
H10
H11
Do Not Stuff
SB to -1 BOM add SPR2
-2 delete SPR5
SPR2
SPRING-6-GP
-3M for EMI
HS7
HS6
2nd = 34.4B417.401
3G Sku
Check test point
3D3V_S0
3D3V_AUX_S5
3D3V_S5
5V_S5
19,27 PM_PWRBTN#
5,22,36 H_CPUPWRGD
27,36 S5_ENABLE
5,18,27,31,36,65,66,82 PLT_RST#
AFTP1
AFTP7
AFTP8
AFTP9
AFTP10
AFTP11
AFTP12
AFTP13
Test Point放在Dimm Door打開可量測處
3D3V_S5
5V_S0
3D3V_S0
RFC9717
RFC9714
RFC9716
RFC9715
RFC9713
3G_RF
DY
AD_JK
1D5V_S3
1D05V_VTT
EC9703
EC9702
EC9706
EC9705
EC9701
EC9704
EC9715
INT_MIC_L_R 29,49
ECL9701
RFC9712
DCBATOUT
EC9714
EC9713
EC9719
EC9718
EC9716
EC9717
SCD01U25V2KX-3GP
RFC9702
RFC9701
RFC9707
RFC9711
RFC9708
SC1000P50V3JN-GP-U
1D5V_S3
1D05V_VGA_S0
RFC9706
RFC9705
RFC9703
RFC9709
RFC9710
RFC9704
SC56P50V2JN-2GP
EC9711
EC9708
EC9707
EC9712
EC9709
EC9710
HR UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
UNUSED PARTS/EMI Capacitors
Size
A3
Document Number
JE40-HR
Rev
-1
Date: Tuesday, March 29, 2011
Sheet 97 of 102

Power Sequence



HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Change History*

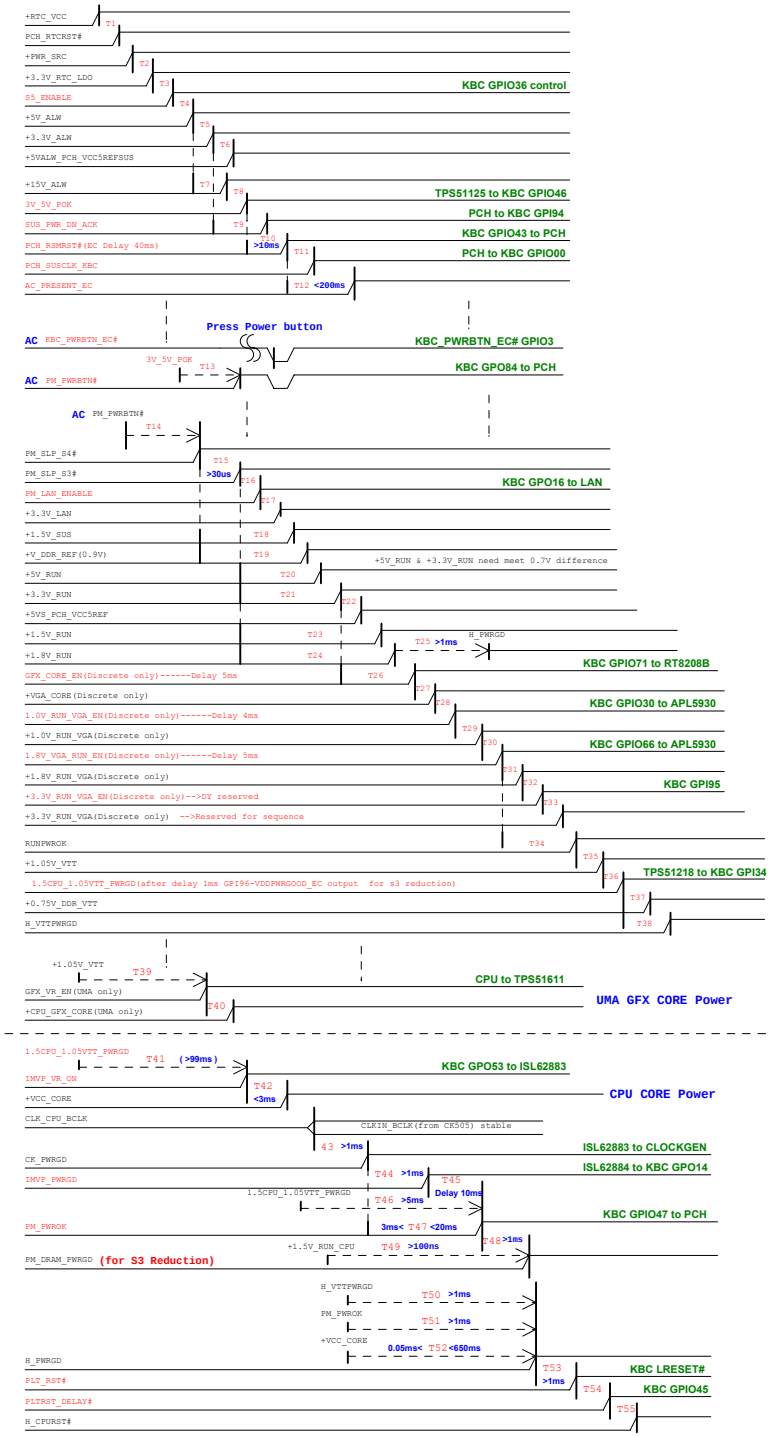
Size	Document Number	Rev
A3	JE40-HR	-1

Date: Tuesday, March 29, 2011 Sheet 98 of 102

Intel-Power Up Sequence

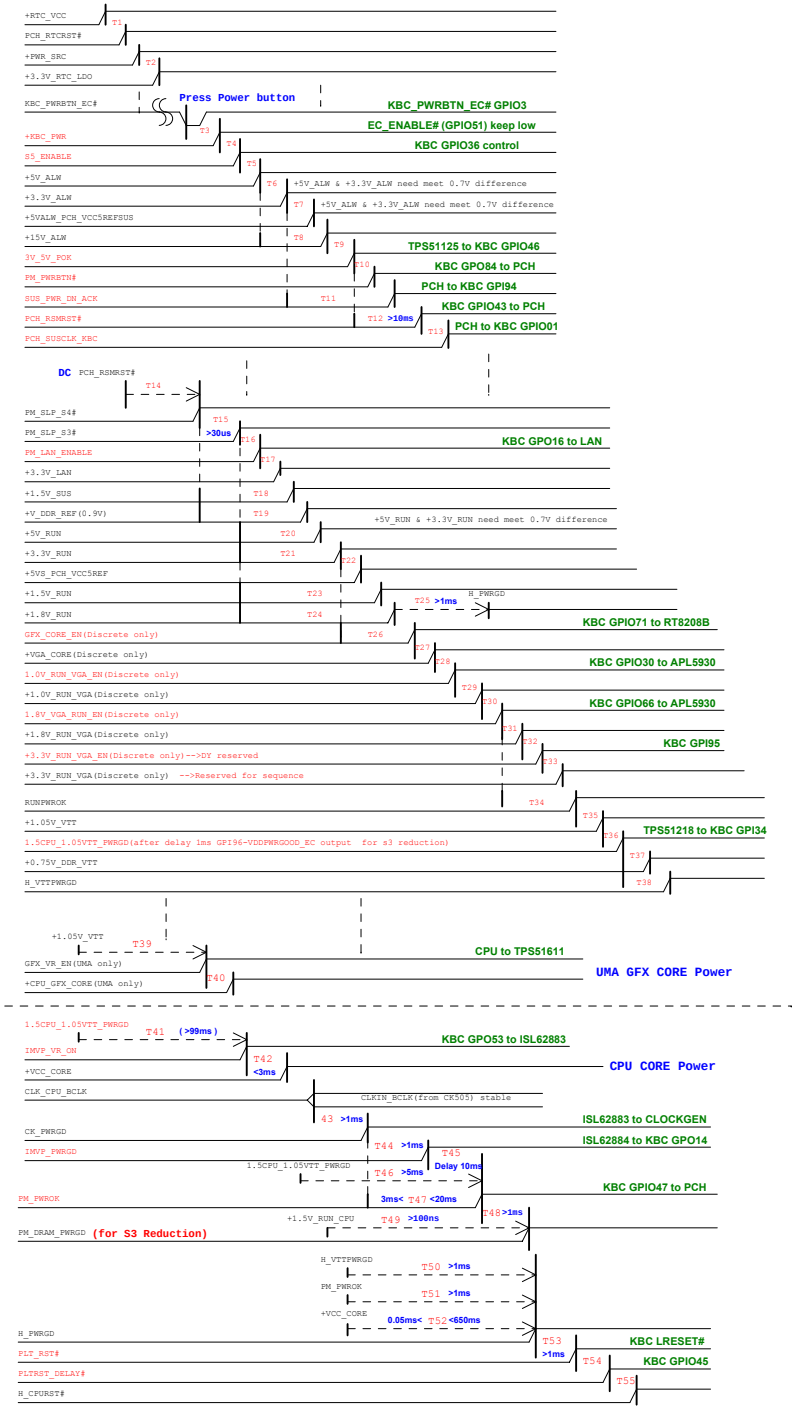
(AC mode)

red word: KBC GPIO



(DC mode)

red word: KBC GPIO



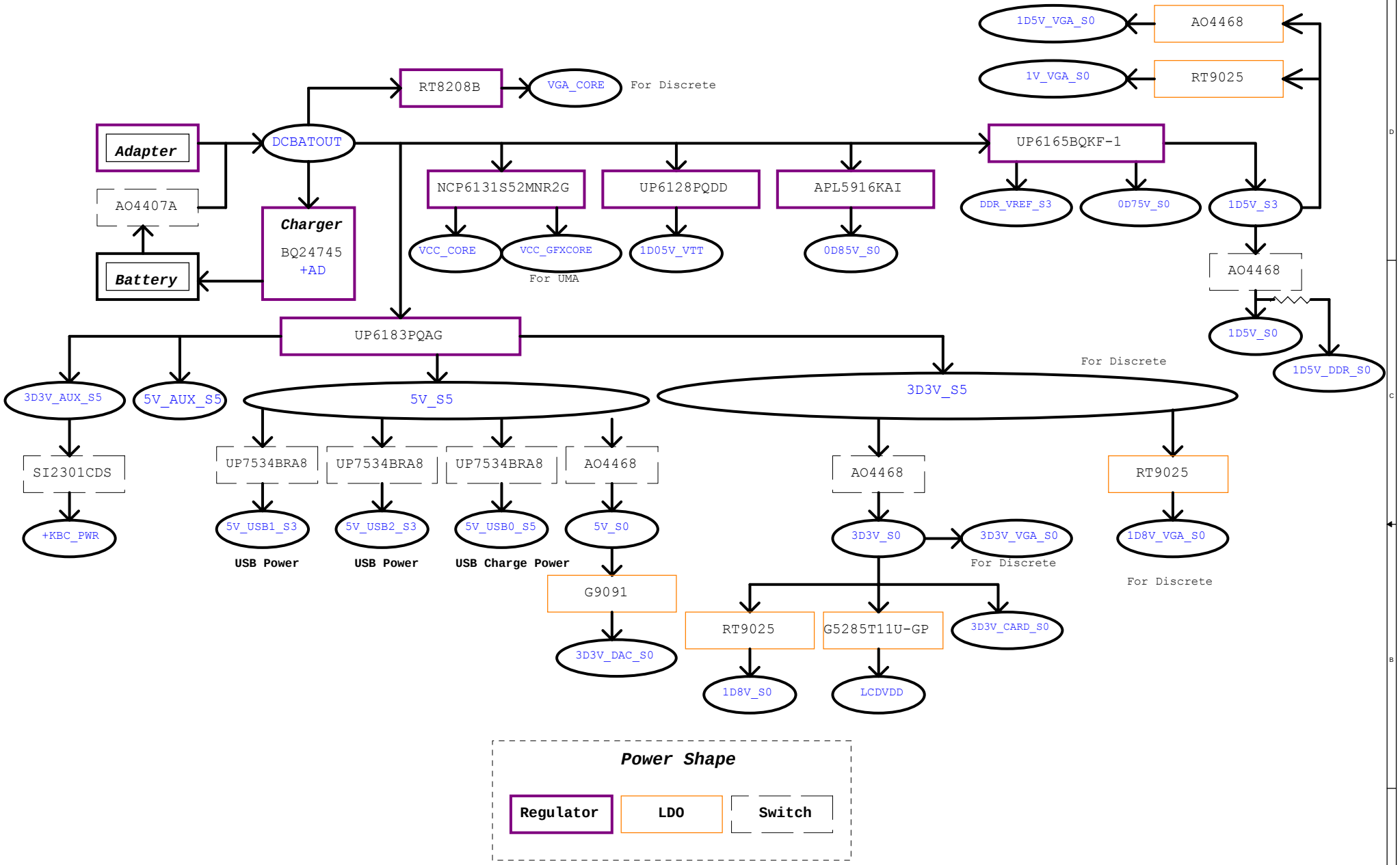
HR UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Sequence

Size: A1 | Document Number: JE40-HR | Rev: -1

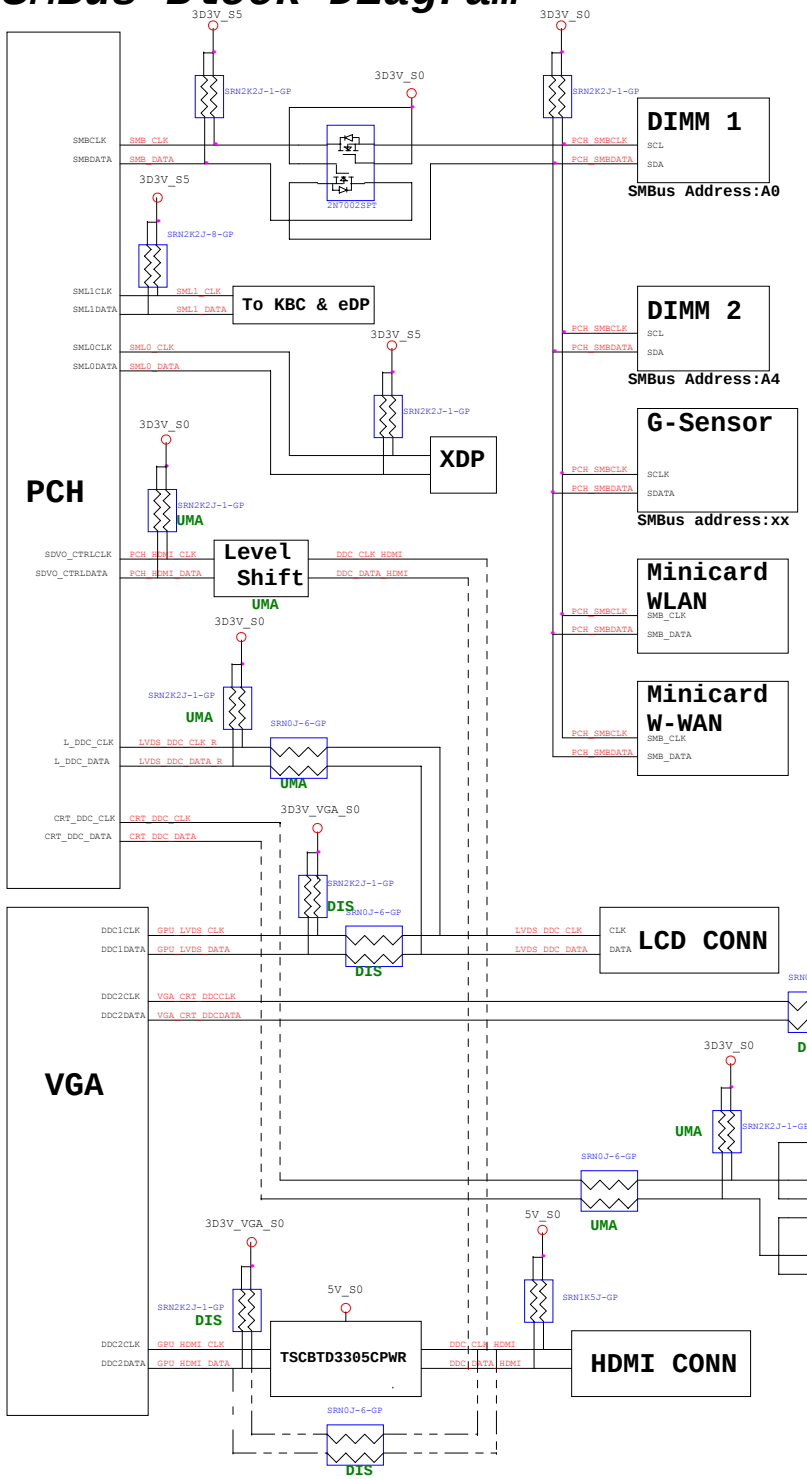
Date: Tuesday, March 25, 2014 | Sheet 99 of 102



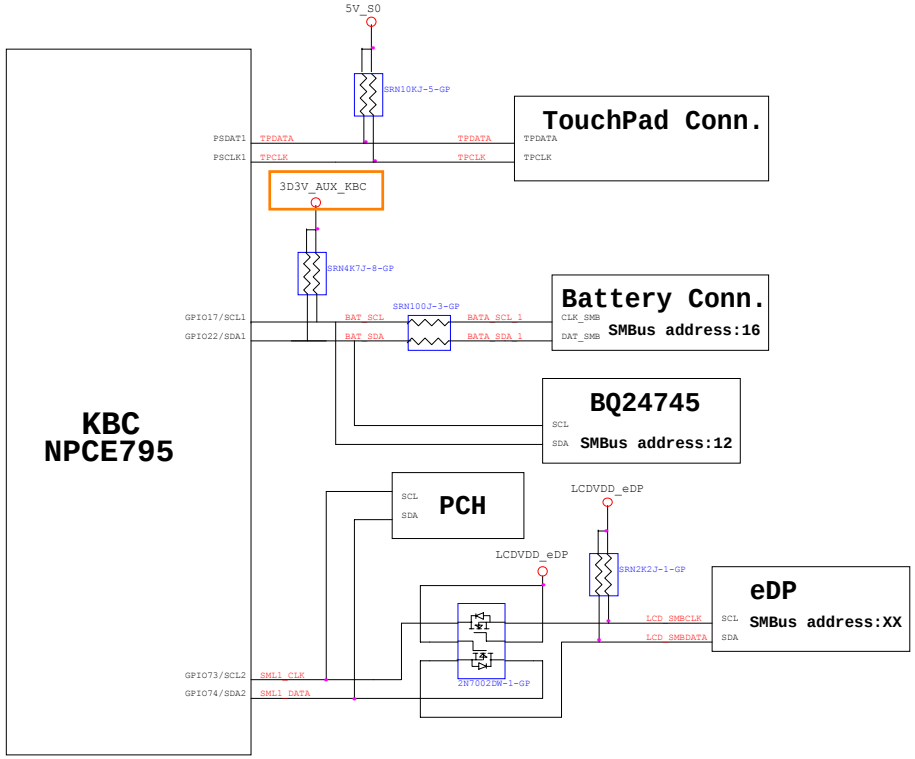
HR UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Power Block Diagram***	
Size A3	Document Number **JE40-HR**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 100 of 102	

PCH SMBus Block Diagram



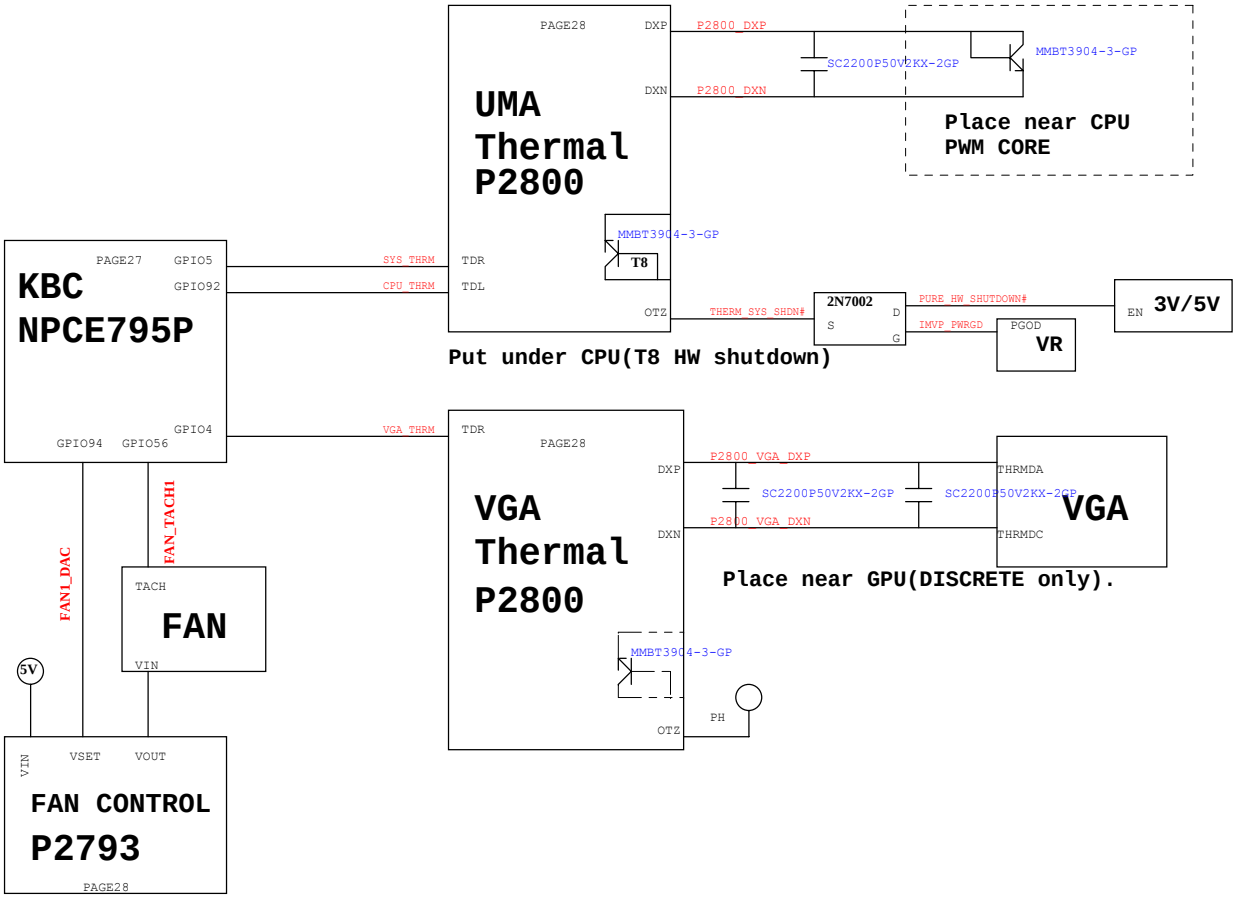
KBC SMBus Block Diagram



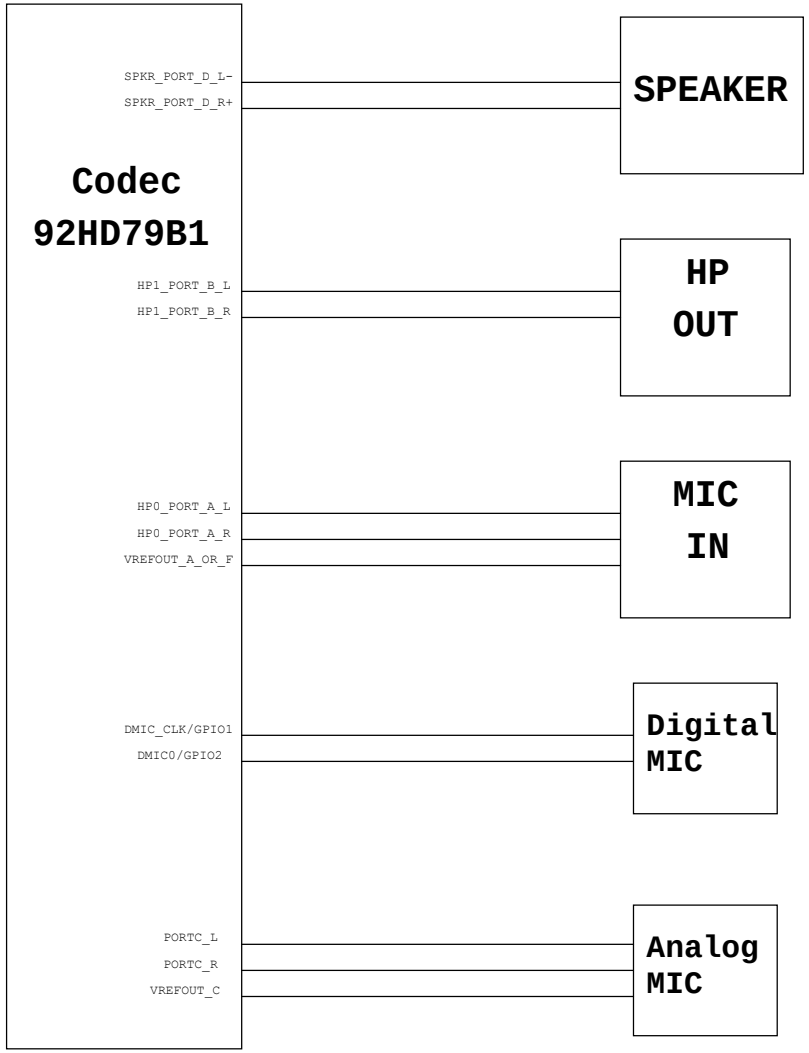
HR UMA

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	SMBUS Block Diagram	
Size A2	Document Number JE40-HR	Rev -1
Date: Tuesday, March 29, 2011	Sheet 101 of 102	

Thermal Block Diagram



Audio Block Diagram



HR UMA

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Thermal/Audio Block Diagram	
Size Custom	Document Number JE40-HR	Rev -1
Date: Tuesday, March 29, 2011	Sheet 102 of 102	