

Compal Confidential

Schematics Document

Intel Huron River Platform
Sandy Bridge (Dual Core BGA 1023) With
Cougar Point Core Logic

LA-7401P

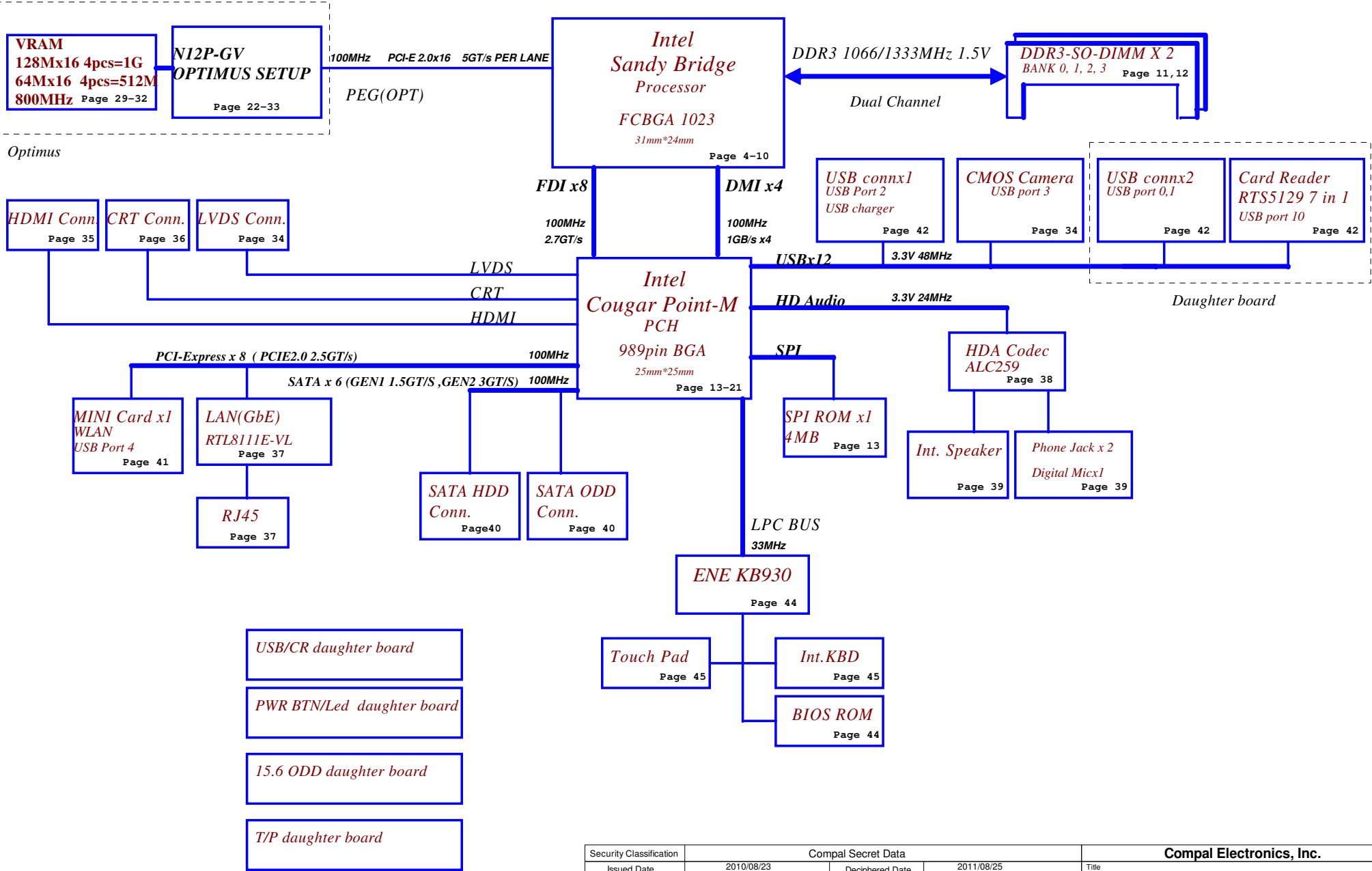
2011-03-24

REV:1.0

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Model Name : PAJ80(14" UMA/Dis)/PAJ90(15.6" UMA/Dis)
File Name : LA-7401P



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				Rev	1.0

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
BATT+	Battery power supply (12.6V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS_DGPU	+1.05VS to +1.05VS_DGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS	+VCCPP to +1.05VS switched power rail for CPU,PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+VRAM_1.5VS	+1.5V to +VRAM_1.5VS power rail for GPU	ON	OFF	OFF
+1.8VS	+5VALW to 1.8VS switched power rail to CPU,PCH	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+LAN_IO	+3VALW to +LAN_IO power rail for LAN	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

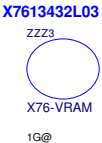
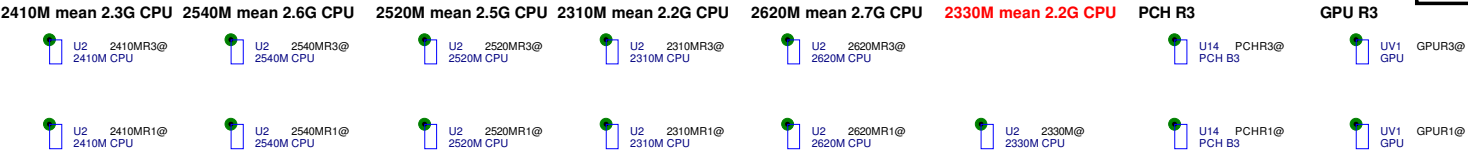
STATE	SIGNAL							
	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

USB 2.0	USB 1.1	Port	2 External USB Port
EHCI1	UHCI0	0	CONN
		1	CONN
		2	CONN
	UHCI1	3	Camera
		4	Mini Card(WLAN/BT)
		5	NA
EHCI2	UHCI2	6	
		7	
		8	NA
	UHCI3	9	NA
		10	Card Reader
		11	
		12	
		13	

BTO Option Table

BTO Item	BOM Structure
Optimus	OPT@
Connector	CONN@
Unpop	@
14" PCB	14@
15.6" PCB	15@
UMA PCB	UMA@
Dis PCB (Optimus)	OPT@
X76 512M	512M@
X76 1G	1G@



PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b

EC SM Bus1 Address

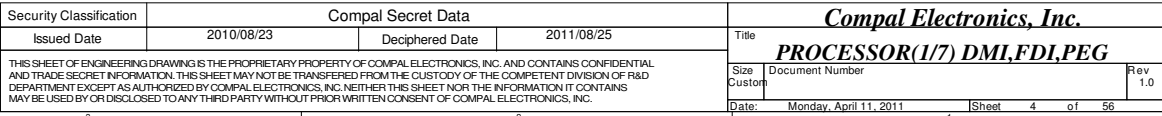
Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b

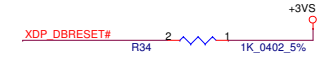
EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b
+3VS	NVIDIA GPU	9E H	1001 1110 b

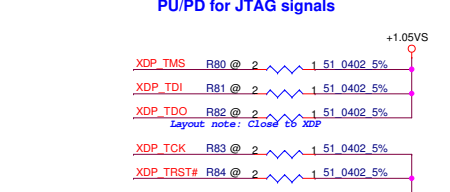
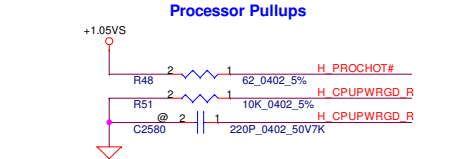
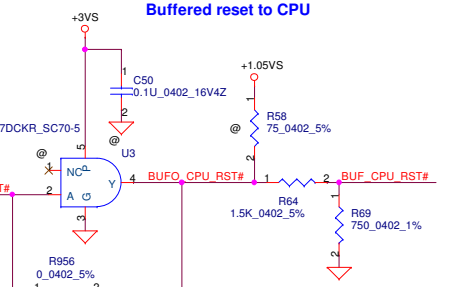
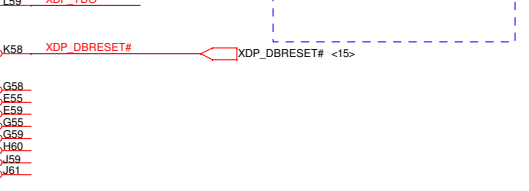
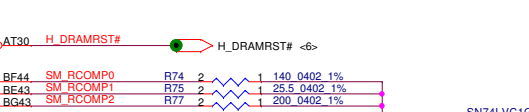
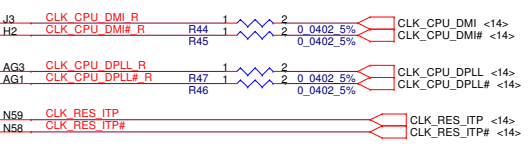
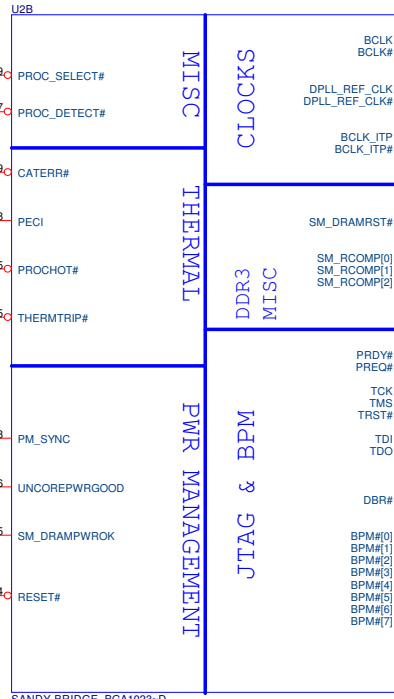
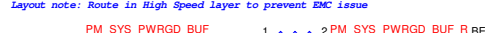
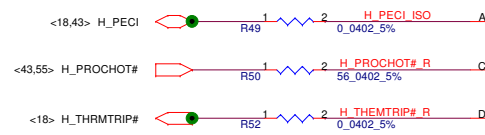
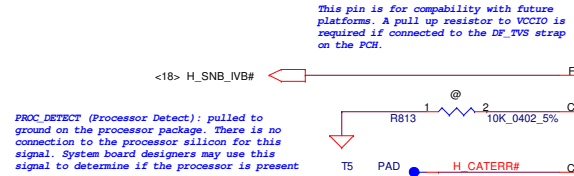
SMBUS Control Table

	SOURCE	BATT	CPU THERMAL SENSOR	SODIMM 0 SODIMM 1	WLAN WWAN	LCD DDC ROM	HDMI DDC ROM	PCH	GPU
EC_SMB_CK1	KB930	V							
EC_SMB_DA1	KB930							V	V
EC_SMB_CK2	KB930								
EC_SMB_DA2	KB930								
PCH_LCD_CLK	PCH					V			
PCH_LCD_DATA	PCH								
SDVO_SCLK	PCH						V		
SDVO_SDATA	PCH								
PCH_SMBCLK	PCH			V	V				
PCH_SMBDATA	PCH								

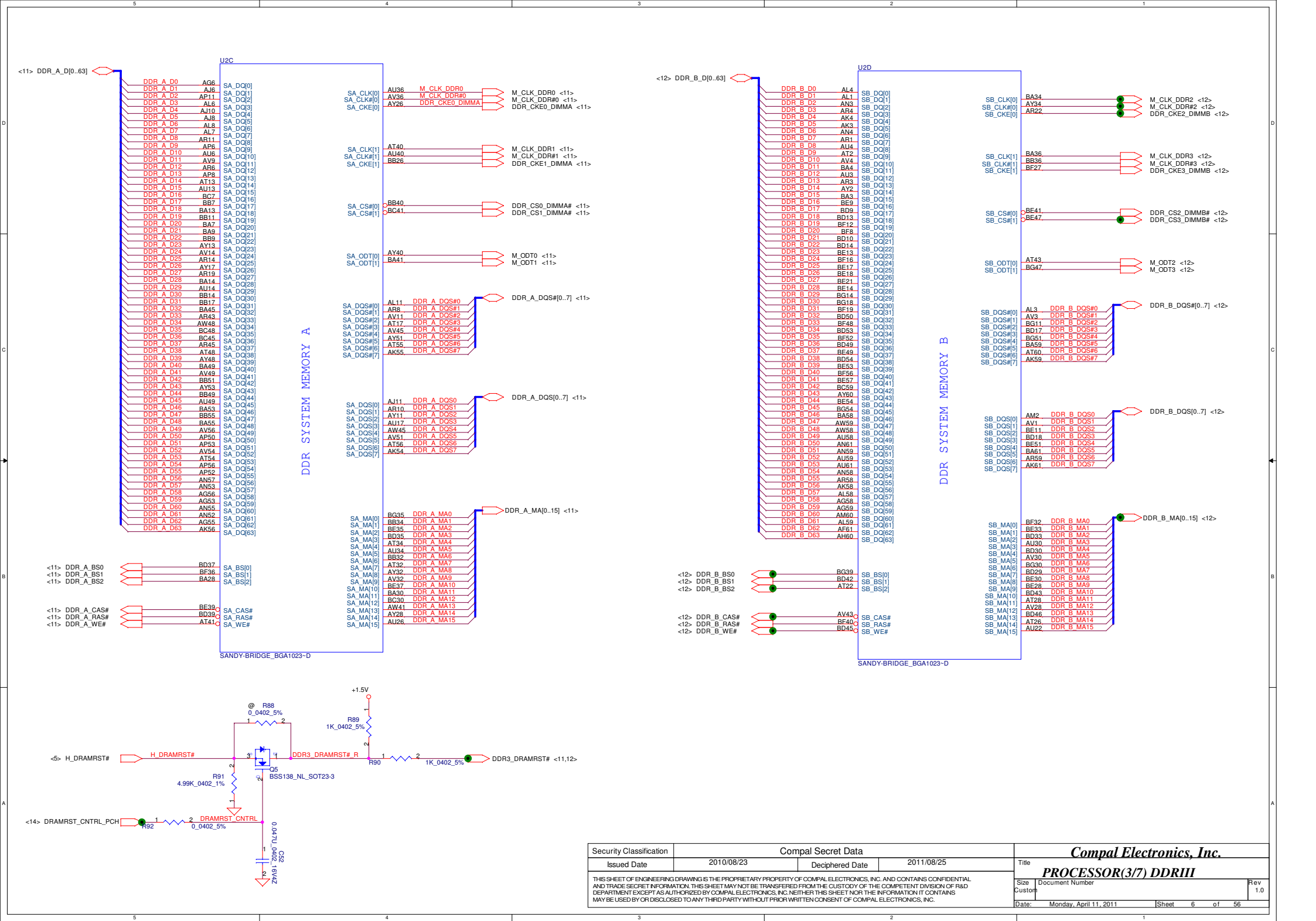


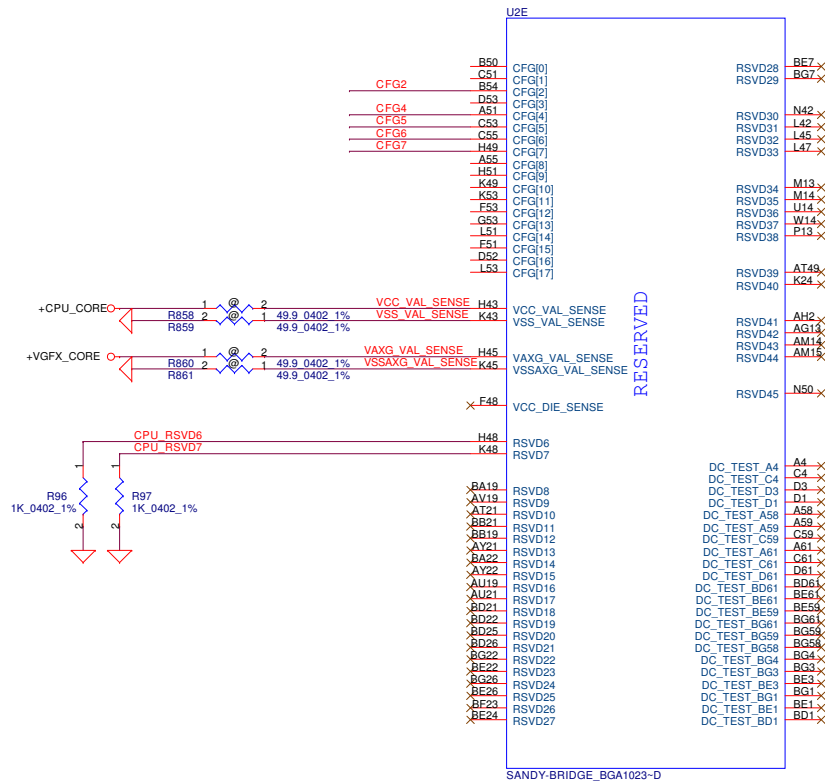


PVT:Remove XDP connector for ESD request

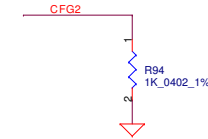


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1.0				Date: Monday, April 11, 2011				Sheet 5 of 56			

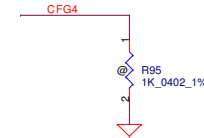




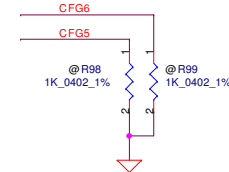
CFG Straps for Processor



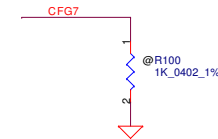
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition ★ 0: Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port ★ 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps	
CFG[6:5]	★ 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

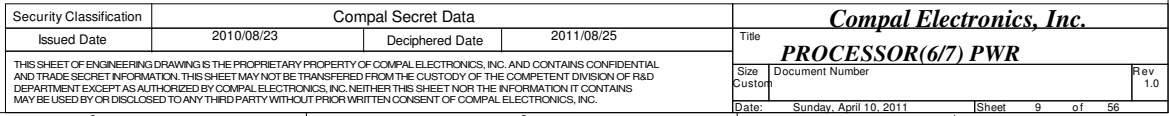
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Issued Date	2010/08/23	Deciphered Date	2011/08/25	Title	PROCESSOR(47) RSVD,CFG
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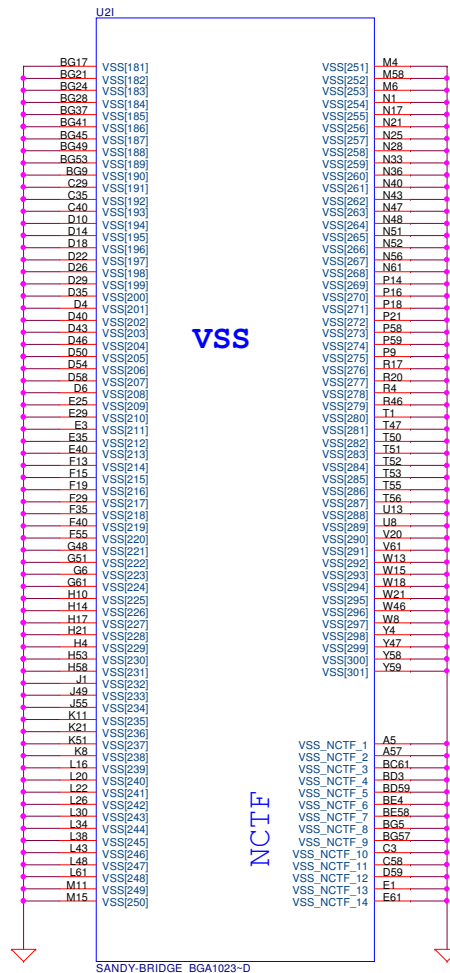
Compal Electronics, Inc.		
Title	PROCESSOR(5/7) PWR,BYPASS	
Size Custom	Document Number	Rev 1.0
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The schematic diagram illustrates the power plane for the SANDY-BRIDGE_BGA1023-03, featuring several key components and sections:

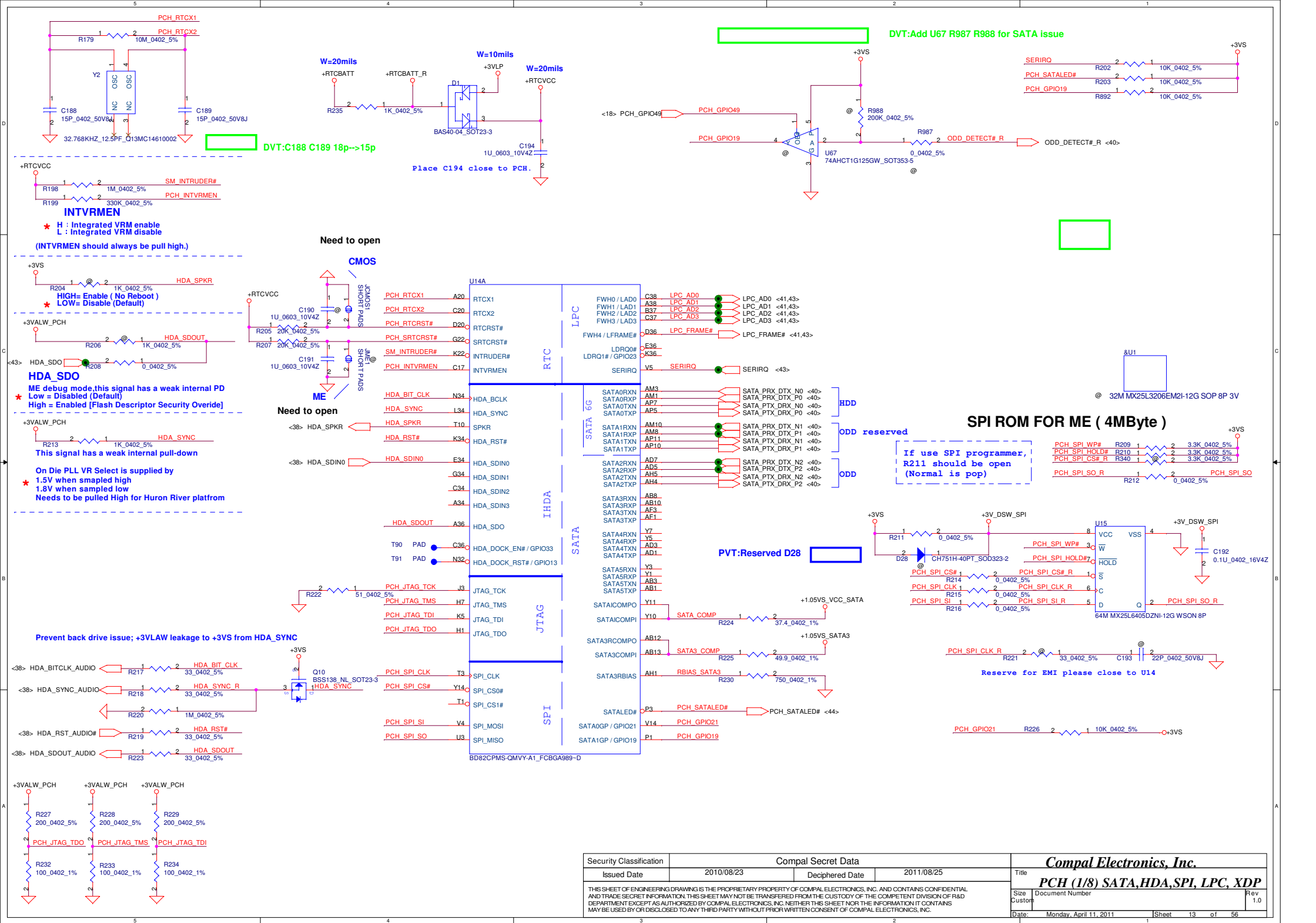
- Power Rails:**
 - 1.5V RAILS:** Includes VDDQ[0] through VDDQ[26] and VDDQ[1] through VDDQ[26].
 - 1.8V RAIL:** Includes VCCSA[1] through VCCSA[16] and VCCSA[1] through VCCSA[16].
 - SA RAIL:** Includes VCCSA[1] through VCCSA[16] and VCCSA[1] through VCCSA[16].
- Decoupling Capacitors:**
 - Mid-Frequency Decoupling:** C110, C111, C112, C113, C114, C115, C116, C117, C118, C119, C120, C121, C122, C123, C124, C125, C126, C127, C128, C129, C130, C131, C132, C133, C134, C135, C136, C137, C138, C139, C140, C141, C142, C143, C144, C145, C146, C147, C148, C149, C150, C151, C152, C153, C154, C155, C156, C157, C158, C159, C160, C161, C162, C163, C164, C165, C166, C167, C168, C169, C170, C171, C172, C173, C174, C175, C176, C177, C178, C179, C180, C181, C182, C183, C184, C185, C186, C187, C188, C189, C190, C191, C192, C193, C194, C195, C196, C197, C198, C199, C200, C201, C202, C203, C204, C205, C206, C207, C208, C209, C210, C211, C212, C213, C214, C215, C216, C217, C218, C219, C220, C221, C222, C223, C224, C225, C226, C227, C228, C229, C230, C231, C232, C233, C234, C235, C236, C237, C238, C239, C240, C241, C242, C243, C244, C245, C246, C247, C248, C249, C250, C251, C252, C253, C254, C255, C256, C257, C258, C259, C260, C261, C262, C263, C264, C265, C266, C267, C268, C269, C270, C271, C272, C273, C274, C275, C276, C277, C278, C279, C280, C281, C282, C283, C284, C285, C286, C287, C288, C289, C290, C291, C292, C293, C294, C295, C296, C297, C298, C299, C300, C301, C302, C303, C304, C305, C306, C307, C308, C309, C310, C311, C312, C313, C314, C315, C316, C317, C318, C319, C320, C321, C322, C323, C324, C325, C326, C327, C328, C329, C330, C331, C332, C333, C334, C335, C336, C337, C338, C339, C340, C341, C342, C343, C344, C345, C346, C347, C348, C349, C350, C351, C352, C353, C354, C355, C356, C357, C358, C359, C360, C361, C362, C363, C364, C365, C366, C367, C368, C369, C370, C371, C372, C373, C374, C375, C376, C377, C378, C379, C380, C381, C382, C383, C384, C385, C386, C387, C388, C389, C390, C391, C392, C393, C394, C395, C396, C397, C398, C399, C400, C401, C402, C403, C404, C405, C406, C407, C408, C409, C410, C411, C412, C413, C414, C415, C416, C417, C418, C419, C420, C421, C422, C423, C424, C425, C426, C427, C428, C429, C430, C431, C432, C433, C434, C435, C436, C437, C438, C439, C440, C441, C442, C443, C444, C445, C446, C447, C448, C449, C450, C451, C452, C453, C454, C455, C456, C457, C458, C459, C460, C461, C462, C463, C464, C465, C466, C467, C468, C469, C470, C471, C472, C473, C474, C475, C476, C477, C478, C479, C480, C481, C482, C483, C484, C485, C486, C487, C488, C489, C490, C491, C492, C493, C494, C495, C496, C497, C498, C499, C500, C501, C502, C503, C504, C505, C506, C507, C508, C509, C510, C511, C512, C513, C514, C515, C516, C517, C518, C519, C520, C521, C522, C523, C524, C525, C526, C527, C528, C529, C530, C531, C532, C533, C534, C535, C536, C537, C538, C539, C540, C541, C542, C543, C544, C545, C546, C547, C548, C549, C550, C551, C552, C553, C554, C555, C556, C557, C558, C559, C560, C561, C562, C563, C564, C565, C566, C567, C568, C569, C570, C571, C572, C573, C574, C575, C576, C577, C578, C579, C580, C581, C582, C583, C584, C585, C586, C587, C588, C589, C590, C591, C592, C593, C594, C595, C596, C597, C598, C599, C600, C601, C602, C603, C604, C605, C606, C607, C608, C609, C610, C611, C612, C613, C614, C615, C616, C617, C618, C619, C620, C621, C622, C623, C624, C625, C626, C627, C628, C629, C630, C631, C632, C633, C634, C635, C636, C637, C638, C639, C640, C641, C642, C643, C644, C645, C646, C647, C648, C649, C650, C651, C652, C653, C654, C655, C656, C657, C658, C659, C660, C661, C662, C663, C664, C665, C666, C667, C668, C669, C670, C671, C672, C673, C674, C675, C676, C677, C678, C679, C680, C681, C682, C683, C684, C685, C686, C687, C688, C689, C690, C691, C692, C693, C694, C695, C696, C697, C698, C699, C700, C701, C702, C703, C704, C705, C706, C707, C708, C709, C710, C711, C712, C713, C714, C715, C716, C717, C718, C719, C720, C721, C722, C723, C724, C725, C726, C727, C728, C729, C730, C731, C732, C733, C734, C735, C736, C737, C738, C739, C740, C741, C742, C743, C744, C745, C746, C747, C748, C749, C750, C751, C752, C753, C754, C755, C756, C757, C758, C759, C760, C761, C762, C763, C764, C765, C766, C767, C768, C769, C770, C771, C772, C773, C774, C775, C776, C777, C778, C779, C780, C781, C782, C783, C784, C785, C786, C787, C788, C789, C790, C791, C792, C793, C794, C795, C796, C797, C798, C799, C800, C801, C802, C803, C804, C805, C806, C807, C808, C809, C810, C811, C812, C813, C814, C815, C816, C817, C818, C819, C820, C821, C822, C823, C824, C825, C826, C827, C828, C829, C830, C831, C832, C833, C834, C835, C836, C837, C838, C839, C840, C841, C842, C843, C844, C845, C846, C847, C848, C849, C850, C851, C852, C853, C854, C855, C856, C857, C858, C859, C860, C861, C862, C863, C864, C865, C866, C867, C868, C869, C870, C871, C872, C873, C874, C875,

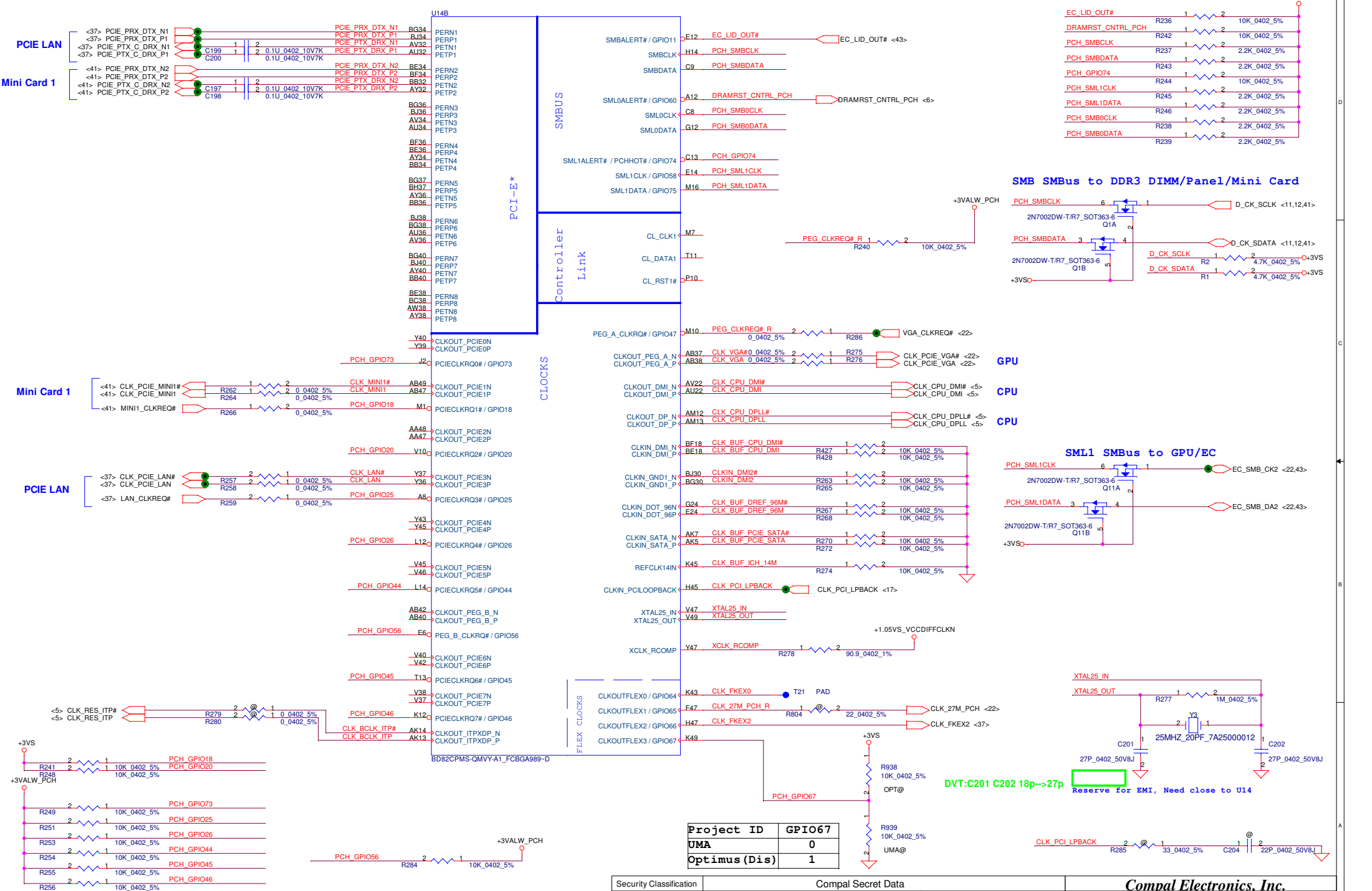


The schematic diagram illustrates the power plane for the CPU_VDDQ pin. It shows the connection from a +3VALW input through a network of resistors (R116, R117, R118, R119, R120, R121), capacitors (C137, C2596, C2597, C2598, C2599), and MOSFETs (Q7, Q8A, Q8B, Q9A) to the CPU_VDDQ pin. The diagram also includes a signal input for CPU1.5V_S3_GATE and a signal output for CPU1.5V_S3. The diagram is labeled "Q9A on P46".



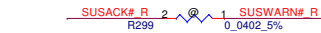
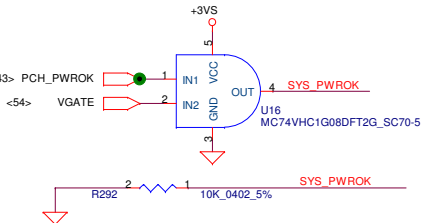
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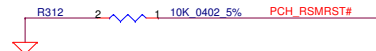
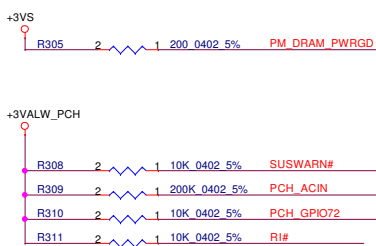


Project ID	GPI067
UMA	0
Optimus (Dis)	1

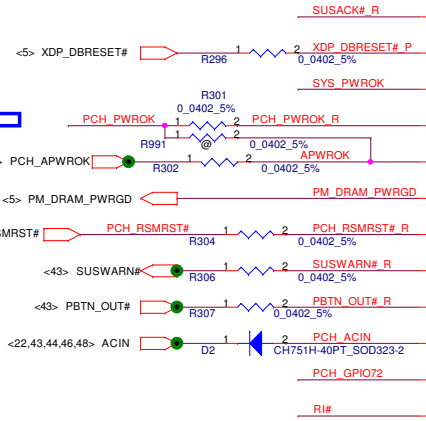
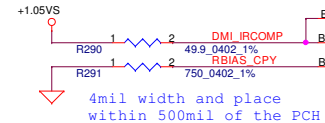
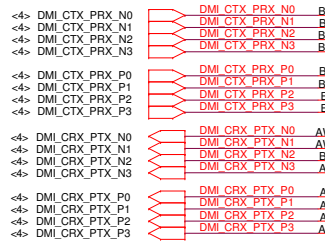
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Issued Date	2010/08/23	Deciphered Date	2011/08/25	PCH (2/8) PCIE, SMBUS, CLK	
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				Date: Monday, April 11, 2011	Sheet 14 of 56



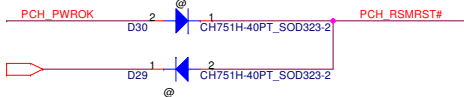
PVT:Reserved R991



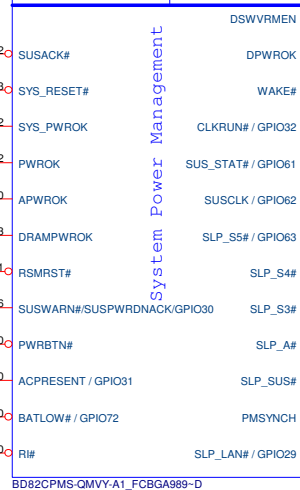
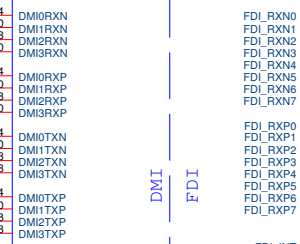
<49,55> SPOK



PVT:Reserved D29 D30

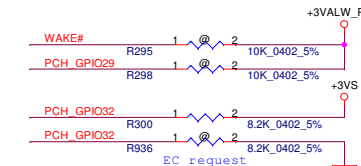
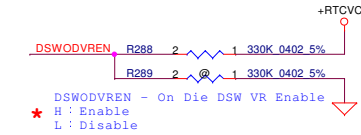
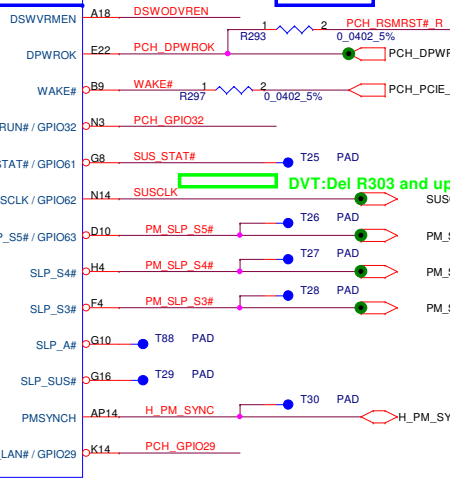
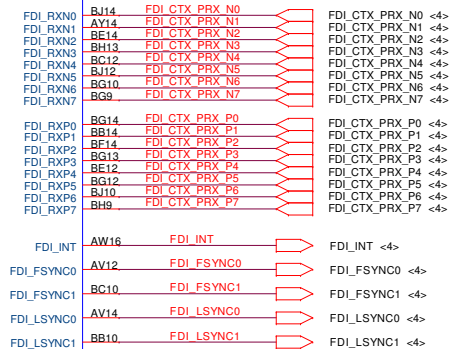


U14C

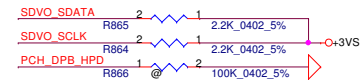
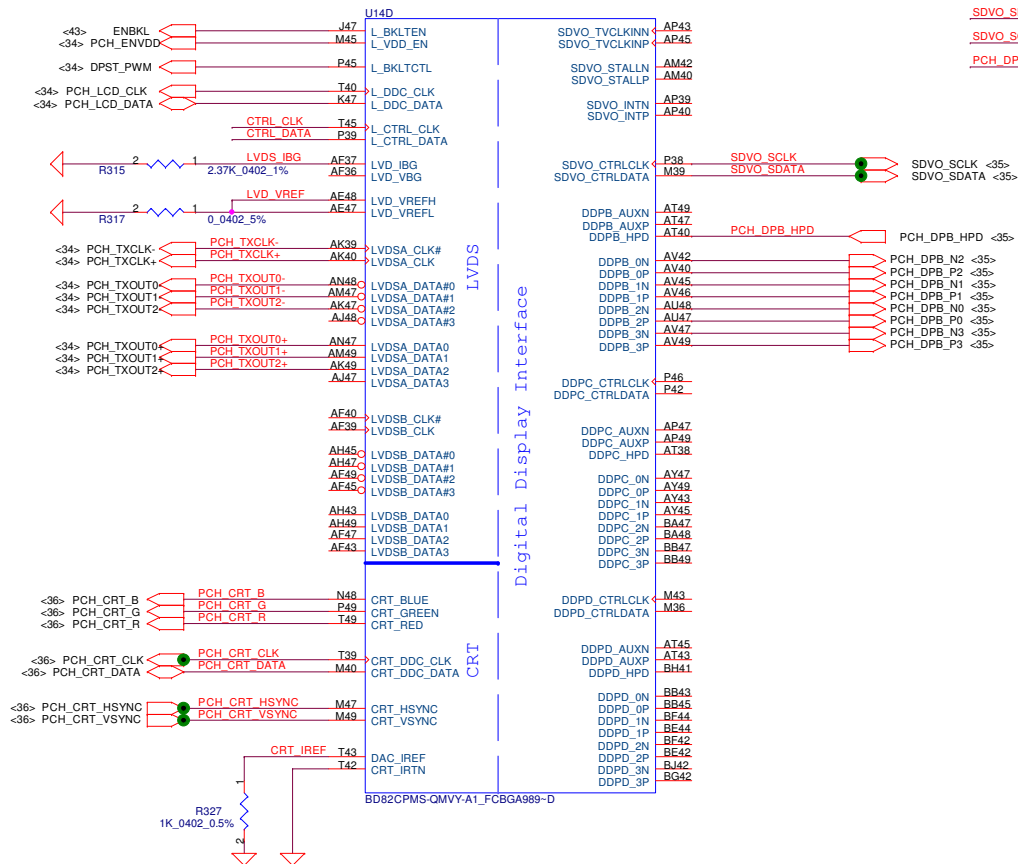
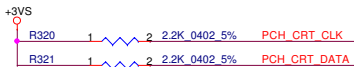
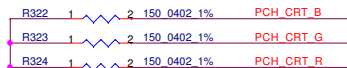
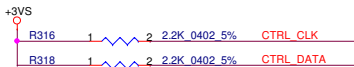
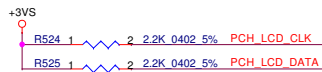
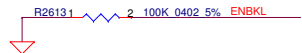


Default DSW Enable

- Note:
- 1.SLP_SUS and SUSACK# are NC if DSW is not supported
 - 2.DPWROK should connect to RSMRST# if DSW not supported
 - 3.The DSW rails must be stable for at least 10ms before DPWROK is asserted to PCH
 - ***4.PCH_DPWROK pull up to +V3S enables DSW wupport. No install R5261 to disable DSW

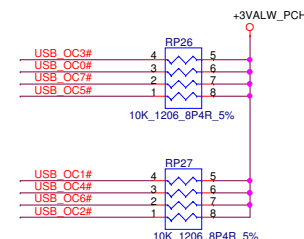
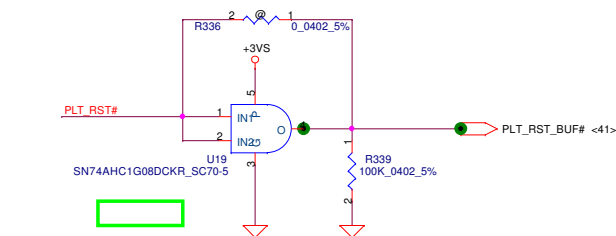
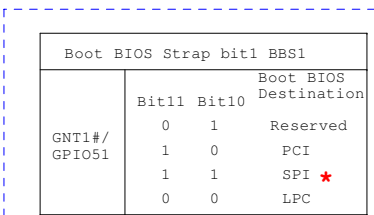


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					Size	Document Number	Rev
					Custom		1.0
					Date:	Monday, April 11, 2011	Sheet
						15 of 56	



HDMI D2
HDMI D1
HDMI D0
HDMI CLK

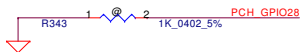
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Issued Date	2010/08/23	Deciphered Date	2011/08/25	Title	
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Size		Document Number		Rev	
Custom		Date: Monday, April 11, 2011		Sheet 16 of 56	
				1.0	



Security Classification		Compal Secret Data		Compal Electronics, Inc. PCH (5/9) PCI, USB, NVRAM	
Issued Date	2010/08/23	Deciphered Date	2011/08/25	Title	
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				Custom	Rev 1.0
Date:		Monday, April 11, 2011		Sheet	17 of 56

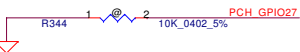
GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

* H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

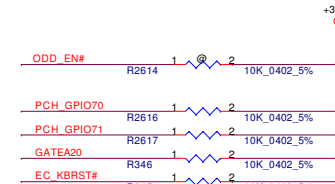
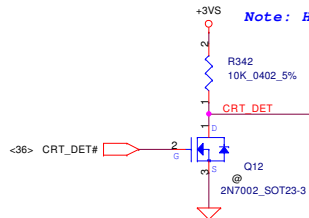
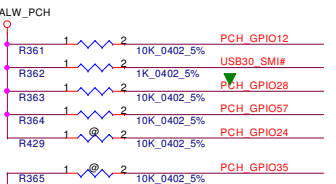
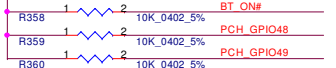
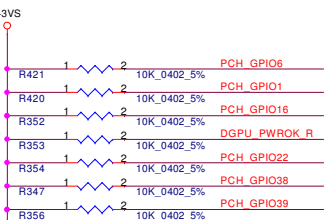
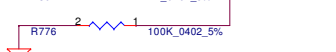


GPIO27
PCH_GPIO27 (Have internal Pull-High)

* High: VCCVRM VR Enable
Low: VCCVRM VR Disable



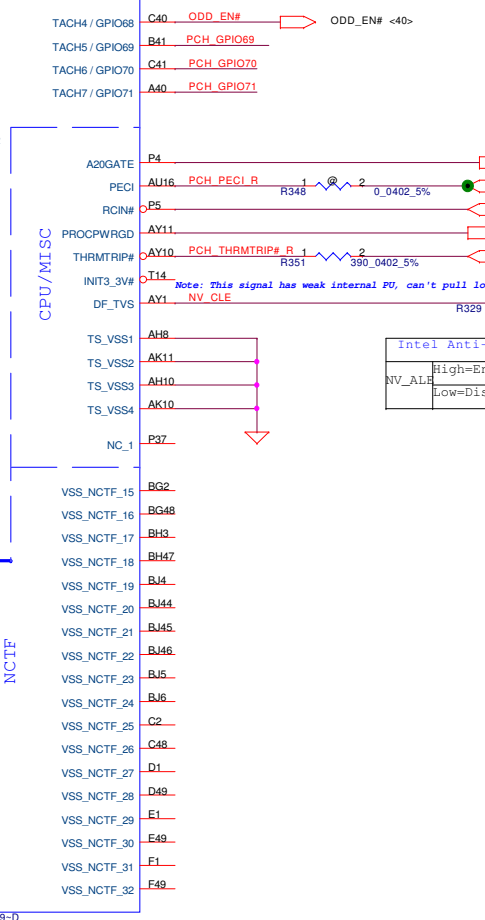
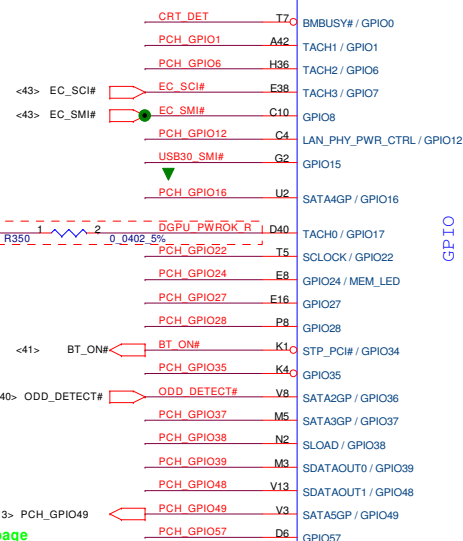
SATA2GP/GPIO36 & SATA3GP/GPIO37
Sampled at Rising edge of PWROK.
Weak internal pull-down. (weak internal pull-down is disabled after PLTRST# de-asserts)
NOTE: This signal should NOT be pulled high when strap is sampled



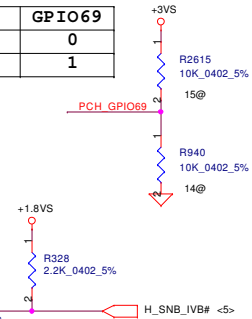
For Optimus



DVT:Add PCH_GPIO49 net off page



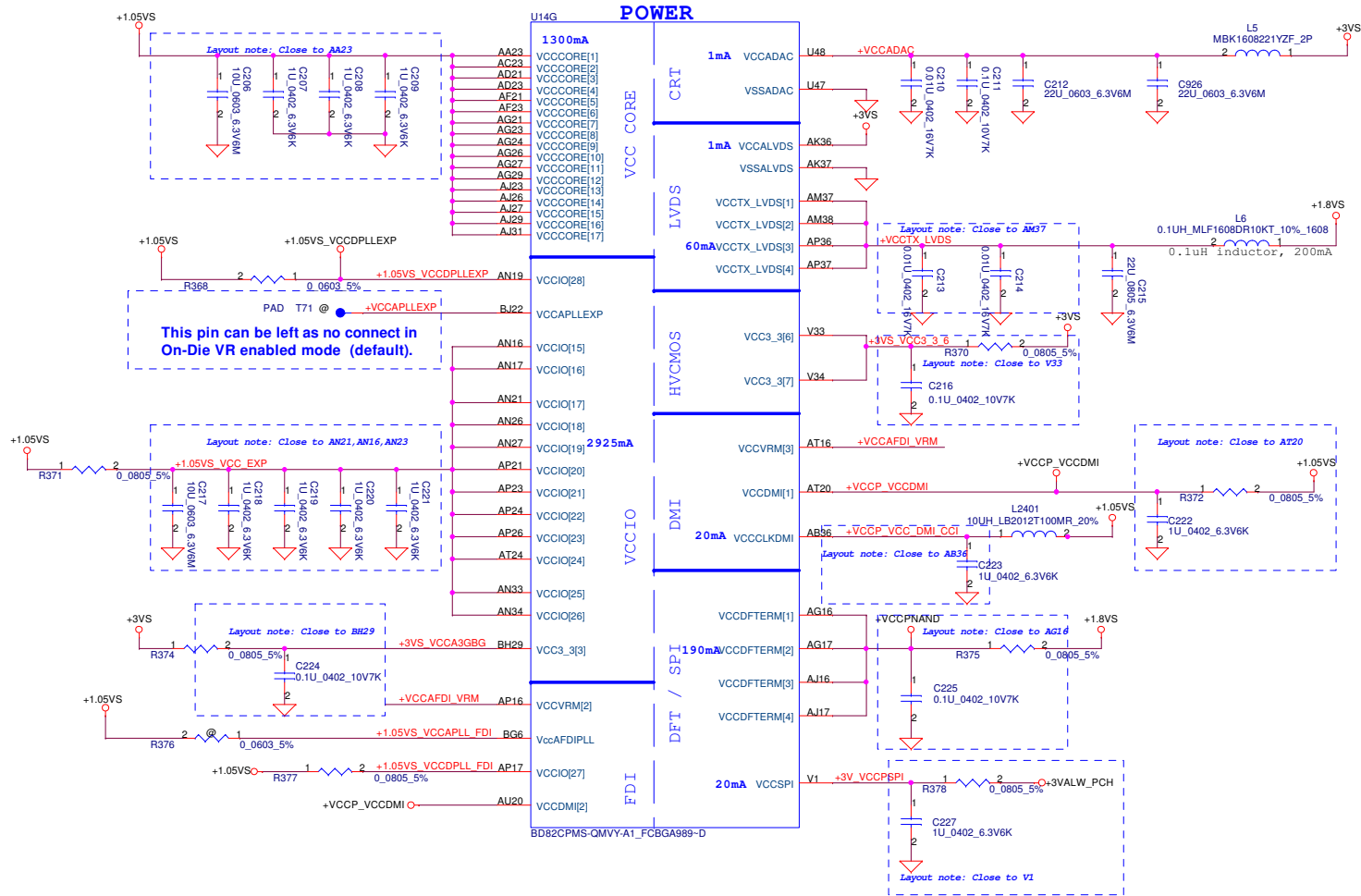
Project ID	GPIO69
14"	0
15.6"	1



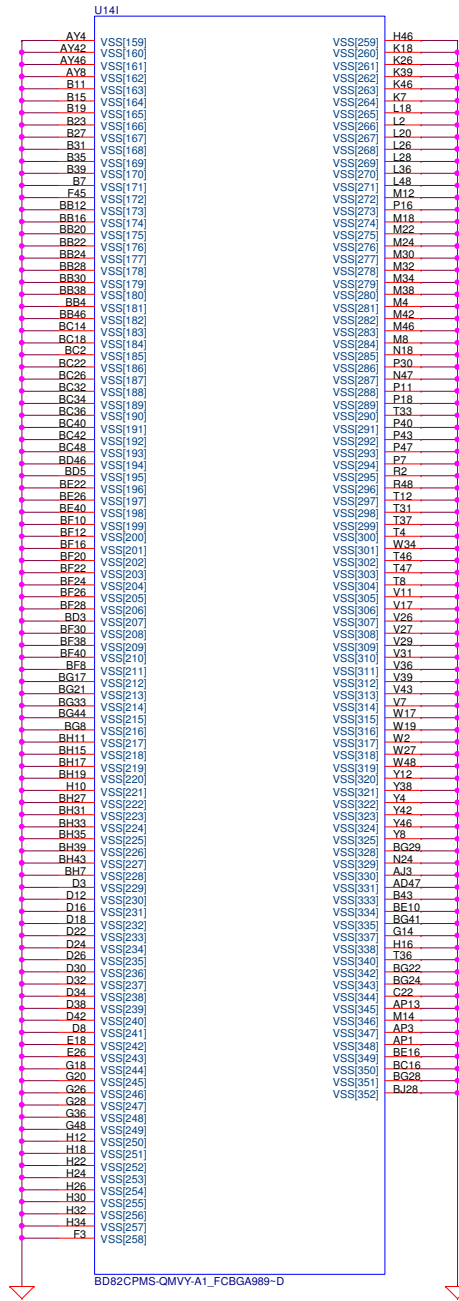
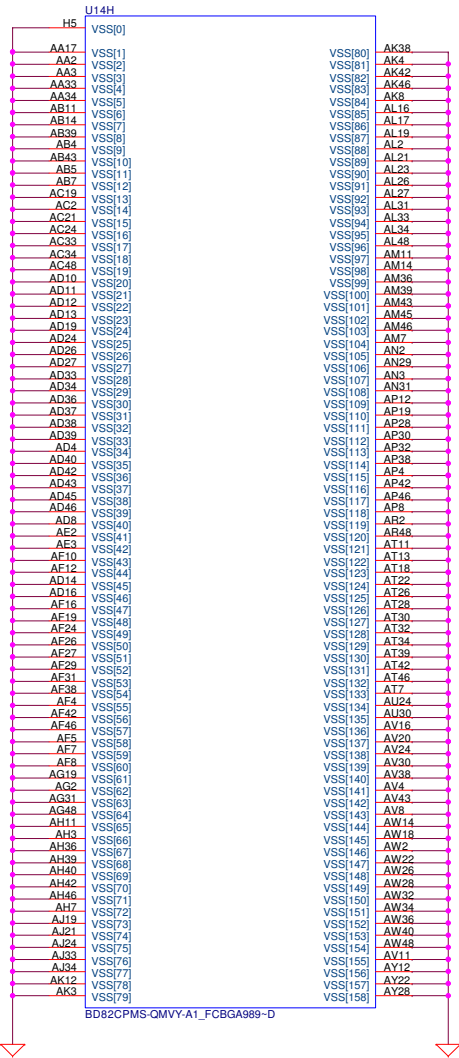
Intel Anti-Theft Technology	
NV_ALE	High=Enabled Low=Disable(floating) *

Layout note: CLOSE TO THE BRANCHING POINT

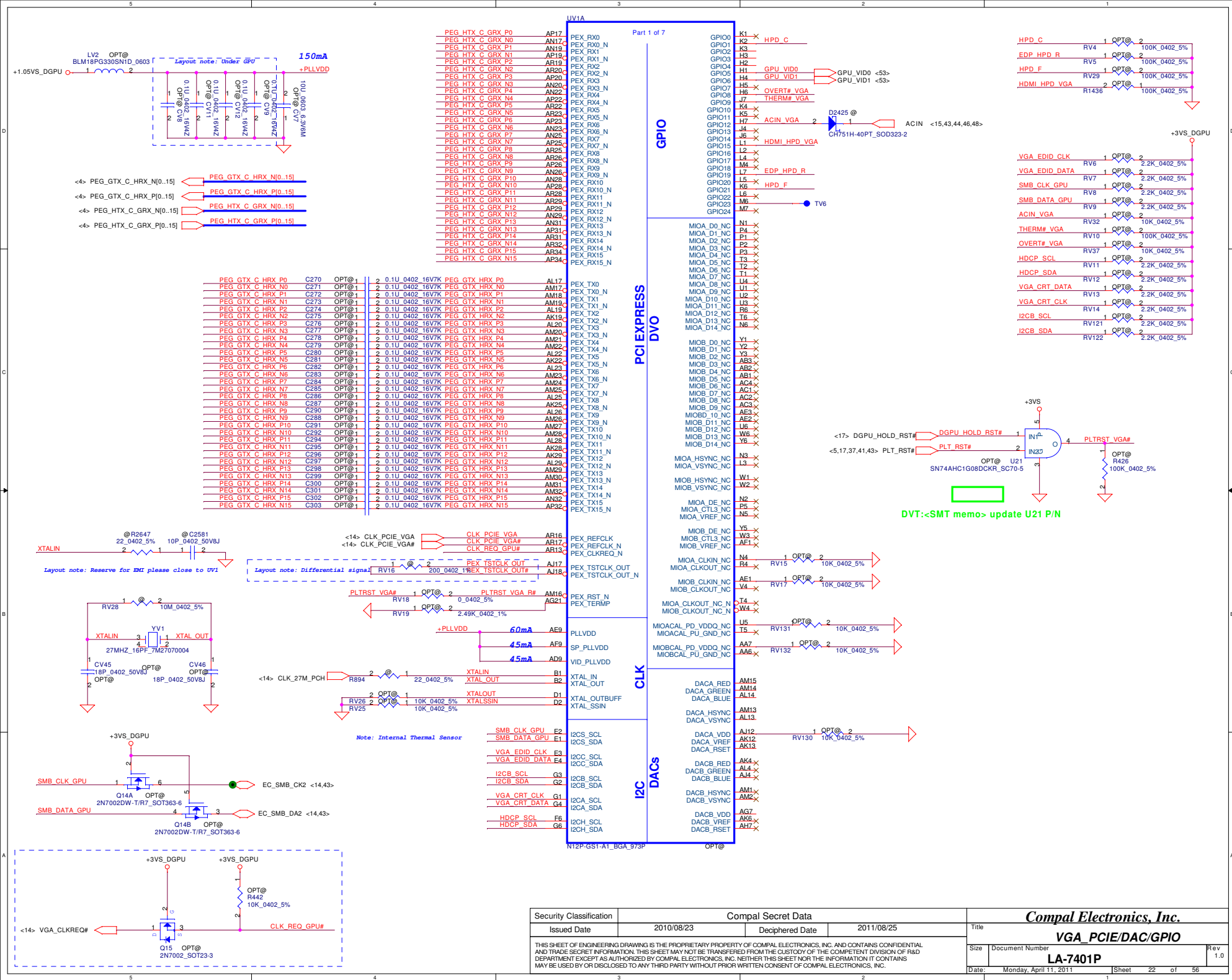
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Size		Document Number		Rev 1.0	
Date:		Monday, April 11, 2011		Sheet 18 of 56	



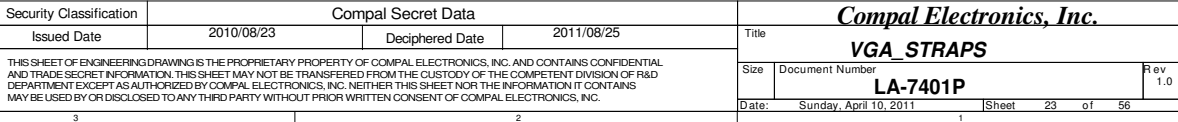
PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLb	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFLKLN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

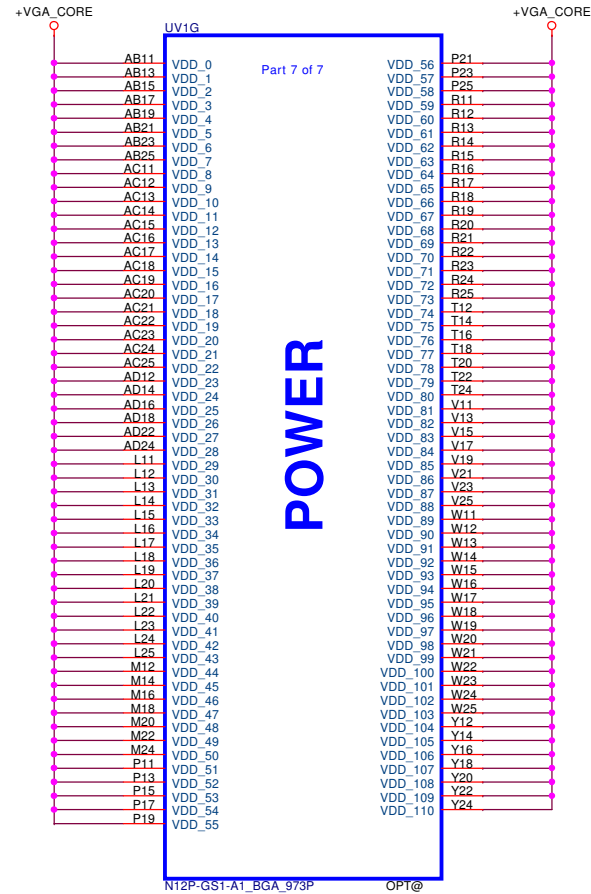


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Date: Sunday, April 10, 2011		Sheet 21 of 56			

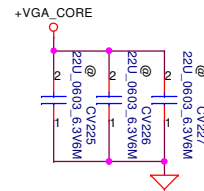
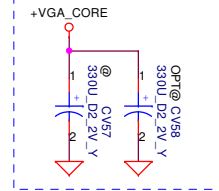


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				Size		Document Number		Rev	
						LA-7401P		1.0	
				Date:		Monday, April 11, 2011		Sheet 22 of 56	
3				2		1			

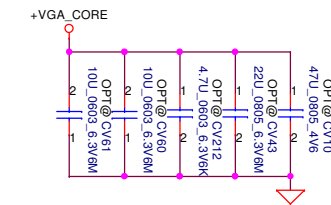




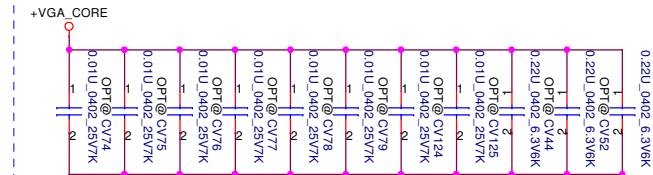
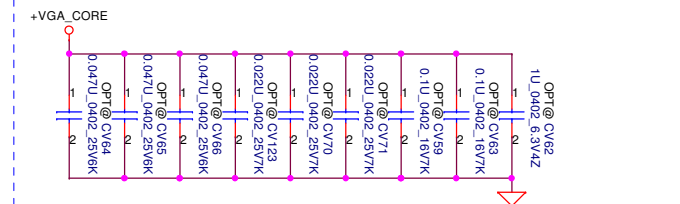
Layout note: Close to Power



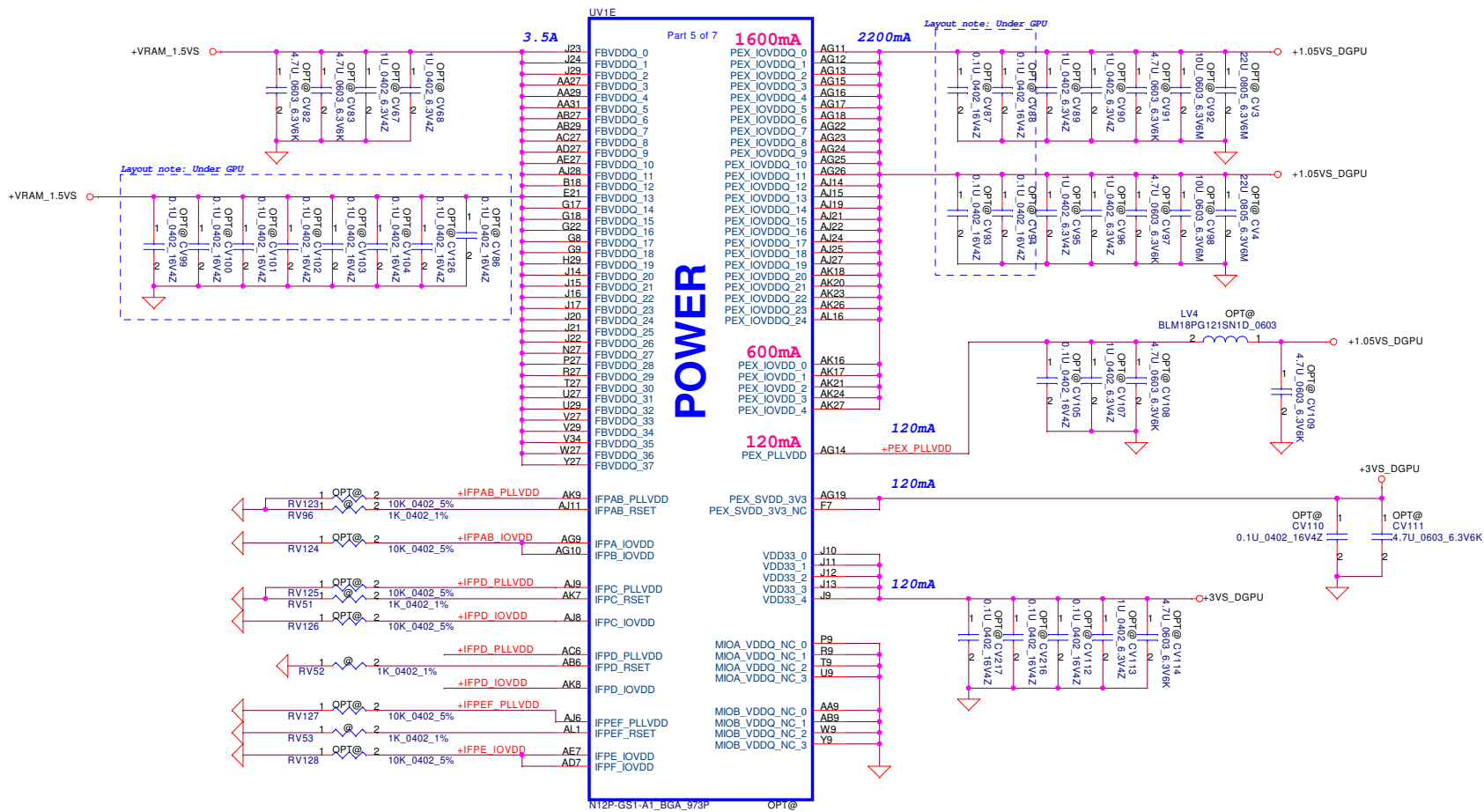
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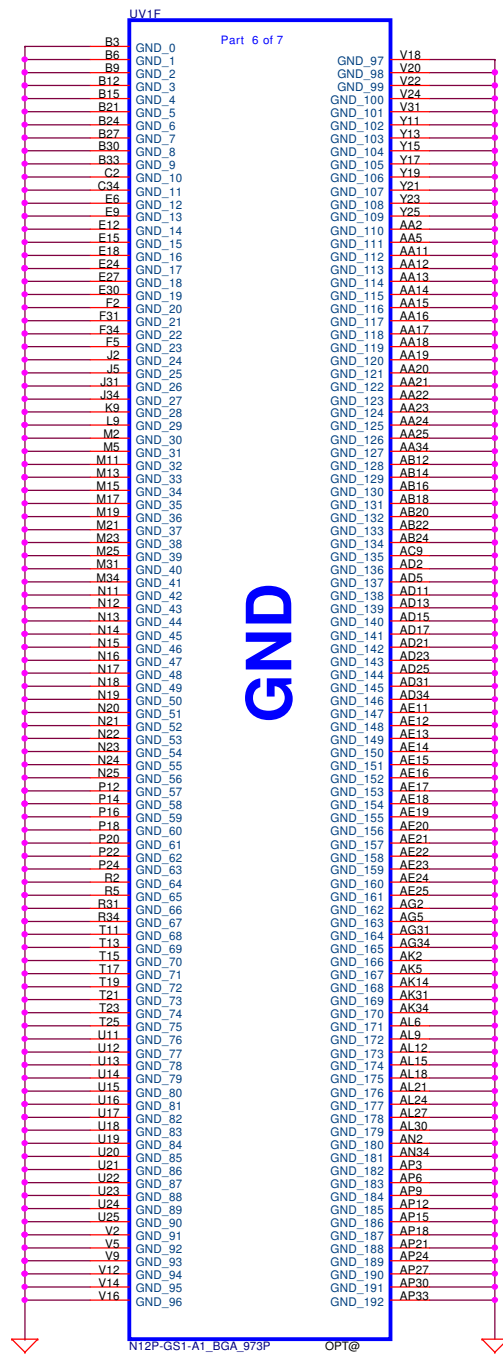


Layout note: Under GPU



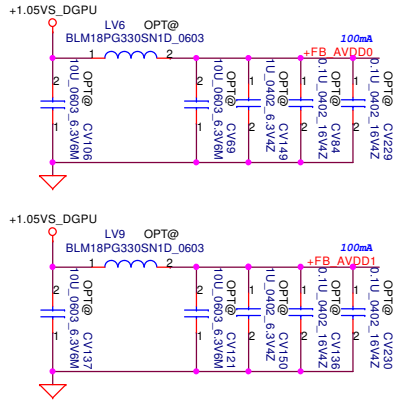
Security Classification		Compal Secret Data		Title	
Issued Date	2010/08/23	Deciphered Date	2011/08/25	VGA_VGA CORE	
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				Size	Document Number
				LA-7401P	
				Date:	Sunday, April 10, 2011
				Sheet	26 of 56
				Rev	1.0

<29,30> MDA[0..63] MDA[0..63]



+VRAM_1.5VS RV101 2 OPT@ 1 60.4 0402 1% RV57 2 OPT@ 1 10K 0402 5%

UV1B

Part 2 of 7

MEMORY INTERFACE

MDA0 L32 FBA_D0
MDA1 N33 FBA_D1
MDA2 L33 FBA_D2
MDA3 N34 FBA_D3
MDA4 N35 FBA_D4
MDA5 P35 FBA_D5
MDA6 P33 FBA_D6
MDA7 P34 FBA_D7
MDA8 K35 FBA_D8
MDA9 K33 FBA_D9
MDA10 K34 FBA_D10
MDA11 K33 FBA_D11
MDA12 G34 FBA_D12
MDA13 G33 FBA_D13
MDA14 E34 FBA_D14
MDA15 E33 FBA_D15
MDA16 G31 FBA_D16
MDA17 F30 FBA_D17
MDA18 G30 FBA_D18
MDA19 G32 FBA_D19
MDA20 K30 FBA_D20
MDA21 K32 FBA_D21
MDA22 N33 FBA_D22
MDA23 K31 FBA_D23
MDA24 L31 FBA_D24
MDA25 L30 FBA_D25
MDA26 M32 FBA_D26
MDA27 N30 FBA_D27
MDA28 M30 FBA_D28
MDA29 P31 FBA_D29
MDA30 R32 FBA_D30
MDA31 R30 FBA_D31
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MDA34 AH31 FBA_D34
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MDA47 AH30 FBA_D47
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MDA59 AE35 FBA_D59
MDA60 AE34 FBA_D60
MDA61 AE33 FBA_D61
MDA62 AB32 FBA_D62
MDA63 AC35 FBA_D63

+FB AVDD0 AG27 FB_DLLAVDD_0
AF27 FB_PLLAVDD_0
+FB AVDD1 J19 FB_DLLAVDD_1
J18 FB_PLLAVDD_1

J27 FB_VREF NC
T30 FBA_DEBBUG0
T29 FBA_DEBBUG1

N12P-GS1-A1_BGA_973P

FBA_CMD0 U30 CMDA0
FBA_CMD1 U31 CMDA2
FBA_CMD2 V32 CMDA3
FBA_CMD3 T35 CMDA4
FBA_CMD4 U33 CMDA5
FBA_CMD5 W32 CMDA6
FBA_CMD6 W33 CMDA7
FBA_CMD7 W31 CMDA8
FBA_CMD8 W34 CMDA9
FBA_CMD9 U34 CMDA10
FBA_CMD10 U35 CMDA11
FBA_CMD11 U32 CMDA12
FBA_CMD12 T34 CMDA13
FBA_CMD13 T33 CMDA14
FBA_CMD14 W30 CMDA15
FBA_CMD15 AB30 CMDA16
FBA_CMD16 AB30 CMDA18
FBA_CMD17 AB31 CMDA19
FBA_CMD18 AB32 CMDA20
FBA_CMD19 AB33 CMDA21
FBA_CMD20 Y32 CMDA22
FBA_CMD21 Y33 CMDA23
FBA_CMD22 AB34 CMDA24
FBA_CMD23 AB35 CMDA25
FBA_CMD24 Y35 CMDA26
FBA_CMD25 W35 CMDA27
FBA_CMD26 Y34 CMDA28
FBA_CMD27 Y31 CMDA29
FBA_CMD28 Y30 CMDA30
FBA_CMD29 W29 CMDA30
FBA_CMD30 Y29

FBA_CMD0 P32 DQMA0
FBA_CMD1 L34 DQMA1
FBA_CMD2 P30 DQMA2
FBA_CMD3 P30 DQMA3
FBA_CMD4 AE32 DQMA4
FBA_CMD5 AL32 DQMA5
FBA_CMD6 AL34 DQMA6
FBA_CMD7 AF35 DQMA7

FBA_DQS_RN0 L35 DQSA#0
FBA_DQS_RN1 G35 DQSA#1
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FBA_DQS_RN7 AC34 DQSA#7

FBA_DQS_WP0 L34 DQSA0
FBA_DQS_WP1 H35 DQSA1
FBA_DQS_WP2 J32 DQSA2
FBA_DQS_WP3 N31 DQSA3
FBA_DQS_WP4 AE31 DQSA4
FBA_DQS_WP5 AJ32 DQSA5
FBA_DQS_WP6 AJ34 DQSA6
FBA_DQS_WP7 AC33 DQSA7

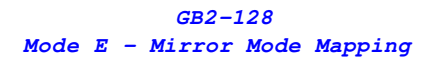
FBA_WCK0 P29
FBA_WCK0_N R29
FBA_WCK1 L29
FBA_WCK1_N M29
FBA_WCK2 AG29
FBA_WCK2_N AH29
FBA_WCK3 AD29
FBA_WCK3_N AE29

FBA_CLK0 T32 CLKA0
FBA_CLK0_N T31 CLKA0#
FBA_CLK1 AC31 CLKA1
FBA_CLK1_N AC30 CLKA1#

DQMA[7..0] <29,30>
DQSA[7..0] <29,30>
DQSA[7..0] <29,30>

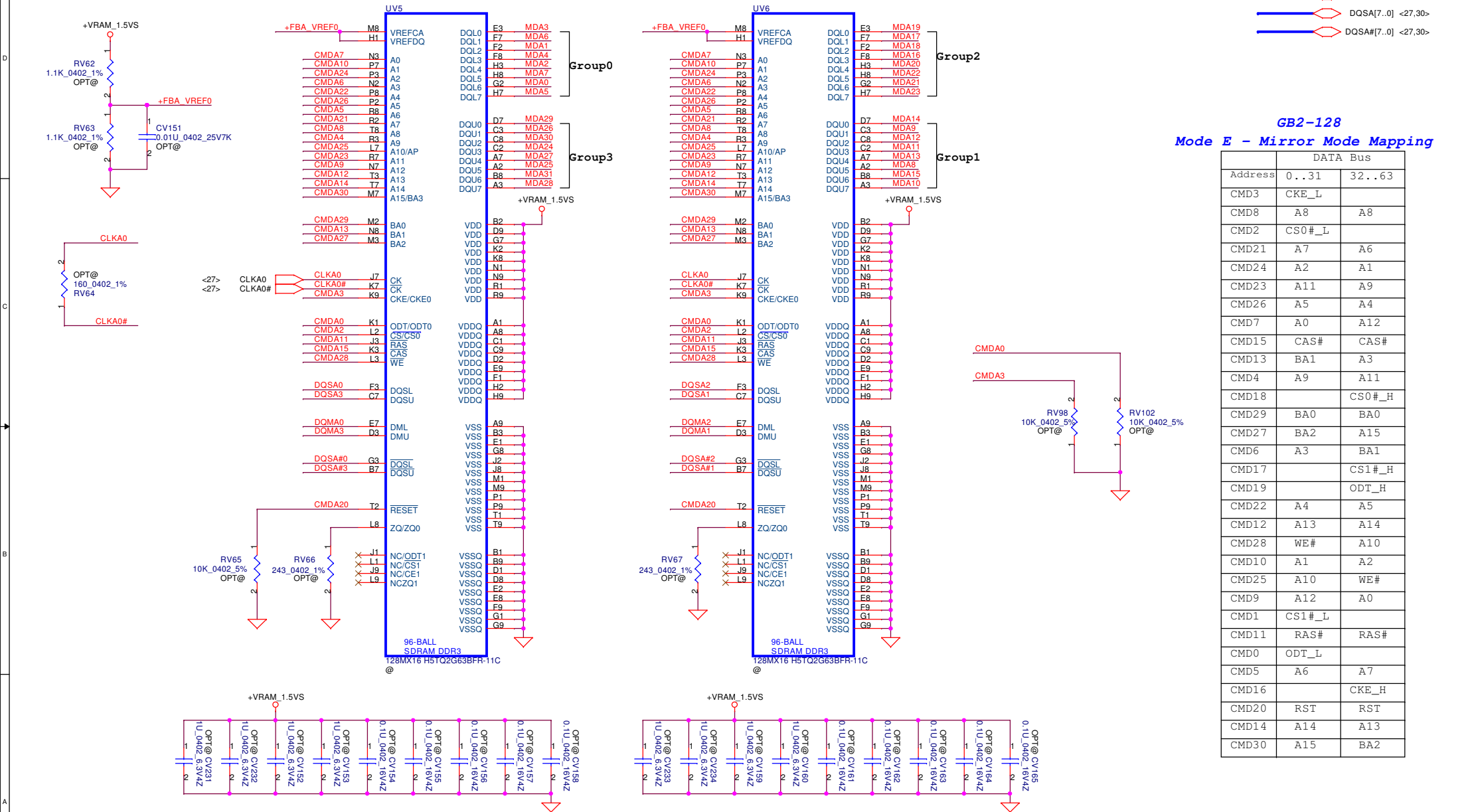
GB2-128 Mode E - Mirror Mode Mapping

DATA Bus		
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

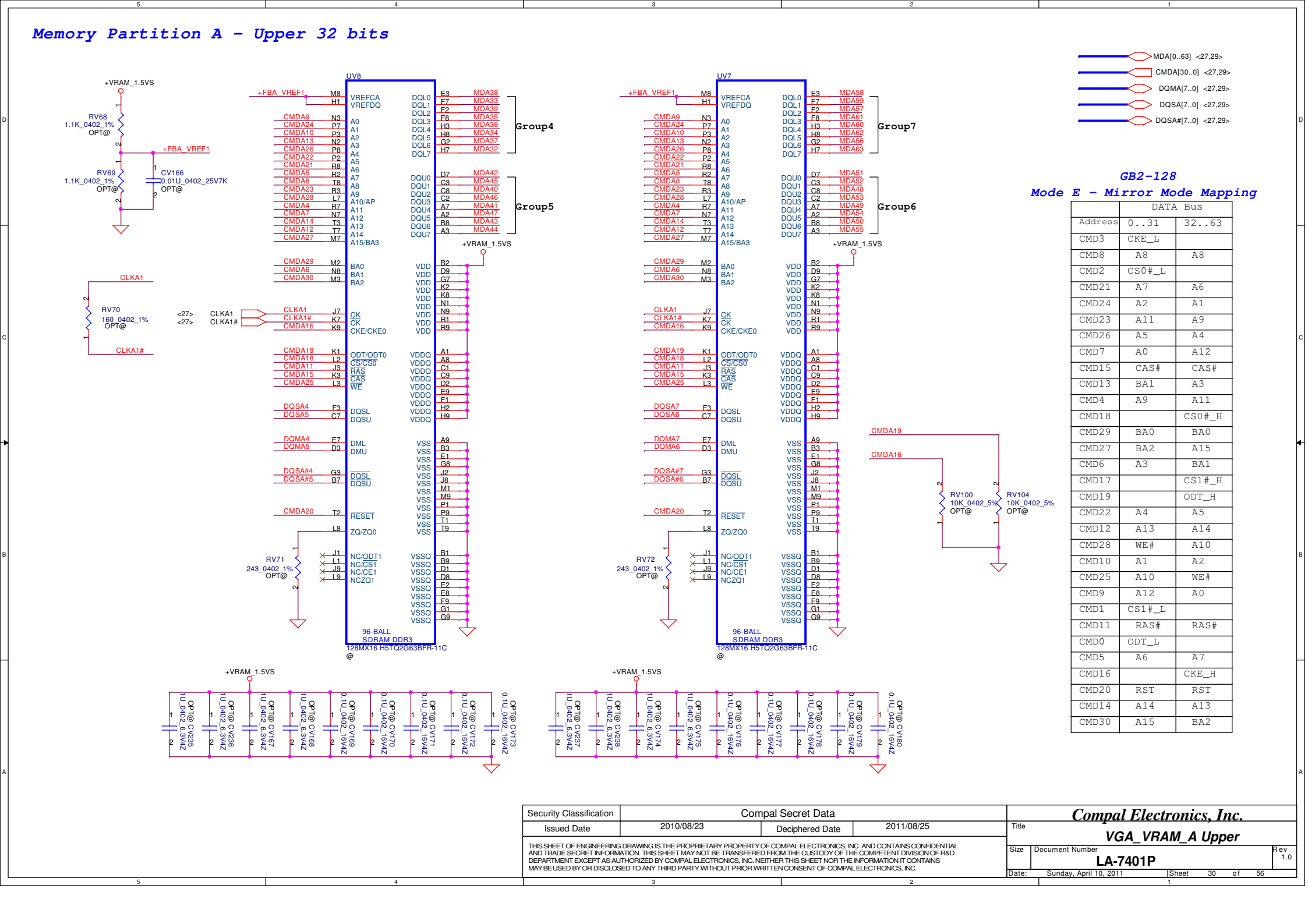
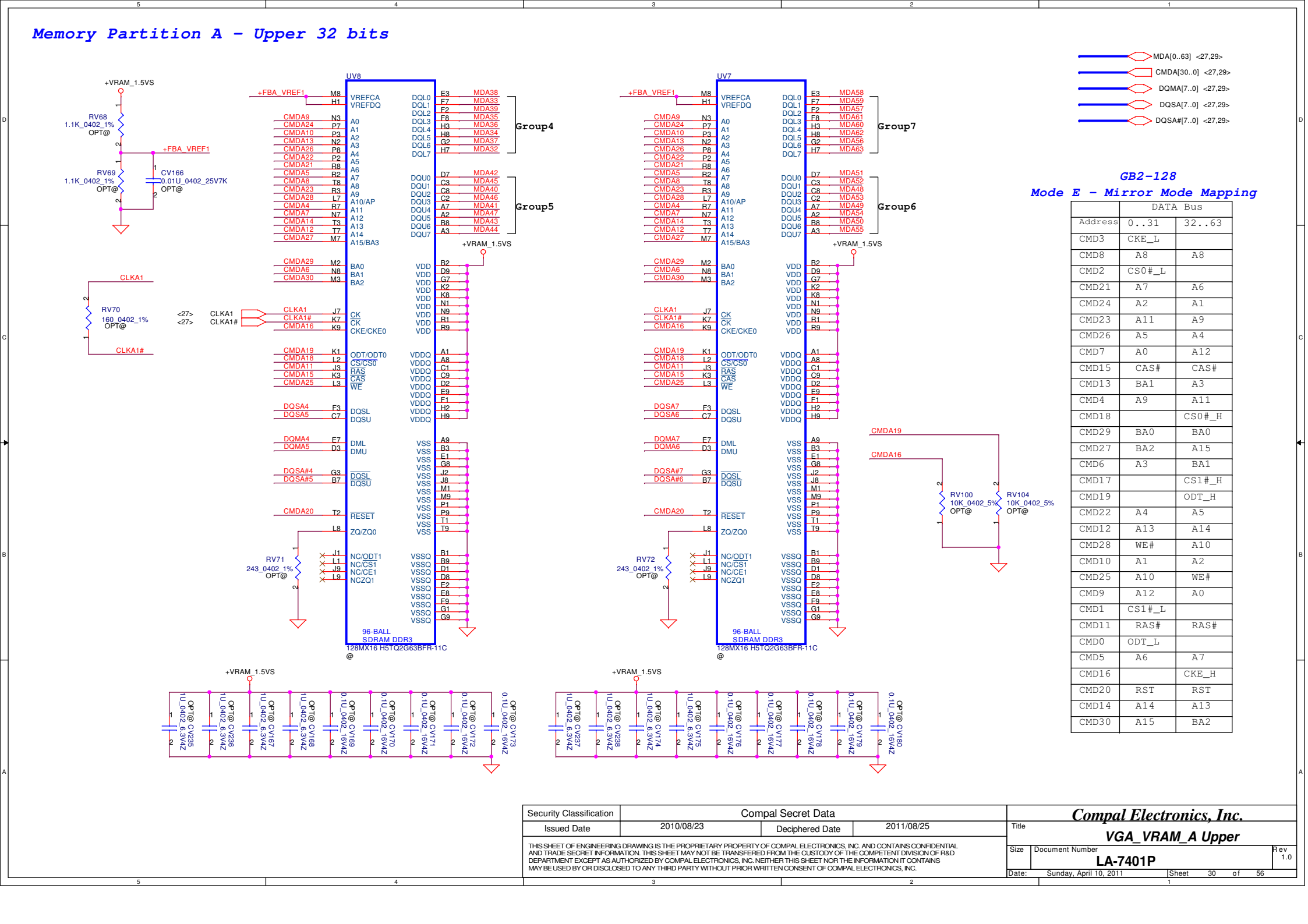


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Memory Partition A - Lower 32 bits



Memory Partition A - Upper 32 bits



Memory Partition A - Upper 32 bits

Legend:

- MDA[0..63] <27,29>
- CMDA[30..0] <27,29>
- DQMA[7..0] <27,29>
- DQSA[7..0] <27,29>
- DQSA#[7..0] <27,29>

Mode E - Mirror Mode Mapping

Address	DATA Bus
CMD3	CKE_L
CMD8	A8
CMD2	CS0#_L
CMD21	A7
CMD24	A2
CMD23	A11
CMD26	A5
CMD7	A0
CMD15	CAS#
CMD13	BA1
CMD4	A9
CMD18	CS0#_H
CMD29	BA0
CMD27	BA2
CMD6	A3
CMD17	CS1#_H
CMD19	ODT_H
CMD22	A4
CMD12	A13
CMD28	WE#
CMD10	A1
CMD25	A10
CMD9	A12
CMD1	CS1#_L
CMD11	RAS#
CMD0	ODT_L
CMD5	A6
CMD16	CKE_H
CMD20	RST
CMD14	A14
CMD30	A15

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Title

Compal Electronics, Inc.
VGA_VRAM_A Upper

Size | **Document Number** | **Rev**

LA-7401P | 1.0

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Memory Partition A - Upper 32 bits

The diagram illustrates the upper 32 bits of Memory Partition A, showing two mirrored memory modules (UV8 and UV7) connected to a central bus. The modules are populated with 96-BALL SDRAM DDR3 (128MX16 H5TQ2G63BFR-11C). The schematic includes power supply connections (+VRAM_1.5VS, +FBA_VREF1), clock signals (CLKA1), and data bus connections (MDA, CMDA, DQSA, DQSA#). A legend on the right defines the bus signals. A table on the right shows the Mode E - Mirror Mode Mapping for the data bus. The bottom of the diagram shows a security classification table and a title block.

Legend:

- MDA[0..63] <27,29>
- CMDA[30..0] <27,29>
- DQMA[7..0] <27,29>
- DQSA[7..0] <27,29>
- DQSA#[7..0] <27,29>

Mode E - Mirror Mode Mapping

Address	DATA Bus
CMD3	CKE_L
CMD8	A8
CMD2	CS0#_L
CMD21	A7
CMD24	A2
CMD23	A11
CMD26	A5
CMD7	A0
CMD15	CAS#
CMD13	BA1
CMD4	A9
CMD18	CS0#_H
CMD29	BA0
CMD27	BA2
CMD6	A3
CMD17	CS1#_H
CMD19	ODT_H
CMD22	A4
CMD12	A13
CMD28	WE#
CMD10	A1
CMD25	A10
CMD9	A12
CMD1	CS1#_L
CMD11	RAS#
CMD0	ODT_L
CMD5	A6
CMD16	CKE_H
CMD20	RST
CMD14	A14
CMD30	A15

Security Classification

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Title

Compal Electronics, Inc.
VGA_VRAM_A Upper
LA-7401P
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Date: Sunday, April 10, 2011 Sheet 30 of 56

Memory Partition A - Upper 32 bits

The diagram illustrates the upper 32 bits of Memory Partition A, showing two mirrored memory modules (UV8 and UV7) connected to a central bus. The modules are populated with 96-BALL SDRAM DDR3 (128MX16 H5TQ2G63BFR-11C). The schematic includes power supply connections (+VRAM_1.5VS, +FBA_VREF1), clock signals (CLKA1), and data bus connections (MDA, CMDA, DQSA, DQSA#). A legend on the right defines the bus signals. A table on the right shows the Mode E - Mirror Mode Mapping for the data bus. The bottom of the diagram shows a security classification table and a title block.

Legend:

- MDA[0..63] <27,29>
- CMDA[30..0] <27,29>
- DQMA[7..0] <27,29>
- DQSA[7..0] <27,29>
- DQSA#[7..0] <27,29>

Mode E - Mirror Mode Mapping

Address	DATA Bus
CMD3	CKE_L
CMD8	A8
CMD2	CS0#_L
CMD21	A7
CMD24	A2
CMD23	A11
CMD26	A5
CMD7	A0
CMD15	CAS#
CMD13	BA1
CMD4	A9
CMD18	CS0#_H
CMD29	BA0
CMD27	BA2
CMD6	A3
CMD17	CS1#_H
CMD19	ODT_H
CMD22	A4
CMD12	A13
CMD28	WE#
CMD10	A1
CMD25	A10
CMD9	A12
CMD1	CS1#_L
CMD11	RAS#
CMD0	ODT_L
CMD5	A6
CMD16	CKE_H
CMD20	RST
CMD14	A14
CMD30	A15

Security Classification

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Title

Compal Electronics, Inc.
VGA_VRAM_A Upper

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Memory Partition C - Lower 32 bits



EVT:Del B ch VRAM

GB2-128
Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Memory Partition C - Upper 32 bits



EVT:Del B ch VRAM

GB2-128
Mode E - Mirror Mode Mapping

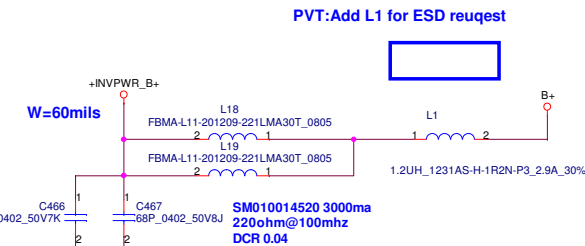
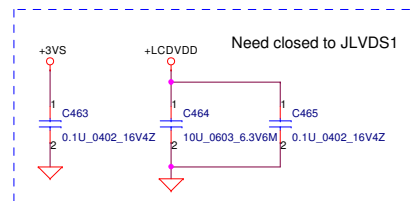
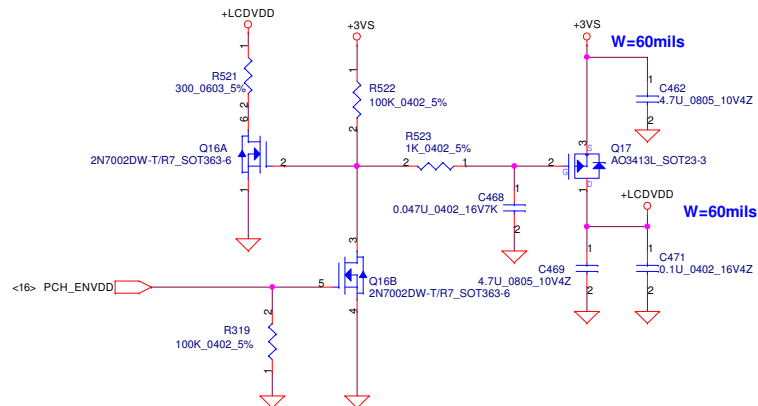
	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2



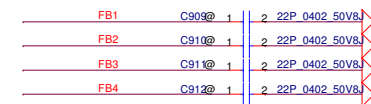
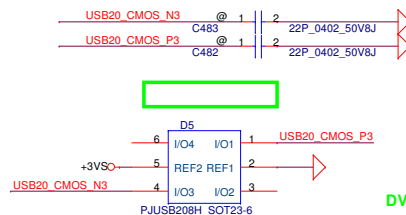
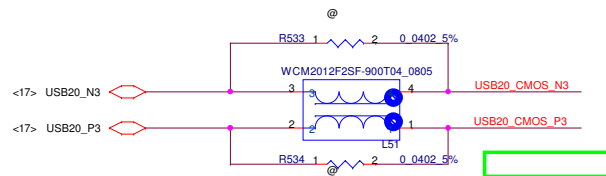
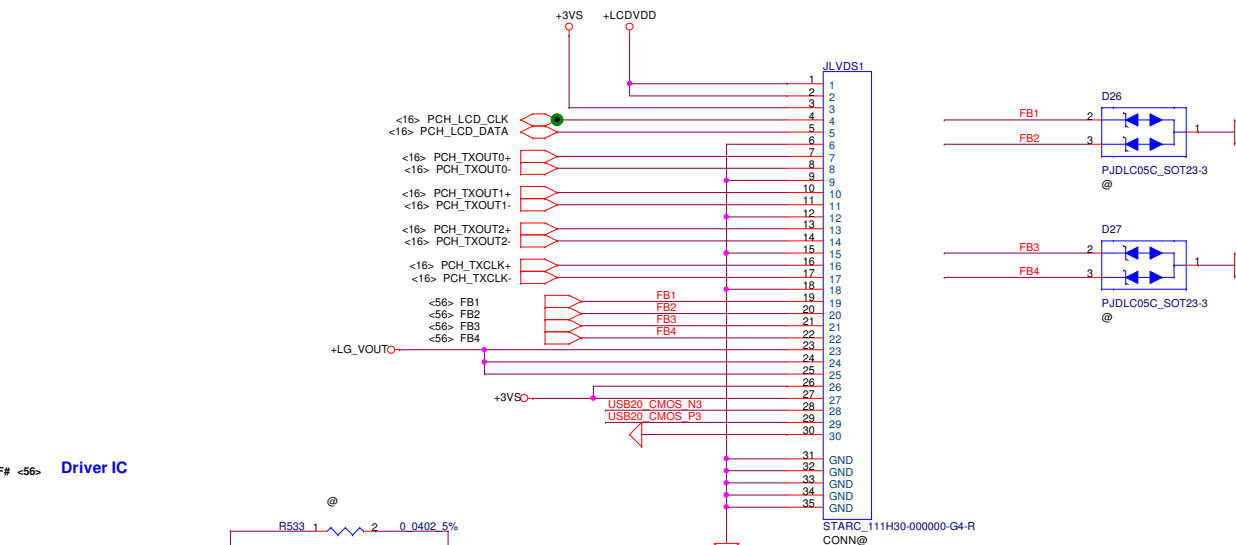
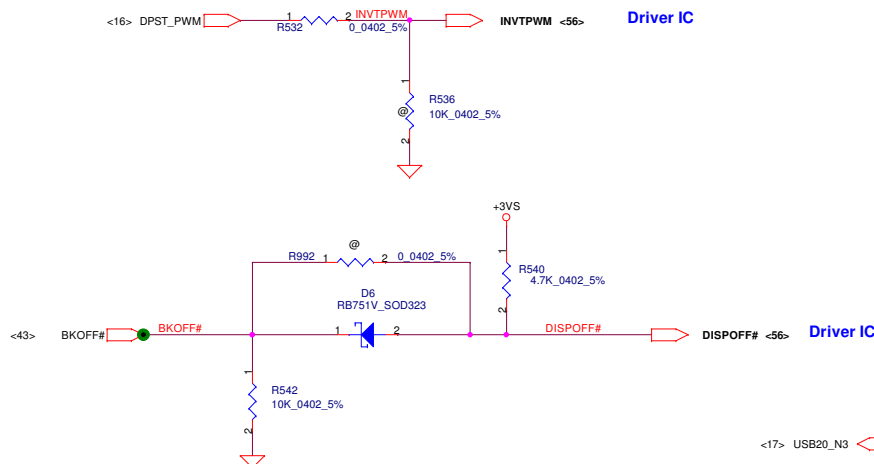
ROM_SI net for VRAM strap

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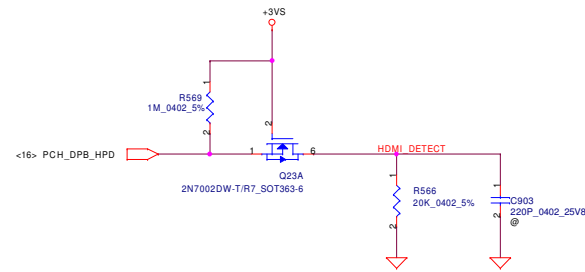
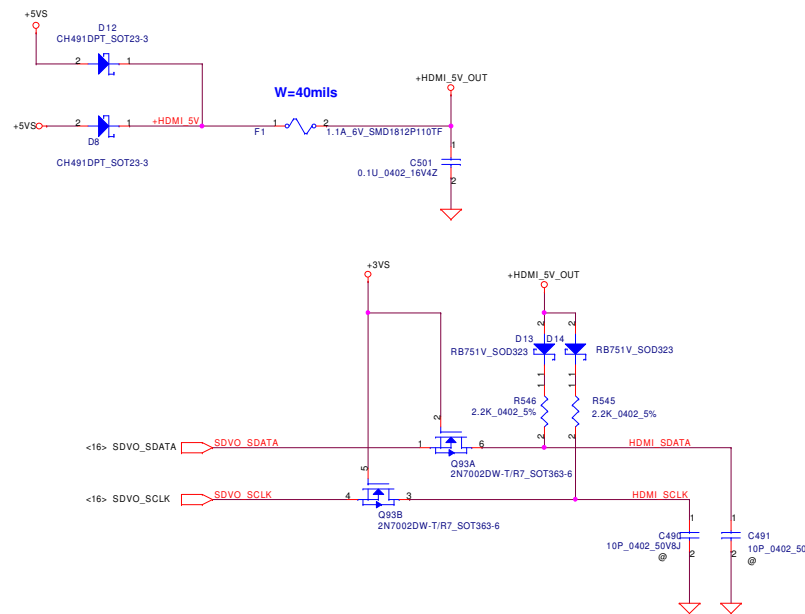
LCD POWER CIRCUIT



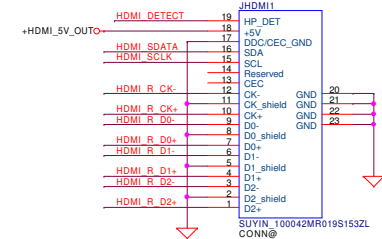
LCD/LED PANEL Connector



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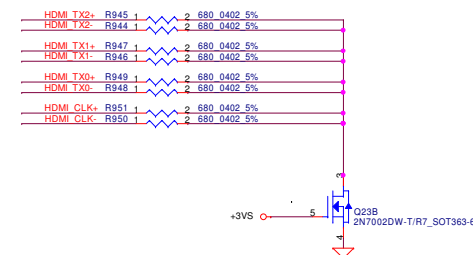
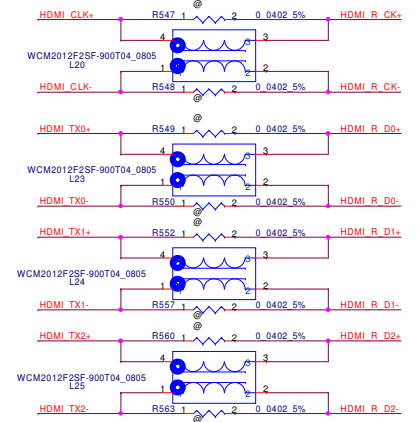


HDMI Connector



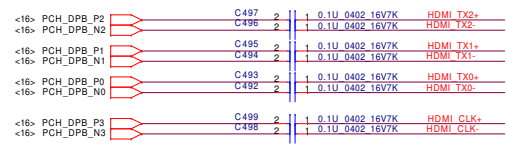
DVT::<EMI>L20 L23 L24 L25 @-->SMT

SM070001310 400mhz@100mhz DCR 0.3



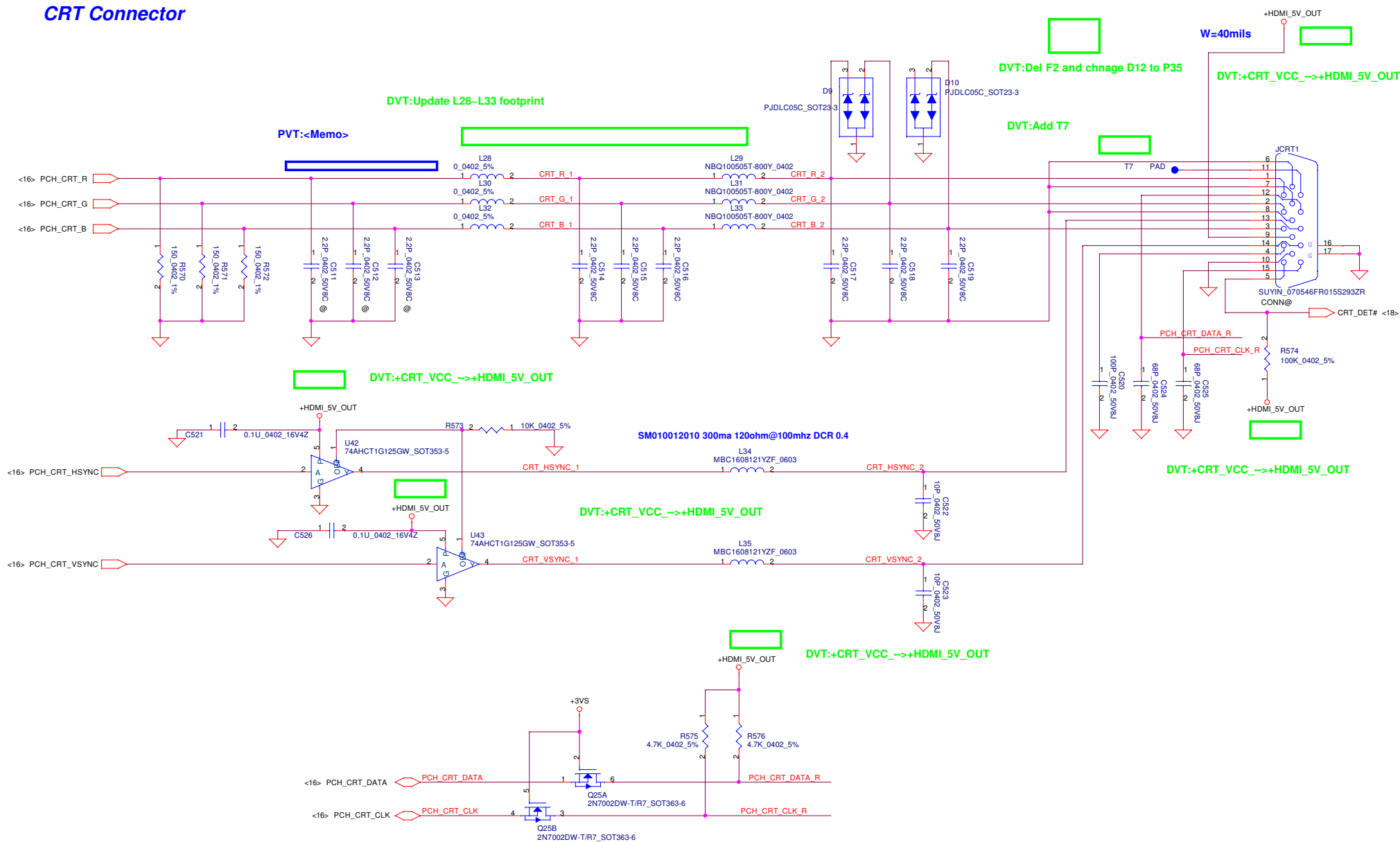
Note: Reresve for RF

Lane Reversed on Page 16

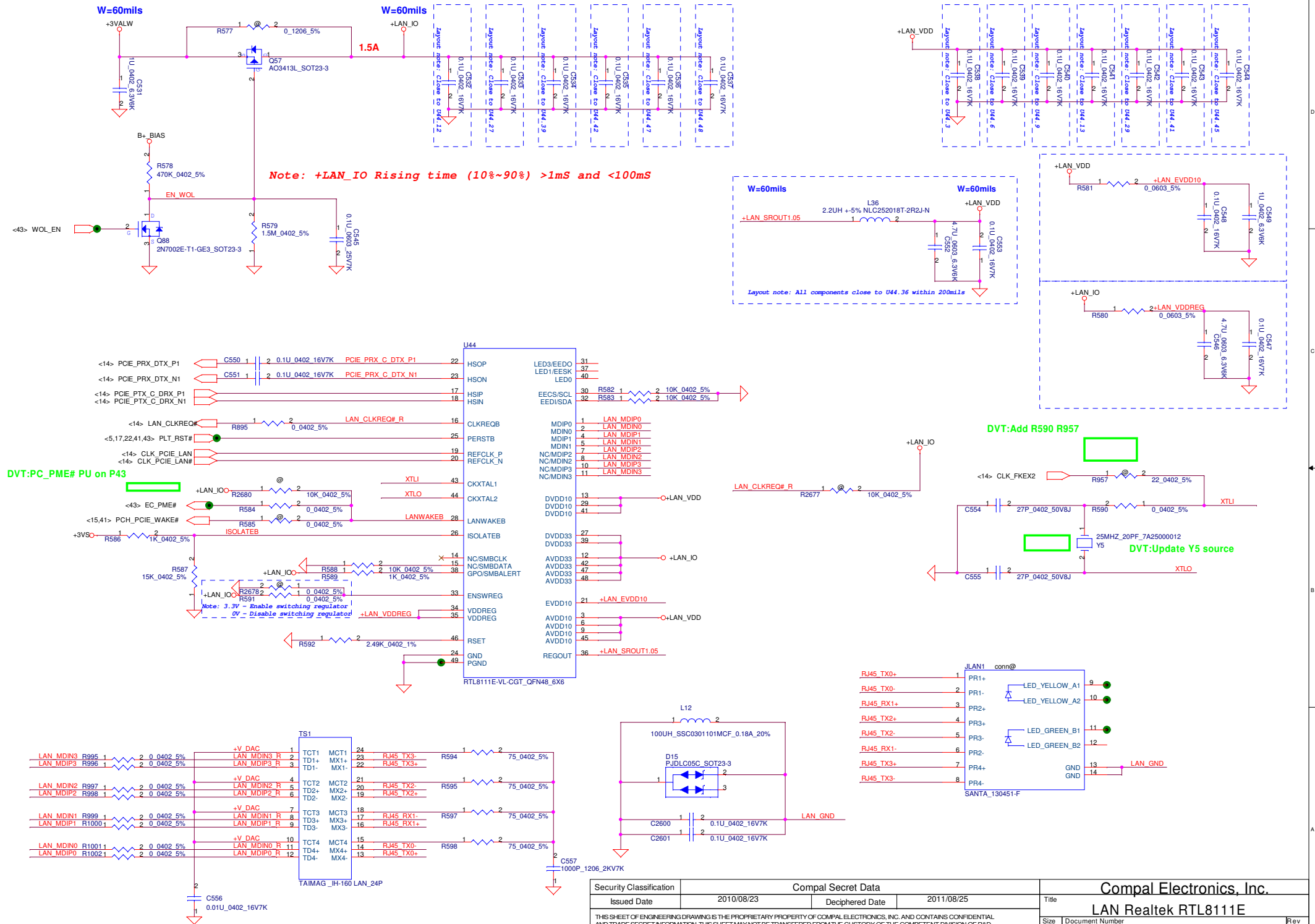


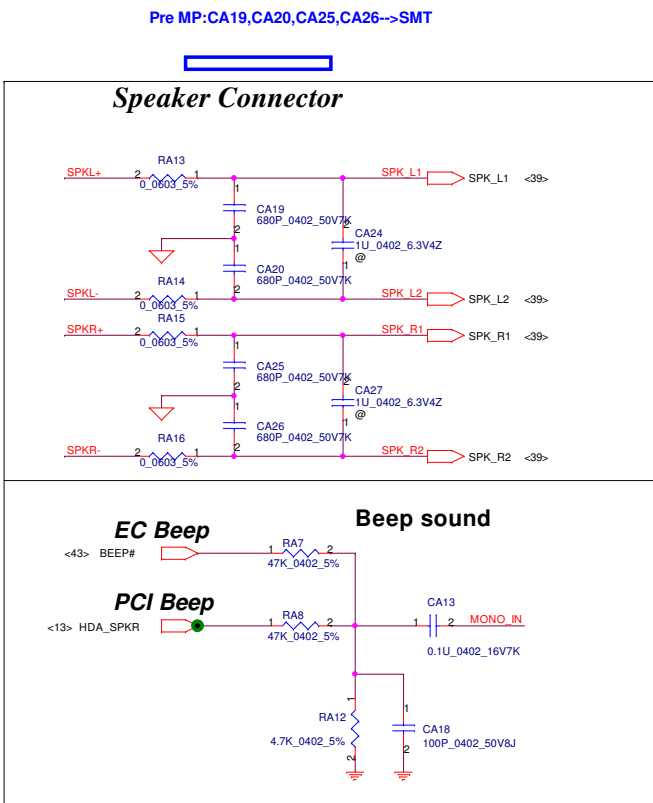
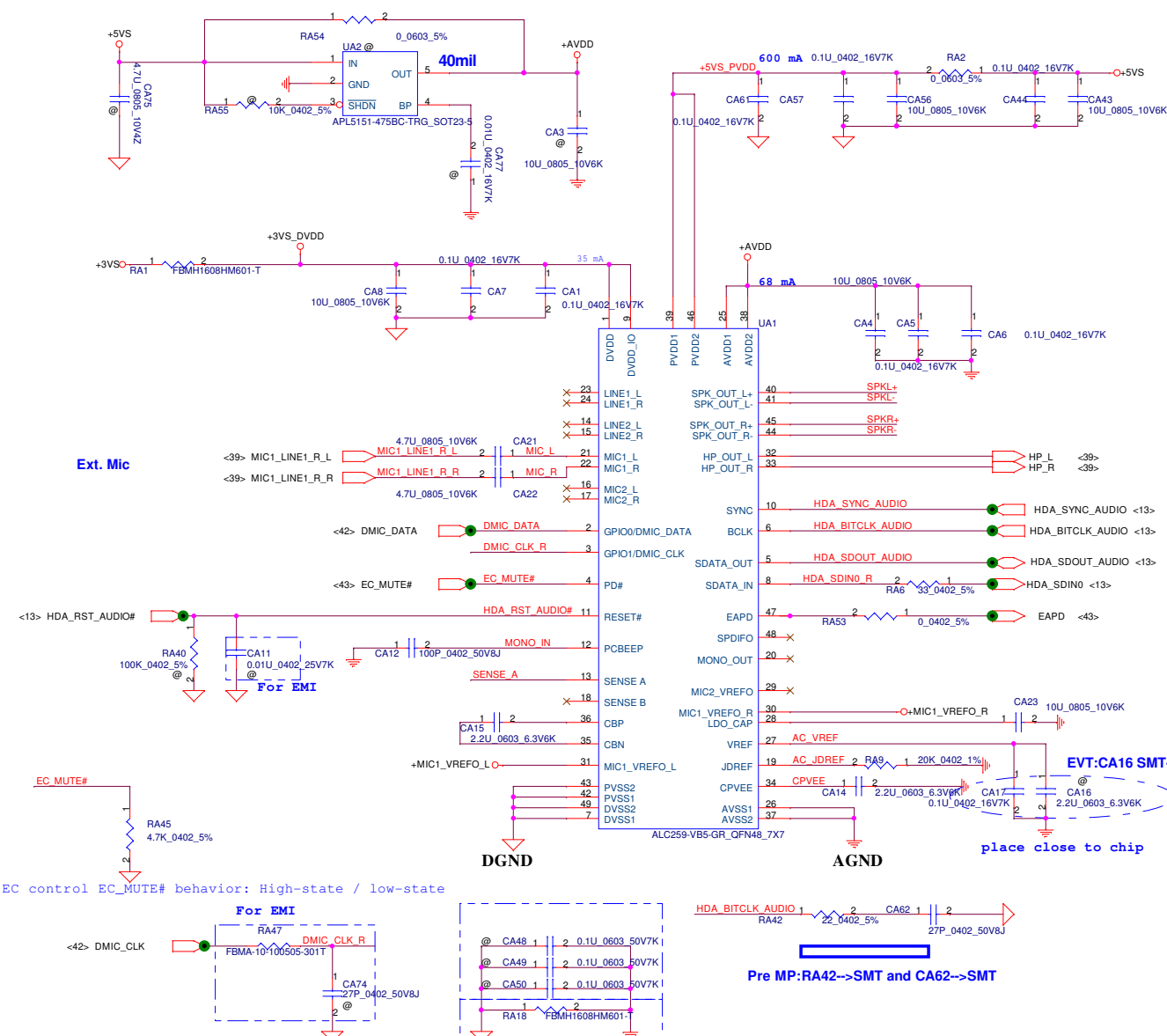
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Issued Date	2010/08/23	Deciphered Date	2011/08/25	Title
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Size	C	Document Number		Rev 1.0
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CRT Connector

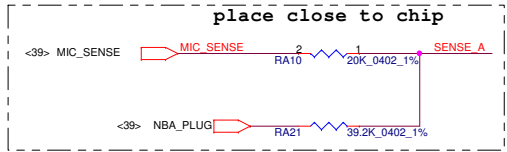


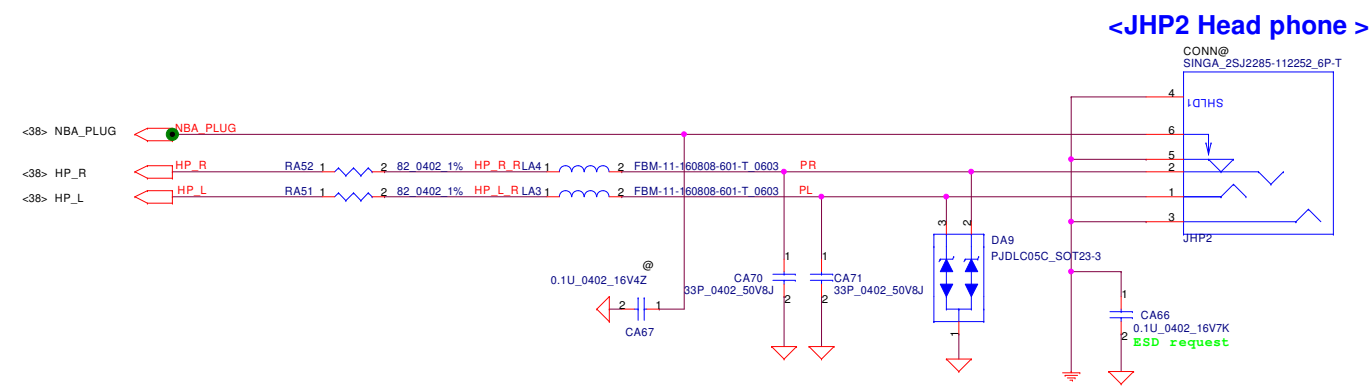
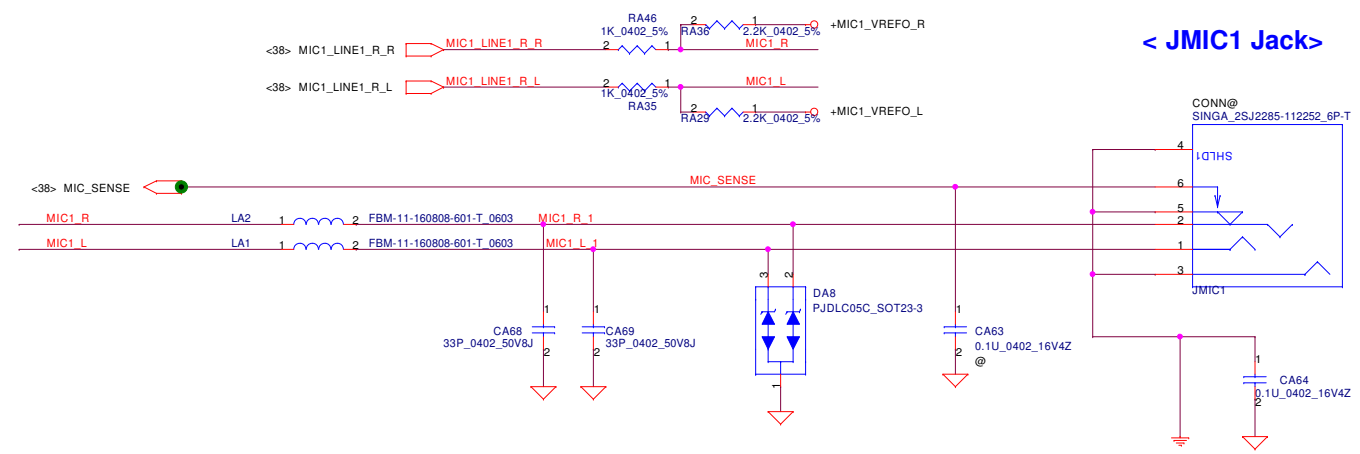
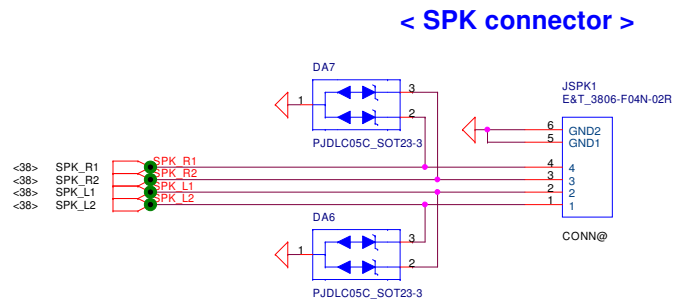
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2010/08/23	Deciphered Date	2011/08/25	Title CRT Connector		
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Date: Sunday, April 10, 2011				Sheet	36	of 56





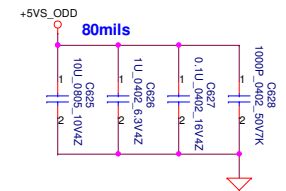
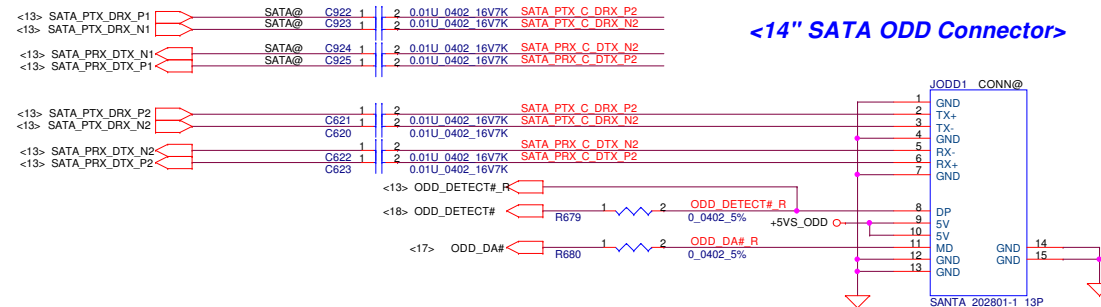
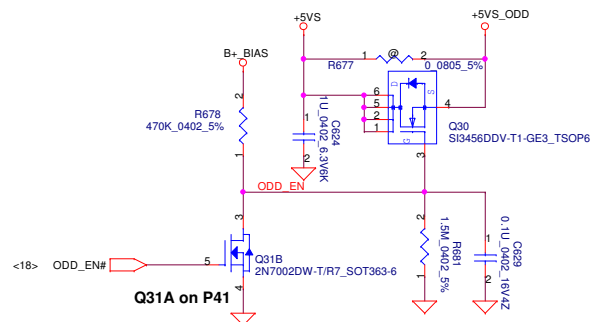
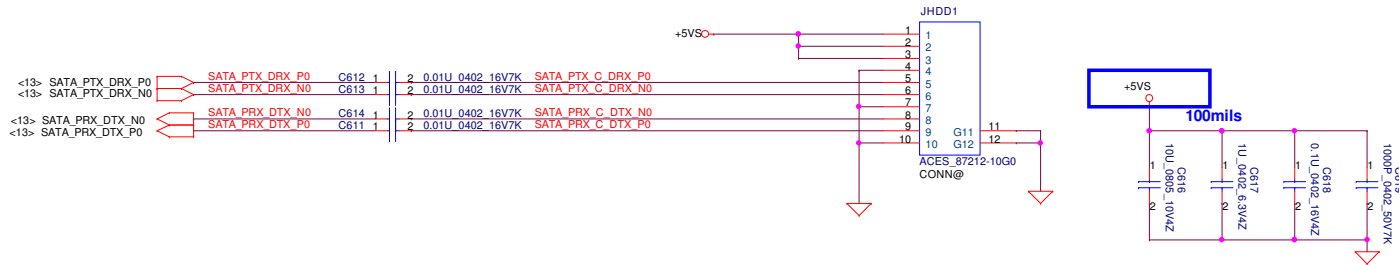
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	





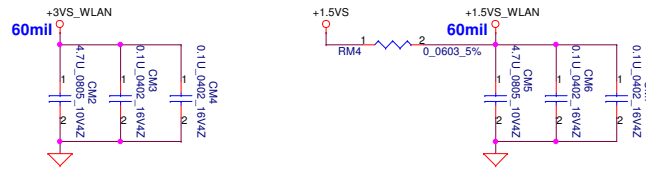
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SATA HDD1 Connector

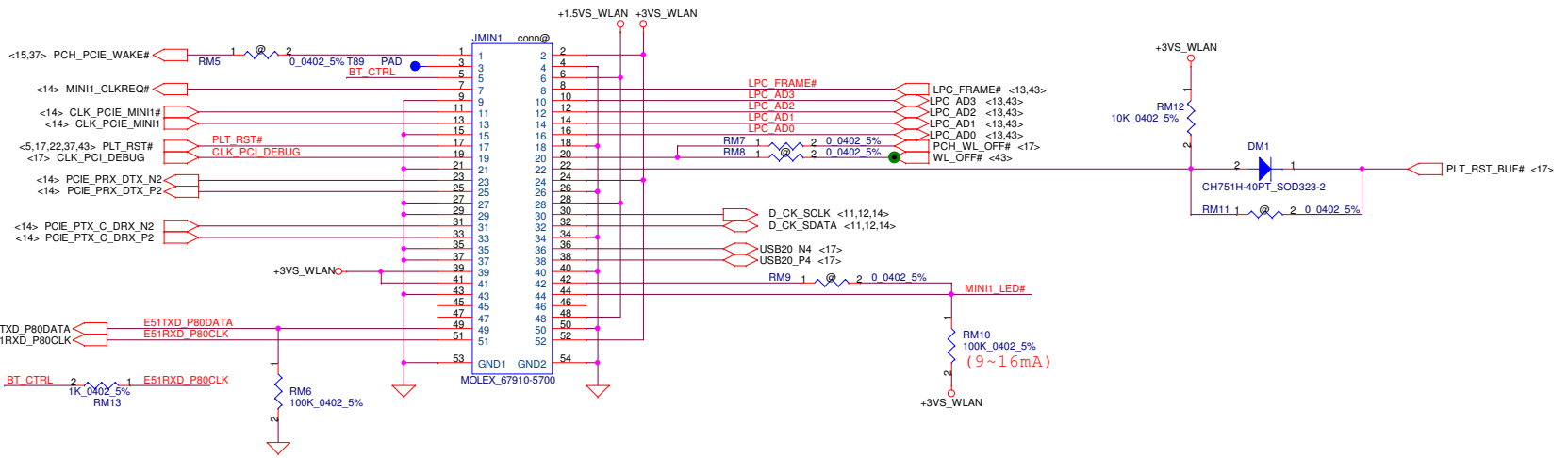


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				Custom			
				Date:	Sunday, April 10, 2011	Sheet 40 of 56	

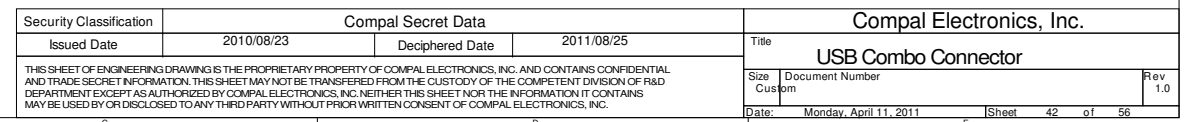
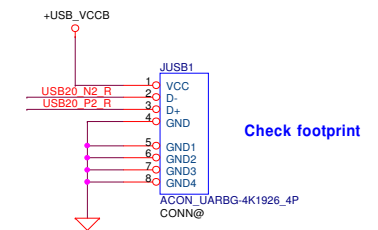
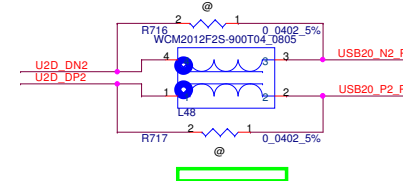
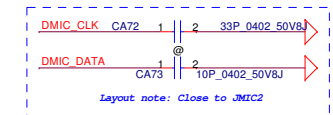
Wireless LAN

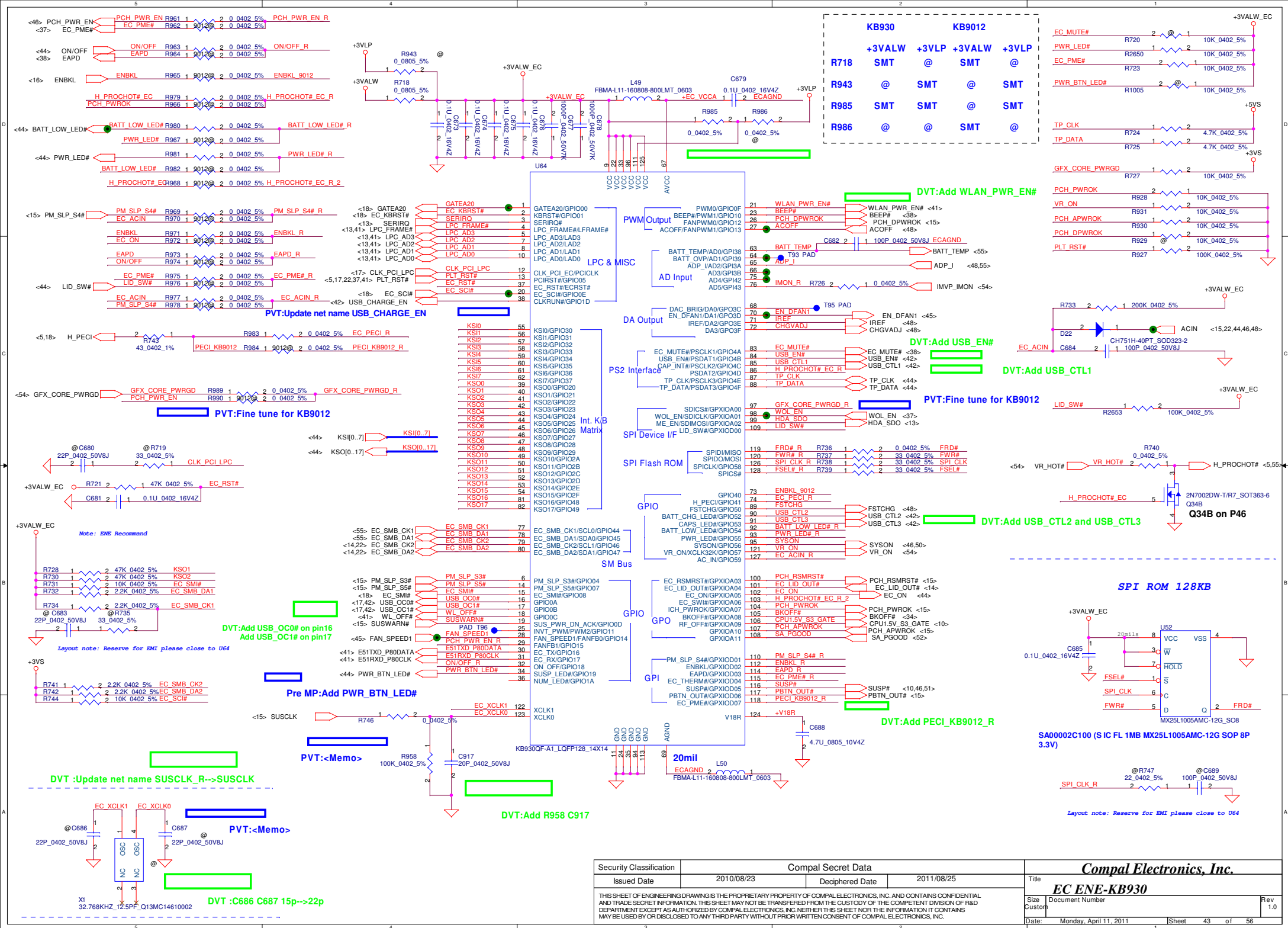


Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



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Deciphered Date				2011/08/25				MINI CARD WLAN & WWAN			
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Date: Monday, April 11, 2011				Sheet 41 of 56							

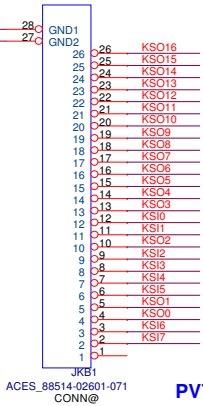




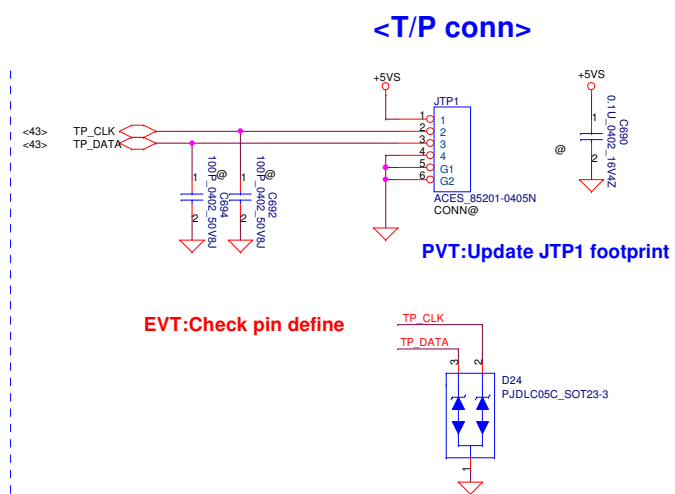
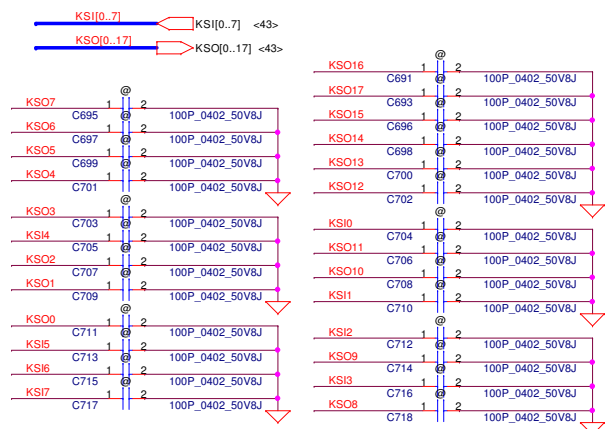
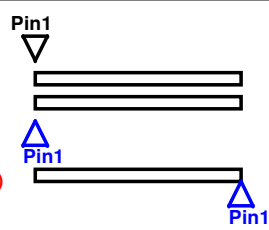
INT_KBD Connector
New key board

Key board pin define (Down)
CIS symbol (DVT)
CIS symbol (PVT need reverse pin define)

Key board Pin 1 is KSO16
Pin 2 is KSO15
...



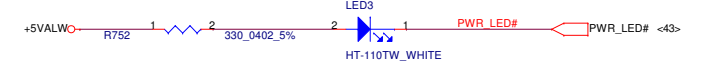
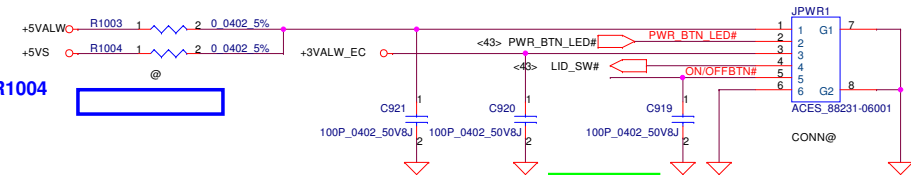
PVT:Update JKB1 footprint



<Power Button/Lid B conn>

<Power on LED>

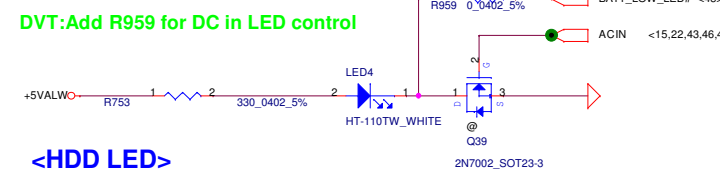
Pre MP:Add R1003 R1004



Power Button

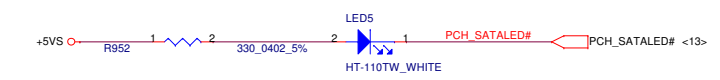
DVT:Update JPWR1 footprint and pin define

<AC in LED>



Pre MP:Update JPWR1 pin define

<HDD LED>



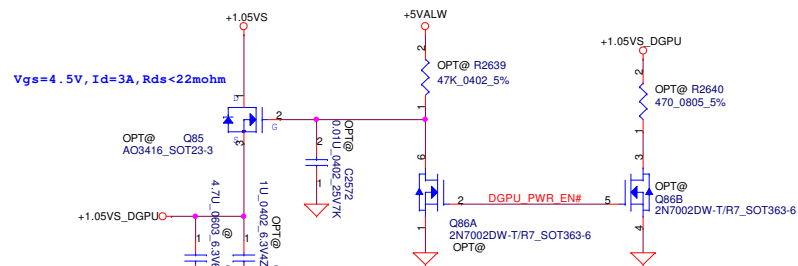
DVT:R759 pin1 +3VALW-->+3VALW_EC

DVT:Del R937

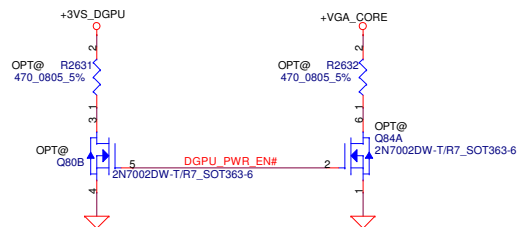
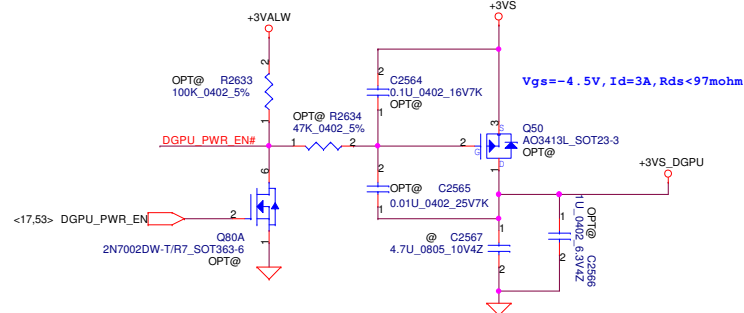
EC requirement

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Size	B	Document Number		Rev		
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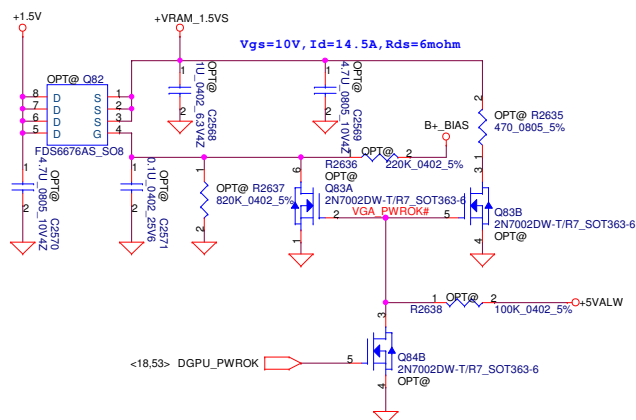
+1.05VS to +1.05VS_DGPU



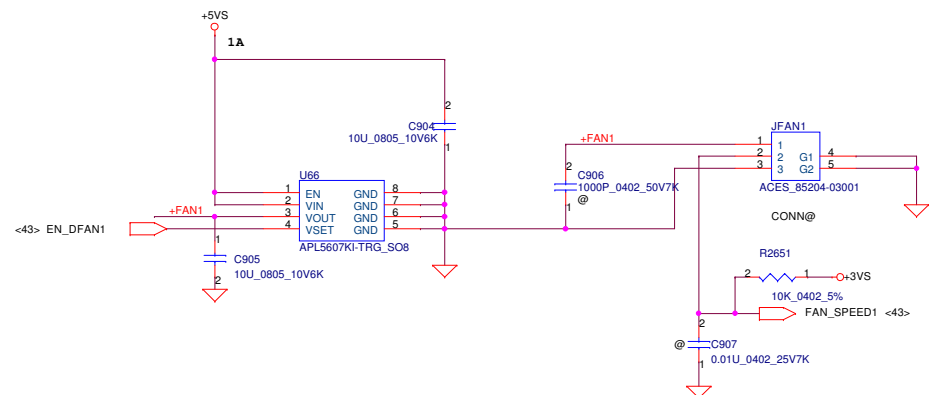
+3VS TO +3VS_DGPU



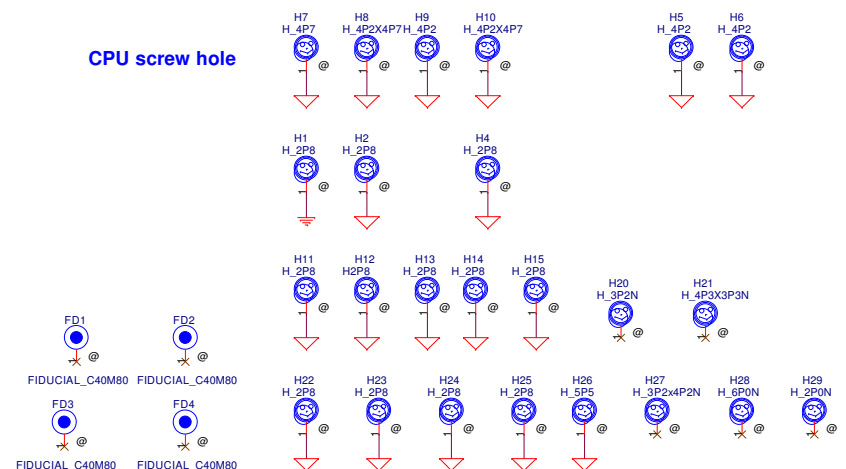
+1.5V to +VRAM_1.5VS



FAN Connector



CPU screw hole

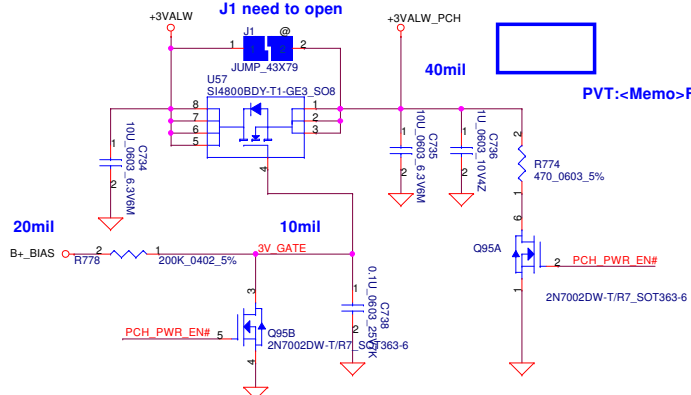


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				Size	Rev
				Custom	1.0
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+3VALW TO +3VALW(PCH AUX Power)

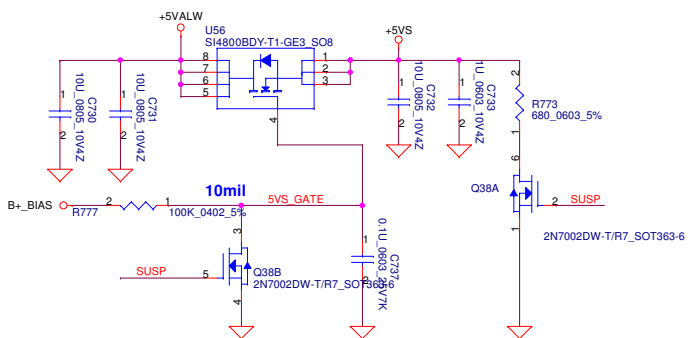
Short J1 for PCH VCCSUS3.3

J1 need to open

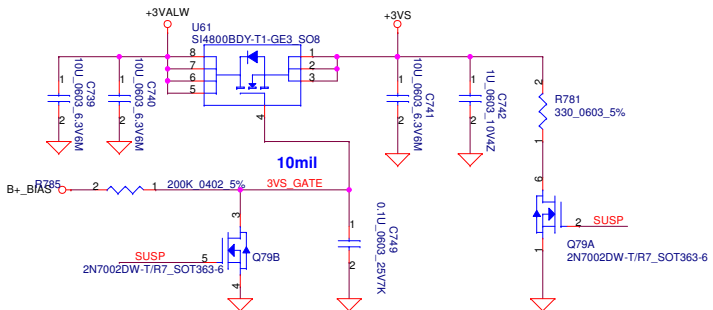


PVT:<Memo>Fine tune +3VALW_PCH power

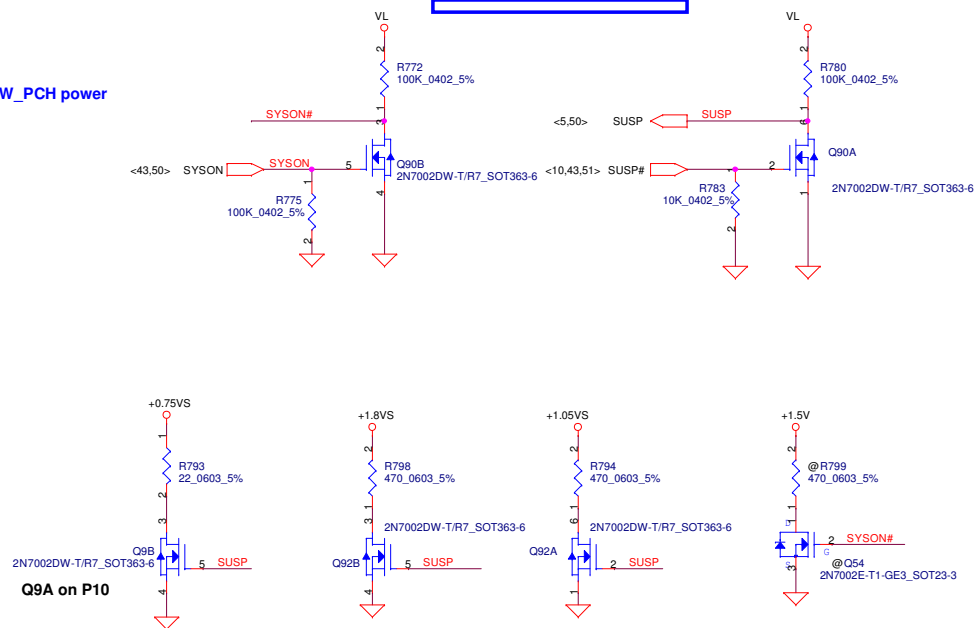
+5VALW TO +5VS



+3VALW TO +3VS

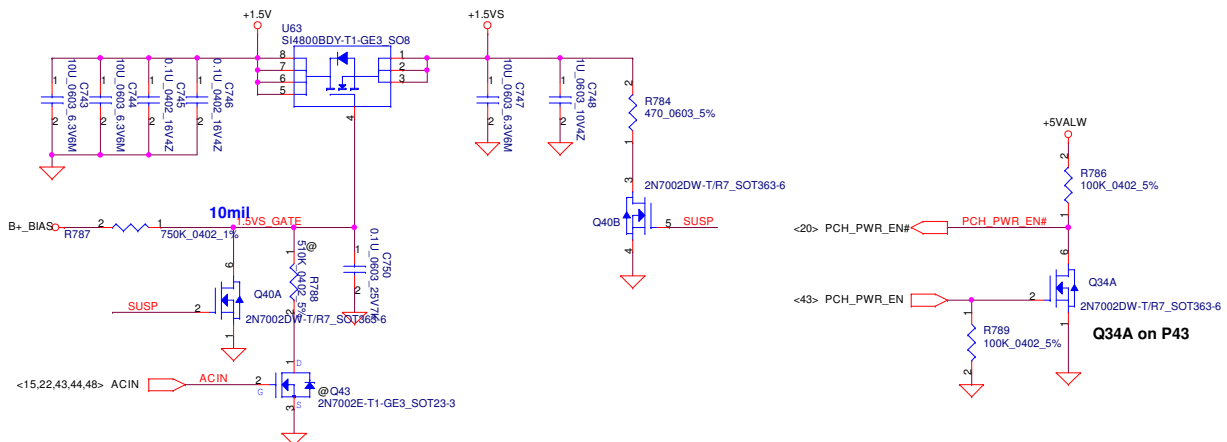


PVT:R780 R772 +5VALW-->VL



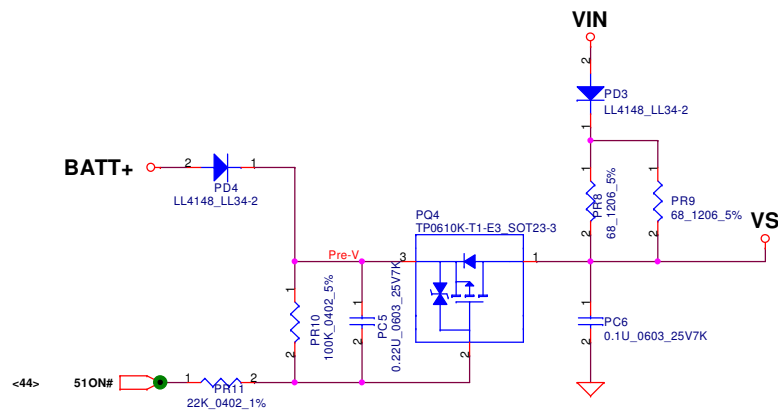
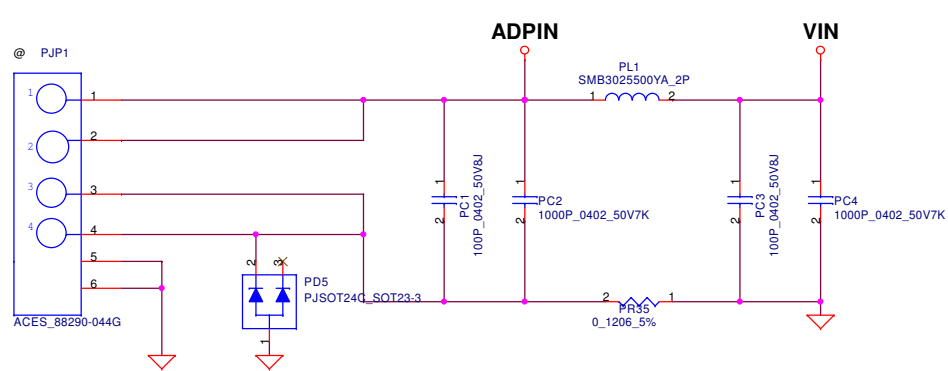
Q9A on P10

+1.5V to +1.5VS

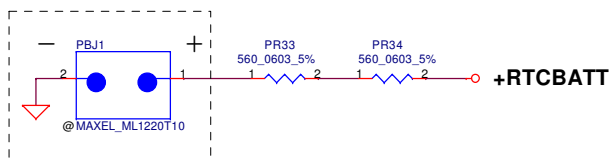


Q34A on P43

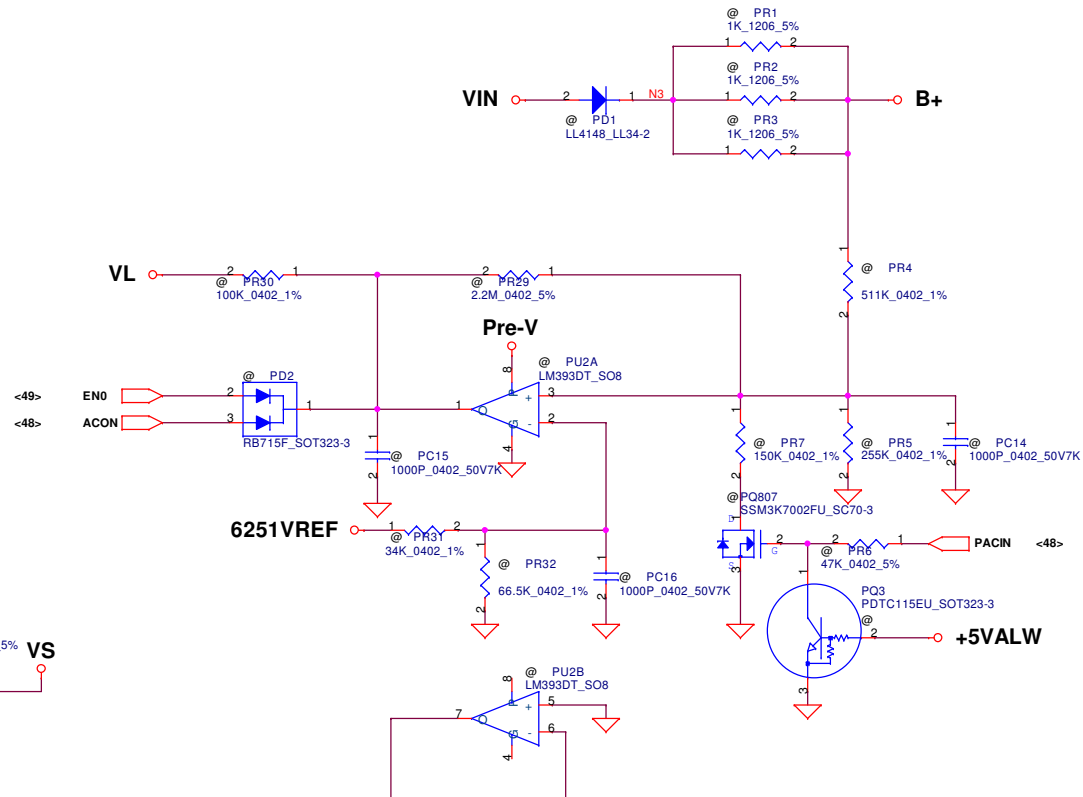
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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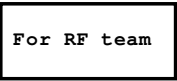
RTC Battery



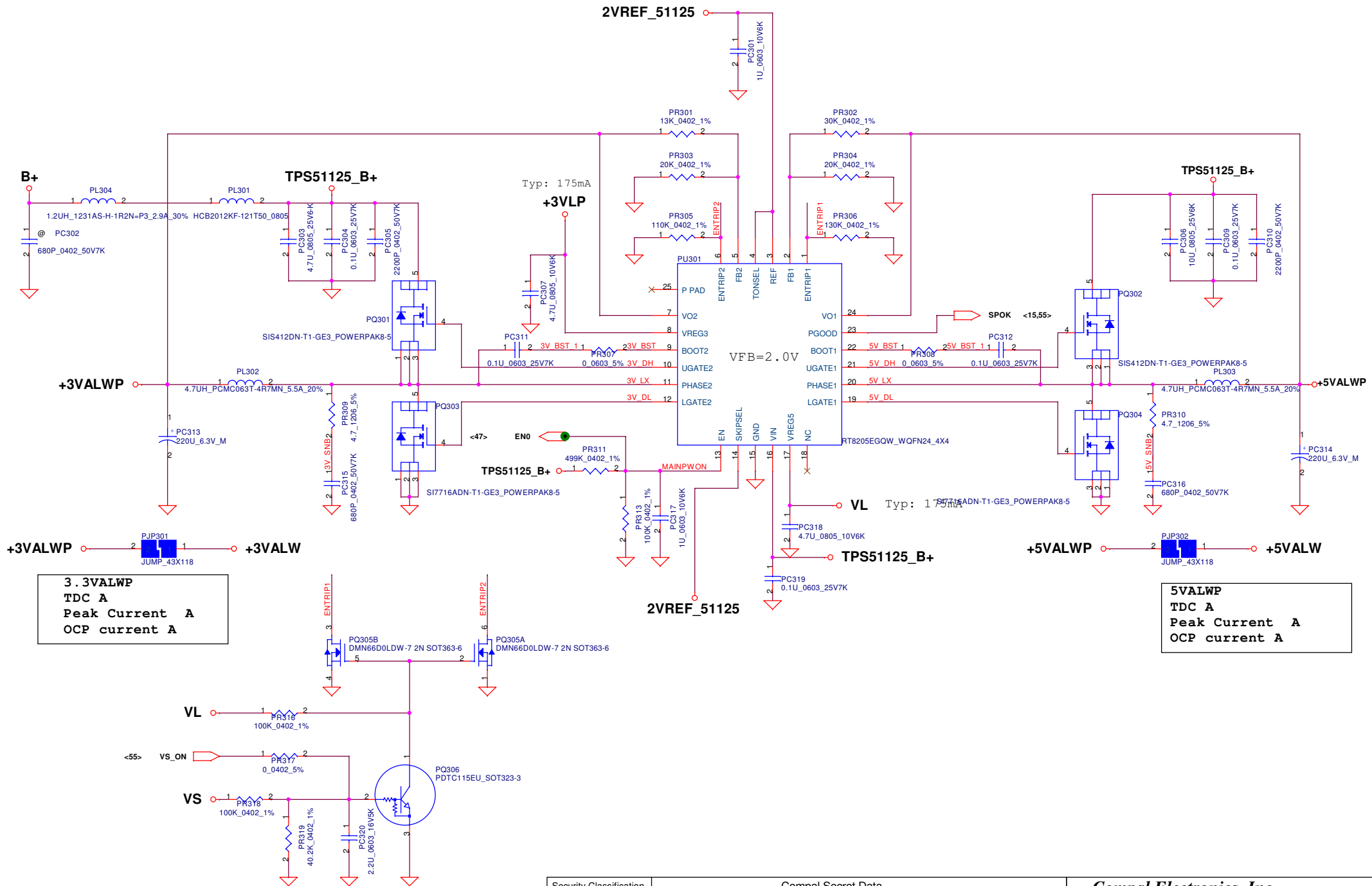
X7999651L01



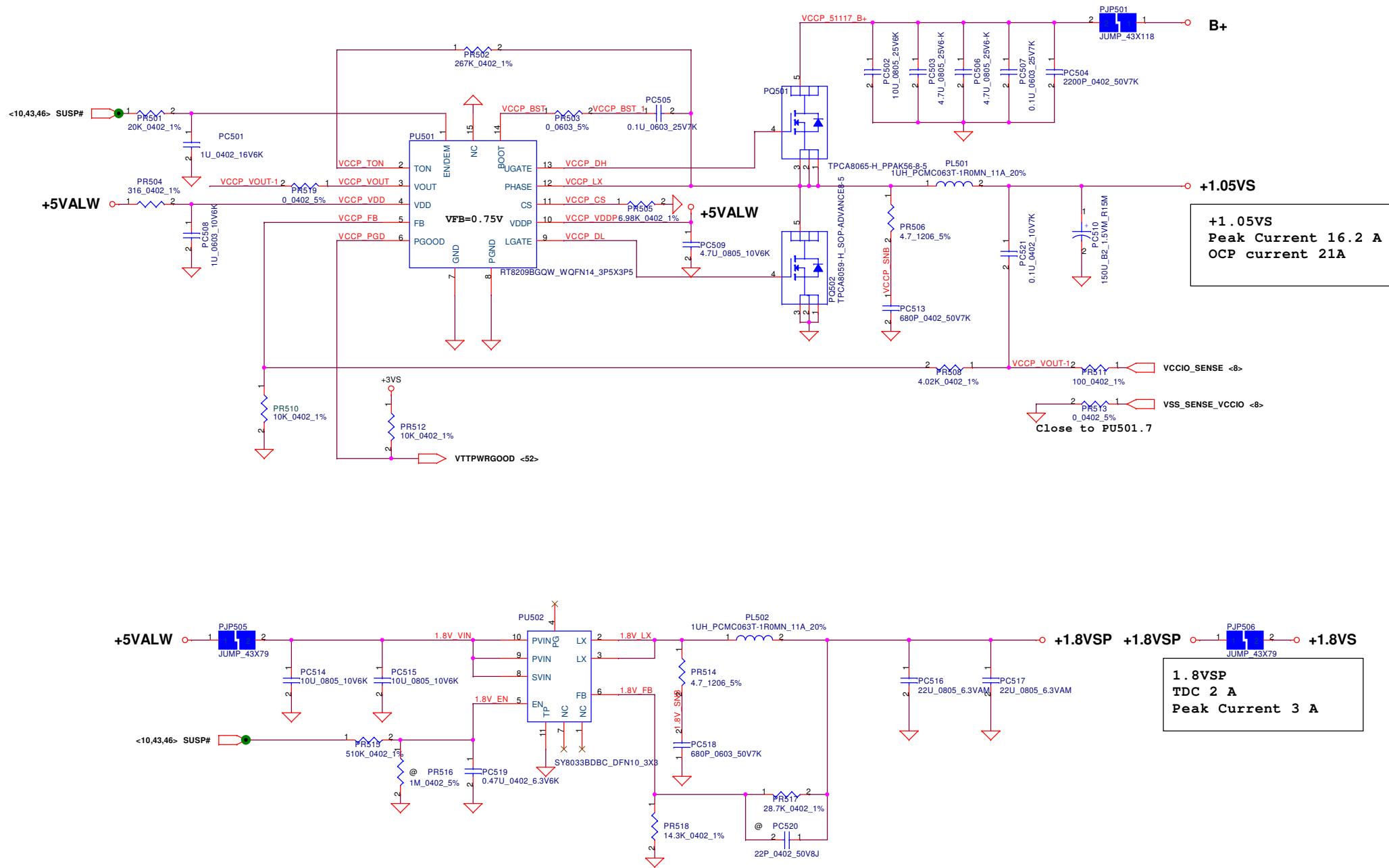
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				Rev	0.1



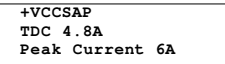
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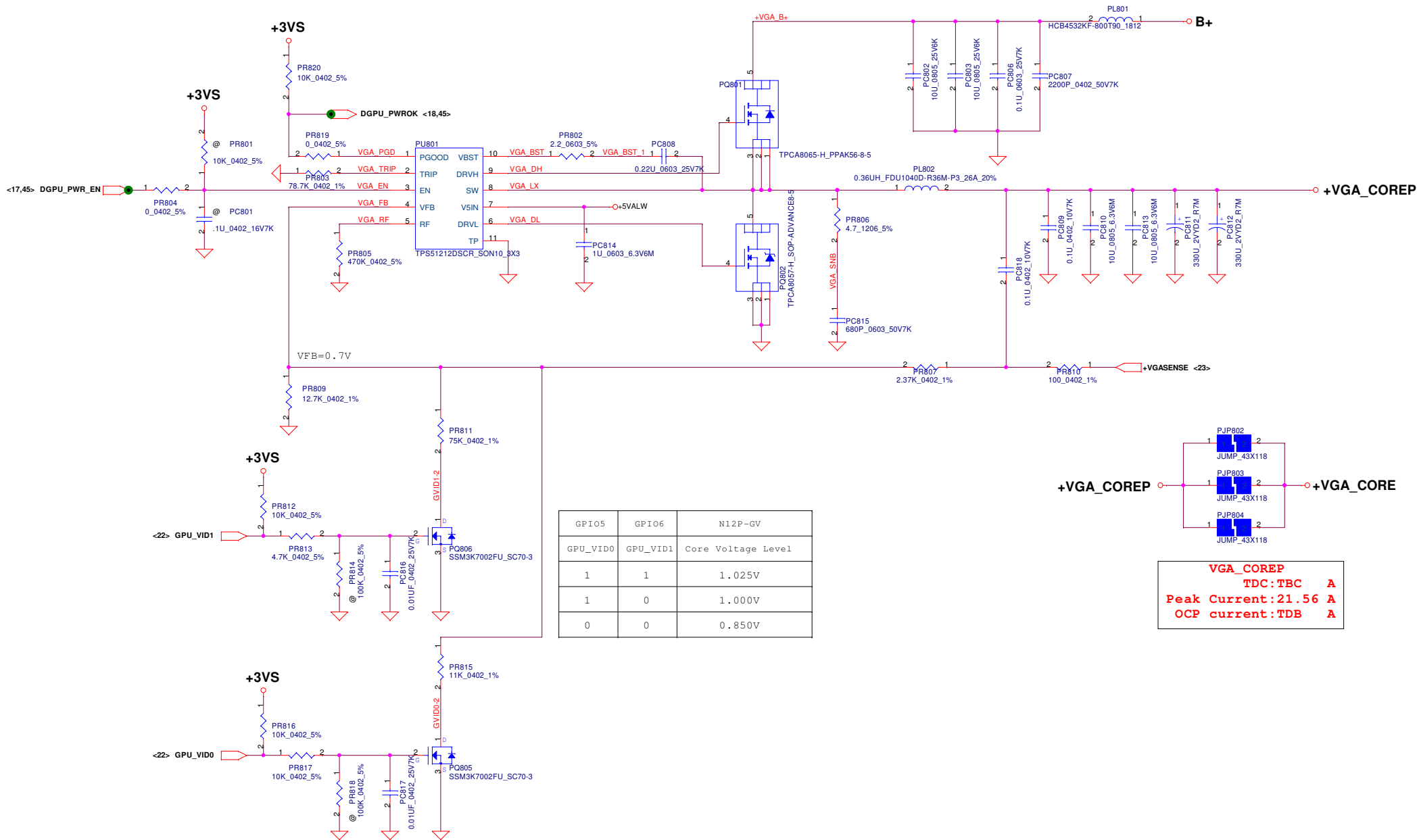
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/08/23	Deciphered Date	2011/12/31	Title	PWR-3VALWP/5VALWP
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					DB-806P	0.1
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Alert# PU resistor need close CPU,
so the PU resistor in HW schematic,
but DAT and CLK need close PWM-IC,
so the PU resistor in POWER schematic.

*Iccmax in Turbo Mode for SV (35W) is 53A

+CPU_CORE

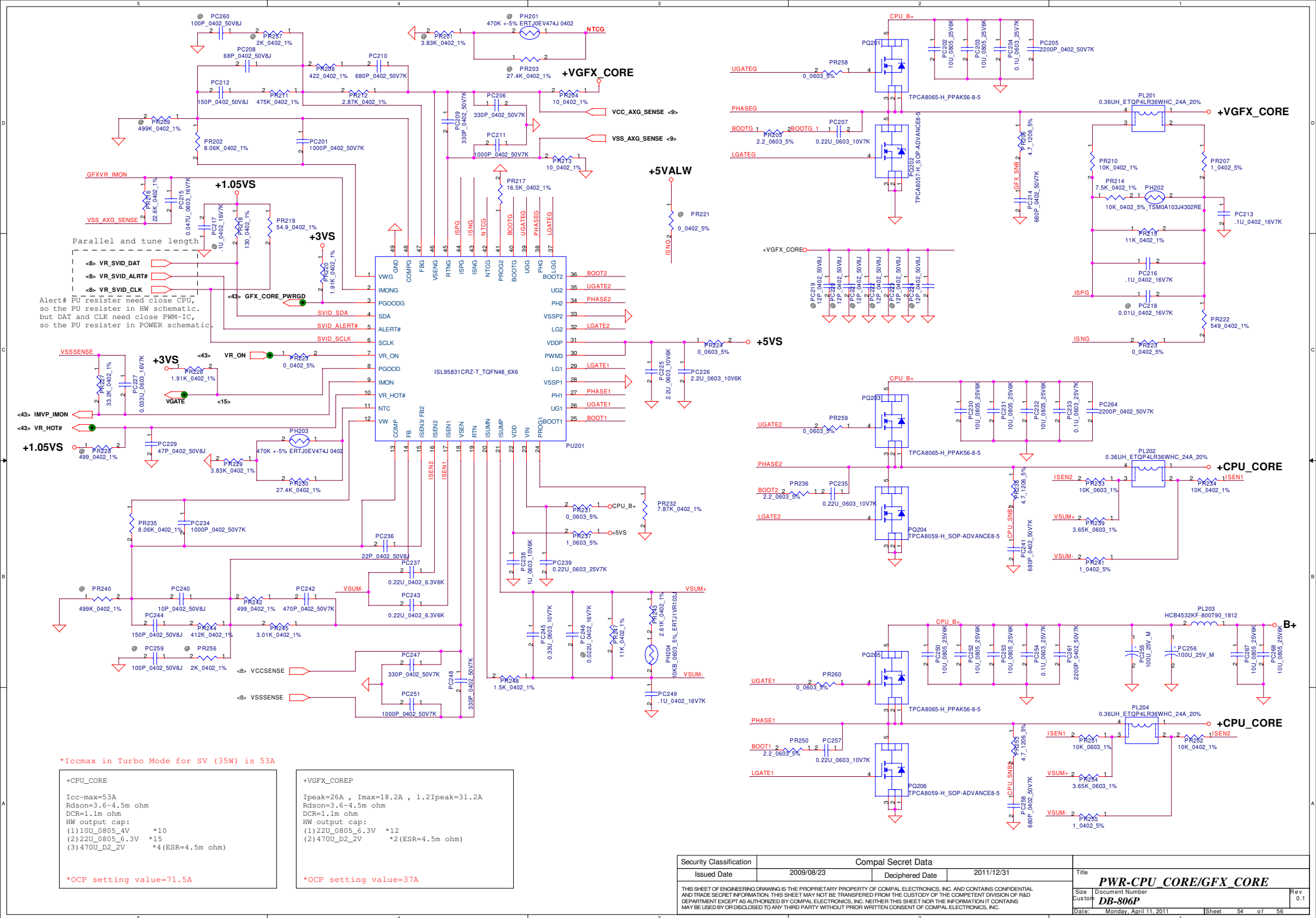
Icc-max=53A
Rdson=3.6~4.5m ohm
DCR=1.1m ohm
HW output cap:
(1) 10U_0805_4V *10
(2) 22U_0805_6.3V *15
(3) 470U_D2_2V *4 (ESR=4.5m ohm)

*OCP setting value=71.5A

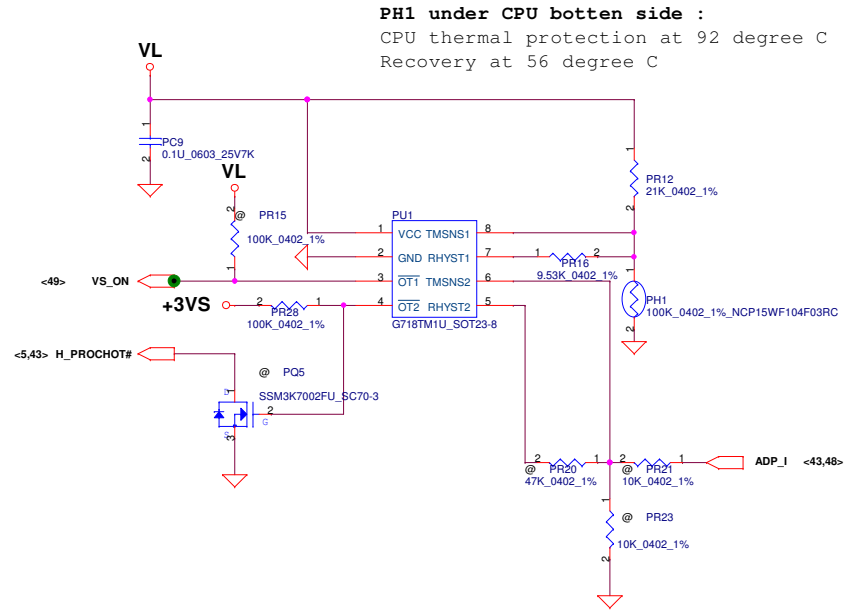
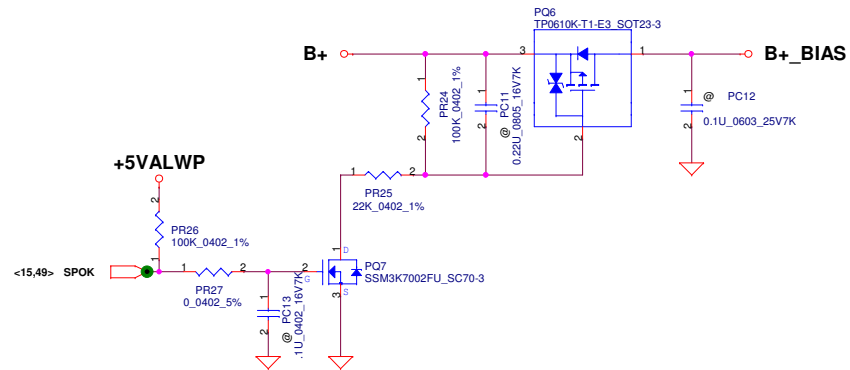
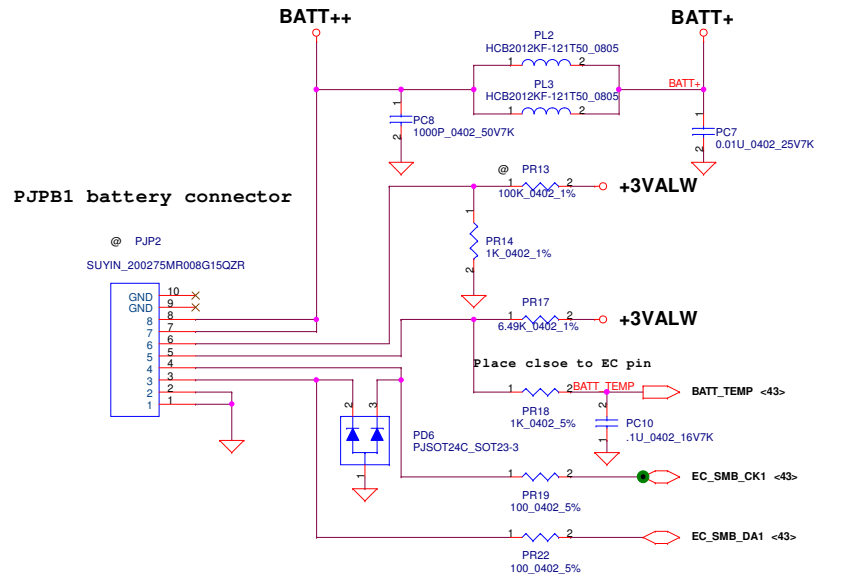
+VGFX_COREP

Ipeak=26A, Imax=18.2A, 1.2Ipeak=31.2A
Rdson=3.6~4.5m ohm
DCR=1.1m ohm
HW output cap:
(1) 22U_0805_6.3V *12
(2) 470U_D2_2V *2 (ESR=4.5m ohm)

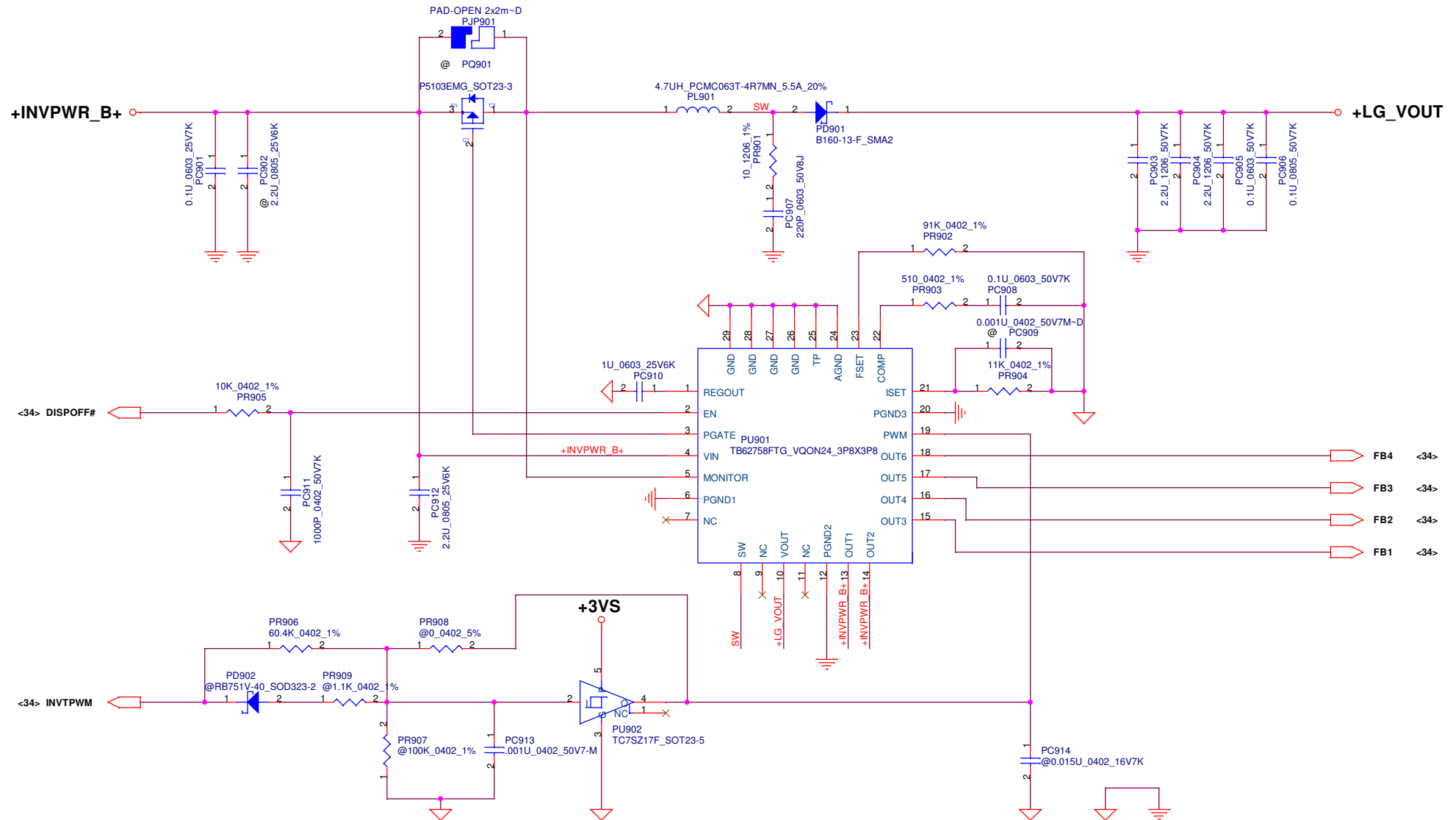
*OCP setting value=37A



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				PWR-LED Converter					
				Size B		Document Number		Rev 0.1	
				DB-806P					
Date:		Sunday, April 10, 2011		Sheet 56 of 56					