Siberia Block Diagram

Project code:91.4Q601.001
PCB P/N :48.4Q613.0SC
REVISION :06248-SC

Thermal Sensor EMC4001 20 — SMBus

Clock Generator CY28547LFXC 4

Intel Mobile CPU
Merom 4M
FSB:667/ 800 Mhz
5,6

HOST BUS — FSB 667/800MHz

SLi Graphic Card
- GPU
- GPU
- Bridge
- LCD — LVDS
- DVI Port — DVI-Out / RGB CRT
- TV-Out — S-Video / SPDIF

Graphic CONN. 15 — PCI-e x16

Crestline-PM
AGTL+ CPU I/F
DDR Memory I/F
EXTERNAL GRAHPICS
7,8,9,10,11,12

DDRII 533/667MHz — 200-PIN DDR2 SODIMM
UNBUFFERED DDR2 SODIMM Socket 13

DDRII 533/667MHz
UNBUFFERED DDR2 SODIMM Socket 14

SPDIF

DMI x4 — C-LINK0

Intel ICH8-M Enhanced
USB 2.0/1.1 ports (10)
PCI Express ports (6)
High Definition Audio
ATA 66/ 100
SATA (3)
LPC I/F
SPI
ACPI 1.1
PCI/PCI BRIDGE
16,17,18,19

- SATA HDD 21 — SATA (P0)
- SATA HDD 21 — SATA (P2) — SATA (2)
- ODD Bay 21 — PATA IDE
- INT. Speaker 5W x 2 25 — Speaker AMP. MAX9714 25
- INT. Digital Array MIC 24 — Azalia CODEC STAC 9228 24 — AZALIA / PCI BUS

PCI Express (6)

USB2.0 (10)

Power Switch 31

- PCIe (Lane4) — Express Card Slot 54mm 30
- PCIe (Lane3) — USB2.0 (P6) / USB2.0 (P4) — Mini-Card WPAN/Robson 31
- PCIe (Lane2) — Mini-Card 802.11a/g/n 30
- PCIe (Lane5) — PPU Card CONN. 29
- PCIe (Lane6) — BCM5754M Giga LAN 27 — RJ45 CONN 28
- PCIe (Lane1) — Mini-Card WWAN 31 — SIM CONN 31

USB2.0 (P9) / USB2.0 (P1) — USB CONN.x1 23

USB2.0 (P2,P3) — W to B CONN. 32 — USB2.0 (P2,P3) — USB CONN.x2 — Sniffer Board

USB2.0 (P8) — W to B CONN. 32 — USB2.0 (P8) — Gaming LCD Module

USB2.0 (P7) — Buletooth 2.1 36

USB2.0 (P5) — Camera Module 35

SPI — LPC

BIOS SPI FLASH 16Mb 36 — SPI

EC SMSC MEC5025 33 — BC — SIO Expander SMSC ECE5021 34

PS/2 — BC

Touch Pad CONN. 35

CIR 36 — CIR Board

PS/2 — BC

Touch Pad — KBC SMSC ECE1077 — Int. KB Numpad

Touch Pad Module

Audio Jack Board
- MIC IN
- LINE OUT / HP2
- LINE OUT / HP1
- W to B CONN. 26
- Headphone AMP. MAX4411 x 2 26

IO Board
- 7 in1 CONN — 7 in1
- 1394 CONN — 1394
- USB CONN.x1 — USB2.0 (P0)
- B to B CONN. 23
- Ricoh R5C833 7 in 1 card reader 1394 22

System DC/DC TPS51120 46

INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW +5V_SUS +3.3V_SUS +3.3V_RTC_LDO

System DC/DC SN0508073 44

+PWR_SRC	+1.5V_RUN +1.25V_RUN

DDR2 DC/DC SN0508073 45

+PWR_SRC	+1.8V_SUS +1.05V_VCCP

LDO TPS51100 47

+1.8V_SUS	+0.9V_DDR_VTT

LDO MAX668 47

+PWR_SRC	+12V_S

Battery Charger ISL88731 41

INPUTS	OUTPUTS
+PWR_SRC	+VCHGR

CPU DC/DC ISL6260C 42,43

INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

PCB LAYER

L1:TOP
L2:GND
L3:Signal
L4:Signal
L5:VCC
L6:Signal
L7:GND
L8:BOT

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CLOCK GEN CY28547

27M_SS/LCD96_100M SELECTION TABLE

BYTE 10

Bit5 S1	Bit4 S0	Spread Spectrum S[1:0]
0	0	-0.5%(Default)
0	1	-1.0%
1	0	-1.5%
1	1	-2.0%

BYTE 15
IO_VOUT[2,1,0]

Bit2 IO_VOUT2	Bit1 IO_VOUT1	Bit0 IO_VOUT0	IO_VOUT[2,1,0]
0	0	0	0.3V
0	0	1	0.4V
0	1	0	0.5V
0	1	1	0.6V
1	0	0	0.7V
1	0	1	0.8V(Default)
1	1	0	0.9V
1	1	1	1.0V

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

INTEL CRESTLINE STRAP PIN

CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4 ★
CFG 9 PCI Express Graphics Lane Reversal	Lane Reversal	Normal Mode(Lanes number in order) ★
CFG 16 FSB Dynamic ODT	Disabled	Enabled ★
CFG 19 DMI Lane Reserved	Normal Operation ★	Lane Reserved
CFG 20 Concurrent SDVO/PCIE	Only PCIE or SDVO is operation ★	PCIE and SDVO are operation simultaneous
SDVO_CTRL_DATA SDVO Present	NO SDVO Card Present ★	SDVO Card Present

CFG 12 CFG 13	XOR/ALL-Z
LL(00)	Reserved
LH(01)	XOR Mode Enabled
HL(10)	All Z Mode Enabled
HH(11)	Normal Operation

PCIE Routing

LANE1	MiniCard WWAN
LANE2	MiniCard WLAN
LANE3	BT/UWB/Robson
LANE4	Express Card
LANE5	PPU card
LANE6	Giba Bit LOM

PCI ROUTING

	IDSEL	INT	REQ	GNT
1394/ MediaCard	AD17	C D	1	1

USB TABLE

ICH

USB0	Ext Lift Side
USB1	Ext Back
USB2	Ext Right Side (Top)
USB3	Ext Right Side (Bottom)
USB4	3rd mini card
USB5	Camera
USB6	Express Card
USB7	BT
USB8	Gaming LCD
USB9	WWAN

INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved. Rising Edge of PWROK.	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCL1_5 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05,VccSus1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIE LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overidden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap

ICH_RSVD/tp3	AZ_DOUT_ICH	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation(default)
1	1	Set PCIE port cofig bit1

A16 swap override strap

PCI_GNT#3	low = A16 swap override enable high = default

BOOT BIOS Strap

PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

integrated VccSus1_05,VccSus1_5,VccCL1_5

SM_INTVRMEN	High=Enable	Low=Disable

integrated VccLan1_05VccCL1_05

LAN100_SLP	High=Enable	Low=Disable

DEFAULE HIGH

No Reboot Strap

SPKR	LOW = Defaule High=No Reboot

8.2K PULL HIGH

INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 10K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST0#	PULL-UP 13K

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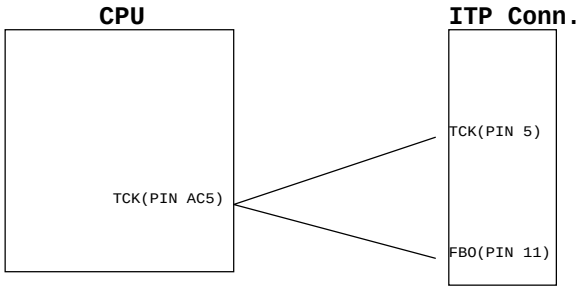

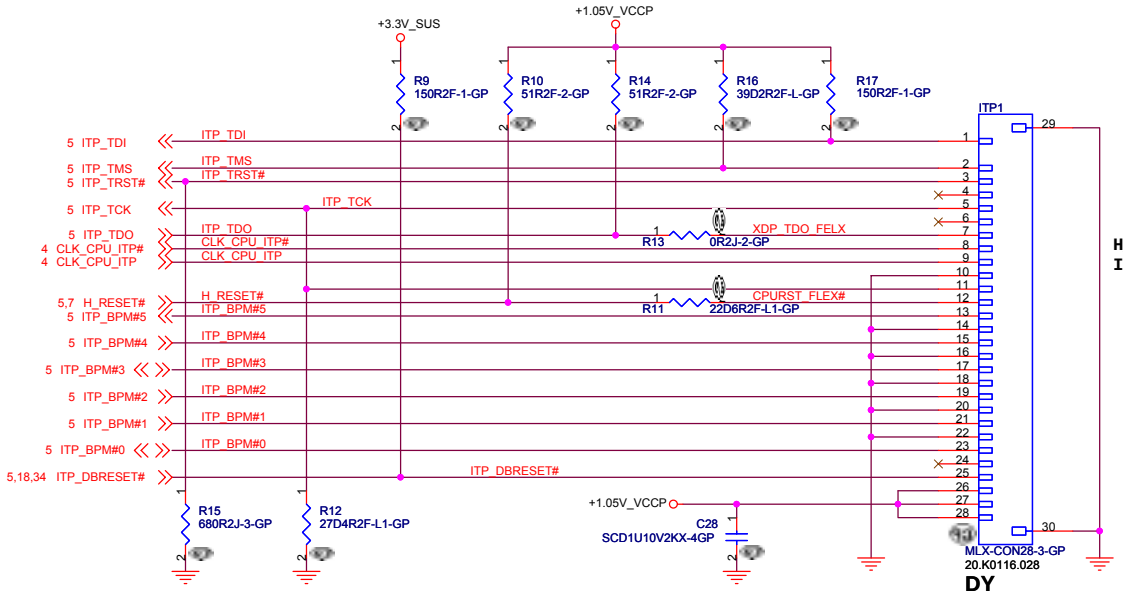

H_RESET# use pull-up Resistor close ITP connector 500 mil (max)

+1.05V_VCCP use Decoupling Capacitor close ITP connector 100 mil (max)

ITP Debug Conn.

<Variant Name>

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SMBus address:D2

Place near C10

Pull low to Decide
VTT_PWRGO Low active

Enable ITP

Enable TME

CL=20pF±0.2pF
Freq. Tolerance:±30ppm

For wireless performance

Clock Gen.
1st source: ICS ICS9LPR333CKLF (71.09333.A03)
2nd source: Cypress CY28547LFXC (71.28547.003)

Solder Thermal Pad to
GND add min 4 vias

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

PCI_TPM=FCTSEL1

PIN34 FCTSEL1	0	1
PIN43	DOT96T	27M_NonSpread
PIN44	DOT96C	27M_Spread
PIN47	LCD100/96T	SRCT_0
PIN48	LCD100/96C	SRCC_0

CLKREQ PULL HIGH

PIN9 PGMODE	PIN39 DISCRIPTION
0	VTT_PWRGD#/PD
1	CKPWRGD/PD#(DEFAULT)

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Title: CLK GEN CY28547

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H_D#[63..0] H_D#[63..0] 7
H_A#[35..3] H_A#[35..3] 7
H_REQ#[4..0] H_REQ#[4..0] 7
H_RS#[2..0] H_RS#[2..0] 7

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ADDR GROUP 0
H_A#3 J4 A3#
H_A#4 L5 A4#
H_A#5 L4 A5#
H_A#6 K5 A6#
H_A#7 M3 A7#
H_A#8 N2 A8#
H_A#9 J1 A9#
H_A#10 N3 A10#
H_A#11 P5 A11#
H_A#12 P2 A12#
H_A#13 L2 A13#
H_A#14 P4 A14#
H_A#15 P1 A15#
H_A#16 R1 A16#
7 H_ADSTB#0 H_ADSTB#0 M1 ADSTB0#

H_REQ#0 K3 REQ0#
H_REQ#1 H2 REQ1#
H_REQ#2 K2 REQ2#
H_REQ#3 J3 REQ3#
H_REQ#4 L1 REQ4#

ADDR GROUP 1
H_A#17 Y2 A17#
H_A#18 U5 A18#
H_A#19 R3 A19#
H_A#20 W6 A20#
H_A#21 U4 A21#
H_A#22 Y5 A22#
H_A#23 U1 A23#
H_A#24 R4 A24#
H_A#25 T5 A25#
H_A#26 T3 A26#
H_A#27 W2 A27#
H_A#28 W5 A28#
H_A#29 Y4 A29#
H_A#30 U2 A30#
H_A#31 V4 A31#
H_A#32 W3 A32#
H_A#33 AA4 A33#
H_A#34 AB2 A34#
H_A#35 AA3 A35#
7 H_ADSTB#1 H_ADSTB#1 V1 ADSTB1#

CONTROL
ADS# H1 H_ADS# H_ADS# 7
BNR# E2 H_BNR# H_BNR# 7
BPRI# G5 H_BPRI# H_BPRI# 7
DEFER# H5 H_DEFER# H_DEFER# 7
DRDY# F21 H_DRDY# H_DRDY# 7
DBSY# E1 H_DBSY# H_DBSY# 7
BR0# F1 H_BR0# H_BR0# 7
IERR# D20 H_IERR#
INIT# B3 H_INIT# H_INIT# 16
LOCK# H4 H_LOCK# H_LOCK# 7
RESET# C1 H_RESET# H_RESET# 3,7
RS0# F3 H_RS#0
RS1# F4 H_RS#1
RS2# G3 H_RS#2
TRDY# G2 H_TRDY# H_TRDY# 7
HIT# G6 H_HIT# H_HIT# 7
HITM# E4 H_HITM# H_HITM# 7

+1.05V_VCCP
R28 56R2J-4-GP

XDP/ITP SIGNALS
BPM0# AD4 ITP_BPM#0 ITP_BPM#0 3
BPM1# AD3 ITP_BPM#1 ITP_BPM#1 3
BPM2# AD1 ITP_BPM#2 ITP_BPM#2 3
BPM3# AC4 ITP_BPM#3 ITP_BPM#3 3
PRDY# AC2 ITP_BPM#4 ITP_BPM#4 3
PREQ# AC1 ITP_BPM#5 ITP_BPM#5 3
TCK AC5 ITP_TCK ITP_TCK 3
TDI AA6 ITP_TDI ITP_TDI 3
TDO AB3 ITP_TDO ITP_TDO 3
TMS AB5 ITP_TMS ITP_TMS 3
TRST# AB6 ITP_TRST# ITP_TRST# 3
DBR# C20 ITP_DBRESET# ITP_DBRESET# 3,18,34

THERMAL
EC_CPU_PROCHOT# 33
PROCHOT# D21 H_THERMDA 20
THRMDA A24 H_THERMDA
THRMDC B25 H_THERMDC
C63 SC2200P50V2KX-2GP DY
H_THERMDC 20
THERMTRIP# C7 H_THERMTRIP# H_THERMTRIP# 20

ICH
16 H_A20M# H_A20M# A6 A20M#
16 H_FERR# H_FERR# A5 FERR#
16 H_IGNNE# H_IGNNE# C4 IGNNE#
16 H_STPCLK# H_STPCLK# D5 STPCLK#
16 H_INTR# H_INTR# C6 LINT0
16 H_NMI# H_NMI# B4 LINT1
16 H_SMI# H_SMI# A3 SMI#

HCLK
BCLK0 A22 CLK_CPU_BCLK CLK_CPU_BCLK 4
BCLK1 A21 CLK_CPU_BCLK# CLK_CPU_BCLK# 4

RESERVED
TPAD28 TP6 CPU_RSVD01 M4 RSVD#M4
TPAD28 TP8 CPU_RSVD02 N5 RSVD#N5
TPAD28 TP7 CPU_RSVD03 T2 RSVD#T2
TPAD28 TP3 CPU_RSVD04 V3 RSVD#V3
TPAD28 TP51 CPU_RSVD05 B2 RSVD#B2
TPAD28 TP4 CPU_RSVD06 C3 RSVD#C3
TPAD28 TP2 CPU_RSVD07 D2 RSVD#D2
TPAD28 TP10 CPU_RSVD08 D22 RSVD#D22
TPAD28 TP5 CPU_RSVD09 D3 RSVD#D3
TPAD28 TP9 CPU_RSVD10 F6 RSVD#F6
B1 KEY_NC

SKT-CPU478P-GP
62.10079.021

Use old Symbol replace New P/N
original value:MEROM-CPU479P-GP-U

U76B 2 OF 4

DATA GRP2
H_D#0 E22 D0#
H_D#1 F24 D1#
H_D#2 E26 D2#
H_D#3 G22 D3#
H_D#4 F23 D4#
H_D#5 G25 D5#
H_D#6 E25 D6#
H_D#7 F23 D7#
H_D#8 K24 D8#
H_D#9 G24 D9#
H_D#10 J24 D10#
H_D#11 J23 D11#
H_D#12 H22 D12#
H_D#13 F26 D13#
H_D#14 K22 D14#
H_D#15 H23 D15#
7 H_DSTBN#0 H_DSTBN#0 J26 DSTBN0#
7 H_DSTBP#0 H_DSTBP#0 H26 DSTBP0#
7 H_DINV#0 H_DINV#0 H25 DINV0#

D32# Y22 H_D#32
D33# AB24 H_D#33
D34# V24 H_D#34
D35# V26 H_D#35
D36# Y23 H_D#36
D37# T22 H_D#37
D38# U25 H_D#38
D39# U23 H_D#39
D40# Y25 H_D#40
D41# W22 H_D#41
D42# Y23 H_D#42
D43# W24 H_D#43
D44# W25 H_D#44
D45# AA23 H_D#45
D46# AA24 H_D#46
D47# AB25 H_D#47
DSTBN2# Y26 H_DSTBN#2 H_DSTBN#2 7
DSTBP2# AA26 H_DSTBP#2 H_DSTBP#2 7
DINV2# U22 H_DINV#2 H_DINV#2 7

DATA GRP3
H_D#16 N22 D16#
H_D#17 K25 D17#
H_D#18 P26 D18#
H_D#19 R23 D19#
H_D#20 L23 D20#
H_D#21 M24 D21#
H_D#22 L22 D22#
H_D#23 M23 D23#
H_D#24 P25 D24#
H_D#25 P23 D25#
H_D#26 P22 D26#
H_D#27 T24 D27#
H_D#28 R24 D28#
H_D#29 L25 D29#
H_D#30 T25 D30#
H_D#31 N25 D31#
7 H_DSTBN#1 H_DSTBN#1 L26 DSTBN1#
7 H_DSTBP#1 H_DSTBP#1 M26 DSTBP1#
7 H_DINV#1 H_DINV#1 N24 DINV1#

D48# AE24 H_D#48
D49# AD24 H_D#49
D50# AA21 H_D#50
D51# AB22 H_D#51
D52# AB21 H_D#52
D53# AC26 H_D#53
D54# AD20 H_D#54
D55# AE22 H_D#55
D56# AF23 H_D#56
D57# AC25 H_D#57
D58# AE21 H_D#58
D59# AD21 H_D#59
D60# AC22 H_D#60
D61# AD23 H_D#61
D62# AF22 H_D#62
D63# AC23 H_D#63
DSTBN3# AE25 H_DSTBN#3 H_DSTBN#3 7
DSTBP3# AF24 H_DSTBP#3 H_DSTBP#3 7
DINV3# AC20 H_DINV#3 H_DINV#3 7

MISC
GTLREF AD26
TEST1 C23
TEST2 D25
TEST3 C24
TEST4 AF26
TEST5 AF1
TEST6 A26
BSEL0 B22
BSEL1 B23
BSEL2 C21

COMP0 R26 COMP0 R297 1 27D4R2F-L1-GP
COMP1 U26 COMP1 R296 1 54D9R2F-L1-GP
COMP2 AA1 COMP2 R22 1 27D4R2F-L1-GP
COMP3 Y1 COMP3 R24 1 54D9R2F-L1-GP
DPRSTP# E5 H_DPRSTP# H_DPRSTP# 8,16,42
DPSLP# B5 H_DPSLP# H_DPSLP# 16
DPWR# D24 H_DPWR# H_DPWR# 7
PWRGOOD D6 H_PWRGOOD H_PWRGOOD 16
SLP# D7 H_CPUSLP# H_CPUSLP# 7
PSI# AE6 H_PSI# H_PSI# 42

SKT-CPU478P-GP

+1.05V_VCCP
R34 1KR2F-3-GP
V_CPU_GTLREF
R33 2KR2F-3-GP
R31 1KR2J-1-GP DY
R298 1KR2J-1-GP DY
C66 SCD1U10V2KX-4GP DY
R299 0R2J-2-GP DY

4,8 CPU_MCH_BSEL0 CPU_MCH_BSEL0
4,8 CPU_MCH_BSEL1 CPU_MCH_BSEL1
4,8 CPU_MCH_BSEL2 CPU_MCH_BSEL2

layout note:Zo =55 ohm , 0.5" MAX for GTLREF

PLACE C66 close to the TEST4 PIN, make sure TEST4 PIN routing is reference to GND and away from other noisy signals

TPAD28 TP11 TEST3
TPAD28 TP1 TEST5
For the purpose of testability, route thes signals through a ground referenced Zo=55ohm trace thatends in a via that is near a GND via and is accessible through an oscilloscope connection.

Note:
H_DPRSTP# need to daisy chain from ICH8 to IMVP6 to CPU

Make COMP[3..0] traces length shorter than 0.5". Trace should be at least 25 mils away from any other toggling signal.
COMP 0,2 connect Zo=27.4ohm.
COMP 1,3 connect Zo=55ohm.

+1.05V_VCCP
R21 1 DY 200R2F-L-GP H_PWRGOOD
R20 1 56R2J-4-GP H_THERMTRIP#
R30 1 56R2J-4-GP EC_CPU_PROCHOT#
R19 1 56R2J-4-GP H_FERR#
R23 1 DY 54D9R2F-L1-GP ITP_BPM#4

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SKT-CPU478P-GP

0SC

For NCTF

TP131 TPAD28

TP132 TPAD28

TP134 TPAD28

TP133 TPAD28

U76C 3 OF 4

SKT-CPU478P-GP

+VCC_CORE

+1.05V_VCCP

+1.05V_RUN

H_VID[6..0]

VCCSENSE

VSSSENSE

R26 100R2F-L1-GP-U

R27 100R2F-L1-GP-U

C508 SC10U6D3V5MX-3GP

C507 SCD01U16V2KX-3GP

TC1 SE220U2VDM-8GP

TC27 SE100U25VM-14GP

TC28 SE100U25VM-14GP

TC30 SE100U25VM-14GP

10uF 0805 X5R -> 85 degree C ,
Or better such As X6S and X7R

Please these inside socket cavity on L8 (North side Secondary)

Need to add 100uF cap on PWR_SRC for cap singing.
Please this capacitor near +VCC_CORE

Layout note:
Place C507 near
PIN B26

Layout note:
Place R26 and R27 within 1" of CPU.
Routing VCC_SENSE and VSS_SENSE at
27.4 ohms with 50 mils spacing.

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU-POWER (2/2)

Size: A3 | Document Number: Siberia | Rev: SC

Date: Friday, May 25, 2007 | Sheet 6 of 50

H_D#[63..0] H_D#[63..0] 5

H_A#[35..3] H_A#[35..3] 5

H_REQ#[4..0] H_REQ#[4..0] 5

H_RS#[2..0] H_RS#[2..0] 5

U84A 1 OF 10

HOST

CRESTLINE-GP-U-NF

H_REF Decoupling Crestline close Crestline 100 mil

+1.05V_VCCP

R49 1KR2F-3-GP

R48 2KR2F-3-GP

C71 SCD1U10V2KX-4GP

CRB v0.9 REQUEST

3,5 H_RESET#

5 H_CPUSLP#

H_SWING routing Trace width and Spacing use 10 / 20 mil

H_SWING Resistors and Capacitors close Caliistoga 500 mil (MAX)

From Schematic Design Checklit v.1201

221 1% pull high 100

1% pull low

R344 221R2F-2-GP

R343 100R2F-L1-GP-U

C548 SCD1U10V2KX-4GP

H_SCOMP and H_SCOMP# Resistors and Capacitors close Caliistoga 500 mil (MAX) Zo=55ohms

R74 54D9R2F-L1-GP

R77 54D9R2F-L1-GP

H_RCOMP routing Trace width and Spacing use 10 / 20 mil

R353 24D9R2F-L-GP

Wistron Corporation
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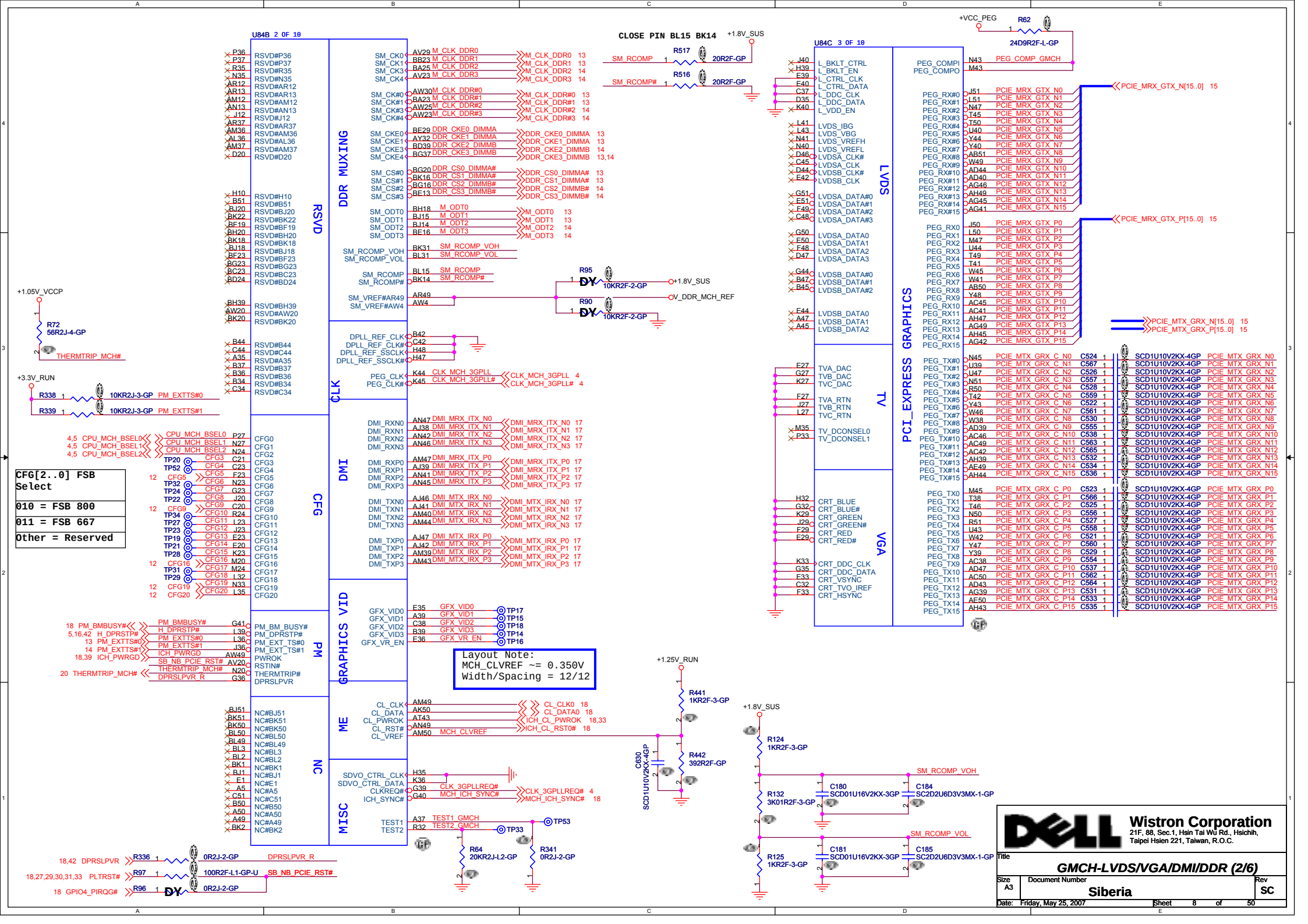
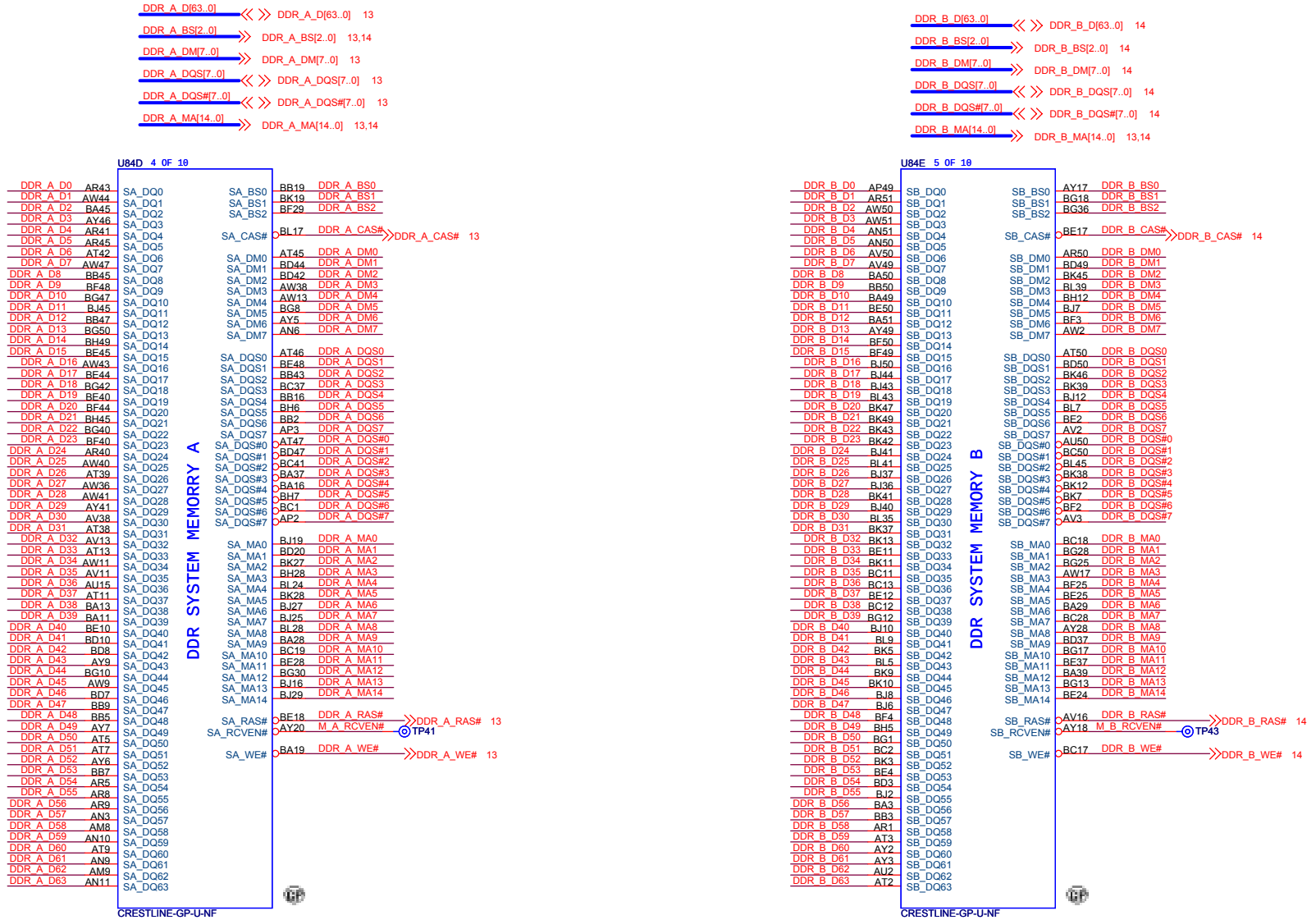
Taipei Hsien 221, Taiwan, R.O.C.

Title: GMCH-FSB LIBC (1/6)

Size: A3 | Document Number: Siberia | Rev: SC

Date: Friday, May 25, 2007 | Sheet 7 of 50


U84B 2 OF 10
RSVD
DDR MUXING
CLK
DMI
CFG
GRAPHICS VID
PM
ME
NC
MISC
U84C 3 OF 10
LVDS
PCI_EXPRESS GRAPHICS
TV
VGA
CLOSE PIN BL15 BK14
+1.8V_SUS
+VCC_PEG
R62
24D9R2F-L-GP
R517
20R2F-GP
R516
20R2F-GP
SM_RCOMP
SM_RCOMP#
R95
DY
10KR2F-2-GP
R90
DY
10KR2F-2-GP
V_DDR_MCH_REF
+1.05V_VCCP
R72
56R2J-4-GP
THERMTRIP_MCH#
+3.3V_RUN
R338
10KR2J-3-GP
PM_EXTTS#0
R339
10KR2J-3-GP
PM_EXTTS#1
CFG[2..0] FSB Select
010 = FSB 800
011 = FSB 667
Other = Reserved
Layout Note:
MCH_CLVREF ~= 0.350V
Width/Spacing = 12/12
+1.25V_RUN
R441
1KR2F-3-GP
R442
392R2F-GP
C630
SCD1U10V2KX-4GP
+1.8V_SUS
R124
1KR2F-3-GP
R132
3K01R2F-3-GP
R125
1KR2F-3-GP
C180
SCD01U16V2KX-3GP
C181
SCD01U16V2KX-3GP
C184
SC2D2U6D3V3MX-1-GP
C185
SC2D2U6D3V3MX-1-GP
SM_RCOMP_VOH
SM_RCOMP_VOL
R64
20KR2J-L2-GP
R341
0R2J-2-GP
TP53
R336
0R2J-2-GP
DPRSLPVR_R
R97
100R2F-L1-GP-U
SB_NB_PCIE_RST#
R96
DY
0R2J-2-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
GMCH-LVDS/VGA/DMI/DDR (2/6)
Size A3
Document Number
Siberia
Rev SC
Date: Friday, May 25, 2007
Sheet 8 of 50



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Title	GMCH-DDR (3/6)
Size: A3	Document Number: Siberia
Rev: SC	
Date: Friday, May 25, 2007	Sheet 9 of 50

Supply	Signal Group	Icc-max	
+1.05V_VCCP	VCC	1.31A	
+1.05V_VCCP	VCC_NCTF	A	
+1.05V_VCCP	VTT	0.85A	
+1.05V_VCCP	VCC_PEG	1.2A	
+1.05V_VCCP	VCC_RXR_DMI	0.25A	
+1.05V_VCCP	VCC_ATX	84.15mA	(Non-AMT)
+1.8V_SUS	VCC_SM	2.4A	
+1.8V_SUS	VCC_SM_CK	0.2A	
+1.25V_RUN	VCCA_HPLL	0.05A	
+1.25V_RUN	VCCA_MPLL	0.15A	
+1.25V_RUN	VCCA_SM	0.735A	(667MHz)
+1.25V_RUN	VCCA_SM_NCTF	A	
+1.25V_RUN	VCCA_SM_CK	0.015A	(667MHz)
+1.25V_RUN	VCCD_HPLL	0.25A	
+1.25V_RUN	VCCA_AXD	0.2A	
+1.25V_RUN	VCCA_AXD_NCTF	A	
+1.25V_RUN	VCCA_PEG_PLL /VCCD_PEG_PLL	0.1A	
+1.25V_RUN	VCCA_AXF	0.35A	
+1.25V_RUN	VCCA_DMI	0.1A	
+1.5V_RUN	VCCD_TVDAC	0.06A	
+3.3V_RUN	VCCA_PEG_BG	0.005A	
+3.3V_RUN	VCC_HV	0.1A	

FOR VCC CORE AND VCC NCTF

FOR VCC AXM NCTF AND VCC AXM

FOR VCC SM

Place CAP where LVDS and DDR2 taps

308 mils from the Edge

Coupling CAP

Place on the Edge

Coupling CAP Inside MCH cavity

Place on the Edge

For NCTF

CRESTLINE-GP-U-NF

CRESTLINE-GP-U-NF

Wistron Corporation
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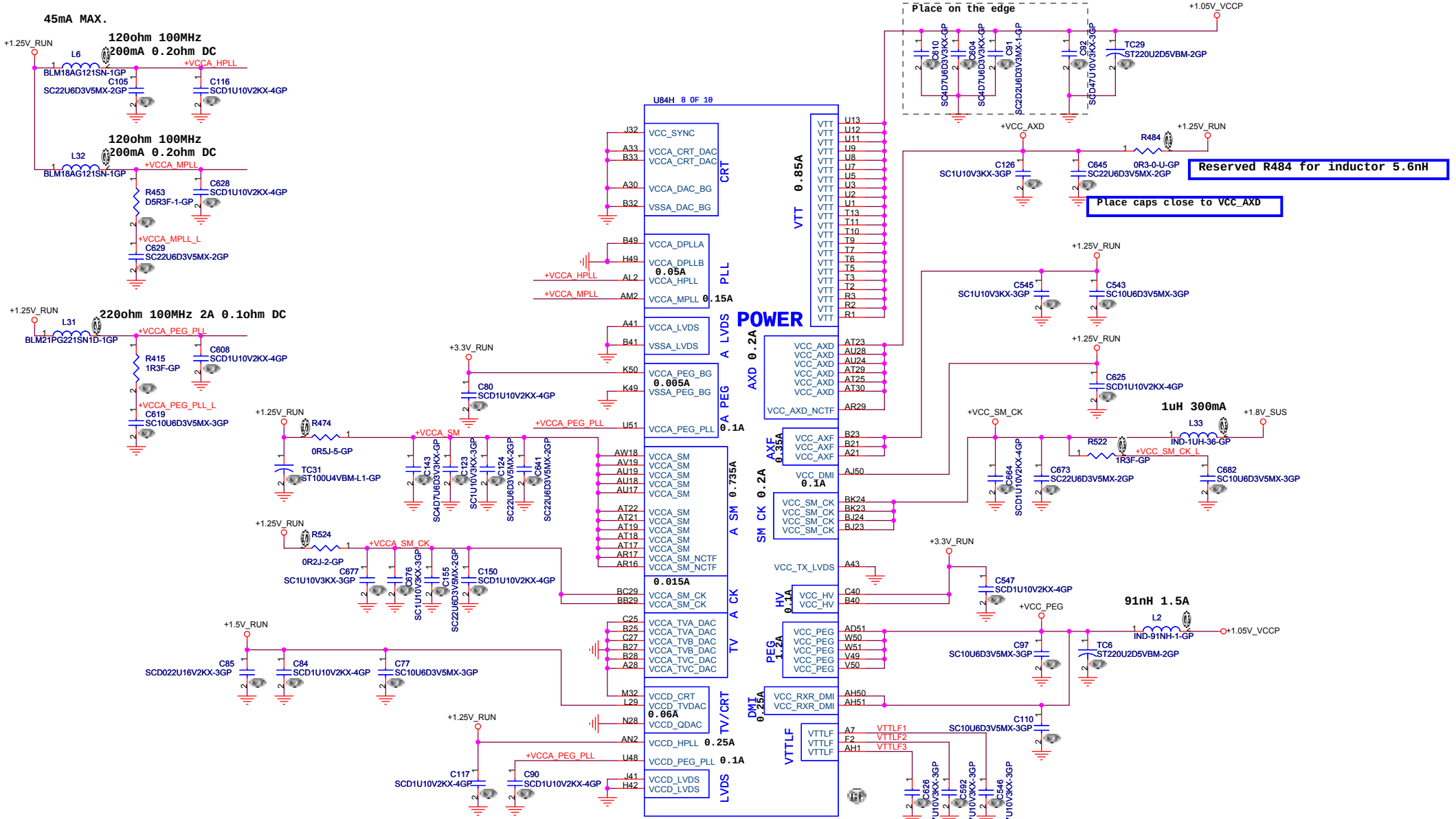
Title: GMCH-POWER (4/6)

Size: A3 | Document Number: Siberia | Rev: SC

Date: Friday, May 25, 2007 | Sheet 10 of 50



Wistron Corporation		
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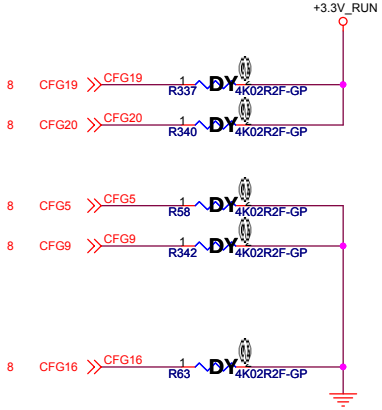
Title	GMCH-POWER/FILTERR (5/6)	
Size: A3	Document Number: Siberia	Rev: SC
Date: Friday, May 25, 2007	Sheet 11 of 50	

Layout Note:
Location of all MCH CFG strap resistors need to be close to trace to minimize stub



CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	★ DMI X 4
CFG 9 PCI Express Graphics Lane Reversal	Lane Reversal	★ Normal Mode(Lanes number in order)
CFG 16 FSB Dynamic ODT	Disabled	★ Enabled
CFG 18 VCC select	★ 1.05V	1.5V
CFG 19 DMI Lane Reversed	★ Normal Operation	Reserved Lane
CFG 20 Concurrent SDVO/PCIE	★ Only PCIE or SDVO is operation	PCIE and SDVO are operation simultaneous

CFG 12 CFG 13	XOR/ALL-Z
LL(00)	Reserved
LH(01)	XOR Mode Enabled
HL(10)	All Z Mode Enabled
HH(11)	Normal Operation ★

9 OF 10
U84I

VSS

A13 A15 A17 A24 AA21 AA24 AA29 AB20 AB23 AB26 AB28 AB31 AC10 AC13 AC3 AC39 AC43 AC47 AD1 AD21 AD26 AD29 AD3 AD41 AD45 AD49 AD5 AD50 AD8 AE10 AE14 AE6 AF20 AF23 AF24 AF31 AG2 AG38 AG43 AG47 AG50 AH3 AH40 AH41 AH7 AH9 AJ11 AJ13 AJ21 AJ24 AJ29 AJ32 AJ43 AJ45 AJ49 AK20 AK21 AK26 AK28 AK31 AK51 AL1 AM11 AM13 AM3 AM4 AM41 AM45 AN1 AN38 AN39 AN43 AN5 AN7 AP4 AP48 AP50 AR11 AR2 AR39 AR44 AR47 AR7 AT10 AT14 AT41 AT49 AU1 AU23 AU29 AU3 AU36 AU49 AU51 AV39 AV48 AW1 AW12 AW16

AW24 AW29 AW32 AW5 AW7 AY10 AY24 AY37 AY42 AY43 AY45 AY47 AY50 B10 B20 B24 B29 B30 B35 B38 B43 B46 B5 B8 BA1 BA17 BA18 BA2 BA24 BB12 BB25 BB40 BB44 BB49 BB8 BC16 BC24 BC25 BC36 BC40 BC51 BD13 BD2 BD28 BD45 BD48 BD5 BE1 BE19 BE23 BE30 BE42 BE51 BE8 BF12 BF16 BF36 BG19 BG2 BG24 BG29 BG39 BG48 BG5 BG51 BH17 BH30 BH44 BH46 BH8 BJ11 BJ13 BJ38 BJ4 BJ42 BJ46 BK15 BK17 BK25 BK29 BK36 BK40 BK44 BK6 BK8 BL11 BL13 BL19 BL22 BL37 BL47 C12 C16 C19 C28 C29 C33 C36 C41

10 OF 10
U84J

VSS

C46 C50 C7 D13 D24 D3 D32 D39 D45 D49 E10 E16 E24 E28 E32 E47 F19 F36 F4 F40 F50 G1 G13 G16 G19 G24 G28 G29 G33 G42 G45 G48 G8 H24 H28 H4 H45 J11 J16 J2 J24 J28 J33 J35 J39 K12 K47 K8 L1 L17 L20 L24 L28 L3 L33 L49 M28 M42 M46 M49 M5 M50 M9 N11 N14 N17 N29 N32 N36 N39 N44 N49 N7 P19 P2 P23 P3 P50 R49 T39 T43 T47 U41 U45 U50 V2 V3

W11 W39 W43 W47 W5 W7 Y13 Y2 Y41 Y45 Y49 Y5 Y50 Y11 P29

T29 MCH_GND1 R71 1 0R2J-2-GP
T31 MCH_GND2 R70 1 0R2J-2-GP
T33 MCH_GND3 R69 1 0R2J-2-GP
R28 MCH_GND4 R66 1 0R2J-2-GP

AA32 AB32 AD32 AF28 AF29 AT27 AV25 H50

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *GMCH-GND (6/6)*

Size	Document Number	Rev
A3	Siberia	SC

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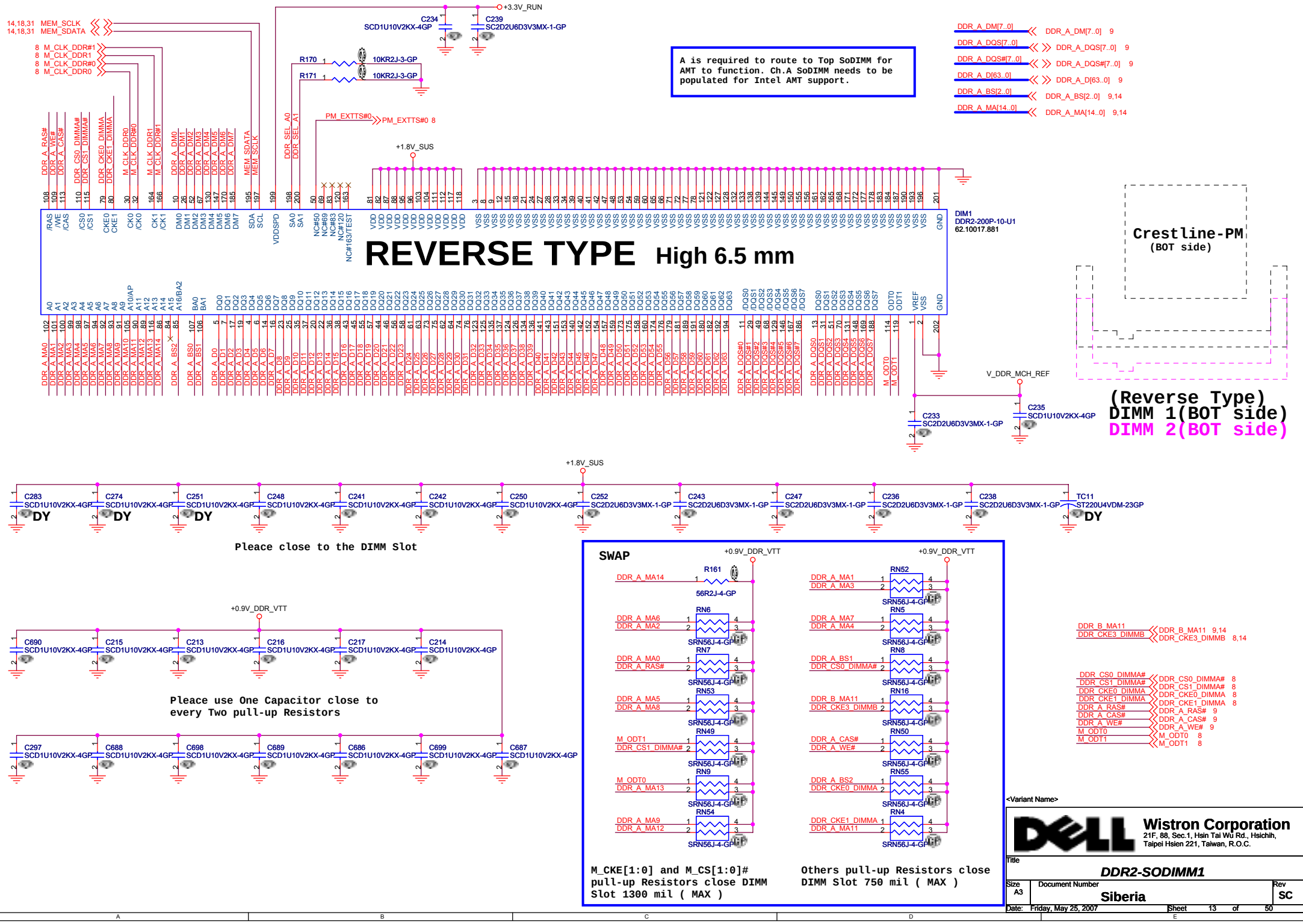

14,18,31 MEM_SCLK
14,18,31 MEM_SDATA
8 M_CLK_DDR#1
8 M_CLK_DDR1
8 M_CLK_DDR#0
8 M_CLK_DDR0
+3.3V_RUN
C234 SCD1U10V2KX-4GP
C239 SC2D2U6D3V3MX-1-GP
R170 10KR2J-3-GP
R171 10KR2J-3-GP
PM_EXTTS#0
PM_EXTTS#0 8
+1.8V_SUS
A is required to route to Top SoDIMM for AMT to function. Ch.A SoDIMM needs to be populated for Intel AMT support.
DDR_A_DM[7..0] DDR_A_DM[7..0] 9
DDR_A_DQS[7..0] DDR_A_DQS[7..0] 9
DDR_A_DQS#[7..0] DDR_A_DQS#[7..0] 9
DDR_A_D[63..0] DDR_A_D[63..0] 9
DDR_A_BS[2..0] DDR_A_BS[2..0] 9,14
DDR_A_MA[14..0] DDR_A_MA[14..0] 9,14
DIM1
DDR2-200P-10-U1
62.10017.881
REVERSE TYPE High 6.5 mm
Crestline-PM
(BOT side)
(Reverse Type)
DIMM 1(BOT side)
DIMM 2(BOT side)
V_DDR_MCH_REF
C233 SC2D2U6D3V3MX-1-GP
C235 SCD1U10V2KX-4GP
C283 SCD1U10V2KX-4GP DY
C274 SCD1U10V2KX-4GP DY
C251 SCD1U10V2KX-4GP DY
C248 SCD1U10V2KX-4GP
C241 SCD1U10V2KX-4GP
C242 SCD1U10V2KX-4GP
C250 SCD1U10V2KX-4GP
C252 SC2D2U6D3V3MX-1-GP
C243 SC2D2U6D3V3MX-1-GP
C247 SC2D2U6D3V3MX-1-GP
C236 SC2D2U6D3V3MX-1-GP
C238 SC2D2U6D3V3MX-1-GP
TC11 ST220U4VDM-23GP DY
Please close to the DIMM Slot
+0.9V_DDR_VTT
C690 C215 C213 C216 C217 C214 SCD1U10V2KX-4GP
Please use One Capacitor close to every Two pull-up Resistors
C297 C688 C698 C689 C686 C699 C687 SCD1U10V2KX-4GP
SWAP
R161 56R2J-4-GP
RN6 RN7 RN53 RN49 RN9 RN54 SRN56J-4-GP
RN52 RN5 RN8 RN16 RN50 RN55 RN4 SRN56J-4-GP
M_CKE[1:0] and M_CS[1:0]# pull-up Resistors close DIMM Slot 1300 mil (MAX)
Others pull-up Resistors close DIMM Slot 750 mil (MAX)
DDR_B_MA11 DDR_B_MA11 9,14
DDR_CKE3_DIMMB DDR_CKE3_DIMMB 8,14
DDR_CS0_DIMMA# DDR_CS0_DIMMA# 8
DDR_CS1_DIMMA# DDR_CS1_DIMMA# 8
DDR_CKE0_DIMMA DDR_CKE0_DIMMA 8
DDR_CKE1_DIMMA DDR_CKE1_DIMMA 8
DDR_A_RAS# DDR_A_RAS# 9
DDR_A_CAS# DDR_A_CAS# 9
DDR_A_WE# DDR_A_WE# 9
M_ODT0 M_ODT0 8
M_ODT1 M_ODT1 8
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDR2-SODIMM1
Size A3
Document Number
Siberia
Rev SC
Date: Friday, May 25, 2007
Sheet 13 of 50

M_CLK_DDR3 and M_CLK_DDR#3
can map to Row/Rank 2

13,18,31 MEM_SCLK
13,18,31 MEM_SDATA
8 M_CLK_DDR#3
8 M_CLK_DDR3
8 M_CLK_DDR#2
8 M_CLK_DDR2

R612 10KR2J-3-GP
R611 10KR2J-3-GP
C266 SCD1U10V2KX-4GP
C263 SC2D2U6D3V3MX-1-GP
+3.3V_RUN
PM_EXTTS#1
PM_EXTTS#1 8
+1.8V_SUS

DDR_B_DM[7..0] DDR_B_DM[7..0] 9
DDR_B_DQS[7..0] DDR_B_DQS[7..0] 9
DDR_B_DQS#[7..0] DDR_B_DQS#[7..0] 9
DDR_B_D[63..0] DDR_B_D[63..0] 9
DDR_B_BS[2..0] DDR_B_BS[2..0] 9
DDR_B_MA[14..0] DDR_B_MA[14..0] 9,13

DIM2
DDR2-200P-33-GP
62.10017.D41

REVERSE TYPE High 11mm

V_DDR_MCH_REF
C270 SC2D2U6D3V3MX-1-GP
C269 SCD1U10V2KX-4GP

+1.8V_SUS
C249 SCD1U10V2KX-4GP DY
C237 SCD1U10V2KX-4GP DY
C748 SCD1U10V2KX-4GP DY
C276 SCD1U10V2KX-4GP
C275 SCD1U10V2KX-4GP
C277 SCD1U10V2KX-4GP
C285 SCD1U10V2KX-4GP
C284 SC2D2U6D3V3MX-1-GP
C278 SC2D2U6D3V3MX-1-GP
C747 SC2D2U6D3V3MX-1-GP
C280 SC2D2U6D3V3MX-1-GP
C749 SC2D2U6D3V3MX-1-GP
TC12 ST220U4VDM-23GP DY

Please close to the DIMM Slot

+0.9V_DDR_VTT
C315 SCD1U10V2KX-4GP
C312 SCD1U10V2KX-4GP
C311 SCD1U10V2KX-4GP
C310 SCD1U10V2KX-4GP
C313 SCD1U10V2KX-4GP
C298 SCD1U10V2KX-4GP

Please use One Capacitor close to
every Two pull-up Resistors

C309 SCD1U10V2KX-4GP
C255 SCD1U10V2KX-4GP
C256 SCD1U10V2KX-4GP
C253 SCD1U10V2KX-4GP
C254 SCD1U10V2KX-4GP
C268 SCD1U10V2KX-4GP
C264 SCD1U10V2KX-4GP

SWAP

+0.9V_DDR_VTT
R186 56R2J-4-GP
DDR_B_MA14
RN13 SRN56J-4-GP
DDR_B_MA3
DDR_B_MA1
RN22 SRN56J-4-GP
M_ODT3
DDR_B_MA13
RN10 SRN56J-4-GP
DDR_CKE2_DIMMB
DDR_B_BS2
RN12 SRN56J-4-GP
DDR_B_MA8
DDR_B_MA5
RN21 SRN56J-4-GP
M_ODT2
DDR_CS2_DIMMB#
RN19 SRN56J-4-GP
DDR_B_BS1
DDR_B_MA0

+0.9V_DDR_VTT
RN51 SRN56J-4-GP
DDR_A_BS0
DDR_A_MA10
RN11 SRN56J-4-GP
DDR_B_MA12
DDR_B_MA9
RN18 SRN56J-4-GP
DDR_B_MA4
DDR_B_MA2
RN17 SRN56J-4-GP
DDR_B_MA7
DDR_B_MA6
RN15 SRN56J-4-GP
DDR_B_CAS#
DDR_CS3_DIMMB#
RN14 SRN56J-4-GP
DDR_B_MA10
DDR_B_BS0
RN20 SRN56J-4-GP
DDR_B_RAS#
DDR_B_WE#

M_CKE[3:2] and M_CS[3:2]#
pull-up Resistors close DIMM
Slot 1300 mil (MAX)

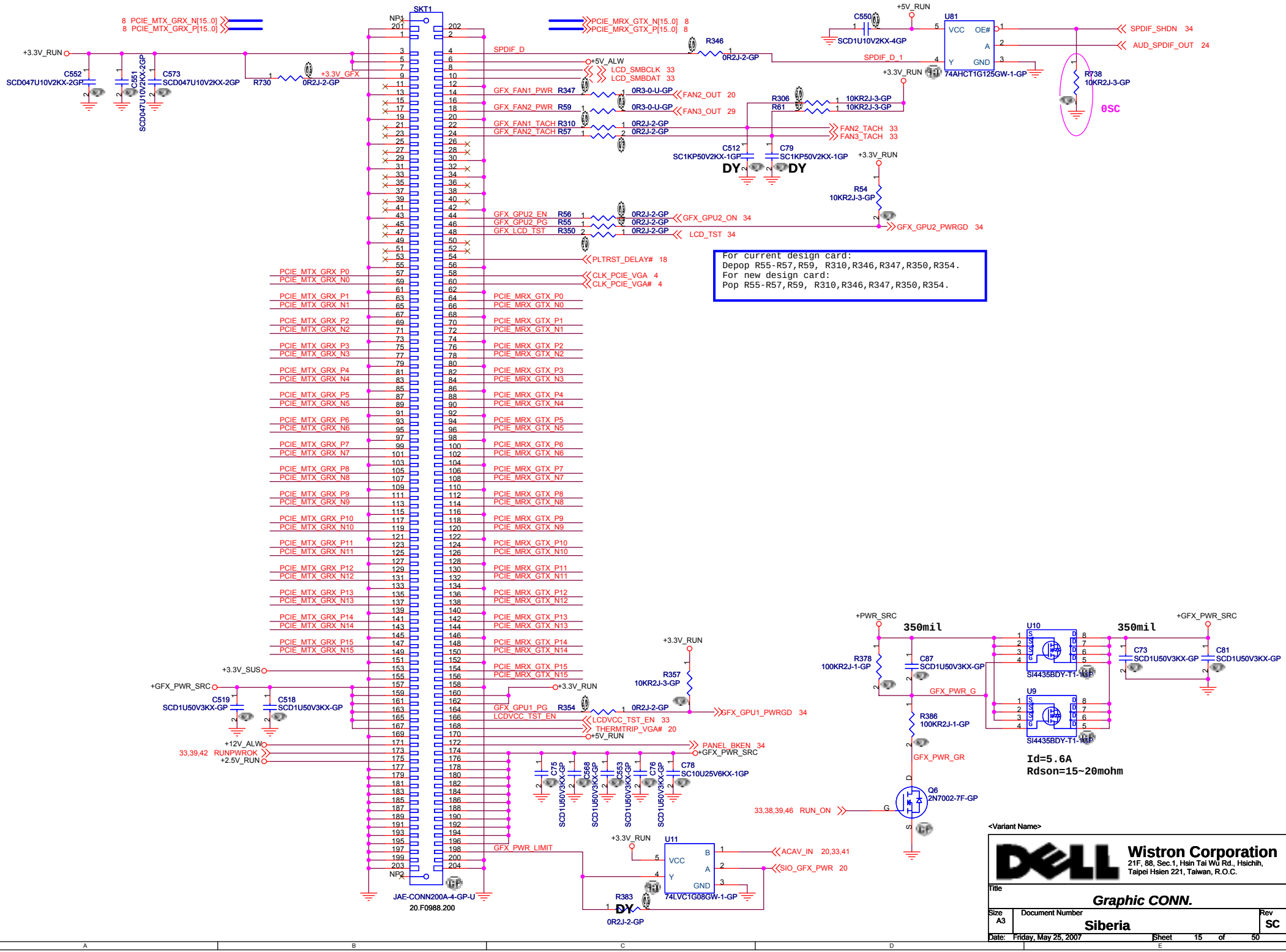
Others pull-up Resistors close
DIMM Slot 750 mil (MAX)

DDR_A_BS0 DDR_A_BS0 9,13
DDR_A_MA10 DDR_A_MA10 9,13

DDR_CS2_DIMMB# DDR_CS2_DIMMB# 8
DDR_CS3_DIMMB# DDR_CS3_DIMMB# 8
DDR_CKE2_DIMMB DDR_CKE2_DIMMB 8
DDR_CKE3_DIMMB DDR_CKE3_DIMMB 8,13
DDR_B_RAS# DDR_B_RAS# 9
DDR_B_CAS# DDR_B_CAS# 9
DDR_B_WE# DDR_B_WE# 9
M_ODT2 M_ODT2 8
M_ODT3 M_ODT3 8

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR2-SODIMM2
Size: A3
Document Number: Siberia
Rev: SC
Date: Friday, May 25, 2007
Sheet 14 of 50



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Graphic CONN.***

Size	Document Number	Rev
A3	**Siberia**	SC

Date: Friday, May 25, 2007 Sheet 15 of 50

RTC circuitry

Place all series terms close to ICH8 except for SDIN input lines, which shoud be close to source.

GLAN_COMP place within 500 mil of ICH8M

56 ohm must be place within 2"of stub

This circuit is only needed if the platform has the SNIFFER

Distance between the ICH8-M and cap on the "P" signal should be identical distance between the ICH8-M and cap on the "N" signal for same pair.

SM_SATASB Place within 500 mil of ICH8-M

ICH8-Strap PIN

No_Reboot_Strap

SPKR	LOW = Defaule High=No Reboot

XOR Chain Entrance Strap

ICH_RSVD	ACZ_DOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation(default)
1	1	Set PCIE port cofig bit1

integrated VccSus1_05,VccSus1_5,VccCL1_5		
ICH_INTVRMEN	High=Enable	Low=Disable
integrated VccLan1_05VccCL1_05		
ICH_LAN100_SLP	High=Enable	Low=Disable

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH8M-RTC/IDE/LPC/DHI (1/4)

Size	Document Number	Rev
A3	Siberia	SC

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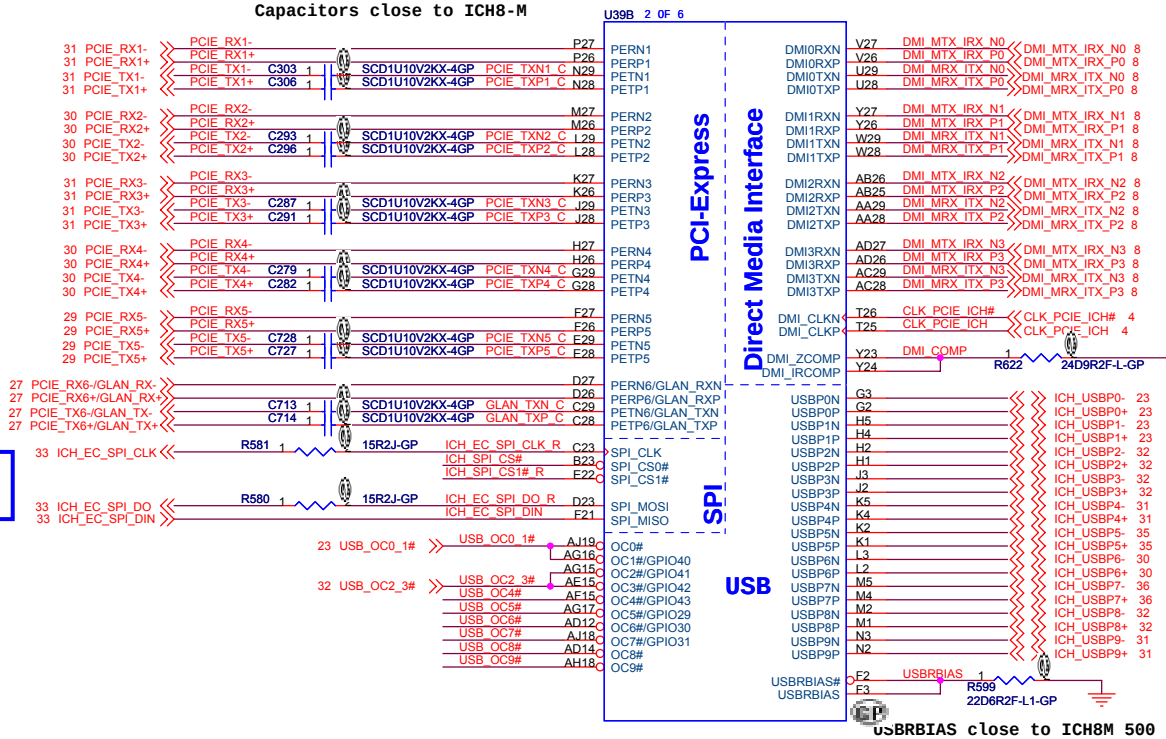
PCIE Interface Routing

LANE1	MiniCard WWAN
LANE2	MiniCard WLAN
LANE3	MiniCard WPAN
LANE4	Express Card
LANE5	PPU Card
LANE6	Giba Bit LOM

PCIE TX dc blocking
Capacitors close to ICH8-M



DMI_COMP R622 place within 500 mil of ICH8M

USBRBIAS close to ICH8M 500 mils and Trace impedance should be 60 ohm +/- 15%

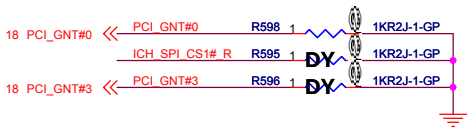
Layout Note:
Place R563, R580 and R581 within 500 mils from ICH.

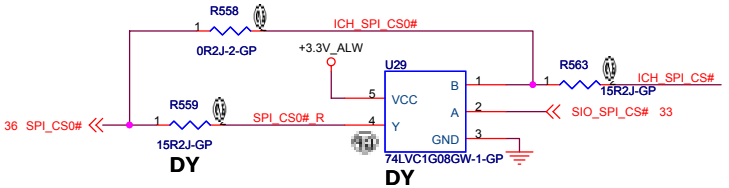
ICH

USB0	Ext Left Side
USB1	Ext Back
USB2	Ext Right Side (Top)
USB3	Ext Right Side (Bottom)
USB4	3rd mini card
USB5	Camera
USB6	Express Card
USB7	BT
USB8	Gaming LCD
USB9	WWAN

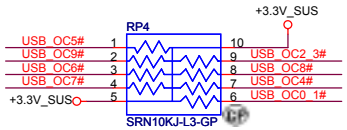
ICH8-Strap PIN

BOOT BIOS Strap		
PCI_GNT#0 (R617)	SPI_CS#1 (R623)	BOOT BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC
A16 swap override strap		
PCI_GNT#3 (R620)	low = A16 swap override enable high = default	





USB OC# PULL HIGH



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Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH8M-PCIE/USB/SPI/DMI (2/4)

Size	Document Number	Rev
A3	Siberia	SC

Date: Friday, May 25, 2007 Sheet 17 of 50

PCI Interface Routing

	IDSEL	INT	REQ	GNT
1394/ MediaCard	AD17	C D	1	1

Add Buffers as need for Loading and Fanout concerns

Option to "Disable" clkrun. Pulling it down will keep the clks running.

Layout Note:
CL_VREF[1:0] ~= 0.405V
Width/Spacing = 12/12

SMBus address D2
FOR DDR2
These are for backdrive issue.

PCI I/F PULL HIGH

CLK_ICHPCI ,CLK_ICH_48M and CLK_ICH_14M EMI Mode
Place close to ICH8-M

EMI

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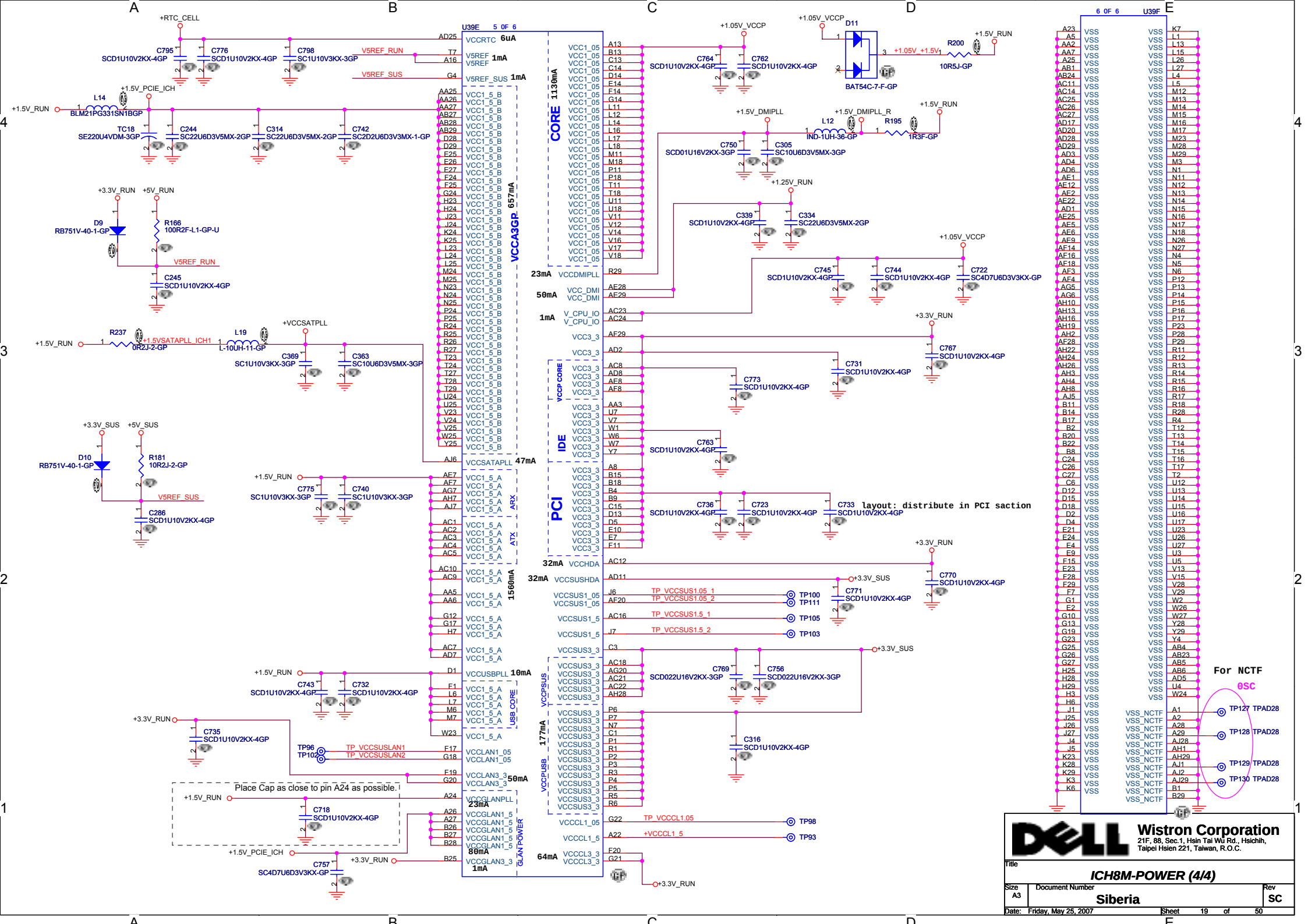
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH8M-PCI/CL/PM/GPIO (3/4)

Size	Document Number	Rev
A3	Siberia	SC

Date: Friday, May 25, 2007 Sheet 18 of 50


U39E 5 OF 6
U39F 6 OF 6
VCCRTC 6uA
V5REF 1mA
V5REF_SUS 1mA
VCCSATAPLL 47mA
VCCUSBPLL 10mA
VCCGLANPLL 23mA
VCCGLAN3_3 1mA
VCCDMIPLL 23mA
VCC_DMI 50mA
V_CPU_IO 1mA
VCCHDA 32mA
VCCSUSHDA 32mA
VCCSUS3_3 177mA
VCCL1_05 64mA
VCCL3_3
VCC1_05 1130mA
VCC1_5_B VCCA3GP 657mA
VCC1_5_A 1560mA
VCCLAN1_05
VCCLAN3_3 50mA
VCCGLAN1_5 80mA
CORE
VCCP CORE
IDE
PCI
ARX
ATX
USB CORE
VCCPSUS
VCCPUSB
GLAN POWER
+RTC_CELL
+1.5V_PCIE_ICH
+1.5V_RUN
+3.3V_RUN
+5V_RUN
+3.3V_SUS
+5V_SUS
+VCCSATAPLL
+1.05V_VCCP
+1.25V_RUN
+1.5V_DMIPLL
+1.5V_DMIPLL_R
+1.05V_+1.5V
V5REF_RUN
V5REF_SUS
+1.5VSATAPLL_ICH1
TP_VCCSUSLAN1
TP_VCCSUSLAN2
TP_VCCSUS1.05_1
TP_VCCSUS1.05_2
TP_VCCSUS1.5_1
TP_VCCSUS1.5_2
TP_VCCCL1.05
+VCCCL1_5
layout: distribute in PCI saction
Place Cap as close to pin A24 as possible.
For NCTF
0SC
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH8M-POWER (4/4)
Size A3
Document Number
Siberia
Rev SC
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Sheet 19 of 50

SSID = THERMAL

REM_DIODE1_N and REM_DIODE1_P routing Trace width and Spacing use 10 / 10 mil

Place inside CPU socket

Locate C586 near Guardian

H_THERMDA and H_THERMDC routing Trace width and Spacing use 10 / 10 mil

Place near the bottom SODIMM CONN

should be placed Bot Side under mini Card

should be placed TOP Side under WLAN

should be placed TOP Side below ICH

Note :

VSET = (Tp - 70) / 21

3.3 * (R411/ R406 + R411) = (Tp - 70) / 21

Where Tp = 70 to 101 degrees C

Tp set at 88 degrees C

Guardian temp tolerance = +/- 3 degrees C

1st GPU FAN

CPU FAN

pull up on EC

<Variant Name>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

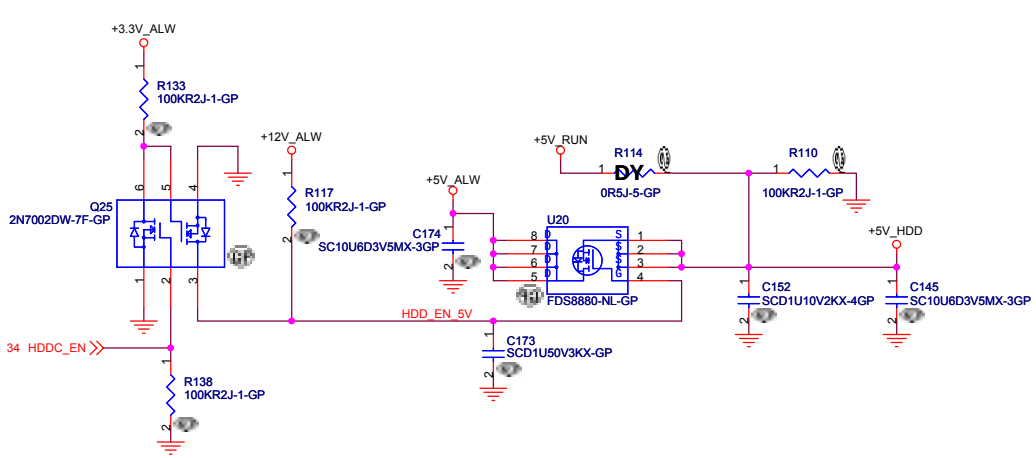
Title: FAN, EMC4001

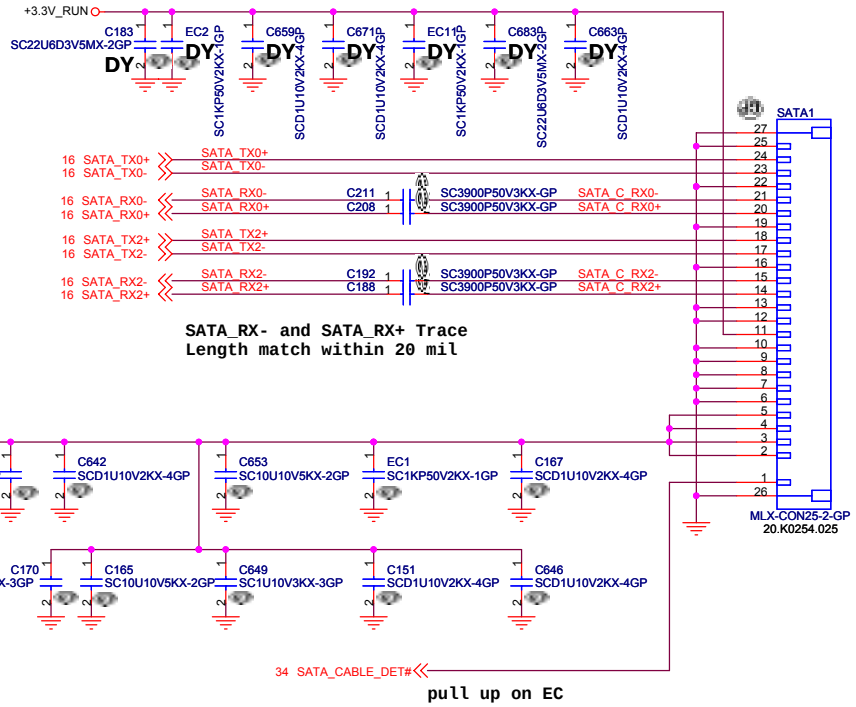
Size: A3 | Document Number: Siberia | Rev: SC

Date: Friday, May 25, 2007 | Sheet 20 of 50

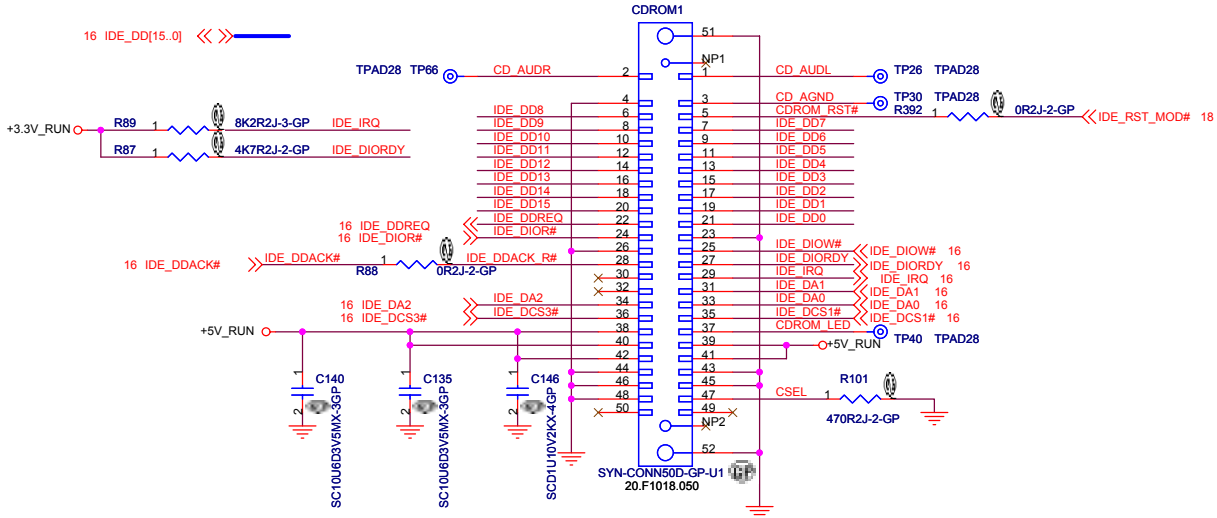
SSID = IDE & SATA

SATA HDD Connector





ODD Connector



<Variant Name>

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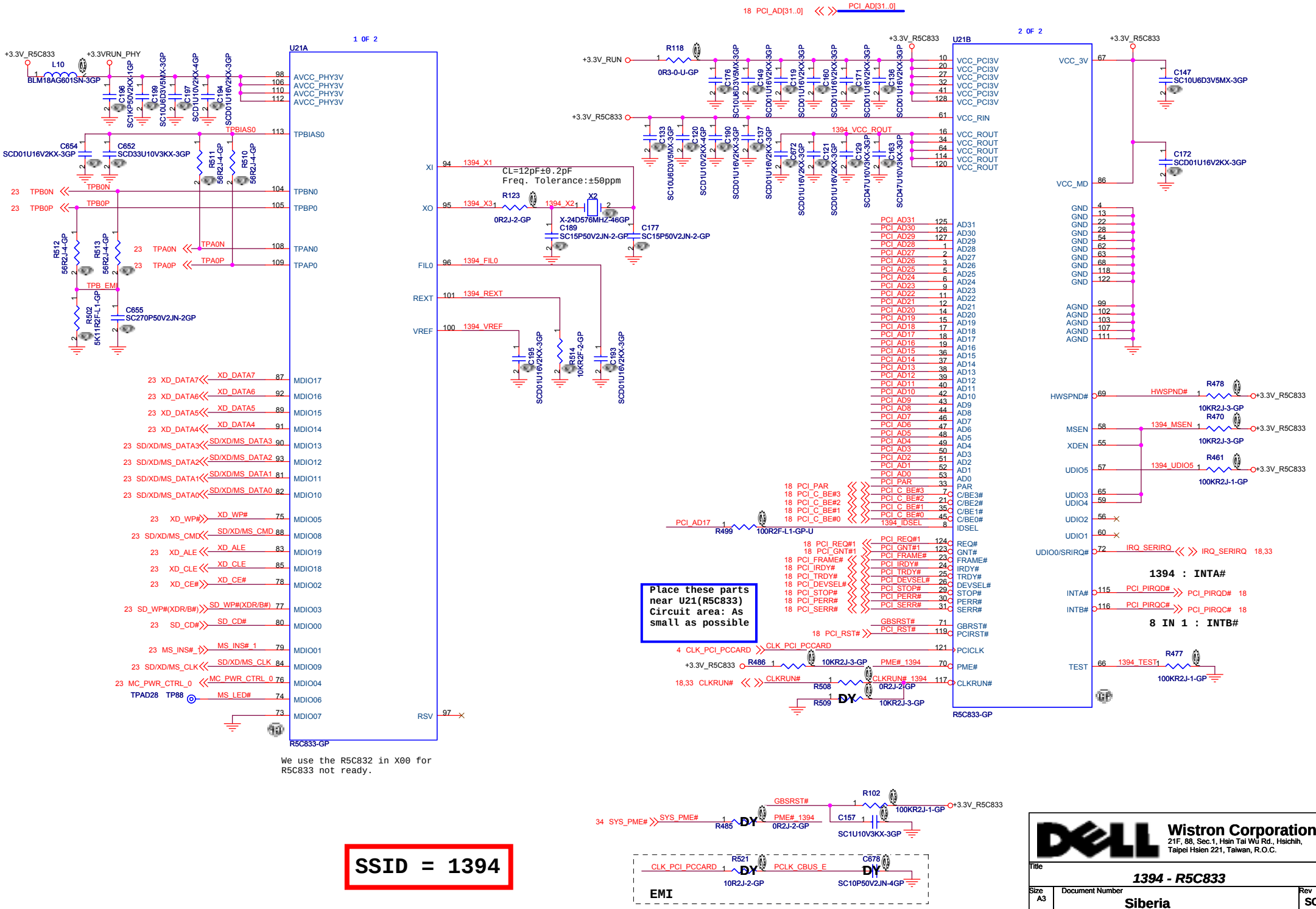
Title: ***HDD&ODD***

Size	Document Number	Rev
A3	Siberia	SC

Date: Friday, May 25, 2007 Sheet 21 of 50


U21A
1 OF 2
R5C833-GP
U21B
2 OF 2
R5C833-GP
+3.3V_R5C833
+3.3VRUN_PHY
+3.3V_RUN
L10
BLM18AG601SN-3GP
TPBIAS0
TPB0N
TPB0P
TPA0N
TPA0P
TPB_EMI
C654
SCD01U16V2KX-3GP
C652
SCD33U10V3KX-3GP
C655
SC270P50V2JN-2GP
R511
56R2J-4-GP
R510
56R2J-4-GP
R512
56R2J-4-GP
R513
56R2J-4-GP
R502
5K11R2F-L1-GP
XI
XO
FIL0
REXT
VREF
RSV
1394_X1
1394_X2
1394_FIL0
1394_REXT
1394_VREF
CL=12pF±0.2pF
Freq. Tolerance:±50ppm
R123
0R2J-2-GP
X2
X-24D576MHZ-46GP
C189
SC15P50V2JN-2-GP
C177
SC15P50V2JN-2-GP
C195
SCD01U16V2KX-3GP
R514
10KR2F-2-GP
C193
SCD01U16V2KX-3GP
R118
0R3-0-U-GP
1394_VCC_ROUT
VCC_PCI3V
VCC_RIN
VCC_ROUT
VCC_3V
VCC_MD
GND
AGND
HWSPND#
MSEN
XDEN
UDIO5
UDIO3
UDIO4
UDIO2
UDIO1
UDIO0/SRIRQ#
INTA#
INTB#
TEST
R478
10KR2J-3-GP
R470
10KR2J-3-GP
R461
100KR2J-1-GP
R477
100KR2J-1-GP
1394_MSEN
1394_UDIO5
1394_TEST
IRQ_SERIRQ
1394 : INTA#
8 IN 1 : INTB#
PCI_AD[31..0]
AD31
AD30
AD29
AD28
AD27
AD26
AD25
AD24
AD23
AD22
AD21
AD20
AD19
AD18
AD17
AD16
AD15
AD14
AD13
AD12
AD11
AD10
AD9
AD8
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
PAR
C/BE3#
C/BE2#
C/BE1#
C/BE0#
IDSEL
REQ#
GNT#
FRAME#
IRDY#
TRDY#
DEVSEL#
STOP#
PERR#
SERR#
GBSRST#
PCIRST#
PCICLK
PME#
CLKRUN#
PCI_PAR
PCI_C_BE#3
PCI_C_BE#2
PCI_C_BE#1
PCI_C_BE#0
PCI_IDSEL
PCI_REQ#1
PCI_GNT#1
PCI_FRAME#
PCI_IRDY#
PCI_TRDY#
PCI_DEVSEL#
PCI_STOP#
PCI_PERR#
PCI_SERR#
PCI_RST#
CLK_PCI_PCCARD
PME# 1394
CLKRUN# 1394
PCI_PIRQD#
PCI_PIRQC#
R499
100R2F-L1-GP-U
R486
10KR2J-3-GP
R508
0R2J-2-GP
R509
10KR2J-3-GP
DY
Place these parts near U21(R5C833) Circuit area: As small as possible
XD_DATA7
XD_DATA6
XD_DATA5
XD_DATA4
SD/XD/MS_DATA3
SD/XD/MS_DATA2
SD/XD/MS_DATA1
SD/XD/MS_DATA0
XD_WP#
SD/XD/MS_CMD
XD_ALE
XD_CLE
XD_CE#
SD_WP#(XDR/B#)
SD_CD#
MS_INS#_1
SD/XD/MS_CLK
MC_PWR_CTRL_0
MS_LED#
MDIO17
MDIO16
MDIO15
MDIO14
MDIO13
MDIO12
MDIO11
MDIO10
MDIO05
MDIO08
MDIO19
MDIO18
MDIO02
MDIO03
MDIO00
MDIO01
MDIO09
MDIO04
MDIO06
MDIO07
TPAD28
TP88
We use the R5C832 in X00 for R5C833 not ready.
SSID = 1394
SYS_PME#
GBSRST#
PME#_1394
R102
100KR2J-1-GP
R485
0R2J-2-GP
C157
SC1U10V3KX-3GP
CLK_PCI_PCCARD
PCLK_CBUS_E
R521
10R2J-2-GP
C678
SC10P50V2JN-4GP
EMI
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title
1394 - R5C833
Size A3
Document Number
Siberia
Rev SC
Date: Friday, May 25, 2007
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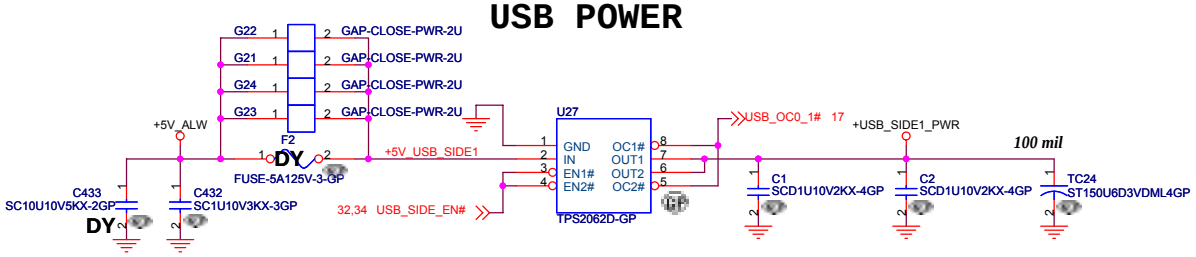
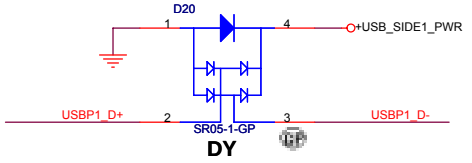
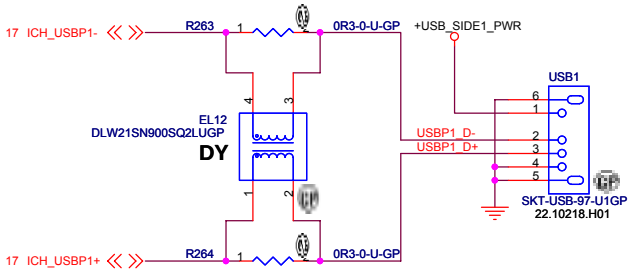
USB POWER



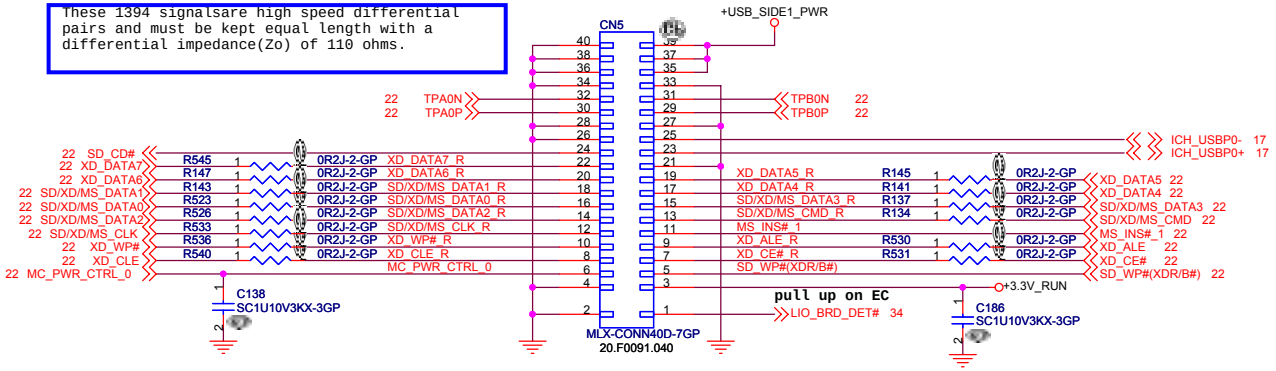


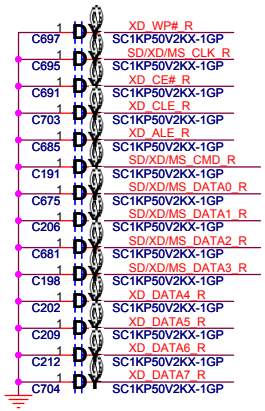
Place ESD diodes as close to the connector as passible.



I/O board conn. (1394/7 IN 1/USB)

These 1394 signalsare high speed differential pairs and must be kept equal length with a differential impedance(Zo) of 110 ohms.





<Variant Name>

Wistron Corporation
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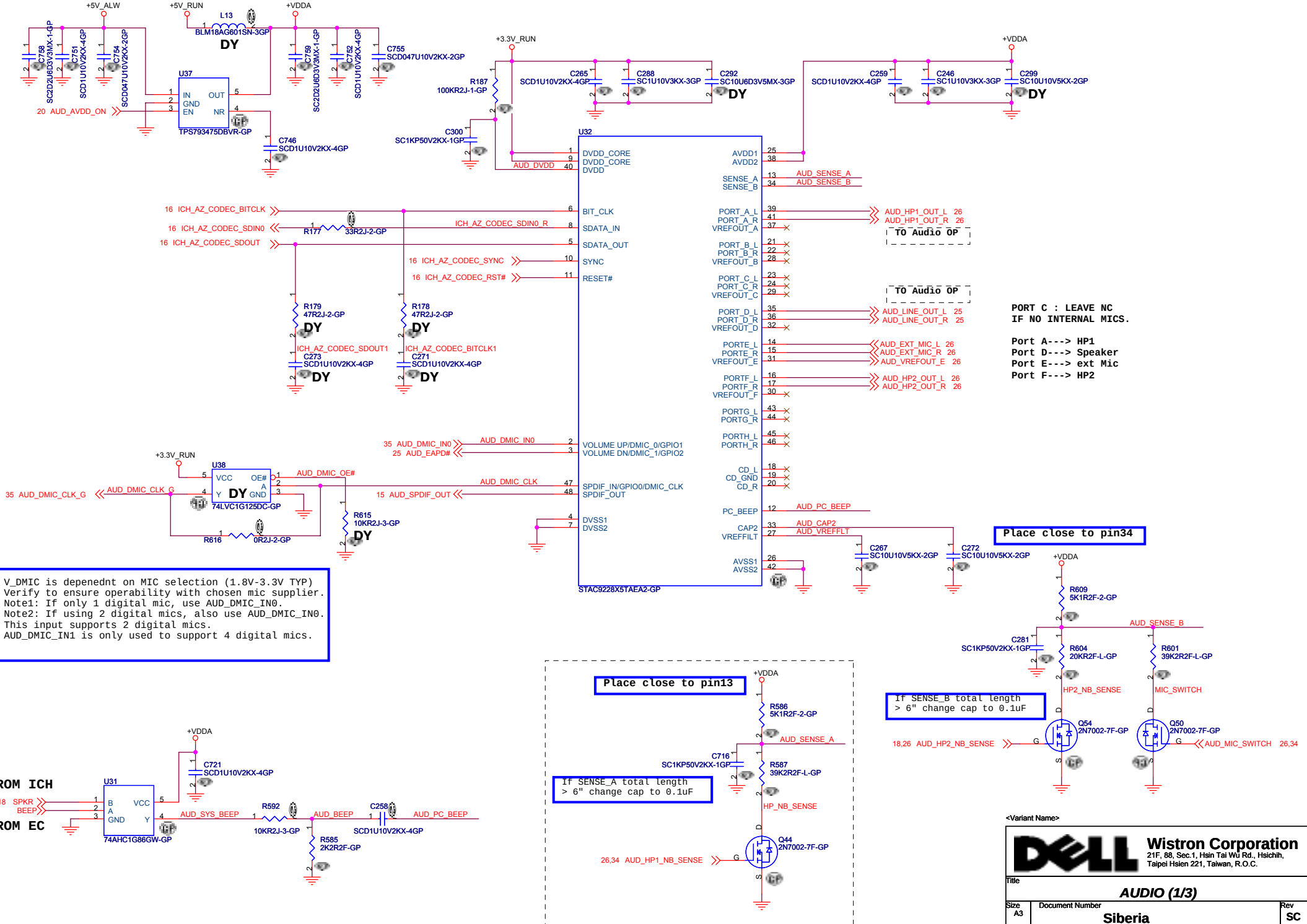
Title	I/O board (1394/7 IN 1/USB) / USB CONN.	
Size A3	Document Number Siberia	Rev SC
Date: Friday, May 25, 2007	Sheet 23 of 50	


+5V_ALW
+5V_RUN
+VDDA
+3.3V_RUN
L13
BLM18AG601SN-3GP
DY
U37
IN
GND
EN
OUT
NR
TPS793475DBVR-GP
20 AUD_AVDD_ON
C746
SCD1U10V2KX-4GP
U32
DVDD_CORE
DVDD_CORE
DVDD
AUD_DVDD
AVDD1
AVDD2
SENSE_A
SENSE_B
AUD_SENSE_A
AUD_SENSE_B
16 ICH_AZ_CODEC_BITCLK
16 ICH_AZ_CODEC_SDIN0
16 ICH_AZ_CODEC_SDOUT
ICH_AZ_CODEC_SDIN0_R
R177
33R2J-2-GP
BIT_CLK
SDATA_IN
SDATA_OUT
16 ICH_AZ_CODEC_SYNC
16 ICH_AZ_CODEC_RST#
SYNC
RESET#
R179
47R2J-2-GP
R178
47R2J-2-GP
ICH_AZ_CODEC_SDOUT1
ICH_AZ_CODEC_BITCLK1
C273
C271
SCD1U10V2KX-4GP
PORT_A_L
PORT_A_R
VREFOUT_A
AUD_HP1_OUT_L 26
AUD_HP1_OUT_R 26
TO Audio OP
PORT_B_L
PORT_B_R
VREFOUT_B
PORT_C_L
PORT_C_R
VREFOUT_C
PORT_D_L
PORT_D_R
VREFOUT_D
AUD_LINE_OUT_L 25
AUD_LINE_OUT_R 25
PORTE_L
PORTE_R
VREFOUT_E
AUD_EXT_MIC_L 26
AUD_EXT_MIC_R 26
AUD_VREFOUT_E 26
PORTF_L
PORTF_R
VREFOUT_F
AUD_HP2_OUT_L 26
AUD_HP2_OUT_R 26
PORTG_L
PORTG_R
PORTH_L
PORTH_R
35 AUD_DMIC_IN0
25 AUD_EAPD#
AUD_DMIC_IN0
VOLUME UP/DMIC_0/GPIO1
VOLUME DN/DMIC_1/GPIO2
CD_L
CD_GND
CD_R
AUD_DMIC_OE#
AUD_DMIC_CLK
SPDIF_IN/GPIO0/DMIC_CLK
SPDIF_OUT
15 AUD_SPDIF_OUT
35 AUD_DMIC_CLK_G
AUD_DMIC_CLK_G
U38
VCC
OE#
Y
GND
74LVC1G125DC-GP
R615
10KR2J-3-GP
R616
0R2J-2-GP
DVSS1
DVSS2
PC_BEEP
AUD_PC_BEEP
CAP2
VREFFILT
AUD_CAP2
AUD_VREFFLT
AVSS1
AVSS2
STAC9228X5TAEA2-GP
C267
SC10U10V5KX-2GP
C272
SC10U10V5KX-2GP
Place close to pin34
R609
5K1R2F-2-GP
C281
SC1KP50V2KX-1GP
R604
20KR2F-L-GP
R601
39K2R2F-L-GP
HP2_NB_SENSE
MIC_SWITCH
If SENSE_B total length
> 6" change cap to 0.1uF
Q54
2N7002-7F-GP
Q50
2N7002-7F-GP
18,26 AUD_HP2_NB_SENSE
AUD_MIC_SWITCH 26,34
PORT C : LEAVE NC
IF NO INTERNAL MICS.
Port A---> HP1
Port D---> Speaker
Port E---> ext Mic
Port F---> HP2
V_DMIC is depenednt on MIC selection (1.8V-3.3V TYP)
Verify to ensure operability with chosen mic supplier.
Note1: If only 1 digital mic, use AUD_DMIC_IN0.
Note2: If using 2 digital mics, also use AUD_DMIC_IN0.
This input supports 2 digital mics.
AUD_DMIC_IN1 is only used to support 4 digital mics.
Place close to pin13
R586
5K1R2F-2-GP
C716
SC1KP50V2KX-1GP
R587
39K2R2F-L-GP
If SENSE_A total length
> 6" change cap to 0.1uF
HP_NB_SENSE
Q44
2N7002-7F-GP
26,34 AUD_HP1_NB_SENSE
FROM ICH
FROM EC
U31
B
A
GND
VCC
Y
74AHC1G86GW-GP
16,18 SPKR
33 BEEP
C721
SCD1U10V2KX-4GP
AUD_SYS_BEEP
R592
10KR2J-3-GP
AUD_BEEP
C258
SCD1U10V2KX-4GP
R585
2K2R2F-GP
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title
AUDIO (1/3)
Size
A3
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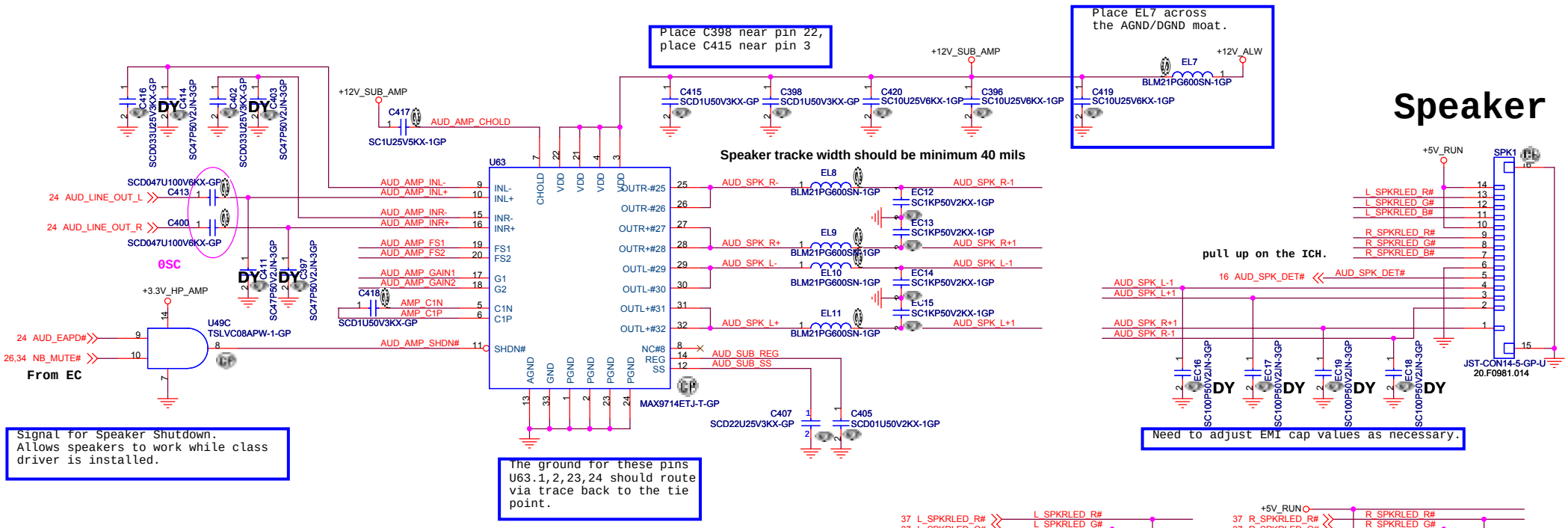
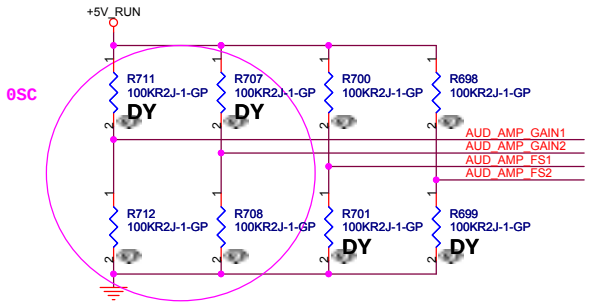
Speaker





Oscillator freuency selection

FS1	FS2	Freq KHz
0	0	335
0	1	460
1	0	236
1	1	335+/-7% (ss mode)

Voltage Gain selection

G1	G2	AV dB	Input Impedance
0	0	22.1dB	31K ohm
0	1	19.1dB	39K ohm
1	0	13dB	58K ohm
1	1	16dB	48K ohm

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO (2/3)

Size	Document Number	Rev
A3	Siberia	SC

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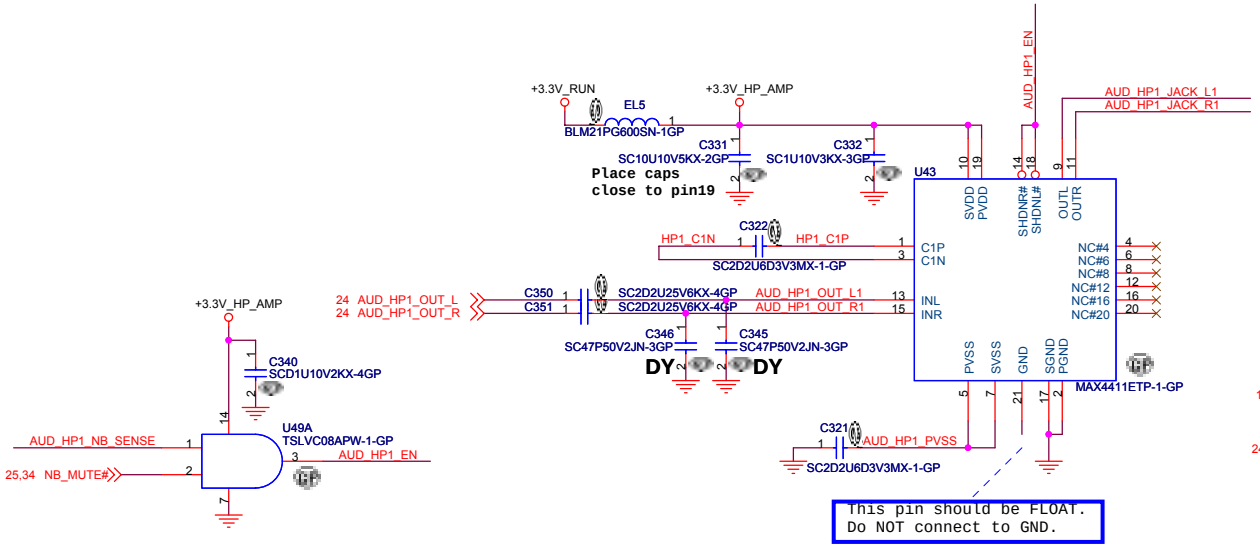
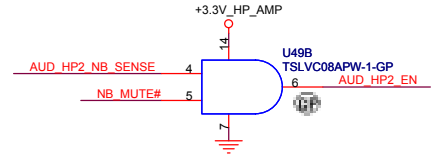
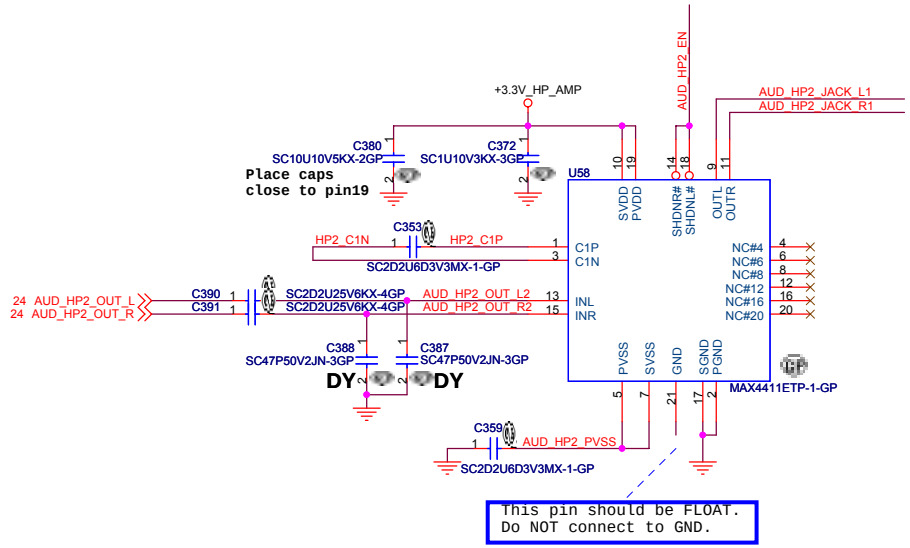
Head Phone 1

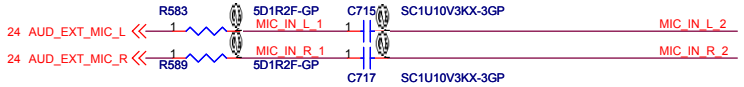


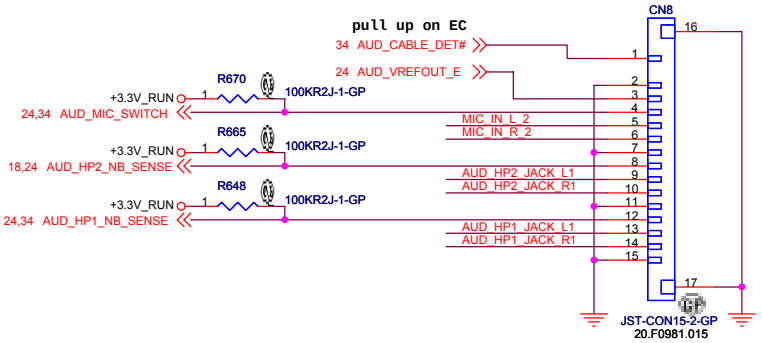


Head Phone 2



MIC





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO (3/3)

Size	Document Number	Rev
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Place filters close to the power pins - 0.1uF should be closest to the power pin. Minimize the loop path from pin to cap to power feed via. The length of the path from the ground side of the cap to the ground via should also be minimized.

Place filters close to the power pin should be closest to the power pin. Minimize the loop path from pin to cap to power feed via. The length of the path from the ground side of the cap to the ground via should also be minimized.

Place one cap close to each of the pins, 38, 45 and 52.

Place resister as close as possible to the ASIC. Pad is needed to measure 125MHz clock for debugging.

Important Layout Note for Dual footprint design:
Atmel part is available in standard package size, where as ST-Micro part is available in narrow package size. Ensure that pads are laid out for bath footprints.
Recommendation: Pads for pins 1 (reference) through 4 can be standard and identically located for both packages. Pads for pins 5-8 need to be larger to accommodate both packages.

rDS(ON) = 10mΩ@VGS = 10V, ID = 11.6A

	SO	SI	CS#	SCLK
Ato-Sense Mode	0	0	1	0
ST M45PE10	1	0	0	0
Atmel AT45DB011B	1	1	0	0

LOM_CABLE_DETECT goes to an input on a system microcontroller that can poll this signal periodically and can de-assert the LOM_LOM_PWR when LOM_CABLE_DETECT signal is high. Connect to an EC GPIO defined by th GPIO mapping.

Place crystal less than 0.75" (~1.9cm) from LAN Controller

CL=18pF±0.2pF
Freq. Tolerance:±30ppm

Layout Note:
PNP Q3 and Q64 needs 0.5 inch by 0.5 inch thermal relief pad.

REGSEN12 and REGSEN25 should be routed using a trace from the load (PNP) back to the controller. Do not use a direct connection to the power plane.

Use 8mils trace width for these signals

Logic High Voltage must be 0.7V to 2.75V

Place C447 as close to pin17 of LOM as possible.

Place C457 as close to pin13 of LOM as possible.

Place high-freqency decoupling cpas close to the power pin. Minimize the loop path from pin to cap to power feed via. The length of the path from the ground side ofthe cap to the ground via should also be minimized.

VDDIOPower Decoupling

VDDP Power Decoupling

Core Power Decoupling

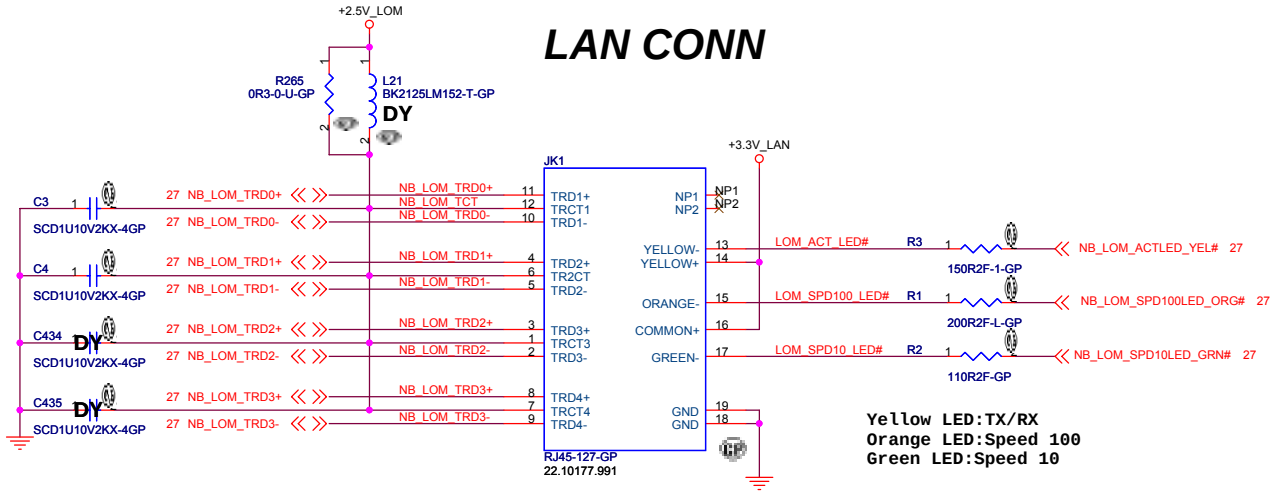
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN BCM5754M

Size: C | Document Number: Siberia | Rev: SC

Date: Friday, May 25, 2007 | Sheet 27 of 50

LAN CONN



Yellow LED:TX/RX
Orange LED:Speed 100
Green LED:Speed 10

1. Route as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. Pairs must be equal lengths.
5. 4mil trace width,7mil separation.
6. 30mil between pairs and any other trace.
7. Must not cross ground moat,except RJ-45 moat.

The blowout from the LAN magnetics to the RJ45 connector maintining the distance between the two to be within 1 inch.

<Variant Name>

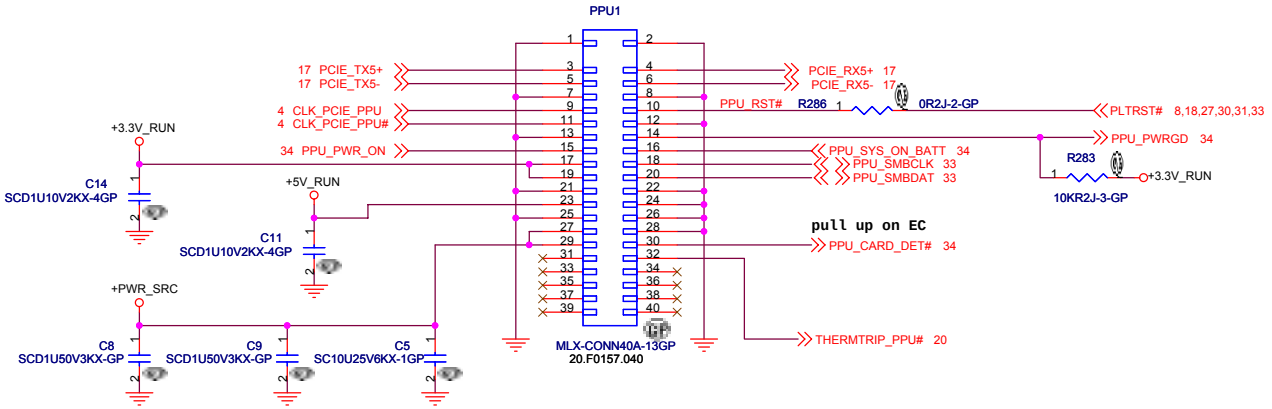
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LAN Connector***

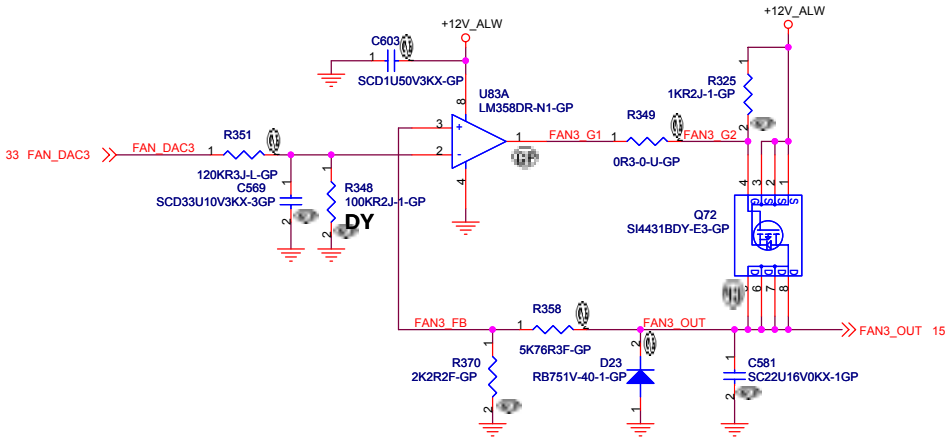
Size	Document Number	Rev
A3	Siberia	SC

Date: Friday, May 25, 2007 Sheet 28 of 50

PPU connector



2nd GPU FAN



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PPU CONN. / 2rd GPU FAN***

Size	Document Number	Rev
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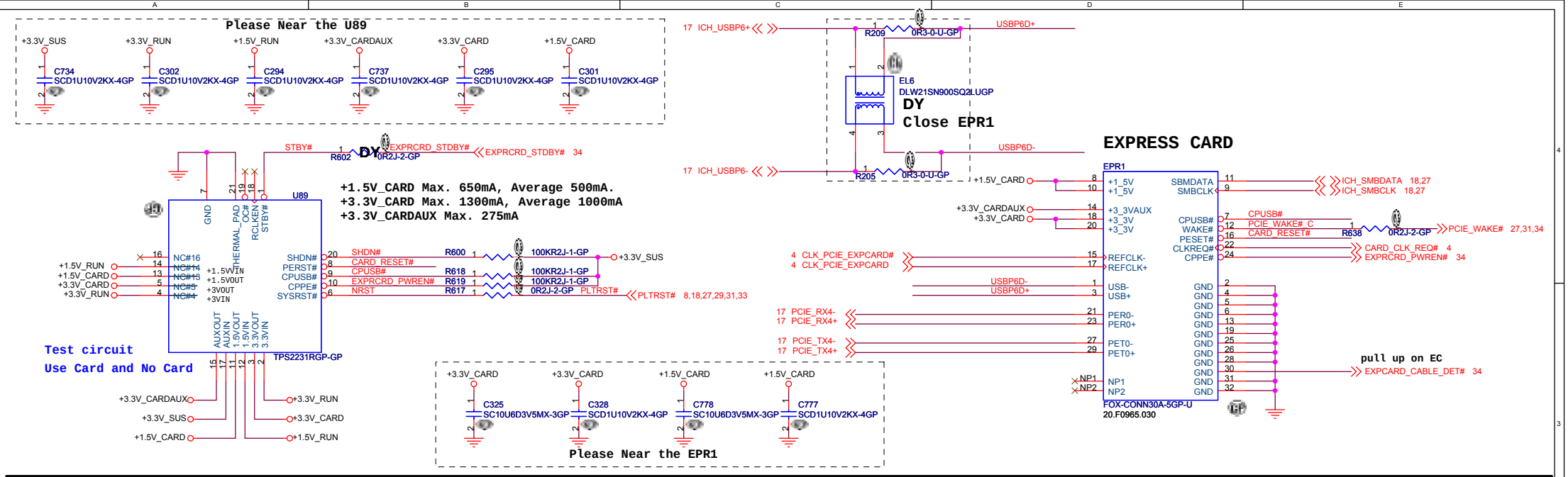
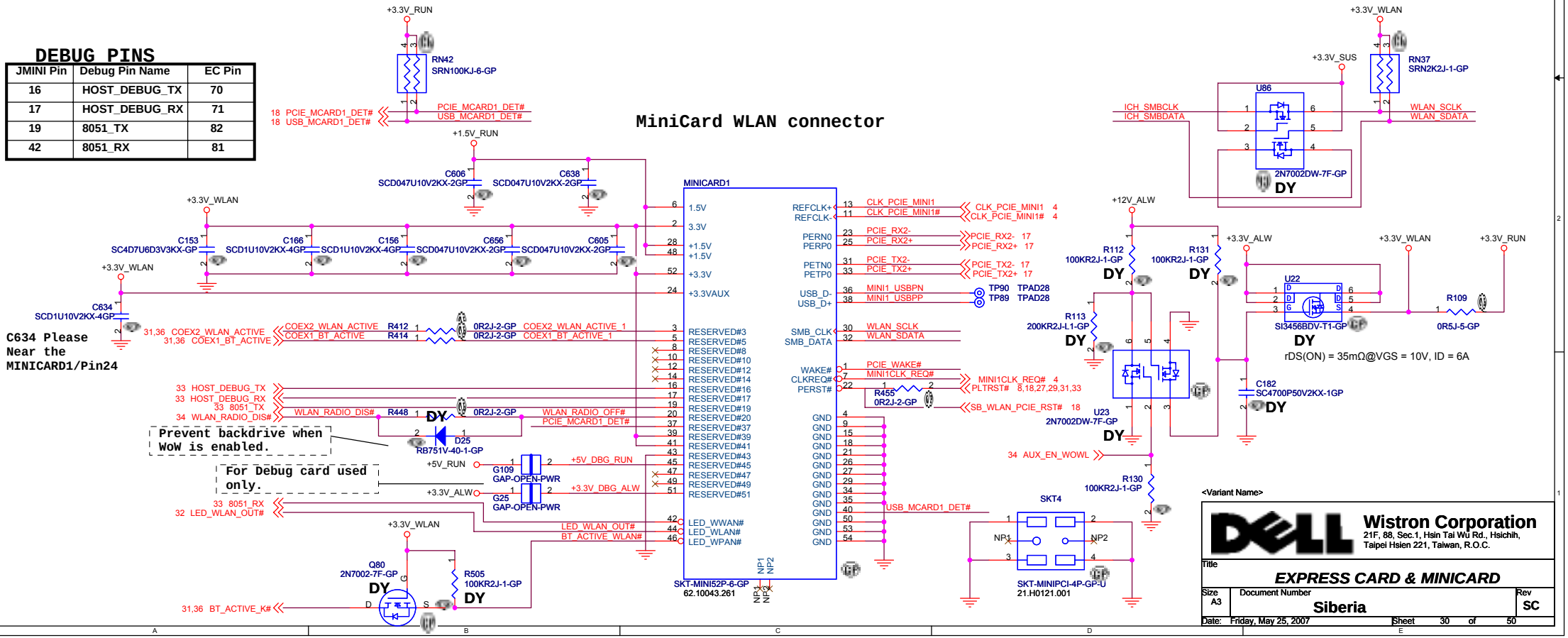
Date: Friday, May 25, 2007 Sheet 29 of 50



DEBUG_PINS

JMINI Pin	Debug Pin Name	EC Pin
16	HOST_DEBUG_TX	70
17	HOST_DEBUG_RX	71
19	8051_TX	82
42	8051_RX	81



<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: EXPRESS CARD & MINICARD

Size	Document Number	Rev
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Date: Friday, May 25, 2007 Sheet 30 of 50

MiniCard WWAN connector

Layout note: Place caps EC8,EC9 close SIM Card connector.

Layout note: Place caps EC3-EC7 close Mini Card connector.

C725 Please Near the MINICARD2/Pin24

Layout Note: Place resistors close to choke as possible to minimize stubs.

Close MINICARD2

MiniCard WPAN connector

C229 Please Near the MINICARD3/Pin24

R593 close to MINICARD3 Pin3

parallel with R593

This circuit is only needed if the platform has the SNIFFER

Layout Note: Place resistors close to choke as possible to minimize stubs.

Close MINICARD3

<Variant Name>

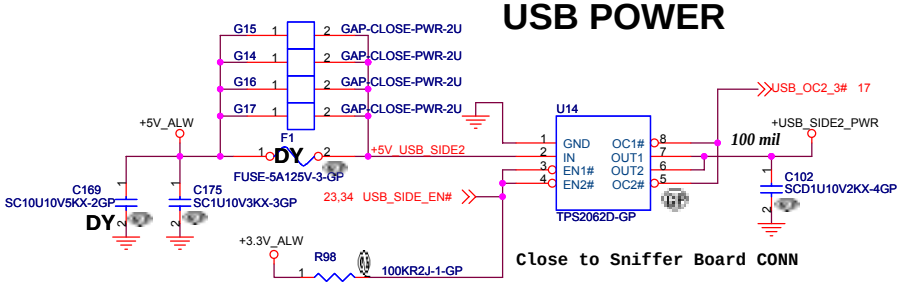
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINICARD

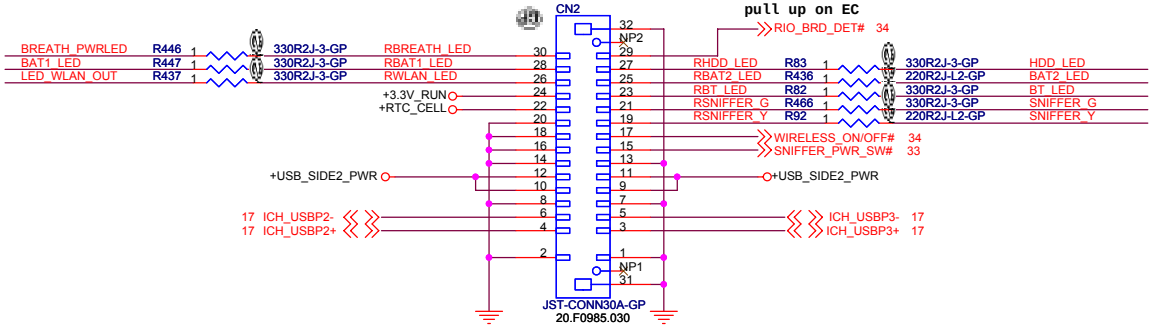
Size: A3 | Document Number: Siberia | Rev: SC

Date: Friday, May 25, 2007 | Sheet 31 of 50

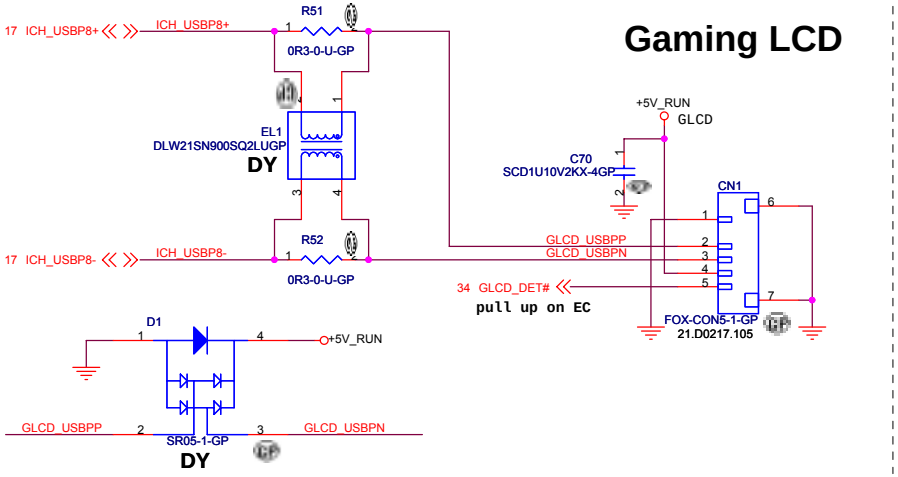
USB POWER



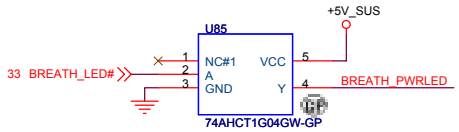
Sniffer board for USB, Indicator LEDs, Sniffer Switch conn.



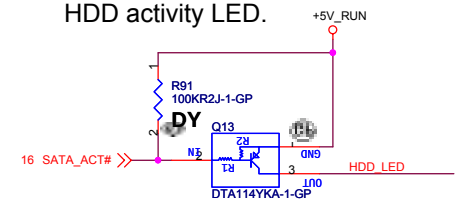
Gaming LCD



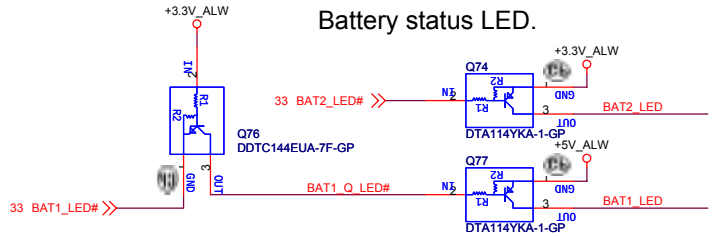
Power & Suspend LED.



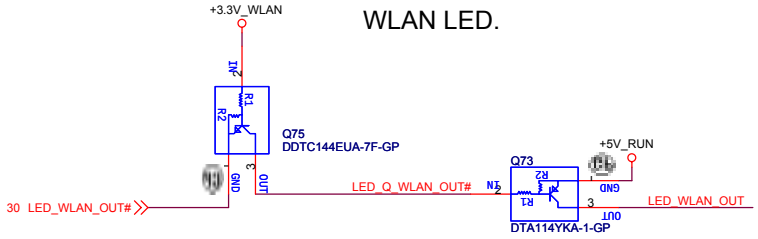
HDD activity LED.



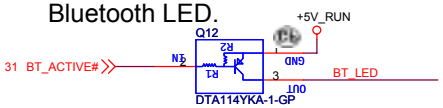
Battery status LED.



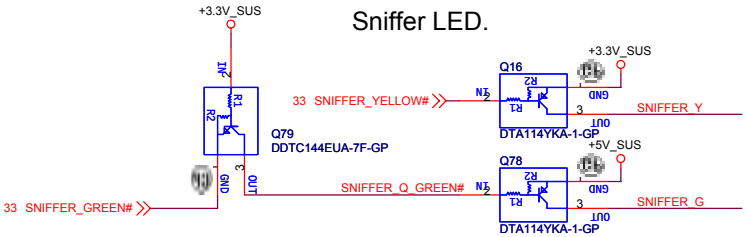
WLAN LED.



Bluetooth LED.



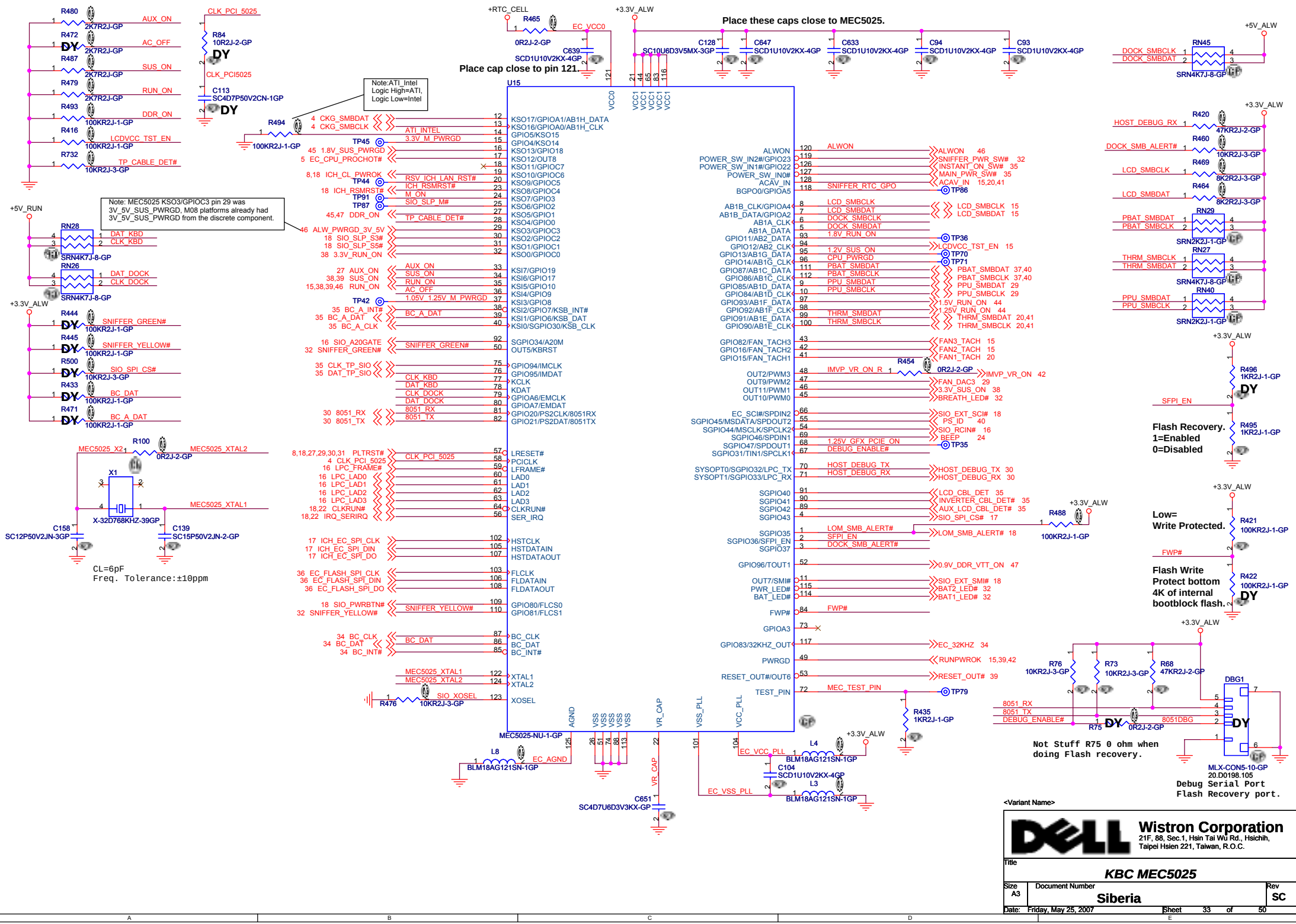
Sniffer LED.



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Sniffer board (USB/Status LEDs) / Gaming LCD*		
Size: A3	Document Number: Siberia	Rev: SC
Date: Friday, May 25, 2007	Sheet 32 of 50	


Place these caps close to MEC5025.
Place cap close to pin 121.
Note:ATI_Intel Logic High=ATI, Logic Low=Intel
Note: MEC5025 KSO3/GPIOC3 pin 29 was 3V_5V_SUS_PWRGD, M08 platforms already had 3V_5V_SUS_PWRGD from the discrete component.
U15
MEC5025-NU-1-GP
CL=6pF
Freq. Tolerance:±10ppm
Low= Write Protected.
Flash Write Protect bottom 4K of internal bootblock flash.
Flash Recovery. 1=Enabled 0=Disabled
Not Stuff R75 0 ohm when doing Flash recovery.
Debug Serial Port Flash Recovery port.
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
KBC MEC5025
Siberia
Friday, May 25, 2007
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CPU IDENTIFY
1 = AMD CPU
0 = Intel CPU

Board ID Straps

+3.3V_ALW

R389 10KR2J-3-GP DY
R388 10KR2J-3-GP DY
R387 10KR2J-3-GP
R408 10KR2J-3-GP DY
R407 10KR2J-3-GP DY
R406 10KR2J-3-GP 0SC

BID0
BID1
CHIPSET_ID1

BID1	BID0	Board Rev.
0	0	ENG1(X00)
0	1	ENG2(X01)
1	0	QT (X02)
1	1	RAMP(A00)

+3.3V_ALW

C612 SCD1U10V2KX-4GP
C89 SCD1U10V2KX-4GP
C578 SCD1U10V2KX-4GP
C122 SCD1U10V2KX-4GP
C100 SCD1U10V2KX-4GP
C86 SCD1U10V2KX-4GP
C74 SCD1U10V2KX-4GP

+3.3V_ALW

U12

VCC1 34, 57, 85, 108

40 PBAT_PRES# — SBAT_PRES# 97 GPIOA0
TP80 CHG_PBATT 98 GPIOA1
TP78 CHG_SBATT 99 GPIOA2
TP75 PBAT_DSCHG 100 GPIOA3
TP76 SYS_PME# 101 GPIOA4
22 SYS_PME# PCIE_WAKE# 102 GPIOA5
27,30,31 PCIE_WAKE# USB_BACK_EN# 103 GPIOA6
TP73 104 GPIOA7

32 WIRELESS_ON/OFF# 24 GPIOH0
36 BT_RADIO_DIS# 25 GPIOH1
30 EXPRCRD_PWREN# 26 GPIOH4
30 EXPRCRD_STDBY# 27 GPIOH5
33 BC_INT# 58 BC_INT#
33 BC_DAT 59 BD_DAT
33 BC_CLK 60 BC_CLK

35 M_LED_BK# 1 GPIOE0
TP57 SW_LED 2 GPIOE1
TP65 AUD_SUB_SHDN_ON_BATT 3 GPIOE2
TP55 TOUCH_PAD_LED# 4 GPIOE3
TP54 LOW_LIGHT 5 GPIOE4
TP81 CAM_IMG_CAPTURE 84 GPIOE5
24,26 AUD_MIC_SWITCH 83 GPIOE6
36 LID_CL_PRES# 6 GPIOE7

23,32 USB_SIDE_EN# 65 GPIOB0
TP38 PWRUSB_OC# 66 GPIOB1
TP82 QBUFEN# 67 GPIOC2
TP39 DOCK_PWR_EN 68 GPIOC3
41 ADAPT_OC 69 GPIOC4
41 ADAPT_TRIP_SET 70 GPIOC5
3,5,18 ITP_DBRESET# 71 GPIOC6
40 PSID_DISABLE# 73 GPIOC7
15 PANEL_BKEN PANEL_BKEN 74 GPIOD0
TP84 DOCKED 75 GPIOC1
DOCK_SMB_PME 76 GPIOC0
25,26 NB_MUTE# 77 GPIOB7
TP85 SIO_GPIOB6 78 GPIOB6
15 SPDIF_SHDN 79 GPIOB5
TP122 DOCK_HP_MUTE# 80 GPIOB4
24,26 AUD_HP1_NB_SENSE 81 GPIOB3
TP74 PWRUSB_EN 82 GPIOB2

36 LID_CL_SIO# 61 GPIOD1/CIRTX
45 1.05V_RUN_ON 62 GPIOD2/CIRRX

TP37 GFX_CORE_ON 63 GPIOD3
TP58 MODPRES# 28 GPIOD4
TP56 DBAY_MODPRES# 29 GPIOD5
21 HDDC_EN 30 GPIOD6
TP62 MODC_EN# 31 GPIOD7

42 IMVP6_PROCHOT# IMVP6_PROCHOT# 32 GPIOH6
39 5V_3V_RUN_PWRGD 33 GPIOH7

R424 10KR2J-3-GP
27 LOM_LOW_PWR LOM_LOW_PWR 88 GPIOG0
TP77 SC_DET# 89 GPIOG1
16,31 LED_MASK# 90 GPIOG2
TP83 SIO_GPIOG3 91 GPIOG3
R434 0R2J-2-GP SIO_EXT_WAK# 92 GPIOG4
18 SIO_EXT_WAKE# 93
18 ICH_PME# 94 GPIOG5
18 ICH_PCIE_WAKE# 95 GPIOG6
30 WLAN_RADIO_DIS# 96 GPIOG7

31 WWAN_RADIO_DIS# 106 GPIOH2
27 LOM_CABLE_DETECT 107 GPIOH3

TP72 LOM_TPM_EN# 109 GPIOF7
R405 10KR2J-3-GP 27 LOM_SUPER_IDDQ 110 GPIOF6
+3.3V_ALW VGA_IDENTIFY 111 GPIOF5
CHIPSET_ID1 112 GPIOF4

TP69 IRTX 113 CIRTX
36 CIRRX CIRRX 114 CIRRX

BID1 115 GPIOF3
BID0 116 GPIOF2
20 ATF_INT# 117 GPIOF1
TP68 SIO_GPIOF0 118 GPIOF0

ECE5021-NU-GP

VCC1 8 +3.3V_ALW
GPIOJ7 14 GLCD_DET# 32
GPIOK4 20 SIO_GPIOK4 TP63
GPIOI1 119 PPU_SYS_ON_BATT 29

GPIOJ2 9 FAN1_DET# FAN1_DET# 20
GPIOJ3 10 FAN2_DET# TP67
GPIOJ6 13 LIO_BRD_DET# LIO_BRD_DET# 23
GPIOJ5 12 KB_LED_DET# KB_LED_DET# 35
GPIOK0 15 SATA_CABLE_DET# SATA_CABLE_DET# 21
GPIOK1 16 AUD_CABLE_DET# AUD_CABLE_DET# 26
GPIOK3 19 EXPCARD_CABLE_DET# 30
GPIOK2 18 RIO_BRD_DET# 32
GPIOK5 21 SIO_GPIOK5 TP59
GPIOK6 22 AUX_EN_WOWL 30

GPIOI6 125 GFX_GPU1_PWRGD 15
GPIOI5 124 GFX_GPU2_ON 15
GPIOI2 120 PPU_CARD_DET# PPU_CARD_DET# 29
CAP_LDO 86 SIO_CAP_LDO
GPIOJ0 127 SIO_GPIOJ0 TP25
C627 SC4D7U6D3V3KX-GP
TEST_PIN 35 RSV_TEST_PIN TP64
GPIOI7 126 GFX_GPU2_PWRGD 15
GPIOI4 123 PPU_PWRGD 29
GPIOI3 122 PPU_PWR_ON 29

VSS 54, 52, 49, 47, 42, 41, 56, 37, 46, 44, 39, 64
VCC1 +3.3V_ALW
NC#46
KHZ_32 96 EC_32KHZ 33

VSS 55, 53, 50, 48, 43, 38, 45, 40
VCC1 +3.3V_ALW
PWRGD 7
OUT65 105 LCD_TST LCD_TST 15

GPIOJ4 11 BRAND_LED BRAND_LED 35
VSS 17
GPIOK7 23 IMVP_PWRGD 18,39,42
VSS 36, 51, 72, 87, 121
VSS 128 SIO_GPIOJ1 TP61
GPIOJ1

+5V_ALW
DOCK_SMB_PME R425 10KR2J-3-GP

+3.3V_ALW
SYS_PME# PCIE_WAKE# RN25 SRN10KJ-5-GP
LID_CL_PRES# PPU_CARD_DET# RN1 SRN100KJ-6-GP
EXPCARD_CABLE_DET# R360 100KR2J-1-GP

RP1 SRN100KJ-7-GP
FAN1_DET#
KB_LED_DET#
GLCD_DET#
AUD_CABLE_DET#
+3.3V_ALW
FAN2_DET#
LIO_BRD_DET#
SATA_CABLE_DET#
RIO_BRD_DET#

+3.3V_RUN
IMVP6_PROCHOT# R365 100KR2J-1-GP
BRAND_LED R359 100KR2J-1-GP
PANEL_BKEN R426 100KR2J-1-GP
LCD_TST R423 100KR2J-1-GP

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SIO ECE5021

Size	Document Number	Rev
A3	Siberia	SC

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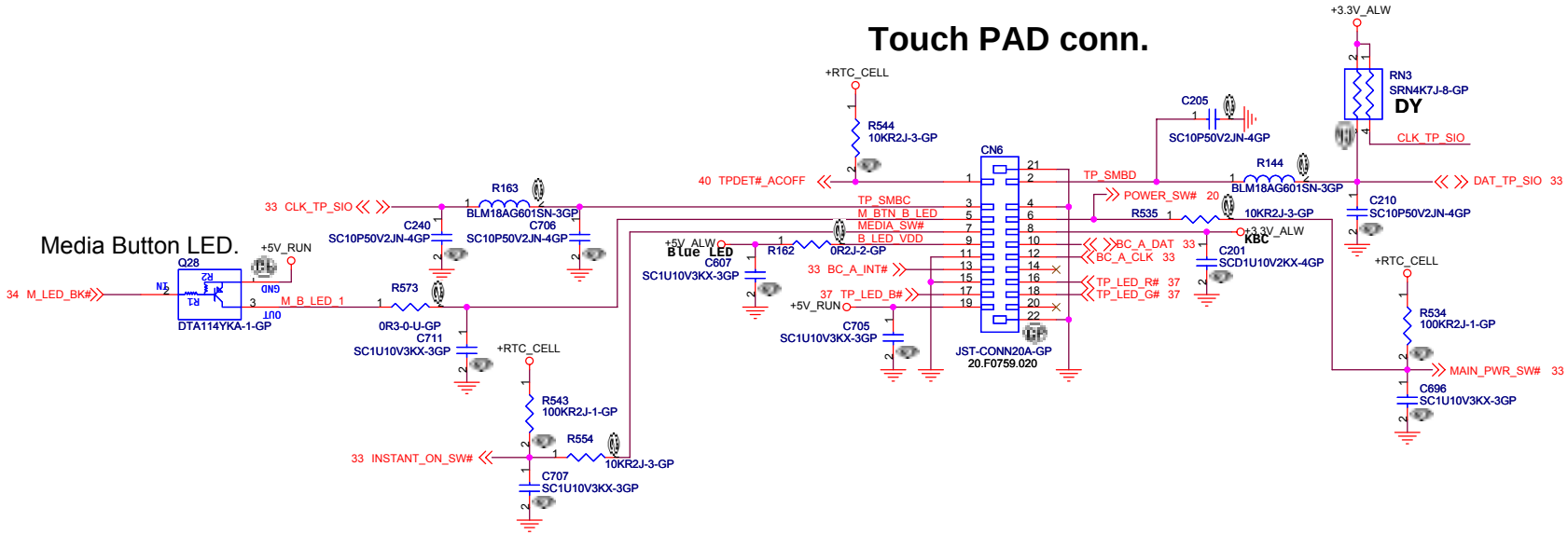
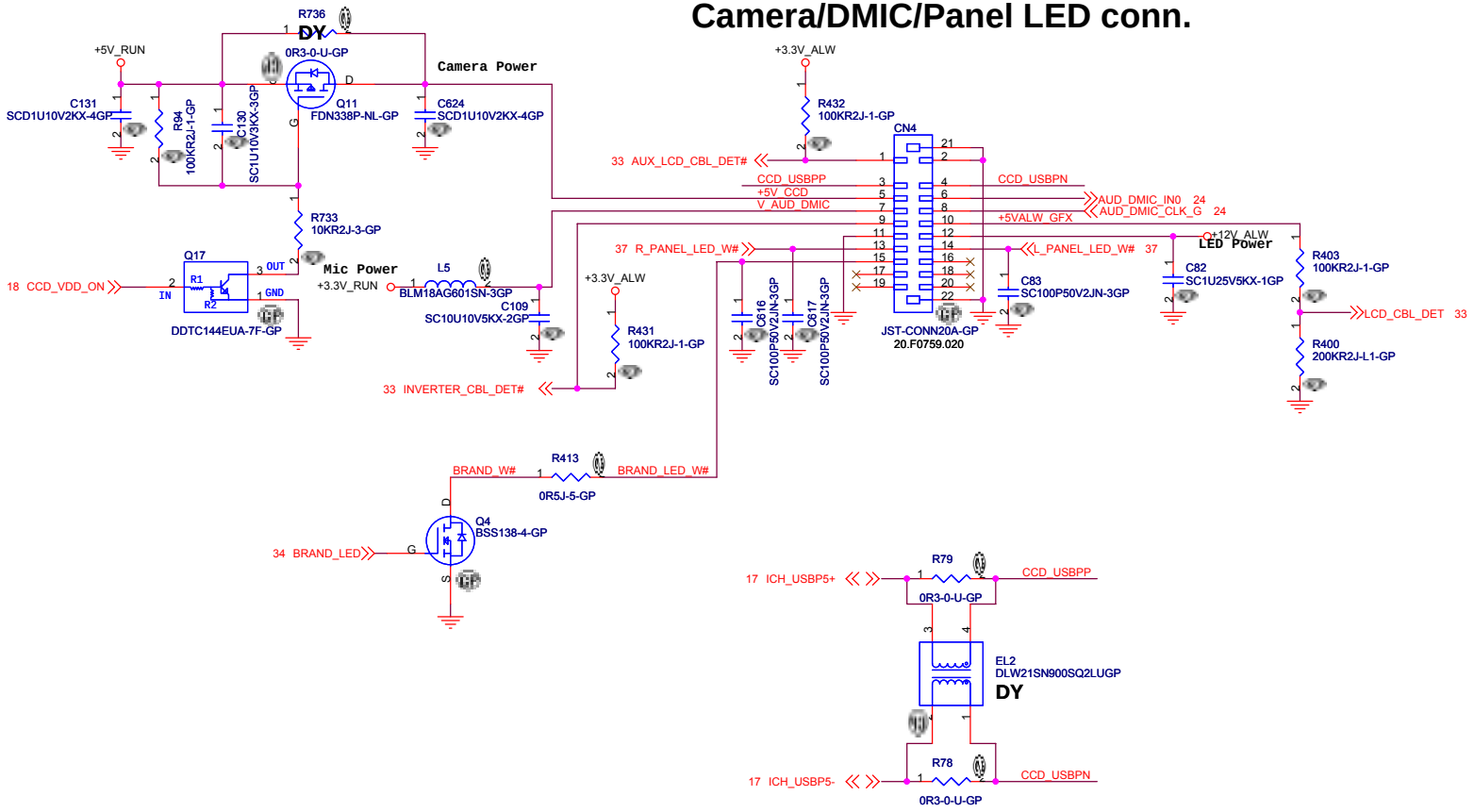
Touch PAD conn.

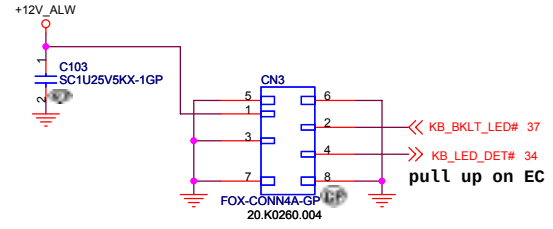


rDS(ON) = 115mΩ@VGS = -4.5V, ID = -1.6A

Camera/DMIC/Panel LED conn.



KB BKLT LED

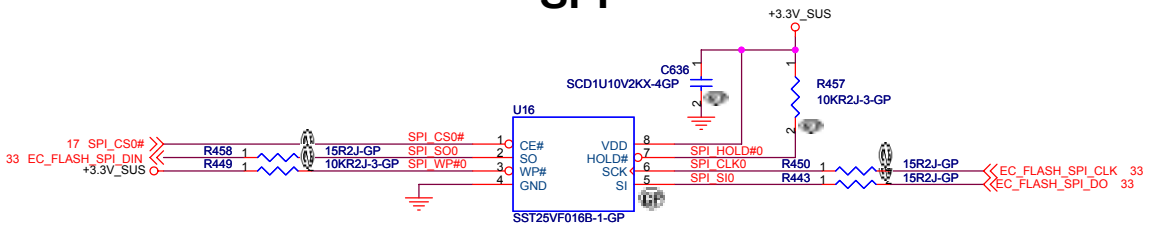


<Variant Name>

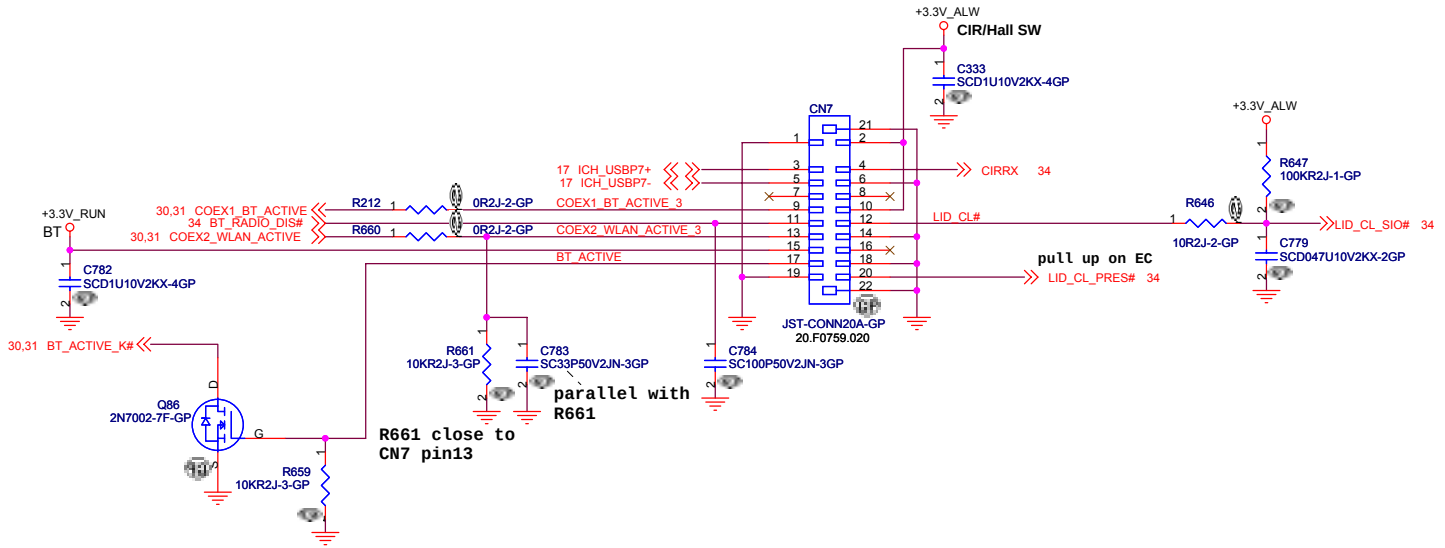
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Touch PAD/Camera/DMIC	
Size: A3	Document Number: Siberia	Rev: SC
Date: Friday, May 25, 2007	Sheet 35 of 50	

SPI



Bluetooth/ CIR/ Hall SW



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***SPI FLASH / Bluetooth / CIR / LID***

Size	Document Number	Rev
A3	Siberia	SC

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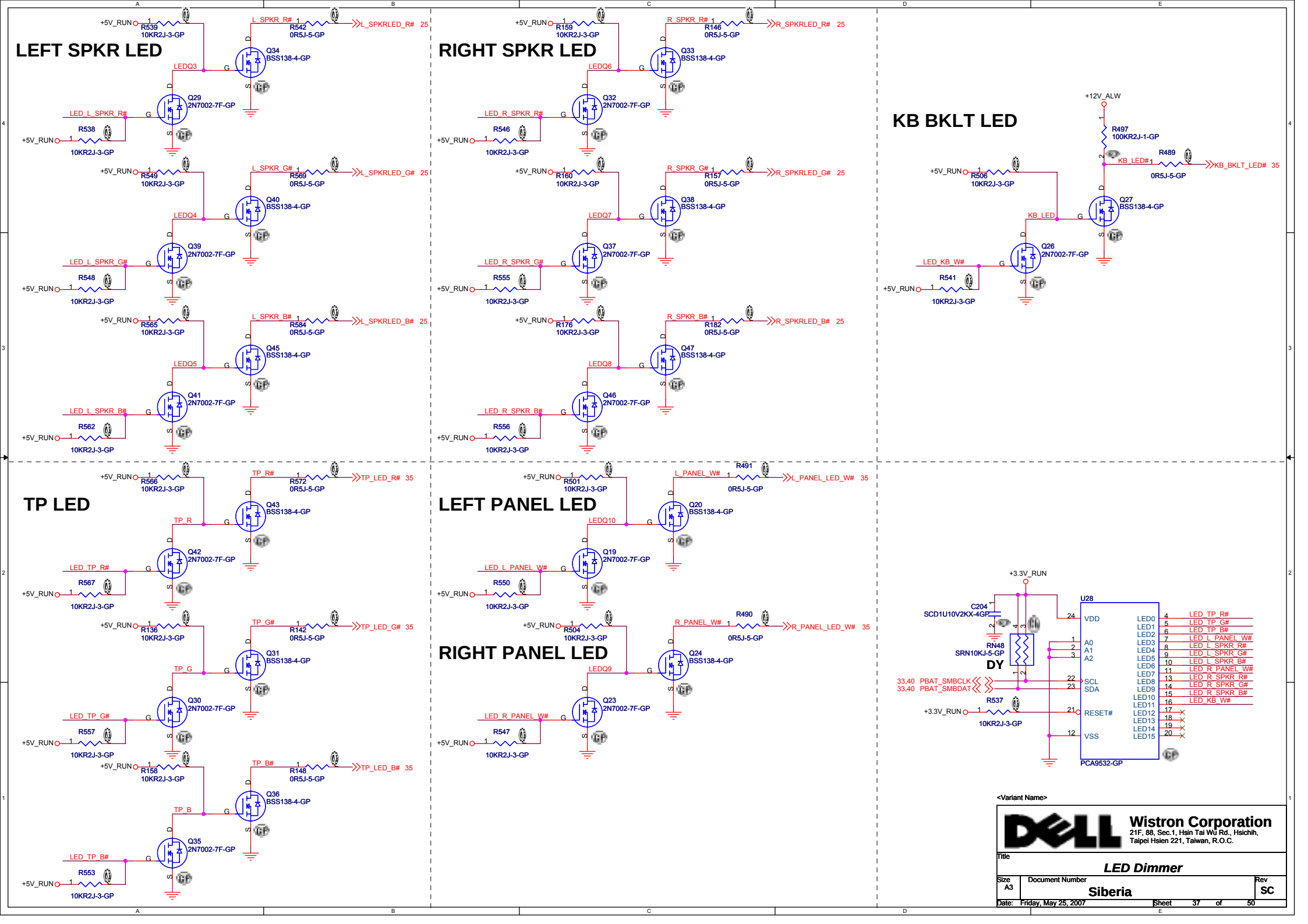
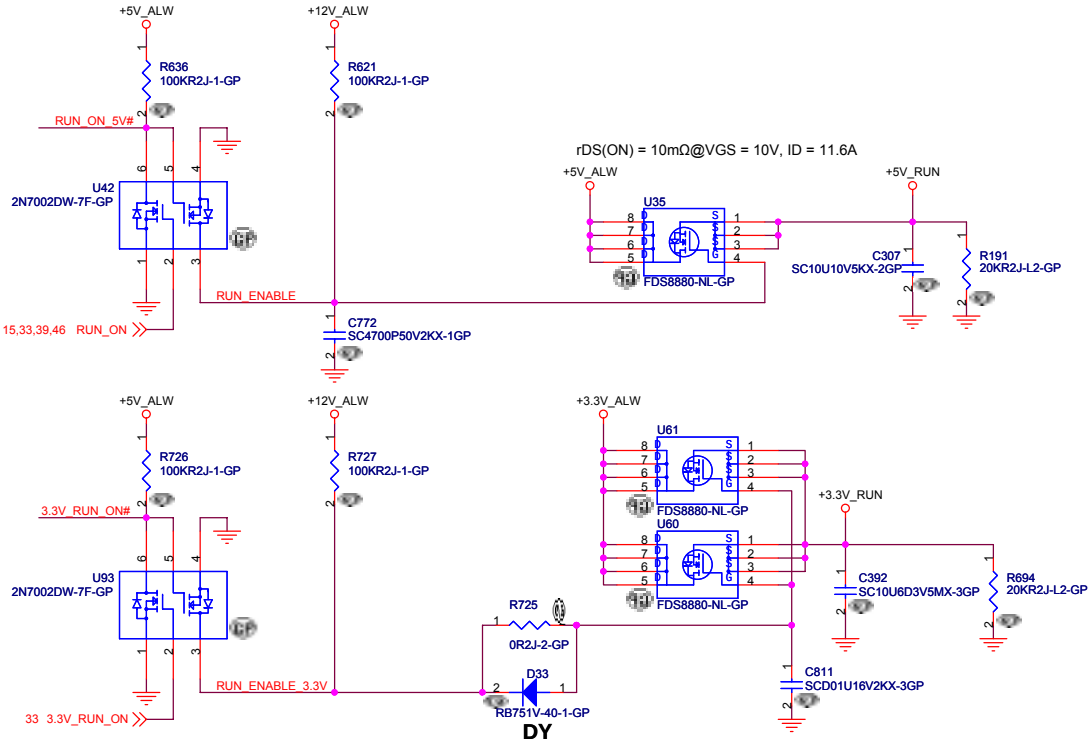
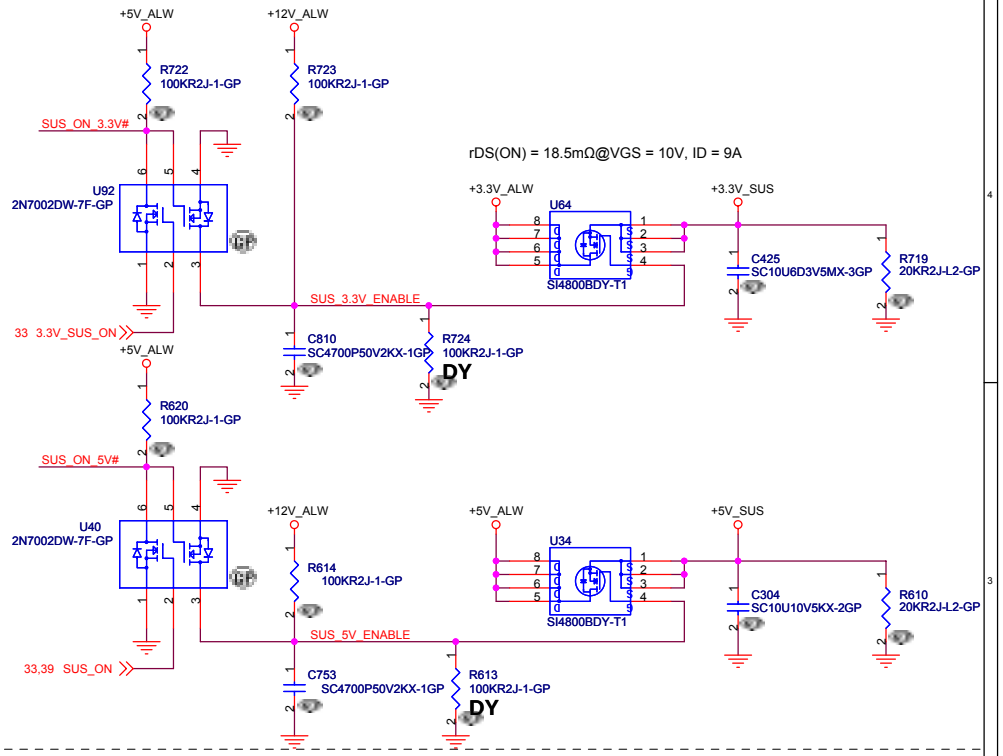
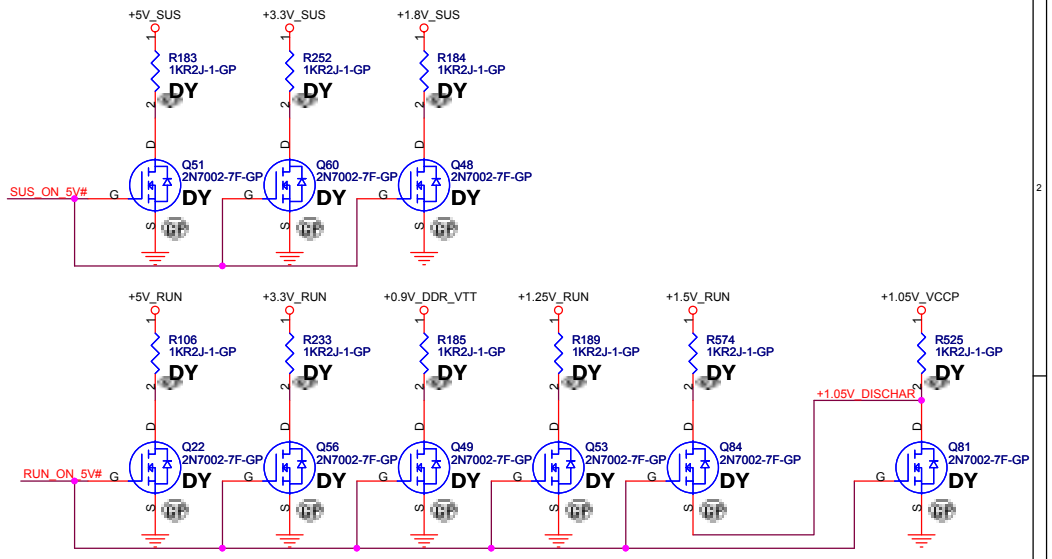

LEFT SPKR LED
+5V_RUN
R539 10KR2J-3-GP
L_SPKR_R#
R542 0R5J-5-GP
L_SPKRLED_R# 25
Q34 BSS138-4-GP
LEDQ3
Q29 2N7002-7F-GP
LED_L_SPKR_R#
R538 10KR2J-3-GP
R549 10KR2J-3-GP
L_SPKR_G#
R569 0R5J-5-GP
L_SPKRLED_G# 25
Q40 BSS138-4-GP
LEDQ4
Q39 2N7002-7F-GP
LED_L_SPKR_G#
R548 10KR2J-3-GP
R565 10KR2J-3-GP
L_SPKR_B#
R584 0R5J-5-GP
L_SPKRLED_B# 25
Q45 BSS138-4-GP
LEDQ5
Q41 2N7002-7F-GP
LED_L_SPKR_B#
R562 10KR2J-3-GP
RIGHT SPKR LED
R159 10KR2J-3-GP
R_SPKR_R#
R146 0R5J-5-GP
R_SPKRLED_R# 25
Q33 BSS138-4-GP
LEDQ6
Q32 2N7002-7F-GP
LED_R_SPKR_R#
R546 10KR2J-3-GP
R160 10KR2J-3-GP
R_SPKR_G#
R157 0R5J-5-GP
R_SPKRLED_G# 25
Q38 BSS138-4-GP
LEDQ7
Q37 2N7002-7F-GP
LED_R_SPKR_G#
R555 10KR2J-3-GP
R176 10KR2J-3-GP
R_SPKR_B#
R182 0R5J-5-GP
R_SPKRLED_B# 25
Q47 BSS138-4-GP
LEDQ8
Q46 2N7002-7F-GP
LED_R_SPKR_B#
R556 10KR2J-3-GP
KB BKLT LED
+12V_ALW
R497 100KR2J-1-GP
R489 0R5J-5-GP
KB_LED#
KB_BKLT_LED# 35
R506 10KR2J-3-GP
KB_LED
Q27 BSS138-4-GP
Q26 2N7002-7F-GP
LED_KB_W#
R541 10KR2J-3-GP
TP LED
R566 10KR2J-3-GP
TP_R#
R572 0R5J-5-GP
TP_LED_R# 35
Q43 BSS138-4-GP
TP_R
Q42 2N7002-7F-GP
LED_TP_R#
R567 10KR2J-3-GP
R136 10KR2J-3-GP
TP_G#
R142 0R5J-5-GP
TP_LED_G# 35
Q31 BSS138-4-GP
TP_G
Q30 2N7002-7F-GP
LED_TP_G#
R557 10KR2J-3-GP
R158 10KR2J-3-GP
TP_B#
R148 0R5J-5-GP
TP_LED_B# 35
Q36 BSS138-4-GP
TP_B
Q35 2N7002-7F-GP
LED_TP_B#
R553 10KR2J-3-GP
LEFT PANEL LED
R501 10KR2J-3-GP
L_PANEL_W#
R491
0R5J-5-GP
L_PANEL_LED_W# 35
Q20 BSS138-4-GP
LEDQ10
Q19 2N7002-7F-GP
LED_L_PANEL_W#
R550 10KR2J-3-GP
RIGHT PANEL LED
R504 10KR2J-3-GP
R_PANEL_W#
R490
0R5J-5-GP
R_PANEL_LED_W# 35
Q24 BSS138-4-GP
LEDQ9
Q23 2N7002-7F-GP
LED_R_PANEL_W#
R547 10KR2J-3-GP
+3.3V_RUN
C204 SCD1U10V2KX-4GP
RN48 SRN10KJ-5-GP
DY
33,40 PBAT_SMBCLK
33,40 PBAT_SMBDAT
R537 10KR2J-3-GP
U28
VDD
A0
A1
A2
SCL
SDA
RESET#
VSS
LED0
LED1
LED2
LED3
LED4
LED5
LED6
LED7
LED8
LED9
LED10
LED11
LED12
LED13
LED14
LED15
PCA9532-GP
LED_TP_R#
LED_TP_G#
LED_TP_B#
LED_L_PANEL_W#
LED_L_SPKR_R#
LED_L_SPKR_G#
LED_L_SPKR_B#
LED_R_PANEL_W#
LED_R_SPKR_R#
LED_R_SPKR_G#
LED_R_SPKR_B#
LED_KB_W#
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
LED Dimmer
Size A3
Document Number
Siberia
Rev SC
Date: Friday, May 25, 2007
Sheet 37 of 50







Reserve discharge path

CRB 0.95:
Insures that +1.05_VCCP and +1.5_RUN ramp down together by discharing +1.5V_RUN into +1.05V_VCCP

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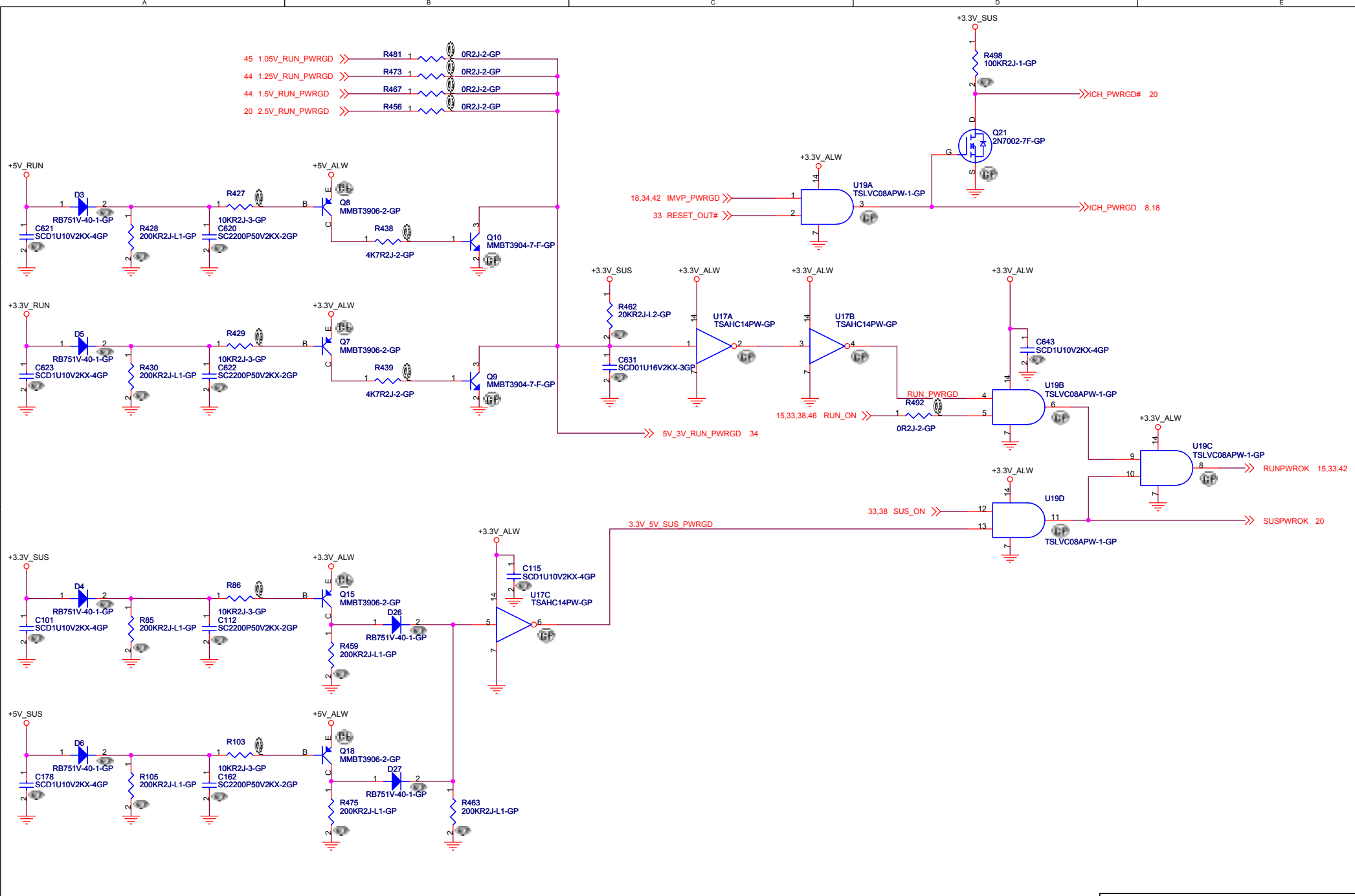
Title: ***Power Plane Enable***

Size	Document Number	Rev
A3	Siberia	SC

Date: Friday, May 25, 2007 Sheet 38 of 50



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: ***Power On Logic***

Size	Document Number	Rev
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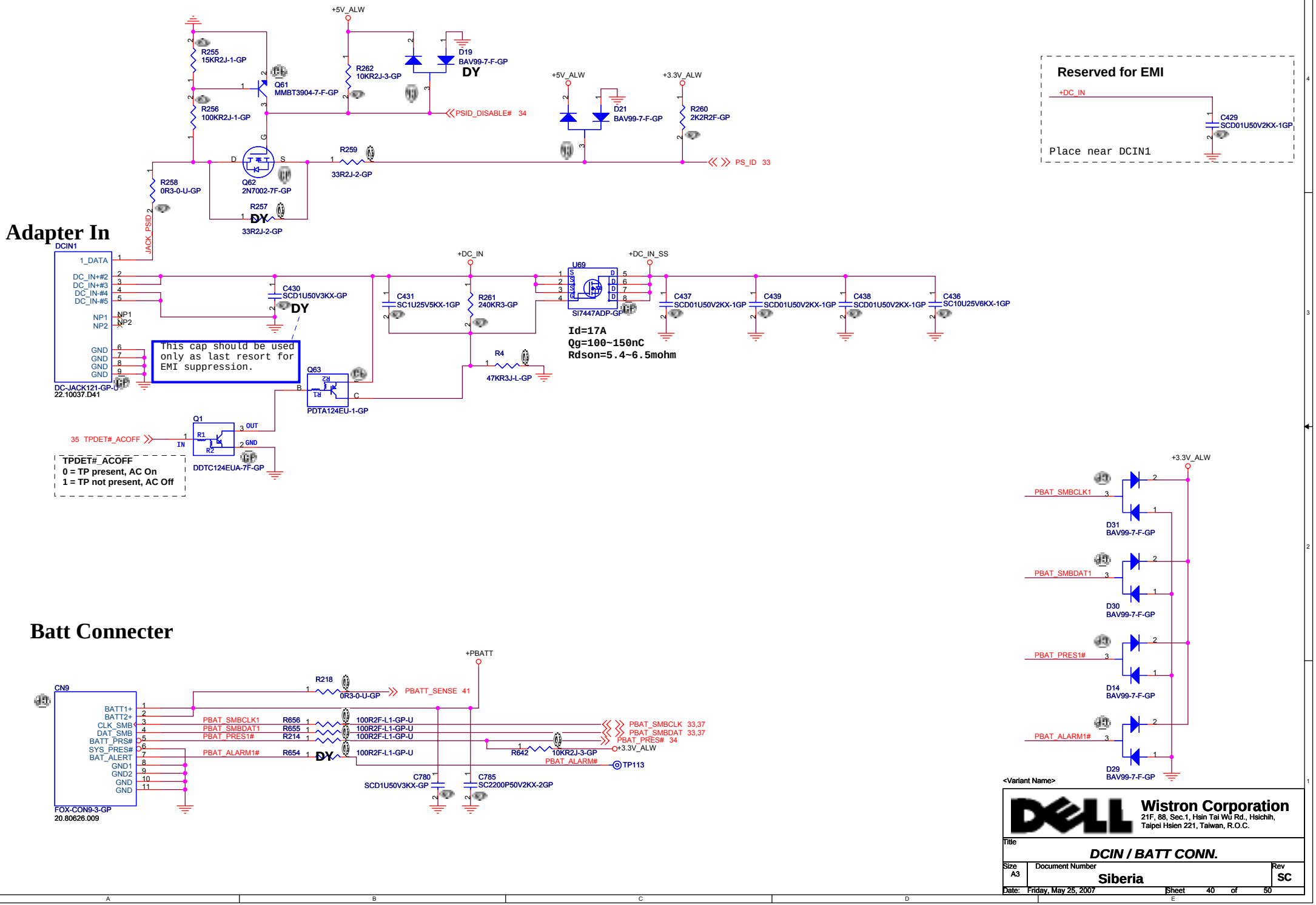
Adapter In
+5V_ALW
R255 15KR2J-1-GP
R256 100KR2J-1-GP
Q61 MMBT3904-7-F-GP
R262 10KR2J-3-GP
D19 BAV99-7-F-GP
DY
PSID_DISABLE# 34
+5V_ALW
D21 BAV99-7-F-GP
+3.3V_ALW
R260 2K2R2F-GP
PS_ID 33
R259 33R2J-2-GP
Q62 2N7002-7F-GP
R258 0R3-0-U-GP
JACK_PSID
R257 DY 33R2J-2-GP
DCIN1
1_DATA
DC_IN+#2
DC_IN+#3
DC_IN-#4
DC_IN-#5
NP1
NP2
GND
GND
GND
GND
DC-JACK121-GP-U
22.10037.D41
C430 SCD1U50V3KX-GP DY
C431 SC1U25V5KX-1GP
+DC_IN
R261 240KR3-GP
+DC_IN_SS
U69
SI7447ADP-GP
C437 SCD01U50V2KX-1GP
C439 SCD01U50V2KX-1GP
C438 SCD01U50V2KX-1GP
C436 SC10U25V6KX-1GP
Id=17A
Qg=100~150nC
Rdson=5.4~6.5mohm
This cap should be used only as last resort for EMI suppression.
Q63
PDTA124EU-1-GP
R4 47KR3J-L-GP
Q1
DDTC124EUA-7F-GP
35 TPDET#_ACOFF
TPDET#_ACOFF
0 = TP present, AC On
1 = TP not present, AC Off
Reserved for EMI
+DC_IN
C429 SCD01U50V2KX-1GP
Place near DCIN1
Batt Connecter
+PBATT
CN9
BATT1+
BATT2+
CLK_SMB
DAT_SMB
BATT_PRS#
SYS_PRES#
BAT_ALERT
GND1
GND2
GND
GND
FOX-CON9-3-GP
20.80626.009
R218 0R3-0-U-GP
PBATT_SENSE 41
PBAT_SMBCLK1
PBAT_SMBDAT1
PBAT_PRES1#
PBAT_ALARM1#
R656 100R2F-L1-GP-U
R655 100R2F-L1-GP-U
R214 100R2F-L1-GP-U
R654 DY 100R2F-L1-GP-U
PBAT_SMBCLK 33,37
PBAT_SMBDAT 33,37
PBAT_PRES# 34
R642 10KR2J-3-GP
+3.3V_ALW
PBAT_ALARM#
TP113
C780 SCD1U50V3KX-GP
C785 SC2200P50V2KX-2GP
+3.3V_ALW
PBAT_SMBCLK1
D31 BAV99-7-F-GP
PBAT_SMBDAT1
D30 BAV99-7-F-GP
PBAT_PRES1#
D14 BAV99-7-F-GP
PBAT_ALARM1#
D29 BAV99-7-F-GP
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DCIN / BATT CONN.
Size A3
Document Number
Siberia
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PIN NAME DIFFERENCES

PIN	MAXIM	INTERSIL
1	GND	NC
3	REF	VREF
4	CCS	ICOMP
5	CCI	NC
6	CCV	VCOMP
7	DAC	NC
8	IINP	ICM
11	VDD	VDDSMB
14	BATSEL	NC
15	FBSA	VFB
16	FBSB	NC
17	CSIN	CSON
18	CSIP	CSOP
20	DLO	LGATE
21	LDO	VDDP
23	LX	PHASE
24	DHI	UGATE
25	BST	BOOT

"NC" means no-connect

This Resistor must be 1% tolerance.

TABLE

MAXIM & INTERSIL BOM DIFFERENCES

REF DES	MAXIM	INTERSIL
R217	8.45K 1%	DUMMY
C323	0.01uF	0.1uF
C352	0.1uF 10V	DUMMY
C341	1uF 10V	DUMMY
R204	365K 1%	215K 1%
R242	0 5%	10 5%
R207	0 5%	10 5%
C382	DUMMY	0.22uF
C349	DUMMY	0.22uF
C343	0.01uF	DUMMY
C342	0.1uF 10V	DUMMY
C374	220pF 50V	DUMMY
D15	1SS400	DUMMY
C330	3.3nF	DUMMY
R232	1 1%	0 5%
R236	100 5%	0 5%
R208	10K 5%	2.2K 5%
C335	0.01uF	0.01uF
C344	0.01uF	0.01uF
R199	0 5%	8.45K 1%
R201	1K 1%	DUMMY
D12	1SS355	DUMMY

Id=17A
Qg=100~150nC
Rdson=5.4~6.5mohm

Charge Current: 4.7A
Discharge Current: 12A maximum for 5 minutes

Change from 0.1U to 0.01U.

R190 should be not stuff when Adapter is 230W

<Core Design>

Wistron Corporation
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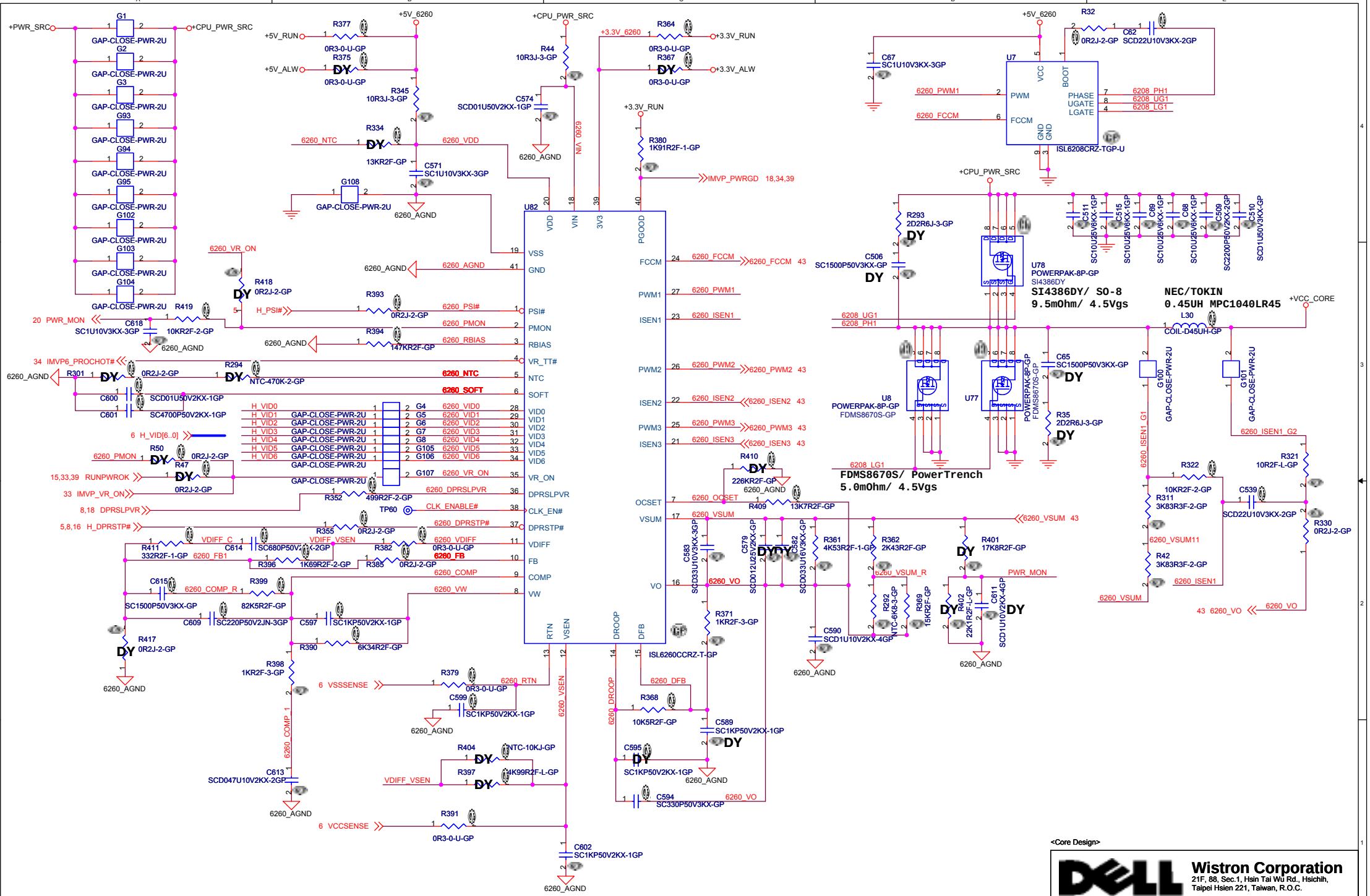
Taipei Hsien 221, Taiwan, R.O.C.

Title: Charger

Size: A3 | Document Number: Siberia | Rev: SC

Date: Friday, May 25, 2007 | Sheet 41 of 50



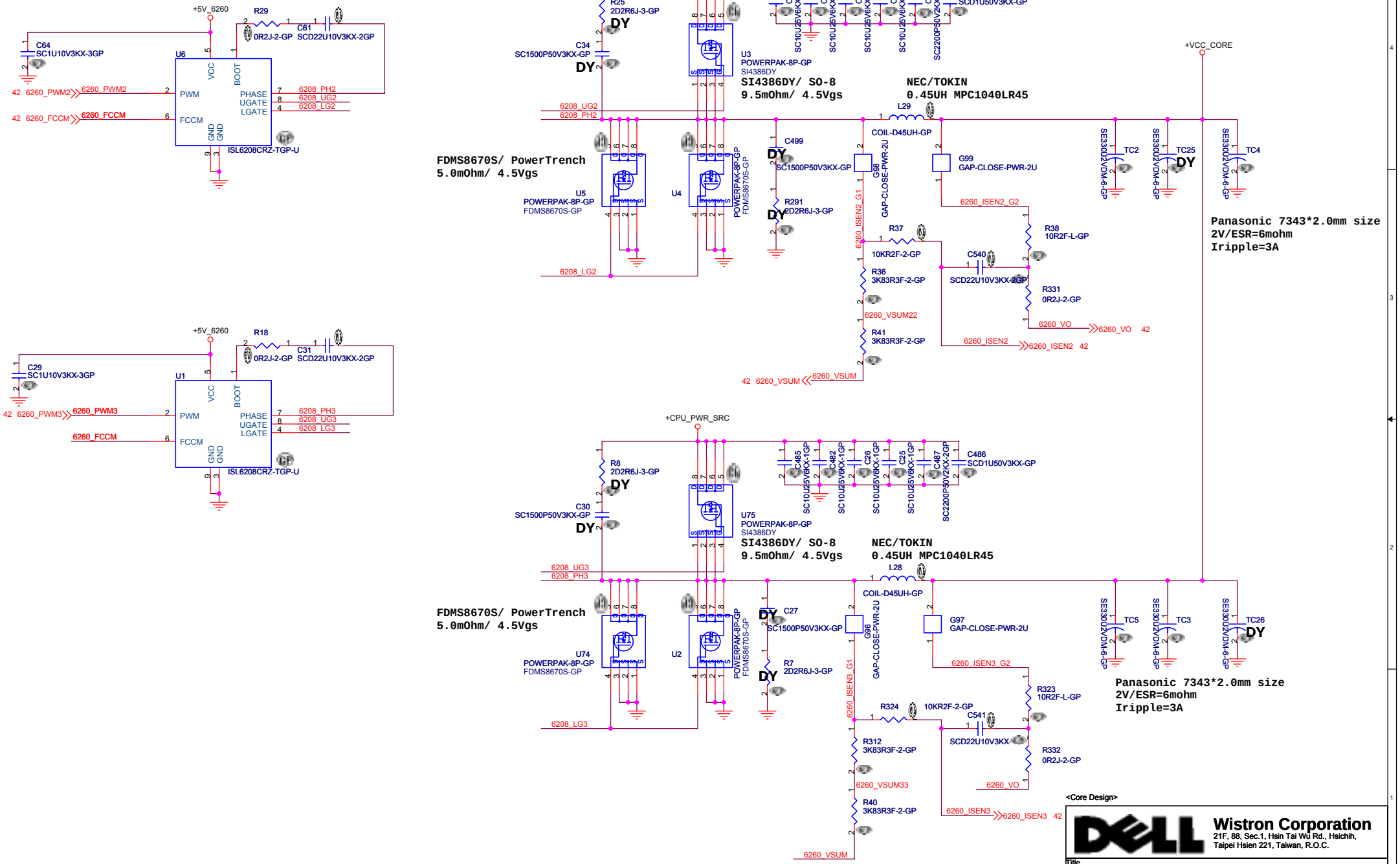
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU Vcore Power_1

Size: A3 | Document Number: Siberia | Rev: SC

Date: Friday, May 25, 2007 | Sheet 42 of 50



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CPU Vcore Power_2*

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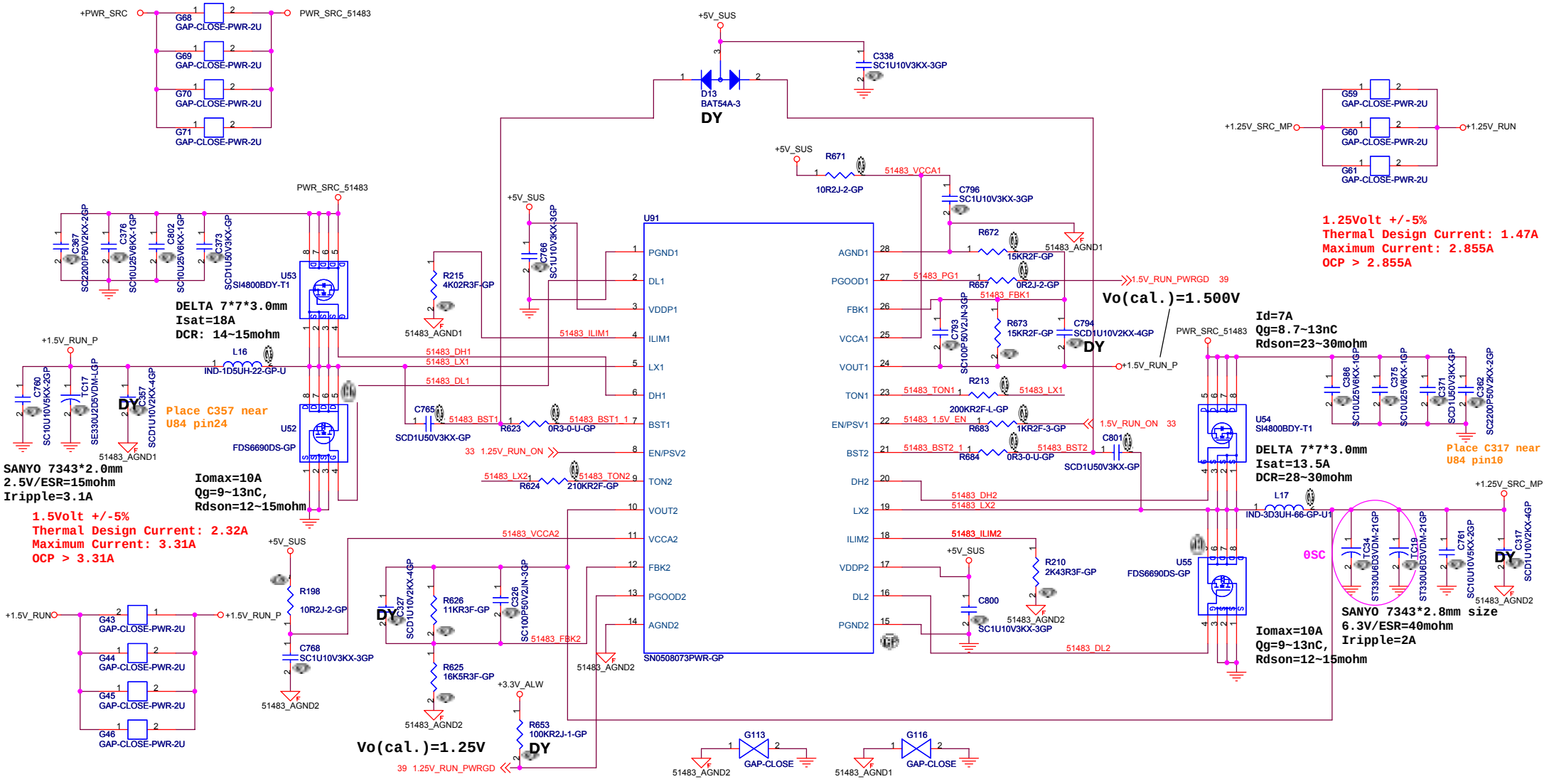
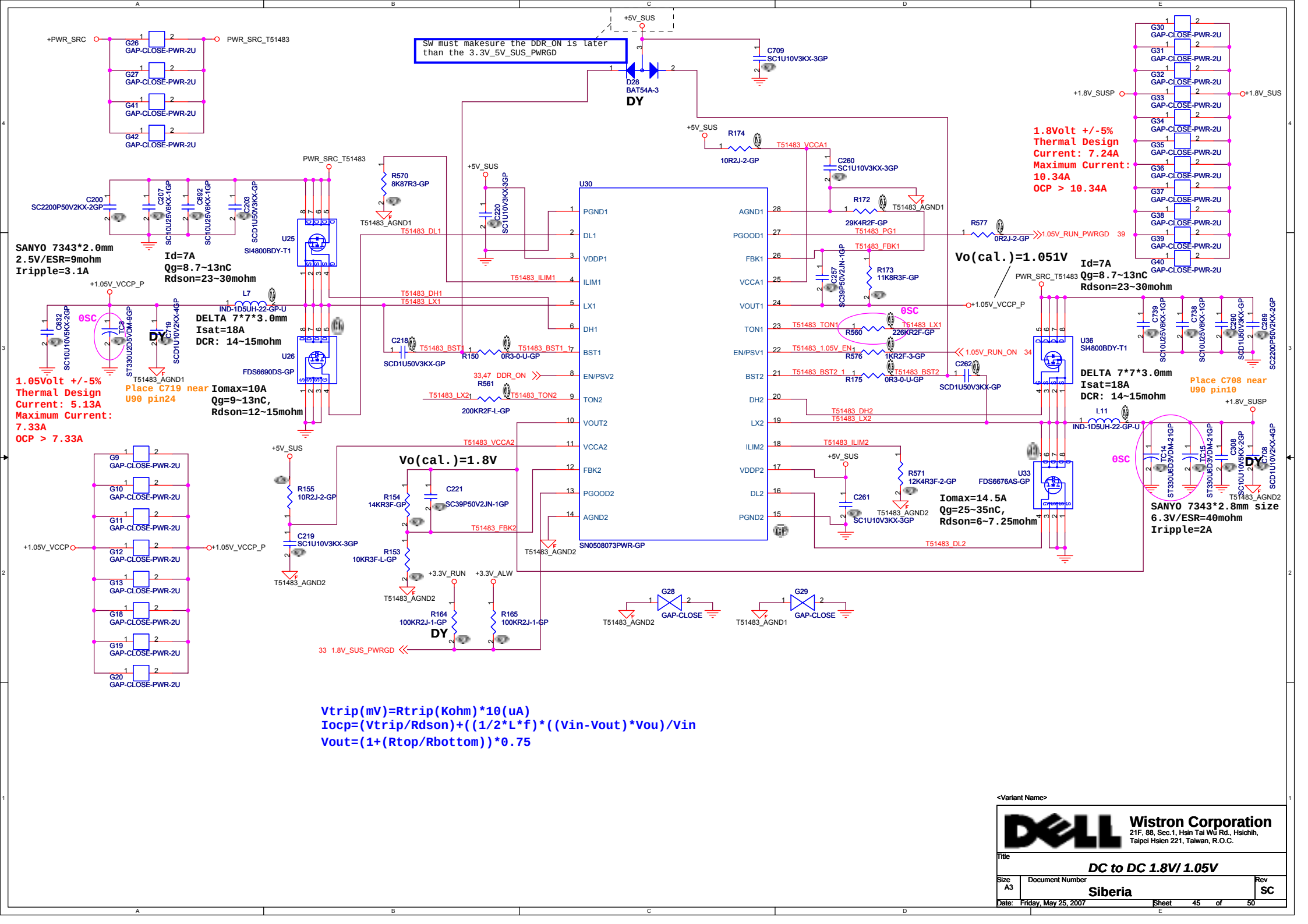


Vtrip(mV)=Rtrip(Kohm)*10(uA)
Iocp=(Vtrip/Rdson)+((1/2*L*f)*((Vin-Vout)*Vou)/Vin
Vout=(1+(Rtop/Rbottom))*0.75

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *DC to DC 1.5V/ 1.25V*		
Size: A3	Document Number: Siberia	Rev: SC
Date: Friday, May 25, 2007	Sheet 44 of 50	


SW must makesure the DDR_ON is later than the 3.3V_5V_SUS_PWRGD
SANYO 7343*2.0mm
2.5V/ESR=9mohm
Iripple=3.1A
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
1.05Volt +/-5%
Thermal Design
Current: 5.13A
Maximum Current:
7.33A
OCP > 7.33A
DELTA 7*7*3.0mm
Isat=18A
DCR: 14~15mohm
Iomax=10A
Qg=9~13nC,
Rdson=12~15mohm
Place C719 near U90 pin24
Vo(cal.)=1.8V
1.8Volt +/-5%
Thermal Design
Current: 7.24A
Maximum Current:
10.34A
OCP > 10.34A
Vo(cal.)=1.051V
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
DELTA 7*7*3.0mm
Isat=18A
DCR: 14~15mohm
Iomax=14.5A
Qg=25~35nC,
Rdson=6~7.25mohm
Place C708 near U90 pin10
SANYO 7343*2.8mm size
6.3V/ESR=40mohm
Iripple=2A
Vtrip(mV)=Rtrip(Kohm)*10(uA)
Iocp=(Vtrip/Rdson)+((1/2*L*f)*((Vin-Vout)*Vou)/Vin
Vout=(1+(Rtop/Rbottom))*0.75
U30
SN0508073PWR-GP
U25
SI4800BDY-T1
U26
FDS6690DS-GP
U36
SI4800BDY-T1
U33
FDS6676AS-GP
D28
BAT54A-3
DY
0SC
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
<Variant Name>
DC to DC 1.8V/ 1.05V
Size A3
Document Number
Siberia
Rev SC
Date: Friday, May 25, 2007
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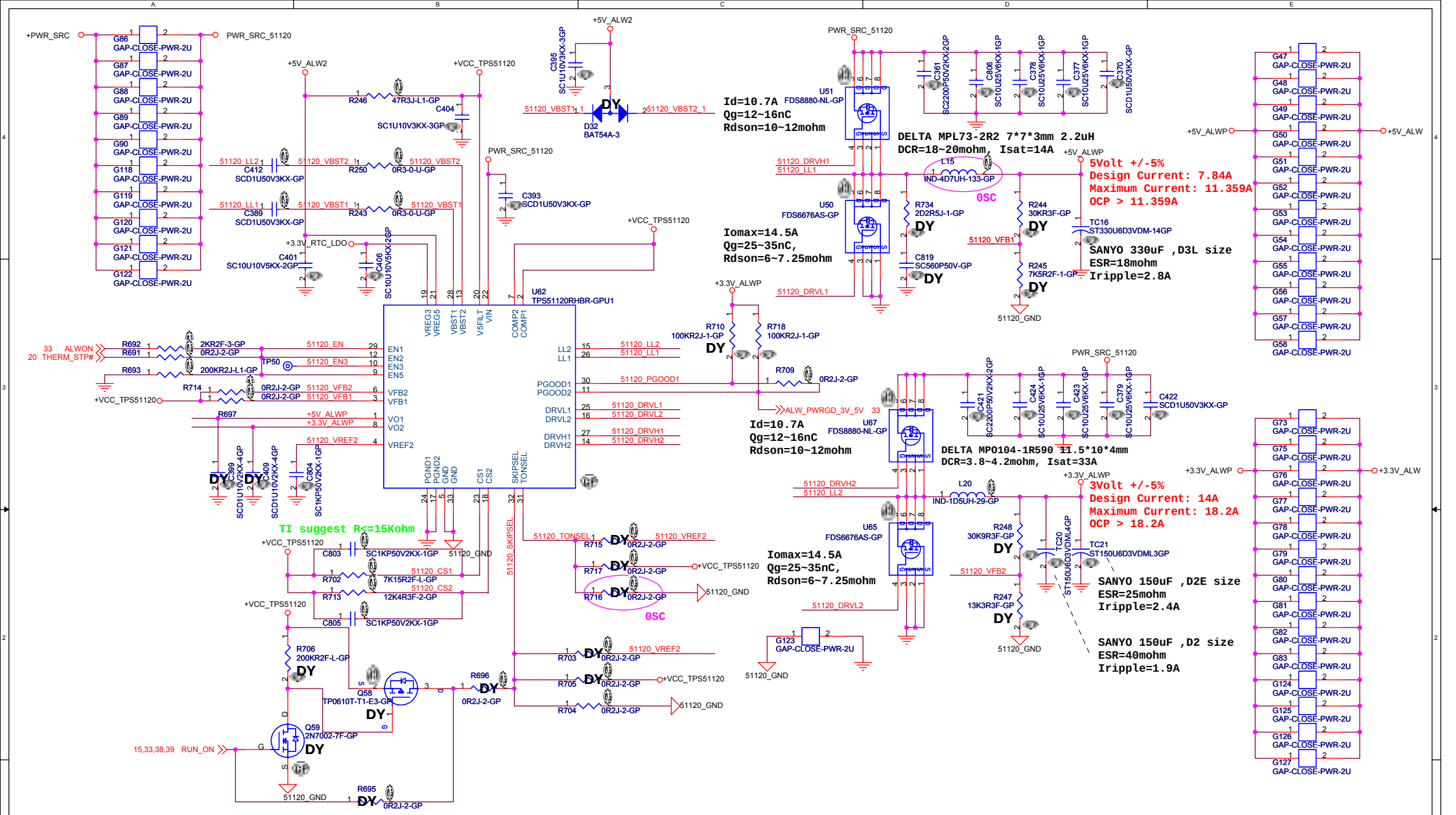

	GND	VREF2	FLOAT	VSFILT
SKIPSEL	**AUTOSKIP**	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	**D-Cap MODE**
TONSEL	380k/CH1 580k/CH2	**280k/CH1 430k/CH2**	220k/CH1 330k/CH2	180k/CH1 2870k/CH2
VFB1	N/A	not use	ADJ.	**5V Fixed Output**
VFB2	N/A	not use	ADJ.	**3.3V Fixed Output**
EN1,EN2	Switcher OFF	not use	Swithchr ON	**Switcher ON**
EN3,EN5	LDO OFF	not use	**LDO ON**	VREG3 on

Vout=1V*(R1+R2)/R2

<Core Design>

Wistron Corporation
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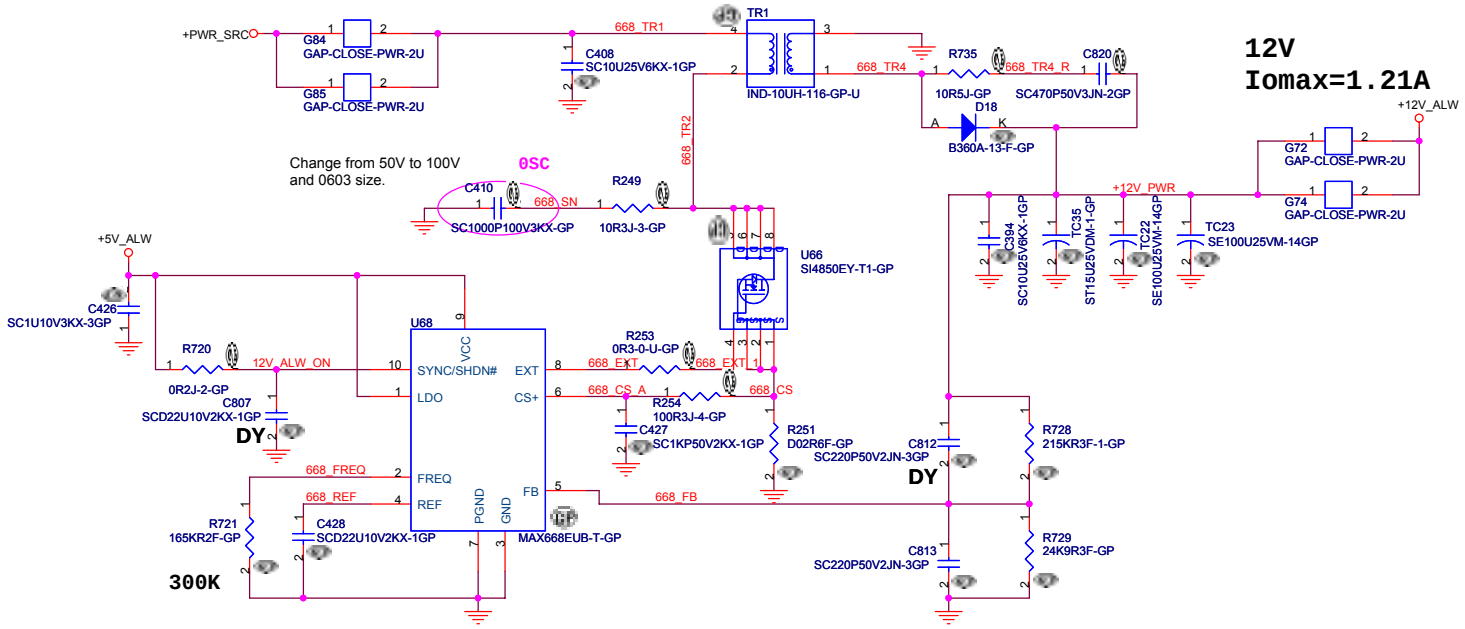
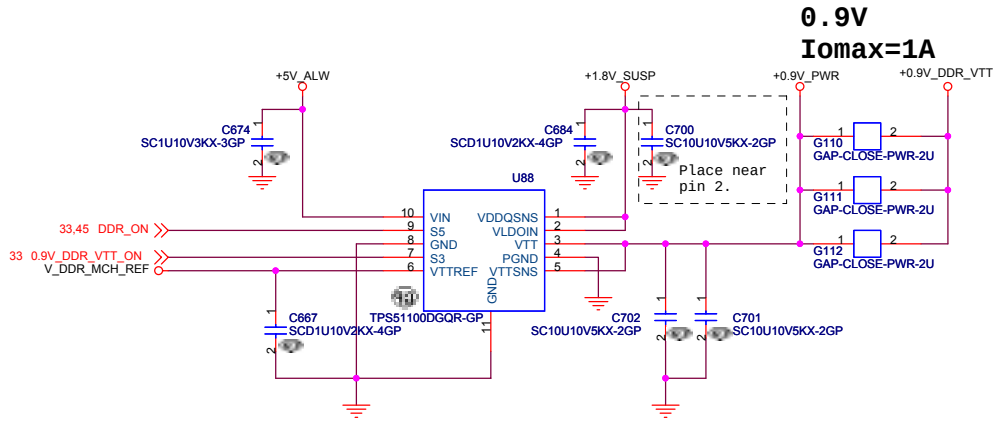
Taipei Hsien 221, Taiwan, R.O.C.

Title: *DC to DC 3.3V / 5V*

Size	Document Number	Rev
A3	Siberia	SC

Date: Friday, May 25, 2007 Sheet 46 of 50





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DC to DC 12V / 0.9V***

Size	Document Number	Rev
A3	Siberia	SC

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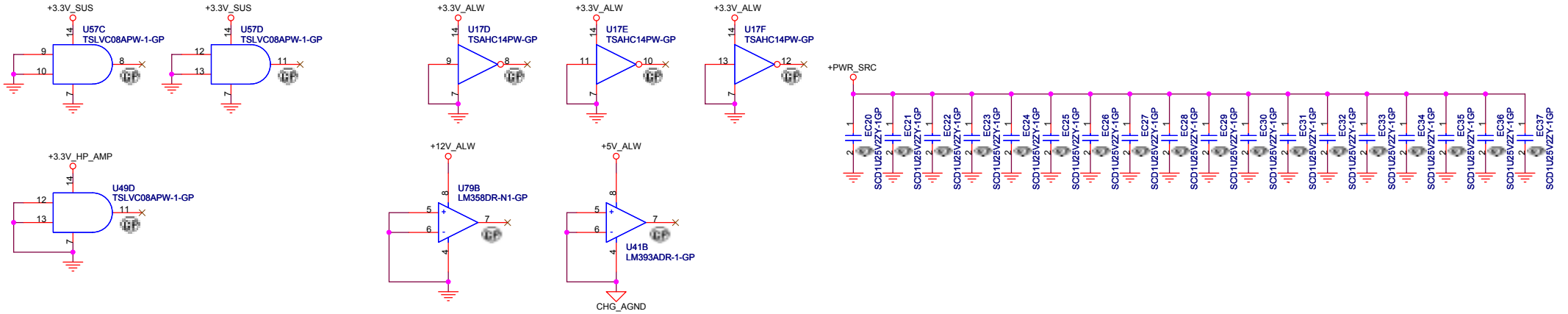

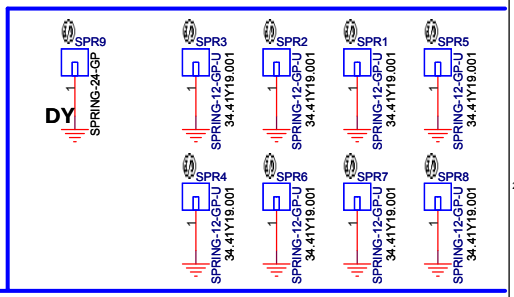

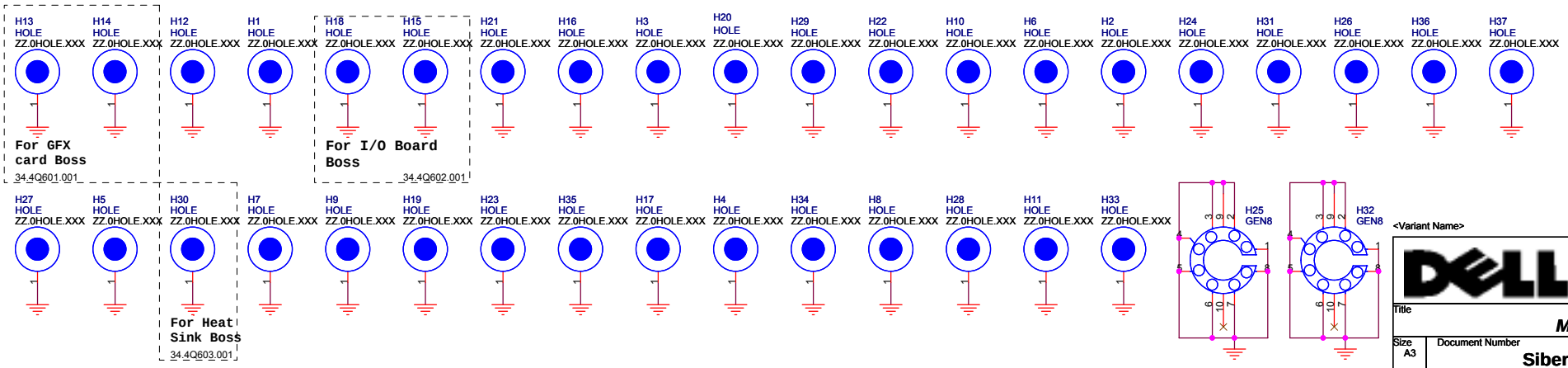

<variant_name>

Wistron Corporation
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Title: MISC & EMI

Size: A3 | Document Number: Siberia | Rev: SC

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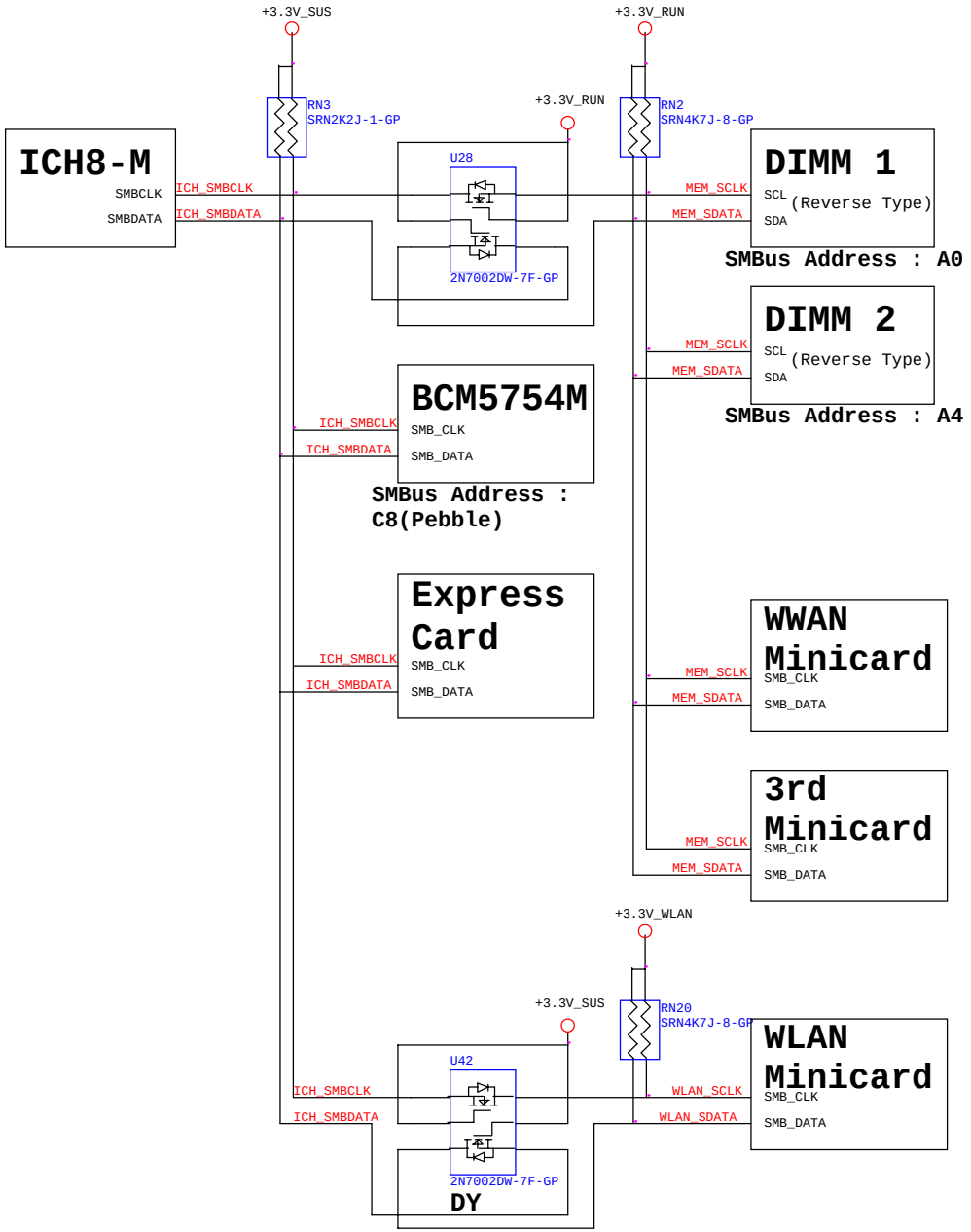
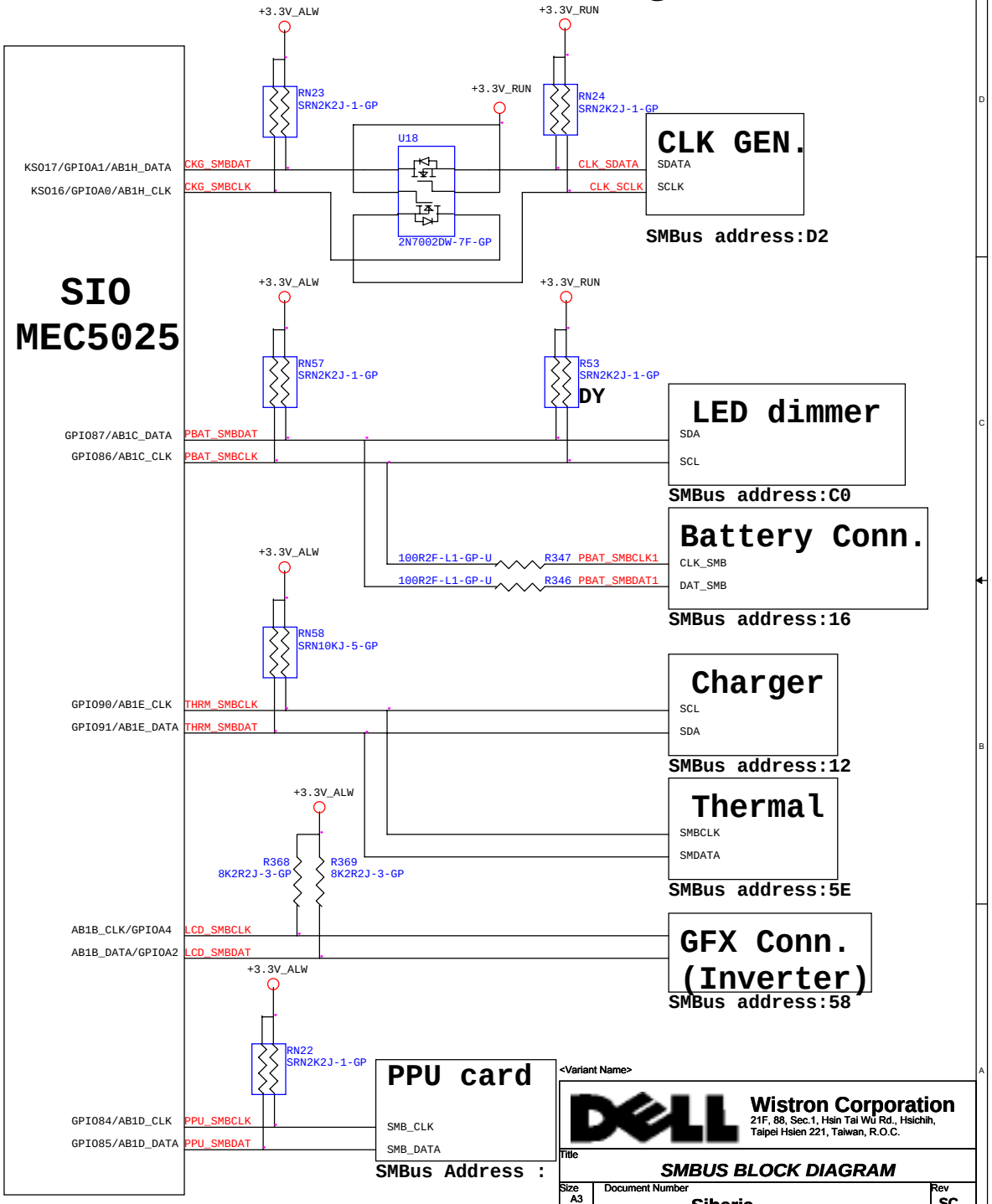
ICH8 SMBus Block Diagram



KBC SMBus Block Diagram



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SMBUS BLOCK DIAGRAM

Size	Document Number	Rev
A3	Siberia	SC

Date: Friday, May 25, 2007 Sheet 49 of 50

DATE	VERSON	ITEM	PAGE	Modify List	Issue Description	OWNER
2007/05/15	X01 to X02	1	41	Change C318 to 0.01U and change R202 to 17.8K and change R194 to 2.87K.	By power team suggestion.	Power
		2	44,45	Change TC14, TC15, TC19, TC34 to 330U.	By power team suggestion.	Power
		3	47	Change C410 to 1000P 100V 0603 size.	Change to 100V because derating is fail.	Power
		4	6,10,19	Add TP123~TP134.	For NCTF.	EE
		5	31	Change ESD1.	Vendor from Semtech to Philips inside DELL PSL.	EE
2007/05/21		6	15	Add 10K ohm resistor to GND at U81 pin1.	Dell's command for SPDIF.	EE
		7	25	Populate R712 and R708, non-populate R711 and R707.	Dell's command for AUDIO noise.	EE
		8	45	Change TC8 to 77.23371.13L.	By power team suggestion.	Power
		9	46	Change L15 to 68.4R71B.10K.	By power team suggestion.	Power
2007/05/22		10	45	Change R560 from 150K ohm to 226K ohm.	Slow down +1.05V_RUN frequency from 600KHz to 400KHz.	Power
		11	46	Non-populate R716.	Slow down +3.3V_ALW frequency from 580KHz to 330KHz, +5V_ALW frequency from 380KHz to 220KHz	Power
2007/05/23		12	25	Change C400, C413 from 0.033U to 0.047U 1206size.	Increase value of capacitor to promote audio performance.	EE
		13	27	Change R274 from 39K ohm to 0 ohm.	Change LOM supper IDDQ setting.	EE
		14	34	Non-populate R407 and R387, populate R388 and R406.	Change board ID from X01 to X02.	EE

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: HISTORY from X00 to X01

Size: A3 | Document Number: Siberia | Rev: SC

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