Compal Confidential

VIUS5 LA-9001P M/B Schematics Document

AMD FP2 Processor with DDRIII + Husdon M3 FCH
AMD VGA Seymour XT

2012-05-31

REV:0.3

Security Classification	Compal Secret Data		
Issued Date	2012/01/15	Deciphered Date	2013/01/15

Compal Electronics, Inc.		
Title: Cover Page		
Size: Custom	Document Number: VAUS5 LA9001P M/B	Rev: 0.3
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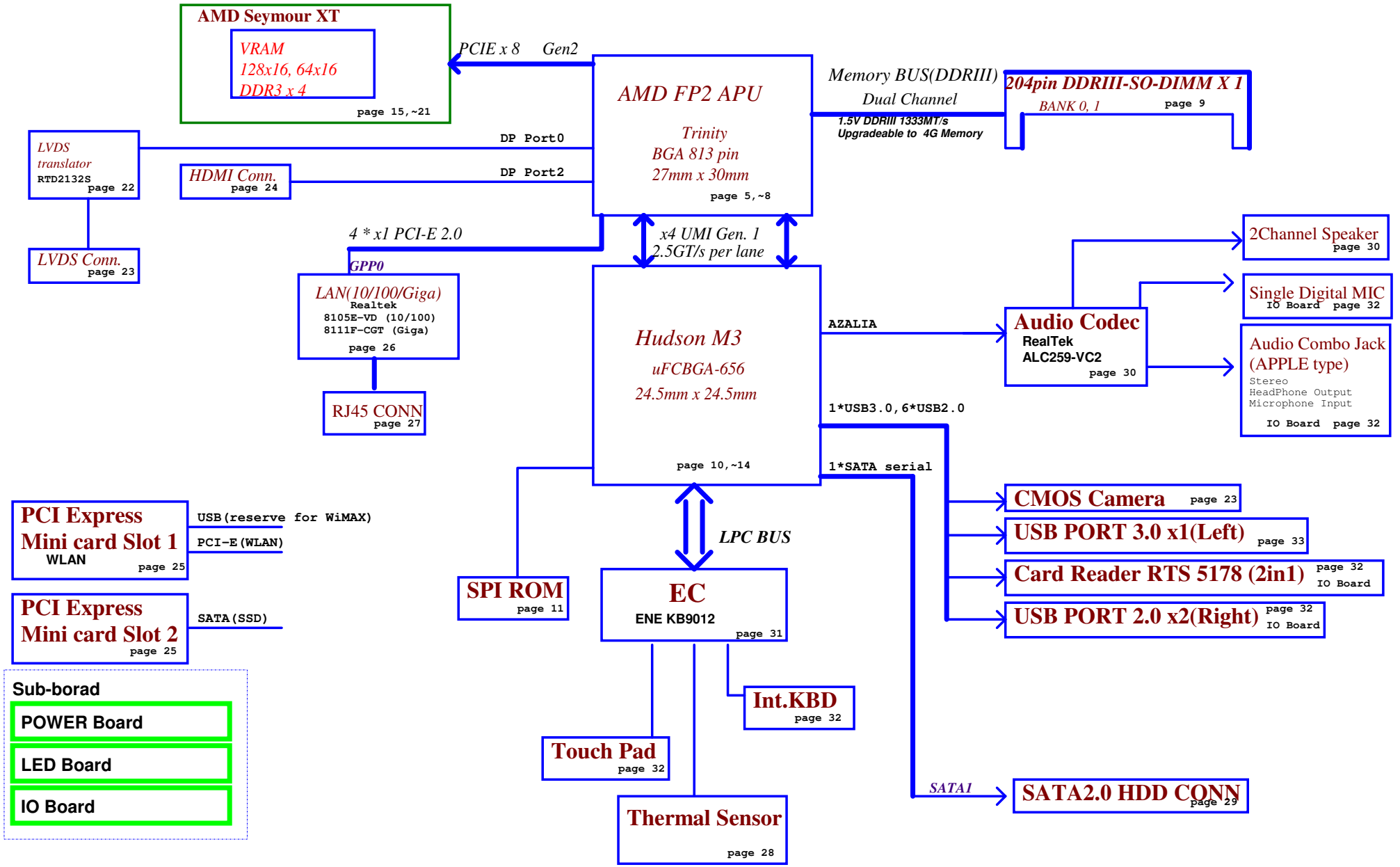

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Compal Electronics, Inc.			
Title	MB Block Diagram		
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Voltage Rails

power plane / State	+B	+5VALW +3VALW +1.1VALW	+1.5V +1.5V_APU	+5VS +3VS +2.5VS +1.5VS +1.2VS +1.1VS +0.75VS +APU_CORE +APU_CORE_NB +VGA_CORE +3.3VGS +1.8VGS +1.5VGS +1.0VGS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

SIGNAL / STATE	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	
1	0.3
2	
3	
4	
5	
6	
7	

Board ID / SKU ID Table for AD channel

ID	BRD ID	Ra	Rb	Vab
0	R10 MP	x	0	0V
1	R03 PVT	100K	8.2K	0.25V
2	R02 DVT	100K	18K	0.5V
3	R01 EVT	100K	33K	0.82V

Ra = R1562
Rb = R1564

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	FCH	APU	RTD2132
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VALW	X	V +3VALW	X	X	X	X	X	X	X
SMB_EC_CK2_SUS SMB_EC_DA2_SUS	KB9012 +3VALW	X	X	X	X	X	X	X	V +1.5V	X
FCH_SCLK0 FCH_SDATA0	FCH +3VS	X	X	X	V +3VS	V +3VS	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VS (LV shifter)	V	X	X	X	X	V	X	X	V

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor	1001_101xb
SB-TSI(default)	1001_100xb
VGA(thermal)	1000_001xb
RTD2132S	1010_1000b

FCH SM Bus address

Device	Address
DDR DIMM1	1001 000Xb

USB Port Table

USB 2.0	USB 3.0		Port	4 External USB Port
			0	USB Port (Right Side 1)
			1	USB Port (Right Side 2)
			2	Mini Card(WLAN)
			3	Camera
			4	
			5	CardReader
			6	
			7	
			8	
			9	
	XHCI	0	10	USB Port (Left Side)
		1	11	
		2	12	
		3	13	

USB OC MAPPING

OC#	USB Port	
0	USB20 port10	USB30 port0
1	USB20 port0 port1	
2		
3		

APU PCIE PORT LIST

Port	Device
1	LAN
2	WLAN
3	
4	

FCH PCIE PORT LIST

Port	Device
1	
2	
3	
4	

BOM Structure Table

BOM Structure	BTO Item
A4R1@	A4 BGA APU (R1 compal part)
A4R3@	A4 BGA APU (R3 compal part)
A6R1@	A6 BGA APU (R1 compal part)
A6R3@	A6 BGA APU (R3 compal part)
A8R1@	A8 BGA APU (R1 compal part)
A8R3@	A8 BGA APU (R3 compal part)
A10R1@	A10 BGA APU (R1 compal part)
A10R3@	A10 BGA APU (R3 compal part)
SXTR1@	Seymour XT GPU (R1 compal part)
SXTR3@	Seymour XT GPU (R3 compal part)
A70MR1@	A70 Hudson M3 FCH (R1 compal part)
A70MR3@	A70 Hudson M3 FCH (R3 compal part)
PX@	Common VGA circuit
CMOS@	CMOS Camera part
UMA@	UMA strap pin
GAS@	Gastube
8105@	RTL8105E
GIGA@	RTL8111F
HDMI@	HDMI part
NONAOAC@	No AOAC function
AOAC@	support AOAC function
ME@	ME part
DEBUG@	Debug Switch (MP will remove)
@	Unpop
SSD@	SSD part

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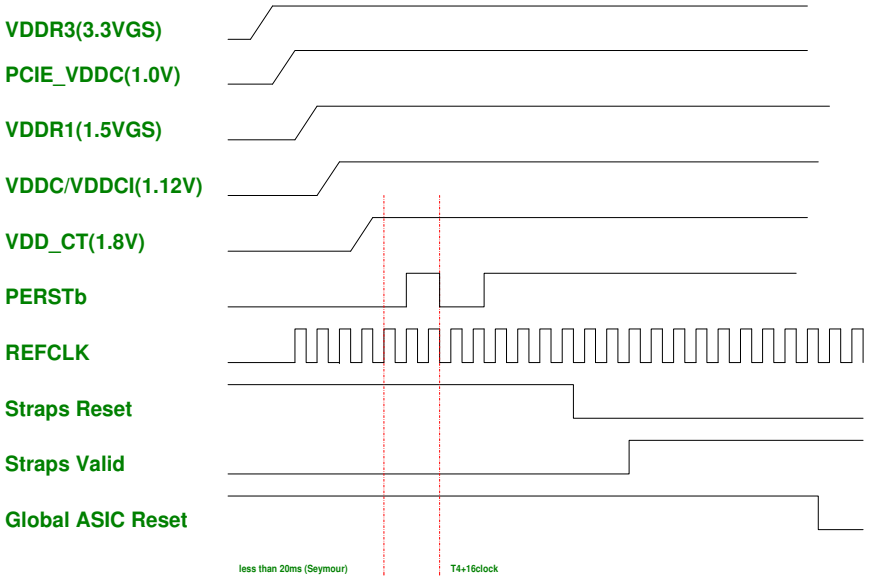
Power-Up/Down Sequence

"Thames" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies, except for VDDR3, must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. There is no timing requirement on the ramp up of VDDR3 relative to other power rails.
- The external pull-up resistors on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.
- VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa). For BACO enabled designs, VDDC must ramp up before VDD_CT at system power up.
- For power down, reversing the ramp-up sequence is recommended



Without BACO option :

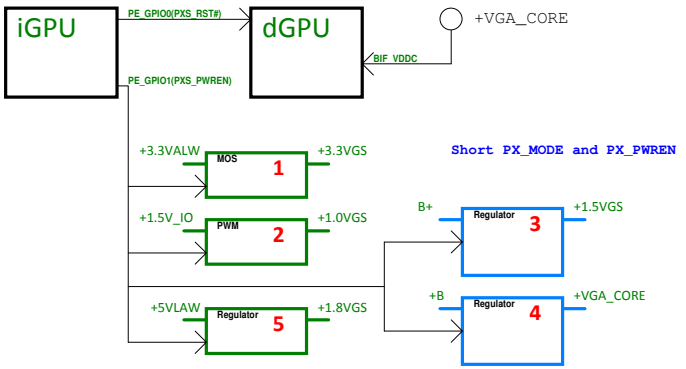
PE_GPIO0 : Low -> Reset dGPU ; High ->Normal operation
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON

BACO option :

PE_GPIO0 : High ->Normal operation (dGPU is not reset on BACO mode)
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON (always High)

dGPU Power Pins	Voltage	PX 3.0	BACO Mode	Max current
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	OFF	ON	1679mA
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	OFF	ON	775mA
PCIE_VDDC	1.0V	OFF	ON	1.1A
VDDR3	3.3V	OFF	ON	60mA
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	OFF	ON Same as PCIE_VDDC	70mA
VDDR1	1.5V	OFF	OFF	1.2A
VDDC/VDDCI	TBD	OFF	OFF	28

PX5.0



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Compal Electronics, Inc.

Title: VGA Notes List

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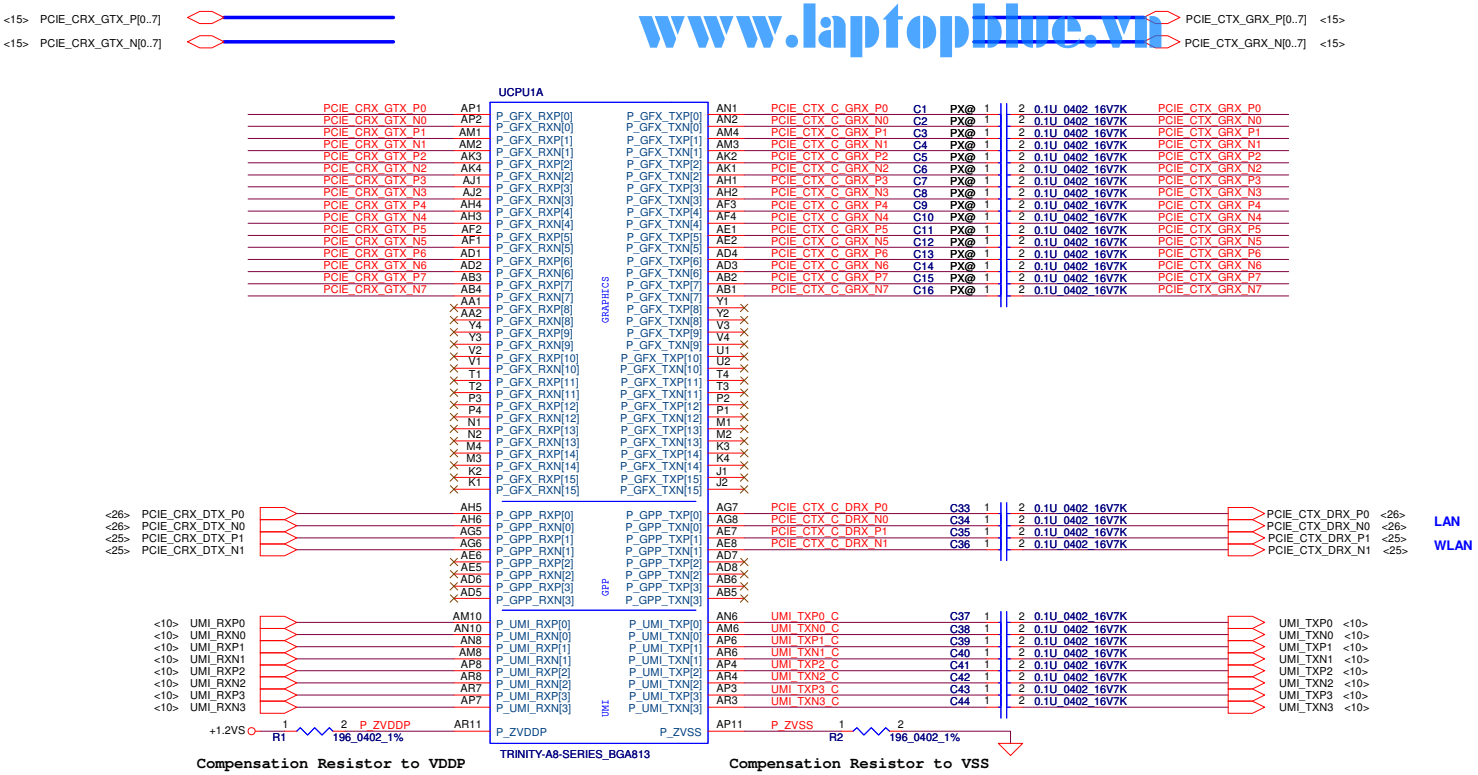
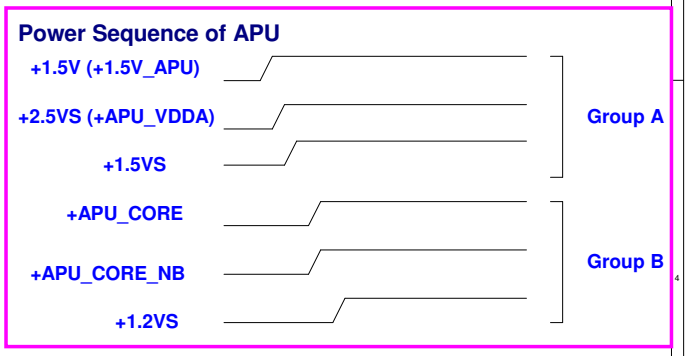


All power supplies in Power Sequencing Group A must be stable and within specification before any power supply in Power Sequencing Group B is greater than 10 percent of its specified typical operating value.

All power supplies in Power Sequencing Group B must be stable and within specification one ms before the assertion of PWROK.

No sequencing relationships are required between the power sequencing groups during S3 entry. DDR3 compatible processors require VDDIO to remain powered and within specification during the S3 sleep state. All other processor power supply planes are powered down during S3.



UCPU1 A4R3@ — A4 SERIES ZM198169E2351 1.9G BGA813
UCPU1 A6R3@ — A6 SERIES ZM212169E2451 2.1G BGA813
UCPU1 A10R3@ — A10 SERIES ZM202268E4451 2G BGA813P
ZZZ1 — LA9001P — DA60000TW00
UCPU1 A4R1@ — A4 SERIES AM4355SHE23HJ 1.9G BGA813
UCPU1 A6R1@ — A6 SERIES AM4455SHE24HJ 2.1G BGA813
UCPU1 A10R1@ — A10 SERIES AM4655SIE44HJ 2G BGA813P
UCPU1 A8R1@ — A8 SERIES AM4555SHE44HJ 1.6G BGA813

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Title: FP2 PCIE/UMI

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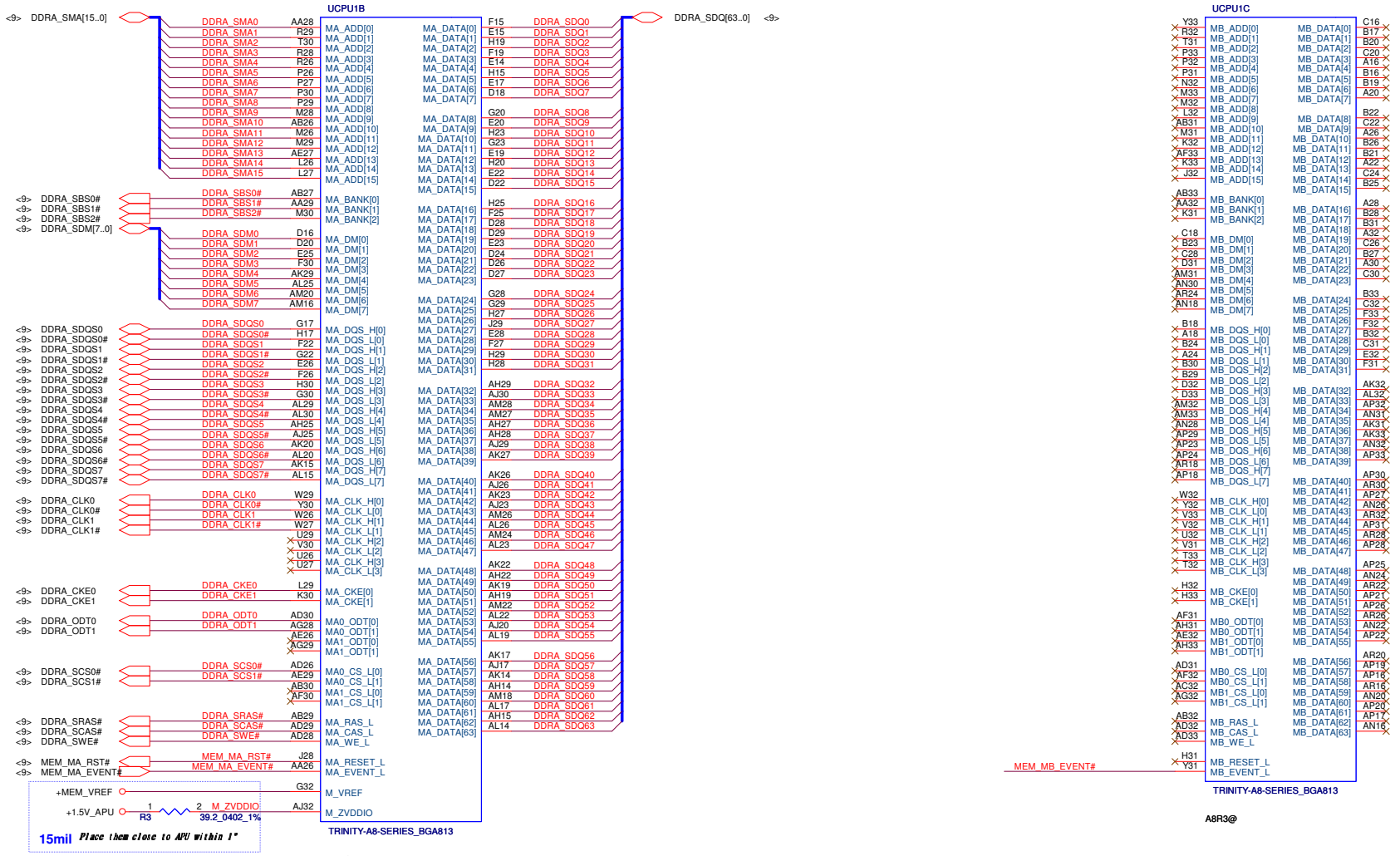
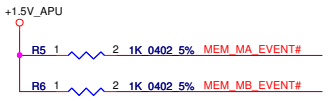
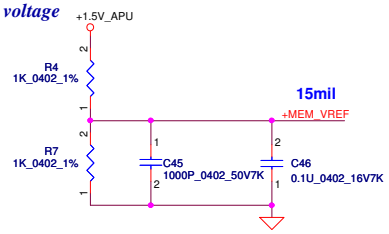


EVENT# pull high



0.75V reference voltage



Security Classification	Compal Secret Data		
Issued Date	2012/01/15	Deciphered Date	2013/01/15

Compal Electronics, Inc.			
Title: FP2 DDRIII Memory I/F			
Size: B/25 Custom	Document Number: VAUS5 LA9001P M/B		Rev: 0.3
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Place near APU

UCPU1D

LVDS

<22> DP0_TXP0_C
<22> DP0_TXN0_C

C47 1 2 0.1U_0402_16V7K DP0_TXP0
C48881 2 0.1U_0402_16V7K DP0_TXN0

DP0_TXP0 H2
DP0_TXN0 H1

DP0_TXP[0] DP0_TXN[0]
DP0_TXP[1] DP0_TXN[1]
DP0_TXP[2] DP0_TXN[2]
DP0_TXP[3] DP0_TXN[3]
DISPLAY PORT 0

DP1_TXP[0] DP1_TXN[0]
DP1_TXP[1] DP1_TXN[1]
DP1_TXP[2] DP1_TXN[2]
DP1_TXP[3] DP1_TXN[3]
DISPLAY PORT 1

DP2_TXP[0] DP2_TXN[0]
DP2_TXP[1] DP2_TXN[1]
DP2_TXP[2] DP2_TXN[2]
DP2_TXP[3] DP2_TXN[3]
DISPLAY PORT 2

DP0_AUXP M5
DP0_AUXN M3
DP1_AUXP L5
DP1_AUXN L6
DP2_AUXP J5
DP2_AUXN J6
DP3_AUXP P5
DP3_AUXN P6
DP4_AUXP R5
DP4_AUXN R6
DP5_AUXP U5
DP5_AUXN U6
DISPLAY PORT MISC.

DP0_AUXP C49 1 2 0.1U_0402_16V7K DP0_AUXP_C <22>
DP0_AUXN C5038 1 2 0.1U_0402_16V7K DP0_AUXN_C <22>

To LVDS Translater

HDMI_CLK <24>
HDMI_DATA <24>

To HDMI

DP0_HPD M7
DP1_HPD L7
DP2_HPD J7
DP3_HPD P7
DP4_HPD R7
DP5_HPD U7

LVDS_HPD <22>
HDMI_DET <24>

DP_BLON C6
DP_DIGON D7
DP_VARY_BL A6
DP_AUX_ZVSS B6

DP_INT_PWM <22>
DP_AUX_ZVSS R15 1 2 150_0402_1%

HDMI

<24> DP2_TXP0
<24> DP2_TXN0
<24> DP2_TXP1
<24> DP2_TXN1
<24> DP2_TXP2
<24> DP2_TXN2
<24> DP2_TXP3
<24> DP2_TXN3

B2 A2 B3 A3 B4 A4 B5 A5

<10> APU_CLK
<10> APU_CLK#
AL9 AK9
CLKIN_H CLKIN_L

<10> APU_DISP_CLK
<10> APU_DISP_CLK#
AL7 AK7
DISP_CLKIN_H DISP_CLKIN_L
CLK

<43> APU_SVC
<43> APU_SVD
<43> APU_SVT
E5 E6 D6
SVC SVD SVT
SER.

APU_SIC AJ11
APU_SID AH11
SIC SID

<10> APU_RST#
<10,43> APU_PWRGD
AK11 AH9
RESET_L PWROK

<10> APU_PROCHOT#
APU_THERMTRIP# AL12 AK5
ALERT_L AR10
PROCHOT_L THERMTRIP_L ALERT_L
CTRL

APU_TDI E11
APU_TDO G11
APU_TCK H12
APU_TMS F11
APU_TRST# H11
APU_DBRDY E8
APU_DBREQ# E7
TDI TDO TCK TMS TRST_L DBRDY DBREQ_L
JTAG

TEST6 Y23
TEST9 V23
TEST10 G9
TEST14 F9
TEST15 E9
TEST16 G8
TEST17 F12 APU_TEST18
TEST18 E12 APU_TEST19
TEST19 F14 APU_TEST20
TEST20 G12 APU_TEST24
TEST24 AJ8 TEST25_H
TEST25_H AH8 TEST25_L
TEST25_L G14
TEST28_H H14
TEST28_L V25
TEST30_H Y25
TEST30_L AH32 APU_TEST37
TEST31 R25
TEST32_H T25
TEST32_L AL5 APU_TEST35
TEST35
TEST

T1 T2 T3 T4 T5 T6 T7 T8 T17 T18 T19 T20 T9 T10

R17 1 2 510_0402_1%
R18 1 2 510_0402_1%
+1.2VS

R21 1 2 39.2_0402_1%

R22 1 HDMI@ 2 300_0402_5%
R23 1 @ 2 300_0402_5%
+1.5V_APU

DMAACTIVE_L AP10
ALLOW_STOP <10>

TEST4 T23
TEST5 R23

RSVD L8 P8 AH12 AJ12 AK12
RSVD

<43> APU_VDD_SEN_L G6
<43> APU_VDDNB_SEN_H H6 H5 G7
<43> APU_VDD_SEN_H G5 H7
VSS_SENSE VDDP_SENSE VDDNB_SENSE VDDIO_SENSE VDD_SENSE VDDR_SENSE
SENSE

Route as differential with APU_VDD_SEN_L

TRINITY-A8-SERIES_BGA813

A8R3@

DP0_AUXP R10 2 1 1.8K_0402_5%
DP0_AUXN R11 2 1 1.8K_0402_5%

Asserted as an input to force the processor into the HTC-active state

+1.5V_APU +3VS

R12 1K_0402_5%
R14 10K_0402_5%
R13 10K_0402_5% @

Q1 @
APU_PROCHOT#
H_PROCHOT# <31,36,43>
MMBT3904_NL_SOT23-3

R16 0_0402_5%

THERMTRIP shutdown temperature: 125 degree

Indicates to the FCH that a thermal trip has occurred. Its assertion will cause the FCH to transition the system to S5 immediately

+1.5V_APU

R19 1K_0402_5%
R20 10K_0402_5%

Q2
APU_THERMTRIP#
MMBT3904_NL_SOT23-3

R24 0_0402_5%
H_THERMTRIP# <12>

@R25 0_0402_5%
MAINPWON <31,36,38>

+1.5V_APU

R215 1 2 1K_0402_5% ALLOW_STOP
R26 1 2 1K_0402_5% APU_SIC
R28 1 2 1K_0402_5% APU_SID
R31 1 2 1K_0402_5% ALERT_L

+1.5VS

R36 1 @ 2 1K_0402_5% ALLOW_STOP
R38 1 2 300_0402_5% APU_RST#
R40 1 2 300_0402_5% APU_PWRGD
R45 1 @ 2 1K_0402_5% APU_SVT
R48 1 @ 2 1K_0402_5% APU_SVC
R50 1 @ 2 1K_0402_5% APU_SVD

CPU TSI interface level shift

C5988 1 2 0.1U_0402_16V4Z

+3VS
R32 1 2 31.6K_0402_1%
R33 1 2 30K_0402_1%

Q3
APU_SID
BSH111 1N_SOT23-3
EC_SMB_DA2_SUS <31>
To EC

Q4
APU_SIC
BSH111 1N_SOT23-3
EC_SMB_CK2_SUS <31>
To EC

BSH111, the Vgs is:
min = 0.4V
Max = 1.3V

HDT Debug conn

+1.5V_APU

JHDT1
SAMTE_ASP-136446-07-B
@

APU_TCK
APU_TMS
APU_TDI
APU_TDO
APU_PWRGD
APU_RST#
APU_DBRDY
APU_DBREQ#
APU_TRST#

R42 1 2 10K_0402_5%
R46 1 2 10K_0402_5%
R49 1 2 10K_0402_5%

R51 2 @ 1 0_0402_5% APU_TEST19
R52 2 @ 1 0_0402_5% APU_TEST18

+1.5V_APU

APU_DBREQ# R27 1 2 1K_0402_5%
APU_TCK R29 1 2 1K_0402_5%
APU_TMS R30 1 2 1K_0402_5%
APU_TDI R34 1 2 1K_0402_5%
APU_TDO R35 1 @ 2 1K_0402_5%
APU_TRST# R37 1 2 1K_0402_5%

APU_TEST18 R39 1 2 1K_0402_5%
APU_TEST19 R41 1 2 1K_0402_5%
APU_TEST20 R43 1 2 1K_0402_5%
APU_TEST24 R44 1 2 1K_0402_5%
APU_DBRDY R47 1 @ 2 1K_0402_5%

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: FP2 Display/MISC/HDT

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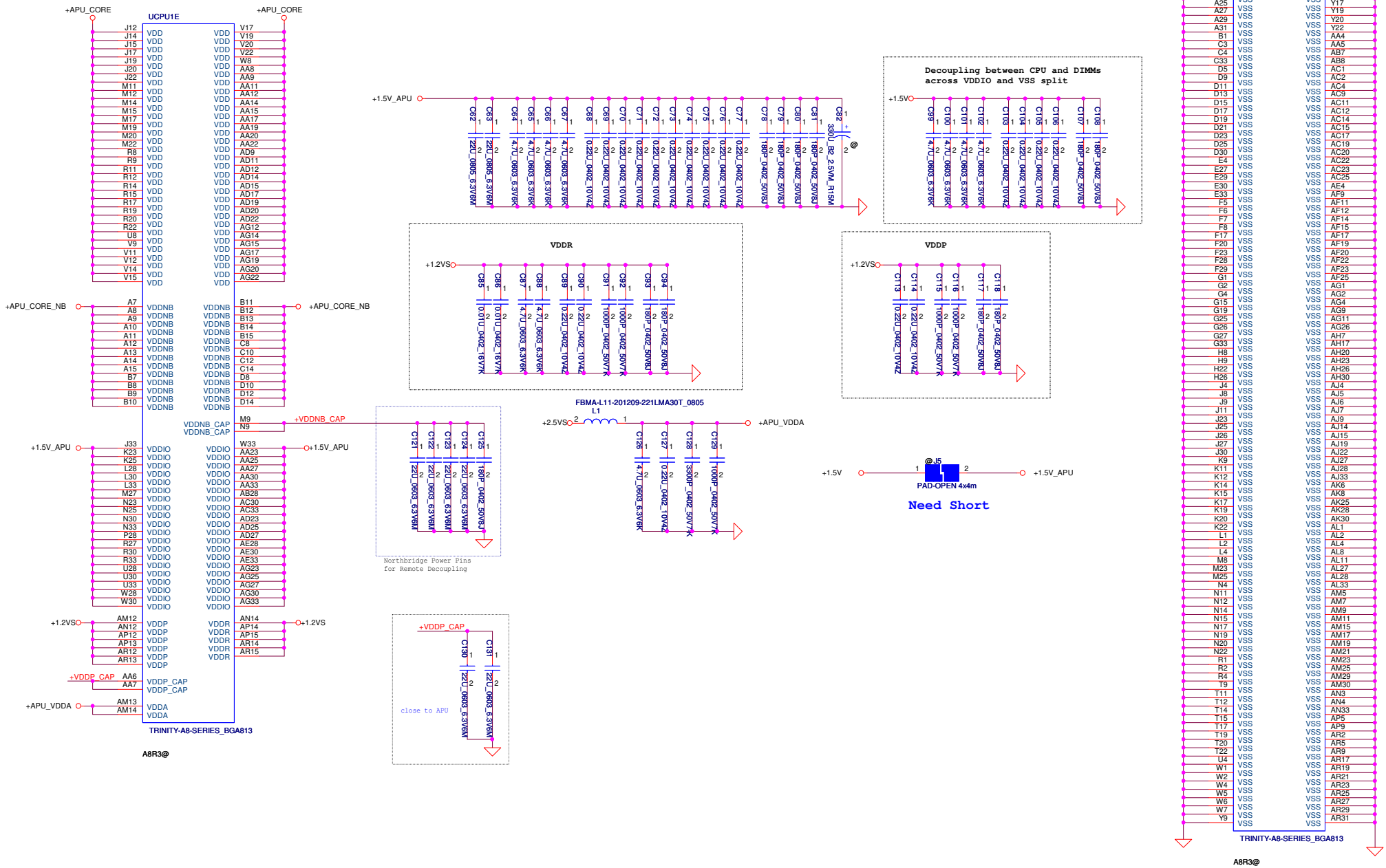

Security Classification	Compal Secret Data		
Issued Date	2012/01/15	Deciphered Date	2013/01/15

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Title	FP2 PWR / GND
Size: B2S Custom	Document Number: VAUS5 LA9001P M/B
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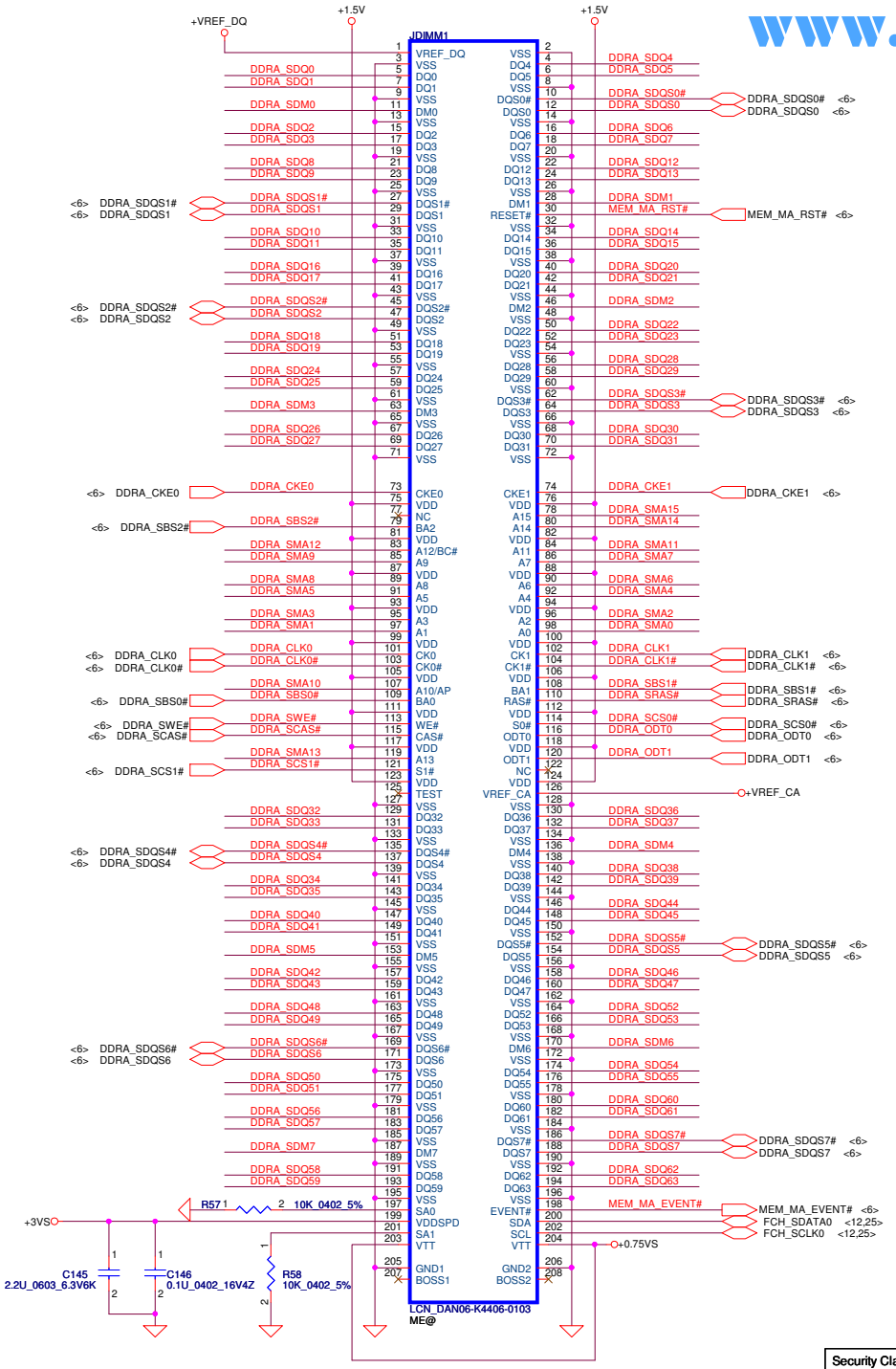
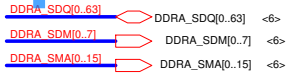
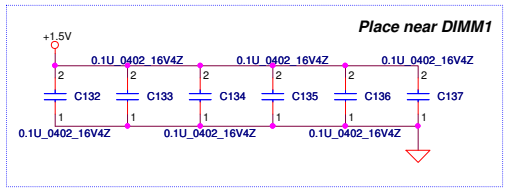
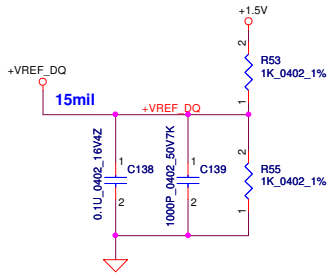
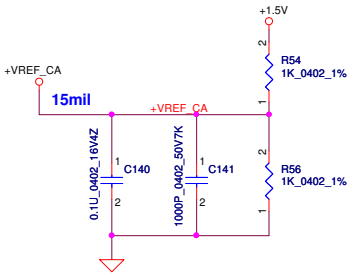
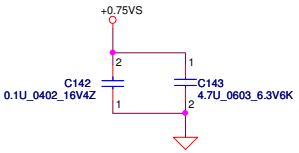


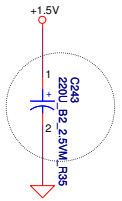












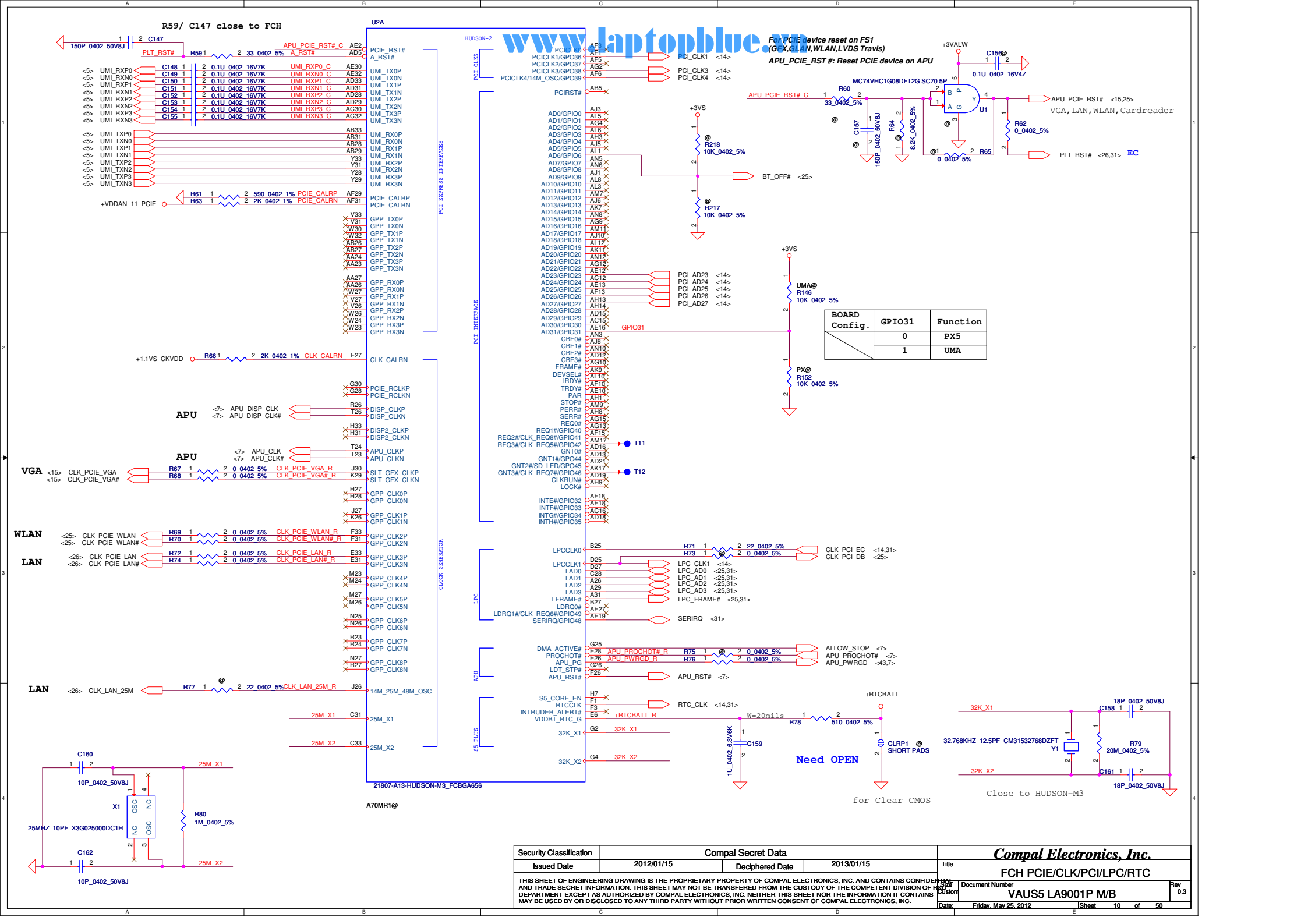
SGA00001700

Reverse Type H:4mm

<Address: 00>

Security Classification	Compal Secret Data		
Issued Date	2012/01/15	Deciphered Date	2013/01/15

Compal Electronics, Inc.			
Title	DDRIII SO-DIMM 1		
Size Custom	Document Number VAUS5 LA9001P M/B		Rev 0.3
Date: Friday, May 25, 2012	Sheet 9 of 50		



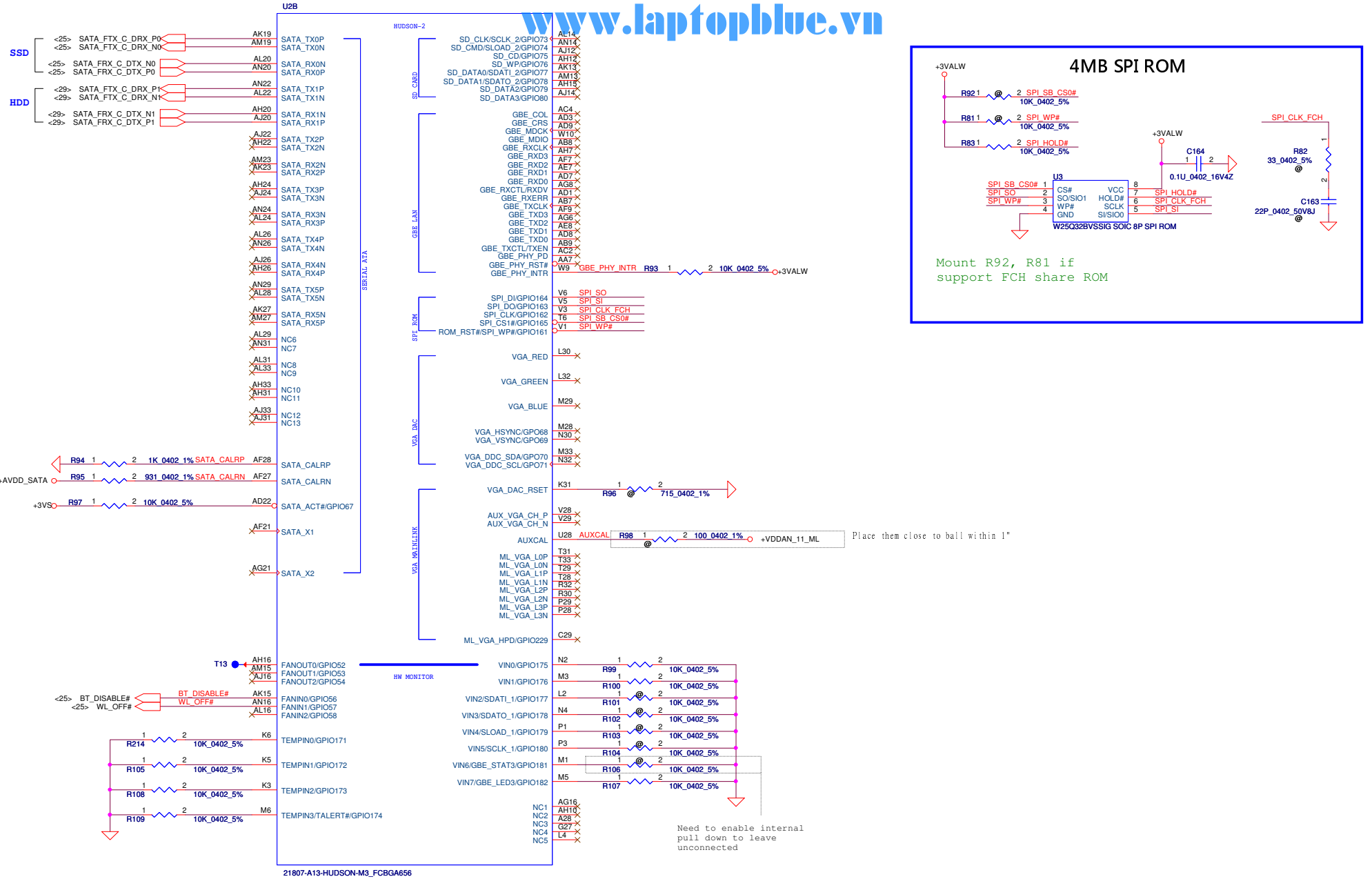
Security Classification	Compal Secret Data		
Issued Date	2012/01/15	Deciphered Date	2013/01/15

Compal Electronics, Inc.

Title: FCH PCIE/CLK/PCI/LPC/RTC

Size: Custom | Document Number: VAUS5 LA9001P M/B | Rev: 0.3

Date: Friday, May 25, 2012 | Sheet 10 of 50



Security Classification	Compal Secret Data		
Issued Date	2012/01/15	Deciphered Date	2013/01/15

Compal Electronics, Inc.

Title: FCH SATA/SPI/VGA/HWM/SD

Size: Custom | Document Number: VAUS5 LA9001P M/B | Rev: 0.3

Date: Friday, May 25, 2012 | Sheet 11 of 50

PCIE_RST2 : Reset PCIE device on Hudson2/3

U2D

+3VALW
R110 10K_0402_5% @ SYS_RESET#

+3VALW For FCH internal debug use
R114 1 @ 2 2.2K 0402 5% TEST0
R115 1 @ 2 2.2K 0402 5% TEST1
R116 1 @ 2 2.2K 0402 5% TEST2

+3VALW
R119 1 2 10K_0402_5% USB_OC0#
R121 1 2 10K_0402_5% USB_OC1#
R122 1 @ 2 10K_0402_5% USB_OC2#
R123 1 @ 2 10K_0402_5% USB_OC3#
R124 1 @ 2 10K_0402_5% USB_OC5#
R127 1 @ 2 10K_0402_5% USB_OC4#
R128 1 @ 2 10K_0402_5% USB_OC6#
R130 1 @ 2 10K_0402_5% USB_OC7#
R132 1 @ 2 10K_0402_5% H_THERMTRIP#
R133 1 @ 2 100K_0402_5% EC_LID_OUT#
R134 1 @ 2 10K_0402_5% FCH_PCIE_WAKE#
R148 1 2 2.2K_0402_5% FCH_SCLK1
R149 1 2 2.2K_0402_5% FCH_SDATA1

+3VS
R141 1 2 2.2K_0402_5% FCH_SCLK0
R142 1 2 2.2K_0402_5% FCH_SDATA0
R143 1 2 10K_0402_5% WD_PWRGD
R144 1 2 8.2K_0402_5% WLAN_CLKREQ#
R145 1 2 8.2K_0402_5% LAN_CLKREQ#
R150 1 2 2.2K_0402_5% EC_RSMRST#
R151 1 @ 2 10K_0402_5% HDA_BITCLK
R154 1 @ 2 10K_0402_5% HDA_SDIN0
R155 1 2 10K_0402_5% PEG_CLKREQ#_R
change back to always mount

<31> EC_LID_OUT# → T14
<31> PM_SLP_S3# → W2
<31> PM_SLP_S5# → J4
<31> PBTN_OUT# → N7 (FCH_PWRGD)
<31,43> FCH_PWRGD
TEST0 T9, TEST1 T10, TEST2 V9
<31> GATEA20 → AE22
<31> KBRST# → AG19
<31> EC_SCI# → R9
<31> EC_SMI# → C26
SYS_RESET# → T5
<25,26> FCH_PCIE_WAKE# → U4
<7> H_THERMTRIP# → K1
WD_PWRGD → V7
<31> EC_RSMRST# → R10
<26> LAN_CLKREQ# → AF19
<30> FCH_SPKR → U2
<25,9> FCH_SCLK0 → AG24
<25,9> FCH_SDATA0 → AE24
<32> FCH_SCLK1 → AE26
<32> FCH_SDATA1 → AF22
<25> WLAN_CLKREQ# → AH17
<15,42> VGA_PWRGD → AG18
<16> PEG_CLKREQ# → R117 2 @ 1 0_0402_5% PEG_CLKREQ#_R → AF24
change back to @
USB_OC7# M7, USB_OC6# R8, USB_OC5# T1, USB_OC4# P6, USB_OC3# F5, USB_OC2# P5, USB_OC1# J7, USB_OC0# T8
<32> USB_OC1#
<33> USB_OC0#
<30> HDA_BITCLK_AUDIO → R125 33_0402_5% HDA_BITCLK → AB3
<30> HDA_SDOUT_AUDIO → R126 33_0402_5% HDA_SDOUT → AB1
<30> HDA_SDIN0 → HDA_SDIN0 → AA2
<30> HDA_SYNC_AUDIO → R129 33_0402_5% HDA_SYNC → Y5
<30> HDA_RST_AUDIO# → R131 33_0402_5% HDA_RST# → AD6
T15 → K19
T16 → J19
J21
<40> DDR3L_EN# → PX@ 0_0402_5% R153 → D21
<15> PXS_RST# → 0_0402_5% R136 → C20
<17,39,42> PXS_PWREN → 0_0402_5% R138 → D23
PX@ 0_0402_5% R147 @ → C22
<31> VGA_GATE# → PX@ Q6 2N7002K_SOT23-3
F21, E20, F20, A22, E18, A20, J18, H18, G18, B21, K18, D19, A18, C18, B19, B17, A24, D17

+3VALW
R112 @ 10K_0402_5%
FCH_SEL
R113 @ 10K_0402_5%

AMD only support FP2 + A70M3,
@ FCH_SEL function

FCH Chip	FCH_SEL
A60M2	Low
A70M3	High

Before setting (for reference)

21807-A13-HUDSON-M3_FCBGA656
A70MR1@

USBCLK/14M_25M_48M_OSC → G8
USB_RCOMP → B9 R111 1 2 11.8K_0402_1%
USB_FSD1P/GPIO186 → H1
USB_FSD1N → H3
USB_FSD0P/GPIO185 → H6
USB_FSD0N → H5
USB_HSD13P → H10
USB_HSD13N → G10
USB_HSD12P → K10
USB_HSD12N → J12
USB_HSD11P → G12
USB_HSD11N → F12
USB_HSD10P → K12 USB30_P10
USB_HSD10N → K13 USB30_N10
USB_HSD9P → B11
USB_HSD9N → D11
USB_HSD8P → E10
USB_HSD8N → F10
USB_HSD7P → C10 USB20_P7
USB_HSD7N → A10 USB20_N7
USB_HSD6P → H9
USB_HSD6N → G9
USB_HSD5P → A8
USB_HSD5N → C8
USB_HSD4P → F8
USB_HSD4N → E8
USB_HSD3P → C6
USB_HSD3N → A6
USB_HSD2P → C5
USB_HSD2N → A5
USB_HSD1P → C1
USB_HSD1N → C3
USB_HSD0P → E1
USB_HSD0N → E3
USBSS_CALRP → C16 USBSS_CALRP R118 1 2 1K_0402_1%
USBSS_CALRN → A16 USBSS_CALRN R120 1 2 1K_0402_1%
+FCH_VDD_11_SSUSB_S
USB_SS_TX3P → A14
USB_SS_TX3N → C14
USB_SS_RX3P → C12
USB_SS_RX3N → A12
USB_SS_TX2P → D15
USB_SS_TX2N → B15
USB_SS_RX2P → E14
USB_SS_RX2N → F14
USB_SS_TX1P → F15
USB_SS_TX1N → G15
USB_SS_RX1P → H13
USB_SS_RX1N → G13
USB_SS_TX0P → J16 USB30_TX_P0
USB_SS_TX0N → H16 USB30_TX_N0
USB_SS_RX0P → J15 USB30_RX_P0
USB_SS_RX0N → K15 USB30_RX_N0
USB30_TX_P0 <33>
USB30_TX_N0 <33>
USB30_RX_P0 <33>
USB30_RX_N0 <33>

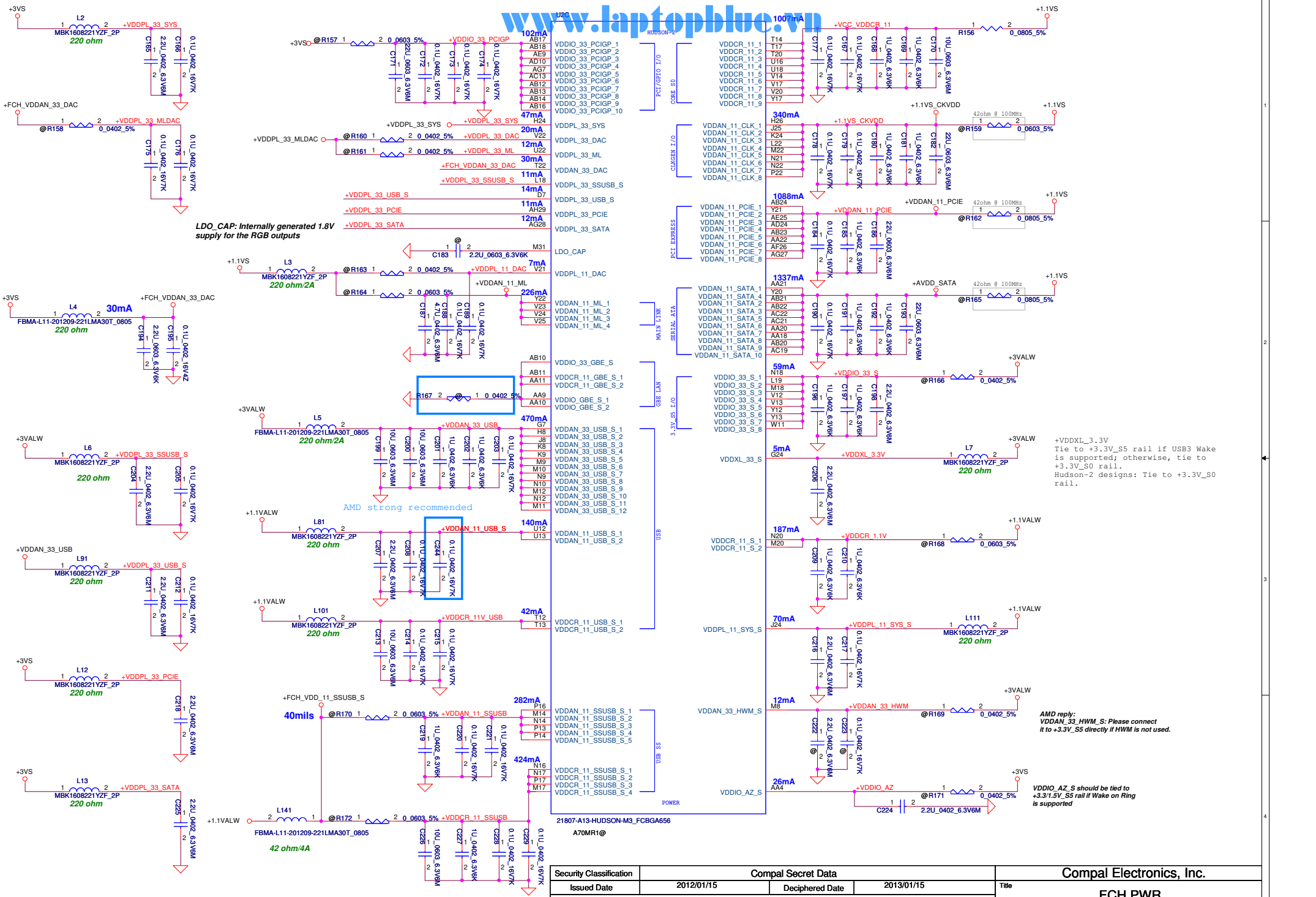
Hudson-M3 OHCI(DEV-20,FUN-5)
Hudson-M3 XHCI(DEV-16,FUN-0) XHCI(DEV-16,FUN-1)
USB30-Left1
Hudson-M3 OHCI(DEV-19,FUN-0) EHCI(DEV-19,FUN-2)
USB20-Left1
Card Reader
Hudson-M3 OHCI(DEV-18,FUN-0) EHCI(DEV-18,FUN-2)
Int. Camera
WLAN
USB20-Right2
USB20-Right1
<Support Wakeup>
Hudson-M3 XHCI(DEV-16,FUN-0) XHCI(DEV-16,FUN-1)
USB30-Left1
USB3.0 and USB2.0 Option

PS2_DAT/SDA4/GPIO187
PS2_CLK/CEC/SCL4/GPIO188
SPI_CS2#/GBE_STAT2/GPIO166
PS2KB_DAT/GPIO189
PS2KB_CLK/GPIO190
PS2M_DAT/GPIO191
PS2M_CLK/GPIO192
EMBEDDED CTRL
SCL2/GPIO193 → H19 R135 1 2 10K_0402_5%
SDA2/GPIO194 → G19 R137 1 2 10K_0402_5%
SCL3_LV/GPIO195 → G22 R139 1 2 10K_0402_5%
SDA3_LV/GPIO196 → G21 R140 1 2 10K_0402_5%
EC_PWM0/EC_TIMER0/GPIO197 → E22
EC_PWM1/EC_TIMER1/GPIO198 → H22
EC_PWM2/EC_TIMER2/WOL_EN/GPIO199 → J22 EC_PWM2
EC_PWM3/EC_TIMER3/GPIO200 → H21
EC_PWM2 <14> strap pin
KSI_0/GPIO201 → K21 FCH_SEL
KSI_1/GPIO202 → K22
KSI_2/GPIO203 → F22
KSI_3/GPIO204 → F24
KSI_4/GPIO205 → E24
KSI_5/GPIO206 → B23
KSI_6/GPIO207 → C24
KSI_7/GPIO208 → F18
KSO_0/GPIO209
KSO_1/GPIO210
KSO_2/GPIO211
KSO_3/GPIO212
KSO_4/GPIO213
KSO_5/GPIO214
KSO_6/GPIO215
KSO_7/GPIO216
KSO_8/GPIO217
KSO_9/GPIO218
KSO_10/GPIO219
KSO_11/GPIO220
KSO_12/GPIO221
KSO_13/GPIO222
KSO_14/GPIO223
KSO_15/GPIO224
KSO_16/GPIO225
KSO_17/GPIO226

Left USB port 3.0 & 2.0 co-lay
USB20_N7 → R1606 @ 0_0402_5%
USB20_P7 → R1607 @ 0_0402_5%
USB30_N10 → R1610 0_0402_5% → USB20_LN → USB20_LN <33>
USB30_P10 → R1611 0_0402_5% → USB20_LP → USB20_LP <33>

Security Classification	Compal Secret Data		
Issued Date	2012/01/15	Deciphered Date	2013/01/15

Compal Electronics, Inc.
Title: FCH-ACPI/USB/HDA/GPIO
Size: B2S Custom
Document Number: VAUS5 LA9001P M/B
Rev: 0.3
Date: Friday, May 25, 2012
Sheet 12 of 50



Security Classification	Compal Secret Data		
Issued Date	2012/01/15	Deciphered Date	2013/01/15

Compal Electronics, Inc.

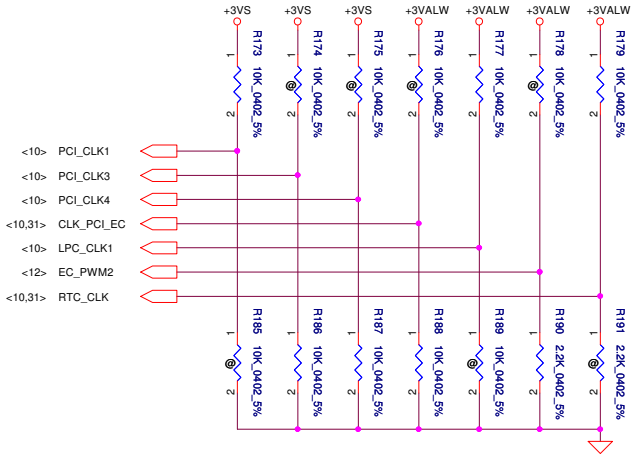
Title: FCH PWR

Size: Custom | Document Number: VAUS5 LA9001P M/B | Rev: 0.3

Date: Friday, May 25, 2012 | Sheet 13 of 50

STRAP PINS

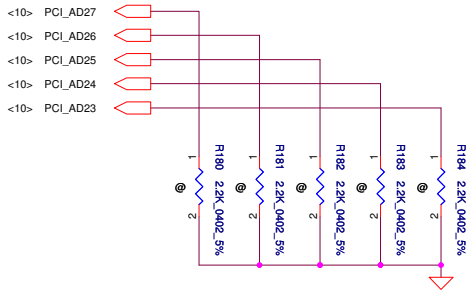
	PCI_CLK1	PCI_CLK3	PCI_CLK4	CLK_PCI_EC	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

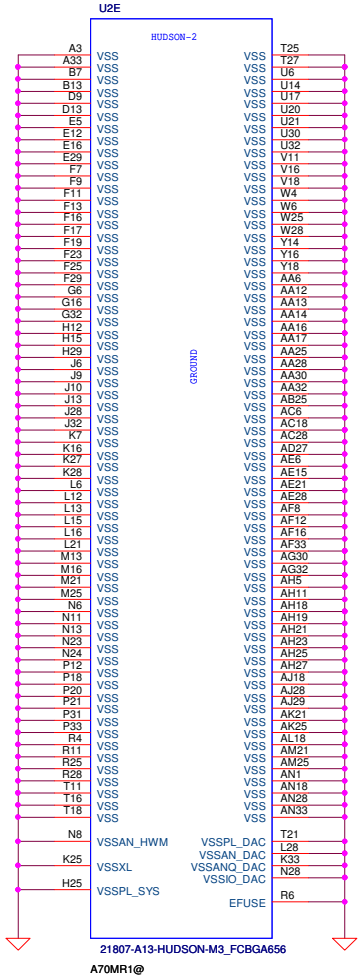


DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

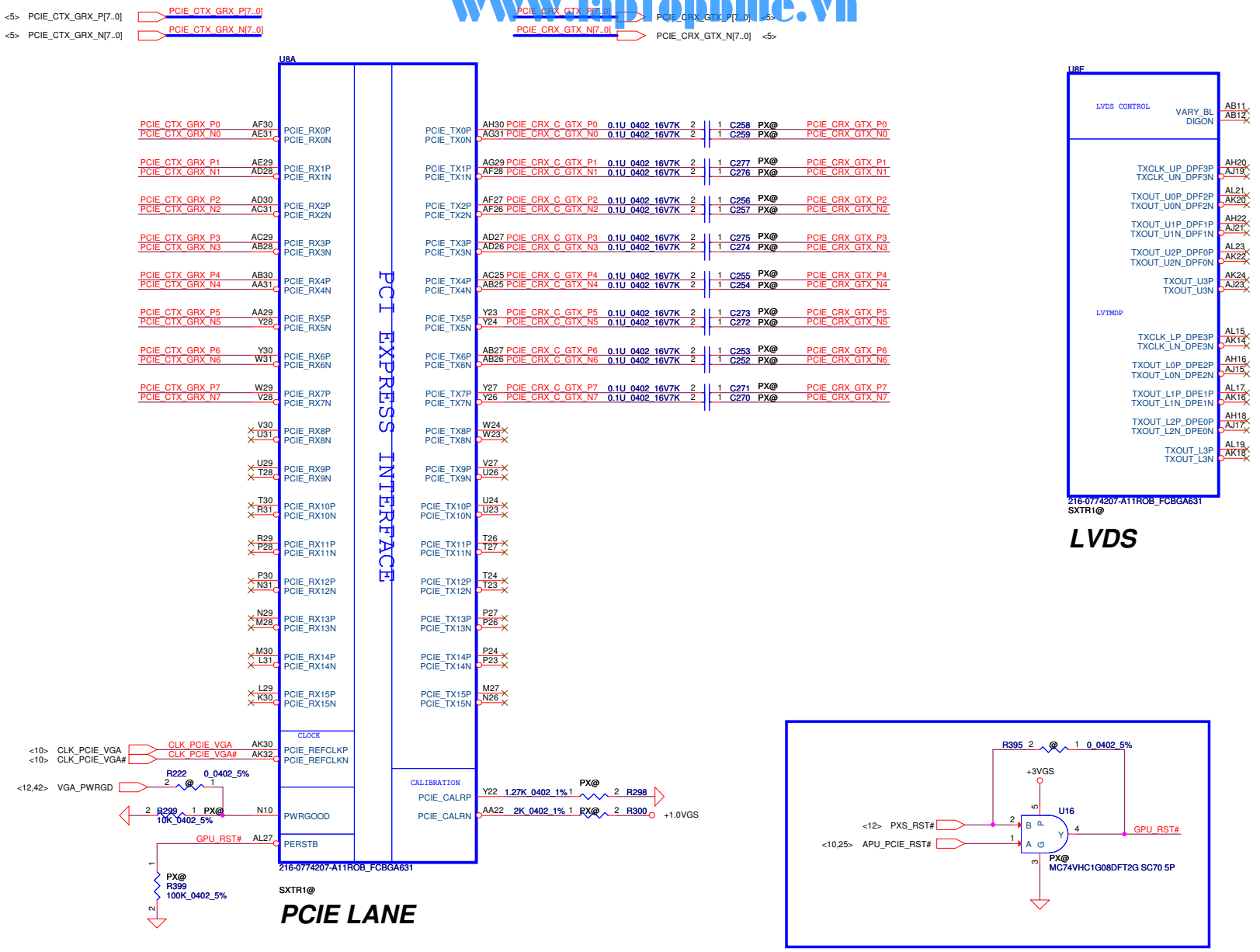
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT





Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/01/15	Deciphered Date 2013/01/15	Title: FCH-VSS/Strap

Size: D Custom	Document Number: VAUS5 LA9001P M/B		Rev: 0.3
Date: Friday, May 25, 2012	Sheet 14 of 50		



U8 SXTR3@

S IC 216-0809024 A11 SEYMOUR XT S3 C38!

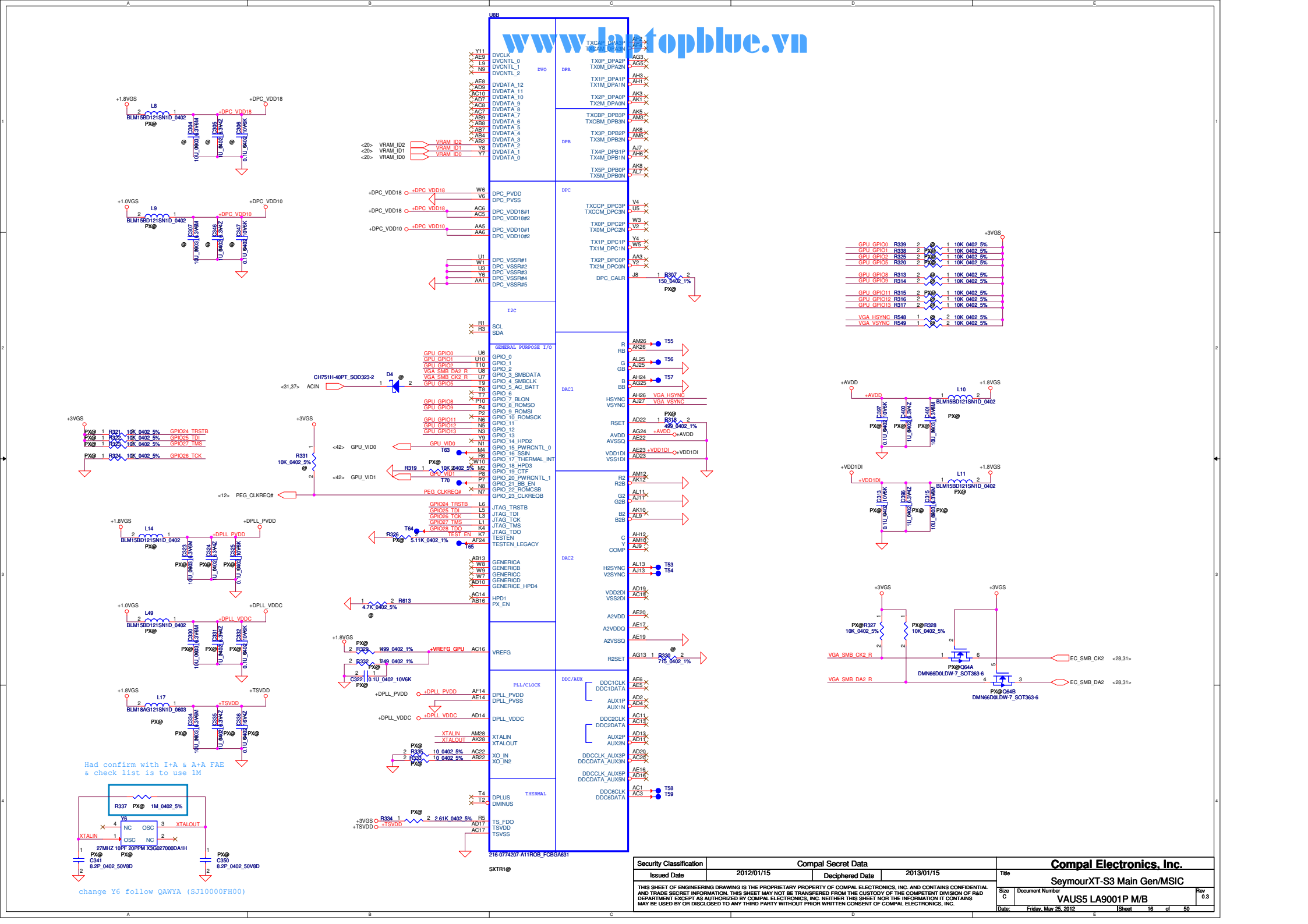
Security Classification	Compal Secret Data		
Issued Date	2012/01/15	Deciphered Date	2013/01/15

Compal Electronics, Inc.

Title: SeymourXT-S3 PCIE/LVDS

Size: Custom | Document Number: VAUS5 LA9001P M/B | Rev: 0.3

Date: Friday, May 25, 2012 | Sheet 15 of 50



Security Classification	Compal Secret Data		
Issued Date	2012/01/15	Deciphered Date	2013/01/15

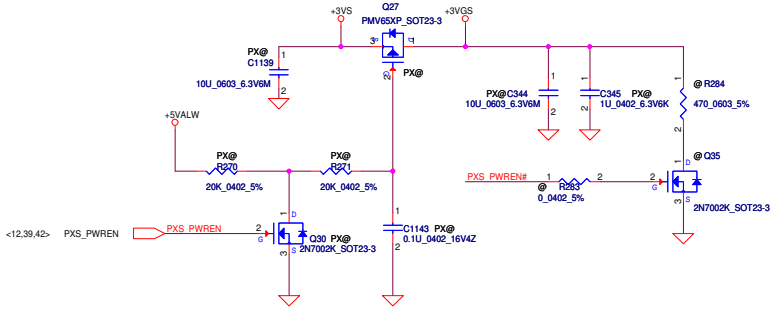
Compal Electronics, Inc.

Title: SeymourXT-S3 Main Gen/MSIC

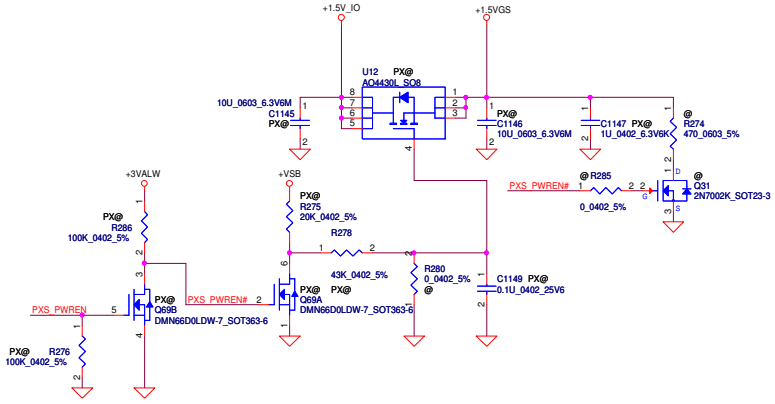
Size	Document Number	Rev
C	VAUS5 LA9001P M/B	0.3

Date: Friday, May 25, 2012 Sheet 16 of 50

+3.3VS TO +3.3VGS



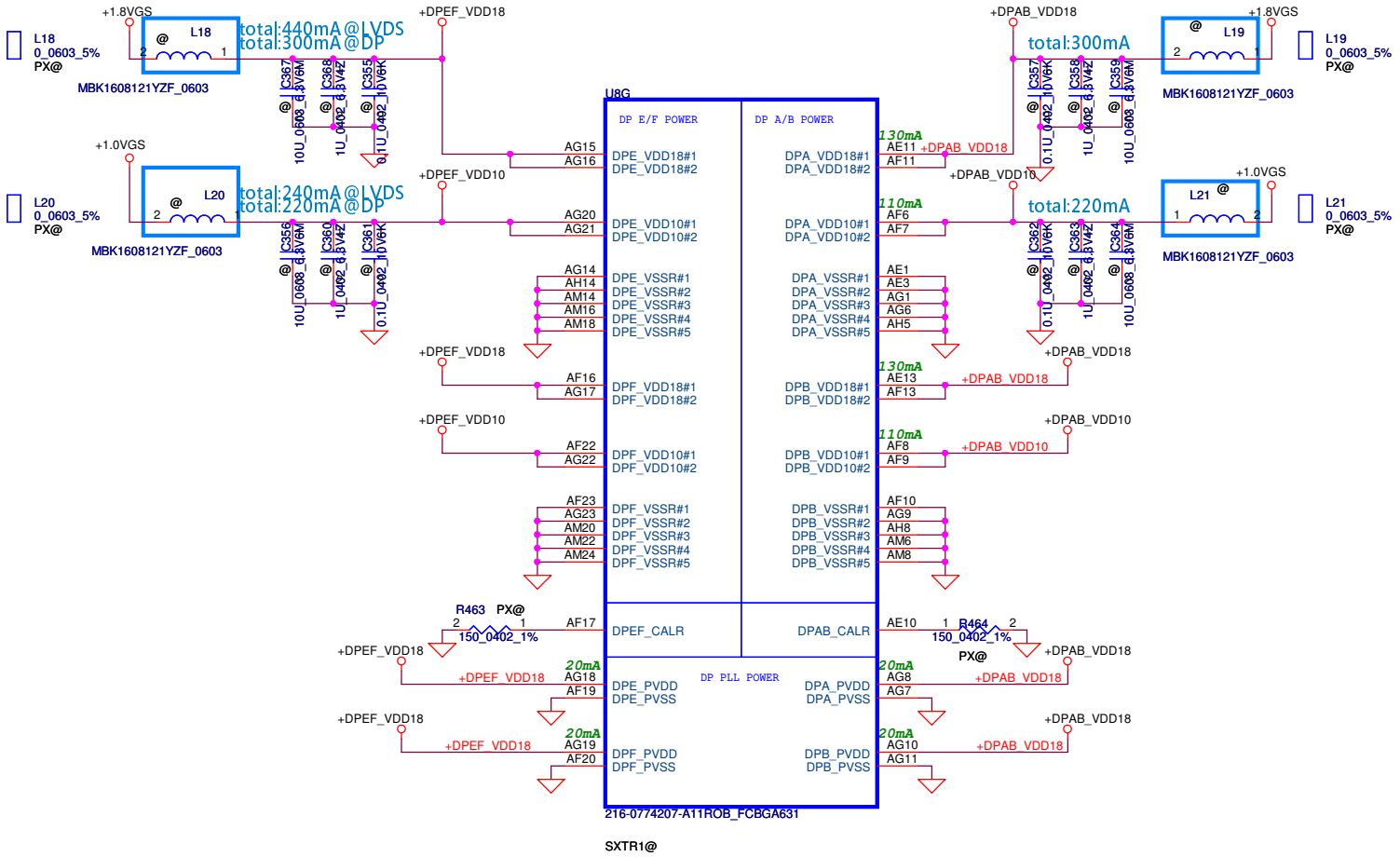
+1.5V_IO TO +1.5VGS



Security Classification	Compal Secret Data		
Issued Date	2012/01/15	Deciphered Date	2013/01/15

Compal Electronics, Inc.

Title	SeymourXT-S3 BACO Power	
Size: C	Document Number: VAUS5 LA9001P M/B	Rev: 0.3
Date: Friday, May 25, 2012	Sheet 17 of 50	



Security Classification	Compal Secret Data		
Issued Date	2012/01/15	Deciphered Date	2013/01/15

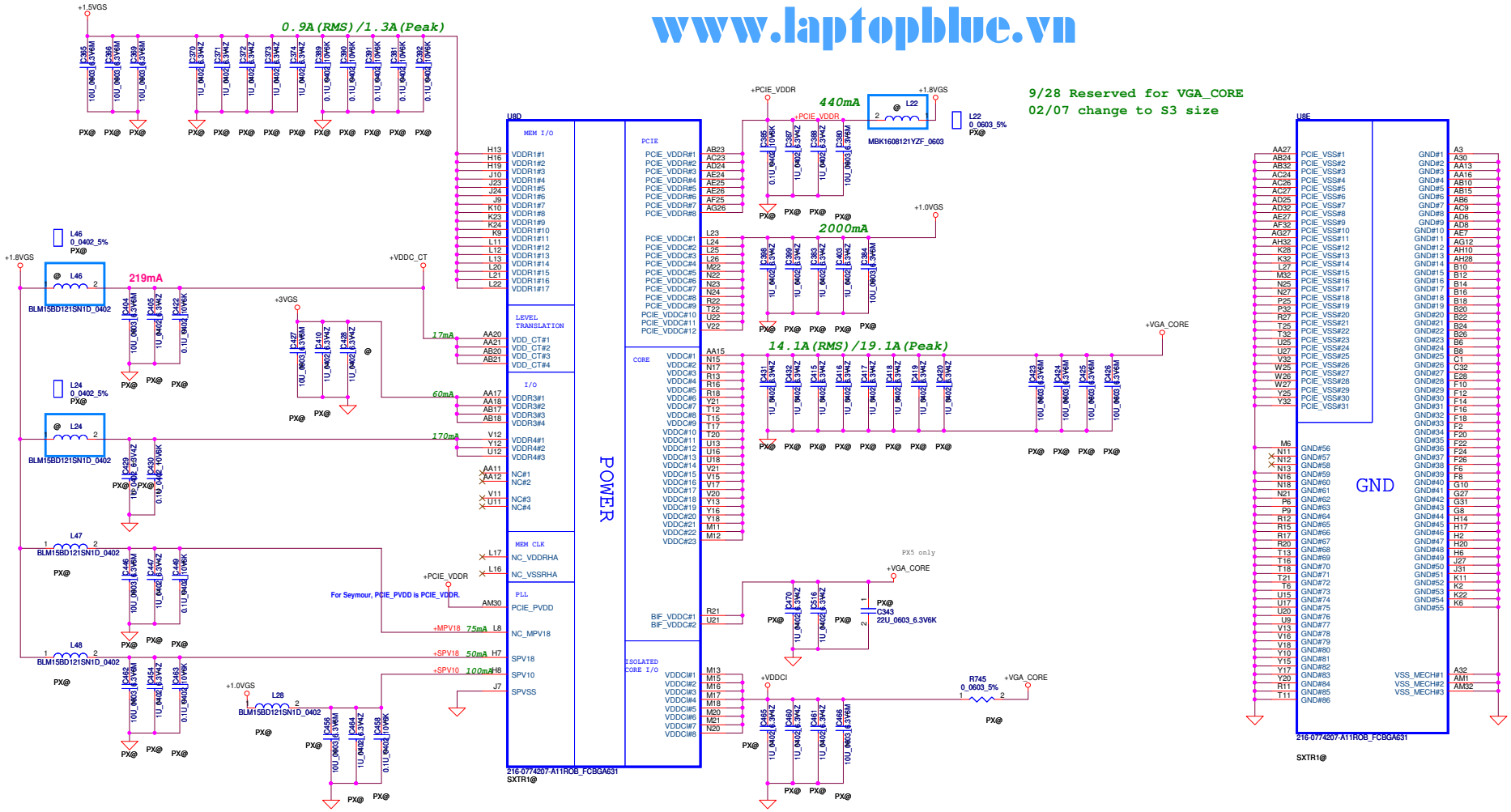
Compal Electronics, Inc.

Title: SeymourXT-S3 DPX Power

Size	Document Number	Rev
B	VAUS5 LA9001P M/B	0.3

Date: Friday, May 25, 2012 Sheet 18 of 50

9/28 Reserved for VGA_CORE
02/07 change to S3 size



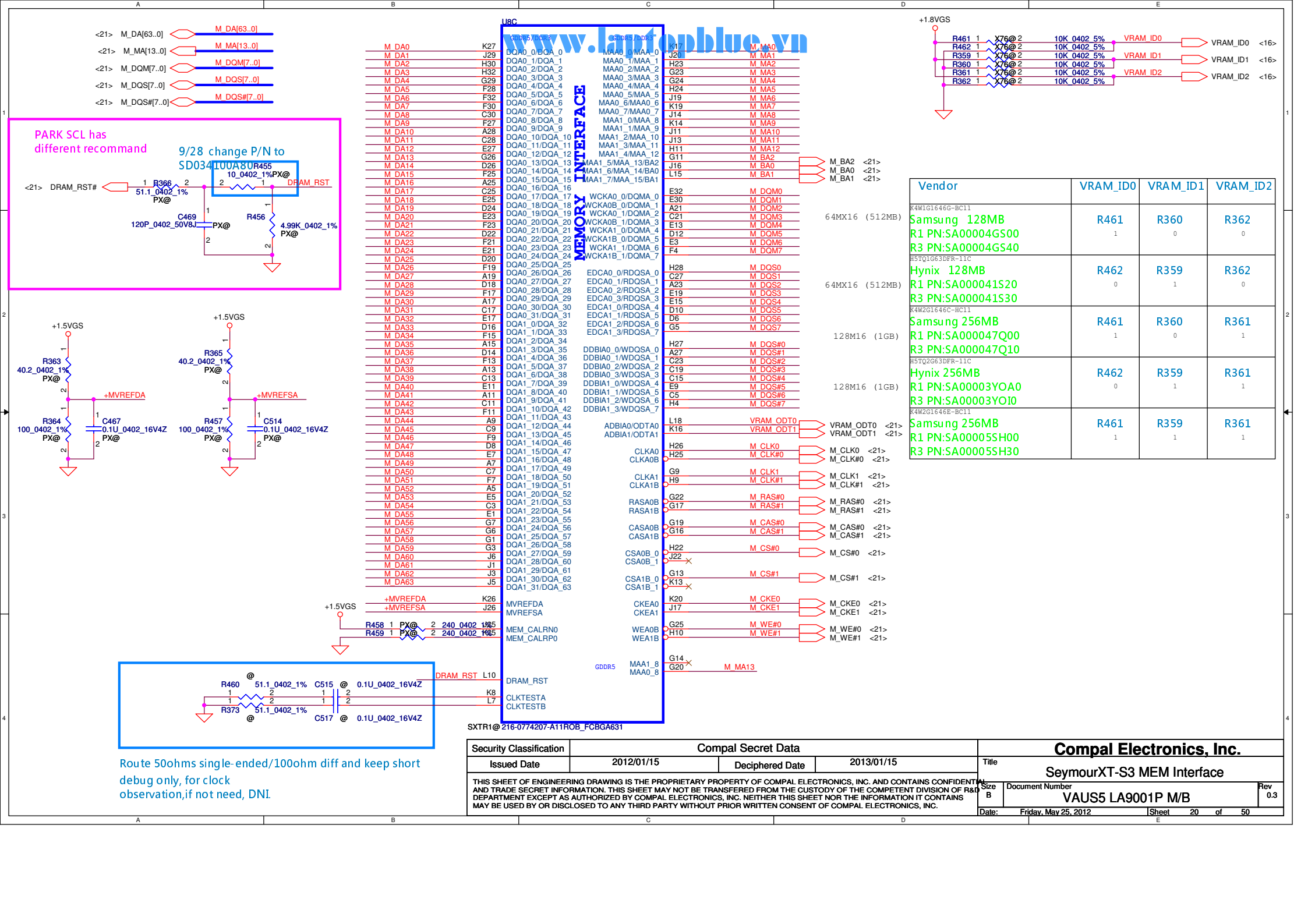
Security Classification	Compal Secret Data		
Issued Date	2012/01/15	Deciphered Date	2013/01/15

Compal Electronics, Inc.

Title: SeymourXT-S3 Power/GND

Size	Document Number	Rev
C	VAUS5 LA9001P M/B	0.3

Date: Friday, May 25, 2012 Sheet 19 of 50



Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2
K4W1G1646G-BC11 Samsung 128MB R1 PN:SA00004GS00 R3 PN:SA00004GS40 (64MX16 (512MB))	R461 1	R360 0	R362 0
H5TQ1G63DFR-11C Hynix 128MB R1 PN:SA000041S20 R3 PN:SA000041S30 (64MX16 (512MB))	R462 0	R359 1	R362 0
K4W2G1646C-HC11 Samsung 256MB R1 PN:SA000047Q00 R3 PN:SA000047Q10 (128M16 (1GB))	R461 1	R360 0	R361 1
H5TQ2G63DFR-11C Hynix 256MB R1 PN:SA00003YOA0 R3 PN:SA00003YOI0 (128M16 (1GB))	R462 0	R359 1	R361 1
K4W2G1646E-BC11 Samsung 256MB R1 PN:SA00005SH00 R3 PN:SA00005SH30	R461 1	R359 1	R361 1

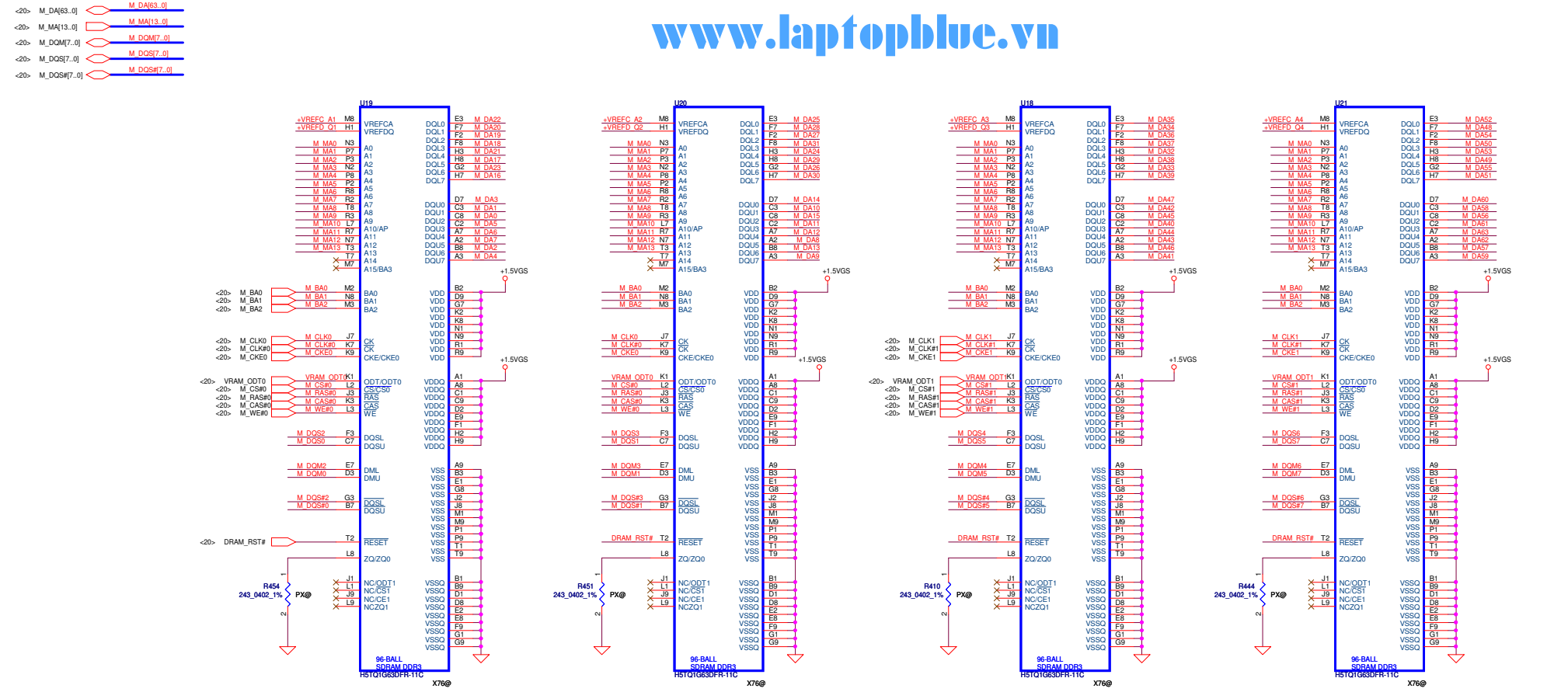
Security Classification	Compal Secret Data		
Issued Date	2012/01/15	Deciphered Date	2013/01/15

Compal Electronics, Inc.

Title: SeymourXT-S3 MEM Interface

Size: B | Document Number: VAUS5 LA9001P M/B | Rev: 0.3

Date: Friday, May 25, 2012 | Sheet 20 of 50



ref 139-02 recommand
add off page
Park SCL recommand pu
60.4 ohm to 1.5VGS 0619 update

VRAM P/N :
Hynix : SA000041S10 (S IC D3 64MX16 H5TQ1G63BFR-11C FBGA C38!)
Samsung : SA000041T10 (S IC D3 64MX16 K4W1G1646E-HC11 FBGA C38!)
update VRAM PN 0619 update

Security Classification	Compal Secret Data		
Issued Date	2012/01/15	Deciphered Date	2013/01/15

Compal Electronics, Inc.

Title	SeymourXT-S3 DDR3 VRAM		
Size C	Document Number VAUS5 LA9001P M/B		Rev 0.3
Date: Friday, May 25, 2012		Sheet 21 of 50	

+3VS — 30mil — R192 0_0603_5% — 30mil — +3VS_PS

Close to Pin3

+DP_V33

10U_0603_6.3V6M C230 0.1U_0402_16V4Z C231 0.1U_0402_16V4Z C232

Close to L15 / Close to Pin18

+SWR_VDD

10U_0603_6.3V6M C233 0.1U_0402_16V4Z C234 22U_0603_6.3V6M C235 0.1U_0402_16V4Z C236 0.1U_0402_16V4Z C237

Close to Pin13

Close to L171

22U_0603_6.3V6M C238 0.1U_0402_16V4Z C239 0.1U_0402_16V4Z C240 0.1U_0402_16V4Z C241

Close to Pin27 / Close to Pin7

+SWR_V12 — R200 0_0805_5% — +1.2VS

20110124 Modify

+3VS_PS

L16 FBMA-L11-201209-221LMA30T_0805 +DP_V33 40mil

L15 FBMA-L11-201209-221LMA30T_0805 +SWR_VDD 60mil

L171 4.7UH_PG0318-4R7MS_1.1A_20% +SWR_LX 60mil

U5 RTD2132S

DP_V33, SWR_VDD, PVCC, SWR_LX, SWR_VCCK, VCCK, DP_V12 — Power

TXEC+/TXEC- → LVDS_ACLK <23> / LVDS_ACLK# <23>

TXE2+/TXE2- → LVDS_A2 <23> / LVDS_A2# <23>

TXE1+/TXE1- → LVDS_A1 <23> / LVDS_A1# <23>

TXE0+/TXE0- → LVDS_A0 <23> / LVDS_A0# <23>

LVDS

<7> DP0_AUXP_C, DP0_AUXN_C — AUX_P, AUX_N

<7> DP0_TXP0_C, DP0_TXN0_C — LANE0P, LANE0N

DP-IN

GPIO(PWM OUT) → TL_INVT_PWM <23> / TL_ENVDD <23>

GPIO(Panel_VCC), GPIO(PWM IN) → APU_INVT_PWM, GPIO(BL_EN) → ENBKL_R

GPIO

CSCL, CSDA — CIICSCL1, CIICSDA1

LVDS EDID MIICSCL1/MIICDA1 → EDID_CLK <23> / EDID_DATA <23>

HPD, DP_REXT, DP_GND

ROM MIICSCL0/MIICDA0 → MIIC_SCL / MIIC_SDA

GND

Other

RTD2132S-VE-CG_QFN32_5X5

Reserved for EC programming ROM
Need EC confirm

<7> LVDS_HPD — R197 1K_0402_5% — LVDS_HPD_R

R198 100K_0402_5%

R199 12K_0402_1%

Change to 12Kohm 1% (DG ref.)
20101114

Will mount R200, @ L171, C238, C239 after DVT

EERom

Will @ U4 after DVT

+SWR_VDD

MIIC_SCL R193 0_0402_5% MIIC_SCL_R

MIIC_SDA R194 0_0402_5% MIIC_SDA_R

U4 CAT24C64WI-GT3_SO8 (VCC, WP, SCL, SDA, A0, A1, A2, GND)

+3VS_PS

R195 4.7K_0402_5%

MIIC_SCL

R196 4.7K_0402_5%

1:RevD W EEPROM
0:RevE W/O EEPROM

+3VS_PS

EDID_DATA R201 4.7K_0402_5%

EDID_CLK R202 4.7K_0402_5%

MIIC_SDA R203 4.7K_0402_5%

Panel PWM

+3VS

R207 47K_0402_5% — R208 4.7K_0402_5%

APU_INVT_PWM

Q7 2N7002K_SOT23-3

<7> DP_INT_PWM — R209 2.2K_0402_5% — Q8 MMBT3904_NL_SOT23-3

R210 4.7K_0402_5%

Vendor advise reserve it
(We delete the 0ohm path between ENBKL_R & TL_BKOFF#)

ENBKL_R — R204 0_0402_5% — ENBKL <31>

R206 100K_0402_5%

+3VS_PS — C242 0.1U_0402_16V7K

<23,31> BKOFF# — U6 MC74VHC1G08DFT2G SC70 5P — TL_BKOFF# <23>

CSDA — R212 0_0402_5% — TL_DATA <31>

CSCL — R213 0_0402_5% — TL_CLK <31>

Security Classification	Compal Secret Data		
Issued Date	2012/01/15	Deciphered Date	2013/01/15

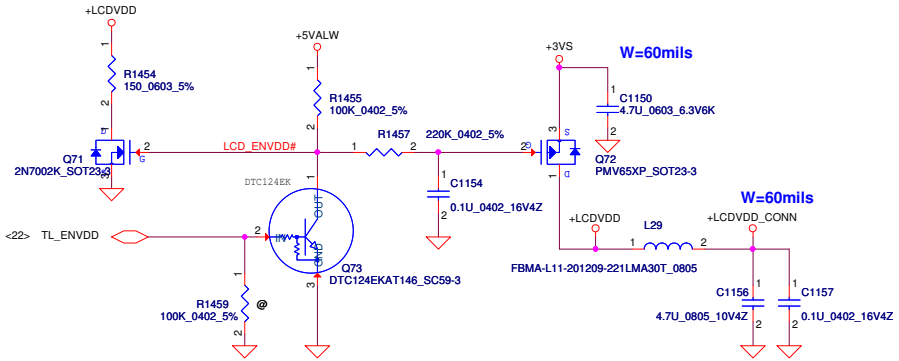
Compal Electronics, Inc.

Title: LVDS Translator - RTD2132S

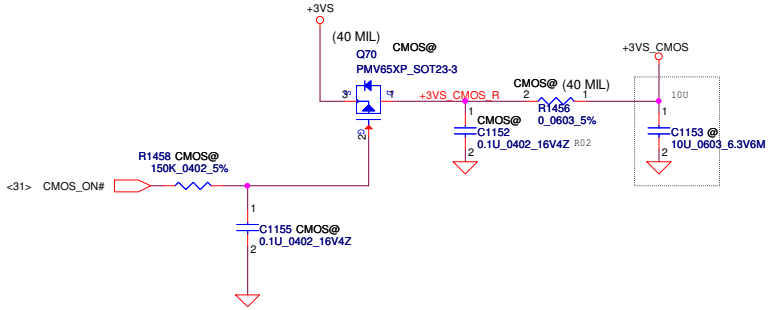
Size: Custom | Document Number: VAUS5 LA9001P M/B | Rev: 0.3

Date: Friday, May 25, 2012 | Sheet 22 of 50

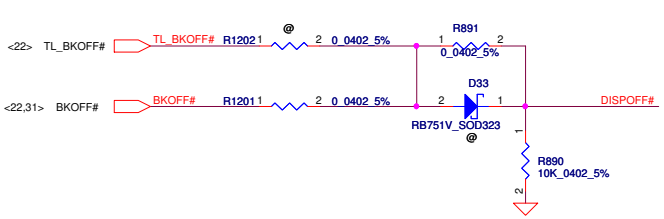
LCD POWER CIRCUIT

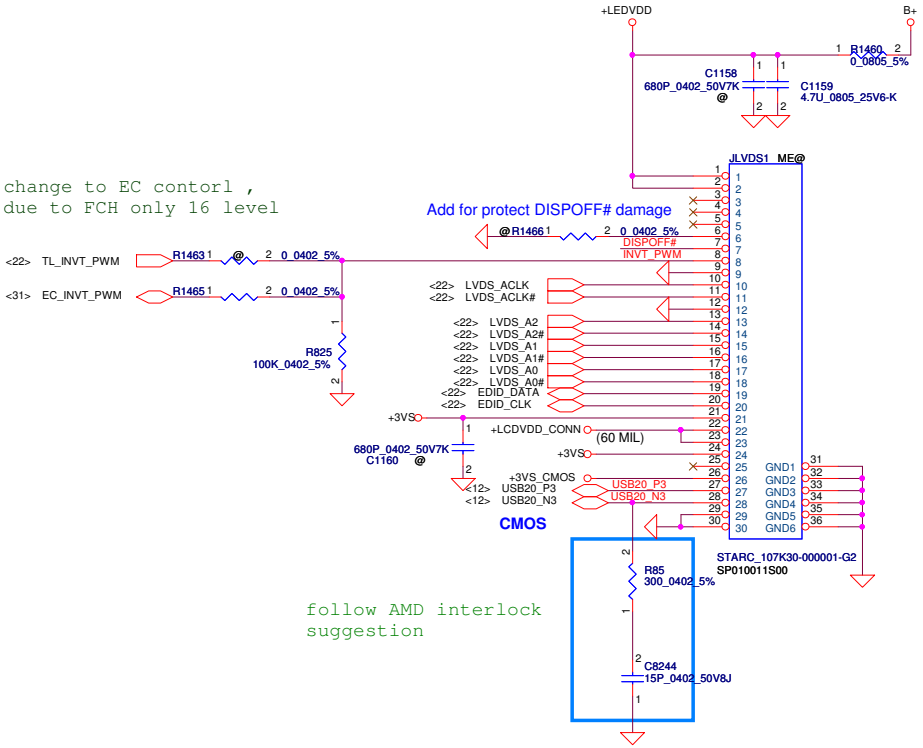


CMOS Camera



VGA LCD/PANEL BD. Conn.





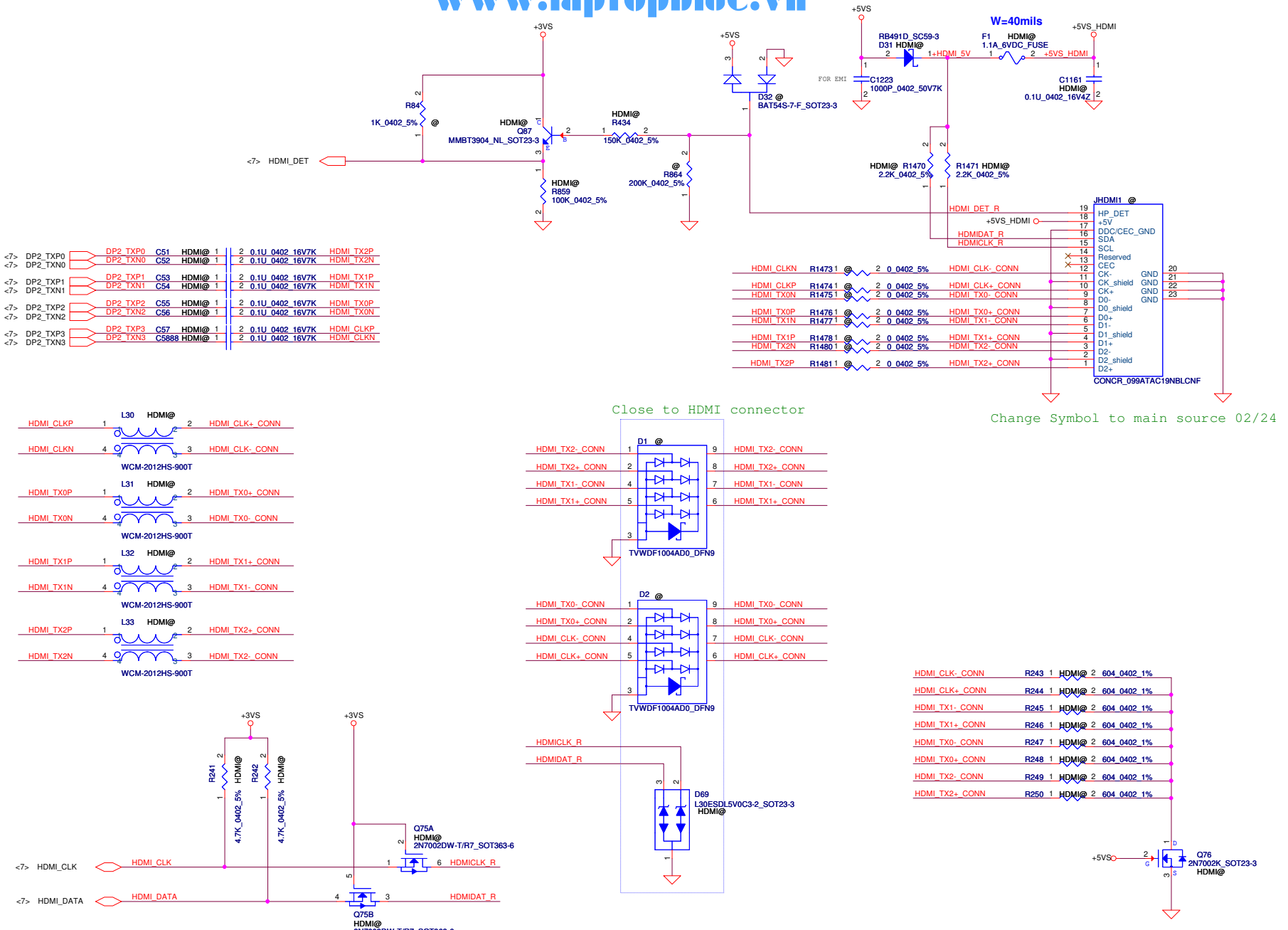
Security Classification	Compal Secret Data		
Issued Date	2012/01/15	Deciphered Date	2013/01/15

Compal Electronics, Inc.

Title: LVDS/CAMERA

Size: Custom | Document Number: VAUS5 LA9001P M/B | Rev: 0.3

Date: Thursday, May 31, 2012 | Sheet 23 of 50

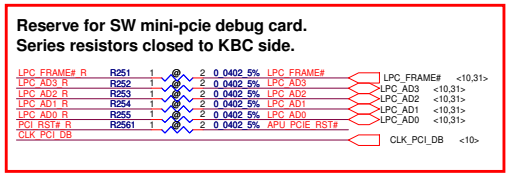


Security Classification	Compal Secret Data		
Issued Date	2012/01/15	Deciphered Date	2013/01/15

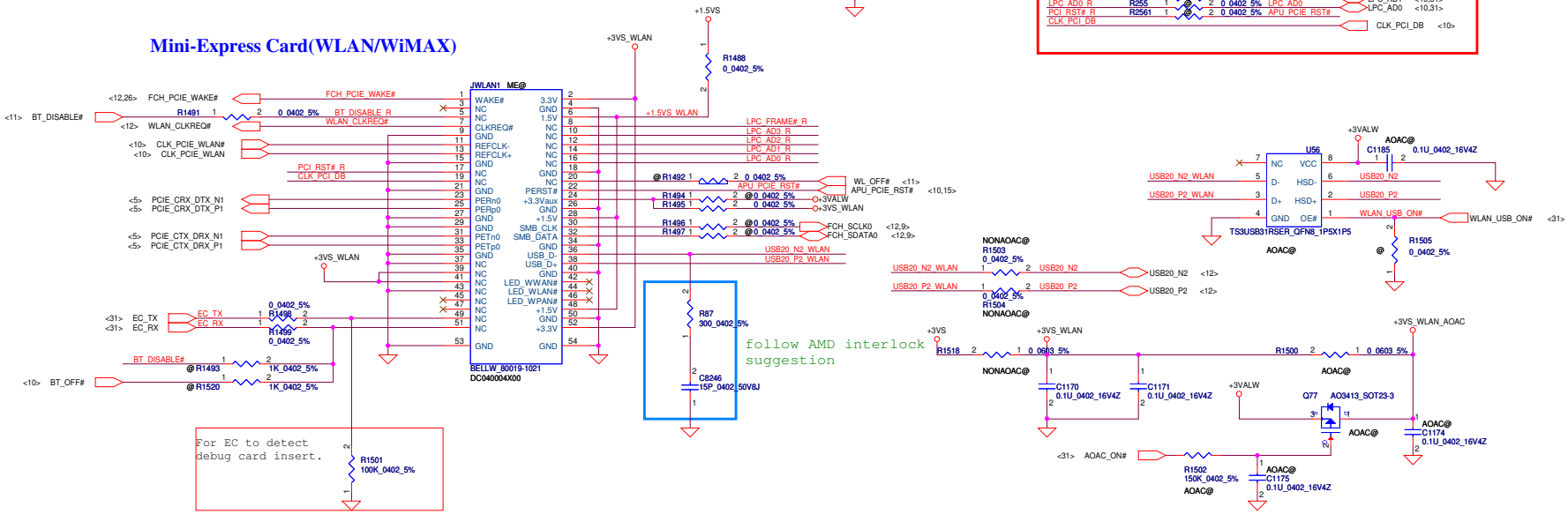
Compal Electronics,Ltd.			
Title	HDMI CONN		
Size	Document Number		Rev
Custom	VAUS5 LA9001P M/B		0.3
Date: Friday, May 25, 2012	Sheet 24 of 50		

Mini-Express Card for WLAN/WiMAX(Half)

Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.



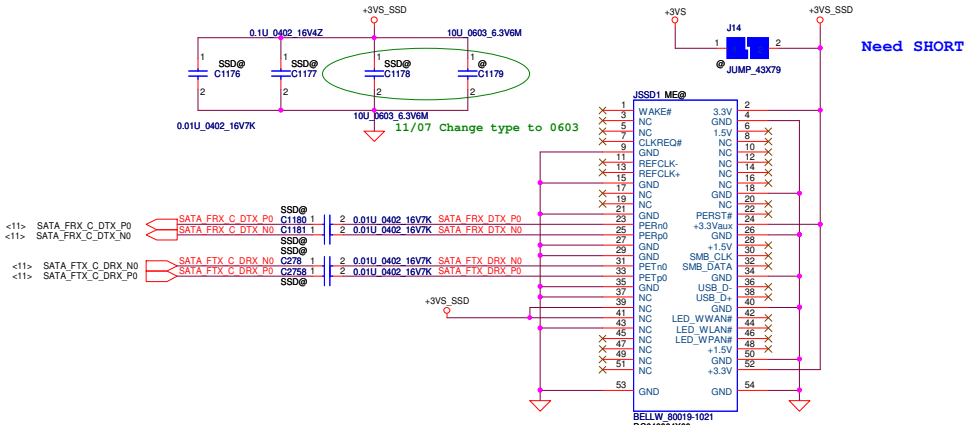
Mini-Express Card(WLAN/WiMAX)



Mini-Express Card for SSD(Full)

Mini-Express Card(WWAN/SSD)

SSD Active:4.5W(1.5A)



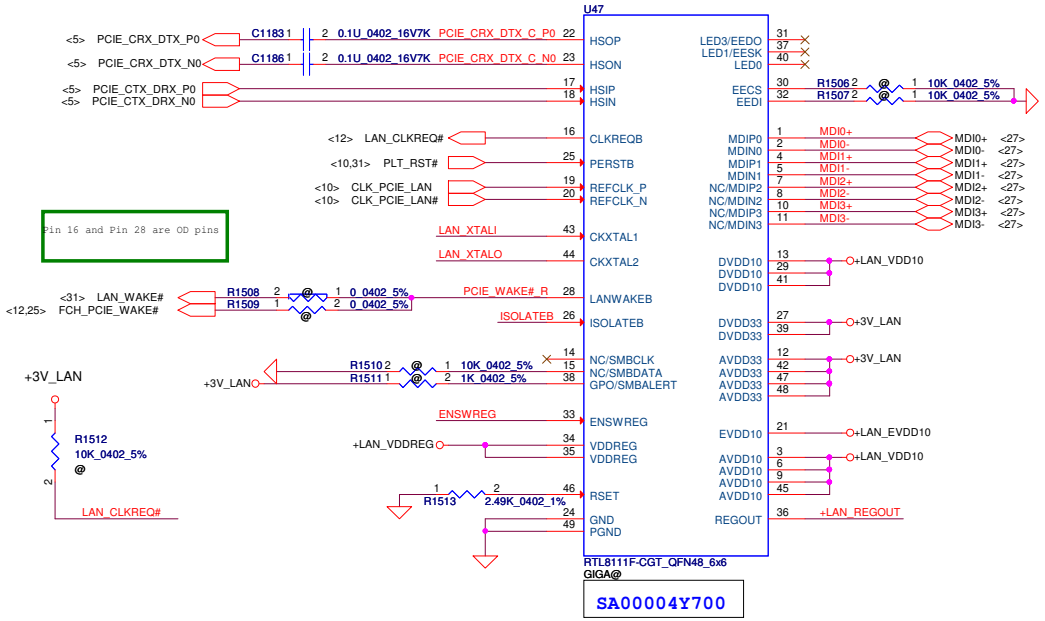
Security Classification	Compal Secret Data		
Issued Date	2012/01/15	Deciphered Date	2013/01/15

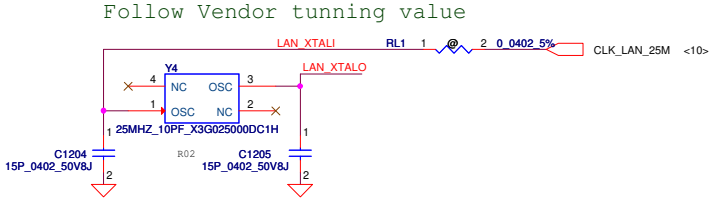
Compal Electronics, Inc.

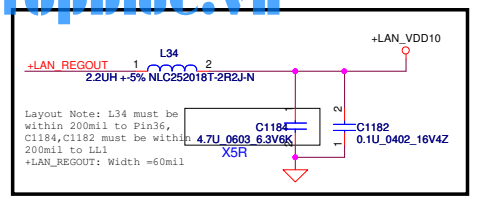
Title: **Mini-Card**

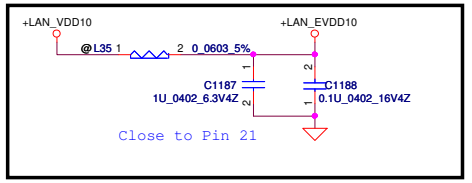
Size	Document Number	Rev
	VAUS5 LA9001P M/B	0.3

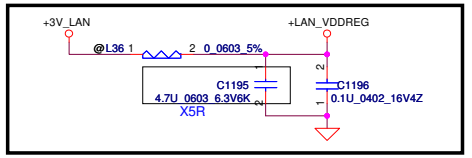
Date: Thursday, May 31, 2012 Sheet 25 of 50

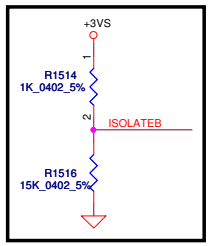


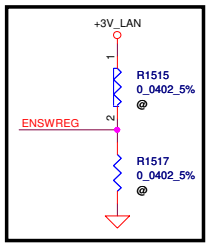




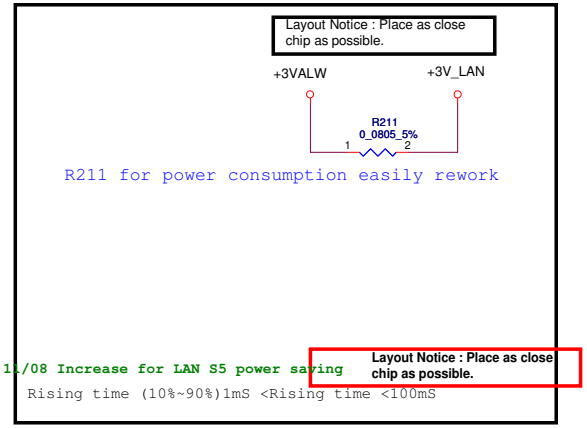


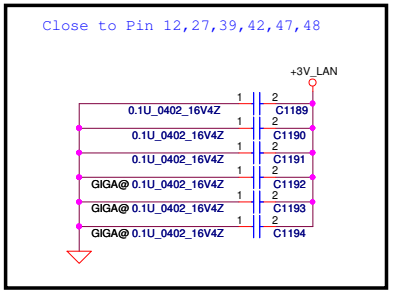


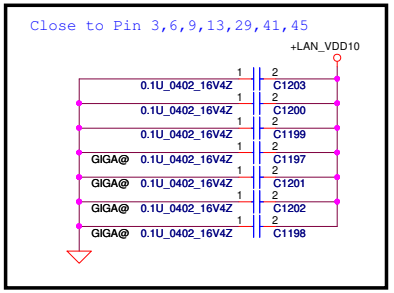




H: Enable internal Regular
L: Disable







Security Classification	Compal Secret Data		
Issued Date	2012/01/15	Deciphered Date	2013/01/15

Compal Electronics, Inc.

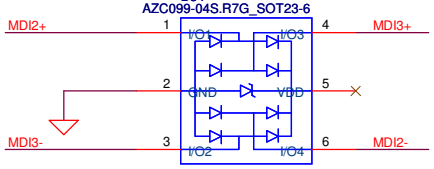
Title: LAN-RTL8111F/8105E

Size: Custom | Document Number: VAUS5 LA9001P M/B | Rev: 0.3

Date: Tuesday, May 29, 2012 | Sheet 26 of 50

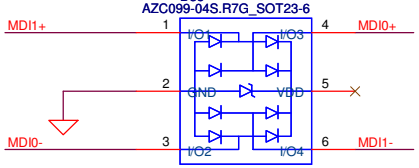
Reserve gas tube for EMI go rural solution

@
D34
AZC099-04S.R7G_SOT23-6



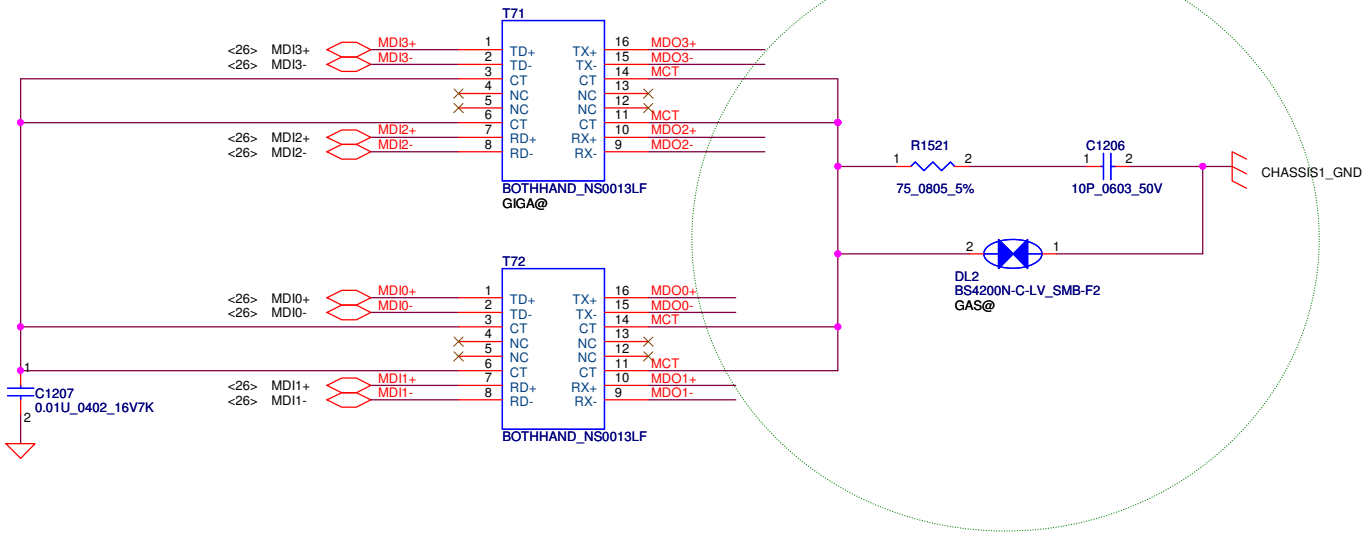
Place Close to T71

@
D35
AZC099-04S.R7G_SOT23-6

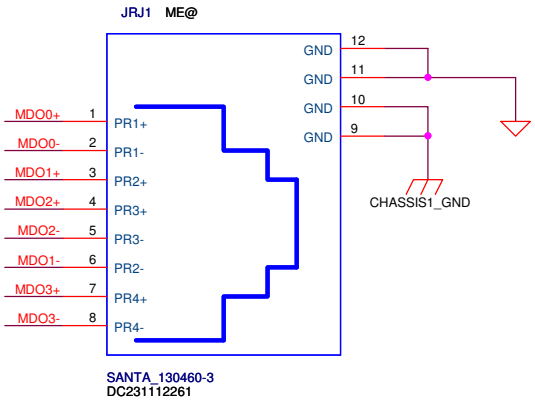


Place Close to T72

D34/D35
1'S PN:SC300001G00
2'S PN:SC300002E00



Place Close to T71,T72



Security Classification	Compal Secret Data		
Issued Date	2012/01/15	Deciphered Date	2013/01/15

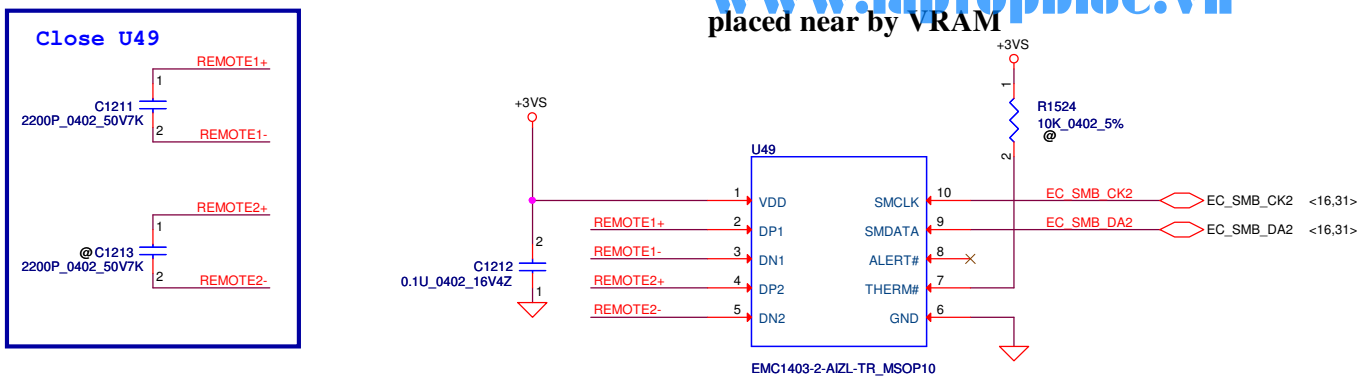
Compal Electronics, Inc.

Title: LAN_Transformer

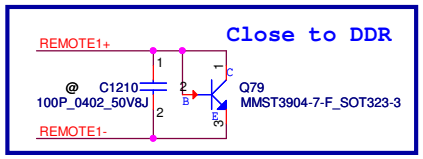
Size: B | Document Number: VAUS5 LA9001P M/B | Rev: 0.3

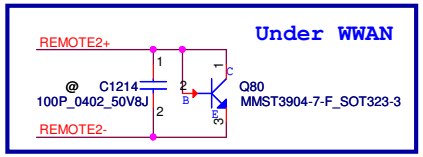
Date: Friday, May 25, 2012 | Sheet 27 of 50

SMSC thermal sensor placed near by VRAM



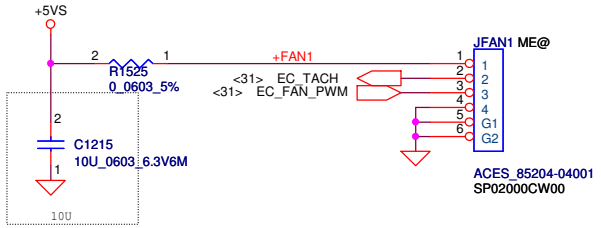
Address 1001_101xb



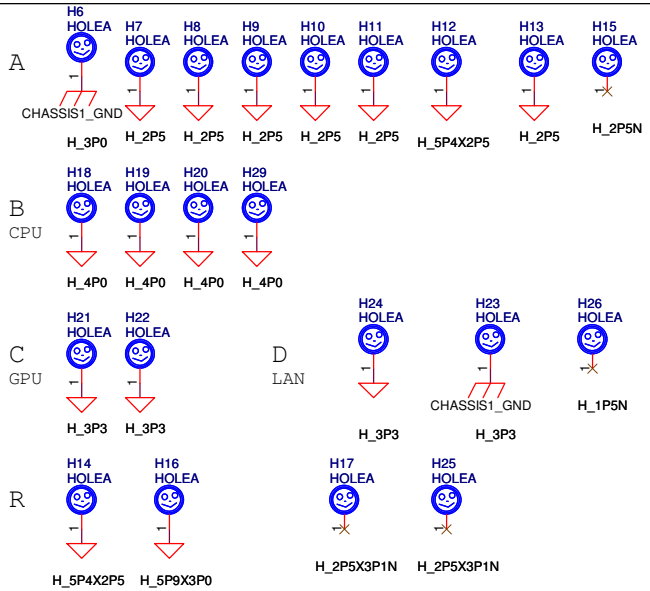


REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

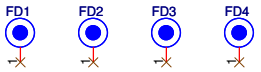
FAN1 Conn



Screw Hole



PCB Fedical Mark PAD



Security Classification	Compal Secret Data		
Issued Date	2012/01/15	Deciphered Date	2013/01/15

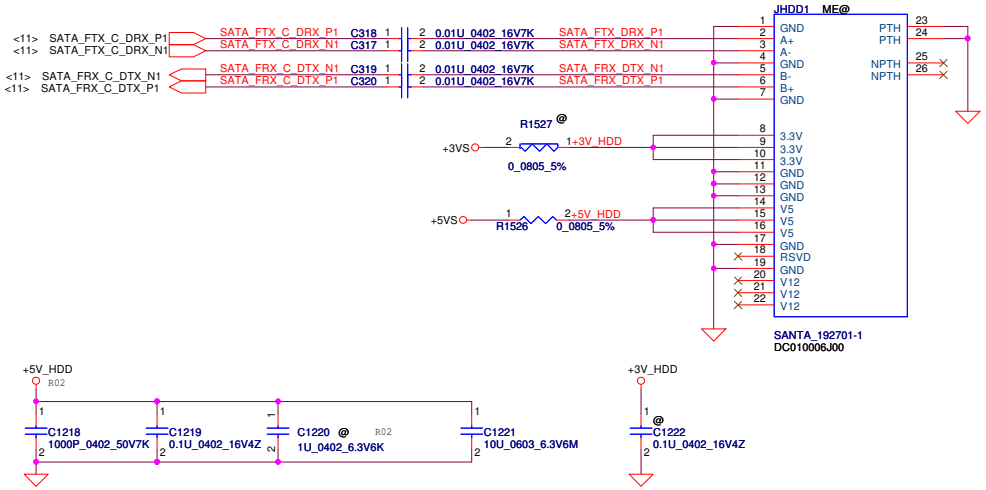
Compal Electronics,Ltd.

Title: **Fintek-Thermal IC/FAN/screw**

Size: B | Document Number: **VAUS5 LA9001P M/B** | Rev: 0.3

Date: Friday, May 25, 2012 | Sheet 28 of 50

SATA HDD Conn.



Security Classification	Compal Secret Data		
Issued Date	2012/01/15	Deciphered Date	2013/01/15

Compal Electronics, Inc.

Title: HDD Connector

Size: Custom	Document Number: VAUS5 LA9001P M/B	Rev: 0.3
Date: Friday, May 25, 2012	Sheet 29 of 50	

600ohms @100MHz 1A
P/N: SM01000BU00

600ohms @100MHz 2A
P/N: SM01000EE00

Power down (PD#) power stage for save power
0V: Power down power stage
3.3V: Power up power stage

Place near Pin25
Place near Pin38
Place near Pin1
Place near Pin9
Place next to pin 27

Vendor recommend. 2.2K
Vendor recommend. 2.2u

external MIC
Internal Speaker
Headphone

MIC Sense
R939 place near pin13
Capless HP Sense
R940 place near pin34

0525 EMI request to add C83 and C84.
Close to U50 Audio IC

S IC ALC259-VC2-CG MQFN 48P CODEC

Pin Assignment	Location	Function
SPK-OUT (Pin40/41/44/45)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
MIC1(Pin21/22)	External	Mic in

wide 25MIL

Reserve for ESD request.

Combo Jack detect (normal open)

PC Beep

EMI

Security Classification	Compal Secret Data	
Issued Date	2012/01/15	Deciphered Date 2013/01/15

Compal Electronics,Ltd.
Title: HD Audio Codec_ALC269Q-VC
Size: C | Document Number: VAUS5 LA9001P M/B | Rev: 0.3
Date: Friday, May 25, 2012 | Sheet 30 of 50

Vcc	3.3V +/- 5%
R1562	100K +/- 5%

Board ID	R1564	VAD_BID min	VAD_BID typ	VAD_BID max	
0	0	0 V	0 V	0 V	MP
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	PVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	EVT

U51 KB9012QF A3 LQFP 128P_14X14

LPC & MISC · PWM Output · AD Input · DA Output · PS2 Interface · Int. K/B Matrix · SPI Device Interface · SPI Flash ROM · SM Bus · GPIO · GPO · GPI

Security Classification	Compal Secret Data		
Issued Date	2012/01/15	Deciphered Date	2013/01/15

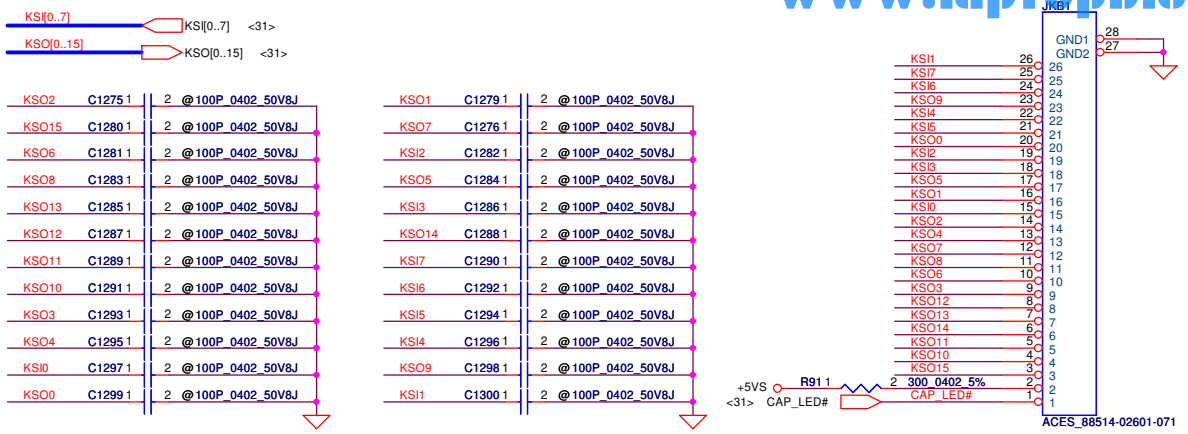
Compal Electronics, Inc.

Title: BIOS & EC I/O Port

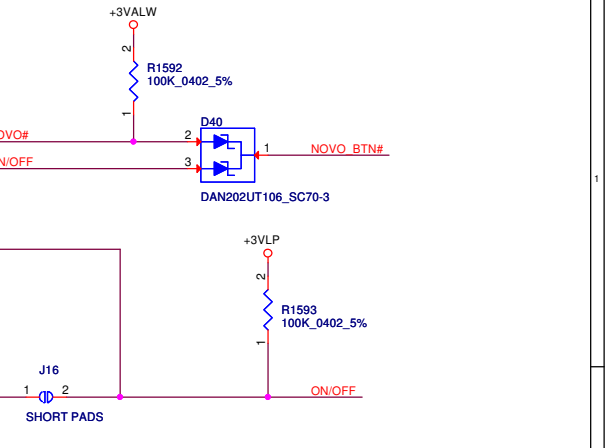
Size: Custom | Document Number: VAUS5 LA9001P M/B | Rev: 0.3

Date: Friday, May 25, 2012 | Sheet 31 of 50

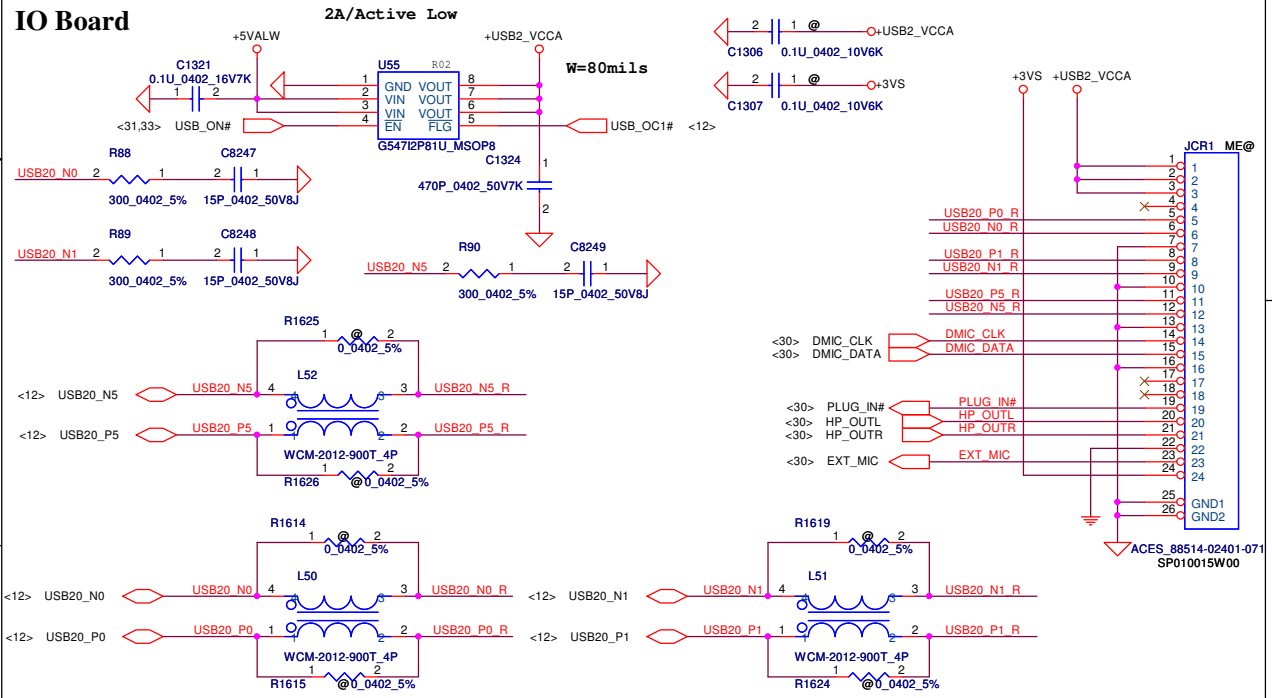
INT_KBD Conn.



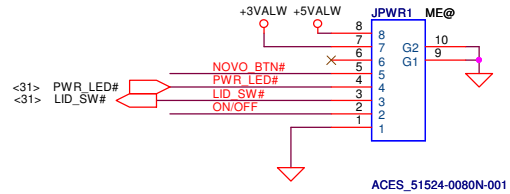
Power Board



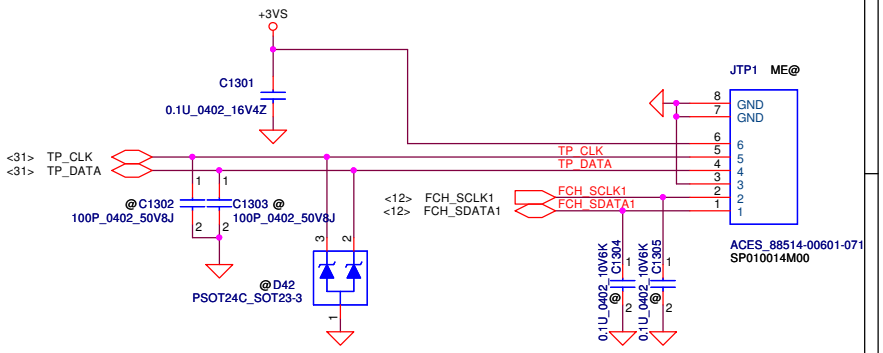
IO Board



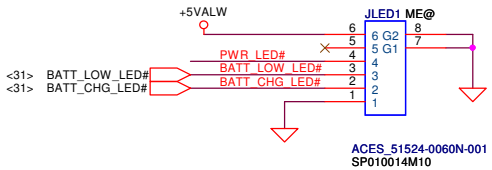
Power Board



TouchPAD Module

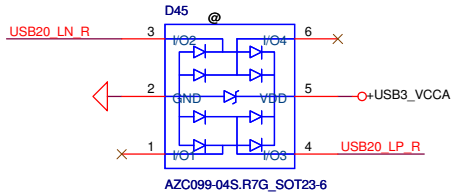


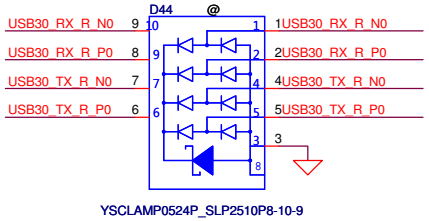
LED Board



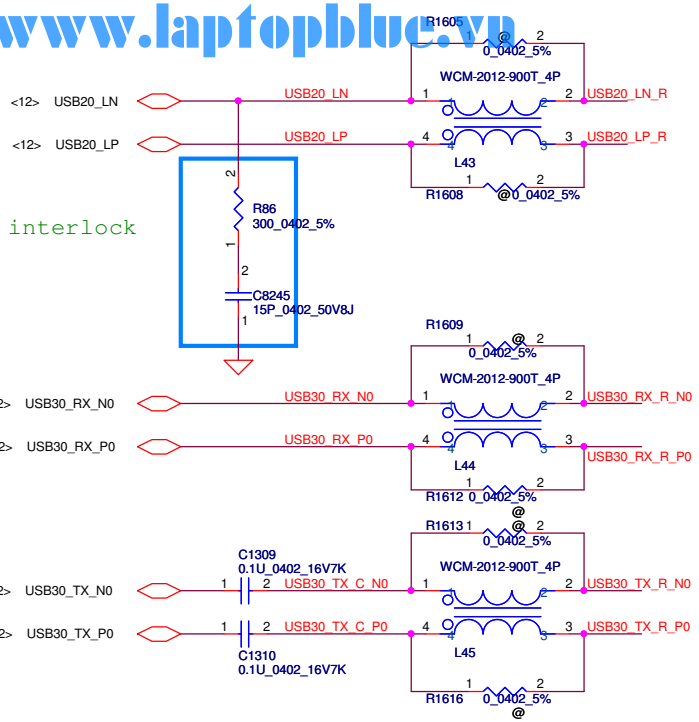
Security Classification	Compal Secret Data		
Issued Date	2012/01/15	Deciphered Date	2013/01/15

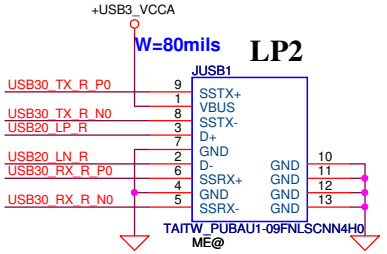
Compal Electronics, Inc.			
Title: KB /SW /LPC Debug Conn.			
Size: Custom	Document Number: VAUS5 LA9001P M/B		Rev: 0.3
Date: Thursday, May 31, 2012	Sheet 32 of 50		



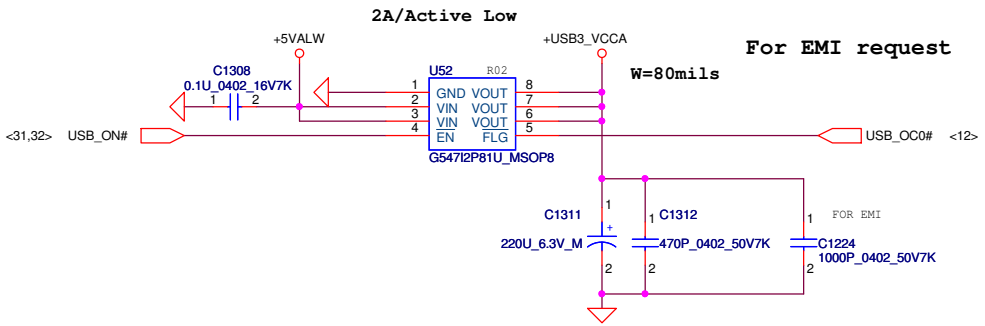


follow AMD interlock suggestion





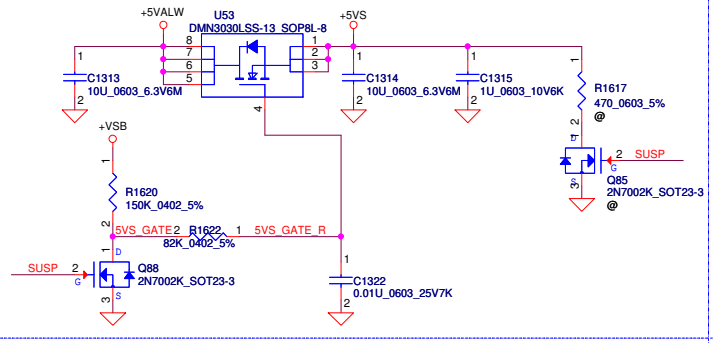
Place TX AC coupling Cap (C1309,C1310). Close to connector



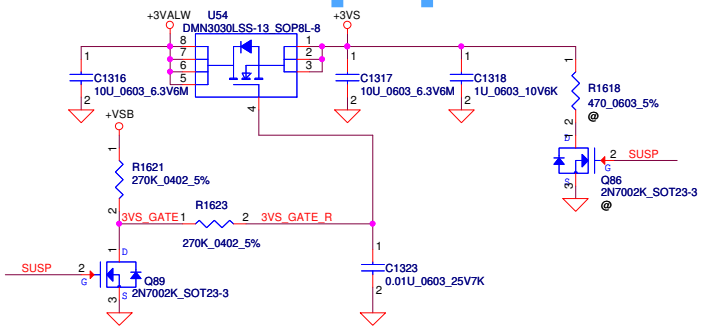
Security Classification	Compal Secret Data For EMI request		
Issued Date	2012/01/15	Deciphered Date	2013/01/15

Compal Electronics, Inc.			
Title: USB3.0 ports			
Size: Custom	Document Number: VAUS5 LA9001P M/B		Rev: 0.3
Date: Thursday, May 31, 2012	Sheet 33 of 50		

+5VALW TO +5VS

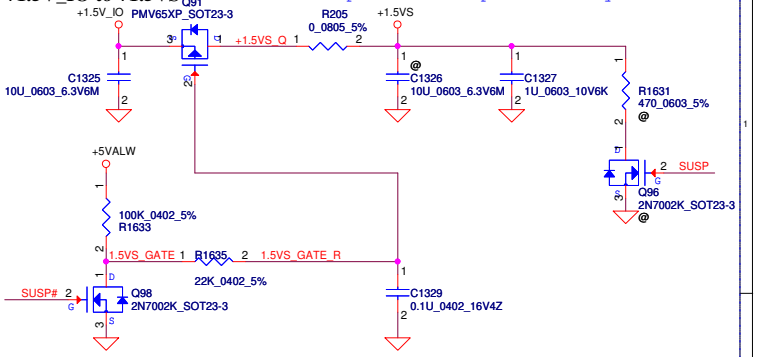


+3VALW TO +3VS

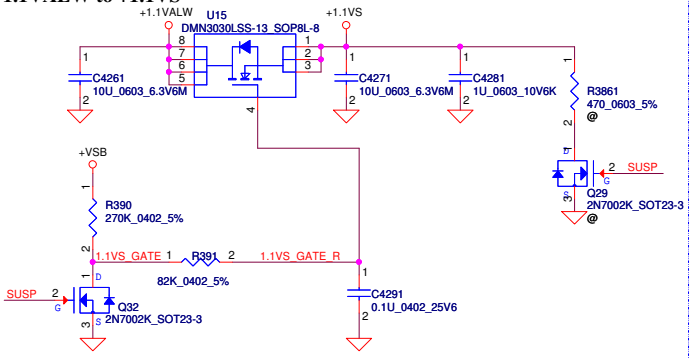


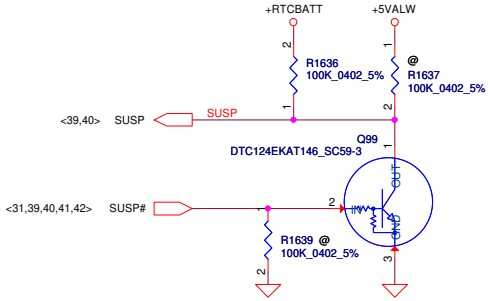
+1.5V_IO to +1.5VS

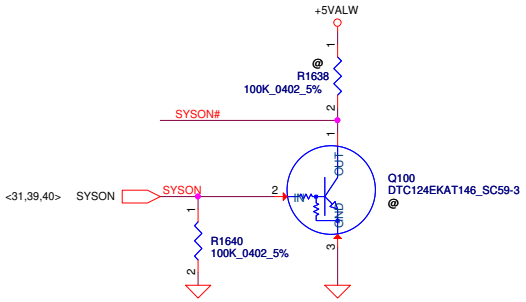
R205 for power consumption easily rework

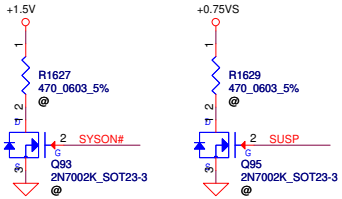


+1.1VALW to +1.1VS









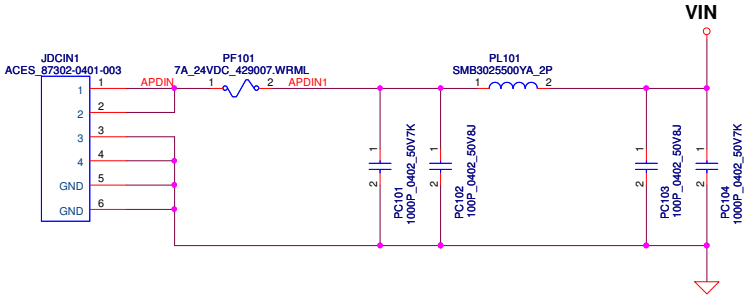
Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2013/06/30

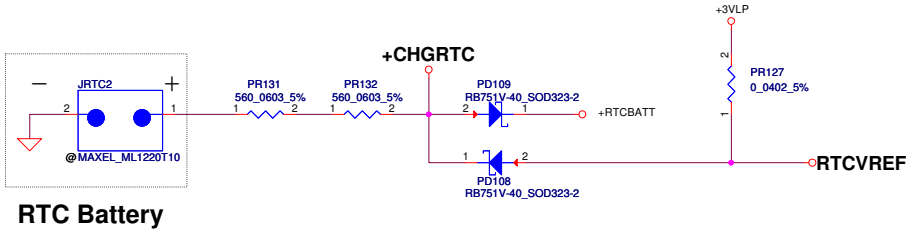
Compal Electronics, Inc.

Title: DC-DC INTERFACE

Size	Document Number	Rev
Custom	VAUS5 LA9001P M/B	0.3

Date: Friday, May 25, 2012 Sheet 34 of 50





RTC Battery

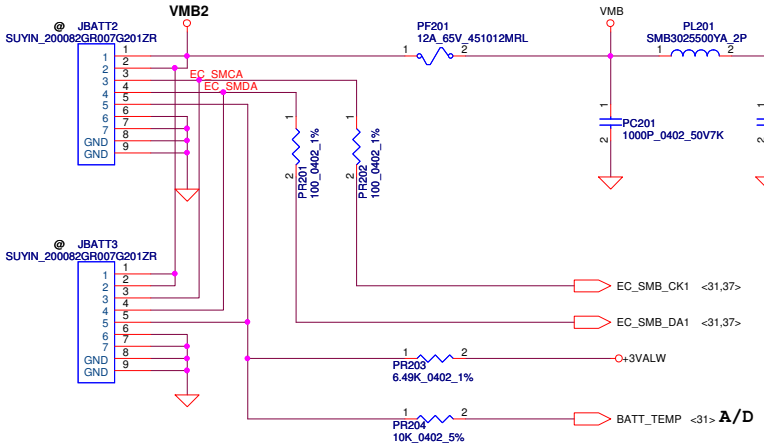
Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: PWR DCIN / Vin Detector /Pre-charge

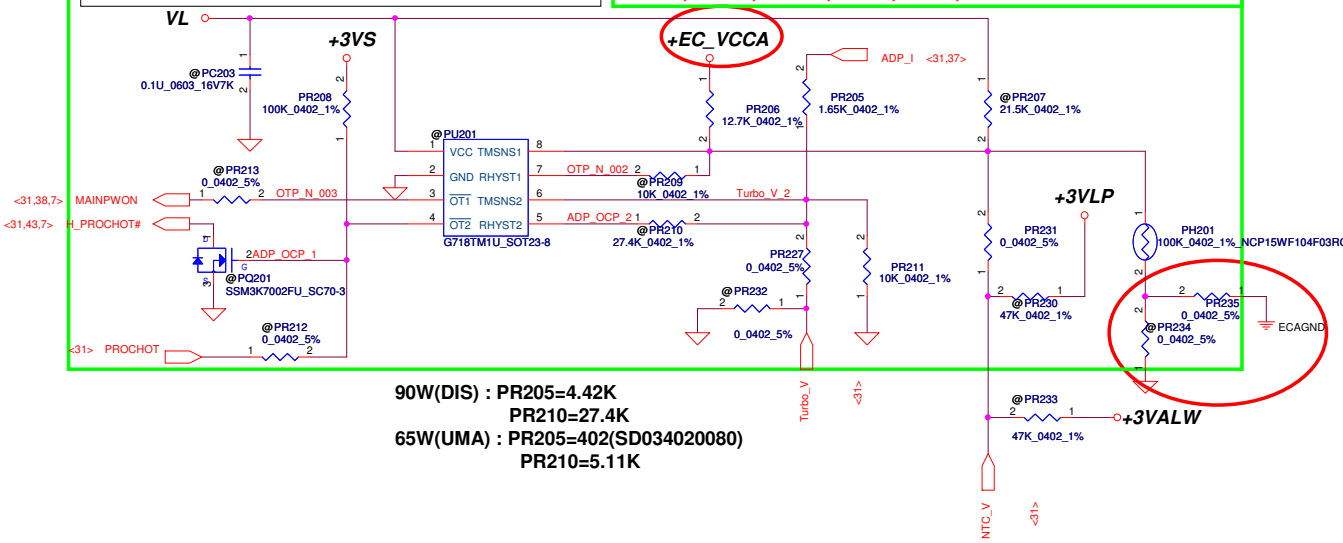
Size: Custom | Document Number: LA9001P | Rev: 0.1

Date: Friday, May 25, 2012 | Sheet 35 of 48

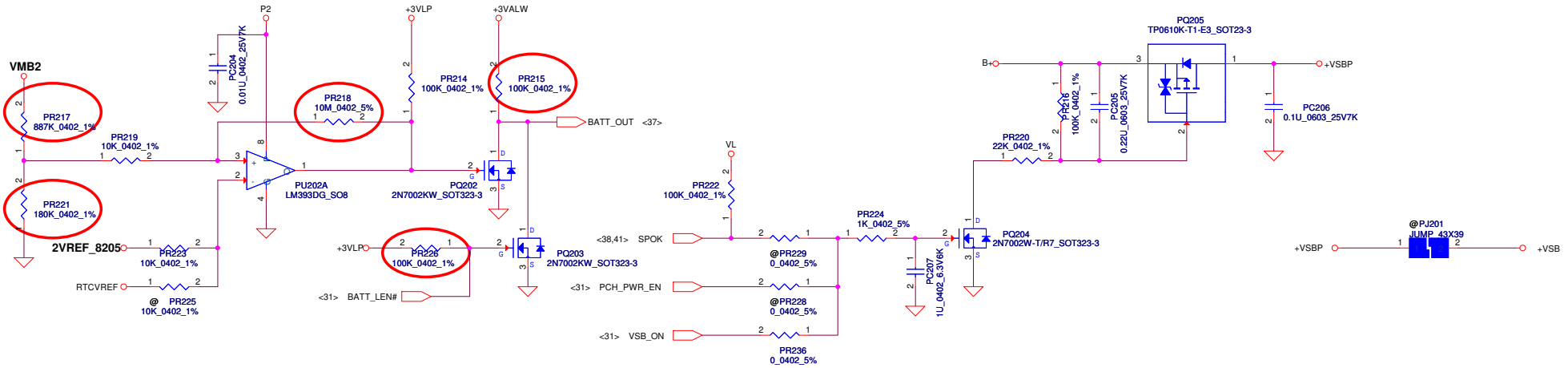


PH1 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

For KB930 --> Keep PU201 circuit
(Vth = 1.25V)
For KB9012 (Red circle) --> Remove PU201 circuit, but keep PR206
PH201, PR205, PR211,PQ201,PR208,PR212



90W(DIS) : PR205=4.42K
PR210=27.4K
65W(UMA) : PR205=402(SD034020080)
PR210=5.11K



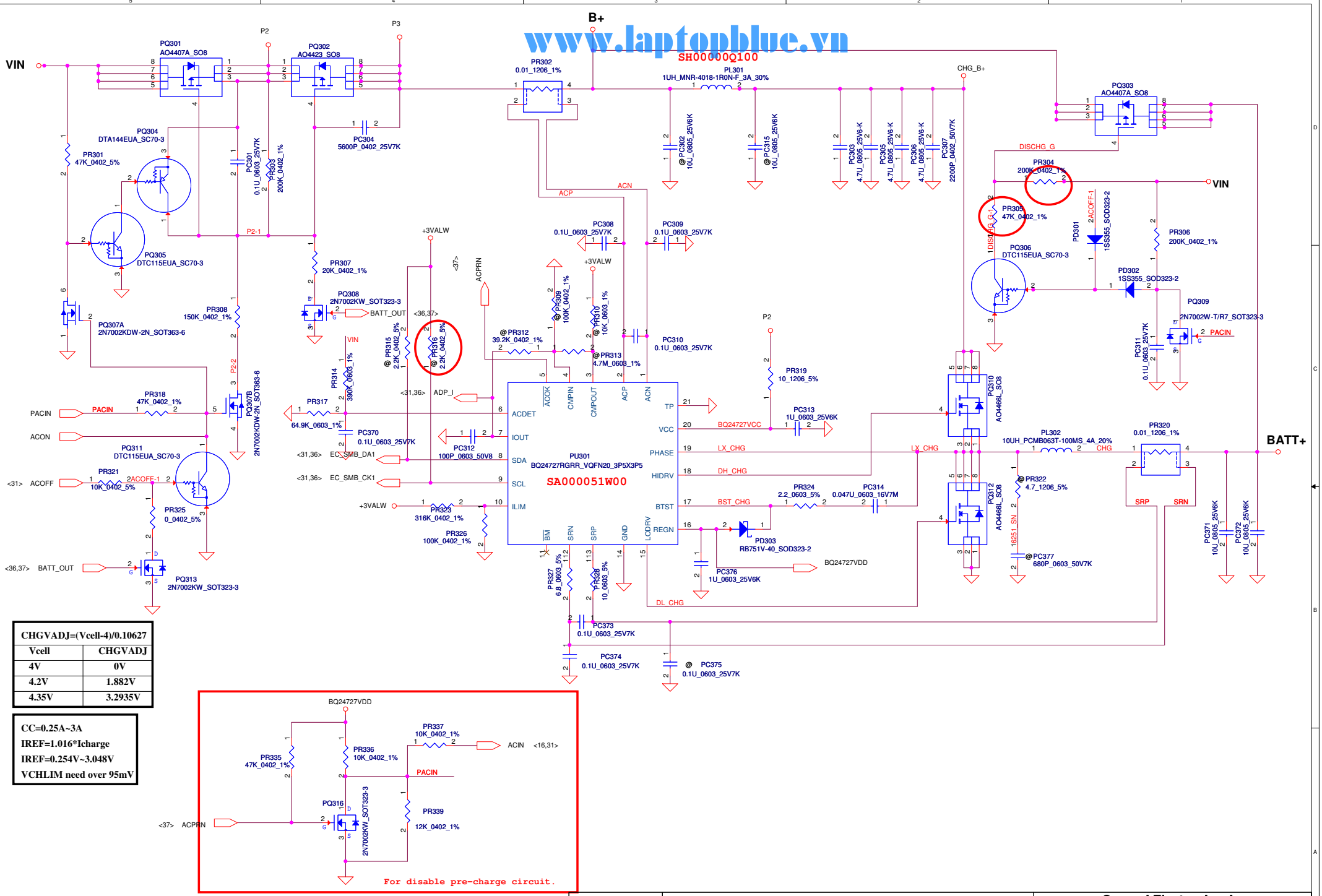
Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: PWR-BATTERY CONN/OTP

Size	Document Number	Rev
Custom	LA9001P	0.1

Date: Friday, May 25, 2012 Sheet 36 of 48



CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

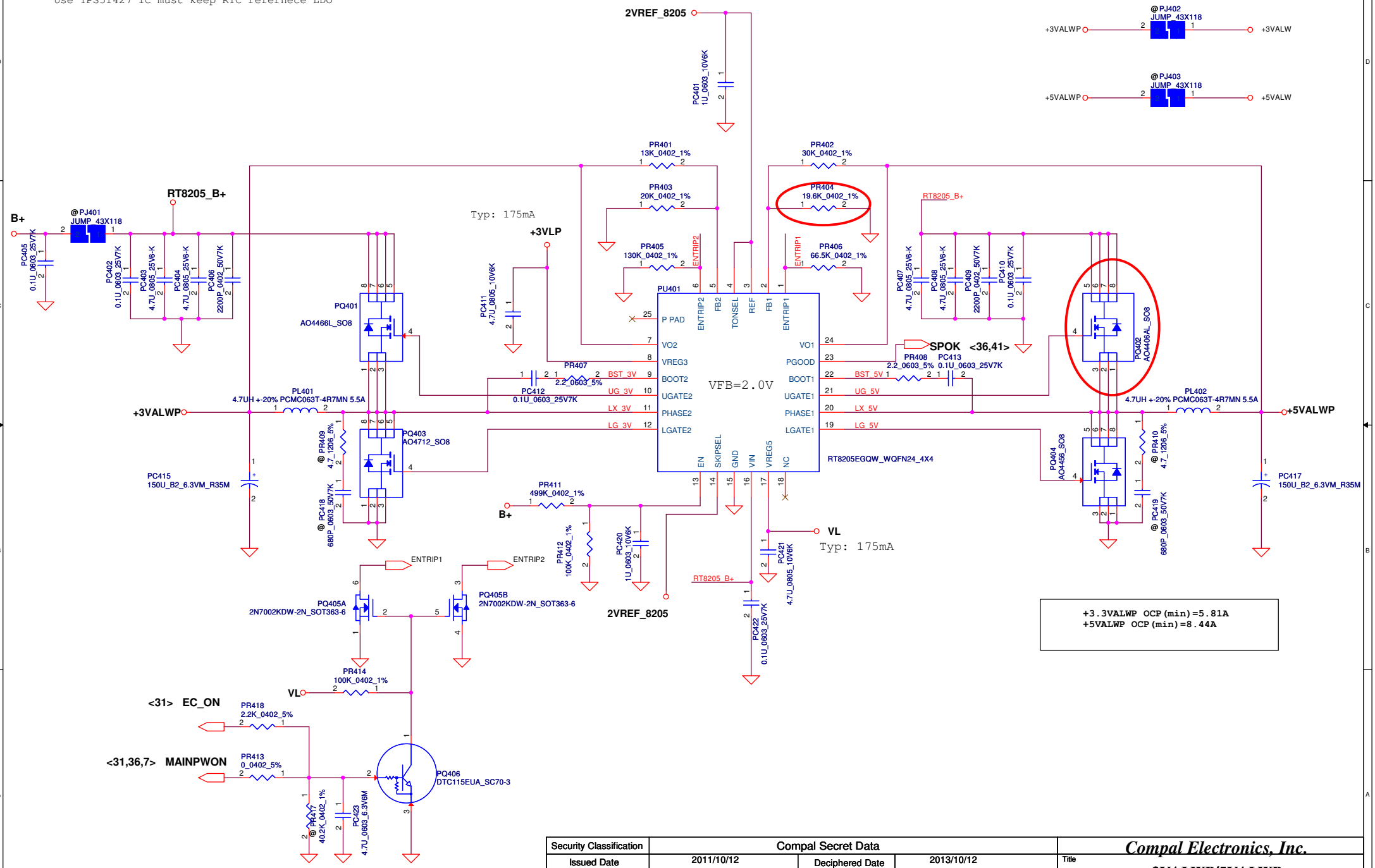
Compal Electronics, Inc.

Title: CHARGER

Size | Document Number: LA9001P | Rev: 0.1

Date: Friday, May 25, 2012 | Sheet 37 of 48

Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

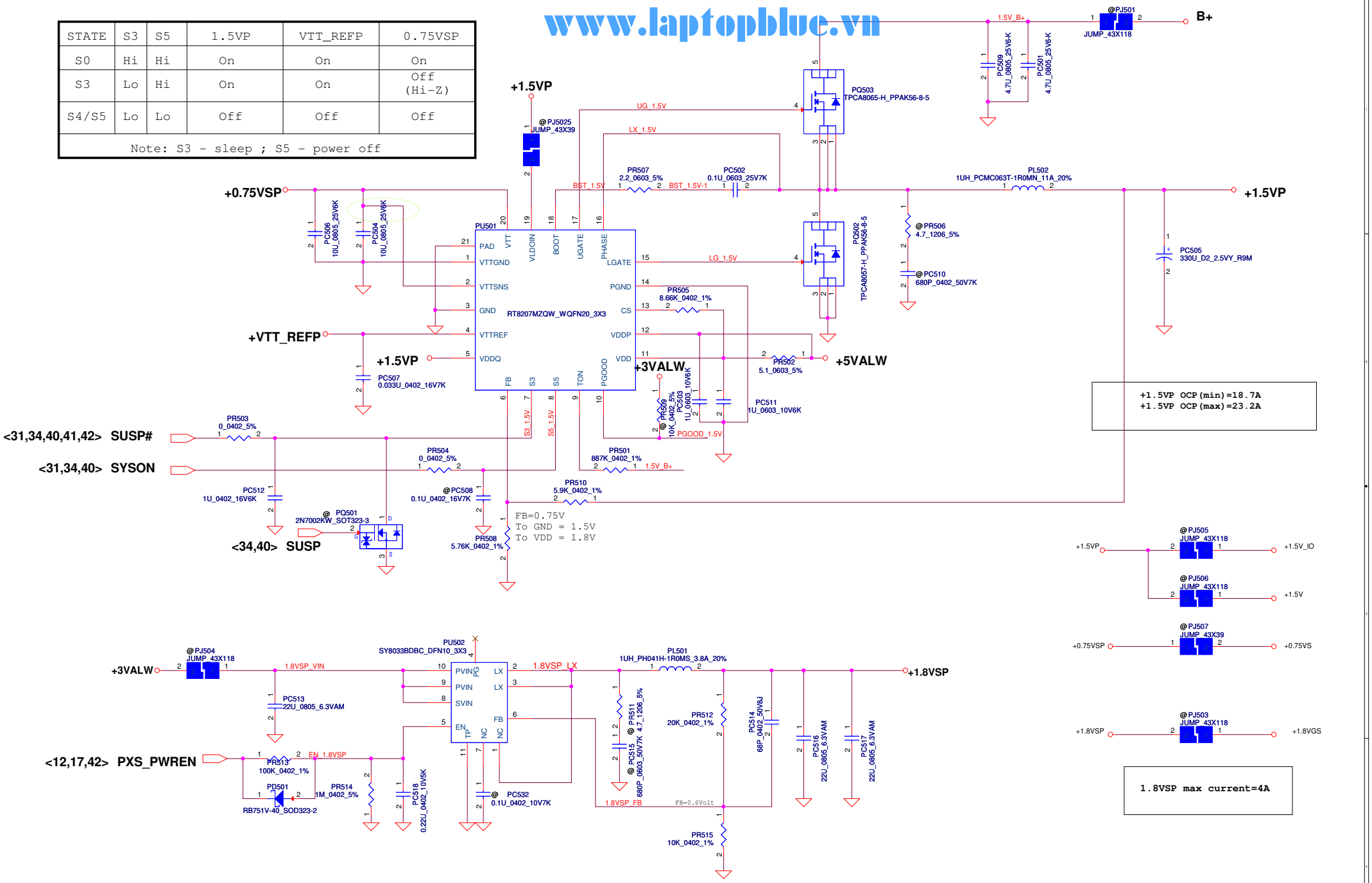
Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size	Document Number	Rev
Custom	LA9001P	0.1

Date: Friday, May 25, 2012 Sheet 38 of 48

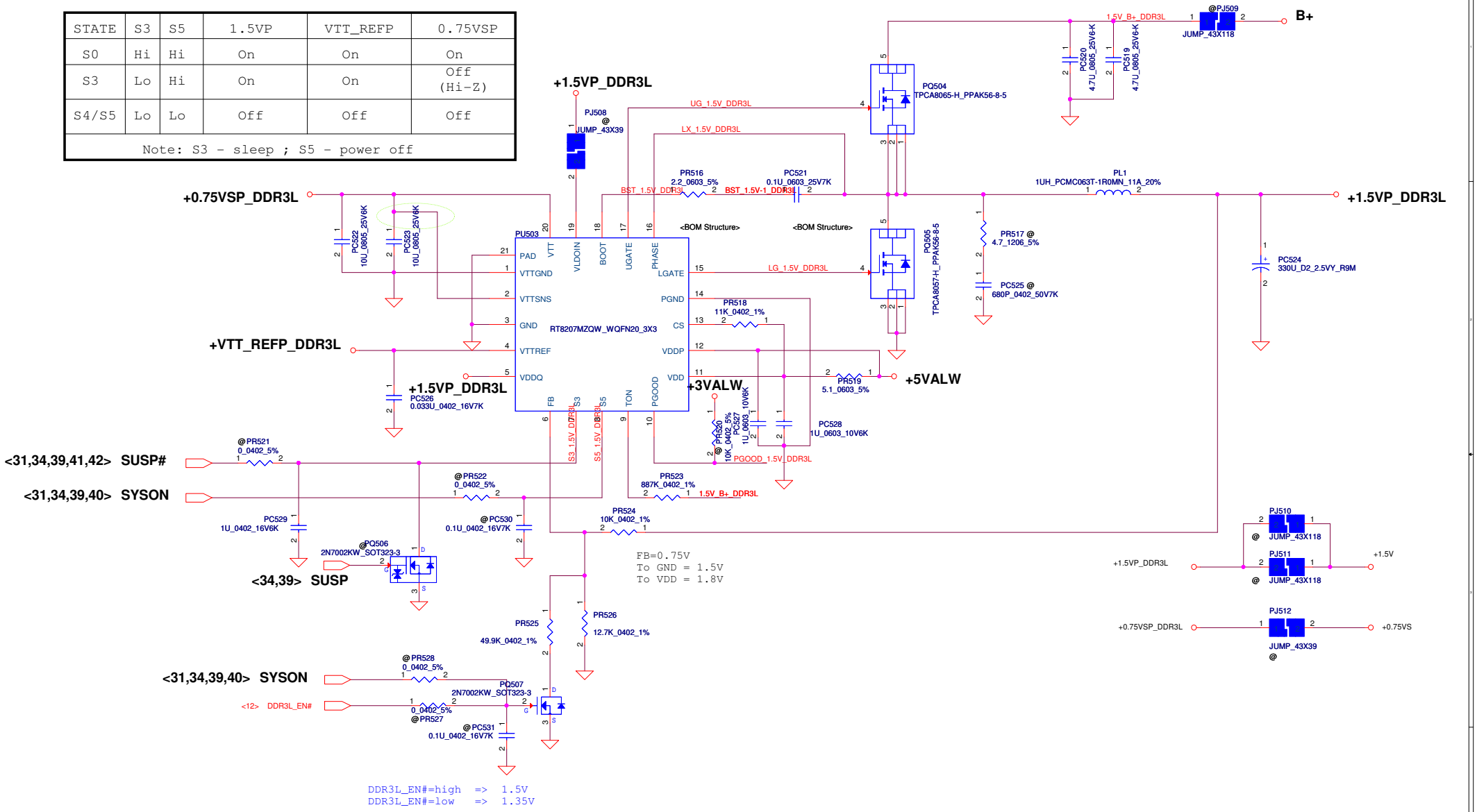
STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off
Note: S3 - sleep ; S5 - power off					



Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

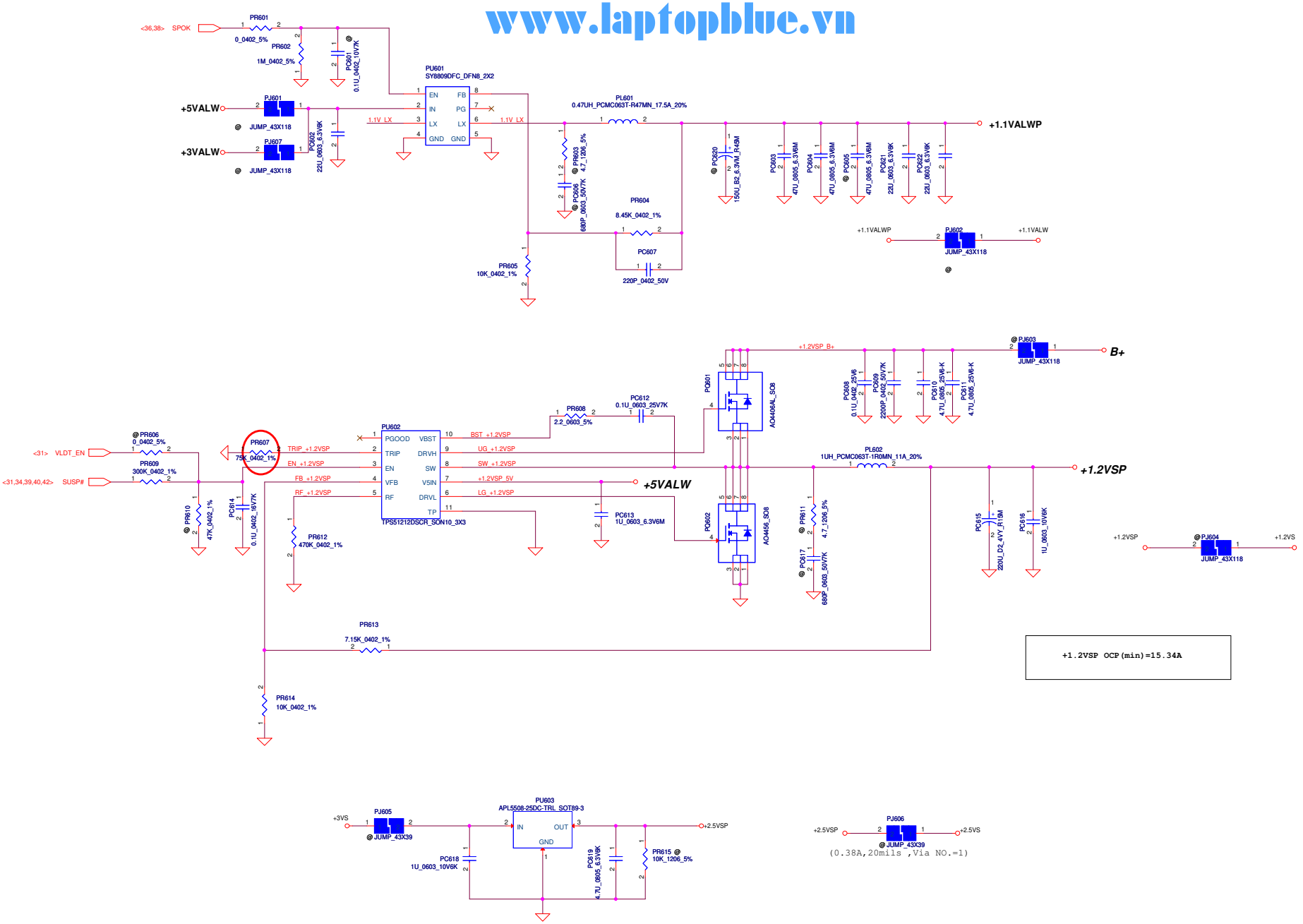
Compal Electronics, Inc.			
Title	PWR-+1.5VP/+0.75VSP/+1.8VSP		
Size: Custom	Document Number: LA9001P		Rev: 0.1
Date: Friday, May 25, 2012	Sheet 39 of 48		

STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off
Note: S3 - sleep ; S5 - power off					



Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

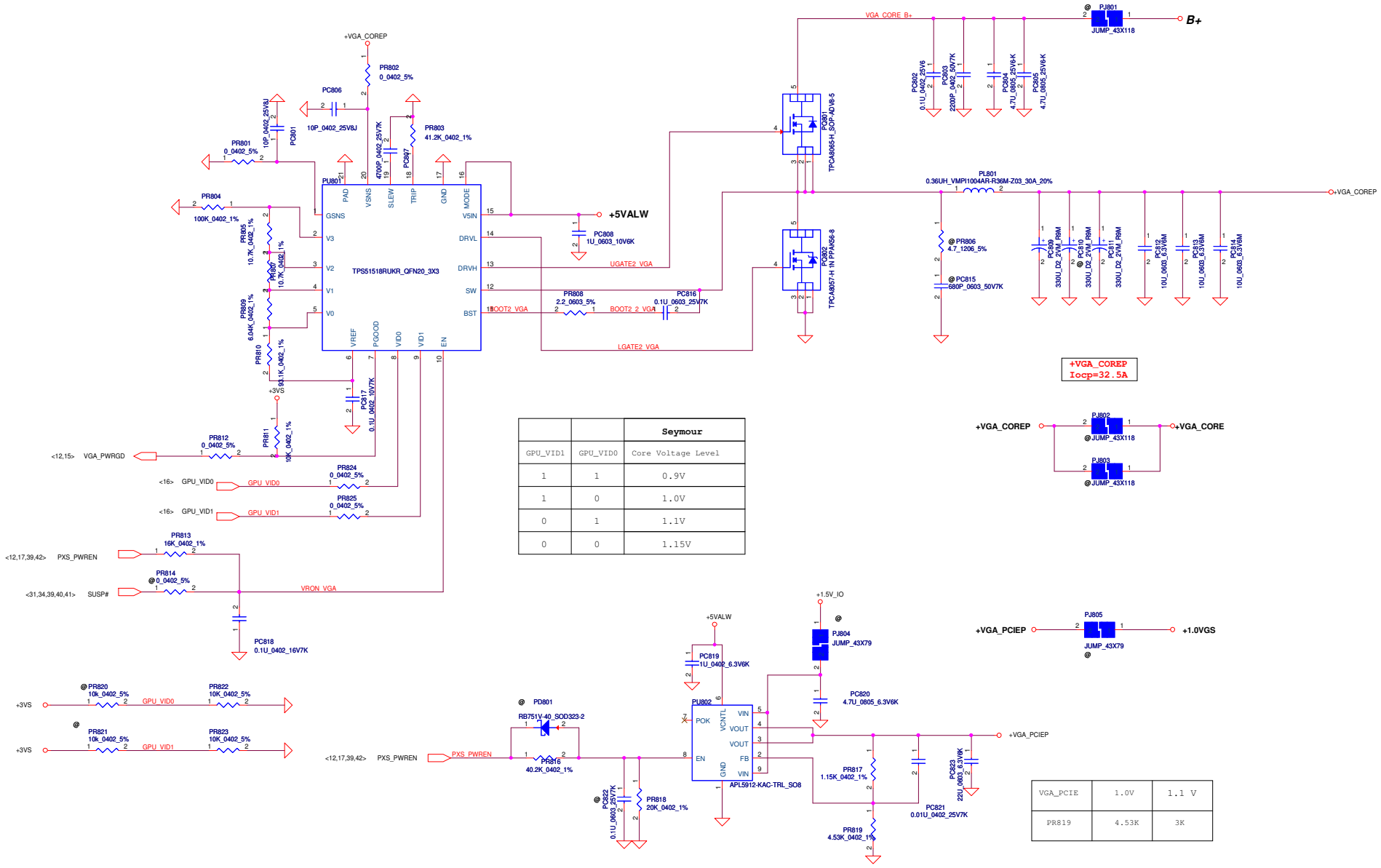
Compal Electronics, Inc.			
Title: PWR-+1.5VP/+1.8VSP			
Size: Custom	Document Number: LA9001P		Rev: 0.1
Date: Friday, May 25, 2012		Sheet 40 of 48	



+1.2VSP OCP(min)=15.34A

Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.			
Title	PWR +1.1VALWP/+1.2VSP/+2.5VSP		
Size C	Document Number LA9001P		Rev 0.1
Date: Friday, May 25, 2012		Sheet 41 of 48	



		Seymour
GPU_VID1	GPU_VID0	Core Voltage Level
1	1	0.9V
1	0	1.0V
0	1	1.1V
0	0	1.15V

VGA_PCIE	1.0V	1.1 V
PR819	4.53K	3K

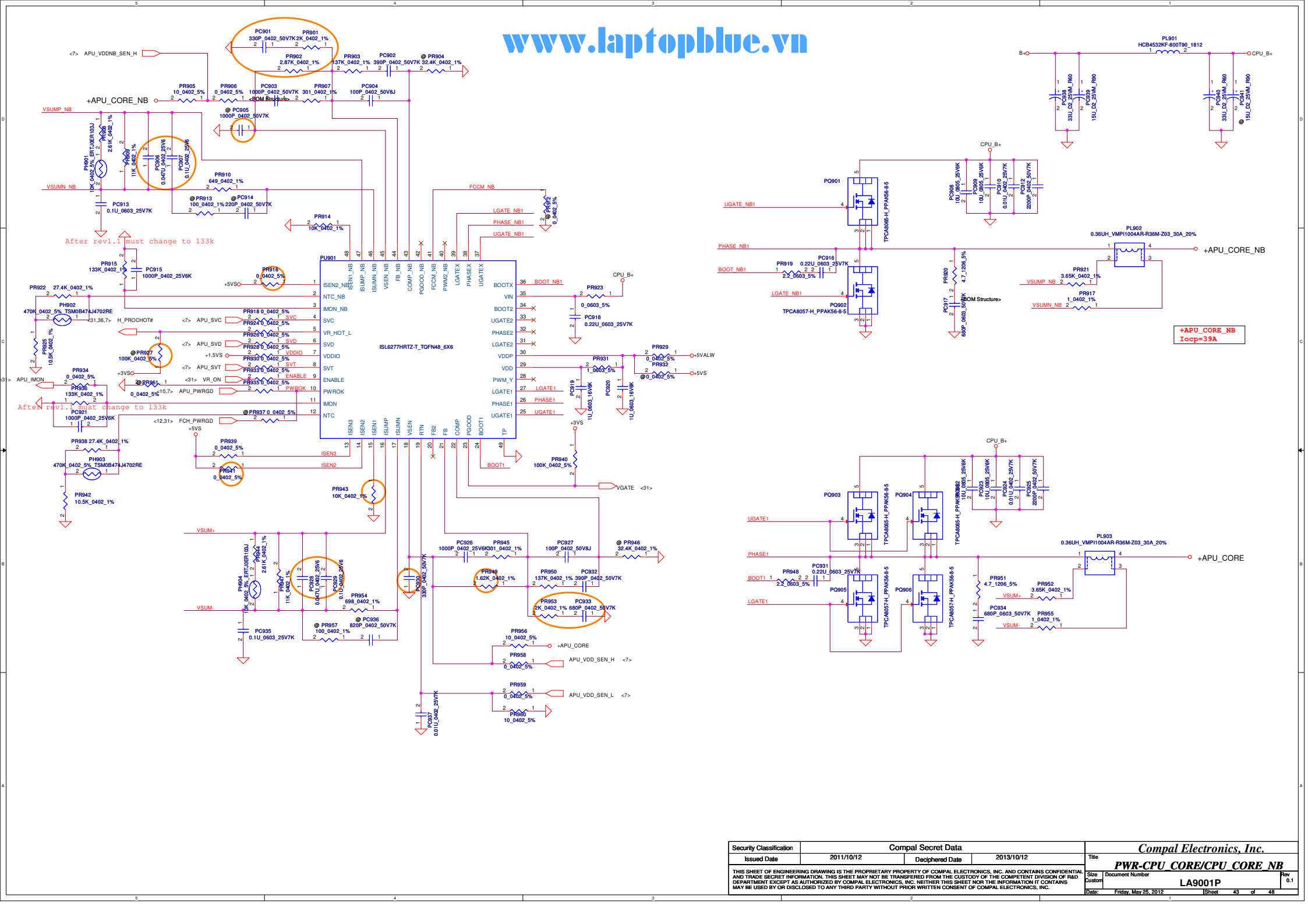
Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: PWR-VGA_CORE/VGA_PCIE

Size | Document Number: LA9001P | Rev: 0.1

Date: Friday, May 25, 2012 | Sheet 42 of 48

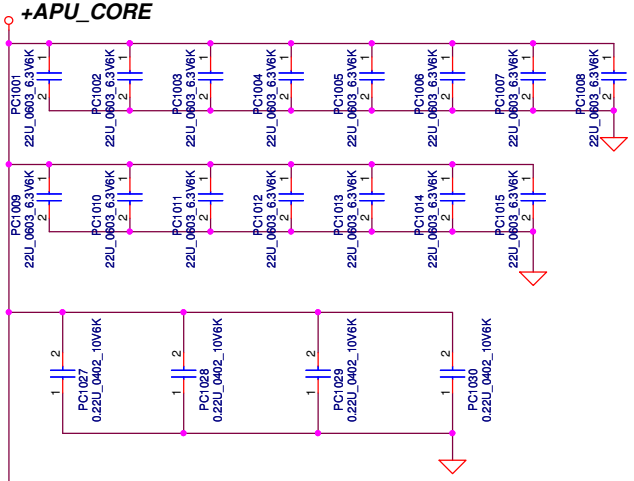


Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

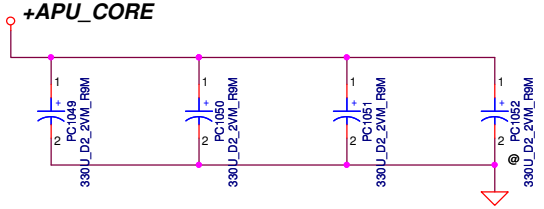
Compal Electronics, Inc.			
Title	PWR-CPU_CORE/CPU_CORE_NB		
Size: Custom	Document Number: LA9001P		Rev: 0.1
Date: Friday, May 25, 2012	Sheet 43 of 48		

+CPU_CORE

+APU_CORE

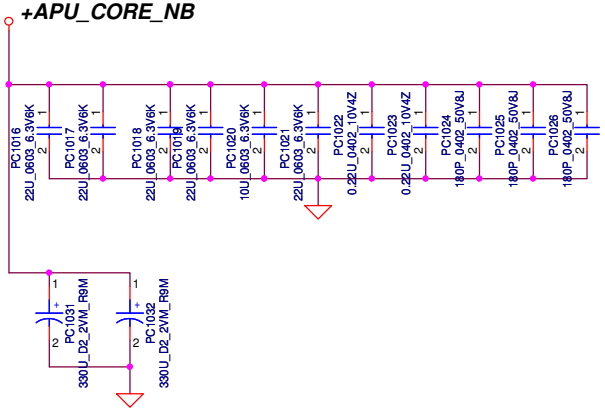


+APU_CORE

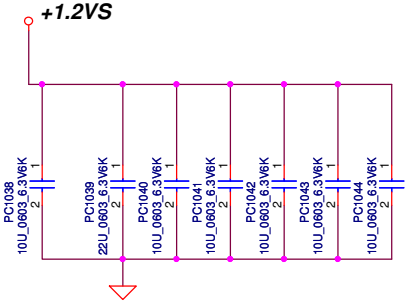


+CPU_CORE_NB

+APU_CORE_NB



+1.2VS



Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: PWR - PROCESSOR DECOUPLING

Size | Document Number: LA9001P | Rev: 0.1

Date: Friday, May 25, 2012 | Sheet 44 of 48

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: **PIR (PWR)**

Size: Custom | Document Number: **LA9001P** | Rev: 0.1

Date: Friday, May 25, 2012 | Sheet 45 of 48

VAUS5 HW PIR List

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE	SDV TO SIV NOTE
1	3/22	26	Change C1204, C1205 from SE071120JN0 to SE071120J80	SE071120JN0 is for A58 only	
2	3/22	27	Modify DL2 from @ to GAS@	For Gastube BOM control	
3	3/22	12	Delete FCH_SEL BOM control	AMD formal announce FP2 only support A70M3	
4	3/22	10	Delete U2 A60MR1 BOM control	AMD formal announce FP2 only support A70M3	
5	3/22	12	Change R117 from PX@ to @, change R155 from @ to always mount	Clock request from GPU will not meet power sequence	
6	3/22	12	Change R1606, R1607 from USBL2@ to @, change R1610, R1611 from USBL3@ to always mount	AMD formal announce FP2 only support A70M3	
7	3/26	10	Change GPIO31 pull high from +3VALW to +3VS	This GPIO pin is Core power rail	
8	4/2	07	Add R215 to pull high +1.5V_APU & @ R36	AMD suggest	
9	4/6	24	Add C1223 1000p	For EMI	
10	4/6	33	Add C1224 1000p	For EMI	
11	4/6	26	Change C1204, C1205 from 12p to 15p	For Vendor tunning value	
12	4/6	16	Change C341, C350 from 15p to 8.2p	For Vendor tunning value	
13	4/6	33	Swap D45	For layout	
14	4/9	31	Change R1564 from 33k to 18k	DVT Board ID	
15	4/9	30	Swap JSPK1	For swap speaker cable	
16	4/9	31	Add VSB_ON on GPIO127	For S5 power saving	
17	4/11	29	Change R1527 to R-short	For cost down	
18	4/11	31	Change R1580, R1586 to R-short	For cost down	
19	4/11	13	Change R167 to R-short	For cost down	
20	4/11	31	Change R1591 to always mount	For MainPowerON power control	
21	4/11	7	Change R51, R52 to R-short	For cost down	
22	4/11	12	Change R1610, R1611 to R-short	For cost down	
23	4/11	17	Change R400 to R-short	For cost down	
24	4/11	22	Mount R200, @ L171, C238, C239	For LVDS Translator 1.2 power rail	
25	4/11	26	Change R1515, R1508 to R-short	For cost down	
26	4/11	27	Delete J17, J19	For LAN surge solution change	
27	4/12	5	Change A6, A10 APU R1 PN	From PC sample to PR sample	
28	4/13	17,19	Change BIF_VDDC to VGA_CORE and move C343 to Page 19	For PX5 only	
29	4/16	27	Change CHASSIS2_GND to GND & CHASSIS1_GND	For common LAN surge solution	
30	4/17	33	Mount L43, L44, L45, @ R1605, R1608, R1609, R1612, R1613, R1616	For EMI (USB3.0 choke)	
31	4/17	32	Add L50, L51, L52 @ R1614, R1615, R1619, R1624, R1625, R1626	For EMI (USB2.0 choke from SB to MB)	
32	4/17	30	Change R937, R1548 from 0 ohm to L172, L173 300ohm Bead	For EMI (DMIC DATA , CLK)	
33	4/17	7	Change R26,R28 from 1k to 10k	For APU_SIC, SID 0'C shut down issue workaround	
34	4/18	7	Change back R26,R28 from 10k to 1k, and mount C5988	For APU_SIC, SID 0'C shut down issue	

Compal Electronics, Inc.

Title: HW-PIR

Size: Custom | Document Number: VAUS5 LA9001P M/B | Rev: 0.3

Date: Friday, May 25, 2012 | Sheet 46 of 50

VAUS5 HW PIR List

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE	SIV TO SIT NOTE
1	5/11	16	Change Q64 from SB00000EO10 to SB00000DH00	For BOM reduce	
2	5/11	23	Reserve R1466	For factory requirement to prevent DISPOFF# damage	
3	5/11	25	Add BOM structure SSD@ for SSD function	For BOM option	
4	5/14	24	Reserve ESD component D1,D2 for HDMI signal	For HDMI hot-plug protection	
5	5/21	7 13 25 26 30	0402 R-Shot modify R24,R160,R161,R158,R163,R171,R169,R166,R1491,R1492 0603 R-Shot modify R157,R164,R170,R172,R168,R159,R1529,L35,L36 0805 R-Shot modify R162,R165,R1531	For BOM reduce	
6	5/21	31	Change R1564 from 18K to 8.2K	For Board ID change	
7	5/22	7	Change back R24 from R-shot to 0ohm		
8	5/22	24	Reserve ESD component D69 for HDMI SMBus	For APU damage when HDMI hot-plug	
9	5/24	25	Reserve R1493	For Intel 2230 WLAN Card Support	
10	5/24	20	Add VRAM Samsung 1G K4W2G1646E-BC11 strap setting	For customer request	
11	5/24	24	Un-mount D1, D2		
12	5/24	12	Change back R1610, R1611 footprint to 0ohm		
13	5/25	30	Add C83, C84 for DMIC noise issue	For EMI request	
14	5/25	27	Change DL2 PN to SCV00001D00	For customer request	
15	5/25	10 25	Add BT_OFF# for other BT combo card	For customer request	
16	5/29	26	Un-mount C1197. C1198 and mount C1200,C1203	For LAN power trace rounting	
17	5/29	7	Change Q3,Q4 PN from SB501110010 to SB501380050	For PUR request	
18	5/29	30	Change R1530 PN from SM01000DI00 to SM010005X00	For PUR request	
19	5/31	23 25 32 33	Change C8244,C8245,C8246,C8247,C8248 and C8249 from 10p to 15p	For AMD suggest	

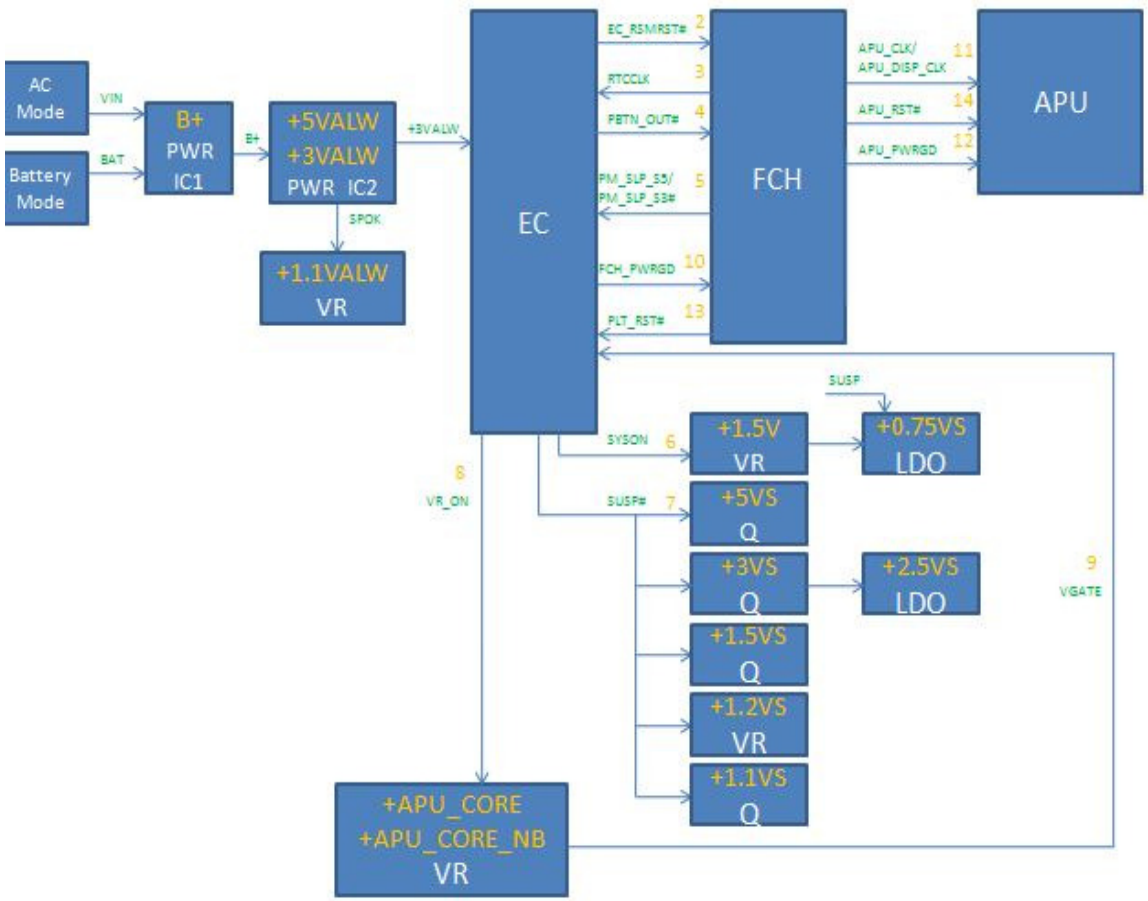
Compal Electronics, Inc.

Title: HW-SIT PIR

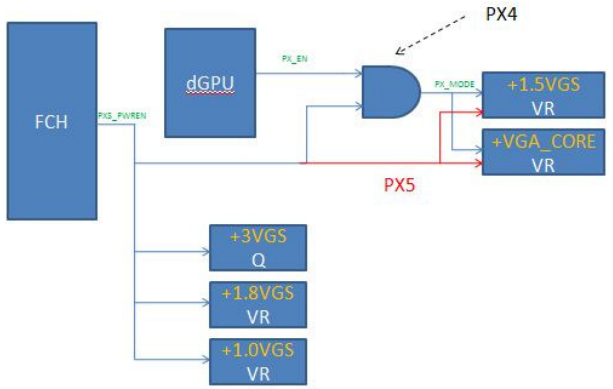
Size: Custom | Document Number: VAUS5 LA9001P M/B | Rev: 0.3

Date: Thursday, May 31, 2012 | Sheet 47 of 50

SYSTEM



VGA



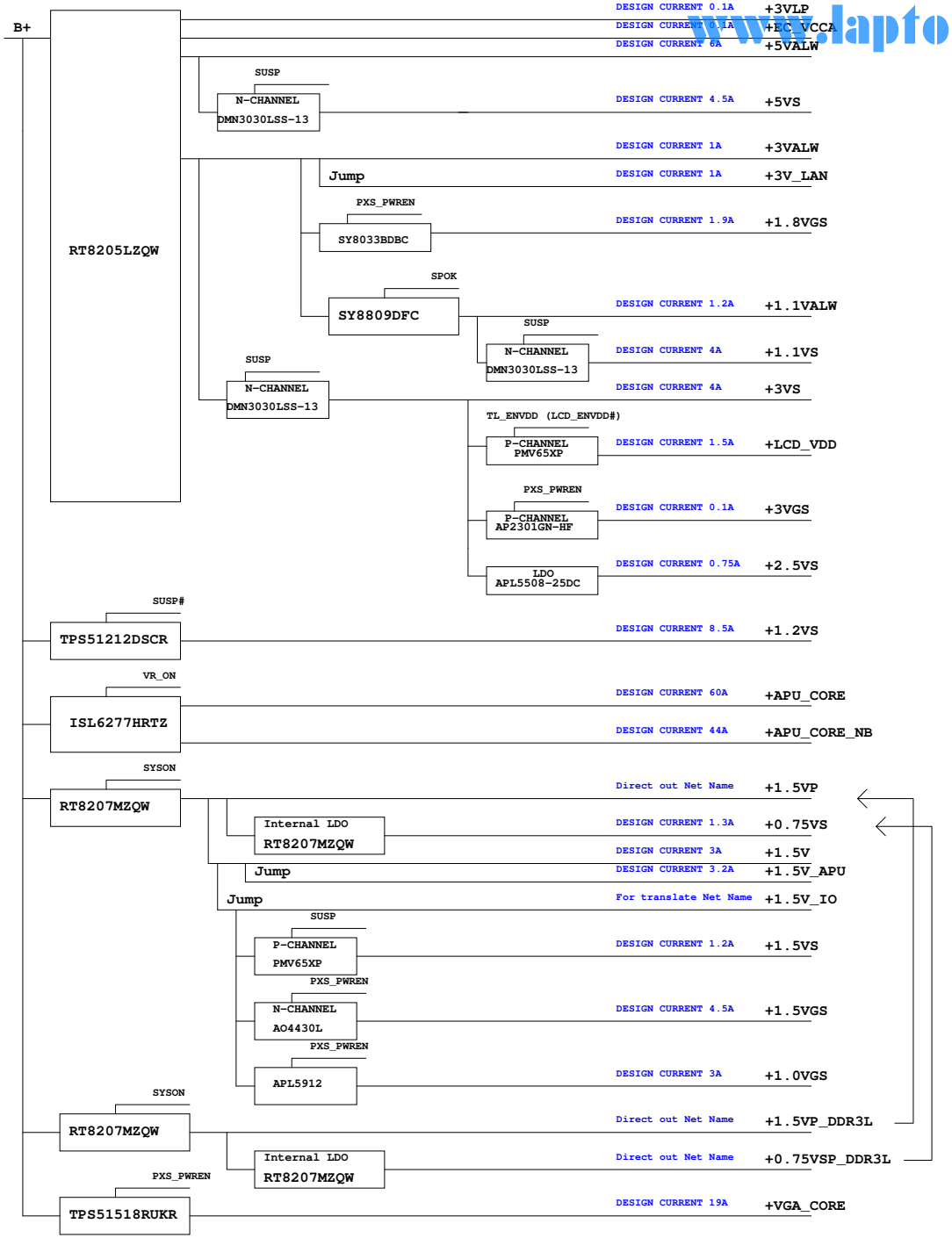
Security Classification	Compal Secret Data		
Issued Date	2012/01/15	Deciphered Date	2013/01/15

Compal Electronics, Inc.

Title: Power sequence

Size: Custom | Document Number: VAUS5 LA9001P M/B | Rev: 0.3

Date: Friday, May 25, 2012 | Sheet 48 of 50



Security Classification	Compal Secret Data		
Issued Date	2011/12/30	Deciphered Date	2013/10/05

Compal Electronics, Inc.

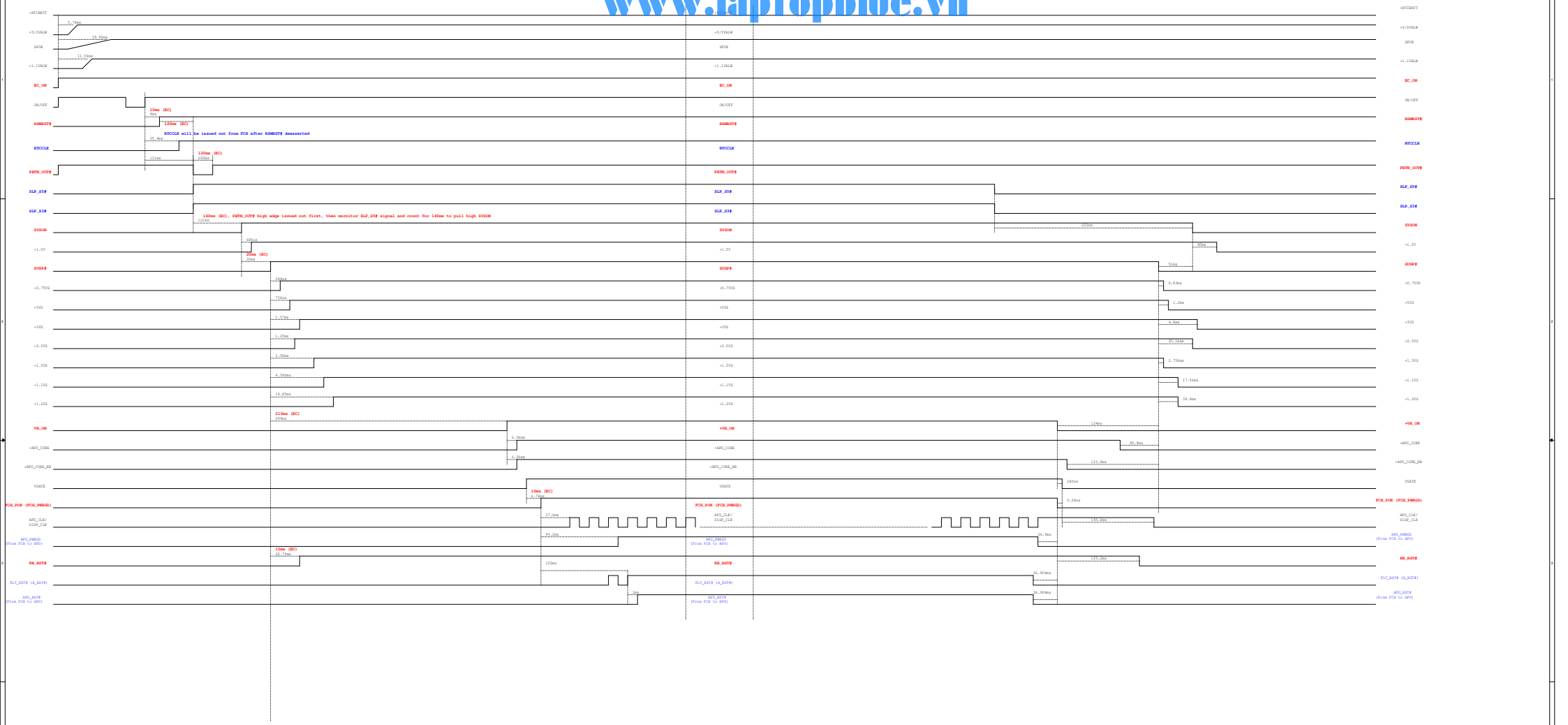
Title: **Power Map**

Size	Document Number	Rev
Custom	VAUS5 LA9001P M/B	0.3

Date: Friday, May 25, 2012 Sheet 49 of 50

VAUS5 Power on / off sequence (AC mode)

S5 - S0 - S5



Security Classification	Compal Secret Data		
Issued Date	2009/10/02	Deciphered Date	2010/10/02

Compal Electronics, Inc.	
Title	S5_Power Sequence
Size	Document Number
Rev	0.3
Date: Friday, May 25, 2012	Sheet 50 of 50