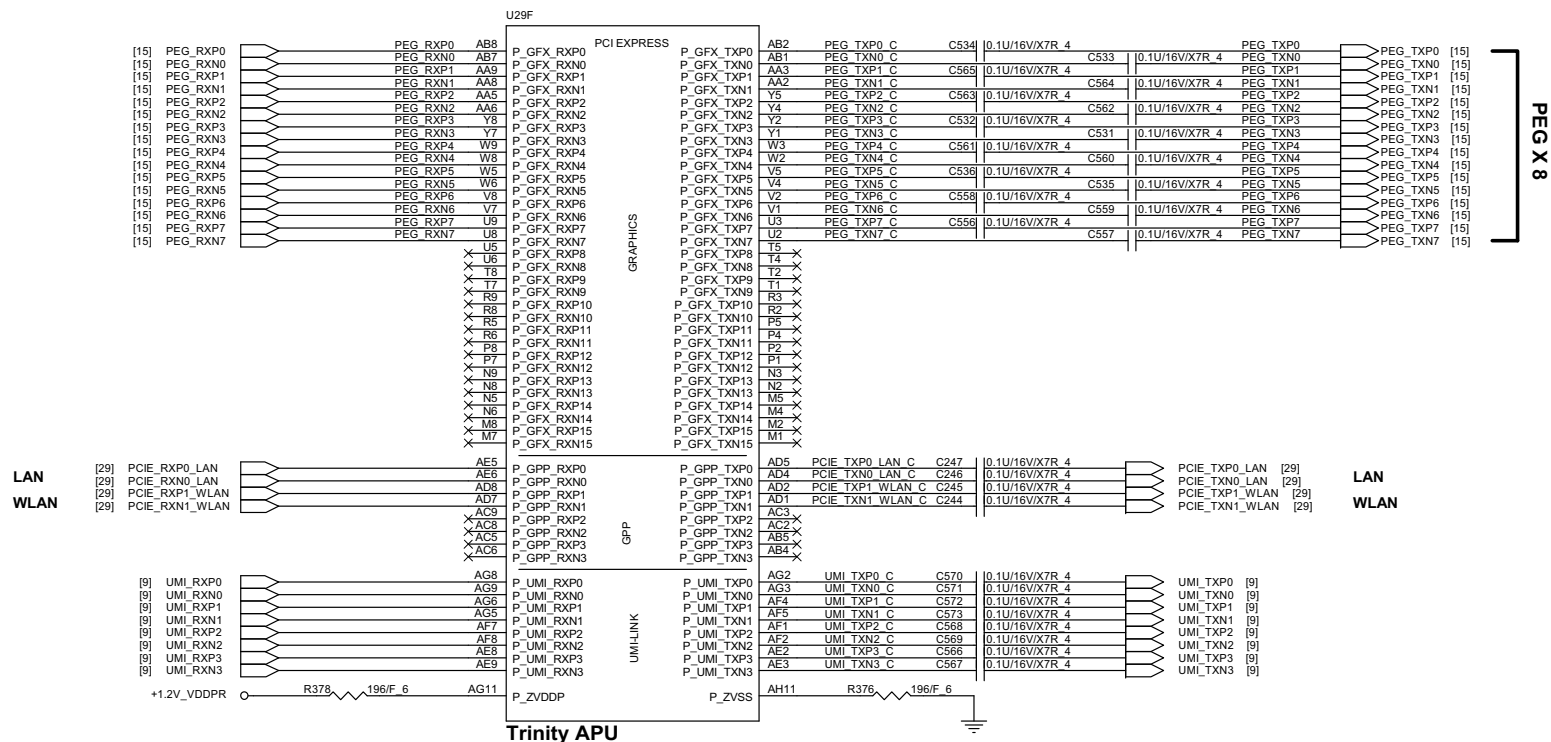
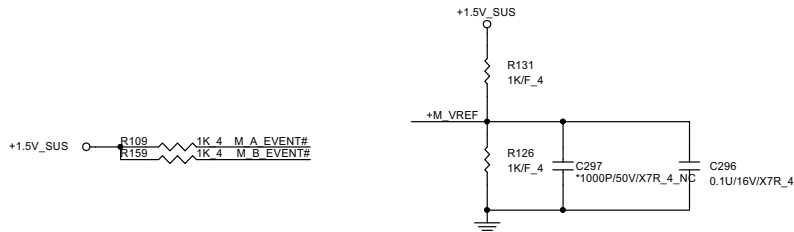
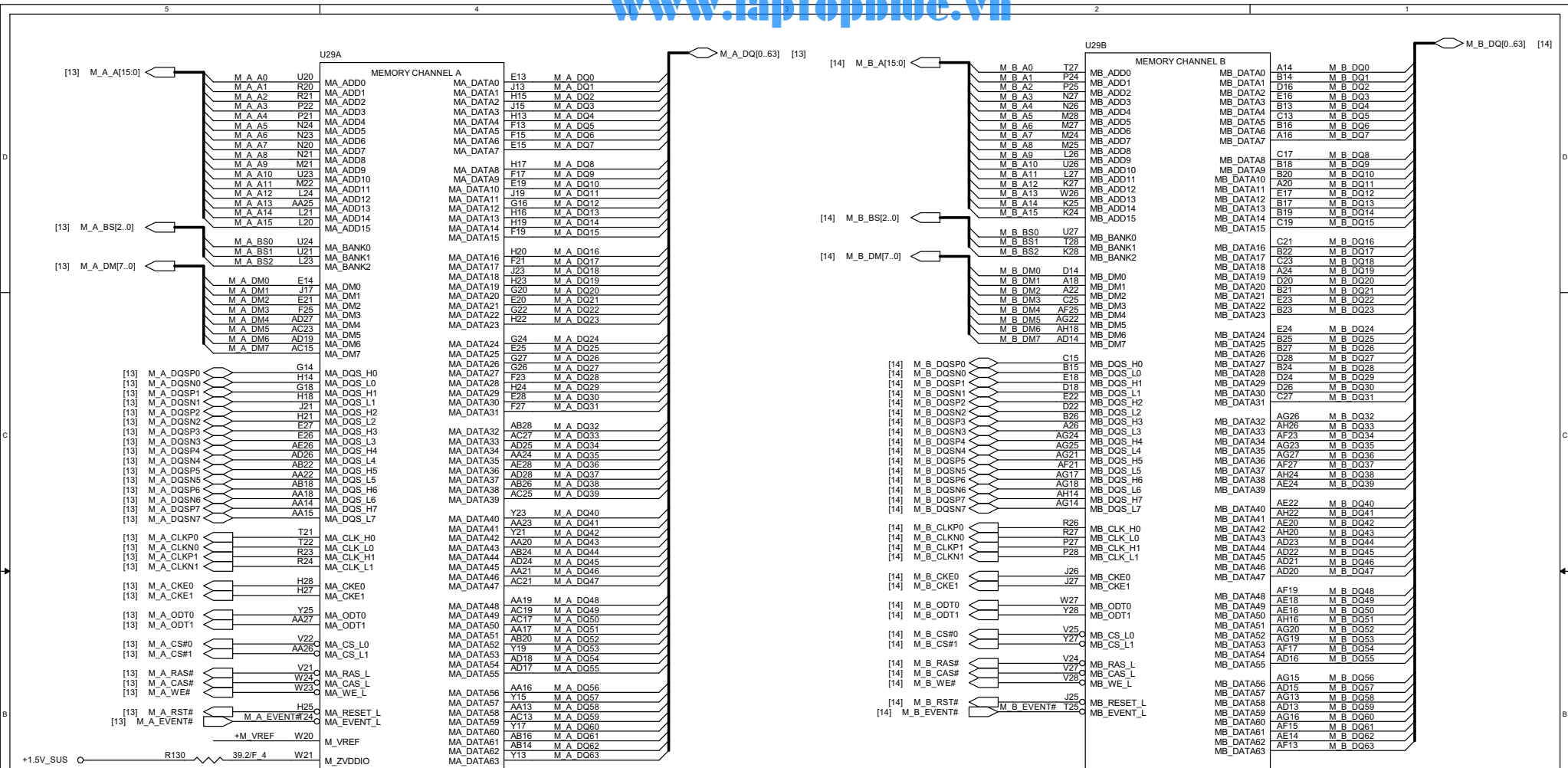


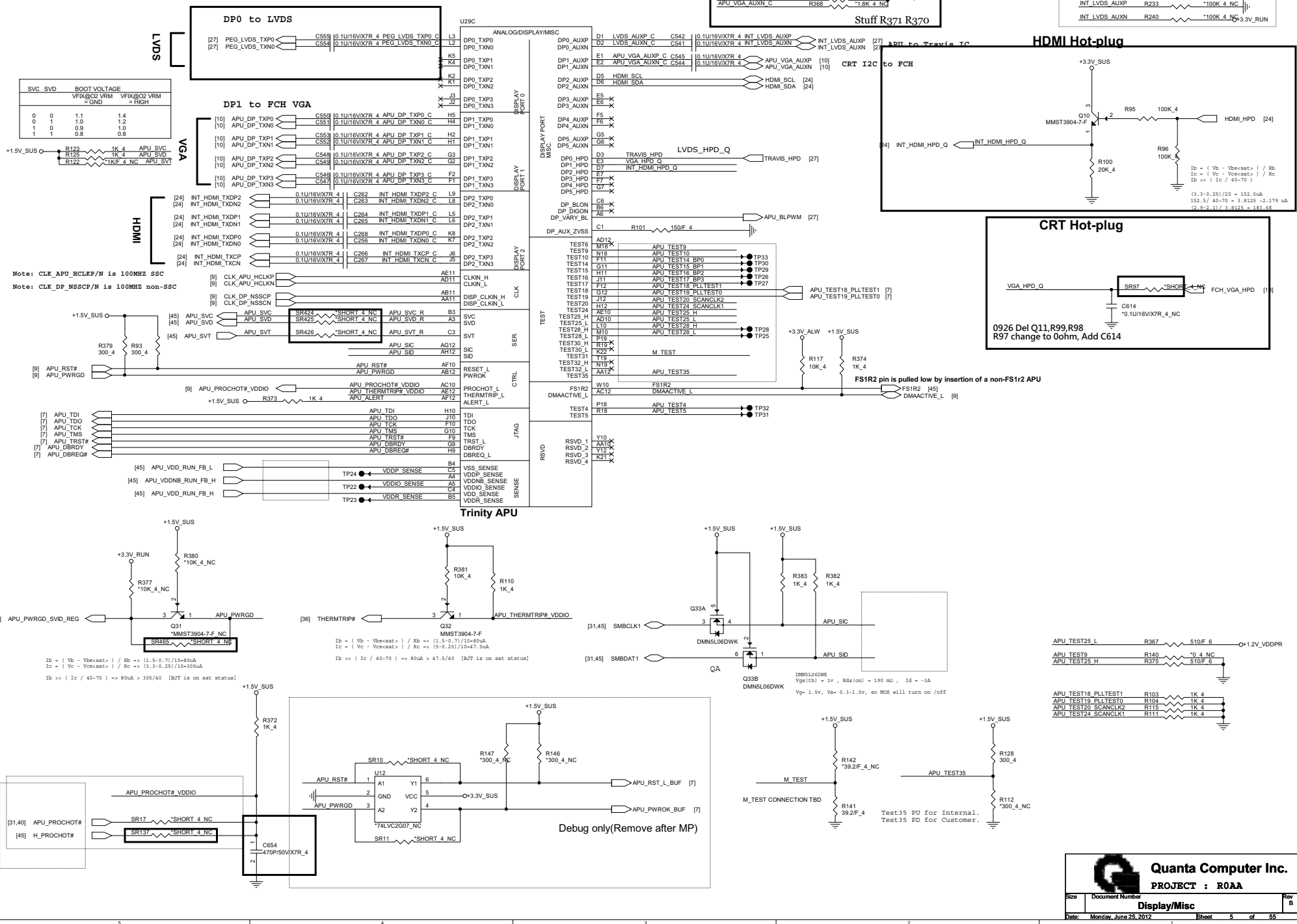
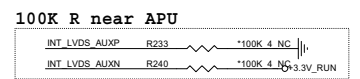
USB Master	Port Assignment
USB0	DEBUG
USB1	MiniCard 1 (WLAN/BT)
USB2	NC
USB3	NC
USB4	NC
USB5	NC
USB6	NC
USB7	Card Reader
USB8	NC
USB9	Camera
USB10	External port#1 (USB3.0)
USB11	External port#2 (USB3.0)
USB12	External port#3 (USB3.0)
USB13	External port#4 (Power share)

SATA Master	Port Assignment
SATA0	HDD
SATA1	ODD
SATA2	NC
SATA3	NC
SATA4	NC
SATA5	NC

PCIE Master	Port Assignment
CPU_GPP 0	LAN
CPU_GPP 1	WLAN
CPU_GPP 2	NC
CPU_GPP 3	NC
FCH_GPP 0	NC
FCH_GPP 1	NC
FCH_GPP 2	NC
FCH_GPP 3	NC

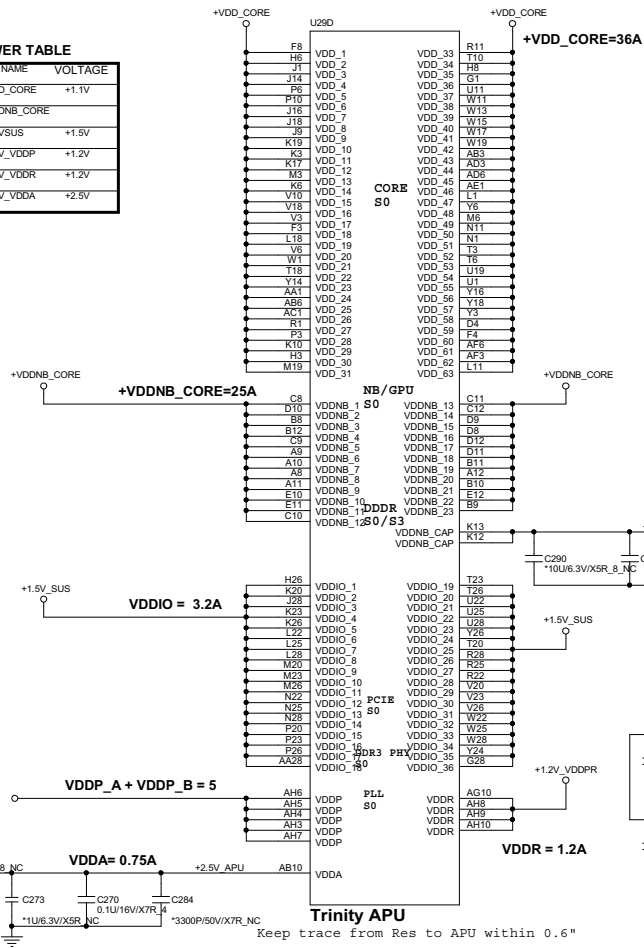






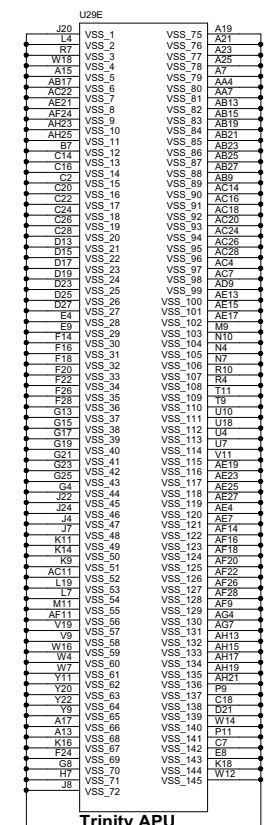
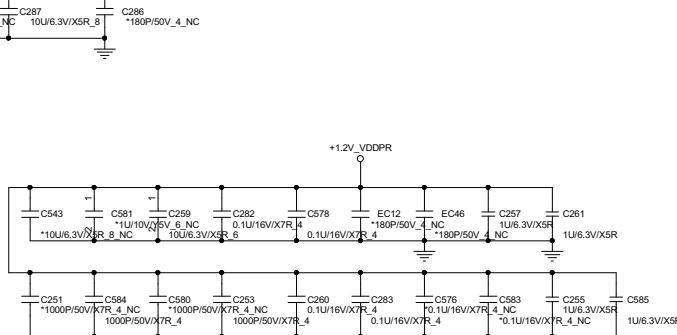
APU POWER TABLE

PIN NAME	NET NAME	VOLTAGE
VDD	+VDD_CORE	+1.1V
VDDNB	+VDDNB_CORE	
VDDIO	+1.5V_SUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V

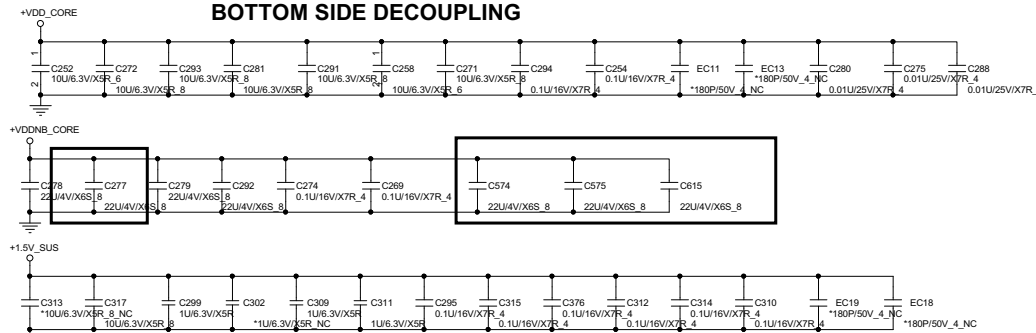


Sequence
GROUP A (VDDIO, VDDA)
!!!
GROUP B (VDD_RUN, VDDNB_RUN, VDDP, VDDR)

New Add Internal Regulator



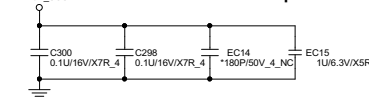
BOTTOM SIDE DECOUPLING



If the VSS plane is cut to create a VDDIO plane, ceramic capacitors are connected across the VDDIO and VSS plane split as follows

DECOUPLING between PROCESSOR and DIMMs

Across VDDIO and VSS split



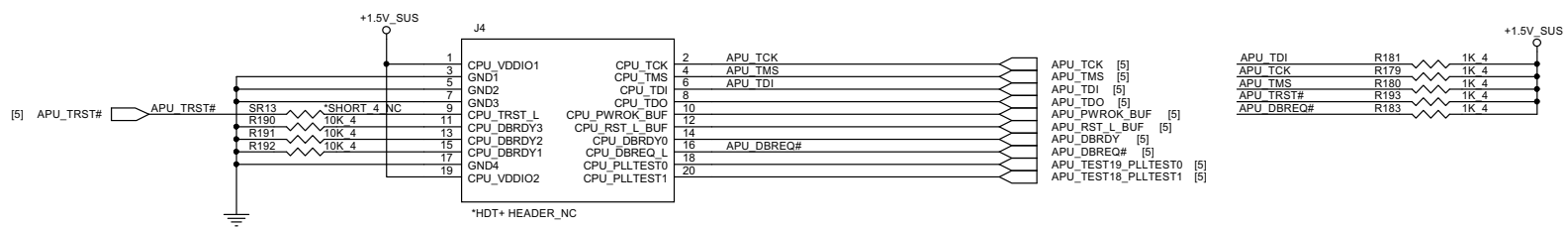
Quanta Computer Inc.

PROJECT : R0AA

Size Document Number
POWER/GND
Date: Monday, June 25, 2012 Sheet 6 of 55

HDT+ Connector Debug only

Remove after MP

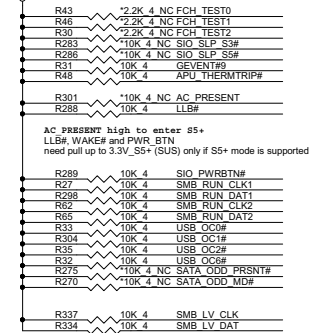


DEL MEMHOT# Function / +3.3V

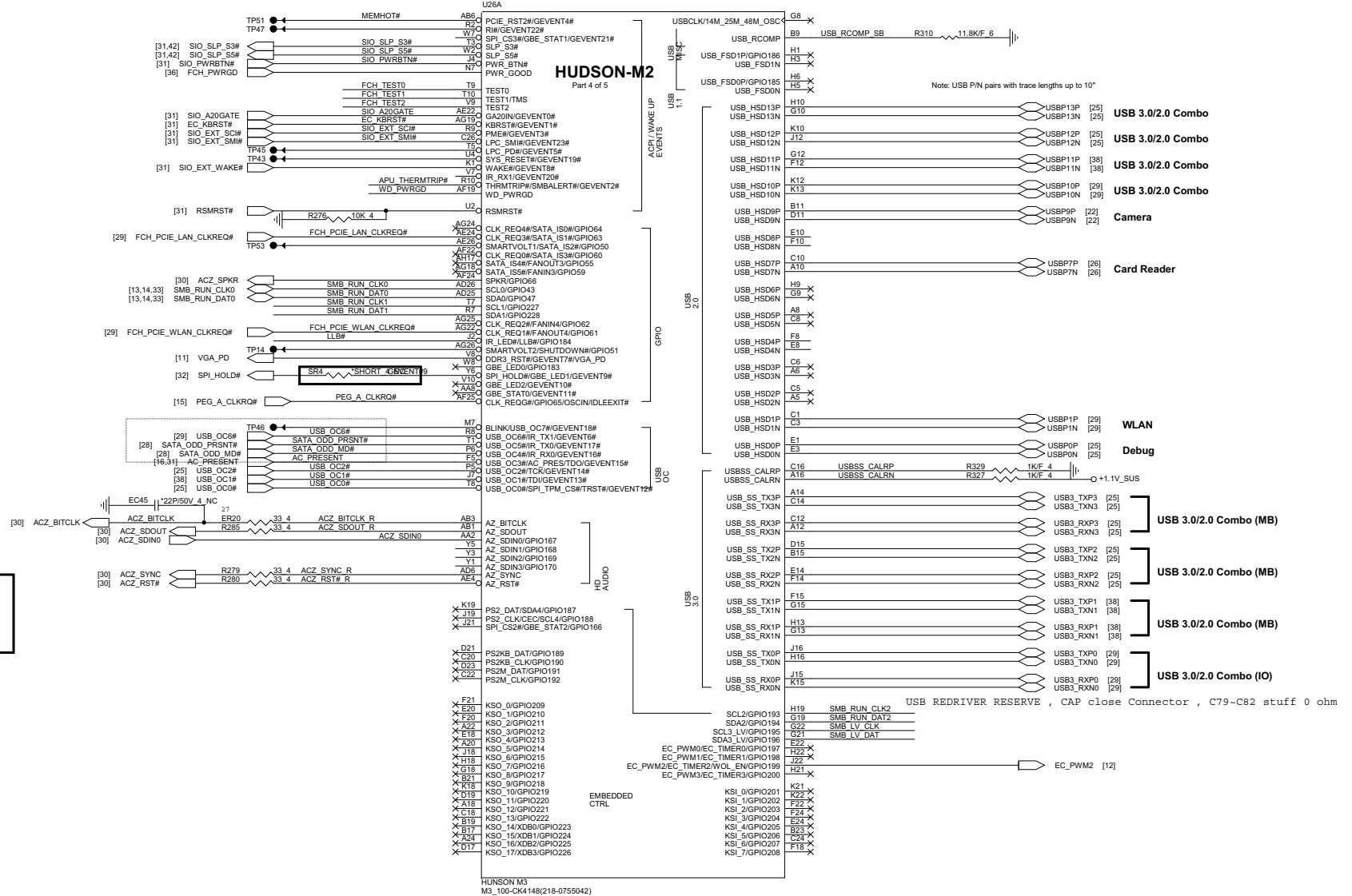
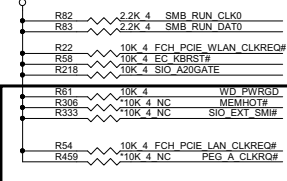
USB_OC#

Function	FCH port
USB12 (MB)	USB_OC0#
USB13 (MB)	*USB_OC2#
USB11 (MB)	USB_OC1#
USB10 (I/O)	USB_OC6#

NC,no install by default



+3.3V_RUN

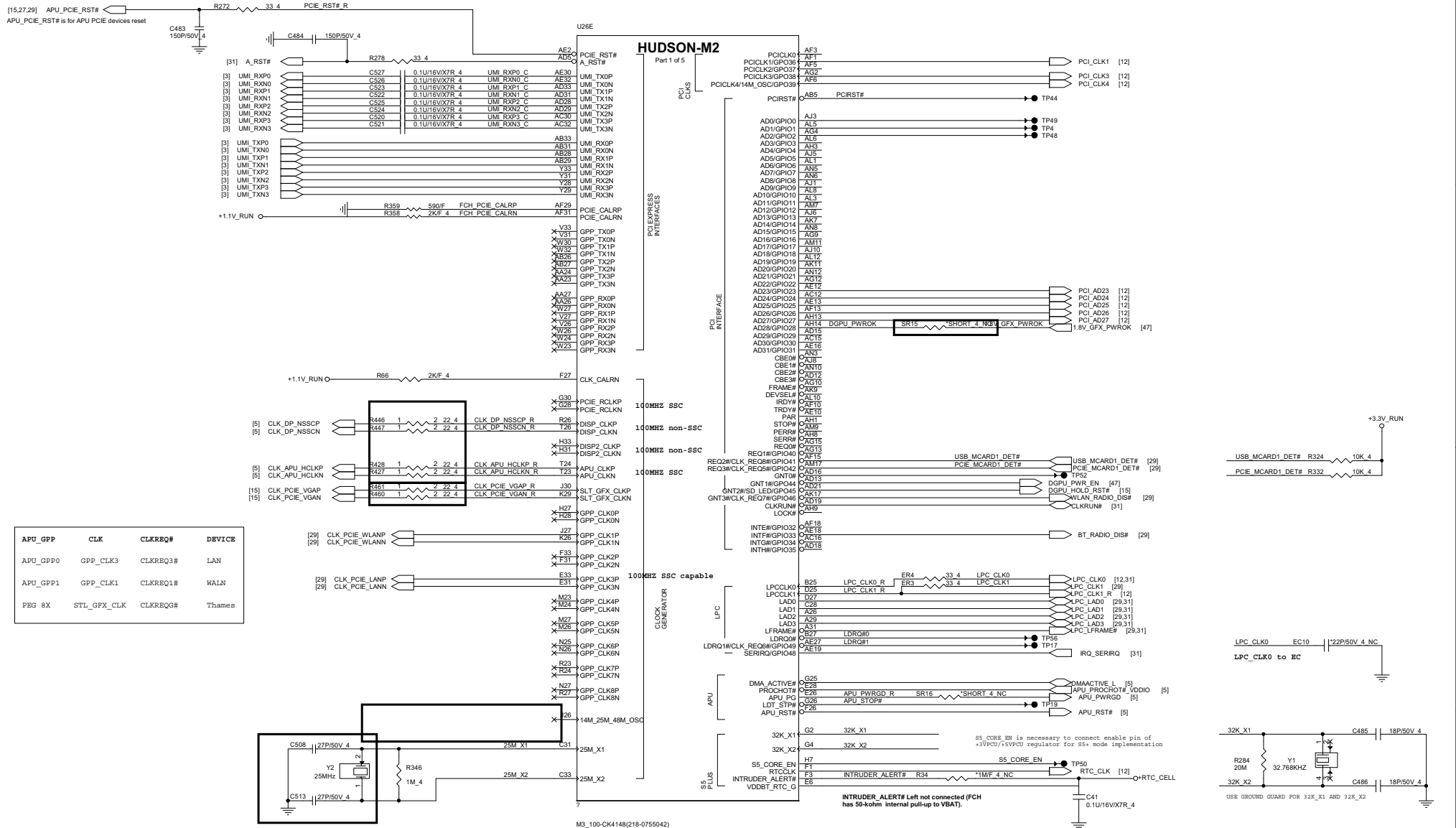


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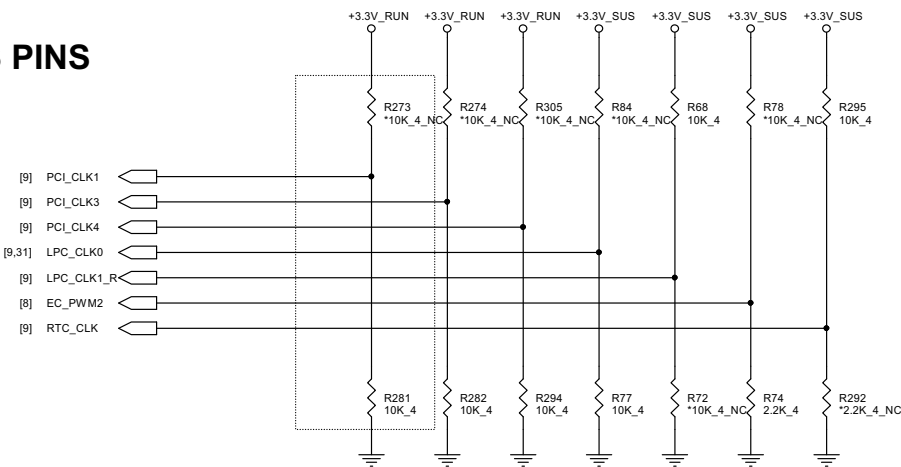
PROJECT : R0AA

Size	Document Number	Rev
	Hudson-M3 GPIO/USB/AZ/RGMII	B
Date	Monday, June 25, 2012	Sheet 8 of 55

Date: Monday, June 25, 2012 Sheet 8 of 55



STRAPS PINS

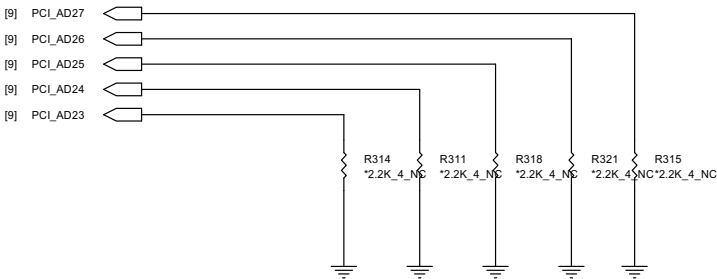


REQUIRED STRAPS

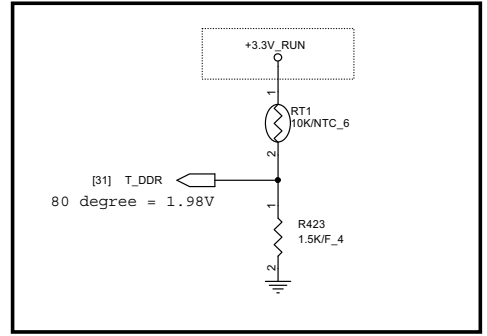
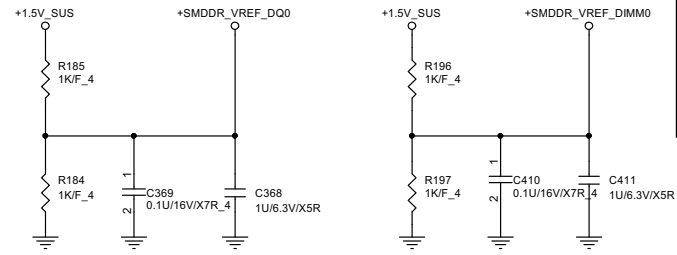
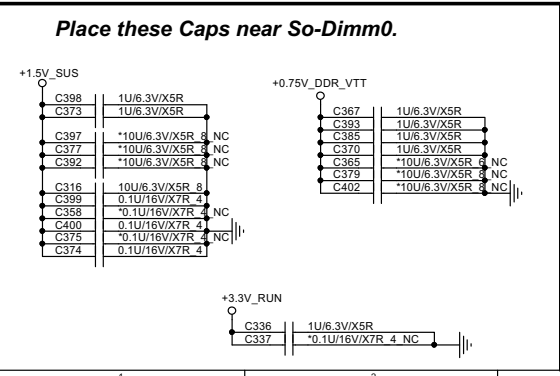
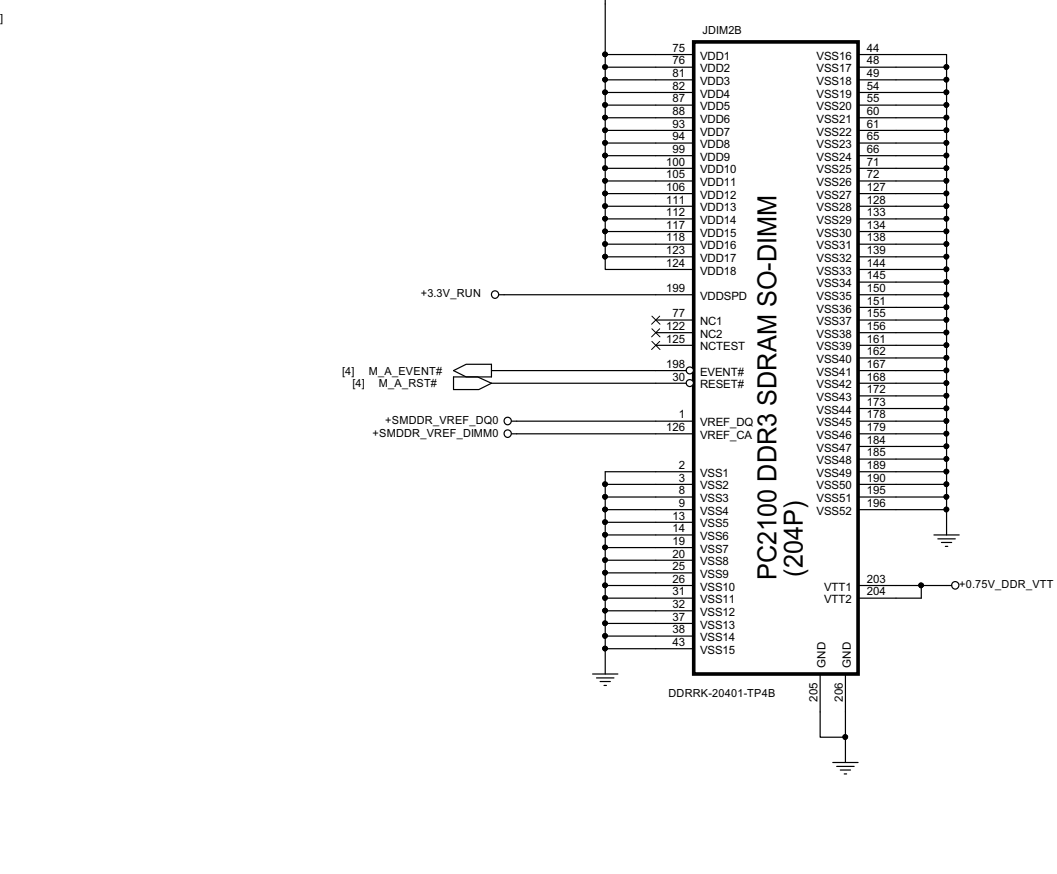
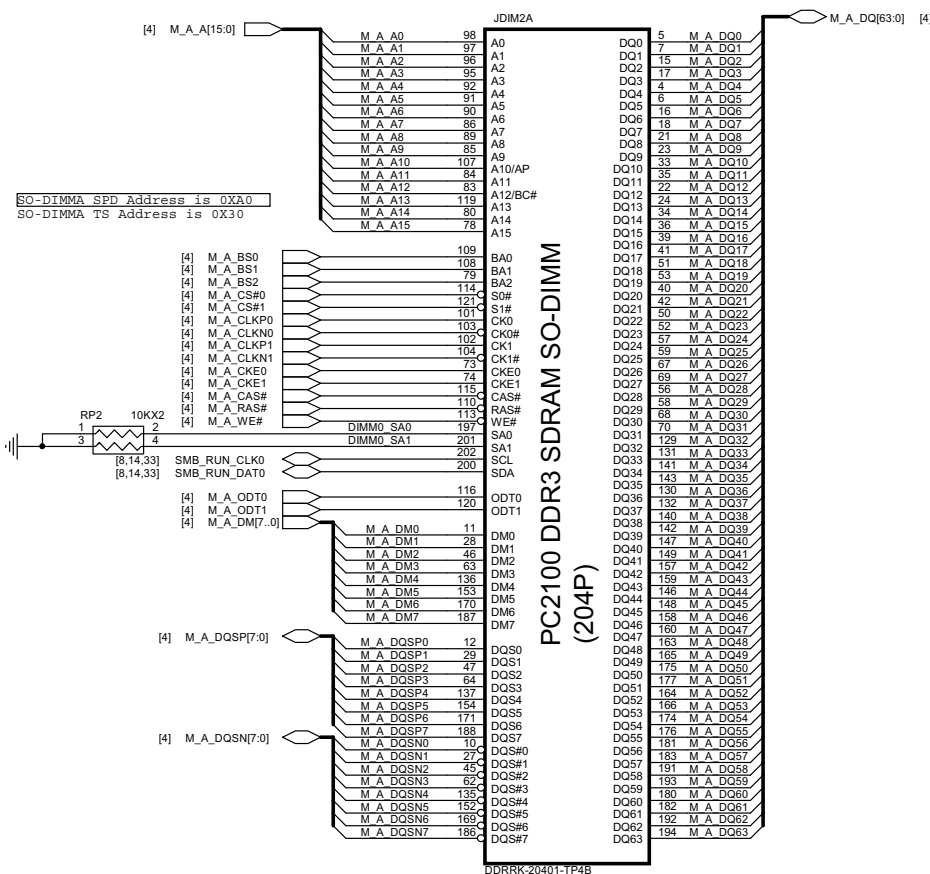
	-----	PCI_CLK1	-----	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	-----	ALLOW PCIE Gen2	-----	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED Setting	LPC ROM	S5 PLUS MODE DISABLED Setting
PULL LOW	-----	FORCE PCIE Gen1 Setting	-----	IGNORE DEBUG STRAP Setting	FUSION CLOCK MODE Setting	EC DISABLED Setting	CLKGEN DISABLED	SPI ROM Setting	S5 PLUS MODE ENABLED

DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

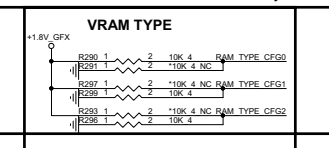
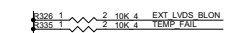
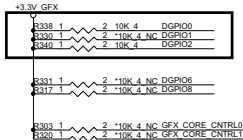


	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL Setting	DISABLE ILA AUTORUN Setting	USE FC PLL Setting	USE DEFAULT PCIE STRAPS Setting	DISABLE PCI MEM BOOT Setting
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

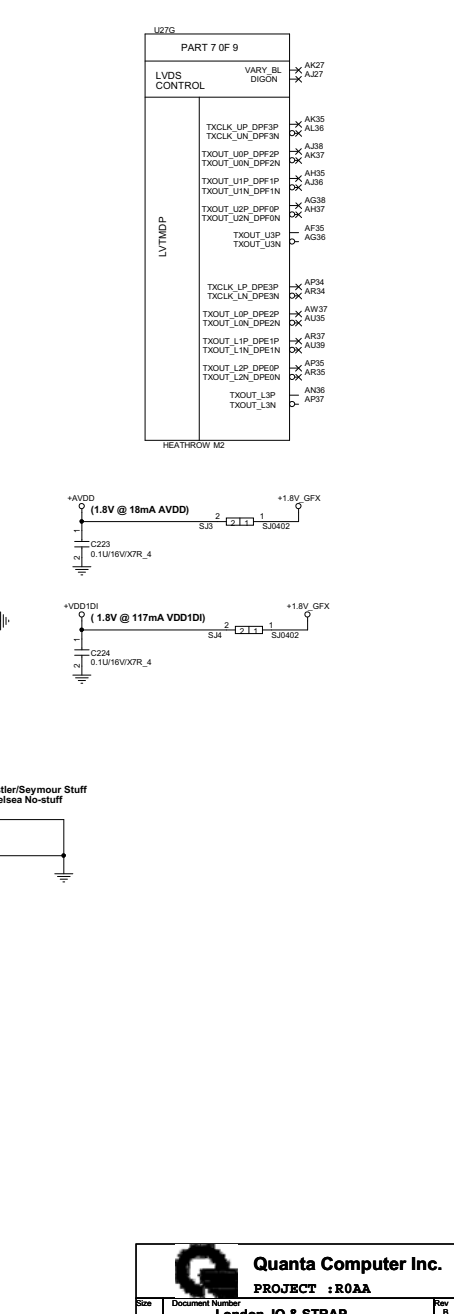
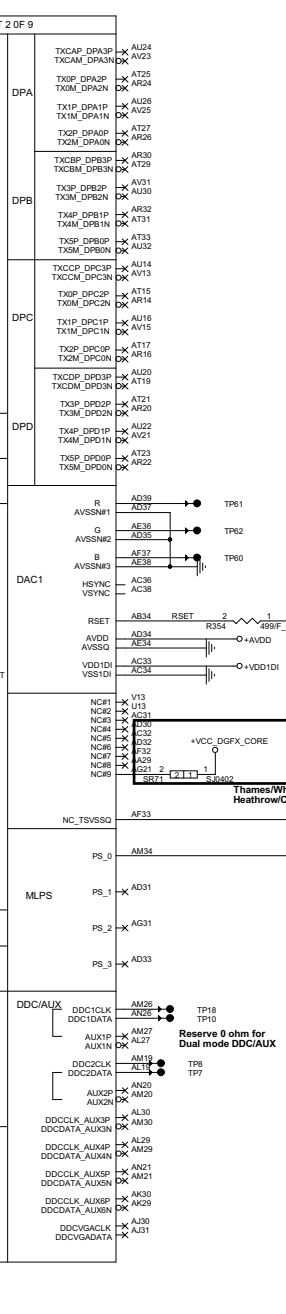
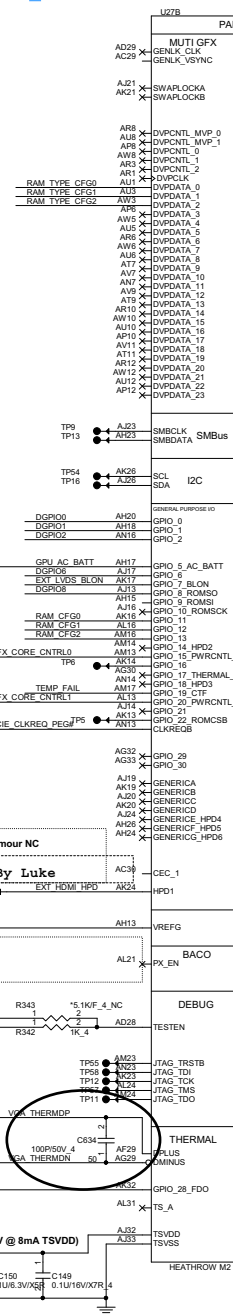
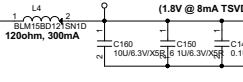
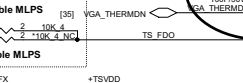
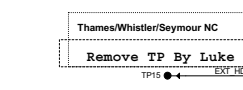
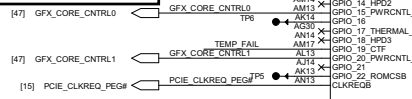
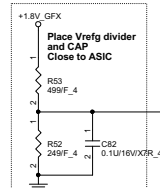
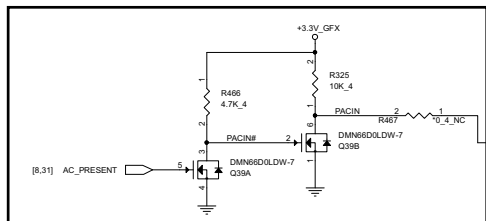


CONFIGURATION STRAPS			
STRAPS	PIN	DESCRIPTION	SET
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING 0 = 50% Tx output swing 1 = Full Tx output swing	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = Disable; 1 = Enable	0
BIF_GEN3_EN_A	GPIO2	PCIE Gen2 Enable 0 = GEN2 not supported at power-on 1 = GEN2 supported at power-on	1
BIF_VGA_DIS	GPIO9	0: VGA Controller capacity enabled 1: VGA Controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 = Disable; 1 = Enable	0
AUD[1] AUD[0]	VGAHSYNC VGA_VSYNC	AUD[1:0]: 00 - No audio function; 01 - Audio for DisplayPort only; 10 - Audio for DisplayPort and HDMI if dongle is detected; 11 - Audio for both DisplayPort and HDMI.	00
CEC_DIS	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0 = Disable; 1 = Enable	0
RESERVED RESERVED RESERVED	GENLK_CLK GPIO8 GPIO21 GENERICC	Allow for Pull-up PADS for the reserved straps but do not install resistor If these GPIOs are used, they must keep low and not conflict during reset	

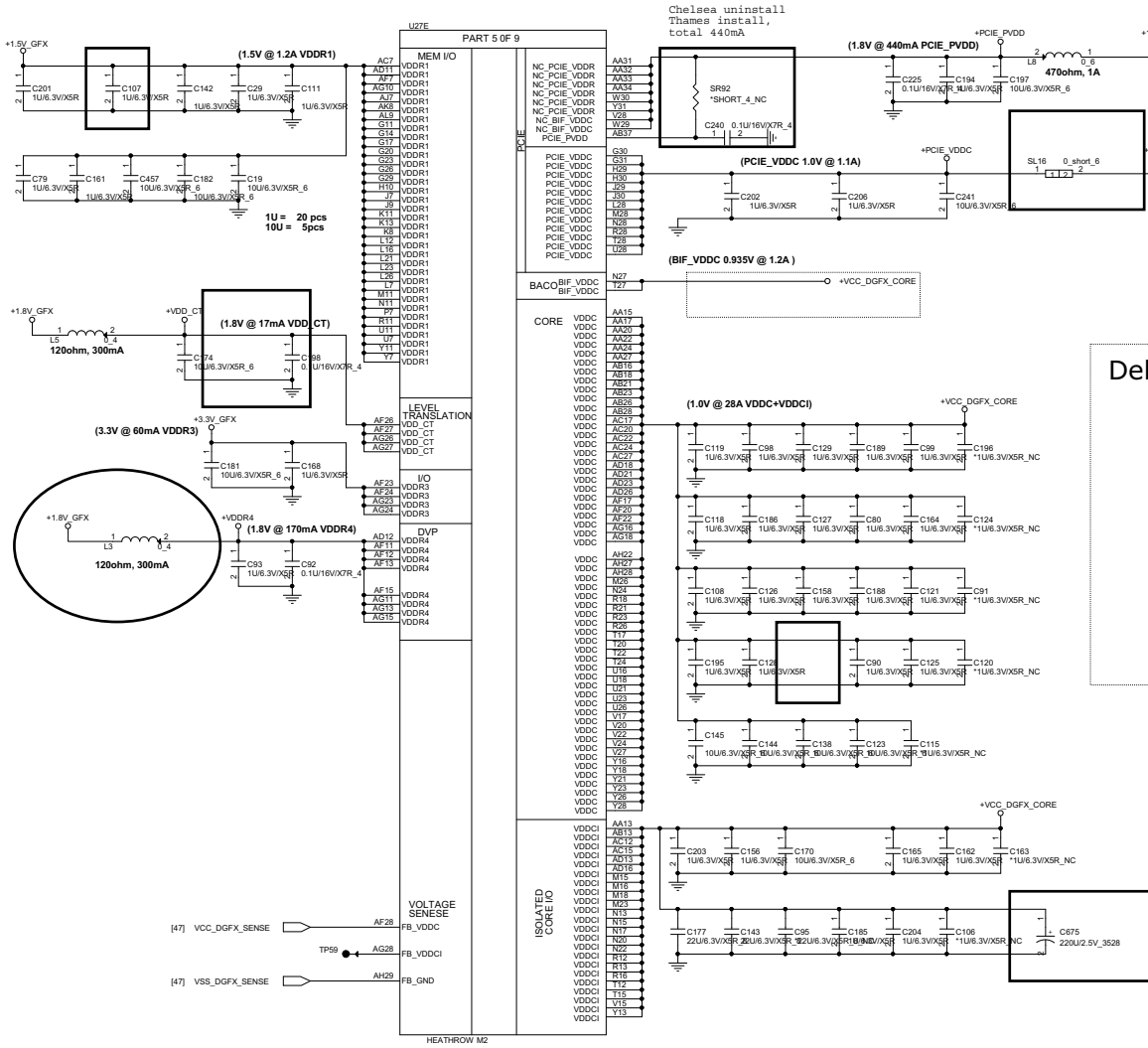
APERTURE SIZE			
MEMORY SIZE	CFG2 GPIO13	CFG1 GPIO12	CFG0 GPIO11
128MB	0	0	0
256MB	0	0	1
64MB	0	1	0



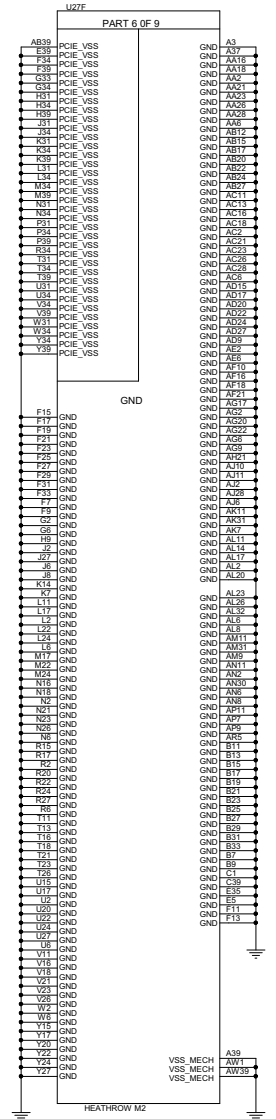
Memory Straps	RAM_TYPE_CFG2	RAM_TYPE_CFG1	RAM_TYPE_CFG0	Quanta PN (QuantaBuy)	Vendor PN	Support GPU
900MHz Samsung 1GB(64M*16*8pcs)	0	0	1	AKD5BQGT509	K4W1G1646G-BC11	For Thames
900MHz Hynix 1GB(64M*16*8pcs)	0	1	0	AKD5LZW7W07	H5TQ1G63DPR-11C	For Thames
900MHz Micron 1GB(64M*16*8pcs)	1	0	0	AKD5EGSTL01	MT41J64M16JT	For Thames

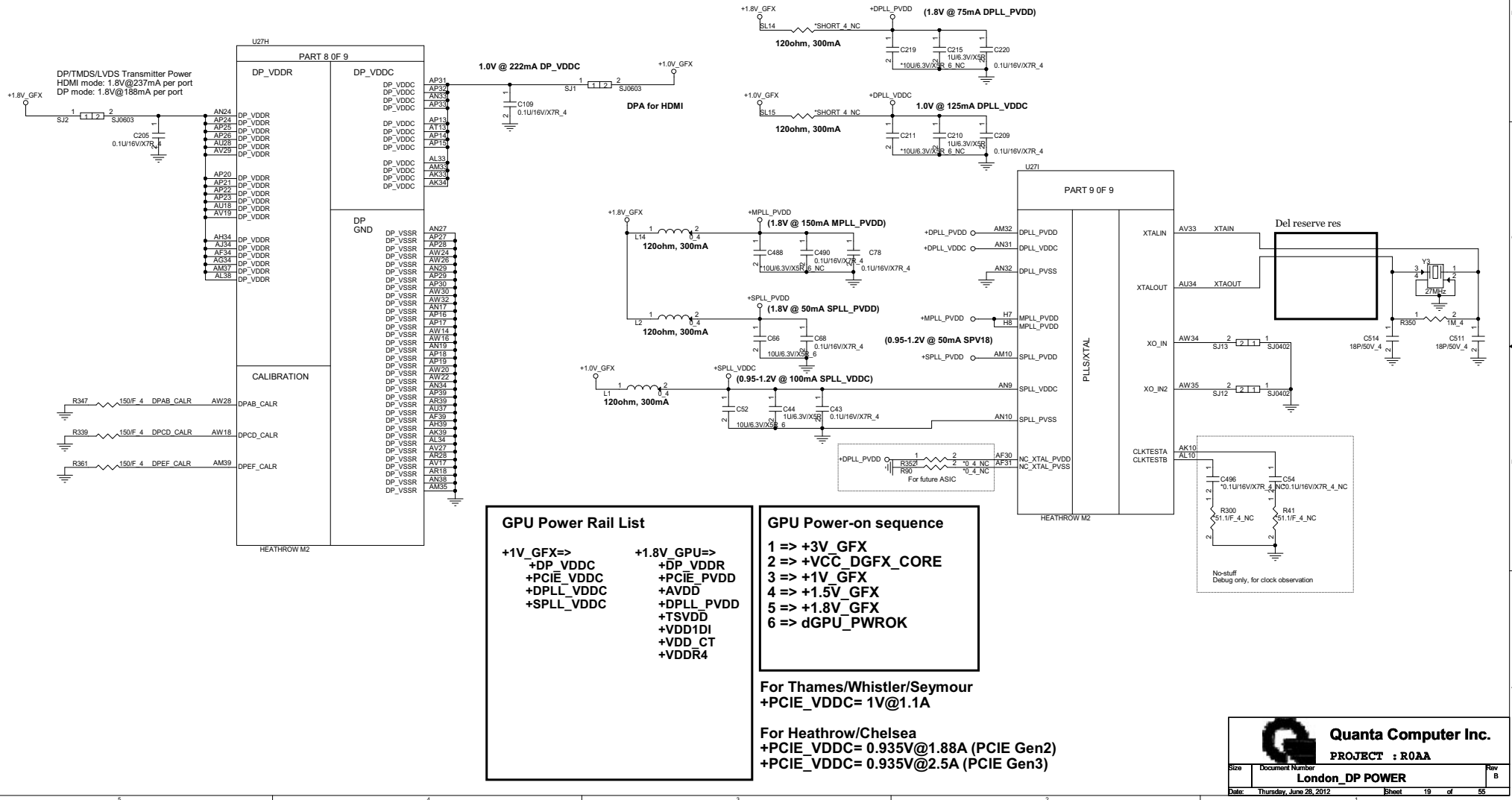


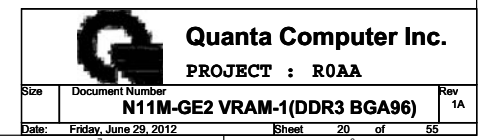
For Thames/Whistler/Seymour
NC_PCIE_VDD0 and NC_BIF_VDD0
should be tied with PCIE_PVDD
consumption about 440mA

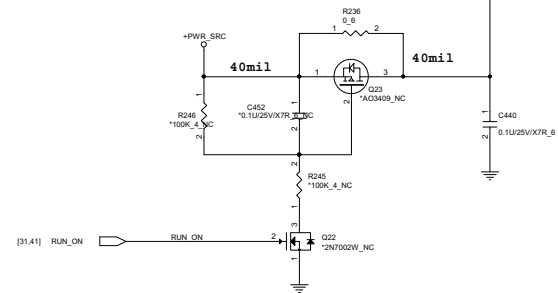
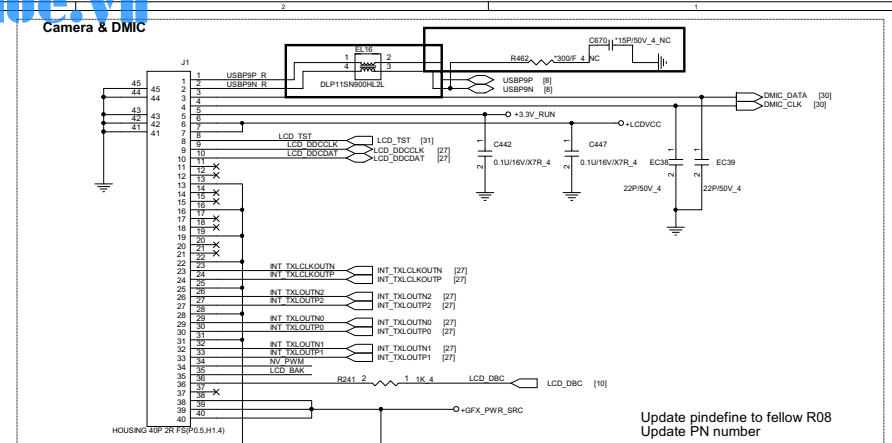



Del BACO circuit

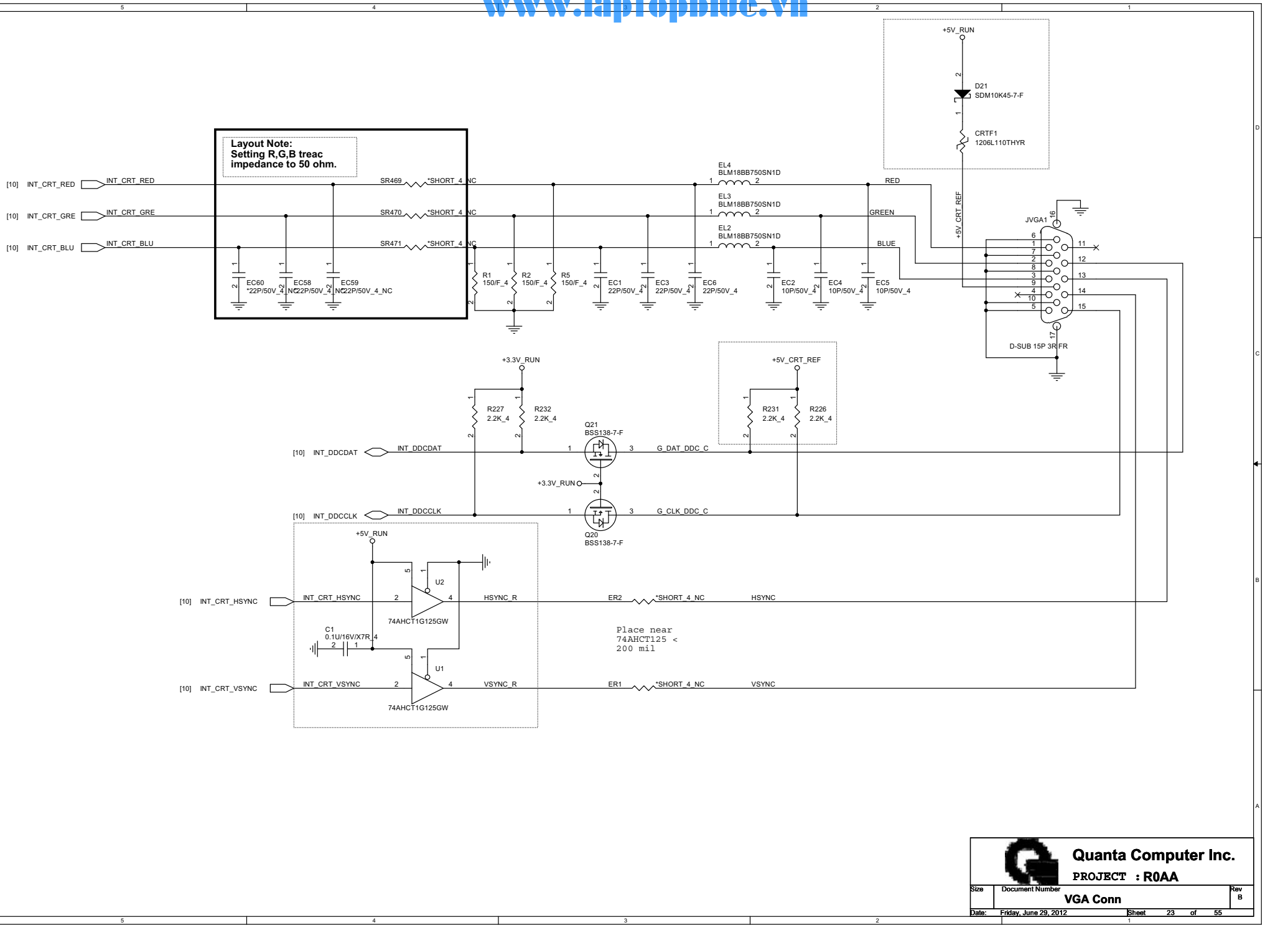




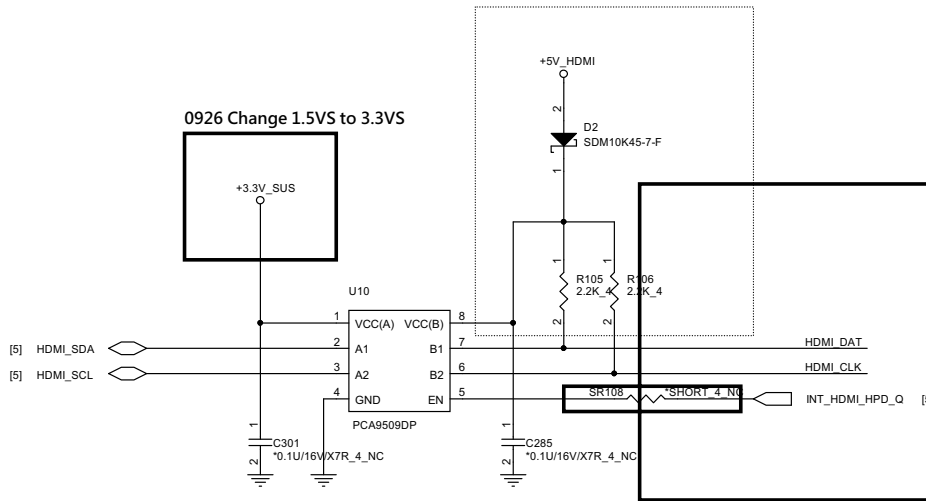




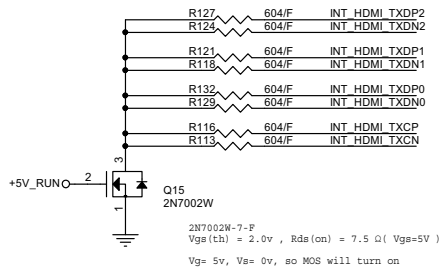
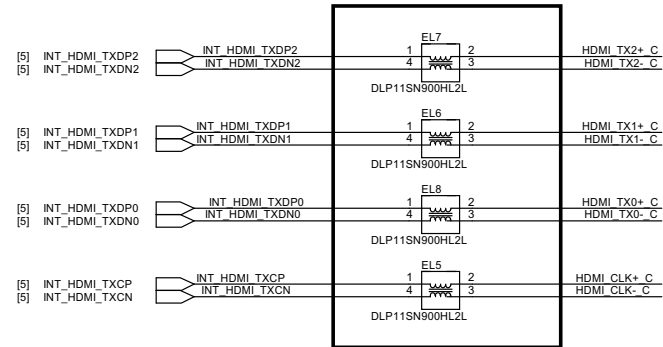
 Quanta Computer Inc. PROJECT : R0AA		Rev B
Size	Document Number	
LVDS Conn.		
Date:	Monday, July 02, 2012	Sheet 22 of 55



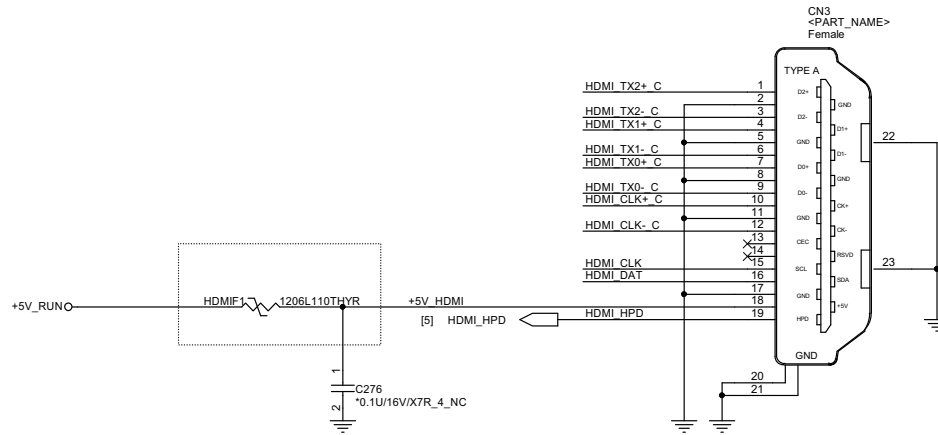
0926 Change 1.5VS to 3.3VS



Reserve for EMI and close to HDMI CONN



HDMI Conn.



Quanta Computer Inc.

PROJECT : R0AA

HDMI CONN

S	OE	Function
X	H	Disconnect
L	L	D=1D
H	L	D=2D

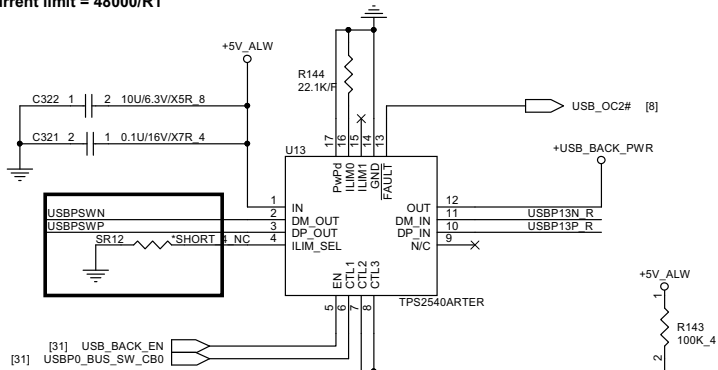
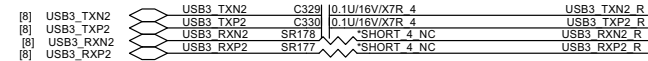
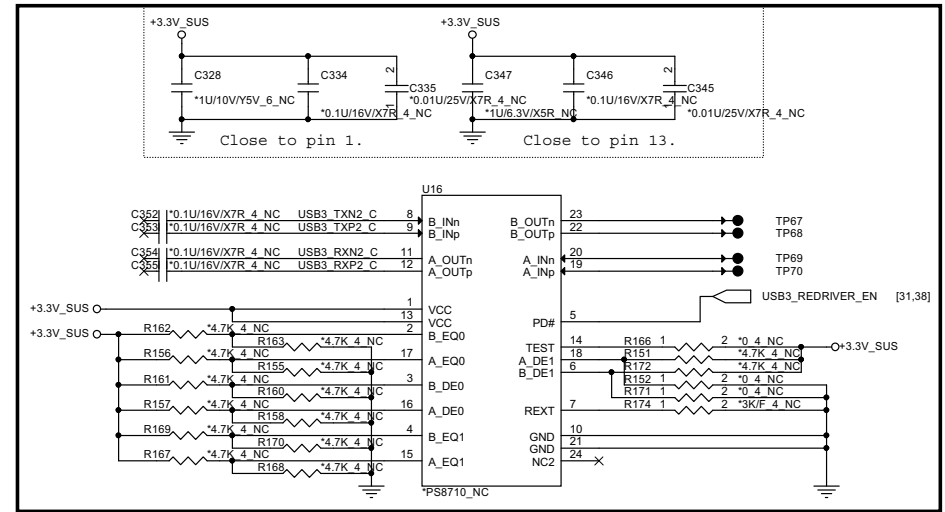
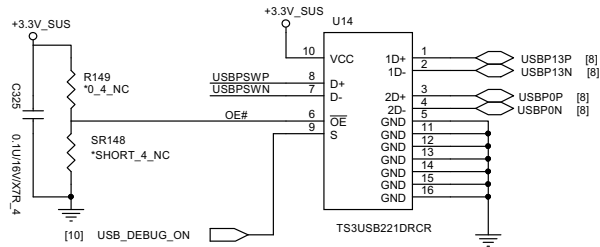
USB Power share

USB0_BUS_SW_CB0	Mode
Low	DCP, Auto-detect
High	CDP, BC Spec 1.1

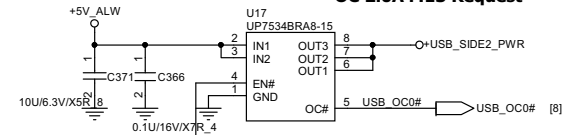
OC limitation	R1	mA
	100k ohm	480
	22.1k ohm	2171

Applied Now

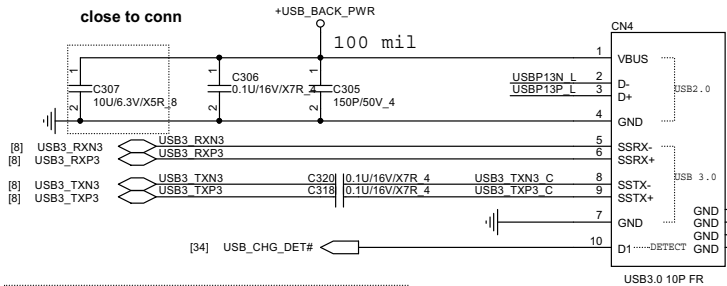
Current limit = 48000/R1



I continuous 1.5A OC 2.0A M13 Request

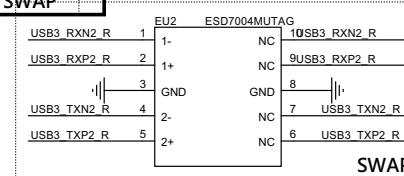
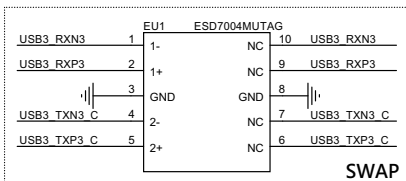
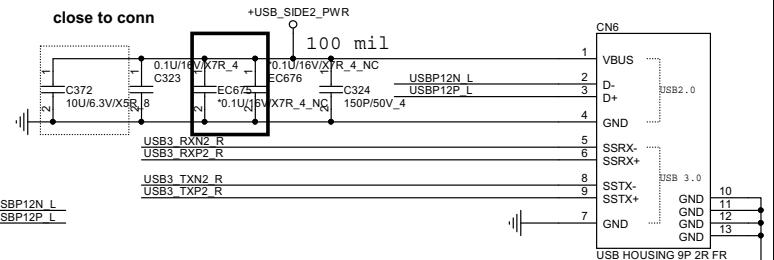
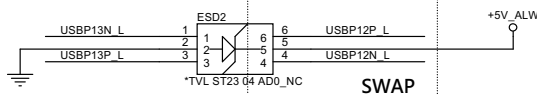


[29,31,38] USB_RIGHT_EN#



ESD Function

Place ESD diodes as close as USB connector.

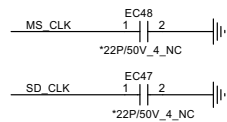
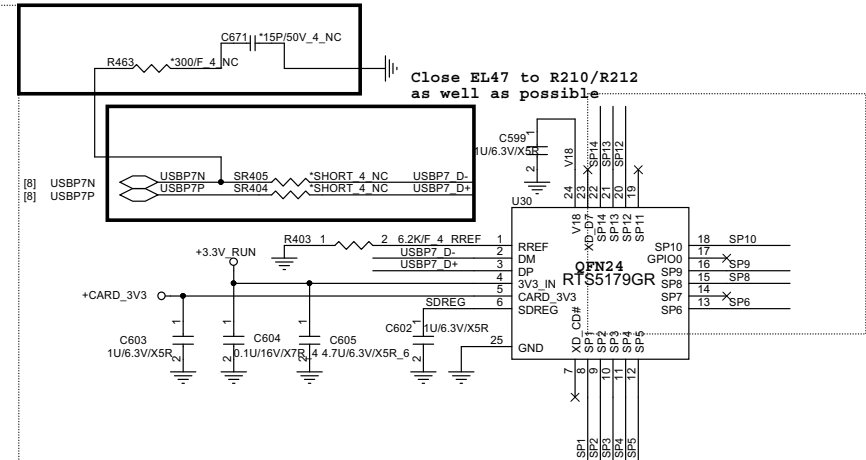
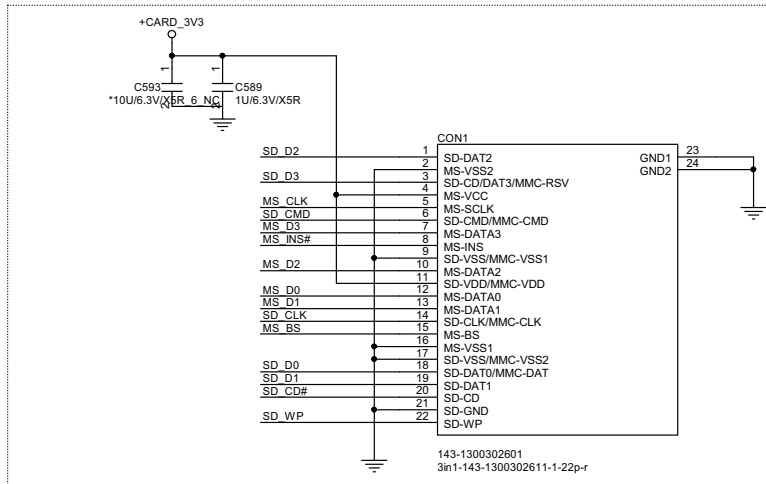


Quanta Computer Inc.
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Size Document Number
USB 3.0 port / USB power share
Date: Thursday, June 28, 2012 Sheet 25 of 55

Cardreader (RTS5179GR) Support SD3.0 USH50

Change CON1 footprint to 3in1-143-1300302611-1-22p-r (follow R09)



SP1	SD_WP	MS_CLK
SP2	SD_D1	MS_INS#
SP3	SD_D0	MS_D7
SP4	SD_D7	MS_D3
SP5	SD_CD#	
SP6		
SP8	SD_CLK	MS_D2
SP9	SD_D5	MS_D0
SP10	SD_CMD	
SP12	SD_D3	MS_D1
SP13	SD_D2	MS_D5
SP14		MS_BS

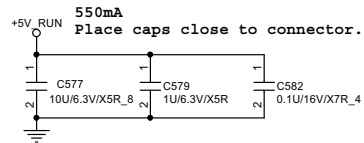
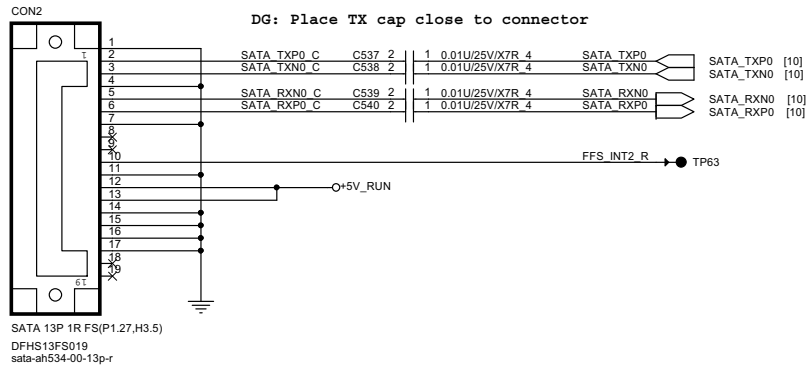
Share Pin

	SD CARD	MS CARD
SP1	SW WP	MS_CLK
SP2		MS_INS#
SP3	SD_D1	
SP4	SD_D0	MS_D7
SP5	SD_D7	MS_D3
SP6	SD_CD#	
SP7	SD_D6	MS_D6
SP8	SD_CLK	MS_D2
SP9	SD_D5	MS_D0
SP10	SD_CMD	
SP11	SD_D4	MS_D4
SP12	SD_D3	MS_D1
SP13	SD_D2	MS_D5
SP14		MS_BS

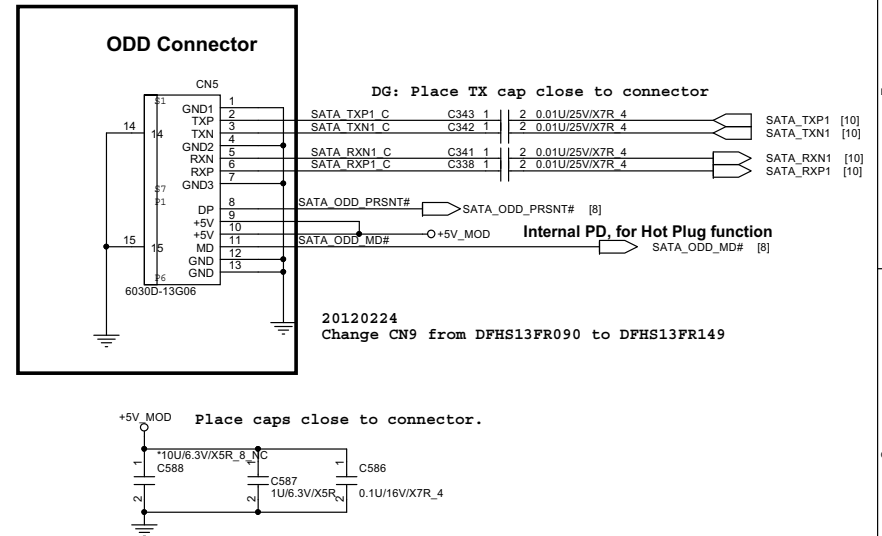


Quanta Computer Inc.
PROJECT : R0AA

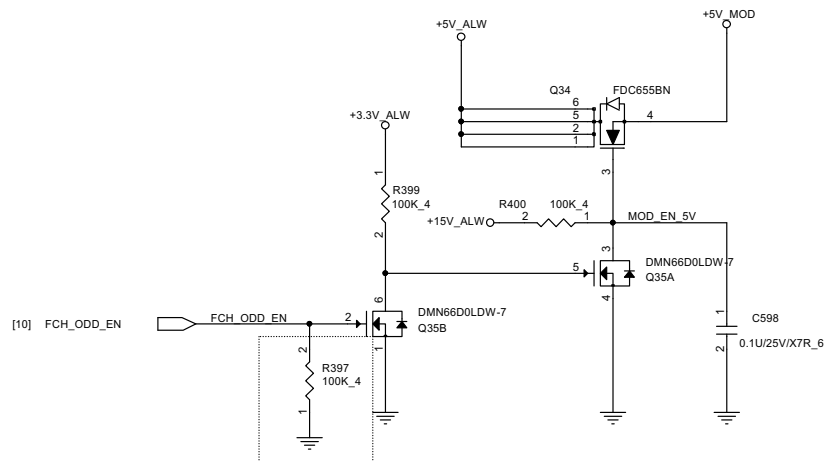
HDD



ODD

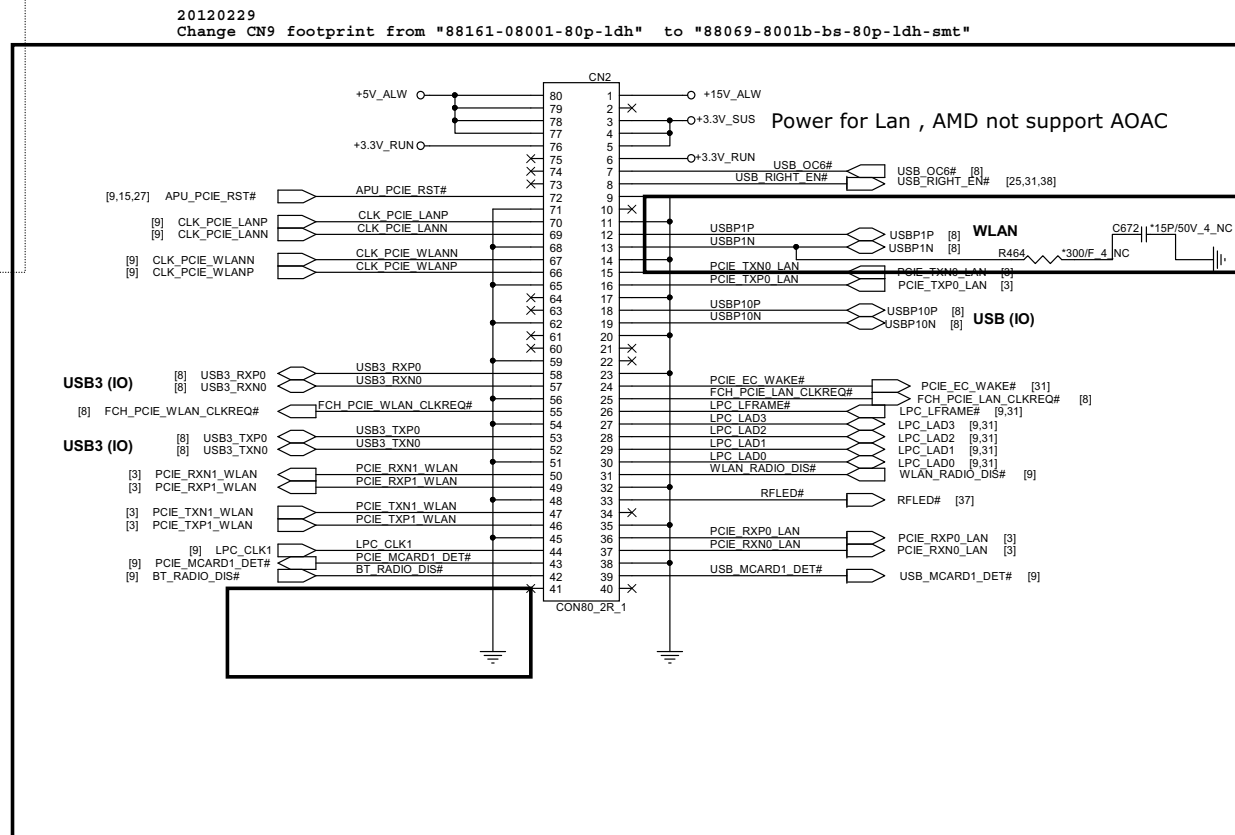


Support Zero power ODD

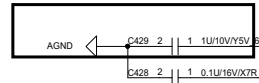


Quanta Computer Inc.
PROJECT : R0AA

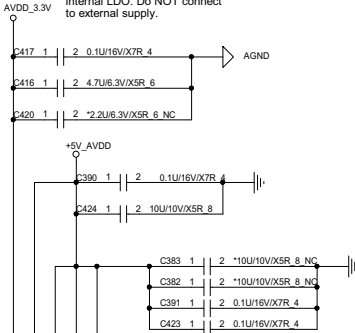
Size	Document Number	Rev
	SATA HDD/ODD	B
Date:	Monday, June 25, 2012	Sheet 28 of 55



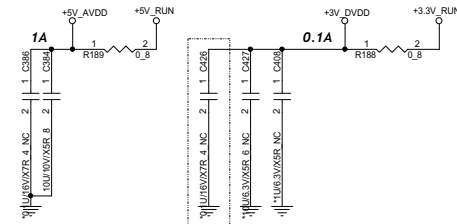
STUFF FOR AUDIO TEST



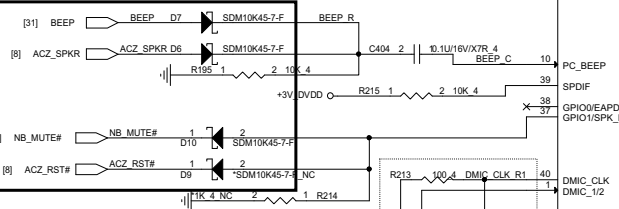
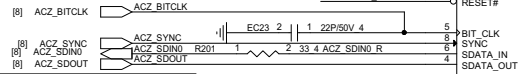
AVDD_3.3 pin is output of internal LDO. Do NOT connect to external supply.



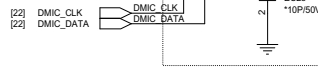
Layout Note: Path from +5V to LPWR_5.0 and RPWR_5.0 must be very low resistance (<0.01 ohms). Place bypass caps very close to device.



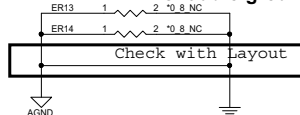
For EMI, close the audio I/O connector.



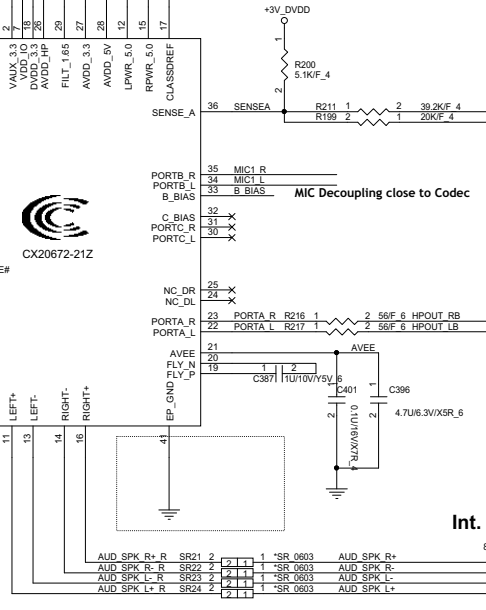
Change D6 D7 D9 D10 to BC010K45004



EMI Reserved Please see Design Guide for audio grounding.

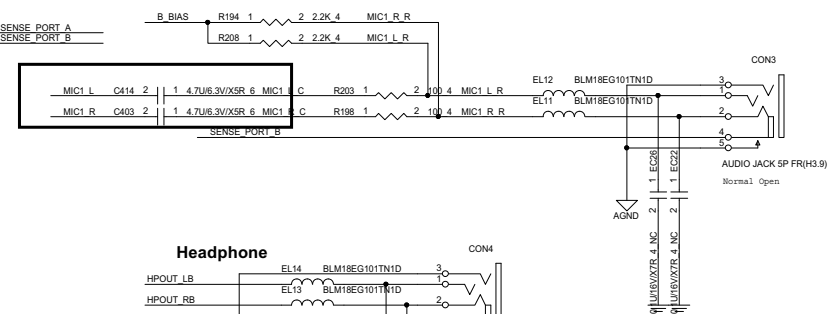


CX20672-21Z

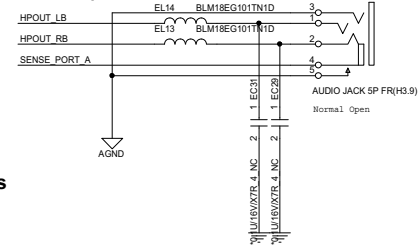


MIC Decoupling close to Codec

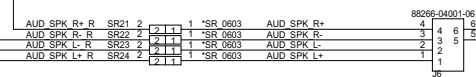
External Stereo microphone

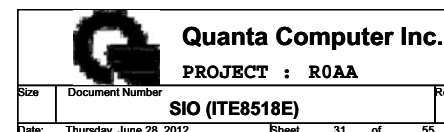


Headphone

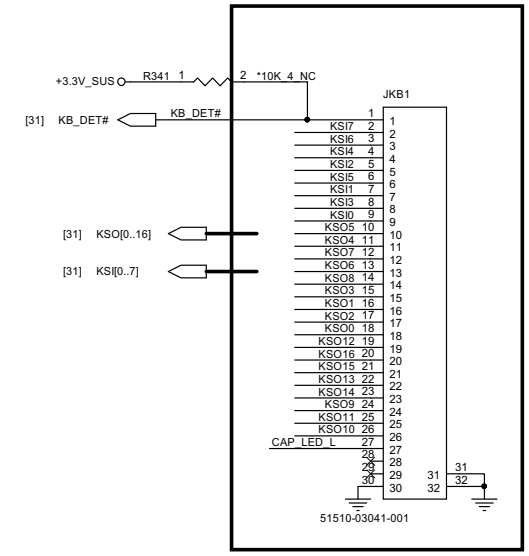
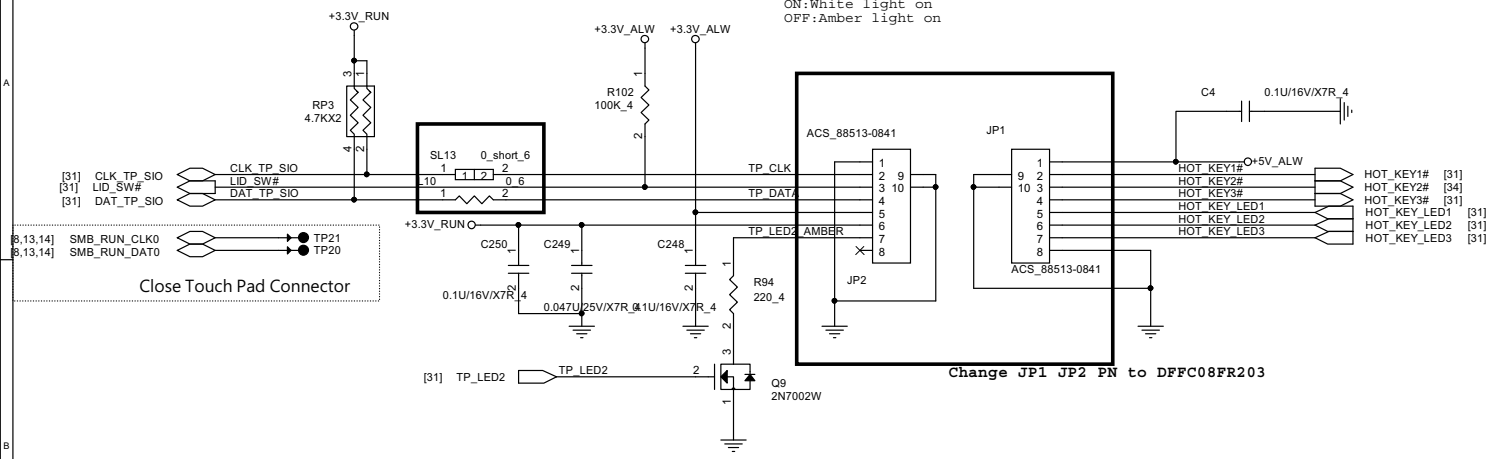


Int. Stereo Speakers

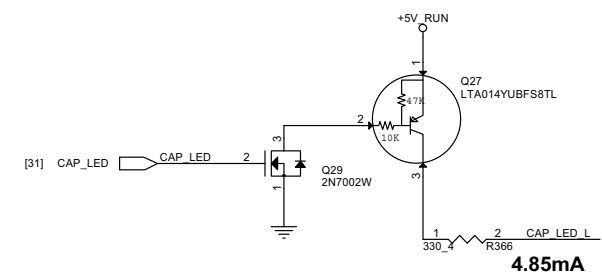




KEYBOARD CONNECTOR



$V_{i(on_max)} = -1.4V$
 $V_{i(off_min)} = -0.3$



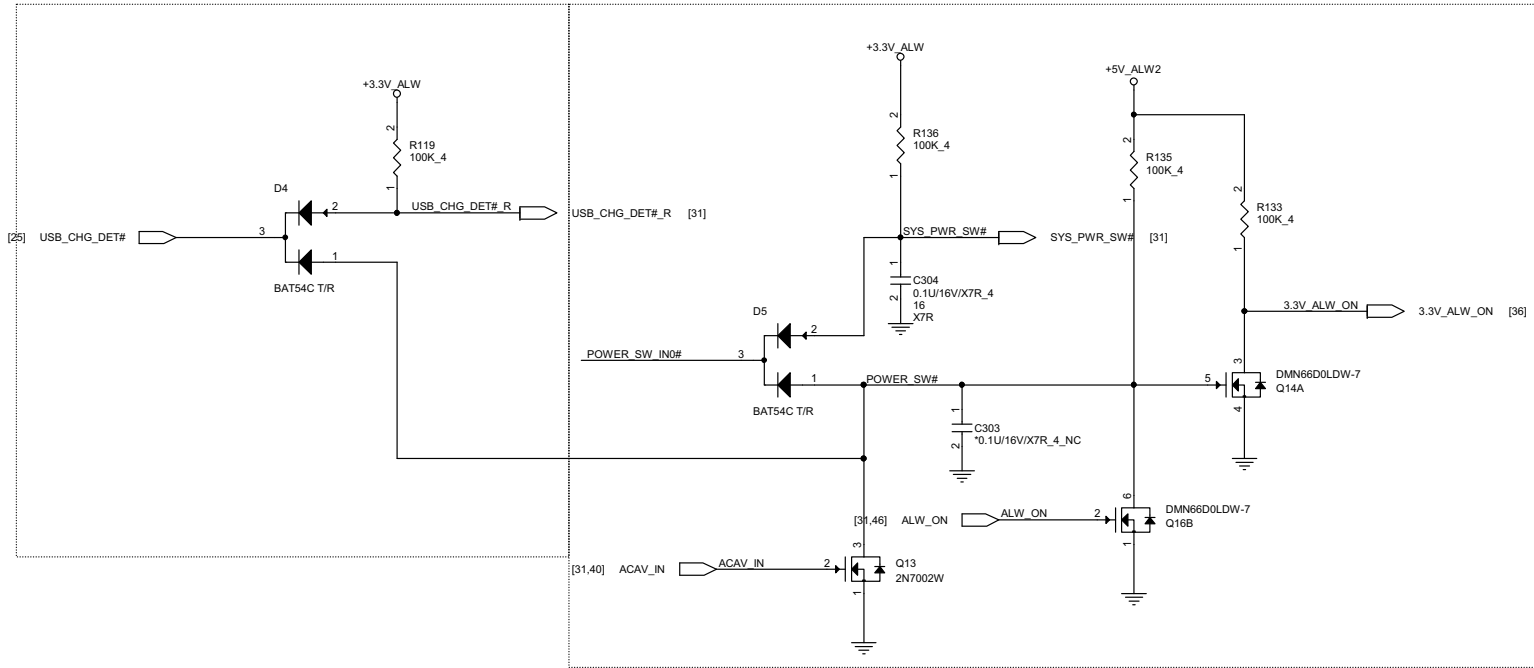
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PROJECT : R07

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	TP / KB	1A

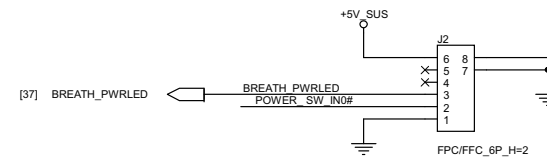
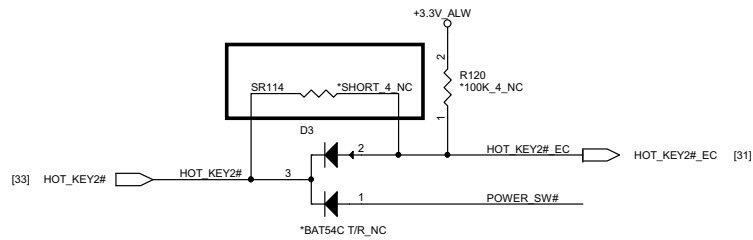
Date: Thursday, June 28, 2012 Sheet 33 of 55

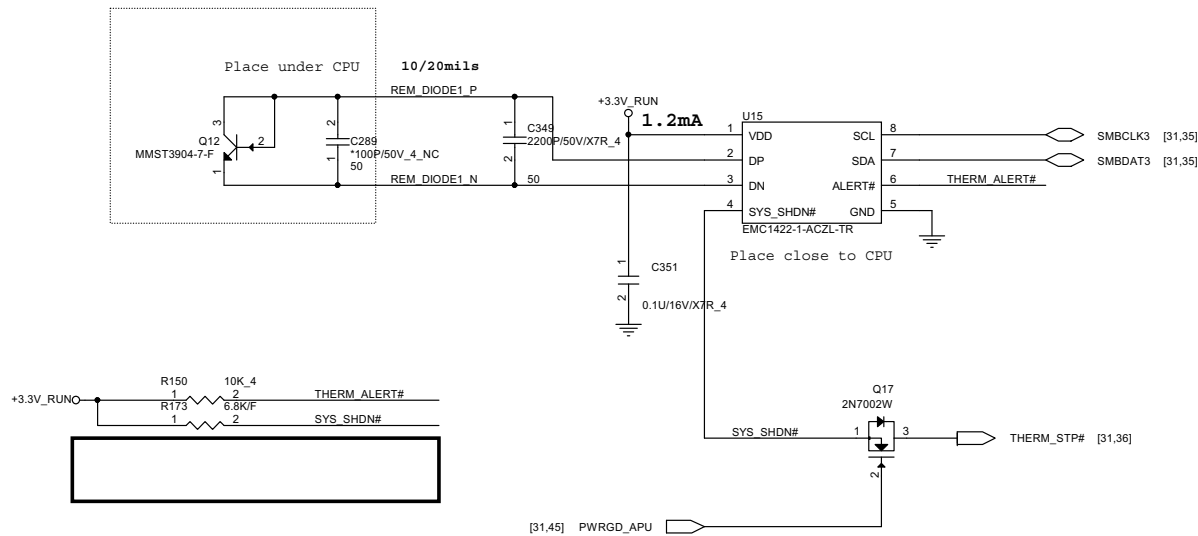
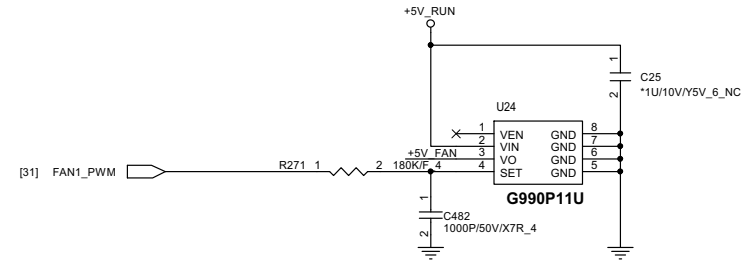
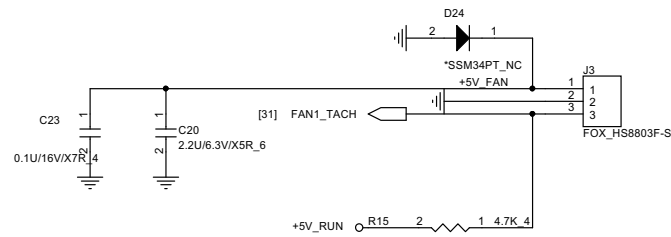
For USB charger usage

3V ALW ON POWER LOGIC

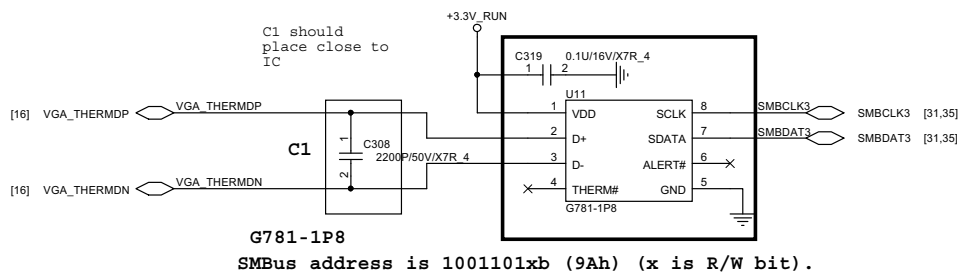


TO PWR button board





SYS_SHD#	4.7K	6.8K	10K	15K	22K	33K
ALERT#	77'C	83'C	89'C	95'C	101'C	107'C
4.7K	77'C	83'C	89'C	95'C	101'C	107'C
6.8K	78'C	84'C	90'C	96'C	102'C	108'C
10K	79'C	85'C	91'C	97'C	103'C	109'C
15K	80'C	86'C	92'C	98'C	104'C	110'C
22K	81'C	87'C	93'C	99'C	105'C	111'C
33K	82'C	88'C	94'C	100'C	106'C	112'C



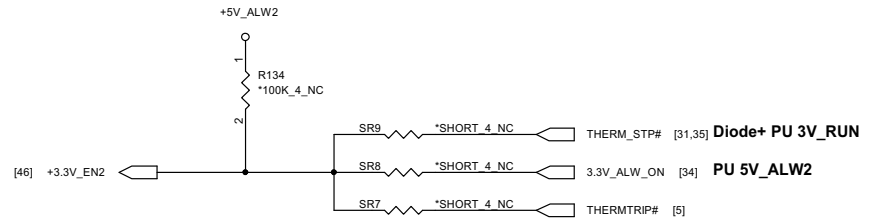
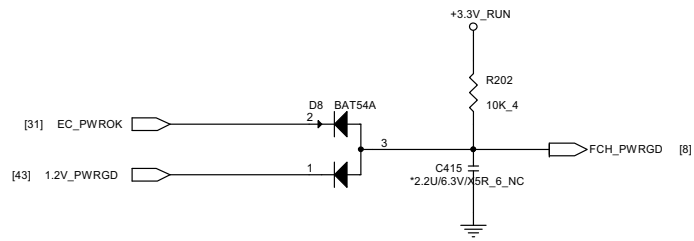
G781-1P8

SMBus address is 1001101xb (9Ah) (x is R/W bit).



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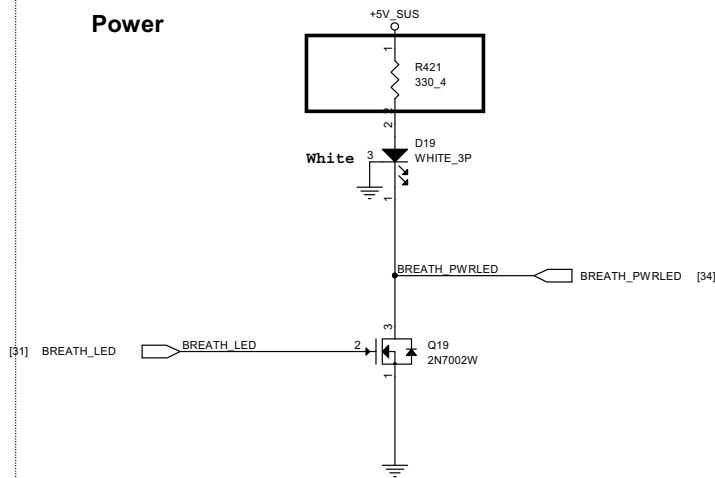


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PROJECT : R07

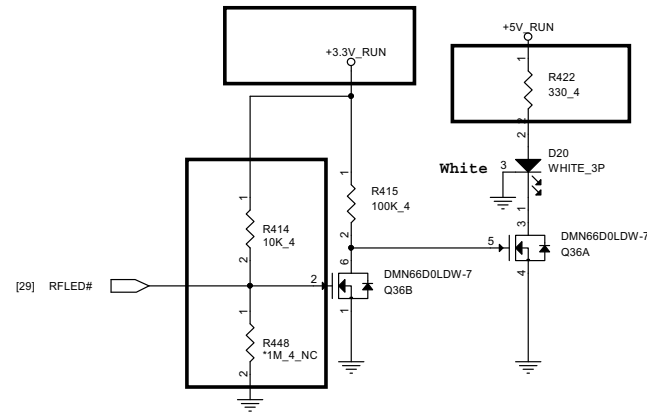
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Date: Monday, June 25, 2012	Sheet 36 of 55	

System Reset Circuit

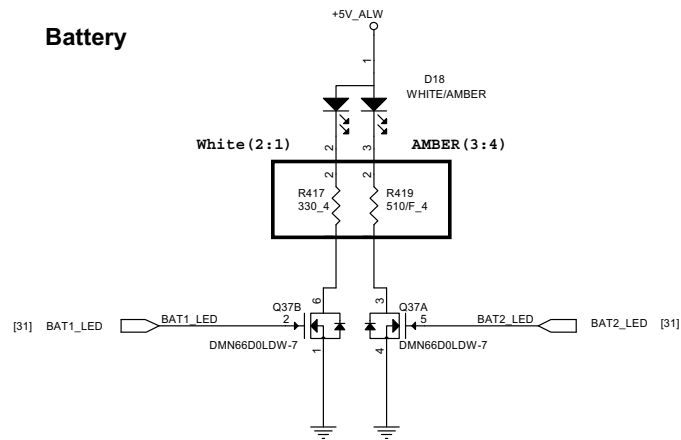
Power



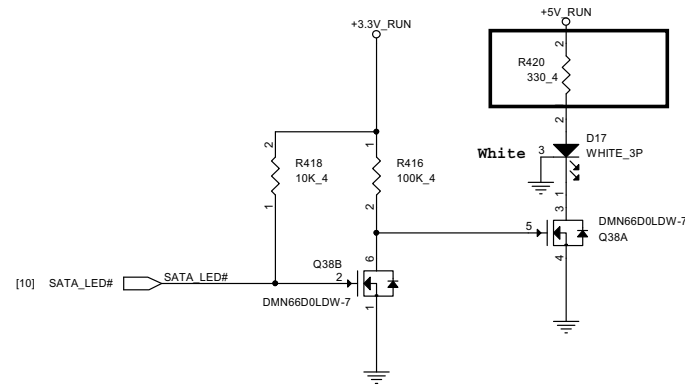
Bluetooth / WLAN on/off LED



Battery

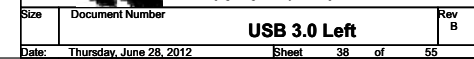
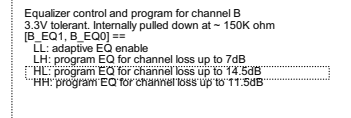
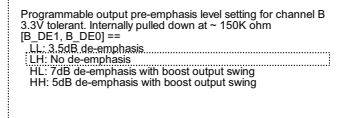
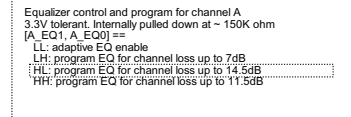
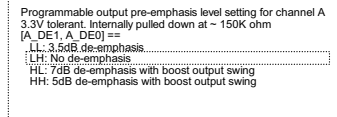
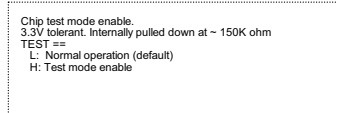
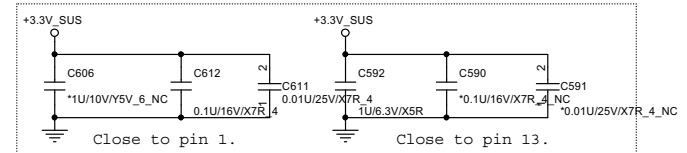
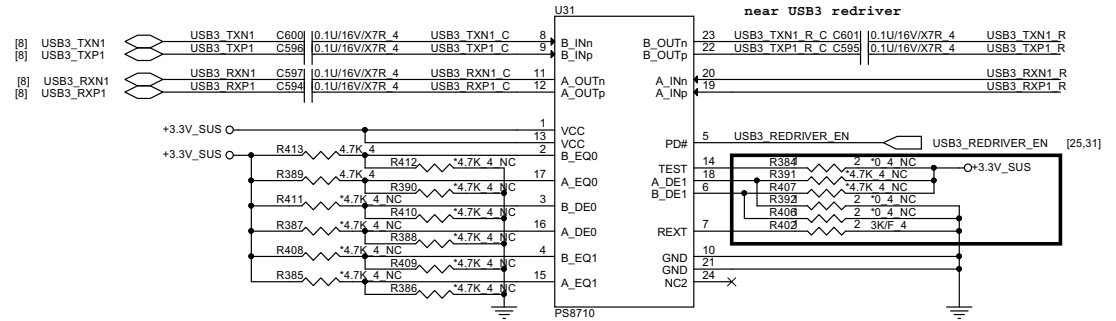


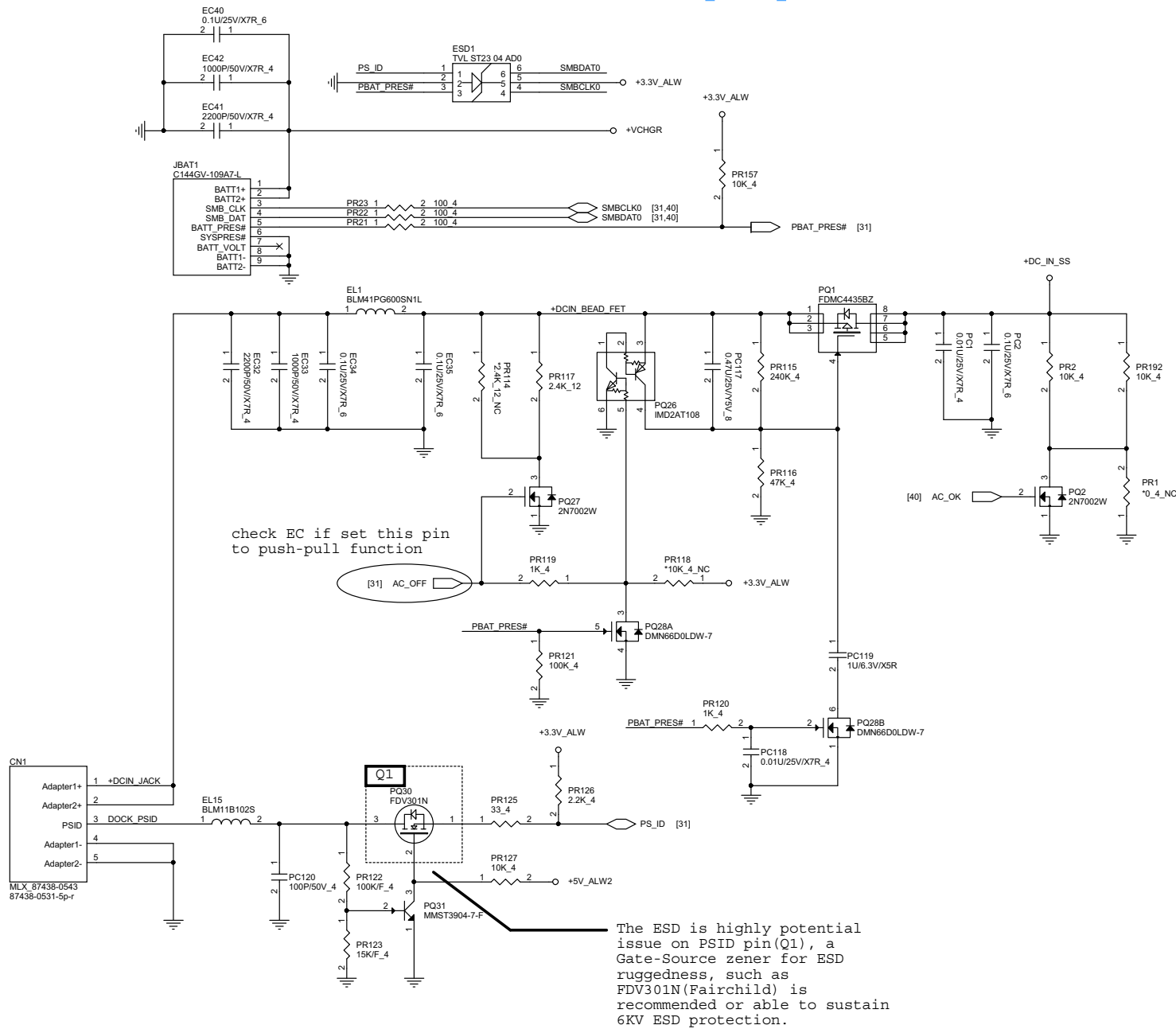
HDD activity LED.

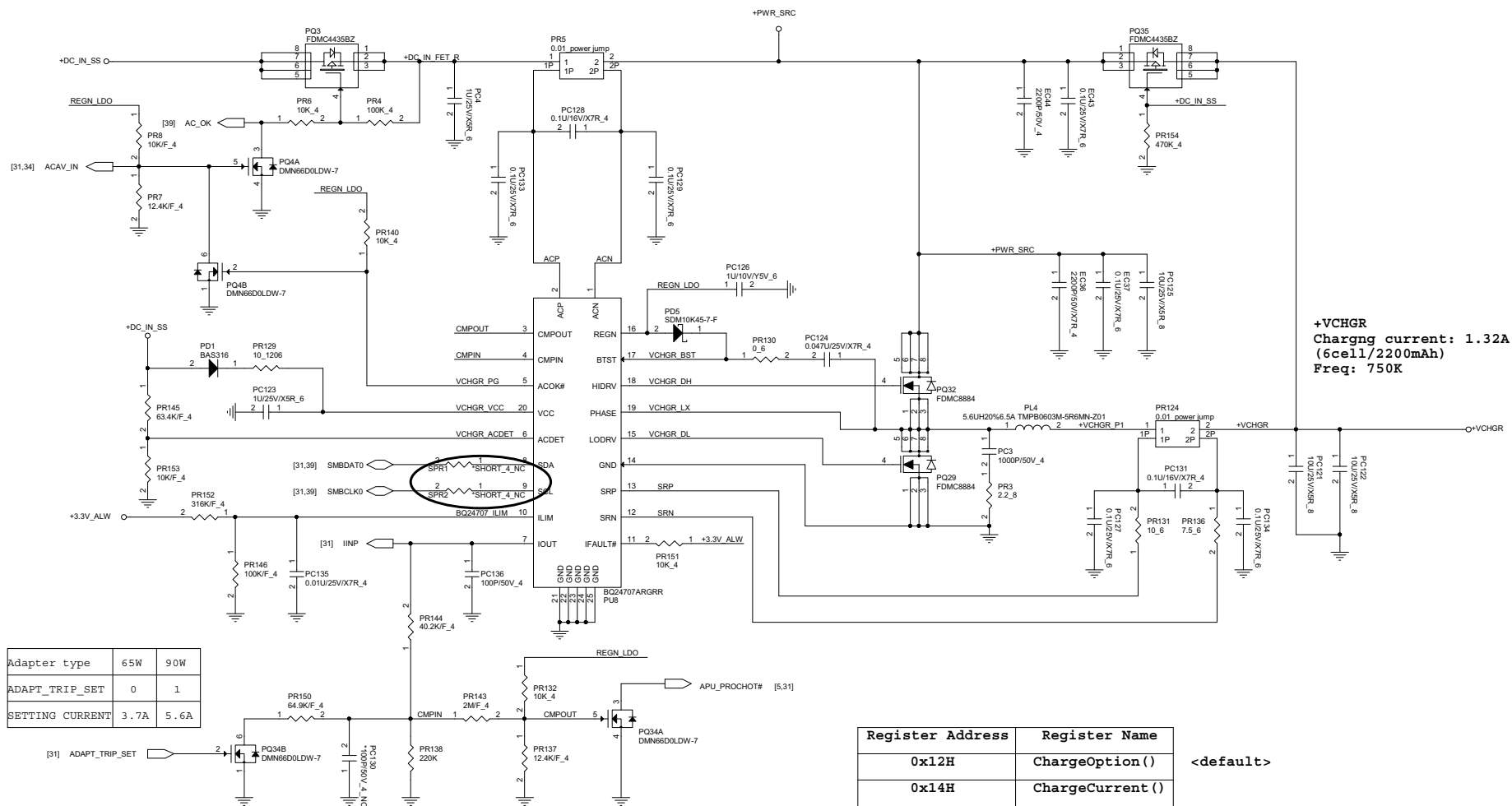


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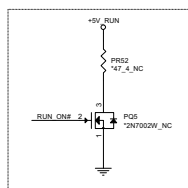
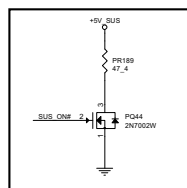
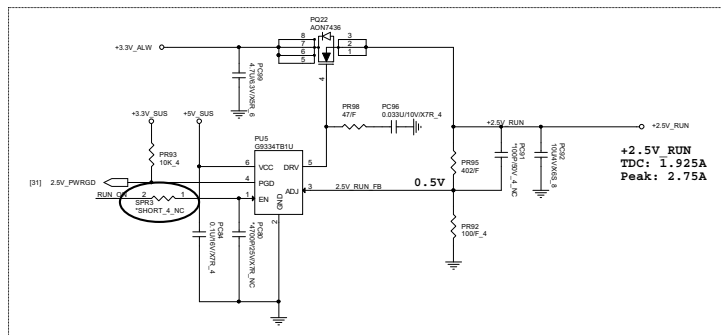
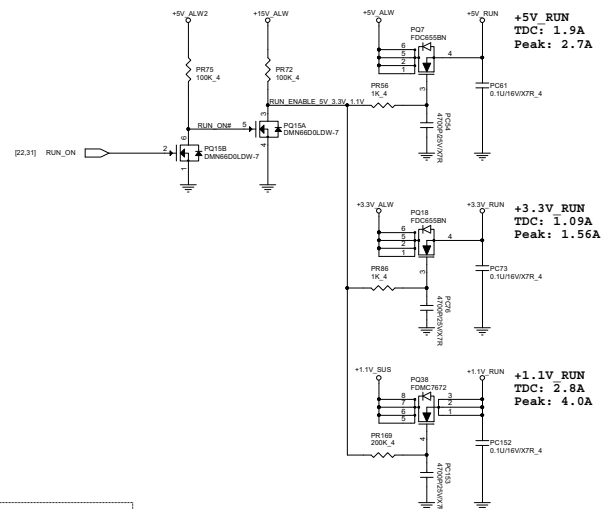
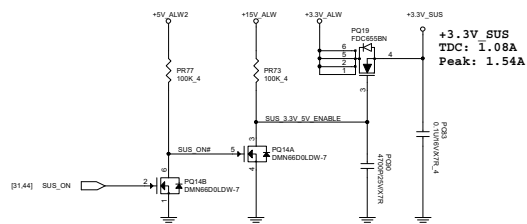


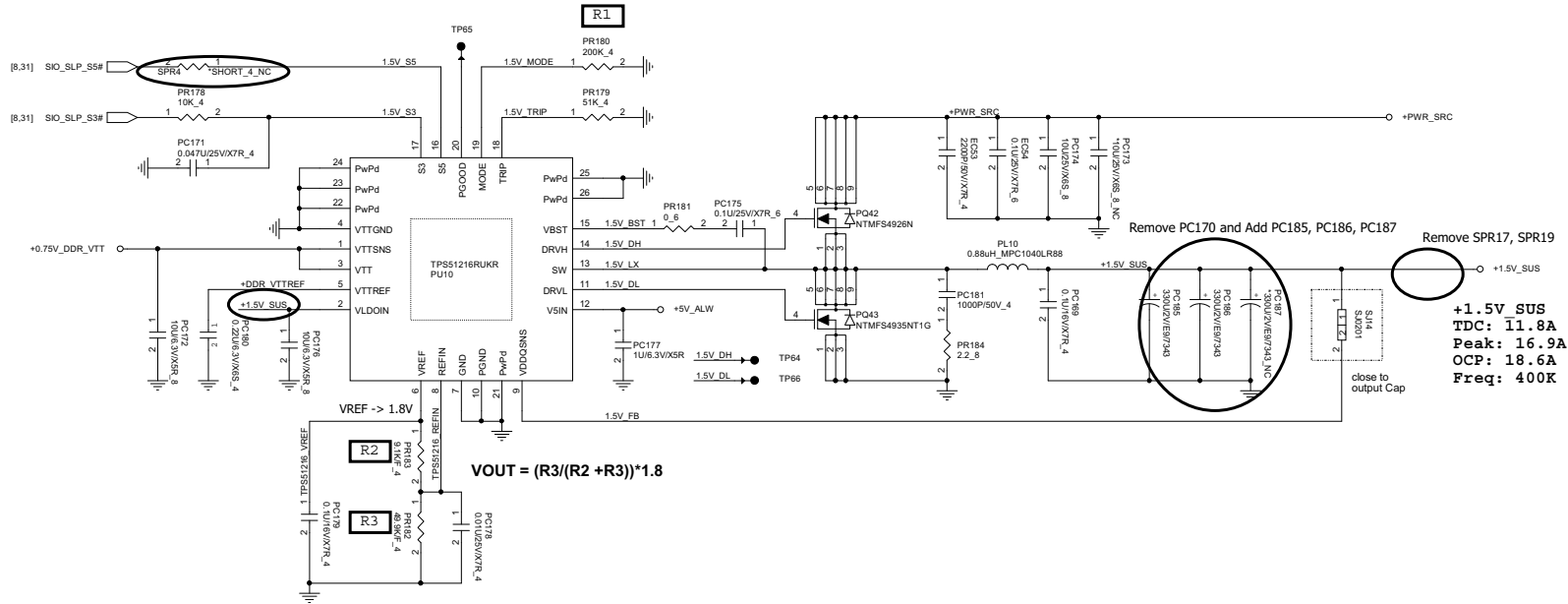




Register Address	Register Name
0x12H	ChargeOption()
0x14H	ChargeCurrent()
0x15H	ChargeVoltage()
0x3FH	InputCurrent()
0xFEH	ManufacturerID()
0xFFH	DeviceID()

<default>





Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	Off (discharge)	Off (discharge)	Off (discharge)

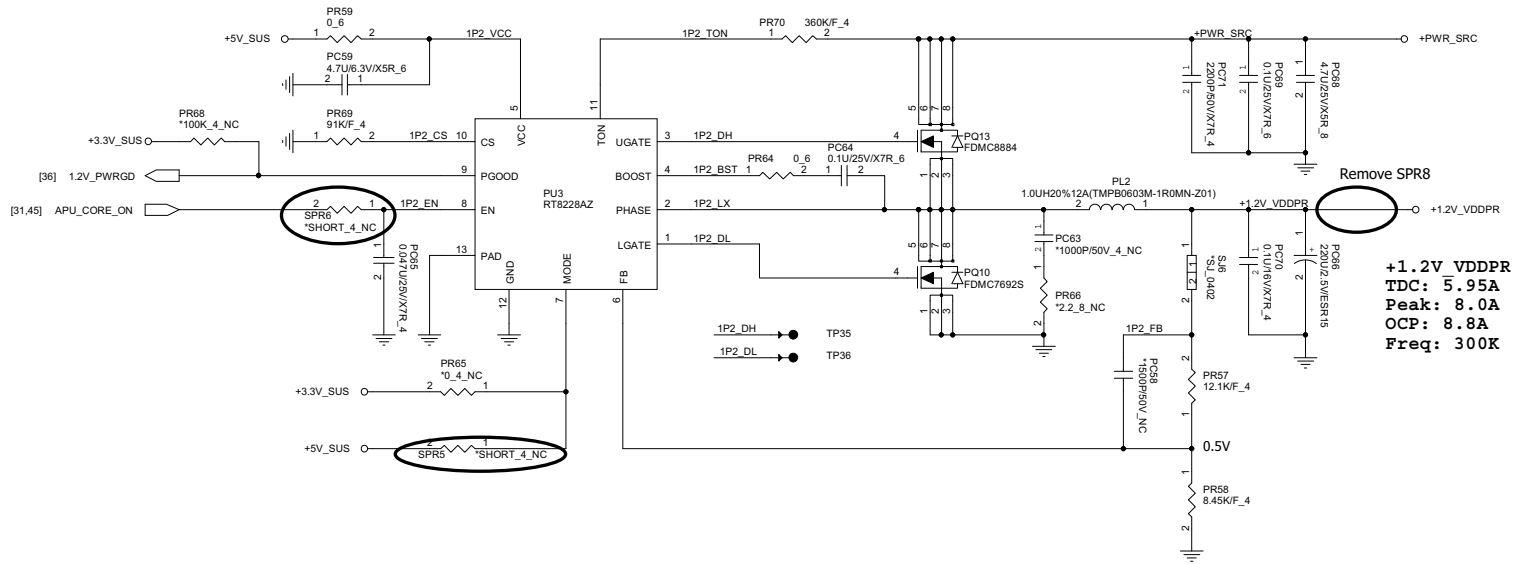
MODE Selection			
	Resistance between MODE and GND	Frequency	Discharge Mode
R1	200K_4	CS42002JB14	400K Hz
R1	100K_4	CS41002JB20	300K Hz
R1	68K_4	CS36802JB12	300K Hz
R1	47K_4	CS34702JB21	400K Hz

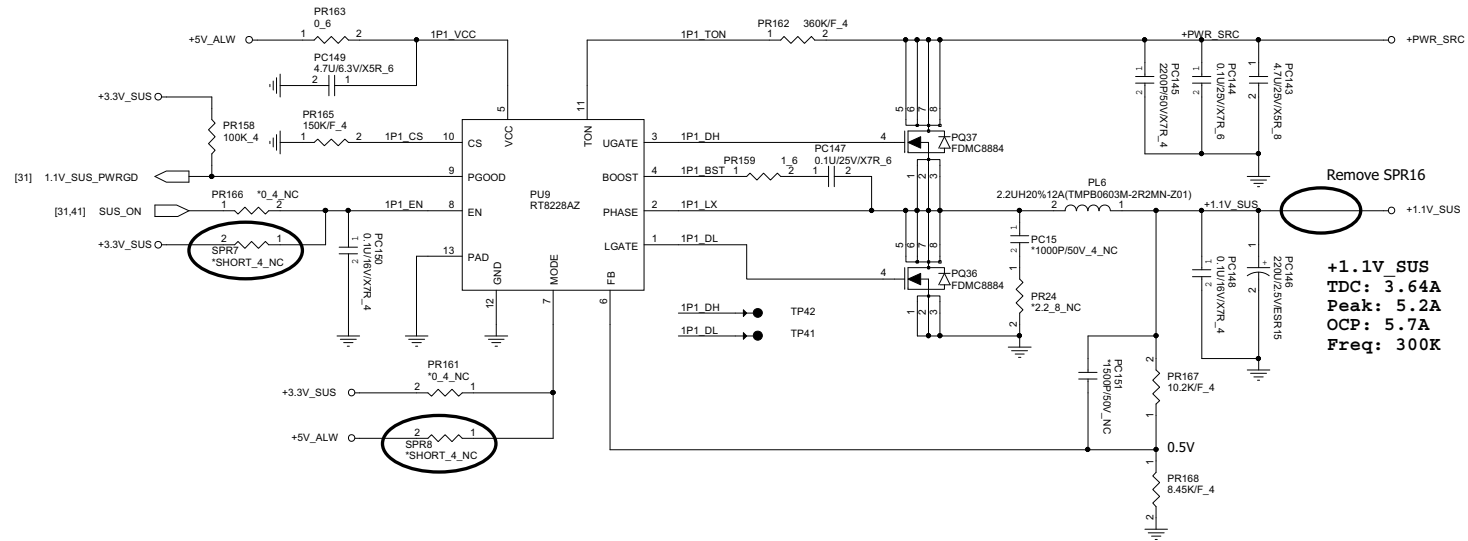


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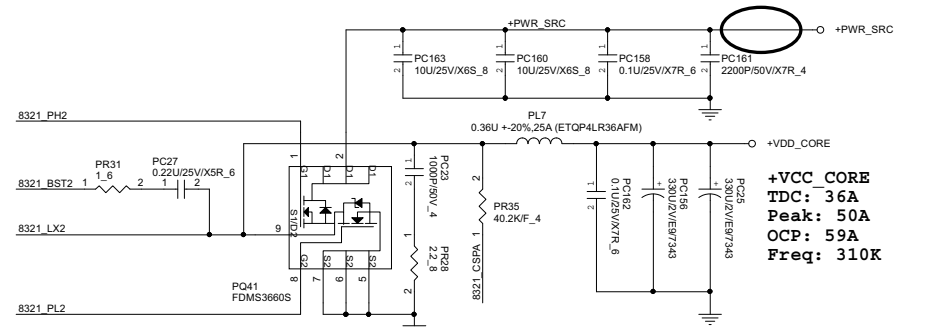
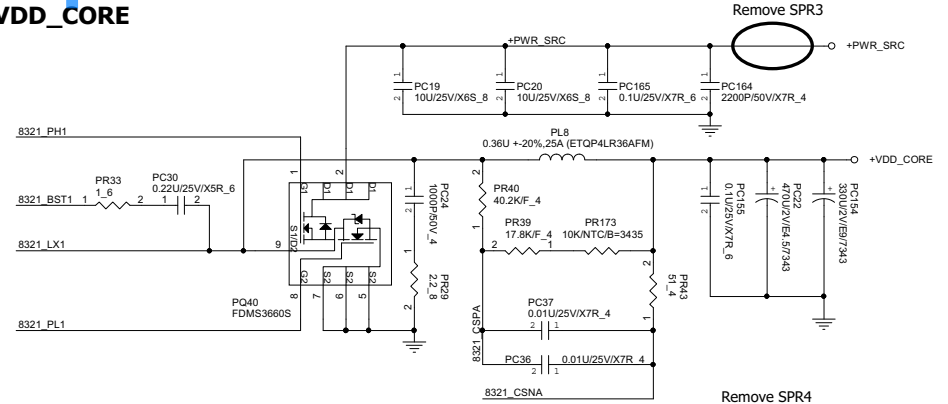
PROJECT : R0AA

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	+1.5V_DDR/0.75V(TPS51216)	B
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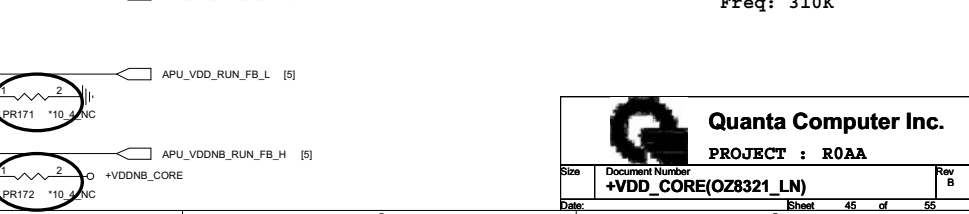
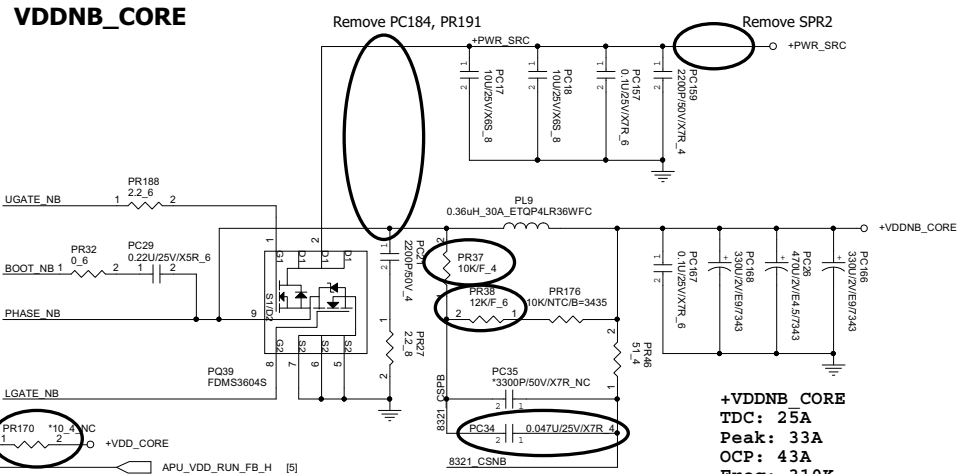




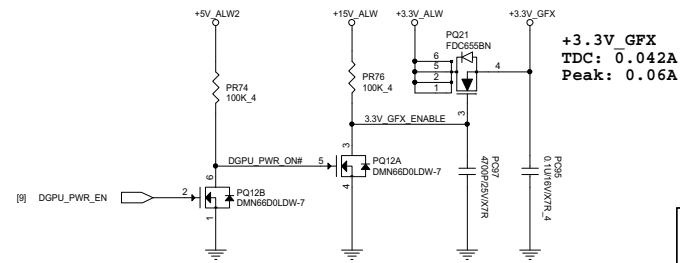
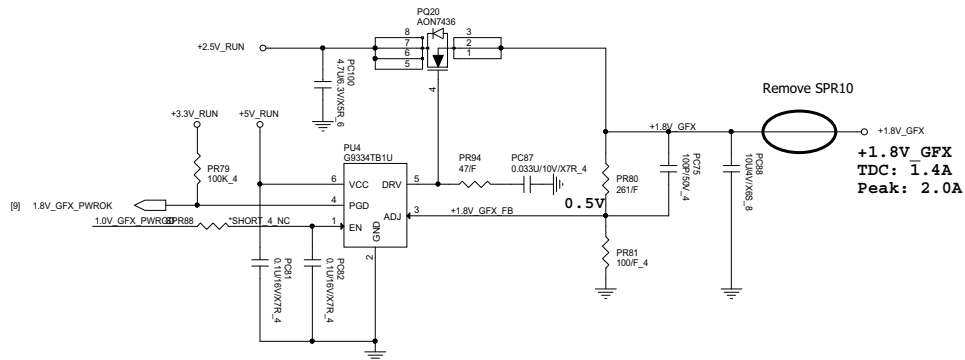
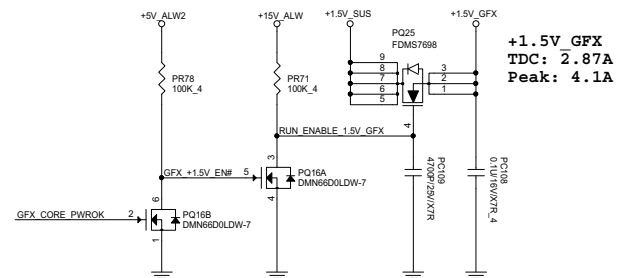
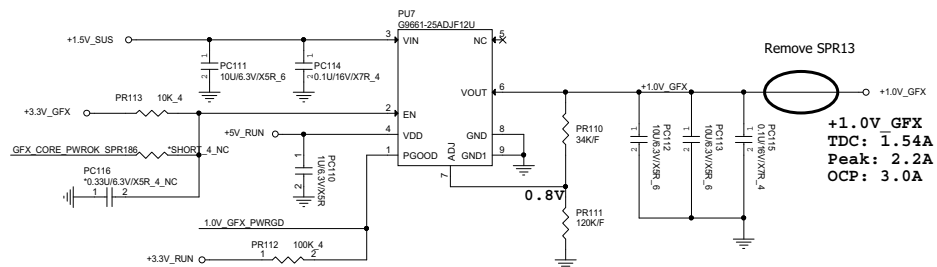
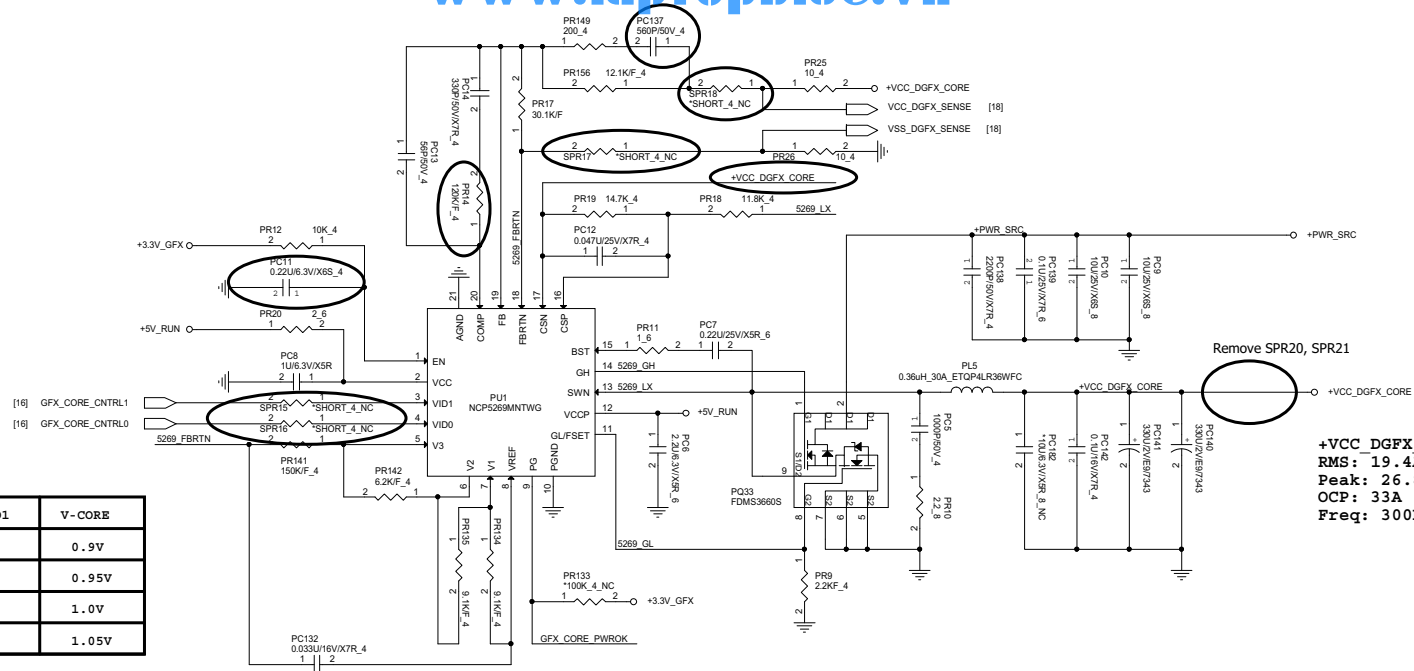
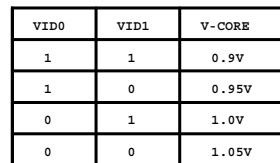
VDD_CORE

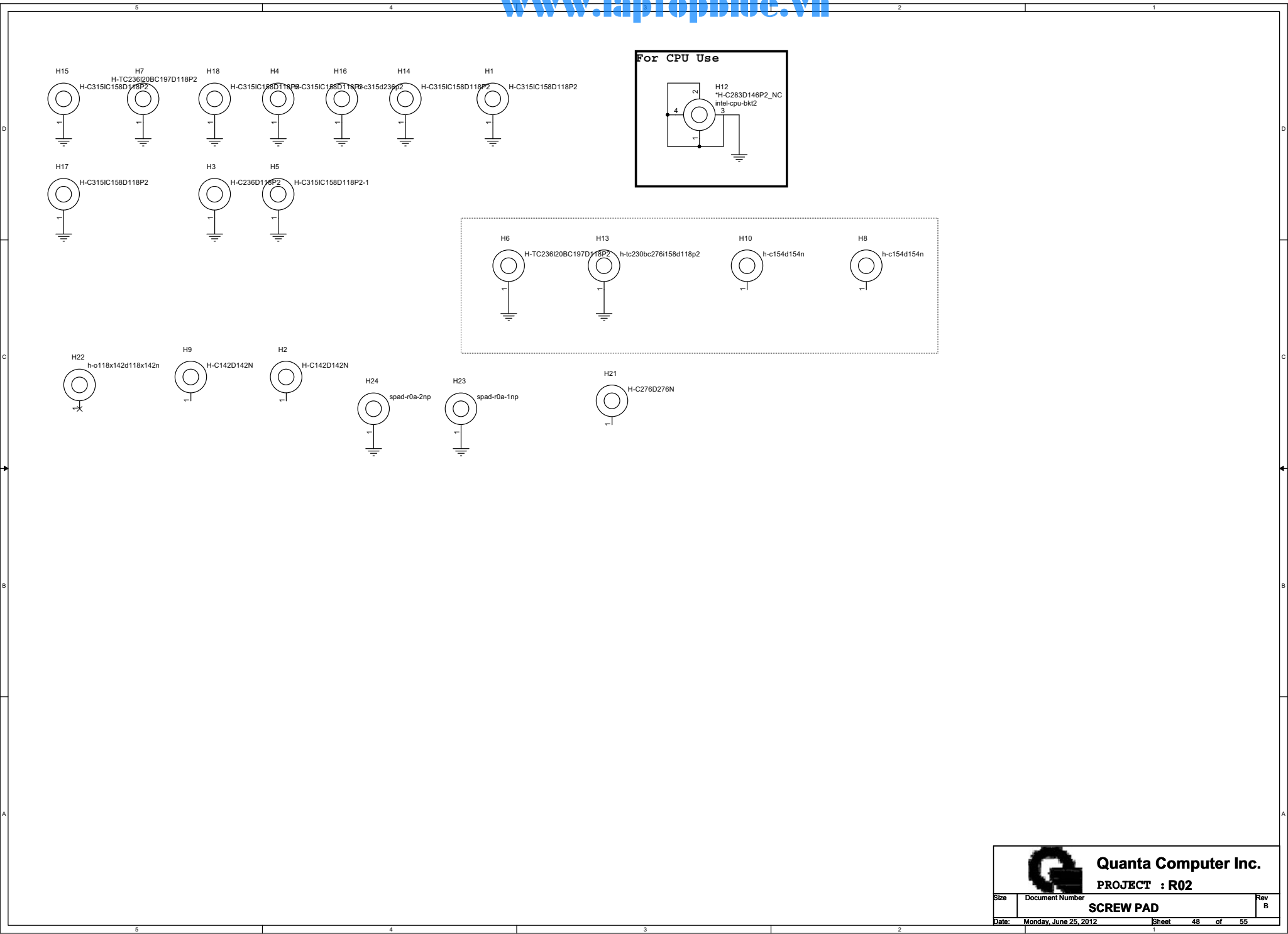


VDDNB_CORE



Register Name	Default Value		Address (HEX)	Notes
	Value	Hex	i2C R/W	
Initial_offset	RailA	0V	00H	Default
	RailB	0V	00H	Default
IDDSpike	RailA	64A	0FH	Default
	RailB	32A	0FH	Default
Slew rate	RailA	10mV/us	03H	Default
	RailB	10mV/us	03H	Default
Special offset	RailA	0V	00H	Default
	RailB	0V	00H	Default
Temp_max	RailA	100C	01H	Default
	RailB	100C	01H	Default
Freq	RailA	3.06usV	12H	Setting by EC
	RailB	3.06usV	12H	Setting by EC





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