

MODEL NAME : *Viking 18*

PCB NO : *LA-9332P*

BOM P/N : *4619KU31L01*

Compal Confidential

Viking 18

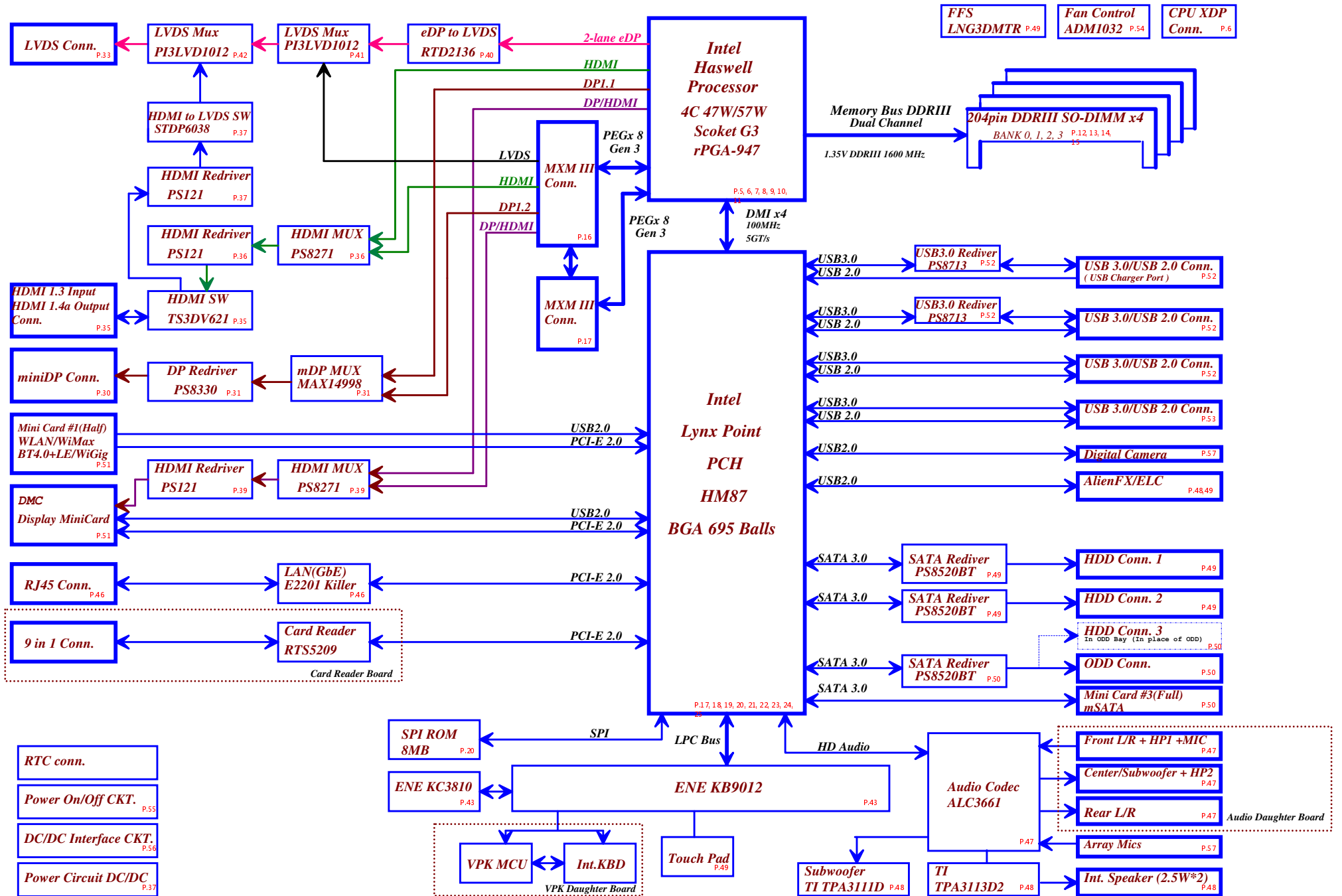
Schematic Document

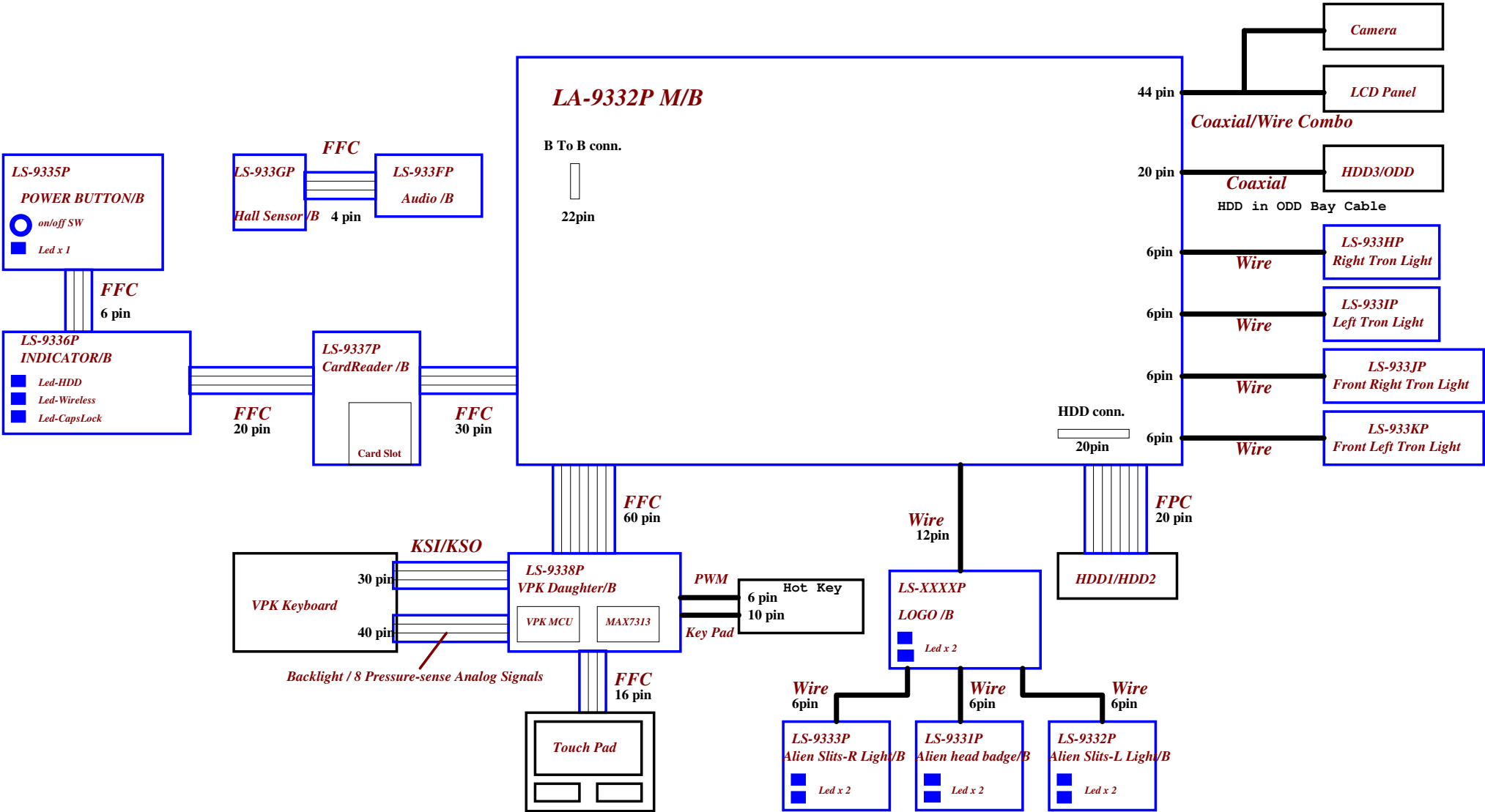
Rev: X02

2012-11-19

@ : Nopop Component

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2012/05/14	Deciphered Date	2013/05/13	Title	Cover Sheet
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Board ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

Board ID	PCB Revision
0	0.1 (SSI)
1	0.2 (PT)
2	0.3 (ST)
3	0.4 (QT)
4	1.0 (MP)
5	
6	
7	

USB 3.0 PORT	Connction
1	JUSB1 (Right side)
2	JUSB2 (Right side)
3	NA
4	NA
5	JUSB3 (Left side)
6	JUSB4 (Left side)

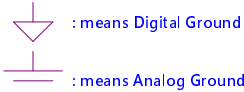
POWER STATES

State	Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0		HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M-OFF		LOW	HIGH		HIGH	LOW	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF		LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF		LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

PM TABLE

State	power plane	+5VALW +3VALW +3VLP +3V_PCH	+1.35V +1.05V	+5VS +3VS +1.5VS +1.05VS +0.675VS +3VMXM +5VMXM +VCC_CORE +1.35V_CPU_VDDQ
S0		ON	ON	ON
S3		ON	ON	OFF
S5 S4/AC		ON	OFF	OFF
S5 S4/AC don't exist		OFF	OFF	OFF

Symbol Note :



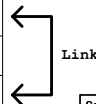
CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	MINI CARD-1 WLAN	CLKOUTFLEX0	None
	CLKOUT_PCIE1	MINI CARD-2 DMC	CLKOUTFLEX1	None
	CLKOUT_PCIE2	10/100/1G LAN	CLKOUTFLEX2	None
	CLKOUT_PCIE3	CARD READER	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_A	MXM		

SATAIII	DESTINATION
SATA0	HDD1
SATA1	HDD2
SATA2	ODD
SATA3	mSATA
SATA4/PCIE LANE1	MINI CARD-1 WLAN
SATA5/PCIE LANE2	MINI CARD-2 DMC

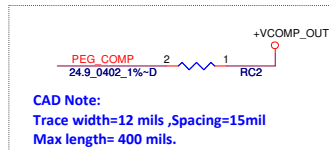
PCI EXPRESS	DESTINATION
Lane 1/USB3.0 Port 3	None
Lane 2/USB3.0 Port 4	None
Lane 3	10/100/1G LAN
Lane 4	CARD READER
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

SMBUS Control Table

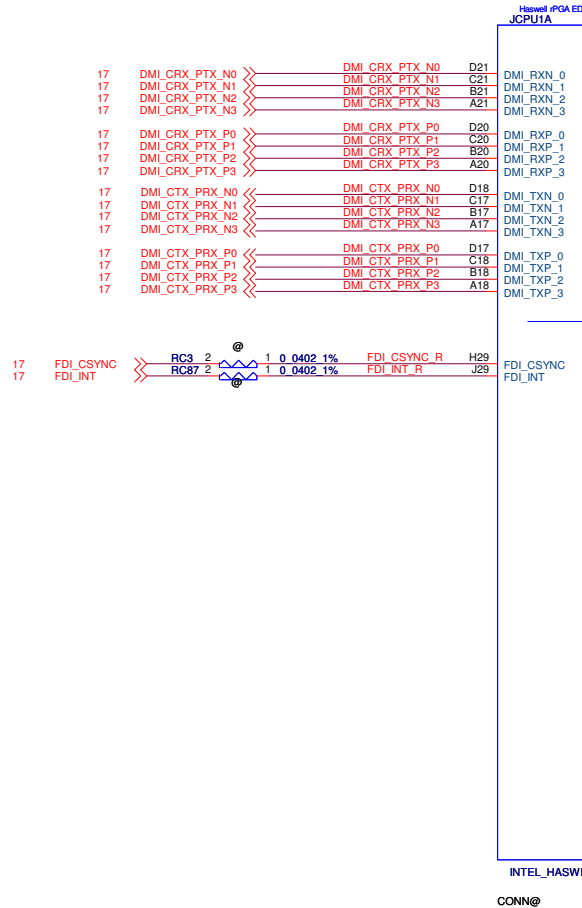
	SOURCE	WLAN	DMC	BATT	DIMM	6038	4028	Thermal Sensor	FFS	2136	VPK MCU	MXM	XDP	Charger	TP	mSATA
EC_SMB_CK1 EC_SMB_DA1	KB9012			V								V		V		
EC_SMB_CK2 EC_SMB_DA2	KB9012					V	V	V		V	V					
PCH_SMLCLK PCH_SML0DATA	PCH															
PCH_SML1CLK PCH_SML1DATA	PCH															
MEM_SMBCLK MEM_SMBDATA	PCH		V		V				V				V		V	V



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PEG_GTX_HRX_P10_15] 29.30
PEG_GTX_HRX_N10_15] 29.30
PEG_HTX_C_GRX_P10_15] 29.30
PEG_HTX_C_GRX_N10_15] 29.30



PEG_RXN_0	E23	PEG_COMP	M29	PEG_GTX_C_HRX_N0	CC1	1	2	0.22U	0402	16V7K-D	PEG_GTX_HRX_N0
PEG_RXN_1	K28	PEG_GTX_C_HRX_N1	CC2	1	2	0.22U	0402	16V7K-D	PEG_GTX_HRX_N1		
PEG_RXN_2	M31	PEG_GTX_C_HRX_N2	CC3	1	2	0.22U	0402	16V7K-D	PEG_GTX_HRX_N2		
PEG_RXN_3	L30	PEG_GTX_C_HRX_N3	CC4	1	2	0.22U	0402	16V7K-D	PEG_GTX_HRX_N3		
PEG_RXN_4	M33	PEG_GTX_C_HRX_N4	CC5	1	2	0.22U	0402	16V7K-D	PEG_GTX_HRX_N4		
PEG_RXN_5	L32	PEG_GTX_C_HRX_N5	CC13	1	2	0.22U	0402	16V7K-D	PEG_GTX_HRX_N5		
PEG_RXN_6	M35	PEG_GTX_C_HRX_N6	CC6	1	2	0.22U	0402	16V7K-D	PEG_GTX_HRX_N6		
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PEG_RXN_8	E29	PEG_GTX_C_HRX_N8	CC8	1	2	0.22U	0402	16V7K-D	PEG_GTX_HRX_N8		
PEG_RXN_9	D28	PEG_GTX_C_HRX_N9	CC9	1	2	0.22U	0402	16V7K-D	PEG_GTX_HRX_N9		
PEG_RXN_10	E31	PEG_GTX_C_HRX_N10	CC10	1	2	0.22U	0402	16V7K-D	PEG_GTX_HRX_N10		
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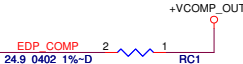
Near MXM Connector

INTEL_HASWELL_HASWELL

CONN@

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Issued Date	2012/05/28	Deciphered Date	2013/05/27	CPU (I7) DMI,PEG	
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COMPENSATION PU FOR eDP

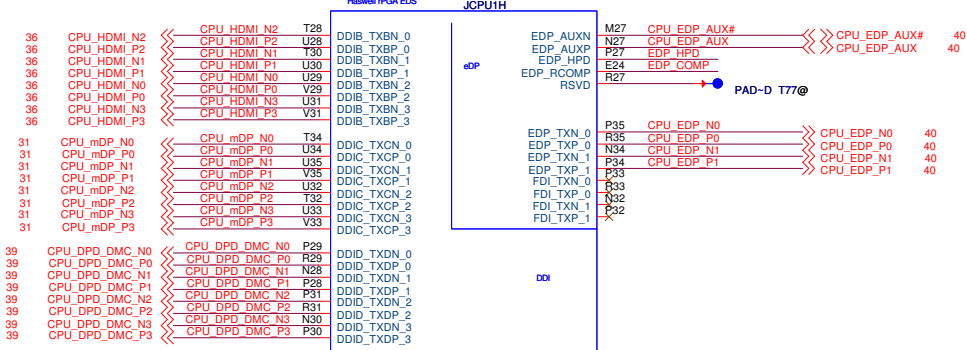


CAD Note:Trace width=20 mils ,Spacing=25mil,
Max length=100 mils.

HDMI

mDP

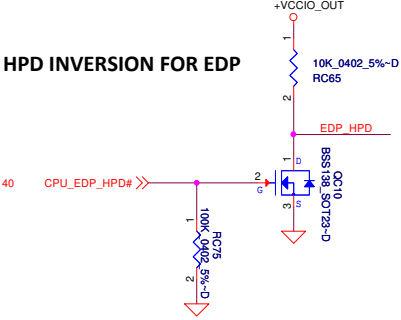
DMC



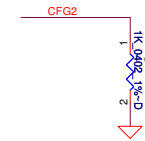
INTEL_HASWELL_HASWELL 8 OF 9

CONN@

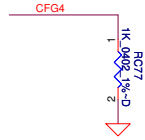
HPD INVERSION FOR EDP



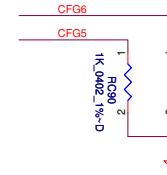
CFG STRAPS for CPU



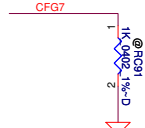
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



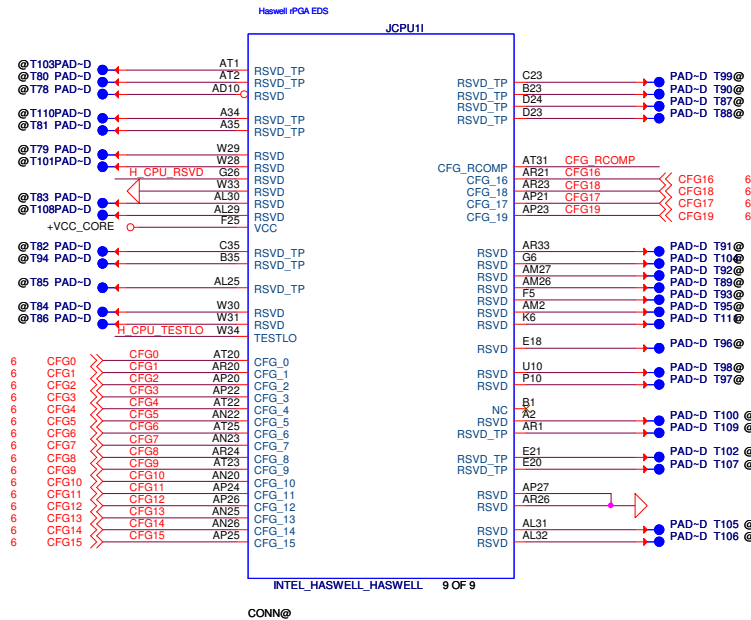
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

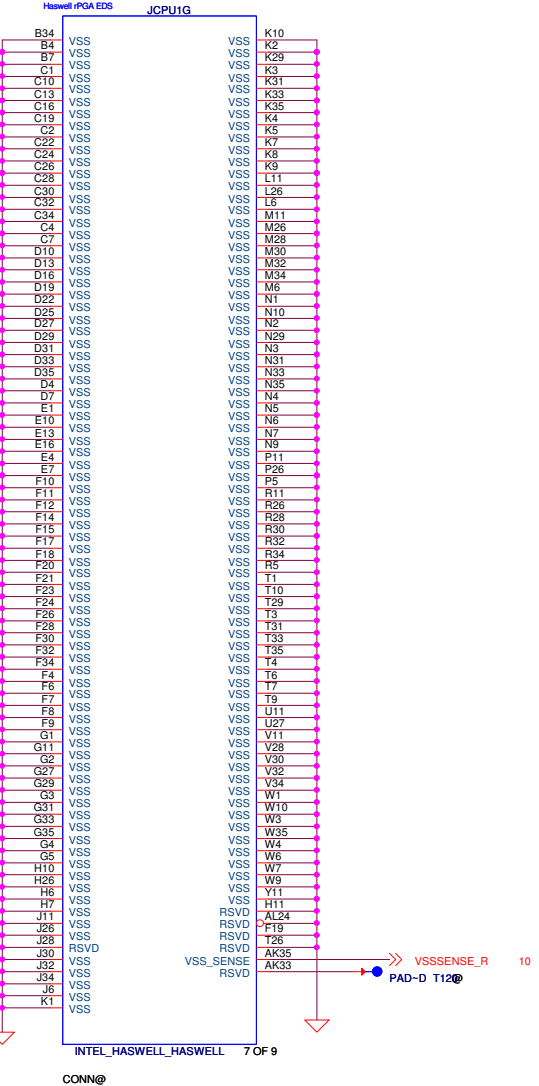
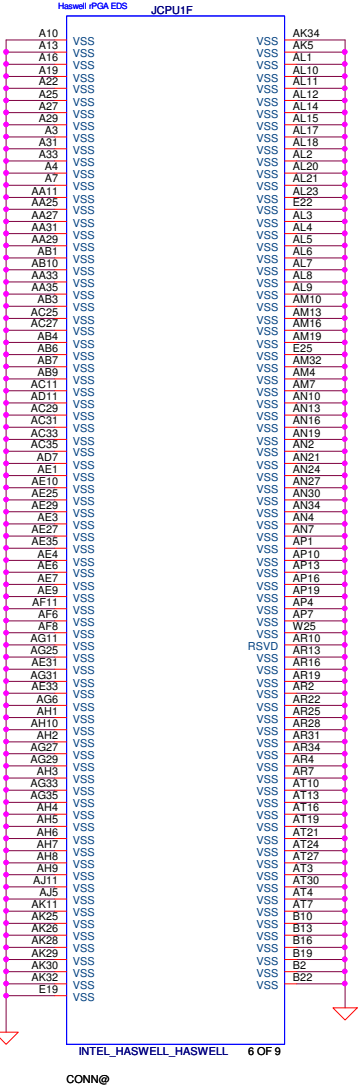


PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training





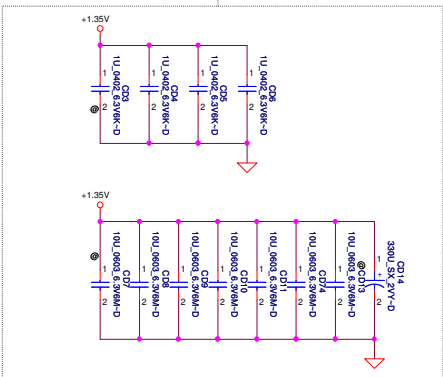
JDIMMA H=9.2mm



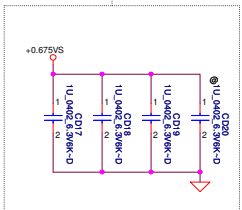
All VREF traces should have 20 mil trace width



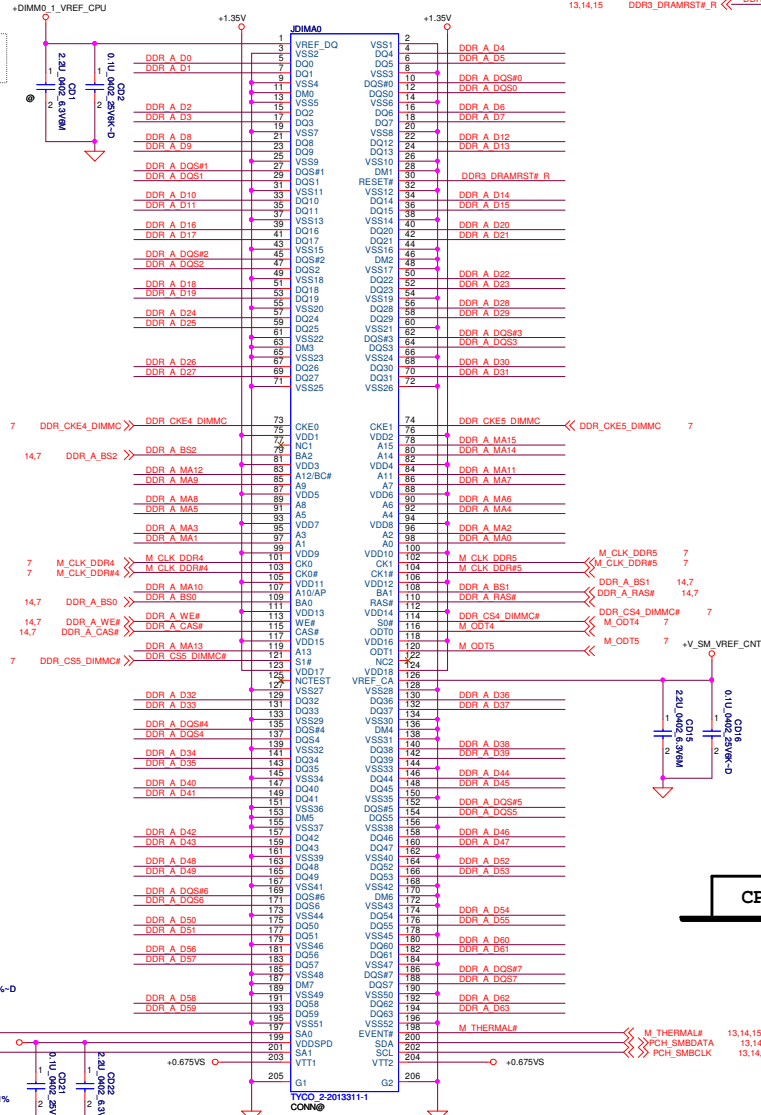
Layout Note:
Place near JDIMMA



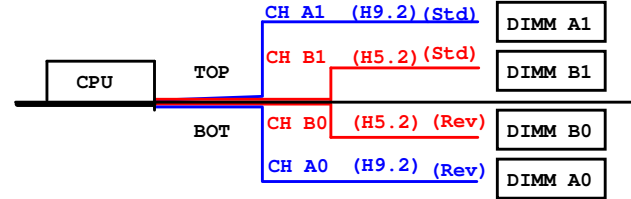
Layout Note:
Place near JDIMMA.203,204



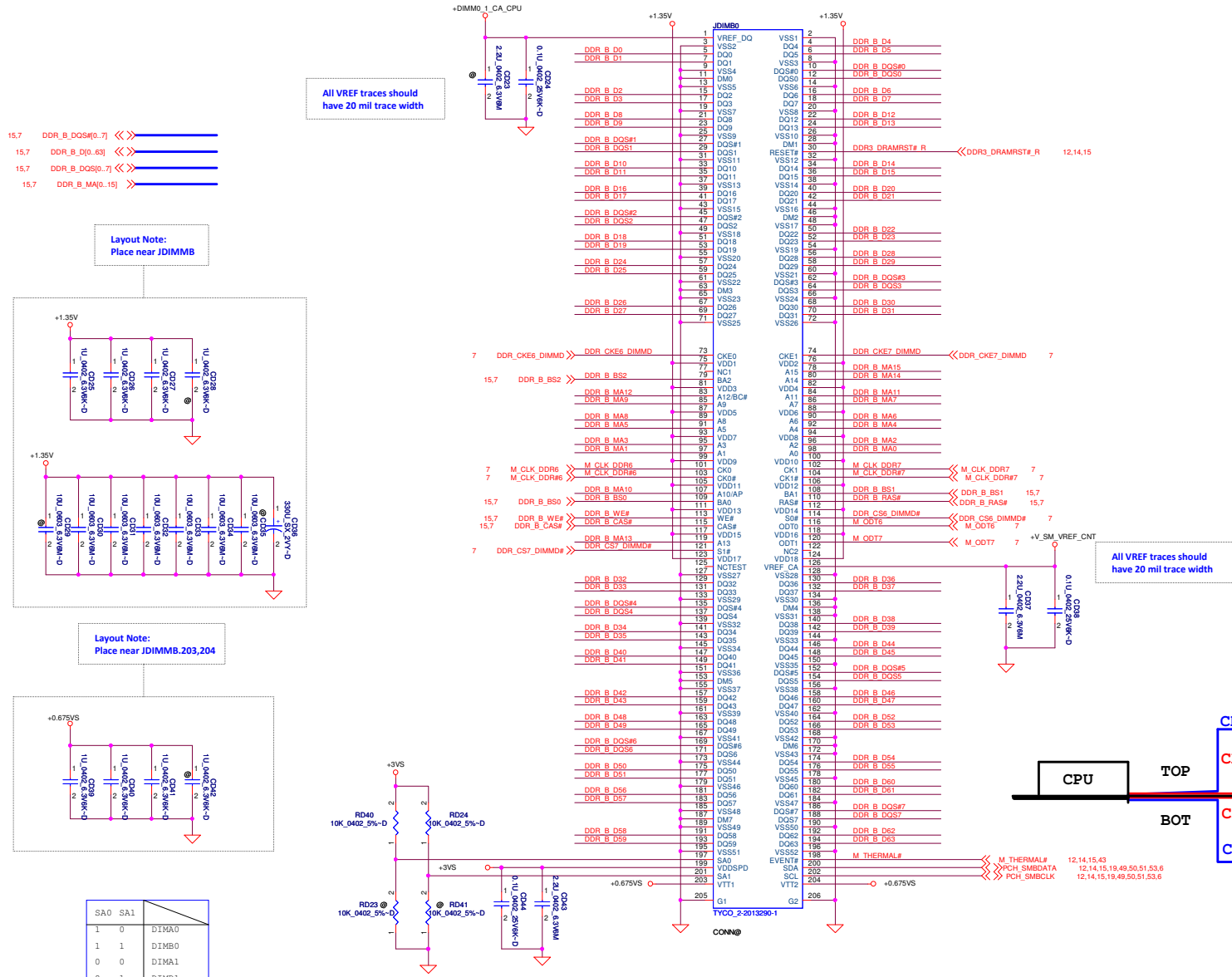
SA0	SA1	
1	0	DIMMA0
1	1	DIMMA1
0	0	DIMMA2
0	1	DIMMA3



All VREF traces should have 20 mil trace width



JDIMMB H=5.2mm

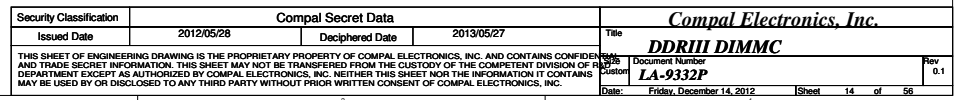


Layout Note:
Place near JDIMMB

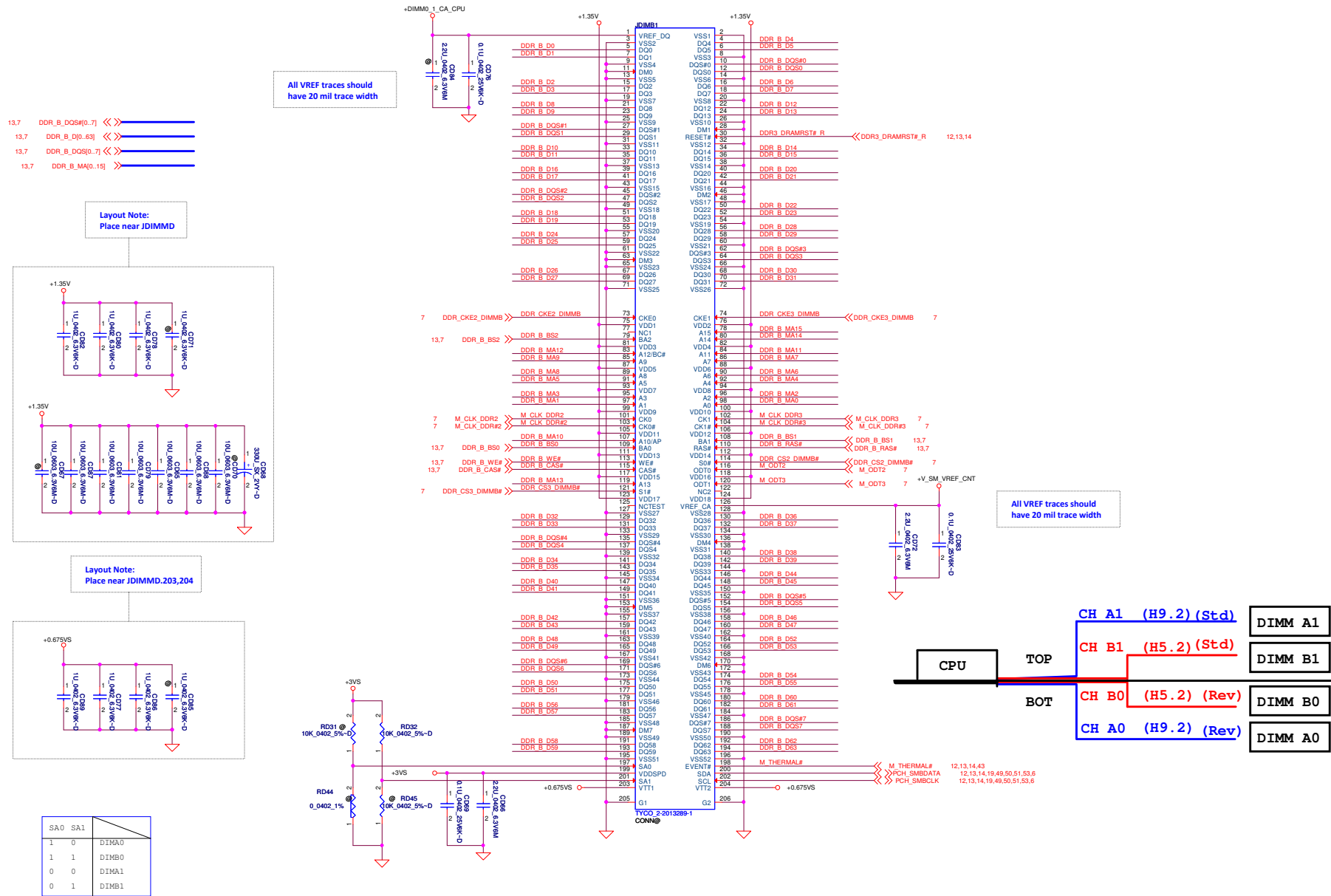
Layout Note:
Place near JDIMMB.203,204

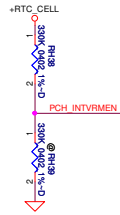
SA0	SA1	
1	0	DIMM0
1	1	DIMM1
0	0	DIMM2
0	1	DIMM3

CH A1 (H9.2) (Std)	DIMM A1
CH B1 (H5.2) (Std)	DIMM B1
CH B0 (H5.2) (Rev)	DIMM B0
CH A0 (H9.2) (Rev)	DIMM A0

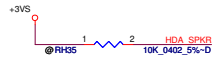


JDIMMD H=5.2mm

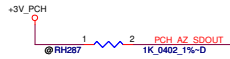




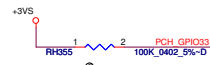
INTVRMEN - INTEGRATED SUS 1.05V VRM
ENABLE
High - Enable Internal VRs
Low - Enable External VRs



NO REBOOT STRAP
DISABLED WHEN LOW (DEFAULT)
ENABLED WHEN HIGH



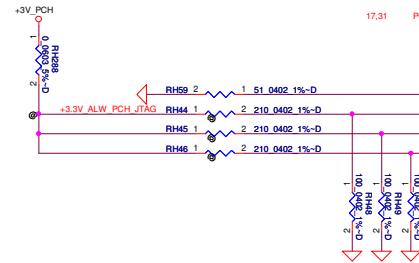
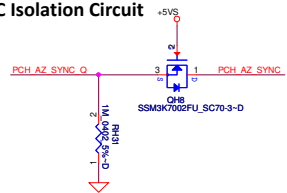
FLASH DESCRIPTOR SECURITY OVERRIDE
LOW = DISABLED (DEFAULT)
HIGH = ENABLED



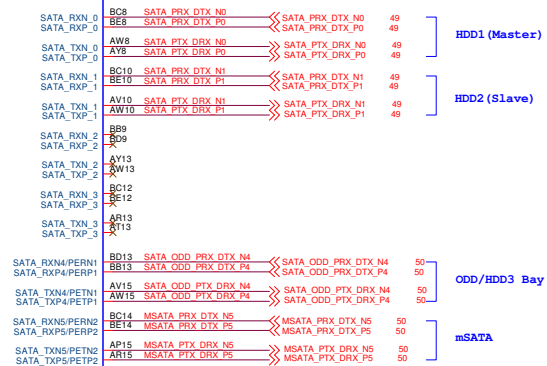
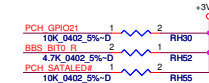
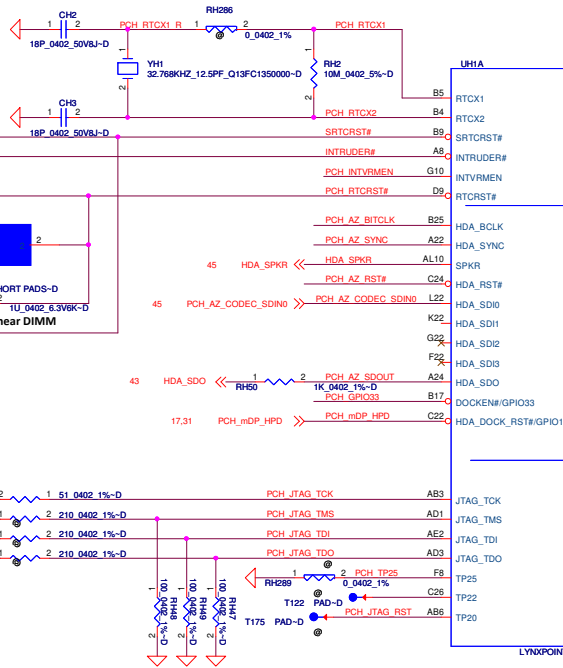
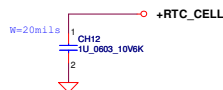
CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

HDA_SYNC Isolation Circuit



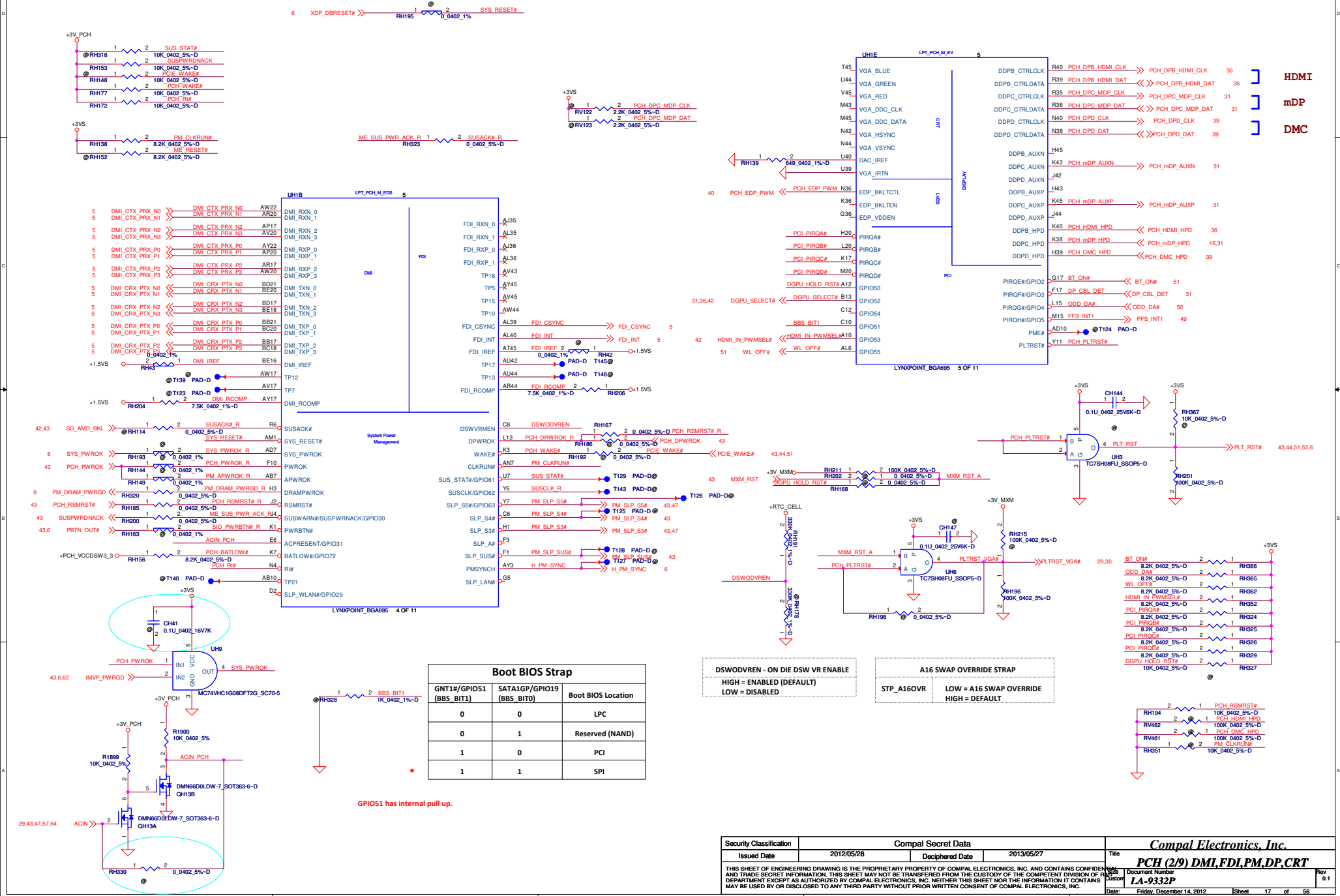
HDA for Codec



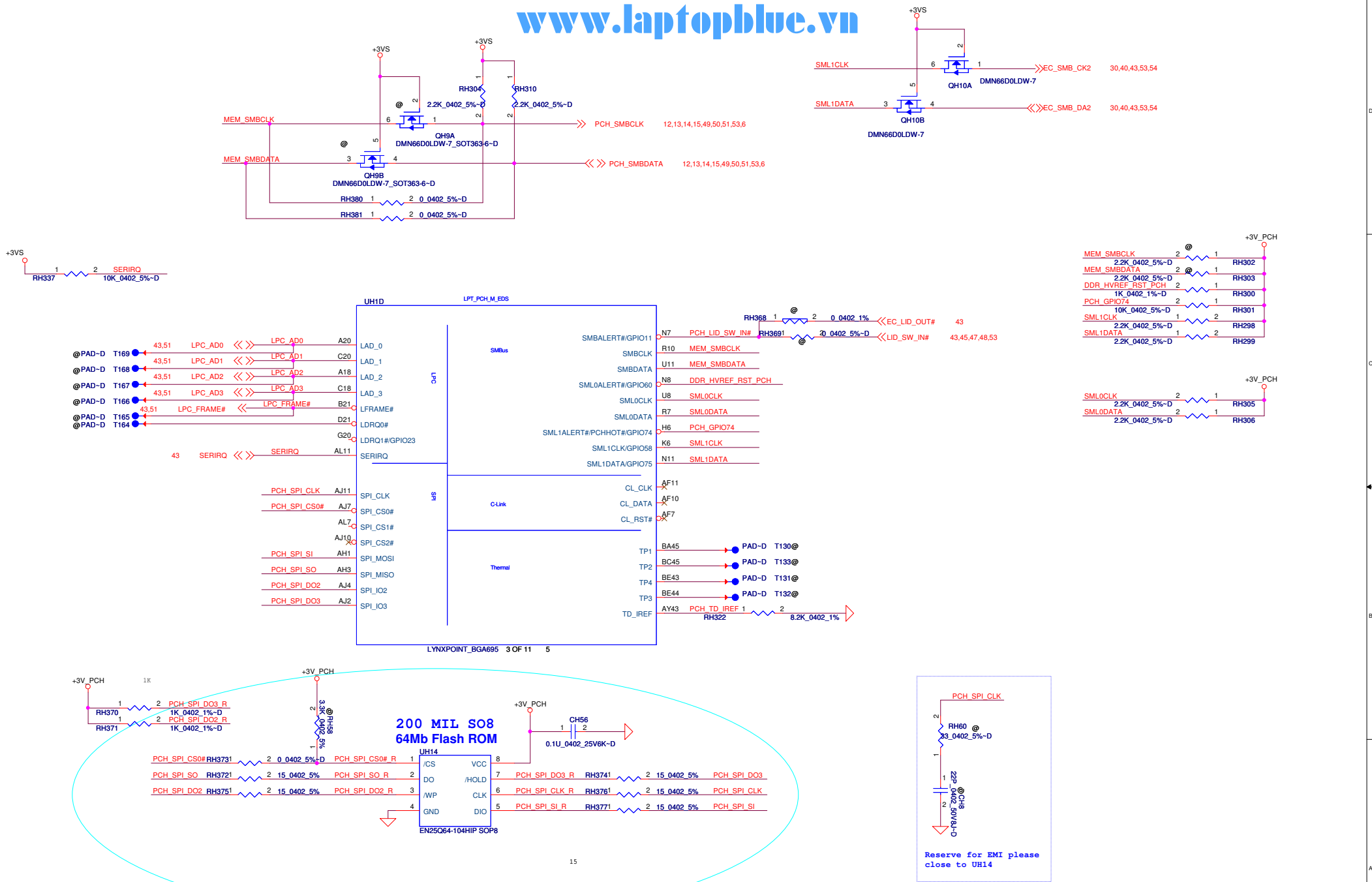
SATA Impedance Compensation

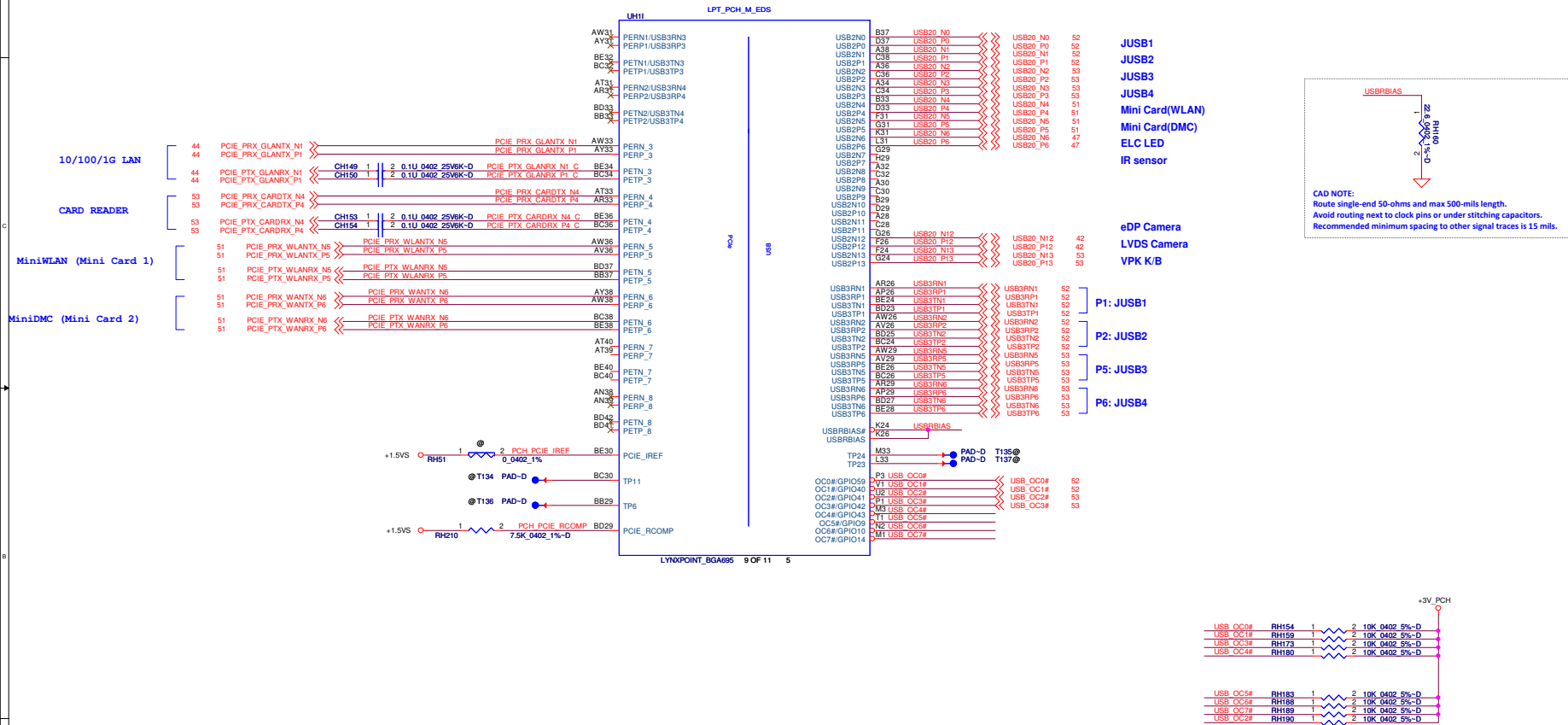


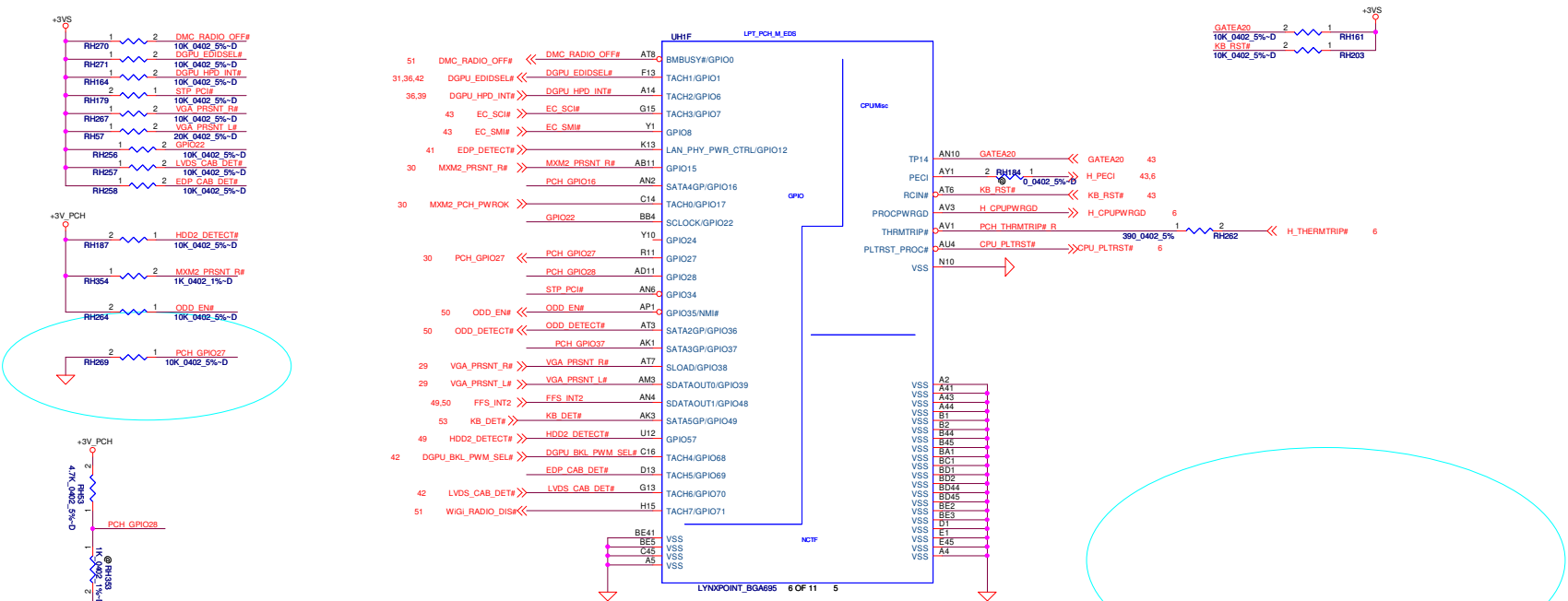
CAD note:
Place the resistor within 500 mils of the PCH. Avoid routing next to clock pins.



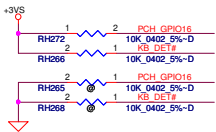






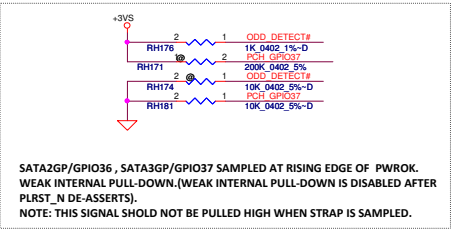


PLL ON DIE VR ENABLE
ENABLED - HIGH(DEFAULT)
DISABLED - LOW

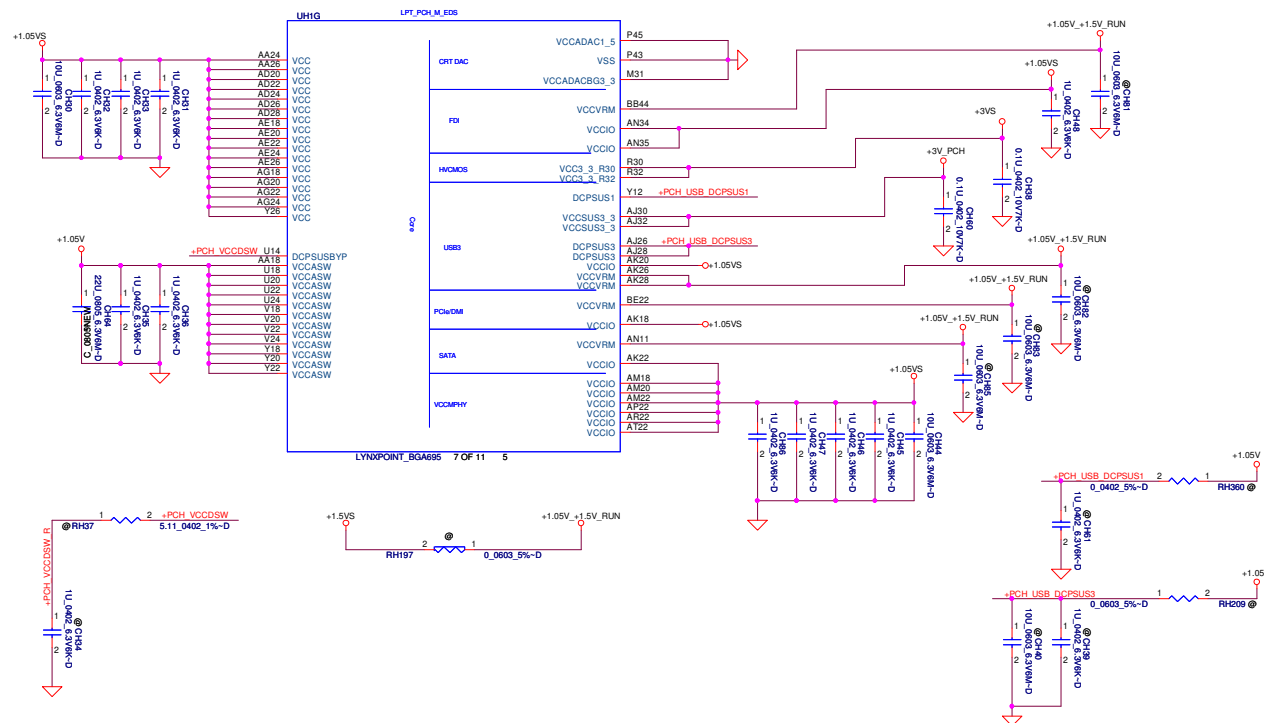


Config	GPIO16,49
USB X4,PCIEX8,SATAx6	11
USB X6,PCIEX8,SATAx4	01

Fixed Signals				Muxed Signals		Fixed Signals						Muxed Signals		Fixed Signals			
USB3 1	USB3 2	USB3 5	USB3 6	PCIE 1	PCIE 2	PCIE 3	PCIE 4	PCIE 5	PCIE 6	PCIE 7	PCIE 8	SATA 4	SATA 5	SATA 0	SATA 1	SATA 2	SATA 3
				(00)	(00)							(00)	(00)				
				USB3 3	USB3 4							PCIE 1	PCIE 2				



SATA2GP/GPIO36, SATA3GP/GPIO37 SAMPLED AT RISING EDGE OF PWROK.
WEAK INTERNAL PULL-DOWN.(WEAK INTERNAL PULL-DOWN IS DISABLED AFTER PLRST_N DE-ASSERTS).
NOTE: THIS SIGNAL SHOULD NOT BE PULLED HIGH WHEN STRAP IS SAMPLED.



PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCADAC1_5	1.5V	0.070 A
VCCADAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A

Security Classification

Compal Secret Data

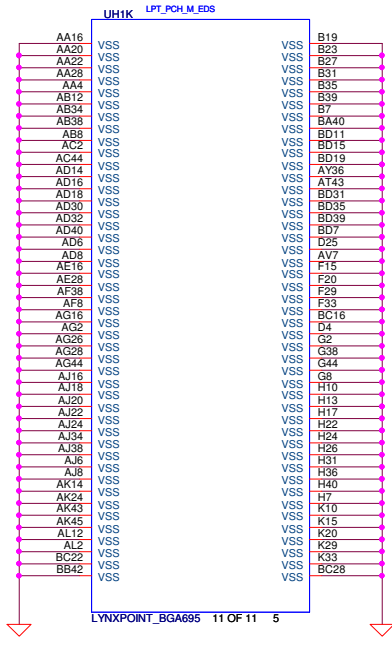
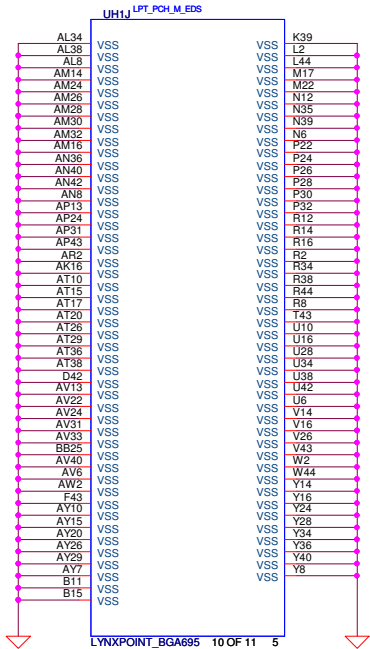
Compal Electronics, Inc.

PCH (7/9) Power

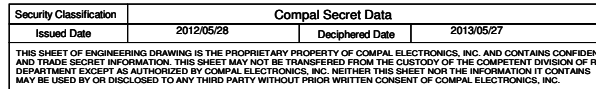
Document Number
LA-9332P

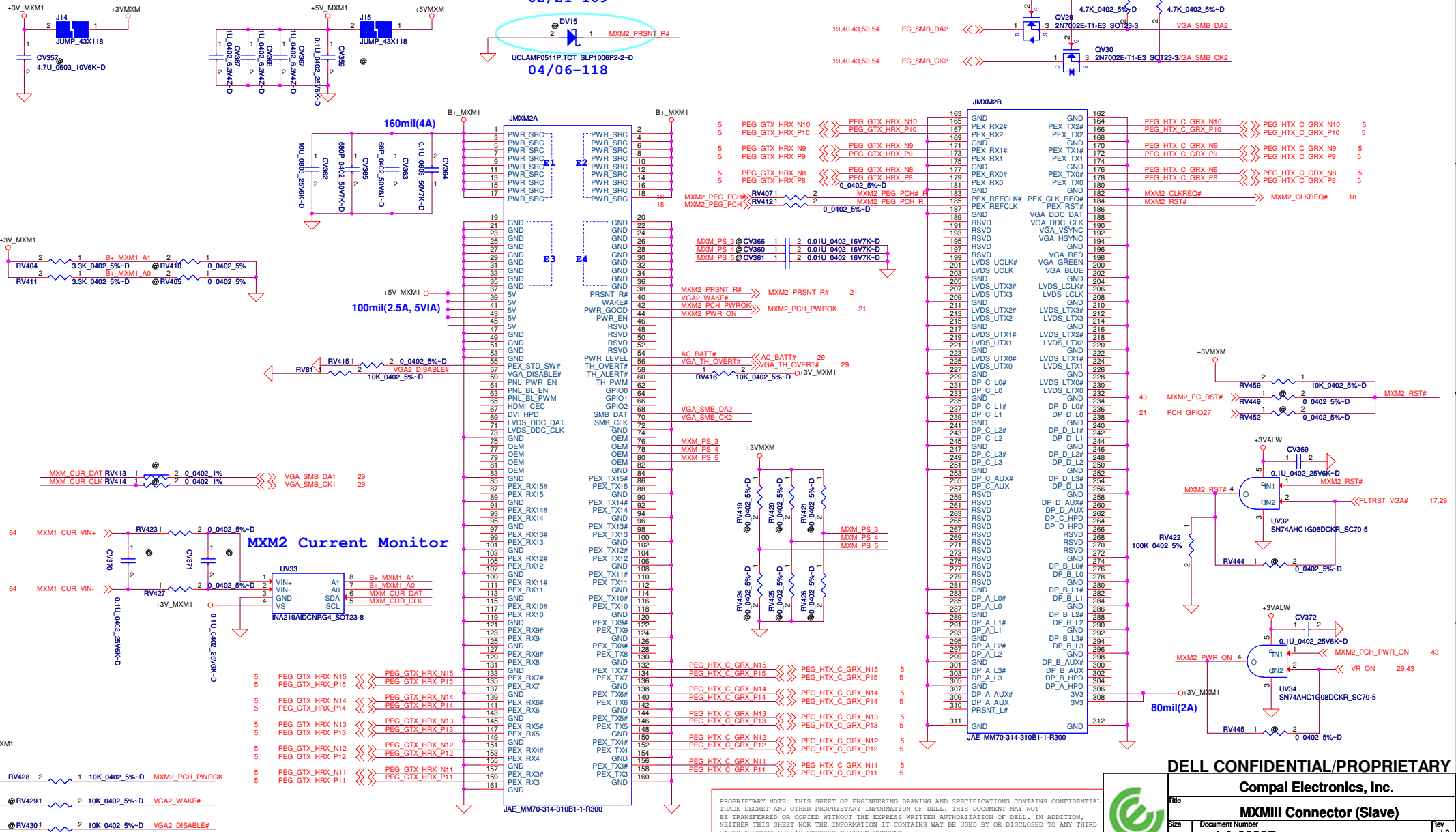
Date:	Friday, December 14, 2012	Sheet	22	of	56
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Rev	
0.1	



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Issued Date	2010/08/25	Deciphered Date	2012/08/25	Title	Cactus (3/4) PWR/VSS/DC-DC
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				Date:	Friday, December 14, 2012
				Sheet	27 of 56
				Rev	0.1





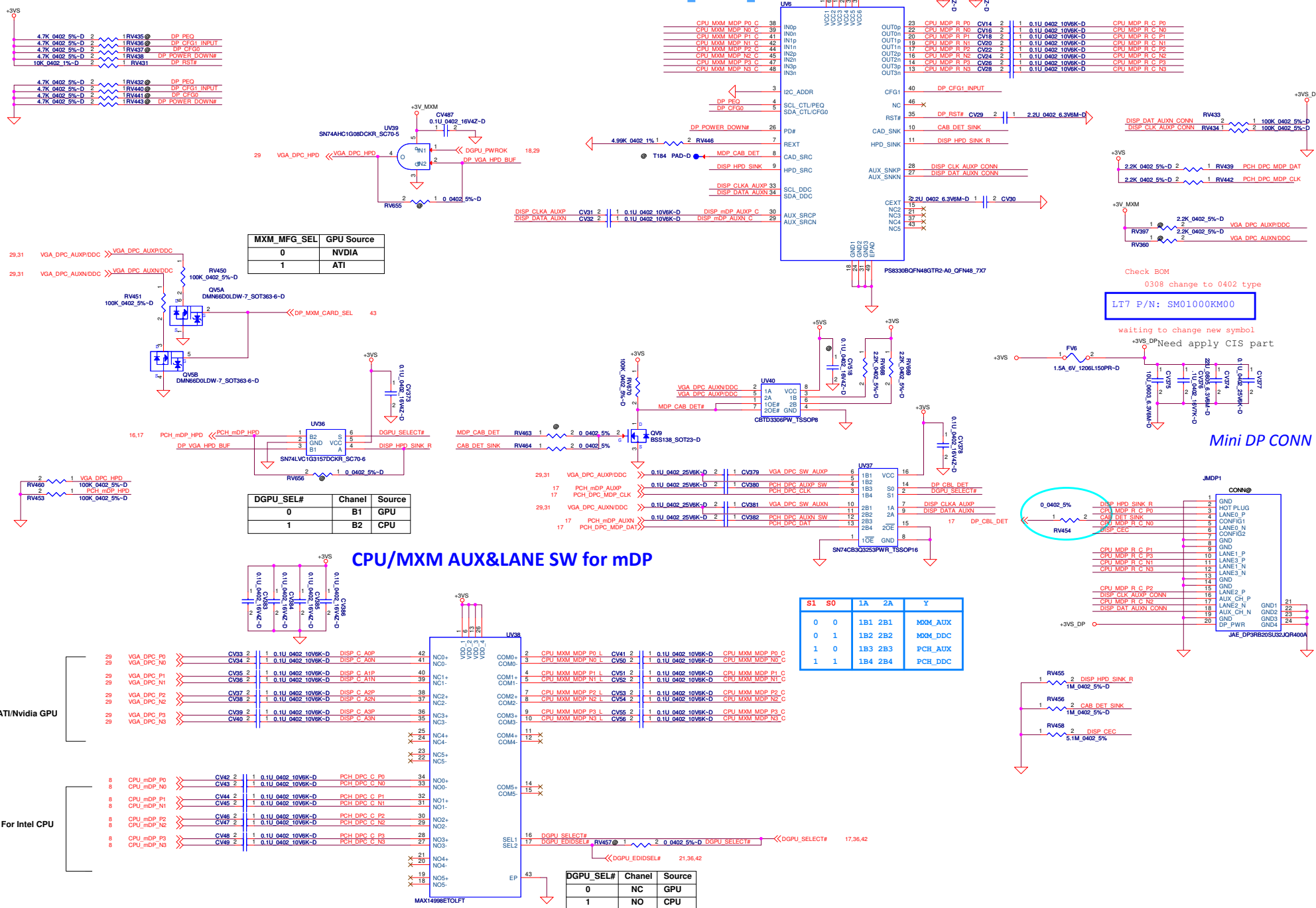
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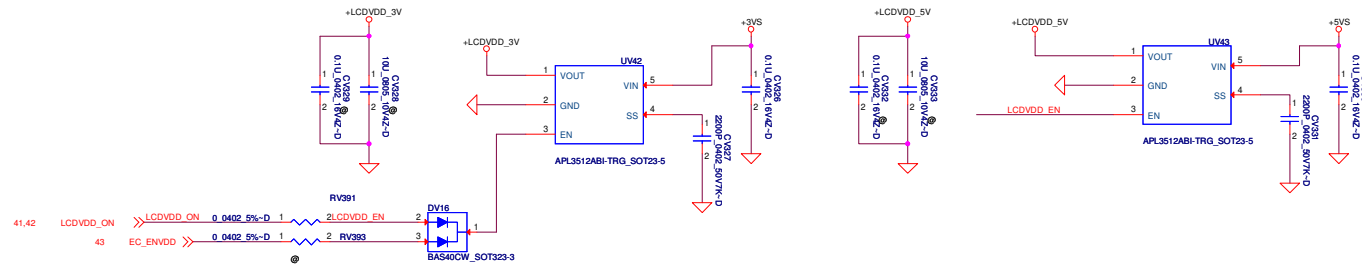
Compal Electronics, Inc.

Title	MXM2 Connector (Slave)		
Size	Document Number	LA-9332P	Rev 1.0
Date	Friday, December 14, 2012	Sheet	30 of 56

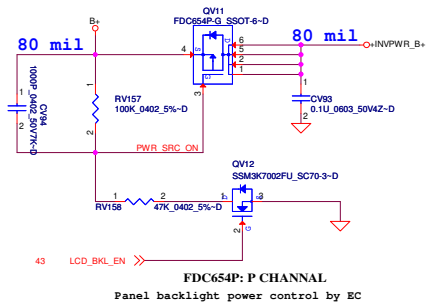


Security Classification	Compal Secret Data		Title	
Issued Date	2012/05/14	Deciphered Date	2013/05/13	Mini DP/Thunder Bolt power
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			Document Number LA-9332P	
			Date Feb-29, December 14, 2012	Sheet 31 of 56

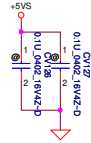
LCD POWER



Back light power



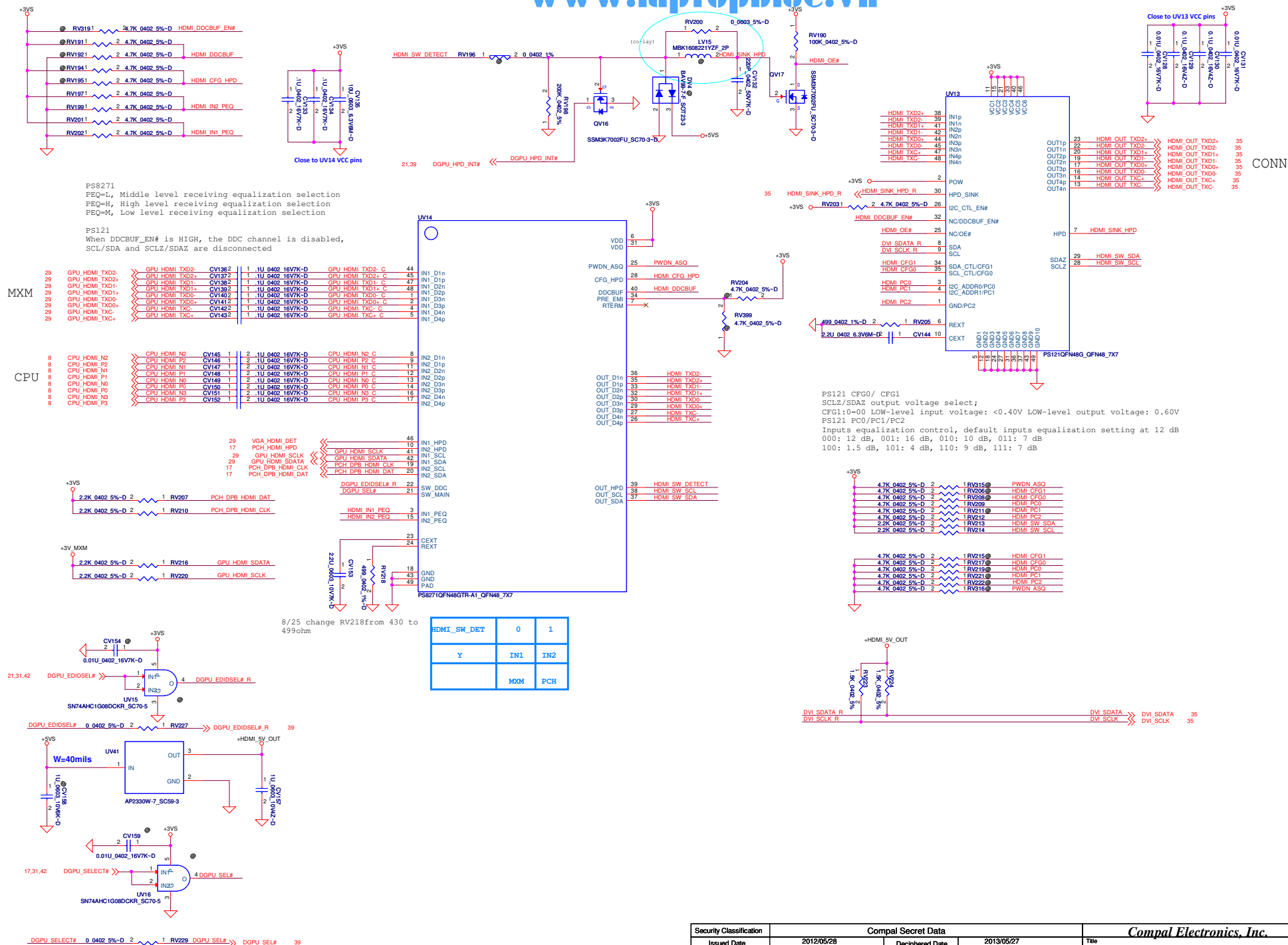
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Date: Friday, December 14, 2012				Sheet 34 of 56	

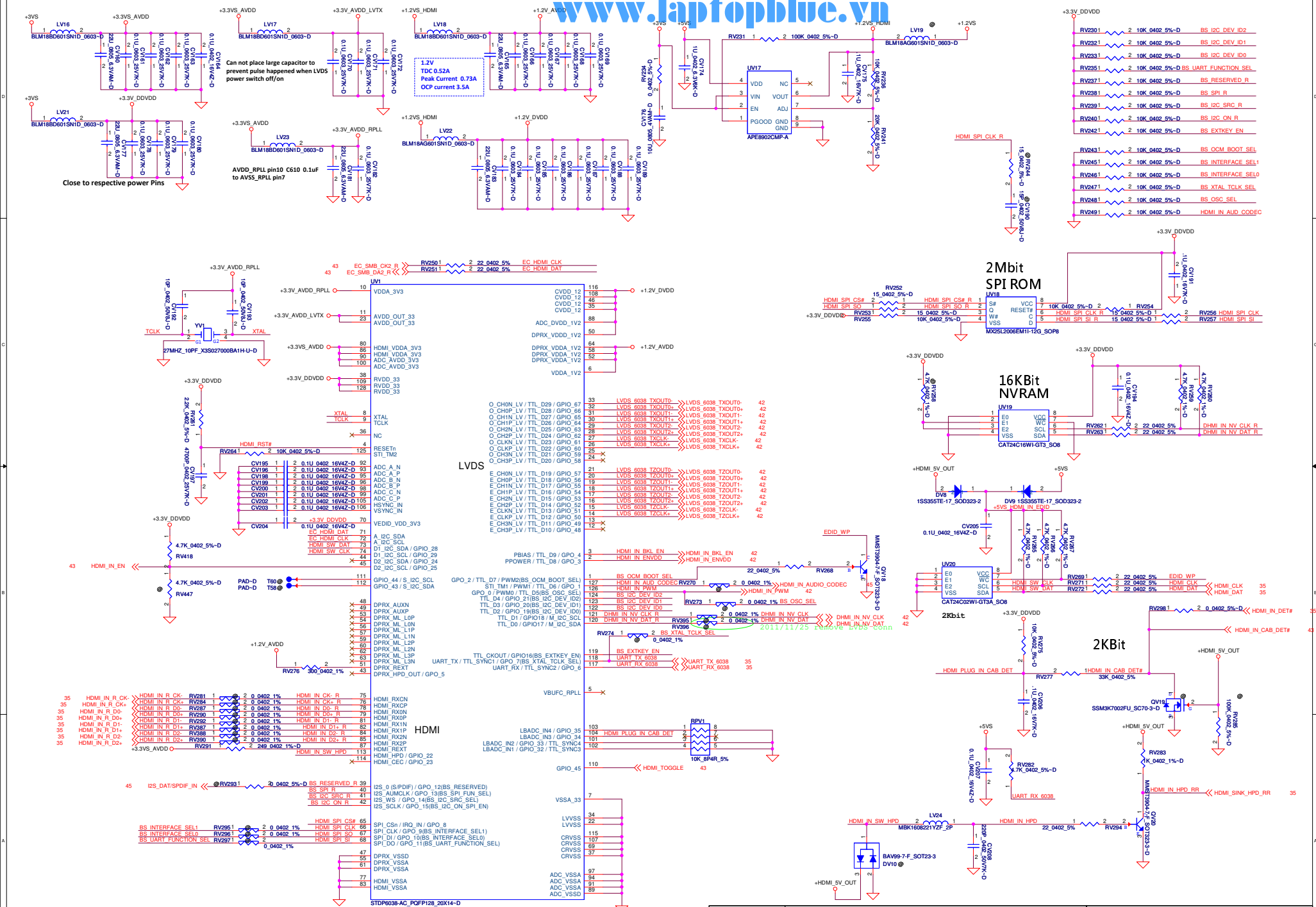


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A-9332P

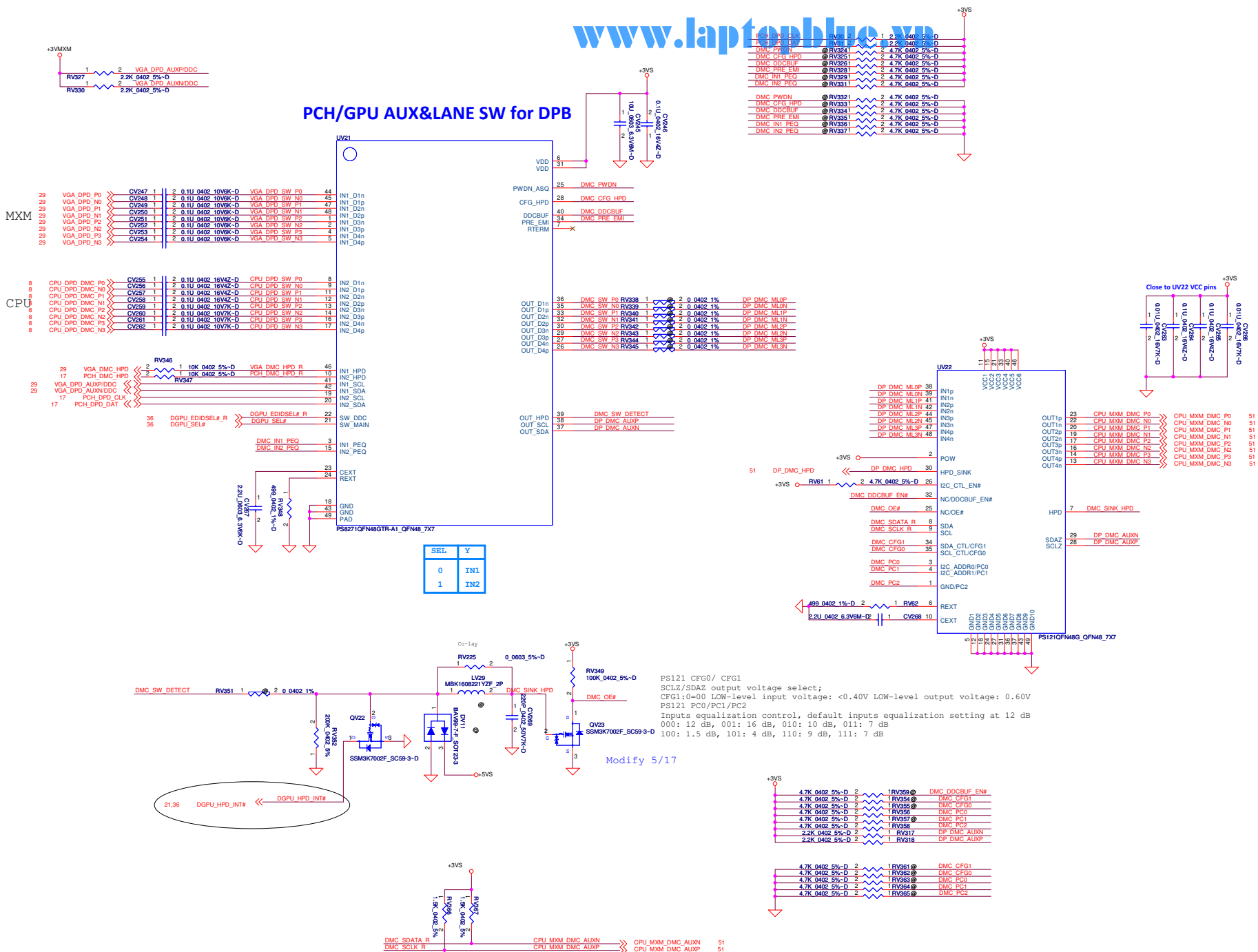
Date: Friday, December 14, 2012 Sheet 35 of 56



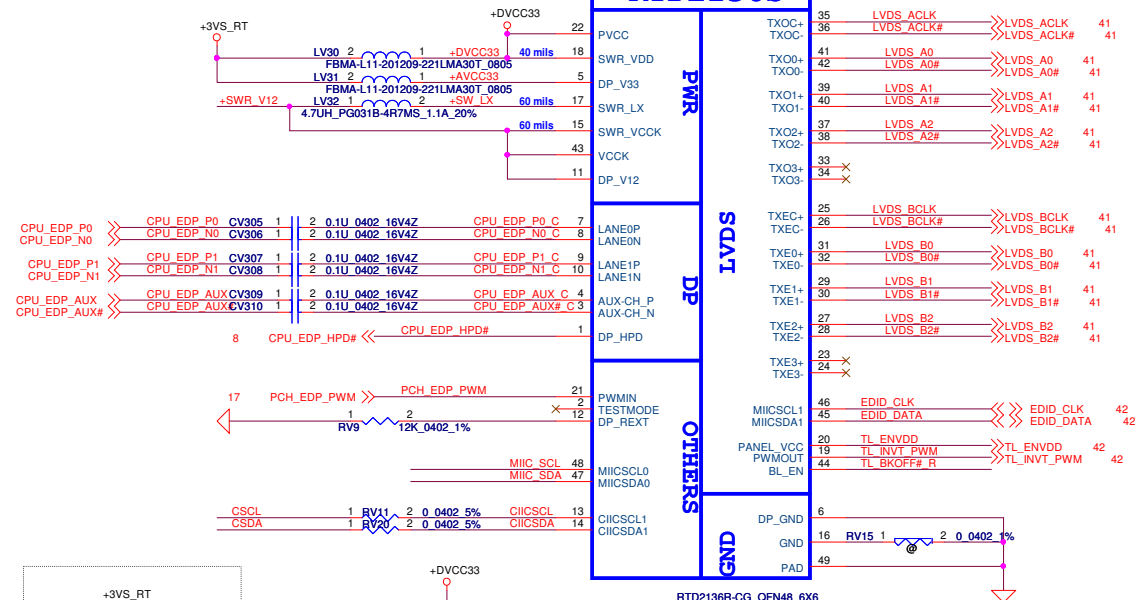
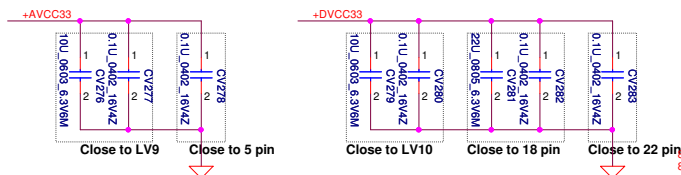
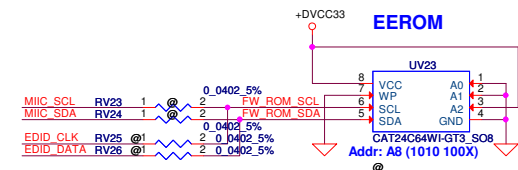


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2012/05/14		2013/05/13		HDMI to LVDS-STD P6038	
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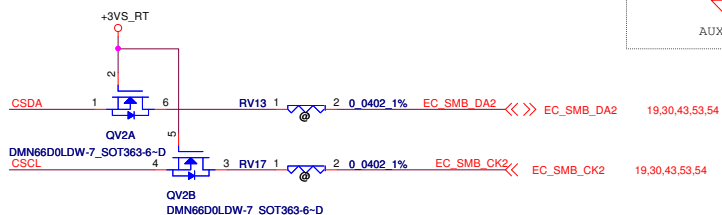
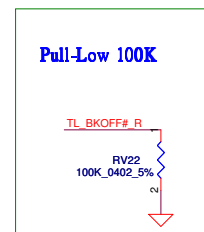
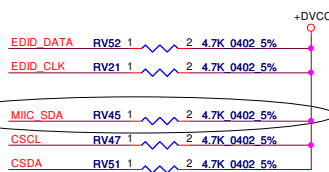
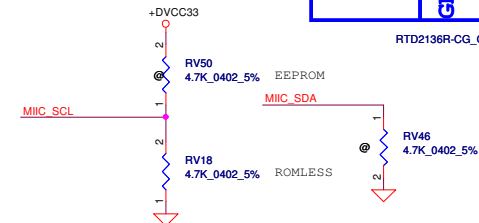
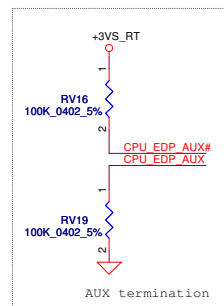
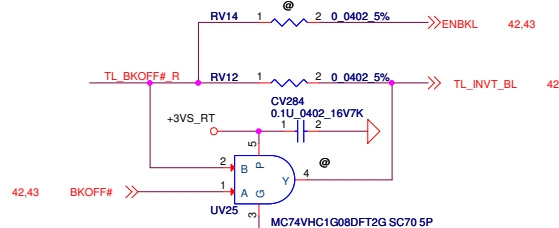
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Issued Date	2012/05/14	Deciphered Date	2013/05/13	Title	LVDS to eDP-STDP4028
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				LA-9332P	0.1
				Date: Friday, December 14, 2012	Sheet 38 of 58



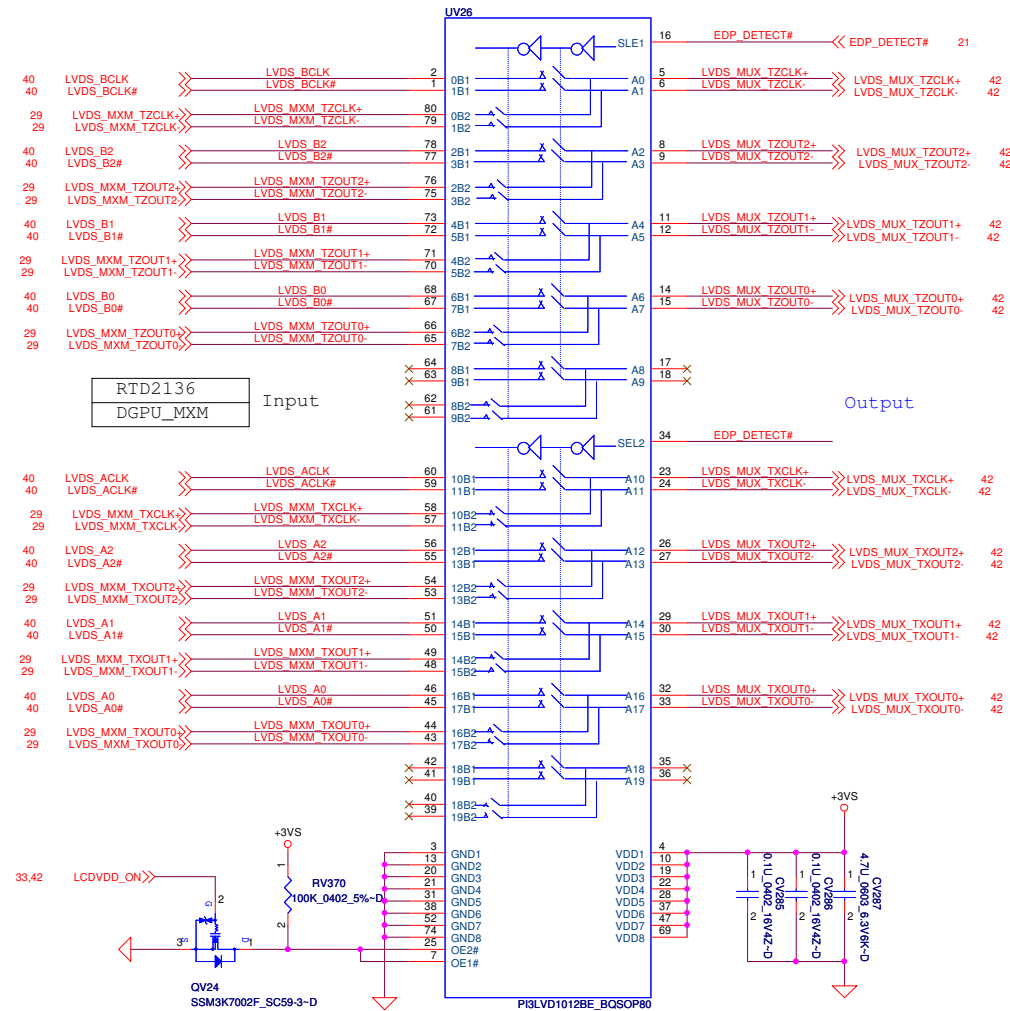
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Issued Date	2012/05/14	Deciphered Date	2013/05/13	Title DP SW for DMC Document Number LA-9332P
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			Sheet	39 of 56



Vendor advise reserve it



STDP6038 SW STDP4028 PCH/GPU AUX for LVDS

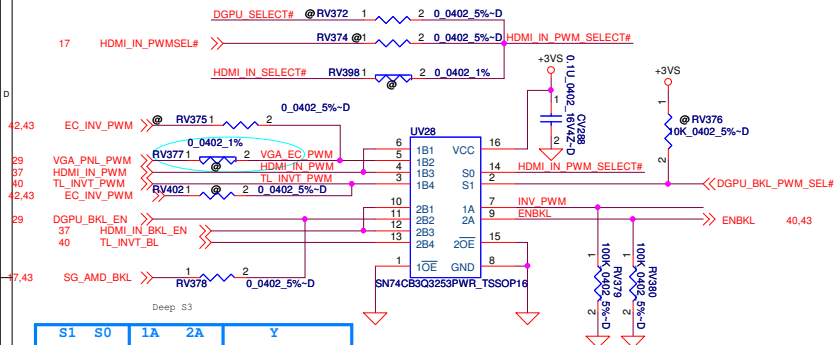


SEL	Y
L	RTD2136
H	DGPU_MXM

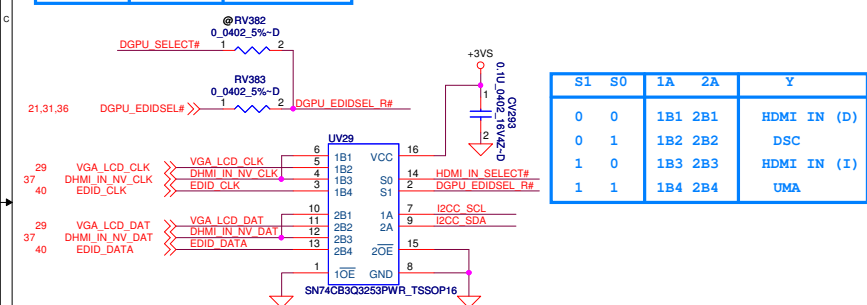
LCD Backlight Selector

PCH/GPU MUX & 6038 MUX SW for LVDS

www.laptopblue.vn



LCD DDC Selector



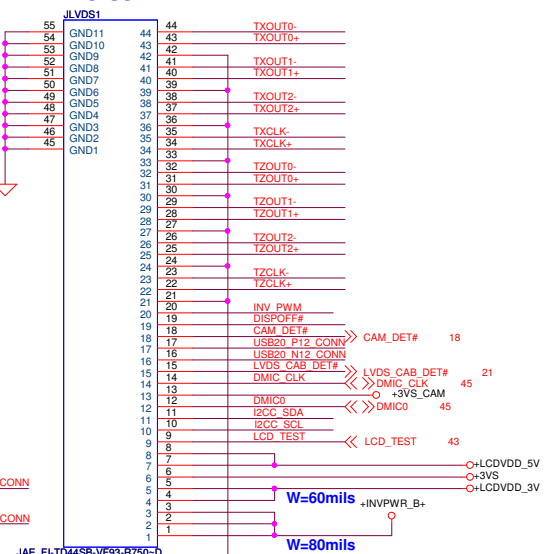
CPU/MXM (MUX)
HDMI IN (6038)

Input

Output

SEL	Y
L	B1
H	B2

LVDS Conn.



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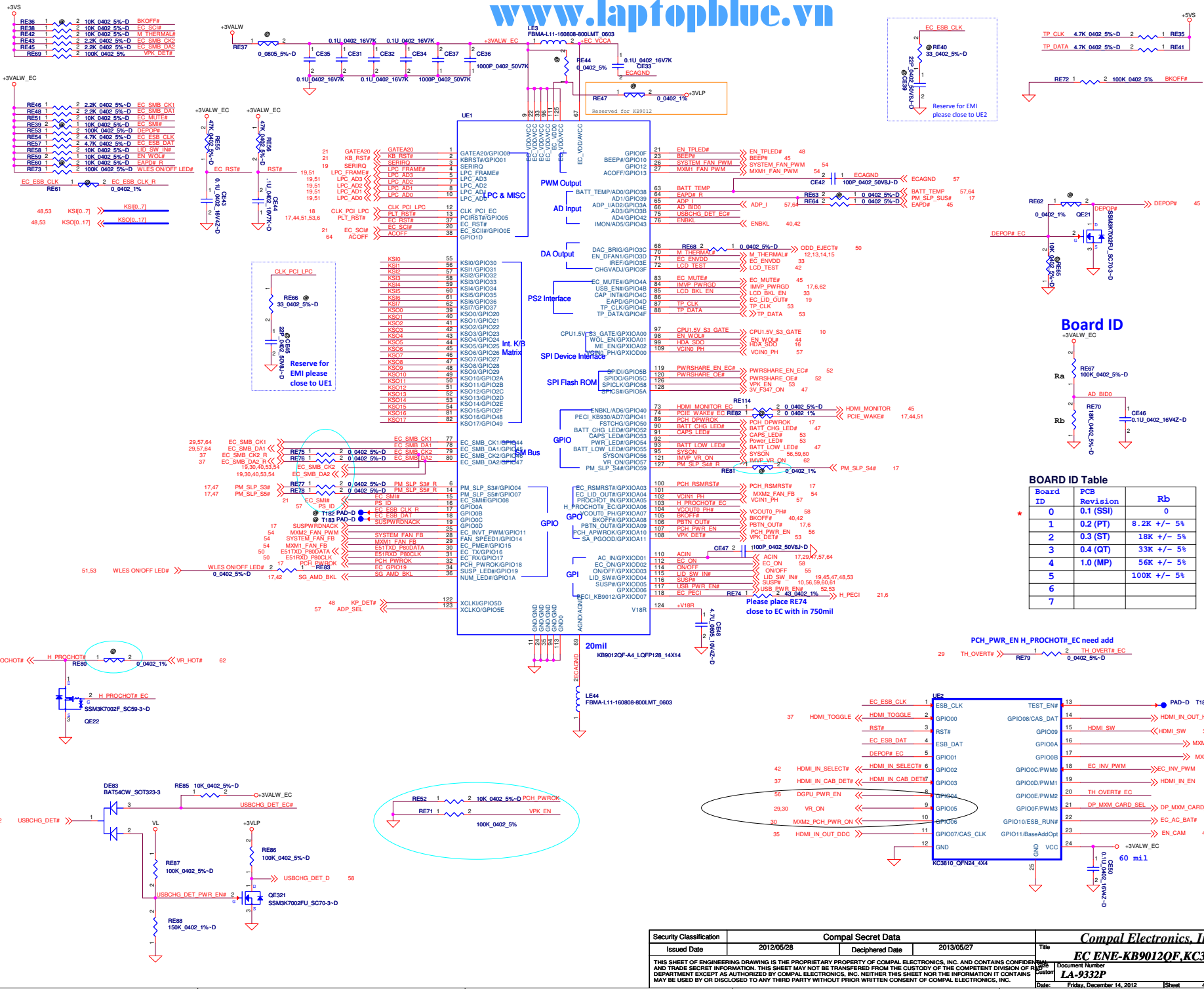
Compal Electronics, Inc.

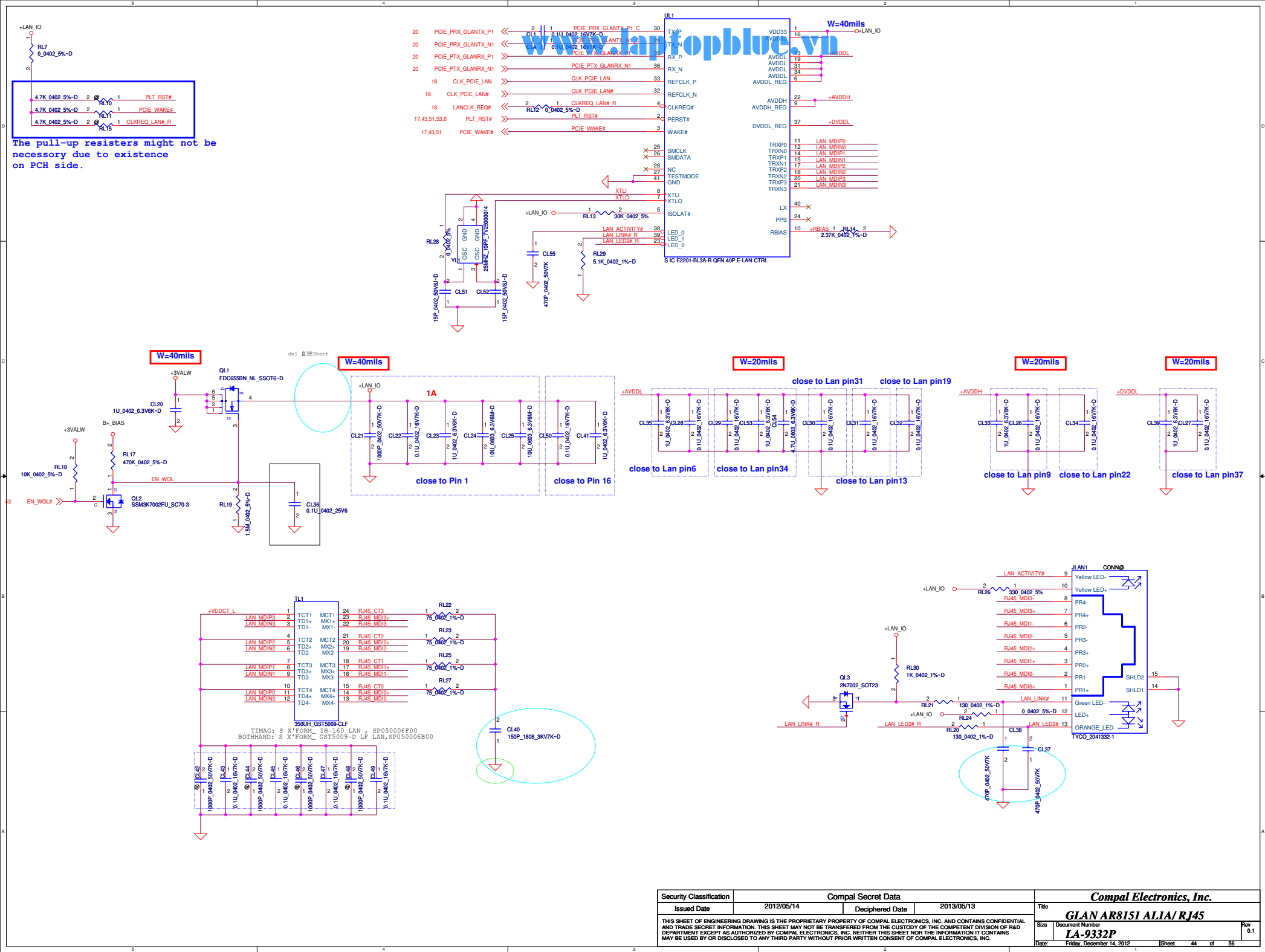
LVDS SW- 6038/SYSTEM & CONN

Size	Document Number	Rev
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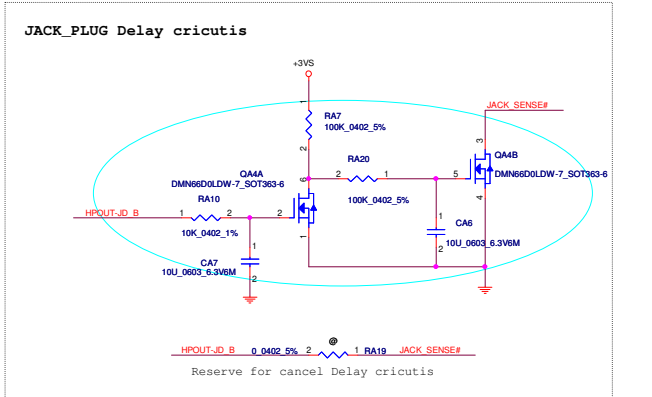
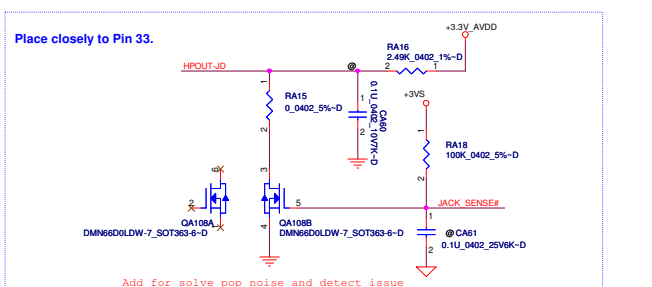
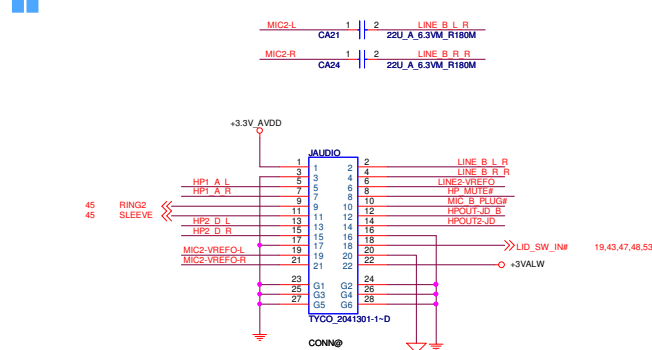
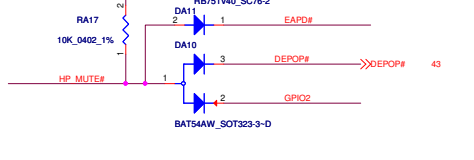
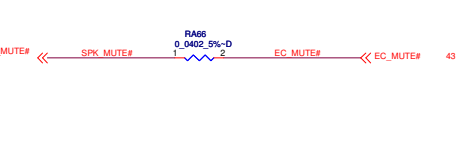
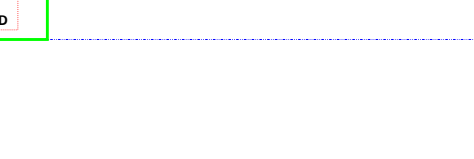
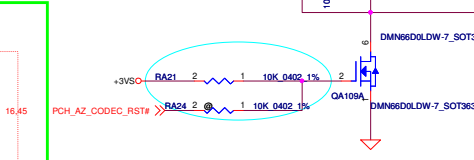
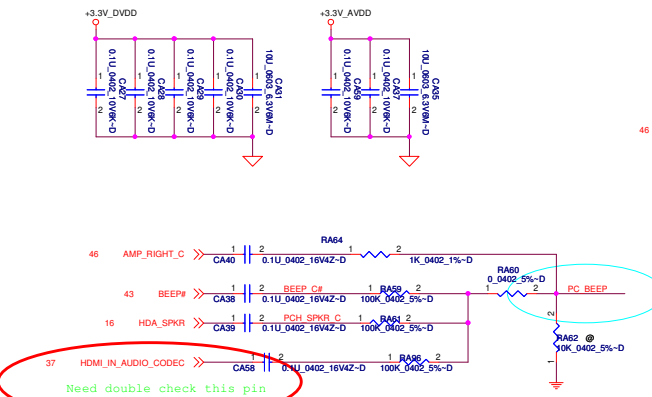
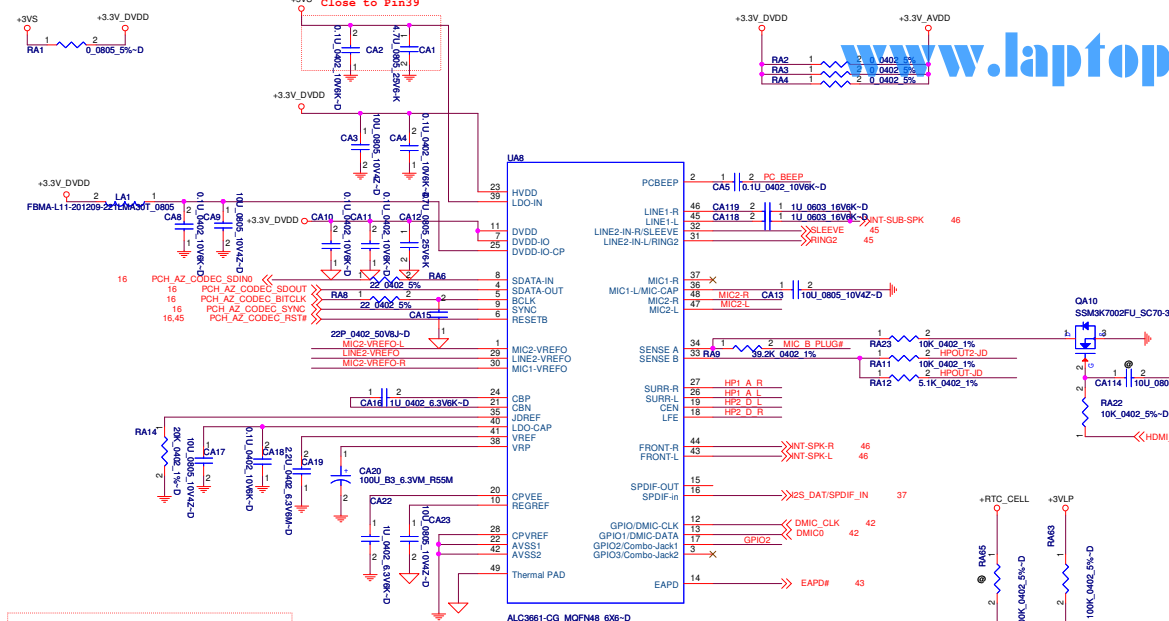
Date: Friday, December 14, 2012 Sheet 42 of 56

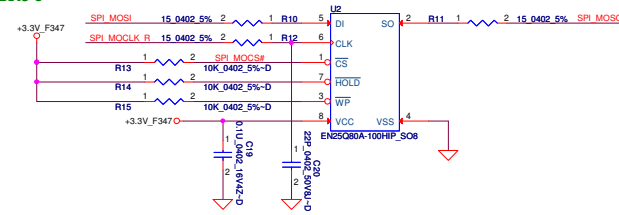
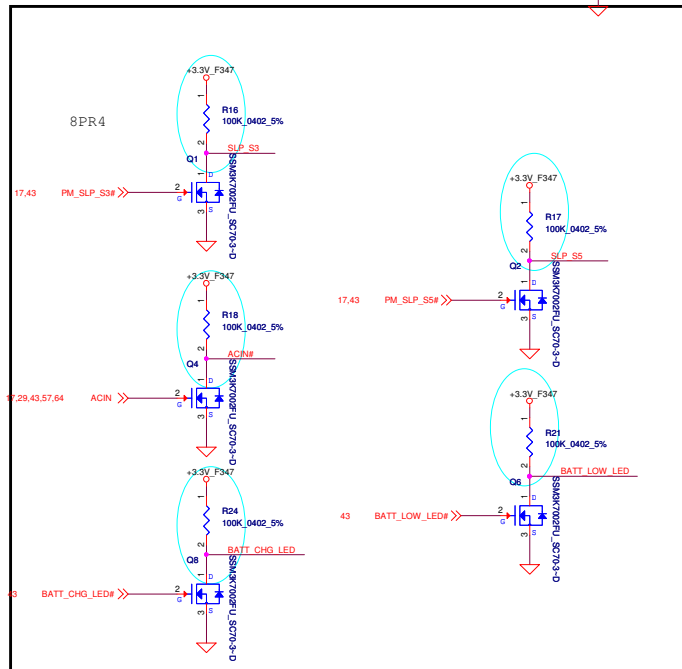
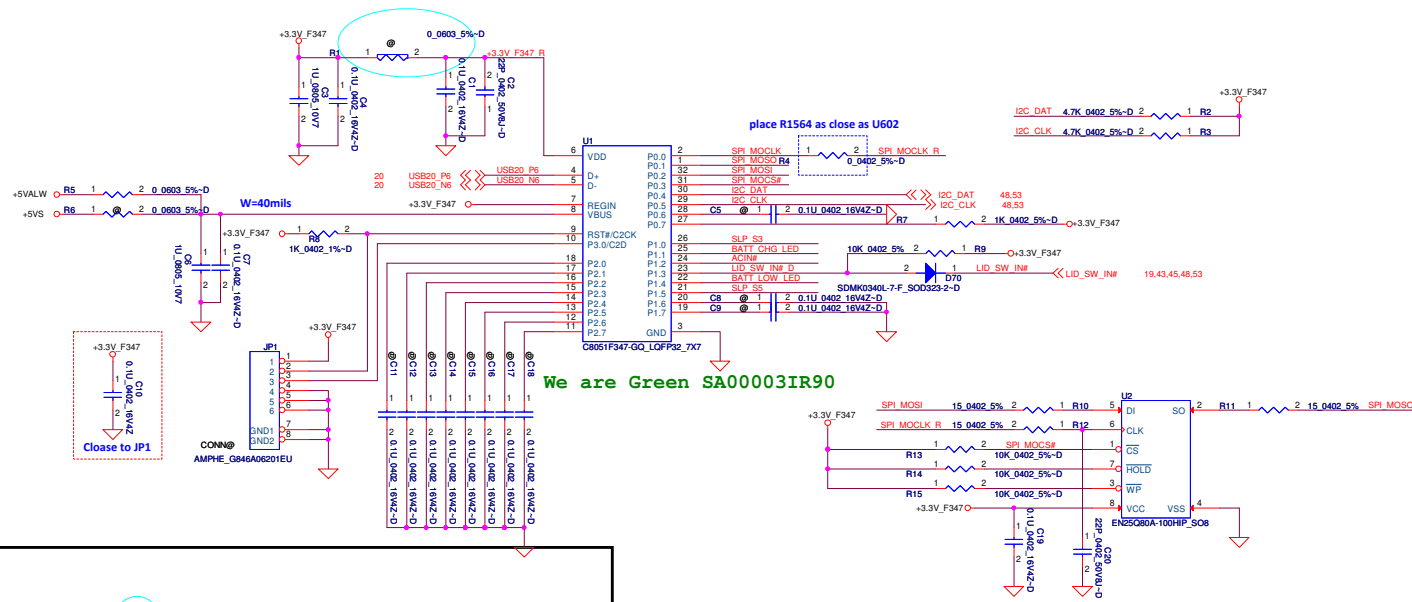
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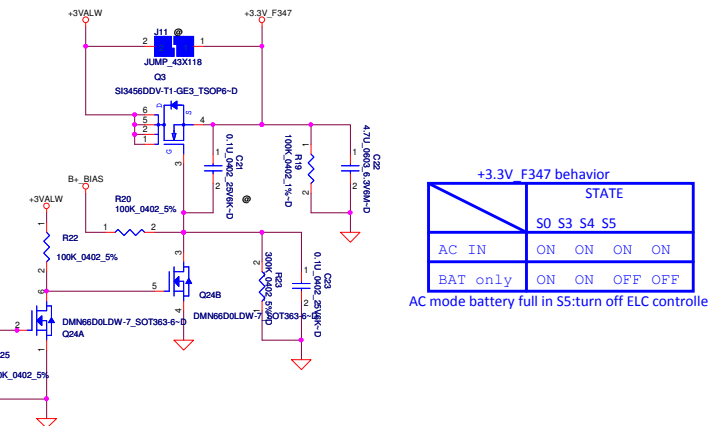


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			Date: Friday, December 14, 2012	Sheet 44 of 56



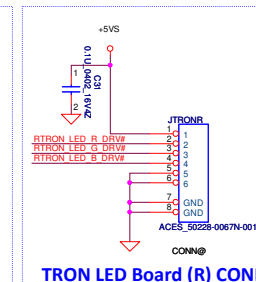
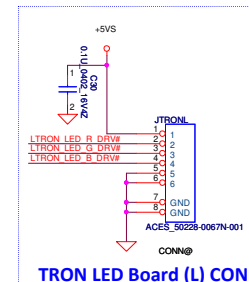
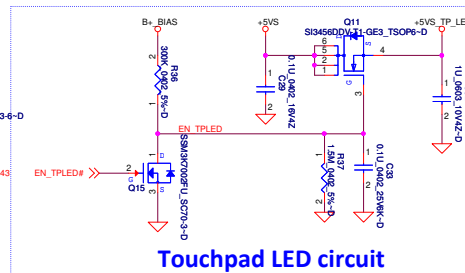
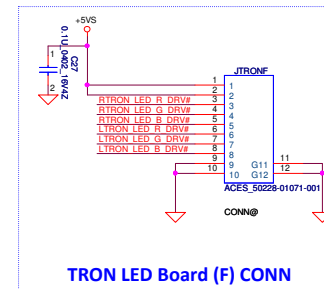
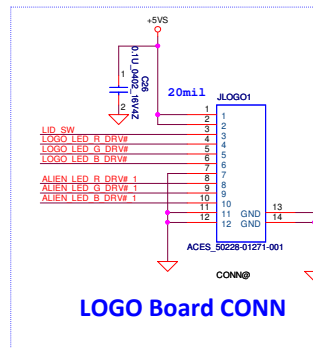
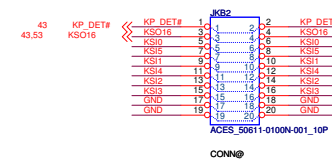
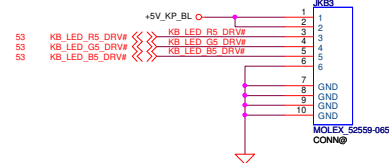
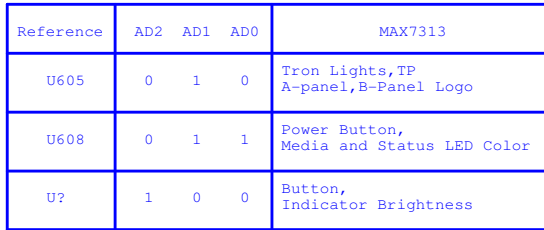


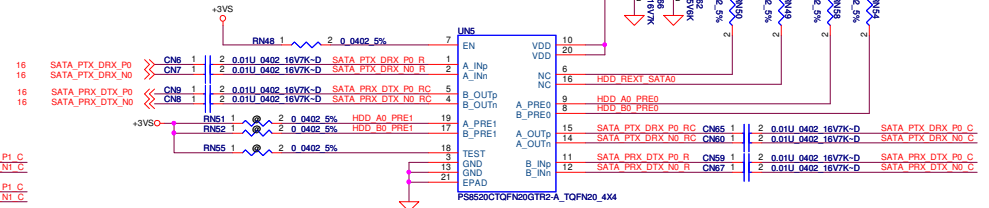
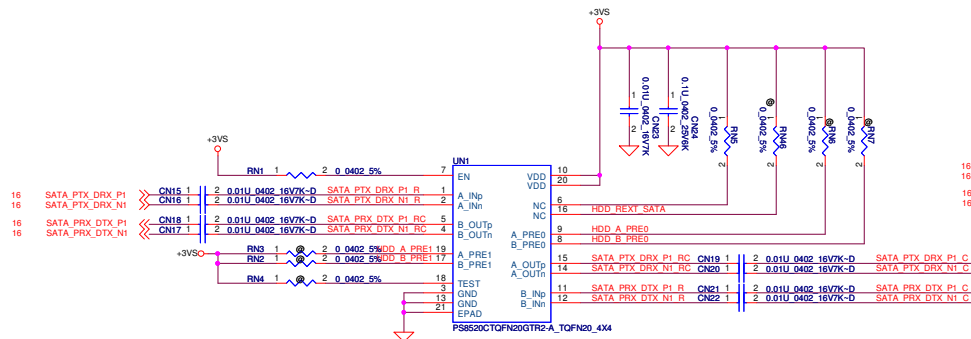
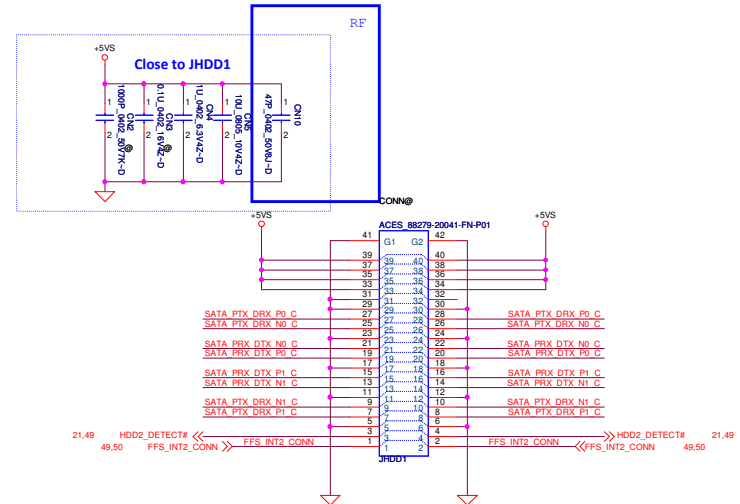
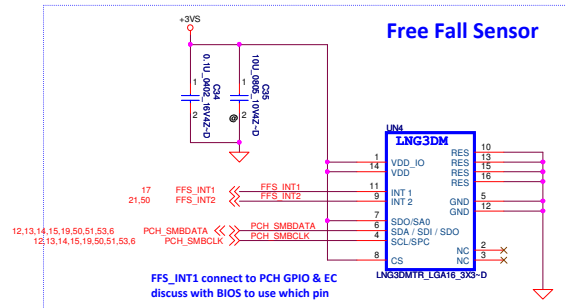
DEVICE	SMBUS ADDRESS
MAXIM - LED	0100 000b
MAXIM - GPIO	0100 001b
I2C EEPROM	1010 000b



+3.3V_F347 behavior	
	STATE
	S0 S3 S4 S5
AC IN	ON ON ON ON
BAT only	ON ON OFF OFF

AC mode battery full in S5 turn off ELC controller





Pin 20:
PARADE PS8250B:
Reserve RN12
PERICOM P13EQX6741ST:
Mount RN46, Reserve RN12
ASMEDIA ASM1466:
Mount RN46, Reserve RN12

Pin 9:
PARADE PS8250B:
Reserve RN11
PERICOM P13EQX6741ST:
Reserve RN11
ASMEDIA ASM1466:
Mount RN11 to pull down

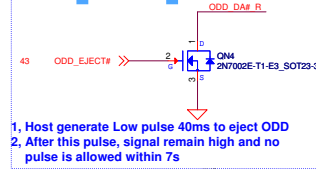
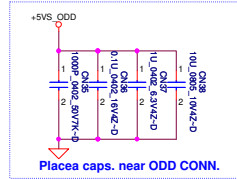
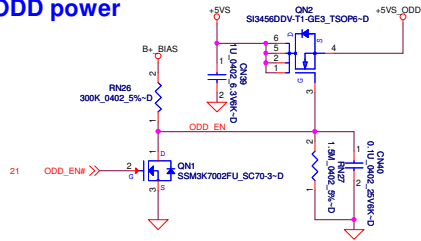
HDD_B_PRE0 RN8 1 2 0.0402 5%
HDD_B_PRE1 RN8 1 2 0.0402 5%
HDD_A_PRE1 RN10 1 2 0.0402 5%
HDD_A_PRE0 RN11 1 2 0.0402 5%
HDD_REXT SATA RN12 1 2 5.1K 0.402 1%

Pin 20:
PARADE PS8250B:
Reserve RN57
PERICOM P13EQX6741ST:
Mount RN49, Reserve RN57
ASMEDIA ASM1466:
Mount RN49, Reserve RN57

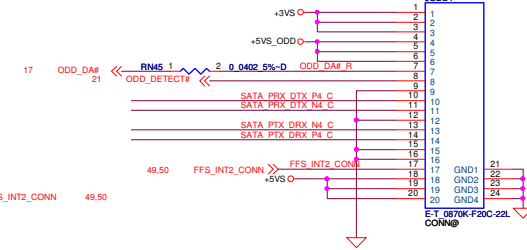
Pin 9:
PARADE PS8250B:
Reserve RN29
PERICOM P13EQX6741ST:
Reserve RN29
ASMEDIA ASM1466:
Mount RN29 to pull down

HDD_B_PRE0 RN3 1 2 0.0402 5%
HDD_B_PRE1 RN6 1 2 0.0402 5%
HDD_A_PRE1 RN7 1 2 0.0402 5%
HDD_A_PRE0 RN9 1 2 0.0402 5%
HDD_REXT SATA RN57 1 2 5.1K 0.402 1%

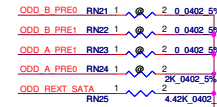
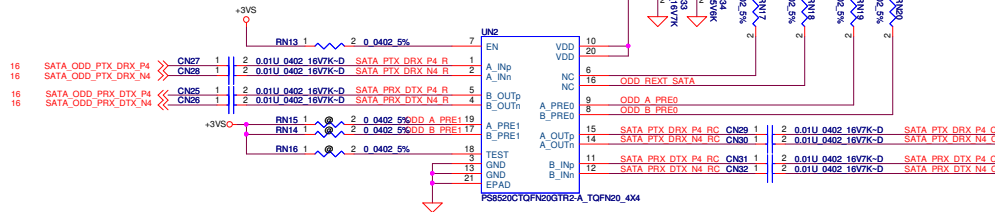
ODD power



SATA ODD Conn.



ODD Redriver



Pin 20:
PARADE PS8250B:
Reserve RN18, Mount RN25

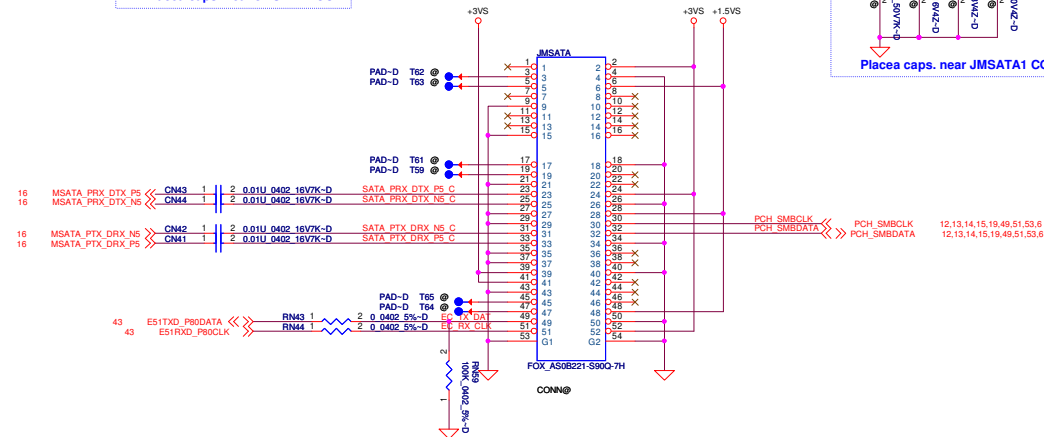
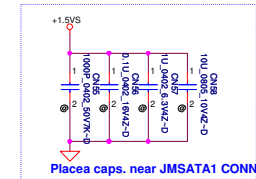
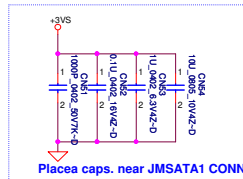
PERICOM PI3EQX6741ST:
Mount RN18, Reserve RN25

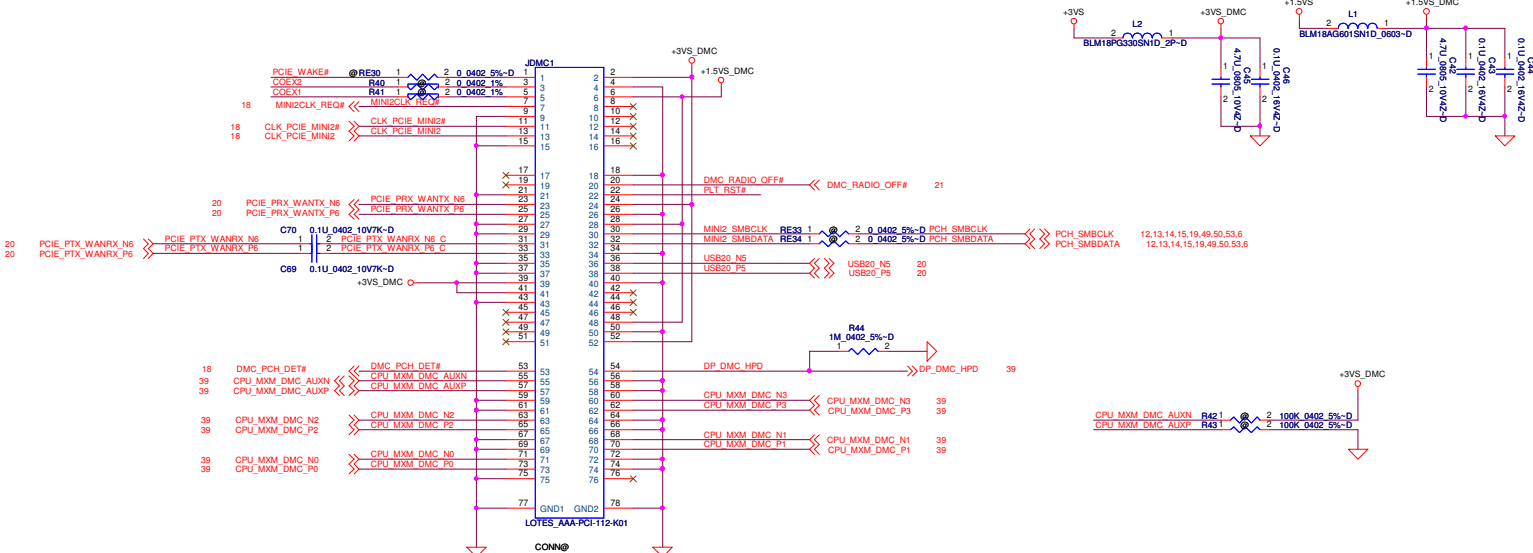
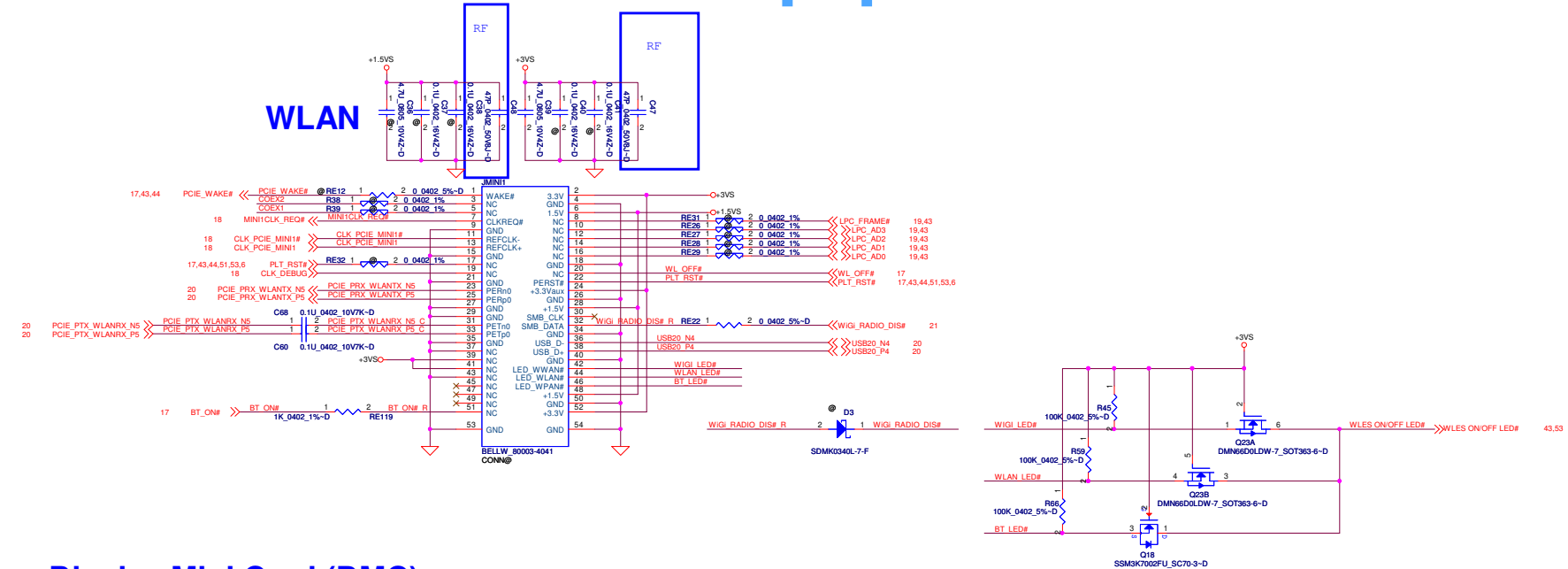
ASMEDIA ASM1466:
Mount RN18, Reserve RN25

Pin 9:
PARADE PS8250B:
Reserve RN24

PERICOM PI3EQX6741ST:
Reserve RN24

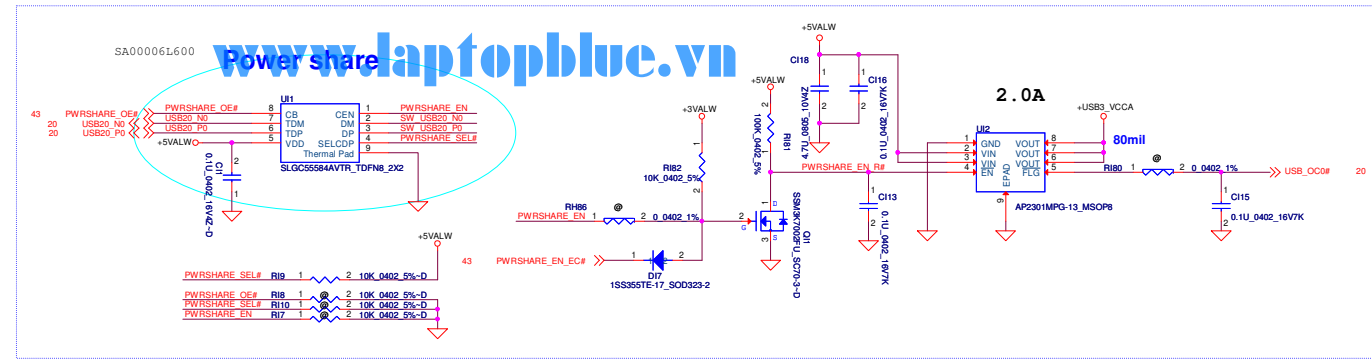
ASMEDIA ASM1466:
Mount RN24 to pull down





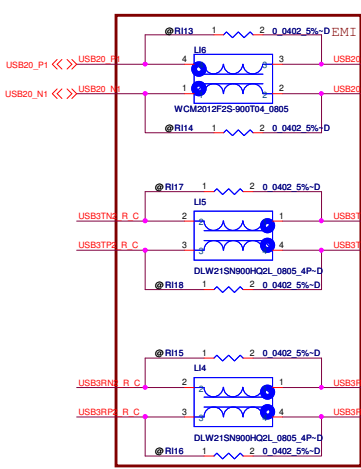
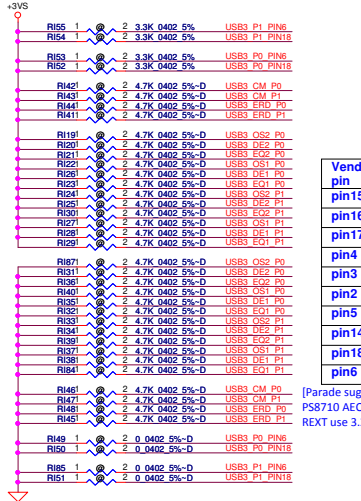
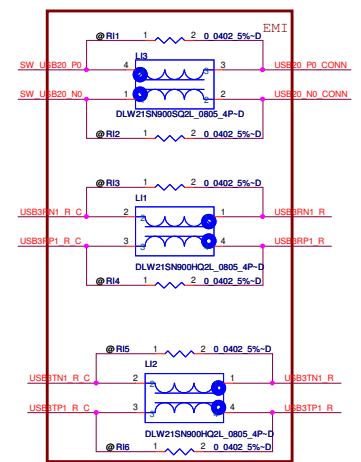
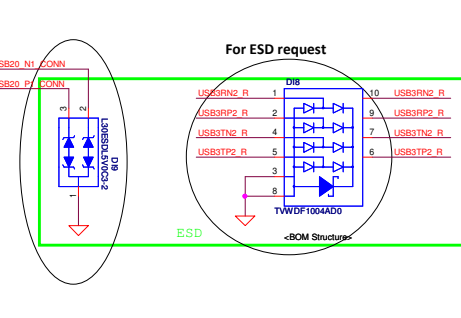
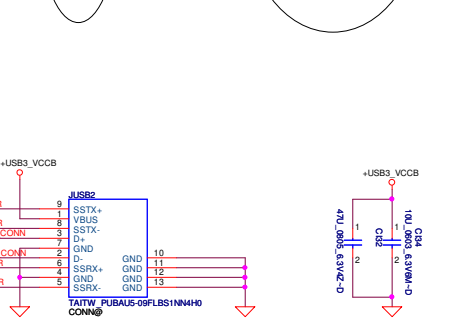
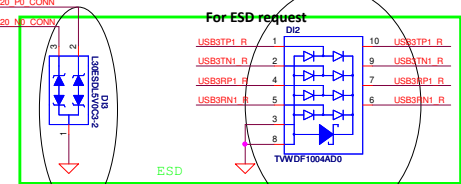
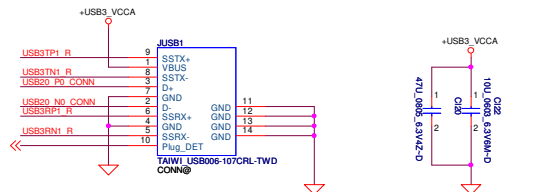
SA00006L600

Power share



2.0A

USB CONN

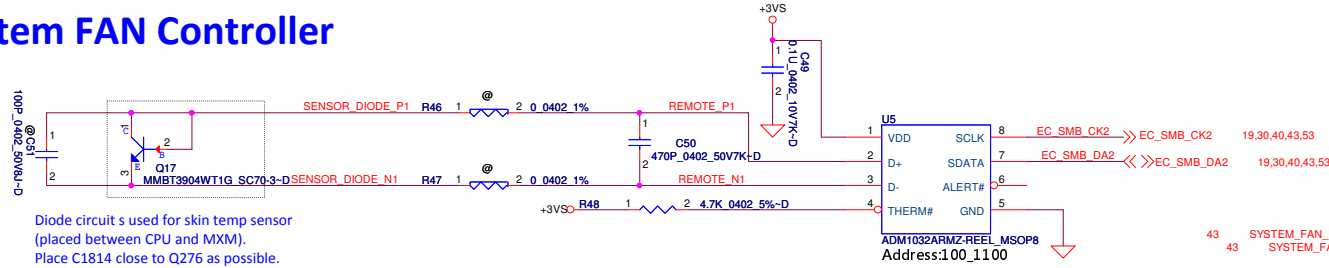


Vendor	PS8710B (default)	TI
pin15	AEQ1	OS2
pin16	ADE0	DE2
pin17	AEQ0	EQ2
pin4	BEQ1	OS1
pin3	BDE0	DE1
pin2	BEQ0	EQ1
pin5	PD	EN_RXD
pin14	TEST	CM
pin18	ADE1	
pin6	BDE1	

PS8710B
PCB footprint and CIS symbol use TI (SN65LVPE502CPRGER)
Compal P/N and value use Parade (PS8710B)

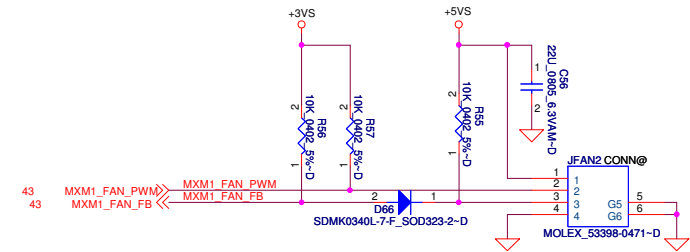
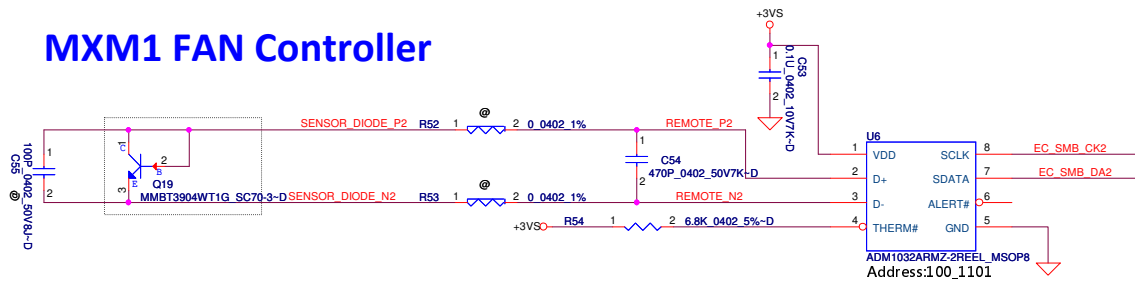
PS8710
[A(B)_DE1, A(B)_DE0] ==
LH: 3.5dB de-emphasis
LH: No de-emphasis
HL: 7dB de-emphasis
HH: 5dB with boost output swing
[A(B)_EQ1, A(B)_EQ0] ==
LL: reserved
LH: program EQ for channel loss up to 7dB
HL: program EQ for channel loss up to 14.5dB
HH: program EQ for channel loss up to 11.5dB
TEST ==
L: Normal operation (default)
H: Test mode enable

System FAN Controller

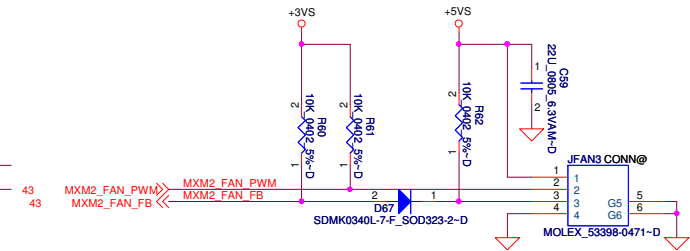
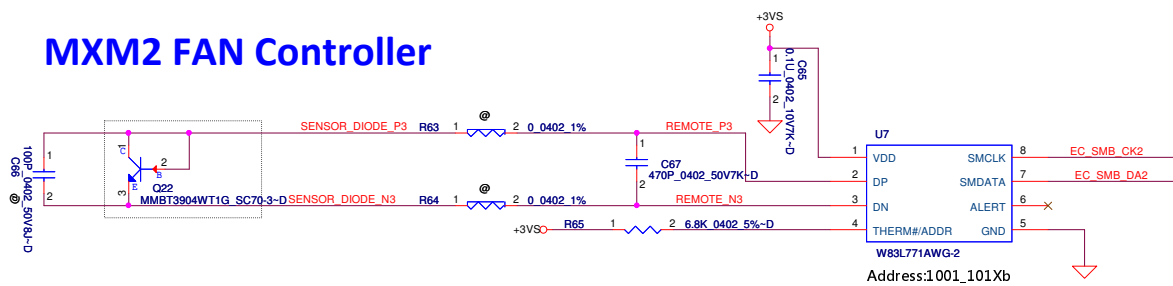


Pull up resistor on thermtrip pin	SMBUS address
4.7k	1111
6.8k	1011
10k	1001
15k	1101
22k	0011
33k	0111

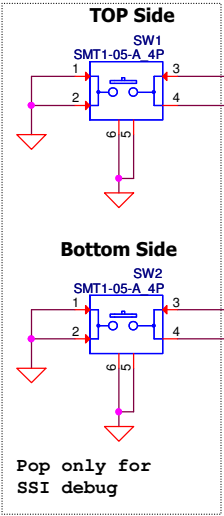
MXM1 FAN Controller



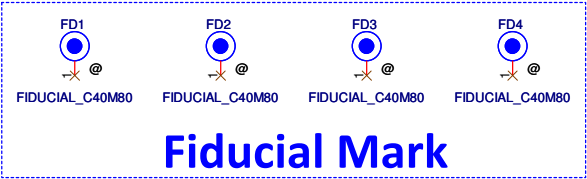
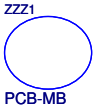
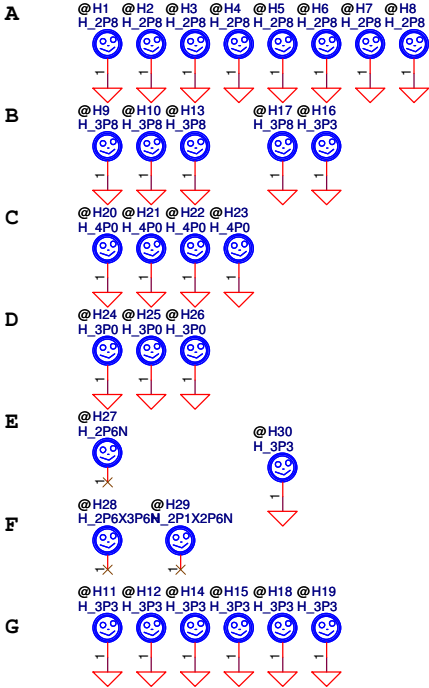
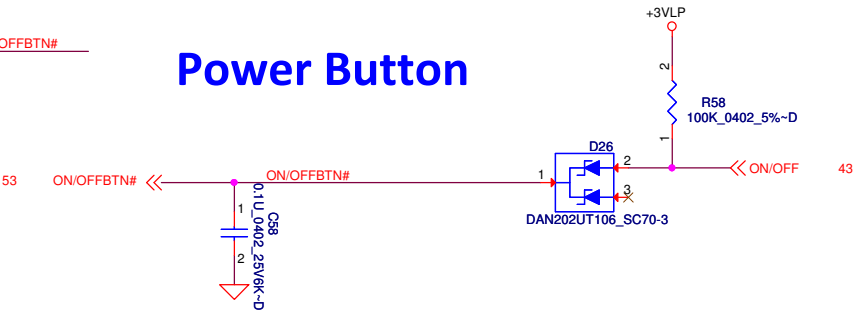
MXM2 FAN Controller



ON/OFF switch

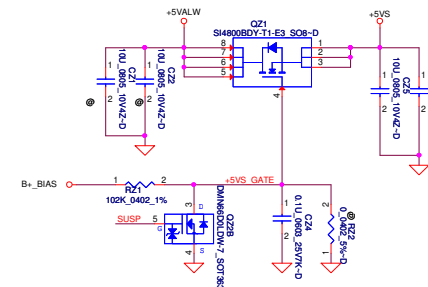


Power Button

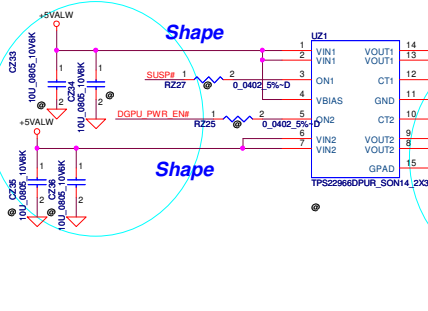


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				Document Number	0.1
				LA-9332P	
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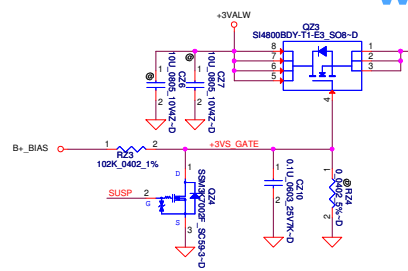
DC to DC +5VALW to +5VS



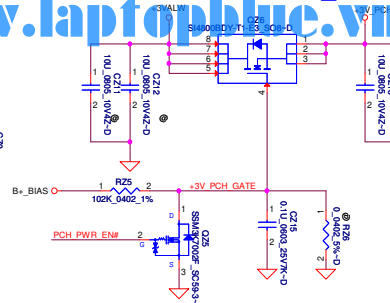
+5VALW to +5VS +3VALW to +3VS



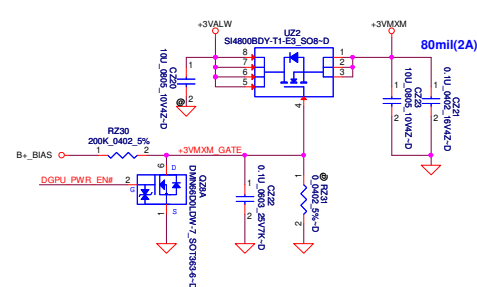
+3VALW to +3VS



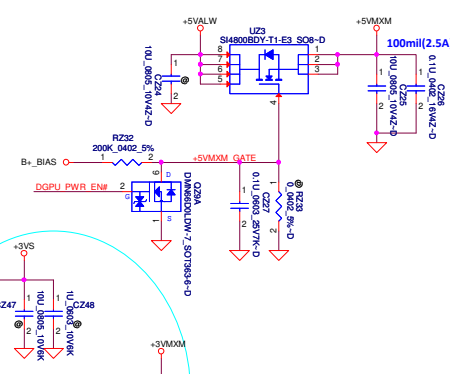
+3VALW to +3V_PCH



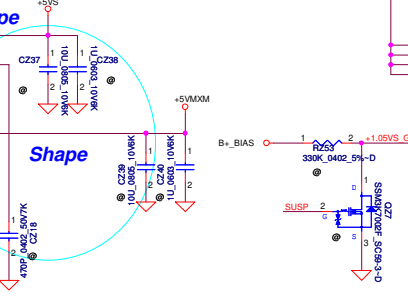
+3VALW to +3VMXM



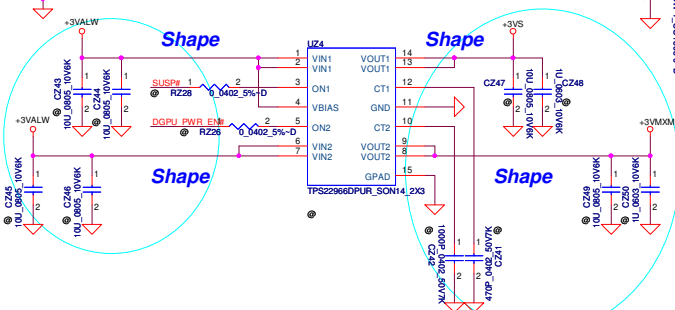
+5VALW to +5VMXM



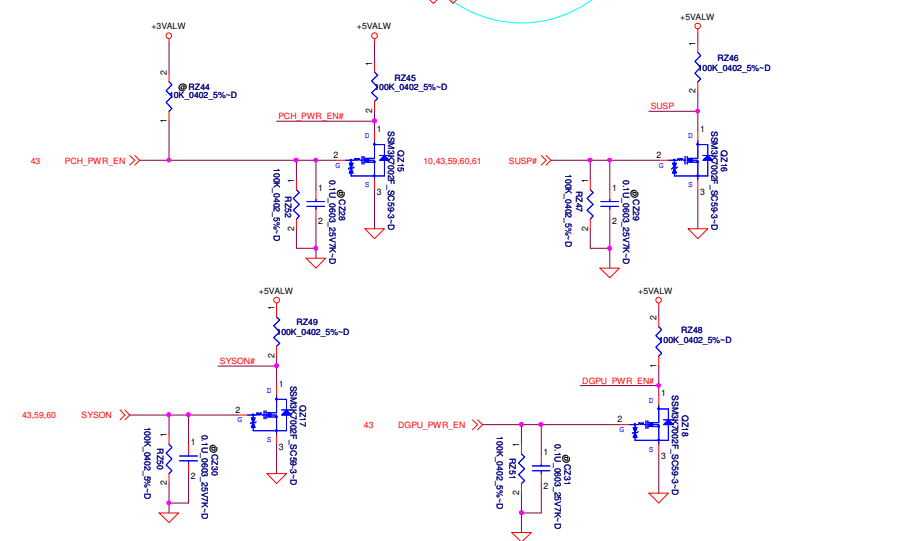
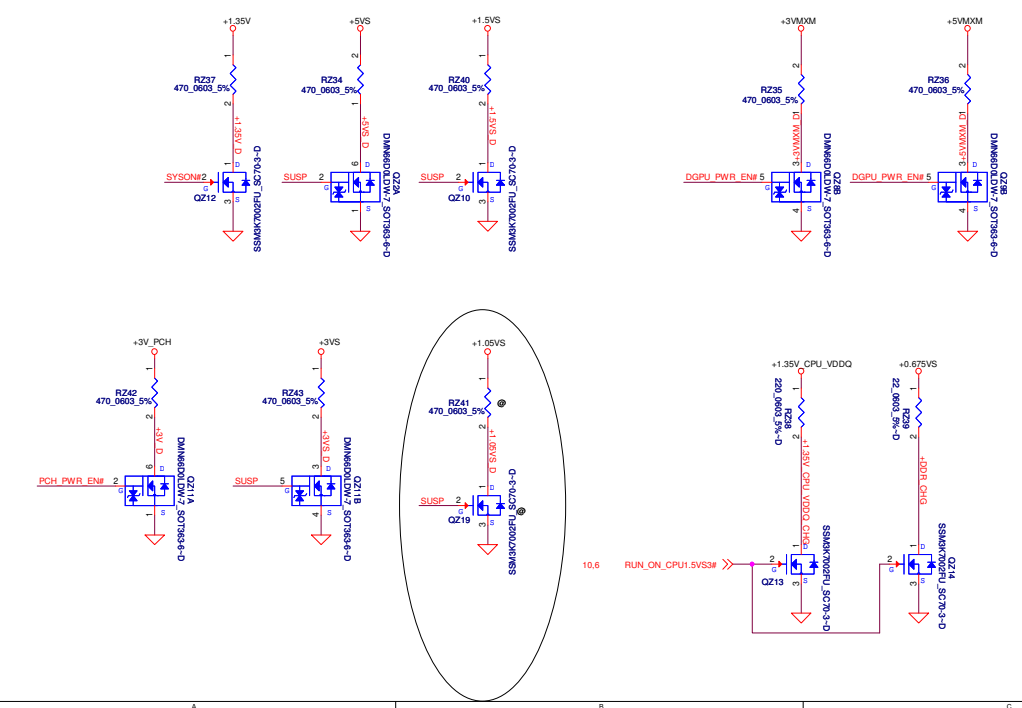
+1.05V to +1.05VS



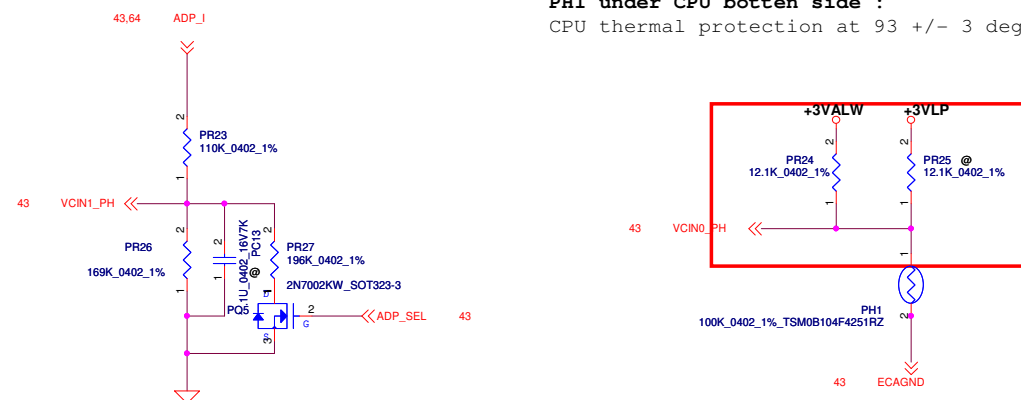
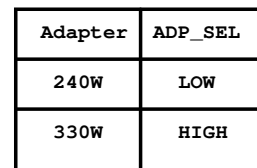
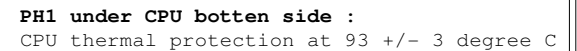
+5VALW to +5VMXM +3VALW to +3VMXM



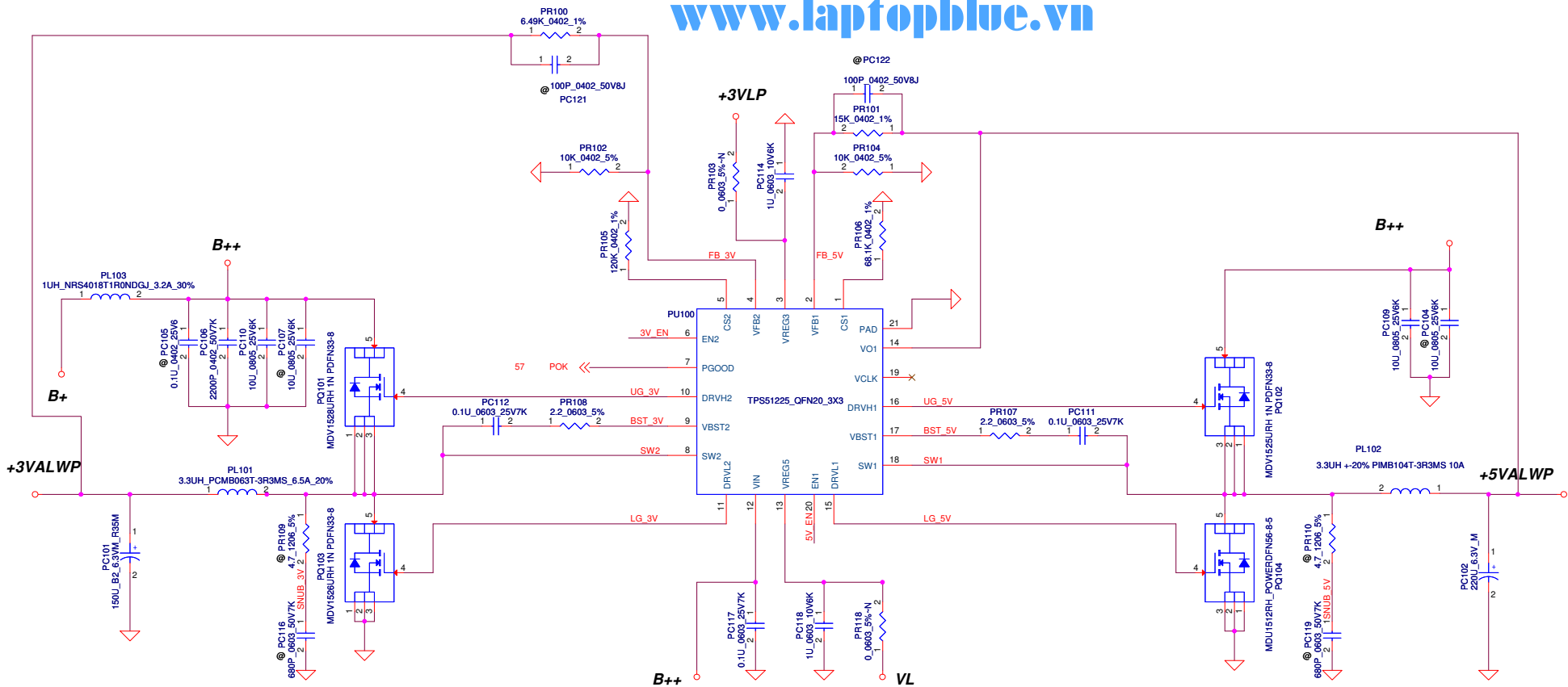
Discharge Circuit



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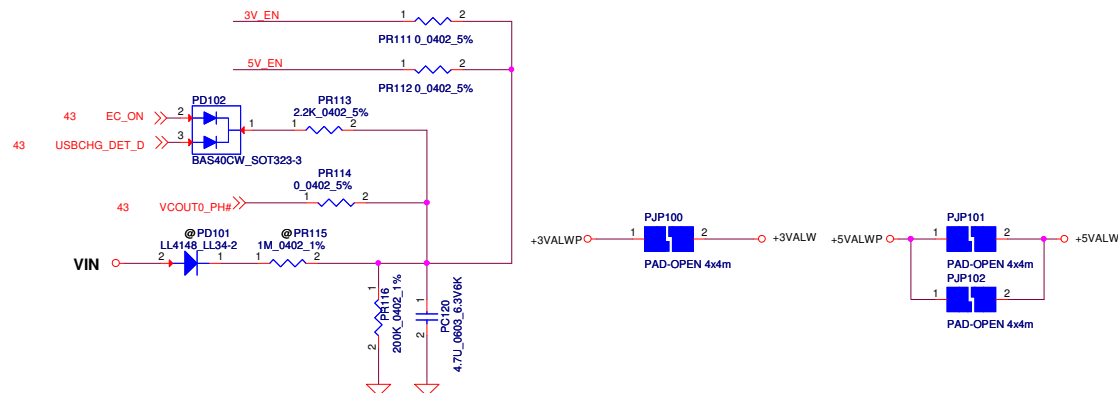


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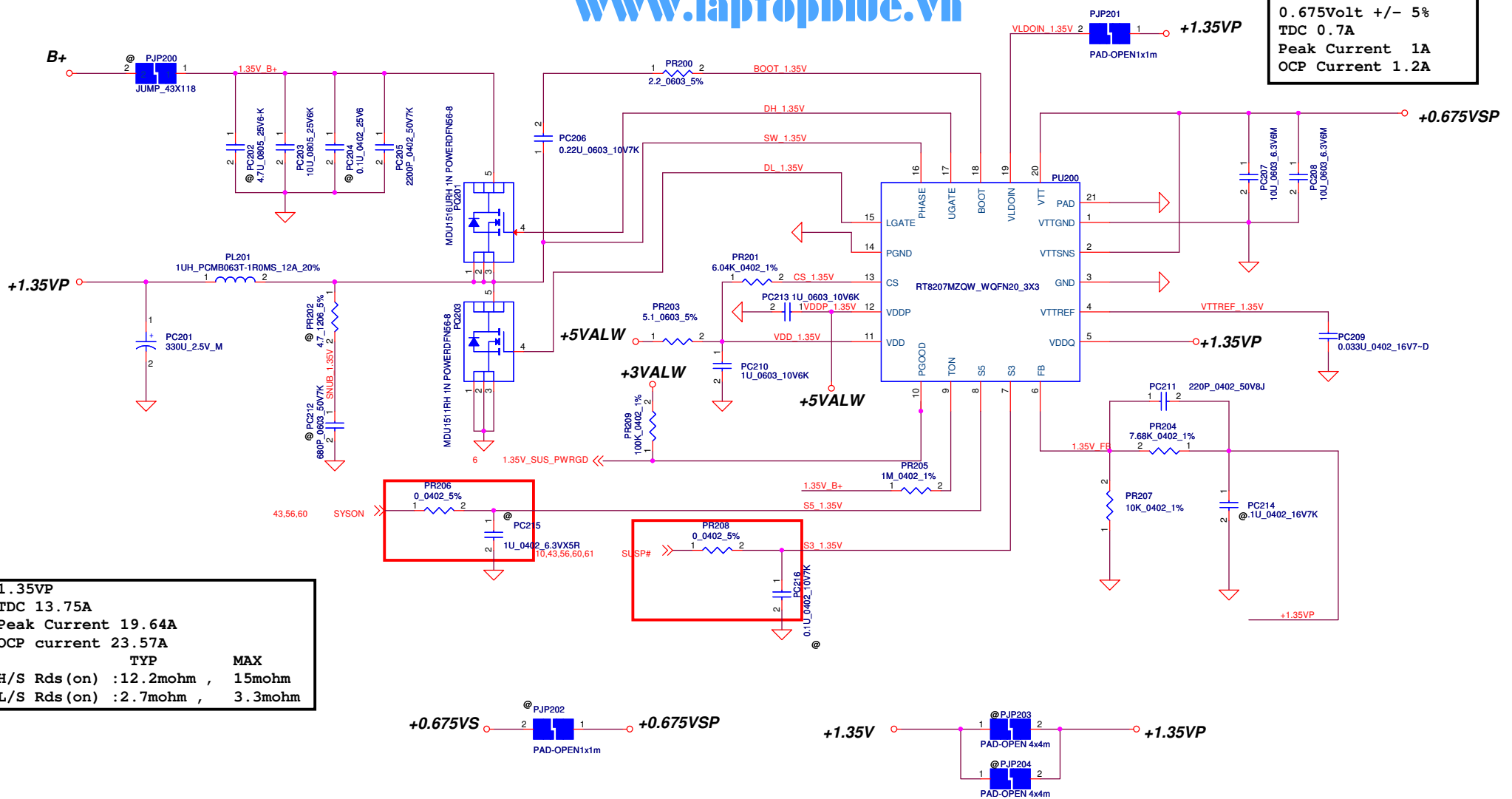
3VALWP
TDC 6.08A
Peak Current 8.11A
OCP current 9.73A

	TYP	MAX
H/S Rds (on)	11.2mohm	14mohm
L/S Rds (on)	3.7mohm	5mohm

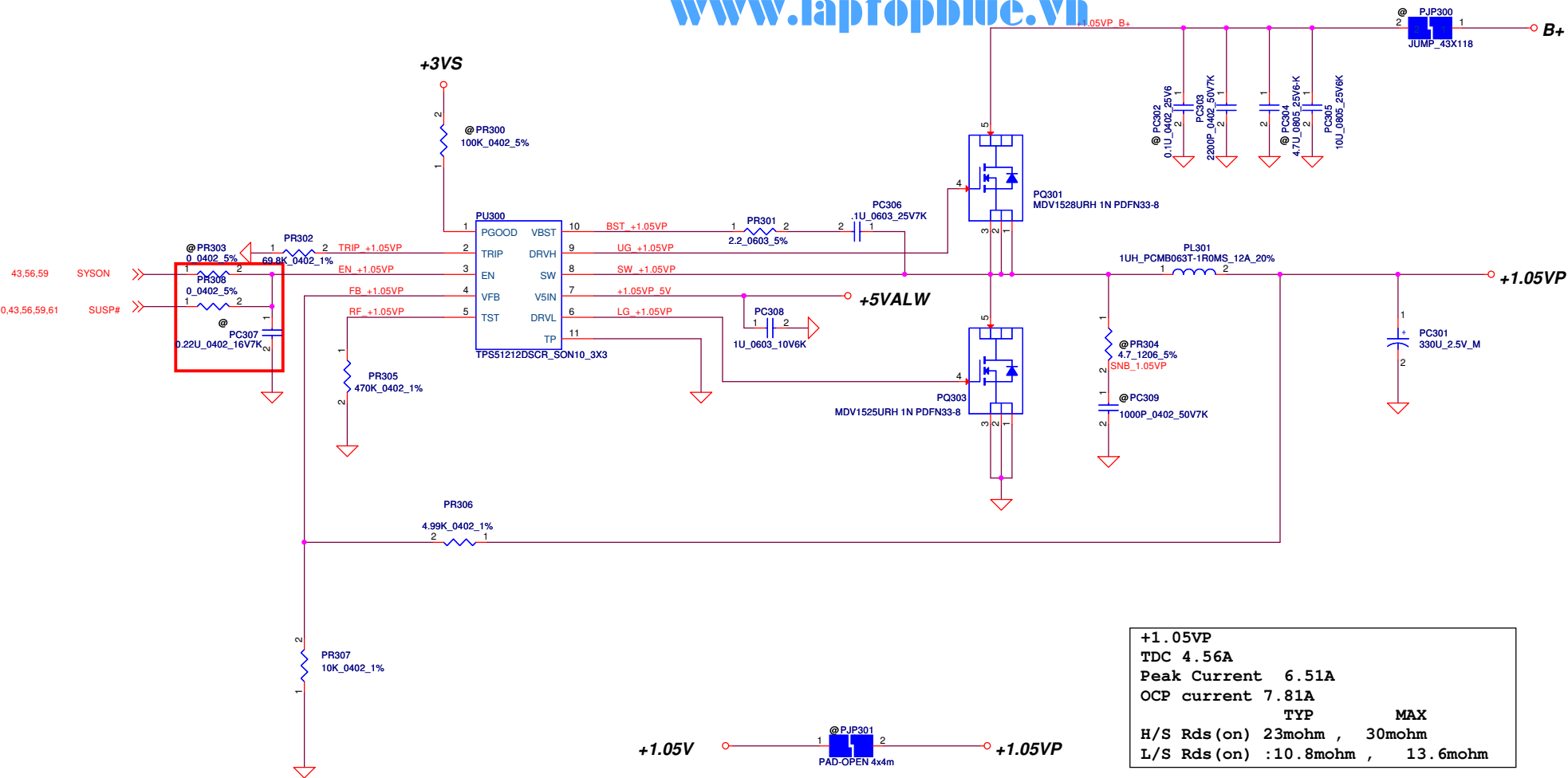


5VALWP
TDC 11A
Peak Current 16A
OCP current 20A

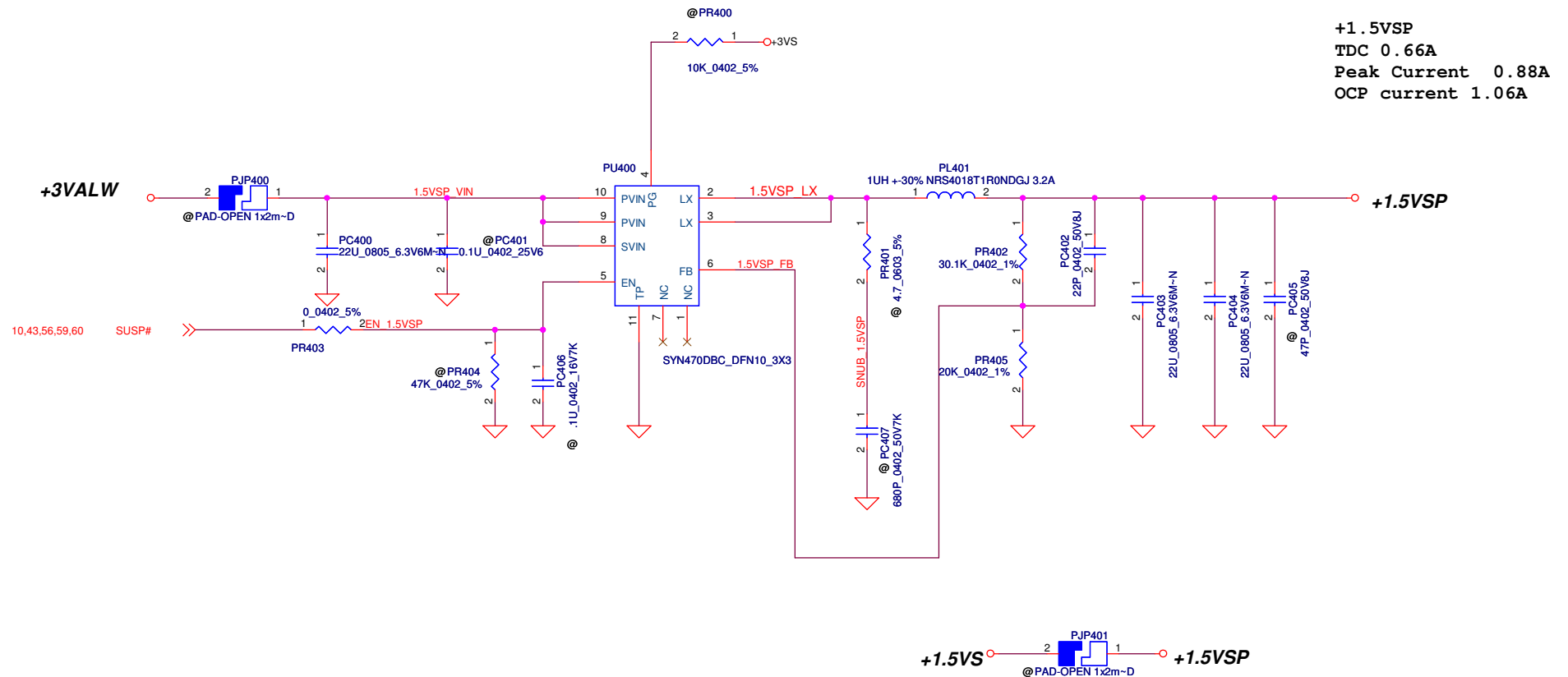
	TYP	MAX
H/S Rds (on)	11.2mohm	14mohm
L/S Rds (on)	3.7mohm	5mohm

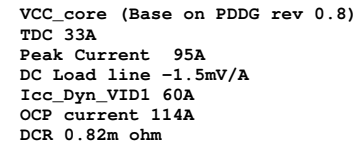


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				Size	Document Number
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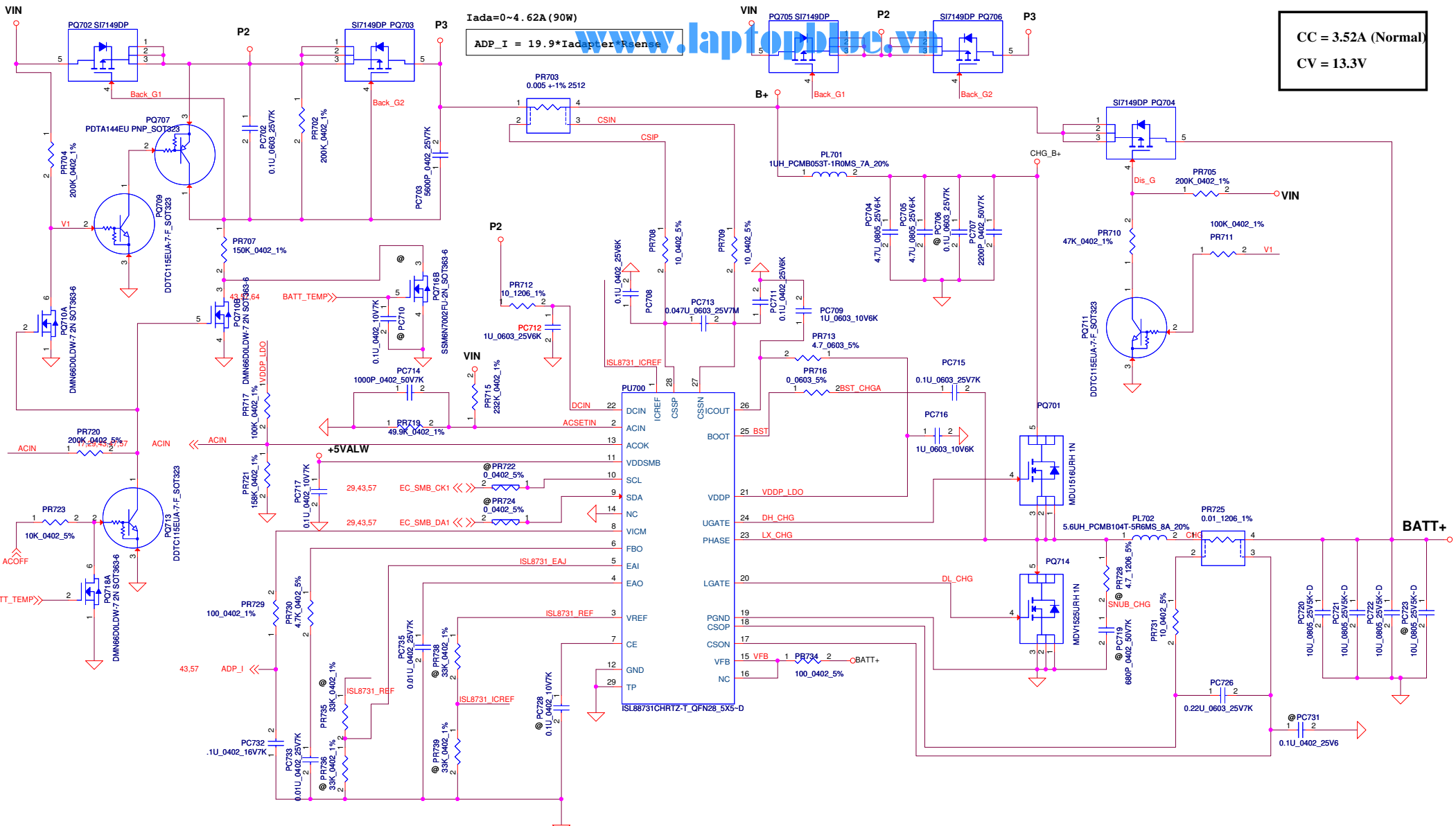


Compal Electronics, Inc.

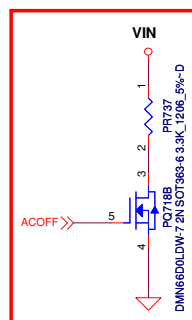
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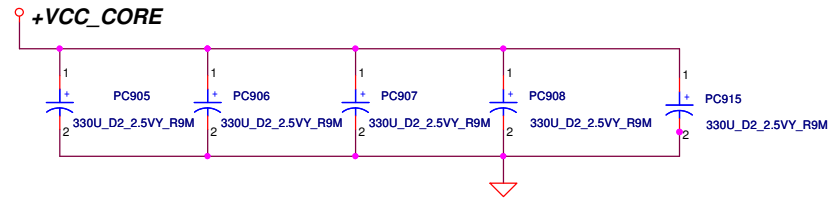
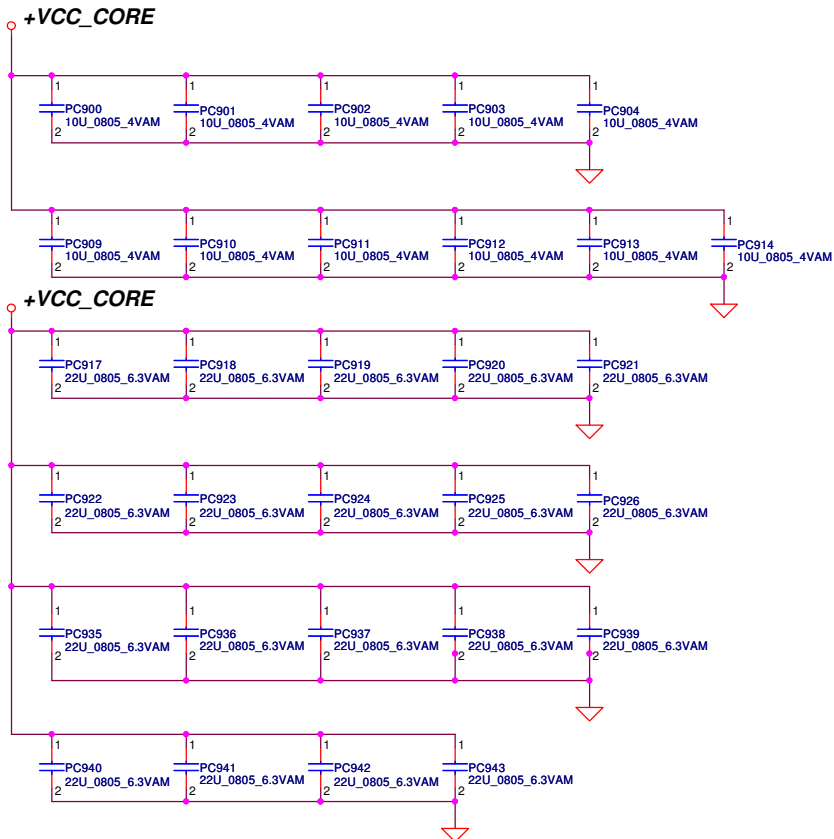
For DT Mode



Iada=0~4.62A (90W)
ADP_I = 19.9*Iadaptee*Reense

CC = 3.52A (Normal)
CV = 13.3V

Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2012/05/28				Title			
Deciphered Date				2013/05/27				PWR-Charger			
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Issued Date	2012/05/28	Deciphered Date	2013/05/27	Title	PWR PROCESSOR DECOUPLING
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Item	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Adjust 1.5V output volatge		P61	change PR402 to 30.1K_0402_1% PR405 to 20K_0402_1%	2012.7.30	SSI
2	Adjust 3.3V OCP seeting		P58	change PR105 to 120K_0402_1%.	2012.7.30	SSI
3	Adjust 3V/5V always OTP seeting		P58	modify PD100 to PR114 0_0402_1%.	2012.7.30	SSI
4	Adjust Vcore OTP seeting		P62	PR531 connect to +5VS	2012.7.30	SSI
5	Add PD3 PD4 for EMD requirement		P57	add PD3 PD4 to PESD24VS2UT_SOT23-3	2012.8.16	SSI
6	hiccup mode issue is not happen so we haven't need solution.		P57	remove Erp lot6 Circuit	2012.8.16	SSI
7	change diode for EMI requirement		P57	use PD2 (6 PIN) to combine combine PD3(2PIN) PD4(2PIN).	2012.8.31	SSI
8	adjust the component for the 88731 schematic		P64	change PR722 and PR724 to short footprint remove PR701 PR706 PC701 PC734 PR732	2012.9.10	SSI
9	adjust RTC circuit for safety concern		P57	add PR2 1K_0402_5%	2012.9.10	SSI
10	change ACIN bead for current limit rating		P57	change PL1 PL4 to C8B BPH 853025_2P	2012.9.10	SSI
11	add PR116 for 3v 5v_EN delay time solution		P58	add PR116 402K_0402_1%	2012.9.18	SSI
12	change output choke to improve efficiency		P59	change PL201 to 1UH_PCMC063T-1R0MN	2012.9.18	SSI
13	change PR500 value to meet INTEL SPEC.		P62	change PR500 to 130_0402_1%-D	2012.10.4	SSI
			P67			
14						
15						
16						
17						

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