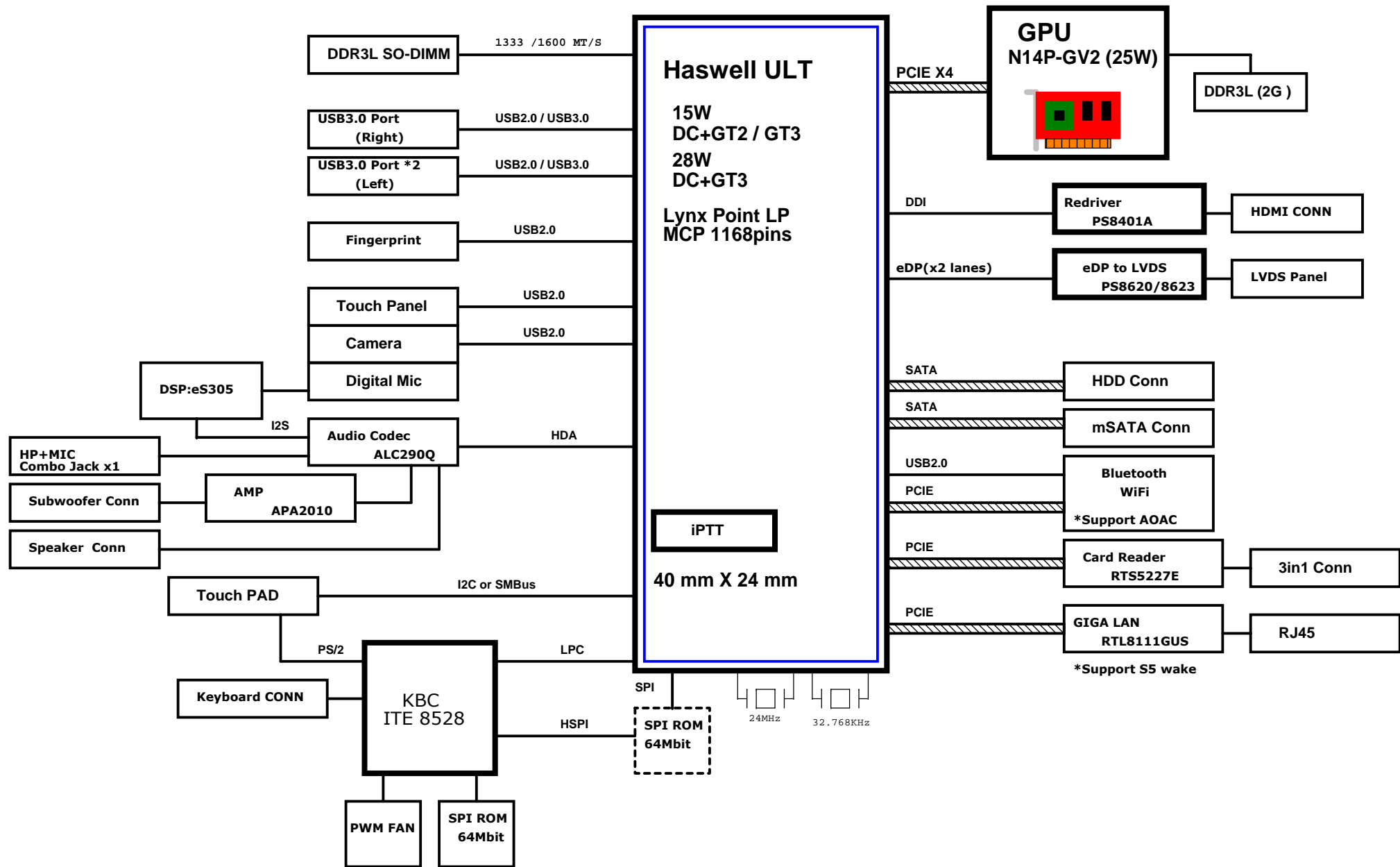


JW8B/C BLOCK DIAGRAM



HSIO Port	USB3.0	PCIE	SATA
1	USB3.0_1 CN6		
2	USB3.0_2 CN4		
3	USB3.0_3 CN5	PCIE1 X	
4	USB3.0_4 X	PCIE2 Card Reader	
5		PCIE3 GIGA LAN	
6		PCIE4 WIFI	
7		PCIE5 GPU 4X	
8		PCIE5 GPU 4X	
9		PCIE5 GPU 4X	
10		PCIE5 GPU 4X	
11		PCIE6 X	SATA3 X
12		PCIE6 X	SATA2 mSATA
13		PCIE6 X	SATA1 HDD
14		PCIE6 X	SATA0 X

PCIE CLK
CLK0 X
CLK1 Card Reader
CLK2 GIGA LAN
CLK3 WIFI
CLK4 GPU 4X
CLK5 X

USB2.0
USB2.0_0 CN4
USB2.0_1 CN6
USB2.0_2 CN5
USB2.0_3 Finger Print
USB2.0_4 Camera
USB2.0_5 eTP
USB2.0_6 Blue Tooth
USB2.0_7 Touch Screen



Quanta Computer Inc.

PROJECT : JW8B

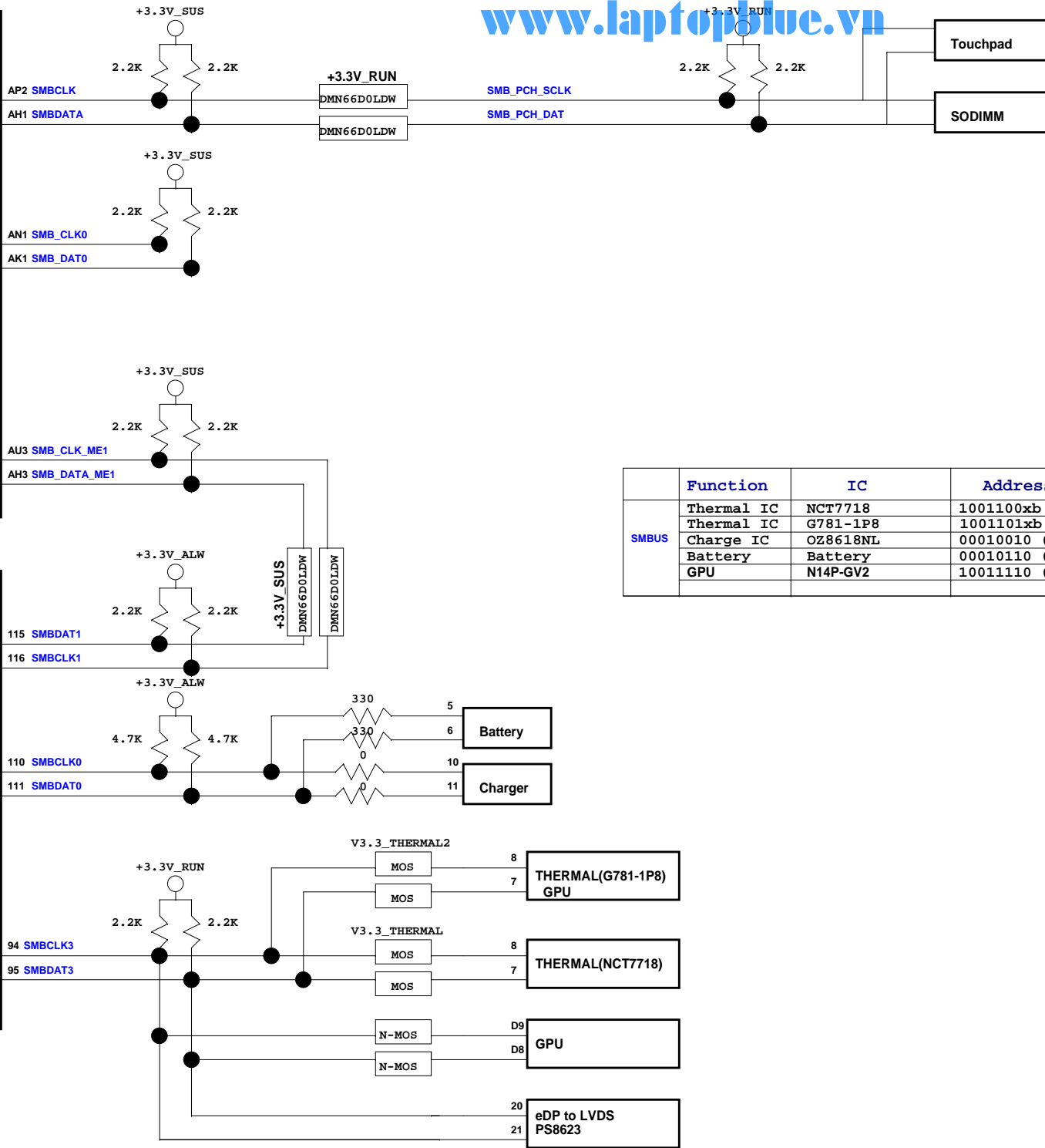
Size	Document Number	Rev A
PORT ASSIGNMENT		
Date: Wednesday, June 19, 2013	Sheet 2 of 57	

MB

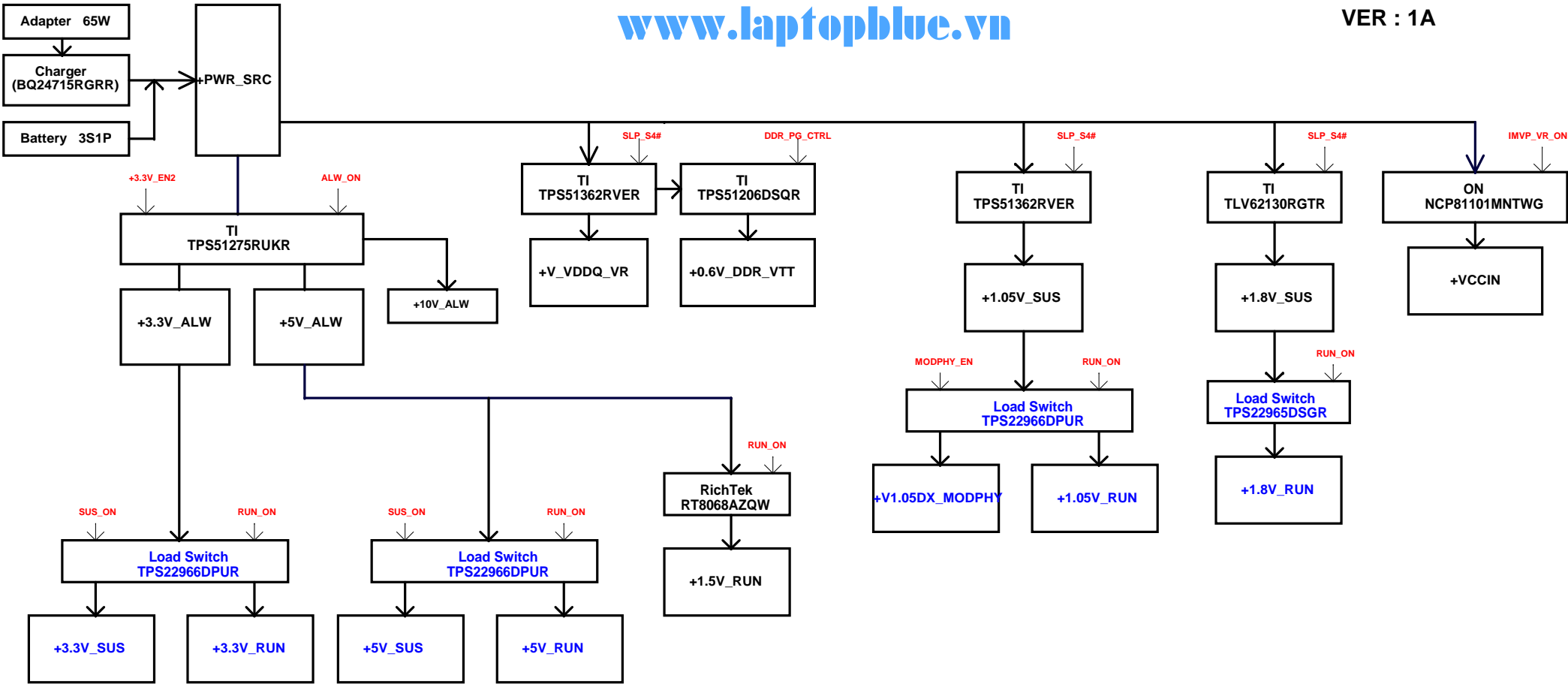
Haswell ULT

MB

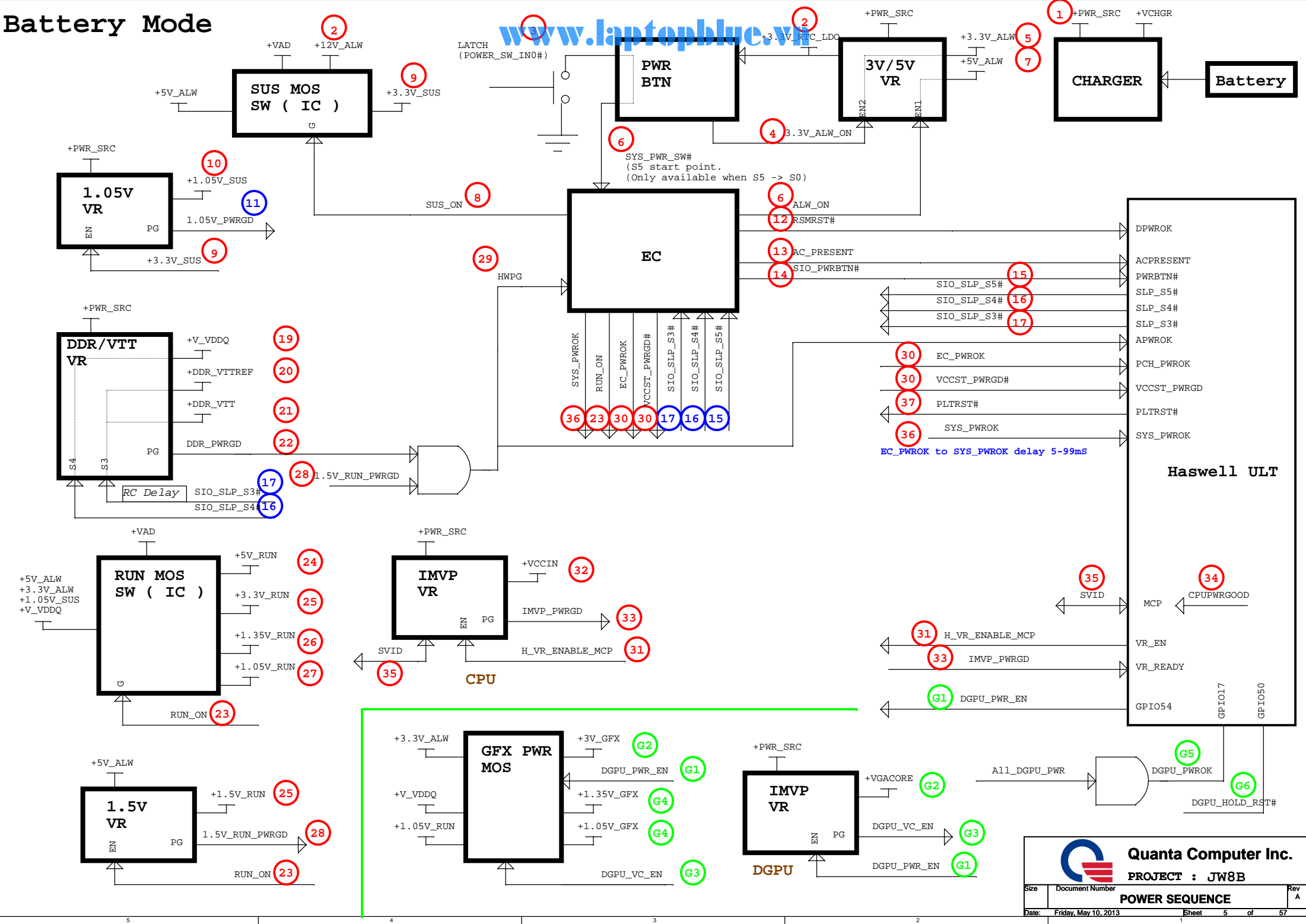
SIO
ITE8528E



	Function	IC	Address
SMBUS	Thermal IC	NCT7718	1001100xb (98h)
	Thermal IC	G781-1P8	1001101xb (9Ah)
	Charge IC	OZ8618NL	00010010 (0x12h)
	Battery	Battery	00010110 (0X16h)
	GPU	N14P-GV2	10011110 (0X9Eh)



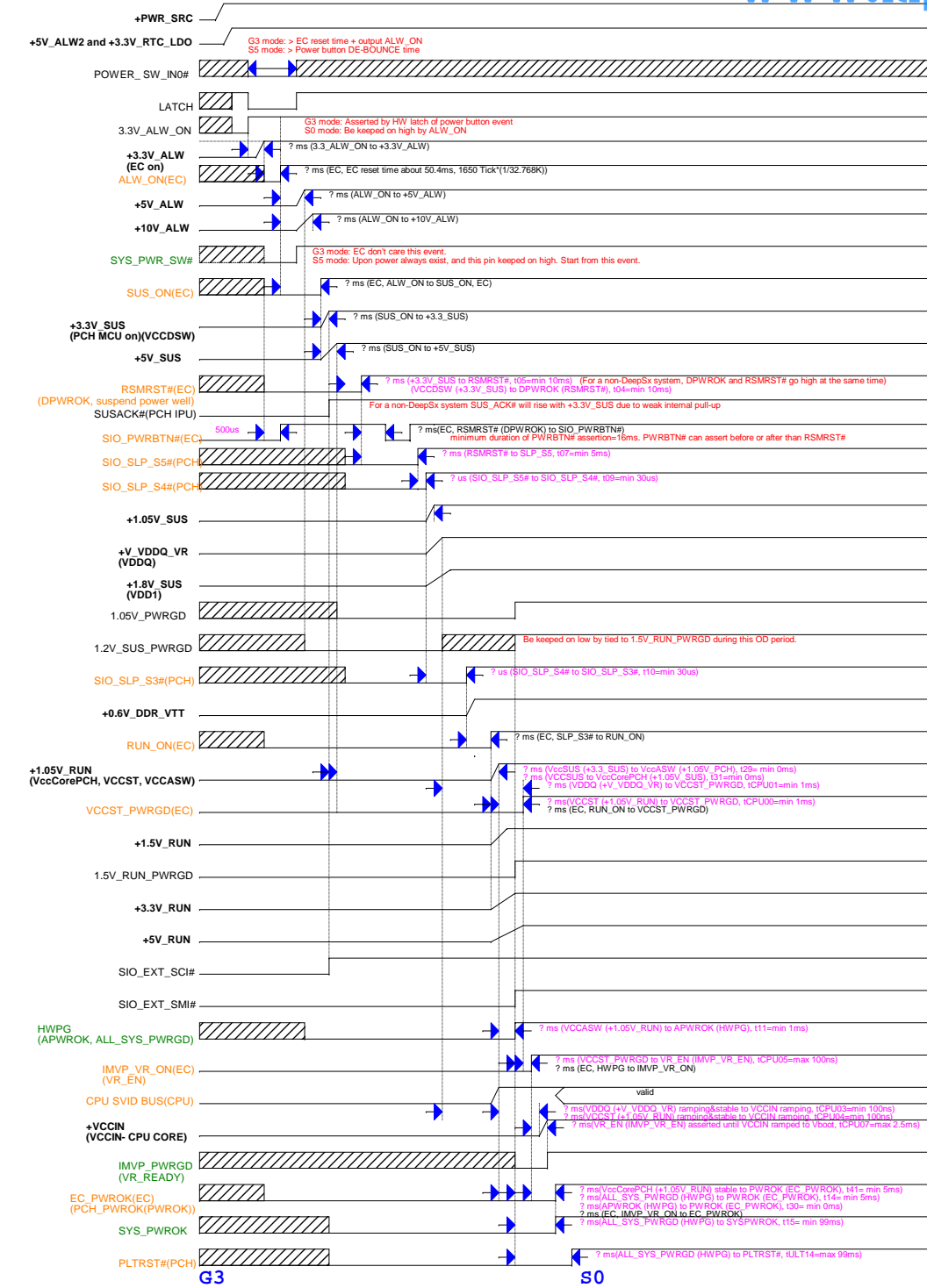
Battery Mode

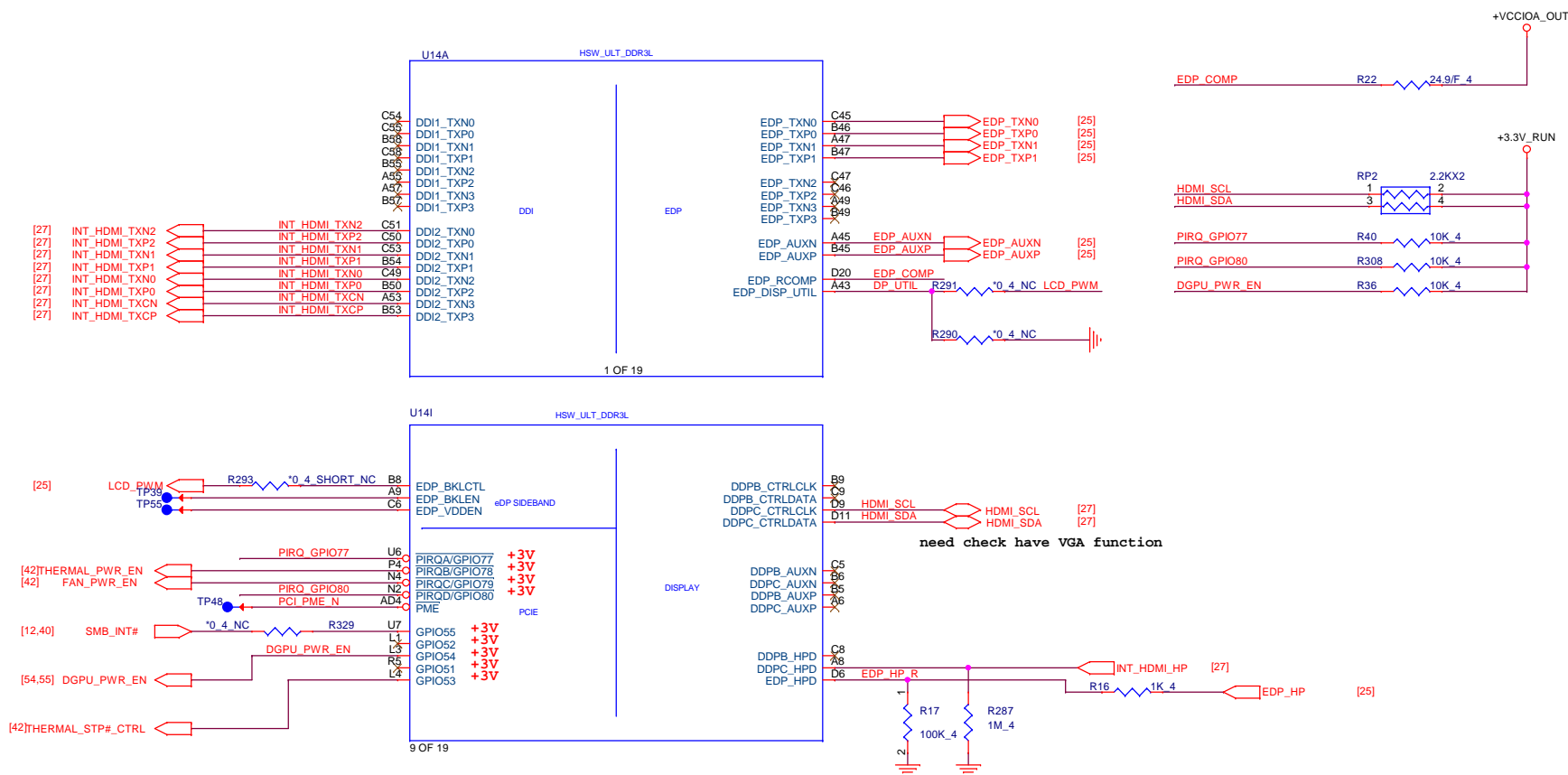


Power Sequence
(G3 to S0)

Shark Bay ULT PSS, 490828, Rev1.1

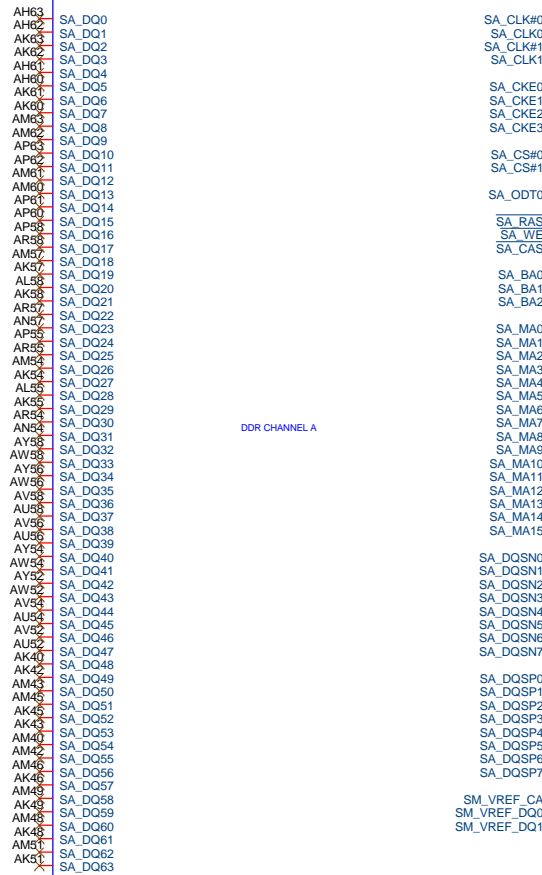
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U14C

HSW_ULT_DDR3L

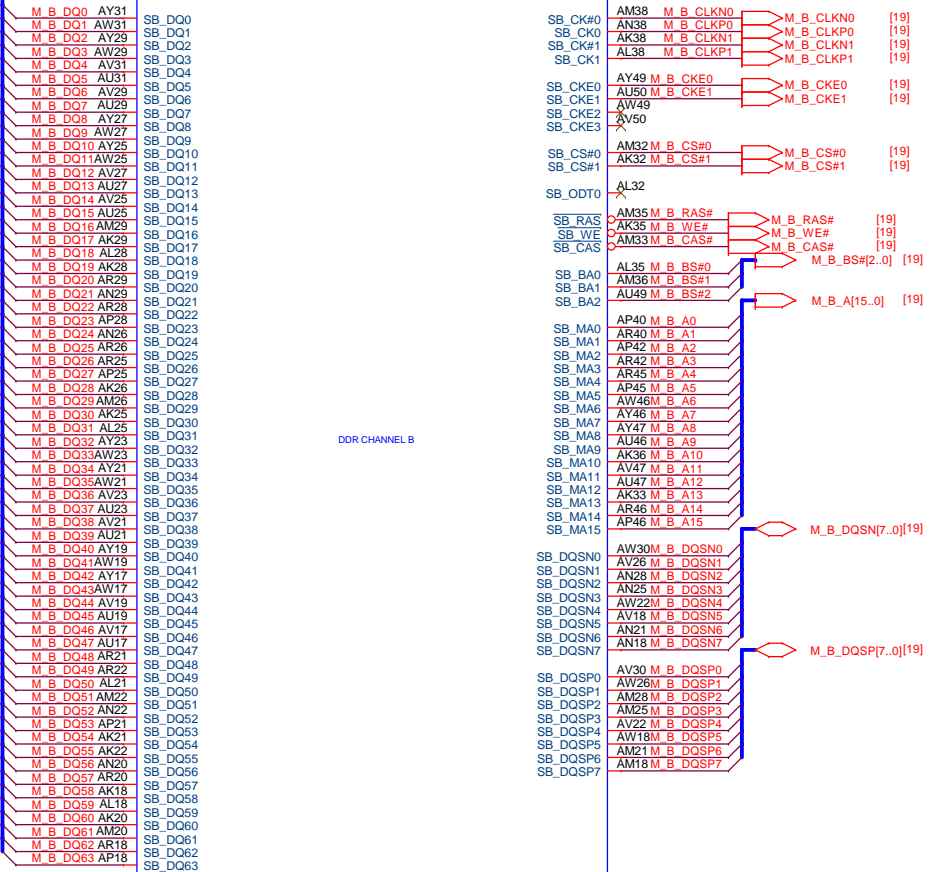


3 OF 19

[19] M_B_DQ[63..0]

U14D

HSW_ULT_DDR3L



4 OF 19

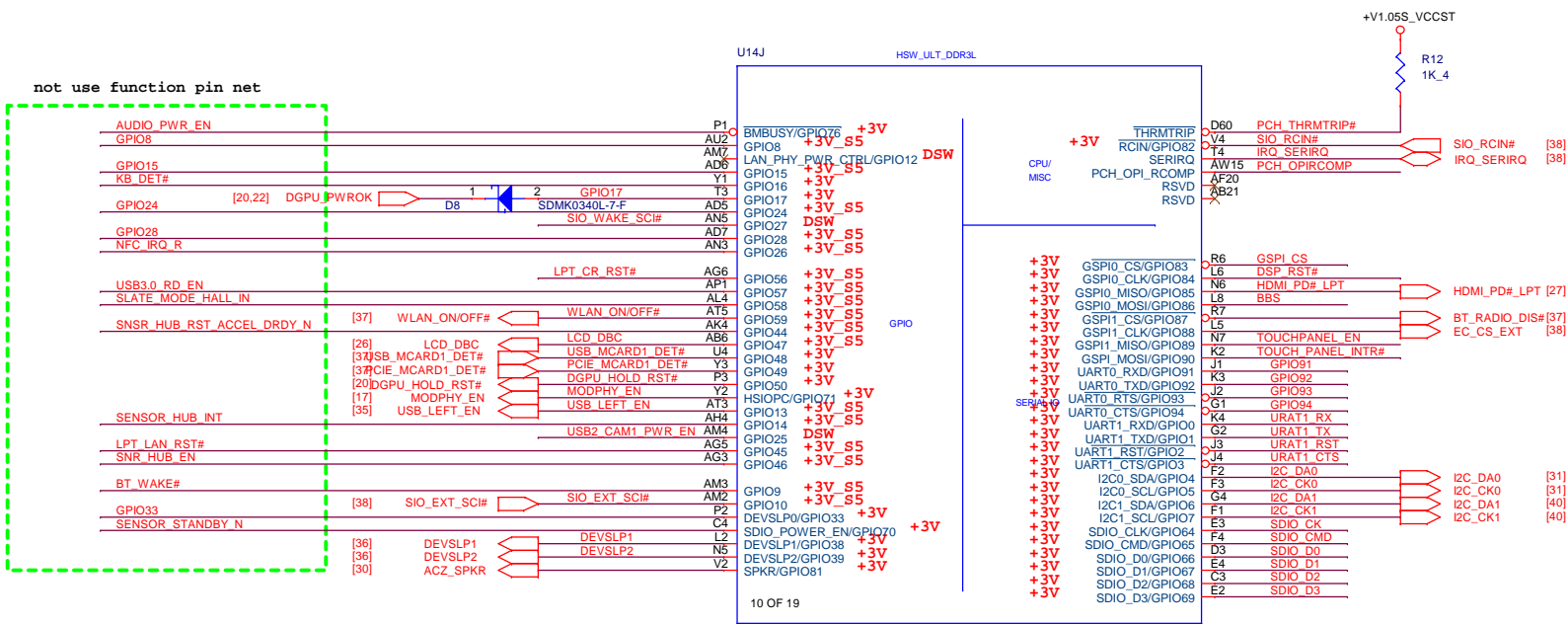
Check if not used. NC ?
12/25 Del SM_VREF_DQ0



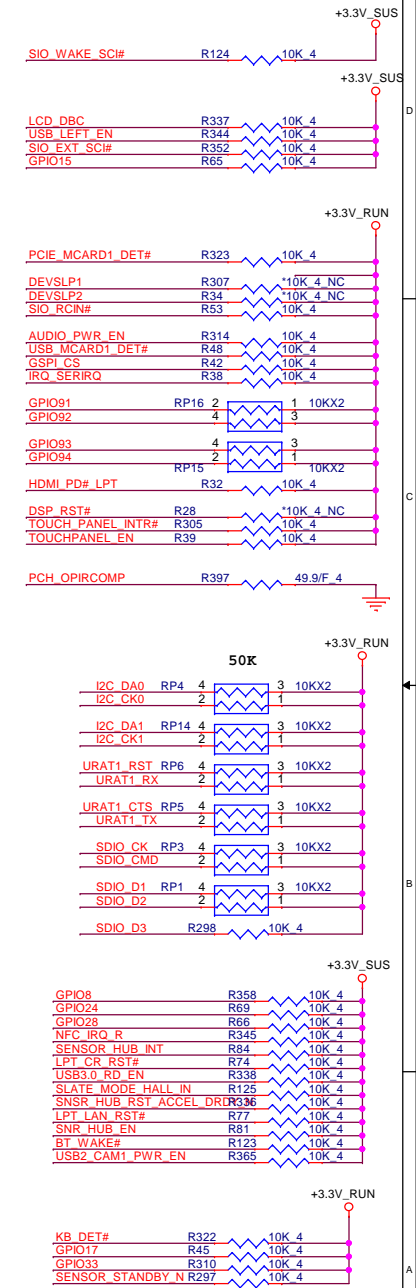
Quanta Computer Inc.
PROJECT : JW8B

Size	Document Number	Rev
	Haswell ULT 2/12	A
Date:	Friday, May 10, 2013	Sheet 8 of 57

Hasswell ULT (GPIO, LPIO, MISC)



GPIO Pull-up/Pull-down (CLG)

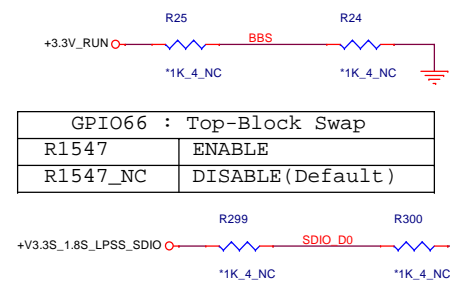


No Reboot Strap(GPIO81)	
NC	Default
PU	EN

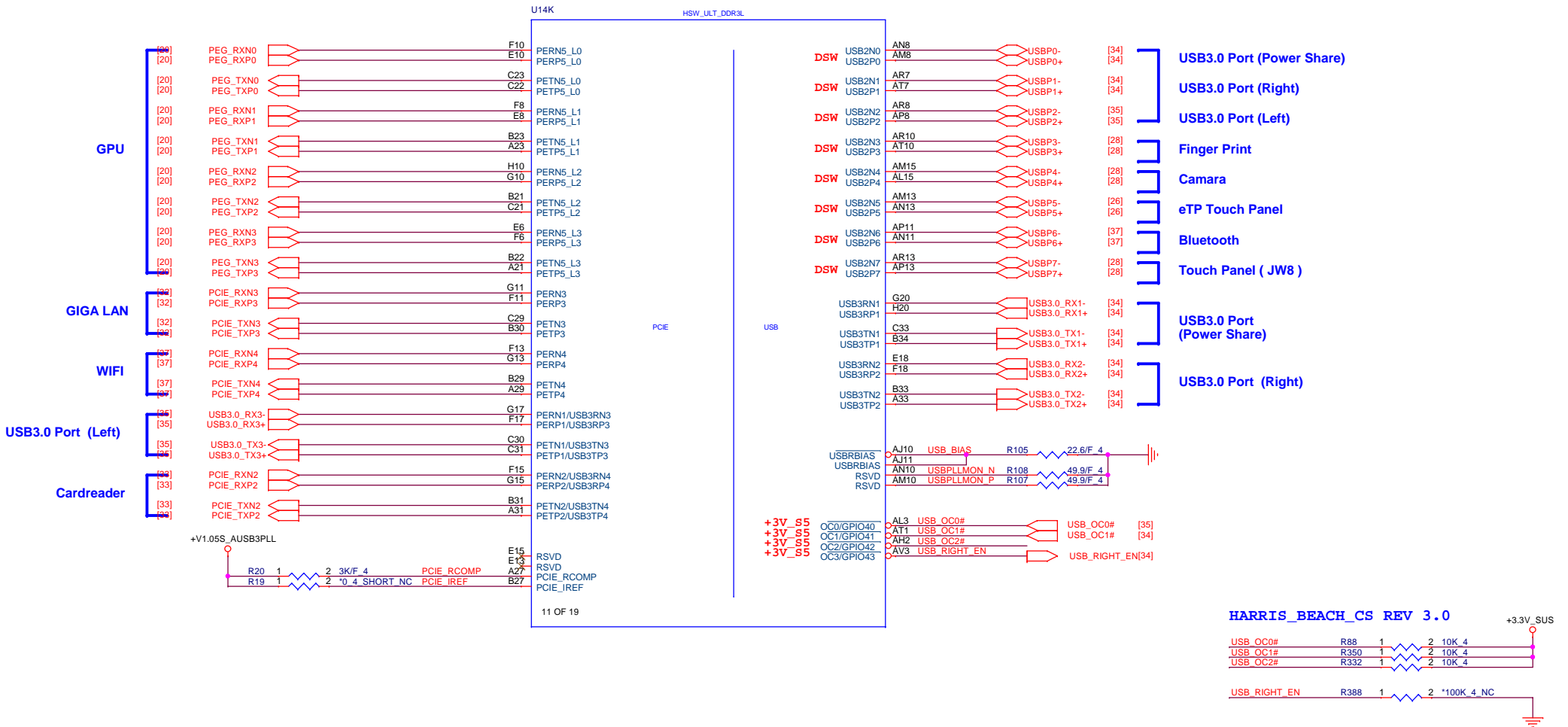
GPIO86:Boot BIOS Strap Bit	
PU	LPC
PD	SPI (Default IPD)

TLS CONFIDENTIALITY STRAP(GPIO15)	
NC	Default
PU	EN

GPIO66 : Top-Block Swap	
R1547	ENABLE
R1547_NC	DISABLE(Default)

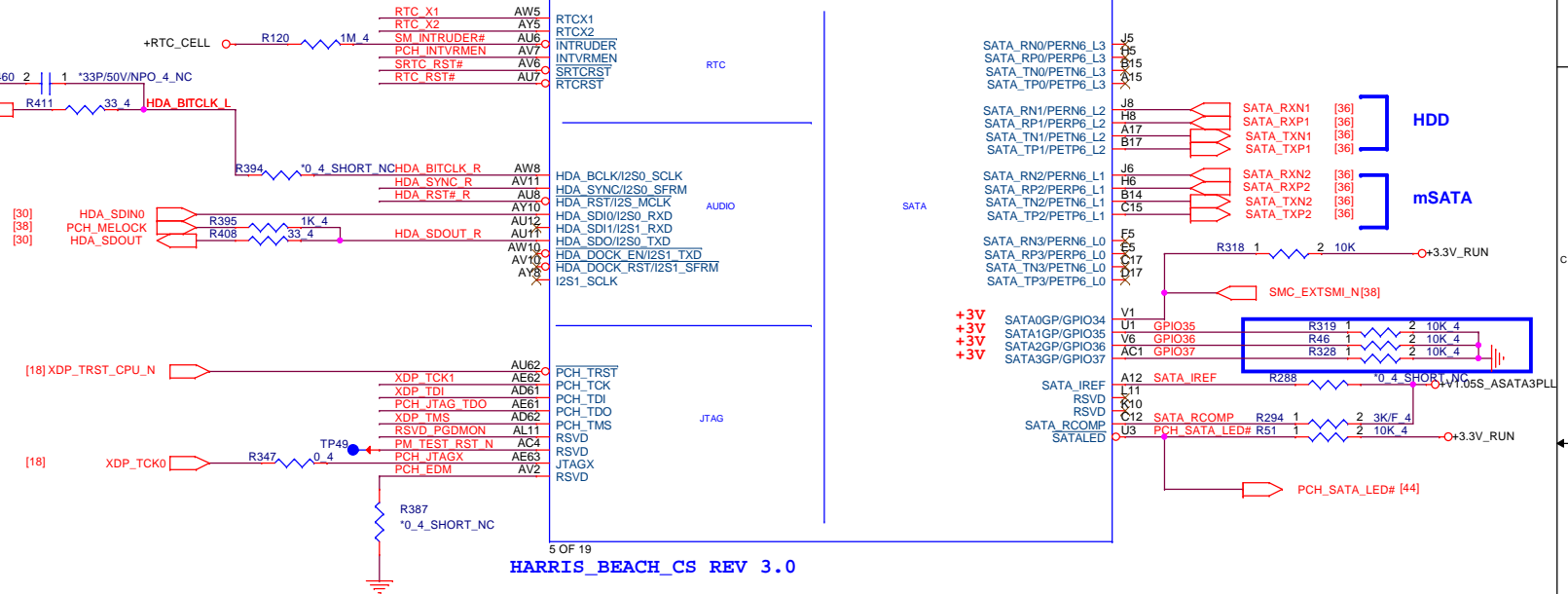


Haswell ULT (PCIE,USB)




Quanta Computer Inc.

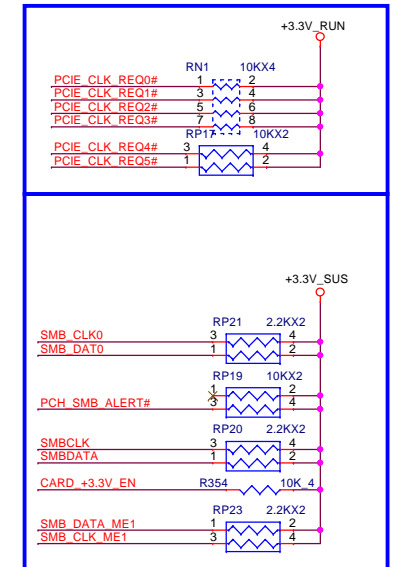
PROJECT : JW8B



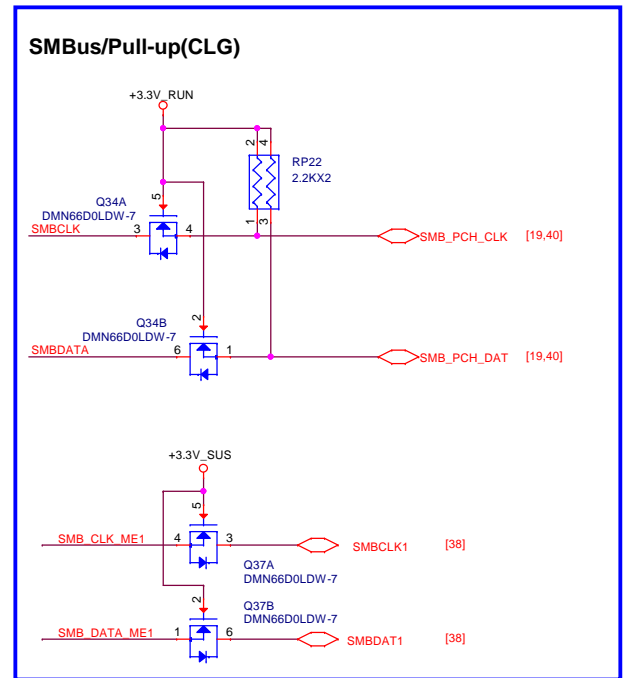
HARRIS_BEACH_CS REV 3.0

PCH Strap Table

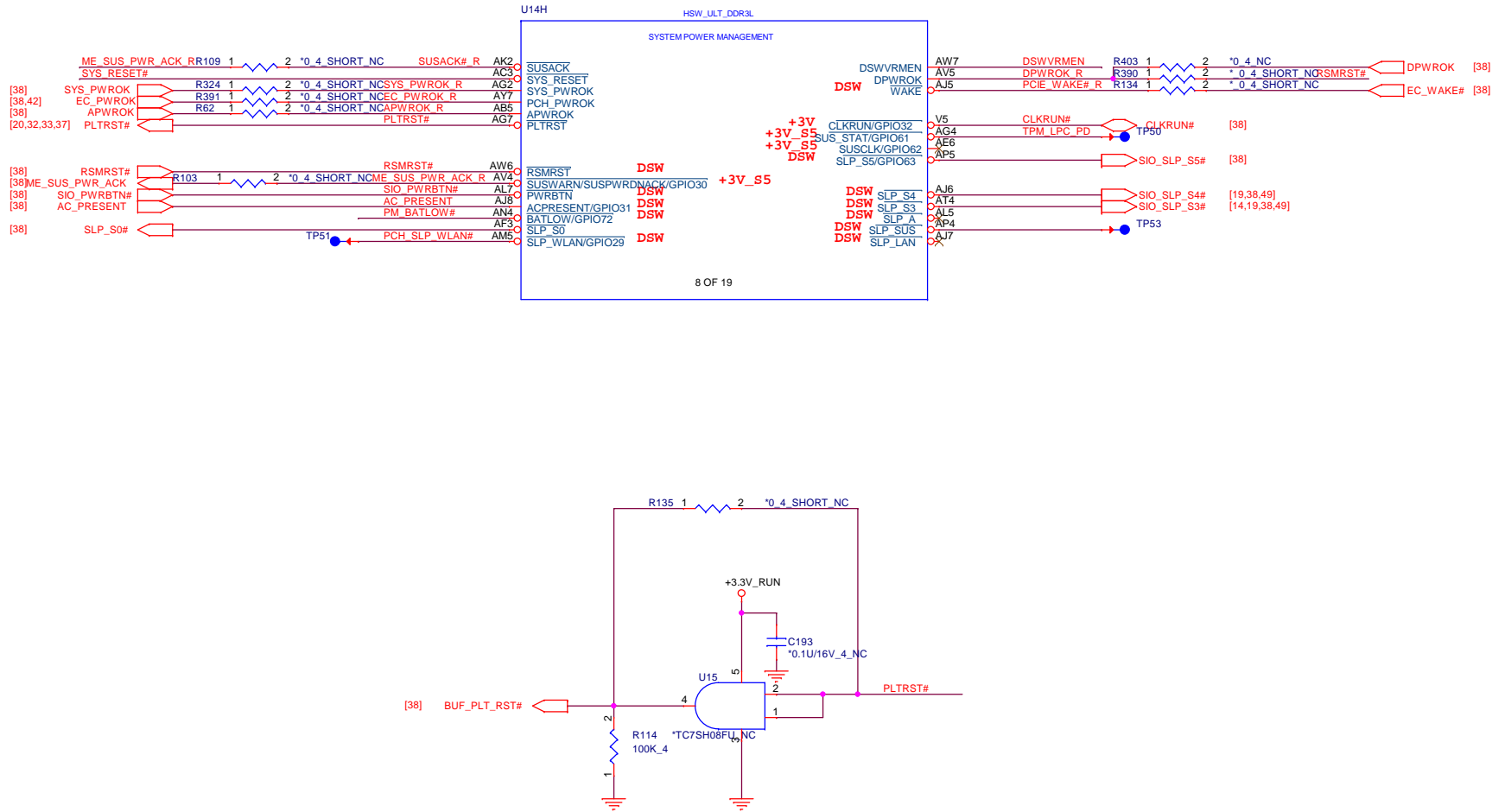
Pin Name	Strap description	Sampled	Configuration	note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Security Effect (Int PD) 1 = Can be Override	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+RTC_CELL 



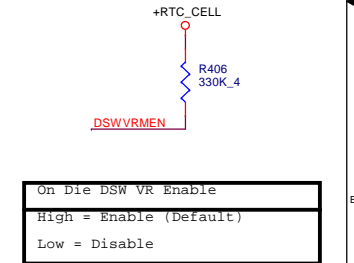
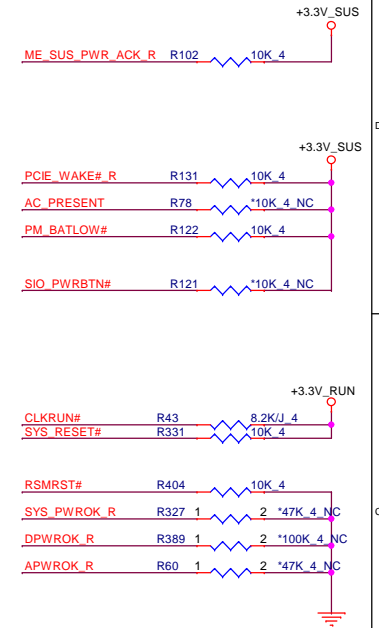
Haswell ULT (LPC/SPI/SMB/CLINK)



Haswell ULT (SYSTEM POWER MANAGEMENT)



PCH Pull-high/low(CLG)



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PROJECT : JW8B

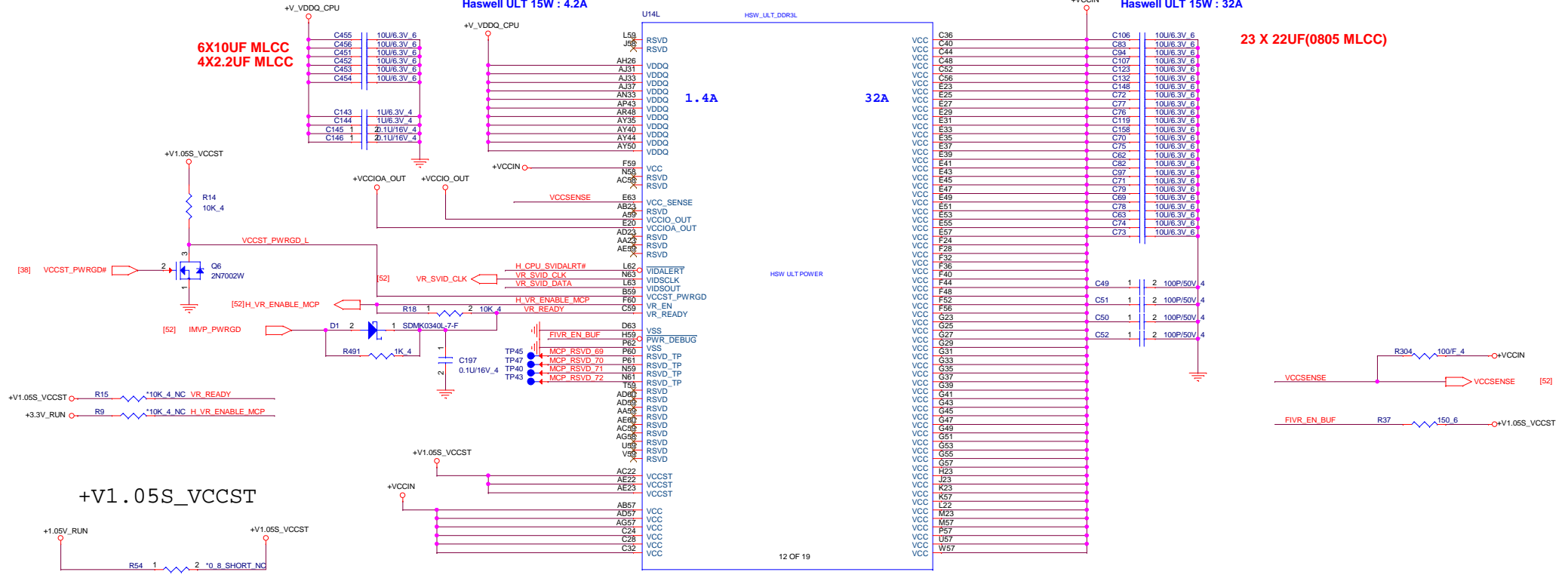
Haswell ULT MCP (POWER)

CPU VDDQ
Haswell ULT 15W : 4.2A

CPU VCC 1/21: 220x23 --> 100x23
Haswell ULT 15W : 32A

6X10UF MLCC
4X2.2UF MLCC

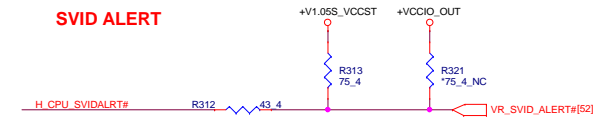
23 X 22UF(0805 MLCC)



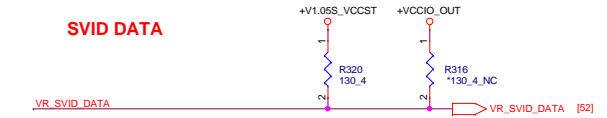
S3 Power reduce

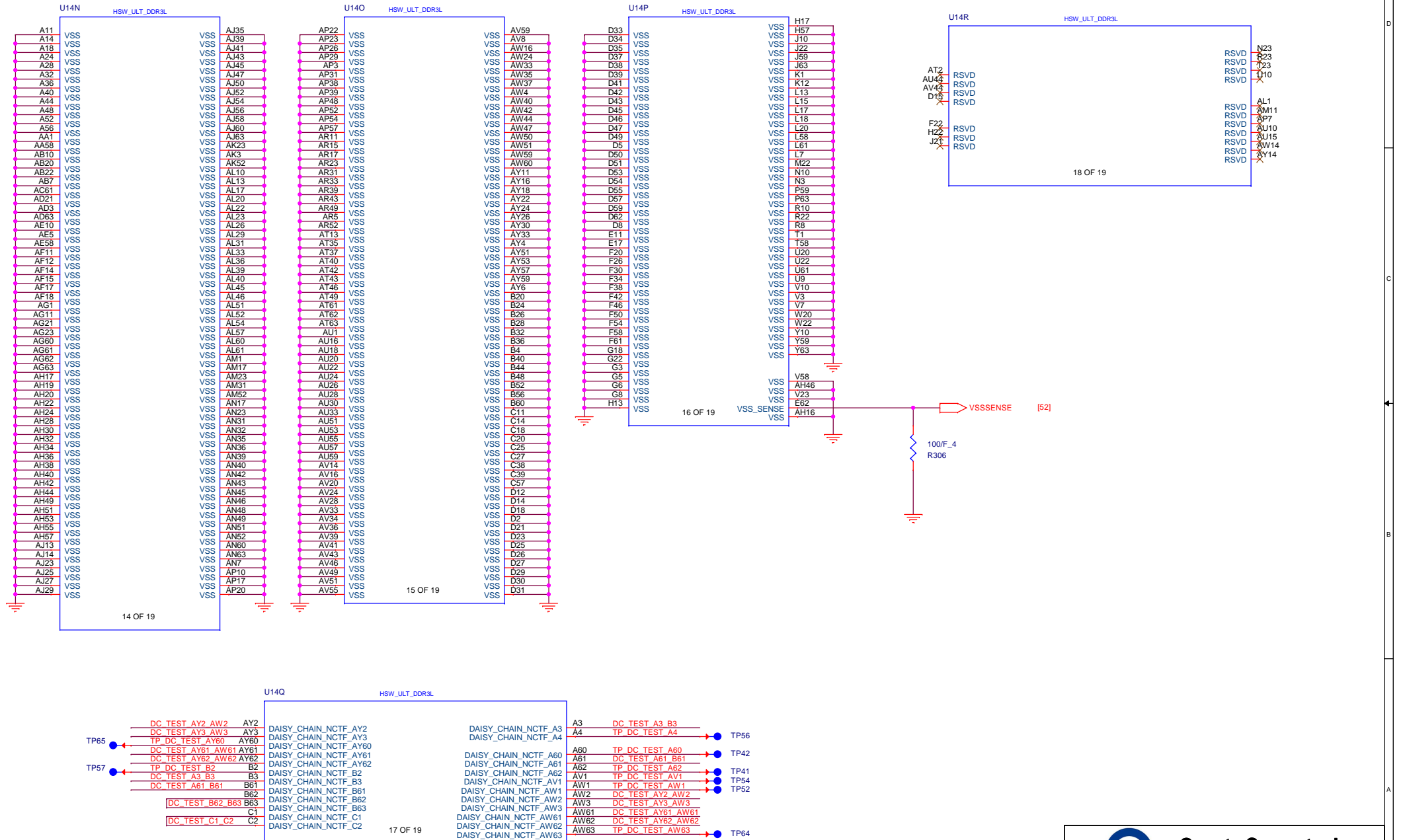


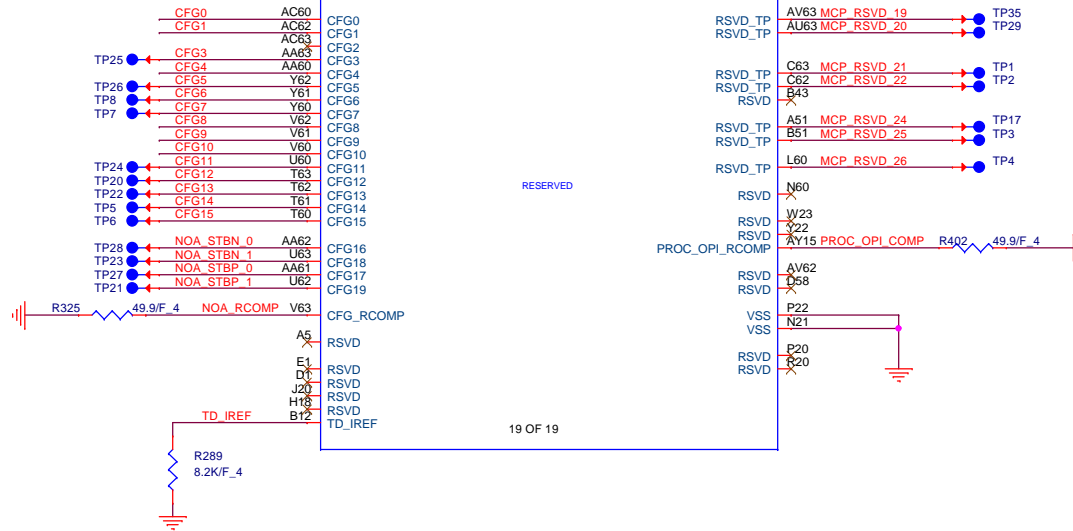
SVID ALERT



SVID DATA







Processor Strapping

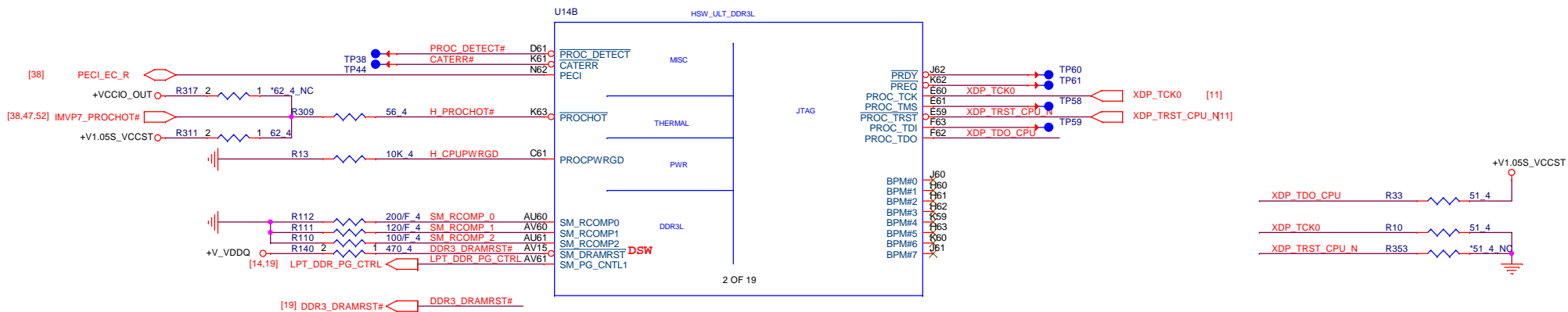
	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	(DEFAULT) NORMAL OPERATION; NO STALL	STALL	CFG0 R339 49.9/F 4 1K 4 NC
CFG1 PCH/ PCH LESS MODE SELECTION	(DEFAULT) NORMAL OPERATION	PCH-LESS MODE	CFG1 R334 49.9/F 4 1K 4 NC
CFG3 PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	CFG3 R330 49.9/F 4 1K 4 NC
CFG4 DISPLAY PORT PRESENCE STRAP	DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	CFG4 R61 49.9/F 4 1K 4
CFG 8 ALLOW THE USE OF NOA ON LOCKED UNITS	DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS	ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT	CFG8 R326 49.9/F 4 1K 4 NC
CFG9 NO SVID PROTOCOL CAPABLE VR CONNECTED	VRS SUPPORTING SVID PROTOCOL ARE PRESENT	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY	CFG9 R58 49.9/F 4 1K 4 NC
CFG10 SAFE MODE BOOT	POWER FEATURES ACTIVATED DURING RESET	POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED	CFG10 R57 49.9/F 4 1K 4 NC

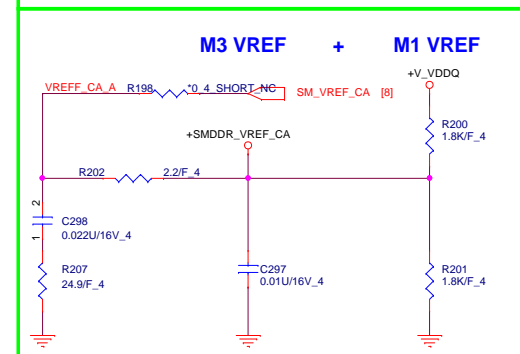
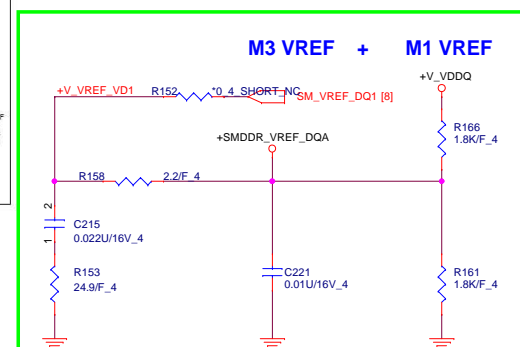
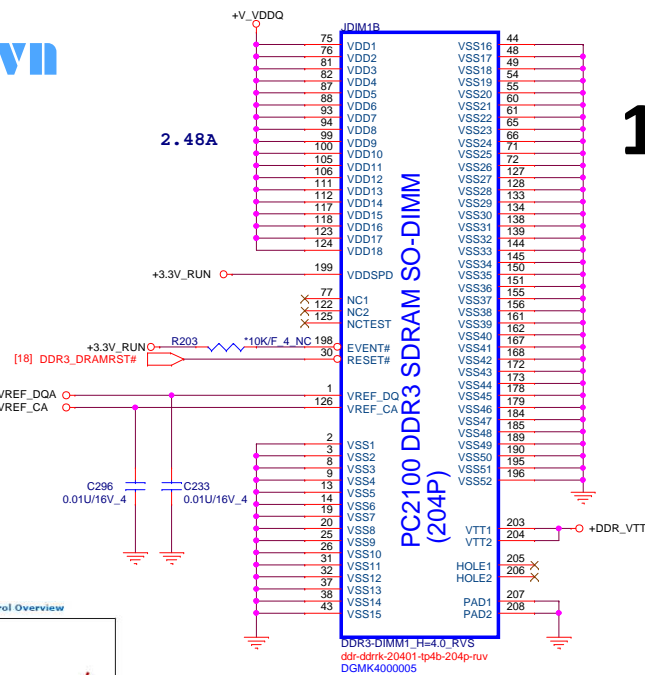


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PROJECT : JW8B







Place these Caps near So-Dimm1.

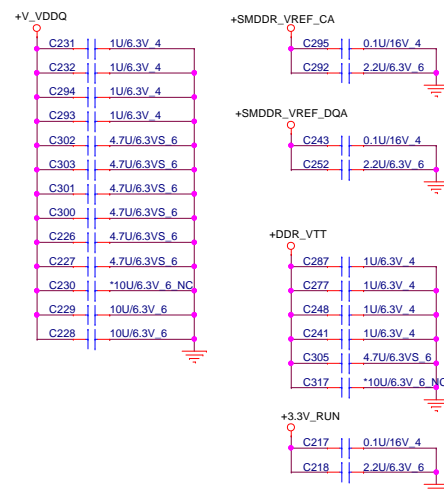


Figure 10 illustrates the pin connections for the PEX1000, divided into two sections: 'Near GPU' and 'Under GPU'. The connections are as follows:

Section	Chip Pin	Board Pin	Signal
Near GPU	C8	A10	PEX_I/OVDD0
	C6	A12	PEX_I/OVDD1
	C15	A16	PEX_I/OVDD2
	C38	A18	PEX_I/OVDD3
Under GPU	C42	A20	PEX_I/OVDD4
	C36	A21	PEX_I/OVDD5
		A22	PEX_I/OVDD6
		A23	PEX_I/OVDD7
		A24	PEX_I/OVDD8
		A25	PEX_I/OVDD9
		A26	PEX_I/OVDD10
		A27	PEX_I/OVDD11

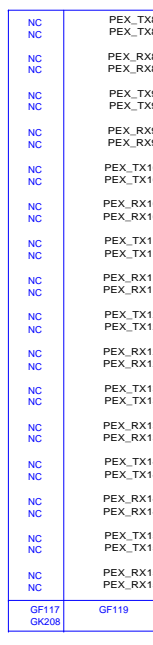
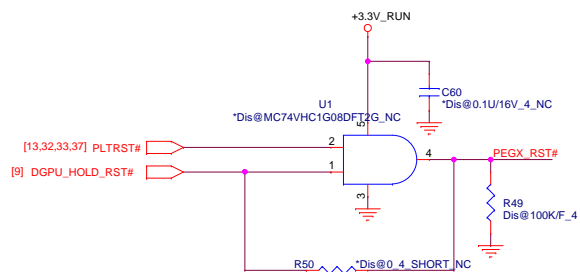
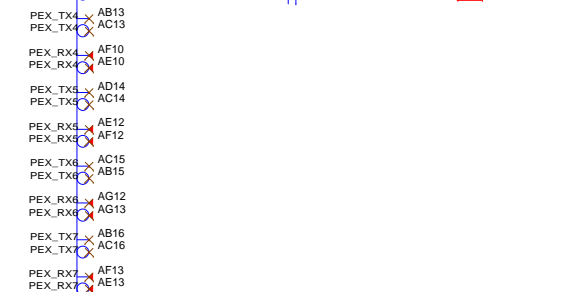
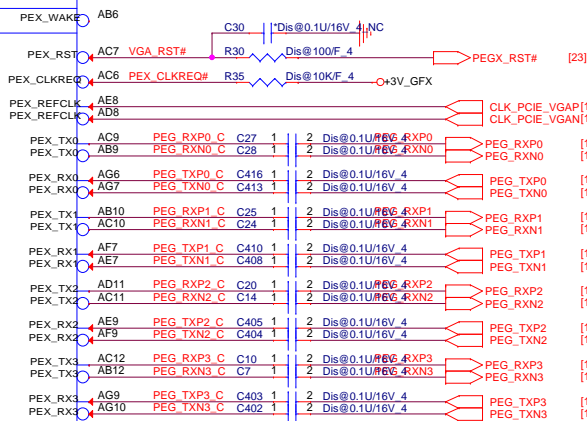
The diagram also indicates a +1.05V_GFX0 supply connected to the board pins A10, A12, A16, A18, A20, A21, A22, A23, A24, A25, A26, and A27.

The schematic diagram illustrates the power plane connections for the Near GPU. It shows three capacitors: C40 (16V), C39 (6.3V), and C54 (6.3V). The connections are as follows:

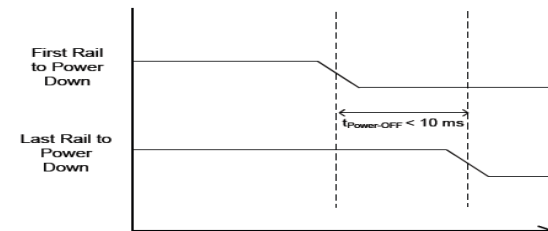
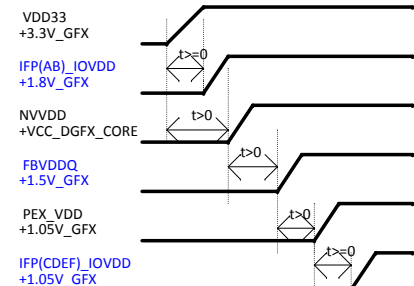
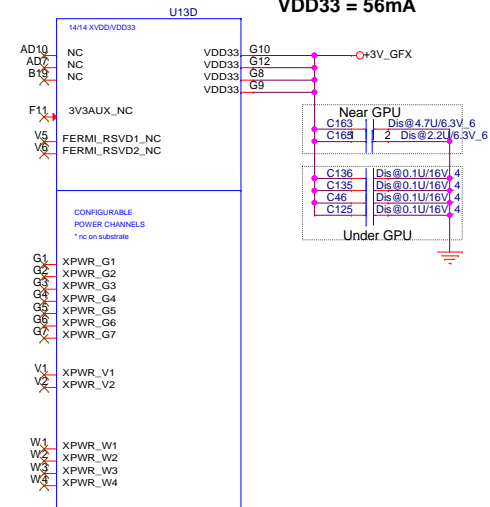
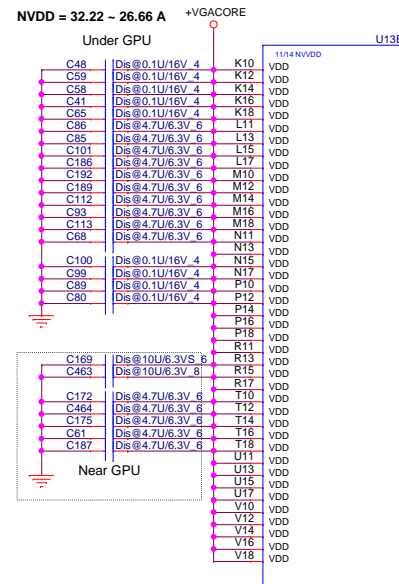
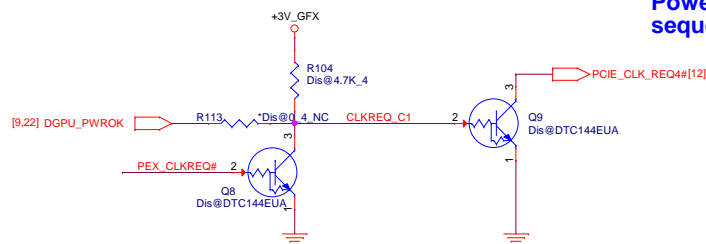
- C40:** Connected to +3V_GFX and Dis@0.1U/16V.
- C39:** Connected to Dis@4.7U/6.3V and AA8.
- C54:** Connected to Dis@4.7U/6.3V and AA9.

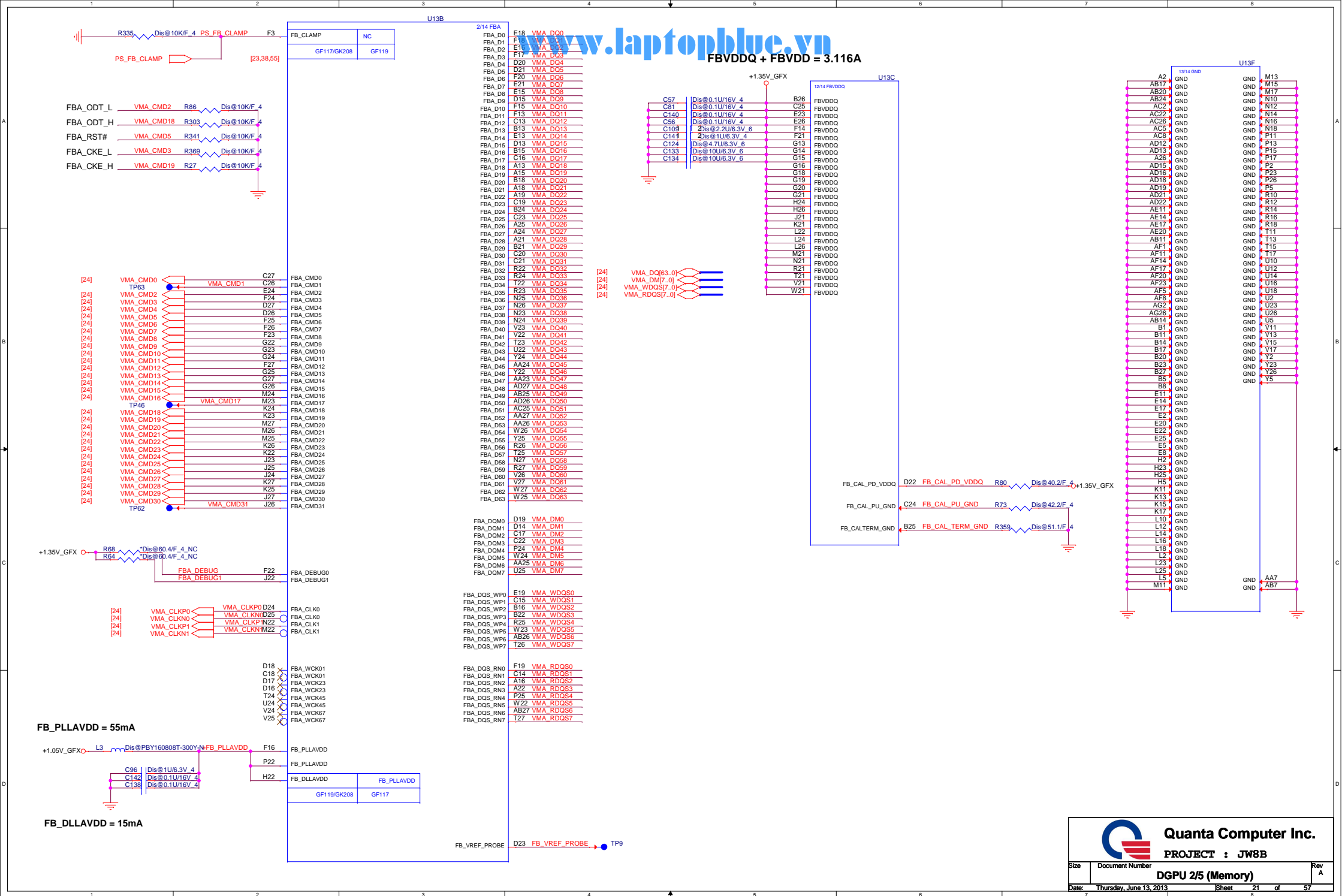
Additional connections shown include:

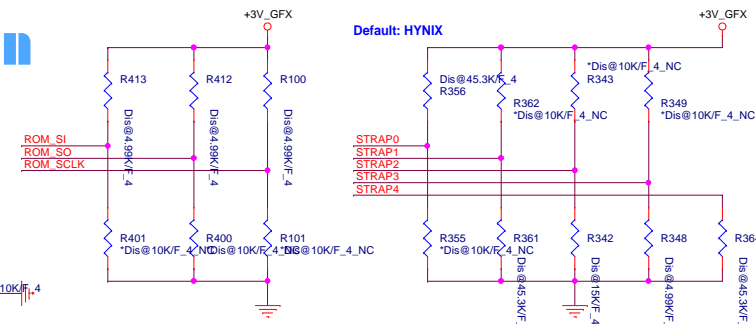
- AA8 connected to PEX_PLL_HVDD.
- AA9 connected to PEX_PLL_HVDD.
- AB8 connected to PEX_SVDD_3V3.

[illegible]

Power down sequence



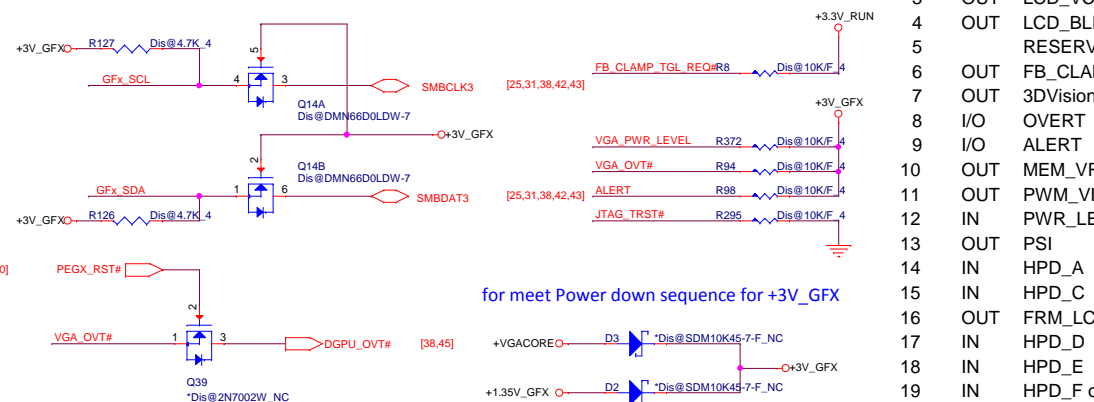


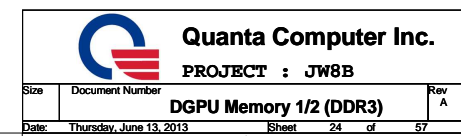


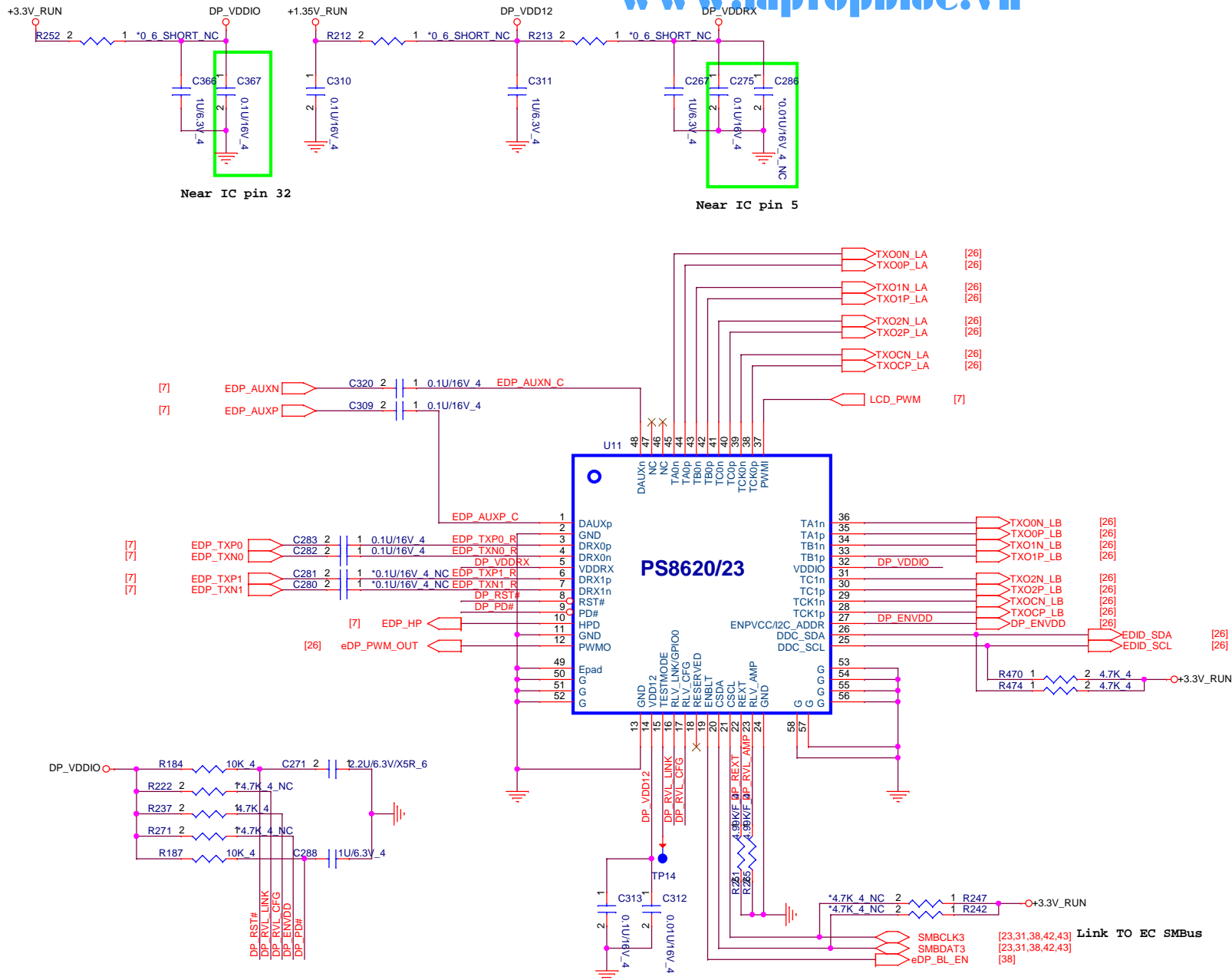
Binary Strap Mode Mapping

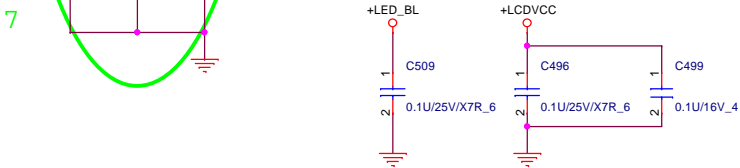
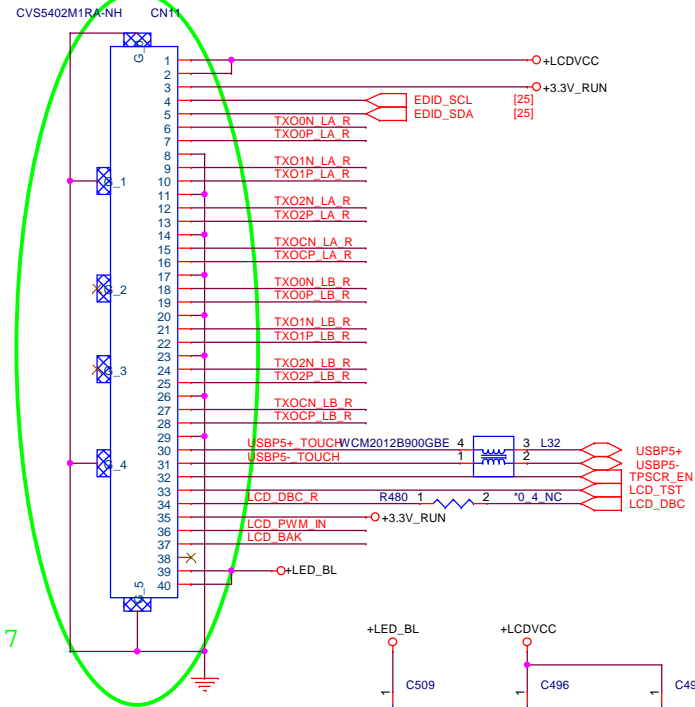
VRAM Configuration Table

GPIO ASSIGNMENTS (GB2-64)

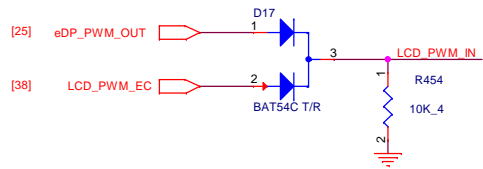
[illegible]



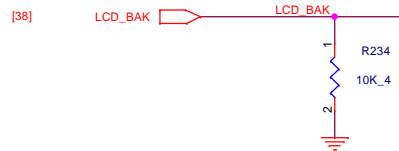




Brightness Control



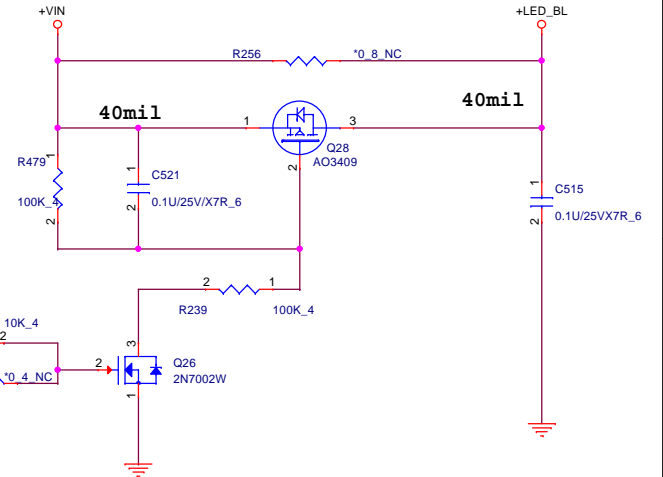
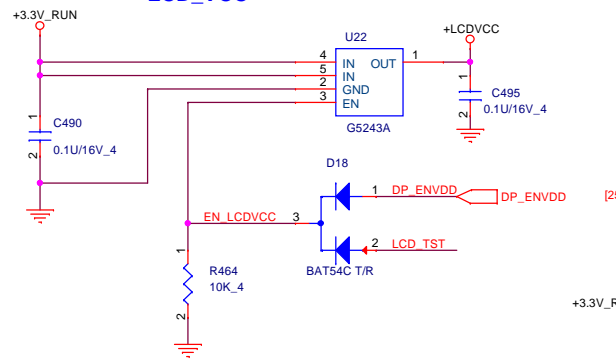
BAK_EN



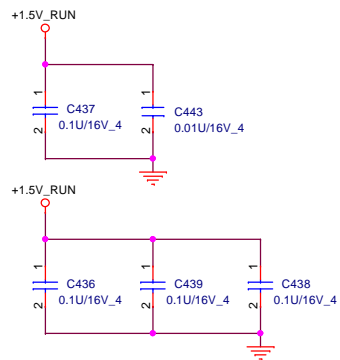
TOUCH SCREEN

[10]
[10]
[38]
[38]
[9]

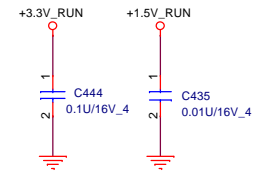
LCD_VCC



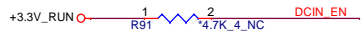
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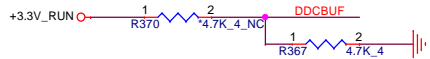
[7] INT_HDMI_TXP2
[7] INT_HDMI_TXN2
[7] INT_HDMI_HP
[7] INT_HDMI_TXP1
[7] INT_HDMI_TXN1
[7] INT_HDMI_TXP0
[7] INT_HDMI_TXN0
[7] INT_HDMI_TXCP
[7] INT_HDMI_TXCN



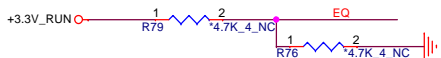
3 Level Input:
L:LOW,internal pull down
H:HIGH, external pull up
M:VDD3/2, both external pill-up and pull-down



Int pull-down 150k , 3.3V IO
L:default,AC coupling input
H:DC coupling input

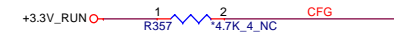
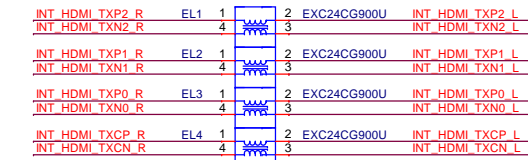
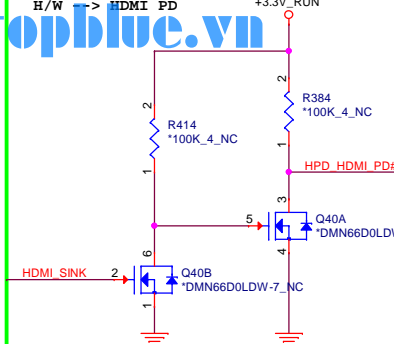
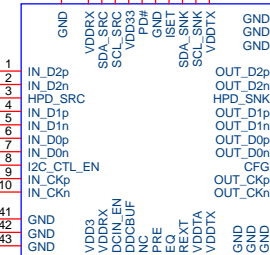


L:default,passive DDC pass-through
H:active DDC buffer with default threshold
M:passive DDC pass-through with internal ~10Kohm pull up



L:programmable EQ for channel loss up to 6.5dB @3Gbps
H:programmable EQ for channel loss up to 9.5dB @3Gbps
M:programmable EQ for channel loss up to 3dB @3Gbps

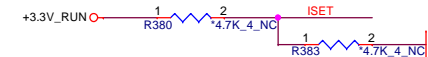
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Int pull-down 150k , 3.3V IO
L:HDMI ID disable
H:HDMI ID enable

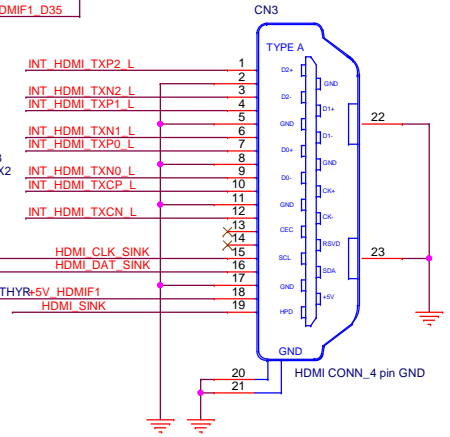


L:no pre-emphasis
H:1.6dB pre-emphasis
M:3.0dB pre-emphasis

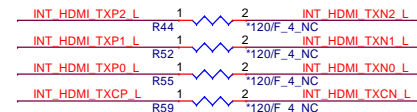


L:default
H:increase +13%
M:increase -13%

HDMI CN



EMI

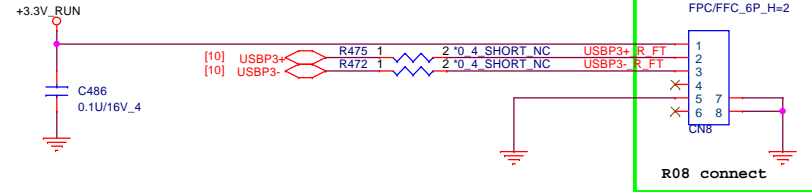
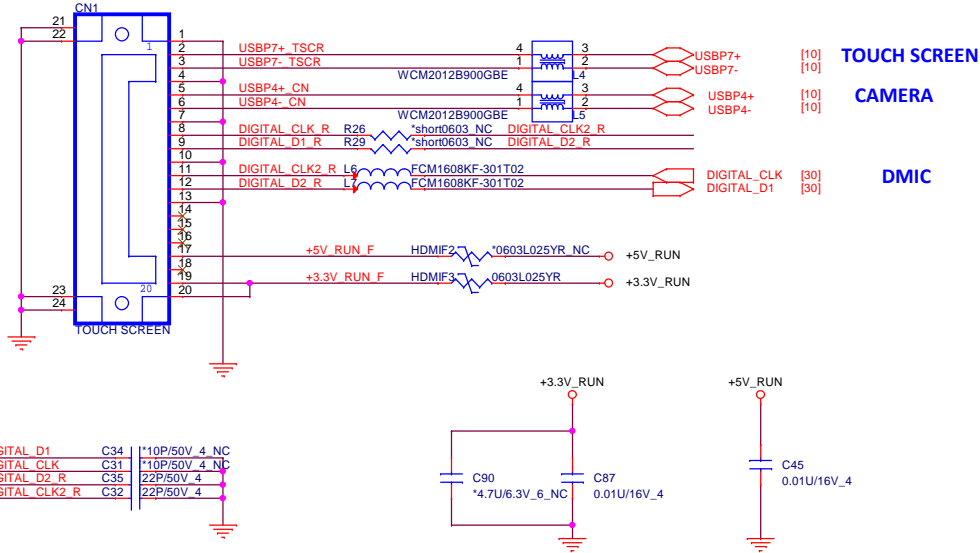


CAMERA / DMIC

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Fingerprint

Conn P/N, Footprint OK. Luke 12/18

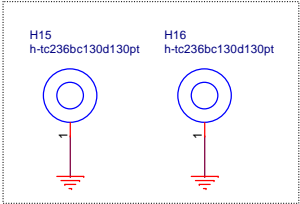


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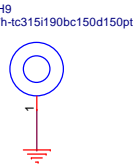
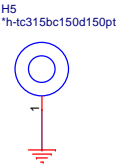
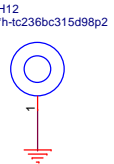
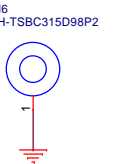
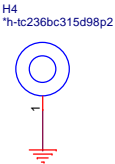
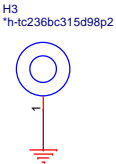
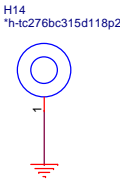
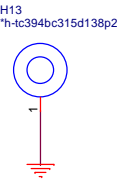
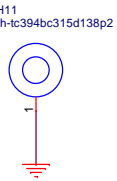
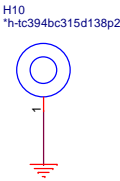
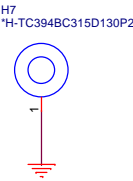
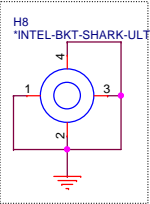
PROJECT : JW8B

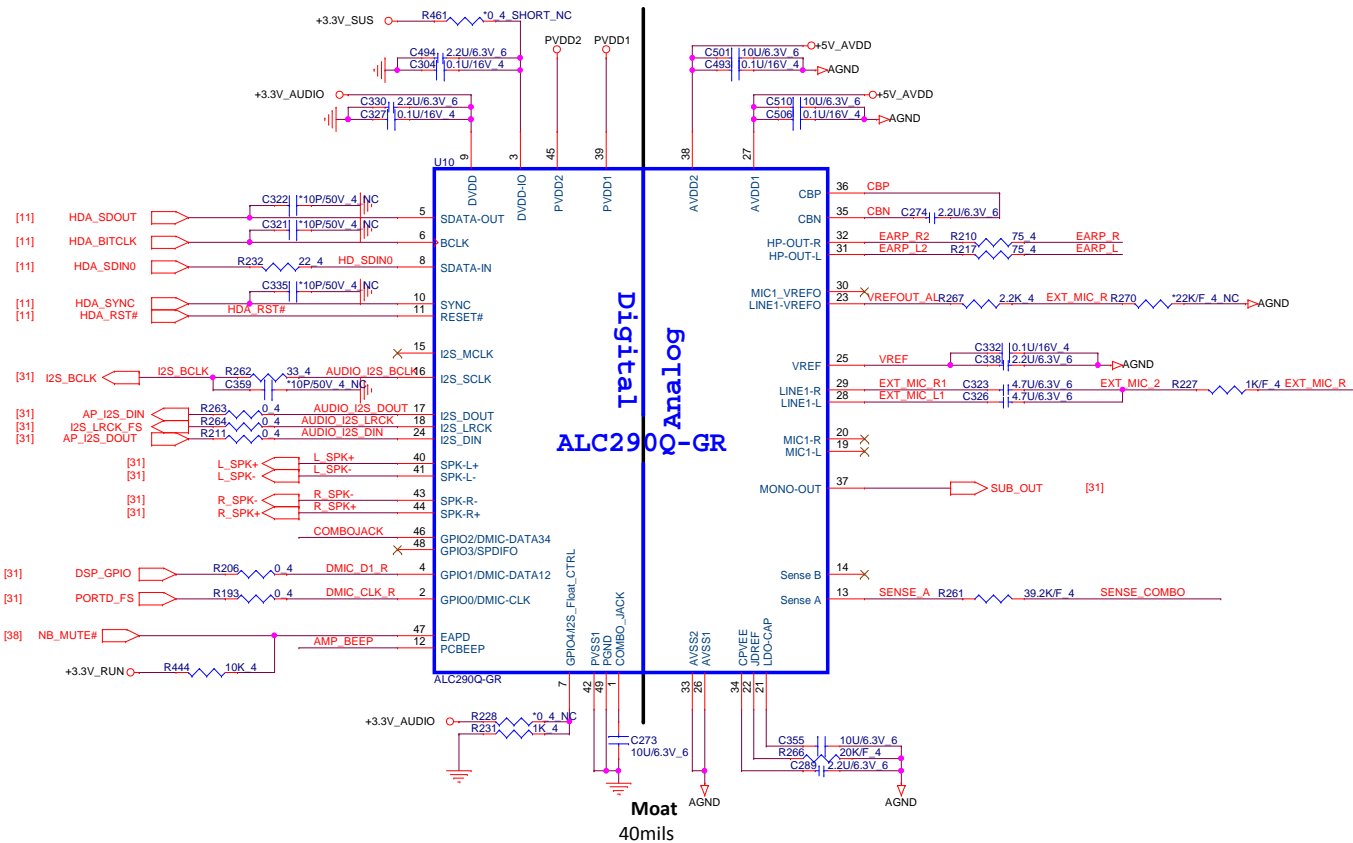
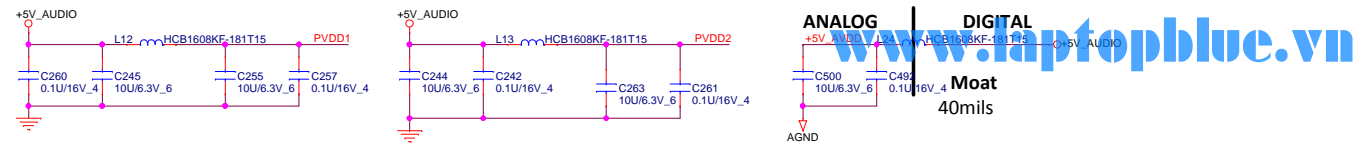
Size	Document Number	Rev
	Camera/Fingerprint Conn	A
Date:	Monday, July 08, 2013	Sheet 28 of 57

Mini-PCIE

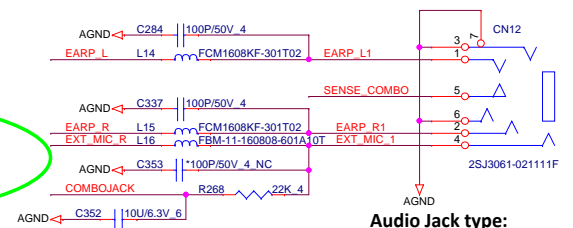


CPU BKT

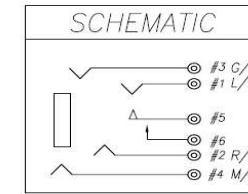
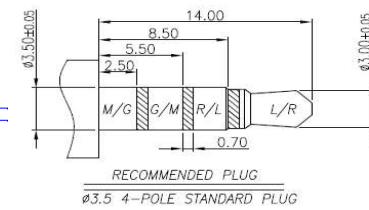
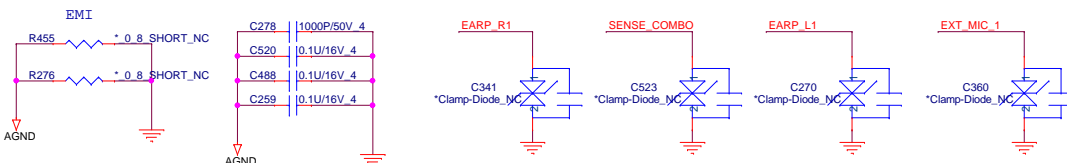
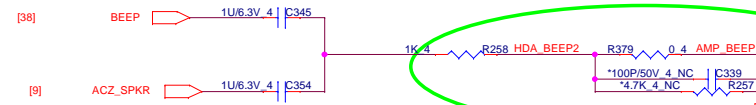
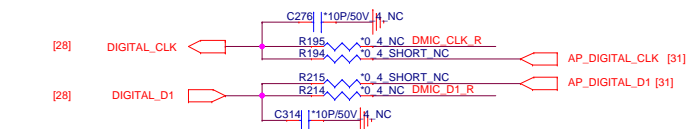




Audio Combo Jack



Audio Jack type:
Normal Open
Combo Jack(IPHONE)



Quanta Computer Inc.

PROJECT : JW8B

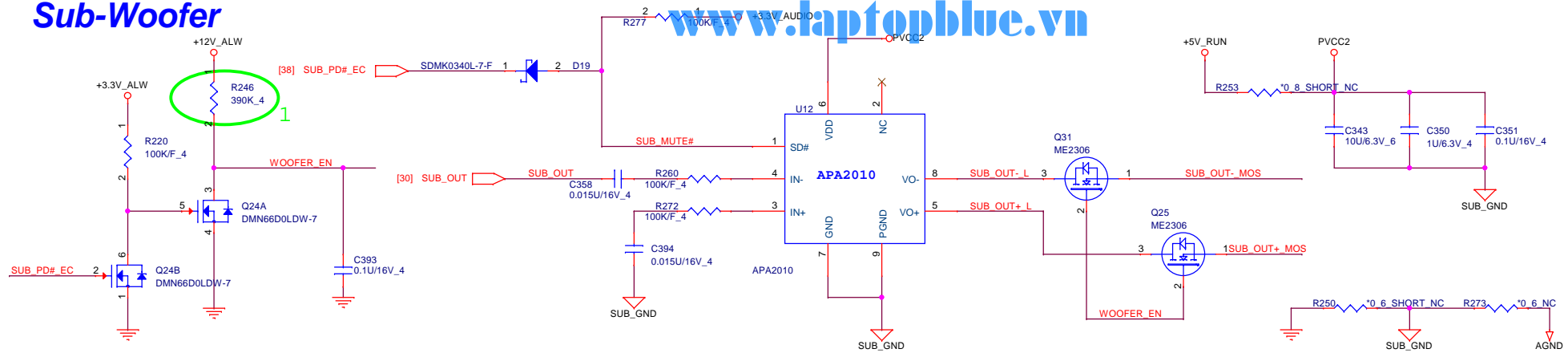
Audio Codec ALC290

Date: Wednesday, July 17, 2013

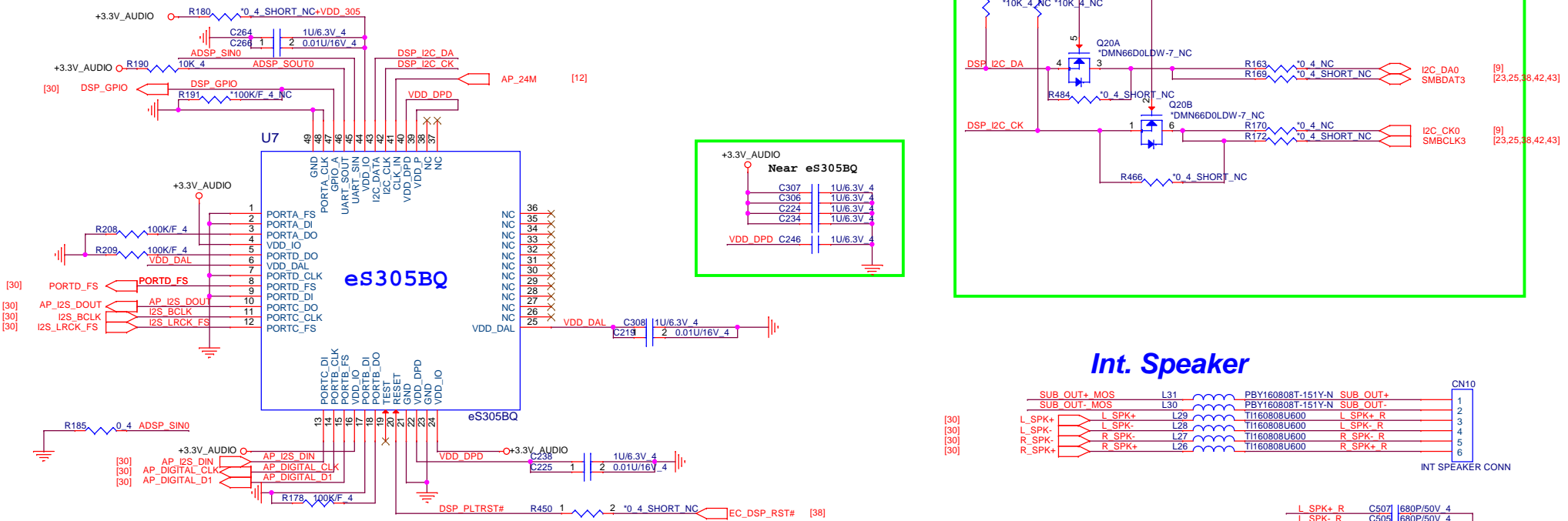
Sheet 30 of 57

Rev A

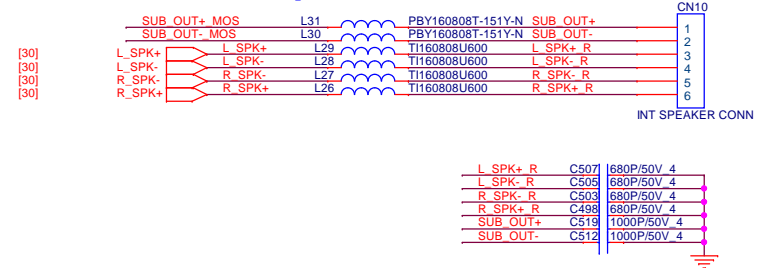
Sub-Woofer



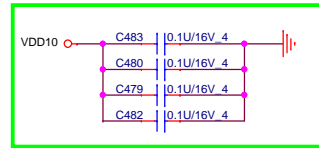
Audio Processor



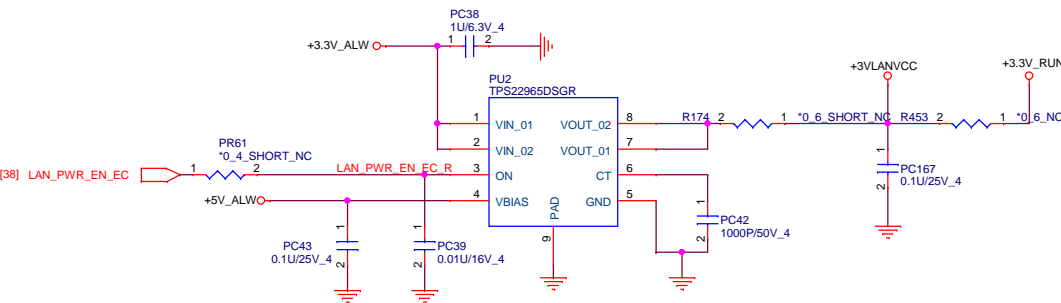
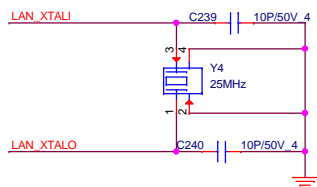
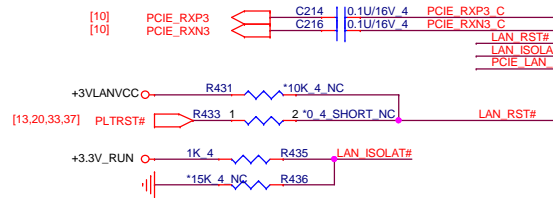
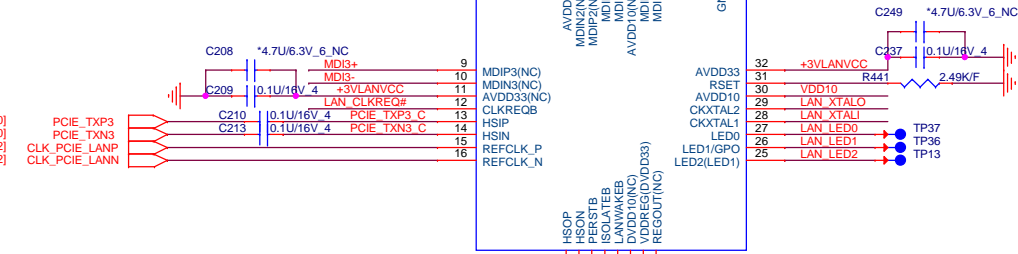
Int. Speaker



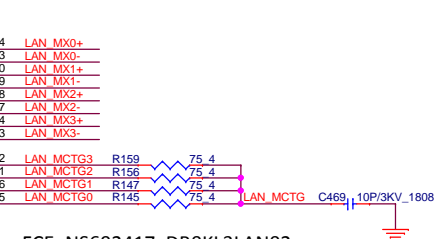
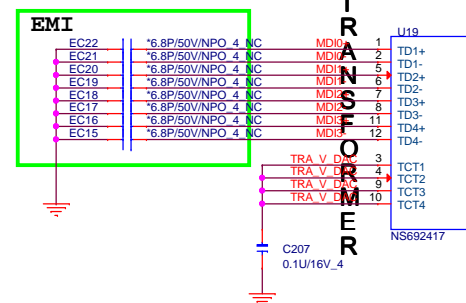
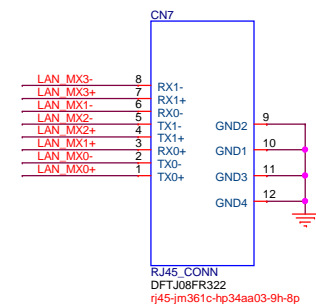
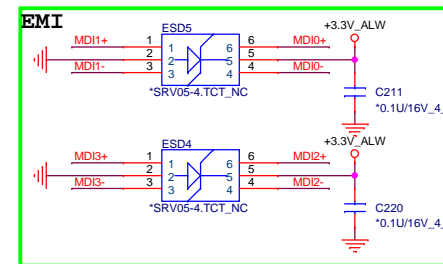
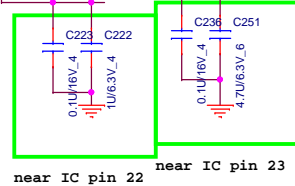
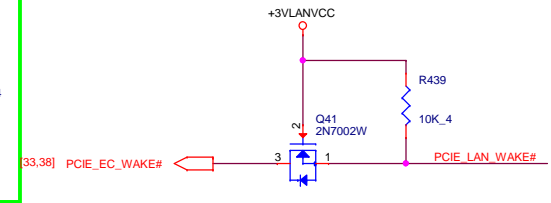
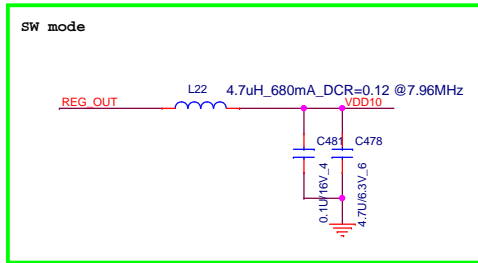
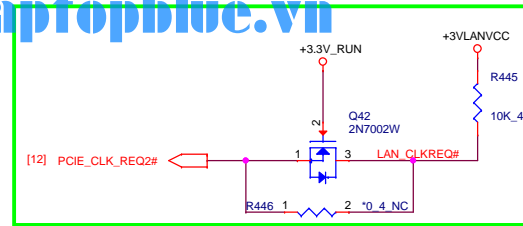
JW8 have support S5 wave up



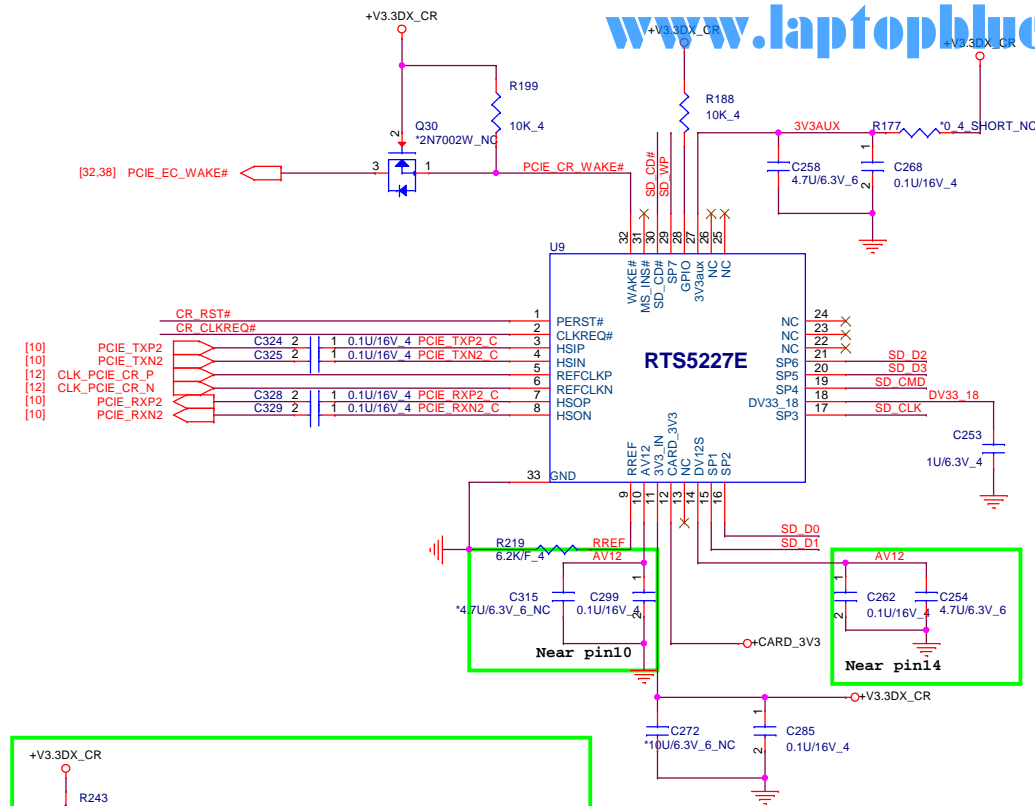
Each CAP near IC pin 3 , 8 , 22 , 30



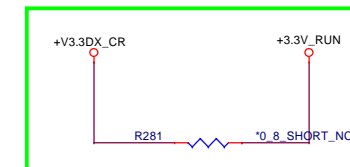
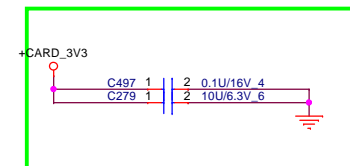
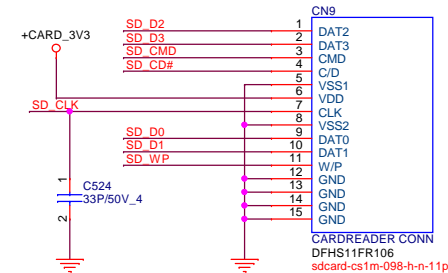
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FCE: NS692417, DBOKL3LAN02
BOT: NA0069R LF, DBOKL3LAN01



SD / MMC CARD READER



Quanta Computer Inc.

PROJECT : JW8B

Card Reader RTS5179

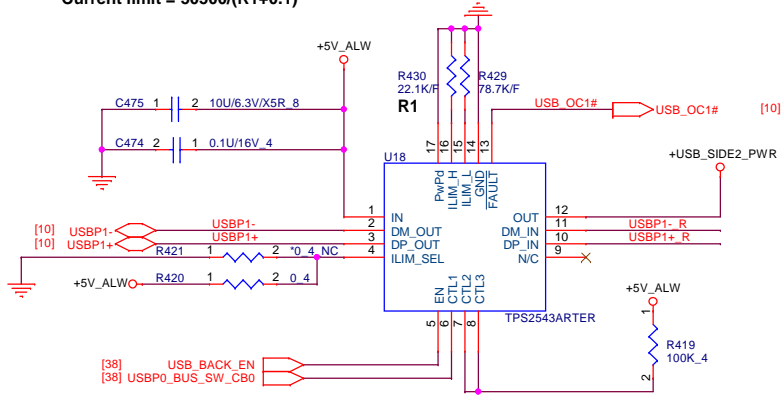
USB3.0 Power Share

USB Power share

USBP0_BUS_SW_CB0		Mode
Low		DCP, Auto-detect
High		CDP, BC Spec 1.2
OC limitation	R1	mA
	100k ohm	504
	22.1k ohm	2274

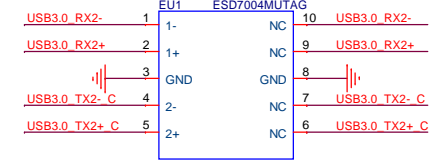
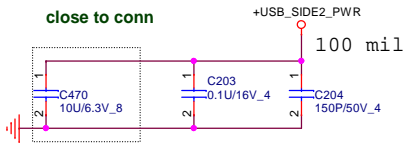
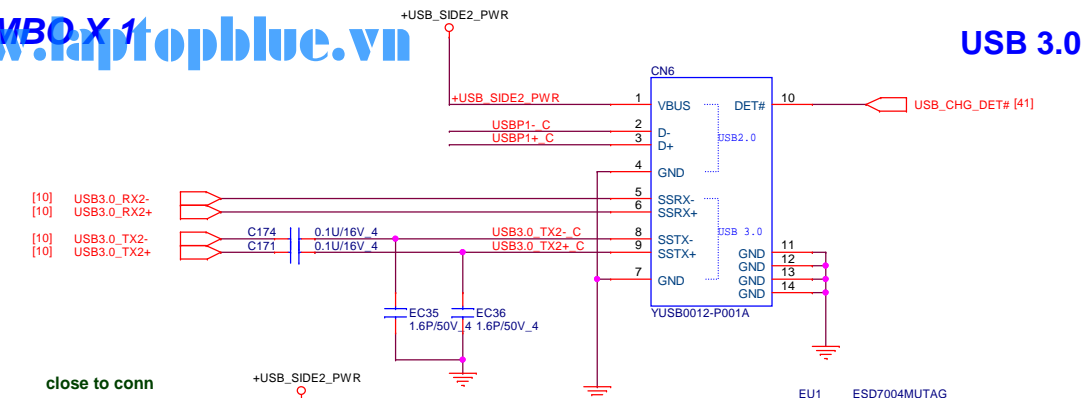
Applied Now

Current limit = 50500/(R1+0.1)



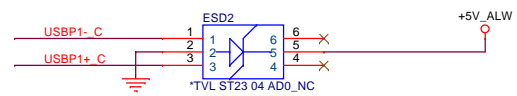
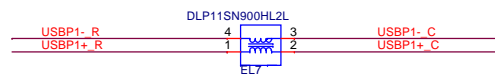
USB3.0/2.0 COMBO X1

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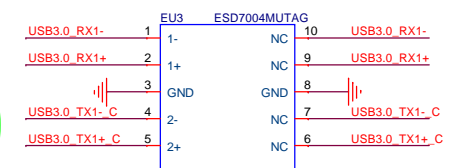
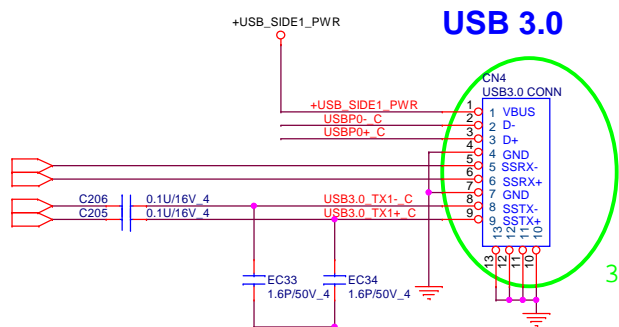
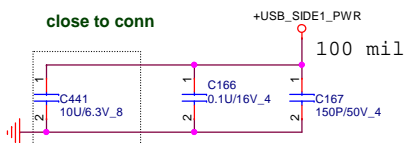
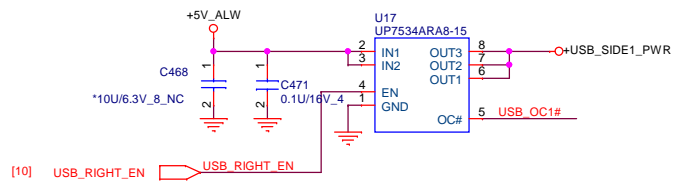
ESD Function

Place ESD diodes as close as USB connector.



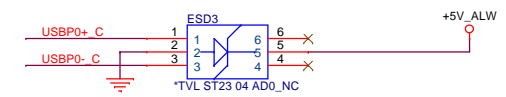
USB3.0/2.0 COMBO

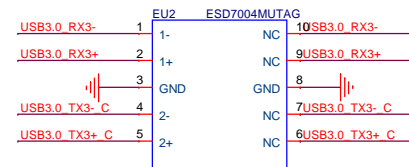
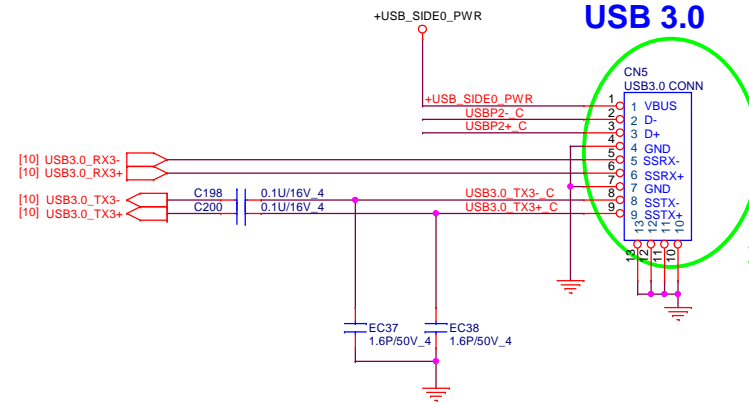
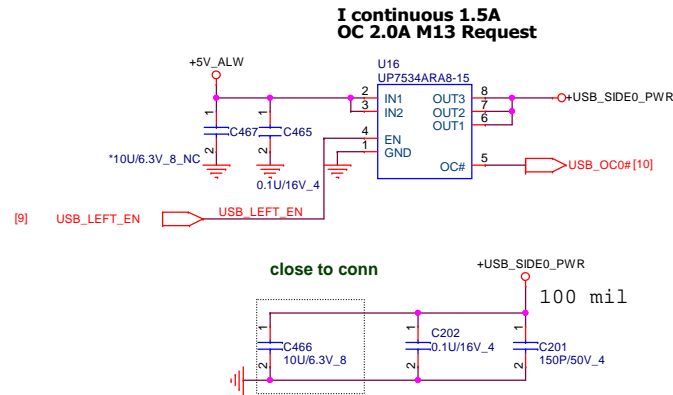
I continuous 1.5A
OC 2.0A M13 Request



ESD Function

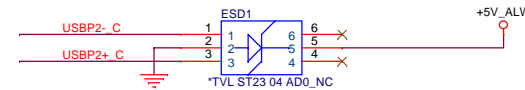
Place ESD diodes as close as USB connector.





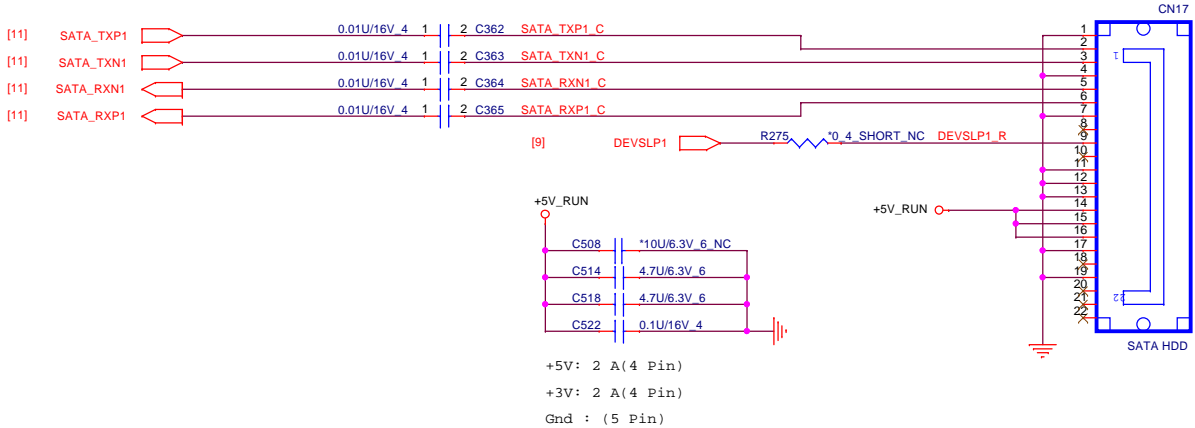
ESD Function

Place ESD diodes as close as USB connector.

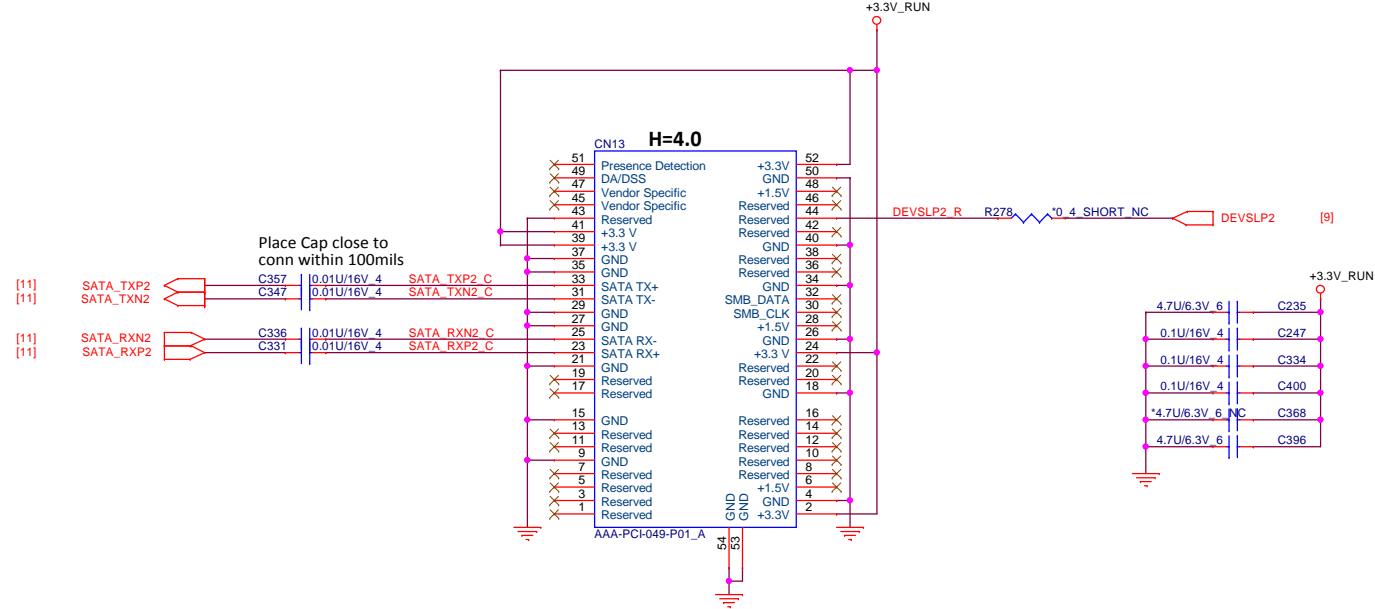


Quanta Computer Inc.

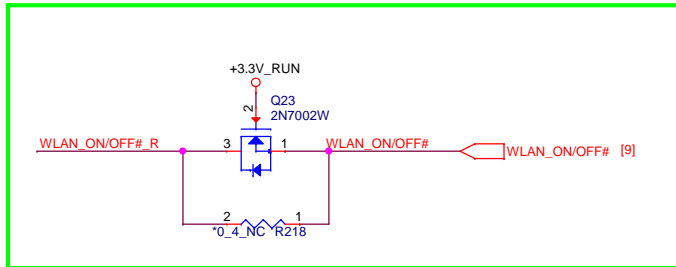
PROJECT : JW8B



mSATA

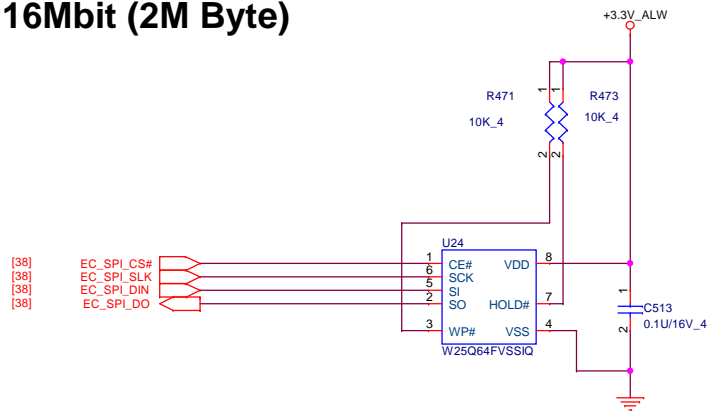


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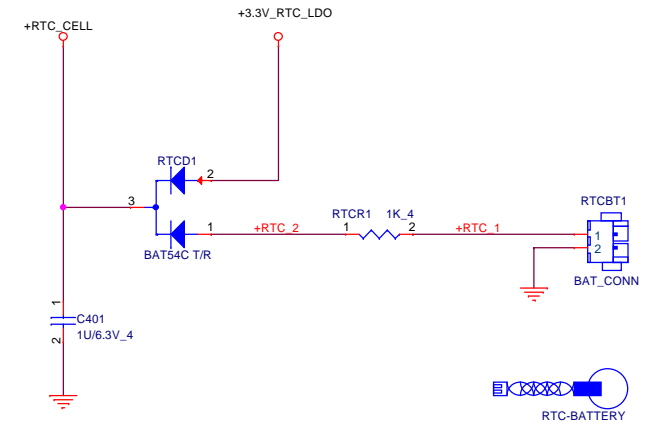




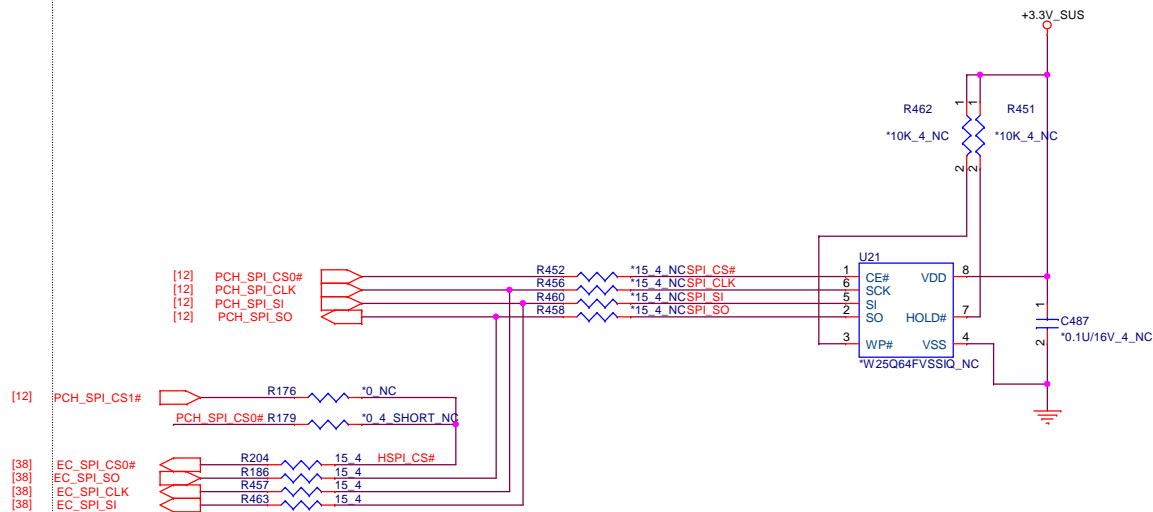
For EC 16Mbit (2M Byte)



RTC BATTERY



For PCH 64Mbit (8M Byte)



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PROJECT : JW8B

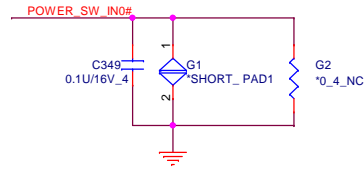
Size	Document Number	Rev
		A
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FLASH / RTC

Keyboard Connector

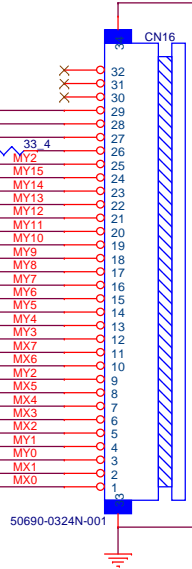
[38] MY[0..15] MY[0..15]
[38] MX[0..7] MX[0..7]

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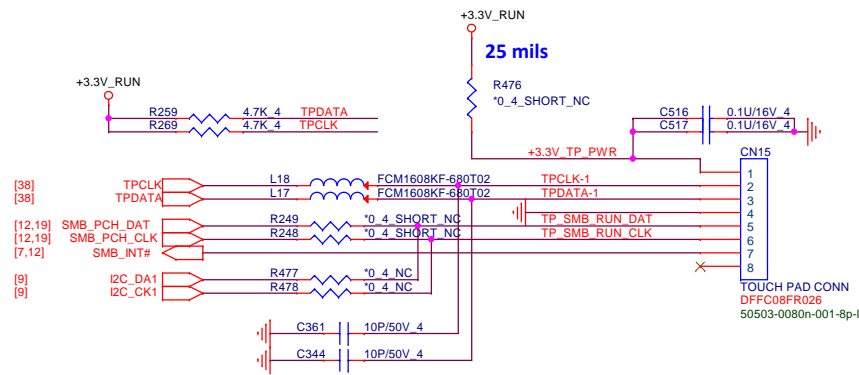
[41,45] POWER_SW_IN0#

+3.3V_RUN



MY1	C389	220P/50V_4
MY2	C384	220P/50V_4
MY4	C380	220P/50V_4
MY0	C390	220P/50V_4
MX4	C386	220P/50V_4
MX6	C383	220P/50V_4
MX3	C387	220P/50V_4
MX2	C388	220P/50V_4
MY5	C379	220P/50V_4
MY6	C378	220P/50V_4
MY3	C381	220P/50V_4
MY7	C377	220P/50V_4
MY8	C376	220P/50V_4
MY9	C375	220P/50V_4
MY10	C374	220P/50V_4
MY11	C373	220P/50V_4
MX7	C382	220P/50V_4
MX0	C392	220P/50V_4
MX5	C385	220P/50V_4
MX1	C391	220P/50V_4
MY12	C372	220P/50V_4
MY13	C371	220P/50V_4
MY14	C370	220P/50V_4
MY15	C369	220P/50V_4

Touch Pad Connector



25 mils

+3.3V_RUN

R476 '0_4_SHORT_NC

+3.3V_TP_PWR

C516 0.1U/16V_4
C517 0.1U/16V_4

TPCLK-1
TPDATA-1

TP SMB RUN DAT
TP SMB RUN CLK

TPCLK
TPDATA

SMB_PCH_DAT
SMB_PCH_CLK
SMB_INT#

I2C_DA1
I2C_CLK1
I2C_CLK2

C361 10P/50V_4
C344 10P/50V_4

TOUCH PAD CONN
DFFC08FR026
50503-0080n-001-8p-l



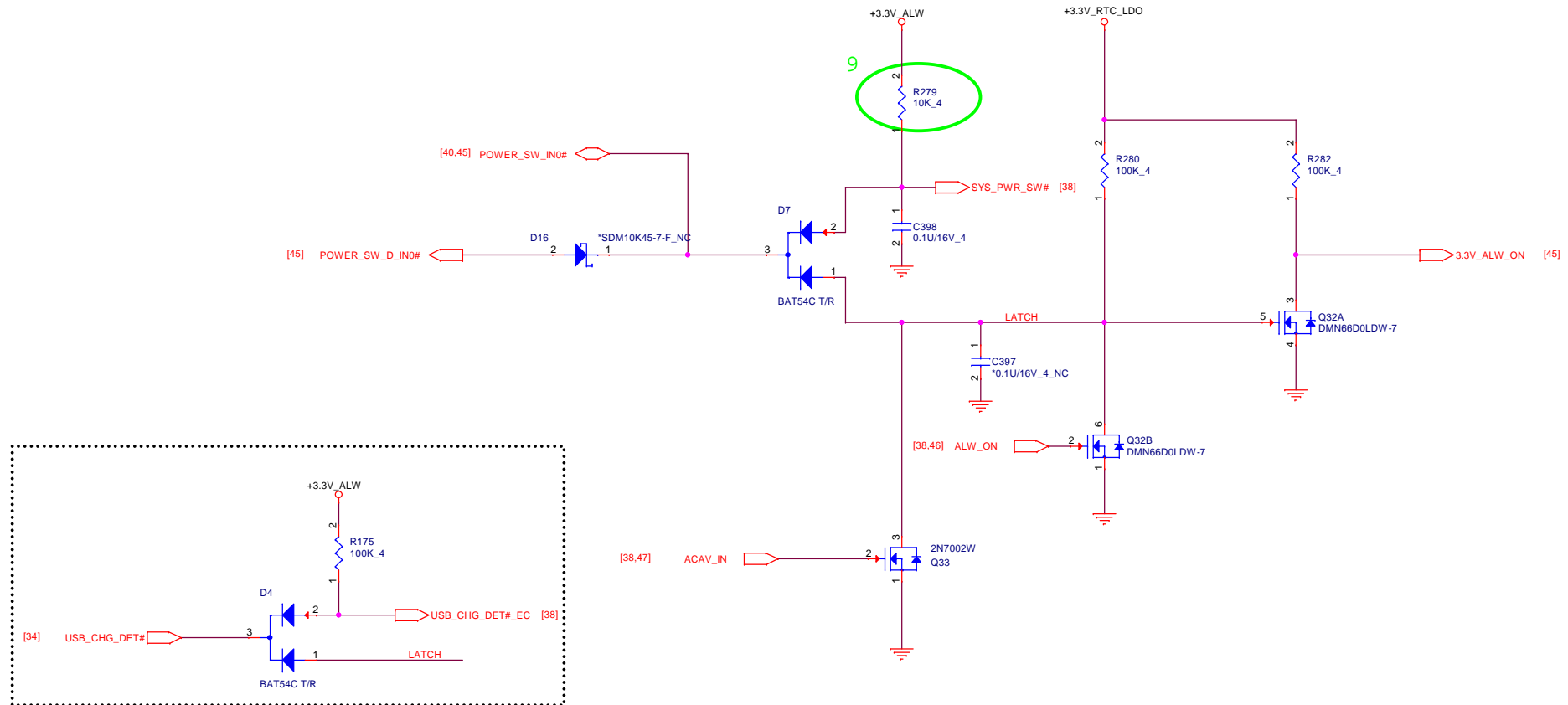
Quanta Computer Inc.

PROJECT : JW8B

KB/CLK Gen/FAN/TP

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		A
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3VALW ON POWER LOGIC



Quanta Computer Inc.

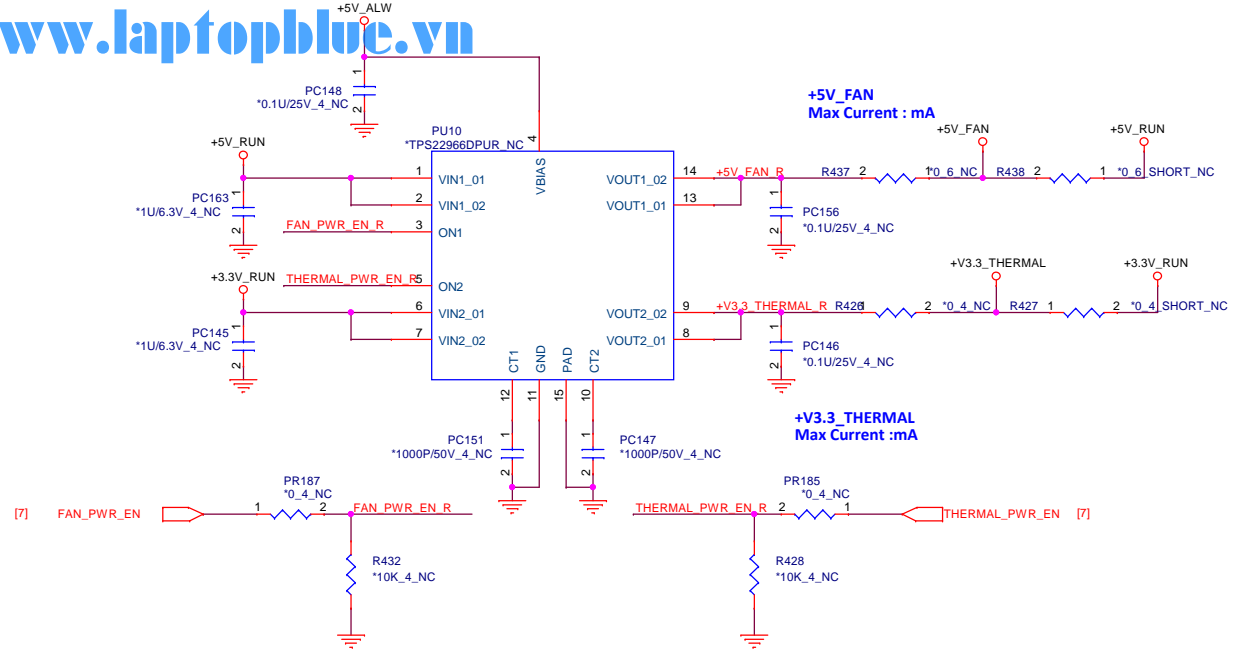
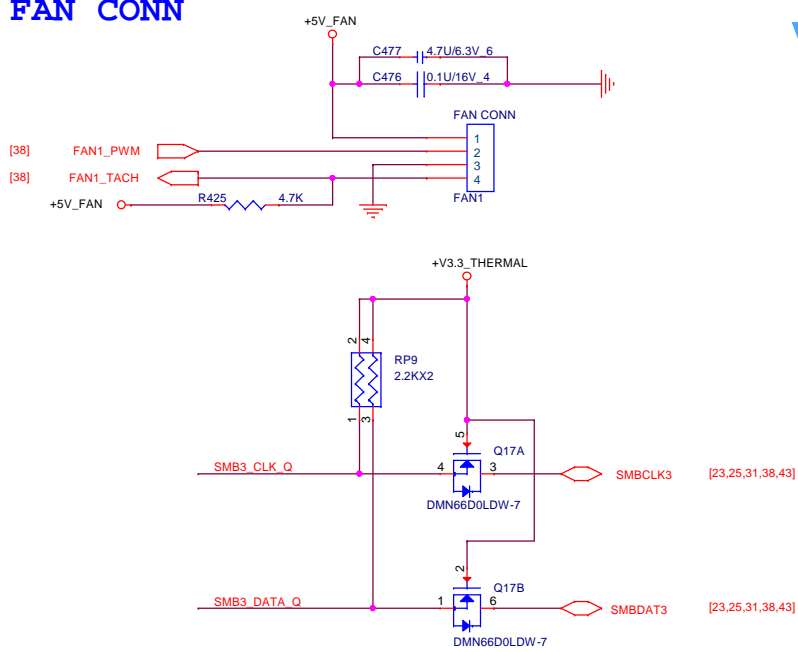
PROJECT : JW8B

3VALW ON POWER LOGIC

Size	Document Number	Rev
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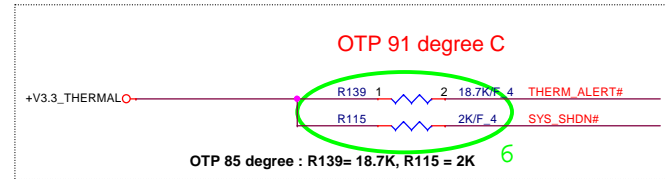
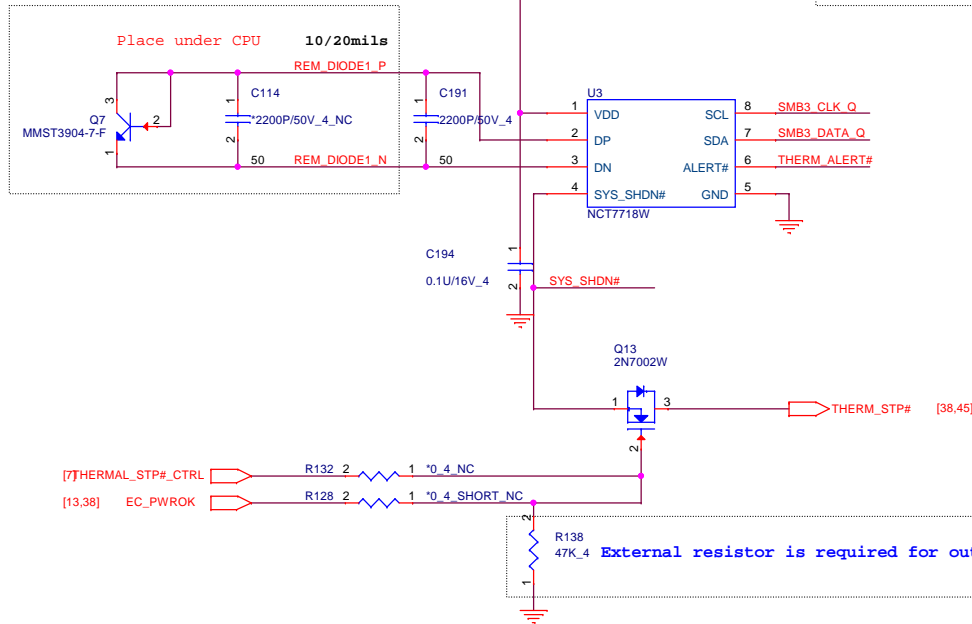
FAN CONN

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THERMAL IC

Need closed to CPU

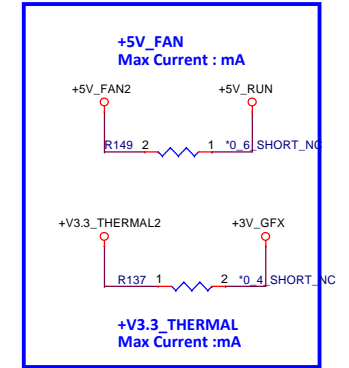
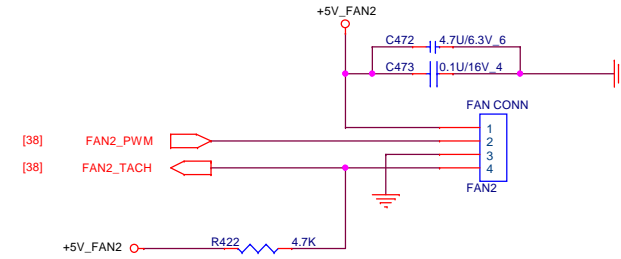
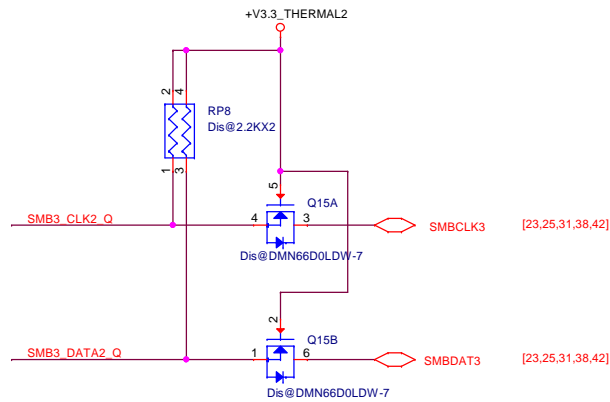
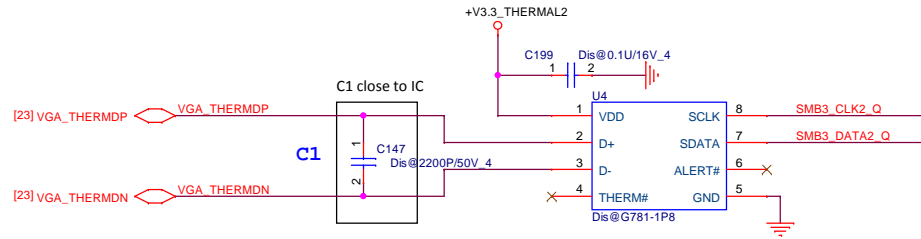


SYS_SHDN#	2K	7.5K	10.5K	14K	18.7K
ALERT#					
2K	77'C	87'C	97'C	107'C	117'C
7.5K	79'C	89'C	99'C	109'C	119'C
10.5K	81'C	91'C	101'C	111'C	121'C
14K	83'C	93'C	103'C	113'C	123'C
18.7K	85'C	95'C	105'C	115'C	125'C

For GPU use

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G781-1P8
SMBus address is 1001101xb (9Ah) (x is R/W bit).

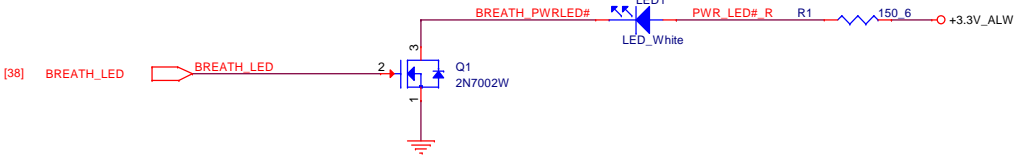


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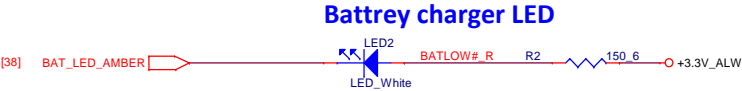
PROJECT : JW8B

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	Thermal GPU	A
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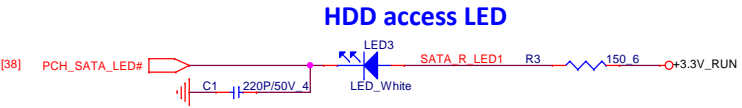
LED Status



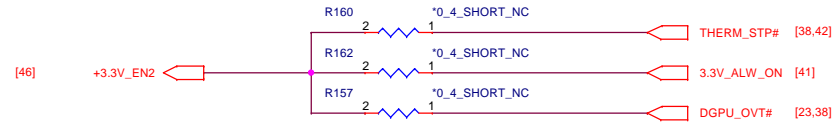
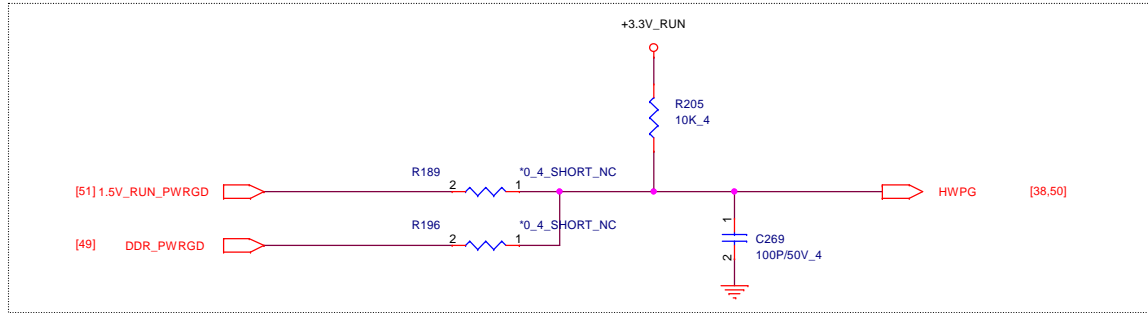
System status LED



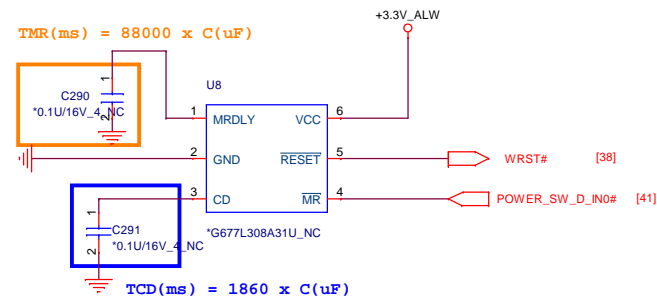
Battrey charger LED



HDD access LED



HW reset IC

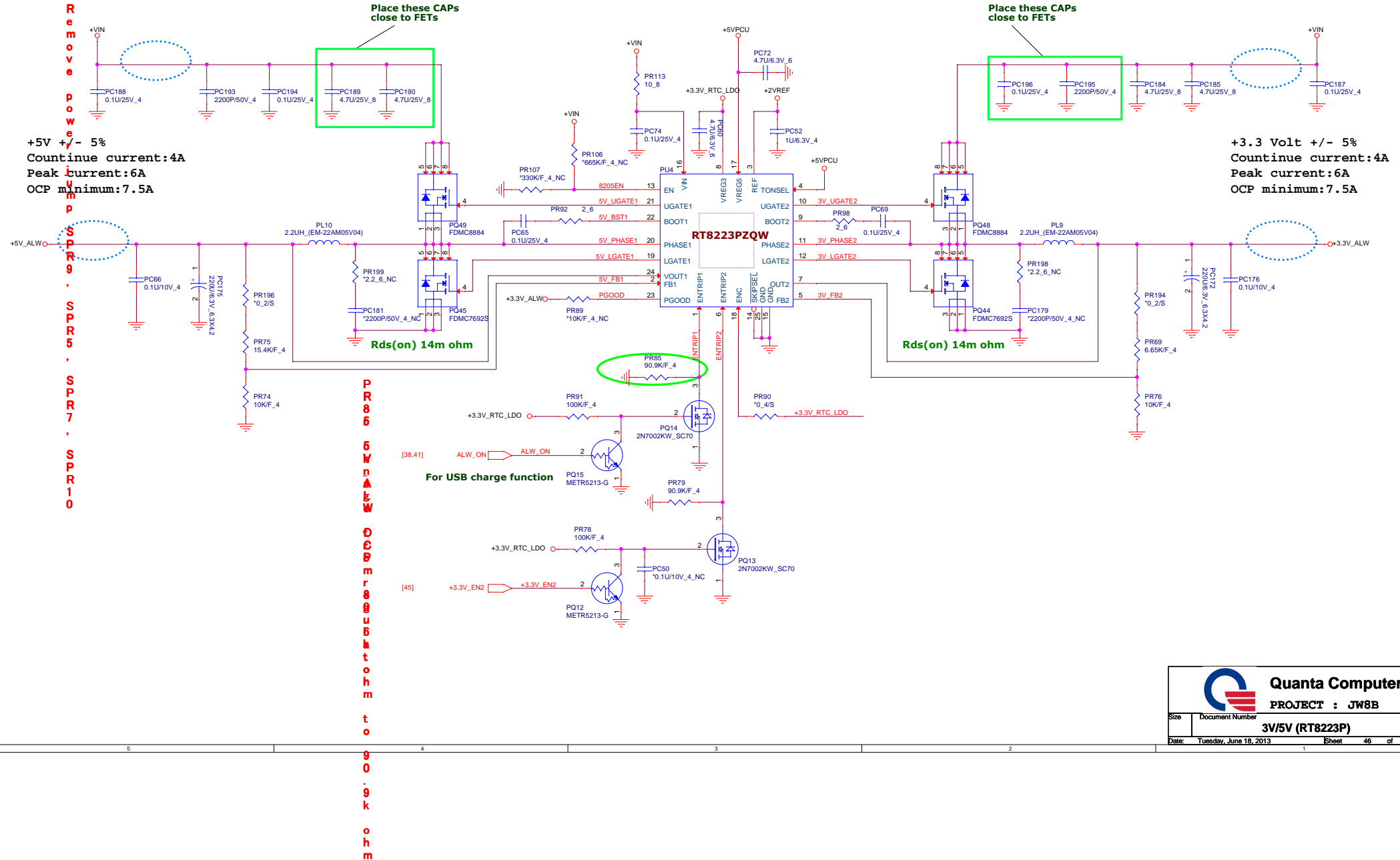


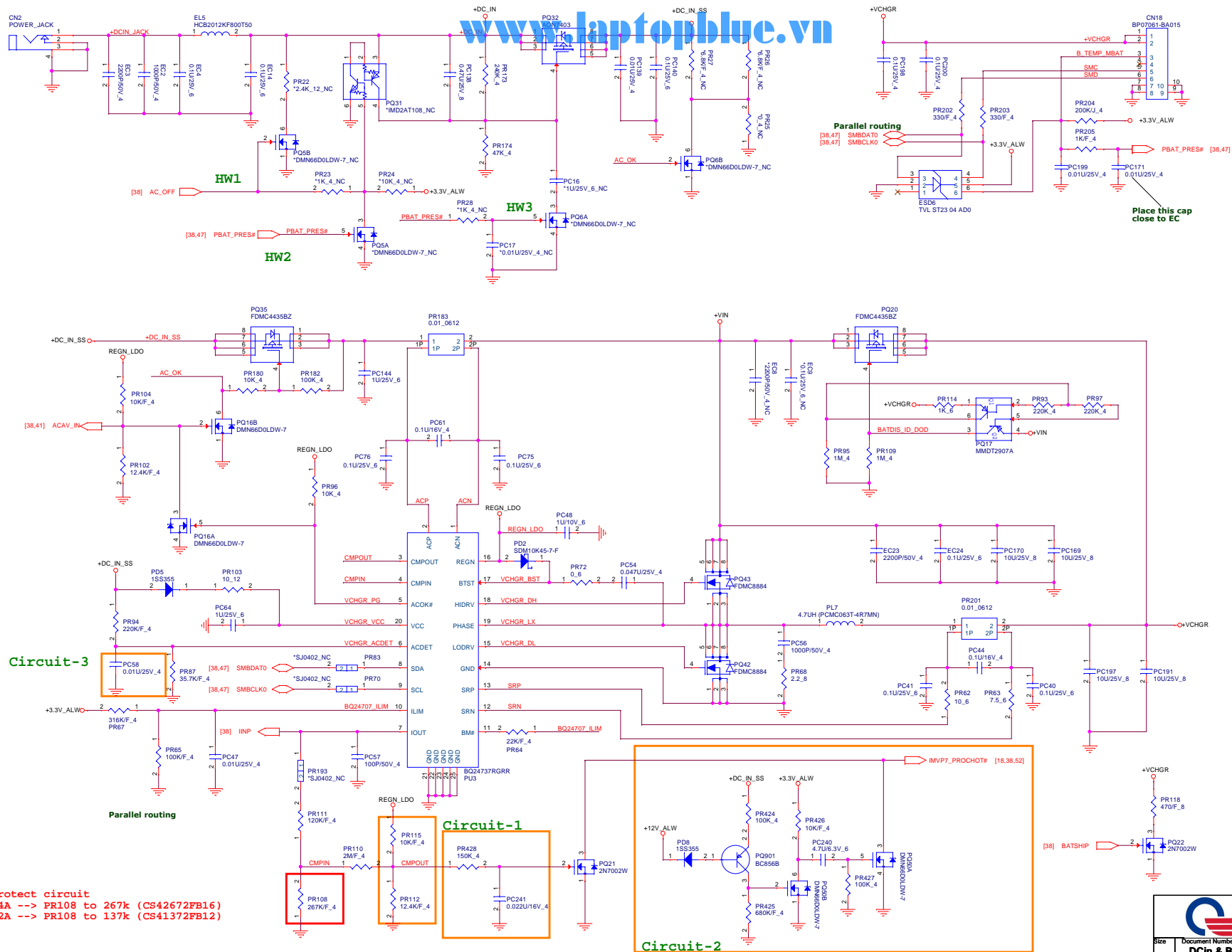
Quanta Computer Inc.

PROJECT : JW8B

System Reset Circuit

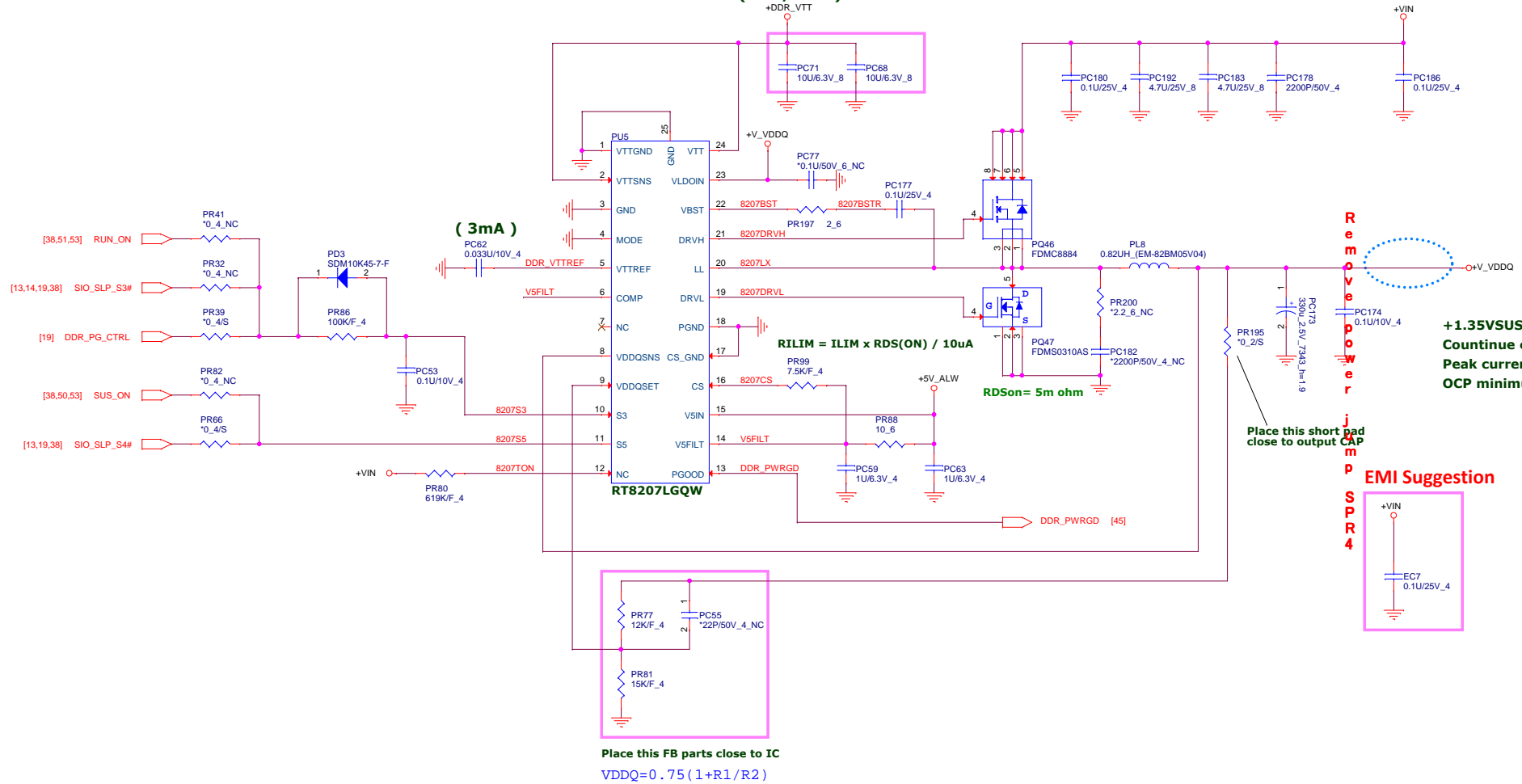
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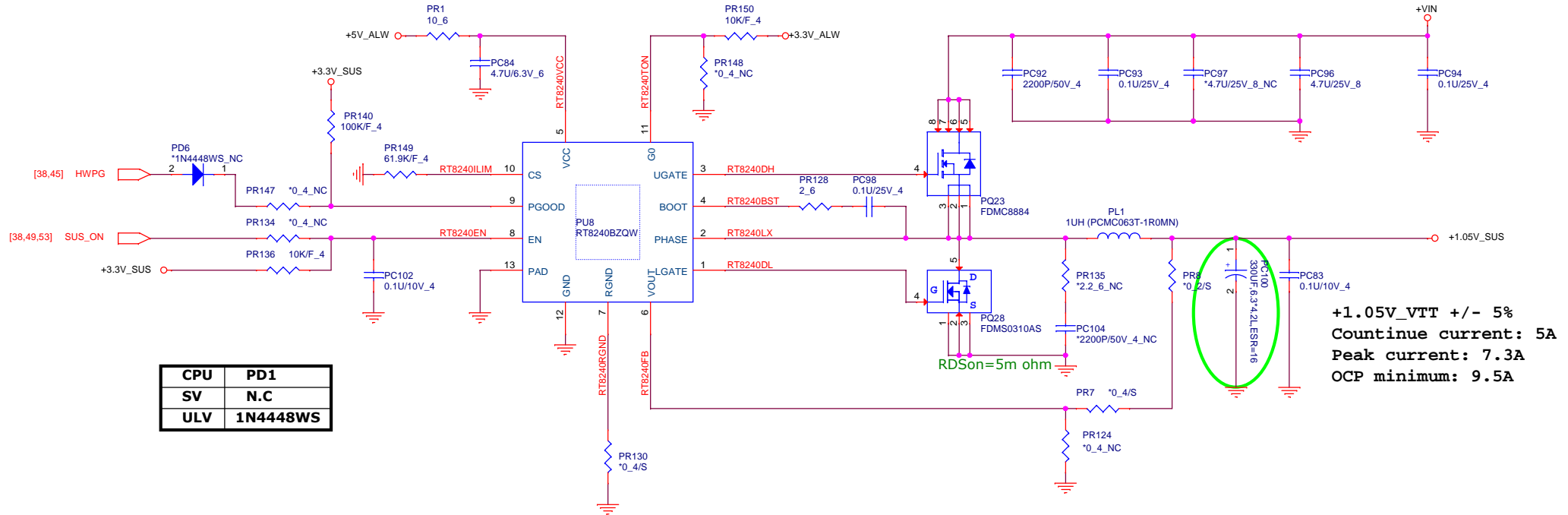




Adaptor protect circuit
65W - 4.34A --> PR108 to 267k (CS42672FB16)
90W - 5.62A --> PR108 to 137k (CS41372FB12)

(VTT/1.5A)





CPU	PD1
SV	N.C
ULV	1N4448WS

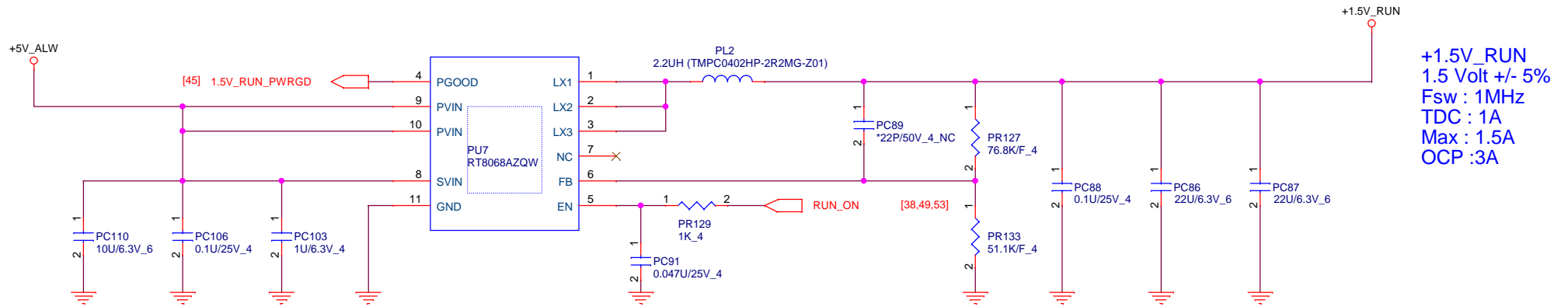


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Size	Document Number	Rev
	+1.05V_SUS (RT8240BZQW)	1A

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PROJECT : JW8B

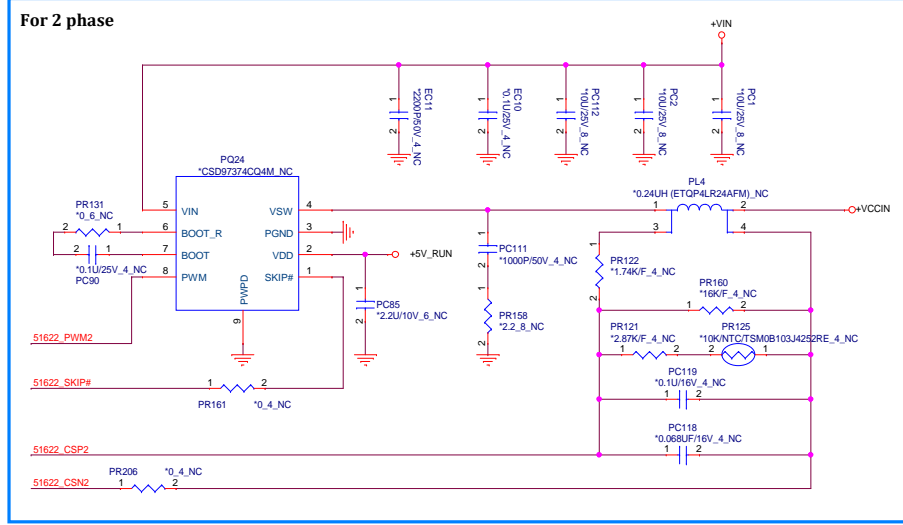
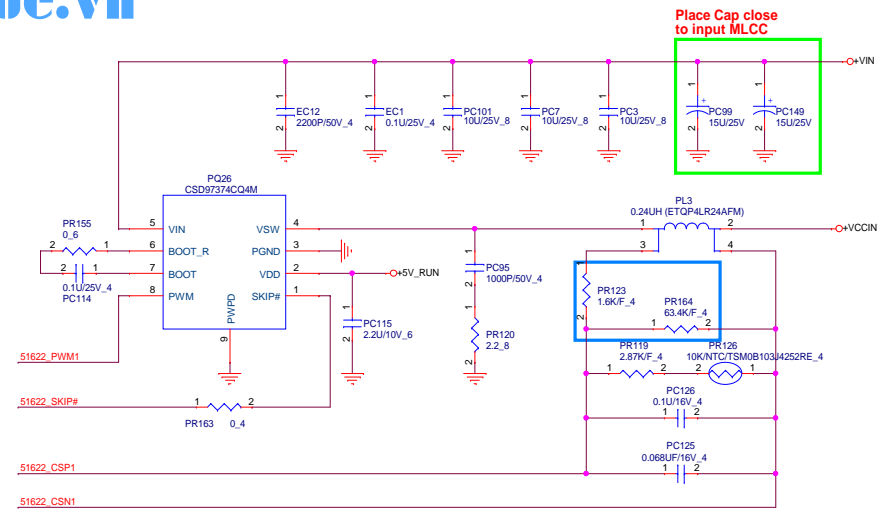
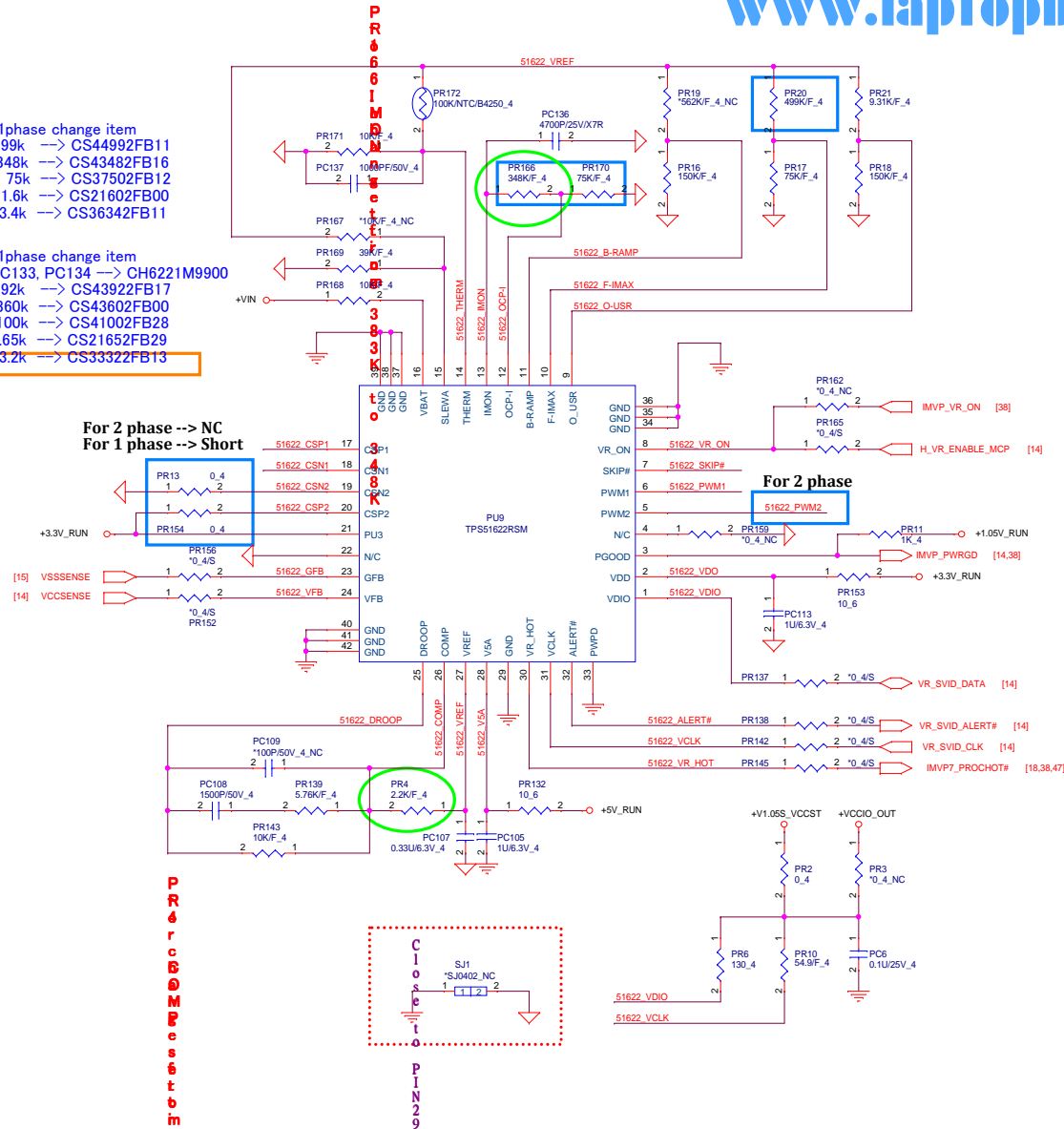
Size	Document Number	Rev
	+1.5V_RUN (RT8068AZQW)	1A

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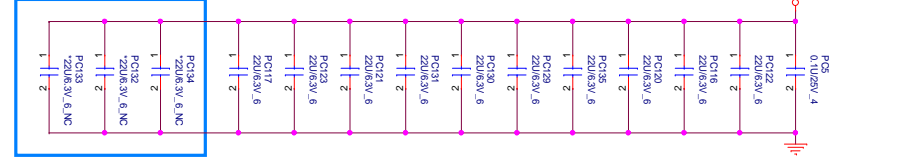
For 15W 1phase change item
 PR20 499k → CS44992FB11
 PR166 348k → CS43482FB16
 PR170 75k → CS37502FB12
 PR123 1.6k → CS21602FB00
 PR164 63.4k → CS36342FB11

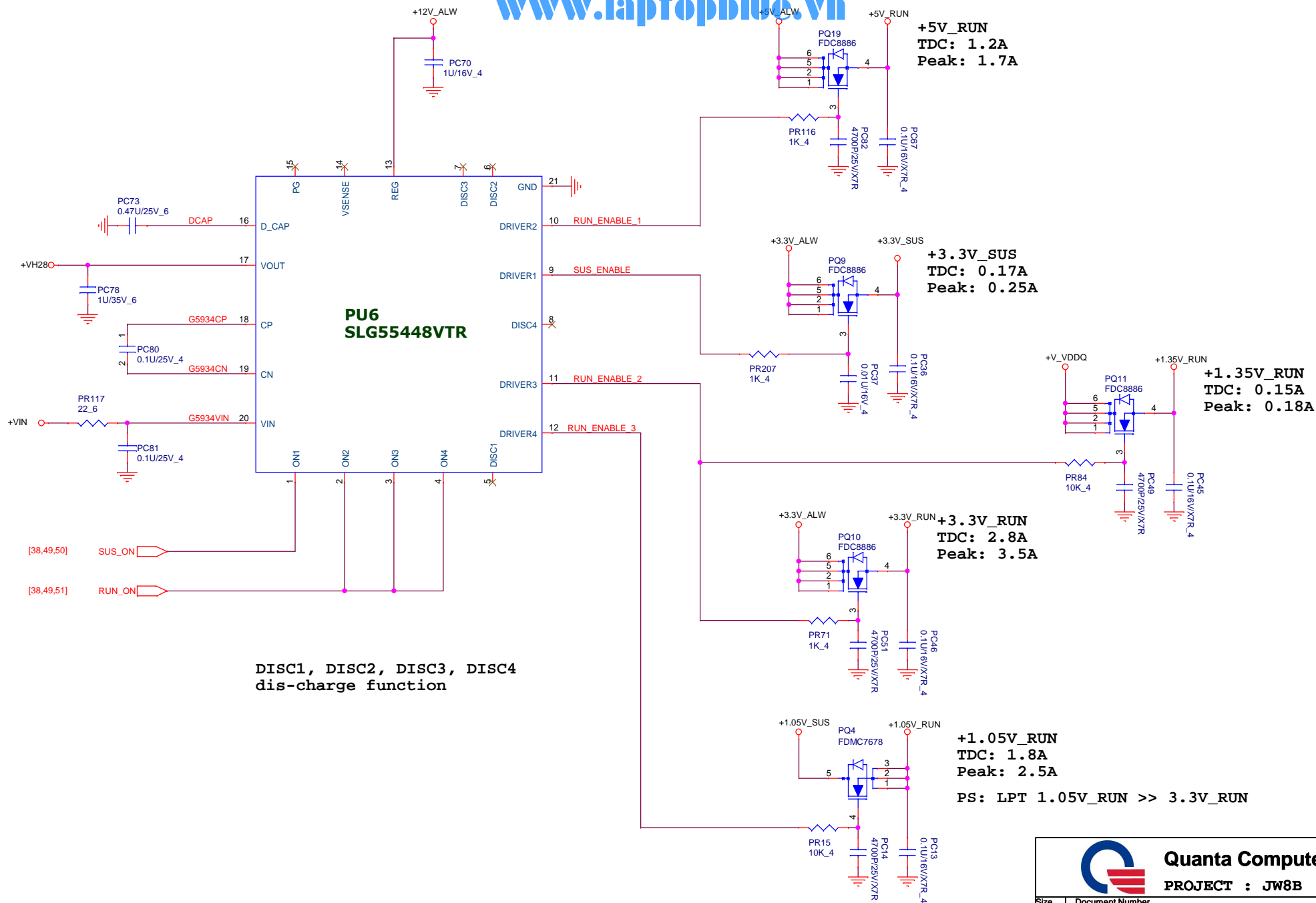
For 28W 1phase change item
 PC132, PC133, PC134 → CH6221M9900
 PR20 392k → CS43922FB17
 PR166 360k → CS43602FB00
 PR170 100k → CS41002FB28
 PR123 1.65k → CS21652FB29
 PR164 33.2k → CS33322FB13

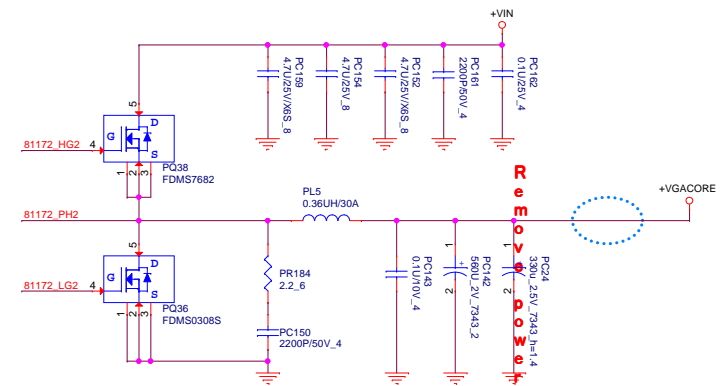
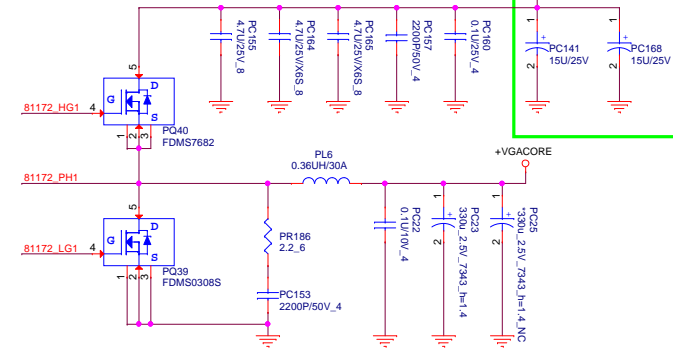
For 2 phase → NC
 For 1 phase → Short



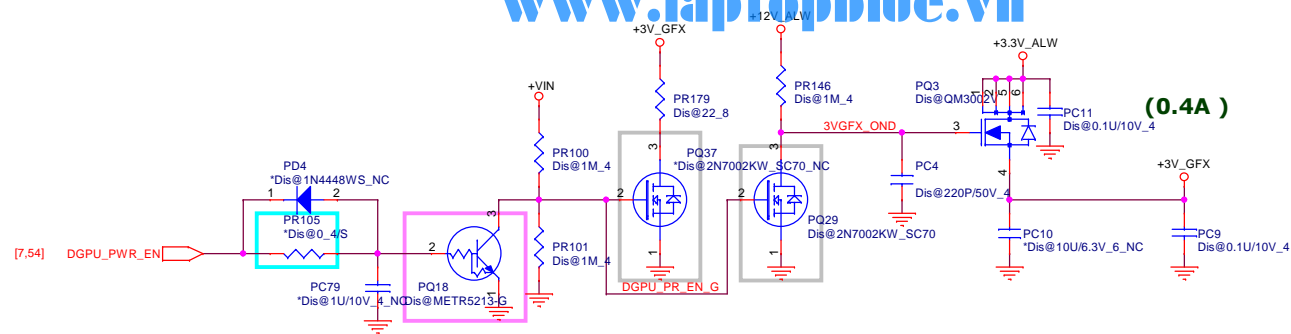
For ULT 28W





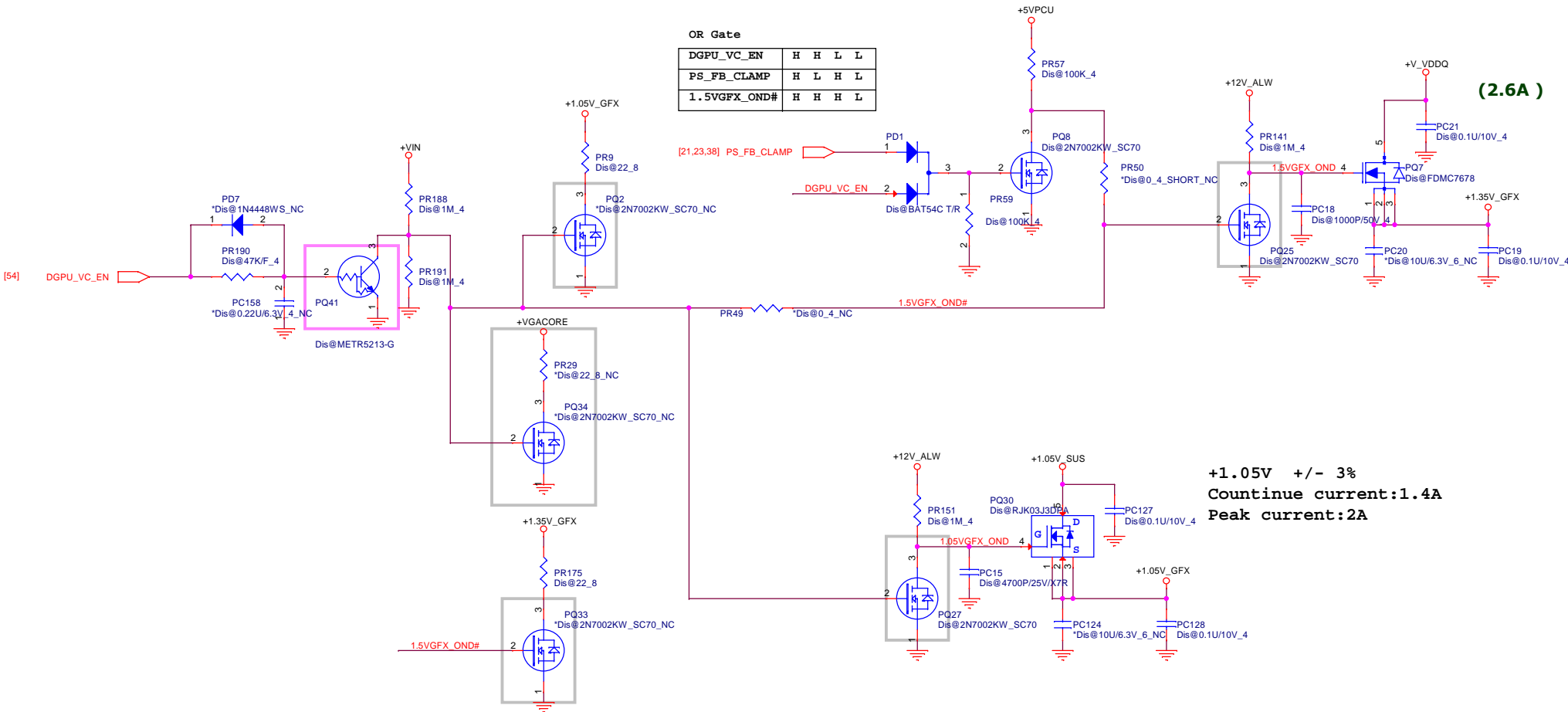


Remove power jump PR176



OR Gate

DGPU_VC_EN	H	H	L	L
PS_FB_CLAMP	H	L	H	L
1.5VGFX_OND#	H	H	H	L



+1.05V +/- 3%
Countinue current:1.4A
Peak current:2A



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